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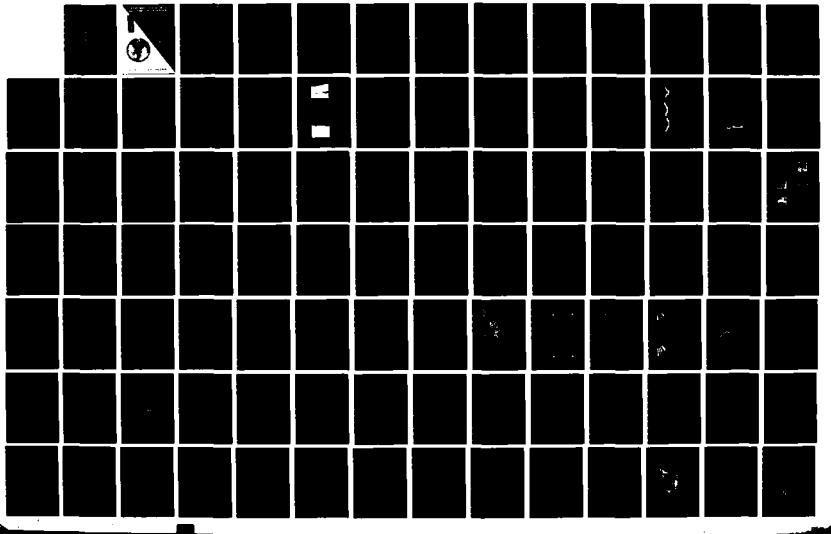

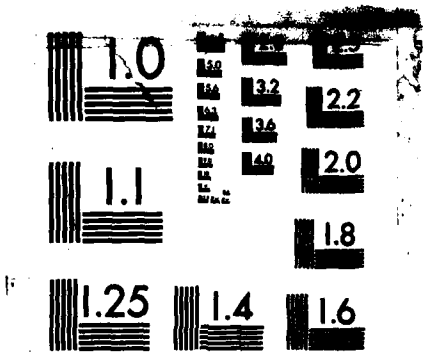

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ANNUAL REPORT

MARCH 1985

HIGH FREQUENCY SILICON BIPOLAR TRANSISTOR WITH SIPOS

HETEROJUNCTION EMITTER AND

ION IMPLANTED RAPID THERMAL ANNEALED BASE REGION

WORK SUPPORTED BY

OFFICE OF NAVAL RESEARCH
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HIGH FREQUENCY SILICON BIPOLAR TRANSISTOR WITH SIPOS HETEROJUNCTION EMITTER AND ION IMPLANTED RAPID THERMAL ANNEALED BASE REGION

Annual Report

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NORTH CAROLINA STATE UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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PREFACE

The work reported here was conducted under the direction of Mr. Max Yoder of the Office of Naval Research, Arlington, VA.

The North Carolina State University personnel are Drs. J. J. Wortman, J. R. Hauser, M. A. Littlejohn and G. A. Rozgonyi. Students are V. H. Ozguz, J. Liu, and T. Alford.

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1.0 Introduction

The research program described in this report is directed toward the investigation of concepts for improved high-frequency, high-speed, silicon bipolar transistors. The research is focused in three major areas: (1) deposition and characterization of semi-insulating polycrystalline silicon (SIPOS) as a heterojunction emitter, (2) use of ion implantation and rapid thermal annealing (RTA) for forming the base of bipolar transistors, (3) investigation of other technologies such as oxide isolation and polycrystalline silicon contacts to reduce parasitic effects to improve limitations at high frequencies. The research ranges from fundamental studies of structural, chemical, electrical, and optical properties of SIPOS deposited over a wide range of compositions on various substrates to the fabrication of transistors with polycrystalline and SIPOS emitters. Much effort has also been directed toward the ion implanted base where numerous techniques for forming the shallow implant and maintaining the profile during further processes were investigated.

A number of investigators have reported the use of polysilicon as an emitter material [1-3]. Their results have shown that significant improvements in gain are possible. Two theoretical models have been proposed to explain the higher gains: (1) tunneling through a thin oxide [4] which is attractive since a native oxide is generally present at the polysilicon-silicon interface due to the cleaning procedures, (2) a reduced mobility in the polysilicon which is part of a two region emitter of polysilicon and crystalline silicon [2]. A unified theory has also been proposed which would take into account current transport in the single crystal emitter, the thin oxide and the polycrystalline emitter [5,6].

2.0 Research Results

2.1 Review of program

This section contains a brief discussion of the work performed.

2.2 Semi-Insulating Polycrystalline Silicon (SIPOS)

2.2.1 SIPOS reactor

The reactor for the deposition of oxygen-doped-polycrystalline silicon (SIPOS) is a low pressure chemical vapor deposition system with a horizontal hot wall quartz tube. Silane and nitrous oxide are used as source gases and nitrogen is used as a purge gas. Table 2.1 is a summary of the system parameters. Oxygen content can be varied over a wide range by carefully controlling the reactant gases and deposition temperature. When parameters are closely controlled good reproducibility is obtained from run to run. The system provides good uniformity across the wafer and the boat. The furnace temperature has a ramp in order to provide uniformity across the boat.

2.2.2 Characteristics of SIPOS

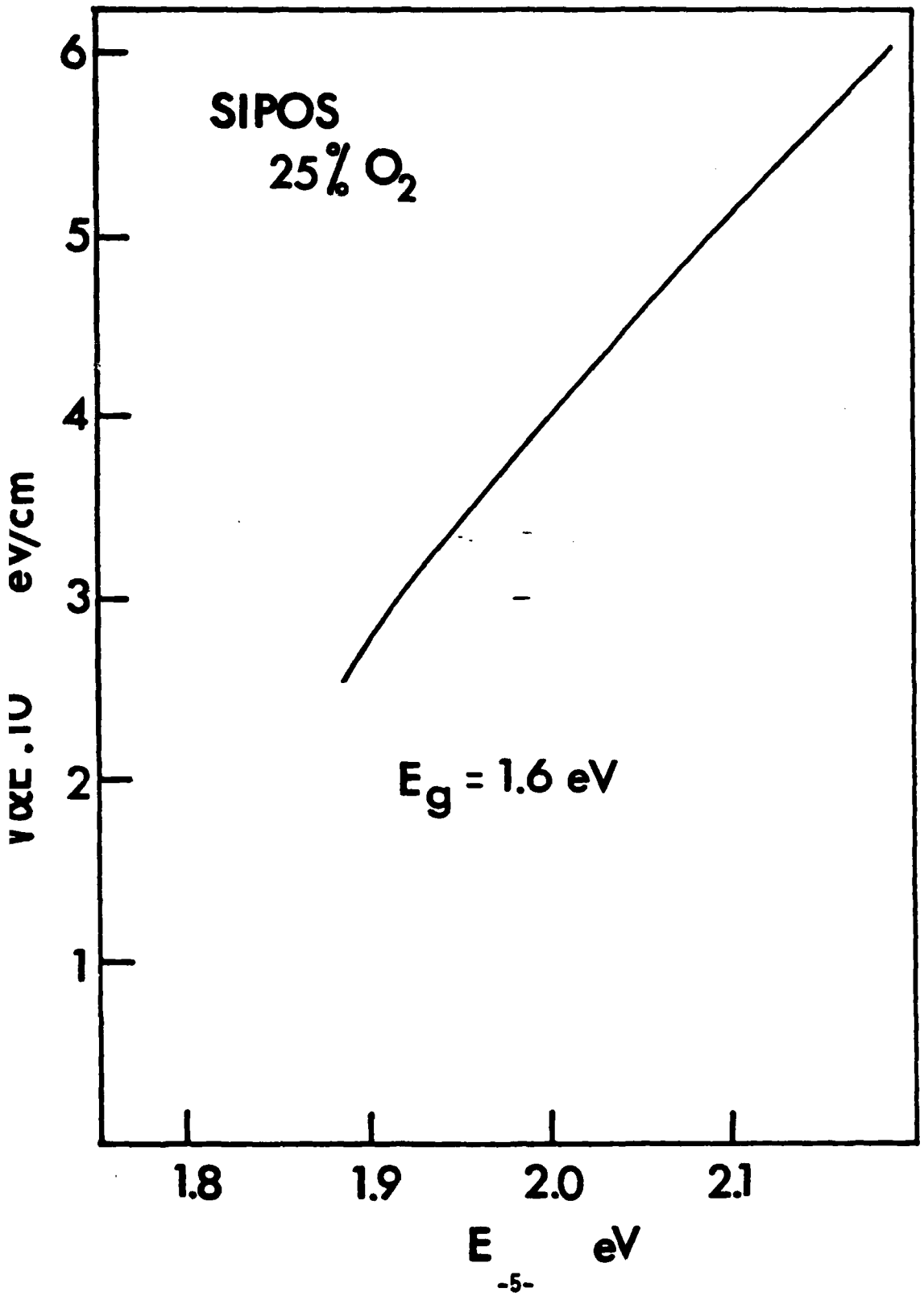
Electrical properties of SIPOS depend strongly on the oxygen content of the film, dopant concentration, anneal time, temperature and ambient. A wide variety of SIPOS films with different oxygen content, dopant ions, dopant concentrations and annealing schedules were deposited on Si crystals and SiO_2 and have been studied. Structural properties obtained from these experiments will be outlined in the next section.

Optical absorption of SIPOS films of different oxygen concentrations were investigated. The results obtained are similar to the results described in the literature [7]. Optical bandgap information can be extracted from a plot of the square root of absorption coefficient and beam energy product vs. beam energy (Fig. 1). This method of extracting the bandgap is used for

Table 2.1 SIPOS Deposition Data

H_4 ow 'min)	N_2O flow (cc/min)	Reaction Tube Pressure (mTorr)	Reaction Tube Temperature (°C)	Deposition Rate A/min) center wafer	N_2O/SiH_4 flow ratio	Value x for SiO(x
).0	0.0	153	614°C	86.3	0	-
).0	3.2	151	614°C	58.1	0.053	0.04
).0	6.7	152	614°C	40.4	0.112	0.08
).0	15.0	161	614°C	17.0	0.250	0.19
0.0	15.0	160	614°C	23.5	0.250	-
0.0	15.0	175	650°C	47.6	0.250	0.6C
0.0	15.0	180	675°C	59.6	0.250	0.6C
0.0	15.0	181	675°C	55.2	0.250	0.62
0.00	15.0	163	614°C	18.4	0.250	0.19

Figure 1. Optical absorption of 25% O_2 SIPOS films.



polycrystalline and amorphous materials and yielded a bandgap of 1.6 eV when used for a SIPOS film with 25% O_2; this value supports results reported earlier in the literature [9] and can also be supported theoretically [8]. This bandgap of SIPOS suggests the possibility of its use as a heterojunction material for the emitter in a silicon bipolar transistor structure.

In order to understand the transport phenomena in impurity doped SIPOS films, which are candidates as emitter material, studies have been made on electrical characterization of various films. Preliminary results are presented in Appendix I. Arsenic, boron and phosphorous ions have all been studied. Implant energies were chosen to insure the same impurity profile in each case. Films of 2500A SIPOS with different O_2 concentration were deposited on SiO_2. Different annealing schemes were studied which include rapid thermal annealing or furnace annealing to activate implanted ions and low temperature forming gas annealing to anneal interface states. Results are shown in Figures 2 through 6. These measurements show that boron is a much more effective dopant in SIPOS; it is easier to activate and it is not greatly affected by different annealing conditions. Arsenic is not as effective as B and results in a large resistance and a strong dependency on annealing conditions. Sheet resistances were found to be a function of oxygen concentration and ion implant doses. A high temperature anneal before implant (preannealing) followed by implant and another anneal to activate the dopant yields lower resistances [Fig. 5 and 6]. In some cases two orders of magnitude reduction in resistance is observed compared to the non-preannealed films. Forming gas annealing helps also in reducing the resistance. An order of magnitude reduction is possible for high oxygen content films. We also found that the use of rapid thermal annealing (RTA) was a good alternative to furnace annealing. As can be seen from Fig. 2 or Fig. 5, RTA gives the same

esults as furnace annealing if a temperature of approximately 100°C higher is used. It should be noted that RTA temperatures were measured by placing a thermocouple near by the sample. The actual temperature of the SIPOS may be higher than that indicated on the thermocouple. The short times (10-20s) used in RTA even though the higher temperatures are used, do not result in as much dopant diffusion as conventional furnace anneals produce. Films annealed by RTA or furnace gave a uniform impurity distribution through the film when measured by secondary ion mass spectrometry (SIMS). We also checked the uniformity in oxygen concentration during high temperature steps (especially preannealing) by SIMS and found them to be uniform.

I-V characteristics of resistors made by implanted SIPOS is linear and the resistors supported 2,000V/cm field strength without a problem. We also performed resistance vs temperature measurements on these resistors. A typical variation of resistivity with temperature can be seen in Fig. 7. An activation energy of 0.074V was extracted for the low temperature region. This type of conduction with two different activation energies has also been observed by others for undoped SIPOS [9,10,11]. Similar characteristics but different activation energies have been reported for polysilicon [12] where a complex transport mechanism was proposed that combined thermionic emission,-thermionic field assisted emission and thermionic emission assisted by grain boundary scattering.

More work is underway in this area which uses the polysilicon model and new concepts for SIPOS. In terms of the temperature coefficient of resistance (TCR), SIPOS resistors give values which are approximately half of the values obtained from diffused resistors in the same operating conditions.

Figure 2. Effect of the annealing temperature on the sheet resistance of implanted SIPOS

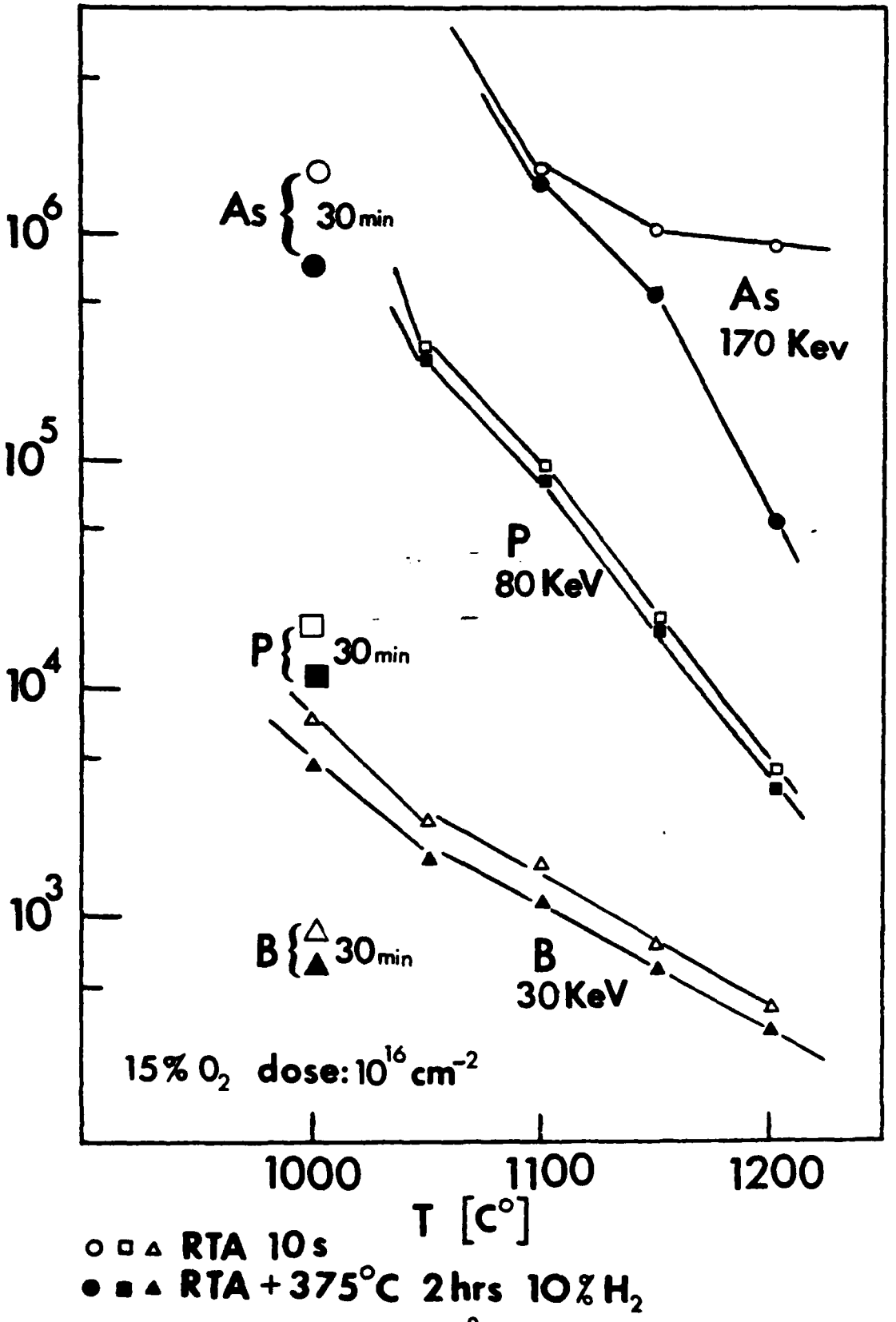
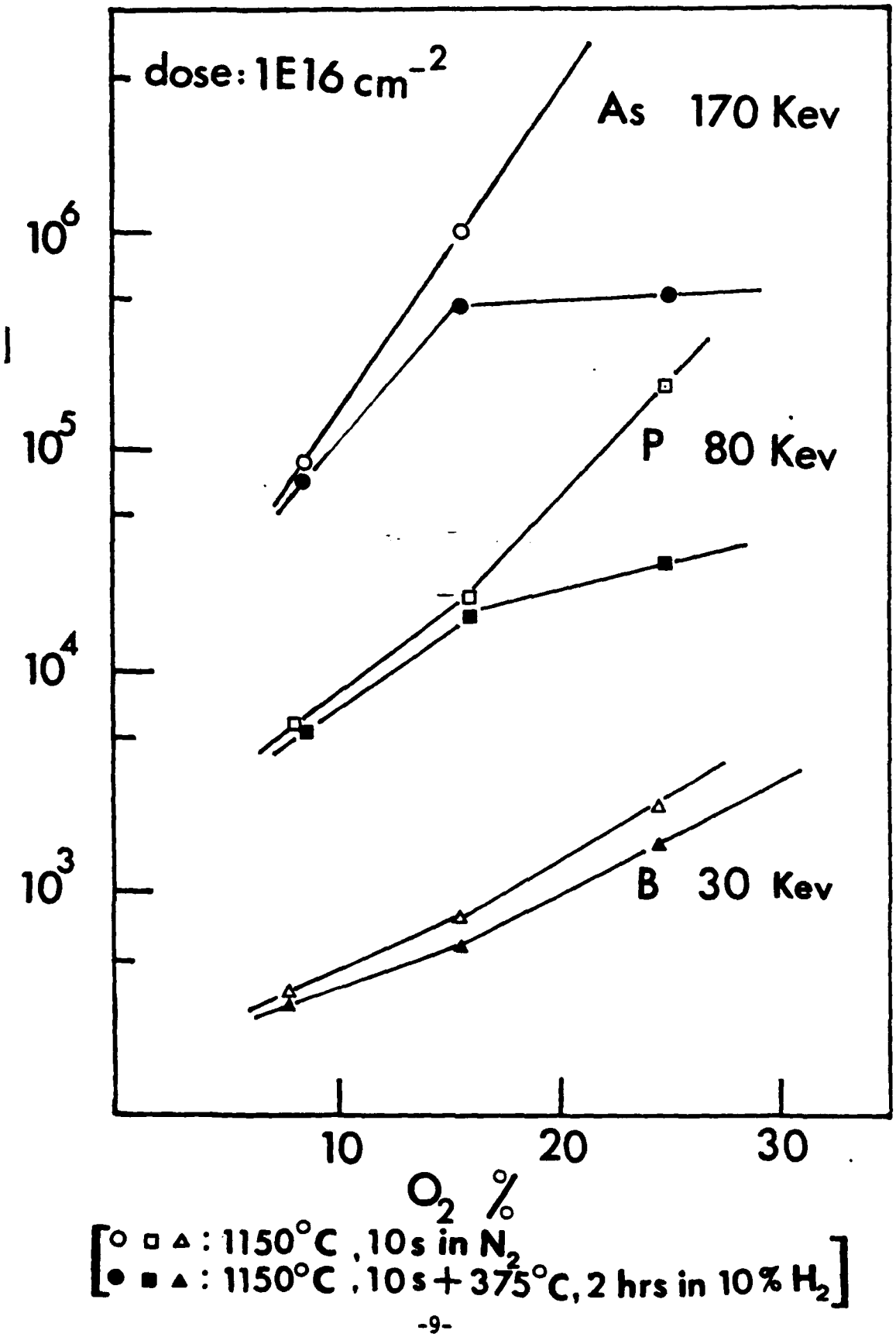


Figure 3. Effect of the oxygen concentration on the sheet resistance of implanted SIPOS



ain fabrication steps of this process are shown in Figure 11. Several runs ave been done with varied process parameters.

To obtain a shallow base, both B and BF_2 implants were studied. ransistors with 25 KeV B and 50 KeV BF_2 implants were fabricated, base mplant doses ranging from 1E13cm^{-2} to 5E14cm^{-2}. Preamorphization with Ge and ;i was also investigated although not included in the transistor process to late. Rapid thermal annealing has been successfully used to insure a minimum change in the implant profile during activation resulting in device quality junctions. Details in this area are discussed in Section 2.3.

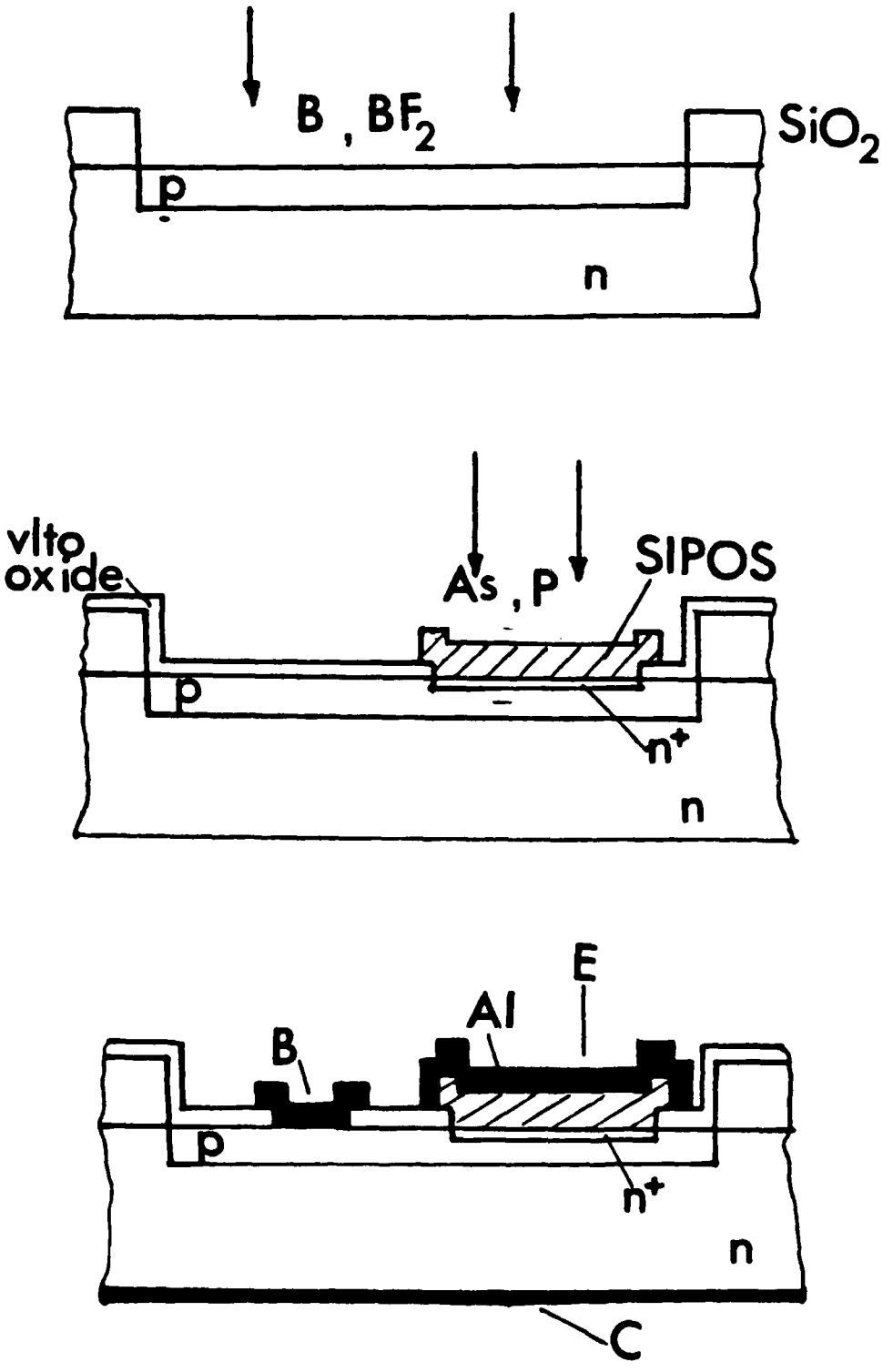
The effect of oxygen content in SIPOS on device performance was evaluated. SIPOS with O_2 content in the range of 10% to 25% was used as an emitter material. A control wafer with a polysilicon emitter was added to each run in order to provide a control.

Arsenic and phosphorous have been implanted into SIPOS to dope the emitter. Since RTA was used, the usual problem of fast diffusion of phosphorous was eliminated.

Different emitter structures were considered. SIPOS emitters of 250nm, SIPOS/Poly emitters (100 nm SIPOS + 150nm Poly) and poly/SIPOS/poly emitter (50nm poly + 100nm SIPOS + 100nm poly) were investigated. The best structure was found to be the SIPOS/poly emitter.

The use of different interface preparation techniques before emitter deposition was investigated. RCA cleaning [NH_4OH:H_2O_2: DI 1:1:5, 75°C 5min + HF dip + HCl:H_2O_2: DI 1:1:5, 75°C 5 min], RCA cleaning followed by HF dip and a quick rinse dry scheme and choline + detergent cleaning were tried. The idea was to either leave or remove the chemical oxide at the interface.

Figure 11. Fabrication steps for simplified bipolar transistor process.



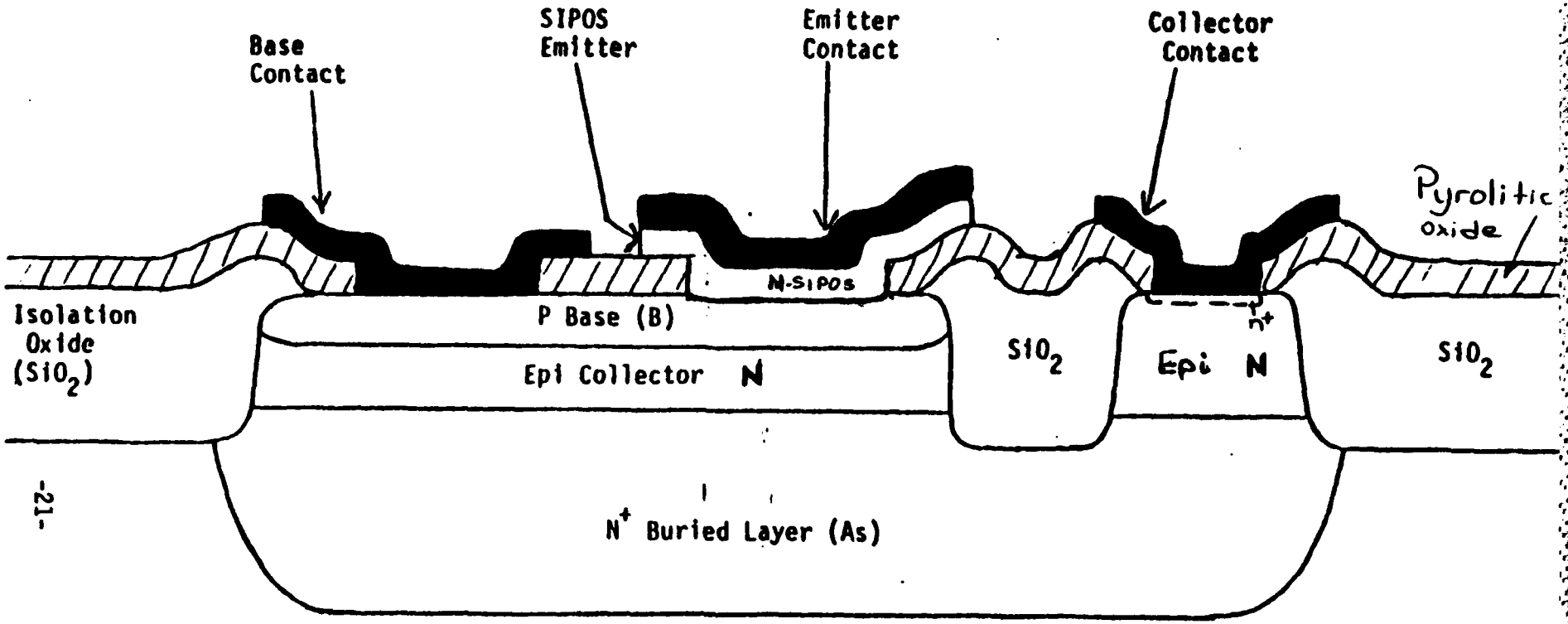


Figure 10. Schematic Cross Section of Proposed SIPOS/Si Heterostructure Bipolar Transistor (HBT).

voltage charactistics if a pre-anneal of 550°C for 30 minutes is used prior to the high temperature anneal-for either a furnace or a RTA anneal. See Appendix VI and XII. In an un-amorphized sample, if a pre-anneal is used, the RTA temperature can be reduced to as low as 950°C for 10 sec. If the sample is pre-amorphized before the B implant the dopants will be in the substitutional sites upon regrowth of the crystal. A 550°C anneal for 30 minutes will regrow the crystal. The only RTA needed is then to remove the damage.

Shallow p-n junctions were made using both B and BF_2 and it was found consistently that the diodes formed with BF_2 were of poor quality compared to those formed with B. Analysis of the samples which used BF_2 showed that it is very difficult to remove the F. It quickly moves to and is trapped at the extended defect location. High temperature anneals are required to remove the F from the sample. Also, it was found that a defect layer is formed at the surface of the sample if BF_2 is used while it does not show up when B is used. Thus, BF_2 should be avoided if possible.

2.4 Transistor structure

Since SIPOS has a bandgap which is larger than silicon, it can be used as an emitter material in a heterojunction bipolar transistor structure. This transistor is expected to have a high current gain with low base sheet resistance values. Also, it should have all of the advantages of polysilicon emitter transistors which are well suited for high frequency high speed operation. A transistor structure with a SIPOS emitter and oxide isolation is the c l for this part of the research work is shown in Figure 10.

2.4.1 Process development

In order to obtain key process parameters required to realize the transistors shown in Figure 10 and to address and answer all of the process oriented questions , a very simple bipolar transistor process was used. The

doped material where the B is implanted after pre-amorphization. See Appendix X. One belief is that the enhanced mobility may result from strain relief since Ge is larger than Si and B is smaller than Si. The net result may be that more than one B atom may be attracted to the Ge atom thereby reducing the impurity scattering. There are many implications to be drawn from this observation and the whole area needs further study.

Aside from the potential benefit of the Ge when used as a pre-amorphization ion it leaves behind, after the anneal, a layer of extended defects. The number of defects is dependent on the sharpness of the amorphous-crystalline interface. These defects can be removed but the temperature-time requirements are such that significant diffusion of the B takes place. One is left with the choice of putting these defects well below the shallow junction (to a place where an extended depletion layer would not extend) or very near the junction. The specific application may decide this choice. Another problem with Ge pre-amorphization is that, contrary to popular belief, Ge can form clusters when it is present at high levels in an amorphous layer which is later recrystallized [19]. Care must be taken to use only the dose of Ge needed to do the pre-amorphization.

Another problem with implanting Ge that must be avoided is to implant only Ge and not GeH or GeH_2. The common source of Ge for implanters is GeH_4. Since Ge has a number of isotopes it is easy to implant GeH as well as Ge unless Ge^{70} (the lowest mass isotope) is used. See Appendix XI. In summary, Ge is a viable candidate for preamorphization provided the proper energy, dose, and anneal cycle is used.

The anneal schedule to remove the radiation damage and to activate the dopant or to regrow the crystal and anneal out the damage is critical. In all cases it was found that significant improvements are possible in the current

would also yield low energy B ions upon impact. This problem was studied extensively -see Appendixes IV, V and VI. It was found that the profiles were somewhat reduced in depth, however, little or no amorphous layer formed to prevent channeling. Detailed studies revealed that higher RTA temperatures were needed to reduce the additional damage caused by the BF_2 ions. Diodes were formed using this technique and rapid thermal annealing, and the electrical properties were measured. Although the results were promising in that reasonably good electrical properties were found, the junction depths were still large for the base application.

Another way to reduce the junction depth is to pre-amorphize the surface of the sample with Si or Ge prior to the low energy B or BF_2 implantation. We have studied both techniques -see Appendices VII, VIII and IX. The studies show that Si pre-amorphization is not a good choice for two reasons. First, the Si surface does not completely amorphize unless the Si wafer is held at liquid nitrogen temperatures. This is a result of beam heating and the small mass of the Si ion. Second, implantation of molecular nitrogen occurs unless ^{29}Si ions are used. The latter is impractical due to source yield in the implanter. Unless the surface is completely amorphous there will be a high density of extended defects formed after annealing which are very difficult to anneal-out. For these reasons it is felt that Si is out of the question as a pre-amorphizing ion.

Germanium on the other hand holds more promise. Data shows that pre-amorphization can be accomplished with Ge ions even without a cooled substrate. The dose required ($\sim 2 \times 10^{14}/cm^2$) is also reduced almost an order of magnitude over that required for Si. The question must be raised as to the influence of the Ge on the devices to be fabricated. Data shows that Ge can result in an enhanced mobility (by a factor of up to 4 times normal) for B

dopant since there are no other viable p-type dopants. The npn structure was chosen because the best results have been obtained by other workers for polysilicon or SIPOS emitter devices using a npn structure [1-3, 13].

2.3.2 Boron Implant

Boron is a small atom relative to Si and hence is subject to significant channeling for low energy implant conditions. One of the problems is that B delivers too little energy density to cause the crystal surface to become amorphous. An other problem is that it is very easy for B ions to be diverted into channeling paths no matter what the orientation of the crystal. Both these problems are treated in Appendixes III and IV. The end result is that even with very low energy implants of B (~10Kev) and careful orientation of the wafer, the profile is a non-Gaussian distribution with a tail that goes to 0.2-0.3 μm after annealing. An additional practical problem is that most commercial implanters are not capable of the low energy implants without modification.

A variety of techniques to produce the shallow B profile were investigated. As a part of this phase of the work, rapid thermal annealing (RTA) was evaluated as a means to remove the radiation damage and to activate the dopants. Having studied the channeling problems and found then difficult to avoid, the next obvious approach was to use a molecular implant (BF_2) as an ion source. Then the energy is distributed according to the mass ratios between the B and F atoms and it turns out both the B and F are implanted to approximately the same depth. This happens eventhough the F atoms break off with more energy than the B atoms since they are larger, however, the range of both is approximately the same due to flourine greater stopping power. It was hoped that the BF_2 molecule would not only render the surface amorphous but

morphologies. Additional information to be gain should include: the degree of solid phase epitaxy of individual grains during annealing, doping distribution after annealing, and oxidation of films.

2.2.4 Summary

As explained above, a correlation exists between structural and electrical properties of SIPOS. Oxygen concentration determines the grain size and is a major factor which affects the resistivity of the films. Oxygen concentration is a function of deposition temperature and the reactant gases concentrations. With a proper selection of oxygen concentration, ion implanted species, doses and annealing conditions, a resistance range from a few hundred ohms to megaohms can be achieved. This makes possible the use of SIPOS resistors in applications where high value resistors are required. The potential application of SIPOS as an emitter material makes this choice more attractive.

2.3 Implanted Base

2.3.1 Problem

Another of the primary objectives of this work is to develop a procedure for the formation of a narrow base for the transistor using ion implantation and RTA This requires not only a very shallow implant, but, a follow-up anneal schedule to remove the radiation damage and to activate the dopant in a way which avoids significant diffusion of the dopants. Other process steps which follow also must not to cause big changes in dopant profiles. A npn bipolar transistor was chosen which by necessity requries that B be used as the base

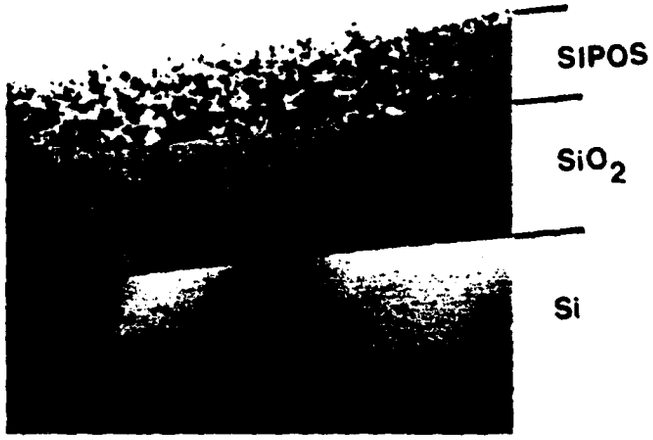


Figure 8. XTEM of a typical SIPOS film after RTA

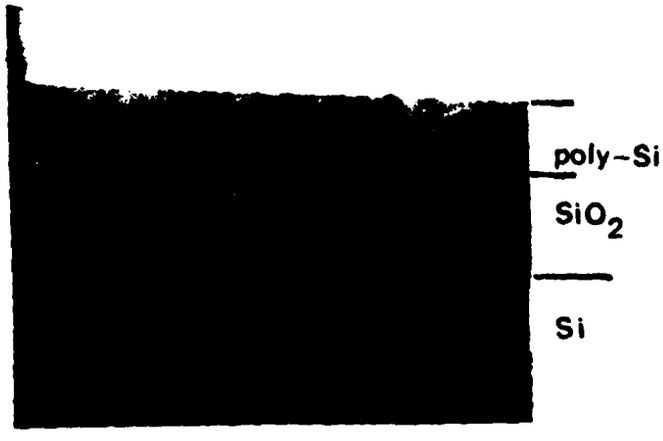


Figure 9. XTEM of a polysilicon film after RTA

2.2.3 Structural properties of SIPOS

The characterization of SIPOS films have been initiated by way of cross section transmission electron microscopy (XTEM). This procedure is advantageous in the study of the grain size morphology and distribution. For more specific detail, refer to Appendix II.

Variables examined were oxygen content, ion implantation conditions, and annealing schemes as summarized in table 1 of Appendix II. The initial investigation revealed that each of the variables influenced the structure morphology. An RTA anneal following deposition and implantation of SIPOS films on silicon oxide film produces a fine equiaxial grain morphology (Fig. 8). This structure differs from the columnar grain of RTA poly-silicon (Fig. 9). The actual grain size decreased with increasing oxygen content. The implanted samples produced a grain distribution that consisted of larger grain which appeared at the SIPOS-SiO_2 interface till the upper third of the SIPOS.

A sequence of first implantation and then RTA produced a finer grain size. Therefore, the initial information suggests that the impurity materials affect the grain nucleation and growth in conjunction with the particular RTA treatment. The analysis of SIPOS films shows that the larger grains the lower the sheet resistance. The larger grains are usually produced by lower oxygen content, and longer annealing time. SIPOS deposited over Si and over SiO_2 shows the same morphology for a given implant, oxygen content and RTA combination.

Microscopic studies will determine the randomness and distribution and orientation of the columnar grains which are found in SIPOS. The understanding of nucleation kinetics will be needed in producing specific grain

Figure 7. Variation of the implanted SIPOS resistance with temperature (R_{REF} at 280°C)

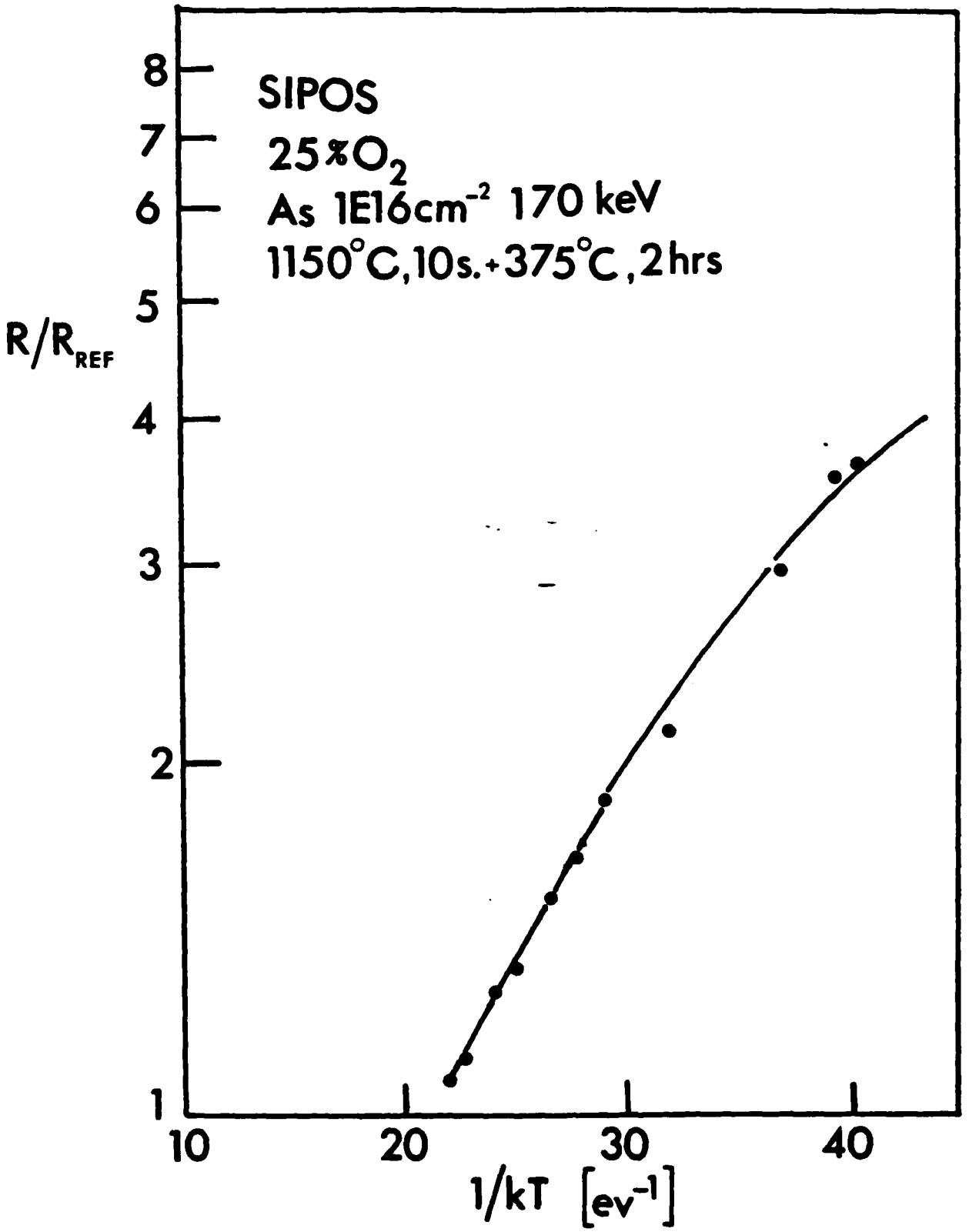


Figure 6. Effect of the preannealing on the sheet resistance of implanted SIPOS cases of $^{11}B^{+}$ and $^{30}P^{+}$; dose: 1E16cm^{-2}.

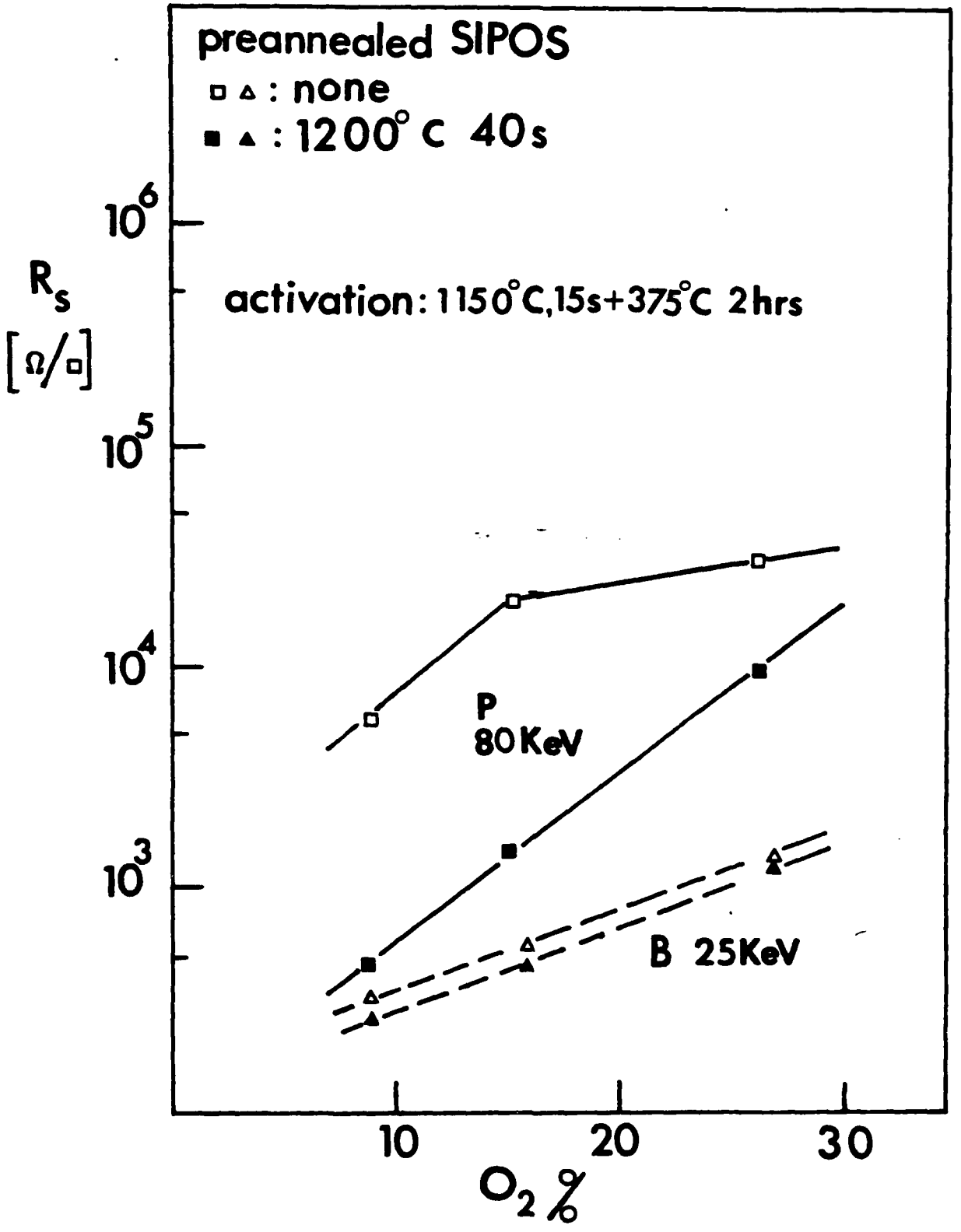


Figure 5. Effect of the preannealing before implant on the sheet resistance of implanted SIPOS; the case of $^{75}As^{+}$

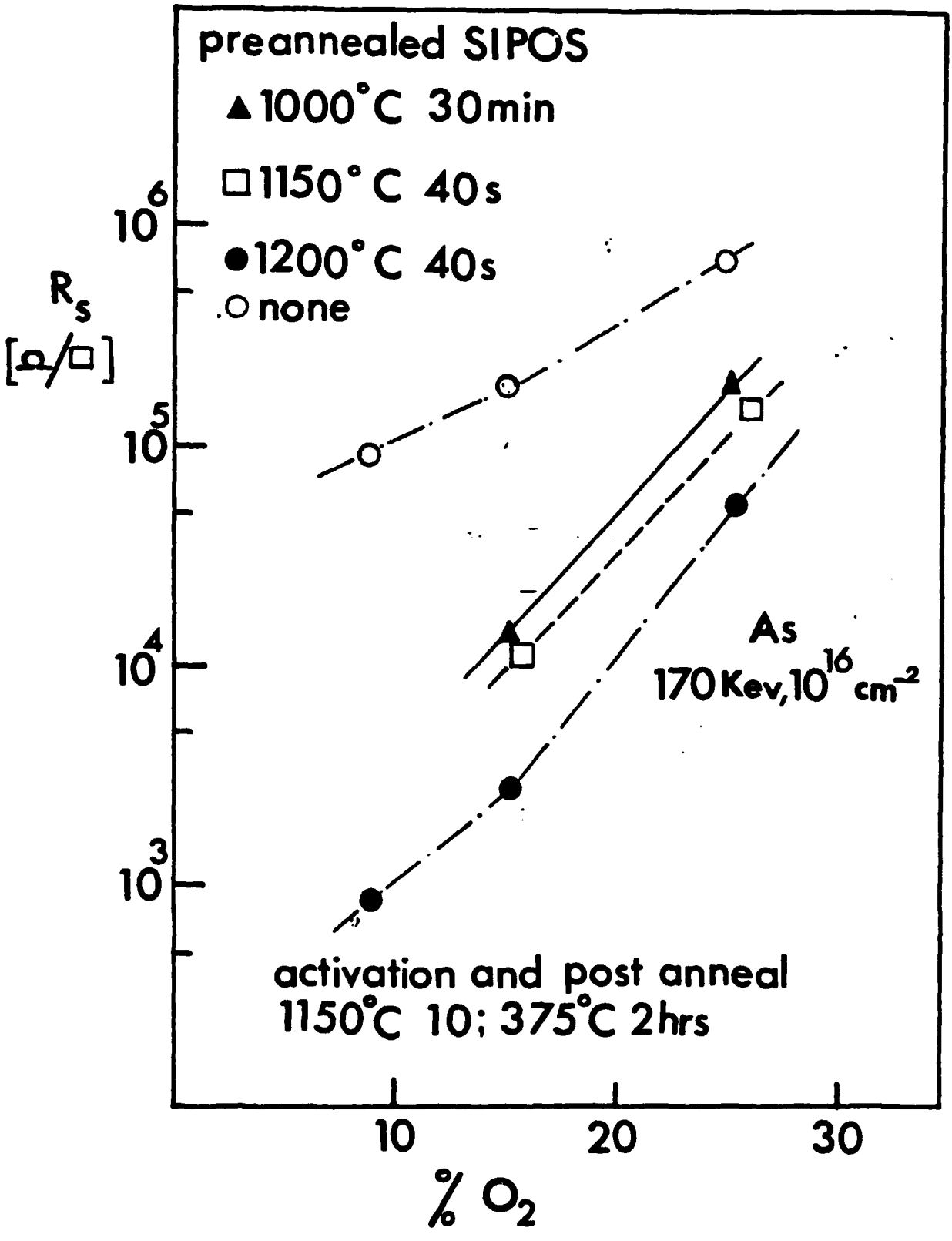
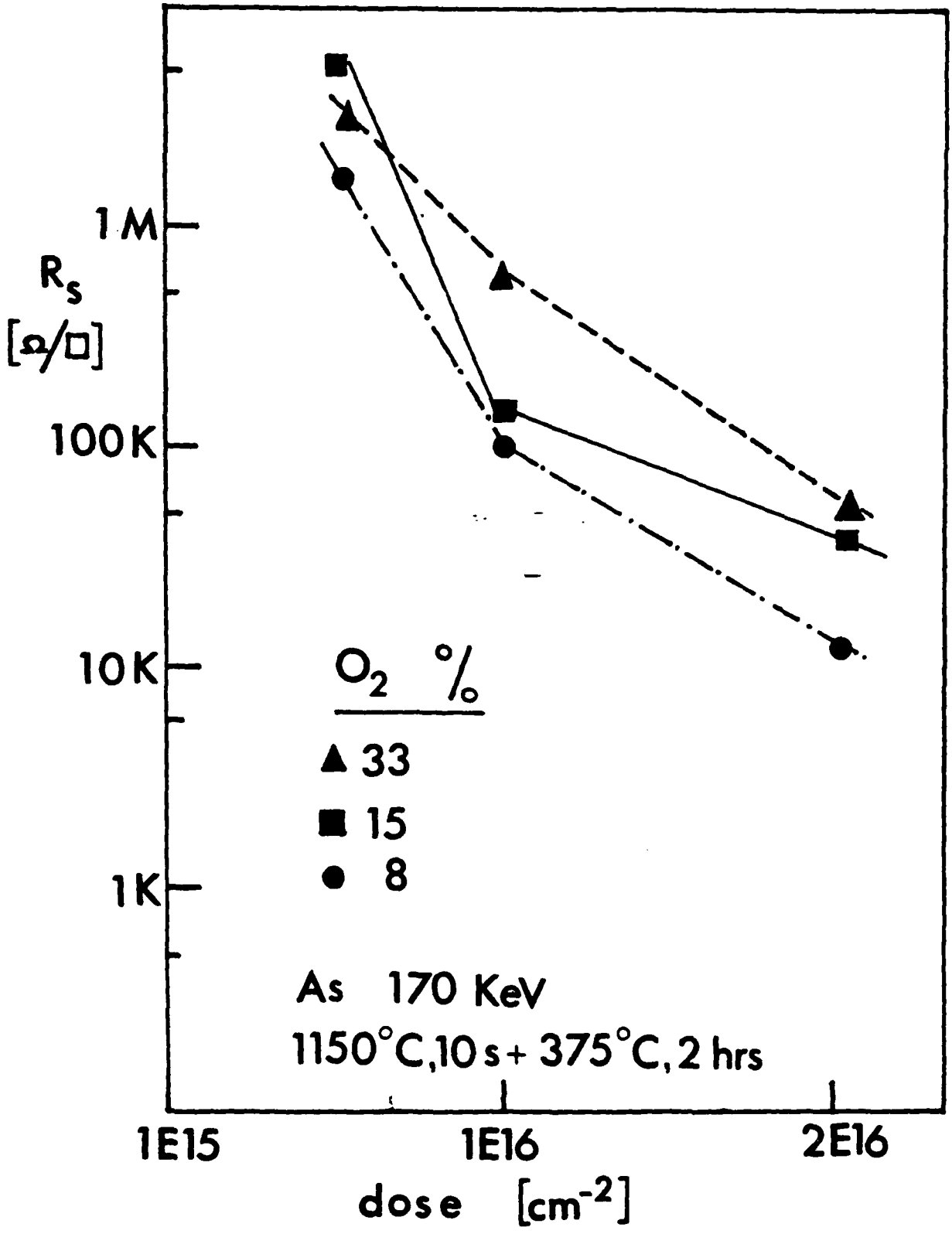


Figure 4. Variation of the SIPOS sheet resistance with ion implantation dose.



An investigation of activation annealing was done in which furnace annealing (1000°C -30 min) and RTA were studied. Since SIPOS requires high temperatures for activation, RTA temperatures used were 1100°C and 1150°C for times of 10 to 20 seconds.

The use of plasma etching of SIPOS was studied. Plasma etching was used to define the SIPOS or poly-Si patterns. A mixture of Freon 14 (10.8%) Freon 13 (2.7%) and oxygen (3.4%) was used at a power level of 175W and a pressure of 3.6 Torr. Worst case selectivity of 4:1 was obtained. The following etch rates were found:

N_2O/SiH_4 ratio during deposition	etch rate [A/sec]
0 (Poly)	120
0.053	92
0.112	70
0.25	30
SiO_2 (VLTO deposited)	10

The results of the above experiments are now summarized. Current gains obtained were up 65. The best figure of merit [$h_{FE}/R_{B\ K\Omega}{}^{-1}$] obtained was 50 for a polysilicon transistor (h_{FE} = 65 R_B = 1.3K) and 40 for a SIPOS transistor (h_{FE} = 10, R_B = 0.25K).

A typical transistor output is shown in Fig. 12. Breakdown voltages of 60V were obtained for 1Ωcm n-type 100 substrates. The current gain, base resistance and breakdown voltage distributions across the wafer were good.

The low gains and other problems are attributed primarily to problems inherent in the simple geometry used to demonstrate the transistors. The lack of an epitaxial layer results in two disadvantages: large collector resistance and large collector area due to the vertical transistor structure. Large leakage currents were caused by the large geometries. A very simple mask

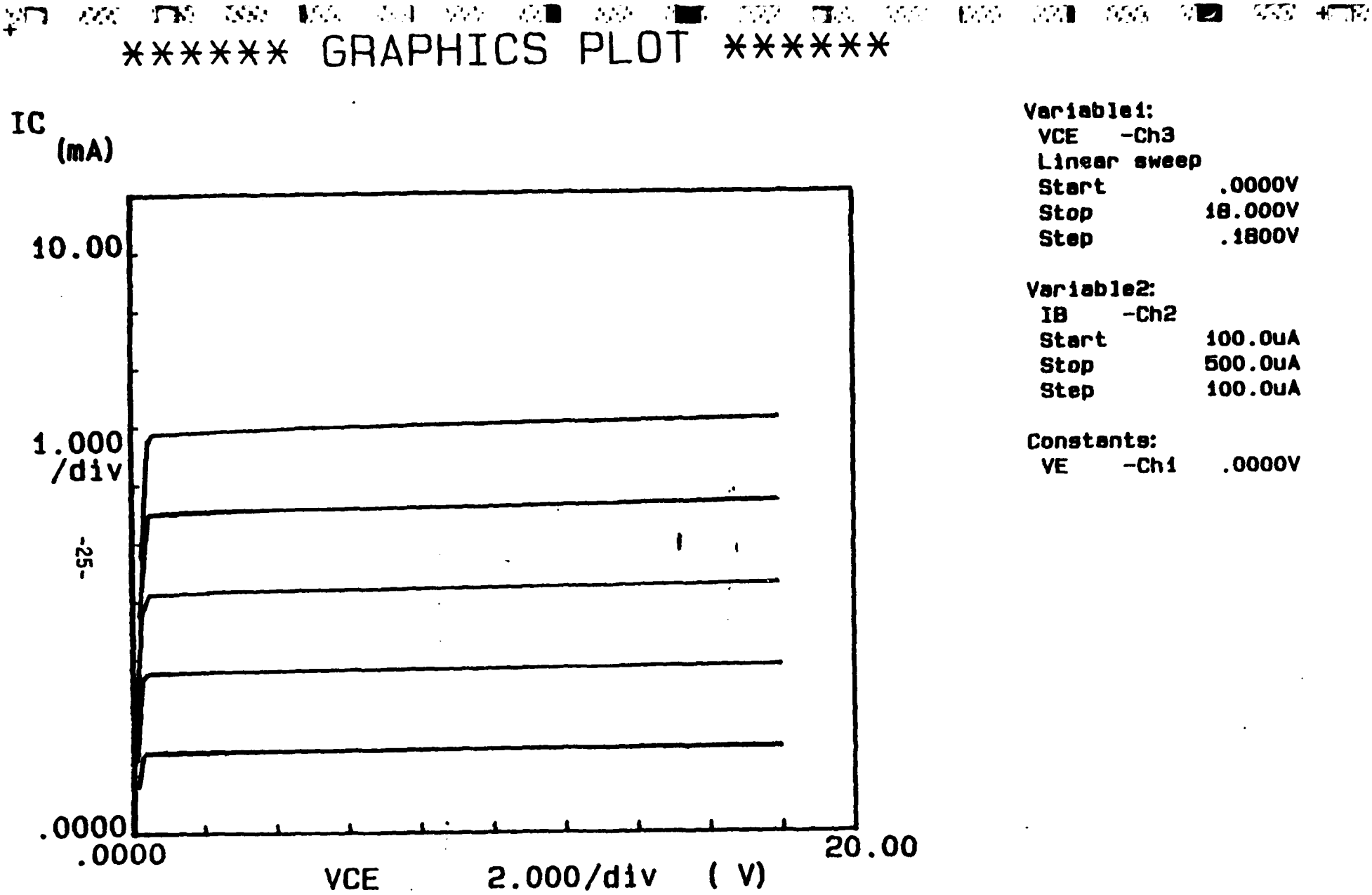
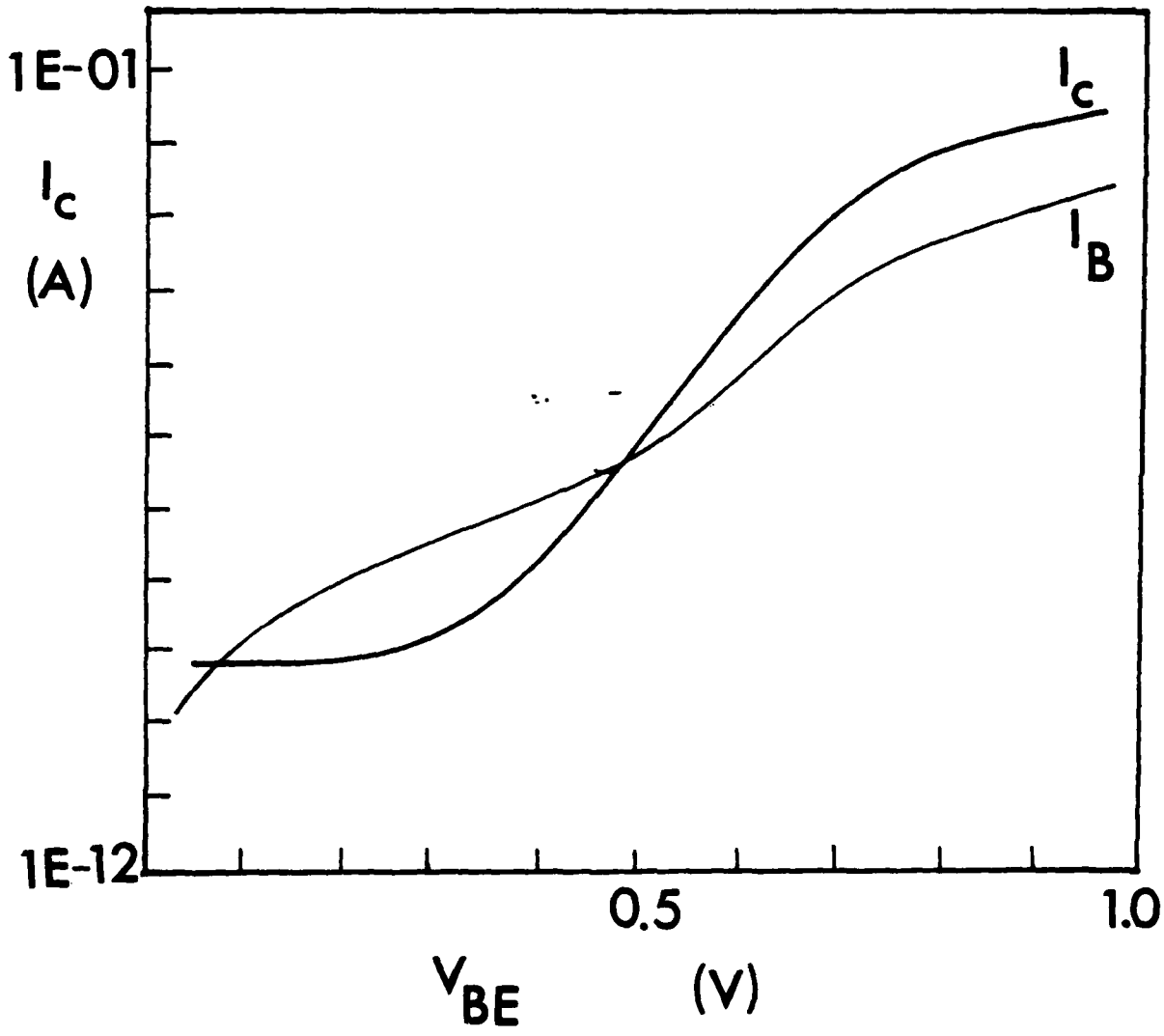


Figure 12. Output characteristics of a typical SIPOS emitter transistor. (25% O_2 SIPOS emitter, 1E16cm^{-2}, 180 KeV As$^+$ implanted; R_B = 0.8 K).

FIGURE 13. I_B, I_C, vs V_{BE} characteristics of a typical SIPOS emitter transistor.



set was used for these runs on which minimum feature size was 50μm with a typical emitter area of 20000μm^2. The relatively high emitter resistance of the SIPOS emitter added to these disadvantages. Thus, at lower current levels active device operation was limited by leakage currents while junction turn-on was increased due to high emitter resistance, and at higher current levels device operation was impeded by high collector and emitter resistances. A plot of collector and base currents vs. base-emitter voltage shows these effects very clearly (Figure 13).

Further studies on transistor structures using SIMS have shown that no n^+ crystalline region was formed by diffusion of As or P from the emitter into substrate. It has been reported that when no crystalline emitter region is formed in SIPOS transistors the current gain is low [13]. Polysilicon emitter transistors are not susceptible to the formation of this region [14,15]. This explains the higher current gain in the polysilicon transistors fabricated. Furthermore, it is believed that hydrogenation done at 375°C for 2 hrs. in 10% H_2 -90% N_2 was not completely effective for annealing interface states.

2.4.2 New designs

In order to avoid design related problems described above a new mask set and a revised process were designed. The new mask set provides:

- minimum feature size of 2.5μm,
- transistors with emitters 2.5μm x 5μm and 5μm x 10μm, different diodes, emitter and resistor sheet resistance structures, base, emitter and collector contact resistance structures, ring oscillators and TTL gates.
- mask levels for buried layers, isolation, N^+ collectors implant, resistor shielding, cross over insulation in addition to standard levels.

A process compatible with this set and which includes oxide isolation, epitaxial collectors is being developed. Meanwhile, a modified version of the simple process with a planar non-isolated transistor structure is being used.

2.4.3 Summary

Although not completely successful, the feasibility of SIPOS emitter transistors with ion implanted SIPOS and rapid thermal annealing was demonstrated. A baseline process for fabrication of simple bipolar transistors was developed and much knowledge on process related problems was obtained.

3.0 Future work

Future research work is being focused in the following areas:

- Conduction mechanisms in SIPOS: more work is needed to investigate the effectiveness of boron in SIPOS; p and n type carrier transport should be experimentally studied in terms of mobility, barriers for transport and activation energies. High frequency behavior of SIPOS conduction needs to be investigated since SIPOS is a candidate for high-frequency devices. A theoretical model is needed to support the experimental work.

- SIPOS junctions: in order to better understand the heterojunction properties of SIPOS, different types (p and n) of SIPOS-silicon, SIPOS-polysilicon and SIPOS-SIPOS junctions need to be studied in terms of I-V and C-V characteristics including temperature and frequency dependences. Effects of process parameters such as low temperature annealing must be included in this study. Hydrogenation by ion implantation is a promising technique to control the amount of H_2 in the film.

- A theoretical model: a good model is needed for SIPOS heterojunction transistors. Previous models for poly-si can not be applied to SIPOS due to smaller grain size of SIPOS and the existence of O_2 in the film. Indeed the

proof of the independence of current gain of polysilicon emitter transistors from the formation of n^+ crystalline regions is significant [14]. The existence of this n^+ crystalline region appears to be required for good SIPOS transistor performance amd indicates that the transport mechanism and the phenomena which increases efficiency at the base-emitter junction may be different for polysilicon and SIPOS transistors. Heterojunction theory is not mature yet and there is still discussion about the basics of the theory [16,17]. This area needs more work from the fundamental theory to its application to SIPOS transistors. Empirical models can be used for the time being for engineering purposes.

- Since it has been shown that preannealing changes structural and electrical properties of SIPOS, this must be incorporated into the device process. However, due to the high temperatures required for pre-annealing, all of the junction formation should be done after preannealing. This may call for a self-aligned process which in itself is attractive for high frequency purposes. This process appears feasible [3,15], however, the base contact formation poses particular problems. SIPOS can be selectively implanted and its insulating properties seem suitable for process purposes. Process development is needed to investigate the realization of self-aligned SIPOS transistors.

- The use of Ge pre-amorphization for the formation of the shallow base needs to be fully demonstrated. Particular emphasis should be on choosing the best Ge dose and energy with respect to the electrical properties of the transistor.

- New structures: superlattices of alternating thin (~100A) silicon and silicon dioxide layers or silicon nitride have been obtained [18]. A superlattice emitter may offer a new possibility, however, the technology to fabricate thin alternative layer of Si or SiO_2 needs further research effort.

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Appendix I

Conductivity of Ion Implanted and Rapid Thermal Annealed Semi-Insulating Poly-Silicon

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Conductivity of Ion Implanted and Rapid Thermal Annealed Semi-Insulating Poly-Silicon

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...i-insulating poly-silicon (SIPOS) ... with ion implantation and rapid ... annealing (RTA) has been investi... for use in integrated circuit fabri... In addition to its insulating and ...tion properties, doped SIPOS can be ...e a high resistance material for ...rs. The possibility of achieving ... functions simultaneously by proper ...nt of a single SIPOS film has been ...gated.

... films used in this study were deposi... 614°C in a low pressure hot wall ...t vapor deposition system. Silane ...trous oxide were used as reactant ... Oxygen content of the films was ... from 5 to 30 atomic percent. Oxygen ... is a function of the deposition ...ture and partial pressure of the re...gases. Arsenic, boron and phosphor...e implanted as dopants. SIPOS layers ... nm thick were deposited on 350 nm ... silicon dioxide.

...t resistance of SIPOS films were ...n be a strong function of oxygen con...purity doping concentration, anneal ...on and annealing environment. In ad... to RTA anneals in the range of 1000°C ...°C for 10 to 20 seconds, a variety of ...als before ion implantation and post ... in forming gas after RTA were investigated. When RTA was used to activate the dopants and to anneal the film, sheet resistance was found to reach a minimum at approximately 1100°C as shown in Figure 1. However if the films were post annealed at low temperatures (350°C - 450°C) in forming gas (10% H_2 - 90% N_2) for 1-2 hours, the sheet resistance was found to decrease approximately one order of magnitude as shown in Figure 1 and 2. No minimum sheet resistance was found for post annealed samples. Post annealing does not affect the sheet resistance unless the dopant atoms are activated as can be seen in Figure 1. Post annealing is also much more effective for high oxygen concentration (see Figure 2). The sheet resistance is a strong function of the dopant dose as shown in Figure 3. Figure 2 and 3 also show the effect of oxygen concentration on sheet resistance.

Preannealing at high temperatures (1000°C-1200°C) prior to ion implantation was investigated to study impurity redistribution. Both long anneals at high temperature as well as short anneals (RTA), were found to significantly lower the sheet resistance as shown in Figure 4. Preanneal temperature appears to be more important in reducing the sheet resistance than does anneal time. Structural analysis has shown that preannealed films have larger grain sizes. Detailed results of the structural analysis is included in an accompanying paper. Conduction of the doped SIPOS films was ohmic. Sheet resistances from 1kΩ/□ to 4MΩ/□ can be obtained by varying the oxygen concentration and dopant dose. In summary we believe that SIPOS coupled with ion implantation and RTA offers a material process which is suitable for integrated circuit fabrication.

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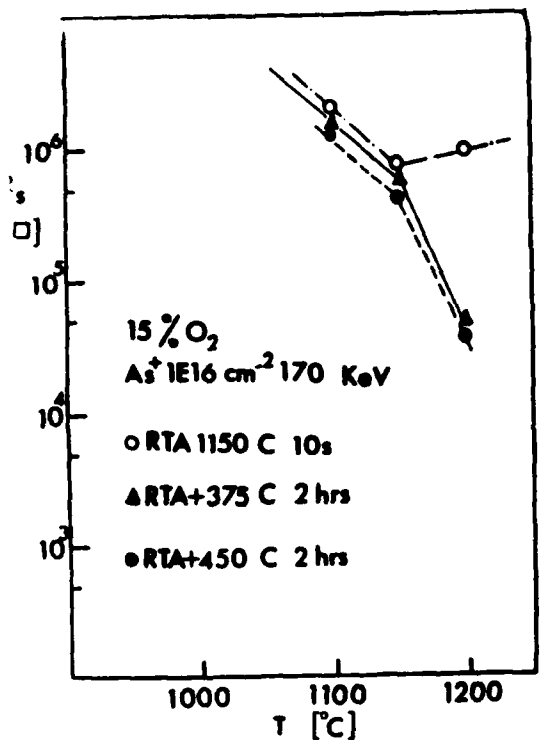

Fig. 1. Variation of the sheet resistance of doped SIPOS with rapid thermal annealing temperature and post annealing

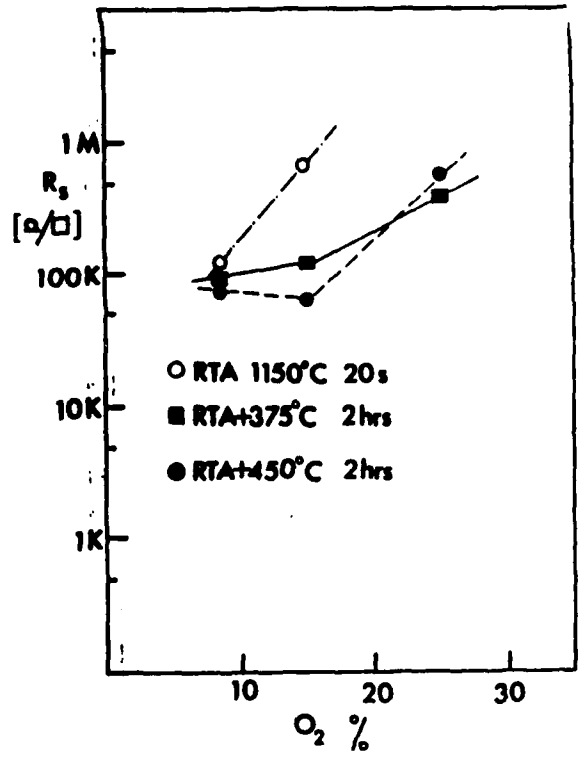

Fig. 2. Effect of oxygen concentration on sh resistance of doped SIPOS

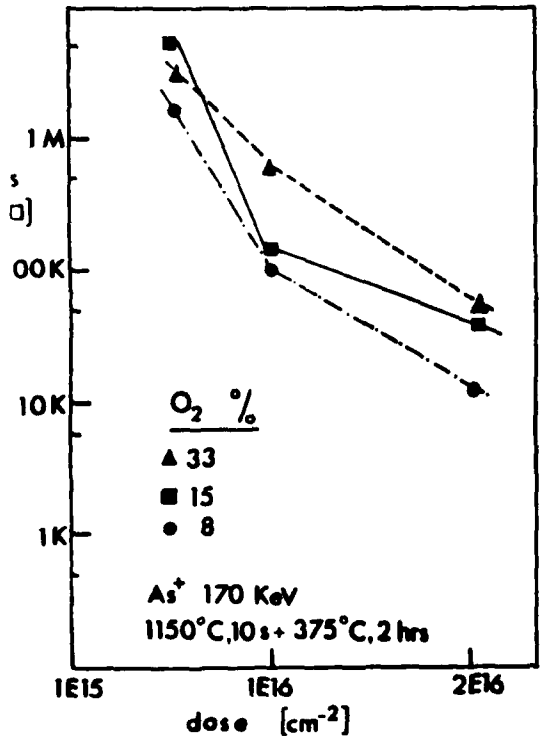

Fig. 3. Effect of dopant dose on sheet resistance of doped SIPOS

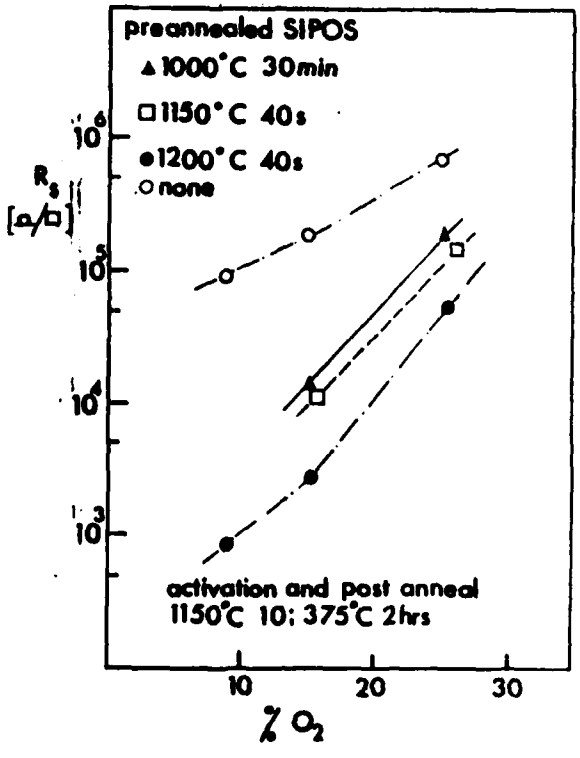

Fig. 4. Effect of preannealing on the sheet resistance of doped SIPOS (Arsenic implanted: 170 KeV, 1E16cm $^{-2}$)

Appendix II

Microstructure of Implanted and Rapid Thermal Annealed SIPOS

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167th Electrochemical Society Meeting
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MICROSTRUCTURE OF IMPLANTED AND RAPID THERMAL ANNEALED SIPOS

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The study of SIPOS (semi-insulating polycrystalline silicon) has gained attention due to its practical importance as a passivation layer in high voltage bipolar silicon devices (1,2). SIPOS can be also used as a high injection efficiency emitter, as well as a high resistance material for resistors. When deposited by atmospheric pressure or low pressure chemical vapor deposition (APCVD or LPCVD), SIPOS is generally found to be amorphous (3-5). Previous investigations suggested that SIPOS films are in the form of SiO_x, where $0 \leq x < 2$ (2,5). It has been shown that the amorphous SIPOS layer can be completely converted into Si microcrystals and amorphous SiO_2-rich intergrain material following an 1100°C anneal (4-7).

In this study the structural aspects of SIPOS layers deposited on thermally-grown SiO_2 by CVD method at 614°C and 170 mTorr for 2 hours were analysed. Samples with SIPOS layers containing 10% and 30% of oxygen were investigated. Some SIPOS samples were ion-implanted with As or B. In the accompanying paper (8), electrical properties of the ion-implanted samples using different rapid thermal annealing processes are discussed. The samples investigated and their treatment schedules are shown in Table 1. The state of crystallization, as well as the magnitude and distribution of grain sizes in the SIPOS layer were determined from cross-section transmission electron micrographs (XTEM). Figure 1 is a XTEM of two pieces of the same amorphous SIPOS layer prepared face to face during the TEM sample thinning procedure. The micrograph is representative of either an as-deposited (sample 1) or an implanted (sample 3) SIPOS layer prior to annealing. The amorphous state was also confirmed by selected area diffraction analysis. Figure 2 shows the microstructure of a SIPOS layer treated via Rapid Thermal Annealing (RTA) at 1200°C for 40 sec (sample 2). The grain size of the polygonal microcrystals shown in Fig. 2 vary from 10 to 40 nm with a tendency for the larger grains to be closer to the deposited SiO_2 buffer layer. This is in contrast with deposited polycrystalline silicon which has a columnar grain structure emanating from the buried interface up to the free surface. If the as deposited SIPOS is first annealed and then subsequently annealed at 1200°C for 40 sec (sample 4, see Figure 3), then a uniform grain size is observed compared to the pre-annealed only layer (sample 2). It suggests the dopant material might have some influence on the grain nucleation and growth. The decrease of grain size in sample 2 would be expected to increase the sheet resistance of the layer. However, amount of free carriers supplied by activated dopant actually decreases the sheet resistance by more than two orders of magnitude. Figure 4 shows sample 6 which was pre-annealed at 1200°C for 40 sec, then ion-implanted and activated during annealing at 1150°C for 10 sec. The grain size is about equal to that of pre-annealed sample 2 but again due to the activated dopant, much lower sheet resistance was obtained.

The data in Figures 1 to 4 were obtained from SIPOS layers with 10% oxygen content of O_2. SIPOS layers with 30% O_2 content were also investigated and found to have a similar morphology to that of the 10% O_2 sample. The grain size of the higher O_2 content samples was about 50% smaller. The results show that the microstructure and the sheet resistance of SIPOS are correlated and depend on fabrication parameters such as oxygen content, concentration of dopants and thermal annealing process. For instance, initial results indicate that achieving a large grain size prior to dopant implantation yields lower sheet resistance layers than a traditional implant anneal sequence. Similarly to Matsushita et al. (3) and Hamasaki et al. (4) we found that the grain size will decrease with oxygen content, while the sheet resistance increases as expected.

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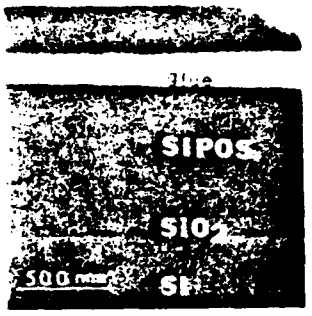
E 1. Treatment Schedule for X-TEM Samples Investigated

Process ple	1200°C 40 sec	As^+ 1E16cm^{-2} 170kev 25°C	1150°C 10 sec
1	-	-	-
2	yes	-	-
3	-	yes	-
4	yes -->	yes	-
5	-	yes -->	yes
6	yes -->	yes -->	yes
7	-	yes -->	yes*

C% O_2 content SIPOS sample has the same reatment as 30%'s
t 1200°C for 40 sec



jure 1. XTEM micrograph for sample representative of as-deposited and /or as-implanted SIPOS prior to any thermal treatment

jure 2. XTEM micrographs for sample 2 following 1200°C, 40 sec pre-anneal (a) dark field (b) selected area diffraction pattern

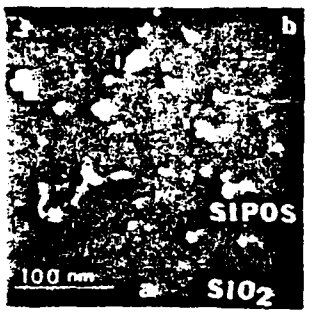


Figure 3. XTEM micrographs for sample 7, following As implantation and 1200°C, 40 sec anneal (a) dark field (b) selected area diffraction pattern

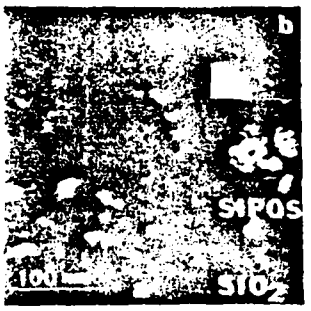


Figure 4. XTEM micrographs for sample 6 which has been both pre-annealed at 1200°C, 40 sec and post As-implantation annealed at 1150°C for 10 sec (a) dark field (b) selected area diffraction pattern

rater depth using a DAKTAK, and the boron ion concentration was calculated by sing the Si signal as a reference. The resulting SIMS profiles of 17 and 45 eV boron are shown in Fig. 5(a) and 5(b) respectively. It is seen that oncentration profiles vary with implant direction. The profile labeled (a) was btained by implanting into a wafer previously amorphized by Si or Ge ion mplantation. These profiles do not have a channeling tail. The ones labeled y (1) are implanted along [100] axis for 45 keV and (210) plane for 17 keV. hey have larger tails than the so called "random" implantation.

V. DISCUSSION AND SUMMARY

We have carried out an analysis of direct channeling during boron mplantation in silicon and made some predictions about which directions will ive less direct channeling. It should be pointed out that the implantation irections predicted for the least channeling probability are different from hose used in industry fabrication of devices. However, most often the exact mplant direction in an industrial process is not known. We have made ion mplantation in Si along well controlled directions and have measured the esulting boron concentration profiles. There are two cutoff conditions for eliminating the high index planes-(i) via the reference angle, and (ii) that he interplanar spacing be smaller than 2 x (screening radius + one dimensinal hermal vibration amplitude). The number of planes included on the map will epend on the incident ion energy only in the first case; however, by combining both conditions, we can select the common area on the map corresponding to $\theta = 5° \sim 6°$ and $\psi = 7° \pm 0.5°$ for 10 ~ 50 keV boron implantation into (100) silicon crystal, where θ is tilt angle from [100] axis and ψ is rotation angle from (100) plane. It is observed that the relative magnitude of the tails in

III. EXPERIMENT

The substrates used were 4 to 11 -Ωcm (100) n-type 2 inch silicon wafers. The silicon crystals were accurately aligned with backscattering of 700 keV $^4He^+$ as outlined in ref. [7], using a 2-axis goniometer (tilt and rotation). Since the [100] surface normal of the wafer is not collinear with the axis of rotation due to the offset of the real surface from the (100) crystal plane, the implant direction (θ and ψ) with respect to the crystal axis frame of reference has been transformed to the rotational axis frame of reference as described in Appendix A. After careful alignment, 17 and 45 keV boron ions to doses of 5×10^{14} and 1×10^{15} cm^{-2} respectively were implanted along various directions as specified in Fig.4c and d at room temperature. We have also implanted boron into the preamorphized silicon wafers as a reference. $^{28}Si^+$ ions with an energy of 150 keV and a dose of $2 \times 10^{15} cm^{-2}$ were first implanted into the silicon crystals at liquid nitrogen temperature and then the 45 keV boron ions were implanted at room temperature. The pre-amorphization of the silicon crystal for 17 keV boron implantations was done by 150 keV Ge^+ implantation at room temperature to a dose of 1×10^{15} cm^{-2}. The boron beam was electrostactically scanned by two sets of parallel plates across the wafer surface. The parallel scan avoids angular variations during the implantation and the beam divergence is estimated to be less than 0.2°. The samples were unannealed and boron concentration profiles were obtained using a CAMECA IMS 3F secondary ion mass spectrometer (SIMS). The primary sputtering beam was O_2^+ with ~ 10.5 keV impact energy and ~ 3000 nA primary current for 45 keV boron concentration profiles, and with ~ 5.5 keV impact energy and ~ 550nA primary current for 17 keV boron concentration profiles. The conversion of time to depth scales was done by measuring the sputter

the interplanar spacing of 0.42 Å is smaller than 2 x (screening radius + one dimensional thermal vibration amplitude). In the case at hand the screening radius is ~0.15 Å and the thermal vibration amplitude at room temperature is ~0.075 Å. Therefore, only planes with $d_p > 0.45$ Å can accomodate planar channeling.

Crystal planes were chosen for inclusion on the map according to the above assumption and are shown in Fig. 3. The others which are marked by an asterisk in Table 1 are considered as random equivalent planes. The interesting area of the stereogram is limited within $\theta \sim 10°$ and $\psi \sim 45°$, since larger tilt angles are unacceptable from a practical point of view due to mask shadowing effects. A straight line approximation for the great circle of Fig. 3 has been used for small angles ($\theta \sim 10°$). The resulting unshaded areas, which are specified by black bars in Fig. 4, were obtained for boron ions into Si crystal at 4 different energies according to the above assumptions. It is interesting to notice that for 45 keV there are four black areas corresponding to low channeling probability, at 10 keV there is one, and at 5 keV there is none. It is seen that there exists a common area located near the {100} plane for energies in the range 10 to 50 keV. Within this area the most favorable implantation direction should be towards a larger θ rather than at the center of the area in order to minimize the scattering "feed in" into the [001] channel.

Four different implantation directions specified by numbers in Fig. 4(c) and (d) were selected for 17 and 45 keV boron implantation into silicon in order to find the dependence of the channeling effect on implant directions.

The reference angle θ_{ref} is defined with reference to Fig. 2 as

$$\theta_{ref} = \arctan\left(\frac{d_p - 2\rho}{d_{row}}\right) \tag{5}$$

where ρ is the one dimensional thermal vibration amplitude and the atomic spacing under consideration, d_{row}, is related to the atomic density of target, N, by

$$d_{row} = (1/d_p N)^{-1/2} \tag{6}$$

The atom locations in Fig. 2 are shown as fixed at the corner of squares with sides equal to d_{row} in the atom plane under consideration and the volume per atom is equal to $d_p \times d^2_{row}$.

For very high index planes the classical critical angle for planar channeling (ψ_p) can be larger than the reference angle and we will regard these planes as random equivalent planes. This assumption is based on the following considerations. The classical critical angle does not adequately describe the physical situation when the incident angle is larger than the reference angle. For instance, when the incident angle is between Ψ_p and θ_{ref} (path ② in Fig. 2), the ion can be considered to be dechanneled by a binary collision. The definite channeling occurs only when the incident angle is smaller than θ_{ref} (path ① in Fig. 2). But θ_{ref} is extremely small for high index planes (e.g. ~.15° for {722}), which planes will not play a significant role in planar channeling compared with low index planes and can be ignored for mapping. The cutoff condition ($\psi_p > \theta_{ref}$) for excluding planes on the map corresponds to a situation where there are more than 13 planes within the lattice constant of silicon (~5.431 Å). It seems quite reasonable that the cutoff planes ($d_p \leq 0.42$ Å) will have a high dechanneling probability since

$$d_\ell = S_\ell \sqrt{h^2 + k^2 + \ell^2}\ d_o \tag{1}$$

and

$$d_p = S_p \left(\sqrt{h^2 + k^2 + \ell^2}\right)^{-1} d_o \tag{2}$$

where d_o is the lattice constant and S_ℓ, S_p the multiplicative constants which are equal to 1 for a cubic structure. For the diamond structure they are respectively given by

$$S_\ell = \begin{cases} 1 & \text{if } h + k + \ell \text{ is odd} \\ 1/2 & \text{if } h, k \text{ and } \ell \text{ are all odd} \\ 1/2 & \text{if } h + k + \ell \text{ is even} \end{cases} \tag{3}$$

and

$$S_p = \begin{cases} 1/2 & \text{if } h + k + \ell \text{ is even} \\ 3/4 & \text{if } h, k \text{ and } \ell \text{ are all odd} \\ 1/4 & \text{otherwise} \end{cases} \tag{4}$$

Since the interatomic and interplanar spacings for all odd integers of h, k and ℓ are not equally spaced but have (1/4, 3/4) combination, S_ℓ for interatomic spacing has been averaged for axial channeling and S_p for interplanar spacing has been assigned by 3/4 for which the planar channeling assumes to be dominant compared to 1/4 spacing.

Table 1 shows the calculated critical angles for boron ions into a Si crystal for different energies. Very high index planes should not be included in the map since the channeling effect vanishes for sufficiently high indices. We have derived a criterion by which high order axes and planes will be excluded from the map. We rule out planes yielding a classically calculated critical angle for channeling which is larger than a crystal lattice related reference angle. The definition of this reference angle and the justification for applying the rule will be given in the following.

we aim at is one where the probabilities for channeling can be compared for different implant directions simply by visual inspection of the map. We have chosen to map implant direction relative to crystallographic directions in stereographic representation. Crystal axes and planes are placed onto this map. Each axis and plane will be surrounded by an area corresponding to the critical angle for channeling. When the representation of an implant direction falls within these areas, the channeling probability for that situation is significant.

We have chosen a stereographic projection to represent crystallographic directions onto a two dimensional surface. One arrives at this image by first representing each direction as a vector from the center of a sphere to its surface. The vector endpoints on the sphere are then projected onto a plane cutting the sphere in two equal halves. The points in this plane are representations of crystallographic axes, and the locus of a great circle through the points will represent a crystal plane. Because of the symmetry of the cubic structure with respect to the [001] direction, all variations will be described in one eighth (θ = 0°~90°, ψ = 0°~45°) of the whole area.

In order to find areas on the stereogram where the incident ions might be well channeled, the critical angles for axial and planar ion channeling were plotted as shown in Fig. 1. The shaded portions of the figure represent areas of high channeling probability; i.e. the unshaded areas represent the incident directions along which the channeling probability might be greatly reduced. The critical angles of boron ions were calculated according to Lindhard[2] together with the suggestion for the "critical approach distances" by Morgan and Van Vliet[5]. These calculations make use of the interatomic spacing along a row, d_ℓ, and the interplanar spacing, d_p. For an axis or plane with the Miller index (h, k, ℓ) and a cubic structure, these are given by:

in order to minimize unintentional channeling; but they did not consider the effect of rotation angle. Liu and Oldham[4] carried out a similar procedure where the substrate was tilted 8° with respect to the 25 keV boron ion beam direction and rotated 8° or 0° away from the (100) plane. Wilson[5] also followed a similar procedure. In that case the (100) Si wafer was tilted 7 ~ 8° with respect to the surface normal and then rotated so that the beam direction made an angle of 18° with respect to the (100) plane which incidentally is very close to the (310) plane (18.5°) as shown in Fig. 3. Another approach which is commonly used to minimize the channeling effect is to tilt the substrate ~ 7^{o} from the normal incidence, leaving the precise rotation angle arbitrary.

In this paper we approach the problem by mapping major crystalline axes and planes near the surface normal of a (100) cut crystal. This procedure will help us in selecting the optimum implant direction for minimizing ion channeling. Experiments have been carried out by implantation along several specific directions. Impurity concentration profiles are qualitatively compared to our analytical predictions.

II. ANALYTICAL TREATMENT; MAPS OF CRYSTAL DIRECTIONS

In this section we will derive a map of crystallographic directions which will be the basis for selecting optimum implantation directions in order to minimize channeling. We have applied the criterion that the implantation direction should not be too far off the surface normal. This requirement would also have to be applied in a practical implantation situation to minimize the shadowing effect and lateral spread at oxide window steps. In this treatment, we have chosen 10° as a maximum allowed tilt. The kind of map

I. INTRODUCTION

Ion implantation is one of the most important processes in impurity doping. This is because ion implantation can precisely control both the dopant concentrations and the dopant's depth distribution. With the trend towards reduced device dimensions to the micrometer or submicrometer range, shallow junction technology for complementary metal-oxide-semiconductor (CMOS) and bipolar junction transistors (BJT) has recently emerged as an important area for VLSI development.

The formation of tails in implant dopant profiles has been known as one of the major problems for shallow junctions, especially for p^+/n junctions in p-MOS devices in which boron ions are the acceptor of choice. Blood, et al. [1] have shown that the tail in implanted profiles in crystalline targets is mainly due to atoms which are scattered into channels rather than an interstitial diffusion mechanism at the implantation temperature. Since low ion energies have to be applied for shallow junction devices and the critical angle for ion channeling increases with decreasing incident energy of the ions[2], channeling tails become a major problem for shallow junction device fabrication. The problem is more significant for light ion implantation such as boron in Si due to the fact that light ions are not effective in making the target crystal amorphous, which for heavier ions will reduce the effect of channeling.

Several attempts have been made to avoid channeling in single crystal silicon targets by implanting along crystallographic directions away from the major planes and axes. Wilson, et al.[3] suggested that the substrate must be oriented so that the nearest low index crystallographic direction is at least twice the classical critical angle for channeling away from the beam direction

CHANNELING EFFECT FOR LOW ENERGY ION IMPLANTATION IN Si

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ABSTRACT

Ion implantation is one of the most important processes in semiconductor device fabrication. Due to the crystalline nature of Si, channeling of implanted ions occurs during this process. Modern devices become smaller and shallower and therefore require ion implantation at lower energies. The effect of channeling on ion implantation becomes a significant problem for low energy ion implantation. The critical angle for axial and planar channeling increases with decreasing energy. This corresponds to an increased probability for channeling with lowering of ion energy. The industry approach to avoid the channeling problem is to employ a tilt angle of 7° between the ion implantation direction and the surface normal. We approach the problem by mapping major crystalline axes and planes near the [100] surface normal. Our analysis indicates that a 7° tilt is not an optimum selection in channeling reduction. Tilt angles in the range 5° to 6° combined with 7° ± 0.5° rotation from the (100) plane are better selections for the reduction of the channeling effect. The range of suitable angles is a function of the implantation energy. Implantations of boron along well specified crystallographic directions have been carried out by careful alignment and the resulting boron profiles measured by SIMS.

Appendix III

Channeling Effect For Low Energy Ion Implantation in Si

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TABLE 4. Treatment Schedule for XTEM Samples Investigated (25% oxygen content O_2^+ ion-implanted sample)

Process +Sample	1200°C 40 sec	O_2^{+*}	1150°C 10 sec	Oxide	Comment
1 (#5)	-	-	-	T++	Columar grain structure emanating from buried interface to surface
2 (3I1)	-	yes	-	T++	Totally amorphous without any notice of lattice damage
3 (3A1)	-	yes --> yes		T++	Fine grain microstructure

+ 25% O_2 content in O_2^+ ion-implanted sample

++ sample 1 to sample 3 contains 35.0nm-thickness thermal-grown silicon dioxide

* O_2^+

energy(kev)	dose amount(cm^{-2})
140	8.5455E16
100	8.3925E15
60	3.1885E15
25	1.3108E15

TABLE 3. Treatment Schedule for XTEM Samples Investigated (5% oxygen content O_2^+ ion-implanted sample)

Process +Sample	1200°C 40 sec	O_2^{+*}	1150°C 10 sec	Oxide	Comment
1 (#5)	-	-	-	T++	Columar grain structure emanating from buried interface to surface
2 (1I1)	-	yes	-	T++	Amorphous
3 (1A1)	-	yes -> yes		T++	Longer grains near SIPOS-Si interface, decreasing in size from substrate to surface
4 (#7)	-	-	-	N++	Finer columar grains
5 (6I1)	-	yes	-	N++	

\+ 5% O_2 content in O_2^+ ion-implanted sample

++ sample 1 to sample 3 contains 35.0nm-thickness thermal-grown oxide and sample 4 to sample 5 contains 1.0 to 1.5nm-thickness *nature oxide*

* O_2^+ energy(kev) dose amount(cm^{-2})

140	1.71E16
100	1.68E15
60	6.38E15
25	2.62E15

[NOTE]

410nm-thickness polysilicon deposited by LPCVD method was onto 80nm-thickness thernally-grown SiO_2 which grew on the CZ-grown n-type Si substrates. The sheet resistance R_s is 220 ohm/□ for polysilicon which is ion-implanted with 1E+16 cm^{-2} As^+ at 100kev, and activated by rapid thermal annealing at 1150°C for 10 sec. Comparatively, R_s is 90 ohm/□ for the single crystal which is ion-implanted with 1E+15cm^{-2} As^+ at 100kev and then 15 sec exposure at 1150°C. (Powell, R. and Chow, R.,J. Electrochem. Soc., 132(1), 194 (1985)

TABLE 2. SIPOS (30% oxygen content)

Process +Sample	1200°C 40 sec	As^+ 1E16cm^{-2} 170kev 25°C	1150°C 10 sec	Comment
1	-	-	-	As deposited, totally amorphous
2	yes	-	-	A fine 175 Å grain structure of SIPOS with some notice of larger grains existing at the SiO_2-SIPOS intterface
3	-	yes	-	Appears as deposited with no resemblence of lattice damage
4	yes -->	yes	-	The top one third of the SIPOS layer was amorphized. The lower two thirds remined crystalline.
5	-	yes -->	yes	A very fine 50 Å grain structure existed
6	yes -->	yes -->	yes	From the SiO_2-SIPOS interface to the upper third of SIPOS, the structure consisted of a mixture of fine and large 175 A grains. The upper third consisted only of the fine grains.
7	-	yes -->	yes*	The grain structure appears as the above sample. The smaller grain size may suggest that the dopants have some influence on grain growth and nucleation

+ Thermally-grown oxide , $H_2 + O_2$
* at 1200°C for 40 sec

Table 1. SIPOS (10% oxgen content)

Process +Sample	1200°C 40 sec	As+ 1E16cm-2 170kev 25°C	1150°C 10 sec	Comment
1	-	-	-	As deposited, totally amorphous, confirmed by selected area diffraction
2	yes	-	-	Textured 250 Å grains with a tendency for the larger grains to appear at the SiO_2 interface.
3	-	yes	-	Appears as deposited, with no notice of any latice damage
4	yes -->	yes	-	After the implantation the upper third of the SIPOS was amorphsized, while the remainder was undamaged
5	-	yes -->	yes	Fine grain size on the order of 125 Å
6	yes -->	yes -->	yes	Mixture of fine and large 250 A grains appearing from the upper one-third of SIPOS. From the surface to the upper one-third of SIPOS, only small grains exist.
7	-	yes -->	yes*	The grains structure is as above. The smaller grains in the upper third may be due to the dopants influence on nucleation and growth.

+ Thermal oxide, furance grown $H_2 + O_2$ (3.5 kÅ)
* at 1200°C for 40 sec

[NOTE]
The increased oxygen content of the 30% SIPOS produced the smaller grains relative to the 10%, even though the identical processes produced like morphologies.

the profiles are in agreement with our predictions. This indicates that direct channeling may play a role in the magnitude of the tail. However, it is also observed for all implantations into single crystals that the tails are substantially larger than for implantations into amorphous material. This means that the scattering "feed in" process is quite important. Ions can get scattered into channels and thus penetrate deeply into the crystal. This latter effect cannot totally be removed by alignment of the crystal targets for low energy ion implantation. Our predictions are that these effects also will be more severe for lower implant energies.

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APPENDIX A. SAMPLE ALIGNMENT PROCEDURE

The target geometry associated with [100] crystallographic axis, ion beam direction and the rotation axis is shown in Fig. 6. Since the implant directions as shown in Fig. 4c and d are related to the crystallographic axis frame of reference and the tilted angle θ'' and rotational angle ψ'' are related to the rotational frame of reference, the implant direction (θ, ψ) with respect to the crystal frame of reference have to be transformed into the rotational frame of reference (θ'', ψ'') as shown in Fig. 7. The real rotational frame (i.e. X '', Y'' and Z'' coordinate) can be transformed by δ-rotation with respect to Z axis followed by β-rotation with respect to Y' axis and the conventional transformation matrix can be applied such that

$$\begin{pmatrix} \sin\theta'' \cos\psi'' \\ \sin\theta'' \sin\psi'' \\ \cos\theta'' \end{pmatrix} = \begin{pmatrix} \cos\beta\cos\delta & \cos\beta\sin\delta & -\sin\beta \\ -\sin\delta & \cos\delta & 0 \\ \sin\beta\cos\delta & \sin\beta\sin\delta & \cos\beta \end{pmatrix} \begin{pmatrix} \sin\theta\cos\psi \\ \sin\theta\sin\psi \\ \cos\theta \end{pmatrix} \quad \text{(A-1)}$$

In order to determine δ and β, the wafer was tiled by 6° from the roughly estimated surface normal and rotated up to 360° with measuring the back-scattered yield by 1° increment. The 8 minimum yields of backscattered $^4He^+$ are corresponding to well-defined planar minima and plotted on polar coordinate graph paper as shown in Fig. 8. Since the incident ions are more well channeled along the (110) plane than along the (100) plane for the diamond structure, it is easy to identify which plane is (100) or (110). The line AA' through the center of the polar diagram and the point of cross section of 4 planar lines can be made and the δ-angle is measured counterclockwisely from

(100) surface line. The fine tuning to find the exact [001] position is the next step by varying only the tilt angle θ by 0.1° increment along the line AA' and θ_1 is assigned to the [001] axis position. The next step is 180° rotation from the point A, and then the same procedure for finding [001] axis position is followed, and θ_2 is assigned to another [001] axis position. Since the rotation axis must lie between θ_1 and θ_2, the angle β can be determined by the following formula:

$$\beta = \frac{1}{2}(\theta_1 + \theta_2) - \theta_2 = \frac{1}{2}(\theta_1 - \theta_2) \qquad \text{(A-2)}$$

With δ and β values, the ion implant direction (θ and ψ) associated with (x, y, Z) coordinate can be transformed by Eq. (A-1) into the real rotational frame of reference (θ'' and ψ'') associated with the goniometer manipulation.

TABLE 1

Calculated Critical Angles for Boron Ion into Silicon

Miller Index		Energy (keV) 5	10	20	50	100	θ_{ref}(deg.)	d_p(Å)
100	axial	5.63	4.90	4.27	3.47	2.86	17.45	1.36
	planar	6.68	4.73	3.34	2.11	1.50		
110	axial	7.42	6.48	5.61	4.48	3.63	28.72	1.92
	planar	7.92	5.62	3.98	2.51	1.78		
111	axial	6.31	5.51	4.79	3.86	3.16	28.07	2.35
	planar	8.60	6.22	4.40	2.78	1.97		
210	axial	2.99	2.57	2.24	1.87	1.60	4.54	0.61
	planar	4.47	3.16	2.24	1.42	1.00		
310	axial	3.92	3.39	2.96	2.45	2.06	8.33	0.86
	planar	5.32	3.76	2.66	1.68	1.19		
511	axial	2.66	2.29	1.99	1.66	1.42	5.06	0.78
	planar	5.08	3.59	2.54	1.60	1.13		
*610	axial	1.33	1.18	1.01	0.84	0.73	0.43	0.22
	planar	2.71	1.92	1.36	0.86	0.61		
*722	axial	1.09	0.99	0.85	0.70	0.61	0.15	0.18
	planar	2.43	1.72	1.22	0.77	0.54		
751	axial	1.77	1.53	1.32	1.10	0.96	2.00	0.47
	planar	2.78	1.97	1.40	0.88	0.62		
*832	axial	0.94	0.88	0.76	0.62	0.54	0.02	0.15
	planar	2.26	1.60	1.13	0.71	0.50		

FIGURE CAPTIONS

Figure 1

A map over implant directions in stereographic representation showing construction of shaded areas by applying the axial and planar critical angles. The unshaded ares, ① and ② represent directions for which the channeling probabilities are less than for ions incident on shaded areas

Figure 2

The geometrical definition of the reference angle, θ_{ref} , where ρ is the one dimensional thermal vibration amplitude and d_p the interplanar spacing and d_{row} the atomic spacing. The ion beam with incident angle less than θ_{ref} (path ①) might be well channeled between the planes, but the ions with angles between the planar critical angle (ψ_p) and θ_{ref} (path ②) might be dechanneled from a binary collision point of view or be channeled via a critical angle concept.

Figure 3

The remaining planes with $\theta = 10°$ and $\psi = 45°$ which affect boron ion channeling into silicon. The straight line approximation for a great circle is used, since the interesting areas of the stereogram are limited by small tilt angle.

Figure 4

"Random directions" (black bars) to avoid channeling during boron ion implantation into silicon crystal at different energies; (a) 5 keV B^+ case, where no "random directions" can be found; (b) 10 keV case, where one area ($4.6° < \theta < 5.8°$, $4.5° < \Psi < 8°$ is obtained; (c) 20 keV case, where three "random areas" ($4° < \theta < 6.5°$, $4° < \psi < 9°$, $4° < \theta < 5.5°$, $21° < \psi < 24°$ and $4° < \theta < 5.5°$, $33° < \Psi < 40°$) are shown. Three implant directions (leveled by ①, ② and ③) are chosen for 17 keV boron implantation, where ① represents the direction along (210) plane away from [100] axis by 7°, ② the direction with $\theta = 8°$, $\psi = 8°$ which point is located outside of the specified black bar, and ③ the suggested "random direction" is given by $\theta = 6.5°$, $\psi = 6°$; (d) 45 keV case, where four possible areas can be obtained within $\theta = 3.5 \sim 6.5°$ and $\psi = 4 \sim 10°$, $13 \sim 17°$, $21 \sim 25°$ and $33 \sim 42°$ respectively. The real implant directions for 45 keV are shown by ①, ②, ③, and ④, which are specified in Fig. 5(b).

Figure 5

SIMS depth profiles of boron implantation into silicon at various tilt and rotation angles; (a) is for 45 keV to a dose of 1×10^{15} cm^{-2}, (b) is for 17 keV to a dose of 5×10^{14} cm^{-2}.

Figure 6

Schematics of target geometry for crystal alignment. The angle β is the offset angle between the crystal [100] direction and the rotation axis of goniometer.

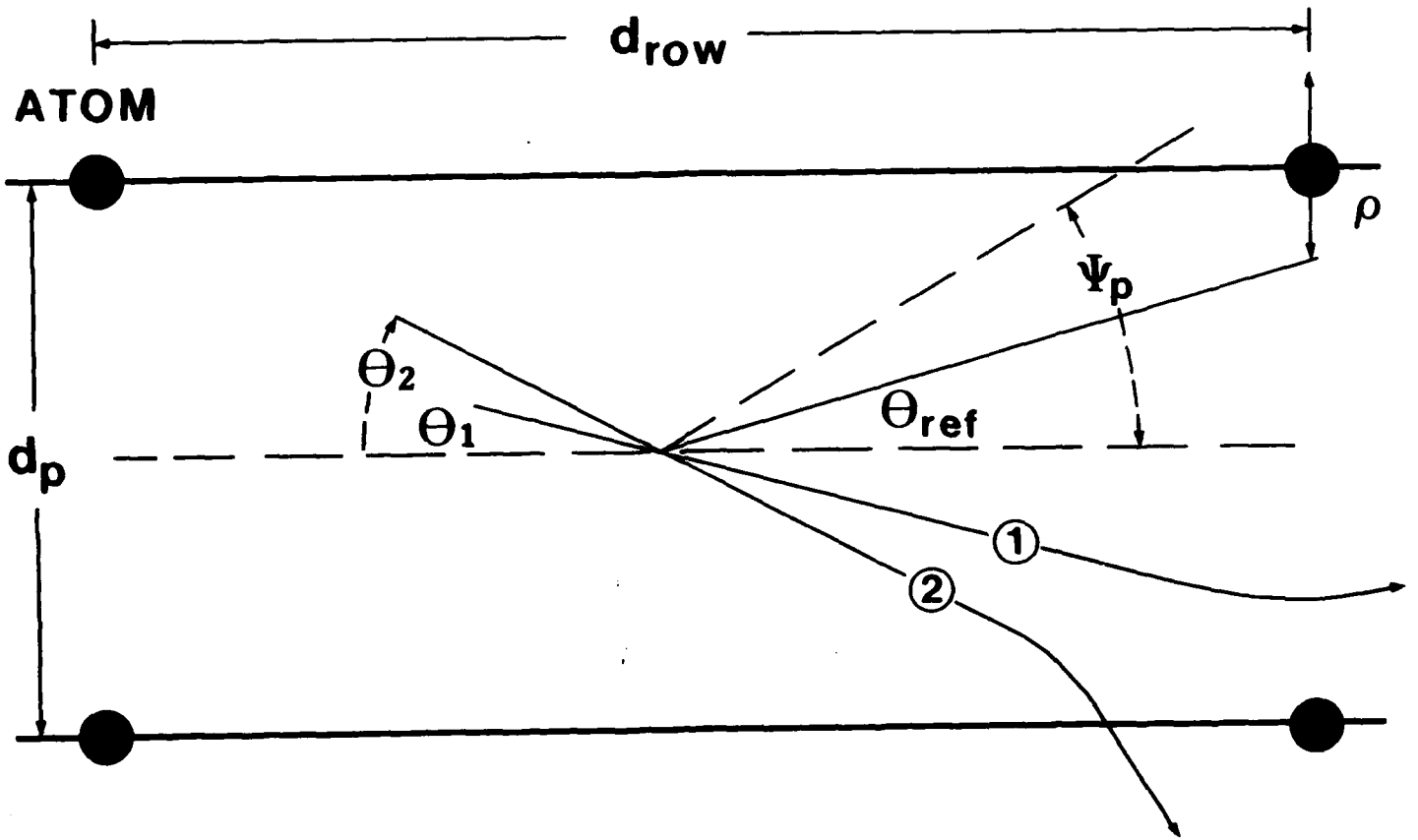
Figure 7

Relationship between coordinates of crystal axes and goniometer. The order of rotations is δ with respect to Z axis and β with respect to Y' axis. The angle β is the same as that in Fig. 6.

Figure 8

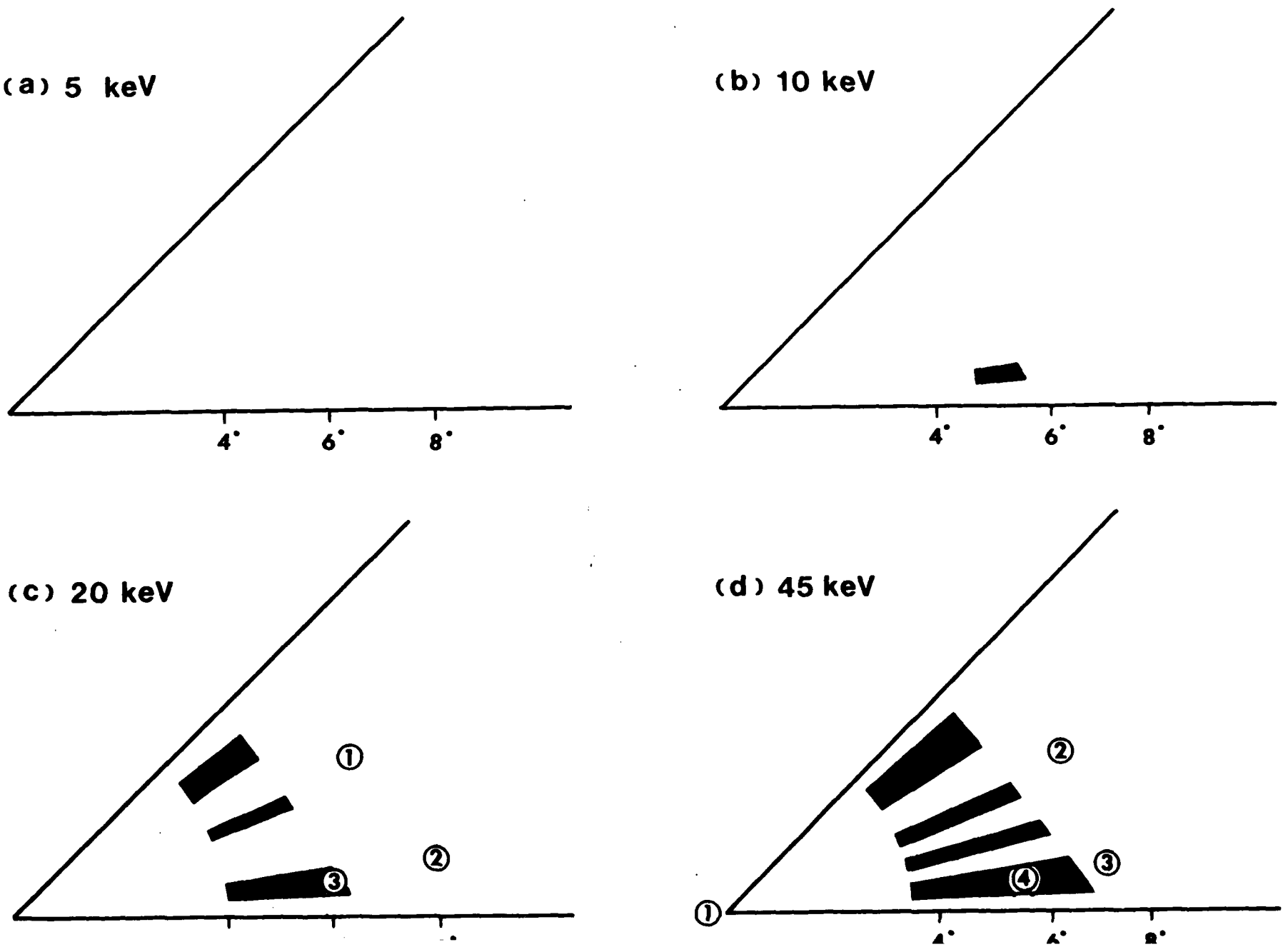
Polar diagram for determination of δ and β. The circle is associated with roughly 6° tilt from the surface normal. By rotating with 1° increment and measuring the backscattered yields of He^+, the eight minima and type of planes are identified. δ is the angle from (100) plane to the line of AA'. Fine tuning along A → A' by 0.1° variation gives the exact position of [100] axis, followed by 180° rotation from A to A' position and fine tuning again. This gives another [100] axis position, and the average value of two different [100] positions is the exact position of the rotation axis of the goniometer.

①,②: unshaded area
[001]
3°
5°
7°
9°
11°
θ (tilt angle)
axial critical angle
planar
critical angle
(100)
5°
15°
25°
35°
Φ (rotation angle)
(210)
(110)

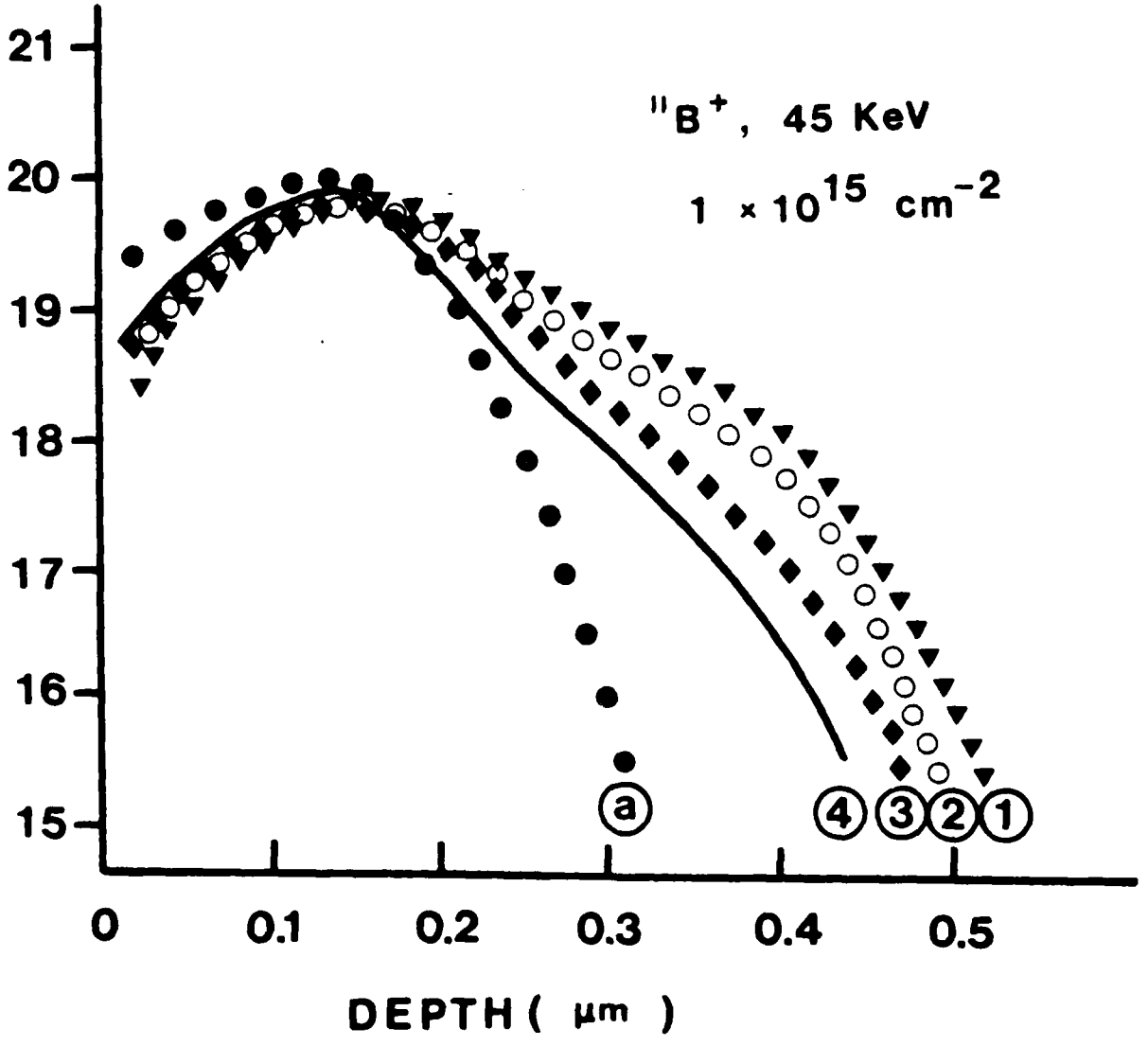


$$\Theta_1 < \Theta_{ref} < \Theta_2 < \Psi_p$$

[001]
2°
4°
6°
8°
10°
(100)
(510)
(310)
(210)
(530)
(110)
[1̄12]
[1̄10]
[1̄19]
[1̄18]
751
751
551
541
731
711
531
711
611
[017]
[016]
-10°
-20°
-30°
-40°


(a) 5 keV
4°
6°
8°
(b) 10 keV
4°
6°
8°
(c) 20 keV
①
②
③
(d) 45 keV
①
②
③
④

		θ	φ	
ⓐ	• • •	7°	?	preamorphous
①	▼ ▼ ▼	0°	0°	[100]
②	○ ○ ○	7°	26.56°	(210)
③	◆ ◆ ◆	7°	7°	
④	——	5.5°	7°	random



FIGRE 5(a)

	Θ	Ψ	
ⓐ ● ● ●	7°		preamorphous
① ◆ ◆ ◆	7°	26 56°	(2 1 0)
② ○ ○ ○	8°	8°	
③ ———	6.5°	6°	random

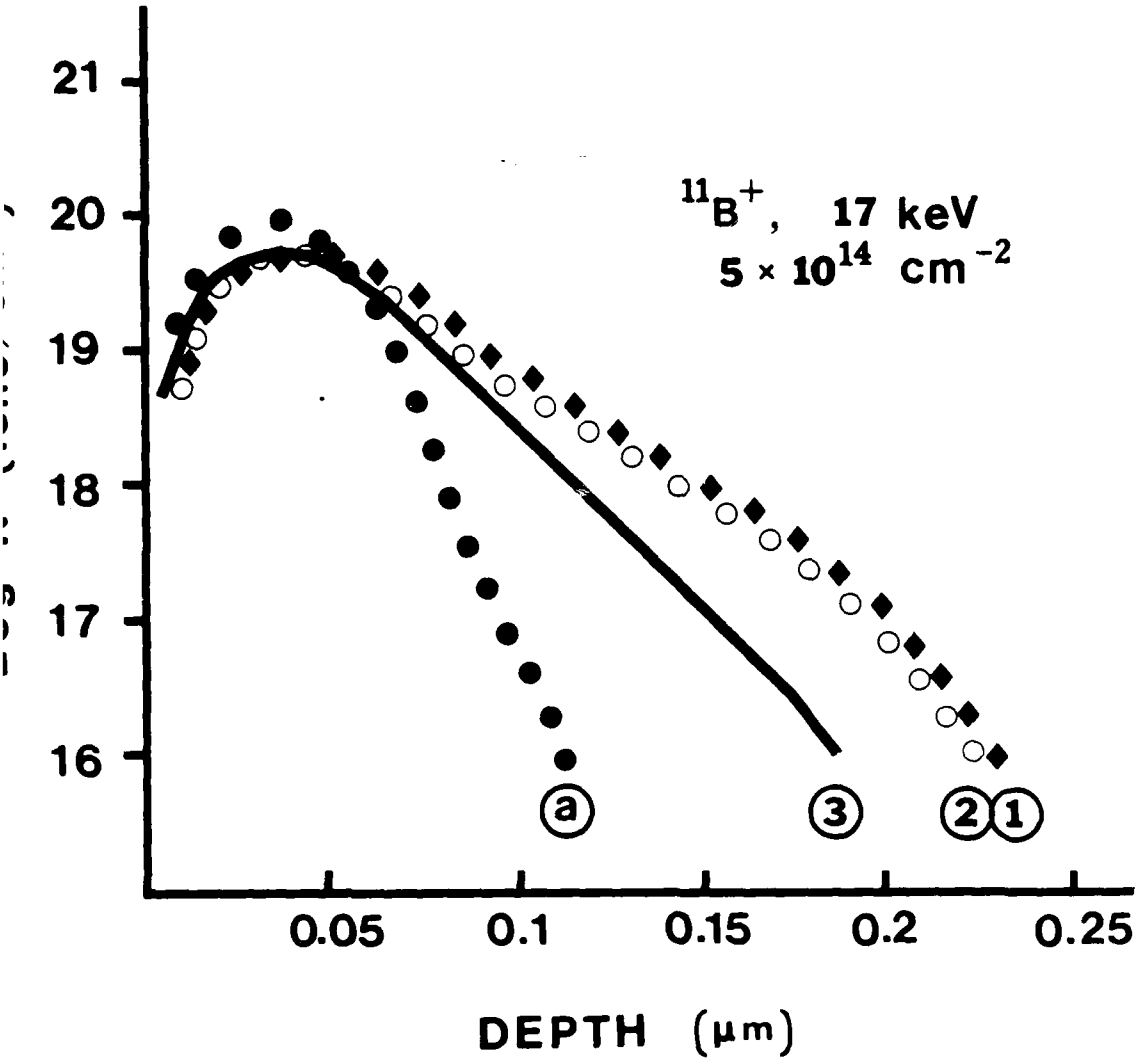


FIGURE 5(b)

sed Laser Annealing of BF_2^+ Implants

The samples for pulse laser annealing experiments were implanted with keV BF_2^+ ions to a dose of 1.0×10^{16} cm^{-2}, or with a low-energy dc glow scharge BF_3^+ ions, and annealed with single pulses of an excimer laser (λ 0.308 μm, τ = 50 ns). The BF_2^+ implanted specimens contained a 800 Å ick band of amorphous layer followed by a 150 Å wide band of dislocation ops. After irradiation with a 1.1 J cm^{-2}, "defect-free" regions were rmed with no amorphous layer and/or dislocation. Similarly a "complete" nealing for amorphous layer and dislocation loops were observed after a 4 J cm^{-2} pulse.

The SIMS results on boron and fluorine concentration profiles, before nd after laser annealing of 1.0×10^{16} cm^{-2} specimens, are shown in Figs.) and 11, respectively. The as-implanted profile is Gaussian with a peak round 400 Å. After laser annealing, the profile broadens considerably oth toward the surface and into the deeper regions of the crystals. From ne dopant profile broadening, the dopant diffusion coefficients were xtracted, which were found to be consistent with the diffusion coefficient f boron in liquid silicon. The amount of broadening increases with ncreasing pulse energy density because larger times for dopant diffusion re available. The peak in the fluorine concentration shifts slightly oward the surface after laser annealing. It is interesting to note that luorine distribution profile does not broaden after laser annealing, which s similar to the results obtained after rapid thermal annealing. The ntegrated amount of fluorine was found to be 95% and 40% of the as-nplanted value after 1.1 and 1.4 J cm^{-2} laser pulses, respectively. igure 12 shows fluorine distribution profiles from glow-discharge

teresting to note that unlike boron distribution profiles, the fluorine stribution profiles do not exhibit broadening with increase in time or mperature of annealing.

The SIMS results on boron distribution profiles from 1.0×10^{15} cm^{-2} iplants are shown in Fig. 8. The as-implanted profile of boron is Gaussian ith a peak around 400 Å. After rapid thermal annealing treatments, the aussian profile broadens both toward the surface and into the deeper regions f the crystal. The depth distribution profiles after 1050°C/5s and 000°C/10s annealing treatments were found to be almost identical. Further ncrease in time and temperature resulted in more broadening of the profile. he amount of broadening was found to be the same for similar annealing reatments of 6.0×10^{14} and 1.0×10^{15} cm^{-2} specimens. The fluorine con-entration profiles from companion specimens before and after rapid thermal nnealing treatments are shown in Fig. 9. The fluorine profile in as-mplanted specimens is Gaussian with a peak around 400 Å. After the rapid hermal annealing, the peak in the fluorine concentration appears at a lepth of 660 Å with a knee around 400 Å depth corresponding to the as-mplanted peak. The peak concentration is higher than the implanted peak :oncentration, indicating segregation of fluorine at the dislocations. ıfter 1050°C/10s and 1100°C/6s annealing treatments, the peak concentration lecreases and the knee at 400 Å depth is eliminated. The concentration of luorine remaining was found to be 60, 40, and 36% of the as-implanted con-:entration after 1050°C/5s, 1050°C/10s, and 1100°C/6s annealing treatments, espectively. Similar to the results shown in Fig. 7, no broadening in the luorine distribution profile is observed after the above annealing treat-ıents.

he segregation of fluorine at the dislocation is clearly delineated in ig. 5. The average size of the bubbles was determined to be 50 Å and they ıre seen to be associated with the dislocations (as indicated by an arrow).

;IMS Results on Boron and Fluorine Distributions

Figure 6 shows boron concentration profiles before and after rapid :hermal annealing treatment of (100) Si specimens implanted with 6.0×10^{14} $^3F_2^+$ ions cm^{-2}. The as-implanted specimens contain a Gaussian profile with a peak around 400 Å. After thermal annealing treatments, the profiles spread toward the surface and into the deeper regions of the material. The dopant profiles after 1000°C/10s and 1050°C/5s annealing treatments were found to be almost identical. As the time or temperature of annealing is increased, the amount of spreading increases. The average profile broadening is less than 500 Å even after 1100°C/6s annealing treatment. The amount of boron integrated over depth remains approximately the same after the various annealing treatments. The results on fluorine distribution profiles from the specimens of Fig. 6, are shown in Fig. 7. The as-implanted fluorine profile is Gaussian with a peak around 400 Å. After rapid thermal annealing treatments, the peak in the fluorine concentration is observed at a depth of about 600 Å, which corresponds to the band of dislocation loops, as shown in Fig. 3. These results show that the fluorine is gettered by the dislocations, which is in agreement with the TEM results shown in Fig. 5. It is interesting to note that fluorine is removed significantly from the regions, which are free from the extended defects such as dislocations. After the 1050°C/5s annealing treatment 76% of the fluorine is retained. These percentages drop to 33 and 31% after 1050°C/10s and 1100°C/6s annealing treatments, respectively. It is

dose of 1.0×10^{14} cm^{-2}. The as-implanted specimens (Fig. 2a) contained a 120 Å thick amorphous layer followed by defect clusters and dislocation loops. After annealing treatment at 1050°C for 5 seconds (1050°C/5s), the amorphous layer has grown "defect-free" and dislocation loops are observed below the original amorphous layer (Fig. 2b). It is interesting to note that some loops appear in the much deeper regions (up to 400 Å depth) compared to the depth (120 Å) of the original amorphous-crystalline interface. After annealing at 1100°C for 10 seconds, the dislocation loop density decreases considerably, almost to a negligible value (Fig. 2c). The results from specimens implanted with 50 keV BF_2^+ ions to a dose of 6.0×10^{14} cm^{-2}, are given in Fig. 3. The as-implanted specimens contained a 440 Å thick amorphous layer followed by a 160 Å wide band of defect clusters and dislocation loops. The microstructures after different annealing treatments are shown in Fig. 3(b) [1000°C/10s], Fig. 3(c) [1050°C/5s], and Fig. 3(d) [1050°C/10s]. In each case, the amorphous layer has grown epitaxially creating a region free from visible defects leaving a residual band of dislocation loops centered at a depth $\sim$600 Å.

The annealing results from specimens implanted with 50 keV BF_2^+ ions to a dose of 1.0×10^{15} cm^{-2}, are shown in Fig. 4. The as-implanted specimens contained a 500 Å thick amorphous layer followed by 160 Å wide band of defect clusters and dislocation loops. After 1000°C/10s and 1100°C/3s annealing treatments, the results are shown in Fig. 4(b) and 4(c), respectively. The amorphous layer has grown epitaxially creating virtually a defect-free zone. The specimens contain a band of dislocation loops centered around 600 Å depth. Figure 5 is a plan-view micrograph from specimens shown in Fig. 4(c), containing dislocation tangles at a depth of 660 Å.

electron microscopy studies were made using a Philips EM-400 electron microscope. Boron and fluorine concentration profiles were measured by secondary ion mass spectrometry (SIMS) techniques using O_2^+ primary ion beam. The depths were calibrated using the Dektak surface profilometer.

RESULTS AND DISCUSSION

A 50 keV BF_2^+ ion, within a few angstrom of penetration, presumably breaks into one 11.2 keV B^+ and two 19.4 keV F^- ions. Figure 1 shows damage energy deposited as a function of depth for 11 keV B^+ and 19 keV F^- ions. The damage peak occurs around 120 Å, the projected range is 431 and 411 Å for 11 keV B^+ and 19 keV F^- ions, respectively. It is interesting to note that out of the 11 keV total energy for B^+ ions 5.8 keV (53%) goes into producing damage, whereas 12.2 keV out of the 19 keV total energy for F^- ions (64%) ultimately results in the damage production. The damage produced by F^- ions is almost twice that produced by B^+ ions and it occurs approximately in the same depth range. It has been shown that boron ion implantation at room temperature normally leads to the formation of dislocation loops. At room temperature the dynamic annealing as a result of vacancy-interstitial recombination during boron ion implantation prevents damaged regions from attaining 6.0×10^{23} eV/cm^3 which is the critical damage energy for amorphization. In the case of BF_2^+ implants, the damaged regions are able to attain the critical damage energy for amorphization even during implantation at room temperature. Therefore, the ion implanted layers are amorphous followed by a band of dislocation loops.

Figure 2 shows cross-section TEM micrographs before and after rapid thermal annealing treatment of (100) Si specimens implanted with BF_2^+ ions to a

EXPERIMENTAL

Silicon single crystals (having <100> orientations, 2–6 Ω-cm, n-type, Cz-grown) were implanted with 50 keV BF_2^+ ions to a dose ranging from 1.0 x 10^{14} to 1.0 x 10^{16} cm^{-2}. Some of the samples were implanted with BF_3^+ ions using dc (1 kV) glow discharge. The as-implanted samples were annealed using either the HEATPULSE or a graphite strip heater system for times 5 to 20 seconds in the temperature range 1050 to 1200°C. The specimen heating chamber of the HEATPULSE system consists of upper and lower banks of high-intensity, quartz-tungsten-halogen lamps enclosed by water-cooled reflective walls. A quartz diffuser plate is placed next to each bank to ensure uniform heating of the specimens that are placed equidistant between the upper and lower light sources. The heating and cooling rates of the specimens were estimated to be about 100°C/sec. The annealing results from the HEATPULSE system were compared with those obtained from a graphite strip heater where the heating and cooling rates are about 120°C/sec. The times and temperatures quoted for the heat treatments are those of the heating chamber or the graphite strip. It was determined that there is a time lag in heating between the specimens and the heating chamber, which varied from 2 (at 1100°C) to 4 (at 1000°C) seconds. Some of the ion-implanted specimens were annealed using a pulsed excimer laser (λ = 0.308 μm, τ = 50 x 10^{-9} seconds). The ion implantation specimens, before and after the annealing treatments, were studied by cross-section and plan-view electron microscopy. The specimens for cross-section electron microscopy were prepared by an ion thinning procedure, whereas the specimens for plan-view electron microscopy were prepared by a chemical polishing technique. The

therefore, amorphization can be attained. The molecular ions split, in the vicinity of the surface, into atomic species having the same velocity as the molecule. This results in low energy ions that create shallow implants with a thin amorphous layer near the surface. For example, a 50 keV BF_2^+ ion breaks into one 11.2 keV B^+ and two 19.4 keV F^+ ions. Thus, a 50 keV B^+ ion has approximately five times higher projected range compared to the 50 keV BF_2^+ ions. It should be pointed out that boron fluoride implants are more economical because they are directly available from the ion sources and, therefore, do not require expensive mass separation in the accelerator.

The annealing of thin amorphous layers having good electrical properties and minimum dopant profile broadening is desired in order to form shallow junctions. The shallow junctions are particularly required for very-large-scale-integrated (VLSI) circuit devices. Using conventional processing in a furnace, considerable dopant profile broadening occurs including the formation of undesirable defects in the substrate as a result of prolonged heating.

In this paper, we present results of a systematic investigation of rapid thermal annealing[5-9] (RTA) of BF_2^+ and BF_3^+ implanted, amorphous layers in which case good electrical characteristics along with minimum dopant profile broadening are obtained. These results are compared with those obtained using pulsed laser irradiation. The RTA involves solid-phase crystallization while the pulsed laser annealing occurs in liquid phase. Attention is focussed to the retention and gettering of fluorine in annealed samples.

INTRODUCTION

Ion implantation is now a well-established method of doping semiconductors. However, the displacement damage produced by energetic ions must be removed to recover electrical activation of dopants and mobility of carriers.[1] The displacement damage created by the ions is usually in the form of amorphous layers or dislocation loops.[2,3] During subsequent heating to remove the displacement damage, the amorphous layers can be annealed by the solid-phase-epitaxial (SPE) growth process; and the dislocation loops anneal out by conservative climb and glide processes.[3] It has been shown that SPE growth of amorphous layers results in much more efficient removal of ion implantation damage compared to the annealing of dislocation loops. Above a certain loop number density, if the separation between the two loops is less than the diameter of the larger loop, the loops coalesce to form yet larger loops, which may frequently lead to the formation of a cross-grid of dislocations. Therefore, one of the goals during ion implantation is to create an amorphous layer which can be annealed by SPE growth at relatively low temperatures. For a p-type doping, ion implantation with a common dopant such as boron results in the formation of only dislocation loops at room temperature. It is believed that light ions such as boron are not able to deposit critical damage energy density needed for amorphization[4] (6.0×10^{23} eV/cm^3), after normal implant doses. In these cases, interstitials and vacancies created by ion implantation cluster to form dislocation loops. In this state, it is more difficult to achieve efficient removal of damage and to attain good carrier concentration and mobility. Using molecular ions such as BF_2^+ for ion implantation, more damage energy is deposited by the F^+ ions over the same range as the B^+ ions and,

RAPID THERMAL AND PULSED LASER ANNEALING OF BORON FLUORIDE IMPLANTED SILICON*

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ABSTRACT

Characteristics of rapid thermal and pulsed laser annealing have been investigated in boron fluoride (BF_2^+ and BF_3^+) implanted silicon using cross-section and plan-view electron microscopy. The amorphous layers recrystallize by the solid-phase-epitaxial growth process, while the dislocation loops below the amorphous layers coarsen and evolve into a network of dislocations. The dislocations in this band getter fluorine and fluorine bubbles associated with dislocations are frequently observed. The secondary-ion mass spectrometry techniques were used to study concomitant boron and fluorine redistributions. The as-implanted Gaussian boron profile broadens as a function of time and temperature of annealing. However, the fluorine concentration peak is observed to be associated with dislocation band and the peak grows with increasing time and temperature of annealing. The electrical properties were investigated using Van der Pauw measurements. The electrical activation of better than 90% and good Hall mobility were observed in specimens with less than 500 Å dopant-profile broadening. In pulsed laser annealed specimens, the boron profile broadens both toward the surface and into the deeper regions of the crystal. However, the fluorine concentration profile exhibits a decrease in peak concentration with only a limited broadening.

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OAK RIDGE, TENNESSEE 37831

July 1984

Appendix IV

Rapid Thermal and Pulsed Laser Annealing of Boron Fluoride Implanted Silicon

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and J. J. Wortman

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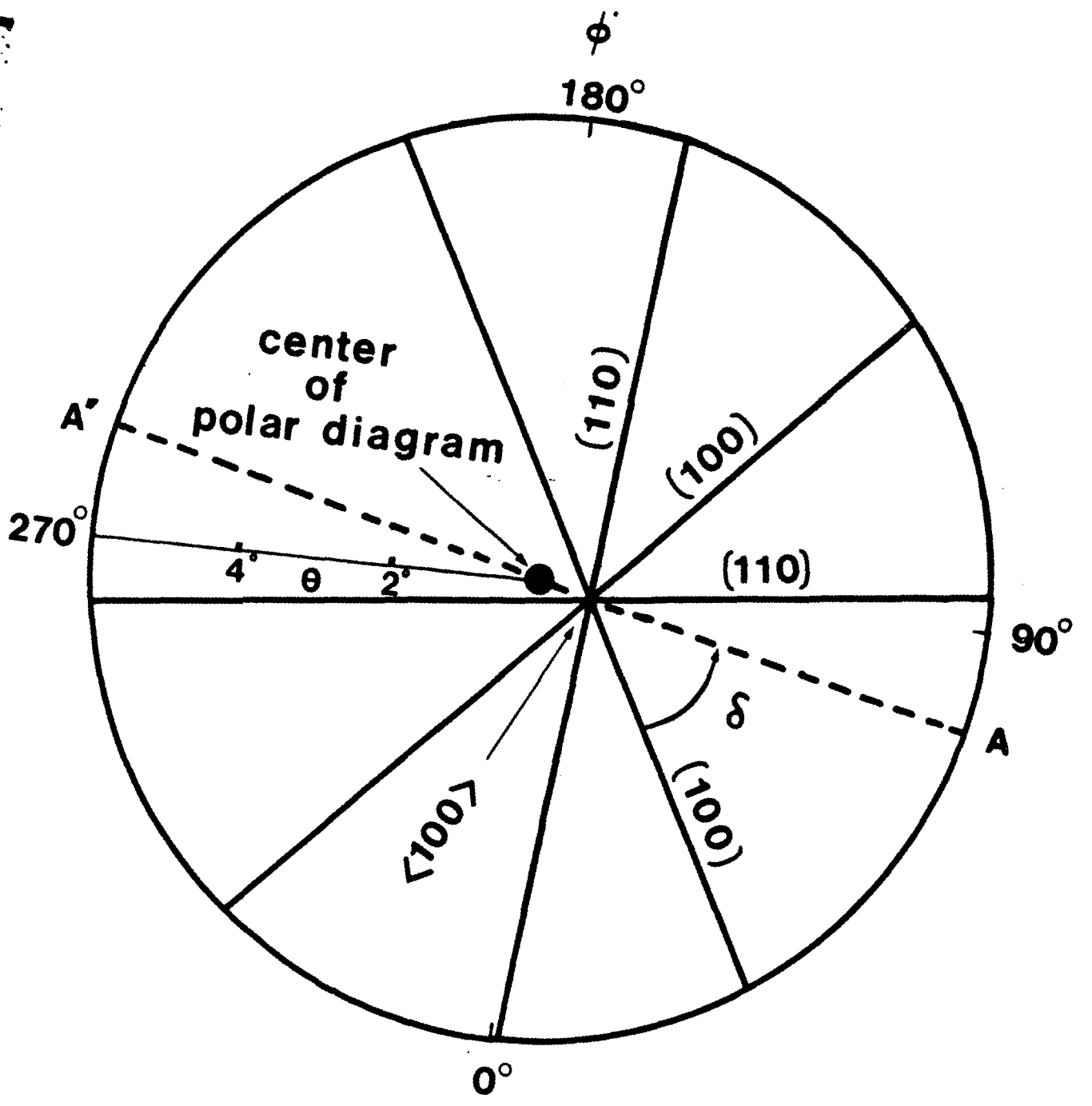
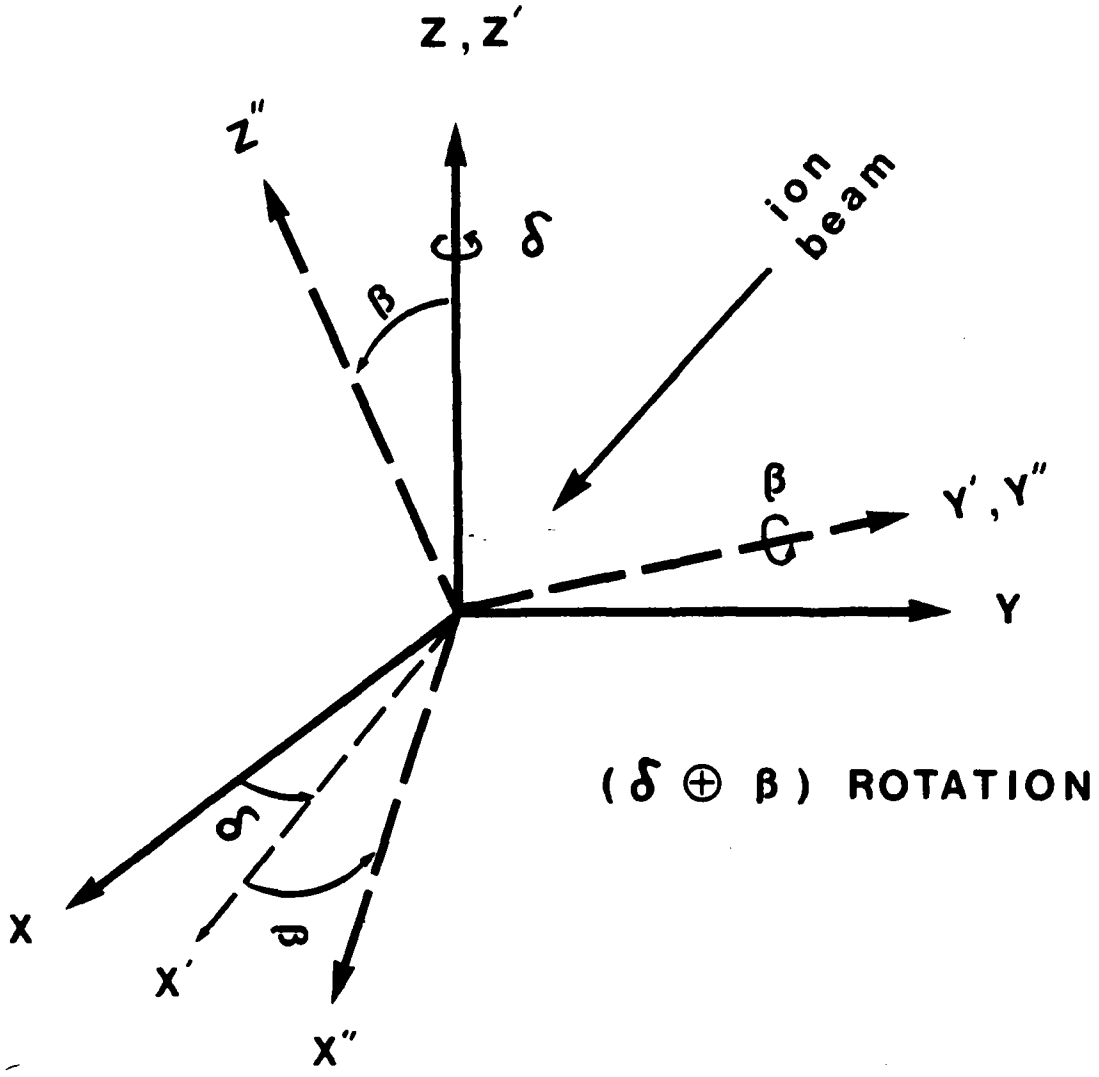

ϕ
180°
center
of
polar diagram
A'
270°
4°
θ
2°
(110)
(100)
(110)
90°
δ
A
⟨100⟩
(100)
0°

FIGURE 8



(X,Y,Z) ; Coordinates of crystal axes

(X",Y",Z") ; Coordinates of goniometer

FIGURE 7

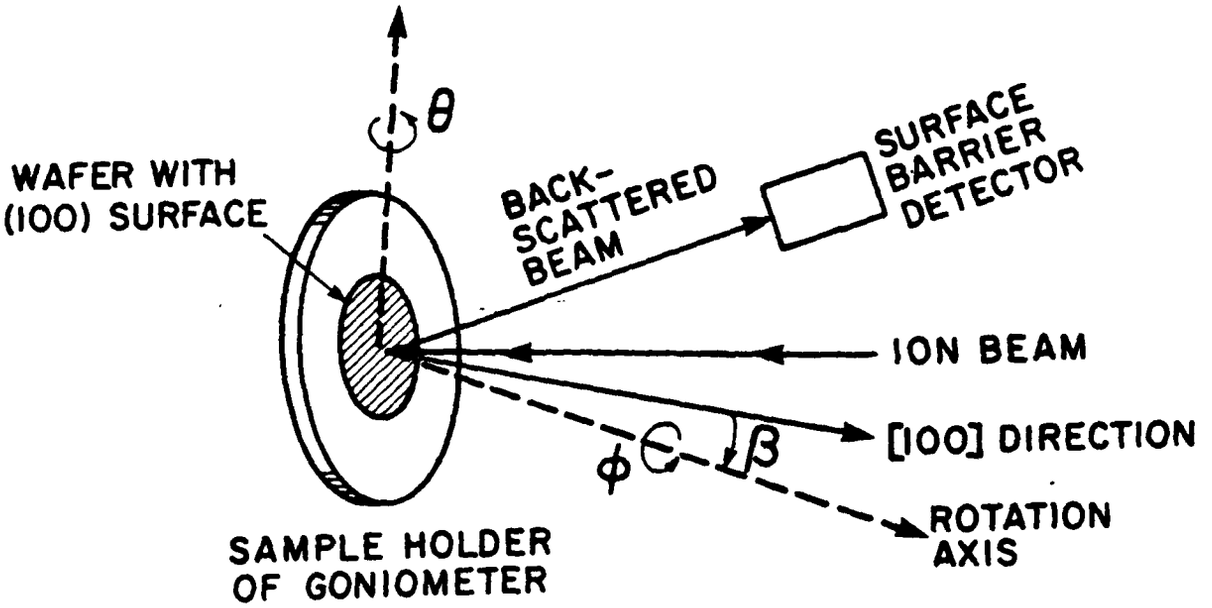

θ
WAFER WITH
(100) SURFACE
BACK-
SCATTERED
BEAM
SURFACE
BARRIER
DETECTOR
ION BEAM
[100] DIRECTION
φ
β
ROTATION
AXIS
SAMPLE HOLDER
OF GONIOMETER

FIGURE 6

implanted specimens. Using the 50 keV, 2.0 x 10^{16} cm^{-2} implant profile as a standard, the as-implanted fluorine concentration was estimated to be 1.0 x 10^{15} cm^{-2}. After 1.4, 1.6, and 3.6 J cm^{-2} laser pulses, the residual concentration of fluorine was determined to be 16, 11, and 5%, respectively. From boron concentration profiles, the depth of melting after 1.6 and 3.6 J cm^{-2} laser pulses was estimated to be 3000 and 7000 Å, respectively. It is interesting to note that the proximity of fluorine concentration peak to the surface leads to more efficient removal of fluorine from the laser annealed specimens.

Table I summarizes electrical properties (resistivity, mobility, and carrier concentration) obtained using Van der Pauw measurements. By RTA treatments up to 95% electrical activation with less than 500 Å dopant profile broadening can be obtained. The mobility is only slightly lower than that achieved by pulsed laser annealing. The pulsed laser annealing leads to 100% electrical activation of dopants. The presence of dislocations near the junction in the RTA samples adversely affects the electrical properties. However, such defects are removed by pulsed laser annealing leading to improved electrical properties.

DISCUSSION AND CONCLUDING REMARKS

During rapid thermal annealing, the amorphous layers anneal by a solid-phase-epitaxial growth process and the underlying dislocation bands either coarsen to form a cross-grid of dislocations or the isolated dislocation loops anneal by a bulk diffusion process. The interface kinetics during SPE growth can be expressed in terms of interface velocity $V = V_0 \exp^{-Ea/kT}$, where pre-expontential factor $V_0[100] = 2.5 \times 10^8$ Å s^{-1} is about 24 times

faster than $V_o[111]$, and 'E_{act}' is the activation energy of the order of 2.8 eV. Olson et al.[10] have measured SPE growth rates, using time-resolved reflectivity techniques, in boron and fluorine ion implanted amorphous layers and compared these results with self-ion implanted silicon specimens. In <100> specimens, V_o and E_a were determined to be 2.59 ± 0.05 eV and 5.35 x 10^8 cm s^{-1}, 3.06 ± 0.05 eV and 4.35 x 10^9 cm s^{-1}, and 2.68 ± 0.05 and 3.07 x 10^8 cm s^{-1}, in boron-, fluorine-, and silicon-ion implanted specimens, respectively. The presence of boron enhances the interface velocity, whereas fluorine decreases the SPE growth. At 550°C, the interface velocity in boron-doped samples was about six times faster than the intrinsic (self-ion implants) growth rate, whereas in fluorine-doped specimens the velocity was about 15 times slower than the intrinsic growth rate. At 1050°C, the interface velocity in boron-, fluorine-, and self-ion implanted specimens was found to be 7.3 x 10^{-2}, 2.2 x 10^{-3}, and 1.9 x 10^{-2} cm s^{-1}, respectively.[10] The SPE growth of a 1000 Å thick layer is completed within a few milliseconds. The remaining time of the order of a few seconds is utilized to remove trapped defects and fluorine in the SPE grown layers and dislocation loops in the underlying dislocation band.

The annealing behavior of dislocation loops in the underlying bands is critically determined by the average loop size and number density. If the separation between the two loops is less than the diameter of the larger loop, the two loops would coalesce. The continued coalescence of dislocation loops results in the formation of large loops and eventually a cross-grid of dislocations.

The boron distribution profiles have been studied as a function of annealing treatments. The observed boron profiles have been fitted using

numerical calculations with 'Dt_n' as a fitting parameter, where 'D' is the diffusion coefficient and 't_n' is a net time of annealing. The values of 't_n' were determined by requiring internal consistency in the amount of spreading and the diffusion coefficient at various temperatures of annealing. These calculations assumed initial Gaussian profile and allowed for spreading with various 'Dt_n' values. From the best fit, we extracted the value of activation energy for diffusion as 2.0 ± 0.2 eV, which is about a factor of two lower than the value for boron in silicon under equilibrium diffusion conditions (3.5 eV).[11] A similar decrease in activation energy was observed in Sb^+ implanted and SPE grown specimens of silicon during subsequent furnace annealing.[12] The lower activation energy is responsible for enhancement in diffusivity during rapid thermal annealing. The enhancement cannot be due to the increased concentration of dopants[13] because it should not reduce the activation energy. Moreover, in the above concentration range, the enhancement in diffusivity is estimated to be less than a factor of 5.[13] It is interesting to note that the diffusion enhancement factor in boron-implanted specimens (where there is no amorphous layer) is about an order of magnitude less, indicating the role of trapped defects in the SPE grown layers.

The dislocations in the underlying bands provide effective gettering agents for fluorine in BF_2^+ implanted and furnace-annealed silicon specimens. Previous studies had indicated the segregation peaks near the damaged regions.[14] The association of fluorine with the dislocations is clearly demonstrated by TEM results that are consistent with SIMS studies. The dislocations, via electronic and elastic interactions, attract fluorine and

provide a convenient lattice site. A continued segregation leads to clustering and void formation. Fluorine is known to attach itself to unsatisfied bonds of silicon and thus reduce the number of dangling bands. This characteristic of fluorine reduces the electrical activation of dislocations. As a result, the dislocations do not act as effective trapping and recombination centers and do not produce deterimental effects on carrier concentration and mobility. Fluorine concentration in laser annealed specimens decreases while the peak shifts toward the surface. These results of present studies are consistent with earlier results.[15] The peak shift toward the surface is probably related to the segregation coefficient of fluorine in the liquid during solidification.

It was found to be most interesting that while boron concentration profile spreads into the deeper regions of the crystal, the fluorine concentration profile does not spread and it moves toward the surface in laser annealed specimens. The fluorine tends to diffuse out of the heated or molten layer of silicon. The results presented in this paper show that amorphous layers created by BF_2^+ implants can be annealed by SPE growth. The interstitials below the amorphous layers cluster to form large dislocation loops and tangles that getter fluorine. The boron is electrically activated despite the presence of fluorine. The electrical properties of RTA annealed semiconductor layers are found to be much superior to those conventionally furnace-annealed specimens. The broadening of dopant profiles can be precisely controlled within 500 Å, while achieving superior electrical properties. The dislocation tangles below the original amorphous layer can be removed by pulsed laser melting below the defective

amorphous layer can be removed by pulsed laser melting below the defective region. In this case crystal growth occurs in liquid-phase in such a way that the underlying defect-free substrate acts as a seed for crystal growth.

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TABLE I. Electrical properties of rapid thermally annealed and pulsed laser annealed specimens.

Implanted (cm^{-2}) Dose	Carrier Concentration, N_c	Hall Mobility μ_H	Resistivity (ρ)	Rapid Thermal Annealing Treatment
3.0×10^{15}	2.8×10^{15}	31.0	47.9	1050°C/15T*
3.0×10^{15} LN_2 Implants	2.1×10^{15}	41.0	48.6	1050°C/10T
3.0×10^{15}	2.0×10^{15}	42.0	50.3	1050°C/10T
3.0×10^{15} RT Implants	2.1×10^{15}	40.0	49.5	1050°C/15T
3.0×10^{15}	3.0×10^{15}	34.0	40.0	Pulsed Laser Annealed 1.4 J cm^{-2} (λ = 0.308 μm, τ = 50 ns)

*'T' refers to total time of current flow in the graphite strip heater.[9]

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FIGURE CAPTIONS

Fig. 1. Damage energy deposited as a function of depth for 11 keV $^{11}B^+$ and 19 keV $^{19}F^+$ ions.

Fig. 2. Cross-section TEM micrographs from (100) Si specimens: (a) as-implanted 50 keV BF_2^+ ions, dose = 1.0×10^{14} cm^{-2}; (b) after annealing at 1050°C for 5 seconds; and (c) after annealing at 1100°C for 10 seconds.

Fig. 3. Cross-section TEM micrographs from (100) Si specimens: (a) as-implanted 50 keV BF_2^+ ions, dose 6.0×10^{14} cm^{-2}; (b) after 1000°C/10s annealing treatment; and (c) 1050°C/5s annealing treatment.

Fig. 4. Cross-section TEM micrographs from (100) Si specimens: (a) as-implanted 50 keV BF_2^+ ions, dose 1.0×10^{15} cm^{-2}; (b) after 1000°C/10s; and (c) 1100°C/3s annealing treatments.

Fig. 5. Plan-view TEM micrograph from the specimen show in Fig. 4(c). The presence of fluorine bubbles at the dislocations is clearly deliniated (for example, see bubble indicated by the arrow).

Fig. 6. Boron concentration profiles before and after RTA treatments in specimens implanted with 6.0×10^{14} cm^{-2} BF_2^+ ions.

Fig. 7. Fluorine concentration profiles before and after RTA treatments in specimens implanted with 6.0×10^{14} cm^{-2} BF_2^+ ions. The fluorine peak in the annealed specimens corresponds to the band of dislocations shown in Fig. 3.

Figure Captions (Contd.)

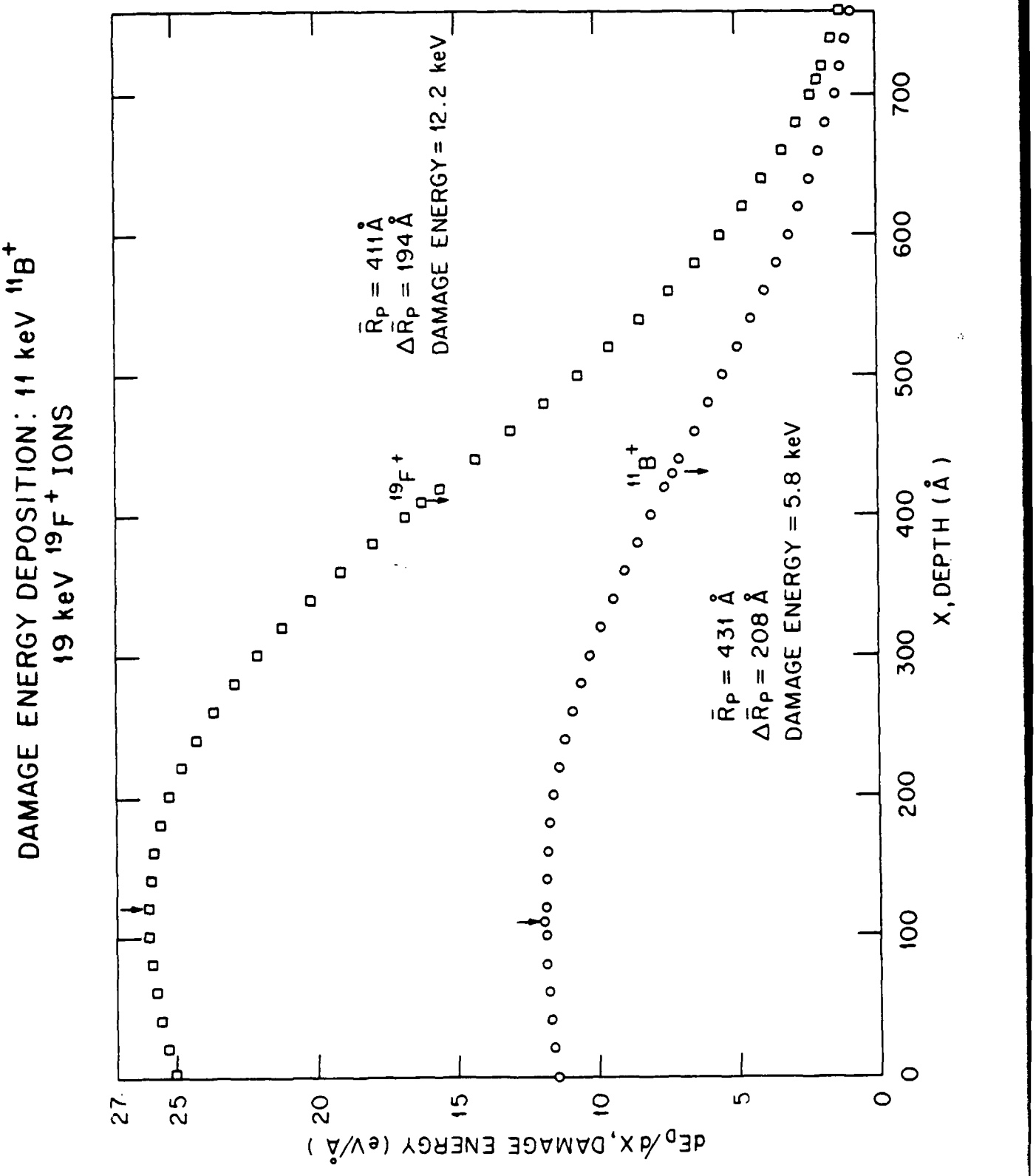
Fig. 8. Boron concentration profiles before and after RTA treatments in specimens implanted with 1.0×10^{15} cm^{-2} BF_2^+ ions.

Fig. 9. Fluorine concentration profiles before and after RTA treatments in specimens implanted with 1.0×10^{15} cm^{-2} BF_2^+ ions. The fluorine peak in the annealed specimens corresponds to the band of dislocations shown in Fig. 4.

Fig. 10. Boron concentration profiles before and after pulsed laser (λ = 0.308 μm, τ = 50 ns) annealing.

Fig. 11. Fluorine concentration profile before and after pulsed laser annealing from companion specimens of Fig. 10.

Fig. 12. Fluorine concentration profiles from glow-discharge (1 kV, dc) primarily BF_3^+ implanted specimens before and after pulsed laser (λ = 0.308 μm, τ = 50 ns) annealing. The profile from 2×10^{16} F^+ cm^{-2} ($\sim$50 kV, 1.0×10^{16} BF_2^+ cm^{-2}) specimens was used as a standard to calculate the fluorine concentrations in glow-discharge implants.


DAMAGE ENERGY DEPOSITION: 11 keV $^{11}B^+$
19 keV $^{19}F^+$ IONS
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$\Delta\bar{R}_p$ = 194 Å
DAMAGE ENERGY = 12.2 keV
$^{19}F^+$
$^{11}B^+$
$\bar{R}_p$ = 431 Å
$\Delta\bar{R}_p$ = 208 Å
DAMAGE ENERGY = 5.8 keV
dE_D/dx, DAMAGE ENERGY (eV/Å)
X, DEPTH (Å)
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5
10
15
20
25
27
0
100
200
300
400
500
600
700

Fig. 1

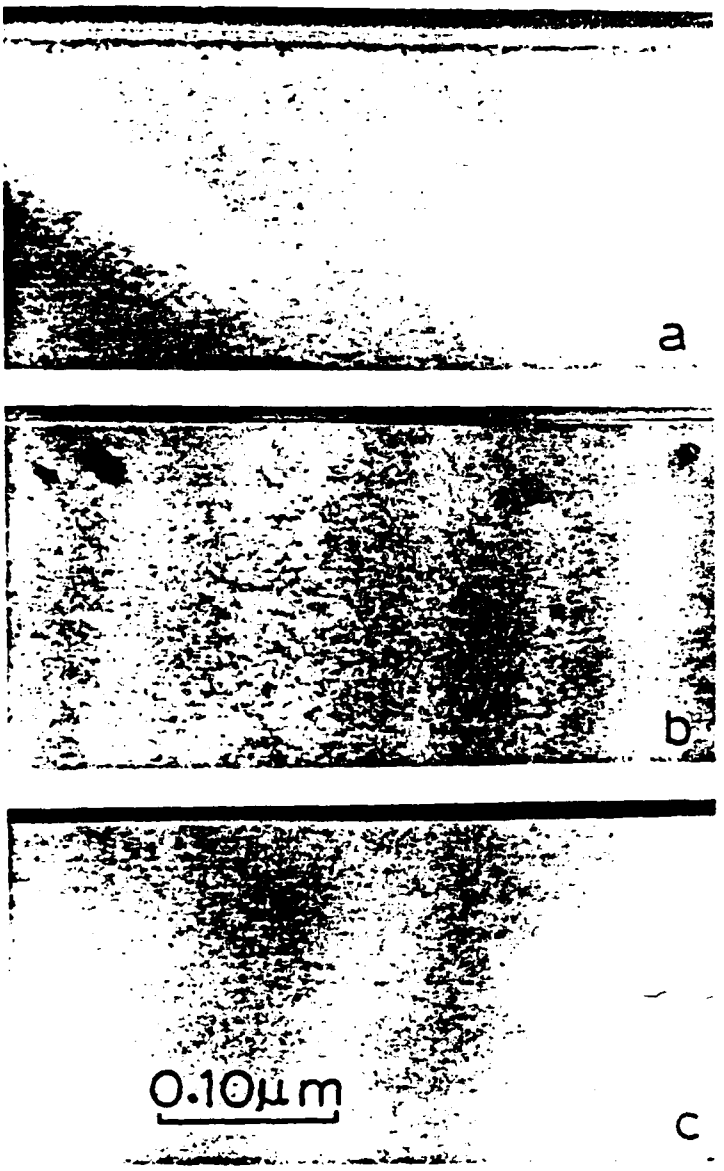


Fig. 2

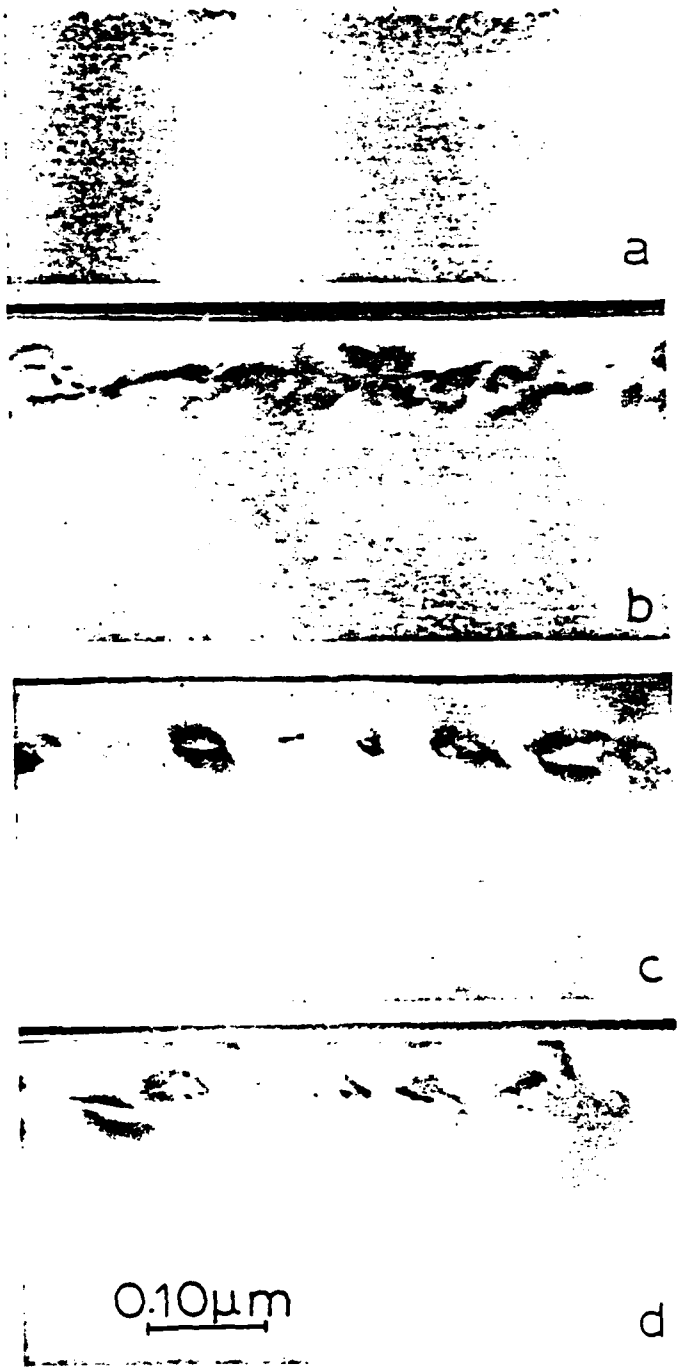


Fig. 3

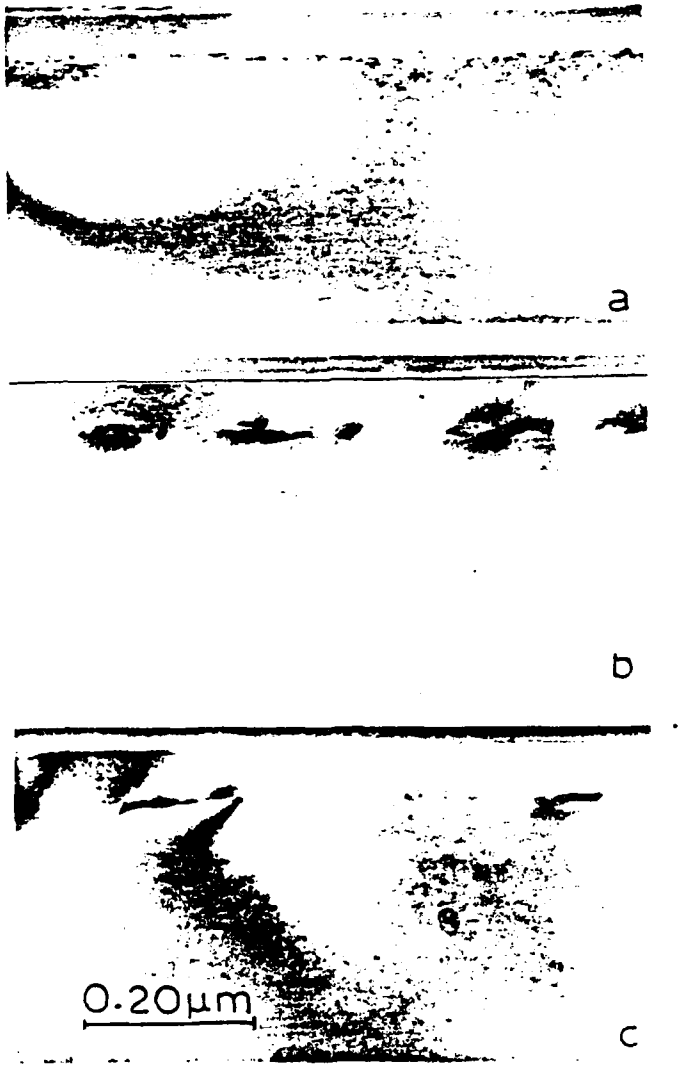
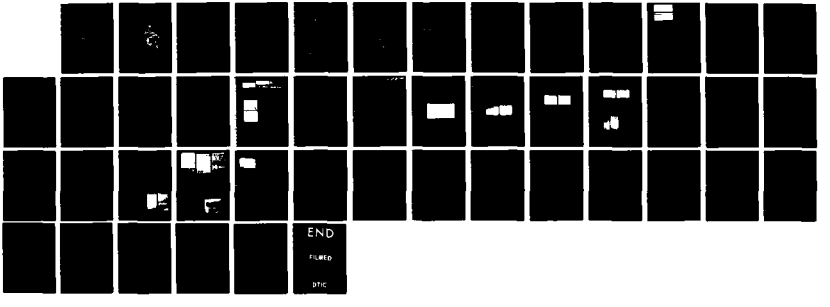


Fig. 4

AD-A157 141 HIGH FREQUENCY SILICON BIPOLAR TRANSISTOR WITH SIPOS (SEMI-INSULATING POL..(U) NORTH CAROLINA STATE UNIV AT RALEIGH DEPT OF ELECTRICAL AND C.. J J WORTMAN ET AL. 2/2

UNCLASSIFIED MAR 85 N00014-82-K-0468 F/G 9/1 NL



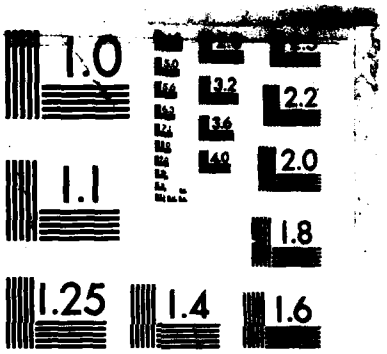
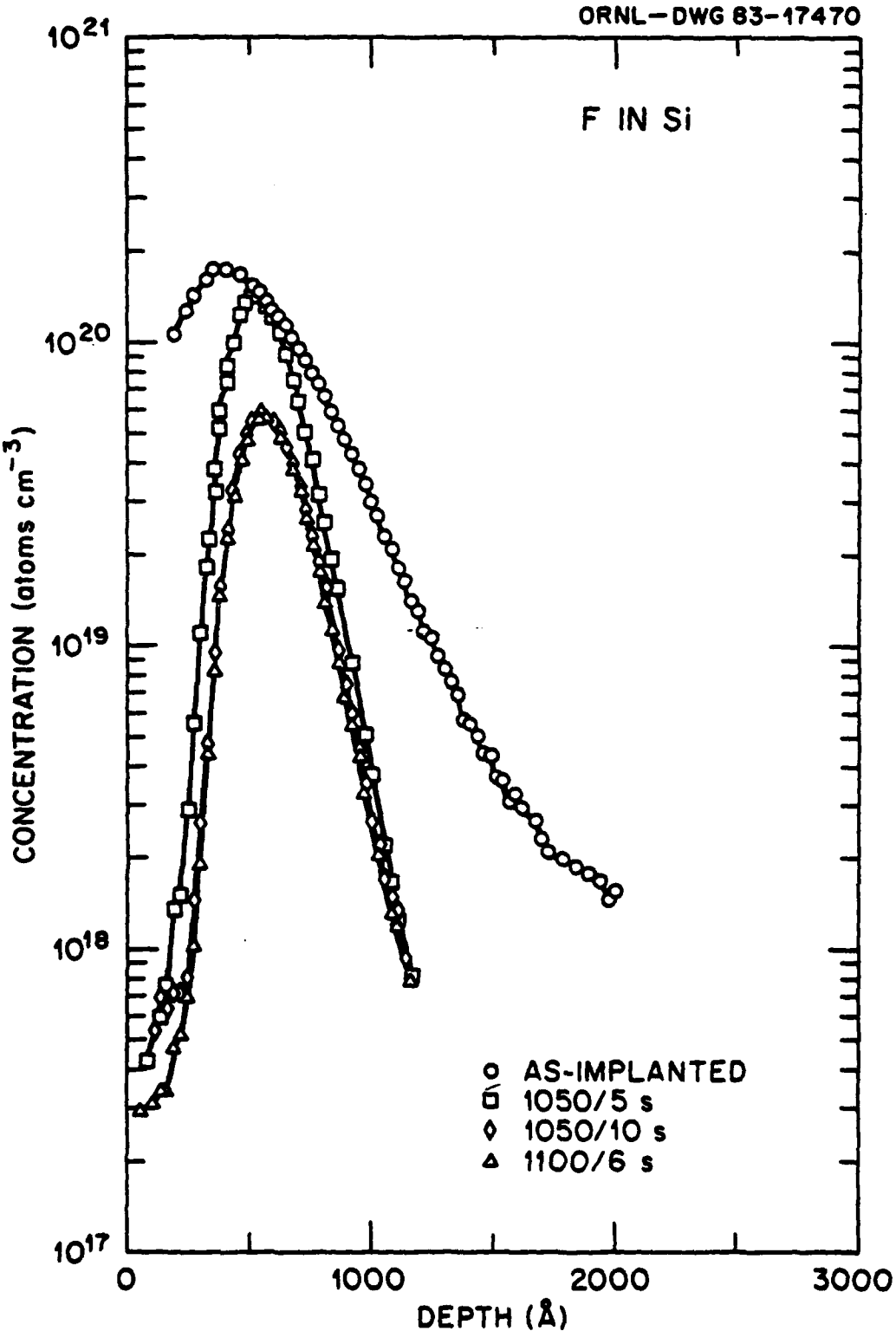


Fig. 5


ORNL—DWG 83-17470
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10^{20}
10^{19}
10^{18}
10^{17}
CONCENTRATION (atoms cm^{-3})
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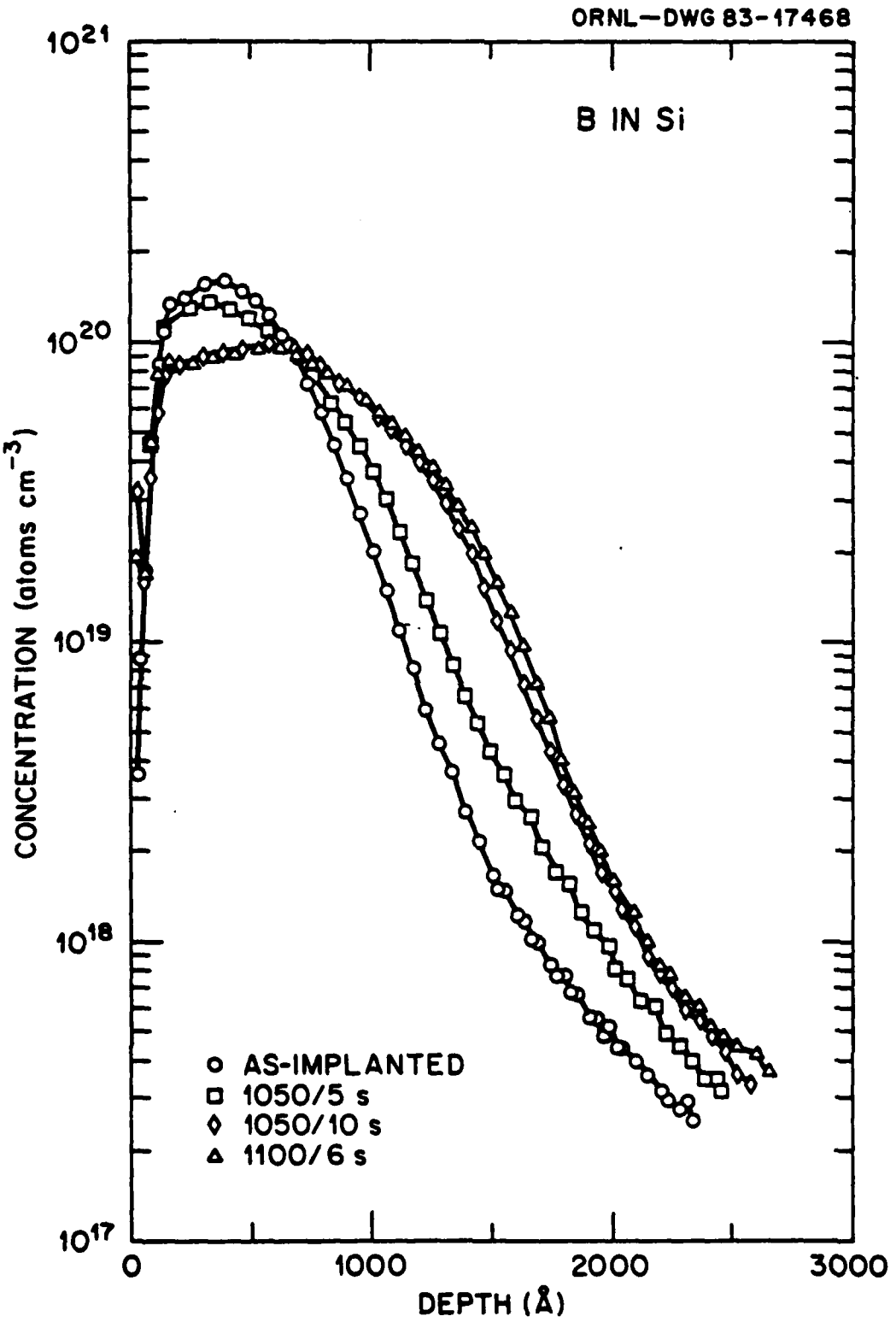
1000
2000
3000
DEPTH (Å)
AS-IMPLANTED
1050/5 s
1050/10 s
1100/6 s

Fig. 7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10^{18}
10^{17}
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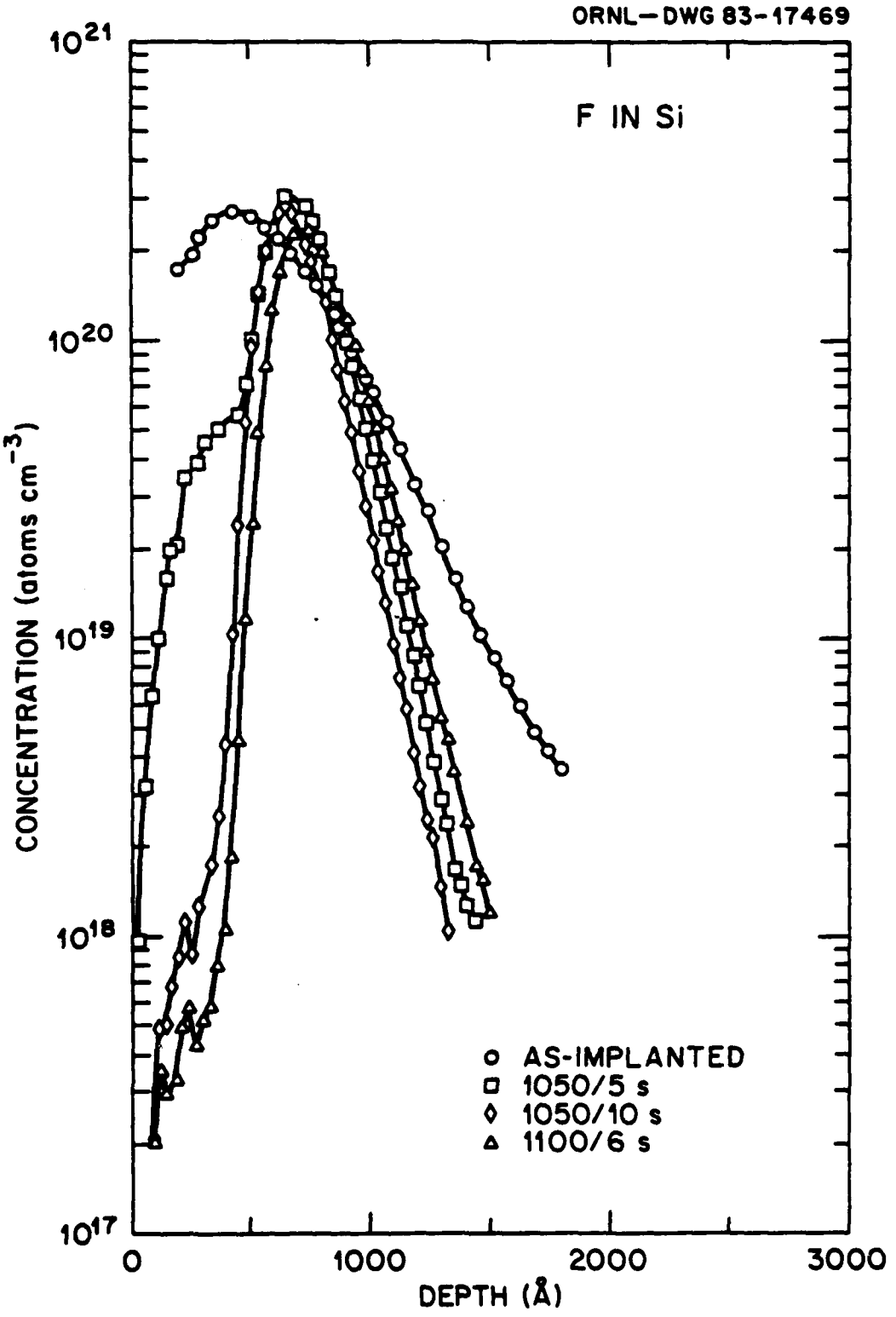
3000
DEPTH (Å)
AS-IMPLANTED
1050/5 s
1050/10 s
1100/6 s

Fig. 8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10^{20}
10^{19}
10^{18}
10^{17}
0
1000
2000
3000
DEPTH (Å)
AS-IMPLANTED
1050/5 s
1050/10 s
1100/6 s

Fig. 9

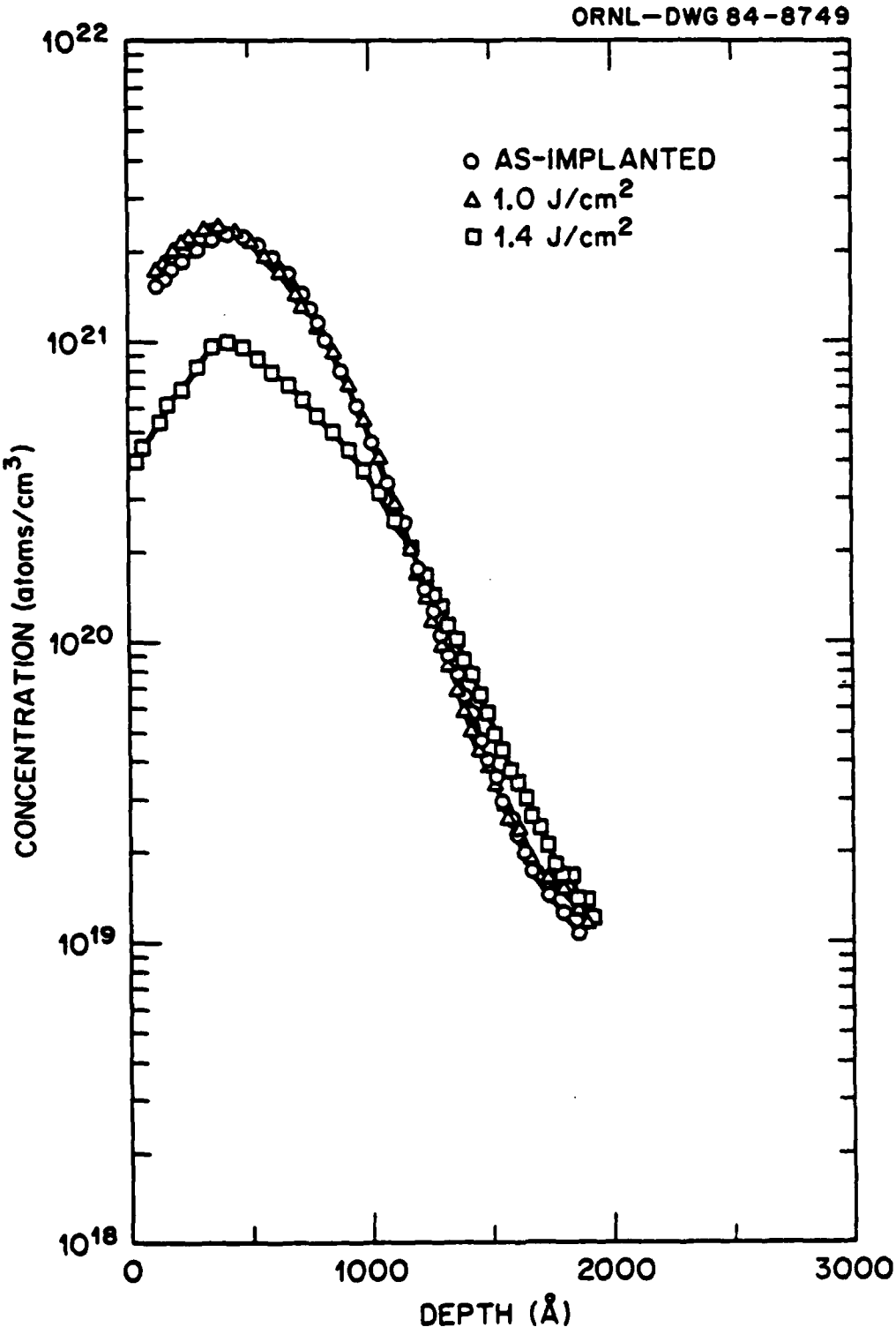
ORNL—DWG 84-8749
10^{22}
10^{21}
10^{20}
10^{19}
10^{18}
CONCENTRATION (atoms/cm^3)
o AS-IMPLANTED
Δ 1.0 J/cm^2
□ 1.4 J/cm^2
0
1000
2000
3000
DEPTH (Å)

Fig. 10

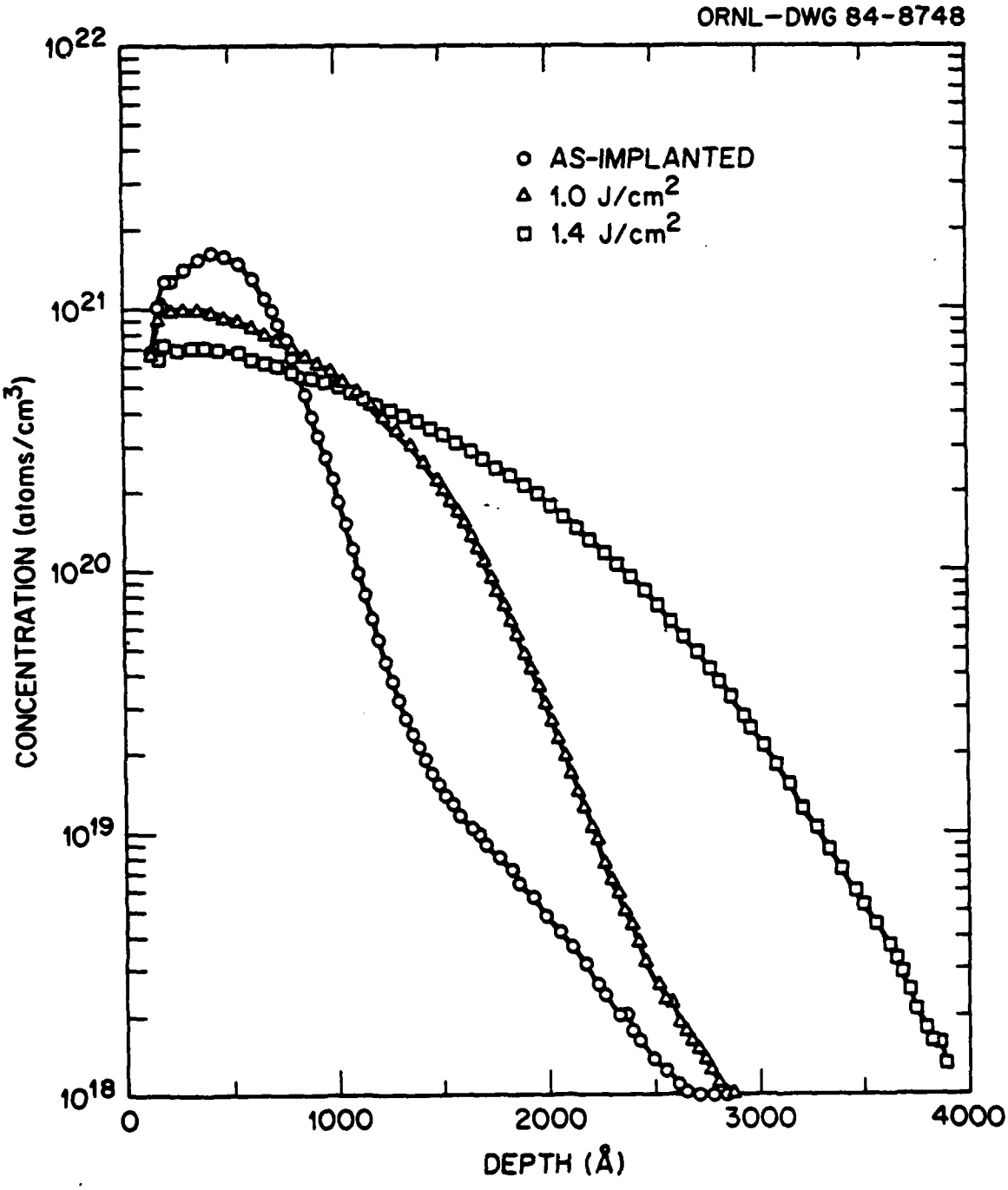
ORNL-DWG 84-8748
AS-IMPLANTED
1.0 J/cm2
1.4 J/cm2
CONCENTRATION (atoms/cm3)
DEPTH (Å)
10^22
10^21
10^20
10^19
10^18
0
1000
2000
3000
4000

Fig. 11

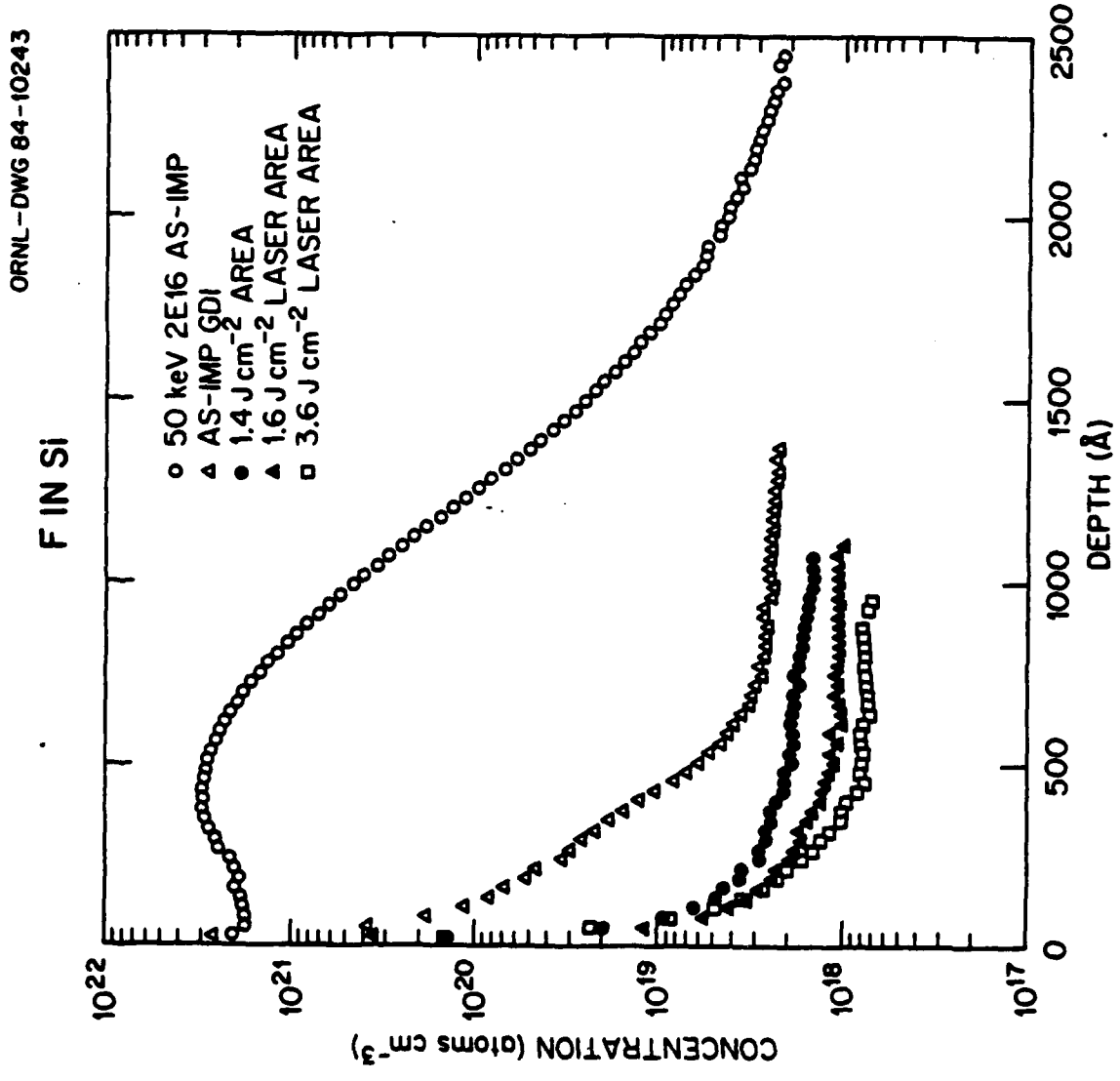
ORNL-DWG 84-10243
F IN Si
o 50 keV 2E16 AS-IMP
Δ AS-IMP GDI
● 1.4 J cm^{-2} AREA
▲ 1.6 J cm^{-2} LASER AREA
□ 3.6 J cm^{-2} LASER AREA
CONCENTRATION (atoms cm^{-3})
10^{22}
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
0
500
1000
1500
2000
2500
DEPTH (Å)

Fig. 12

Appendix V

Electrical, Structural and Chemical Analysis Of p-n Junctions Formed By BF_2 Implantation and Rapid Thermal Annealing

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and G. A. Rozgonyi

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Cincinnati, May 1984.

*Work sponsored by ONR

Electrical, Structural and Chemical Analysis of p-n Junctions Formed by BF_2 Implantation and Rapid Thermal Annealing *

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Diodes have been fabricated to study the electrical properties of p-n junctions formed using rapid thermal annealing (RTA) procedures. The starting material was 10-20 ohm-cm, CZ, n-type (100) silicon. The junctions were formed by implanting BF_2 at 50 keV to a dose of 10^{14} cm^{-2}. Following the implant, the samples were either annealed by RTA at 1000°C for 10 seconds, or furnace pre-annealed at 550°C for 30 minutes followed by the same RTA cycle. Figure 1 is a graph of the sheet resistance as a function of RTA temperature (all for 10 seconds) as measured by a four point probe. As can be seen in Fig. 1, an RTA temperature of 950°C for 10 seconds is sufficient to almost fully activate (>95%) the implanted boron. The junction leakage current was found to be highly dependent on the RTA temperature. Figure 2 is a plot of the leakage current as a function of temperature. As shown in Fig. 2, the reverse leakage current is lower for the lower anneal temperatures (950°C). This was not expected since the higher temperatures (~1100°C) are needed to anneal out extended defects. A pre-anneal of 550°C for 30 minutes before RTA was found to significantly enhance the junction properties for all RTA temperatures above 950°C as shown in Fig. 2.

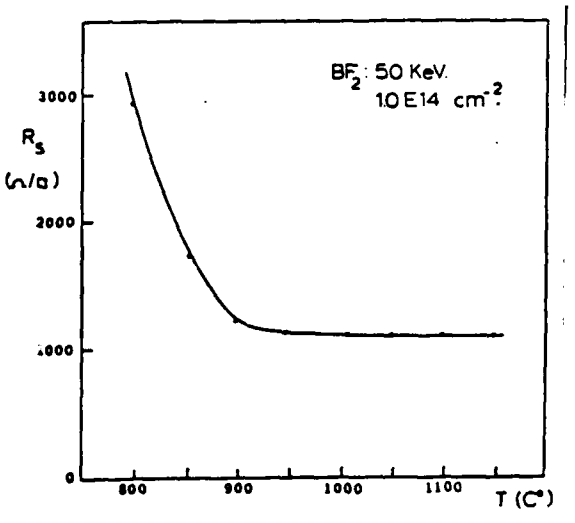

Fig. 1: Sheet resistance as a function of RTA temperature for a 10 second anneal.

Cross-sectional transmission electron microscopy (XTEM) of the unannealed sample did not show any visible damage (Fig. not included) in the entire implanted region, indicating that individual damage zones were dynamically annealed during implantation. The XTEM results from direct RTA and 550°C furnace plus RTA are shown in Fig. 3. Although both samples showed a layer of scattered dislocation loops (250A diameter) below the surface, there were subtle differences in the nature and distribution of secondary defects in the two cases. For example, the directly annealed sample showed loops located at a mean depth of ~1100A, whereas in the two step annealed sample, the loops were within 650A from the surface. Furthermore, a band of small clusters was also superimposed in the depth range 0-1000A over the loops in the latter case. The band of small clusters (without loops) was also observed in the 550°C/30 minute annealed sample (not shown). The SIMS profiles of B before and after RTA are shown in Fig. 4a. The enhanced diffusion of B observed in the RTA case is typically associated with the transient point defects flux available during such a short process.

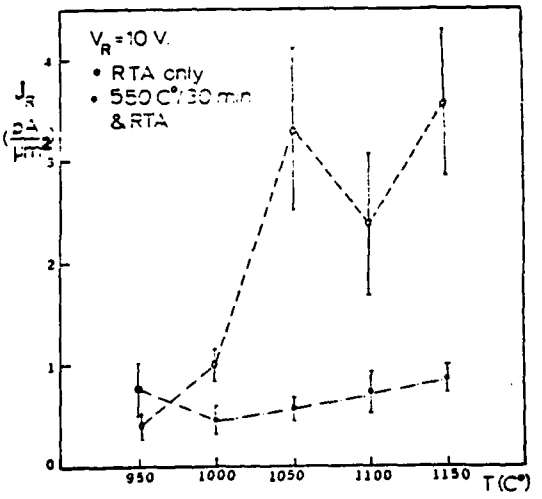

Fig. 2: Leakage current as a function of RTA temperature for directly annealed and two step annealed samples.

Correlation between the electrical measurements such as the leakage current in Fig. 2 and XTEM does not appear to be straightforward. For example, in the direct RTA sample, the sheet resistance data indicate the 98% of B is electrically active and the XTEM results show fewer defects in the implanted region as compared with the two step annealed sample. However, the leakage current data is not consistent with the XTEM results. It may be that F is playing a role in the leakage current measurements. In the two step annealed samples, perhaps the fine clusters represent trapped F, whereas in the direct RTA sample, such trapping does not occur. Further work is underway to obtain depth profiles of F and electrical carriers in the two cases.

* Work sponsored by Office of Naval Research

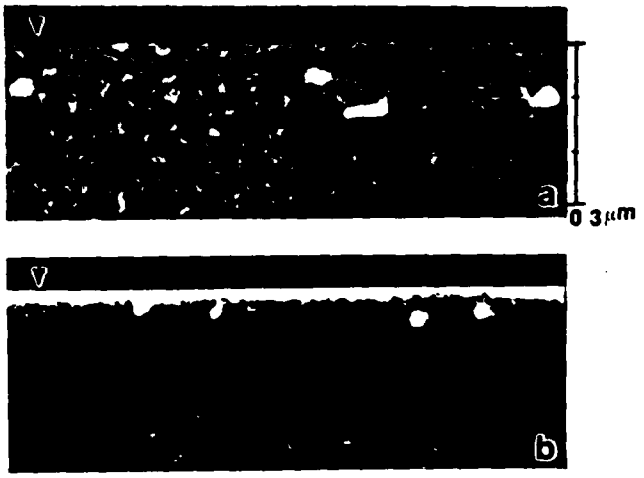

Fig. 3: XTEM weak-beam micrographs showing damage distributions in (a) direct RTA and (b) 550°C furnace plus RTA samples. Note dislocation loops in (b) are closer to the surface than (a). Arrow points to the sample surface.

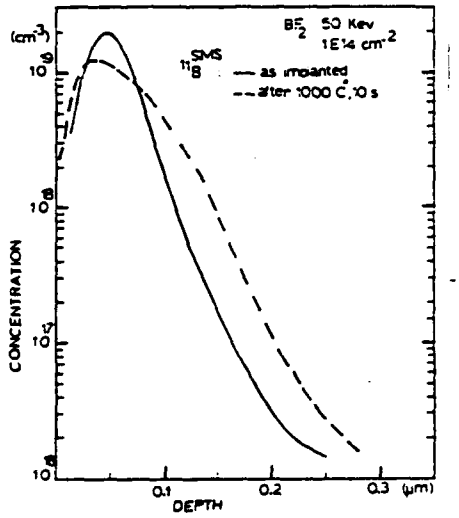

Fig. 4: Boron concentration as a function of depth before and after RTA.

Appendix VI

Electrical Properties of Implanted and Rapid Thermal Annealed Shallow p^+-n Junctions

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rical properties of implanted and rapid thermal annealed shallow p^+-n ions-

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The electrical properties of shallow junctions fabricated using a 50-keV BF_2 ion implantation into ⟨100⟩ n-Si followed by rapid thermal annealing (RTA) have been investigated. The junction depth was 0.25 μm. Sheet resistance measurements have shown that annealing at 950 °C for only 10 s results in approximately 90% electrical activation. In addition this annealing cycle gives the optimum leakage current. The leakage current density obtained was 1 fA/μm^2 (at 10-V reverse bias voltage, for 2–4-Ω cm n-type substrate). The results indicate that RTA can be used to obtain reproducible shallow junctions without significantly changing the implanted profile.

rinkage in physical dimensions of semiconductor de- equires that shallow electrical junctions be realized. gh low-energy implants can be used to obtain a de- unction depth, dopant redistribution during a conven- urnace annealing (900–950 °C, 30–60 min) is a severe ion to obtaining shallow junctions. A very promising chnique to overcome this difficulty is rapid thermal ing (RTA). Previous studies have been reported which nvestigated residual structural damage (dislocation) aterial properties of implanted and rapid thermal an- silicon.[1,2]

hese studies using secondary ion mass spectrometry), Rutherford backscattering channeling, transmis- ectron microscopy (TEM), and lap and stain measure- echniques have shown that defect-free (within the re- n of these instruments and techniques) fully activated, allized layers can be obtained by RTA of implanted Si it significant diffusion of the dopant profile. In this he electrical characteristics of BF_2 implanted and rap- mal annealed silicon have been investigated and the lity of this technique for future devices is analyzed he point of view of electrical performances.

he system used for RTA in this work was a Heatpulse tungsten halogen lamp heated system.[3] The annealing rature/time and the heating/cooling rates are com- controlled.

iodes were fabricated to evaluate the electrical prop- of the RTA junctions. Sheet resistance measurements ade on wafers processed in the same batch. Different temperatures and heating/cooling rates were studied ide a comparison of the variables of RTA. The recrys- ion rate of Silicon is known to be very fast at the tem- re used for activation (i.e., on the order of millisec- The possibility of obtaining a better junction with a e annealing precrystallization step at lower tempera- round 500 °C) for long times (30–60 min) followed by o activate the implanted dopants was also investigat-

n outline of the diode process is given in the following. The wafers used are ⟨100⟩ 2–4-Ω cm CZ n-type silicon. The wafers were first cleaned using an RCA clean, followed by a field oxidation in steam O_2 for 30 min at 1100 °C, to obtain 450–460 nm of oxide. The first photolithographic step was applied to open the junction windows. Then the wafers were implanted with BF_2, with implant parameters of 50-keV energy at a dose of 10^{14} cm^{-2}. The wafers were given an RCA cleaning step and then annealed. The parameters of the annealing step are shown in Table I. Aluminum was used to provide electrical contact, which was patterned with a second photolithographic step and then sintered for 10 min at 450 °C in 6% H_2-94% N_2 ambient. Junction depth was 0.25 μm. The junctions were rectangular with a total area of 1250 μm^2.

The sheet resistance was measured with a four-point probe. The leakage current was measured with a HP 4145 A semiconductor parameter analyzer at a reverse bias of 10 V.

The change in doping profile of implanted layers after RTA is shown in Fig. 1. Secondary ion mass spectrometry (SIMS) measurements have indicated an average displacement of the doping profile around 30 nm and the junction depth is still less than 0.3 μm. A typical variation of sheet resistance with the RTA temperature is shown in Fig. 2. It can be seen that the sheet resistance increases for annealing temperatures less than 900 °C. Although not shown in Fig. 2, it was also observed that the recrystallization at 550 °C had no effect on the variation of sheet resistance with annealing temperature.

TABLE I. RTA parameters.

RTA time (s)	RTA temperature (°C) 950	1000	1050	1100	1150
10	S, F	S, F	S, F	S, F	S, F
15	S, F	S, F	S, F	S, F	S, F

S: Slow heating/cooling rate (5% s^{-1} of final intensity).
F: Fast heating/cooling rate (15% s^{-1} of final intensity).

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pipe diffused quantity, the value of D_d will become somewhat smaller than estimated. The discrepancy becomes more significant when samples with lower dislocation density are considered in such an estimate.

CONCLUSIONS

Whether it is routine dopant implantation (in the case of heavy ions) or doping preceeded by a preamorphization process, the resulting amorphous layer can potentially contain nuclei at its interface with crystalline zones which would initiate the growth of hairpin dislocation during subsequent annealing process. Misoriented small crystallites present in a/c transition region have been identified as the nuclei. Roughness of this region due to ion straggling determines the density of hairpins with more nonuniformity leading to a higher density. Dynamic annealing occurring due to ion beam heating causes coarsening and broadening of the transition region thus contributing to a further increase of the hairpin density. Post-implantation, low temperature annealing or beam heating of the a/c interface by a secondary, shallower implantation process can also induce increase of the density. A pipe diffusion of doping ions along the dislocations occurs at a highly accelerated rate and can cause a significant shift of the dopant concentration profile toward the bulk of the sample. The pipe diffusion coefficient, D_d, for boron diffusion along hairpin dislocation was evaluated to be about 10^4 times higher than its bulk value, D_v, at 1150°C.

ACKNOWLEDGMENTS

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Where: D_v = bulk diffusion coefficient, D_{eff} = effective diffusion coefficient for the sample with high concentration of dislocations, ΔR_p = straggling of implanted ion distribution. We can safely neglect dislocation density of the first sample ($N_d<10^3$) and consider its $D=D_v$. For $Q=0.01$ and $\Delta R_p=0.019$ μm (BF_2 implant energy was 42 keV, 9.5 keV of which is shared by boron) $D_v/D_{eff}=0.52$. Measurement at $Q=0.001$ produced a result within 2% of the previous one.

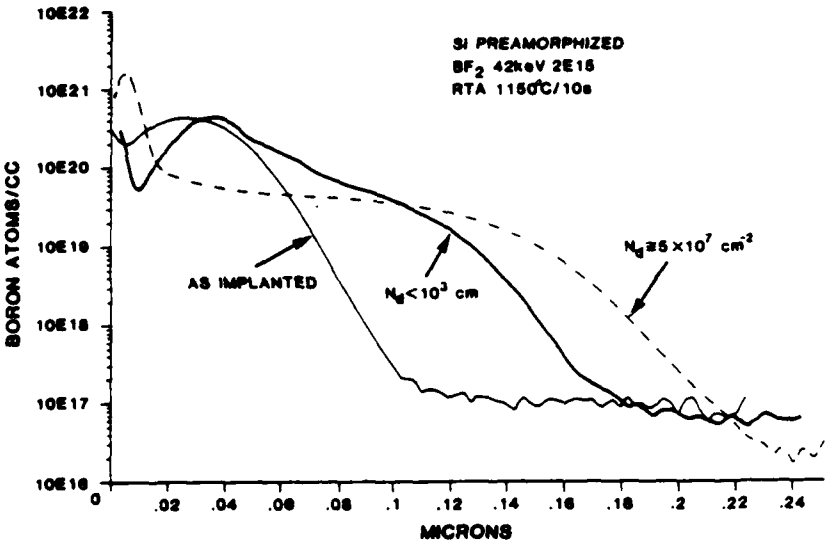


Fig. 7. SIMS profiles of B in Si^+ preamorphized, BF_2 implanted, RTA 1150°C/10s annealed samples showing different densities of hairpin dislocations.

Assuming that the diffusion coefficient for pipe diffusion, D_d, is much greater than bulk diffusion coefficient, D_v, we can neglect any flux of ions taking place beside the dislocation pipes. Therefore, it can be concluded from Fick's first law for directional flow of the point defects that the effective diffusion coefficient, D_{eff}, as calculated from a concentration profile (SIMS measurement represents average concentration over 250 x 250 μm raster area) is related to the actual pipe diffusion coefficient as follows:

$$D_d = D_{eff}A/A_d$$

Where: A = unit area perpendicular to the flux (here assumed equal to 1 cm^2), A_{eff} = cross section area of all pipes crossing the unit area. The value of the radius of dislocation pipe was assumed to be r_o = .01 μm after ref. [20]. It is also assumed that the dislocations are perpendicular to the sample surface (actual angle between the hairpin arm and the surface was evaluated in TEM studies to be about 70°). Since the hairpin consists of two arms, the total concentration of dislocation pipes is $N_d=5 \times 10^7 cm^{-2}$ and $A_d=N_d\pi r_o^2$, hence $D_d=6.4 \times 10^{-3}$ $D_{eff}=1.2 \times 10^4 D_v$. This result is, of course, only approximate and if, contrary to our assumption, the mass transported through bulk diffusion process is not totally negligible with respect to the

Based upon these observations the following model for nucleation of hairpin dislocation is proposed (Fig. 6). During RTA, the advancing and recrystallizing a/c growth front intersects a small misoriented crystallite in the a/c transition region. A perfect dislocation segment is formed at the intersection to accommodate the misorientation. As the combined growth front continues to move, the dislocation segment wraps around the misoriented material to form a half loop. As the annealing continues, the hairpin arms diverge since the growth front protrusion of misoriented material is spreading laterally as well as vertically. During further annealing the dislocation shortens its length by moving toward the surface along the glide cylinder defined by the inclined Burgers vector and line direction. The model clearly implies that the density of hairpins is related to availability of the misoriented crystallites within a/c transition region, i.e., the narrower and sharper the region, the lesser are the chances for hairpin nucleation.

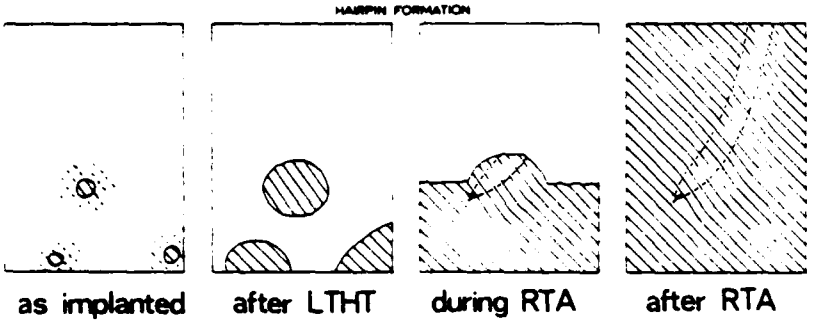


Fig. 6. Schematic diagram illustrating model for hairpin nucleation during RTA (see text for description). The hairpin is shown in almost edge-on orientation.

PIPE DIFFUSION ALONG HAIRPINS

Two Si^+ preamorphized samples with identical BF_2 implants, which were found to have significantly different densities of hairpins, have been used for boron concentration profile examination in secondary ion mass spectroscopy (SIMS). The densities N_d were $<10^3$ and about $2.5 \times 10^7 cm^{-2}$. A boron SIMS profile of the sample with a higher density of hairpins, annealed via RTA at 1150°C for 10 seconds, shows a significant shift toward the bulk with respect to the profile of the other sample (Fig. 7). We attribute this shift to the enhanced diffusion along the defects. An approximate evaluation of diffusion coefficient, D_d, of boron along hairpins based upon preliminary experimental results is given below.

Following derivations by Sedgwick et al. [18] and Seidel and MacRae [19] for assumed Gaussian dopant density the ratio of diffusion coefficients of two samples annealed in identical conditions can be expressed in terms of profile shifts Δx_1, Δx_2 between the as implanted and annealed profiles for each sample at some fraction, Q, of the peak concentration:

$$\frac{D_v}{D_{eff}} = \frac{\Delta x_1^2 + 2\Delta x_1 \Delta R_p (2\ln 1/Q)^{1/2}}{\Delta x_2^2 + 2\Delta x_2 \Delta R_p (2\ln 1/Q)^{1/2}}$$

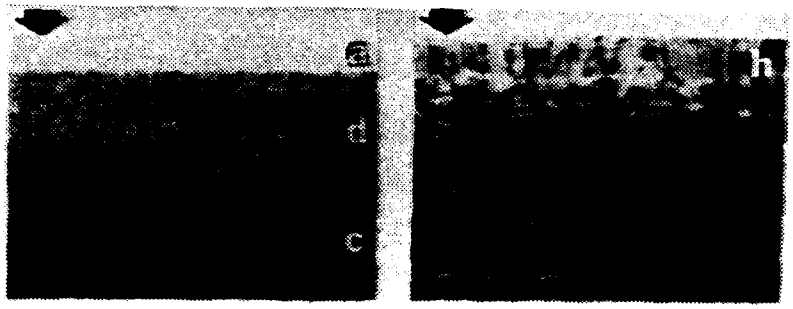


Fig. 4. TEM micrograph of silicon amorphized with Si^+ at nominal room temperature with the same energies and doses as samples in Fig. 2a, (a) before and (b) after rapid thermal annealing at 950°C/10s. d - heavy damage layer.

HAIRPIN GEOMETRY AND ORIGIN

More detailed information about hairpin geometry and its origin was obtained by tilting experiments on plan-view and cross section TEM samples. The dislocations were found to be perfect with Burgers vector b=a/2<101> inclined by 45° to the <100> sample surface. Observation of a partially SPE regrown amorphous layer indicates that the hairpin tips are located in the region corresponding to the coarse a/c transition region (Figs. 3 and 4). The transition region can be quite broad. High resolution imaging of the sample in Fig. 2b (Fig. 5) reveals the presence of misoriented crystallites surrounded by amorphous material. The misorientation is thought to be a result of stresses in the transition region which result from the difference in density [17] between amorphous and crystalline silicon.

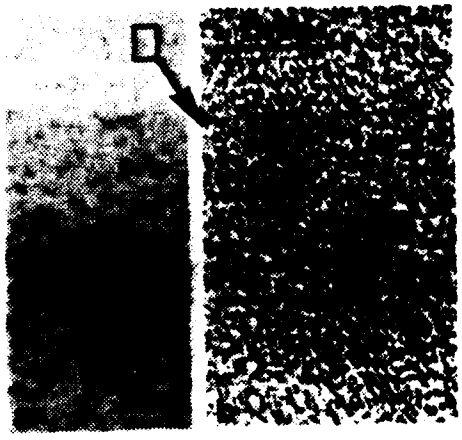
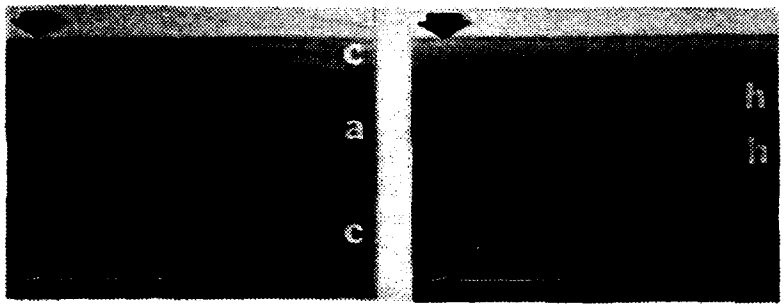
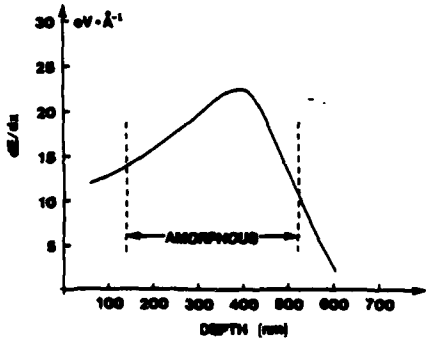


Fig. 5. Cross-sectional, high magnification image of the a/c interface of the sample shown in Fig. 2b. Microcrystallites imbedded in amorphous surroundings show a 4° misorientation relative to the substrate.

cooled Si sample implanted with Si^+ at 300 keV, 1E16 cm^{-2} dose. These conditions produce a buried amorphous layer with two a/c interfaces. Note that the a/c interface closer to the surface appears rougher than the deeper one (Fig. 3a) and was observed to generate about an order of magnitude more hairpins after RTA than the latter (Fig. 3b). The difference is probably associated with a different gradient of damage energy density at the depths corresponding to each interface (Fig. 3c). The steeper the curve, the less spatial straggle of the amorphous-to-crystalline threshold zone would be expected. A preamorphization under similar implantation conditions with heavier ions like germanium yields steeper damage energy density curves, sharper a/c interfaces and fewer hairpins after RTA.



a b

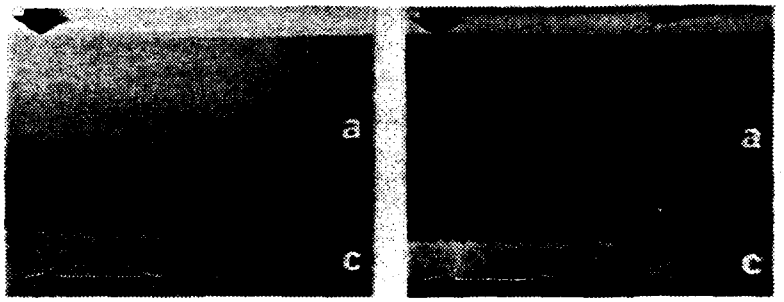


c

Fig. 3. (a) Buried amorphous layer after single 300 keV, 1E16cm^{-2} Si^+ implant into LN cooled Si substrate, (b) after RTA, 950°C/10s, annealing hairpin dislocations (h) grow from each a/c interface toward the middle of amorphous layer. The density in the upper layer is about one order of magnitude higher than in the lower one, (c) corresponding damage energy density curve [16].

If the temperature of the substrate during implantation is sufficiently high to cause the diffusion of radiation induced defects, part of the damaged area regrows. This so-called dynamic regrowth does not necessarily reproduce the crystalline structure in its original form. Instead, a highly damaged, although not amorphous, transition layer develops between amorphous and crystalline regions. Amorphization may not occur at all if the heating is sufficient. This in effect overcomes the residual ion straggling nonuniformity of a/c interface and becomes a dominating factor determining its roughness. Figure 4 shows cross section TEM micrograph of a Si sample implanted with Si^+ under the same conditions as the sample of Fig. 2a (i.e., 300 keV 1E16cm^{-2}, 150 keV 5E15cm^{-2}, 70 keV 5E15cm^{-2}), but at RT. The surface amorphous layer was reduced from about 0.6 μm to 0.15 μm, and the a/c interface became coarse and fragmented (Fig. 4a). The RTA at 950°C/10s produced about 10^7 cm^{-2} hairpins, evaluated from TEM observations in Fig. 4b.

implanted at liquid nitrogen temperature (LN) with heat conducting silver paste applied between the back of the wafer and a cooled sample holder. Since the temperature of the secondary implant was the only parameter different for both samples, beam heating was suspected as the cause of the increase in hairpin density, N_d. In order to simulate heating effects during BF_2 implantation, Si^+-preamorphized samples were given furnace heat treatments (250-350°C for 1h) in inert atmosphere prior to RTA. There was no appreciable increase of hairpin density over that of the preamorphized sample with LN BF_2 implant ($N_d<10^6 cm^{-2}$). However, samples which received a furnace heat treatment at 500°C for 1 hour prior to RTA were found to contain hairpins whose density was comparable to that of preamorphized sample with BF_2 implanted at room temperature. These results suggest that the existing a/c interface can be modified in similar fashion by beam and furnace heating and that this process can lead to an increase in the population of hairpin dislocations. The modification is presumably a ripening process of very small crystallites [11] in the part of amorphous layer in close proximity to the a/c interface which otherwise may be annihilated during high temperature RTA process. Cross section TEM of both BF_2 implanted samples observed prior to RTA process has shown that the RT BF_2 implant produced significant coarsening of the interface. Figure 2 shows the TEM micrographs of the preamorphized sample before and after BF_2 implantation at RT. The sample with BF_2 implantation performed at LN exhibits similar features to those of a preamorphized only sample.



a b

Fig. 2. Morphology of a/c interface in the sample (a) preamorphized with Si^+ at LN and (b) subsequently implanted with BF_2 at RT (0.1 W/cm^2). a - amorphous, c - crystalline layer. Distance marker in this and following micrographs indicates 0.5 μm.

Although beam heating of the a/c interface during the second (doping) implantation can have, as was just shown, remarkable impact on the dislocation density, the quality of the interface due to amorphization process will play a dominant role in determining the density of the hairpins. If the temperature of the sample during amorphizing implantation is low enough to prevent radiation induced defects from significant diffusion (recall that the negative vacancy in Si has been observed to become mobile above 100K [15]), the appearance of the a/c interface can be sharp and smooth, with possible undulations due to ion straggling effect only. The TEM micrographs of Fig. 3 show a LN

arsenic [9] and silicon [6], as well as in those preamorphized with Si [9-11] or Ge [12] and subsequently implanted with shallow BF_2. In our experiments we have also observed the defects in the Si preamorphized samples implanted with boron.

Krimmel et al. [9] who observed "dislocation pairs" or hairpins in As implanted and electron beam annealed silicon postulated that the defects originate from small dislocation loops acting as nuclei. Two segments of dislocation loops [6], or half-loop [5] intersected by the a/c interface have been proposed in other works as an origin of the hairpin dislocation. The form and specific location of the dislocation-along the gradient of implanted dopant(s) and hence across the interface(s) of p-n junction(s) suggests its potentially significant and detrimental role in device performance. To our knowledge, no detailed information about the role and relation of the defect's existence and population to the implantation process has been published. Early studies of ionic transport in pipe diffusion process along dislocations in Si [13,14] indicate a four to six orders of magnitude increase in diffusion coefficients of such ions as Sb, Ag, In, and P in the 900-1200°C temperature range. In this investigation the origin, the relation to the morphology of a/c interface, and the role in the dopant pipe diffusion of hairpin dislocations will be examined.

Fig. 1. Cross-section TEM showing hairpin dislocations (h) spanning the region where amorphous layer existed before annealing.

DYNAMIC ANNEALING AND HAIRPIN DENSITY

Our previous investigation [5] showed that there is a strong correlation between the concentration of hairpin defects in the preamorphized samples implanted with BF_2 and annealed via rapid thermal annealing (RTA), and the temperature of the wafer during dopant implantation. Samples implanted at nominal room temperature (RT), without proper heat sinking, at a power density of about $0.1 W/cm^2$ exhibited a high density of hairpins. An etch pit count for the sample subjected to a Secco etch for 30 seconds revealed about 7×10^4 dislocations per cm^2. Almost no hairpin defects were observed in the sample

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DYNAMIC ANNEALING PHENOMENA AND THE ORIGIN OF RTA INDUCED "HAIRPIN" DISLOCATIONS

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ABSTRACT

The geometry, origin, and diffusion along hairpin defects in Si were investigated using TEM and SIMS techniques. The defect that grows from the amorphous-crystalline (a/c) interface following solid phase epitaxy growth front was found to be a perfect dislocation with a/2(101) Burgers vector. Misoriented microcrystallites within the a/c transition region are proposed to be nucleation sites for the hairpin dislocations. The density of the crystallites increases with an overall coarsening of the interface which occurs during dynamic annealing processes stimulated by implantation or post-implantation low temperature annealing. Hairpin dislocations were found to pipe-diffuse boron at much higher rates than bulk processes significantly shifting dopant profiles. The diffusion coefficient of boron pipe diffusion at 1150°C was found to be about 10^4 times higher than the bulk one.

INTRODUCTION

The ion implantation process has become a routine means of doping semiconductors. An electrical activation of the dopants requires an annealing at elevated temperatures. Although temperatures as low as 600-650°C can provide proper activation [1-3] in an amorphized substrate, temperatures of the order of 1000°C are necessary to fully activate the impurity when the structure of host crystal has not been rendered amorphous before or during implantation. It is also well known that implantation into a preamorphized substrate eliminates channeling of ions along major crystallographic directions assuring tight control of the dopant concentration profile and junction location. Silicon self-implantation has been chosen by several workers [3-5] as a preamorphization process to avoid any chemical interaction with the dopant. While the regrowth of the deep amorphous layer accomplished through the solid phase epitaxy (SPE) process during annealing removes any residual damage caused by the shallower dopant implantation, it may introduce certain characteristic defects of its own. A heavy dose of the dopant may induce precipitation and microtwin formation [6,7] or polycrystallinity [8] during regrowth. Regardless of the dose the recrystallized layer contains interstitial type dislocation loops near the original location of the amorphous-crystalline (a/c) interface. Also, it has been observed [5,6,9-11] that elongated, V-shaped "hairpin" dislocations span the regrowing layer (Fig. 1). The latter dislocation follows the regrowing a/c interface and in the case of an amorphization extending to the surface of the wafer terminates at that surface. The hairpins have been observed in samples amorphized with

Appendix VIII

Dynamic Annealing And The Origin of RTA Induced "Hairpin" Dislocations

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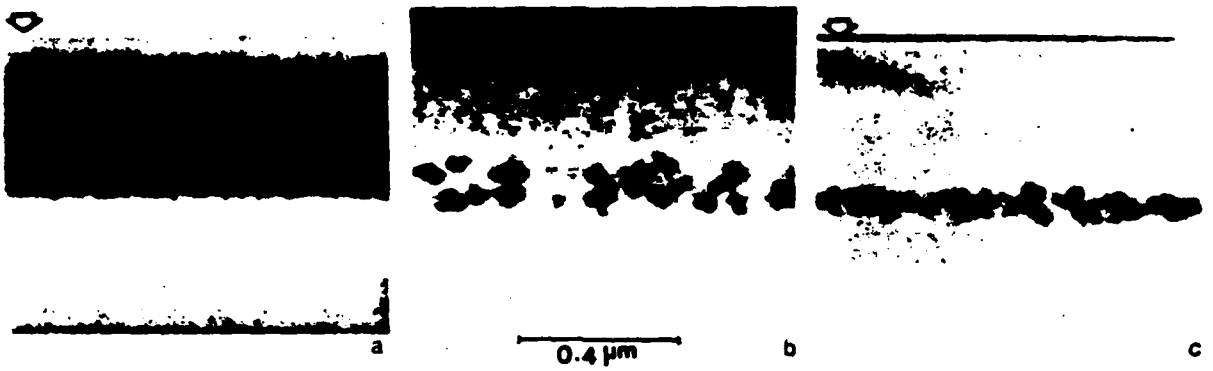

Figure 1. $Ge^{+} \longrightarrow$ (100) Si, 300 keV, 10^{16} cm^{-2}, XTEM micrographs showing (a) a continuous amorphous layer (dark band) in the unannealed sample (b) dislocation loops due to straggling ion damage at the amorphous/crystalline interface in the RTA (1100°C/10 sec) sample (c) same as (b) but with shallow BF_2 implant (42 keV, 2 x 10^{15} cm^{-2}).

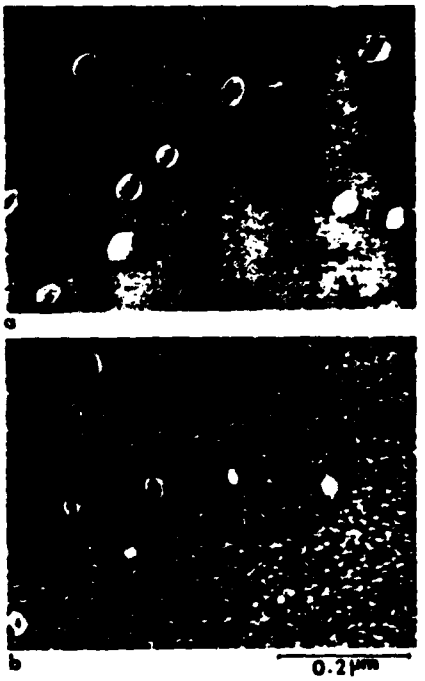

Figure 2. Weak-beam TEM plan view micrographs, (a) corresponding to Fig. 1b and (b) corresponding to Fig. 1c. Note a high density of fine clusters (≈50Å) in Fig. 2b.

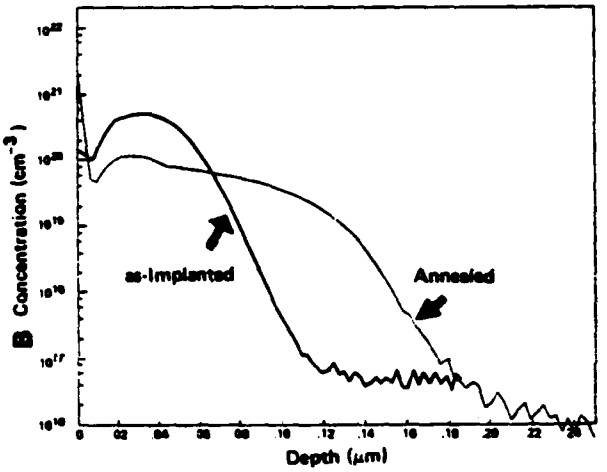

Figure 3. SIMS profiles of boron before and after RTA at 1100°C/10 sec.

defect-free regrowth again occurred in the originally amorphous region (Fig. 1c). Hair-pin shaped dislocations (not shown) were occasionally observed in this region (type II defects in ref. 5). Small dislocation loops due to straggling ion damage were also present in the interfacial region. Although the bright field XTEM micrograph did not show any surface damage (type III in ref. 5), the weak-beam TEM micrograph (Fig. 2b) from a plan view sample corresponding to the surface region of Figure 1c revealed a high density of uniformly distributed fine defect clusters (≈50A). Such clusters were absent in a similar TEM micrograph (Fig. 2a) from the sample without the BF_2. A similar phenomenon has been observed on RTA of self-implanted samples with a shallow BF_2 layer.[5]

The B and F profiles from the samples of Fig. 1c before and after the RTA are shown in Figures 3 and 4. The as-implanted profiles of both B and F showed Gaussian distributions with peaks occurring at 300A (Fig. 3) and 250A (Fig. 4). The peak concentrations of B and F were found to be 5 x 10^{20} cm^{-3} and 8 x 10^{20} cm^{-3} respectively. During

RTA, however, a high concentration ($\approx 10^{21}$ cm^{-3}) of B was found to segregate toward the surface which created a pile-up there. Pronounced diffusion into the deeper regions (up to 0.2μm) also occurred (Fig. 3). The F profile from the RTA sample did not show high surface concentrations. The F peak remained at Rp although it became narrower as compared to that in the unannealed sample indicating its precipitation at this depth. Diffusion of F toward the peak was observed from either side of the peak. Comparison of the weak-beam TEM results with the SIMS data in Figs. 3 and 4 confirms that the fine clusters are related to the presence of B and/or F.

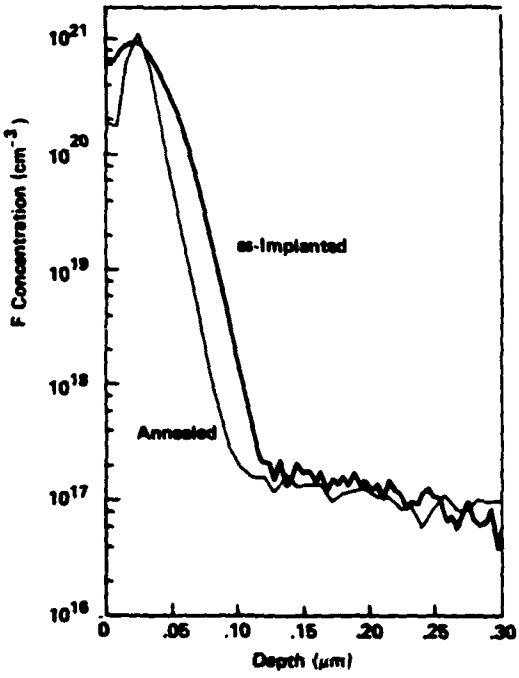

Figure 4. SIMS profiles of fluorine before and after RTA at 1100°C/10 sec.

From the results presented above, it appears that Ge can be a suitable alternative for pre-amorphization of Si. The structural quality obtained after RTA of the pre-amorphized layer with or without BF_2 is comparable to or better than that achieved in the Si-implanted case.[5,6] For example, in both procedures three types of major secondary defects are found to be present with BF_2: (I) surface damage (II) 'hair-pin' shaped dislocations within the implanted region and (III) dislocation loops due to straggling ion damage at the amorphous crystalline interface. However, in the Ge implanted samples the density of type II defects is an order of magnitude less than that in the Si implanted samples. The nature of the surface damage in the two cases is also found to be different. For example, in the Ge case only uniformly distributed fine defect clusters are observed in the surface region (Fig. 2b). In the Si case microtwins and other irregular structures are observed in addition to the clusters. Comparison of atomic profiles of F show that the redistribution of F in both the unannealed and annealed samples can be significantly reduced in the Ge case. However, the B profiles following BF_2^+ implantation show qualitatively similar results in the two cases although B segregation at the surface is more pronounced in the Ge case than the Si case. Experiments on RTA behavior of shallow B^+ and As^+ into Ge implanted Si are now underway. The electrical results from these samples will be published elsewhere.

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Germanium Implantation into Silicon

An Alternate Pre-Amorphization/Rapid Thermal Annealing Procedure for Shallow Junction Formation

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INTRODUCTION

Control of electric charge in the surface region of modern miniature Si devices is achieved by shallow (0.5μm) dopant implantation followed by a furnace or rapid thermal annealing (RTA) treatment.[1] However, for light impurities, such as B, complete amorphization of the surface layer by ion implantation does not occur even at high doses (10^{15} cm^{-2}) and an extended tail in the B distribution is usually observed due to channeling during implantation.[2,3] Removal of partially amorphous implantation damage is difficult to achieve on subsequent annealing. Furthermore, high doses of smaller covalent radii dopants create a dislocation network in the implanted region in addition to several other kinds of extended defects. Therefore, recent shallow implants of light impurities are conducted into pre-amorphized Si substrates and then furnace[4] or rapid thermally annealed[5] to circumvent the problems addressed above. The pre-amorphization is usually achieved by multiple energy self-implantation of Si to very high doses ($10-10^{16}$ cm^{-2}). Since Ge has infinite solid solubility in Si, and it does not appear to alter the electrical properties of Si significantly, we have amorphized Si prior to dopant implant with Ge rather than a typical multi energy Si implant. A similar approach is being investigated by others.[6,7] The presence of large covalent radius Ge on substitutional site in Si is expected to compensate the lattice strain that arises after subsequent high dose shallow implant/annealing of impurities like B or P. This should prevent the formation of a dislocation network which would otherwise be present without Ge. In this communication, RTA behavior of pre-amorphized surface layers in Si produced by Ge implantation with or without subsequent BF_2 implant is presented. A comparison between RTA results from Si and Ge induced amorphous surface layers is also discussed.

EXPERIMENTAL

Silicon wafers of (100) orientation were implanted with Ge^+ to a dose of 10^{16} cm^{-2}. The implantation was conducted at 300keV at either liquid nitrogen (LN) or room temperature (RT). Some of the wafers were subsequently implanted with 42 keV BF_2^+ at RT to a dose of $2x10^{15}$ cm^{-2}. Both types of wafers then underwent RTA at 1100°C for 10 seconds in an intense incoherent light system. The structural characterization on all cross-section samples was performed by bright-field transmission electron microscopy (TEM) whereas both bright-field and weak-beam TEM were performed on plan view samples. The atomic profiles of B, F and Ge before and after the RTA were obtained by secondary ion mass spectrometry (SIMS).

RESULTS AND DISCUSSION

Figures 1a and b show typical XTEM micrographs from a Ge implanted (at LN or RT) sample before and after RTA at 1100°C for 10 seconds. From these micrographs and their corresponding diffraction patterns (not shown) it was found that the unannealed sample contained a 4000A wide amorphous layer extending from the surface (Fig. 1a). Upon annealing at 1100°C for 10 seconds, defect-free regrowth occurred in the amorphous region (Fig. 1b). However, the amorphous/crystalline interfacial region in the annealed sample contained a discrete layer of small dislocation loops typical of the coalescence of straggling ion damage.[8] The RBS/MeV He^+ channeling from the samples of Figure 1a and b indicated that 92% of Ge occupied substitutional lattice sites after the RTA.[9] Comparison of the Ge profiles from the unannealed and annealed samples show that very little redistribution of Ge occurs on RTA.[9]

The XTEM micrograph from the subsequently shallow (42 keV) BF_2 implanted but unannealed sample showed that there was no change in the width of the original amorphous layer. The RTA of this sample showed that essentially

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key words: rapid thermal annealing, Ge, implantation, TEM, SIMS, damage

Appendix VII

Germanium Implantation Into Silicon: An Alternate Pre-Amorphization Rapid Thermal Annealing Procedure For Shallow Junction Technology

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J. Electrochem. Soc. 131 (4) 1984

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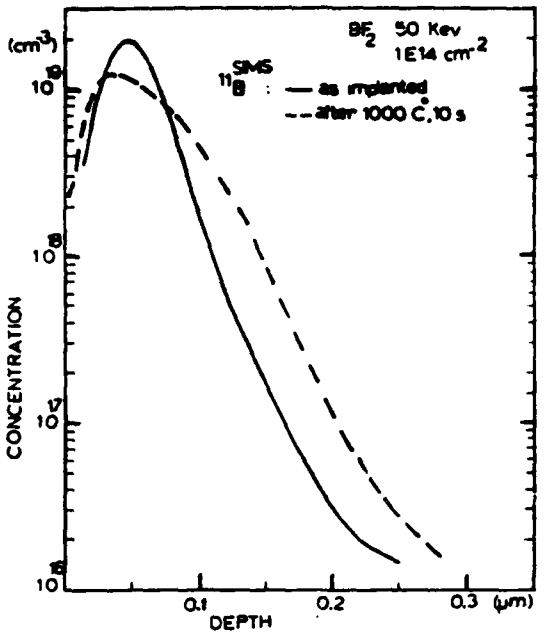

FIG. 1. Concentration vs depth profile of "B" for BF_2^+ implant in silicon before and after RTA.

The sheet resistance saturates above 950 °C and the saturated value of the sheet resistance corresponds approximately to 90% activation and to a mobility value of 110 cm^2/Vs. With the implant parameters used, the peak concentration is 2×10^{19} cm^{-3} and the mobility value is adequate for this concentration level.[6] The leakage current is greatly affected by the thermal steps. A typical variation of the junction leakage current with RTA temperature is shown in Fig. 3. The wafers which were preannealed at 550 °C (30 min in N_2 ambient) do not show an RTA temperature dependence since the recrystallization takes place in the preanneal step. A slight decrease with increasing RTA temperature was observed in some of the data sets. However, the leakage current of the junctions with only RTA showed a strong RTA temperature dependence. When the heat pulse ramp rate was decreased, the leakage current also decreased. All of the data sets examined have shown the same trend. Lower annealing time values (less than 10 s) seemed to have some reproducibility problems.

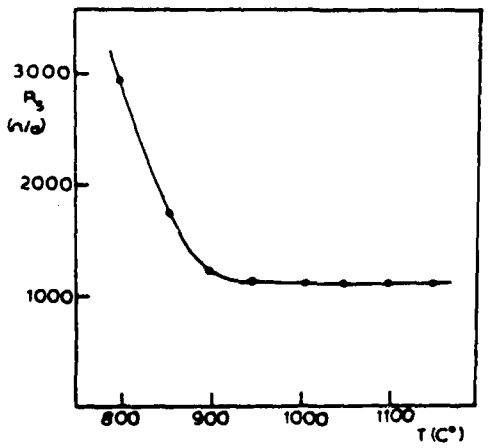

FIG. 2. Variation of the sheet resistance of the implanted layer with RTA temperature (anneal time: 10 s, fast ramp).

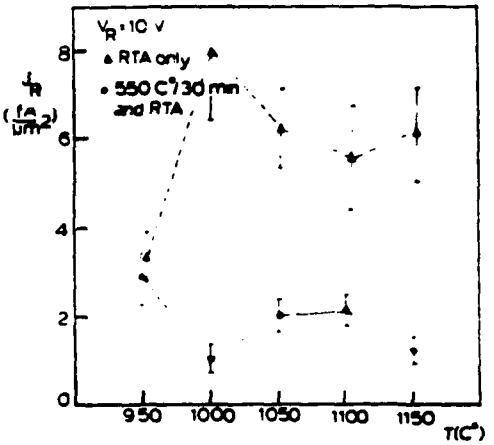

FIG. 3. Dependence of the junction leakage current density to the RTA temperature with and without preanneal step (anneal time: 10 s, fast ramp).

These results suggest that 950 °C is the optimum RTA temperature in terms of both leakage current and sheet resistance. At this temperature it appears that the preanneal step can be omitted, eliminating a furnace anneal step, since the leakage current value is almost equal to the value obtained with preanneal step. The sheet resistance also reaches its saturation value at this temperature.

The leakage current density obtained was around 1 fA/μm^2 (at 10-V reverse bias voltage). This value includes a contribution due to surface leakage since no measure was taken to avoid it. For comparison a set of diodes has been fabricated using conventional annealing techniques (900 °C, 30 min) and the value of leakage current density was found to be around 2 fA/μm^2 at 10 V.

An ideality factor η of 1.3–1.4 was obtained from the forward bias characteristics of the RTA diodes.

In conclusion, we have demonstrated that when the temperature is adequately selected RTA can replace a conventional furnace annealing. The optimum RTA temperature is observed to be around 950 °C. RTA apparently minimizes the problem of dopant redistribution during annealing and offers a very flexible, easy to handle processing tool. The results suggest that RTA can be implemented in a device or integrated circuit process for annealing purposes without sacrificing electrical performance. A 550 °C preannealing before RTA should improve the quality of the crystal regrowth. But it seems that for the implant parameters chosen, the preannealing can be omitted.

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Appendix IX

Residual Defects Following Rapid Thermal Annealing of Shallow Boron and Boron Fluoride Implants Into Preamorphized Silicon

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Residual defects following rapid thermal annealing of shallow boron and boron fluoride implants into preamorphized silicon

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Shallow BF_2 and B implants (42 keV, 2×10^{15} cm^{-2}) were conducted at either liquid nitrogen or room temperature into deeply preamorphized (100) Si. Cross-sectional transmission electron microscopy revealed that subsequent rapid thermal annealing (RTA) of the room-temperature implanted BF_2 sample in the temperature range 950–1150 °C for 10 s created three classes of secondary defects at three different depth levels. The depths corresponded closely to the projected range of the BF_2 implant, the deep amorphous/crystalline interface, and the region immediately below the interface. In contrast, RTA of preamorphized Si with or without the shallow B implant both resulted in a high perfection surface region with secondary defects only in the region below the deep amorphous/crystalline interface. A phenomenological model for nucleation of the separate layers of defects is presented.

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Rapid thermal annealing (RTA) techniques employing incoherent light sources with heating cycles of 1–10 s are currently being explored[1–3] as an alternative to furnace annealing of ion implantation induced damage. RTA is becoming popular in device development labs. because it has been demonstrated recently that very high dopant activation with reduced redistribution of the initial implanted profile can be achieved by this method.[4,5] The simplicity and energy efficiency of RTA equipment compared with scanning laser or electron beam sources make this process promising for high volume manufacturing of integrated circuits. Channeling, residual defects, and incomplete electrical activation in the tail region of dopant profiles are major problems when ion implantation is used to form shallow junctions. This is particularly true for B as well as BF_2 implants, since the latter breaks up upon impact.[6,7] For heavy atoms and high doses, an amorphous layer is formed which reduces channeling and improves the subsequent solid phase epitaxy. Little, if any, amorphous material is formed by B or BF_2 when the implant is performed into a substrate that has either no heat sink or a poor heat sink. The extent and nature of lattice damage is highly dependent on the substrate temperature during implantation as well as the dose.[8] The use of a deep Si implant to form a wide amorphous layer prior to the shallow dopant implantation has been considered to circumvent channeling and incomplete electrical activation on furnace or RTA.[9–12] Although electrical and atomic distributions of dopants have been reported in the literature,[2,3,9–12] the studies of residual defects after RTA have been limited. In this letter, detailed investigations of defect structures in B^+ and BF_2^+ implants into preamorphized Si are reported using transmission electron microscopy.

Uniform preamorphization to a depth of 650 nm was achieved by performing a triple-energy Si self-implantation at 300, 150, and 70 keV and doses of 10^{16}, 5×10^{15}, and 5×10^{15} cm^{-2}, respectively. During the implantation, the wafers were held at either liquid nitrogen (LN) or room temperature with a good thermal contact to the wafer mount or with essentially no thermal contact to the mount. Only LN implantation with a good thermal contact resulted in a completely amorphized surface layer with a sharp amorphous/crystalline (a/c) interface as revealed by cross-sectional transmission electron microscopy [Fig. 1(a)]. At other implantation temperatures, complicated multilayer amorphous or heavily damaged structure formed due to *in situ* annealing effects. Therefore, only wafers preamorphized at

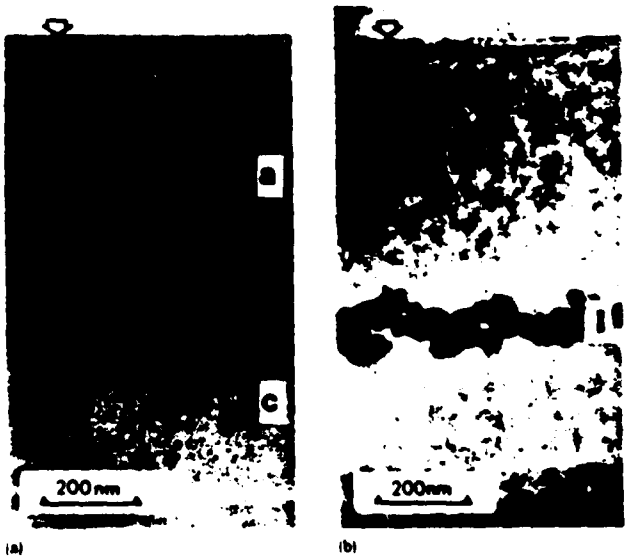

FIG. 1. Cross-section TEM micrographs of (100) silicon implanted with Si at 300, 150, and 70 keV and doses of 10^{16}, 5×10^{15}, and 5×10^{15} cm^{-2}, respectively, at LN. (a) as implanted, (b) RTA at 1150 °C for 10 s. Arrows point to the surface. c—crystalline, a—amorphous, I—type I damage.

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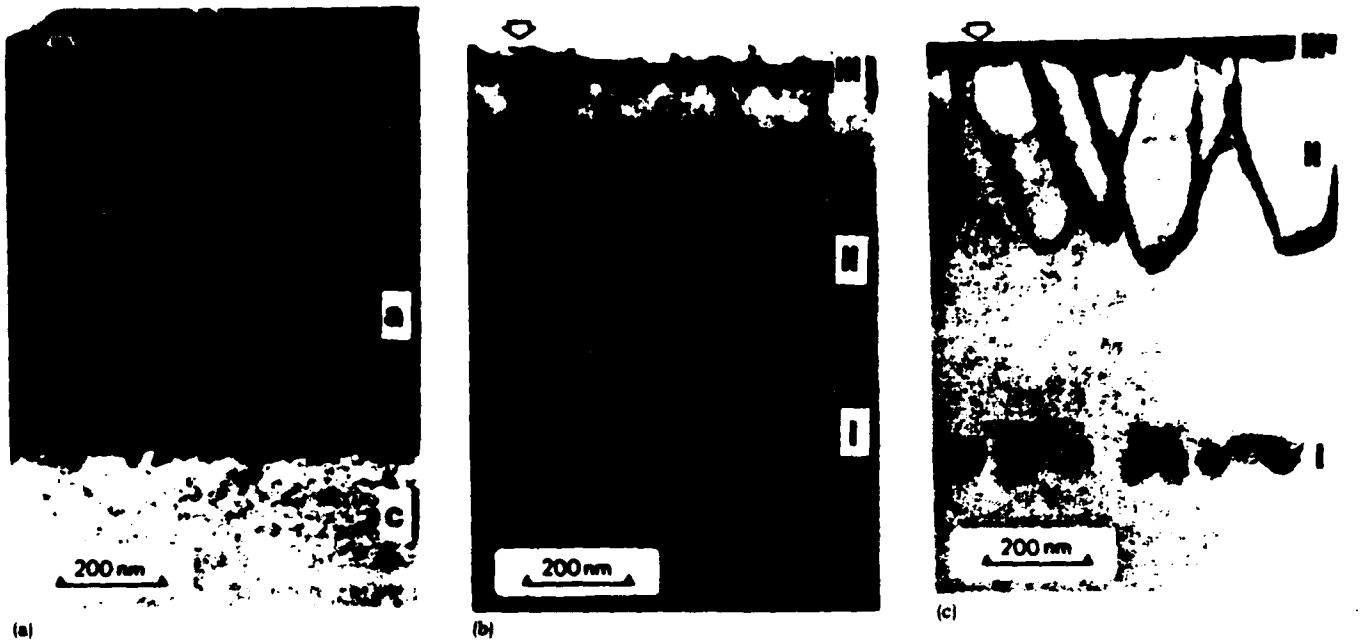

FIG. 2. Cross-section TEM micrographs of (100) silicon preamorphized such as the sample of Fig. 1(a) and implanted with BF_2 at 42 keV and a dose of 2×10^{15} cm^{-2} at nominal room temperature. (a) as implanted, (b) RTA at 950 °C for 10 s, (c) RTA at 1150 °C for 10 s. I—type I damage, II—type II damage, III—type III damage.

LN were used for subsequent 42-keV BF_2 or B implantation to a dose of 2×10^{15} cm^{-2} at room or liquid nitrogen temperature. Figure 1 shows the recrystallization behavior of the preamorphized Si layer (without any subsequent dopant implant) *under* RTA conditions at 1150 °C for 10 s. The amorphous layer regrew perfectly by solid phase epitaxy on the underlying Si substrate leaving no secondary defects. This is evident from the XTEM micrograph of Fig. 1(b), as well as from the corresponding transmission electron diffraction pattern which showed single crystal (110) spots. However, a layer of dislocation loops remained at a mean depth of 640 nm which corresponded closely to the original a/c interface. This is indicated as type I damage in Fig. 1(b).

The subsequent shallow BF_2 implantation at nominal room temperature into the preamorphized Si substrate caused sufficient beam heating and thus *in situ* annealing during the implantation such that observable changes in the structure and morphology of the original amorphous/crystalline interface occurred [Fig. 2(a)]. Subsequent RTA of these samples in the temperature range 950–1150 °C for 10 s created three separate layers of secondary defects including type I damage which was located at a mean depth of 700 nm [Fig. 2(b)]. The dominant looking "hair-pin" shaped dislocations, hereafter referred to as type II damage nucleated in the 950 °C 10-s RTA sample at a mean depth of 640 nm which corresponded to a depth slightly above the a/c interface in Fig. 2(a). The depth of these dislocations decreased to 430 nm and their "hair-pin" ends became flatter following RTA at 1150 °C 10 s. In addition, a 90-nm-wide band of fine defect clusters was present in the surface region that was implanted with BF_2 [Fig. 2(b)]. Secondary-ion mass spectrometry analysis has shown this region to be rich in fluorine. This F related surface damage has been designated as type III damage.

The dominant type II "hair-pin" damage seen in Fig. 2(b) was no longer present (see Fig. 3) when the BF_2^+ was implanted at LN temperature into preamorphized Si followed by RTA under the same conditions as Fig. 2(c); only types I and III damage occurred. The band of the type III damage was slightly narrower (60 nm) and the mean depth of type I damage was shallower (630 nm) than that observed in Fig. 2, but the latter was at the same depth as in Fig. 1(b). The fine clusters were also observed when BF_2 was implanted into single crystal Si substrates and subsequently rapid thermally annealed.

Figure 4 shows the RTA behavior of the sample implanted with B^+ at LN or room temperature into a preamorphized Si substrate. The B^+ implantation, unlike the room-temperature BF_2^+ implant, did not cause any observable change in the nature of the a/c interface of the preamorphized region. The RTA of these samples at 1150 °C for 10 s showed striking results in that defect-free regrowth occurred for the entire preamporphized region, including the B-rich surface region, although the type I damage at 630 nm remained. This is in sharp contrast to the earlier results of B either implanted or diffused into single crystal Si to high concentrations ($< 10^{20}$ cm^{-3}). In such cases, a dislocation

FIG. 3. Cross-section TEM micrograph of (100) Si implanted and annealed in the same manner as Fig. 2(c) but the BF_2 was implanted at LN.

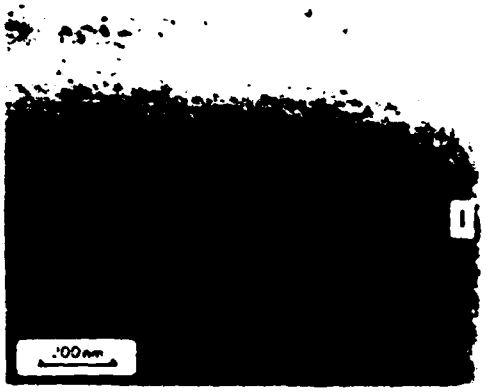

FIG. 4. Typical cross-section TEM micrograph of (100) Si preamorphized in the same manner as Fig. 1(a) and implanted with B at 42 keV and a dose of 2×10^{15} cm^{-2} at either LN or room temperature, and RTA at 1150 °C for 10 s.

network is always found to occur at a depth corresponding to the peak of the B distribution in Si both under furnace and/or RTA conditions.[5]

We now discuss the origin of types I, II, and III damage in the preamorphized layer with or without B or BF_2 (Figs. 1–3). The amorphous layer regrows on top of the underlying single crystal Si substrate via solid phase epitaxy[13] and the recrystallization behavior depends critically on the nature of the disorder at the a/c interface.[14] If the dimensions of damage clusters remain below a certain critical size (perhaps 10–15 Å) at and below the a/c interface, the regrowth in (100) Si occurs in a defect-free manner. Such is the case with the LN implanted samples of Figs. 1, 3, and 4. However, if *in situ* annealing, e.g., due to room-temperature BF_2^+ implant is allowed to occur, the damage clusters may aggregate and conceivably form small embryonic dislocation loops at and below the a/c interface. We believe such is the case with the sample of Fig. 2(a). It is possible that some of the small loops are truncated at the a/c interface. The two ends of the truncated loops then act as nucleating sites for the hair-pin dislocations (type II damage). Similar dislocation/stacking fault nucleation phenomena have been observed earlier in epitaxial layers grown on substrates containing dislocation loops,[15] and also during high power pulsed laser annealing when the depth of the initial molten surface layer matched closely with that of the amorphous layer.[16] These dislocations move toward the surface during high-temperature annealing treatments explaining why the ends of the hair-pin dislocations are found to be slightly (70 nm) above the apparent a/c interface in the 950 °C annealed sample and considerably above (270 nm) the a/c interface in the 1150 °C annealed samples.

During solid phase epitaxy, the advancing a/c interface will encounter a F-rich region at the surface. Since F has a low solid solubility in single crystal Si, it is expected to remain in the amorphous material as long as thermodynamically possible. Eventually, however, regrowth of the heavily F-rich amorphous layer will be retarded leading to a breakdown of the a/c interface due to the nucleation of precipitates, misoriented crystallites, microtwins, etc. These defects collectively provide the type III residual damage in the surface region of the micrographs of Figs. 2 and 3. Similar surface clustering phenomenon has been observed in Ag-implanted (100) Si that was subsequently annealed in a furnace.[17]

The type I damages observed in all of the samples in the present study and also reported many times in the literature are generally attributed to straggling ion damage.[12,18] The loops have been found to be of interstitial type (extra layer of atoms). The extra Si interstitials at the a/c interface probably diffuse both toward the *a*-Si layer and into the bulk. The latter interstitials coalesce to form the loops and grow at the expense of smaller loops or point defect clusters. The extra Si within the amorphous layer is presumably consumed in adding extra (100) layers of atoms above the initial surface.

In summary, the recrystallization behavior of BF_2 and B implants into preamorphized Si substrates has been studied under RTA conditions. We have demonstrated for the first time via cross-sectional TEM that defect-free regrowth can be achieved for B^+ implants under these conditions. Although the regrowth results of the preamorphized layer were sensitive to the subsequent BF_2 implantation temperature, fine defect clusters in the BF_2-rich region at the surface were observed irrespective of the implantation temperature. A phenomenological model considering the size distribution of damage aggregates at the a/c interface has been used to describe the nucleation of secondary defects. Our results clearly suggest that a BF_2^+ implant followed by a simple RTA treatment may not be a suitable processing choice for fabricating shallow junction devices. On the other hand, B implanted into preamorphized substrates looks very promising.

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Appendix X

Shallow p^+n Junctions For CMOS VLSI Applications Using Ge Pre-amorphization

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Boulder, Colorador, June 1985

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SHALLOW P^+-N JUNCTION FOR CMOS VLSI APPLICATION USING GERMANIUM PREAMORPHIZATION**

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With the need to scale VLSI design rules, there is the critical requirement to form very shallow junctions. This study investigates the electrical properties of shallow p^+-n junctions formed by low energy ion implantation of B into preamorphized silicon followed by RTA (rapid thermal annealing). Preamorphization is required since low energy B is known to channel to depths approximately twice that which occurs if the target is amorphous, thereby severely limiting the fabrication of very shallow junctions (< 0.1 μm). Germanium was chosen over silicon as the ion to preamorphize the wafer for several reasons: (1). It is very difficult to use silicon ion implantation to form complete amorphization unless the wafer is cooled to liquid nitrogen temperature [1]. (2). It is difficult to implant silicon without implanting some N_2 unless Si^{29} is used which severely reduces the implantation beam current. (3). Larger doses of silicon are required as compared to germanium. In general it is found that it is very difficult to remove the radiation damage after a silicon preamorphization implant [2].

In our studies the wafer was preamorphized with Ge without cooling. With appropriate RTA treatments, regrowth of the preamorphized region into good quality material is possible [2]. We found leakage currents of less than $5x10^{-14}$ A/cm^2 at -1 volt reverse voltage with breakdown voltage greater than 20 volts. These devices were formed by implanting B at 10 KeV at a dose of 1.0 E15/cm^2. in N-type (100) Si with 5 ohm-cm resistivity. The junction depth was measured using SIMS and was found to be approximately 0.15 μm. Furnace preannealing at 550 C^0 for 30 minutes followed by RTA was found to be the key to the formation of shallow junction, low-leakage-current devices. Shallow junction PMOS devices with retrograde n-wells were also fabricated in a like manner and low leakage currents resulted. The effective gate length of these devices was approximately 1.5 μm with a source/drain junction depth of 0.15 μm.

Hall measurements were made on Ge preamorphized samples. The hole mobility was found to be significantly enhanced (up to 4 times the normal value) in the Ge preamorphized material, it is believed that strain compensation by Ge may cause this difference.

A program simulator "PREDICT I [3]" was used to predict the profile in the devices. This model includes carrier transient diffusion phenomena which occurs in RTA processing as well as traditional diffusion phenomena [3]. The simulation indicated that shallow junctions formed by low energy B implanted into preamorphized silicon and annealed by RTA are very sensitive to further heat treatments. The experimental results agree well with the simulation and indicate that the heat treatment for silicide formation and PSG reflow, for example, cannot be ignored in submicron CMOS device fabrication processes.

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2. D. K. Sadana et. al. J. Electrochem. Soc. 131, 943 (1984)
3. R. B. Fair, MCNC process simulator

** Work supported by Naval Research Office and Semiconductor Research Corp.

Appendix XI

Interface Traps Caused By Ge Pre-Amorphization

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J. J. Wortman

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INTERFACE TRAPS CAUSED BY Ge PRE-AMORPHIZATION

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INTRODUCTION

Modern CMOS VLSI technologies require shallow source-drain junctions for both p-channel and n-channel devices. Junction depths between 0.1 and 0.25 micrometers will be necessary in order to minimize both source-drain leakage currents and threshold voltage reduction due to short channel effects. This is particularly difficult for p-channel transistors because of the channeling and the high diffusivity of boron in silicon. However, these effects can be minimized by applying both pre-amorphization techniques and rapid thermal annealing (RTA).[1-3] More recently, silicon pre-amorphization using Germanium implantation was shown to be a suitable choice for Si pre-amorphization, since it has a high solid solubility in Si and because it does not appear to alter the electrical properties of Si significantly.[3] In order to be compatible with self-aligned poly-silicon gate technology, the damage caused by high energy implantation must be prevented from degrading the silicon-silicon dioxide interface. MOSFET characteristics can be degraded if the damage is not removed by annealing. In our recent work, the interface traps caused by the Ge pre-amorphization were observed even with very low implant energy. A comparison between different isotopes of germanium showed that the effect was due to hydrogen, not germanium. The purpose of this communication is to document the effect and to alert other workers to the adverse impact of GeH implantation.

EXPERIMENTAL

Starting with ‹100› p-type Si wafers, a 38nm gate oxide was thermally grown. A 0.25 μm polysilicon layer was then deposited. After $POCl_3$ doping, a 0.15 μm CVD oxide was deposited to increase the height of the gate barrier up to 0.4 μm. Then, Ge was implanted at several energies with a dose of 2E15 cm^{-2}. Two isotopes of Ge (Ge(70) and Ge(74)) were used using GeH_4 as the source. The CVD oxide layer on the top of poly was etched off and standard MOS capacitors were generated by plasma etching the poly-silicon. Rapid thermal annealing was then performed at 1000^oC and 1100^oC, respectively, for 10 seconds. The C-V characteristics of the capacitors were obtained and the results were compared.

RESULTS AND DISCUSSIONS

Figure 1.a show the C-V characteristics of the MOS capacitors with Ge(74) implantation at 75 kev, after RTA 1000^oC for 10 seconds. There is a hysteresis in the C-V characteristics between forward and retrace curves. The minority carrier lifetime of the devices is so low that the device can not be driven into the deep depletion. Similar results had been obtained on the samples with Ge(74) implantation at the energies of 150 kev and 300 kev. These results indicate that the interface damage exists even with very low implant energy(75 kev). Such damage can be removed only by RTA at 1100^oC for 10 seconds,(Fig. 1.b) and was not observed on the control wafer without implantation. The LSS projected range and standard deviation for Ge in Si are listed in Table I. The estimated depths of amorphous layer are 0.39 μm, 0.21 μm, and 0.11 μm for the energies of 300 kev, 150 kev, and 75 Kev, respectively. TEM cross sectional analysis for Ge implantation at 300 kev showed the amorphous layer to be about 0.4 μm.[3] Thus Ge penetration through the thick poly-gate stack(0.15 μm CVD oxide/0.25 μm polysilicon/oxide) was considered unlikely at 75 kev and 150 kev. Nevertheless, the defects were clearly caused by the implantation

process.

Since Ge has several isotopes(Table II), the Ge(74) is usually selected because of the highest percentage. Unfortunately, implantation with 74 AMU might include Ge(73)H and Ge(72)H_2 in addition to Ge(74). In an ion implanter with a pre-analysis system, the mass analysis takes place at low extraction voltage, and the beam then passes through an acceleration stage to reach its final energy. Post-analysis dissociation of GeH(74) could occur before high energy acceleration, giving the hydrogen atoms enough energy to penetrate the poly-gate and gate oxide. Indeed, the hysteresis and low lifetime phenomena due to the interface defects are not seen in 150 kev Ge(70) implanted samples after RTA at 1000^{o}C for 10 seconds.(see Fig. 2) As a further verification that defects are due to hydrogen penetration, samples with only H_2 implantation were fabricated by the same manner. C-V hysteresis and low minority carrier lifetime were seen in the C-V curves(Fig. 3) of 100 kev H_2 implanted wafers; furthermore, the C-V curves exhibited considerable variability from die to die. Based on these experiments we conclude that anomalously high energy H implantation can occur during Ge(74) implantation. We are unable to determine whether this causes from pre-acceleration dissociation, charge exchange with residual H_2 or during dissociation of GeH at the wafer.

At 300 kev, the defects were observed in both Ge(70) and Ge(74) implanted wafers. It showed that the Ge penetrated the 0.4 μm gate barrier and caused damage at the oxide-silicon interface confirming the previous work of XTEM analysis by D. K. Sadana et al.[3]

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Table I. The LSS projected range of Ge in Silicon[4]

Energy	R_p	ΔR_p
300 kev	0.17	0.055
150 kev	0.087	0.030
75 kev	0.047	0.017

Table II. The major isotopes of Ge [5]

Isotope	Percentage
Ge(70)	20.55%
Ge(72)	27.37%
Ge(73)	7.67%
Ge(74)	36.74%
Ge(76)	7.67%

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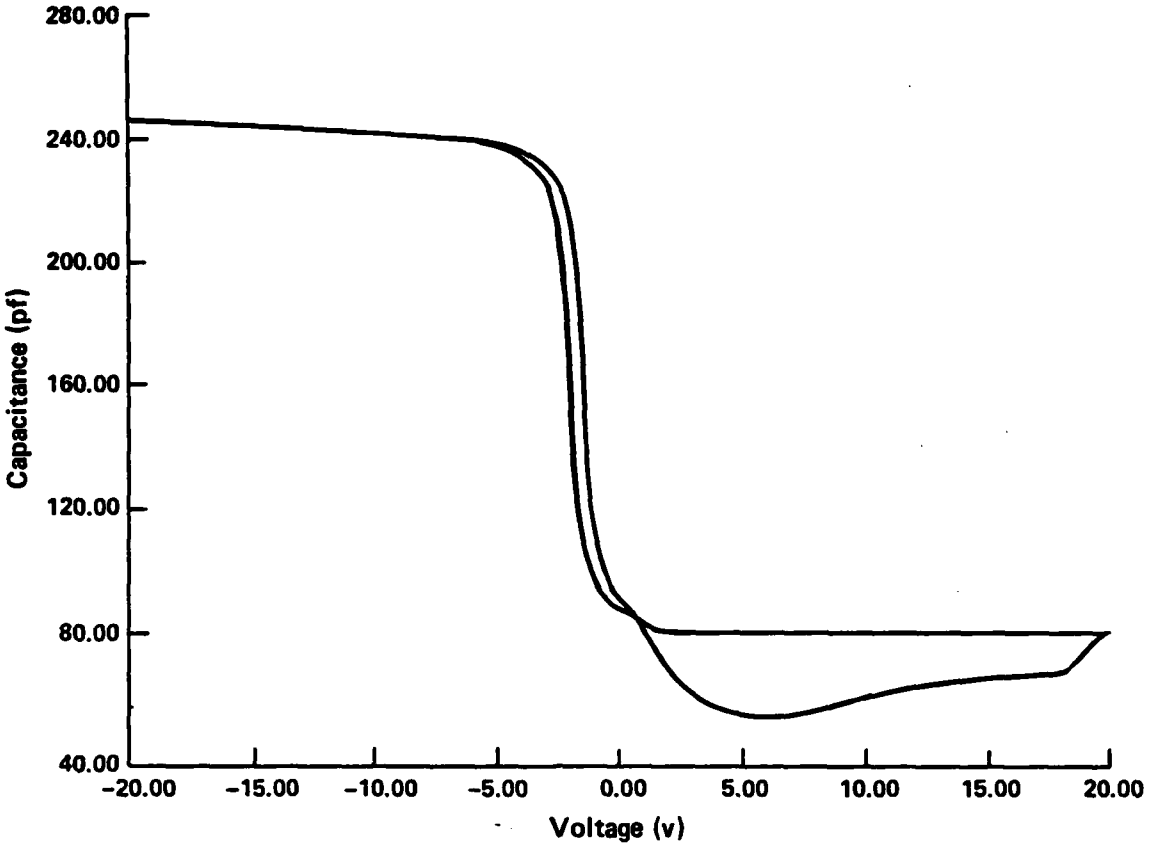
FIGURE CAPTIONS

Fig. 1 The C-V characteristics of capacitor with Ge(74) implantation (energy = 75 kev, dose = 2×10^{15}), (a) after RTA 1000°C, 10 seconds; and (b) after RTA 1100°C, 10 seconds.

Fig. 2 The C-V characteristics of capacitor with Ge(70) implantation (energy = 150 kev, dose = 2×10^{15}), after RTA 1000°C, 10 seconds.

Fig. 3 The C-V characteristics of capacitor with H_2^+ implantation (energy = 100 kev, dose = 1×10^{15}), (a) after RTA 1000°C, 10 seconds; and (b) after RTA 1100°C, 10 seconds.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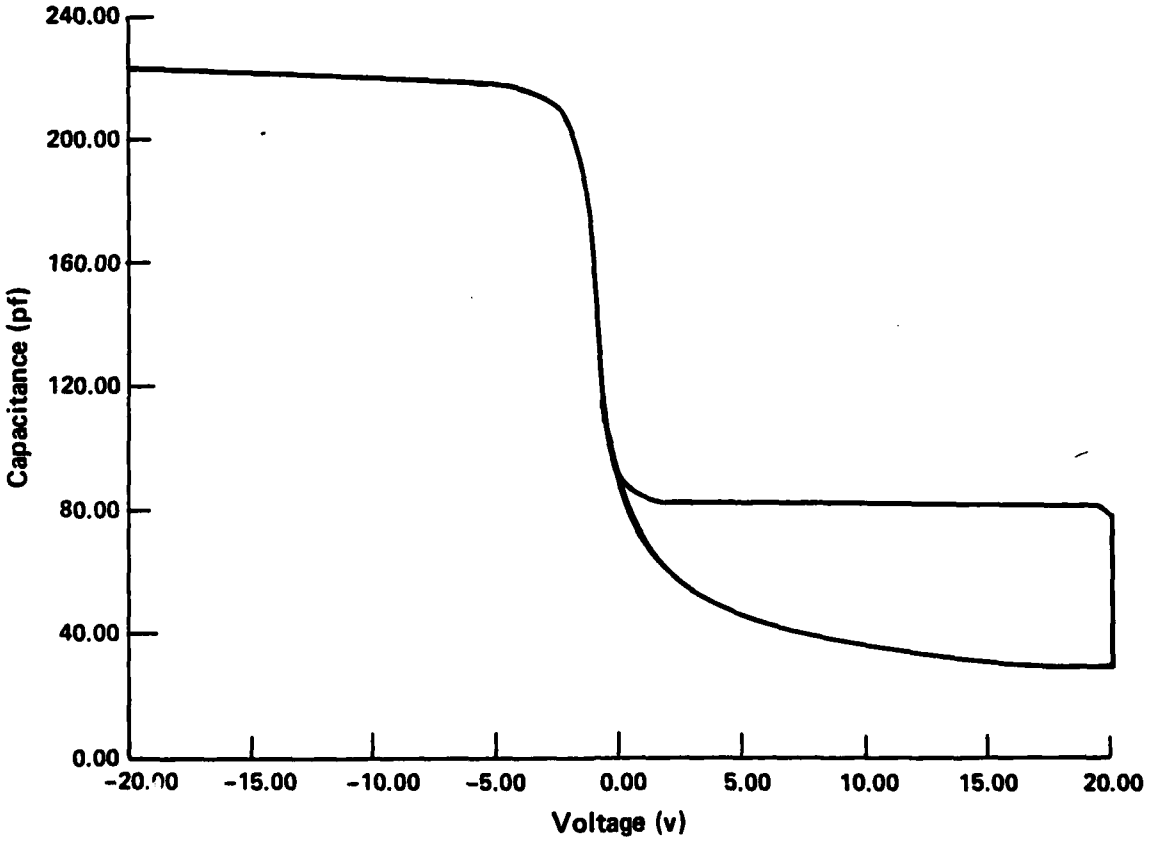
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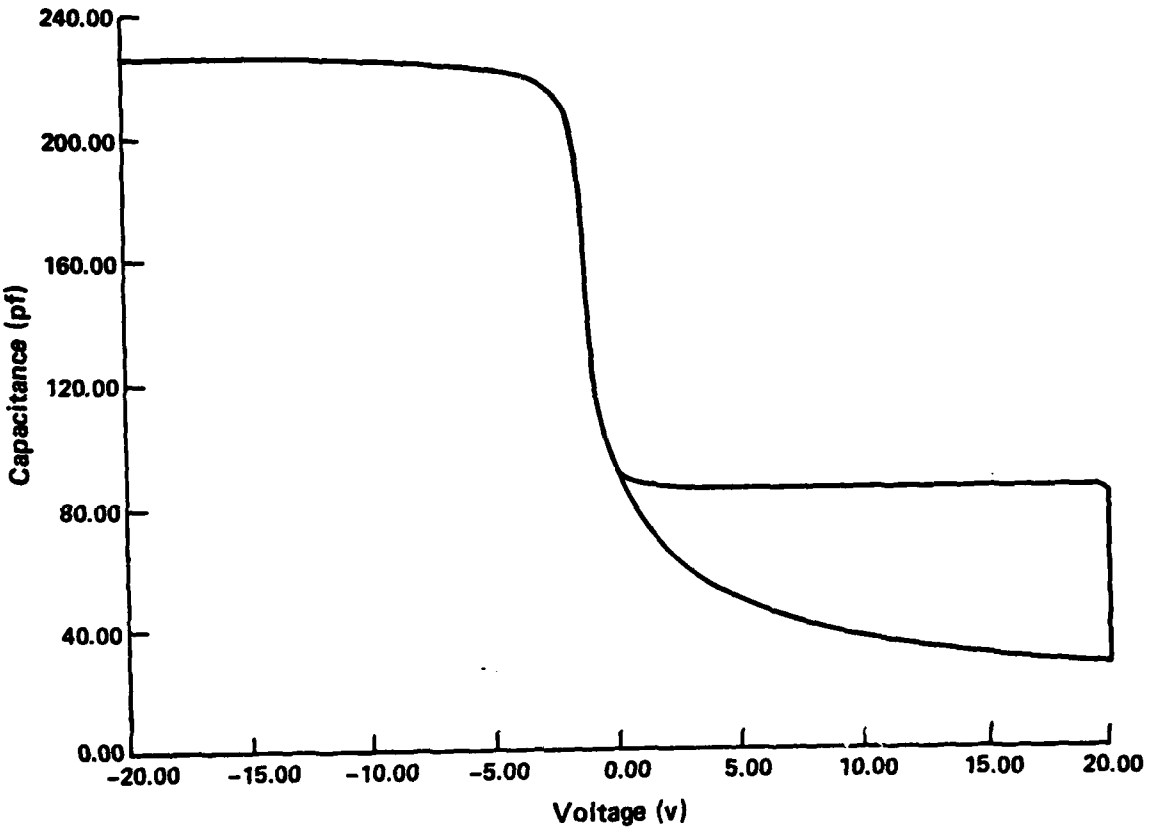
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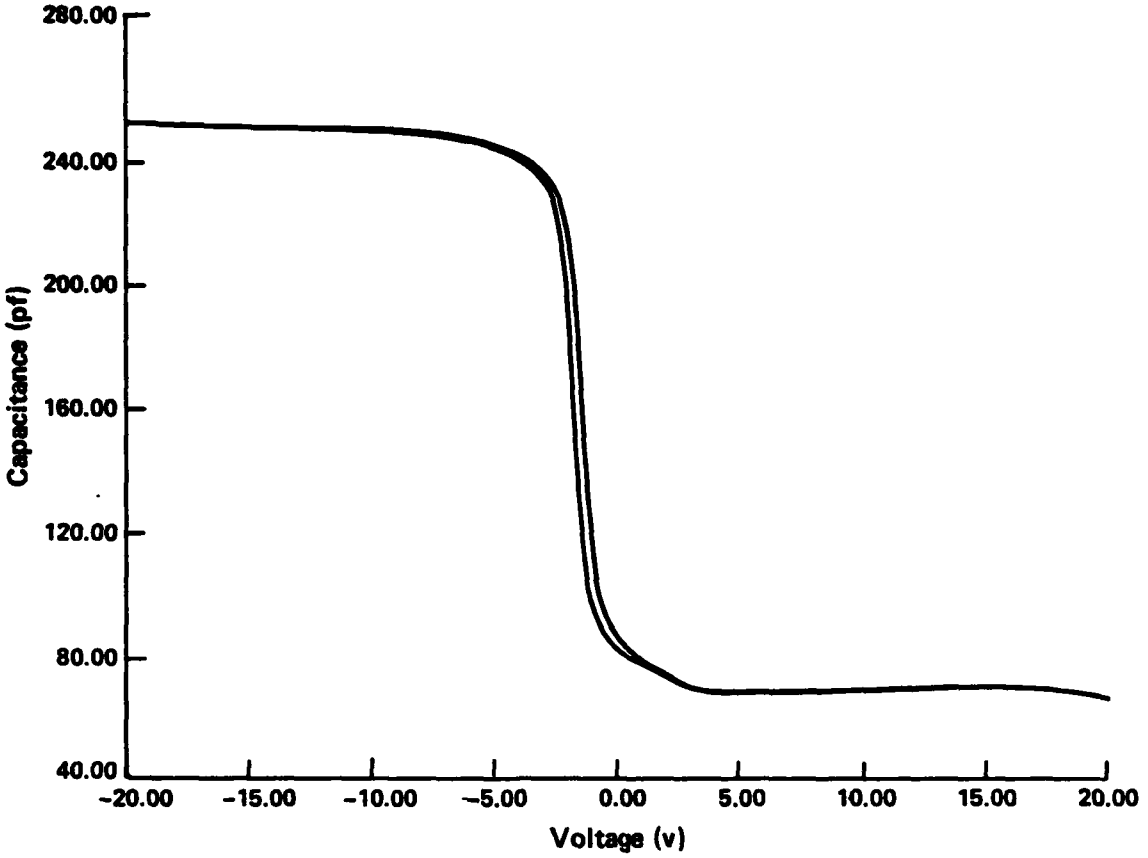
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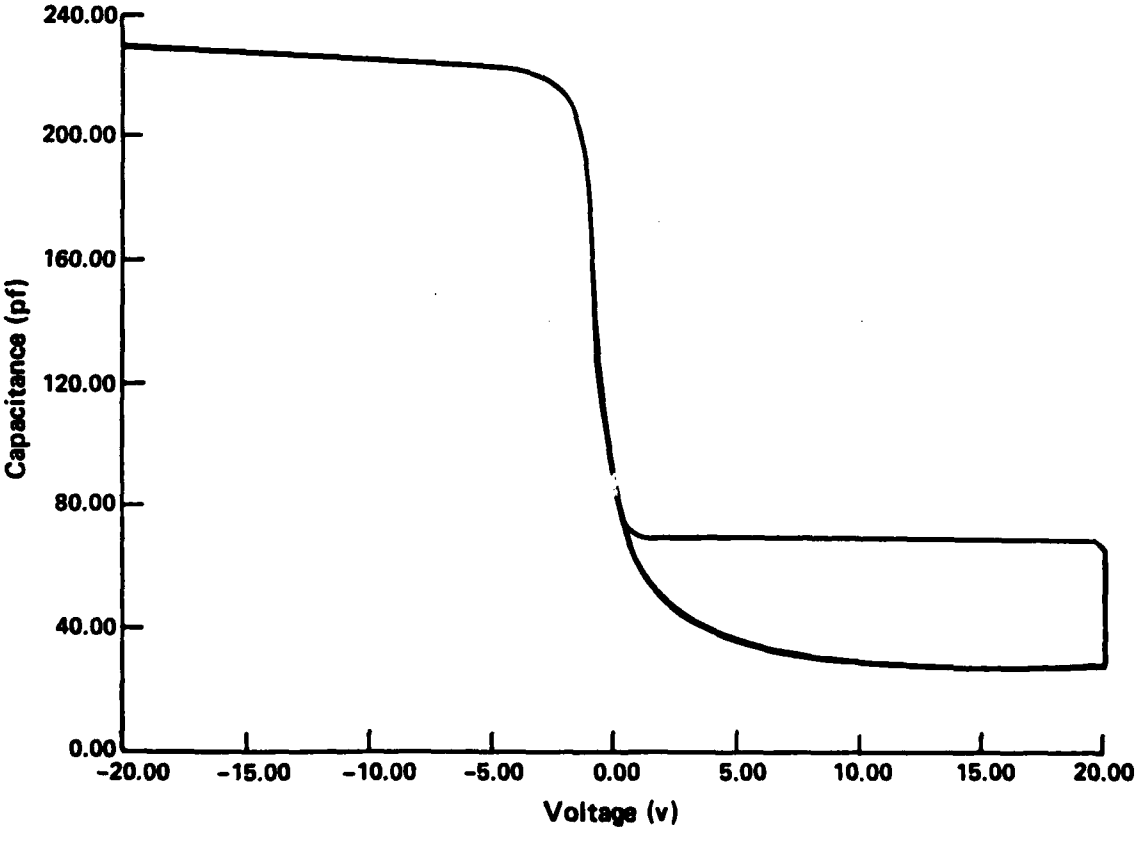
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Voltage (v)

Appendix XII

Effects of Two Stage Annealing On Ion Implanted Boron In Silicon

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Abstract Submitted
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Bulletin Subject Heading
in which Paper should be placed
Ion Implantation

Effect of Two Stage Annealing on Ion Implanted Boron in Silicon. M. Z. Numan, K. Cho, S. S. Choi, W. T. Finstad & W. K. Chu, University of North Carolina, Chapel Hill, and J. Liu, & J. J. Wortman, North Carolina State University — Isochronal furnace annealing (250°C-550°C) followed by rapid thermal annealing (RTA) at 1100°C/10 s is employed to study resulting diffusion of ion-implanted B^+ in Si. Secondary ion mass spectroscopy (SIMS), differential hall effect and sheet sensitivity measurements are used to obtain total and electrically active dopant concentration profiles. Comments will be made on the contributin of dislocation formation to the boron dopant reverse annealing phenomena over the temperature range of 500°C-600°C.

This work was sponsored by SRC under contract No. 3270.

Submitted by

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