



MICROCOPY RESOLUTION TEST CHART NATIONAL BUREAU OF STANDARDS 1963 A

日本には「日本のののため」というという。

NPS52-85-003

# NAVAL POSTGRADUATE SCHOOL Monterey, California



THE USE OF VLSI TECHNOLOGY FOR THE REAL-TIME GENERATION OF GRAPHICS DISPLAYS: A PROPOSAL

Michael J. Zyda

March 1985

Approved for public release; distribution unlimited

Prepared for: Chief of Naval Research Arlington, VA 22217

DTIC FILE COPY

ECTE

MAY 1 6 1985

A

### NAVAL POSTGRADUATE SCHOOL Monterey. California

Commodore R. H. Shumaker Superintendent D.A. Schrady Provost

The Work reported herein was supported in part by the Foundation Research Program of the Naval Postgraduate School with funds provided by the Chief of Naval Research.

Reproduction of all or part of this report is authorized.

This report was prepared by:

Marcha ( ) ) (

ž

MICHAEL J. ZYDA Assistant Professor of Computer Science

Reviewed by:

x. . . . .

BRUCE J. MacLENNAN Acting Chairman Department of Computer Science

Keah T. Man

KNEALE T. MARSHALL Dean of Information and Policy Sciences

| RI  | REPORT DOCUMENTATION PAGE  |  | READ INSTRUCTIONS   |  |
|---|--|--|---|--|
| . REPORT NUMBER   |  | 2. GOVT ACCESSION NO.  | J. RECIPIENT'S CATALOG NUMBER   |  |
|   |  |  |   |  |
| NP352-85-003  |  |  | S TYPE OF REPORT & REMON COVERED  |  |
| The Use Of V<br>Generation o  | LSI Technology For<br>f Graphics Displays  | The Real-Time<br>· A Proposal  | S. THE OF REPORT & PERIOD COVERED   |  |
|   |  |  | 6. PERFORMING ORG. REPORT NUMBER  |  |
| 7. AUTHOR(#)  |  |  | 8. CONTRACT OR GRANT NUMBER(*)  |  |
| Michael J. Z  | yda  | ;  |   |  |
| PERFORMING OR   | GANIZATION NAME AND ADD  | RESS   | 10. PROGRAM ELEMENT, PROJECT, TASK<br>AREA & WORK UNIT NUMBERS  |  |
| Naval Postgraduate School   |  | 61152N; PR000-01-NP  |   |  |
| Monterey, CA  | 93943  |  | N00014851mA1005   |  |
| L CONTROLLING   | FICE NAME AND ADDRESS  |  | 12. REPORT DATE   |  |
| Chief of Nav  | al Research  |  | March 1985  |  |
| Arlington, V  | A 22217  |  | 13. NUMBER OF PAGES   |  |
|   |  |  | 14  |  |
| 4. MONITORING AC  | ENCY NAME & ADDRESS(II di  | fferent from Controlling Office)   | 15. St. CURITY CLASS. (of this report)  |  |
|   |  |  | 154. DECLASSIFICATION/DOWNGRADING<br>SCHEDULE   |  |
| Approved fo   | r public release; d  | listribution unlimite  | ed  |  |
| Approved to   | TATEMENT (of the ebetract on   | listribution unlimite  | ed<br>m Report)   |  |
| Approved to   | TATEMENT (of the ebetract on<br>RY NOTES   | listribution unlimite  | Report)   |  |
| Approved fo<br>7. DISTRIBUTION S<br>10. SUPPLEMENTAR<br>9. KEY WORDS (Con<br>CONTOUR SURF   | TATEMENT (of the ebotrect on<br>TATEMENT (of the ebotrect on<br>TY NOTES   | listribution unlimite<br>tered in Block 20, 11 different from<br>ry end identify by block number)<br>ion, real-time displ  | ay generation   |  |
| Approved to<br>17. DISTRIBUTION S<br>18. SUPPLEMENTAR<br>9. KEY WORDS (Con<br>CONTOUR SURF  | TATEMENT (of the ebetrect on<br>RY NOTES   | tored in Block 20, 11 different from<br>tored in Block 20, 11 different from<br>the second s   | ay generation   |  |
| Approved fo<br>7. DISTRIBUTION S<br>9. KEY WORDS (Con<br>Contour Surfa<br>This Stuc<br>time display<br>taking a sele<br>that performs<br>tial for VLS1<br>effort will t<br>graphics disp<br>generation. | TATEMENT (of the obstract on<br>TATEMENT (of the obstract on<br>ATTEMENT (of the | tered in Block 20, 11 different from<br>tered in Block 20, 11 different from<br>ion, real-time displ<br>ion, real-time displ<br>ion is the development<br>is the development<br>bal is the development<br>ba | A Report)<br>A Report<br>Ay generation<br>VLSI architectures for real-<br>nt of a methodology for<br>roducing a silicon system<br>orithms that have the poten-<br>studied. Part of this<br>the architecture of the<br>ion of such real-time display |  |
| Approved fo<br>T. DISTRIBUTION S<br>S. REY WORDS (Con<br>Contour Surfa<br>This Stuc<br>time display<br>taking a sele<br>that performs<br>tial for VLSI<br>effort will t<br>graphics disp<br>generation. | TATEMENT (of the obstract on<br>TATEMENT (of the obstract on<br>Ary NOTES<br>Thus on reverse olds if necessa<br>ace display generat<br>dy proposes to look<br>generation. The go<br>ected computer graph<br>is that algorithm. So<br>that algorithm. So<br>implementation wi<br>be a characterization<br>olay system made necessary  | tered in Block 20, 11 different free<br>ion, real-time displ<br>at special purpose<br>bal is the development<br>nics algorithm and p<br>Several graphics alg<br>ll be identified and<br>on of the changes in<br>cessary by the addit   | A Report)<br>A Report<br>ay generation<br>VLSI architectures for real-<br>nt of a methodology for<br>roducing a silicon system<br>orithms that have the poten-<br>studied. Part of this<br>the architecture of the<br>ion of such real-time display |  |

•••

•

• •

### The Use of VLSI Technology for the Real-Time Generation

of Graphics Displays: A Proposal ‡

Michael J Zyda

Naval Postgraduate School.

Code 52, Dept. of Computer Science,

Monterey, California 93943

### ABSTRACT

This study proposes to look at special purpose VLSI architectures for realtime display generation. The goal is the development of a methodology for taking a selected computer graphics algorithm and producing a silicon system that performs that algorithm. Several graphics algorithms that have the potential for VLSI implementation will be identified and studied. Part of this effort will be a characterization of the changes in the architecture of the graphics display system made necessary by the addition of such real-time display generators.

Categories and Subject Descriptors: I.3.1 [Hardware Architecture]: architectures, parallel processing, VLSI implementations; I.3.2 [Graphics Systems]: multiprocessing systems: I.3.3 [Picture/Image Generation]: surface visualization: I.3.5 [Computational Geometry and Object Modeling]: data structures. discrete planar contours, surface approximation, surface generation, surface representation, surfaces, 3D graphics: I.3.6 [Methodology and Techniques]: contouring. interactive systems. parallel processing; I.3.7 [Three-Dimensional Graphics and Realism]: line drawings, line generation algorithms, real-time graphics, surface plotting, surface visualization. surfaces; I.3.m [Miscellaneous]: VLSI.

General Terms: Algorithms, architecture;

Additional Key Words and Phrases: contour surface display generation, real-time display generation;

DOC QUALIT

PFC

t The writing of this proposal has been supported by the NPS Foundation Research Program. The work proposed is an extension of the work originally funded by the NPS Foundation Research Program as "The Effects". of Real Time Display Generation on the Architecture of Graphics Display Systems".

### 1. Background

Highly reactive displays for weapons systems, and highly interactive simulators are an obvious need of the Department of Defense. Both of these areas rely on the capabilities of graphics systems for the real-time generation and display of computer images. The idea behind real-time, interactive systems is to provide the human user of such a system immediate feedback of visual information in response to any physical control manipulations made. Such capabilities are necessary in visual training simulators, command-control situations, and other time-critical applications. The cost-effectiveness of flight training simulators is well-known [Collier,1983], [Orlansky.1983], [Needham.1983], and [Schachter,1983]. Historically, the effort to improve the capabilities for such systems has been a push-and-pull cycle of improved algorithms driving special hardware additions to the graphics system. This cycle has been seen several times in the development of the graphics system.

The first cycle of hardware improvements to the graphics system was the development of matrix multipliers for the real-time matrix operations necessary for rotating, scaling, and translating vectors. This had a direct effect on the architectures of display devices in that such special purpose hardware was quickly added to the commercially produced graphics systems. This addition to the display system was quite important in that it allowed the development of real-time interactive applications not previously possible without the special hardware. (One example of this has been the abandonment in the field of chemistry of the use of hard models of large molecules for the more readily manipulated computer models).

The second cycle of improvements has been the offloading of the graphics and interaction functionalities from the host computer to a special processor dedicated to the graphics system. The goal behind this was again performance improvement. The real-time operations desired by the interactive graphics user community had risen to such a level of sophistication that the traditional time-sharing host for the graphics system could no longer provide sufficient response.

The third cycle of hardware improvements to the graphics system is currently beginning. This cycle is driven both by the continuing need for performance improvements in the computation of graphics algorithms. and by the emerging capabilities of the VLSI chip. VLSI technology provides the capability for the parallel operation of large numbers of relatively inexpensive processors [Mead,1980] and [Sutherland,1977]. This technology has proven to be very seductive to the graphics community in that research has begun at several institutions on broadening the scope of the real-time operation capability of the graphics system [Clark,1981], [Clark,1982], [Hoffman,1983], [Roman,1981], [Sproull,1981]. [Weinberg,1983], [Zyda,1984a], [Zyda,1984b], and [Zyda,1984c].

### 2. Proposed Program of This Research

The research proposed in this study is part of the third cycle. It concerns the design of special purpose VLSI architectures for real-time display generation. The thrust of this research is the development of a methodology for taking a selected computer graphics algorithm and producing a silicon chip and system that performs that algorithm. This work can be thought of as a VHSIC insertion project. The scope of this work is quite large in comparison to the other cycles of special graphics hardware development. It encompasses the areas of real-time graphics software engineering, and VLSI computer architectures. Real-time graphics software engineering is part of this effort in that before one commits to implementing a particular graphics algorithm in silicon, one needs to be able to evaluate whether or not that algorithm can be computed in real-time on a currently available, high-performance graphics system. The research effort in this part of the project is to produce a system that can automatically model the desired algorithm such that runtime parameters can be obtained for hypothetical architectures.

VLSI computer architectures are part of this effort in that the hypothetical architectures which we are modeling are those capable of being implemented in VLSI. The research effort in this part of the project is twofold. The first part is the determination and evaluation of a special architecture for the studied algorithm. The determination of the architecture is accomplished through iterative design refinement driven by previous experience with such special processors. The evaluation of the architecture is both a runtime evaluation, and a technological evaluation. The runtime evaluation determines if the studied algorithm is capable of being executed in real-

- 3 -

time on the hypothetical architecture. The technological evaluation determines if the proposed architecture is capable of being built within current technological constraints. Part of this effort is the examination of the changes required in the design of the graphics system that receives the output of the real-time display generator.

The second part of the proposed research in the area of VLSI computer architectures is the evaluation and refinement of the software tools available for putting an architecture on silicon. Since VLSI technology is relatively new, the available software tools for producing special purpose VLSI chips are crude. The research plan outlined to this point presupposes the existence of such software. Consequently, the proposed research necessarily encompasses the refinement and development of such software tools.

### 3. Specific Work Objectives

ľ

D

The first objective of this study is to examine the proposed architecture of one real-time display generator, the contour surface display generator of [Zyda,1984a], [Zyda.1984b], and [Zyda,1984c]. This requires a detailed study of both the architecture of the contour surface display generator, and its intended application. Part of this study will be the development of a modeling methodology for evaluating the physical parameters inherent to both the application, and the architecture.

The second objective of this study is an examination of the input and output parameters obtained from the system model in order to determine exactly how that display generator can be interfaced to a graphics system. This study will be made with respect to relevant commercially available graphics systems in that the current functionality of those systems will be maintained. The result of this study will be a characterization of the changes necessary in the design of current graphics display systems in order to allow the addition of the contour surface display generator.

The third objective of this study is the identification of other graphics algorithms that have the potential for implementation in VLSI. Since the full evaluation of the identified algorithms is

- 4 -

a substantial research project, this study will only be a cursory examination of those algorithms for their distributability among multiple processors. Part of this study will attempt to determine if the changes proposed for the graphics system for the contour surface display generator are applicable to other real-time display generators.

The fourth objective of this study is to acquire and examine the available hardware and software technology necessary for the actual construction of the contour surface display generator. The beginning of this step will be the refinement of the architecture proposed from the results of objectives one and two for the contour surface display generator.

The final objective proposed for this study will be an evaluation of the steps performed in the design of the contour surface display generator, with the goal of establishing a methodology for facilitating the implementation of other graphics algorithms in VLSI. Part of this methodology will be a recommendation as to the design changes necessary in the graphics system for support of such real-time display generators.

### 4. References

1. Clark, James H. "A System Design Revolution," Computer Graphics: A Quarterly Report of SIGGRAPH-ACM, Vol. 15, No. 3 (August 1981), pp. 79-80.

2. Clark. James H. "The Geometry Engine: A VLSI Geometry System for Graphics," Computer Graphics: A Quarterly Report of SIGGRAPH-ACM, Vol. 16, No. 3 (July 1982), p. 127.

3. Collier, Allen "An Overview of Military Training-System Development," Computer Image Generation, Edited by B.J. Schacter, p. 189. New York: John Wiley & Sons, 1983.

4. Hoffman, Thomas R. "The Role of LSI/VLSI in Computer Image Generation," Computer Image Generation, Edited by B.J. Schachter, p. 173, New York: John Wiley & Sons, 1983.

5. Mead. Carver and Conway, Lynn Introduction to VLSI Systems, Reading, Massachusetts: Addison-Wesley Publishing Company, 1980.

6. Needham. R.C., Edwards, B.J., and Prather, D.C. "Flight Simulation in Air-Combat Training." *Computer Image Generation*, Edited by B.J. Schachter, p.209, New York: John Wiley & Sons. 1983.

7 Orlansky, Jesse and String, Joseph "Reaping the Benefits of Flight Simulation." Computer Image Generation, Edited by B.J. Schachter, p. 191, New York: John Wiley & Sons, 1983.

8. Roman. Gruia-Catalin and Kimura. Takayuki "VLSI Perspective of Real-Time Hidden-Surface Elimination," *Computer-Aided Design*, Vol. 13, No. 2 (March 1981), pp. 99-107.

- 5 -

9. Schachter. Bruce J. "Training Centers for Business Aircraft." Computer Image Generation. Edited by B.J. Schachter, p. 219, New York: John Wiley & Sons. 1983.

10. Sproull. Robert "Custom VLSI Chips for Graphics." Computer Graphics: A Quarterly Report of SIGGRAPH-ACM. Vol. 15, No. 3 (August 1981), p. 79.

11. Sutherland, I.E. and Mead. C.A. "Microelectronics and Computer Science," Scientific American, September 1977, pp. 210-228.

12. Weinberg. Richard "VLSIC Architectures for Image Generation." Computer Image Generation, Edited by B.J. Schachter, p. 179, New York: John Wiley & Sons, 1983.

13. Zyda. Michael J. "Multiprocessor Considerations in the Design of a Real-Time Contour Display Generator." Technical Memorandum 42. St. Louis: Department of Computer Science, Washington University, December 1981.

14. Zyda. Michael J. "A Contour Display Generation Algorithm for VLSI Implementation," Computer Graphics: A Quarterly Report of SIGGRAPH-ACM, Vol. 16, No. 3 (July 1982), p. 135.

15. Zyda, Michael J. "A Contour Display Generation Algorithm for VLSI Implementation." Selected Reprints on VLSI Technologies and Computer Graphics, Compiled by Henry Fuchs, p. 459. Silver Spring, Maryland: IEEE Computer Society Press, 1983.

16. Zyda, Michael J. Algorithm Directed Architectures for Real-Time Surface Display Generation, D.Sc. Dissertation, Dept. of Computer Science, Washington Univ. St. Louis, Missouri, January 1984a.

17. Zyda, Michael J. "Real-Time Contour Surface Display Generation," Technical Report NPS52-84-013, Monterey, California: Department of Computer Science, Naval Postgraduate School, September 1984b.

18. Zyda, Michael J. "The Feasibility of a Multiprocessor Architecture for Real-Time Contour Surface Display Generation." Technical Report NPS52-84-025, Monterey, California: Department of Computer Science, Naval Postgraduate School, December 1984c.

# Distribution List for Papers Written by Michael J. Zyda

Dr. Henry Fuchs. 208 New West Hall (035A), University of North Carolina, Chapel Hill, NC 27514

Dr. Kent R. Wilson, University of California, San Diego B-014, Dept. of Chemistry, La Jolla, CA 92093

Dr. Guy L. Tribble, III Apple Computer, 20525 Mariani Ave, Cupertino, CA 95014

Dr. Victor Lesser, University of Massachusetts, Amherst Dept. of Computer and Information Science, Amherst, MA 01003

Dr. Gunther Schrack, Dept. of Electrical Engineering, University of British Columbia, Vancouver, B.C., Canada V6T 1W5

Dr. R. Daniel Bergeron, Dept. of Computer Science, University of New Hampshire, Durham. NH 03824

Dr. Ed Wegman, Division Head, Mathematical Sciences Division, Office of Naval Research, 800 N. Quincy Street, Arlington, VA 22217

Dr. Gregory B. Smith. ATT Information Systems. 190 River Road. Summit, NJ 07901 Dr. Lynn Conway. Defense Advanced Research Projects Agency IPTO. 1400 Wilson Blvd., Arlington, VA 22209

Dr. John Lowrance, SRI International, 333 Ravenswood Ave, Menlo Park, CA 94025

Dr. Paul Schneck, Office of Naval Research. Code 433, 800 North Quincy St. Arlington, VA 22217

Dr. Richard Lau, Office of Naval Research, 1030 E. Green St., Pasadena, CA 91106

Dr. Y.S. Wu, Naval Research Laboratory, Code 7007. Washington, D.C. 20375

Dr. Joel Trimble. Office of Naval Research. Code 251, Arlington, VA 22217

Robert A. Ellis, Calma Company, 527 Lakeside Drive, Sunnyvale, CA 94086

Dr. James H. Clark. Silicon Graphics, Inc. 630 Clyde Court, Mountain View, CA 94043

Shinji Tomita, Dept. of Information Science, Kyoto University, Sakyo-ku, Kyoto, 606, Japan Hiroshi Hagiwara, Dept. of Information Science, Kyoto University, Sakyo-ku, Kyoto, 606, Japan

Dr. Alain Fournier. Dept. of Computer Science. University of Toronto, Toronto, Ontario Canada M5S 1A4

Dr. Andries Van Dam, Dept. of Computer Science, Brown University, Providence, RI 02912

Dr. Brian A. Barsky, Berkeley Computer Graphics Laboratory, Computer Sciences Division, Dept. of Electrical Engineering and Computer Sciences, University of California. Berkeley, CA 94720

Dr. Ivan E. Sutherland. Carnegie Mellon University, Pittsburg. PA 15213

Turner Whitted. 205 New West Hall (035A). University of North Carolina. Chapel Hill, NC 27514

Dr. Robert B. Grafton, Office of Naval Research, Arlington, Virginia 22217

Professor Eihachiro Nakamae, Electric Machinery Laboratory, Hiroshima University, Higashihiroshima 724, Japan

Carl Machover. Machover Associates, 199 Main Street. White Plains. New York 10601 Dr. Buddy Dean, Naval Postgraduate School. Code 52, Dept. of Computer Science. Monterey, California 93943

# INITIAL DISTRIBUTION LIST

| Cameron Station<br>Alexandria, VA 22314  | 2  |
|--|----|
| Dudley Knox Library<br>Code 0142<br>Naval Postgraduate School<br>Monterey, CA 93943                      | 3  |
| Office of Research Administration<br>Code 012A<br>Naval Postgraduate School<br>Monterey, CA 93943        | 1  |
| Chairman, Code 52ML<br>Department of Computer Science<br>Naval Postgraduate School<br>Monterey, CA 93943 | 40 |
| Assistant Professor Michael J. Zyda  | 70 |

Department of Computer Science Naval Postgraduate School Monterey, CA 93943



# FILMED

6-85

DTIC