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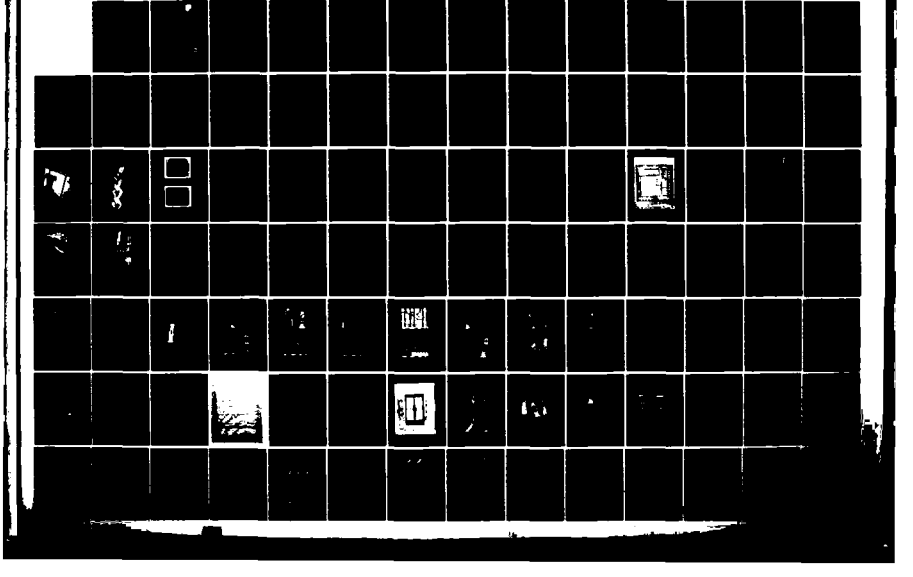

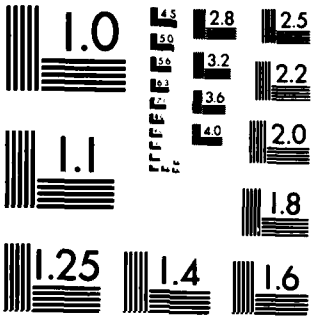

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Final Technical Report
September 1984

EOS PROTECTION FOR VLSI DEVICES

Martin Marietta Denver Aerospace

David D. Wilson, William E. Echols and Mark G. Rossi

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RADC-TR-84-183 has been reviewed and is approved for publication.

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The sensitivity of eight complex integrated circuits to ESD was studied. This included both the human body ESD simulation and the charged device ESD simulation. Failure Analysis and data analysis were performed to understand the sensitivity variations and to allow recommendations to be made on input protection networks for VLSI devices.

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EVALUATION

Many of the major semiconductor manufacturers have published the results of their own in-house design evaluations of new electrostatic discharge (ESD) protection networks. Several major users have published test and evaluation results on the ESD protection networks used on a wide cross-section of popular device types available today. The present work was undertaken to expand that data base and to compare the failure mechanisms which occur in devices subjected to both the human body and the charged device ESD simulation tests.

The conclusions of this report are similar to those other workers. Failure mechanisms induced with the human body model are primarily electrothermal junction shorting, often associated with aluminum/silicon contacts near the bonding pads (an interlevel polysilicon layer placed between the aluminum and silicon in such contacts significantly raises the failure threshold). Layout 'mistakes' such as closer spacing of protective network components to other junctions can cause significantly lowered failure thresholds for a pin. Interlayer oxide shorts were found to occur in some networks. The charged device test induced failures at much lower voltages but the failure mechanisms were similar in the best protective networks. In almost every case there were easily recognized reasons for increased sensitivity on one or more pins which could be fixed by minor layout changes.

It appears that the best approach to ESD protection is to use standard networks with identical layout placed near the bonding pad of each pin which requires ESD protection. It is also clear that the entire ESD current path through the device must be considered in addition to the local protection network.

Advances in integrated circuit technologies are resulting in basic circuit structures which are increasingly sensitive to electrostatic discharge (ESD) damage because of decreasing oxide thicknesses, shallower junction depths and smaller junction areas. A comparison of the sensitivity of present day integrated circuits to damage by ESD to that of devices designed only a few years ago must be done on a vendor-to-vendor basis and often, unfortunately, within some vendors on a department or designer basis. Even so, this work has shown that certain vendors' product lines have exhibited reduced ESD sensitivity in spite of technology advances. These cases indicate that significant progress has been made in the design of effective ESD protection networks (which are integrated into virtually all of today's devices).

Further progress must be made for two reasons: 1) future devices are expected to be more sensitive to damage as scaling continues and 2) the best protective networks available today cannot withstand a healthy zap from a human (>5000v, 100 pf, 1500 ohm test) or a low level zap from themselves (2000v, charged device test).

Daniel J. Burns

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RADC/RBRP

I. INTRODUCTION

The purpose of this study is to gain further information on the sensitivity of advanced semiconductor devices to electrical overstress (EOS). The electrical overstress investigated was electrostatic discharge (ESD) using both the charged device (CD) model and the human body discharge (HBD) model.

This study included 1. Literature Search, 2. Test Procedure Development, 3. Test Equipment Fabrication, 4. ESD Sensitivity Testing, and 5. Protection Scheme Study.

II. LITERATURE SEARCH

A literature search was performed to gather published information on EOS/ESD work. This information was used in the rest of the study to establish the test procedure and test equipment in order that the best possible test could be developed.

A computer search through the Martin Marietta reference library was initiated by a subject/key word method. The subjects which were researched were electrical overstress and electrostatic discharge. The databases which were used include:

1. NASA RECON - Includes report literature indexed in Scientific and Technical Aerospace Reports (STAR), International Aerospace Abstracts (IAA), announcements of NASA research in progress, and reports issued by the Aerospace Safety Research and Development Institute.

2. Lockheed DIALOG, SDC ORBIT - These database vendors offer a selection of over 125 databases covering various fields of knowledge. Four of those used are listed below:

   a. INSPEC (Institute of Electrical Engineers) - Provides on-line access to the three sections of Science Abstracts (Physics Abstracts, Electrical and Electronics Abstracts, Computer and Control Abstracts).

   b. SPIN (American Institute of Physics) - Indexes a variety of the world's physics journals.

   c. COMPENDEX (Engineering Index) - Provides worldwide coverage of engineering literature.

   d. NTIS (National Technical Information Service) - Covers government-sponsored research.

3. Defense RDT and E Online System (Research, Development, Test, and Evaluation) - Provides access to Department of Defense current and completed research as well as projects planned for the future.

The paper abstracts and/or titles were obtained and selected articles were ordered.

Pertinent articles which were available from symposium proceedings which are kept on file in the Failure Analysis Laboratory were also obtained. The proceedings reviewed included the Physics of Failure/Reliability Physics Symposium proceedings from 1967 to present, the EOS/ESD Symposium proceedings from 1979 to present, and the ATFA/ISTFA Symposium proceedings from 1977 to present.

With the papers obtained from these sources, each was reviewed and categorized. The categories included:

1. Human body discharge model
2. Charge/discharge model (charged device)
3. Electrical overstress
4. Protection networks
5. Equipment
6. Review paper
7. Theoretical paper

Within each of these categories, the papers were summarized for significant information. As an example for the equipment category the type of resistors, capacitors, relays, switches, and materials were noted. Contacts were also made with several of these authors to discuss their systems.

In addition to categorizing the articles, other data was compiled. These include:

1. Devices tested
2. Failure threshold
3. Waveform monitoring
4. Voltage steps utilized
5. Data analysis methods

During later stages of the testing the RAC "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" publication was obtained and reviewed.

A listing of 66 articles which were reviewed follows:

Categories

HBD Human Body Discharge Model
CD Charged Device Model
EOS Electrical Overstress Model
PN Protection Networks Information
EQ Equipment Information
R Review Paper
T Theoretical

ARTICLES

Category	Title
EOS, PN, R	1. "The Application of Electrical Overstress Models to Gate Protective Networks", D. Wunsch in IRPS, 1978
EOS, T	2. "Calculation of Minimum Power Level for Device Burnout", Itsu Arimura, Boeing Document
EOS	3. "Screening of Time-Dependent Dielectric Breakdowns", E. Anolick, L. Chen in IRPS, 1982
EOS	4. "Electromigration Resistance of Fine-line Al for VLSI Applications", S. Vaidya, D. Fraser, A. Sinha in Elec. Comp. Conf., 1980
EOS, T	5. "Analysis of Electrical Overstress Failures", J. Smith in IRPS, 1973
EOS	6. "Electrical Overstress Failure Analysis in Microcircuits", J. Smith in IRPS, 1978
EOS	7. "Degradation of Thin-Gate MOSFETs Under High Electric Field Stress", H. Ishinchi, Y. Matsumoto. S. Sawada and O. Ozawa in IRPS, 1982
HBD, EQ, PN	8. "Reliability Influences from Electrical Overstress on LSI Devices", A. Hart, T. Teng and A. McKenna in Elec. Comp. Conf., 1980
EOS	9. "Electromigration Failure Under Pulse Test Conditions", R. Miller in IRPS, 1978
EOS	10. "Failure of Small Thin-film Conductors due to High Current-Density Pulses", E. Kinsbron, C. Mellian-Smith, A. English and T. Chynoweth in IRPS, 1978

ARTICLES (Cont.)

Category	Title
EQ	11. "Electrostatic Discharge Tester", T. Madzy, L. Price and M. Ruduski in IBM Bulletin, 1977
PN	12. "Multiple I/O Protection with Single Protective Device", S. Chen, S. Park, R. Wong in IBM Bulletin, 1980
PN	13. "Voltage Programmable Protect Circuit", C. Hoffman and F. Wiedman in IBM Bulletin, 1980
PN	14. "Electrostatic Discharge Protective Device for Bipolar Circuits", W. Carlson, V. Klimanis and R. Seeger in IBM Bulletin, 1978
PN	15. "Protective Circuit for Integrated Semiconductor Devices", O. Alameddine in IBM Bulletin, 1978
R, PN	16. "Susceptibility of Semiconductors to Damage from Electrostatic Discharge", R. Funk in Int. Elec. Packaging and Prod. Conf., 1980
PN	17. "Floating Plate Protective Device", Y. Huang in in IBM Bulletin, 1977
PN, EQ	18. "The Evaluation of CMOS Static-Charge Protection Networks and Failure Mechanisms with Overstress Conditions as Related to Device Life", L. Gallace and H. Pujol, IRPS, 1977
PN	19. "CMOS/SOS Gate-Protection Networks", R. Pancholy and T. Oki in IEEE Trans. on Electron Devices, 1978
PN	20. "CMOS/SOS LSI Input/Output Protection Networks", B. Allport, J. Cricchi and D. Barth in IEEE Trans. on Electron Devices, 1978

ARTICLES (Cont.)

Category	Title
PN	21. "H-MOS Reliability", S. Rosenberg, D. Crook and B. Euzent in IRPS, 1978
PN	22. "Voltage Breakdown Characteristics of Close Spaced Aluminum Arc Gap Structures on Oxidized Silicon", F. Hickernell and J. Crawford in IRPS, 1977
PN	23. "Gate Protection for CMOS/SOS", R. Pancholy in IRPS, 1977
EOS	24. "Electrical Overstress Failures in Silicon Devices", C. Lane in DTIC Technical Report
PN	25. "A Study of the Input Protection Networks of Some NMOS Memory Chips", D. Hinds and R. Crockett in R202 Technical Memorandum
EQ, HBD	26. "Input Protection for MOS Circuits - Supplement" Ferranti Limited in DTIC Technical Report
R, HBD, PN	27. "The Effects of Electrostatic Discharge on Micro Electronic Devices - A Review", Conf. Record of the Industry Applications Society, IEEE, 1981
HBD, CD, EQ, R	28. "Electrostatic Discharge Failures", B. Unger in Circuits Manufacturing, 1981
HBD, CD	29. "Electrostatic Discharge Failures of Semiconductor Devices", B. Unger in IRPS, 1981
HBD	30. "Electrostatic Discharge Effects on MOS Memory ICs", T. Nakamura, H. Kunita and H. Ihara in NEC Research and Development, 1980

ARTICLES (Cont.)

Category	Title
HBD, EQ	31. "Procedure for Testing Electrostatic Discharge Susceptibility of MOS Devices", A. Goel in IRPS, 1981
EQ, HBD	32. "Surprising Patterns of CMOS Susceptibility to Electrostatic Discharge and Implications on Long Term Reliability", J. Schawank, R. Baker and M. Armendariz in EOS/ESD Proc., 1980
HBD, EQ	33. "Control of Electrostatic Discharge Damage to Semiconductors", E. Freeman, J. Beall in IRPS, 1974
Isolated Device Charge Model	34. "A New Technique for Input Protection Testing", D. Fisch in IRPS, 1981
HBD, EQ	35. "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to Electrostatic Discharge", T. Speakman in IRPS, 1974
HBD, EQ	36. "Predicting ESD Related Reliability Effects", A. Hart, J. Smyth and S. Gorski in IRPS, 1982
HBD, EQ	37. "Effects of Electrostatic Discharge on Linear Bipolar Integrated Circuits", R. Minear and G. Dodson in IRPS, 1978
HBD, EQ	38. "Electrostatic Damage Susceptibiliy of Semiconductor Devices", L. Schreier in IRPS, 1978
R	39. "Electrostatic Discharge in Microcircuits, Detection and Protection Techniques", A. Trigonis, JPL Report, 1975

ARTICLES (Cont.)

Category	Title
HBD, EQ	40. "Failure Modes and Analysis Techniques for CMOS Microcircuits", A. Shumka, E. Miller and R. Piety, in ATFA, 1977
HBD, EQ	41. "741 Operational Amplifier Electrostatic Discharge Sensitivity and Subsequent Shifts in Electrical Parameters", D. Baar in Lear-Siegler Report
HBD, EQ	42. "Module Electrostatic Discharge Simulator", T. Madzy, L. Price in EOS/ESD Proc., 1979
HBD, EQ, EOS	43. "Reliability of EOS Screened Gold Doped 4002 CMOS Devices", D. McCullogh, C. Lane, A. Blore in EOS/ESD Proc., 1979
HBD, EQ, PN, EOS	44. "Electrostatic Discharge and CMOS Logic", G. Branberg in EOS/ESD Proc., 1979
EOS	45. "Effects of Electrical Overstress on Digital Bipolar Microcircuits and Analysis Techniques for Failure Site Location", D. Rutherford, J. Perkins in EOS/ESD Proc., 1979
HBD, EQ, PN	46. "Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature", T. Teng, A. Hart, A. McKenna in EOS/ESD Proc., 1979
HBD, EQ, PN	47. "Electrical Overstress Versus Device Geometry" C. Petrizio in EOS/ESD Proc., 1979
HBD, EQ, PN	48. "The Phanton Emitter -- An ESD-Resistant Bipolar Transistor Design and Its Applications to Linear Integrated Circuits", R. Minear, G. Dodson in EOS/ESD Proc., 1979

ARTICLES (Cont.)

Category	Title
HBD, CD	49. "ESD Damage From Triboelectrically Charged IC Pins", P. Bossard, R. Chemelli, B. Unger in EOS/ESD Proc., 1980
PN	50. "Transient Protection with ZnO Varistors: Technical Considerations", H. Philipp, L. Levinson in EOS/ESD Proc., 1980
PN, EQ	51. "Protection of MOS Integrated Circuits From Destruction by Electrostatic Discharge", J. Keller, in EOS/ESD Proc., 1980
HBD, PN	52. "LSI Design Considerations for ESD Protection Structures Related to Process and Layout Variations", A. Hart, T. Teng in EOS/ESD Proc. 1980
HBD, PN	53. "Electrostatic Sensivity of Various Input Protection Networks", T. Turner, S. Morris in EOS/ESD Proc., 1980
HBD, EOS, EQ	54. "Microcircuit Electrical Overstress Tolerance Testing and Qualification", R. Antinone in EOS/ESD Proc., 1980
EQ	55. "Measurements of Fast Transients and Applications to Human ESD", H. Calvin, H. Hyatt, H. Mellberg and D. Pellinen in EOS/ESD Proc., 1980
R, HBD, EQ	56. "A Closer Look at the Human ESD Event", H. Hyatt, H. Calvin and H. Mellberg in EOS/ESD Proc., 1981
PN	57. "The Effects of VLSI Scaling on EOS/ESD Failure Threshold", R. Pancholy in EOS/ESD Proc., 1981

ARTICLES (Cont.)

Category	Title
EQ, PN	58. "On Chip Protection of High Density NMOS Devices", T. Hulett in EOS/ESD Proc., 1981
HBD, PN, EQ	59. "Input Protection Design for the 3u NMOS Process", R. Taylor in EOS/ESD Proc., 1981
EQ, HBD	60. "Susceptibility of ICs in Electrostatic Damage Step-Stress Tests", J. Enders in EOS/ESD Proc., 1981
EOS, R	61. "An Overview of Electrical Overstress Effects on Semiconductor Devices", D. Pierce, D. Durgin in EOS/ESD Proc., 1981
EOS, T	62. "Modeling of EOS in Silicon Devices", N. Kusnezov, J. Smith in EOS/ESD Proc., 1981
EOS, T	63. "Semiconductor Device Failure Criteria for Sinusoidal Stresses", R. Thomas in EOS/ESD Proc., 1981
EOS, T	64. "EOS/ESD Failure Threshold Analysis Errors, Their Source, Size and Control", E. Horgan, O. Adams, W. Rowan and L. Templar in EOS/ESD Proc., 1981
HBD, EQ	65. "Time-Related Improvements of Electrical Characteristics in Electrostatically Damaged Operational Amplifiers", G. Head in EOS/ESD Proc., 1981
HBD, CD EQ, PN	66. "Evaluation of Electrostatic Discharge (ESD) Damage to 16K EPROMS", E. Chase in EOS/ESD Proc., 1981

III. TEST PROCEDURES

Test procedures were developed to be used as destructive step stress to failure tests to determine the voltage level at which device failure occurs. Two test procedures were written, one for the human body simulation and one for the charged device simulation.

The human body simulation test procedure was written in a manner similar to MIL-STD-883B Method 3015.1. The major difference was that each pin on the device was stressed in sequence with all of the other pins connected together as the return path. This configuration is more difficult to implement but allows the weakest path for each pin to be determined as well as testing the power pins which are normally treated differently than the other pins. It is believed that this will provide sensitivity information which closely approximates the sensitivity level of a part in a circuit.

The charged device test is a new procedure which has no similar MIL-STD Method. This method simulates handling, transportation, or non-grounded storage types of failures where a part becomes charged and then it discharges through a pin to a ground plane or to a large object at a different potential. A fixed position for the device, with the device placed upside down on an 8 mil thick teflon glass tape above a ground plane was chosen. Each pin in sequence was slowly charged to a voltage level and then discharged rapidly to ground. The two test procedures follow.

A. "Human Body" Electrostatic Discharge Step Stress to Failure

Test Procedure

1. PURPOSE

This method establishes the means for measuring the level of a simulated electrostatic discharge stress required to produce a failure on a microelectronic circuit. This method will be used for analyzing the sensitivity level of each pin on a device and for quantifying the variation in sensitivity levels between pins.

The simulated electrostatic discharge stress utilized is the waveform as illustrated in Figure 2. This is the "human body" simulation which is designed to produce a waveform comparable to that which will occur if a person charged to a potential level relative to a part comes into contact with that part and there is a current return path out of the part.

1.1 Definition - The following definition for the purpose of this Test Method shall apply:

1.1.1 Electrostatic Discharge (ESD) - An electrical current flow (induced by an electrostatic field) between two substances at different potentials.

2. APPARATUS

The apparatus required is an ESD simulation circuit similar to that shown in Figure 1 which will produce the waveform shown in Figure 2. This system should be capable of producing stress levels from -5,000 volts to +5,000 volts.

3. PROCEDURE

The pulse waveform and parameters as specified in Figure 2 (Note 3 only) shall be verified across the DUT socket, using an oscilloscope with a 1500 ohm resistor in the test socket. A photograph of this pulse waveform shall be taken and kept for reference; one picture shall be taken for each group tested.

a. Pretest - Set high voltage supply to zero. Wire all pins to ground. Insert device in test socket.

b. Set voltage level to +250 VDC. Change pin 1 from its ground connection to the output of the ESD simulation circuit. Apply stress to DUT. Reconnect pin 1 to ground and proceed to next pin. Repeat process until all pins are stressed.

c. Measure device DC electrical parameters at 25°C. If a pin has out of specification leakage, or is non-functional, remove it from further stress by disconnecting that pin from ground and do not connect that pin to the stress circuitry. Stop test on this device when half of the pins fail this criteria.

d. Repeat a. through c. with negative voltage at the same level.

e. Increment voltage upward in 250 volt steps and perform a. through d.

NOTE:

1. Value of R_1 shall have a minimum limit of 800 kohm, and a maximum limit of 3 Gohm; and be of a high voltage type.

2. All components, and interconnecting wiring shall have voltage and current rating greater than the maximum specified supply value. (NOTE: This does not apply to resistors).

3. Resistors R_2 and R_3 shall be a matched pair (within 10%), and noninductive, and high voltage withstanding.

4. Waveform shall be measured with a 100 MHz minimum oscilloscope (see note 5).

5. A high voltage, high impedance ($\geq$ 10 Mohm), low capacitance ($\leq$ 5 pF) probe shall be used when measuring pulse waveform.

6. Relay RS_1 contacts shall be of bounceless type (mercury wetted or equivalent), and have a dielectric breakdown voltage and current greater than the maximum specified voltage supply value.

7. Effective capacitance shall be determined by charging C_1 to 2,000 Vdc +5% and with no device in test socket and test switch open, discharging C_1 into an electrometer or coulometer connected between points A and B of Figure 2 and calculating effective capacitance which shall be 100 pf ± 10%. Effective insulation resistance for C_1 shall be 10^{10} ohms minimum.

8. All pins of DUT not associated with test procedure shall be connected to ground.

9. Resistor R_3 shall be placed in socket across terminals A and B only, when initially discharging circuit for waveform photograph (see 3). Test waveform only will be ≈ 50% Vp and ≈ $2t_d$.

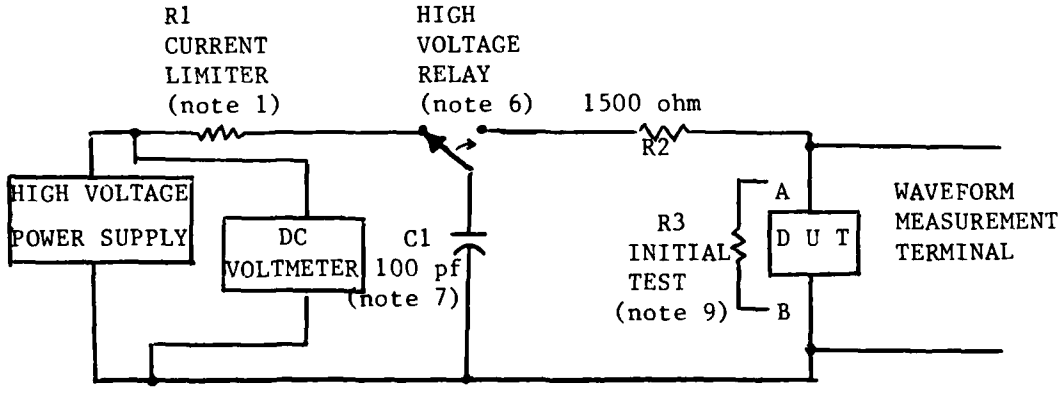


FIGURE 1 ESD Test Circuit

NOTES:

1. The rise time, tr, of the pulse voltage, Vp, shall be measured from 10% to 90% of the peak amplitude, Vpeak, and shall not exceed 15 nanoseconds.

2. The pulse decay across R_2 to ground shall be a single exponential waveform whose decay time, t_d, when measured between Vpeak and 36.8% Vpeak, is $R_2 \times C_1 \pm 10\%$, or ≈ 150 ns.

3. For initial waveform test only the voltage waveform will have the following characteristics: $V_p = 50\% \pm 15\%$ of voltages in the pulse decay time, t_d, will be $(R_2 + R_3) \times C_1$ or ≈ 300 ns.

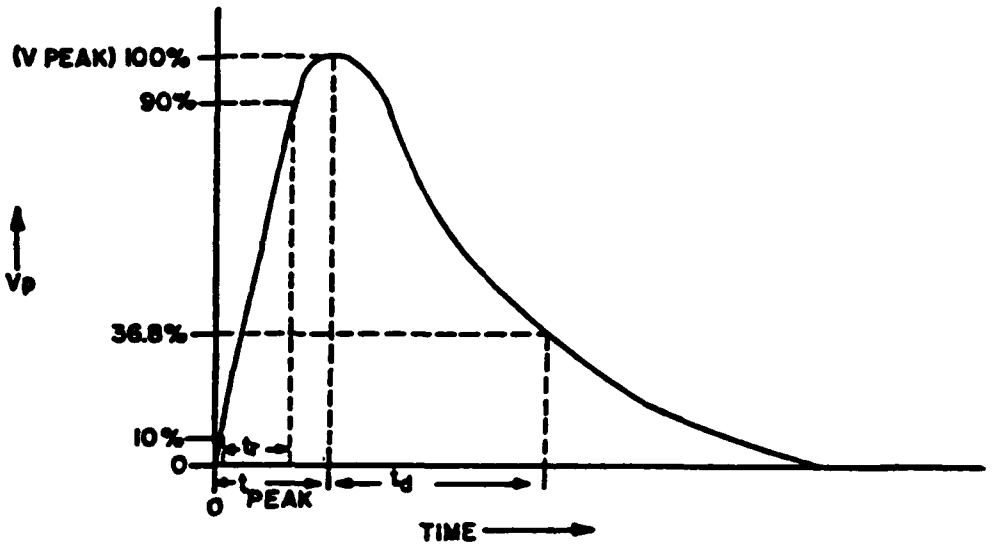


FIGURE 2 ESD Test Circuit Voltage Waveform

B. "Charged Device" Electrostatic Discharge Step Stress to Failure

Test Procedure

1. PURPOSE

This method establishes the means for measuring the level of a simulated electrostatic discharge stress required to produce a failure on a microelectronic circuit. This method will be used for analyzing the sensitivity level of each pin on a device and for quantifying the variation in sensitivity levels between pins.

The simulated electrostatic discharge stress utilized is a waveform similar to that illustrated in Figure 2 (Note 1). This is the "charged device" simulation which is designed to produce a waveform comparable to that which will occur it a part charged to a potential level comes into contact with an object at ground potential and the charge on the part is discharged into that object.

1.1 Definition - The following definition for the purpose of this Test Method shall apply:

1.1.1 Electrostatic Discharge (ESD) - An electrical current flow (induced by an electrostatic field) between two substances at different potentials.

2. APPARATUS

The apparatus required is an ESD simulation circuit similar to that shown in Figure 1 which will produce the waveform shown in Figure 2. This system should be capable of producing stress levels from -5,000 volts to +5,000 volts.

3. PROCEDURE

The pulse waveform and parameters as specified in Figure 2 (Note 3 only) shall be verified on the 100 pf test capacitor across a 1500 ohm resistor, using an oscilloscope. A photograph of this pulse waveform shall be taken and kept for reference; one picture shall be taken for each group tested.

a. Pretest - Set high voltage supply to zero. Place device on ground plane with leads facing upwards.

b. Set voltage level to +250 VDC. Connect charge/discharge wire to pin 1. Actuate relays to charge and discharge device. Move charge/discharge wire to next pin. Repeat process until all pins are stressed.

c. Measure device DC electrical parameters at 25°C. If a pin has out of specification leakage, or is non-functional, remove it from further stress. Stop test on this device when half of the pins fail this criteria.

d. Repeat a. through c. with negative voltage at the same level.

e. Increment voltage upward in 250 volt steps and perform a. through d.

NOTE:

1. Value of R_1 shall have a minimum limit of 200 Mohm, and a maximum limit of 3 Gohm; and be of a high voltage type.

2. All components, and interconnecting wiring shall have voltage and current rating greater than the maximum specified supply value. (NOTE: This does not apply to resistors).

3. Waveform shall be measured with a 100 MHz minimum oscilloscope (see note 4).

4. A high voltage, high impedance ($\geq$ 10 Mohm), low capacitance ($\leq$ 5 pF) probe shall be used when measuring pulse waveform.

5. Relay RS_1 and RS_2 contacts shall be of bounceless type (mercury wetted or equivalent), and have a dielectric breakdown voltage and current greater than the maximum specified voltage supply value. Relay RS_2 will close before RS_1 opens and will remain closed until RS_1 opens.

6. All pins of DUT not associated with test procedure shall be open.

7. Resistor R_2 shall be placed in socket across terminals A and B instead of the shorting bar and capacitor C_1 shall be placed from C to ground when initially discharging circuit for waveform photograph.

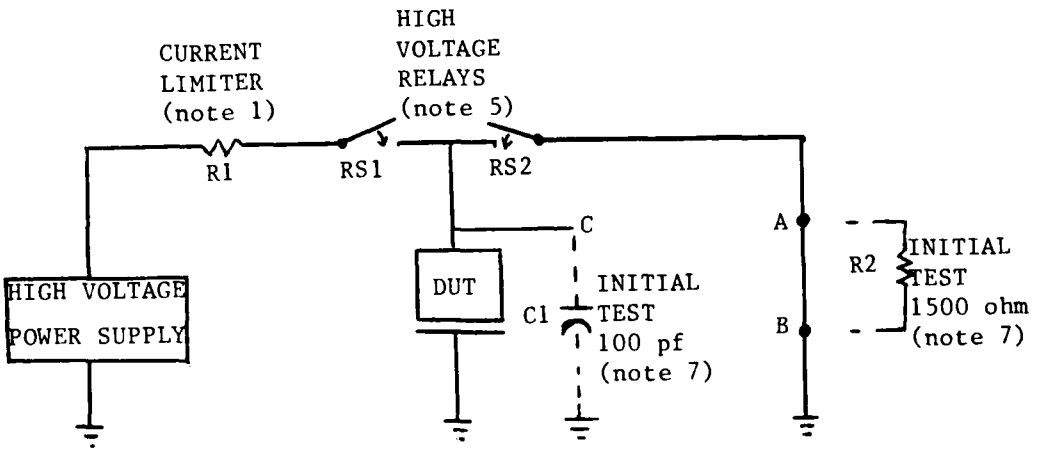


FIGURE 1 ESD Test Circuit

NOTES:

1. The waveform appearance during initial test is a damped sinusoid superimposed on an exponential. This is an underdamped case with $LC < 4R^2C^2$. Actual waveform will be the overdamped case since $LC > 4R^2C^2$ as R decreases.

2. This waveform will reach a peak higher than the input voltage level and will decay in approximately 150 nanoseconds.

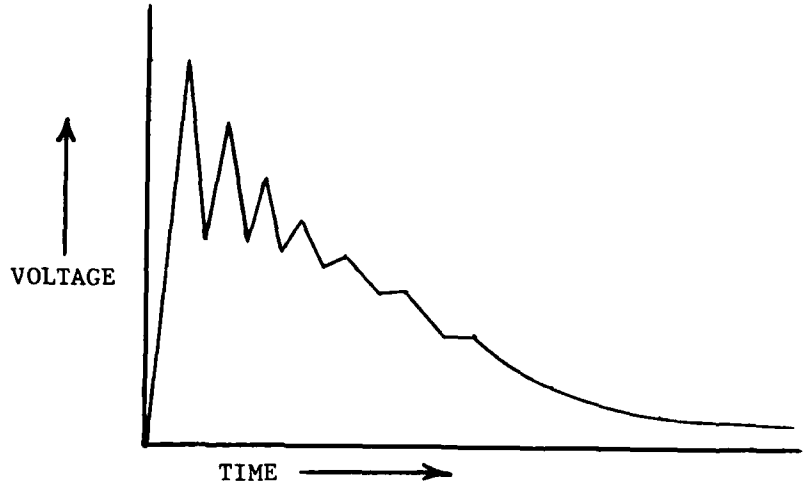


FIGURE 2 ESD Test Circuit Voltage Waveform

IV. TEST EQUIPMENT

The objective in the design of the test equipment was to allow easy and rapid testing of devices with up to 64 pins. The original idea was to build an automatic or semi-automatic system that would stress each pin in sequence. Discussions with persons that have attempted to build an automated system and research performed for this study, determined that this was not within the scope of this effort. The system shown in Figure IV-1 was developed to accomplish the testing. Additional apparatus is shown in Figure IV-2. The boards can handle standard dual-in-line packages from 14 to 64 pins.

The test tool has a variable supply from -5,000 volts to +5,000 volts. This allows parts to be taken in a step stress manner to failure rather than establishing just a fixed susceptibility level. The polarity is controlled by a switch on the front panel and the level is controlled by two sets of potentiometers, fine and coarse. The other control on the front panel switches the model from the human body discharge simulation (HBD) to the charged device (CD) simulation. The boards have parasitic capacitance of 9.1 pf, 10.4 pf and 13.2 pf going from the 20 pin fixture up to the 64 pin fixture. The bottom sides of the zero insertion force sockets and the first termination of the wires coming from the socket are coated with silastic-E, a high breakdown voltage, silicone potting compound. This combined with silicone rubber wiring eliminates the chance for corona discharge between adjacent pins. The stress application point is connected to the appropriate device pin by a shorting pin which slips through the top jack and board, a guide hole in the middle board and into a jack connected to a copper trace on the bottom PC board. The simulation circuit is the standard 100 pf, 1500 ohm RC discharge network. The risetime of the pulse was about 5 ns with no test board in place and about 15 ns with the 64 pin fixture. It was a repeatable exponentially decaying waveform with no apparent ringing (Figure IV-3). A single pin is connected to the discharge circuit. The remaining pins are connected to a trace that goes to ground via shorting pins.

The charged device model board is as shown on the right-hand side of Figure IV-2. The part is placed upside down on a piece of teflon glass tape (8 mil) that is attached to a copper clad PC board. The copper clad board is tied directly to ground and the part is connected through a silicone wire to the stress voltage. The entire device is slowly charged to a voltage level and is then shorted to ground. The short to ground is applied before the charging voltage is removed from the device and both switches are opened at the same time. The capacitances measured between the ground pin on each device and the copper plate were:

Device	Pins	Capacitance (pf)
Part G	64	34
Part E	40	19
Part A	40	18
Part H	40	16
Part B	24	11
Part C	20	8
Part D	20	6
Part F	18	5

To allow examination of the signal for the charged device model a plate was constructed which measured 100 pf when placed on the fixture. This had a pin which was connected to the stress circuit and a 1500 ohm resistor was used between the relay and ground. The waveform was measured across this resistor. This waveform is as shown in Figure IV-4. The ringing is due to the inductance of the discharge circuitry.

The schematic for the test tool is shown in Figure IV-5. The two time delay relays were designed into the circuit to allow control of the timing between the activation of the first mercury displacement relay and the activation of the second mercury displacement relay. Analysis with devices in the charged device circuit found that it was necessary to have the second relay discharge the device to ground prior to the first relay opening. The non-inductive 100 megohm resistor was placed between the two relays to provide additional current limiting and isolation between the device under test and the first relay.

The test tool operation is as follows:

General

1. Connect power cord to 120 VAC.
2. Set front panel rocker arm switch to ON.
3. Set voltage controls to zero (Counterclockwise).

Human Body Discharge

1. Set test switch to human body discharge.
2. Place test fixture on test tool (20, 40 or 64 pin).
3. Place part (D.U.T.) in test fixture.
4. Select pin to receive stress by connecting to inside (red) track.
5. Connect remainder of pins to ground (black).
6. Set polarity and voltage level, set voltage level of polarity not used to zero.
7. Press stress button and hold for 1 second.
8. Repeat steps 4 - 7 at next pin.

Charged Device Model

1. Set test switch to charged device model.
2. Place CDM test fixture on test tool.
3. Place part (D.U.T.) on test fixture with legs pointing upward.
4. Connect wire to pin to be stressed.

5. Set polarity and voltage level, set voltage level of polarity not used to zero.

6. Press stress button and hold for 1 second.

7. Repeat steps 4 - 6 at next pin.

The parts utilized for this test equipment are as follows:

Test Tool Parts List

Name	Number	Manufacturer
Slant Front Cabinet	DSSF-10506	Buckeye
Mercury Displacement Relay	WM35A-120A	Magnecraft
Digital Panel Meter	RM-452TB/DC	Non-Linear Systems
72 Volt Unregulated Power Supply	U72Y25	Acopian
Positive High Voltage Power Supply	PMT-50A-P	Bertan
Negative High Voltage Power Supply	PMT-50A-N	Bertan
High Voltage Relay	24HV1A-75	Douglas Kandall
On Delay Timer	SSC12AAA	Beabout
24 Volt Power Supply	524H1-C	EKA Transpac
Potentiometer, 100 ohm, 10 turn	3540S-1-101	Bournes
Potentiometer, 5000 ohm, 10 turn	3540S-1-502	Bournes
High Voltage Silicone Wire	37F2103	Dearborn
Resistor, 100 Megohm	ROX-1	Dale Electronics
On/Off Switch	35-620	GC Electronics
Resistor, 1500 ohm	FERW	Dale Electronics
High Voltage Ceramic Disc Capacitors	DD60-XXX	Centralab
Interval Timer	SSC52AAA	Beabout
Momentary Switch	35-844	GC Electronics
DPDT Switches	35-138	GC Electronics
Silicone Potting	E	Dow Corning
Connector	143-012-01	Amphenol
Fuse	1 amp	
Power Cord	3 Prong	

Test Board Parts List

Name	Number	Manufacturer
Copper Clad PC Boards	22-263	GC Electronics
Shorting Pins	Custom	LVC Industries
Horizontal Jacks, Red	105-0752-001	E.F. Johnson
Horizontal Jacks, Black	105-0753-001	E.F. Johnson
Zip Dip Socket, 64 Pin	264-4493-00-0602	Textool
Zip Dip Socket, 40 Pin	240-3346-00-0605	Textool
Zip Dip Socket, 20 Pin	220-3342-00-0605	Textool
Banana Jacks	Male	-
Teflon/Glass Tape	6085-06	Taconic

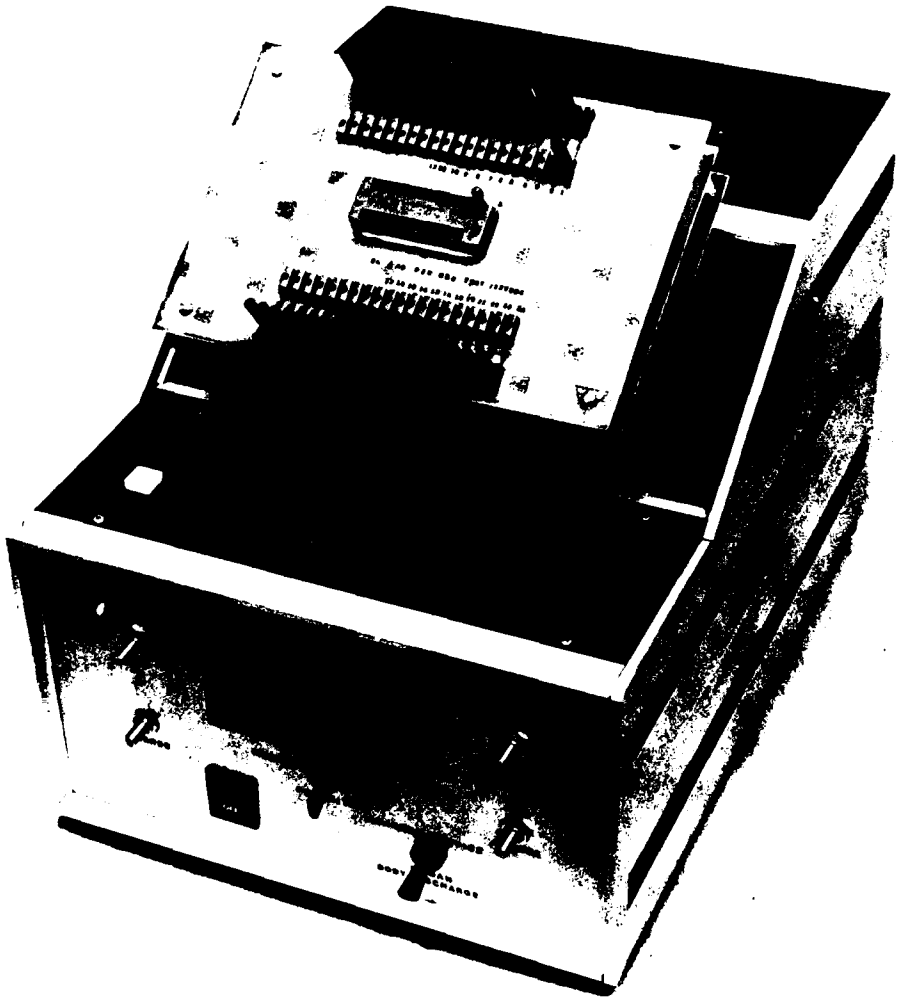


Figure IV-1 - ESD Simulation Test Tool.

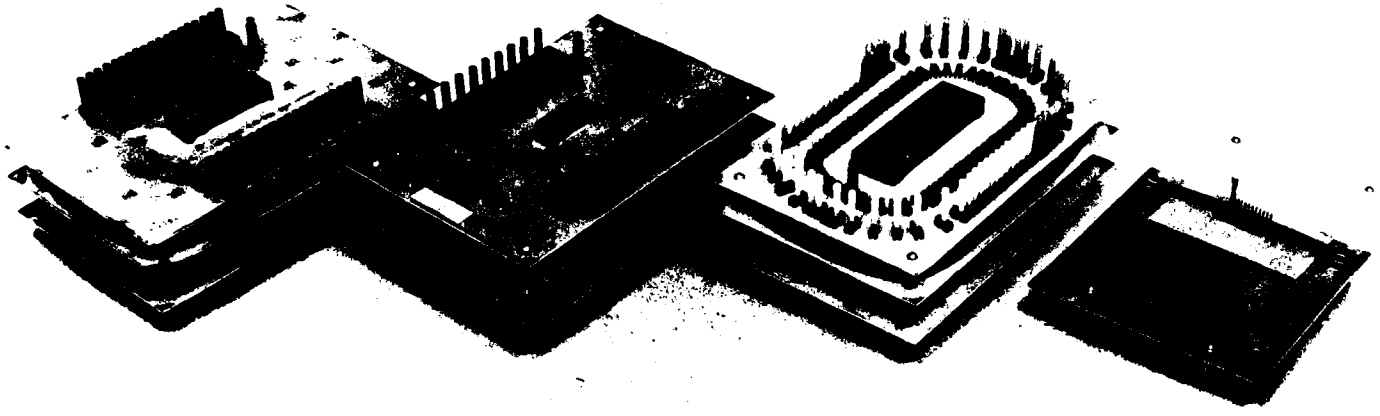


Figure IV-2 - ESD Test Fixtures.

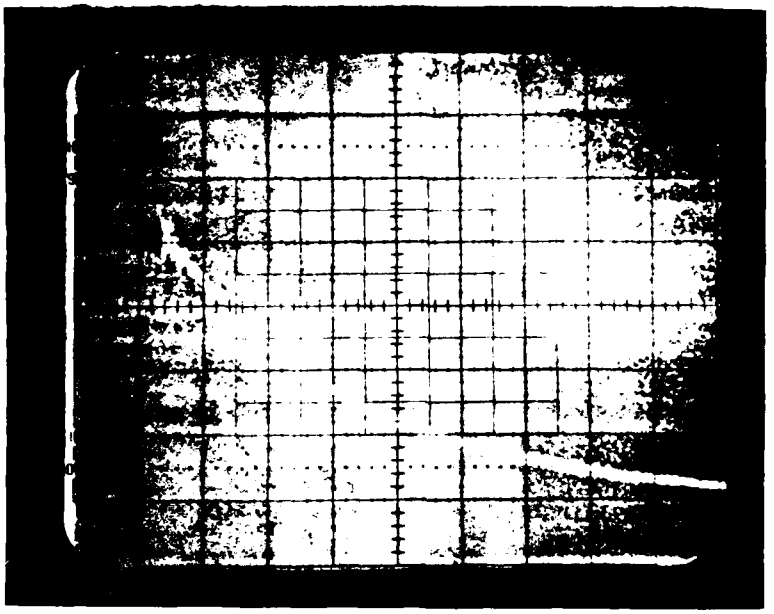


Figure IV-3 - Human Body Simulation ESD Test Waveform, 200 volts/div, 100 nanoseconds/div.

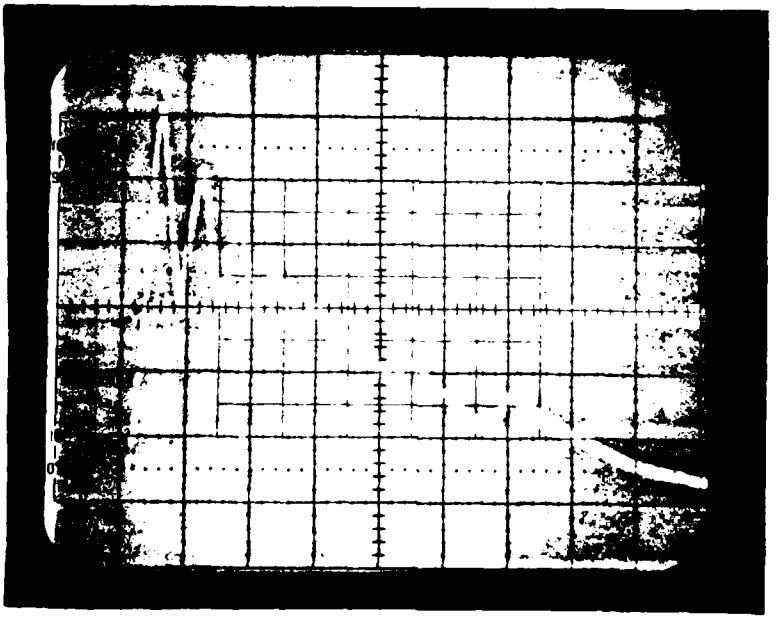


Figure IV-4 - Charged Device Simulation ESD Test Waveform, 100 volts/div, 50 nanoseconds/div.

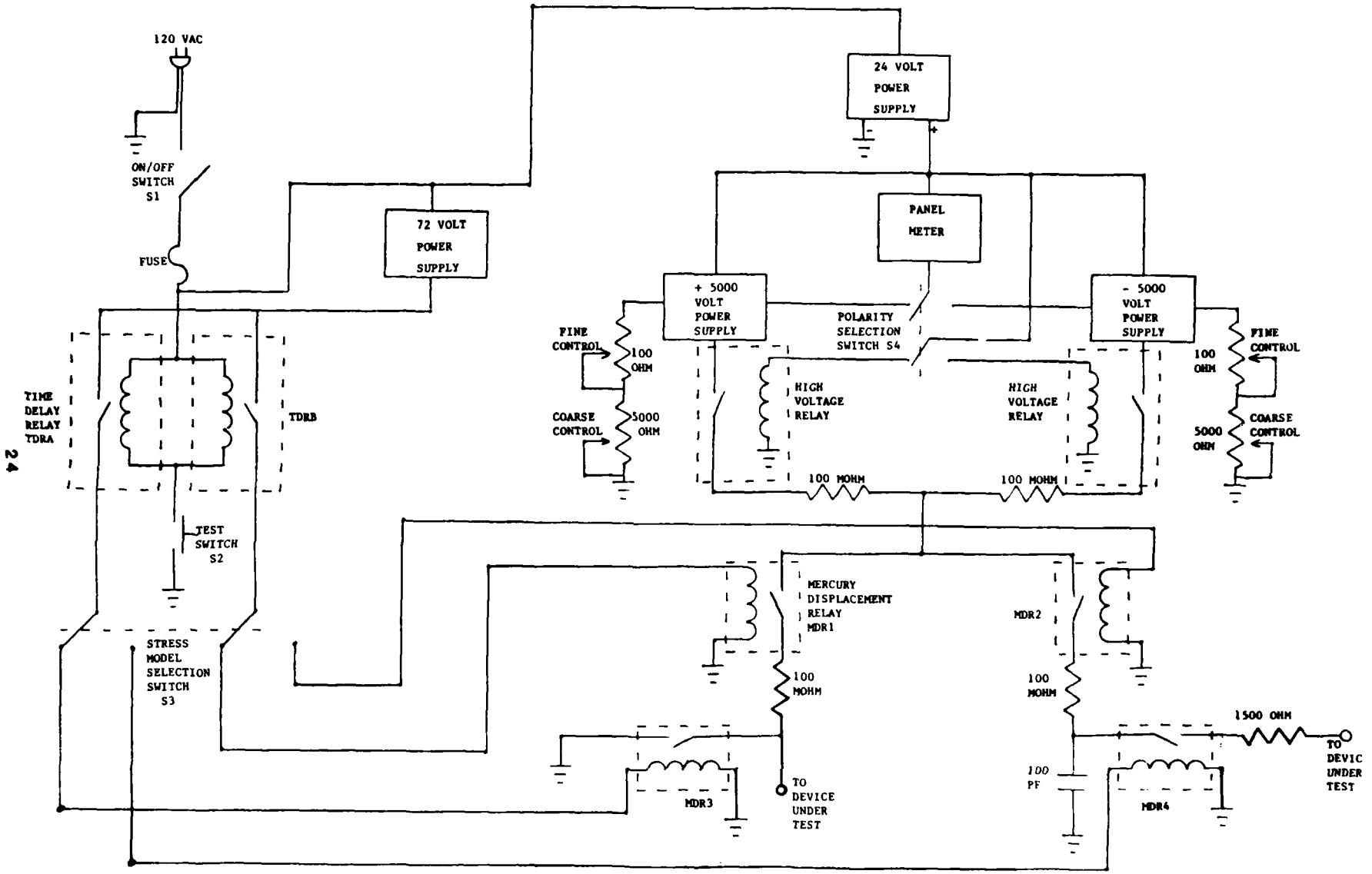


FIGURE IV-5 ESD Test Tool Schematic

V. DEVICE CHARACTERIZATION AND TESTING

Parts were selected for this study to provide a variety of technologies, functional types, and manufacturers. Within these constraints, parts with the finest linewidths were selected. The table below lists the parts chosen. Thirty-five devices of each group were ordered, providing 5 devices for physical analysis, control parts and test set up. The remaining thirty parts were divided into two groups of fifteen parts each for the two ESD simulation models.

Device	Function	Technology
Part A	1K RAM, I/O, Timer	CMOS
Part B	8K Static RAM	NMOS
Part C	Octal Latch	Schottky
Part D	Octal Latch	Schottky
Part E	2K RAM, I/O, Timer	NMOS
Part F	4K Static RAM	CMOS
Part G	Microprocessor	NMOS
Part H	Microprocessor	NMOS

The parts chosen included six MOS devices and two bipolar devices. This ratio was picked due to the greater sensitivity of MOS devices and due to the smaller dimensions generally available. NMOS was the most common technology chosen due to the number of small geometry LSI and VLSI circuits in this category. The Schottky parts were included to obtain a bipolar part in the study and due to its reported sensitivity to ESD. The difference in failure mechanisms and ESD model sensitivity was also considered. These Schottky devices were the simplest circuits functionally. The specific functional types were kept to four to allow intercomparisons between manufacturers, technologies, and function.

Characterization was performed on each of the eight devices. This characterization included schematic development of the interface circuits, electrical measurement of these components, measurement of dimensions, and microsections.

The same procedure was followed on each device. The package was opened and the die was examined on the light microscope at 50X to 600X. The general layout of the supply metallizations was traced. The layout of the circuitry for each of the other pins was examined. Variations in the layout or the appearance of the circuitry were noted at this time and specific pins were selected for schematic development. The schematics were developed for a typical input, typical output, and for a portion of the circuitry connected to the supply lines (V+, V- and ground). If variations in the electrical schematic were evident, then the schematic for each type was developed.

The glass passivation was stripped as necessary to allow examination and identification of the circuit components.

A minimum of one device of each type was microsectioned. These microsections were performed through areas that provided information related to the failure modes.

Each of the eight parts will be discussed individually. These are included in sections A through H which follow.

A. Part A Analysis

This device is a RAM-I/O-Timer fabricated using a P^2CMOS silicon gate technology. This device has 1024 bits of static RAM (128 x 8), 22 programmable I/O ports, and two programmable 16-bit binary counters.

These devices have one layer of metallization and two layers of polysilicon. This was in a 40-pin dual-in-line metal lid ceramic package. An overall die photo is shown in Figure V.A.1. VCC is pin 40 at the top of Figure V.A.1 and VSS is pin 20 at the bottom. VCC is also connected to the package substrate via a bond wire. VCC is distributed around the perimeter of the die by both a polysilicon stripe and an overlying metallization stripe. VSS traverses around the die on the inside edge of the bond pads.

The VCC bond pad is shown in Figure V.A.2. It is connected to the substrate, to the body connection for the N-Channel MOS transistors, and to the sources of the P-Channel MOS transistors.

The VSS bond pad is shown in Figure V.A.3. This metallization is connected to the body connection of the P-Channel MOS devices and to the sources of the N-Channel MOS devices.

An input structure is shown in Figure V.A.4 and the schematic is shown in Figure V.A.5. This structure has diodes to both VCC and VSS as shown. The junction breakdown of each of these diodes and of the drain to body junction on the N-Channel and P-Channel FETs is about 30 volts. The gate dielectric breakdown was 70 volts . The input protect resistor is polysilicon and the connections to the protect diodes comes from the point at which the resistance measurement was taken.

An input/output structure is shown in Figure V.A.6 and the schematic is shown in Figure V.A.7. The input protect diodes are incorporated into the output transistors rather than being separate components. The output is the standard CMOS configuration. The output only pins had protect diodes present. An example is shown in the photograph in Figure V.A.8 and the schematic in Figure V.A.9.

The schematics for each of the inputs and I/O combinations were identical, however the protect resistor, protect diodes and output transistor layouts varied slightly.

Microsections were performed through the input/output sections. This appeared to be the standard CMOS process with an n-type substrate. The thicknesses measured were: polysilicon = 0.35 microns, metallization = 1.2 microns, p diffusion for N-Channel body = 8 microns, n+ and p+ diffusions = 1 micron, dielectric between two polysilicon layers = 0.1 microns, dielectric between polysilicon and aluminum = 1.0 microns.

The standard CMOS processing along with a top and side view of a section through an input/output is shown in Figure V.A.10.

Electrical Test

Electrical testing was performed on the Tektronix 3260 after each stress. This testing consisted of V_{OH}, V_{OL}, I_{OL} and I_{IL}. A sample printout of the initial electrical test is provided in Figure V.A.11. This same serial number is shown in Figure V.A.12 following the -1500 volt stress. I_{IL} and I_{OL} provided information on the gradual degradation of the inputs and output.

This testing also provided a functional check of the following. The control logic (CE, WR, RD, IOT/M, ALE, and RESET), ports and associated data direction registers, and the address/data buffers and latches were tested for operation in their various modes. The mode definition register, the handshake logic, T0 high and low order registers, and the T0 prescale and command registers were partially tested. One 8 bit wide section of the 128 section RAM was accessed. The T1 high and low order registers, and the T1 prescale and command registers were not accessed.

Charged Device Data Analysis

Serial numbers 17 through 31 were subjected to the charged device model of ESD stress. Device damage occurred at low voltage levels with 5 devices being removed from stress following the +750 volt stress and the remaining parts being removed from test following the -750 volt stress.

The parameter which changed first with the stress was the I_{IL} reading. This parameter did not degrade through the nanoamp region as was experienced with Part B but went to high microamps or milliamps at first indication of failure. A summary of the pins that failed this parameter and the level at which this occurred is shown in Figure V.A.13. The pin 9 failures occurred at the first stress point and pin 3 failures occurred at the second stress point. As the pins failed they were removed from further stress. Pin 9 was the RD-not input which enables AD0-AD7. When pin 9 failed the I_{IL} test, a functional failure of V_{OH} and V_{OL} occurred on these eight pins. Other functional failures occurred related to damage at other inputs.

All of the devices were opened and analyzed. There was more damage present than had been expected from the leakage current measurements. The amount of damage explained the reason for the loss of functionality on the parts. Each device was examined and some mechanical probing and measurements were done to verify the visual indications.

The seven input pins are shown in Figures V.A.14 - V.A.20. Pins 4 and 11 have similar layout configurations, and pins 7, 8, and 10 have similar configurations. Pins 3 and 9 were different than the rest. They are shown in Figures V.A.19 and V.A.20 and have a condition which made them more susceptible to damage. Within close proximity to the input polysilicon resistor there was another polysilicon stripe.

On pin 3 the polysilicon stripe ran parallel to the input polysilicon. This parallel stripe was just a continuation of the input resistor, however, during stress a potential level would develop between these two stripes and a breakdown would occur. Electrically this created leakage down to the substrate or up to overlying metallization.

Pin 9 had a layout like pin 4 and 11 except for a polysilicon stripe that ran underneath the input resistor. This created the most easily damaged input structure.

Eight devices were categorized for failure mode appearance. These were serial numbers 17, 19, 20, 27, 28, 29, 30, and 31. The pins which had similar layouts exhibited similar damage. Pins 4 and 11 were by far the least damaged. No damage or only slight damage was seen on pin 4 on 5 of the devices. No damage or only slight damage was seen on pin 11 on 3 of the devices. The type of damage seen is shown in Figures V.A.21 - V.A.33. Pin 7, 8, and 10 were visibly damaged on all parts. This damage was generally in the bottom of the U-shaped portion of the polysilicon resistor. Several of these are shown in Figures V.A.25 - V.A.28. Two other damage conditions were seen. On serial numbers 27, 28, 30 and 31 damage occurred at the first contact point between polysilicon and metallization (Figure V.A.29). This may have been due to a resistive contact at that point. On serial number 28 pin 10, a breakdown through the thermal oxide occurred. There was likely a defect in the oxide at that point (Figure V.A.30). The failures on pin 3 appeared as shown in Figures V.A.31 and V.A.32.

The stress on pin 9 was stopped after a single application of +250 volts. Shorts were created between the two polysilicon stripes, however, there was no visible damage on 6 of the devices. Damage which was visible on the other devices is as shown in Figure V.A.33.

The charged device model stress was found to cause damage to all of the input circuits and none of the output circuits. In electrical testing pins 9 and 3 showed up first. These pins could be made less sensitive by a minor layout change. The best configuration to use if a polysilicon resistor is incorporated into the protection network is a straight run since damage occurred first at corners.

Human Body Discharge Data Analysis

Serial numbers 2 through 16 were subjected to the human body ESD simulation test method. Device damage was measurable electrically following the -250 volt stress. The first device was removed from test after the -750 volt stress and all devices were failed after the -1500 volt stress.

A summary of the cumulative leakage failures is shown in Figure V.A.34. Pin 9 was the most sensitive to stress followed by pin 3. Pins 3, 7, 8, 9, 10 and 11 are inputs and pins 19, 27 and 33 are input/outputs. Failure analysis on serial number 3 which had the failures on pins 10, 27 and 33 found that pins 27 and 33 were related to the state the output was being driven to during the measurement, rather than an actual failure in the output.

All devices were visually examined and eight of these were categorized. There was no output damage visible and the inputs were damaged as shown in Figure V.A.35. A subjective analysis of the visible surface damage was performed and the pins classified. The classification of open meant polysilicon open, short meant breakdown between two polysilicon stripes, slight damage meant minor indications of heating such as discoloration or small cracks, and damage meant significant physical damage to the polysilicon but not to the point of open.

Figure V.A.35 shows that parts that were taken through -1500 volt stress generally failed with open polysilicon. The part that was stopped at -750 volts showed only slight visible damage. These results indicate that polysilicon does degrade partially at low stress levels, however, there is no way to monitor that using external measurements. The probable change which occurs is an increase in resistance.

Photographs of the damage are shown in Figures V.A.36 - V.A.42. Figure V.A.36 shows pin 3 damage. There is a breakdown between the two adjacent polysilicon stripes and also some small cracks which ran parallel to the resistor. Figure V.A.37 shows the type of slight damage that was seen. This is pin 4 and there are small cracks in the resistor. Figure V.A.38 shows a polysilicon open on pin 4. Figure V.A.39 shows a polysilicon open on pin 7. Figure V.A.40 shows a polysilicon open on pin 10. Figures V.A.41 and V.A.42 shown opens on pin 11. All of the opens shown occur immediately before the contact window to the protect diodes. This may indicate a current crowding effect causing the heating.

The failure modes seen are different for the two stress modes. The human body discharge stress required a higher voltage however when the parts failed more severe damage was done. The location of the damage was repeatable within the two stress groups but was slightly different when comparing between the two groups. This difference is likely related to pulse duration and the polysilicon heating which occurs.

The subcatastrophic damage that occurs at low levels to the polysilicon makes it possibe for latent problems to exist. This has not been proven but is a concern. The use of polysilicon stripes in the input sections does not appear to be desirable. A latent defect study on parts which are stressed below the catastrophic level could provide this information. An ESD stress test followed by a dynamic life test would be a method to investigate this concern.

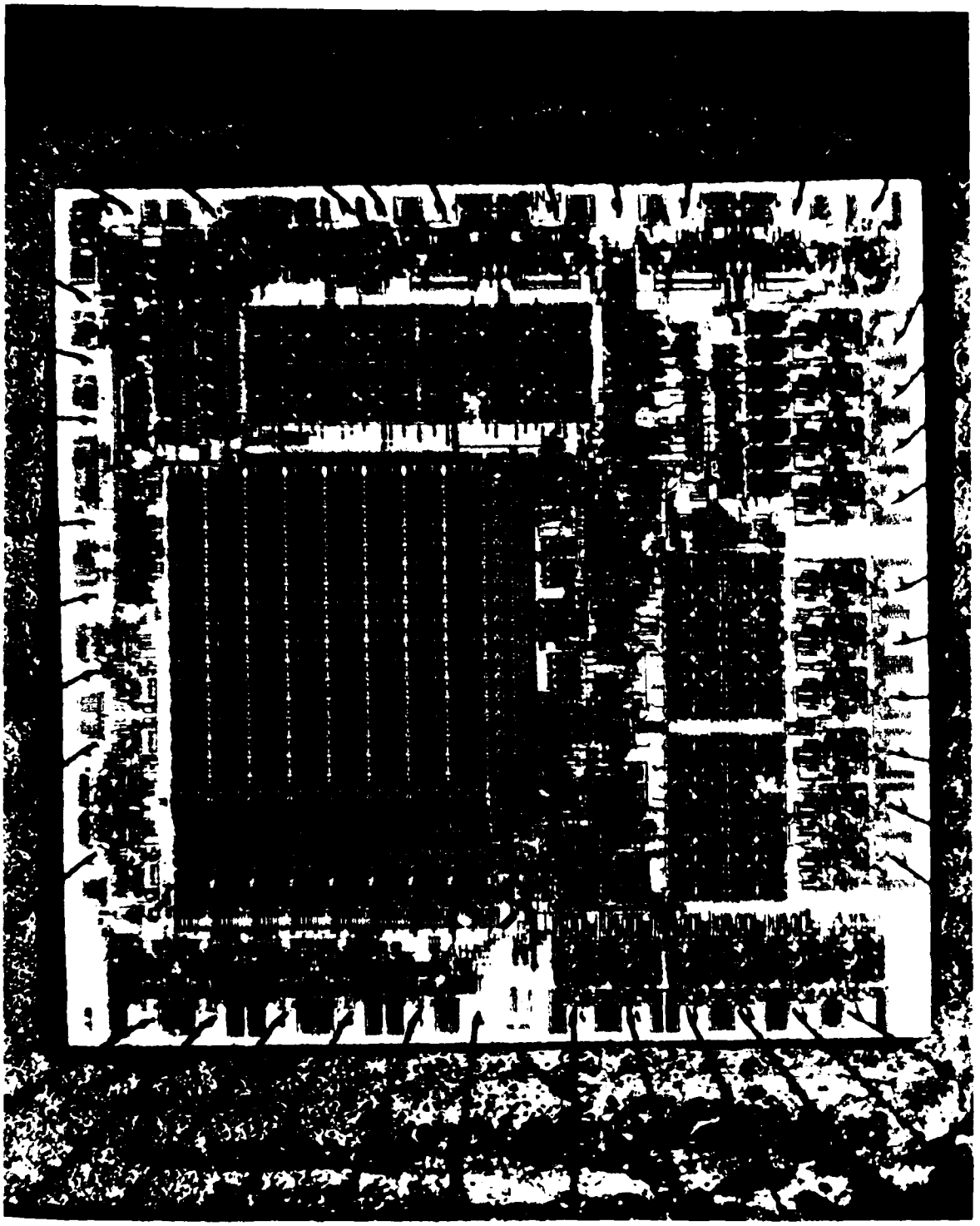


Figure V.A.1 - Overall Die Photograph

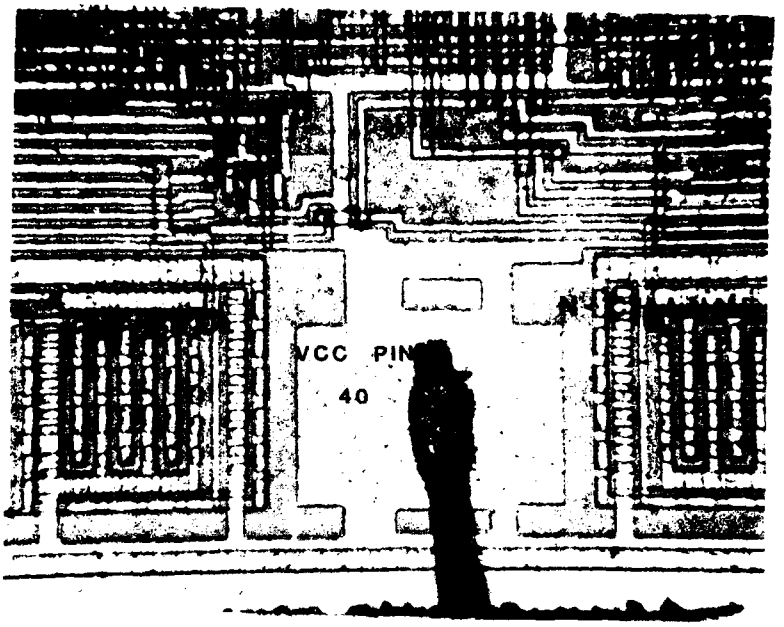


Figure V.A.2 - VCC Bond Pad and Connections

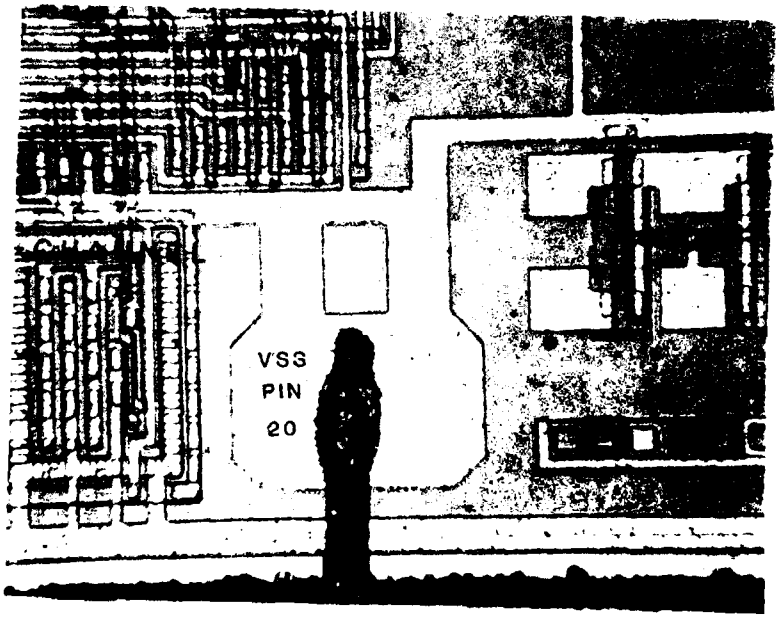


Figure V.A.3 - VSS Bond Pad and Connections

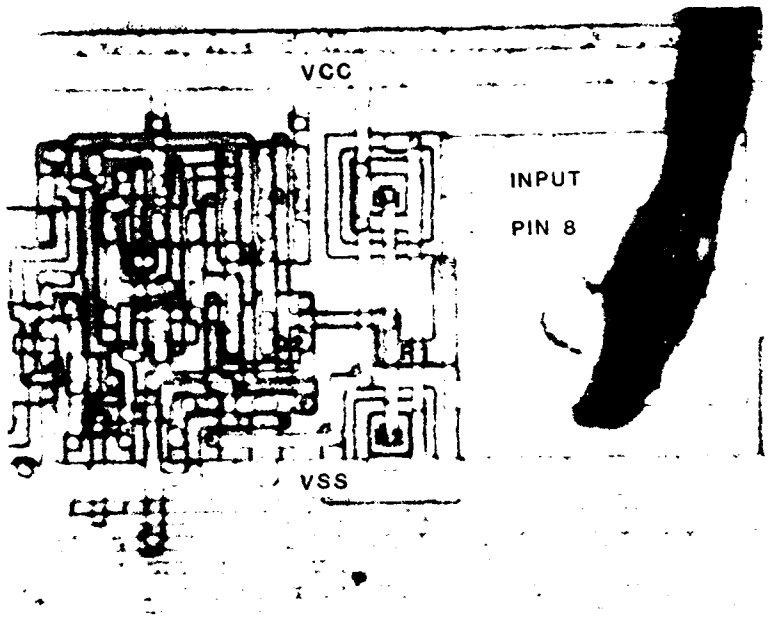


Figure V.A.4 - Pin 8 Input

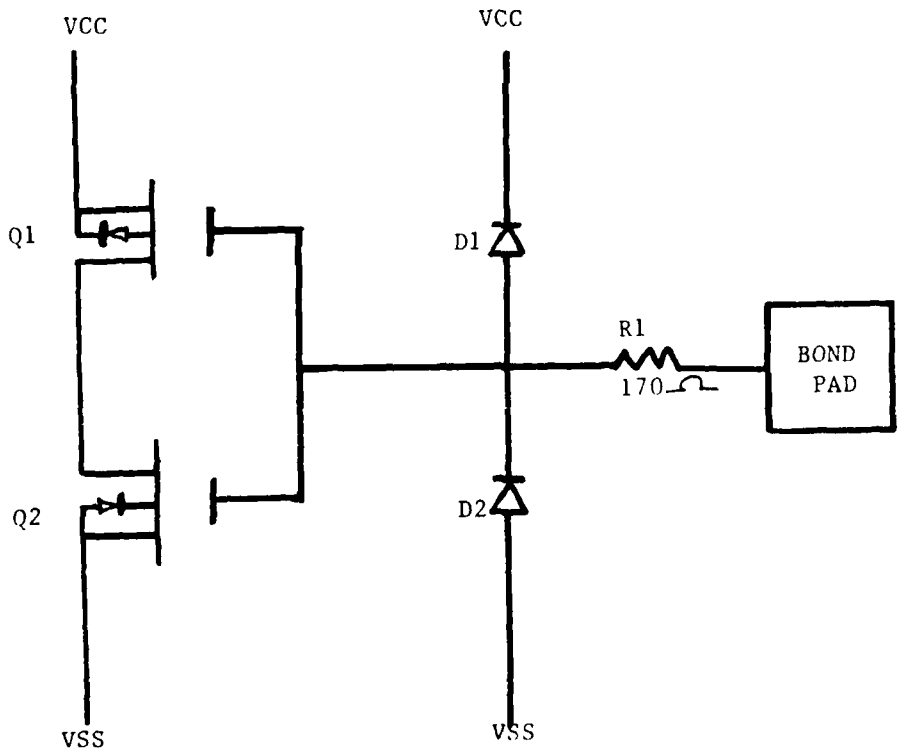


Figure V.A.5 - Input Schematic

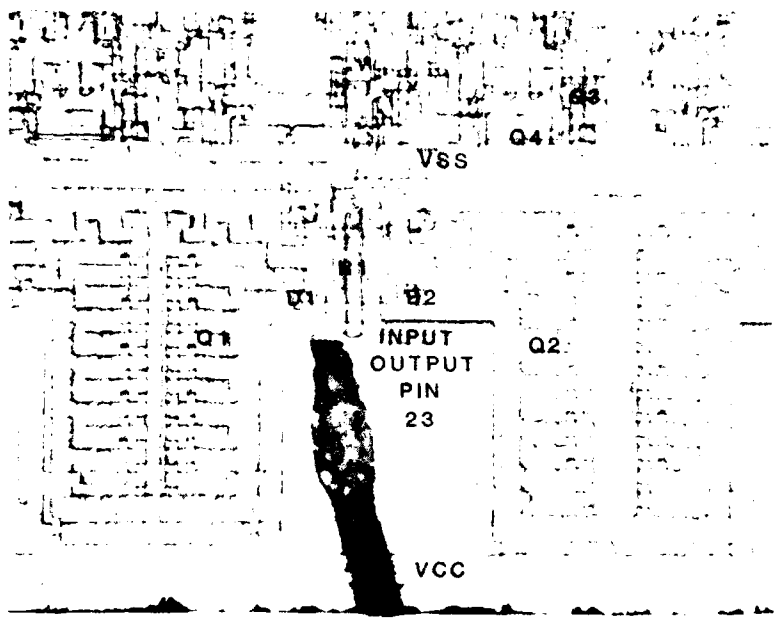


Figure V.A.6 - Pin 23 Input/Output

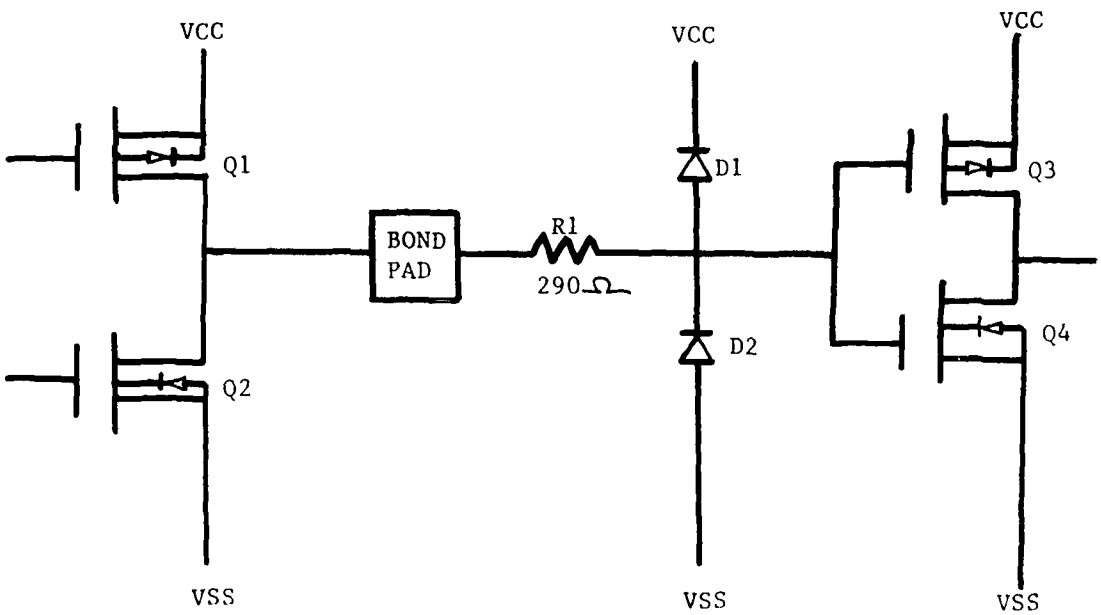


Figure V.A.7 - Input/Output Schematic

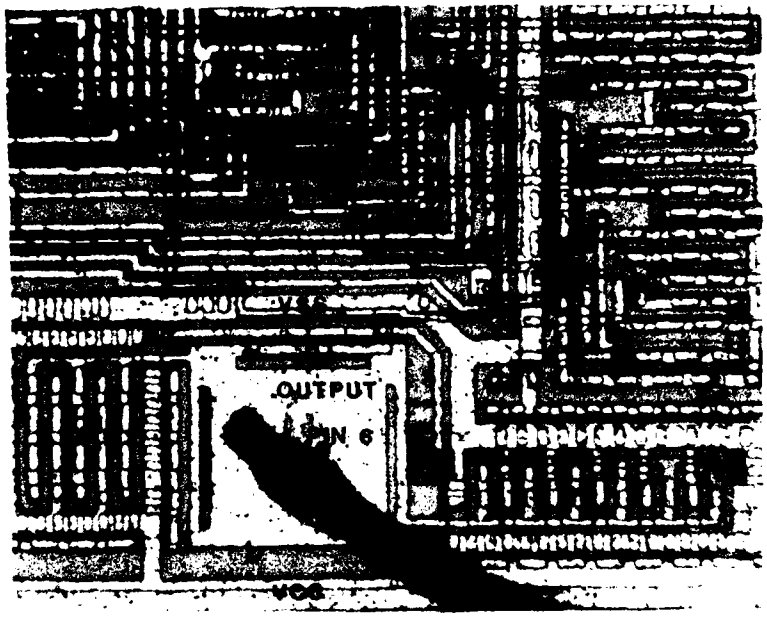


Figure V.A.8 - Pin 6 Output

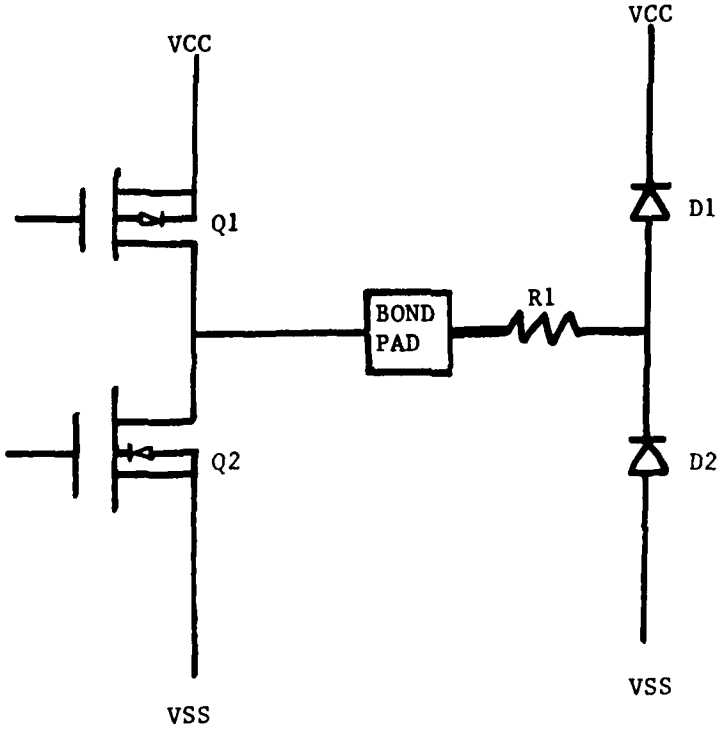


Figure V.A.9 - Output Schematic

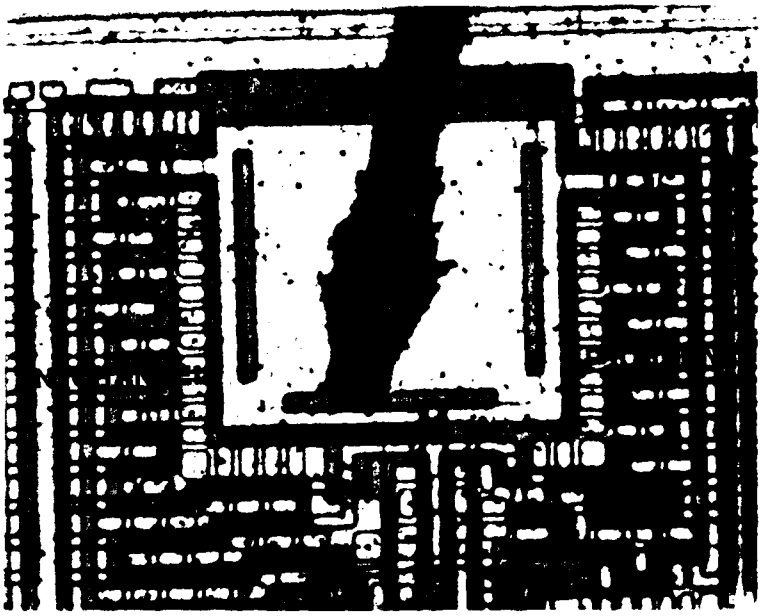


Figure V.A.10 - A. Input/Output Surface Layout

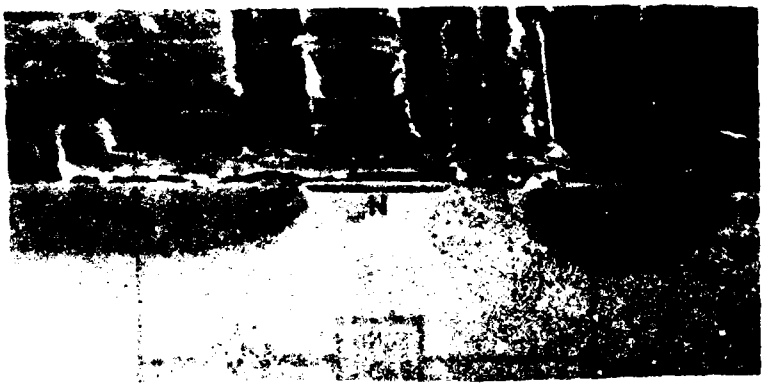


Figure V.A.10 - B. Cross-section Through Area Marked in A

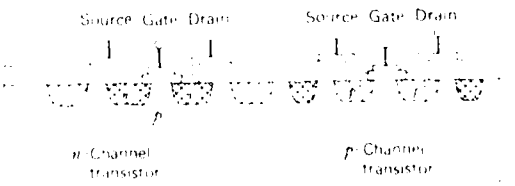


Figure V.A.10 - C. CMOS Structure

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

PART NUMBER - FILE UID :149 SERIAL NUMBER - 5
TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 14 JUL 83 AT 12:55:32 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.365 V	2.400 V	--
	VOH1 - - - - - -	4.365 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.360 V	2.400 V	--
	VOH1 - - - - - -	4.365 V	2.400 V	--
	VOH1 - - - - - -	4.365 V	2.400 V	--
	VOH1 - - - - - -	4.365 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH1 - - - - - -	4.355 V	2.400 V	--
	VOH1 - - - - - -	4.350 V	2.400 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.490 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.490 V	4.000 V	--
	VOH2 - - - - - -	4.490 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--
	VOH2 - - - - - -	4.495 V	4.000 V	--

Figure V.A.11 - Initial Electrical Test

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO. 1 ELECTRICAL

ON 14 JUL 83 AT 12:56:04 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	VOH2	- - - - - - -	4.490 V	4.000 V	--
	VOH2	- - - - - - -	4.490 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.490 V	4.000 V	--
	VOH2	- - - - - - -	4.490 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.495 V	4.000 V	--
	VOH2	- - - - - - -	4.490 V	4.000 V	--
	VOL1	- - - - - - -	114.0mV	--	400.0mV
	VOL1	- - - - - - -	106.5mV	--	400.0mV
	VOL1	- - - - - - -	105.0mV	--	400.0mV
	VOL1	- - - - - - -	84.50mV	--	400.0mV
	VOL1	- - - - - - -	85.50mV	--	400.0mV
	VOL1	- - - - - - -	85.50mV	--	400.0mV
	VOL1	- - - - - - -	84.00mV	--	400.0mV
	VOL1	- - - - - - -	83.50mV	--	400.0mV
	VOL1	- - - - - - -	83.50mV	--	400.0mV
	VOL1	- - - - - - -	85.50mV	--	400.0mV
	VOL1	- - - - - - -	86.00mV	--	400.0mV
	VOL1	- - - - - - -	86.50mV	--	400.0mV
	VOL1	- - - - - - -	88.00mV	--	400.0mV
	VOL1	- - - - - - -	87.50mV	--	400.0mV
	VOL1	- - - - - - -	89.00mV	--	400.0mV
	VOL1	- - - - - - -	91.00mV	--	400.0mV
	VOL1	- - - - - - -	92.00mV	--	400.0mV
	VOL1	- - - - - - -	98.00mV	--	400.0mV
	VOL1	- - - - - - -	98.50mV	--	400.0mV
	VOL1	- - - - - - -	98.50mV	--	400.0mV
	VOL1	- - - - - - -	97.00mV	--	400.0mV
	VOL1	- - - - - - -	96.50mV	--	400.0mV
	VOL1	- - - - - - -	97.50mV	--	400.0mV
	VOL1	- - - - - - -	99.50mV	--	400.0mV
	VOL1	- - - - - - -	97.50mV	--	400.0mV
	VOL1	- - - - - - -	118.0mV	--	400.0mV
	VOL1	- - - - - - -	119.0mV	--	400.0mV
	VOL1	- - - - - - -	126.0mV	--	400.0mV
	VOL1	- - - - - - -	127.0mV	--	400.0mV
	VOL1	- - - - - - -	122.0mV	--	400.0mV
	VOL1	- - - - - - -	117.0mV	--	400.0mV
	VOL2	- - - - - - -	2.100mV	--	100.0mV
	VOL2	- - - - - - -	1.950mV	--	100.0mV
	VOL2	- - - - - - -	2.000mV	--	100.0mV
	VOL2	- - - - - - -	1.300mV	--	100.0mV

Figure V.A.11 - Initial Electrical Test (Cont.)

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO. 1 ELECTRICAL

ON 14 JUL 83 AT 12:56:35 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	VOL2	- - - - - - -	1.000MV	--	100.0MV
	VOL2	- - - - - - -	800.0UV	--	100.0MV
	VOL2	- - - - - - -	600.0UV	--	100.0MV
	VOL2	- - - - - - -	500.0UV	--	100.0MV
	VOL2	- - - - - - -	600.0UV	--	100.0MV
	VOL2	- - - - - - -	650.0UV	--	100.0MV
	VOL2	- - - - - - -	950.0UV	--	100.0MV
	VOL2	- - - - - - -	1.250MV	--	100.0MV
	VOL2	- - - - - - -	800.0UV	--	100.0MV
	VOL2	- - - - - - -	750.0UV	--	100.0MV
	VOL2	- - - - - - -	500.0UV	--	100.0MV
	VOL2	- - - - - - -	750.0UV	--	100.0MV
	VOL2	- - - - - - -	1.000MV	--	100.0MV
	VOL2	- - - - - - -	1.100MV	--	100.0MV
	VOL2	- - - - - - -	750.0UV	--	100.0MV
	VOL2	- - - - - - -	800.0UV	--	100.0MV
	VOL2	- - - - - - -	750.0UV	--	100.0MV
	VOL2	- - - - - - -	700.0UV	--	100.0MV
	VOL2	- - - - - - -	700.0UV	--	100.0MV
	VOL2	- - - - - - -	1.000MV	--	100.0MV
	VOL2	- - - - - - -	1.100MV	--	100.0MV
	VOL2	- - - - - - -	900.0UV	--	100.0MV
	VOL2	- - - - - - -	950.0UV	--	100.0MV
	VOL2	- - - - - - -	3.650MV	--	100.0MV
	VOL2	- - - - - - -	3.400MV	--	100.0MV
	VOL2	- - - - - - -	3.350MV	--	100.0MV
	VOL2	- - - - - - -	3.400MV	--	100.0MV
	IIL	- - - - - - -	2.200NA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	1.700PA	-1.000UA	1.000UA
	IIL	- - - - - - -	200.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.850NA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	950.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	500.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.600NA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	1.100NA	-1.000UA	1.000UA
	IIL	- - - - - - -	400.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.600NA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	1.100NA	-1.000UA	1.000UA
	IIL	- - - - - - -	450.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	300.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	300.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	400.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.750NA	-1.000UA	1.000UA
	IIL	- - - - - - -	900.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	800.0PA	-1.000UA	1.000UA

Figure V.A.11 - Initial Electrical Test (Cont.)

FILE NO. 119 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 14 JUL 83 AT 12:57:09 WITH THE 3340 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	IIL	- - - - - -	1.150NA	-1.000UA	1.000UA
	IIL	- - - - - -	400.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - -	500.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	-100.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.800NA	-1.000UA	1.000UA
	IIL	- - - - - -	-650.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	-600.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	-900.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.700NA	-1.000UA	1.000UA
	IIL	- - - - - -	-850.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.700NA	-1.000UA	1.000UA
	IIL	- - - - - -	-800.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.500NA	-1.000UA	1.000UA
	IIL	- - - - - -	-950.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.500NA	-1.000UA	1.000UA
	IIL	- - - - - -	-850.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.050NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.050NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.250NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.000NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.150NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.000NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.350NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.900NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.500NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.450NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.900NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	2.000NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.650NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.950NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.550NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.850NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.450NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.900NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.950NA	-1.000UA	1.000UA

Figure V.A.11 - Initial Electrical Test (Cont.)

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO. 1 ELECTRICAL

ON 14 JUL 83 AT 12:57:43 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	IOL	- - - - - - -	200.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.800NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-600.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.700NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-700.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.850NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-650.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.800NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-650.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.550NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-550.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.550NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-800.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.500NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.000NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.400NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.400NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.550NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.200NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.100NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-600.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	1.950NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-750.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.000NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-750.0PA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.100NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.100NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.500NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.300NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.650NA	-1.000UA	1.000UA
	IOL	- - - - - - -	-1.500NA	-1.000UA	1.000UA
	IOL	- - - - - - -	2.650NA	-1.000UA	1.000UA

TEST RUNTIME IS 19 SECONDS

PRINT / DISPLAY TIME IS 156 SECONDS

Figure V.A.11 - Initial Electrical Test (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :149 SERIAL NUMBER - 5
TESTED AT 25 DEG. C NO.13 ELECTRICALS
ON 27 SEP 83 AT 08:06 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
****	VOH1	- - - - - - -	-519.0MV	2.400 V	--
****	VOH1	- - - - - - -	-541.5MV	2.400 V	--
****	VOH1	- - - - - - -	-544.0MV	2.400 V	--
****	VOH1	- - - - - - -	-560.0MV	2.400 V	--
****	VOH1	- - - - - - -	-573.0MV	2.400 V	--
****	VOH1	- - - - - - -	-575.0MV	2.400 V	--
****	VOH1	- - - - - - -	-587.0MV	2.400 V	--
****	VOH1	- - - - - - -	-590.0MV	2.400 V	--
****	VOH1	- - - - - - -	-585.5MV	2.400 V	--
****	VOH1	- - - - - - -	-587.5MV	2.400 V	--
****	VOH1	- - - - - - -	-587.5MV	2.400 V	--
****	VOH1	- - - - - - -	-588.0MV	2.400 V	--
****	VOH1	- - - - - - -	-589.5MV	2.400 V	--
****	VOH1	- - - - - - -	-590.5MV	2.400 V	--
****	VOH1	- - - - - - -	-596.0MV	2.400 V	--
****	VOH1	- - - - - - -	-592.0MV	2.400 V	--
****	VOH1	- - - - - - -	-590.0MV	2.400 V	--
****	VOH1	- - - - - - -	-596.0MV	2.400 V	--
****	VOH1	- - - - - - -	-590.5MV	2.400 V	--
****	VOH1	- - - - - - -	-590.0MV	2.400 V	--
****	VOH1	- - - - - - -	-589.0MV	2.400 V	--
****	VOH1	- - - - - - -	-591.5MV	2.400 V	--
****	VOH1	- - - - - - -	-591.5MV	2.400 V	--
****	VOH1	- - - - - - -	-590.5MV	2.400 V	--
****	VOH1	- - - - - - -	-591.5MV	2.400 V	--
****	VOH1	- - - - - - -	-602.5MV	2.400 V	--
****	VOH1	- - - - - - -	-602.5MV	2.400 V	--
****	VOH1	- - - - - - -	-469.0MV	2.400 V	--
****	VOH1	- - - - - - -	-469.0MV	2.400 V	--
****	VOH1	- - - - - - -	-466.5MV	2.400 V	--
	VOH1	- - - - - - -	4.345 V	2.400 V	--
****	VOH2	- - - - - - -	-325.0MV	4.000 V	--
****	VOH2	- - - - - - -	-340.5MV	4.000 V	--
****	VOH2	- - - - - - -	-339.5MV	4.000 V	--
****	VOH2	- - - - - - -	-347.5MV	4.000 V	--
****	VOH2	- - - - - - -	-355.0MV	4.000 V	--
****	VOH2	- - - - - - -	-362.0MV	4.000 V	--
****	VOH2	- - - - - - -	-369.5MV	4.000 V	--
****	VOH2	- - - - - - -	-377.0MV	4.000 V	--
****	VOH2	- - - - - - -	-367.5MV	4.000 V	--
****	VOH2	- - - - - - -	-369.5MV	4.000 V	--
****	VOH2	- - - - - - -	-370.0MV	4.000 V	--
****	VOH2	- - - - - - -	-372.0MV	4.000 V	--
****	VOH2	- - - - - - -	-372.5MV	4.000 V	--
****	VOH2	- - - - - - -	-374.0MV	4.000 V	--
****	VOH2	- - - - - - -	-370.0MV	4.000 V	--
****	VOH2	- - - - - - -	-374.0MV	4.000 V	--
****	VOH2	- - - - - - -	-374.0MV	4.000 V	--

Figure V.A.12 - Post -1500 Volt Electrical Test

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO.13 ELECTRICALS

ON 27 SEP 83 AT 08:06 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
****	VOH2	- - - - - - -	-373.5MV	4.000 V	--
****	VOH2	- - - - - - -	-374.0MV	4.000 V	--
****	VOH2	- - - - - - -	-371.0MV	4.000 V	--
****	VOH2	- - - - - - -	-372.0MV	4.000 V	--
****	VOH2	- - - - - - -	-374.0MV	4.000 V	--
****	VOH2	- - - - - - -	-373.5MV	4.000 V	--
****	VOH2	- - - - - - -	-372.0MV	4.000 V	--
****	VOH2	- - - - - - -	-373.5MV	4.000 V	--
****	VOH2	- - - - - - -	-377.0MV	4.000 V	--
****	VOH2	- - - - - - -	-378.0MV	4.000 V	--
****	VOH2	- - - - - - -	-273.0MV	4.000 V	--
****	VOH2	- - - - - - -	-273.0MV	4.000 V	--
****	VOH2	- - - - - - -	-243.5MV	4.000 V	--
	VOH2	- - - - - - -	4.490 V	4.000 V	--
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.940 V	--	400.0MV
****	VOL1	- - - - - - -	4.760 V	--	400.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.935 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV

Figure V.A.12 - Post -1500 Volt Electrical Test (Cont.)

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO.13 ELECTRICALS
ON 27 SEP 83 AT 08:06 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.950 V	--	100.0MV
****	VOL2	- - - - - - -	4.940 V	--	100.0MV
****	VOL2	- - - - - - -	4.945 V	--	100.0MV
****	VOL2	- - - - - - -	4.490 V	--	100.0MV
	IIL	- - - - - - -	600.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	150.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.950NA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	450.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	200.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.400NA	-1.000UA	1.000UA
	IIL	- - - - - - -	-450.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	350.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	200.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.300NA	-1.000UA	1.000UA
	IIL	- - - - - - -	-600.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	400.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	300.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	1.300NA	-1.000UA	1.000UA
	IIL	- - - - - - -	-650.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	-500.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	250.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	500.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - - -	350.0PA	-1.000UA	1.000UA
	IIL	- - - - - - -	650.0PA	-1.000UA	1.000UA
****	IIL	- - - - - - -	2.100MA	-1.000UA	1.000UA

Figure V.A.12 - Post -1500 Volt Electrical Test (Cont.)

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO.13 ELECTRICALS
ON 27 SEP 83 AT 08:06 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
****	IIL	- - - - - -	2.100MA	-1.000UA	1.000UA
****	IIL	- - - - - -	7.670MA	-1.000UA	1.000UA
****	IIL	- - - - - -	7.670MA	-1.000UA	1.000UA
	IIL	- - - - - -	0.000 A	-1.000UA	1.000UA
	IIL	- - - - - -	800.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	250.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	-400.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	2.000NA	-1.000UA	1.000UA
	IIL	- - - - - -	-350.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.950NA	-1.000UA	1.000UA
	IIL	- - - - - -	-500.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.800NA	-1.000UA	1.000UA
	IIL	- - - - - -	-600.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	-650.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.700NA	-1.000UA	1.000UA
	IIL	- - - - - -	-750.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.700NA	-1.000UA	1.000UA
	IIL	- - - - - -	-800.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.500NA	-1.000UA	1.000UA
	IIL	- - - - - -	-800.0PA	-1.000UA	1.000UA
	IIL	- - - - - -	1.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.000NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.300NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.300NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.250NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.250NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.400NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.600NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.450NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.450NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.200NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.150NA	-1.000UA	1.000UA
	IIL	- - - - - -	-1.750NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.150NA	-1.000UA	1.000UA
	IIL	- - - - - -	-3.100NA	-1.000UA	1.000UA
	IIL	- - - - - -	1.150NA	-1.000UA	1.000UA
****	IIL	- - - - - -	-1.685MA	-1.000UA	1.000UA
****	IIL	- - - - - -	1.105MA	-1.000UA	1.000UA

Figure V.A.12 - Post -1500 Volt Electrical Test (Cont.)

FILE UID :149 SERIAL NUMBER - 5

TESTED AT 25 DEG. C NO.13 ELECTRICALS
ON 27 SEP 83 AT 08:06 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IOL	- - - - - -	550.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	2.550NA	-1.000UA	1.000UA
	IOL	- - - - - -	-200.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	2.250NA	-1.000UA	1.000UA
	IOL	- - - - - -	-300.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	2.150NA	-1.000UA	1.000UA
	IOL	- - - - - -	-400.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	2.000NA	-1.000UA	1.000UA
	IOL	- - - - - -	-550.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.900NA	-1.000UA	1.000UA
	IOL	- - - - - -	-700.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.750NA	-1.000UA	1.000UA
	IOL	- - - - - -	-800.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.600NA	-1.000UA	1.000UA
	IOL	- - - - - -	-1.000NA	-1.000UA	1.000UA
	IOL	- - - - - -	1.400NA	-1.000UA	1.000UA
	IOL	- - - - - -	-1.600NA	-1.000UA	1.000UA
	IOL	- - - - - -	2.100NA	-1.000UA	1.000UA
	IOL	- - - - - -	-1.300NA	-1.000UA	1.000UA
	IOL	- - - - - -	1.900NA	-1.000UA	1.000UA
	IOL	- - - - - -	-950.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.600NA	-1.000UA	1.000UA
	IOL	- - - - - -	-500.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.200NA	-1.000UA	1.000UA
	IOL	- - - - - -	-400.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.250NA	-1.000UA	1.000UA
	IOL	- - - - - -	-600.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.500NA	-1.000UA	1.000UA
	IOL	- - - - - -	-950.0PA	-1.000UA	1.000UA
	IOL	- - - - - -	1.950NA	-1.000UA	1.000UA
	IOL	- - - - - -	-1.350NA	-1.000UA	1.000UA
	IOL	- - - - - -	2.050NA	-1.000UA	1.000UA

Figure V.A.12 - Post -1500 Volt Electrical Test (Cont.)

Number of Failures at Pin Locations

3	7	8	9	10			Cumulative # Removed		Voltages
			14						+250
15		2	14						-250
15		3	15	2					+500
15	2	3	15	3					-500
15	3	5	15	5			5		+750
15	15	15	15	15			15		-750

Figure V.A.13 - CD Stress, Cumulative Leakage Current Failures

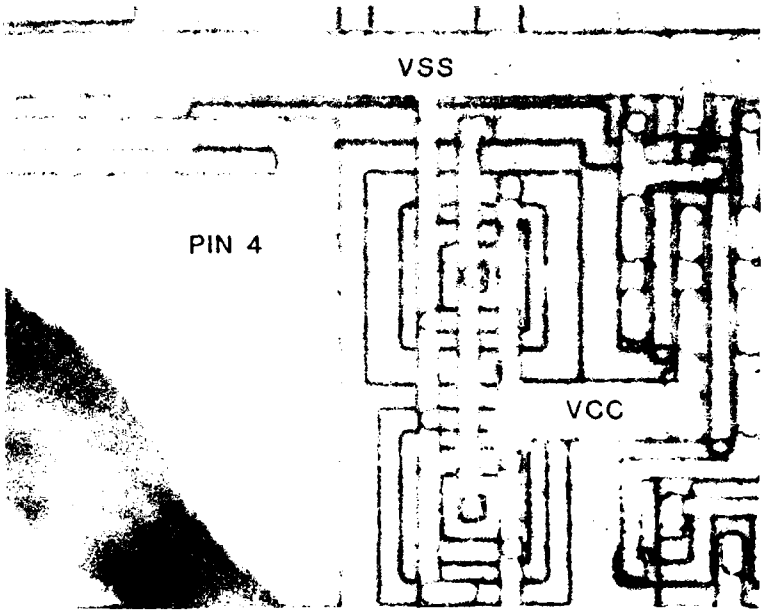


Figure V.A.14 - Pin 4 Input

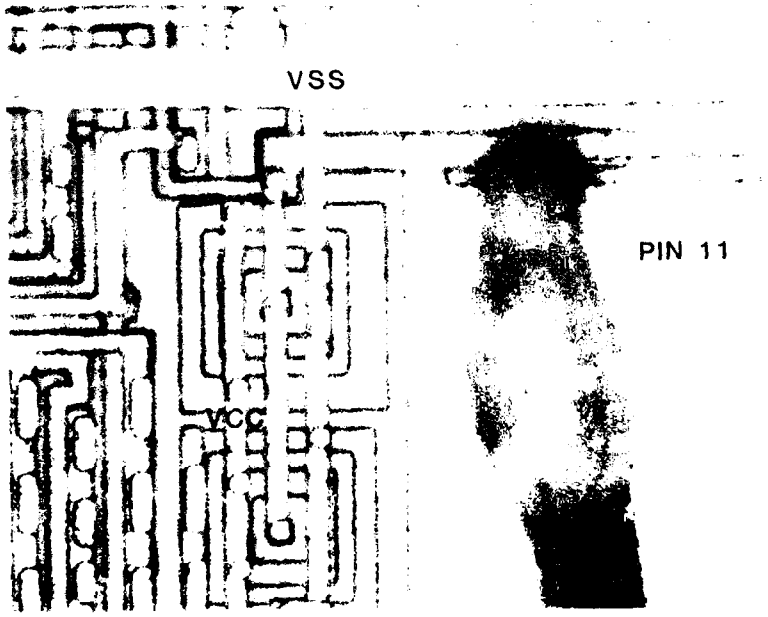


Figure V.A.15 - Pin 11 Input

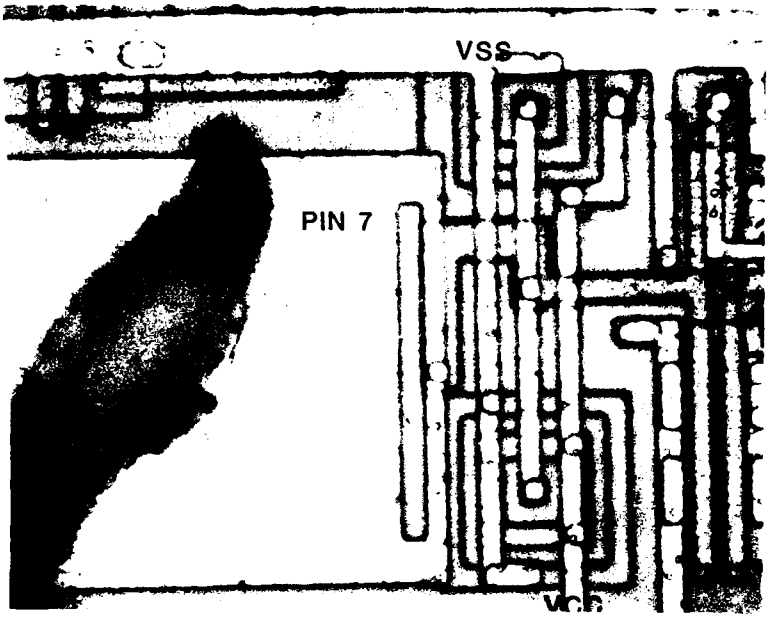


Figure V.A.16 - Pin 7 Input

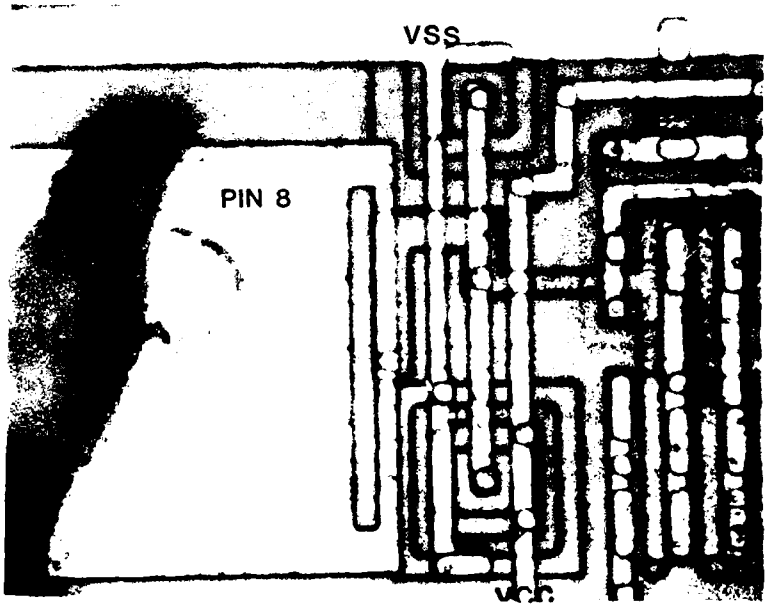


Figure V.A.17 - Pin 8 Input

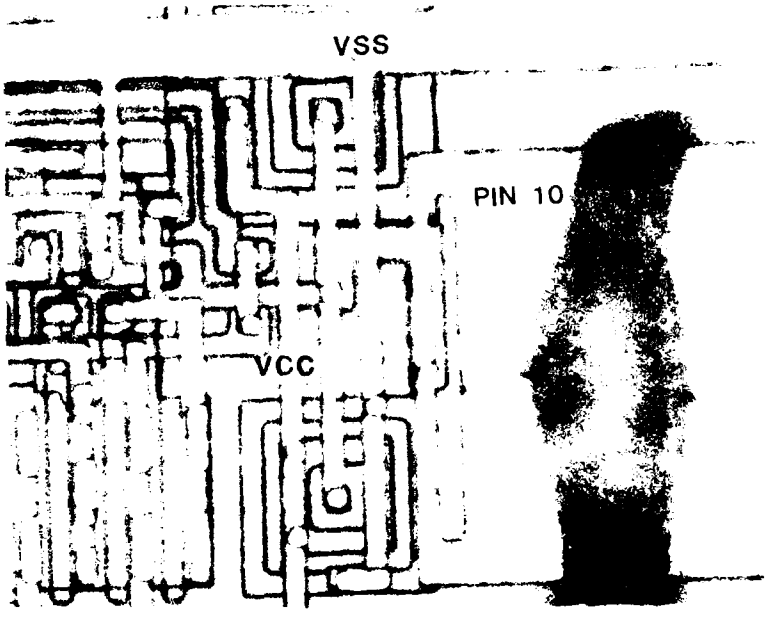


Figure V.A.18 - Pin 10 Input

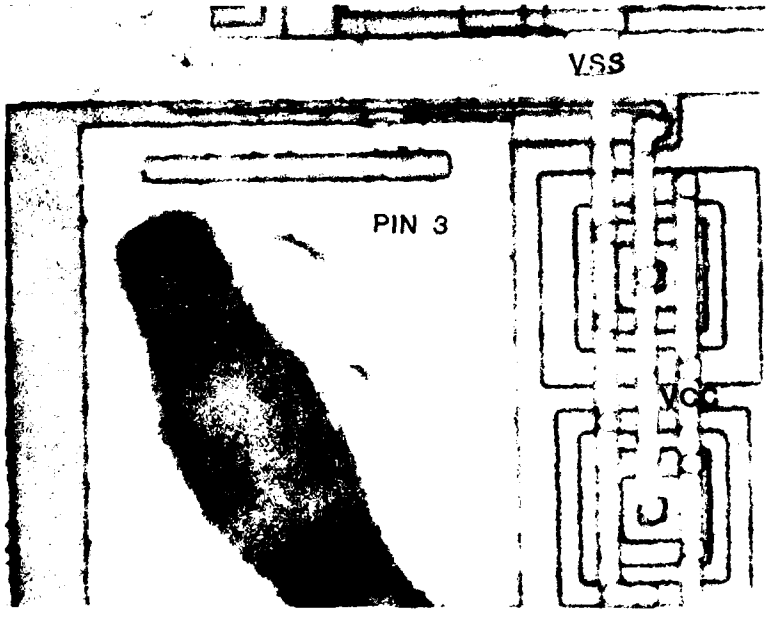


Figure V.A.19 - Pin 3 Input

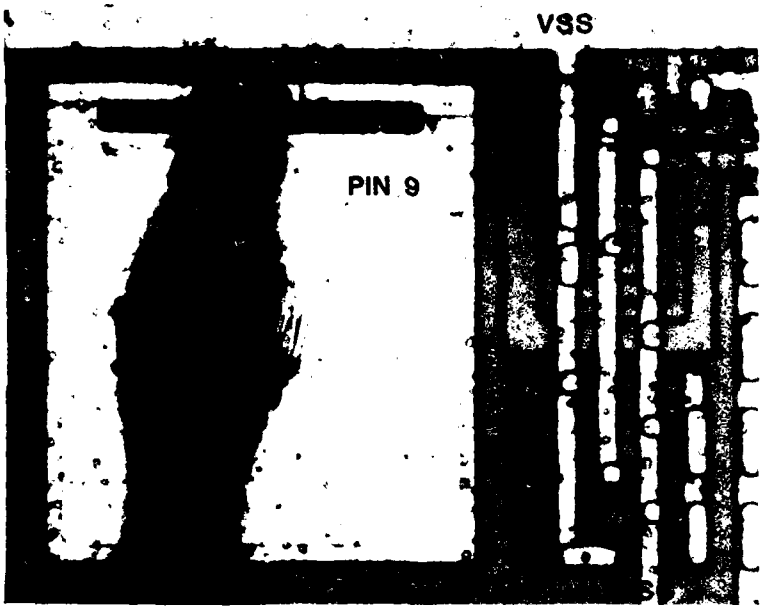


Figure V.A.20 - Pin 9 Input

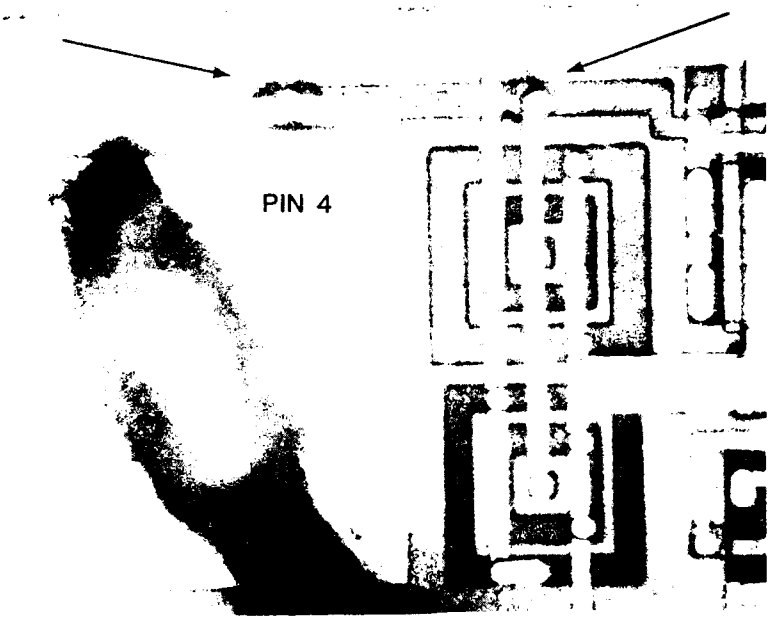


Figure V.A.21 - CD Stress, Pin 4 Input Polysilicon Damage

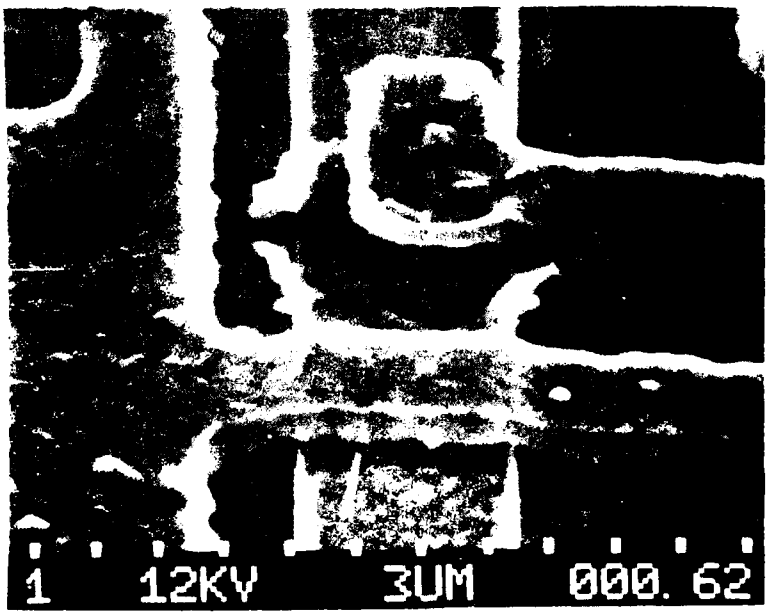


Figure V.A.22 - CD Stress, SEM Micrograph of Pin 4 Polysilicon at Diode Metalization Contact

Figure V.A.23 - CD Stress, Pin 11 Input Polysilicon Damage

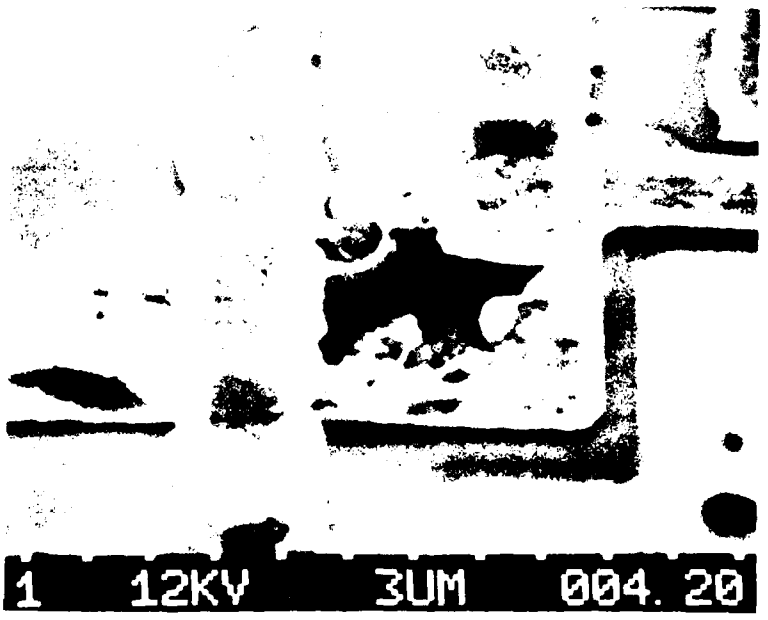


Figure V.A.24 - CD Stress, SEM Micrograph of Pin 11 Input Polysilicon.

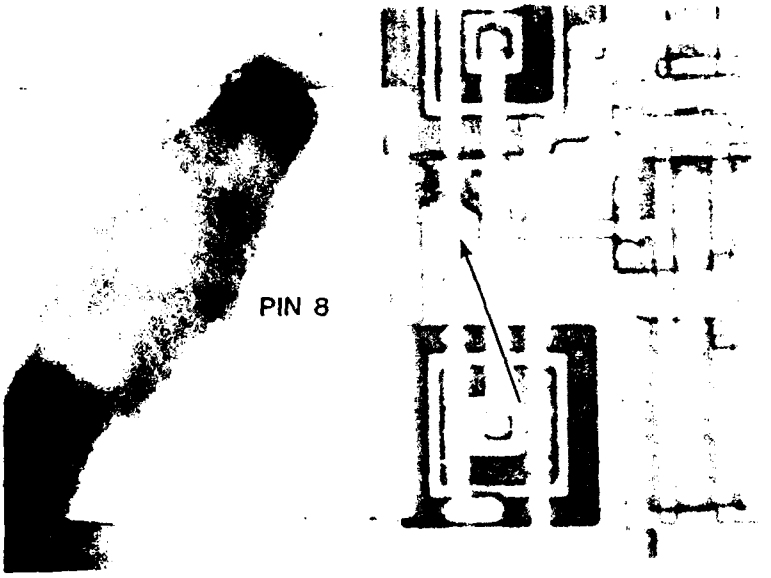


Figure V.A.25 - CD Stress, Pin 8 Input Polysilicon Damage

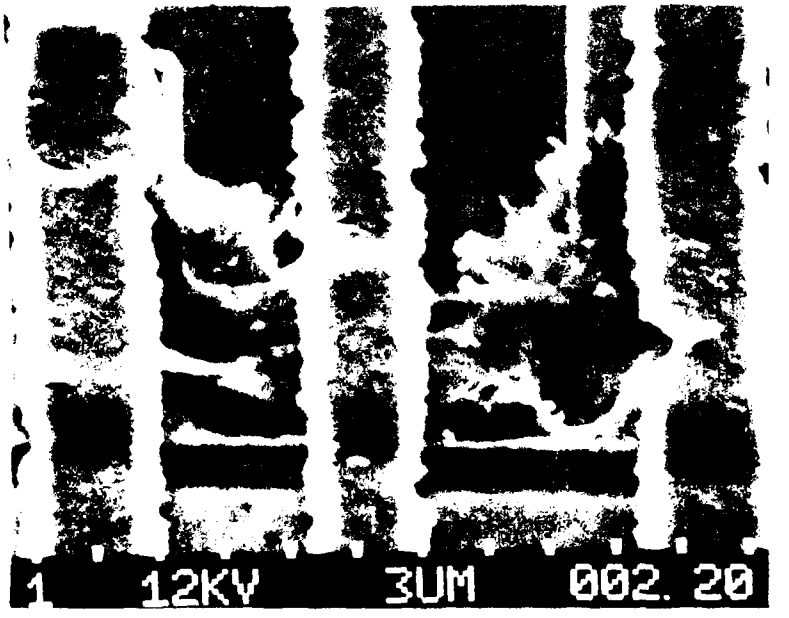


Figure V.A.26 - CD Stress, SEM Micrograph of Pin 8 Input Polysilicon Damage

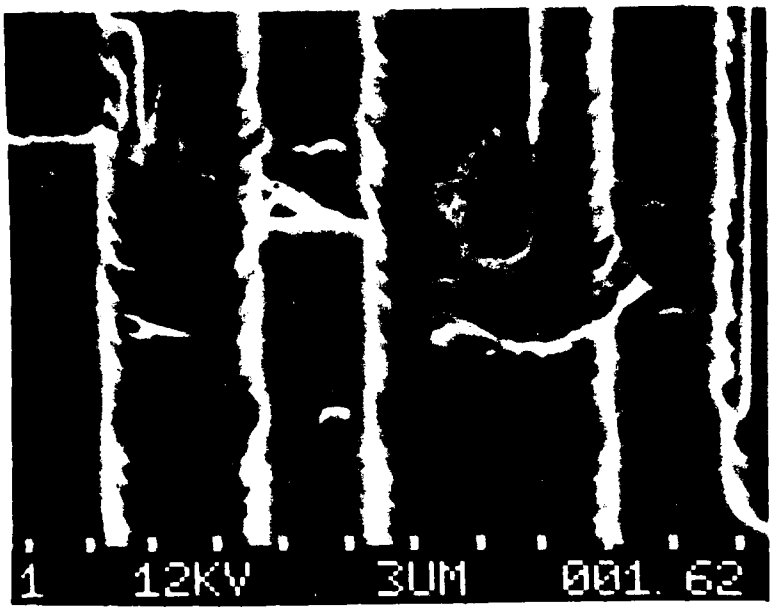


Figure V.A.27 - CD Stress, SEM Micrograph of Pin 7 Input Polysilicon Damage

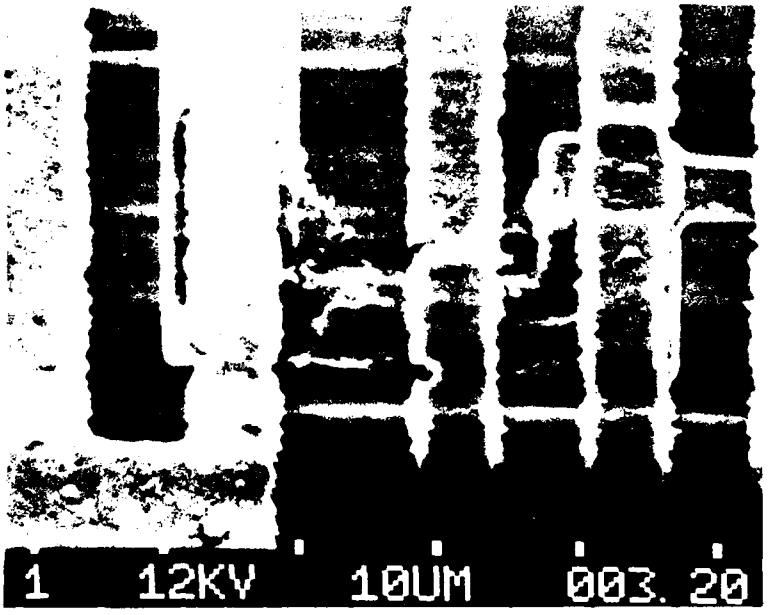


Figure V.A.28 - CD Stress, SEM Micrograph of Pin 9 Input Polysilicon Damage

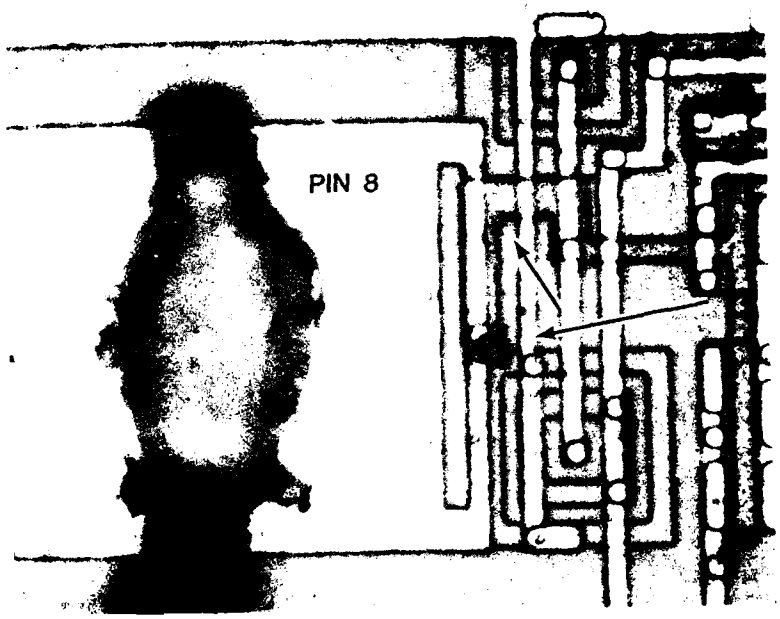


Figure V.A.29 - CD Stress, SEM Micrograph of Pin 8 Input Polysilicon Damage

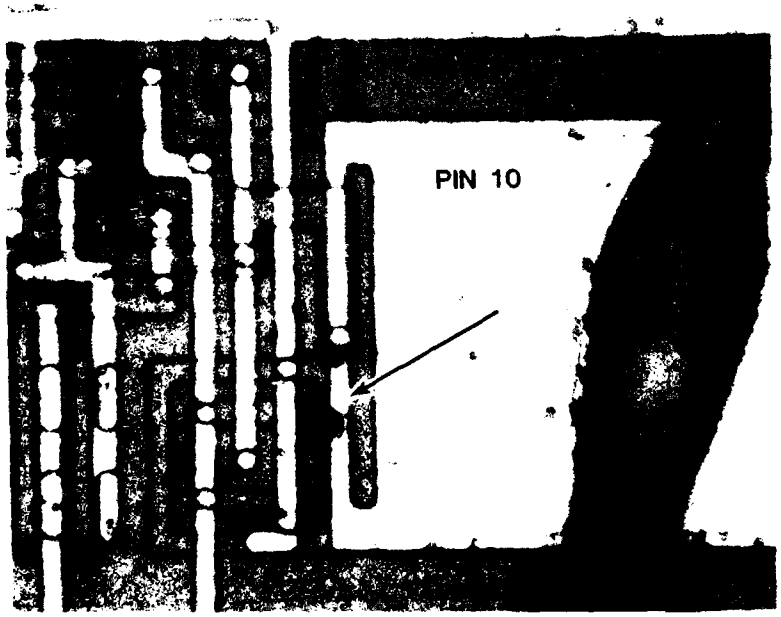


Figure V.A.30 - CD Stress, Pin 10 Breakdown Site from Metallization to Silicon

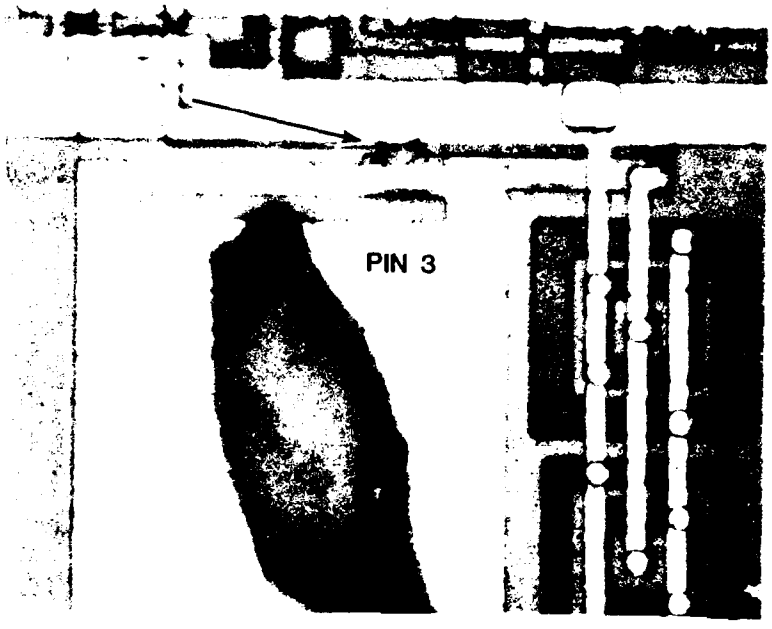


Figure V.A.31 - CD Stress, Pin 3 Input Polysilicon Damage

Figure V.A.32 - CD Stress, SFM Micrograph of Pin 3 Polysilicon Damage

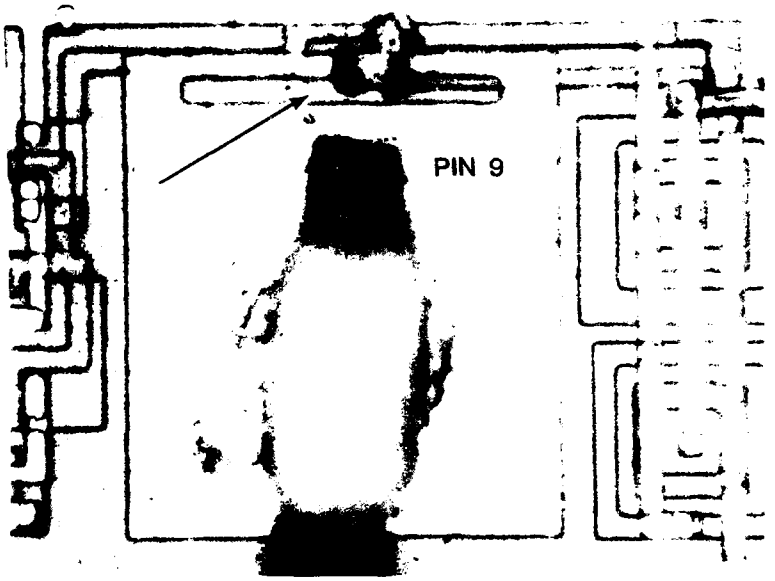


Figure V.A.33 - CD Stress, SEM Micrograph of Pin 9 Polysilicon Damage

Number of Failures at Pin Locations										
3	7	8	9	10	11	19	27	33	Cumulative # Removed	Voltage
										+250
			1			1				-250
			1			1				+500
			1			1				-500
			11			1				+750
			12			1	1	1	1	-750
			15	1		1	1	1	2	+1000
			15	1		1	1	1	2	-1000
2			15	1		1	1	1	2	+1250
10			15	1		1	1	1	4	-1250
15			15	1		1	1	1	5	+1500
15	1	2	15	3	1	1	1	1	15	-1500

Figure V.A.34 - HBD Stress, Cumulative Leakage Failure

Serial Number								LEGEND: O = open, X = short, S = slight damage, ✓ = damage, ND = no visible damage
2	6	8	9	11	12	15	16	
S	X	S	X	S	S	S	S	pin 3
S	O	S	S	S	ND	S	ND	pin 4
S	✓	O	O	S	S	S	✓	pin 7
S	O	O	O	S	S	S	O	pin 8
ND	ND	ND	ND	ND	O	ND	ND	pin 9
S	S	S	O	S	S	S	O	pin 10
ND	O	O	O	ND	S	O	✓	pin 11
-750	-1500	-1500	-1500	+1250	+1250	+1500	-1500	Final Voltage Stress

Figure V.A.35 - HBD Stress, Damage Summary

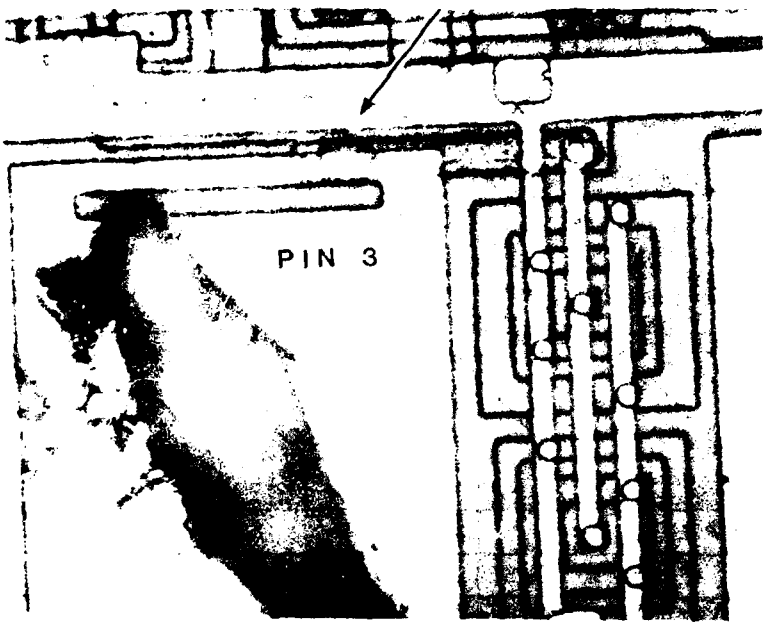


Figure V.A.36 - HBD Stress, Pin 3 Input Polysilicon Damage

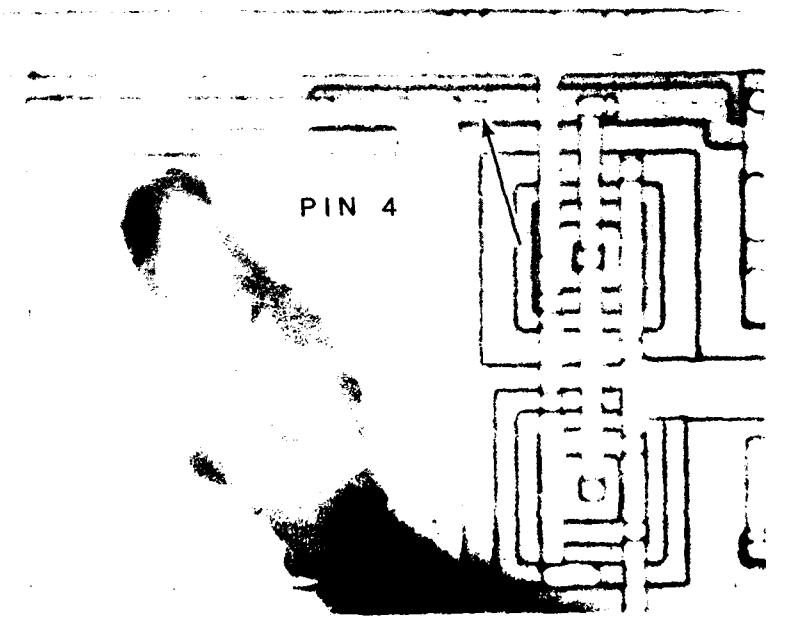


Figure V.A.37 - HBD Stress, Pin 4 Input with Minor Polysilicon Damage

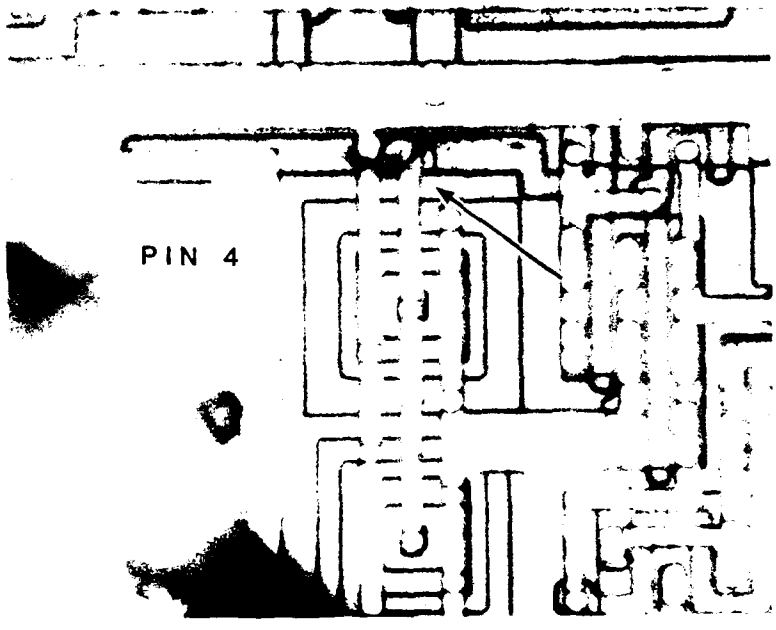


Figure V.A.38 - HBD Stress, Pin 4 Input Polysilicon Damage

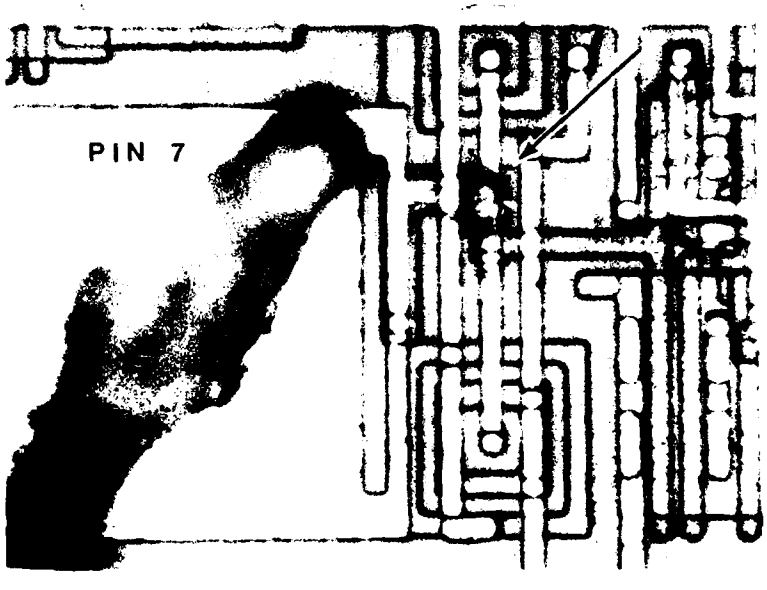


Figure V.A.39 - HBD Stress, Pin 7 Input Polysilicon Damage

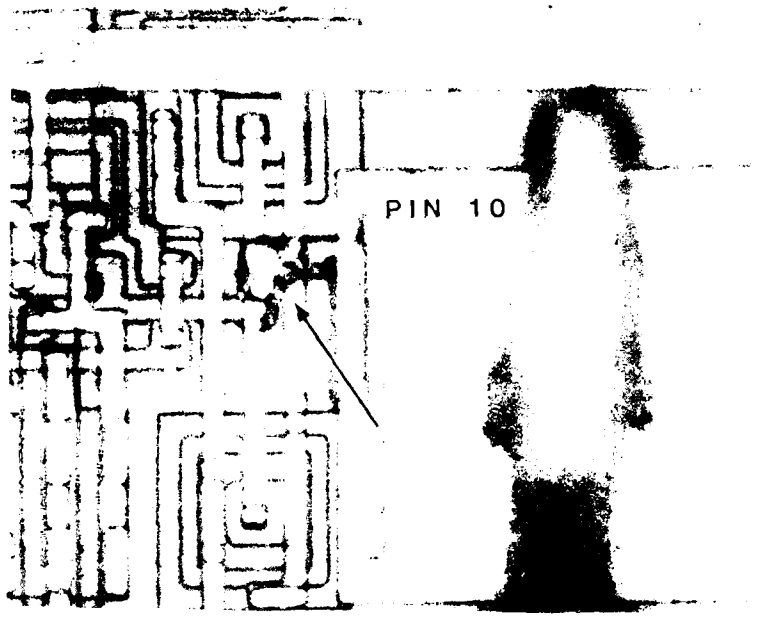


Figure V.A.40 - HBD Stress, Pin 10 Input Polysilicon Damage

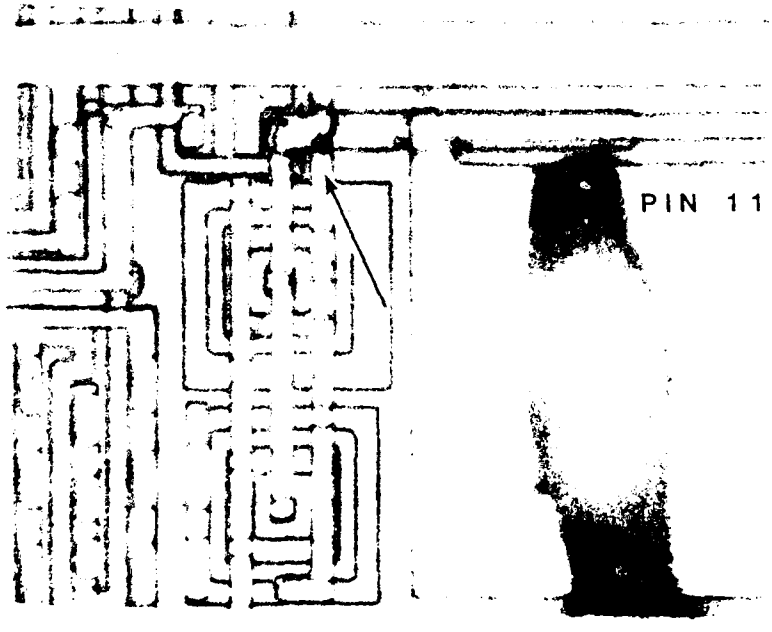


Figure V.A.41 - HBD Stress, Pin 11 Input Polysilicon Damage

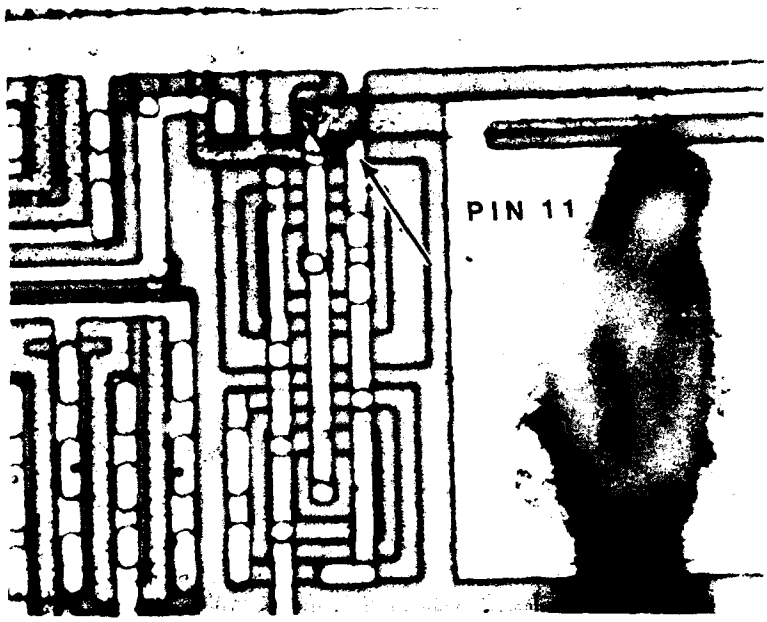


Figure V.A.42 - HBD Stress, Pin 11 Input Polysilicon Damage

B. Part B Analysis

This device is a 1K x 8-bit static RAM manufactured using an advanced NMOS process. The metallization and polysilicon linewidths are 3 microns. There is one polysilicon layer and one metallization layer. This was in a 24-pin dual-in-line ceramic package. An overall die photo is shown in Figure V.B.1. VCC is pin 24 at the top of Figure V.B.1 and VSS is pin 12 at the bottom. VCC and VSS are distributed via aluminum metallization across the die. The distribution pattern was noted for future reference to use during geometric sensitivity analysis. The VCC bond pad is shown in Figure V.B.2. The metallization connects to numerous n+ source diffusions. No points were found where it connected to polysilicon gates. The VSS metallization pad is shown in Figure V.B.3. The multi-contact metallization directly below the pad is part of the input protection network for pin 13. The ground metallization connects to numerous n+ source diffusions. This metallization does not connect to polysilicon. Between pins 1 and 2 is a bond pad (substrate bias generator) which has a wire connected from it to the substrate (Figure V.B.4). This connection does not come to the outside. The bond pad is connected to polysilicon which runs along the outside edge of the die and is also connected to the silicon die substrate. An input circuit is shown in Figure V.B.5. The bond pad metallization makes contact to an n+ diffusion and then continues on as a thick oxide gate between that n+ diffusion and an n+ diffusion which is connected to VSS or VCC. Pins 1-4 and 21-23 go to VSS and pins 5-8 and 18-20 go to VCC. The resistor travels about halfway around the pad and connects to an n+ source diffusion. Above a portion of this resistor is a polysilicon stripe which is connected back to the substrate. A schematic representation is shown in Figure V.B.6. The resistor measured 650 ohms. The gate dielectric failed at 45 VDC. The input resistor to substrate breakdown voltage was 22 VDC. This is the same as the transistor junction breakdown.

A second input protection circuit is shown in Figure V.B.7. This is connected to pin 8 and is located along the edge of the die away from the bond pad. The components are labeled.

One of the combination input-output pins is shown in Figure V.B.8. The input section is identical to the inputs discussed previously and the output schematic is shown in Figure V.B.9. Pin 13 has its input protect transistor going to VSS and pins 9-11 and 14-17 go to VCC.

Microsections were performed to examine the construction of the protect network. Figure V.B.10 shows an input with an area marked where a cross-section was performed. The cross-section is below the photograph. The polysilicon was approximately 0.6 microns thick, the metallization was 1.0 microns thick, and the diffusion depth was about 0.5 microns. The thick oxide areas beneath the polysilicon were approximately 1.0 microns thick. The gate oxide thickness was not discernible in this microsection. Two photographs of a microsection are shown in Figure V.B.11.

Electrical Testing

A sample of the electrical data taken on each of the stressed parts and the control part at each iteration during the testing is shown in Figures V.B.12 and V.B.13. Figure V.B.12 shows the initial readings on serial number 9 and Figure V.B.13 shows the readings after the -2000 volt stress. The data in/data out pins were measured for V_{OH}, V_{OL}, and I_{OL}. The I_{OL} reading was taken with the outputs in the high impedance configuration. This reading was influenced by the condition of the inputs during the latter stages of the stress due to the outputs not being fully disabled. The V_{OH} and V_{OL} measurements indicated that the outputs could be forced to a given state. Note that the limits were not correct on the initial readings. They should be as shown in Figure V.B.13. This testing also provided a functional check of the following. The control lines (OE, WE, and CE) and the I/O bus were completely tested. In the memory cell matrix only address 000 was written and read as 1's and 0's.

The I_{IL} reading provided leakage measurements on each of the address lines. This was measured with the input at 5 volts and did provide data which indicated the gradual damage being done to the input circuits. These data were supplemented by curve tracer data taken after the stresses at 500 volts, 1000 volts, 1500 volts, and 2000 volts. The voltage level at a current reading of 25 microamps was recorded for each of the pins. The pins were taken positive with respect to VSS.

Charged Device Data Analysis

The fifteen devices, S/N 17-31, proceeded through the -500 volt stress level with no device functional failures. No evidence of output leakage occurred, however, there was low level leakage evident on input pins as will be discussed. The maximum leakage was 21.8 nanoamps after the -500 volt stress. After the +750 volt stress there were eight devices with functional failures. These were S/N 17, 18, 20, 21, 22, 27, 28, and 30. The failure mode was an inability of the part to force the outputs to V_{OH} or V_{OL} at the proper times. There was no increase in output leakage currents. The maximum input leakage current was 1.2 microamps.

Following the -750 volt stress there were no new failures except for 1 device which failed 1 V_{OH} measurement.

Following the +1000 volt stress the remaining 7 devices failed functionally. Failures for V_{OH}, V_{OL}, and I_{OL} occurred. Leakage currents up to the maximum forced by the automatic test equipment (1.024 milliamps) occurred.

The data and the devices were analyzed to understand the failure modes and the sensitivity variations. The average of the input leakage currents were calculated for the stress levels up through +750 volts. These are shown in Figure V.B.14. The last column shows the maximum leakage current level measured at each voltage level. There is an increase in leakage current following each level of positive voltage stress and a slight decrease in leakage following the negative voltage stresses. The

Human Body Discharge Data Analysis

Device serial numbers 2 through 16 were stressed with the human body ESD simulation test method.

These parts went through -1250 volts of stress with no parametric or functional failures. Following the stress at +1500 volts there were 2 parts with input current leakage failures, this increased to 7 parts following the +1750 volt stress, and to 14 parts following the +2000 volt stress. As was seen for the charged device model, the negative stress did not have much of an effect on the leakage failures.

After the +2000 volt stress 6 devices had I_{OL} failures. The output transistors were not in the fully disabled state. There were still no functional failures. Serial number 7 was pulled for failure analysis. The -2000 volt stress did affect the parts. This indicates that the magnitude was more important than the polarity at this level. Functional failures occurred on 5 of the remaining 14 devices. All devices exhibited I_{IL} failures and 8 exhibited I_{OL} failures. The stress testing was stopped at this point.

A summary of the leakage current after 0 volts, +500 volts, +1000 volts, and +1500 volts is given in Figure V.B.26. The two inputs with the long metallization runs had a decreased sensitivity to stress. This was likely due to a reduction in the voltage level reaching the input resistor due to the parasitic capacitance and inductance of the metallization.

Pin 5 was the most sensitive to HBD stress. It was also the most sensitive to CD stress. The failures on it caused silicon damage in the necked down portion of the protect resistors. This is apparently a less tolerant system to stress than the other resistor layouts. The reason for the increased sensitivity of pin 4 is not evident, and it may not be significant since it has a very low leakage level at +1000 volts and was higher only after the + 1500 volt stress.

The increase in leakage current is shown in a different manner in Figure V.B.27. This shows the maximum leakage current at each voltage level and the serial number and pin association. This shows the leakage level increase after each positive stress and the high level of the leakage at the end of the stressing.

Failure analysis was performed on serial numbers 4, 7, 9 and 11. It was found that the location of the breakdown site could be determined by applying power to the part with liquid crystal (MBBA) on the device. The polysilicon on the resistor would appear to show movement within the liquid crystal when viewed under crossed polarizers depending upon the location of the failure. About half of the leaky pins were shorted to the polysilicon. Visually all of the first contact points between metallization and the input resistor showed some damage. The polysilicon shorts were not visible. The enable transistor gate oxides were not checked on these devices. The analysis only identified shorts that went to VCC, VSS, or Substrate.

The appearance seen is shown on serial number 4 in Figures V.B.28 - V.B.31. Figure V.B.28 shows pin 5 which was the most sensitive to leakage increase. Figure V.B.29 shows pin 22 which is layout style number 1. Figure V.B.30 shows pin 21 which is layout style number 2. Figure V.B.31 shows pin 20 and the adjacent input protect resistor which is not connected to any pin. The damage on pin 20 can be compared with the undamaged resistor.

Output pins did not exhibit any visible damage and electrical measurement found no increase in leakage current. The parametric failures on the output pins were due to the output transistors not being fully disabled because of other circuit problems.

The human body discharge stress found results similar to the charged device model stress. Inputs were susceptible to the stress and outputs were not. Pin 5 was the most sensitive to increases in low level leakage current with stress. The level at which parts exhibited functional failure was relatively high, -2000 volts. The major difference in sensitivity was the fact that the long metallization stripes prior to the protect circuits decreased sensitivity to the human body discharge stress and had no apparent effect upon the charged device stress.

This analysis indicates that one of the principle failure modes was shorting to the substrate polysilicon stripe. Removal of this polysilicon or an increase in the oxide thickness would likely produce a more tolerant system. The second failure mode, current leakage to an adjacent n+ diffusion, could be made less likely by increasing the spacing between the two n+ diffusions or by keeping corners farther apart.

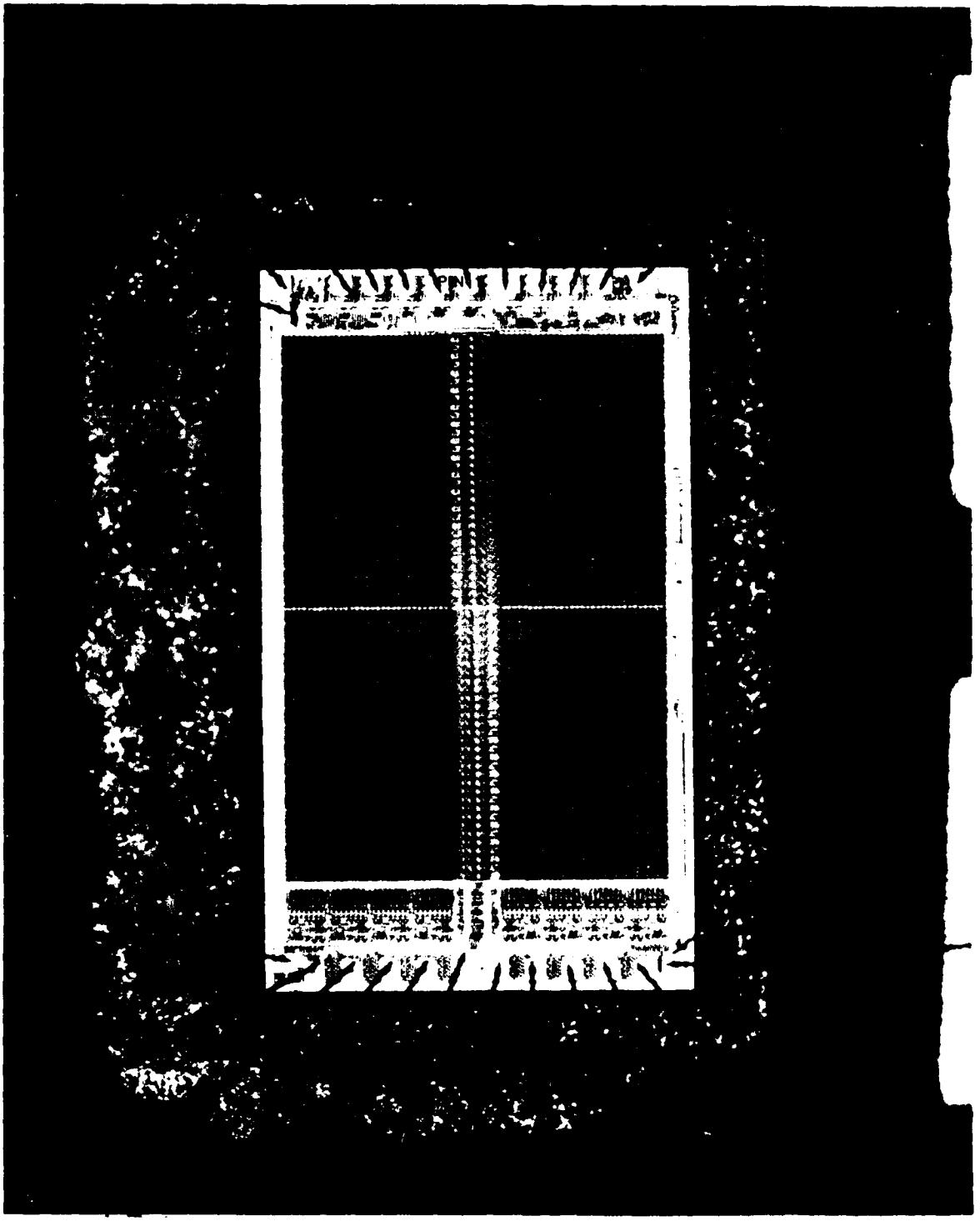


Figure V.B.1 - Overall Die Photograph

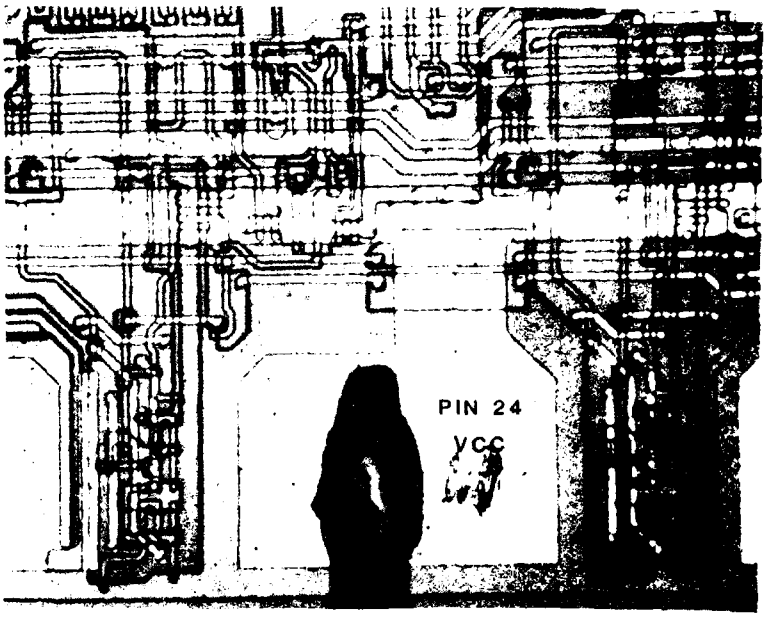


Figure V.B.2 - VCC Bond Pad and Connections

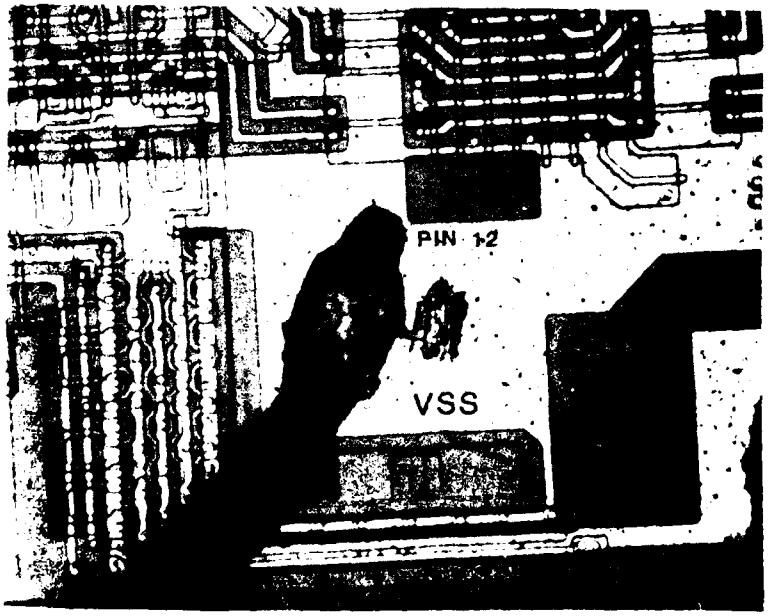


Figure V.B.3 - VSS Bond Pad and Connections

Figure V.B.4 - Substrate Bias Generator Pad

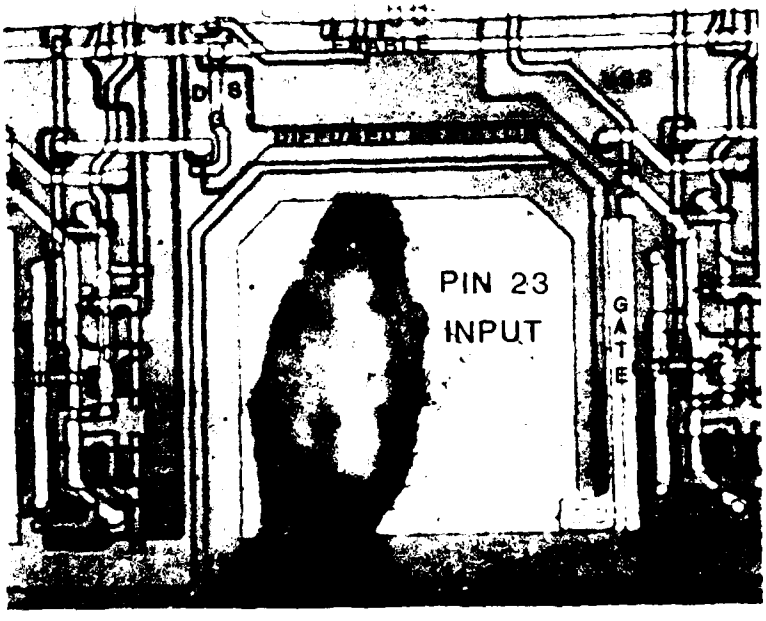


Figure V.B.5 - Pin 23 Input

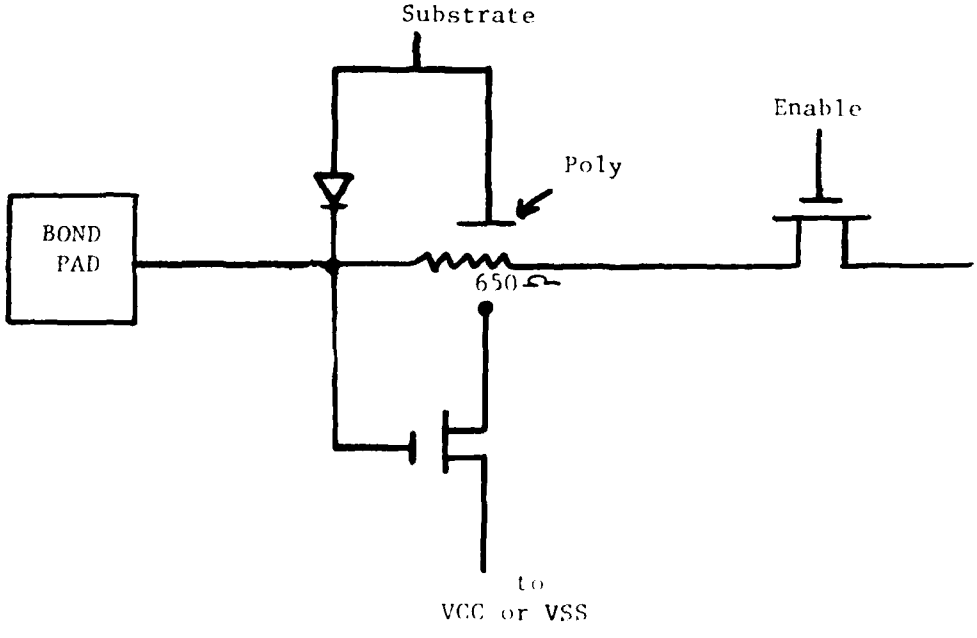


Figure V.B.6 - Input Schematic

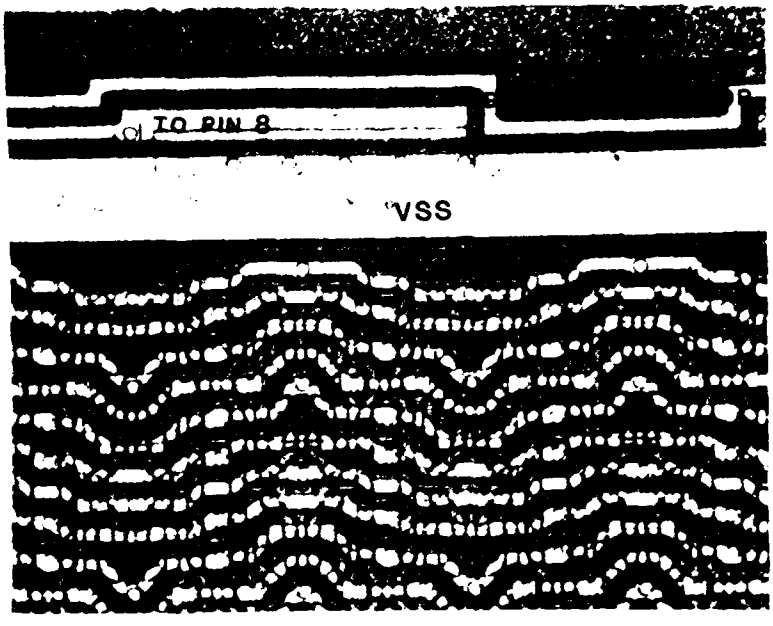


Figure V.B.7 - Pin 8 Input

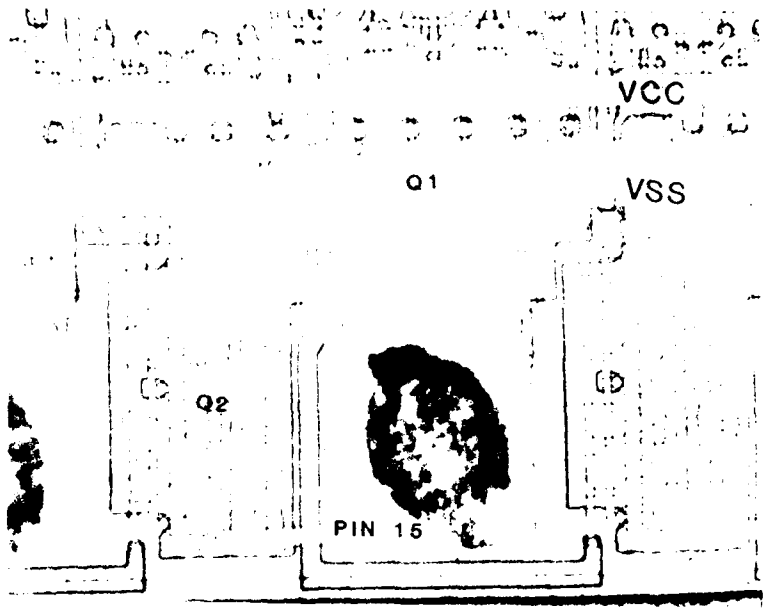


Figure V.B.8 - Pin 15 with Output Components Labeled.

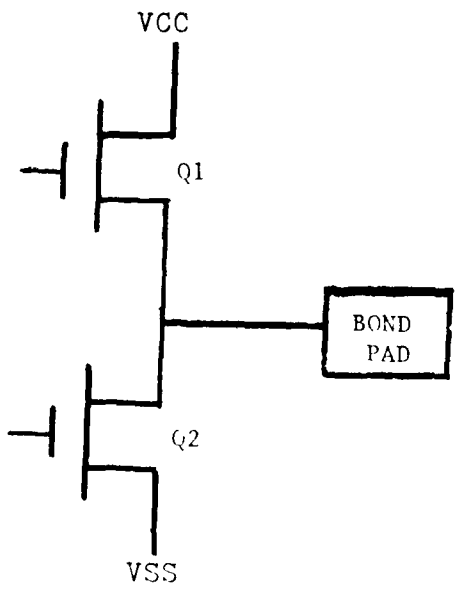
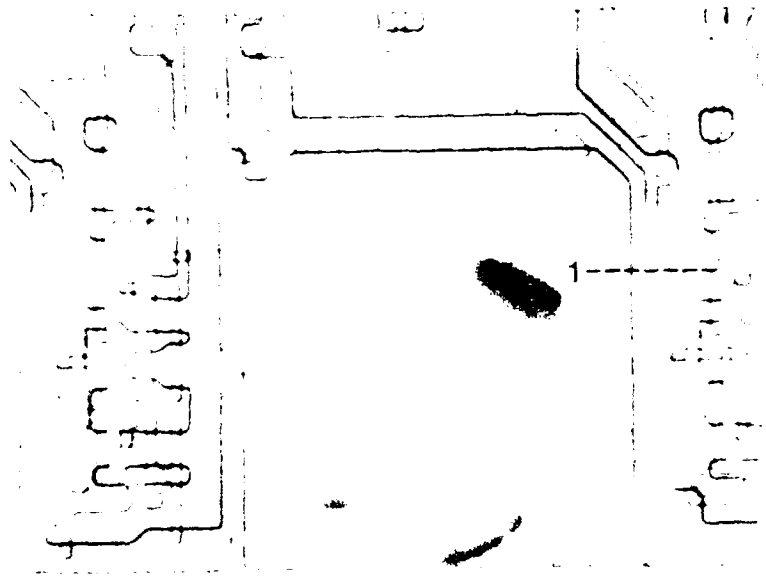


Figure V.B.9 - Output Schematic



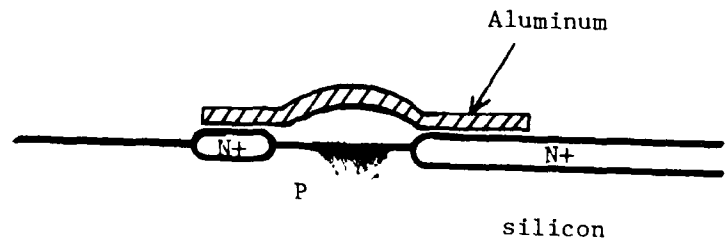


Figure V.B.10 - Input Pin with Location of Cross-Section and Drawing of Appearance of Cross-Section

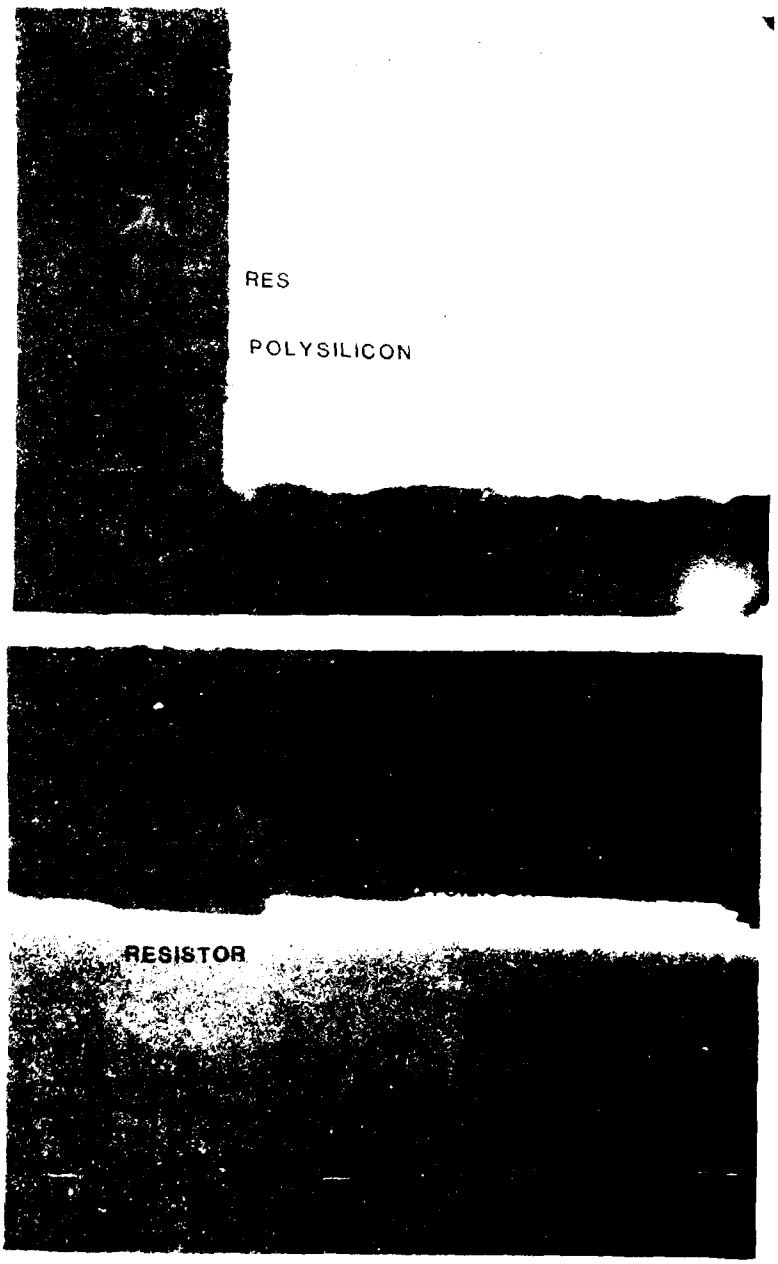


Figure V.E.11 - Input Resistor and Polysilicon Top and Side Views

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :150 SERIAL NUMBER - 9
TESTED AT 25 DEG. C INITIAL ELECTRICAL TEST
ON 13 JUN 83 AT 12:17:17 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	VOH	- - - - - - -	3.900 V	2.400 V	--
	VOH	- - - - - - -	3.910 V	2.400 V	--
	VOH	- - - - - - -	3.905 V	2.400 V	--
	VOH	- - - - - - -	3.900 V	2.400 V	--
	VOH	- - - - - - -	3.895 V	2.400 V	--
	VOH	- - - - - - -	3.900 V	2.400 V	--
	VOH	- - - - - - -	3.895 V	2.400 V	--
	VOH	- - - - - - -	3.890 V	2.400 V	--
	VOL	- - - - - - -	73.50MV	--	400.0MV
	VOL	- - - - - - -	71.50MV	--	400.0MV
	VOL	- - - - - - -	71.00MV	--	400.0MV
	VOL	- - - - - - -	72.50MV	--	400.0MV
	VOL	- - - - - - -	71.50MV	--	400.0MV
	VOL	- - - - - - -	72.00MV	--	400.0MV
	VOL	- - - - - - -	72.50MV	--	400.0MV
	VOL	- - - - - - -	75.00MV	--	400.0MV
	ICC1	- - - - - - -	48.00MA	--	125.0MA
	IIL	- - - - - - -	1.200NA	-200.0UA	--
	IIL	- - - - - - -	850.0PA	-200.0UA	--
	IIL	- - - - - - -	1.000NA	-200.0UA	--
	IIL	- - - - - - -	550.0PA	-200.0UA	--
	IIL	- - - - - - -	500.0PA	-200.0UA	--
	IIL	- - - - - - -	550.0PA	-200.0UA	--
	IIL	- - - - - - -	400.0PA	-200.0UA	--
	IIL	- - - - - - -	450.0PA	-200.0UA	--
	IIL	- - - - - - -	500.0PA	-200.0UA	--
	IIL	- - - - - - -	500.0PA	-200.0UA	--
	IOL	- - - - - - -	1.000NA	-10.00UA	10.00UA
	IOL	- - - - - - -	850.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	500.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	600.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	650.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	600.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	500.0PA	-10.00UA	10.00UA
	IOL	- - - - - - -	650.0PA	-10.00UA	10.00UA

TEST RUNTIME IS 8 SECONDS
PRINT / DISPLAY TIME IS 26 SECONDS

Figure V.B.12 - Initial Electrical Readings

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :150 SERIAL NUMBER - 9
TESTED AT 25 DEG. C RE-RUN WITH CHANGED LIMITS 18OCT83
ON 18 OCT 83 AT 09:44:36 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	VOH	- - - - - - -	3.865 V	2.400 V	--
	VOH	- - - - - - -	3.345 V	2.400 V	--
	VOH	- - - - - - -	3.865 V	2.400 V	--
	VOH	- - - - - - -	3.865 V	2.400 V	--
	VOH	- - - - - - -	3.905 V	2.400 V	--
	VOH	- - - - - - -	3.900 V	2.400 V	--
	VOH	- - - - - - -	3.900 V	2.400 V	--
	VOH	- - - - - - -	3.905 V	2.400 V	--
	VOL	- - - - - - -	74.00MV	--	400.0MV
	VOL	- - - - - - -	207.0MV	--	400.0MV
	VOL	- - - - - - -	71.00MV	--	400.0MV
	VOL	- - - - - - -	84.50MV	--	400.0MV
	VOL	- - - - - - -	71.50MV	--	400.0MV
	VOL	- - - - - - -	72.50MV	--	400.0MV
	VOL	- - - - - - -	73.00MV	--	400.0MV
	VOL	- - - - - - -	74.50MV	--	400.0MV
	ICC1	- - - - - - -	54.50MA	--	120.0MA
	IIL	- - - - - - -	10.60NA	-10.00UA	10.00UA
	IIL	- - - - - - -	10.05NA	-10.00UA	10.00UA
	IIL	- - - - - - -	17.45NA	-10.00UA	10.00UA
****	IIL	- - - - - - -	22.50UA	-10.00UA	10.00UA
	IIL	- - - - - - -	7.350NA	-10.00UA	10.00UA
	IIL	- - - - - - -	4.000NA	-10.00UA	10.00UA
	IIL	- - - - - - -	4.530UA	-10.00UA	10.00UA
	IIL	- - - - - - -	1.865UA	-10.00UA	10.00UA
	IIL	- - - - - - -	200.5NA	-10.00UA	10.00UA
	IIL	- - - - - - -	36.85NA	-10.00UA	10.00UA
	IOL	- - - - - - -	5.730UA	-50.00UA	50.00UA
****	IOL	- - - - - - -	1.024MA	-50.00UA	50.00UA
	IOL	- - - - - - -	5.460UA	-50.00UA	50.00UA
	IOL	- - - - - - -	5.080UA	-50.00UA	50.00UA
	IOL	- - - - - - -	3.910UA	-50.00UA	50.00UA
	IOL	- - - - - - -	4.770UA	-50.00UA	50.00UA
	IOL	- - - - - - -	5.100UA	-50.00UA	50.00UA
	IOL	- - - - - - -	5.115UA	-50.00UA	50.00UA

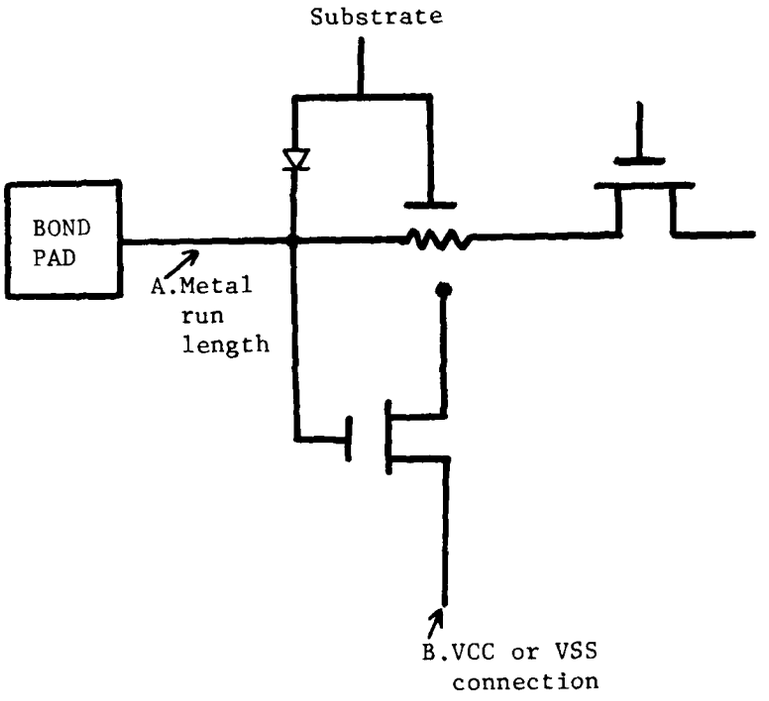
TEST RUNTIME IS 8 SECONDS
PRINT / DISPLAY TIME IS 26 SECONDS

Figure V.B.13 - Post -2000 Volt Electrical Readings

Leakage Current by Pin Number (nA)

1	2	3	4	5	6	7	8	22	23	Max Level	Voltage
0.7	0.8	1.2	0.8	0.9	0.9	1.6	1.1	0.7	1.1	1.9	0
0.6	0.6	1.0	0.8	0.8	0.9	1.5	0.9	0.5	1.1	4.2	+250
0.6	1.1	1.0	1.3	1.2	0.8	1.6	1.1	0.5	1.3	5.9	-250
1.0	1.6	1.2	3.3	9.4	1.1	2.5	1.7	0.6	2.0	27.8	+500
1.1	1.5	1.1	2.7	7.7	1.0	2.3	1.4	0.7	1.9	21.8	-500
3.0	4.0	2.6	4.0	10.8	1.6	7.3	3.7	1.5	3.5	25.1	+750
3	2	3	2	1	3	2	2	3	2		Sensitivity Classif.
short	short	short	short	short	short	long	long	short	short		A. Metal Run Length
V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}		B. V_{CC} or V_{SS} Connect
1	2	1	2	3	1	4	4	1	2		C. Layout Style

Figure V.B.14 - CD Stress, Leakage Current Summary (S/N 17-31)



Layout Style

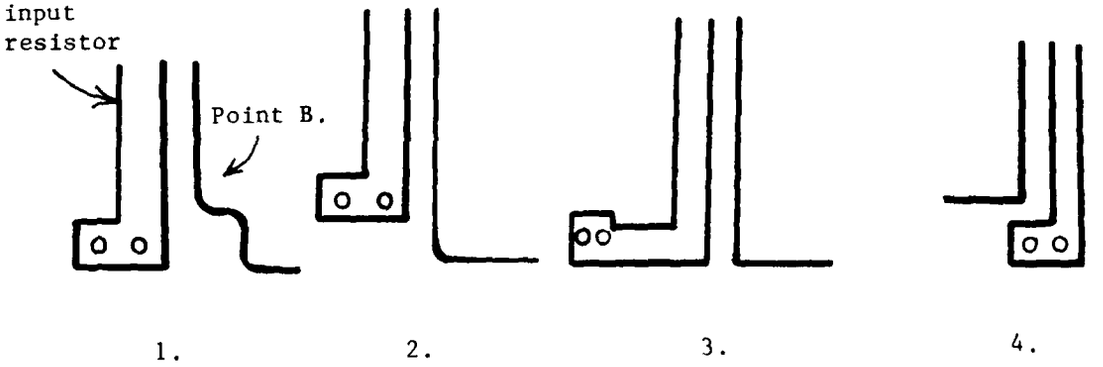


Figure V.B.14A - Layout Variations and Input Schematic

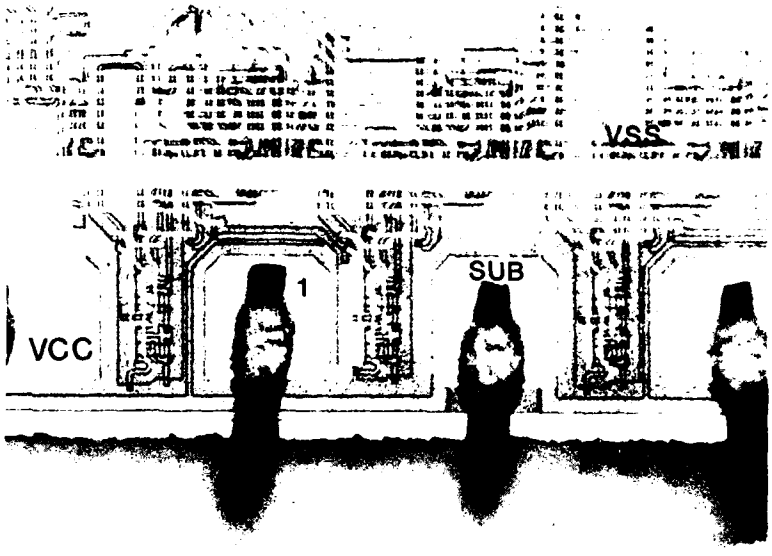


Figure V.B.15 - Pin 1 Input

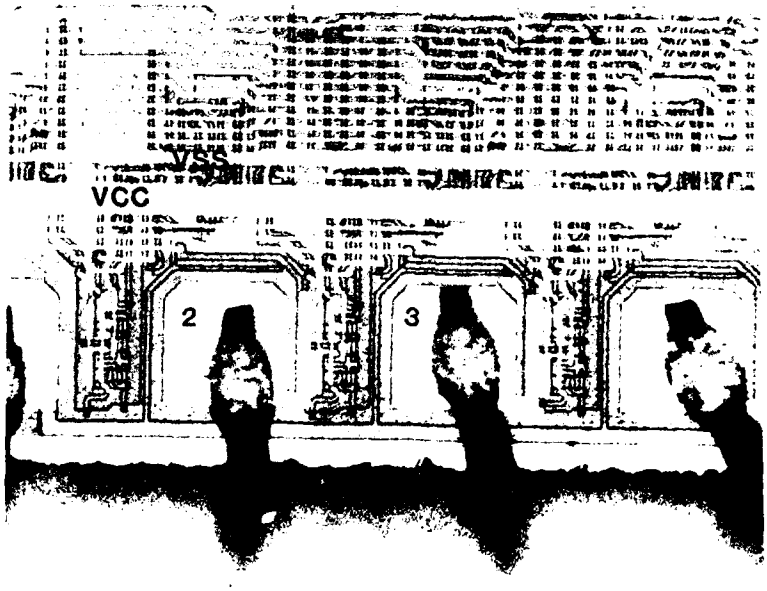


Figure V.B.16 - Input Pins 2 and 3

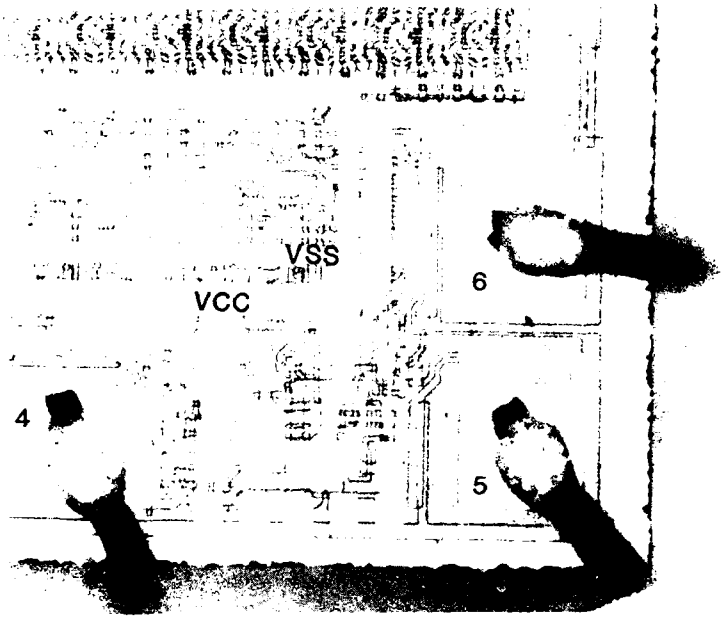


Figure V.B.17 - Input Pins 4, 5 and 6

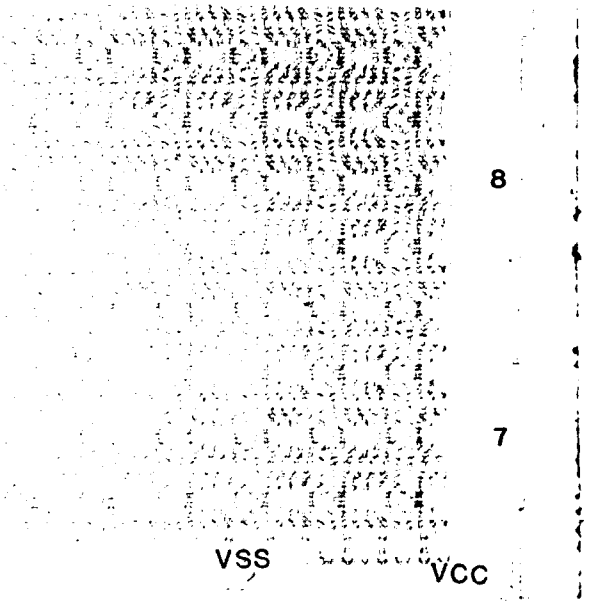


Figure V.B.18 - Input Resistors for Pins 7 and 8

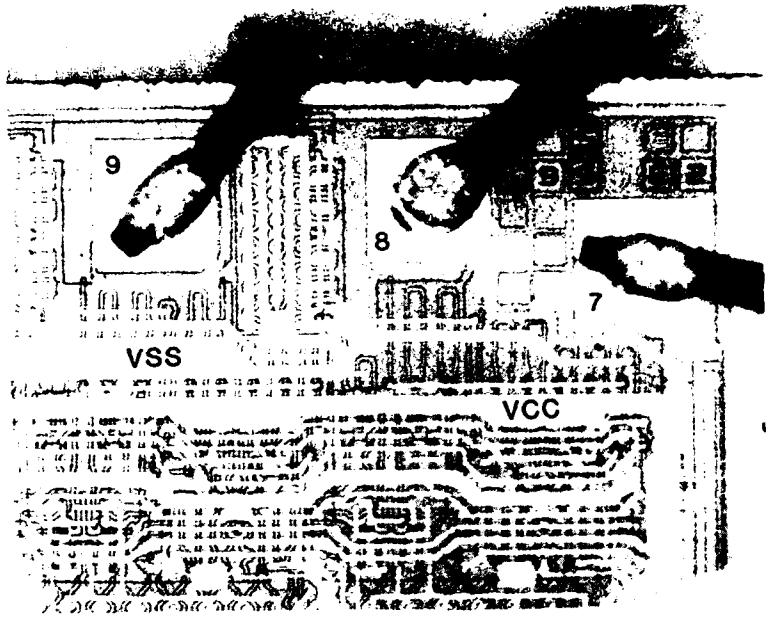


Figure V.B.19 - Input Pins 7, 8 and 9

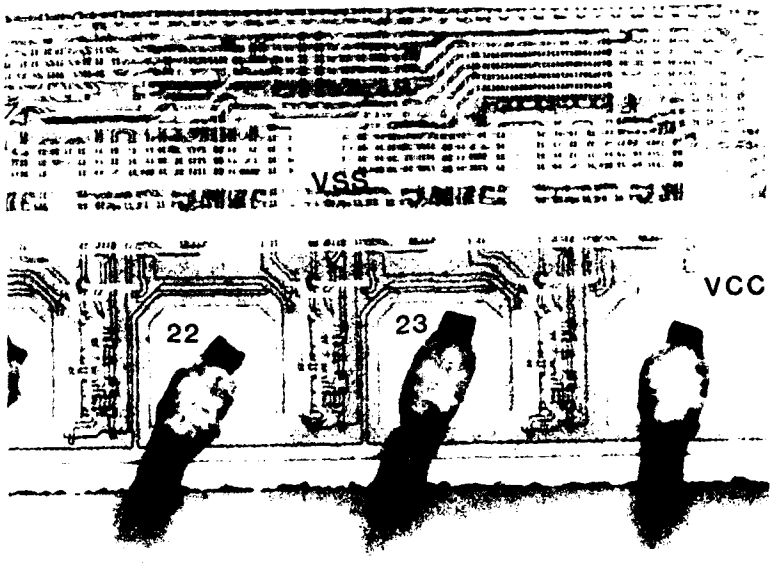


Figure V.B.20 - Input Pins 22 and 23

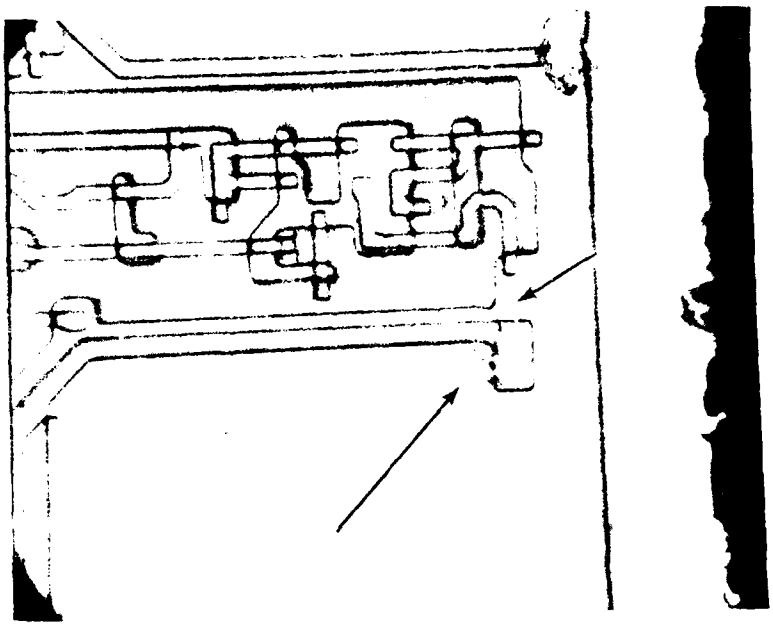


Figure V.B.21 - CD Stress, Pin 22 Input Damage

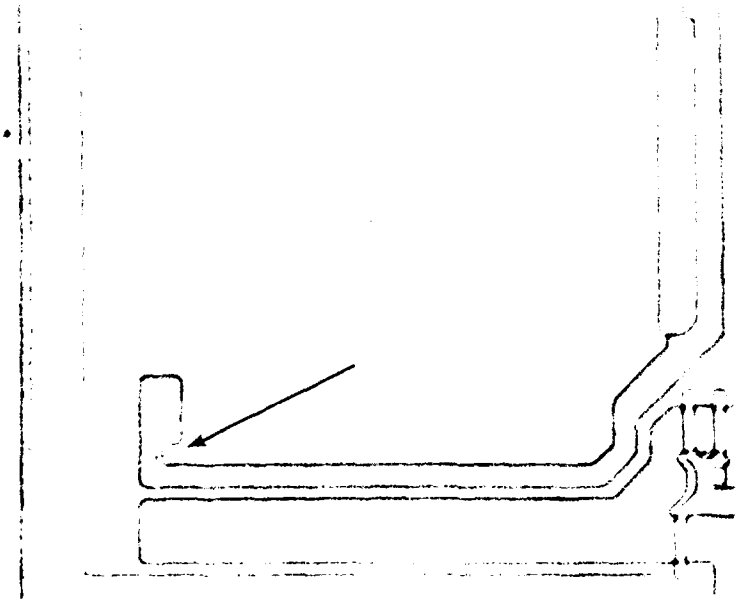


Figure V.B.22 - CD Stress, Pin 5 Input Damage

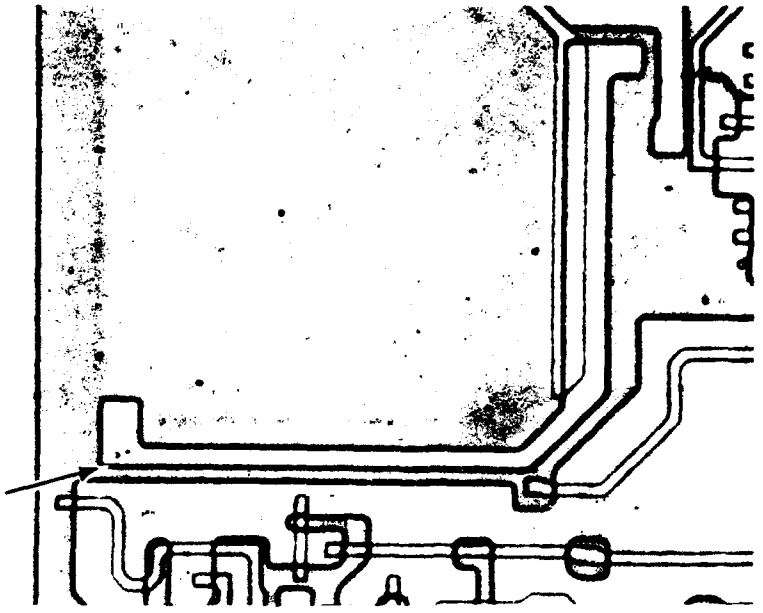


Figure V.B.23 - CD Stress, Pin 4 Input Damage

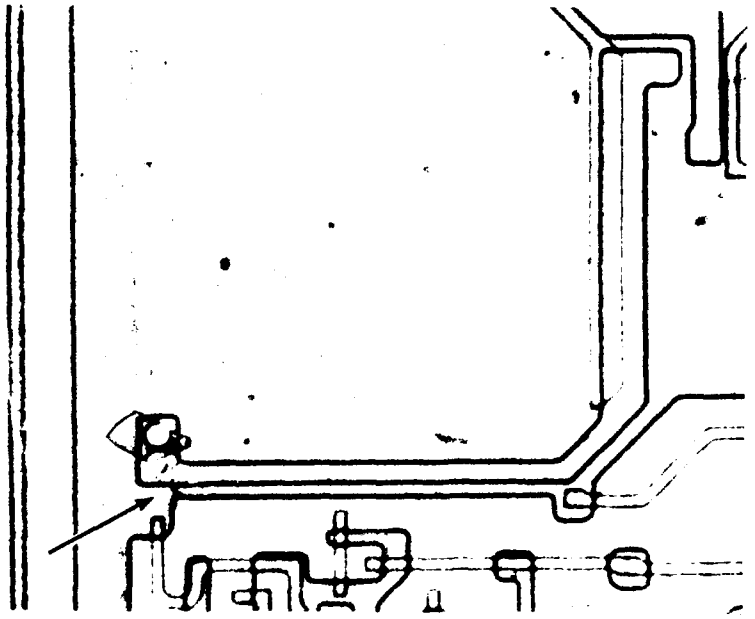


Figure V.B.24 - CD Stress, Pin 3 Input Damage

Figure V.B.25 - CD Stress, Pin 13 Input/Output Circuit with No Visible Damage

Leakage Current by Pin Number (nA)

1	2	3	4	5	6	7	8	22	23		Voltage
0.8	0.8	1.1	0.9	0.9	0.9	1.5	0.9	0.8	1.0		0
2.0	1.0	1.8	1.1	0.9	1.4	2.3	1.4	1.5	3.1		+500
35.2	13.0	17.5	10.8	50.9	37.1	11.5	9.2	41.0	22.0		+1000
36.3	33.1	25.3	108.6	132.7	46.5	15.1	19.4	28.3	29.0		+1500
2	2	2	1	1	2	3	3	2	2		Sensitivity Classif.
short	short	short	short	short	short	long	long	short	short		A. Metal Run Length
V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{SS}		B. V_{CC} or V_{SS} Connect
1	2	1	2	3	1	4	4	1	2		C. Layout Style

Figure V.B.26 - HBD Stress, Leakage Current Summary

Current Level	Serial Number	Pin Number	Voltage
1.9nA	5	7	0
3.5nA	15	23	+250
6.4nA	15	23	-250
8.2nA	15	23	+500
6.1nA	15	23	-500
73nA	5	1	+750
70nA	5	1	-750
270nA	15	5	+1000
277nA	15	5	-1000
340nA	11	3	+1250
369nA	11	3	-1250
15uA	7	22	+1500
15uA	7	22	-1500
21uA	11	23	+1750
20uA	11	23	-1750
692uA	11	2	+2000
756uA	11	2	-2000

Figure V.B.27 - HRD Stress, Maximum Leakage Current at each Stress Level

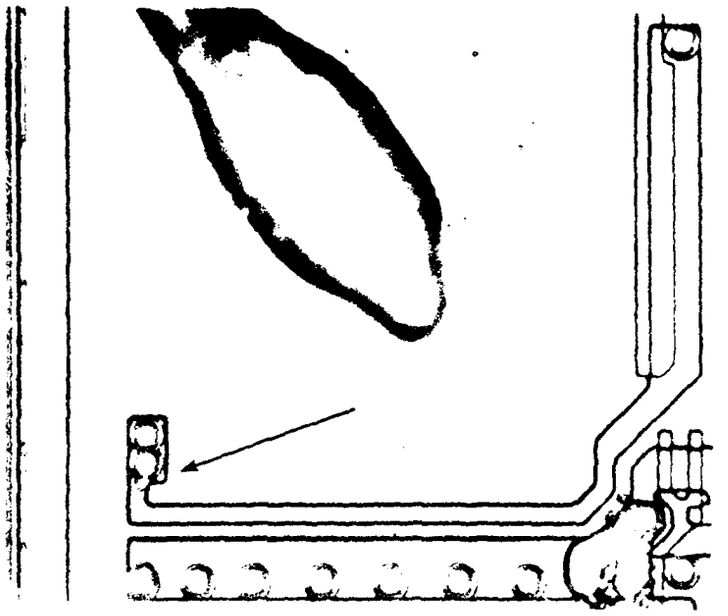


Figure V.B.28 - HBD Stress, Pin 5 Input Damage

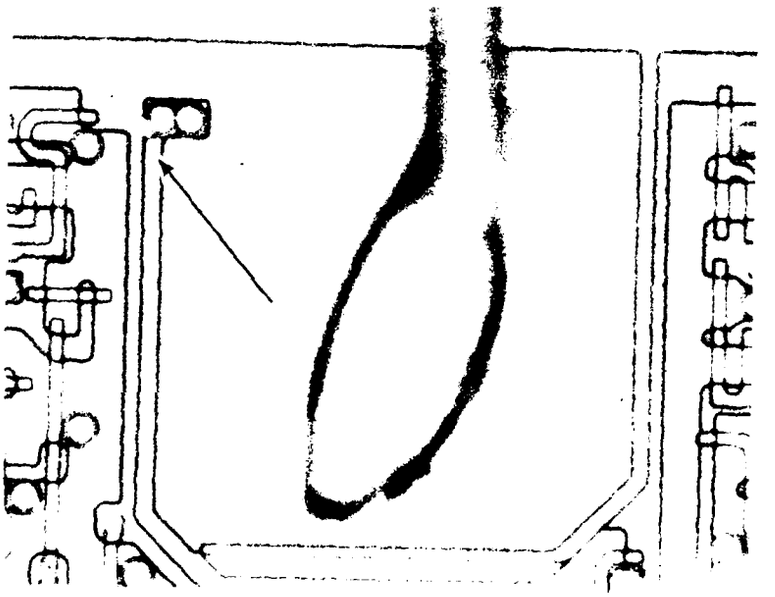


Figure V.B.29 - HBD Stress, Pin 22 Input Damage

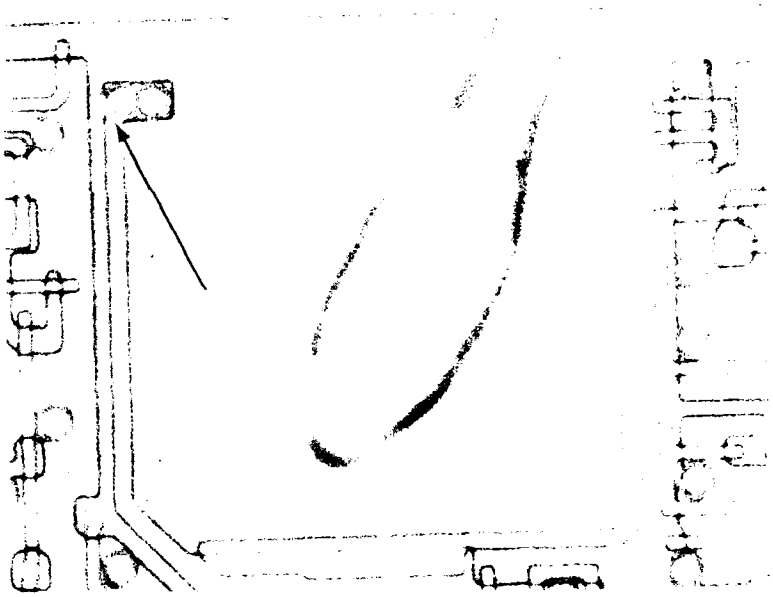


Figure V.B.30 - HBD Stress, Pin 21 Input Damage

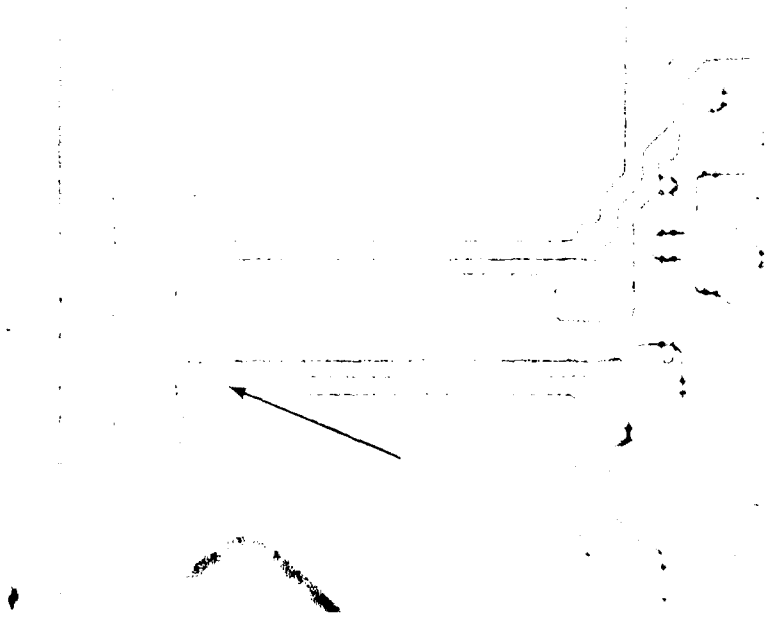
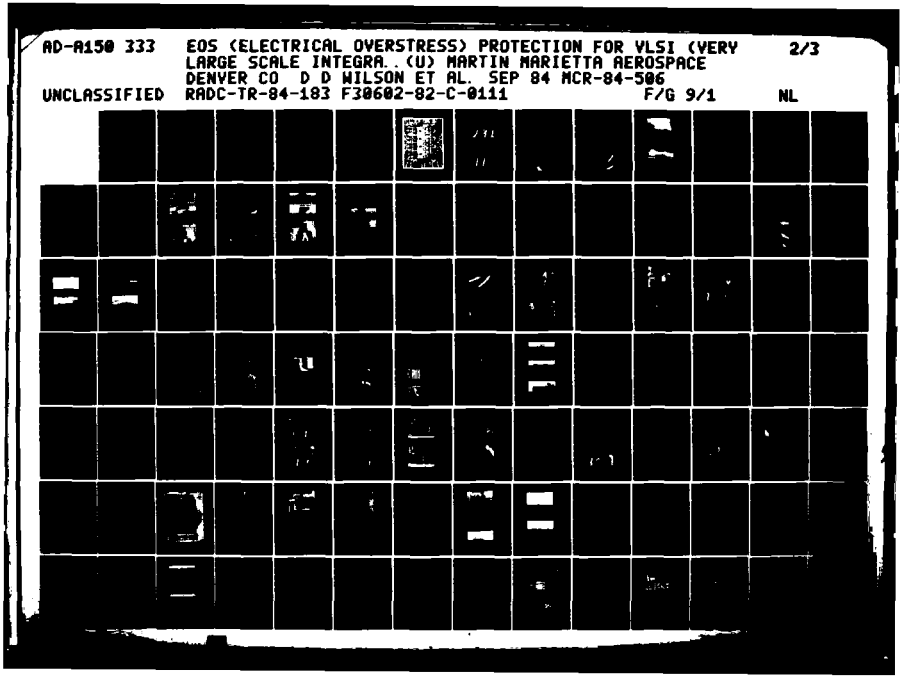
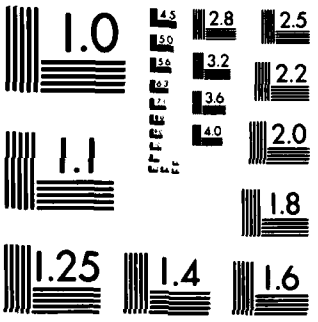


Figure V.B.31 - HPD Stress, Pin 20 Input Damage

AD-A150 333 EOS (ELECTRICAL OVERSTRESS) PROTECTION FOR VLSI (VERY 2/3
LARGE SCALE INTEGRA..(U) MARTIN MARIETTA AEROSPACE
DENVER CO D D WILSON ET AL. SEP 84 MCR-84-506
UNCLASSIFIED RADC-TR-84-183 F30602-82-C-0111 F/G 9/1 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

C. Part C Analysis

This device is an octal D-type transparent latch manufactured using Advanced Low-Power Schottky (ALS) processing. This utilizes an oxide-isolated, ion-implanted process.

There are two layers of metallization. The top layer is primarily the VCC and VSS interconnects. This part was in a 20-pin dual-in-line ceramic package. An overall die photo is shown in Figure V.C.1. VCC is pin 20 at the top of the figure and VSS is pin 10 at the bottom.

The VCC pin is shown in Figure V.C.2. It has two bond wires and the metallization exits from it and goes to numerous points, primarily pull-up resistors.

The ground pin is shown in Figure V.C.3 and it also has two bond wires. The metallization is connected to diodes and to the emitter of numerous transistors.

The 8 latch input pins are along the left side of the die. These are identical except for longer metallization runs on pins 2, 3, 8 and 9. A typical input is shown in Figure V.C.4. The components are labeled and correspond to the schematic in Figure V.C.5. The inputs on pins 1 and 11 are a different layout than the other eight. The schematics are essentially the same.

The reverse bias junction breakdowns of D1 and Q1 base-emitter and Q1 base-collector were all 28 volts. The NPN transistor was characterized and had a base-emitter breakdown of 7 volts and a base-collector breakdown of 30 volts. Other component configurations were electrically characterized to aid in the failure isolation. It was difficult to determine visually the different junction contacts, however, by characterizing the test structures the components could be more easily recognized.

The eight outputs are along the right hand side of Figure V.C.1 and one of these is shown in Figure V.C.6. This is a standard output stage as shown in Figure V.C.7.

The output layouts are identical except for longer metallization runs to pins 12, 13, 18 and 19.

Microsections were performed to examine the structures utilized. Figure V.C.8 shows a microsection through an input structure. The components are labeled the same way as in Figure V.C.4. A second microsection is shown in Figure V.C.9. This was etched for a shorter time and the diffusion depths are more readily measurable. The dimensions measured include: epitaxial thickness = 7 microns, p-diffusion = 4 microns, n-type layer = 1 micron, shallow p-diffusion = 0.5 microns, dielectric between metallization layers = 0.5 microns, dielectric between metallization and silicon = 0.5 to 1.5 microns.

Electrical Testing

A sample of the electrical data taken on each of the stressed parts and the control part at each iteration during the testing is shown in Figures V.C.10 and V.C.11. Figure V.C.10 shows the initial readings on serial number 3 and Figure V.C.11 shows the readings after the +1000 volt stress.

The input pins were measured for I_I, I_{IH}, I_{IL} and V_{IK}. The first three measurements are input current measurements taken at 7.0 volts, 2.7 volts, and 0.4 volts respectively. The V_{IK} measurement verifies the presence of a reverse bias protection diode at each input.

The output pins were measured for V_{OH}, V_{OL}, I_O, I_{OZH} and I_{OZL}. These measurements verified proper functional operation of the outputs in their normal operating mode and in their high impedance mode.

A functional verification of the output control pin was included, however, the enable pin was not placed in the low state (disabled condition).

Charged Device Data Analysis

Serial numbers 17-31 were stressed with the charged device simulation model. A summary of the pins which failed the I_{IH} or I_I measurements and the point at which they failed is shown in Figure V.C.12. These data indicate that the parts are more susceptible to a negative stress than a positive stress and that there is a significant difference in sensitivity between pins.

The leakage currents seen on a single device, serial number 17, are shown in Figure V.C.13. The leakage currents go from low nanoamp readings to microamp readings. This size of change is different than was seen on the bipolar input protect circuitry on the MOS devices, which degraded slowly through the nanoamp region.

No functional failures occurred during this testing. The inputs were removed from stress as soon as they exceeded the 20 microamp specification. This leakage current level was enough to provide sensitivity information without creating excessive damage to the part.

The input pin layouts are shown in Figures V.C.14 through 18. Figure V.C.14 shows pin 1 and Figure V.C.15 shows pin 11. These inputs have similar layouts. The junction which became leaky was the base/collector and this is labeled. This is the standard PNP input with the base connected to the input pin and the collector connected to ground.

Pins 2 through 9 have the same input schematic and layout with the only difference being the length of the metallization connecting the bond pad to the base.

The layout of pin 2 is the same as pin 9 and the layout of pin 3 is the same as pin 8. These are shown in Figures V.C.16 and V.C.17.

Pins 4 through 7 have identical layouts and are as shown in Figure V.C.18.

Visual inspection found no apparent damage on the inputs which had excessive leakage current. Various failure analysis techniques were used to locate the failures. Input to ground electrical measurements found that the damage on pins 1 and 11 created leakage at low voltage levels, i.e. 10 microamps at 0.2 volts. The damage on pins 2 through 9 created leakage at a higher voltage level, i.e. 10 microamps at 2.0 volts. Inputs 1 and 11 developed degraded base/collector junctions while inputs 2 through 9 developed degraded D1 diodes (reference Figure V.C.5).

One device was chemically stripped and examined. No damage was visible on the die surface. The part was stained with sirtl etch and examined. No damage was visible. Current was forced through the damaged junctions on a second device, serial number 18, with liquid crystal on the part. The locations of the failures were evident. The die surface was then washed to remove the liquid crystal and higher current (50 mA) was forced through the failure sites to make the damaged area visible for documentation. The damage produced was at the leakage current sites and made the damage much worse than was caused by the ESD stress.

Input pin 11 is shown in Figure V.C.19. This was typical of the location of the failures which occurred on pins 1 and 11. Input pin 7 is shown in Figure V.C.20. The location is typical of the location of the failures which occurred on pins 2 through 9.

With an understanding of the physical layout and the failure modes a better understanding of the variation in pin sensitivity is possible. The stress which created the major leakage on these parts was the negative voltage. This is due to the fact that this polarity produced a reverse bias stress on the input junction. The device is charged negative and then discharges out of the pin which is connected for stress. The pin is the cathode connection and the rest of the part which is charged negative is the anode connection, thus the reverse bias stress. Note that this is opposite of that which occurs for the human body discharge failure mode.

In Figure V.C.12 the -750 volt stress level appears to be the best point at which to analyze the data since all parts were still in stress and all but four of the pins were damaged.

Pins 1 and 11 are not very susceptible to damage. The base/collector junction is much more tolerant of ESD stress than the Schottky diode. Pins 2, 3, 8 and 9 are much less susceptibe to damage than pins 4, 5, 6 and 7. This is due to the longer metallization in series with the discharge path.

Two changes could decrease the input sensitivity; 1. Place the Schottky diodes (D1) on the opposite side of the input structure from the base contact, 2. Increase the metallization length between the bond pad and the

base contact. The first change appears to be a practical method for reduced sensitivity. The second change may require excessive chip real estate and some loss in speed, however, it could also be incorporated with little change in the manufacturing of the device.

Human Body Discharge Data Analysis

Device serial numbers 2 through 16 were stressed with the human body ESD simulation test method. A summary of the pins which failed I_{IH} or I_I measurements and the point at which they failed is shown in Figure V.C.21. These data indicate that the parts are more susceptible to a positive stress than a negative stress.

The leakage currents seen on a single device, serial number 3, are shown in Figure V.C.22. These leakage currents go from low nanoamp readings to microamp readings. This is the same type of change as that experienced by the charged device parts.

No functional failures occurred during this testing. This is due to the inputs being removed from stress when they reached 20 microamps. The sensitivity of the devices to the positive stress is due to the input being an n-type diffusion. The reverse biased input junction is much more susceptible to stress than a forward biased junction.

Visual inspection was performed on each of the 15 parts. There was no visible damage. One device was sequentially stripped and examined and no damage was visible. Serial number 8 was then examined with liquid crystal and the failure locations were found to be the same as seen for the charged device group. Examples of two of these inputs are shown in Figures V.C.23 and V.C.24. The failure sites were accentuated by forcing current through them.

The major factor that affects the sensitivity of the various inputs is the type of diffusion that is adjacent to the input base contact. Pins 1 and 11 have the collector adjacent to the base and these were the least sensitive. This remains true up to the final stress with the exception of pin 9 which is very insensitive to damage. No physical reason was found for this.

The two groups of parts were found to fail with the same failure mode and with similar layout sensitivity. The HBD stress created earlier leakage current failures than the CD stress but the CD parts all had failed at a lower voltage.

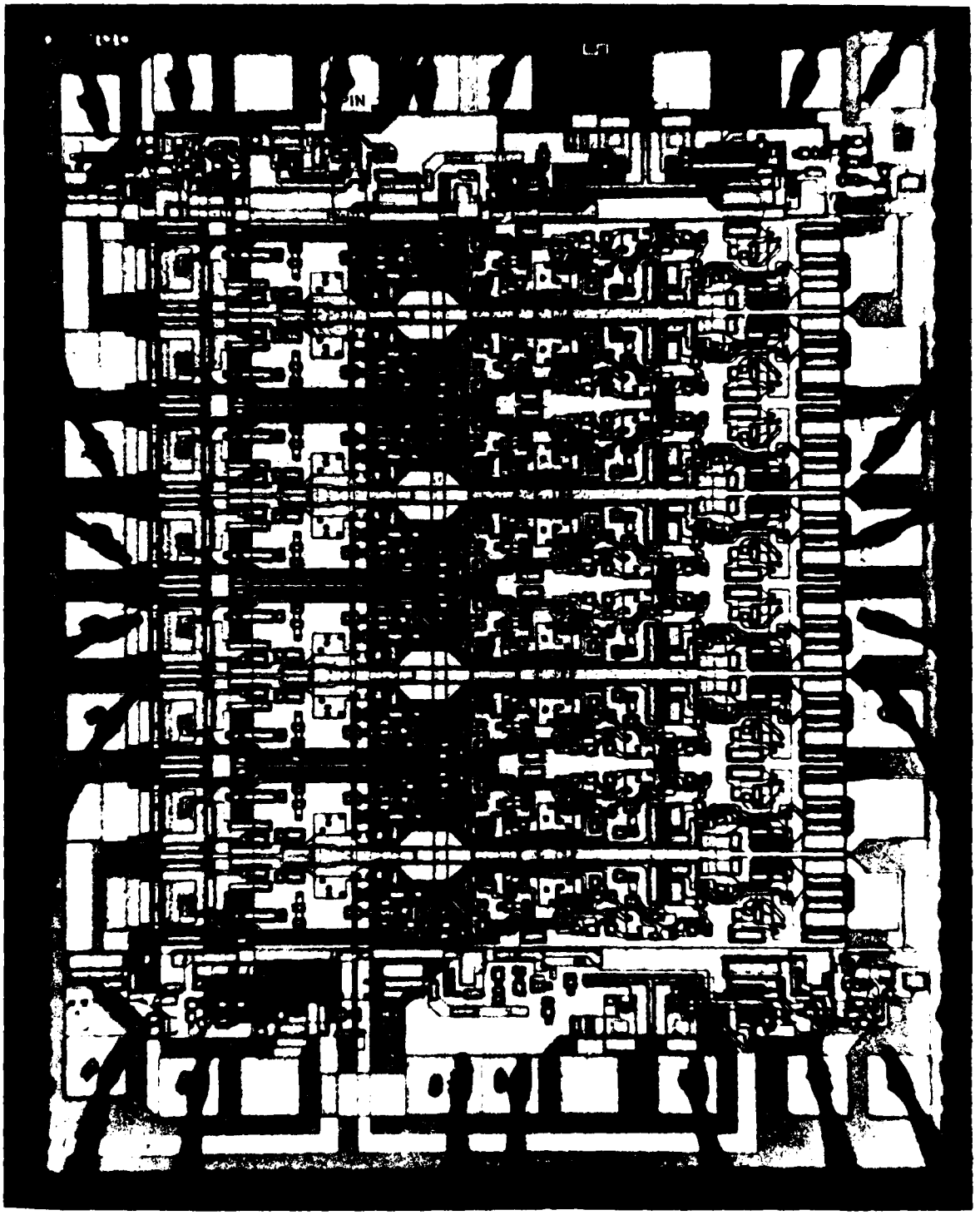


Figure V.C.1 - Overall Die Photograph

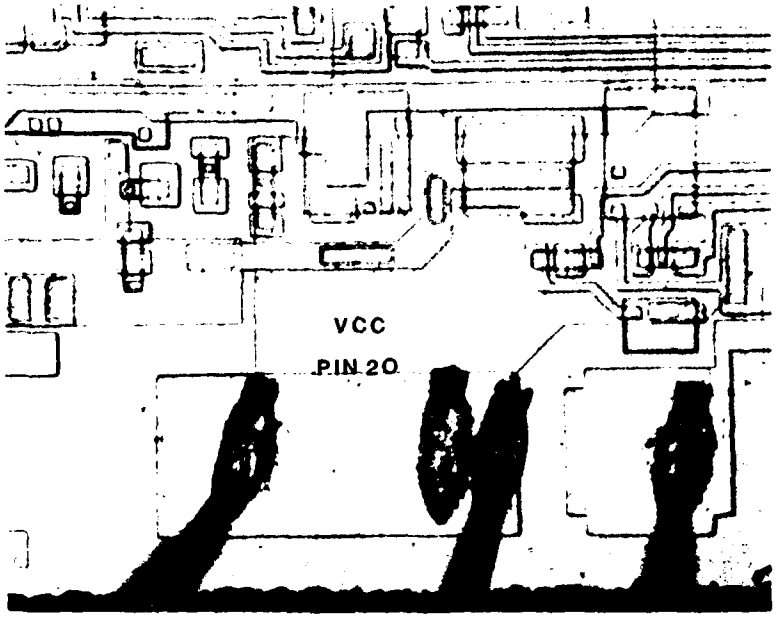


Figure V.C.2 - VCC Bond Pad

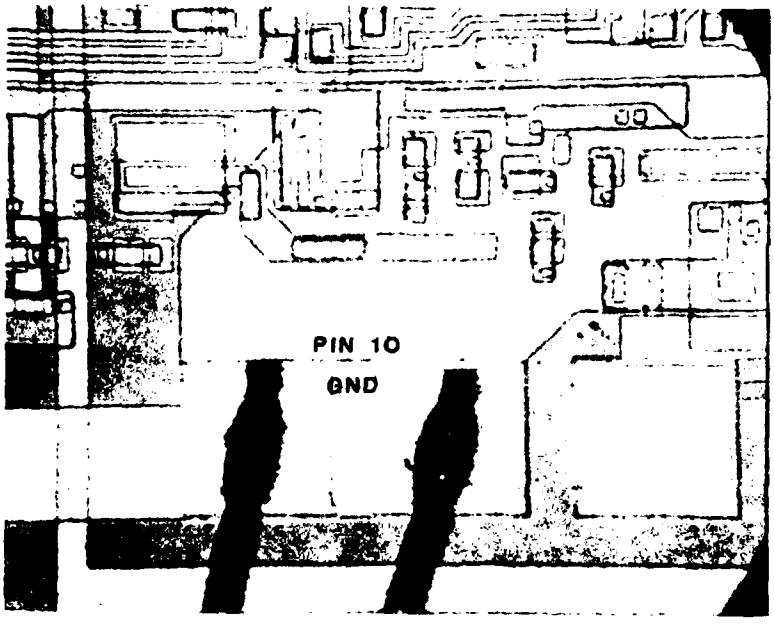


Figure V.C.3 - VSS Bond Pad

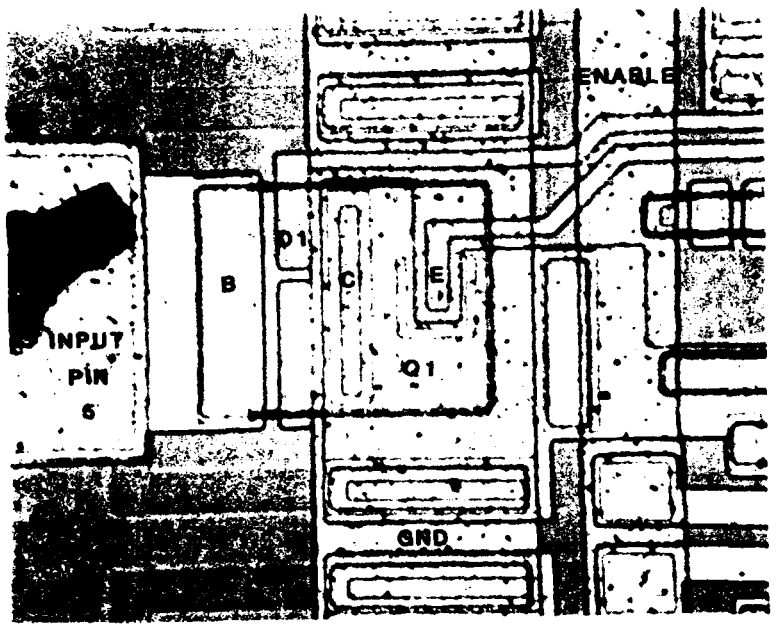


Figure V.C.4 - Pin 5 Input

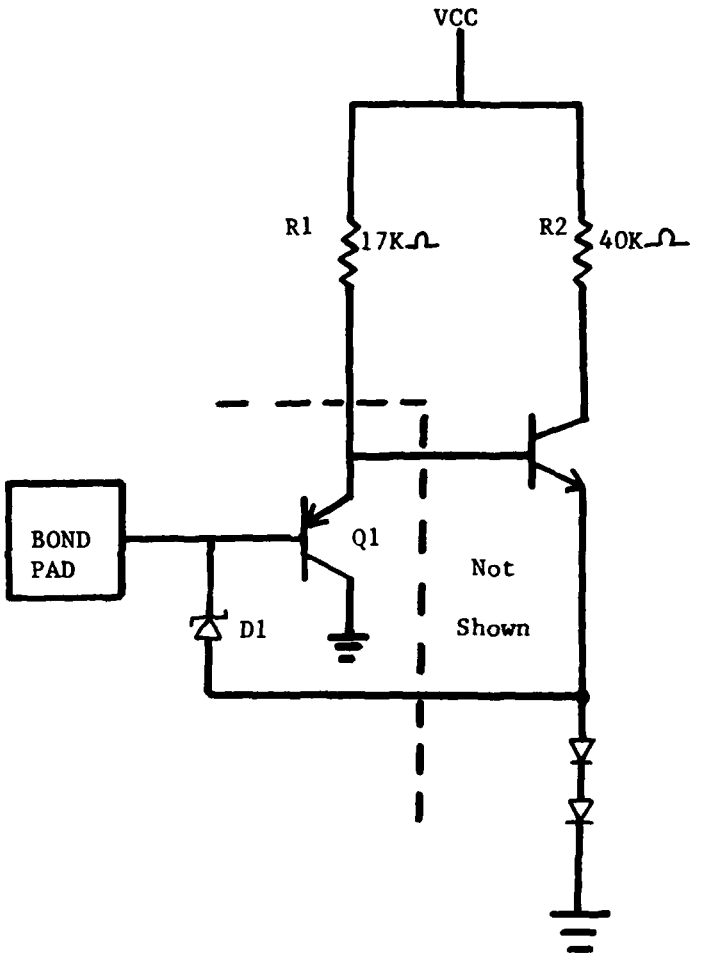


Figure V.C.5 - Input Schematic

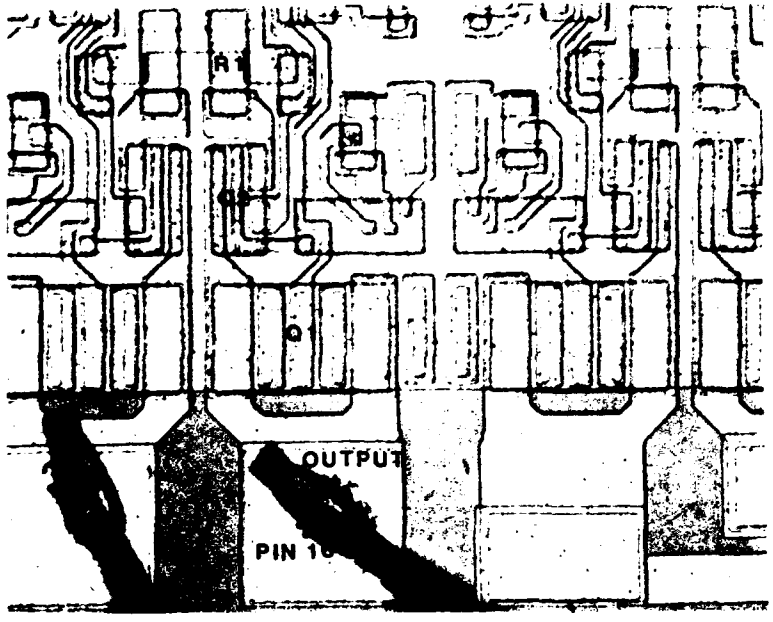


Figure V.C.6 - Pin 16 Output

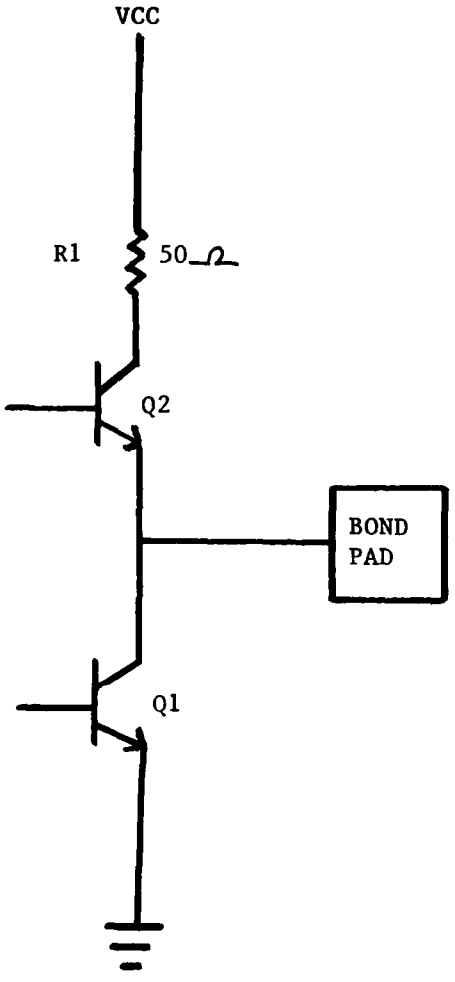


Figure V.C.7 - Output Schematic

Figure V.C.8 - Input Transistor Cross-Section

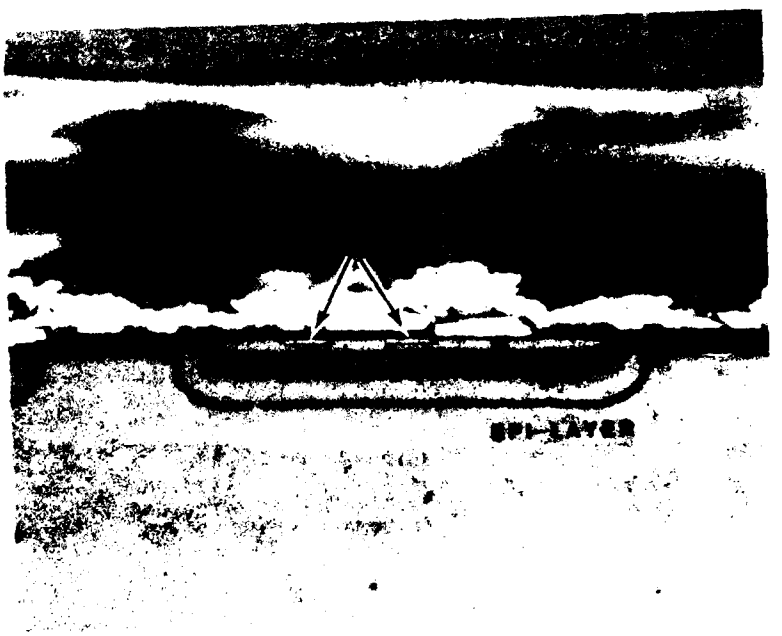


Figure V.C.9 - Internal Transistor Cross-Section

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :147 SERIAL NUMBER - 3
TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 30 JUN 83 AT 08:16:51 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	VOH	- - - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOL	- - - - - - -	274.5MV	--	400.0MV
	VOL	- - - - - - -	272.5MV	--	400.0MV
	VOL	- - - - - - -	268.0MV	--	400.0MV
	VOL	- - - - - - -	267.5MV	--	400.0MV
	VOL	- - - - - - -	268.5MV	--	400.0MV
	VOL	- - - - - - -	294.0MV	--	400.0MV
	VOL	- - - - - - -	274.0MV	--	400.0MV
	VOL	- - - - - - -	272.5MV	--	400.0MV
	VIK	- - - - - - -	-925.0MV	-1.500 V	--
	VIK	- - - - - - -	-925.0MV	-1.500 V	--
	VIK	- - - - - - -	-920.0MV	-1.500 V	--
	VIK	- - - - - - -	-920.0MV	-1.500 V	--
	VIK	- - - - - - -	-920.0MV	-1.500 V	--
	VIK	- - - - - - -	-920.0MV	-1.500 V	--
	VIK	- - - - - - -	-925.0MV	-1.500 V	--
	VIK	- - - - - - -	-925.0MV	-1.500 V	--
	IIH	- - - - - - -	2.650NA	--	20.00UA
	IIH	- - - - - - -	1.650NA	--	20.00UA
	IIH	- - - - - - -	1.450NA	--	20.00UA
	IIH	- - - - - - -	1.350NA	--	20.00UA
	IIH	- - - - - - -	1.400NA	--	20.00UA
	IIH	- - - - - - -	1.300NA	--	20.00UA
	IIH	- - - - - - -	1.350NA	--	20.00UA
	IIH	- - - - - - -	1.400NA	--	20.00UA
	IIL	- - - - - - -	-40.50UA	-200.0UA	--
	IIL	- - - - - - -	-40.00UA	-200.0UA	--
	IIL	- - - - - - -	-41.00UA	-200.0UA	--
	IIL	- - - - - - -	-40.50UA	-200.0UA	--
	IIL	- - - - - - -	-42.00UA	-200.0UA	--
	IIL	- - - - - - -	-41.50UA	-200.0UA	--
	IIL	- - - - - - -	-40.00UA	-200.0UA	--
	IIL	- - - - - - -	-40.00UA	-200.0UA	--
	IO	- - - - - - -	-35.90MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-36.30MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-36.30MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-36.50MA	-120.0MA	-20.00MA

Figure V.C.10 - Initial Electrical Measurements

FILE UID :147 SERIAL NUMBER - 3

TESTED AT 25 DEG. C NO. 1 ELECTRICAL

ON 30 JUN 83 AT 08:17:20 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IO	- - - - - - -	-36.25MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-35.20MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-36.05MA	-120.0MA	-20.00MA
	IO	- - - - - - -	-36.25MA	-120.0MA	-20.00MA
	ICCH	- - - - - - -	11.15MA	--	14.00MA
	ICCL	- - - - - - -	17.05MA	--	22.00MA
	ICCZ	- - - - - - -	18.15MA	--	24.00MA
	IOZH	- - - - - - -	4.350NA	--	20.00UA
	IOZH	- - - - - - -	3.500NA	--	20.00UA
	IOZH	- - - - - - -	3.750NA	--	20.00UA
	IOZH	- - - - - - -	3.100NA	--	20.00UA
	IOZH	- - - - - - -	3.050NA	--	20.00UA
	IOZH	- - - - - - -	2.950NA	--	20.00UA
	IOZH	- - - - - - -	3.200NA	--	20.00UA
	IOZH	- - - - - - -	3.050NA	--	20.00UA
	IOZL	- - - - - - -	1.750NA	-20.00UA	--
	IOZL	- - - - - - -	1.700NA	-20.00UA	--
	IOZL	- - - - - - -	1.900NA	-20.00UA	--
	IOZL	- - - - - - -	1.950NA	-20.00UA	--
	IOZL	- - - - - - -	2.150NA	-20.00UA	--
	IOZL	- - - - - - -	1.950NA	-20.00UA	--
	IOZL	- - - - - - -	2.200NA	-20.00UA	--
	IOZL	- - - - - - -	2.150NA	-20.00UA	--
	II	- - - - - - -	7.100NA	--	100.0UA
	II	- - - - - - -	4.650NA	--	100.0UA
	II	- - - - - - -	4.000NA	--	100.0UA
	II	- - - - - - -	3.500NA	--	100.0UA
	II	- - - - - - -	3.000NA	--	100.0UA
	II	- - - - - - -	3.000NA	--	100.0UA
	II	- - - - - - -	3.000NA	--	100.0UA
	II	- - - - - - -	2.900NA	--	100.0UA

TEST RUNTIME IS 11 SECONDS

PRINT / DISPLAY TIME IS 53 SECONDS

Figure V.C.10 - Initial Electrical Measurements (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID #147 SERIAL NUMBER - 3

TESTED AT 25 DEG. C NO. 7 ELECTRICALS

ON 02 SEP 83 AT 08:38 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	VOH	-2.930 V	2.930 V	2.400 V	--
	VOH	-2.925 V	2.925 V	2.400 V	--
	VOH	-2.930 V	2.930 V	2.400 V	--
	VOH	-930.0MV	2.930 V	2.400 V	--
	VOH	-2.923 V	2.930 V	2.400 V	--
	VOH	-1.000E+33 V	2.920 V	2.400 V	--
	VOH	-1.915 V	2.915 V	2.400 V	--
	VOH	-2.920 V	2.925 V	2.400 V	--
	VOL	-290.0MV	290.0MV	--	400.0MV
	VOL	-282.5MV	282.5MV	--	400.0MV
	VOL	-277.4MV	277.5MV	--	400.0MV
	VOL	1.718 V	282.0MV	--	400.0MV
	VOL	-283.0MV	283.0MV	--	400.0MV
	VOL	-321.0MV	321.0MV	--	400.0MV
	VOL	29.66 V	338.0MV	--	400.0MV
	VOL	-281.0MV	281.0MV	--	400.0MV
	VIK	930.0MV	-930.0MV	-1.500 V	--
	VIK	925.0MV	-925.0MV	-1.500 V	--
	VIK	935.0MV	-935.0MV	-1.500 V	--
	VIK	925.0MV	-925.0MV	-1.500 V	--
	VIK	940.0MV	-940.0MV	-1.500 V	--
	VIK	925.0MV	-925.0MV	-1.500 V	--
	VIK	965.0MV	-965.0MV	-1.500 V	--
	VIK	935.0MV	-935.0MV	-1.500 V	--
****	IIH	-11.00UA	11.00UA	--	20.00UA
	IIH	-2.050NA	1.300NA	--	20.00UA
****	IIH	-33.50UA	33.50UA	--	20.00UA
****	IIH	-66.50UA	66.50UA	--	20.00UA
****	IIH	-36.80UA	36.80UA	--	20.00UA
	IIH	-2.650NA	1.650NA	--	20.00UA
	IIH	-25.00PA	1.400NA	--	20.00UA
****	IIH	-73.75UA	73.75UA	--	20.00UA
	IIH	950.0PA	400.0PA	--	20.00UA
****	IIH	-81.25UA	81.25UA	--	20.00UA
	IIL	2.000 A	-42.00UA	-200.0UA	--
	IIL	39.50UA	-39.50UA	-200.0UA	--
	IIL	43.50UA	-43.50UA	-200.0UA	--
	IIL	43.00UA	-43.00UA	-200.0UA	--
	IIL	1.000 A	-44.50UA	-200.0UA	--
	IIL	400.0MA	-41.00UA	-200.0UA	--
	IIL	-1.000E+33 A	-40.00UA	-200.0UA	--
	IIL	1.000 A	-42.50UA	-200.0UA	--
	IIL	25.53MA	-26.00UA	-200.0UA	--
	IIL	51.00UA	-51.00UA	-200.0UA	--
	IO	35.25MA	-35.25MA	-120.0MA	-20.00MA

Figure V.C.11 - Electrical Measurements Following the +1000 Volt Stress

FILE UID :147 SERIAL NUMBER - 3

TESTED AT 25 DEG. C NO. 7 ELECTRICALS

ON 02 SEP 83 AT 08:38 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IO	223.5E+06 A	-35.90MA	-120.0MA	-20.00MA
	IO	35.85MA	-35.85MA	-120.0MA	-20.00MA
	IO	35.80MA	-35.80MA	-120.0MA	-20.00MA
	IO	35.65MA	-35.65MA	-120.0MA	-20.00MA
	IO	34.00MA	-34.00MA	-120.0MA	-20.00MA
	IO	33.20MA	-33.20MA	-120.0MA	-20.00MA
	IO	35.85MA	-35.85MA	-120.0MA	-20.00MA
	ICCH	-11.15MA	11.15MA	--	14.00MA
	ICCL	-16.85MA	16.85MA	--	22.00MA
	ICCZ	-18.10MA	18.10MA	--	24.00MA
	IOZH	-5.150NA	5.150NA	--	20.00UA
	IOZH	-4.100NA	4.100NA	--	20.00UA
	IOZH	-4.250NA	4.250NA	--	20.00UA
	IOZH	-3.550NA	3.550NA	--	20.00UA
	IOZH	-3.400NA	3.400NA	--	20.00UA
	IOZH	3.250NA	3.250NA	--	20.00UA
	IOZH	3.300NA	3.300NA	--	20.00UA
	IOZH	3.000NA	3.000NA	--	20.00UA
	IOZL	906.8E+09 A	2.000NA	-20.00UA	--
	IOZL	10.51E+06 A	1.850NA	-20.00UA	--
	IOZL	-1.850NA	1.850NA	-20.00UA	--
	IOZL	219.4KA	1.800NA	-20.00UA	--
	IOZL	-1.750NA	1.750NA	-20.00UA	--
	IOZL	203.6KA	1.700NA	-20.00UA	--
	IOZL	-1.700NA	1.700NA	-20.00UA	--
	IOZL	1.650NA	1.650NA	-20.00UA	--
***	II	-526.5UA	526.5UA	--	100.0UA
	II	3.315 A	3.050MA	--	100.0UA
***	II	-442.5UA	442.5UA	--	100.0UA
***	II	-753.5UA	753.5UA	--	100.0UA
***	II	-283.0UA	283.0UA	--	100.0UA
	II	-3.750NA	3.750NA	--	100.0UA
	II	-3.000NA	3.000NA	--	100.0UA
***	II	-1.024MA	1.024MA	--	100.0UA
	II	-3.250NA	3.250NA	--	100.0UA
***	II	-1.024MA	1.024MA	--	100.0UA

Figure V.C.11 - Electrical Measurements Following the +1000 Volt Stress (Cont.)

Number of Failures at Pin Locations

1	2	3	4	5	6	7	8	9	11	Cumulative # Removed	Voltage
											+250
											-250
											+500
											-500
					3	1					+750
1		2	6	6	9	5	2	1			-750
1	1	3	7	8	9	6	2	2	1	3	+1000
2	6	8	11	12	11	7	9	3	11	15	-1000

Figure V.C.12 - CD Stress, Cumulative Leakage Failures

Leakage Current by Pin Number (nA except as noted)

1	2	3	4	5	6	7	8	9	11	Voltage
-	2.1	1.3	0.8	0.7	0.6	0.6	0.4	0.5	-	0
-	2.4	1.3	1.1	0.7	0.6	0.6	0.6	0.6	-	+250
-	2.1	1.2	1.0	0.7	0.6	0.7	0.6	0.6	-	-250
-	2.4	1.4	1.1	1.0	0.7	1.0	1.0	1.1	-	+500
0.8	2.7	1.7	1.4	1.2	1.0	1.0	0.9	1.0	0.8	-500
4.2	2.8	2.5	2.5	1.0uA	4.1	1.4	1.1uA	6.7	0.6	+750
4.2	2.3	2.0	2.2	1.0uA	15uA	0.6	28uA	7.2	1.0	-750
4.0	2.6	2.4	2.5	1.0uA	19uA	0.5	11uA	6.6	1.0	+1000
4.0	35uA	19	6.0	1.9uA	61uA	10	35uA	1.0uA	167uA	-1000

Figure V.C.13 - CD Stress, Serial Number 17 Leakage Current Summary

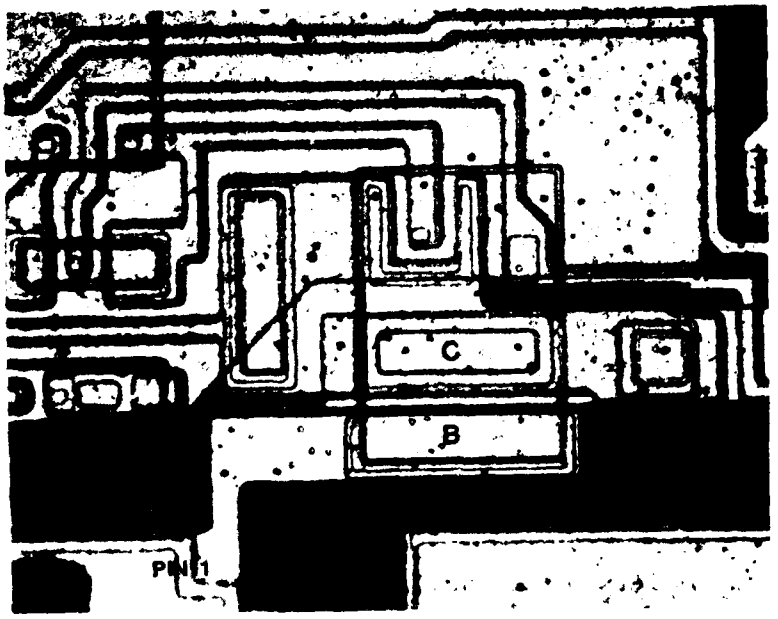


Figure V.C.14 - Pin 1 Input

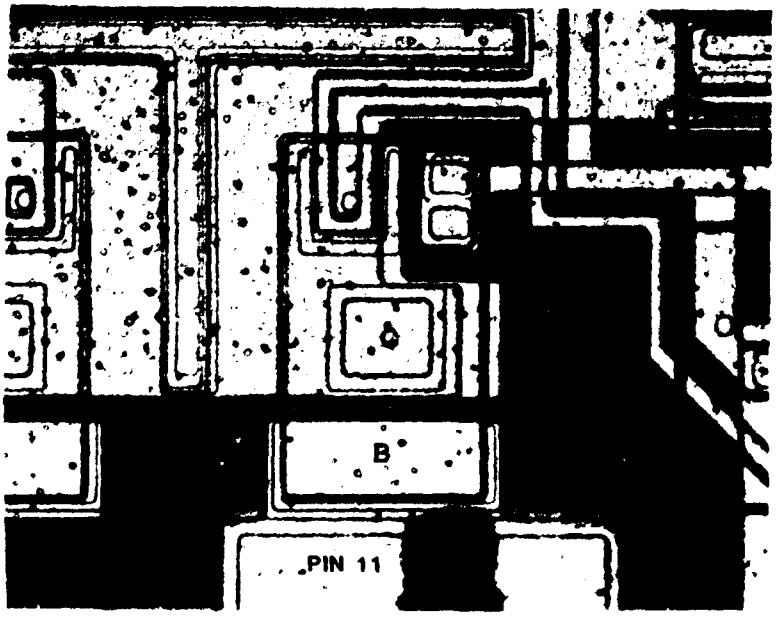


Figure V.C.15 - Pin 11 Input

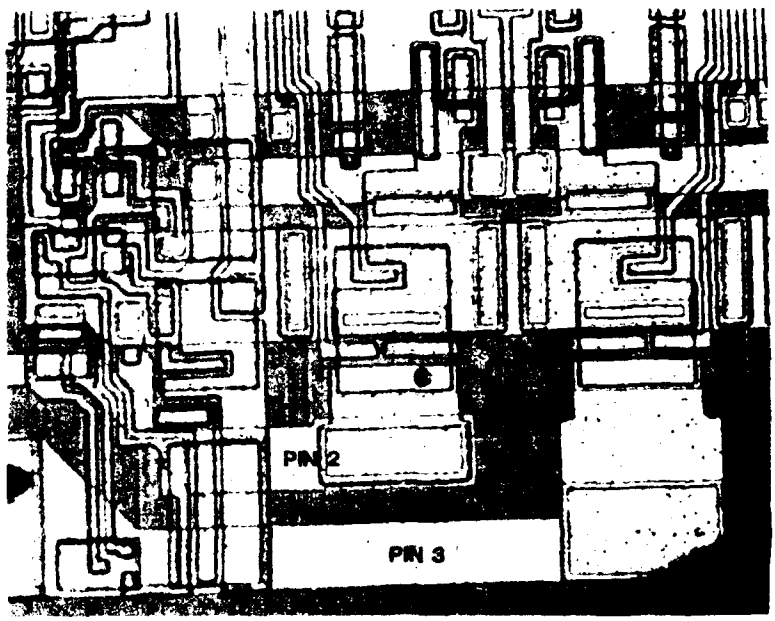


Figure V.C.16 - Input Pins 2 and 3

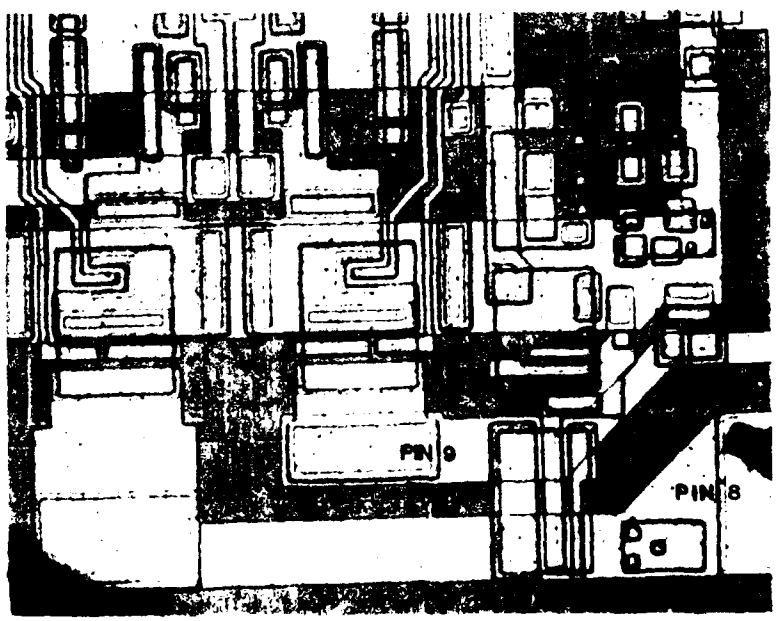


Figure V.C.17 - Input Pins 8 and 9

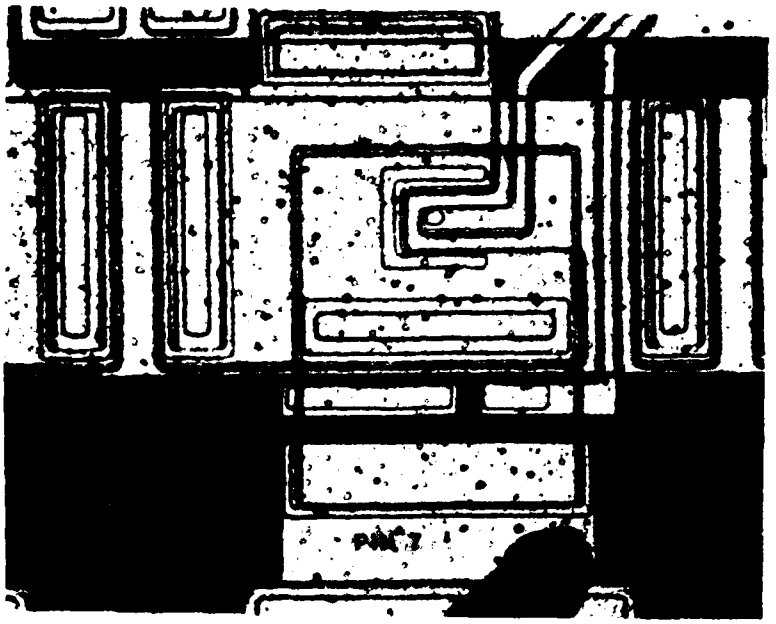


Figure V.C.18 - Pin 7 Input

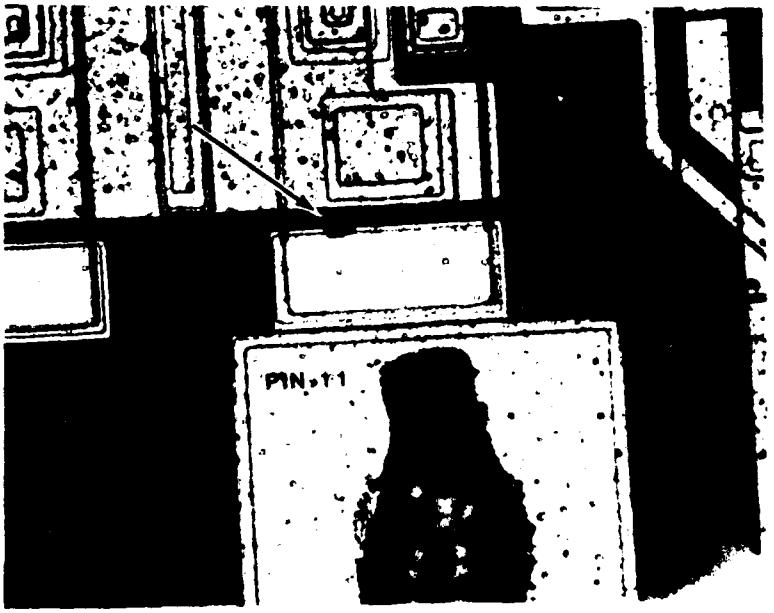


Figure V.C.19 - Pin 11 Input Failure Location.

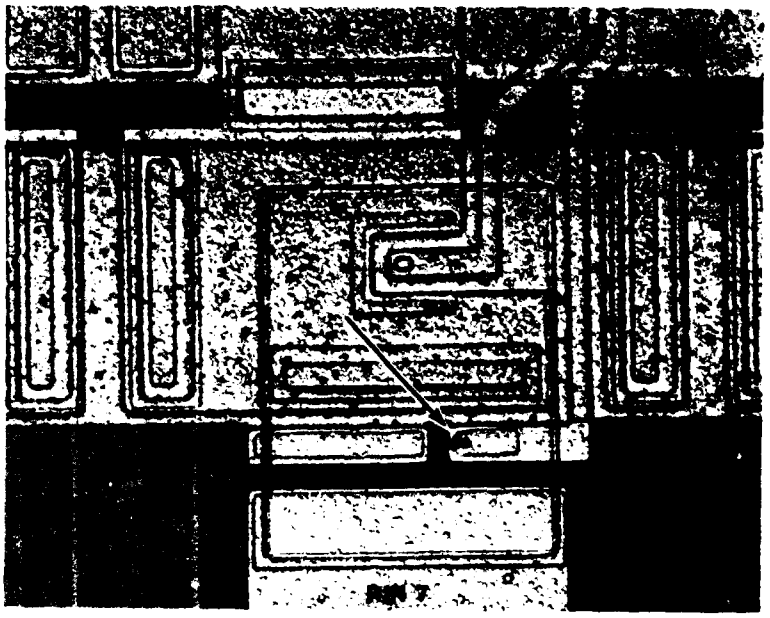


Figure V.C.20 - Pin 7 Input Failure Location.

Number of Failures at Pin Locations

1	2	3	4	5	6	7	8	9	11	Cumulative # Removed	Voltage
							1				+250
							1				-250
	2	2	3	2	2	1	5		1		+500
	2	2	3	2	2	1	5		1		-500
	2	2	3	2	2	1	5		1		+750
	2	2	3	2	2	1	5		1		-750
	4	4	4	3	4	2	5	2	2	3	+1000
	4	4	4	3	5	2	6	2	2	3	-1000
	5	5	5	7	9	4	7	2	3	5	+1250
	5	5	5	7	9	4	7	2	3		-1250
4	10	13	9	10	11	5	8	3	11	15	+1500

Figure V.C.21 - HBD Stress, Cumulative Leakage Failures

Leakage Current by Pin Number (nA except as noted)

1	2	3	4	5	6	7	8	9	11	Voltage
-	2.6	1.6	1.4	1.3	1.4	1.3	1.3	1.4	-	0
-	2.7	1.9	1.7	1.6	1.5	1.6	1.5	1.6	-	+250
-	2.6	1.8	1.5	1.4	1.4	1.4	1.4	1.4	-	-250
-	2.4	1.4	43uA	1.6	83uA	0.9	0.7	0.8	-	+500
1.3	3.0	2.1	36uA	1.2	80uA	1.7	1.5	1.4	1.4	-500
0.8	2.7	1.9	21uA	1.6	58uA	1.1	0.9	0.9	0.8	+750
0.6	2.0	1.2	44uA	1.0	35uA	1.2	0.9	0.8	0.7	-750
0.4	41uA	1.4	44uA	66uA	37uA	1.6	1.4	73uA	81uA	+1000

Figure V.C.22 - HBD Stress, Serial Numbr 17 Leakage Current Summary

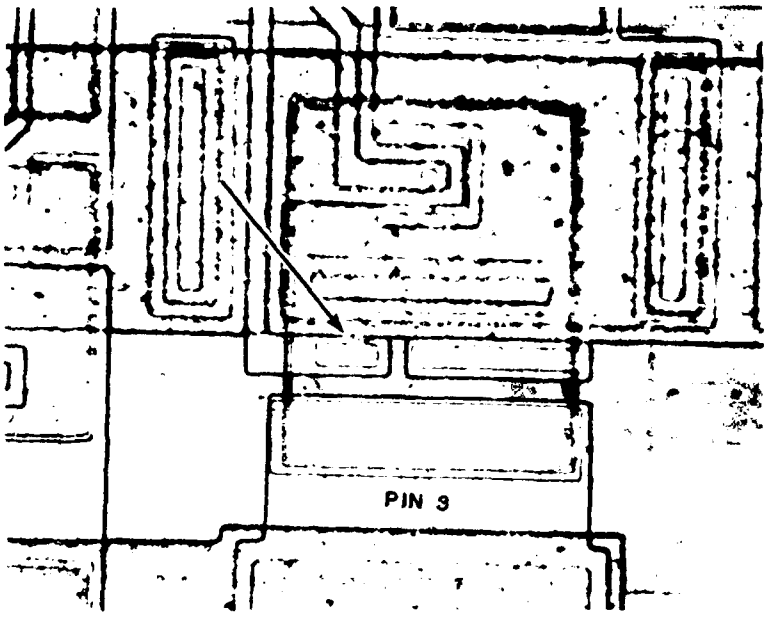


Figure V.C.23 - HBD Stress, Pin 3 Input Damage

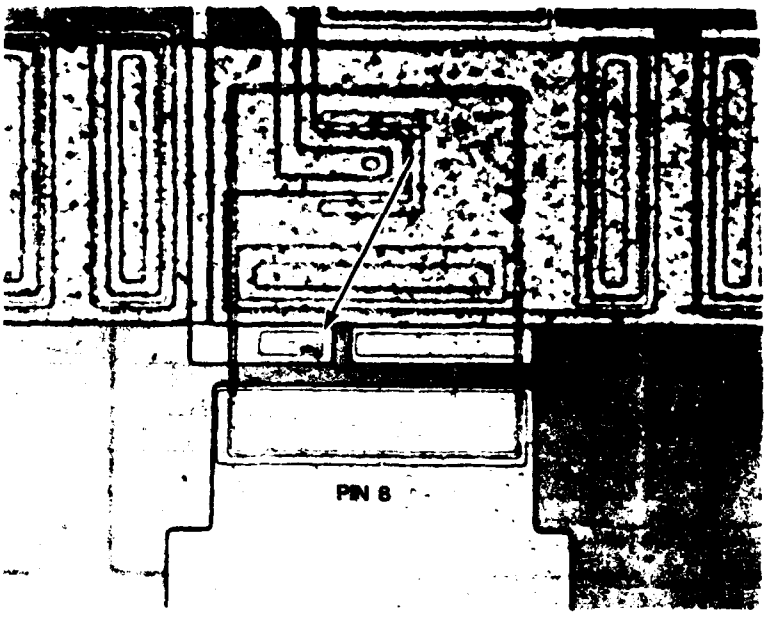


Figure V.C.24 - HBD Stress, Pin 8 Input Damage

D. Part D Analysis

This device is an Octal Transparent Latch with 3-state outputs manufactured with the Isoplanar II process. This is an oxide isolated technique which allows the oxide to come up to the edge of the emitter contact (walled emitter). This has a single level of metallization for the interconnects. These parts were in 20-pin dual-in-line ceramic packages.

An overall die photograph is shown in Figure V.D.1. VCC is pin 20 and is at the top of the figure and GND is pin 10 at the bottom of the figure. The ground metallization runs around the perimeter of the die and provides the contact to the anode for the diode on each input and output. The VCC metallization is in the center of the die. It is connected to pull-up resistors.

An input structure is shown in Figure V.D.2. The components are labeled corresponding to Figure V.D.3. The input transistor base-emitter and base-collector junctions and diode D1 all measured 20 VDC breakdown.

An output structure is shown in Figure V.D.4 and the schematic is shown in Figure V.D.5. The protect diode is not shown in Figure V.D.4 but is visible in the overall photograph.

Microsections were performed to examine the construction of the components. The input transistor is shown in Figure V.D.6. The top view is shown at 500X while the side view is shown at 1200X. The approximate thicknesses of the layers are: Metallization = 1.0 microns; p-Layer = 1.8 microns; n-Layer = 1.0 microns, dielectric between metallization and silicon = 1.0 microns.

The p-type emitter diffusion was not visible in the sections. The Schottky diode on each pin was also microsectioned and is shown in Figure V.D.7. The p-type Schottky diffusion is very shallow and is not visible in the section.

Electrical Testing

A sample of the electrical data which was taken on each of the stressed parts and the control part at each iteration during the testing is shown in Figure V.D.8 and V.D.9. Figure V.D.8 shows the initial readings on serial number 11 and Figure V.D.9 shows the readings on serial number 11 after the -2500 volt stress.

The VCD measurement verified the presence of the protect diode. Four devices failed this measurement at initial test, a resistive Schottky contact was found on these parts and they were not included in this test. These were serial numbers 2, 15, 16, and 18.

Device functionality was verified by the VOH and VOL tests. A functional verification of the output enable pin was included, however, the

latch enable pin was not placed in the low state (disabled condition). Leakage current at the inputs was measured with the I_{IH} (V_{IN} = 2.7 V) and I_{IL} (V_{IN} = 0.5 V) readings. Output circuit leakage was measured with the I_{OZH} (V_{OUT} = 2.4 V) and I_{OZL} (V_{OUT} = 0.5 V) readings.

The two readings which provide the most information on the gradual leakage increase are I_{IH} and I_{OZH}. I_{IH} increased considerably while little change occurred in the outputs.

Charged Device Data Analysis

Fourteen devices, serial number 17 and 19 through 31, were subjected to the charged device ESD simulation model. The first leakage failure (greater than 20 microamps) occurred at -750 volts and all parts were removed from test after the +1500 volt stress. All inputs became leaky and no other pins became leaky. The pin number and the voltage level at which leakage failures occurred are shown in Figure V.D.10. It is apparent that pins 1 and 11 were more sensitive to stress. It is also evident that the negative stress causes more damage than the positive stress. The negative stress sensitivity is consistent with the results seen on part C. This stress reverse biases the junction connected to the input pins and results in junction breakdown degradation.

The leakage current changes with stress application are shown for pin 1 on serial number 26 in Figure V.D.11. There is a jump from picoamps to microamps and damage is only worsened by the negative stress.

All inputs had identical layouts except for pins 1 and 11. The input shown in Figure V.D.2 and the inputs shown in Figure V.D.12 are the layout used on pins 3, 4, 7, 8, 13, 14, 17 and 18. The layout shown in Figure V.D.13 is the layout for pins 1 and 11.

Failure analysis found no evidence of physical damage; however, mechanical probing and isolation determined the component which degraded. This was the Schottky diode on the input. Slight degradation of the base-collector junction on the input transistor was noted for some pins. Current was forced through pin 18 and pin 11 on serial number 27. This accentuated the failure sites and these are shown in Figure V.D.14 and V.D.15.

The increased sensitivity of pins 1 and 11 is apparently due to the fact that the current is forced to flow out of the contact at the end of the Schottky diffusion rather than spread over the whole diode. Additional heating and damage results. The large ground metallization acts as a major portion of the capacitance which discharges out of the pin being stressed. This is the reason for the Schottky diode being damaged (as will be discussed, this is not the junction that is damaged by the human body discharge model).

Human Body Discharge Data Analysis

Twelve devices, serial numbers 3 through 14, were subjected to the human body ESD simulation model. The first leakage failure occurred at +500 volts and the last device was removed after the +2750 volt stress (Figure V.D.16). The failures at +500 V and +750 V occurred primarily on serial numbers 7 and 9. These were removed and there were no additional leakage failures until +1250 volts. The positive stress causes the major device damage due to the reverse biased junctions for this polarity. Typical leakage current changes are shown in Figure V.D.17 for pin 1 on serial number 3.

Failure analysis found no evidence of physical damage. Mechanical isolation and probing found that the junction which degraded was the base-collector junction on the input transistor. This was not expected since the Schottky diode had failed on the parts stressed with the charged device model. Current was forced through pins 7 and 11 on serial number 4 to accentuate the failure sites. These are shown in Figure V.D.18 and V.D.19.

This result indicates that the weakest junction is the base-collector. This junction was not damaged for the charged device model because it received a much lower stress level than the Schottky diode. The increased sensitivity of pins 1 and 11 to the HBD stress does not appear to be strictly related to physical layout. The layout does not appear to provide an explanation for the sensitivity difference. There is a difference in the current path to ground. The schematic is basically the same but the components are not identical. The junction marked D4 in Figure V.D.2 is different than the base-emitter junction on transistor Q1 in Figure V.D.20. The general layout and interconnects are also different.

These results indicate the significance of the different stress methods. The charged device model causes damage to junctions which are connected to large metallization areas while the human body model damages the most susceptible junction in the current path to ground.

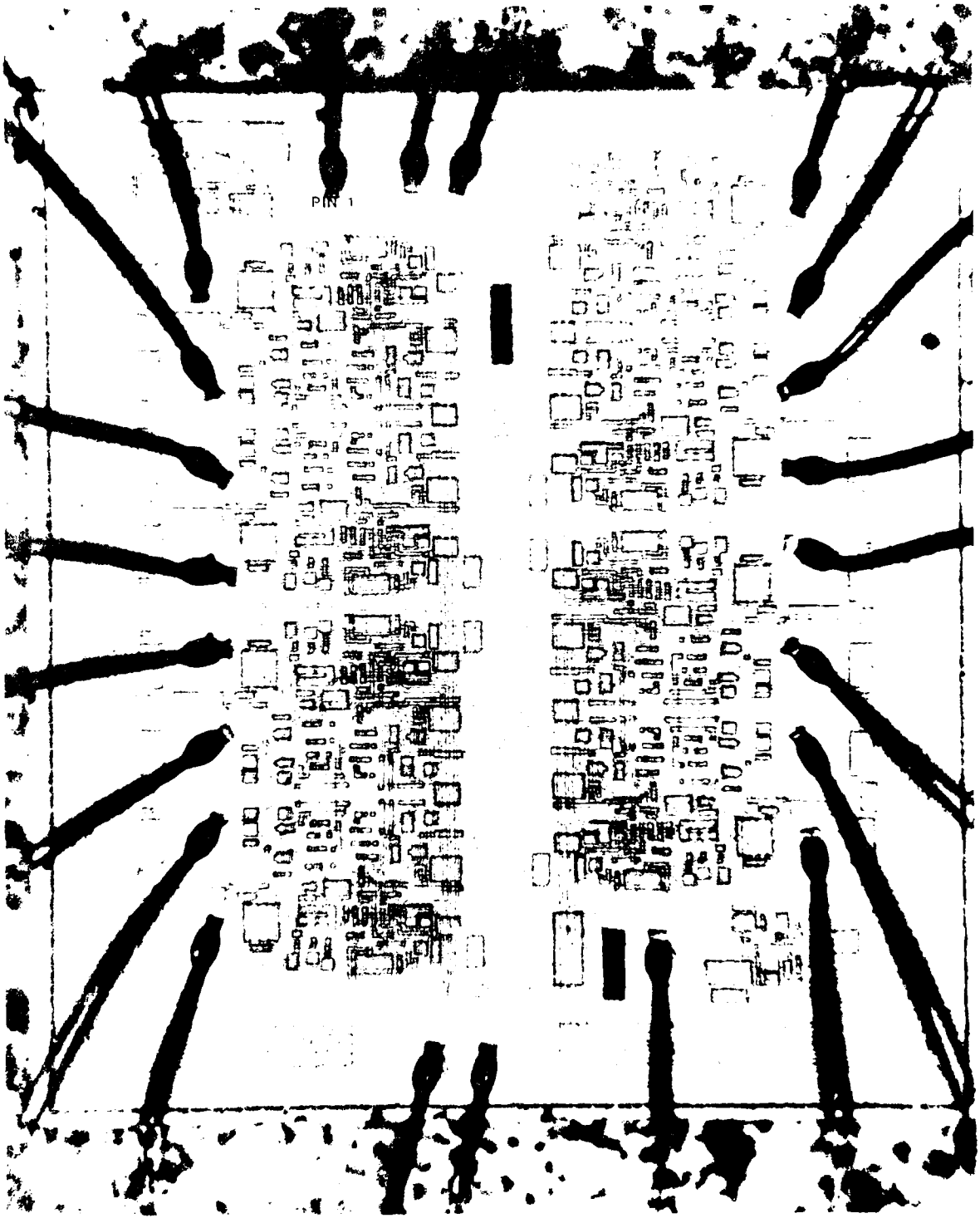


Figure V.P.1 - Overall Die Photograph

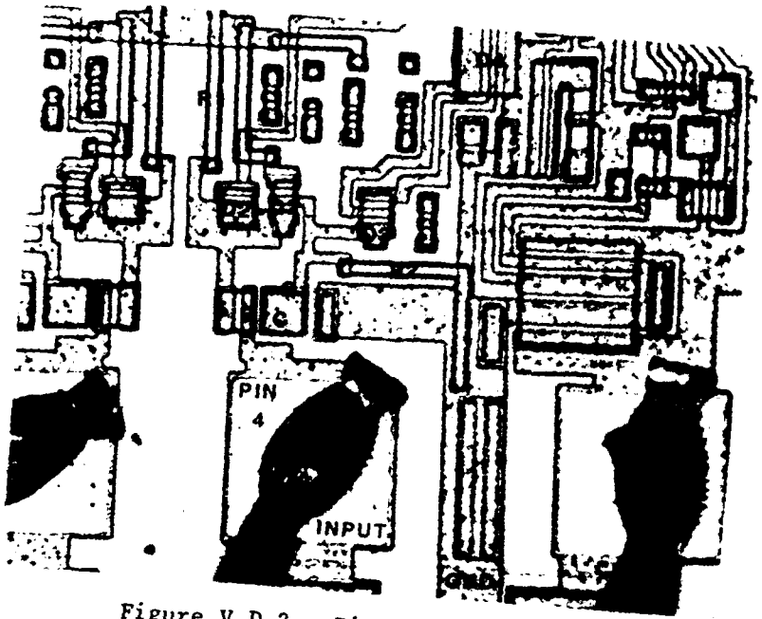


Figure V.D.2 - Pin 4 Input

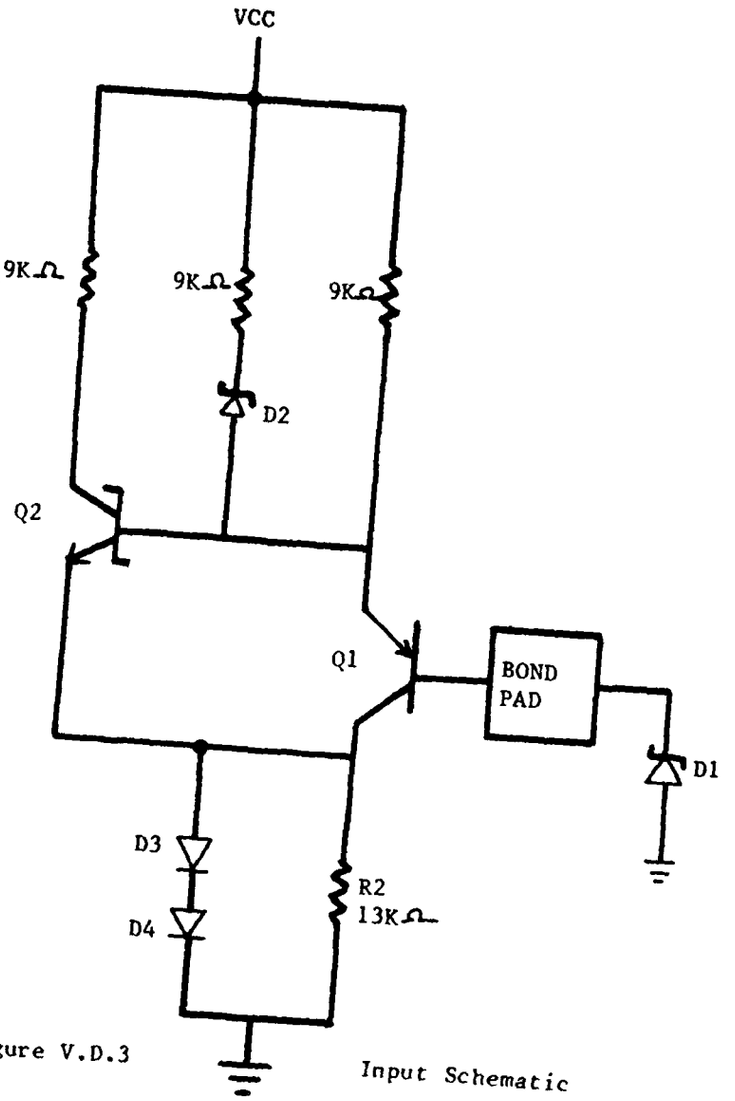


Figure V.D.3 Input Schematic

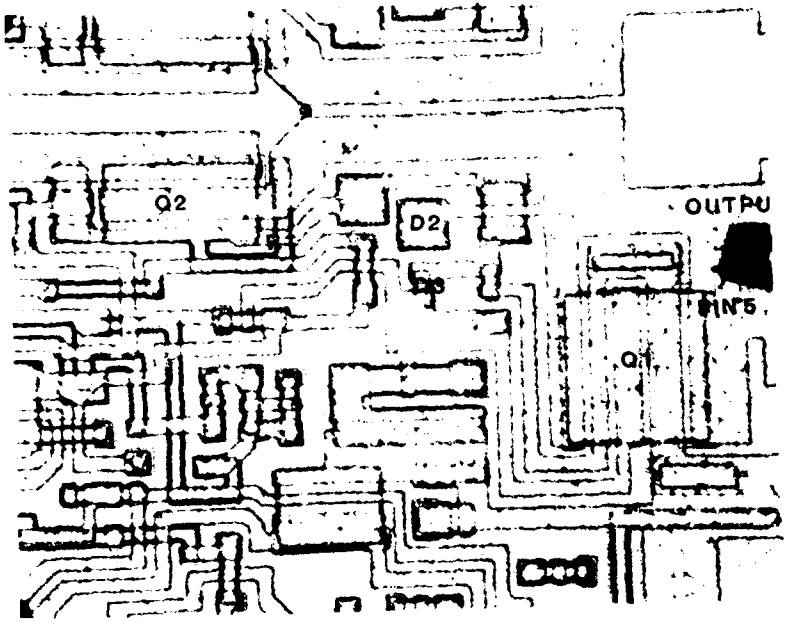


Figure V.D.4 - Pin 5 Output

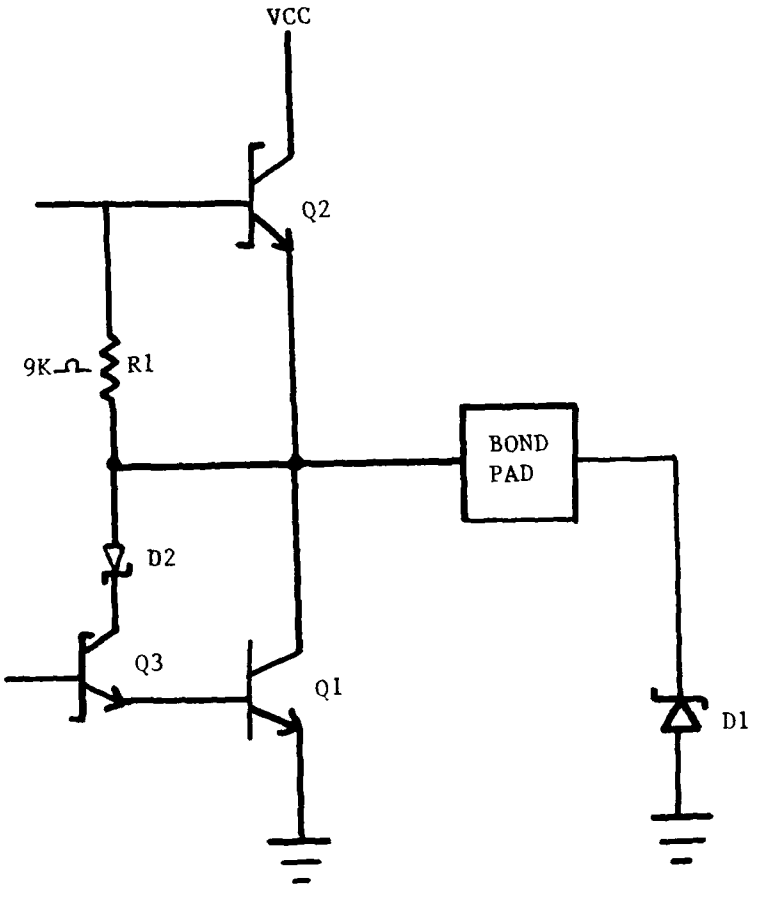


Figure V.D.5 - Output Schematic

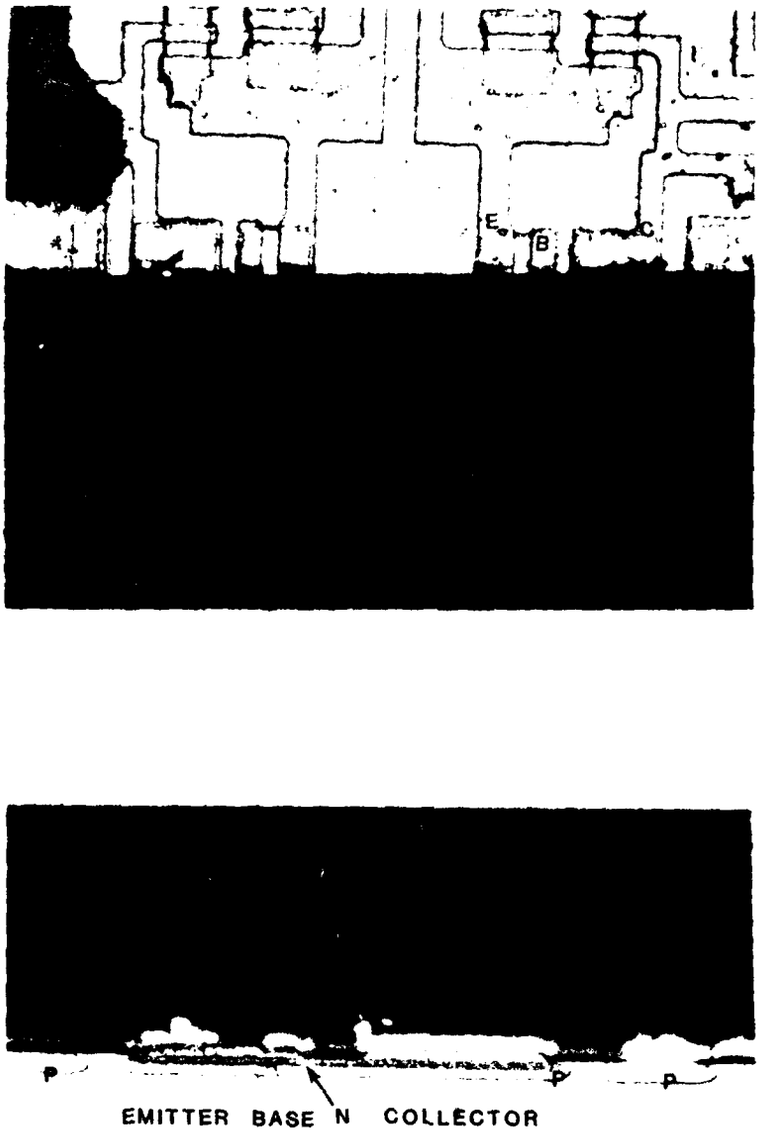
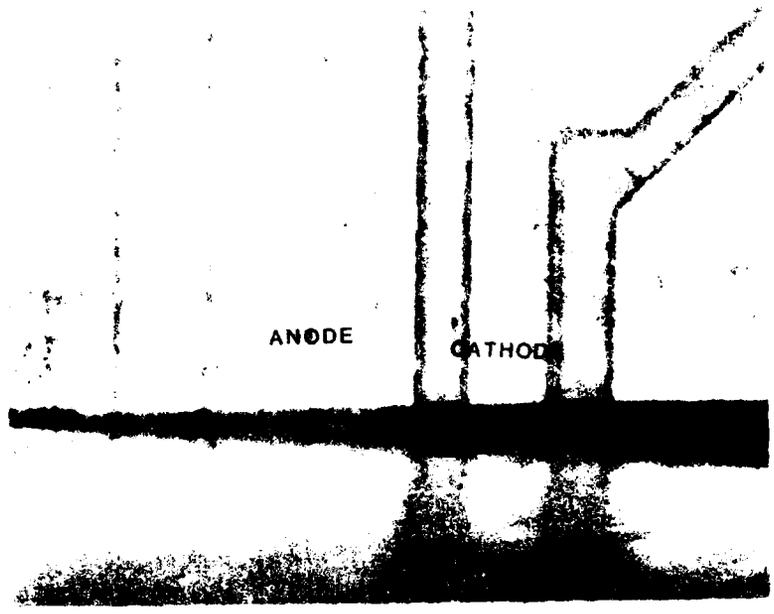


Figure V.D.6 - Input Transistor



ANODE CATHODE

Figure V.D.7 - Input Diode Top View and Side View

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :146 SERIAL NUMBER - 11
TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 04 AUG 83 AT 15:36:27 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	ICC	- - - - - -	30.10MA	--	55.00MA
	VCD	- - - - - -	-705.0MV	-1.200 V	--
	VCD	- - - - - -	-705.0MV	-1.200 V	--
	VCD	- - - - - -	-705.0MV	-1.200 V	--
	VCD	- - - - - -	-705.0MV	-1.200 V	--
	VCD	- - - - - -	-705.0MV	-1.200 V	--
	VCD	- - - - - -	-700.0MV	-1.200 V	--
	VCD	- - - - - -	-700.0MV	-1.200 V	--
	VCD	- - - - - -	-700.0MV	-1.200 V	--
	VCD	- - - - - -	-720.0MV	-1.200 V	--
	VCD	- - - - - -	-710.0MV	-1.200 V	--
	VOH	- - - - - -	3.160 V	2.700 V	--
	VOH	- - - - - -	3.165 V	2.700 V	--
	VOH	- - - - - -	3.160 V	2.700 V	--
	VOH	- - - - - -	3.155 V	2.700 V	--
	VOH	- - - - - -	3.160 V	2.700 V	--
	VOH	- - - - - -	3.165 V	2.700 V	--
	VOH	- - - - - -	3.160 V	2.700 V	--
	VOH	- - - - - -	3.155 V	2.700 V	--
	VOL	- - - - - -	353.5MV	--	500.0MV
	VOL	- - - - - -	349.0MV	--	500.0MV
	VOL	- - - - - -	349.0MV	--	500.0MV
	VOL	- - - - - -	351.0MV	--	500.0MV
	VOL	- - - - - -	353.0MV	--	500.0MV
	VOL	- - - - - -	349.5MV	--	500.0MV
	VOL	- - - - - -	351.5MV	--	500.0MV
	VOL	- - - - - -	359.0MV	--	500.0MV
	IIH	- - - - - -	450.0PA	--	20.00UA
	IIH	- - - - - -	500.0PA	--	20.00UA
	IIH	- - - - - -	700.0PA	--	20.00UA
	IIH	- - - - - -	-200.0PA	--	20.00UA
	IIH	- - - - - -	950.0PA	--	20.00UA
	IIH	- - - - - -	700.0PA	--	20.00UA
	IIH	- - - - - -	500.0PA	--	20.00UA
	IIH	- - - - - -	250.0PA	--	20.00UA
	IIH	- - - - - -	300.0PA	--	20.00UA
	IIH	- - - - - -	600.0PA	--	20.00UA
	IIL	- - - - - -	-356.5UA	-600.0UA	--
	IIL	- - - - - -	-351.5UA	-600.0UA	--
	IIL	- - - - - -	-353.0UA	-600.0UA	--
	IIL	- - - - - -	-351.0UA	-600.0UA	--
	IIL	- - - - - -	-357.5UA	-600.0UA	--
	IIL	- - - - - -	-360.5UA	-600.0UA	--
	IIL	- - - - - -	-358.0UA	-600.0UA	--

Figure V.D.8 - Initial Electrical Data

FILE UID :146 SERIAL NUMBER - 11

TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 04 AUG 83 AT 15:36:57 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IIL	- - - - - - -	-360.5UA	-600.0UA	--
	IIL	- - - - - - -	-352.5UA	-600.0UA	--
	IIL	- - - - - - -	-370.0UA	-600.0UA	--
	IOZH	- - - - - - -	4.700NA	--	50.00UA
	IOZH	- - - - - - -	3.000NA	--	50.00UA
	IOZH	- - - - - - -	3.200NA	--	50.00UA
	IOZH	- - - - - - -	127.0NA	--	50.00UA
	IOZH	- - - - - - -	4.600NA	--	50.00UA
	IOZH	- - - - - - -	178.0NA	--	50.00UA
	IOZH	- - - - - - -	312.0NA	--	50.00UA
	IOZH	- - - - - - -	601.0NA	--	50.00UA
	IOZL	- - - - - - -	1.300NA	-50.00UA	--
	IOZL	- - - - - - -	1.100NA	-50.00UA	--
	IOZL	- - - - - - -	700.0PA	-50.00UA	--
	IOZL	- - - - - - -	3.450NA	-50.00UA	--
	IOZL	- - - - - - -	2.600NA	-50.00UA	--
	IOZL	- - - - - - -	2.950NA	-50.00UA	--
	IOZL	- - - - - - -	3.000NA	-50.00UA	--
	IOZL	- - - - - - -	37.75NA	-50.00UA	--
	IOS	- - - - - - -	-68.00MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.50MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.50MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.00MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.00MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-72.00MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.50MA	-150.0MA	-60.00MA
	IOS	- - - - - - -	-71.00MA	-150.0MA	-60.00MA

TEST RUNTIME IS 21 SECONDS
PRINT / DISPLAY TIME IS 51 SECONDS

Figure V.D.8 - Initial Electrical Data (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :146 SERIAL NUMBER - 11
TESTED AT 25 DEG. C N2500V STRESS
ON 15 NOV 83 AT 12:31:09 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	ICC	- - - - - - -	29.60MA	--	55.00MA
	VCD	- - - - - - -	-780.0MV	-1.200 V	--
	VCD	- - - - - - -	-730.0MV	-1.200 V	--
	VCD	- - - - - - -	-780.0MV	-1.200 V	--
	VCD	- - - - - - -	-750.0MV	-1.200 V	--
	VCD	- - - - - - -	-855.0MV	-1.200 V	--
	VCD	- - - - - - -	-830.0MV	-1.200 V	--
	VCD	- - - - - - -	-755.0MV	-1.200 V	--
	VCD	- - - - - - -	-730.0MV	-1.200 V	--
	VCD	- - - - - - -	-725.0MV	-1.200 V	--
	VCD	- - - - - - -	-955.0MV	-1.200 V	--
	VOH	- - - - - - -	3.110 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.105 V	2.700 V	--
	VOH	- - - - - - -	3.110 V	2.700 V	--
	VOL	- - - - - - -	386.5MV	--	500.0MV
	VOL	- - - - - - -	381.5MV	--	500.0MV
	VOL	- - - - - - -	382.0MV	--	500.0MV
	VOL	- - - - - - -	383.5MV	--	500.0MV
	VOL	- - - - - - -	380.0MV	--	500.0MV
	VOL	- - - - - - -	376.5MV	--	500.0MV
	VOL	- - - - - - -	377.0MV	--	500.0MV
	VOL	- - - - - - -	400.0MV	--	500.0MV
****	IIH	- - - - - - -	103.0UA	--	20.00UA
	IIH	- - - - - - -	2.450NA	--	20.00UA
	IIH	- - - - - - -	336.5NA	--	20.00UA
	IIH	- - - - - - -	5.200NA	--	20.00UA
	IIH	- - - - - - -	128.5NA	--	20.00UA
	IIH	- - - - - - -	300.0PA	--	20.00UA
	IIH	- - - - - - -	27.35NA	--	20.00UA
****	IIH	- - - - - - -	122.0UA	--	20.00UA
****	IIH	- - - - - - -	77.95UA	--	20.00UA
****	IIH	- - - - - - -	229.5UA	--	20.00UA
	IIL	- - - - - - -	-355.0UA	-600.0UA	--
	IIL	- - - - - - -	-345.0UA	-600.0UA	--
	IIL	- - - - - - -	-346.5UA	-600.0UA	--
	IIL	- - - - - - -	-344.5UA	-600.0UA	--
	IIL	- - - - - - -	-350.5UA	-600.0UA	--
	IIL	- - - - - - -	-354.0UA	-600.0UA	--
	IIL	- - - - - - -	-351.0UA	-600.0UA	--

Figure V.D.9 - Post -2500 Volt Electrical Data

FILE UID :146 SERIAL NUMBER - 11

TESTED AT 25 DEG. C N2500V STRESS
ON 15 NOV 83 AT 12:31:38 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IIL	-359.0UA	-600.0UA	--
	IIL	-353.0UA	-600.0UA	--
	IIL	-375.5UA	-600.0UA	--
	IOZH	3.400NA	--	50.00UA
	IOZH	2.200NA	--	50.00UA
	IOZH	1.800NA	--	50.00UA
	IOZH	108.5NA	--	50.00UA
	IOZH	2.600NA	--	50.00UA
	IOZH	154.5NA	--	50.00UA
	IOZH	263.0NA	--	50.00UA
	IOZH	528.5NA	--	50.00UA
	IOZL	350.0PA	-50.00UA	--
	IOZL	800.0PA	-50.00UA	--
	IOZL	1.200NA	-50.00UA	--
	IOZL	2.400NA	-50.00UA	--
	IOZL	1.200NA	-50.00UA	--
	IOZL	1.700NA	-50.00UA	--
	IOZL	2.500NA	-50.00UA	--
	IOZL	30.80NA	-50.00UA	--
	IOS	-60.00MA	-150.0MA	-60.00MA
	IOS	-63.50MA	-150.0MA	-60.00MA
	IOS	-64.00MA	-150.0MA	-60.00MA
	IOS	-63.00MA	-150.0MA	-60.00MA
	IOS	-65.00MA	-150.0MA	-60.00MA
	IOS	-65.00MA	-150.0MA	-60.00MA
	IOS	-65.50MA	-150.0MA	-60.00MA
	IOS	-63.50MA	-150.0MA	-60.00MA

TEST RUNTIME IS 20 SECONDS
PRINT / DISPLAY TIME IS 51 SECONDS

Figure V.D.9 - Post -2500 Volt Electrical Data (Cont.)

Number of Failures at Pin Locations											
1	3	4	7	8	11	13	14	17	18	Cumulative # Removed	Voltage
					1						-750
					1						+1000
10	2		1	1	10	2	1	1	3	2	-1000
12	2		1	1	13	2	1	1	4	2	+1250
14	9	9	9	10	14	8	9	6	9	10	-1250
14	10	10	9	10	14	9	11	8	10	14	+1500

Figure V.D.10 - CD Stress, Cumulative Leakage Failures (14 parts total)

INITIAL	+750 V	-750 V	+1000 V	-1000 V
450 pA	400 pA	11.8 uA	7.6 uA	50.5 uA

Figure V.D.11 - CD Stress, Serial Number 26 Pin 1 Leakage Current

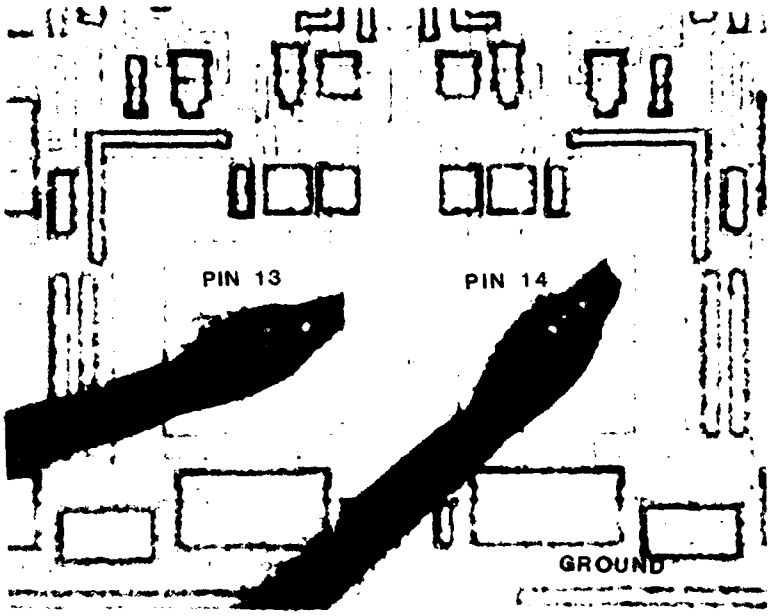


Figure V.D.12 - Input Pins 13 and 14

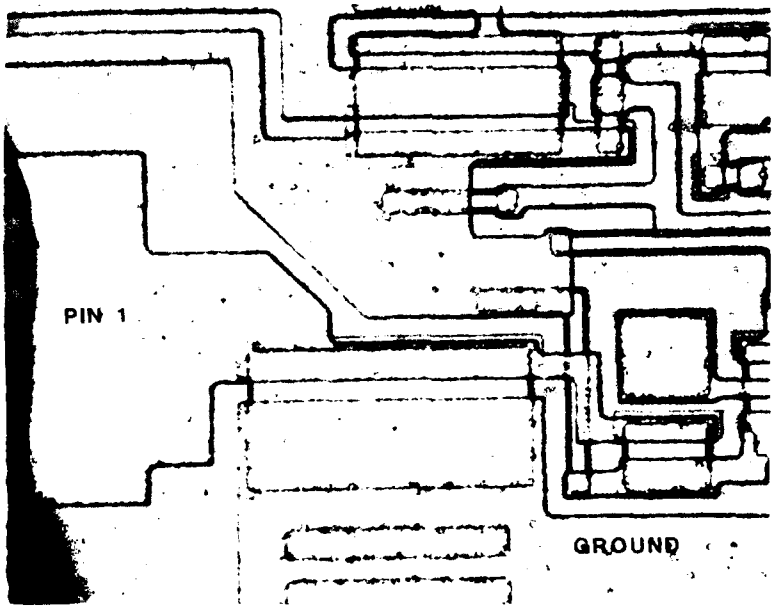


Figure V.D.13 - Input Pin 1

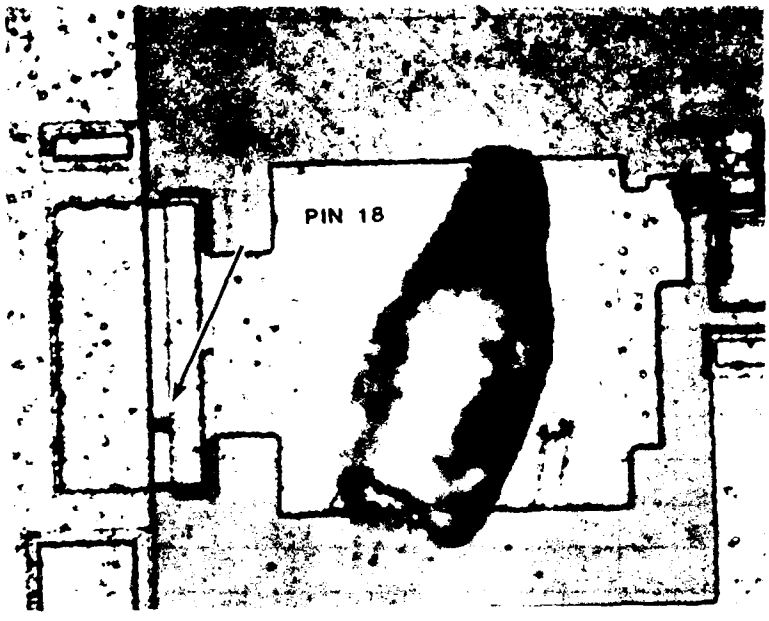


Figure V.D.14 - CD Stress, Input Pin 18 Damage Site

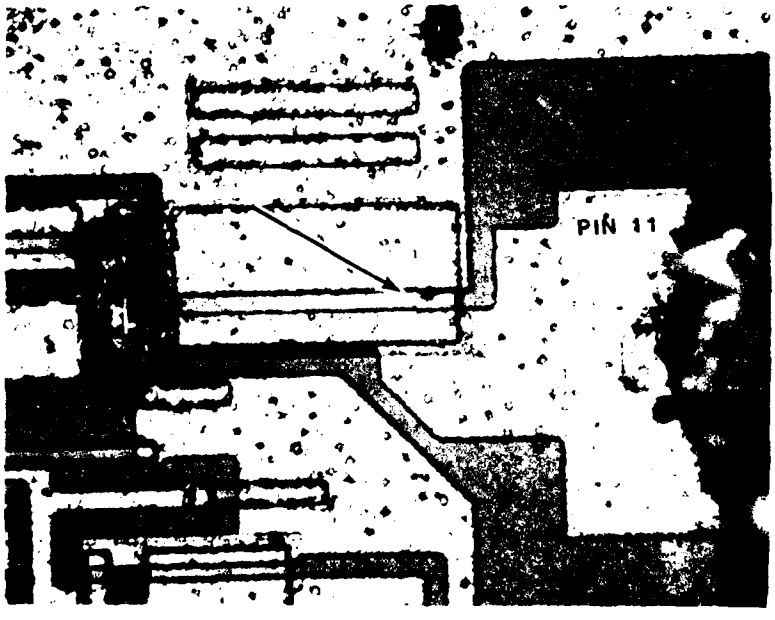


Figure V.D.15 - CD Stress, Input Pin 11 Damage Site

Number of Failures at Pin Locations											
1	3	4	7	8	11	13	14	17	18	Cumulative # Removed	Voltage
1	1	2	1		1	1		1	2		+500
											-500
3				1	2		2	3		2	+750
											-750
											+1000
											-1000
						2					+1250
											-1250
9					3						+1500
											-1500
12	2	3	2		5			4			+1750
					6						-1750
	3			2	10		3		4		+2000
		4									-2000
12	5	5	2	3	11	2	4		8	4	+2250
											-2250
	9	7	4				7	5	11	8	+2500
											-2500
12	10	8	5	5	11	3	8	6	11	12	+2750

Figure V.D.16 - HBD Stress, Cumulative Leakage Failures (12 parts total)

Initial	-1250 volts	+1500 volts
600 pA	300 pA	63.2 u A

Figure V.D.17 - HBD Stress, Serial Number 3 Pin 1 Leakage Current

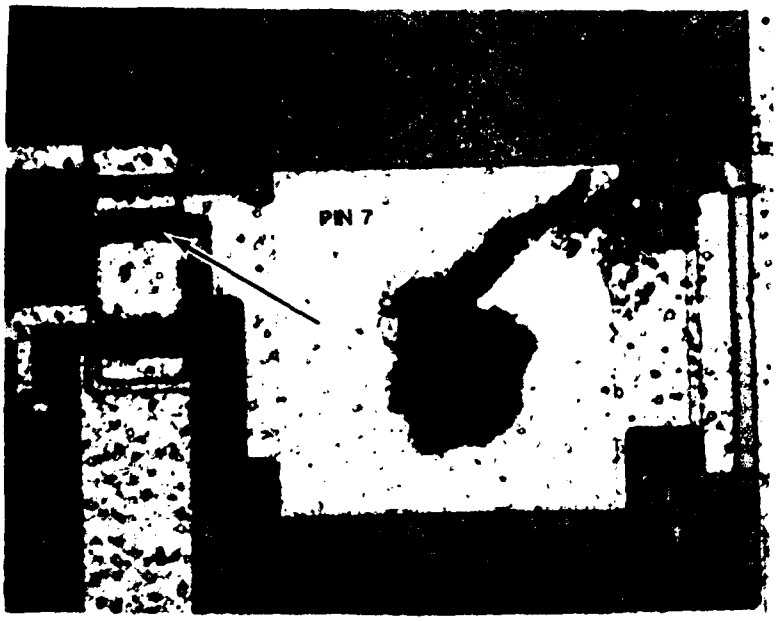


Figure V.D.18 - HBD Stress, Input Pin 7 Damage Site

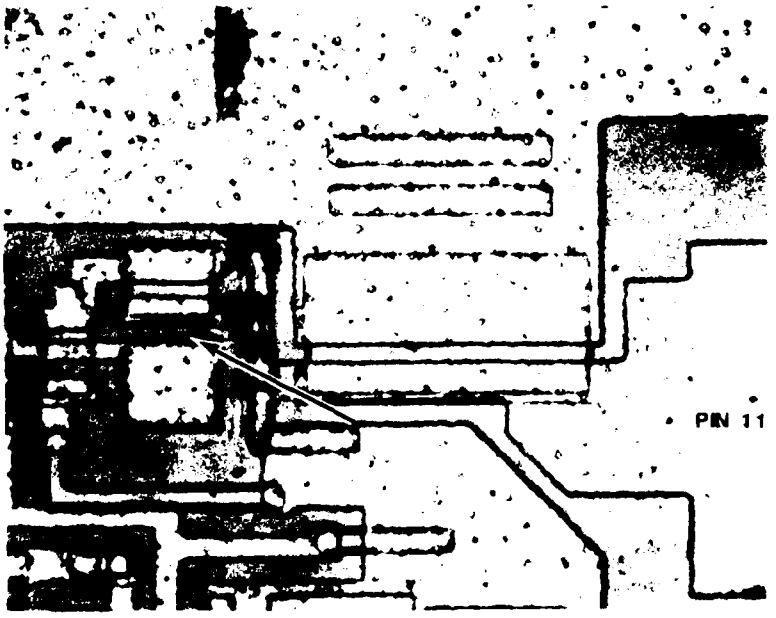


Figure V.D.19 - HBD Stress, Input Pin 11 Damage Site

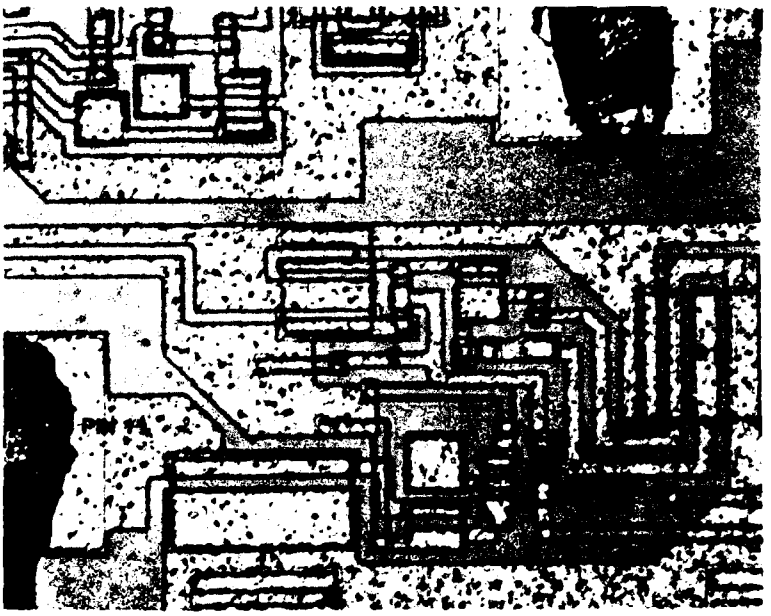


Figure V.D.20 - Pin 11 Layout

E. Part E Analysis

This device is a RAM-I/O-Timer manufactured using an n-channel, depletion load, silicon gate (HMOS) technology. There is a 2048-bit static RAM, 2 programmable 8-bit I/O ports, 1 programmable 6 bit I/O port, and a 14-bit timer. There is one metallization layer and one polysilicon layer. Both conductors are approximately 3.5 microns in width.

An overall die photograph is shown in Figure V.E.1. VCC, pin 40, is at the top of the figure. On its left is a bond pad that is only connected to the substrate. VSS, pin 20, is at the bottom of the figure. The distribution pattern is basically an interdigitated structure. The VSS metallization has two parallel stripes that are approximately 8 microns apart near the outer edge. The reason for the separation may be that the wider outside stripe carries the majority of the current flow and the inside stripe is a solid ground reference for the internal circuitry.

The VCC metallization is shown in Figure V.E.2. This contacts n+ source diffusions. The VSS metallization is shown in Figure V.E.3. The two parallel metallization stripes are visible. This metallization also contacts n+ source diffusions.

The substrate connection is shown in Figure V.E.4.

A typical input is shown in Figure V.E.5 with the corresponding schematic in Figure V.E.6. The input layouts were identical on the different pins. The input metallization overlays the input resistor and acts as a gated diode. Dielectric breakdown on the gates was 100 VDC. The input resistor is a diffused resistor. The breakdown voltage from it to the substrate was 28 VDC. This is the same as the transistor junction breakdown.

An output is shown in Figure V.E.7 and the corresponding schematic is shown in Figure V.E.8. This is pin 6 which is the only output on this device that is not an input/output combination.

An input/output combination is shown in Figure V.E.9 and the corresponding schematic is shown in Figure V.E.10. The input section is identical to the other inputs and the output layout is the same as the outputs on the other I/O pins.

Microsections were performed to examine the construction of this device. Very shallow diffusions were used. An input resistor diffusion is shown in Figure V.E.11. The edge of the bond pad is on the right hand side of the photograph and the metallization which interconnects the bond pad and the resistor is above the diffusion. This diffusion is 0.4 microns deep and the metallization is 1.2 microns thick. A transistor structure is shown in Figure V.E.12. The polysilicon gate is 0.4 microns thick. The edge of the die is shown in Figure V.E.13. There is an n diffusion which is about 2 microns deep which travels around the perimeter of the die and

is contacted by metallization on its inside edge. The oxide thickness between the polysilicon and the metallization is 1.2 microns and the thickness between the polysilicon and the silicon is 0.9 microns.

Electrical Testing

A sample of the electrical data taken on each of the stressed parts and the control part at each iteration during the testing is shown in Figures V.E.14 and V.E.15. V_{OH} and V_{OL} were measured on the output pin and on each of the 30 input/output pins. Current leakage was measured at +5 volts and 0 volts on all pins except the timer output, VCC and VSS. This measurement provided interface circuit damage information. This testing also provided a functional check of the following. The control logic (IO/M, CE, ALE, RD, WR, and RESET), the three ports and associated data direction registers, the timer, and the address/data buffers and latches were tested for operation in their various modes. One 8 bit wide section of the 256 section RAM was accessed.

Charged Device Data Analysis

Fourteen devices, serial numbers 15 through 28 were stressed with the charged device ESD stress simulation. The principle failure mode experienced was input circuit leakage. A summary of the inputs and the point at which they developed leakage current is shown in Figure V.E.16. The inputs are seen to degrade with positive stress. The order of sensistivity is: 4, 7, 9, and 10 most sensitive 3 and 11 less sensitive, and pin 8 least sensitive.

Numerous V_{OH} and V_{OL} failures occurred, however, this was due to the input damage. In addition to the input becoming inoperative because of the junction damage the substrate bias generator would not be able to keep the part properly biased with the additional current load put on it through the inputs.

Three devices exhibited leakage on pins other than the inputs. Serial numbers 17 and 25 had leakage on output pin 6 and serial number 21 had leakage on output pin 6 and I/O pin 2.

The layouts are as shown in Figure V.E.17 through V.E.23. Pin 2 in Figure V.E.17 is an input/output and pin 3 is an input only. Input pins 3 and 4 are shown in Figure V.E.18. Figure V.E.19 shows input/output pin 5 and output pin 6. Figures V.E.20 through V.E.22 show input pins and Figure V.E.23 shows input pin 11 and input/output pin 12.

Curve tracer measurements were performed on all devices. Input leakages were noted on pins 3, 4, 7, 8, 9, 10, and 11 on most devices. Pin 6 was leaky on serial numbers 17, 21, and 25. Pin 2 was leaky on serial number 21.

Internal visual examination was performed on all of the devices. No damage was visible on the input/output pins which did not exhibit leakage. Damage was seen on numerous pins and this is documented on two parts, serial numbers 20 and 21. Serial number 21 had leakage on pins 2 and 6 in addition to the inputs.

Failure appearance on serial number 20 is documented in Figures V.E.24 and V.E.25. This is pins 7, 8, and 9. The current path is from the n-type resistor to the n-type diffusion around the perimeter of the die. This latter diffusion is not connected to any other point so the current flows from it back to a grounded pin.

The failures on pins 7 and 8 on serial number 21 are shown in Figure V.E.26. The failure on pin 2 (input/output) is different than the failures on the inputs (Figure V.E.27). The breakdown sites which indicate the direction of the current are on the edge of the resistor contact closest to pin 3. The distance from the edge of the pin 2 resistor diffusion to the edge of the pin 3 resistor diffusion is 26 microns. This is shorter than the distance to the edge of the die (32 microns). The damage created indicates that a stress occurred between pins 2 and 3. Numerous pairs of input/output pins had this same spacing between resistors (26 microns) but they were not damaged. This indicates that the damage on pin 2 was not the result of a stress originating at pin 2 but rather was the result of an opposite polarity pulse originating at pin 3. The close spacing to the adjacent pin resulted in the stress occurring between these points rather than to the edge of the die.

The failure on pin 6 produced a visible breakdown site (Figure V.E.28). This site was verified by mechanically isolating the other two contact points and probing each. The only one that was leaky was the one shown. This was drain to body leakage.

With an understanding of the physical layouts and an understanding of the failure modes, the sensitivity variations can be analyzed.

Pin 8 is less sensitive to stress than the other inputs because it is connected to an additional diffusion. This makes its sensitivity less than the other inputs but more than the outputs which have more than one diffusion contact.

Pins 3 and 11 were the next most sensitive and they have in common the fact that they are paired with an input/output pin (Figures V.E.17 and V.E.23) and they are the last input pin either direction around the die. Since current flow occurs out to the edge of the die and then back through a grounded circuit, the pins on the end would tend to receive less stress. The ones in the middle would be stressed when pins on either side of them receive a stress.

For the same reason as stated above the four internal input pins 4, 7, 9, and 10 were the most sensitive during this test. For a single stress event it is likely that the inputs would exhibit a more uniform stress sensitivity.

Due to the lack of a low resistance current path back to the substrate these parts were very resistant to ESD stress.

Human Body Discharge Data Analysis

Thirteen devices, serial numbers 2 through 14 were subjected to the human body discharge ESD simulation. A summary of the input circuit leakage failures with voltage stress is shown in Figure V.E.29. The first leakage failure which occurred was pin 4 on serial number 5 at +2000 volts. Two devices proceeded all of the way through the -5000 volt stress level. One of these was functional and had only slight current leakage.

In addition to the input leakages listed, pins were leaky as shown here: serial number 2 pin 1, and pin 37, serial number 4 pin 13, serial number 5, pin 12 and pin 37, serial number 7, pin 2 and pin 6, serial number 8, pin 12, serial number 9 pin 2 and serial number 14 pin 12. The HBD stress caused failures on more different pins than the CD stress. With the exception of pin 37 these were all physically close to the input pins.

All 13 parts were opened and visually examined. The damage was much less severe than on the CD stressed parts. Very slight damage was visible on a few inputs but stripping was required to enhance the failure sites.

Serial number 2 was analyzed since it had leakage on pins 1 and 37 as well as inputs. The leakage on pins 1 and 37 was low, measuring 10 microamps at 6.5 volts on pin 1 and 10 microamps at 9.5 volts on pin 37. There was no visible damage on these two pins. Pins which did exhibit damage are shown in Figures V.E.30 through V.E.33. Figure V.E.30 shows input/output pin 2 and input pin 3. Figure V.E.31 shows input pin 4. Figure V.E.32 shows input pins 7 and 8. Figure V.E.33 shows input pin 11 and input/output pin 12.

Input/output pins 2 and 12 were the only two I/O pins which exhibited visible damage. They both had leakage currents of 1 microamp at 10 volts. The input pins generally had damage on the side of the resistor closest to the edge of the die. There is also visible damage along the edge of the n-diffusion on the perimeter of the die.

There was very little difference in sensitivity between pins like was seen on the CD stressed parts. The susceptibility to damage was low on these parts with the inputs being more sensitive to stress than outputs or I/O combinations. This part is designed very well for ESD tolerance due to the absence of a current path from the inputs through the substrate back to an external ground.

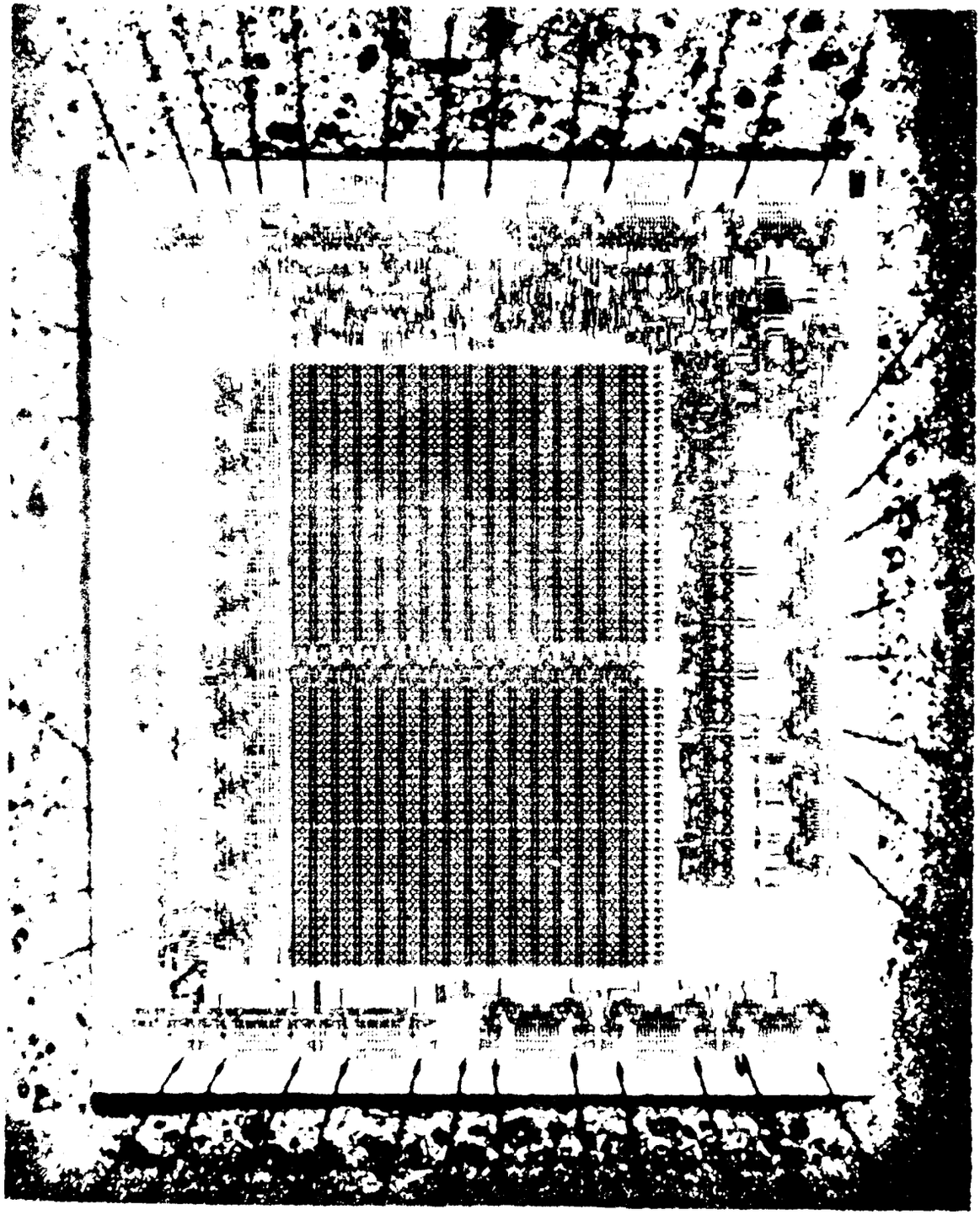


Figure V-5.1 - Overall Die Photograph

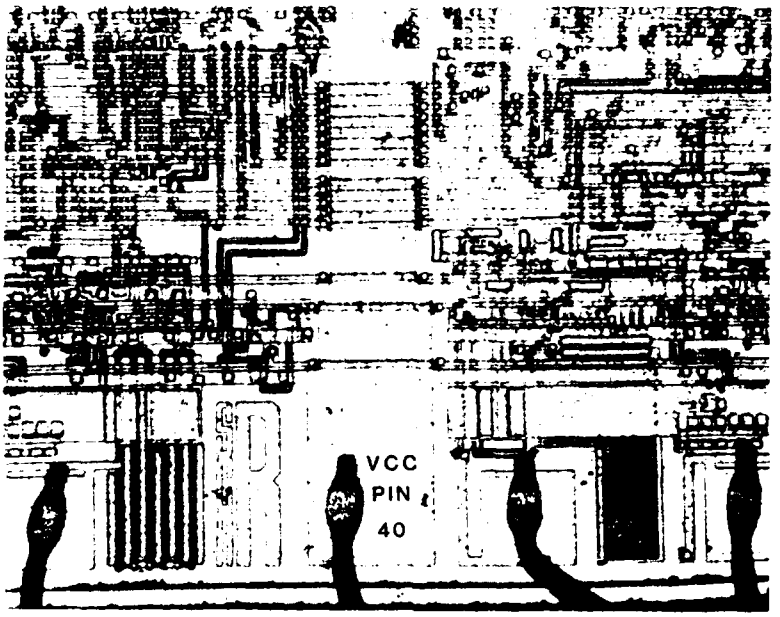


Figure V.E.2 - VCC Bond Pad

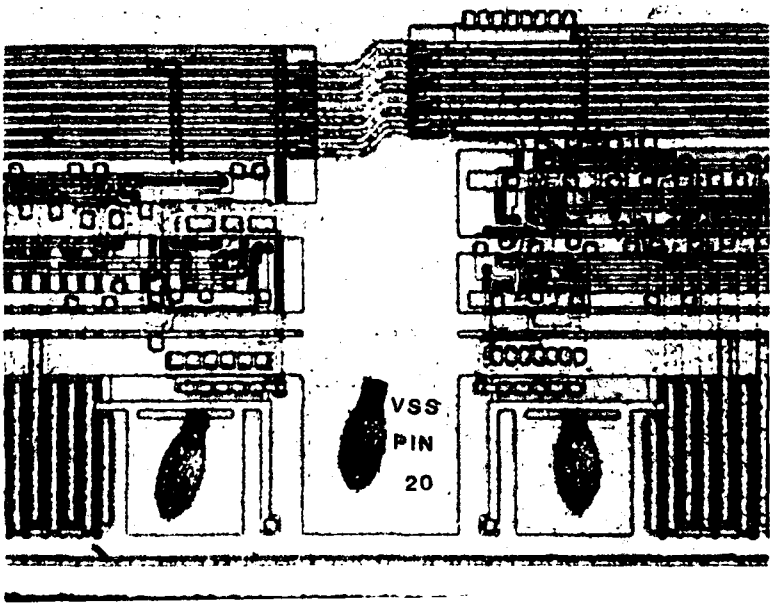


Figure V.E.3 - VSS Bond Pad

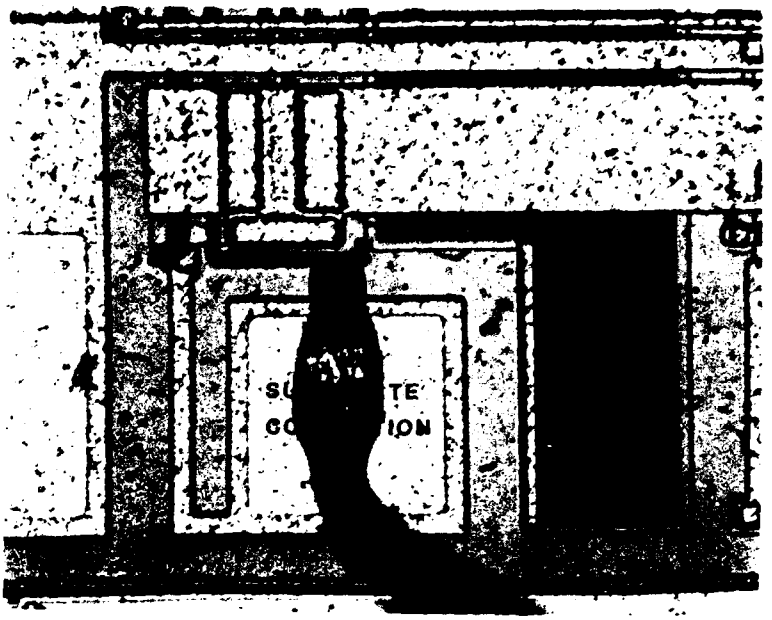


Figure V.E.4 - Substrate Connection

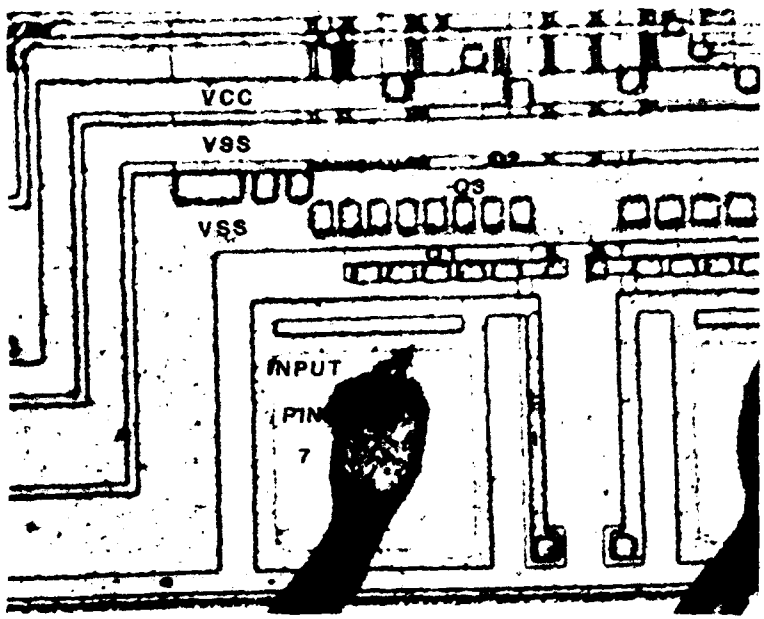


Figure V.E.5 - Pin 7 Input

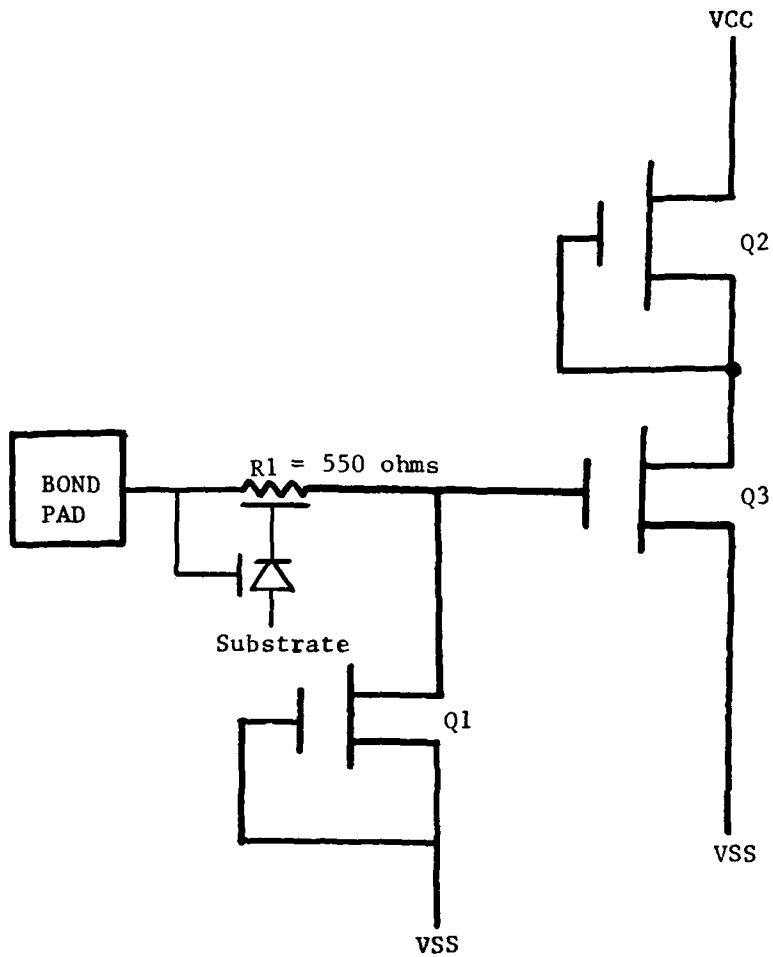


Figure V.E.6 - Input Schematic

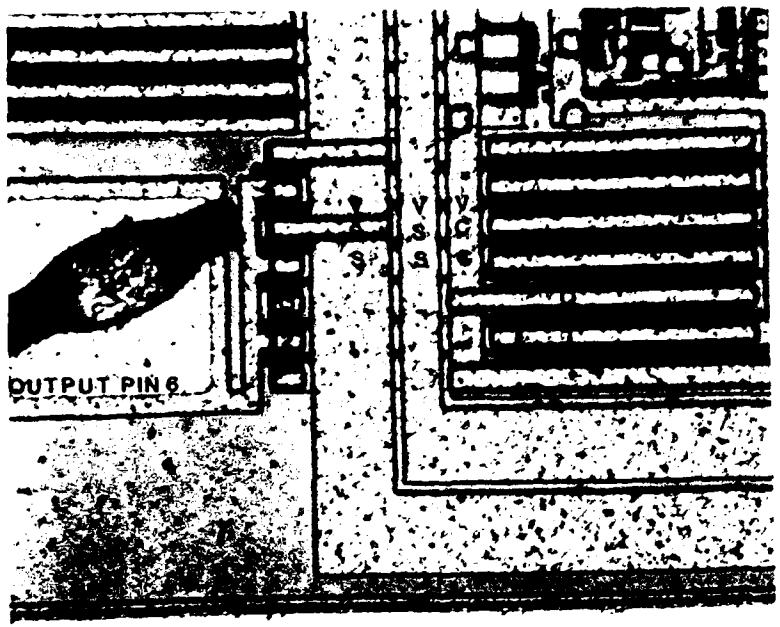


Figure V.E.7 - Pin 6 Output

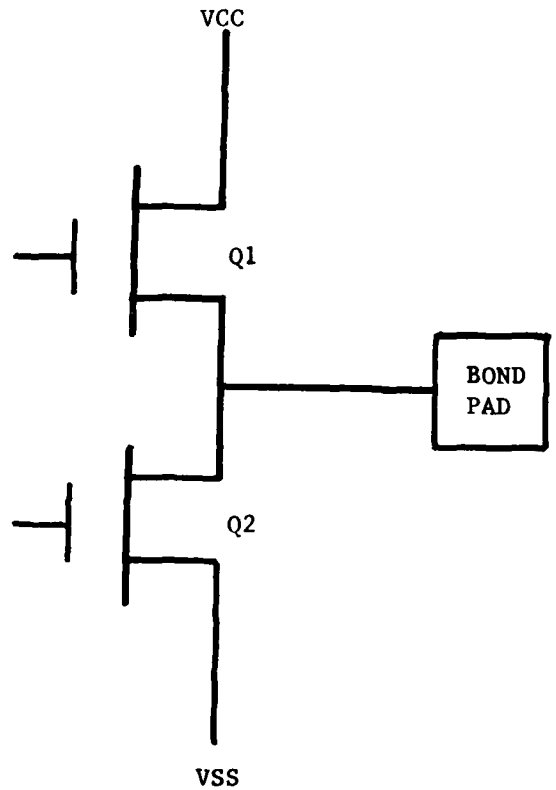


Figure V.E.8 - Output Schematic

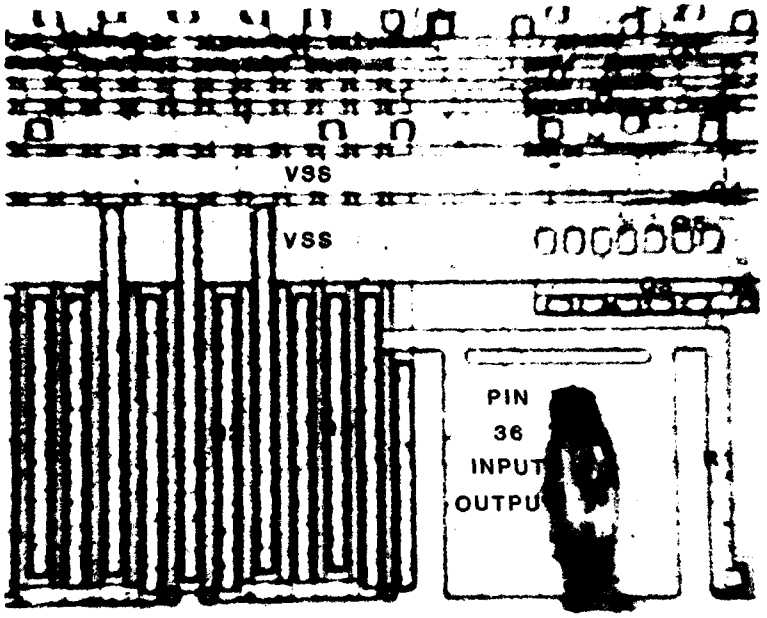


Figure V.E.9 - Pin 36 Input/Output

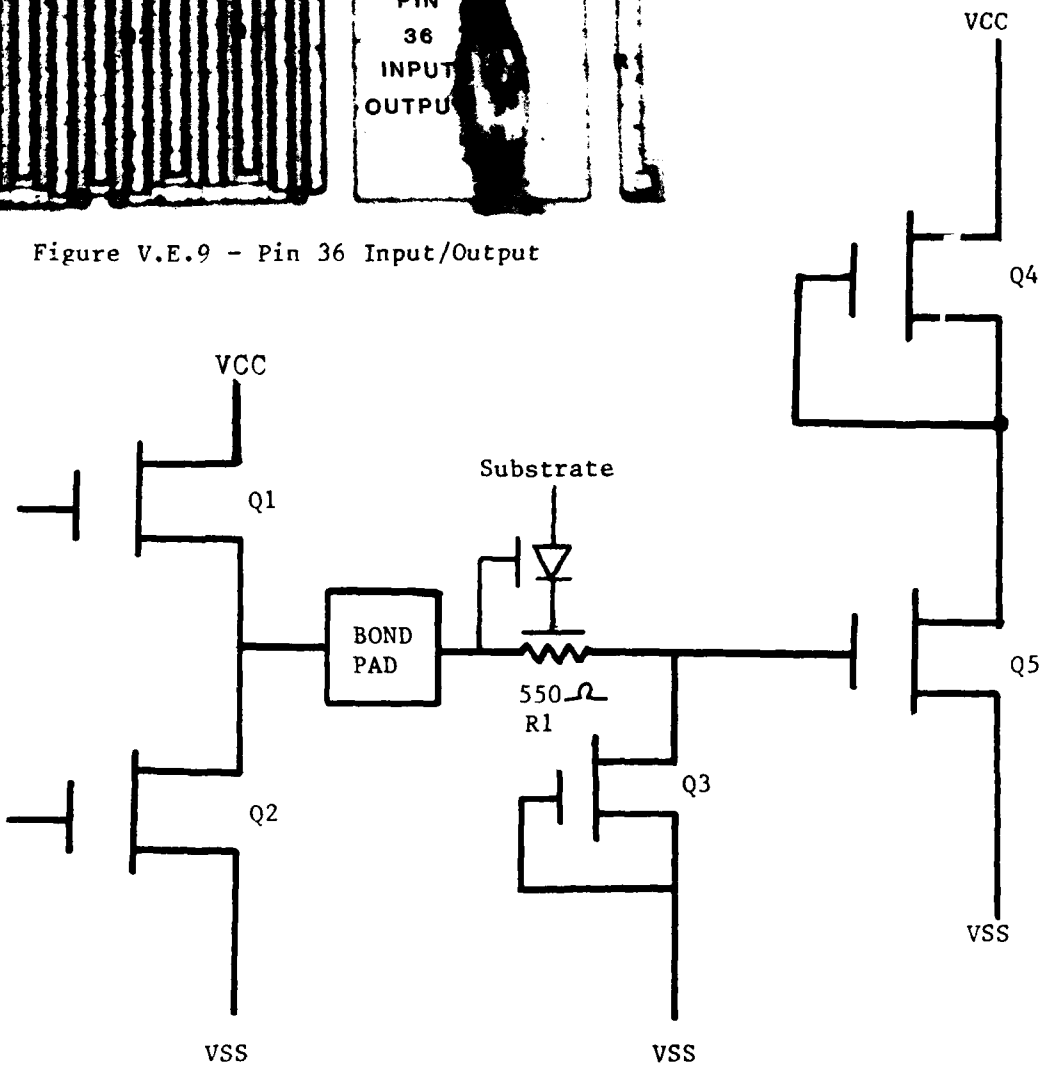


Figure V.E.10 - Input/Output Schematic

Figure V.E.11 - Input Resistor Diffusion Side View

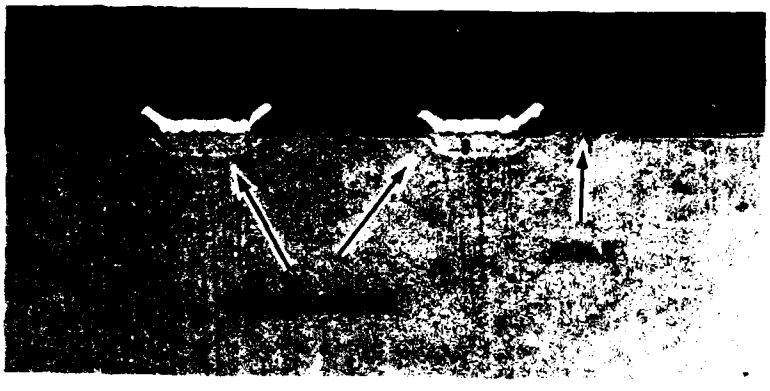


Figure V.E.12 - Transistor Cross-Section

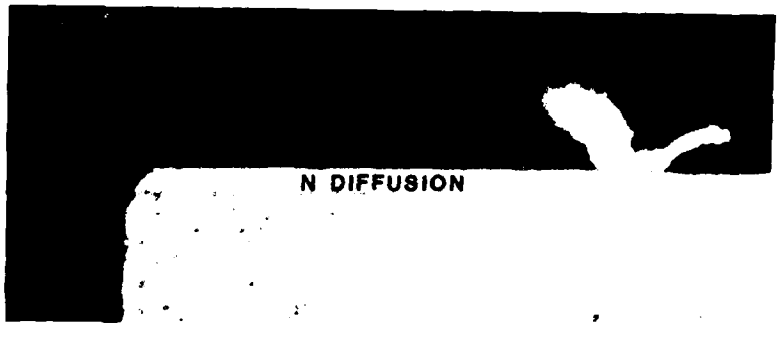


Figure V.E.13 - Side View of Edge of Die

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

PART NUMBER - FILE UID : SERIAL NUMBER - 9
TESTED AT 25 DEG. C

ON 03 AUG 83 AT 14:10 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	VOH	- - - - - -	2.910 V	2.400 V	--
	VOH	- - - - - -	2.890 V	2.400 V	--
	VOH	- - - - - -	2.895 V	2.400 V	--
	VOH	- - - - - -	2.905 V	2.400 V	--
	VOH	- - - - - -	2.900 V	2.400 V	--
	VOH	- - - - - -	2.905 V	2.400 V	--
	VOH	- - - - - -	2.875 V	2.400 V	--
	VOH	- - - - - -	2.890 V	2.400 V	--
	VOH	- - - - - -	2.920 V	2.400 V	--
	VOH	- - - - - -	2.890 V	2.400 V	--
	VOH	- - - - - -	2.920 V	2.400 V	--
	VOH	- - - - - -	2.915 V	2.400 V	--
	VOH	- - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - -	2.920 V	2.400 V	--
	VOH	- - - - - -	2.900 V	2.400 V	--
	VOH	- - - - - -	2.910 V	2.400 V	--
	VOH	- - - - - -	2.905 V	2.400 V	--
	VOH	- - - - - -	2.905 V	2.400 V	--
	VOH	- - - - - -	2.895 V	2.400 V	--
	VOH	- - - - - -	2.900 V	2.400 V	--
	VOH	- - - - - -	2.895 V	2.400 V	--
	VOH	- - - - - -	2.900 V	2.400 V	--
	VOH	- - - - - -	2.950 V	2.400 V	--
	VOH	- - - - - -	2.955 V	2.400 V	--
	VOH	- - - - - -	2.950 V	2.400 V	--
	VOH	- - - - - -	2.945 V	2.400 V	--
	VOH	- - - - - -	2.955 V	2.400 V	--
	VOH	- - - - - -	2.960 V	2.400 V	--
	VOH	- - - - - -	2.955 V	2.400 V	--
	VOH	- - - - - -	2.970 V	2.400 V	--
	VOH	- - - - - -	2.935 V	2.400 V	--
	VOL	- - - - - -	166.5MV	--	450.0MV
	VOL	- - - - - -	167.0MV	--	450.0MV
	VOL	- - - - - -	175.5MV	--	450.0MV
	VOL	- - - - - -	159.5MV	--	450.0MV
	VOL	- - - - - -	161.5MV	--	450.0MV
	VOL	- - - - - -	160.0MV	--	450.0MV
	VOL	- - - - - -	164.5MV	--	450.0MV
	VOL	- - - - - -	162.0MV	--	450.0MV
	VOL	- - - - - -	160.0MV	--	450.0MV
	VOL	- - - - - -	162.0MV	--	450.0MV
	VOL	- - - - - -	159.5MV	--	450.0MV
	VOL	- - - - - -	160.0MV	--	450.0MV
	VOL	- - - - - -	157.5MV	--	450.0MV
	VOL	- - - - - -	157.5MV	--	450.0MV
	VOL	- - - - - -	167.5MV	--	450.0MV
	VOL	- - - - - -	167.0MV	--	450.0MV
	VOL	- - - - - -	167.5MV	--	450.0MV

Figure V.E.14 - Initial Electrical Measurements

PART NUMBER - FILE UID : SERIAL NUMBER - 9
TESTED AT 25 DEG. C

ON 03 AUG 83 AT 14:10 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	VOL	- - - - - - -	167.0MV	--	450.0MV
	VOL	- - - - - - -	169.5MV	--	450.0MV
	VOL	- - - - - - -	169.5MV	--	450.0MV
	VOL	- - - - - - -	171.0MV	--	450.0MV
	VOL	- - - - - - -	170.0MV	--	450.0MV
	VOL	- - - - - - -	161.5MV	--	450.0MV
	VOL	- - - - - - -	161.0MV	--	450.0MV
	VOL	- - - - - - -	179.5MV	--	450.0MV
	VOL	- - - - - - -	182.5MV	--	450.0MV
	VOL	- - - - - - -	180.5MV	--	450.0MV
	VOL	- - - - - - -	187.0MV	--	450.0MV
	VOL	- - - - - - -	183.5MV	--	450.0MV
	VOL	- - - - - - -	171.0MV	--	450.0MV
	VOL	- - - - - - -	270.0MV	--	450.0MV
	IIL	- - - - - - -	2.900NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.350NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.950NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-700.0PA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.800NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.400NA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.500NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.150NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.550NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.100NA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.350NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.450NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.800NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-900.0PA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.250NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.550NA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.200NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-750.0PA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.500NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.550NA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.200NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.000NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.300NA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.500NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.300NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.550NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.450NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.700NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.650NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	2.600NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.550NA	-10.00UA	10.00UA

Figure V.E.14 - Initial Electrical Measurements (Cont.)

PART NUMBER - FILE ID SERIAL NUMBER -
TESTED AT 25 DEG C

ON 05 AUG 83 AT 14 10 WITH THE 3250 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	IIL	- - - - - -	2.700NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.500NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.500NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.400NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.600NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.400NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.750NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.400NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.300NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.250NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.350NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.200NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.600NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.200NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.350NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.150NA	-10.00UA	10.00UA
	IIL	- - - - - -	2.950NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.250NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.300NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.800NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.050NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.150NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.700NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.350NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.200NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.050NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.350NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.100NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.300NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.000NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.250NA	-10.00UA	10.00UA
	IIL	- - - - - -	-900.0PA	-10.00UA	10.00UA
	IIL	- - - - - -	3.400NA	-10.00UA	10.00UA
	IIL	- - - - - -	-1.000NA	-10.00UA	10.00UA
	IIL	- - - - - -	3.200NA	-10.00UA	10.00UA
	IIL	- - - - - -	-800.0PA	-10.00UA	10.00UA
	IOL	- - - - - -	-600.0PA	-10.00UA	10.00UA
	IOL	- - - - - -	3.550NA	-10.00UA	10.00UA
	IOL	- - - - - -	-1.200NA	-10.00UA	10.00UA
	IOL	- - - - - -	3.400NA	-10.00UA	10.00UA
	IOL	- - - - - -	-1.450NA	-10.00UA	10.00UA
	IOL	- - - - - -	3.350NA	-10.00UA	10.00UA
	IOL	- - - - - -	-1.350NA	-10.00UA	10.00UA
	IOL	- - - - - -	3.200NA	-10.00UA	10.00UA
	IOL	- - - - - -	-1.250NA	-10.00UA	10.00UA
	IOL	- - - - - -	2.900NA	-10.00UA	10.00UA
	IOL	- - - - - -	-1.050NA	-10.00UA	10.00UA
	IOL	- - - - - -	2.700NA	-10.00UA	10.00UA
	IOL	- - - - - -	-750.0PA	-10.00UA	10.00UA
	IOL	- - - - - -	2.100NA	-10.00UA	10.00UA

Figure V.E.14 - Initial Electrical Measurements (Cont.)

PART NUMBER - FILE UID SERIAL NUMBER -
TESTED AT 25 DEG C

ON 03 AUG 83 AT 14 10 WITH THE 3350 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	IOL	- - - - - -	-750.0PA	-10.00UA	10.00UA
	IOL	- - - - - -	2.600NA	-10.00UA	10.00UA
	ICC	- - - - - -	60.60MA	--	180.0MA
	IILCE	- - - - - -	24.20UA	-100.0UA	100.0UA
	IILCE	- - - - - -	-726.5NA	-100.0UA	100.0UA

Figure V.E.14 - Initial Electrical Measurements (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :151 SERIAL NUMBER - 9

TESTED AT 25 DEG. C P5000V STRESS

ON 17 NOV 83 AT 09:06:53 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
****	VOH	- - - - - - -	23.85MV	2.400 V	--
****	VOH	- - - - - - -	21.50MV	2.400 V	--
****	VOH	- - - - - - -	19.70MV	2.400 V	--
****	VOH	- - - - - - -	22.10MV	2.400 V	--
****	VOH	- - - - - - -	20.80MV	2.400 V	--
****	VOH	- - - - - - -	18.30MV	2.400 V	--
****	VOH	- - - - - - -	20.20MV	2.400 V	--
****	VOH	- - - - - - -	22.75MV	2.400 V	--
	VOH	- - - - - - -	2.925 V	2.400 V	-
	VOH	- - - - - - -	2.910 V	2.400 V	--
	VOH	- - - - - - -	2.950 V	2.400 V	--
	VOH	- - - - - - -	2.935 V	2.400 V	--
	VOH	- - - - - - -	2.955 V	2.400 V	--
	VOH	- - - - - - -	2.955 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.915 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.930 V	2.400 V	--
	VOH	- - - - - - -	2.950 V	2.400 V	--
	VOH	- - - - - - -	2.945 V	2.400 V	--
	VOH	- - - - - - -	2.970 V	2.400 V	--
	VOH	- - - - - - -	3.000 V	2.400 V	--
	VOH	- - - - - - -	3.005 V	2.400 V	--
	VOH	- - - - - - -	3.035 V	2.400 V	--
	VOH	- - - - - - -	3.020 V	2.400 V	--
	VOH	- - - - - - -	3.050 V	2.400 V	--
	VOH	- - - - - - -	3.030 V	2.400 V	--
	VOH	- - - - - - -	3.030 V	2.400 V	--
	VOH	- - - - - - -	3.040 V	2.400 V	--
	VOH	- - - - - - -	2.985 V	2.400 V	--
	VOL	- - - - - - -	166.5MV	--	450.0MV
	VOL	- - - - - - -	165.0MV	--	450.0MV
	VOL	- - - - - - -	169.0MV	--	450.0MV
	VOL	- - - - - - -	158.0MV	--	450.0MV
	VOL	- - - - - - -	159.0MV	--	450.0MV
	VOL	- - - - - - -	158.0MV	--	450.0MV
	VOL	- - - - - - -	161.0MV	--	450.0MV
	VOL	- - - - - - -	159.0MV	--	450.0MV
	VOL	- - - - - - -	172.5MV	--	450.0MV
	VOL	- - - - - - -	173.5MV	--	450.0MV
	VOL	- - - - - - -	174.5MV	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
	VOL	- - - - - - -	192.0MV	--	450.0MV

Figure V.E.15 - -5000 Volt Electrical Measurement

FILE UID :151 SERIAL NUMBER - 9

TESTED AT 25 DEG. C P5000V STRESS
ON 17 NOV 83 AT 09:07:25 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	VOL	- - - - - - -	191.5MV	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.910 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
	VOL	- - - - - - -	200.0MV	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
	VOL	- - - - - - -	201.0MV	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	VOL	- - - - - - -	4.905 V	--	450.0MV
****	IIL	- - - - - - -	217.5UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-992.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	220.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-938.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	186.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-918.5UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	196.5UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-915.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	185.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-886.5UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	187.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-882.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	165.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-816.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	168.5UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-840.0UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	27.20UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	-17.40UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	107.0UA	-10.00UA	10.00UA
	IIL	- - - - - - -	-6.570UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	83.40UA	-10.00UA	10.00UA
	IIL	- - - - - - -	8.620UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	48.00UA	-10.00UA	10.00UA
	IIL	- - - - - - -	3.790UA	-10.00UA	10.00UA
****	IIL	- - - - - - -	13.55UA	-10.00UA	10.00UA
	IIL	- - - - - - -	154.5NA	-10.00UA	10.00UA
	IIL	- - - - - - -	16.35NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.790UA	-10.00UA	10.00UA
	IIL	- - - - - - -	14.00NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-1.435UA	-10.00UA	10.00UA
	IIL	- - - - - - -	10.05NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-2.075UA	-10.00UA	10.00UA
	IIL	- - - - - - -	916.5NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-2.030UA	-10.00UA	10.00UA
	IIL	- - - - - - -	12.20NA	-10.00UA	10.00UA
	IIL	- - - - - - -	-2.425UA	-10.00UA	10.00UA

Figure V.E.15 - Post -5000 Volt Electrical Measurements (Cont.)

FILE UID :151 SERIAL NUMBER - 9

TESTED AT 25 DEG. C P5000V STRESS
ON 17 NOV 83 AT 09:07:59 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	IIL	- - - - - -	13.90NA	-10.00UA	10.00UA
	IIL	- - - - - -	-2.425UA	-10.00UA	10.00UA
	IIL	- - - - - -	43.85NA	-10.00UA	10.00UA
	IIL	- - - - - -	-5.035UA	-10.00UA	10.00UA
	IIL	- - - - - -	334.5NA	-10.00UA	10.00UA
	IIL	- - - - - -	-7.810UA	-10.00UA	10.00UA
	IIL	- - - - - -	73.45NA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.270UA	-10.00UA	10.00UA
	IIL	- - - - - -	56.15NA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.765UA	-10.00UA	10.00UA
	IIL	- - - - - -	54.80NA	-10.00UA	10.00UA
	IIL	- - - - - -	-6.585UA	-10.00UA	10.00UA
	IIL	- - - - - -	235.0NA	-10.00UA	10.00UA
	IIL	- - - - - -	-6.550UA	-10.00UA	10.00UA
	IIL	- - - - - -	48.95NA	-10.00UA	10.00UA
	IIL	- - - - - -	-4.425UA	-10.00UA	10.00UA
	IIL	- - - - - -	29.90NA	-10.00UA	10.00UA
	IIL	- - - - - -	-4.090UA	-10.00UA	10.00UA
	IIL	- - - - - -	46.20NA	-10.00UA	10.00UA
	IIL	- - - - - -	-7.915UA	-10.00UA	10.00UA
	IIL	- - - - - -	50.15NA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.145UA	-10.00UA	10.00UA
	IIL	- - - - - -	49.45NA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.230UA	-10.00UA	10.00UA
	IIL	- - - - - -	125.5NA	-10.00UA	10.00UA
	IIL	- - - - - -	-7.985UA	-10.00UA	10.00UA
	IIL	- - - - - -	61.60NA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.185UA	-10.00UA	10.00UA
	IIL	- - - - - -	915.5NA	-10.00UA	10.00UA
****	IIL	- - - - - -	-10.25UA	-10.00UA	10.00UA
****	IIL	- - - - - -	14.50UA	-10.00UA	10.00UA
	IIL	- - - - - -	-9.755UA	-10.00UA	10.00UA
	IIL	- - - - - -	39.60NA	-10.00UA	10.00UA
	IIL	- - - - - -	-8.520UA	-10.00UA	10.00UA
****	IIL	- - - - - -	25.25UA	-10.00UA	10.00UA
	IIL	- - - - - -	512.0NA	-10.00UA	10.00UA
****	IOL	- - - - - -	-479.0UA	-10.00UA	10.00UA
****	IOL	- - - - - -	58.90UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-434.0UA	-10.00UA	10.00UA
****	IOL	- - - - - -	59.85UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-391.5UA	-10.00UA	10.00UA
****	IOL	- - - - - -	45.85UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-371.5UA	-10.00UA	10.00UA
****	IOL	- - - - - -	43.40UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-359.0UA	-10.00UA	10.00UA
****	IOL	- - - - - -	40.05UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-359.5UA	-10.00UA	10.00UA
****	IOL	- - - - - -	41.60UA	-10.00UA	10.00UA
****	IOL	- - - - - -	-310.5UA	-10.00UA	10.00UA
****	IOL	- - - - - -	35.65UA	-10.00UA	10.00UA

Figure V.E.15 - Post -5000 Volt Electrical Measurements (Cont.)

FILE UID :151 SERIAL NUMBER - 9

TESTED AT 25 DEG. C P5000V STRESS
ON 17 NOV 83 AT 09:08:33 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
****	IOL	- - - - - -	-317.5UA	-10.00UA	10.00UA
****	IOL	- - - - - -	36.45UA	-10.00UA	10.00UA
	ICC	- - - - - -	102.3MA	--	180.0MA
	IILCE	- - - - - -	98.30UA	-100.0UA	100.0UA
	IILCE	- - - - - -	-25.75UA	-100.0UA	100.0UA

TEST RUNTIME IS 19 SECONDS
PRINT / DISPLAY TIME IS 109 SECONDS

Figure V.E.15 - Post -5000 Volt Electrical Measurements (Cont.)

Number of Failures at Pin Locations								
3	4	7	8	9	10	11	Cumulative # Removed	Voltage
		1		1	2			+1250
	1	1		2	2			-1250
	6	4	1	6	5	3		+1500
	7	4	1	6	5	3		-1500
8	10	7	1	7	9	8	1	+1750
8	11	11	1	7	10	8	4	-1750
13	14	14	8	13	13	13	14	+2000

Figure V.E.16 - CD Stress, Cumulative Leakage Current Failures

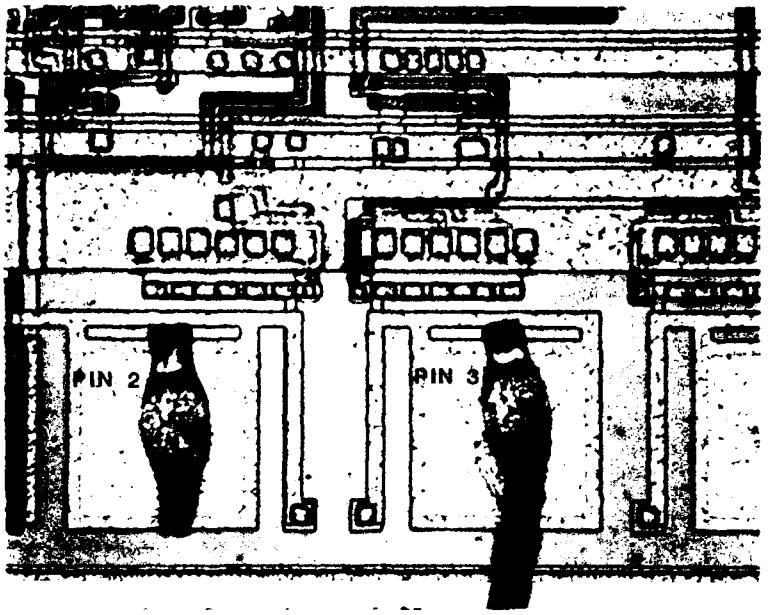


Figure V.E.17 - Input Pin 3 and Input/Output Pin 2.

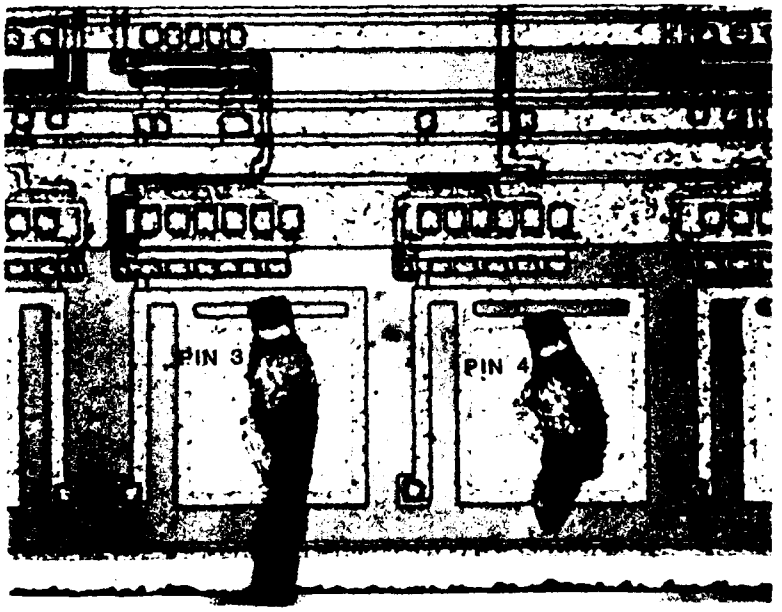


Figure V.E.18 - Input Pins 3 and 4.

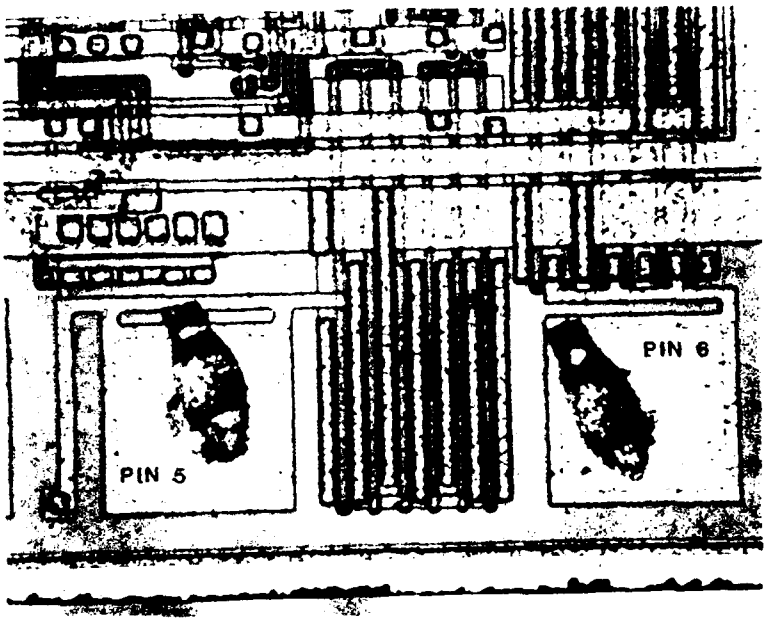


Figure V.E.19 - I/O Pin 5 and Output Pin 6

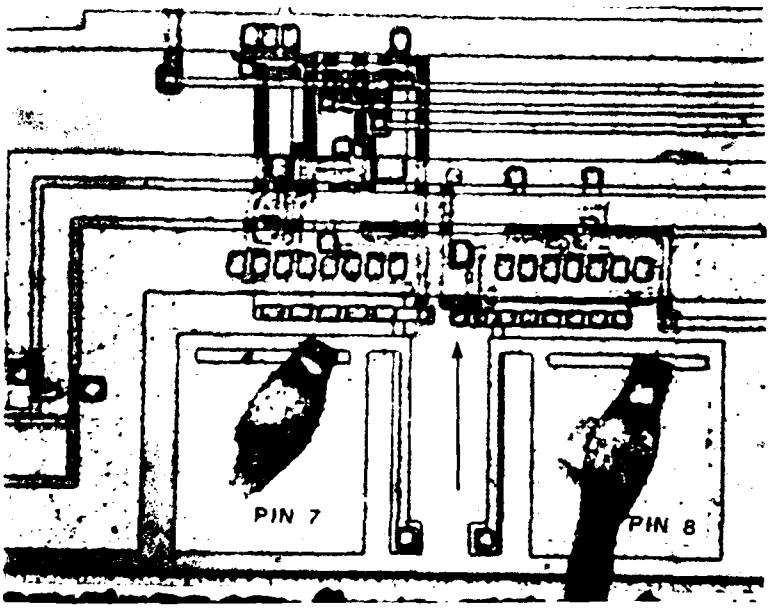


Figure V.E.20 - Input Pins 7 and 8, Arrow Indicates Extra Diffusion Contact

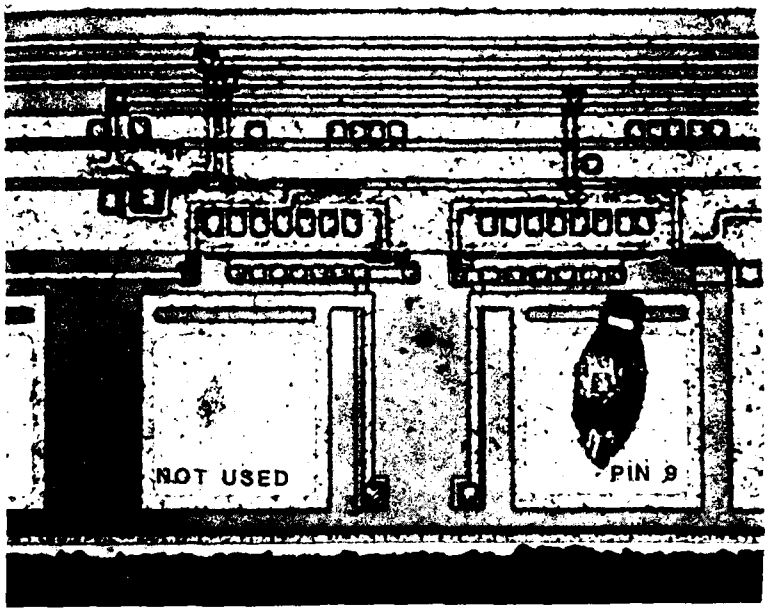


Figure V.E.21 - Pin 9 Input

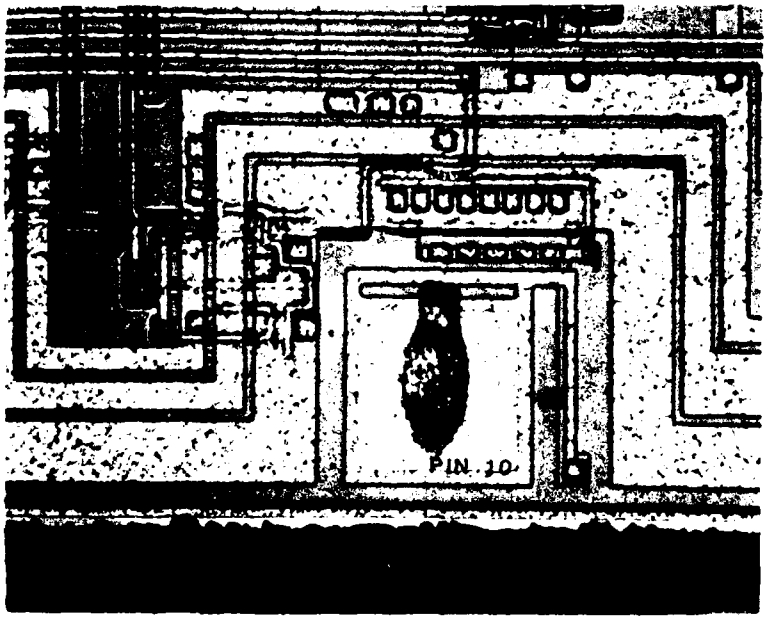


Figure V.E.22 - Pin 10 Input

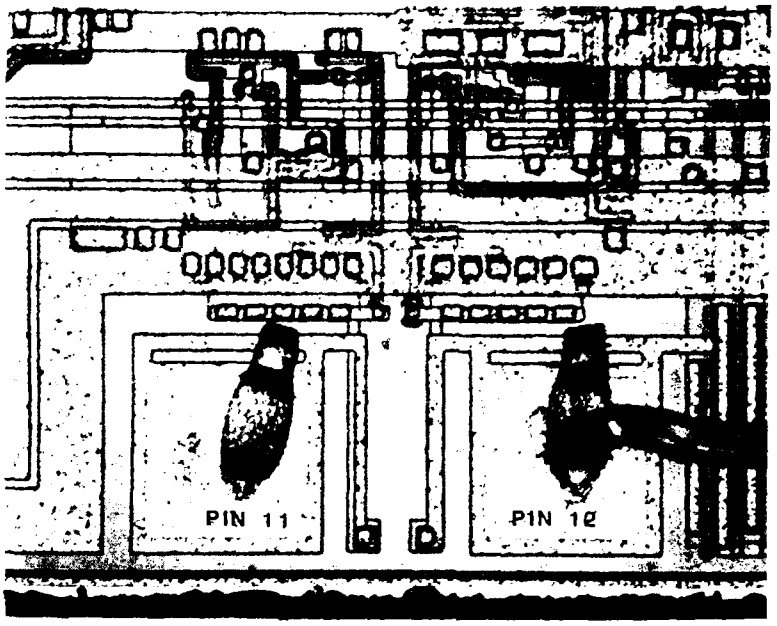


Figure V.E.23 - Pin 11 Input and Pin 12 Input/Output

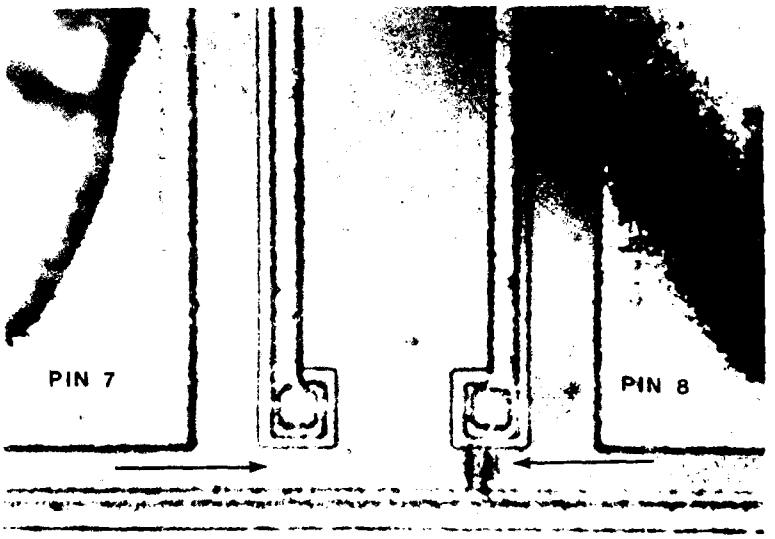


Figure V.E.24 - CD Stress, Damage on Pins 7 and 8

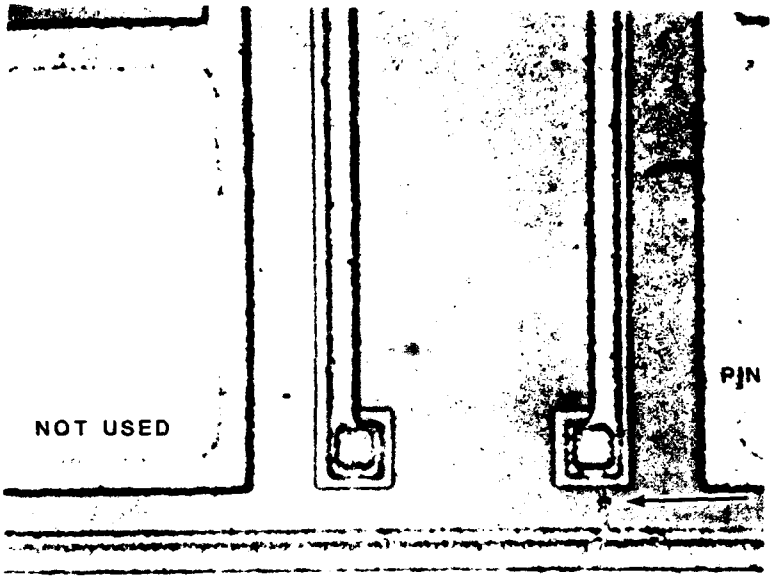


Figure V.E.25 - CD Stress, Damage on Pin 9

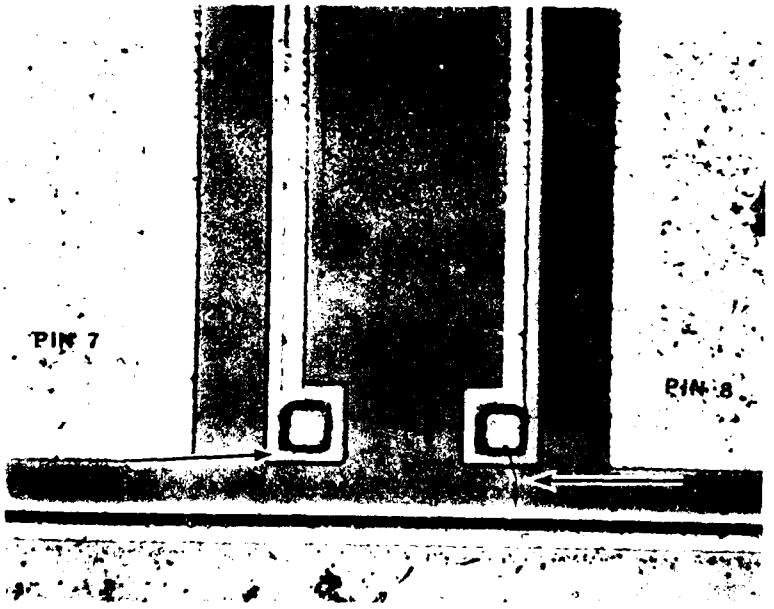


Figure V.E.26 - CD Stress, Damage on Pins 7 and 8

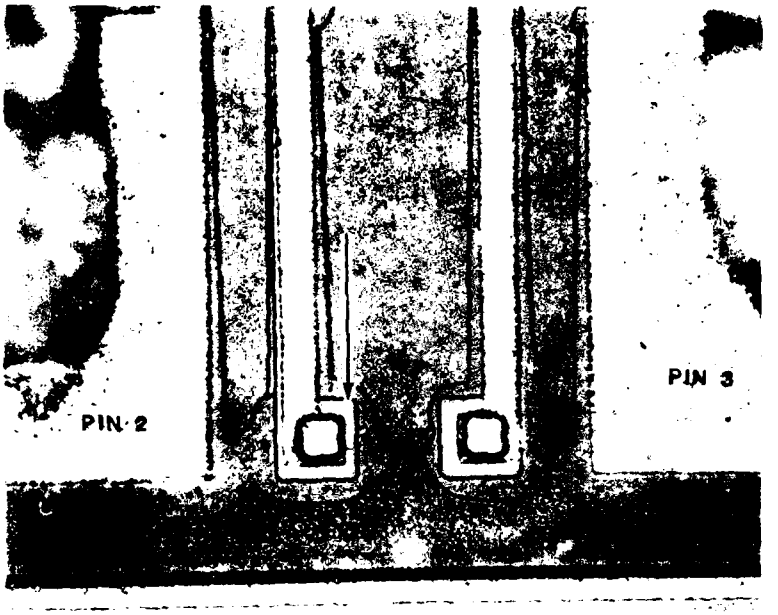


Figure V.F.27 - CD Stress, Damage on Pins 2 and 3

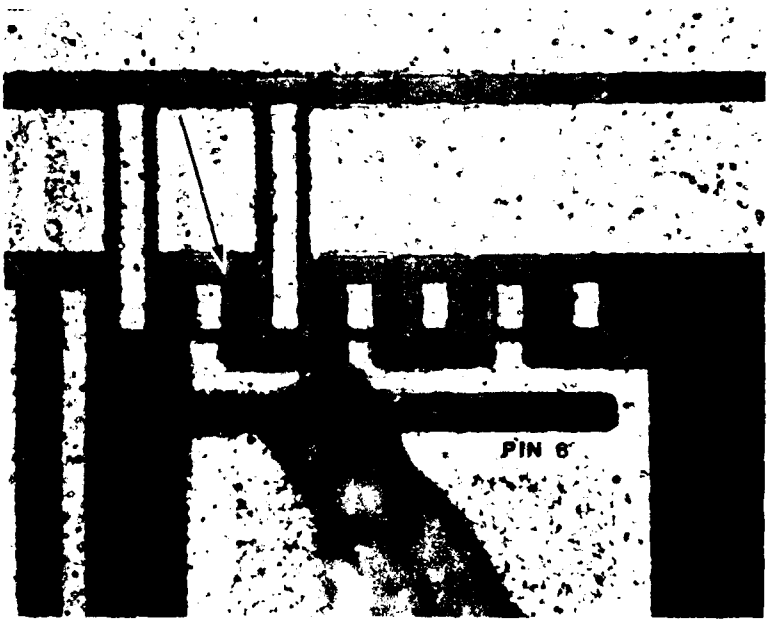


Figure V.F.28 - CD Stress, Pin 6 Output Damage

Number of Failures at Pin Locations								
3	4	7	8	9	10	11	Cumulative # Removed	Voltage
1	1	1	1				2	less than +3500
		2	2		2	1	2	+3500
		4	3	2			3	+3750
2					3		5	-3750
4	2	6				2		+4000
	3			3		3	7	-4000
	4	7				4		+4250
				4			8	-4250
5		8						+4500
		9	4				9	-4500
6	4	9	4	5	4	4	11	-4750

Figure V.E.29 - HBD Stress, Cumulative Leakage Current Failures (13 devices total)

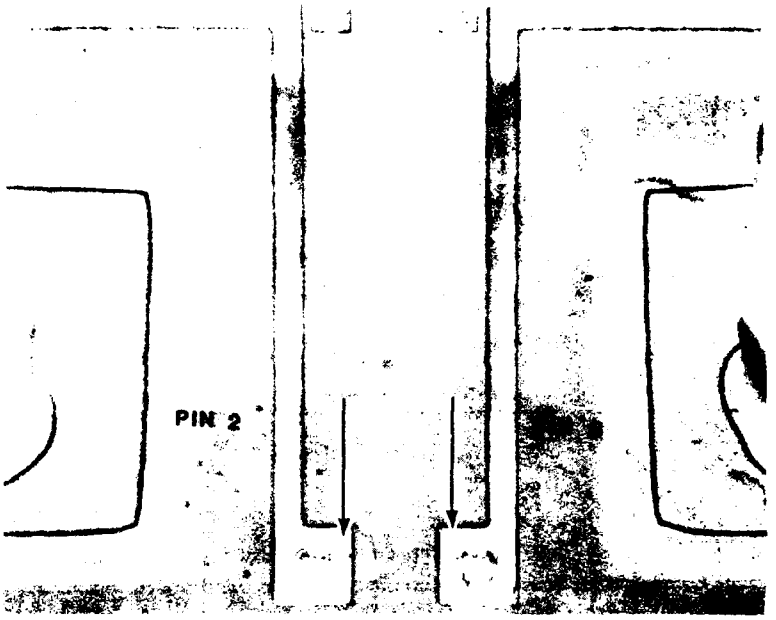


Figure V.E.30 - HBD Stress, Damage on Pins 2 and 3

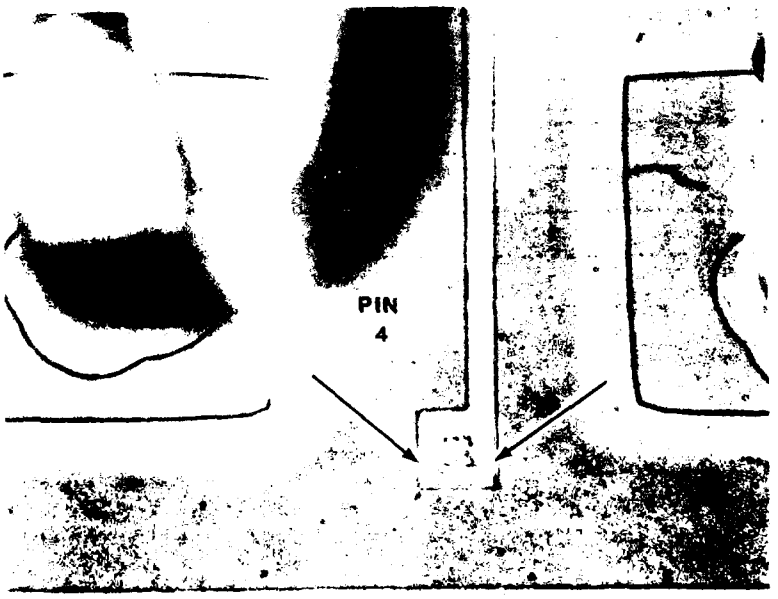


Figure V.E.31 - HBD Stress, Damage on Pin 4

Figure V.E.32 - HBD Stress, Damage on Pins 7 and 8

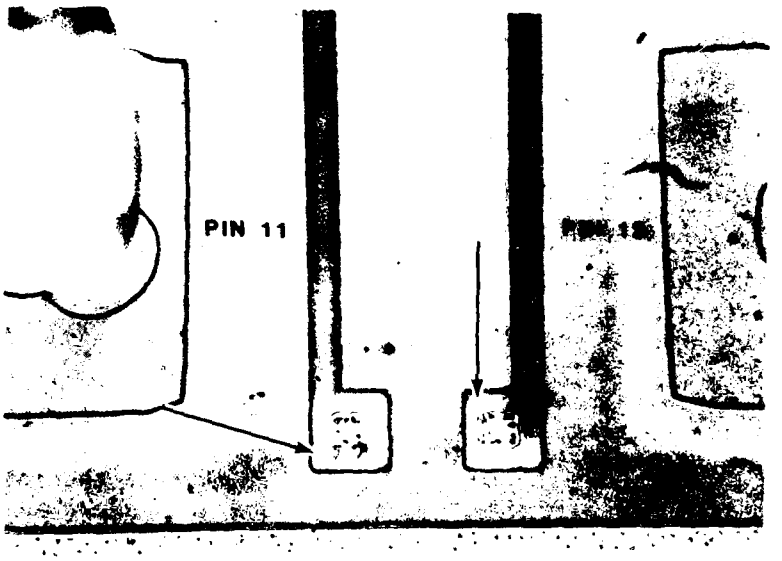


Figure V.E.33 - HBD Stress, Damage on Pins 11 and 12

F. Part F Analysis

This device is a 4096 x 1-bit static RAM manufactured using a CMOS polysilicon self aligned process. The metallization linewidth was about 4.5 microns and the two polysilicon layer linewidths were about 3.0 microns. This was in an 18-pin dual-in-line ceramic package.

An overall die photograph is shown in Figure V.F.1. VCC is pin 18 at the top of Figure V.F.1 and GND is pin 9 at the bottom. VCC is shown in Figure V.F.2. A bond wire from pin 18 also is connected to a chip on the package substrate. The VCC metallization makes contact to the substrate at various points around the perimeter of the die, it contacts the protect diodes, and the source diffusions on the P-channel MOS transistors.

Groun is shown in Figure V.F.3. Its metallization makes contact to the protect diodes and to the source diffusion on the N-channel MOS transistors.

An input circuit is shown in Figure V.F.4 and the corresponding schematic is shown in Figure V.F.5. The connection to the body of the transistors were not evident in the input section.

The layouts of the inputs varied considerably. A second type of input structure is shown in Figure V.F.6 (input A5) and in the schematic in Figure V.F.7. The polysilicon gate for the P-Channel transistor is in series with the N-Channel transistor and there is a shift in the order of the resistors and diodes.

There are 5 separate input layouts. These include the two shown above and the following combinations: 1) resistor, VCC diode, resistor, GND diode, series gates; 2) resistor, diodes, resistor, series gates; 3) resistor, diodes, resistor, series gates and also another resistor to parallel gate inputs. The resistors vary from about 280 ohms to 900 ohms. The gate dielectric breakdown was about 45 volts. D1 breakdown was 28 VDC, D2 breakdown was 25 VDC, Q1 junction breakdown was 25 VDC, and Q2 junction breakdown was 20 VDC.

There is a single output on this device. It is connected to the two output transistors by a long metallization run. The transistors are shown in Figure V.F.8 and the schematic is shown in Figure V.F.9.

Microsections were performed to look at the transistor diffusions and the metallization coverage over the polysilicon. Figure V.F.10 shows the metallization and polysilicon. The metallization is about 1.0 microns thick, the polysilicon is about 0.35 microns thick, and the insulating oxide is about 0.5 microns on either side of the polysilicon. The polysilicon was approximately 55 ohms per square.

Cross-sections through the output transistors are shown in Figures V.F.11 - V.F.13. Figure V.F.11 is a top view showing the location of the high magnification cross-section photographs. Figure V.F.12 shows the edge

of the N-Channel transistor. Figure V.F.13 shows the other edge of the N-Channel transistor and the edge of the P-Channel transistor. The diffusion depths are approximately, n+ diffusion = 0.5 microns, p body diffusion = 3.0 microns, and p+ diffusions = 1.2 microns.

Electrical Testing

A sample of the electrical data which was taken on each of the stressed parts and the control part at each iteration during the testing is shown in Figures V.F.14 and V.F.15. Figure V.F.14 shows the initial readings on serial number 9 and Figure V.F.15 shows the readings after the -1000 volt stress. Supply current, input leakage at 0 volts and 5.5 volts, leakage current with output disabled, and the output high and low voltage levels were measured. This testing provided a functional verification of the control lines (W,E) and of the data input pin. Additional testing was performed at the same points as the parametric testing. This was done with a benchtop test setup and included writing and reading all highs and all lows and verifying the functions of write enable and chip enable.

In Figure V.F.15 the supply current readings are very high and one of the inputs is shorted. Testing with the part having this type of parametric readings found them to be nonfunctional.

Charged Device Data Analysis

Fifteen devices, serial numbers 17-31 were stressed with the charged device model. There was no gradual change in the device characteristics. The parts would work properly following one stress level and would then fail with high supply current and input leakage after the next stress. The input pins which showed leakage and the point at which they showed the leakage are shown in Figure V.F.16. This is a summary for only 10 of the devices. Five parts were pulled and analyzed after they failed functionally.

The wide variations in physical layout did cause variations in the sensitivity. Unfortunately the failures encountered on these parts were not due to limitations in the design used for the input protect circuits. The failures occurred due to the layouts of the polysilicon and metallization coming from the device pins and weaknesses in the oxide beneath these two layers. Comparison of the results on this part to the results on the other devices indicates the importance of input layout to sensitivity. The protect network on pins 1-3 and 15-17 worked well while the remainder of the pins had numerous problems. The layout for these 6 acceptable pins is similar to that shown in Figure V.F.4 while the extended layout problems were due to layouts similar to that shown in Figure V.F.6.

Failure analysis found shorts between metallization and polysilicon, and between polysilicon and silicon. Several of these are shown in Figures V.F.17 - V.F.22. Figures V.F.17 and V.F.18 show a short between pins 7 and 14. This is at a point where metallization goes over a polysilicon crossunder. Figures V.F.19 and V.F.20 show shorts which occurred between

pins 6 and 7 and between pin 6 and the substrate. Figure V.F.21 shows a short between the metallization going to pin 7 and the polysilicon connected to pin 12. A more subtle failure is shown in Figure V.F.22. This is damage to the polysilicon line connected to pin 13.

The failure threshold of these parts to charged device ESD stress was very low. This was due to poor layout and possibly inadequate oxide thickness or processing.

Human Body Discharge Data Analysis

Device serial numbers 2 through 16 were stressed with the human body discharge test method.

A summary of the input pins and the point at which they failed leakage testing are shown in Figure V.F.23. The inputs went rapidly from no leakage to high leakage conditions.

The failure analysis on these parts found the same basic failure modes as the charged device model with some differences in location. Pins 1-3 and 15-17 were somewhat more sensitive to this stress than to the CD stress.

Samples of several of these failures are shown in Figures V.F.24 - V.F.27, Figure V.F.24 shows a breakdown between pins 6 and 7. This is similar to the HBD stress failures. Figure V.F.25 shows a failure between pins 12 and 7 and also between GND and pin 13. Figure V.F.26 shows damage which occurred on the polysilicon input resistor on pin 1. This was shorted to VCC (substrate). Figure V.F.27 shows damage on pin 17 input. This point had shorted to the substrate.

The polysilicon resistors do become damaged with stress as evidenced in Figure V.F.26. This limits their usefulness for input protection circuits. On this device the major limitation was the physical layout which allowed overlying metallization and input polysilicon to cross. There is little useful sensitivity variation information available from this device.

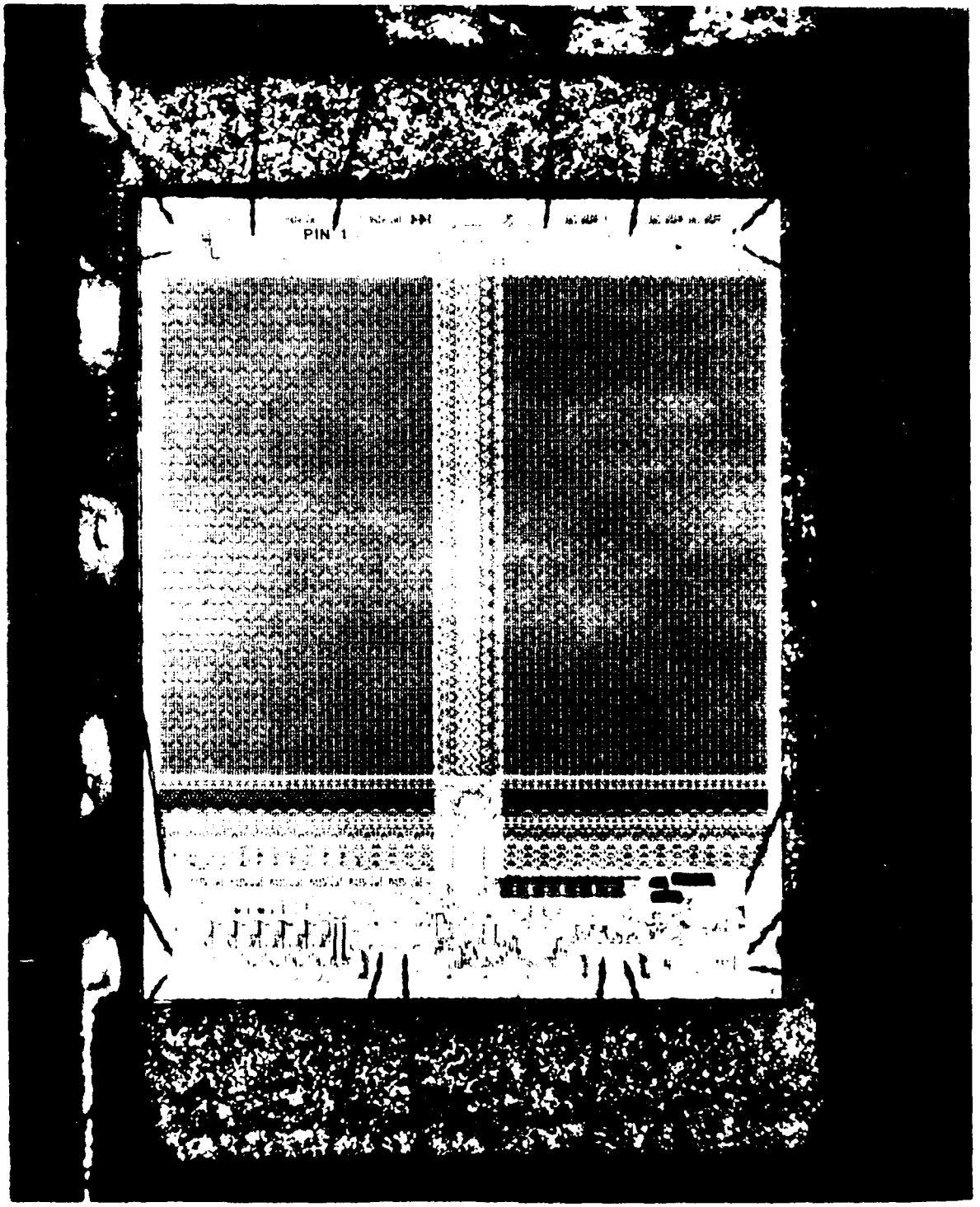


Figure V.F.1 - Overall Die Photograph

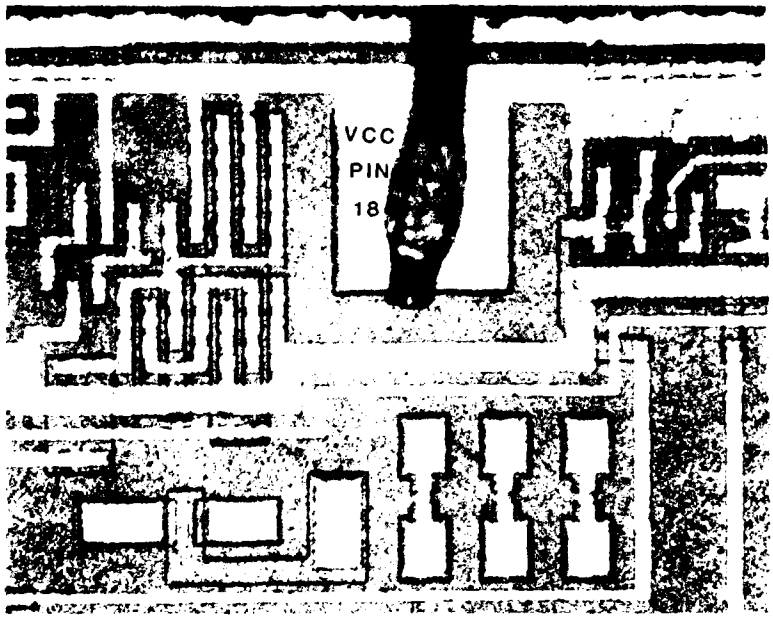


Figure V.F.2 - VCC Bond Pad

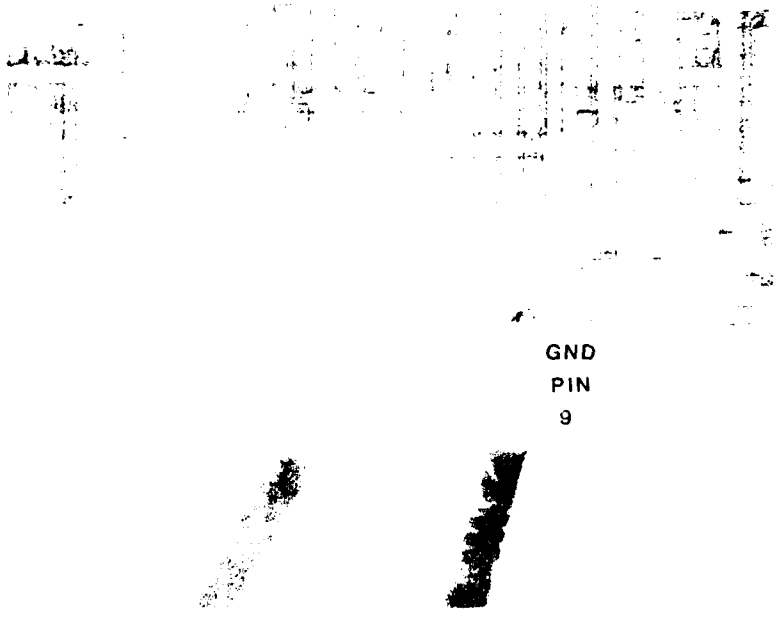


Figure V.F.3 - GND Bond Pad

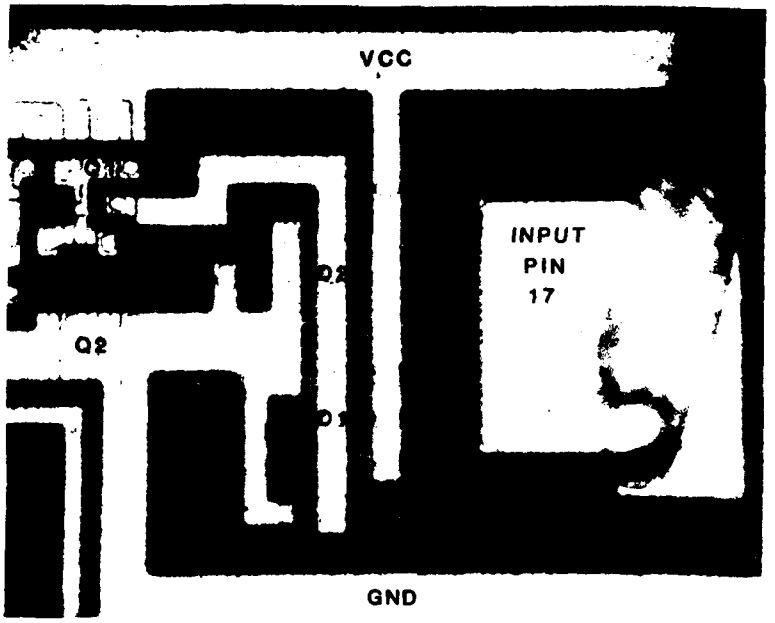


Figure V.F.4 - Pin 17 Input

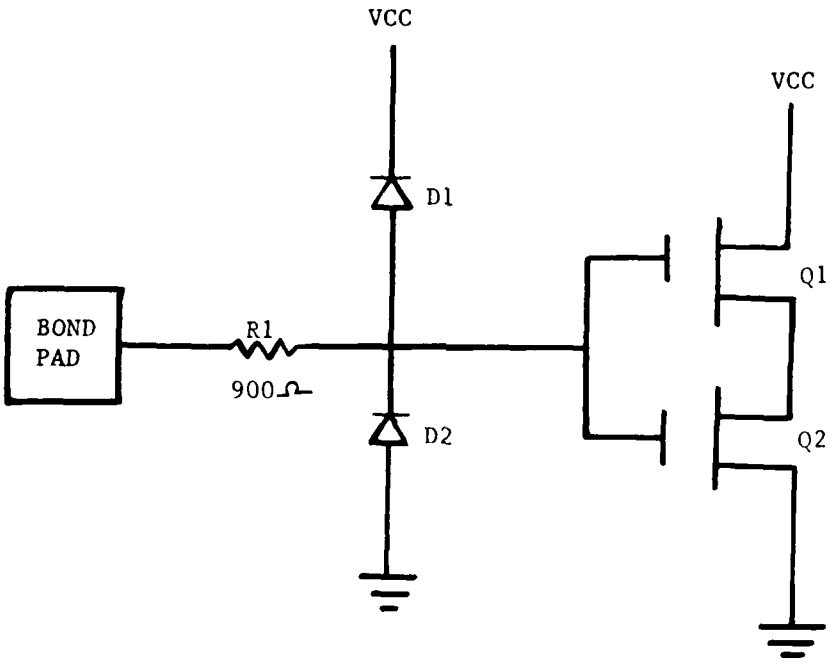


Figure V.F.5 - Pin 17 Input Schematic

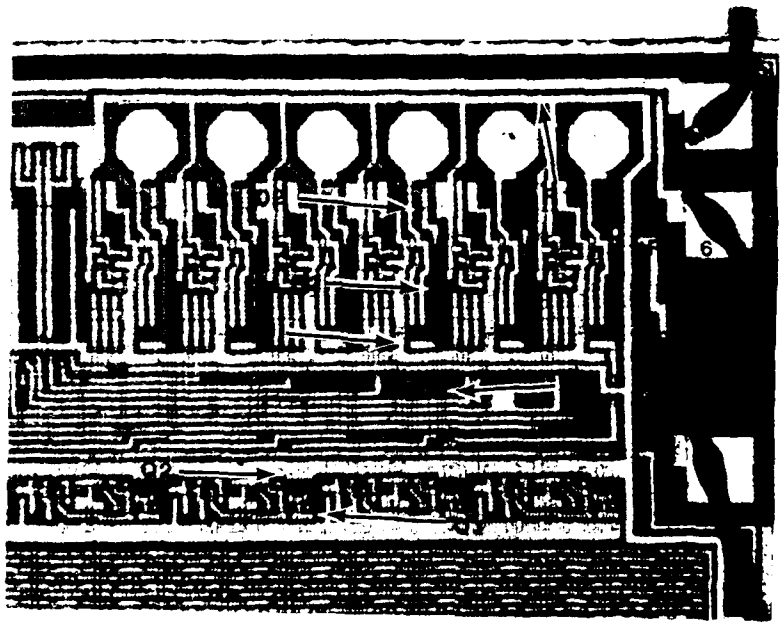


Figure V.F.6 - Pin 6 Input

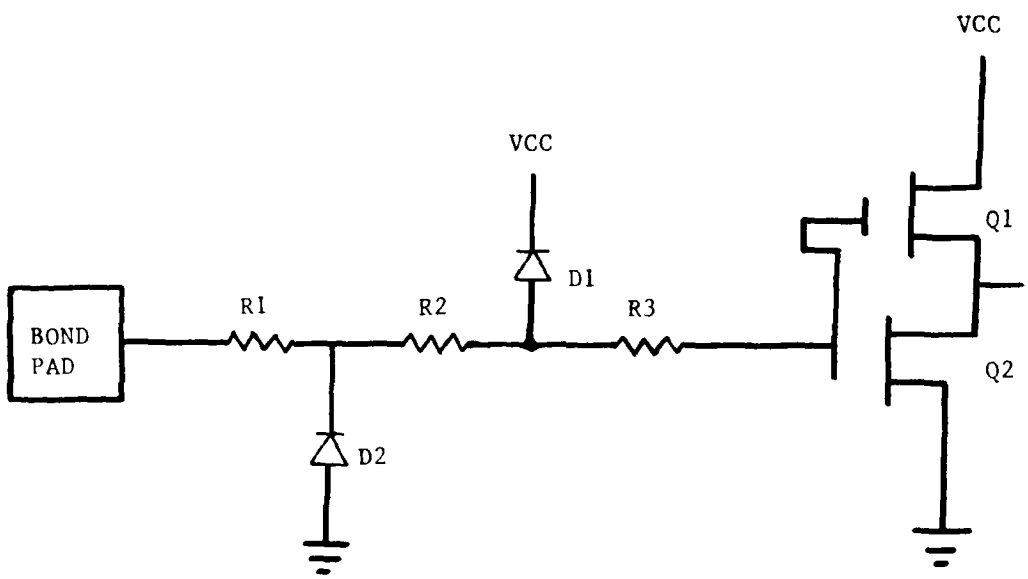


Figure V.F.7 - Pin 6 Input Schematic

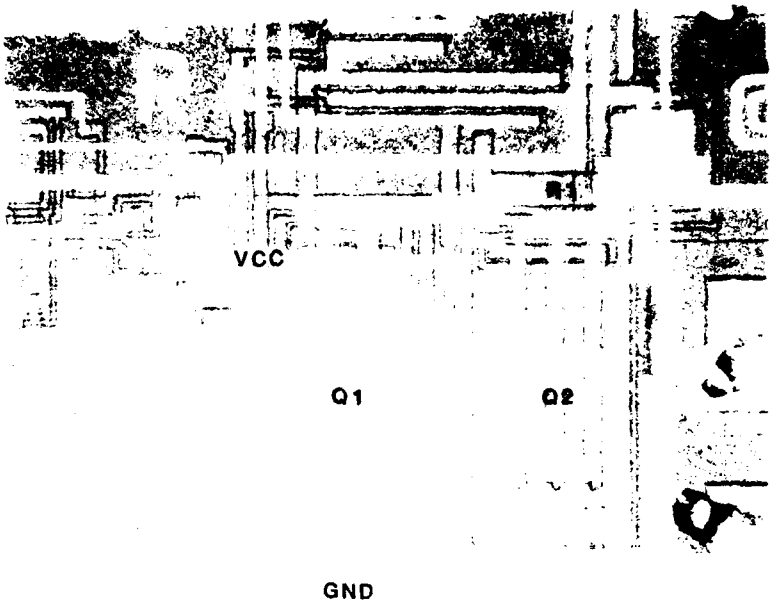


Figure V.F.8 - Pin 7 Output

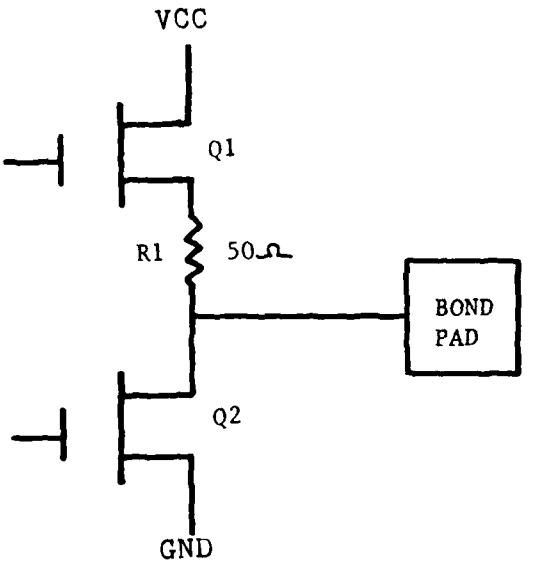


Figure V.F.9 - Pin 7 Output Schematic

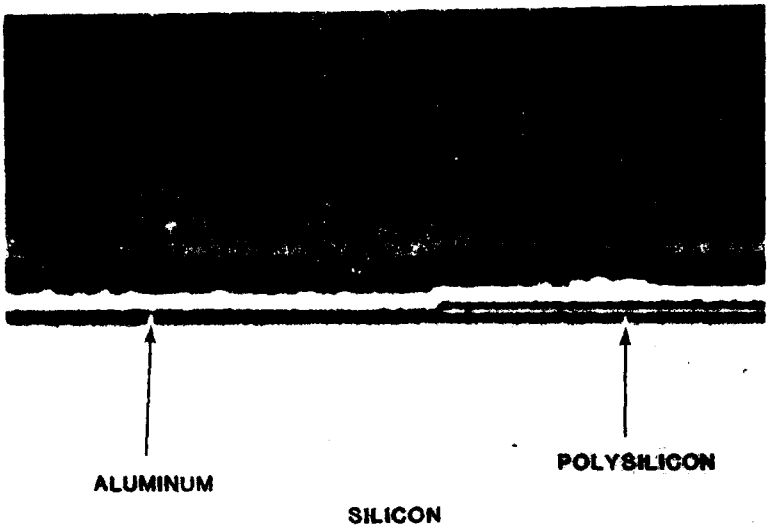


Figure V.F.10 - Cross-Section of Metallization and Polysilicon

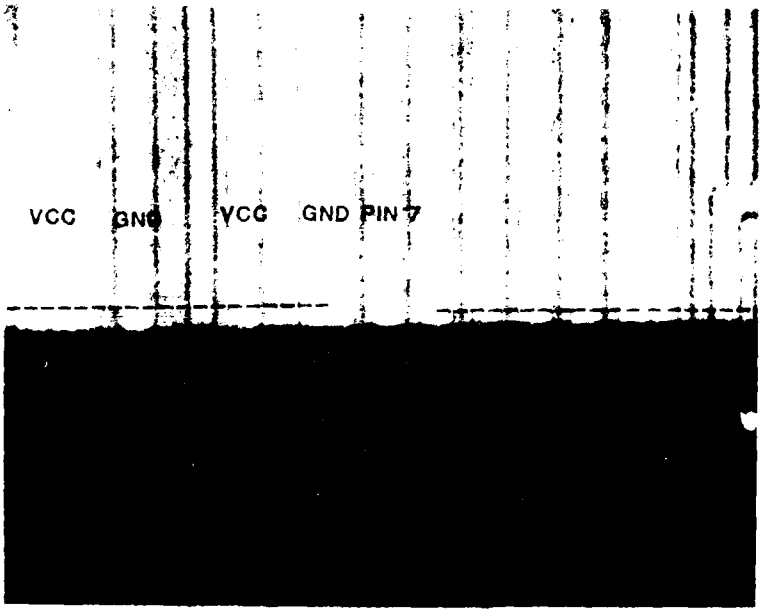


Figure V.F.11 - Top View of Output Transistors

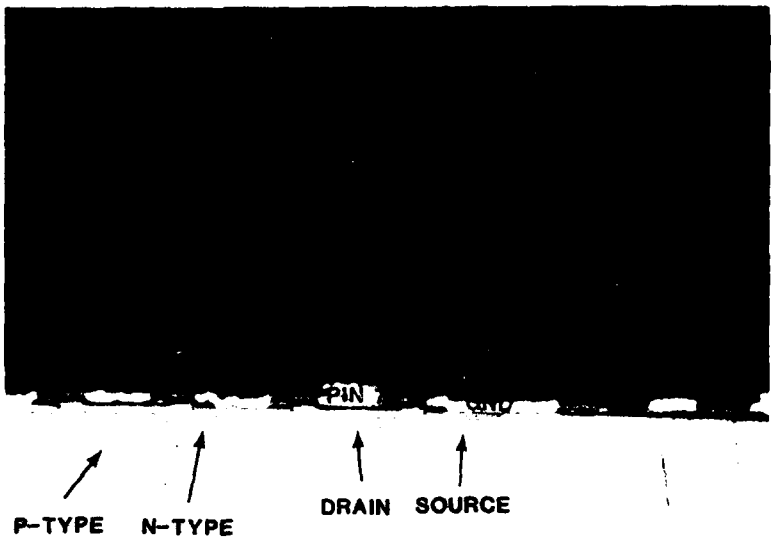


Figure V.F.12 - Cross-Section of N-Channel Transistor

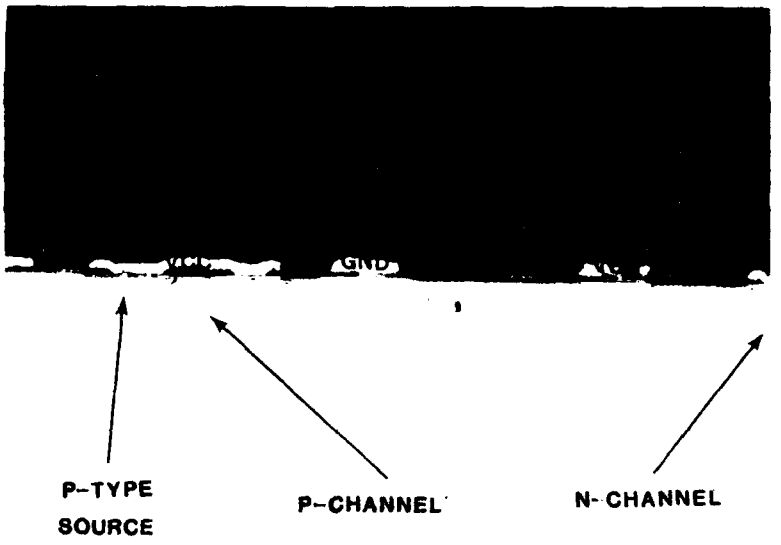


Figure V.F.13 - Cross-Section of edge of P-Channel and edge of N-Channel Transistors

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID 1148 SERIAL NUMBER - 4

TESTED AT 25 DEG. C NO. 1 ELECTRICAL
ON 13 JUL 83 AT 14:45:09 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	ICCSB - - - - - -	2.400NA	--	50.00UA
	ICCSB - - - - - -	2.200NA	--	50.00UA
	ICCOP - - - - - -	3.751MA	--	7.000MA
	ICCDR - - - - - -	500.0PA	--	25.00UA
	ICCDR - - - - - -	1.000NA	--	25.00UA
	II - - - - - -	-290.0PA	-1.000UA	1.000UA
	II - - - - - -	1.220NA	-1.000UA	1.000UA
	II - - - - - -	-500.0PA	-1.000UA	1.000UA
	II - - - - - -	1.150NA	-1.000UA	1.000UA
	II - - - - - -	-530.0PA	-1.000UA	1.000UA
	II - - - - - -	1.150NA	-1.000UA	1.000UA
	II - - - - - -	-520.0PA	-1.000UA	1.000UA
	II - - - - - -	1.090NA	-1.000UA	1.000UA
	II - - - - - -	-515.0PA	-1.000UA	1.000UA
	II - - - - - -	1.085NA	-1.000UA	1.000UA
	II - - - - - -	-540.0PA	-1.000UA	1.000UA
	II - - - - - -	1.085NA	-1.000UA	1.000UA
	II - - - - - -	-565.0PA	-1.000UA	1.000UA
	II - - - - - -	1.150NA	-1.000UA	1.000UA
	II - - - - - -	-540.0PA	-1.000UA	1.000UA
	II - - - - - -	1.100NA	-1.000UA	1.000UA
	II - - - - - -	-560.0PA	-1.000UA	1.000UA
	II - - - - - -	1.180NA	-1.000UA	1.000UA
	II - - - - - -	-540.0PA	-1.000UA	1.000UA
	II - - - - - -	1.090NA	-1.000UA	1.000UA
	II - - - - - -	-560.0PA	-1.000UA	1.000UA
	II - - - - - -	1.090NA	-1.000UA	1.000UA
	II - - - - - -	-575.0PA	-1.000UA	1.000UA
	II - - - - - -	1.115NA	-1.000UA	1.000UA
	II - - - - - -	-585.0PA	-1.000UA	1.000UA
	II - - - - - -	1.130NA	-1.000UA	1.000UA
	II - - - - - -	-590.0PA	-1.000UA	1.000UA
	II - - - - - -	1.100NA	-1.000UA	1.000UA
	II - - - - - -	-650.0PA	-1.000UA	1.000UA
	II - - - - - -	1.140NA	-1.000UA	1.000UA
	IOZ - - - - - -	3.400NA	-1.000UA	1.000UA
	IOZ - - - - - -	-1.800NA	-1.000UA	1.000UA
	VOL - - - - - -	74.50MV	--	400.0MV
	VOH - - - - - -	4.355 V	2.400 V	--

TEST RUNTIME IS 71 SECONDS
PRINT / DISPLAY TIME IS 29 SECONDS

Figure V.F.14 - Initial Electrical Measurement

```
[illegible] MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION [illegible]

                                   FILE UID  1148    SERIAL NUMBER -
 TESTED AT  25 DEG. C        NO. 9
ON [illegible] SEP 83 AT 15:25:49 WITH THE 3260 TEST SYSTEM
--------------------------------------------------------------------------
           TEST                         MEASURED          L I M I T S
FAIL       TYPE                          VALUE         MINIMUM     MAXIMUM
--------------------------------------------------------------------------
           ICCSB    - - - - - - -     -8.400uA           --       [illegible]
****       ICCSB    - - - - - - -      9.500mA           --       [illegible]

****       ICCOF    - - - - - - -      13.14mA           --       [illegible]

****       ICCLR    - - - - - - -      162.0uA           --       [illegible]
****       ICCOR    - - - - - - -      3.430mA           --       [illegible]

           II       - - - - - - -     -155.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      800.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -335.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      725.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -345.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      705.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -340.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      685.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -325.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      955.0PA      -1.0000UA     [illegible]
****       II       - - - - - - -     -10.24mA      -1.0000UA     [illegible]
           II       - - - - - - -     -986.1nA      -1.0000UA     [illegible]
           II       - - - - - - -     -325.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      660.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -385.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      675.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -380.0PA      -1.0000UA     [illegible]
           II       - - - - - - -      735.0PA      -1.0000UA     [illegible]
           II       - - - - - - -     -295.0PA      [illegible]   [illegible]
           II       - - - - - - -      4.[illegible] [illegible]  [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]
           II       - - - - - - -     [illegible]   [illegible]   [illegible]

           IOZ      - - - - - - -     [illegible]   [illegible]   [illegible]
           [illegible] - - - - - - -  [illegible]   [illegible]   [illegible]

           [illegible] - - - - - - -  [illegible]        --       [illegible]

           [illegible] - - - - - - -  [illegible]   [illegible]   [illegible]

[illegible]
[illegible]
```

Figure V.F.15 - Post -1000 Volt Electrical Measurement

Number of Failures at Pin Locations

1	2	3	4	5	6	8	10	11	12	13	14	15	16	17	Voltage
										3					+250
										7					-250
			7	1	2	2	1	1	1	9	5				+500
					5	9	3	9	4	10					-500
			10	9	6		7	10	5		6	1			+750
		1	10	9	7	9	10	10	6	10		2			-750

Figure V.F.16 - CD Stress, Cumulative Leakage Failures (Summary of 10 parts)

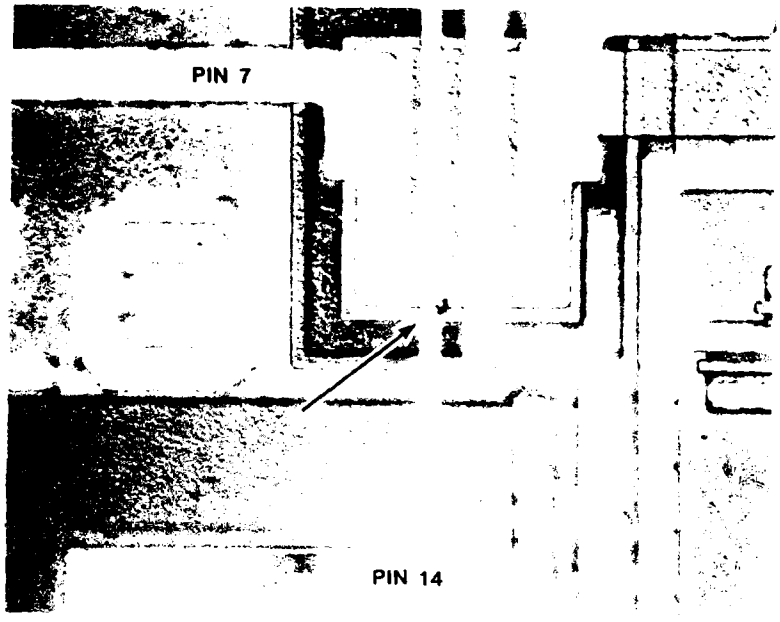


Figure V.F.17 - CD Stress, Pin 7 to Pin 14 Short

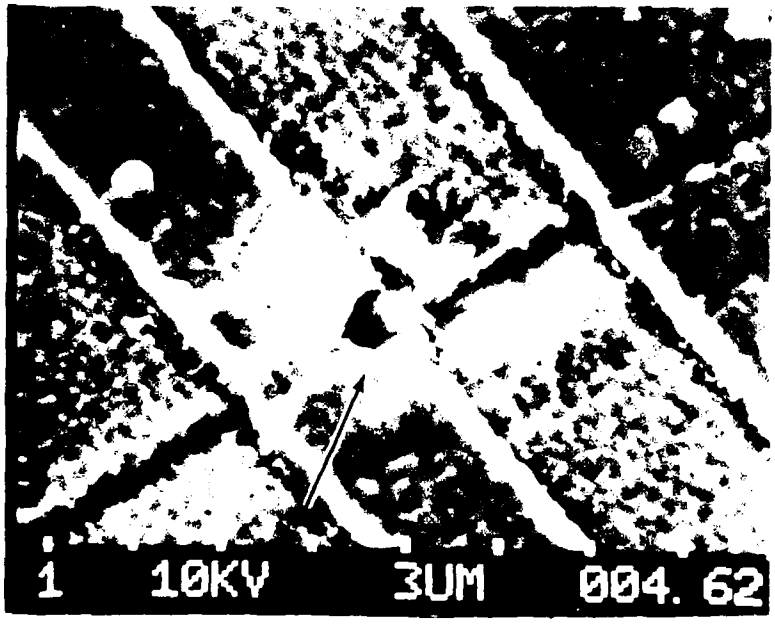


Figure V.F.18 - CD Stress, SEM Micrograph of Pin 7 to Pin 14 Damage

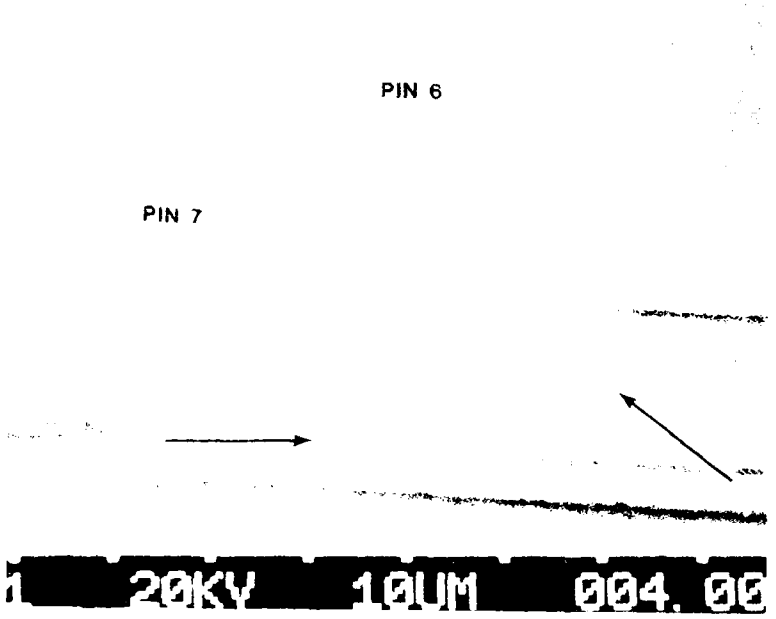


Figure V.F.19 - CD Stress, SEM Micrograph of Pin 6 to Pin 7 Damage

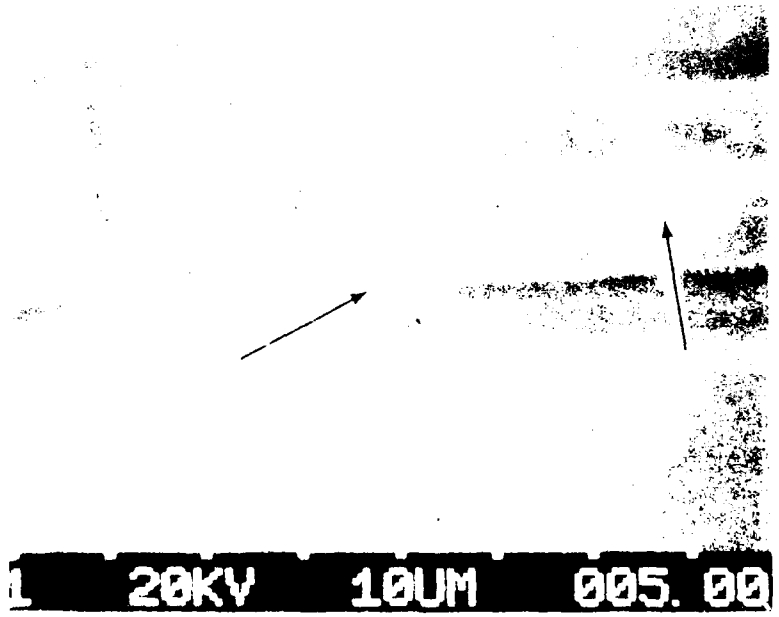


Figure V.F.20 - CD Stress, SEM Micrograph of Same Area as Previous Photo

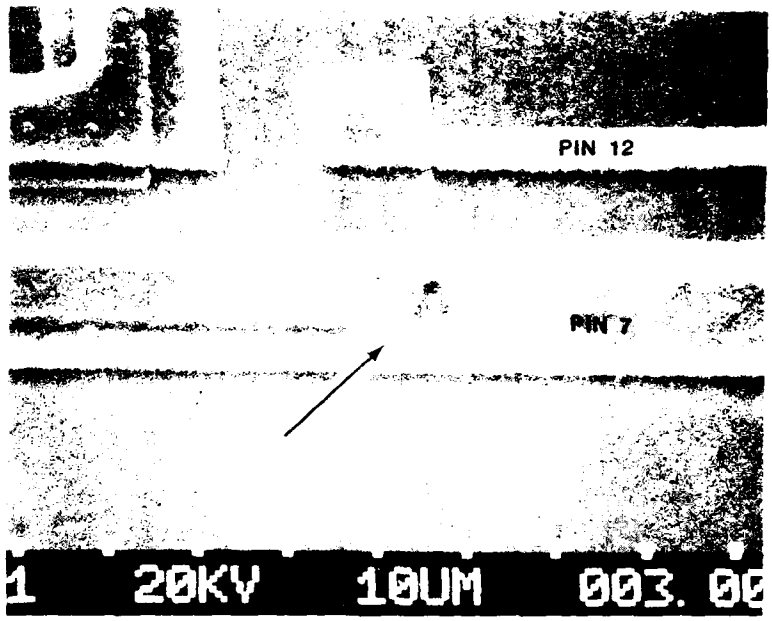


Figure V.F.21 - CD Stress, Short Between Pins 7 and 12

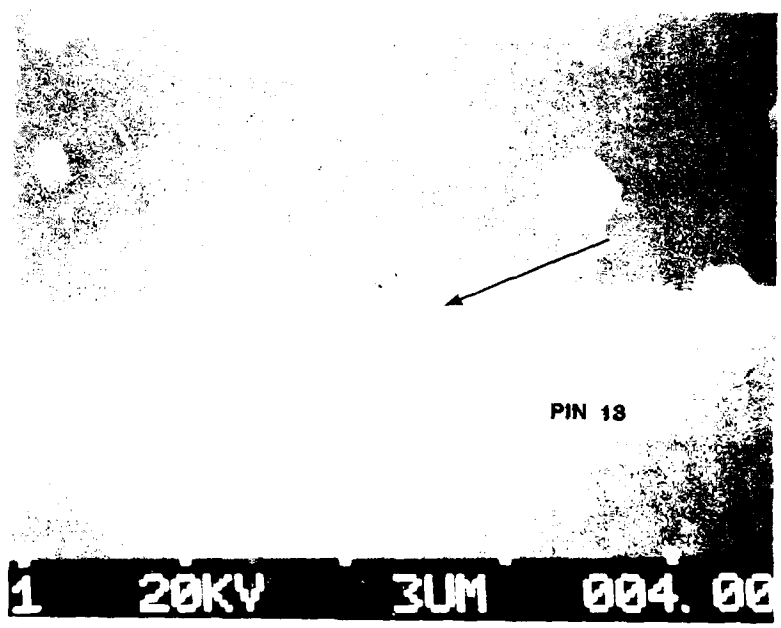


Figure V.F.22 - CD Stress, Short to Pin 13 Polysili

Number of Failures at Pin Locations

1	2	3	4	5	6	8	10	11	12	13	14	15	16	17	Voltage
										2	1				-500
1							1				2				+750
2	1	1	1	1	1	1	2	1	1	5	3	1	1	1	-750
					3						4				+1000
					7				2	6					-1000
	2	2	2	4	8	2	4	2	4	8	7	2	2	2	+1250
3	3	3	3	5	9	3	5	3	5	9	9	3	3	3	-1250
3	3	3	3	7	9	4	5	3	5	9	9	3	3	3	+1500

Figure V.F.23 - HBD Stress, Cumulative Leakage Failures (Summary of 10 Parts)

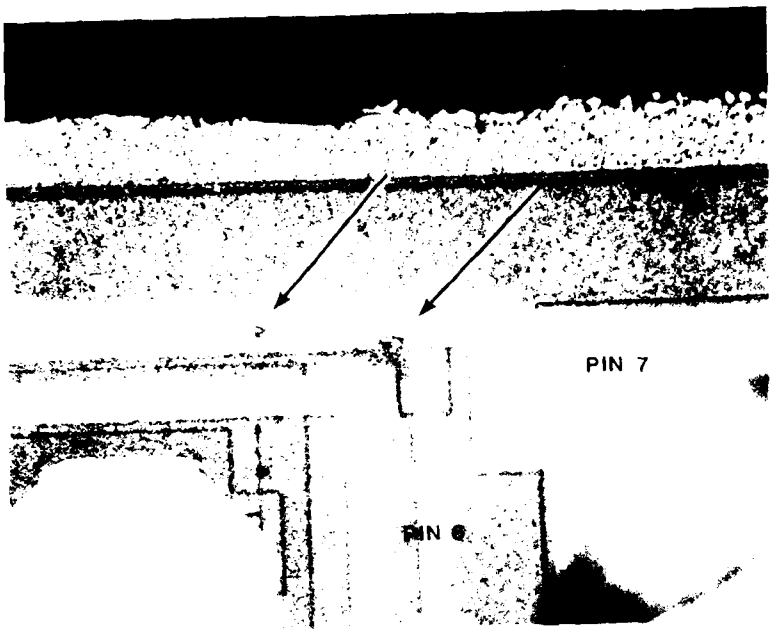


Figure V.F.24 - HBD Stress, Pin 6 to Pin 7 Damage

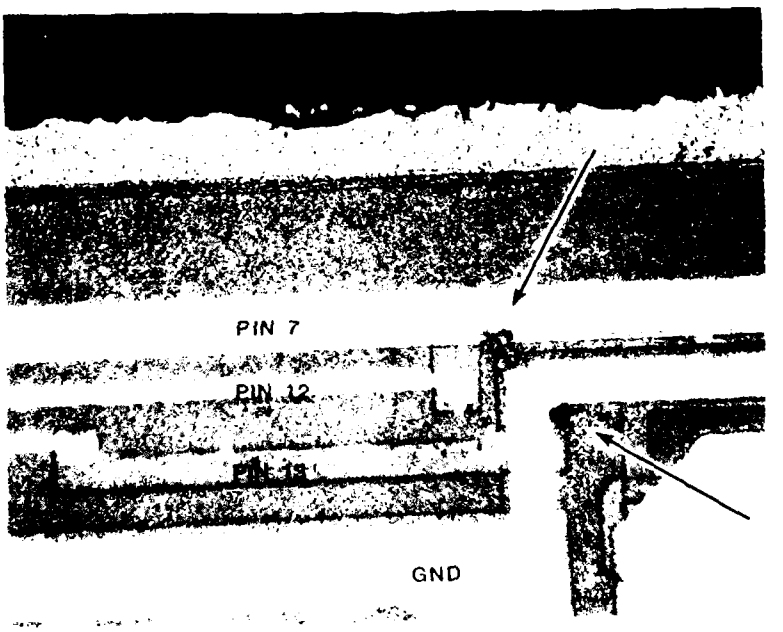


Figure V.F.25 - HBD Stress, Damage Sites Between Pins 7 and 12 and Between Pin 13 and GND

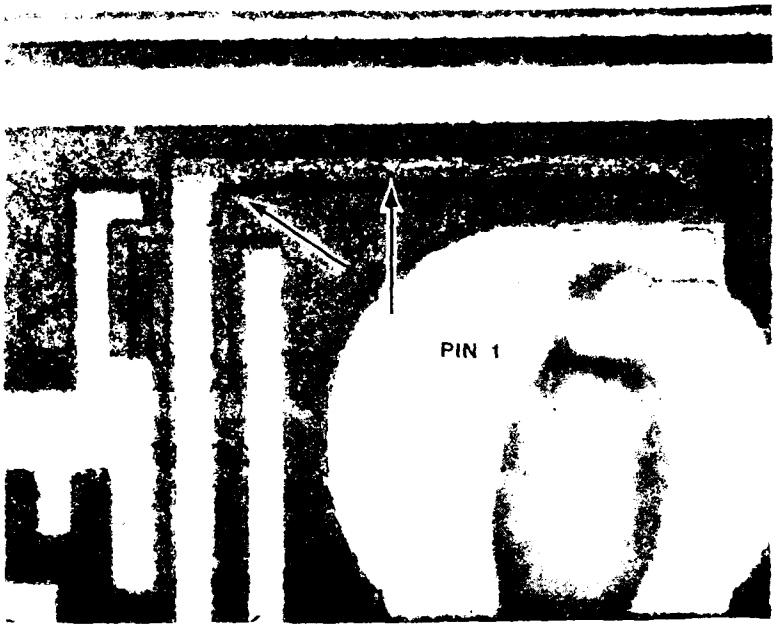


Figure V.F.26 - HBD Stress, Polysilicon Damage and Possible Short Site at Corner

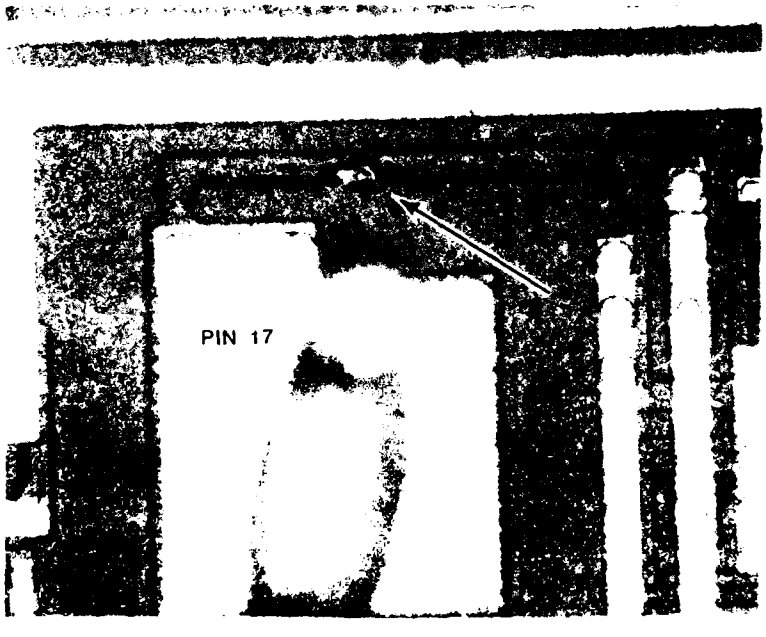


Figure V.F.27 - HBD Stress, Pin 17 Polysilicon Damage

G. Part G Analysis

This device is a 16-Bit Microprocessor manufactured using a high-density, N-channel silicon-gate depletion load process (HMOS). There is one layer of metallization and one layer of polysilicon. The metallization stripes are approximately 3.5 microns wide and the polysilicon is 2.5 microns wide. This was in a 64-pin dual-in-line ceramic package with a metal lid.

An overall die photo is shown in Figure V.G.1. VCC is connected to pins 14 and 49 and GND is connected to pins 16 and 53. These are shown in Figures V.G.2 and V.G.3. The metallization distribution pattern is visible in the photograph. There is a pad (substrate bias generator) which is connected to a metal chip on the substrate between pads 16 and 17. This does not go to the external pins. A photograph of this pin is shown in Figure V.G.4.

An input is shown in Figure V.G.5 and the corresponding schematic is shown in Figure V.G.5a. The contact between the diffused resistor and the bond pad is a polysilicon pad. The ground metallization is over the edge of the resistor making a gated diode to substrate. The dielectric breakdown measured on Q3 was 38 volts. The diode to substrate is the n-type resistor to p-type substrate. The clock input has a resistor which measured 425 ohms. The resistors on the other inputs are 2 to 3 times this value as indicated by their physical dimensions. The breakdown voltage for the input transistor junctions and the input resistor to the substrate is 22 volts.

An output circuit is shown in Figure V.G.6 and in the schematic in Figure V.G.7. This is the standard NMOS output circuit. There is no separate protection circuitry.

An input/output circuit is shown in Figure V.G.8 and in the schematic in Figure V.G.9. The circuitry is the same as shown previously however the layout is different.

Microsections were performed to examine the device construction and dimensions. A section through an input polysilicon to resistor connection is shown in Figures V.G.10 and V.G.11. Figure V.G.10 shows the top view and Figure V.G.11 shows the side view. The metallization is approximately 1.0 microns thick, the polysilicon is 0.25 microns thick, and the oxide on either side of the polysilicon is 0.5 microns thick. The microsection was chemically stained and the diffusions were examined. A top view is shown in Figure V.G.12 and a side view is shown in Figure V.G.13. The diffusions are about 0.4 microns deep.

Electrical Testing

Electrical data was taken on each of the stressed parts and the control part at each iteration during the testing. If the parts did not have a leakage failure, the data was not printed except at the initial, +500, +1000, +1500, +2000, +2500, and +3000 volt levels. In addition to the

leakage current information by serial number the average leakage current at each voltage level for each pin was calculated. These data are shown in Figures V.G.14 and V.G.15. Figure V.G.14 is the initial averages and Figure V.G.15 is the averages following the +2250 volt stress.

The readings taken on the Tektronix 3260 ATE were the input current leakage of each pin with respect to VCC and GND which were connected together. The readings were taken at +3 volts (NDV) and +10 volts (NDVR). This provides information on interface circuit damage. One additional measurement should have been made to ensure continuity. The failure mode which developed on the inputs was often opens rather than shorts and this was not easily identifiable in this test.

Functional testing was performed on a Part Type G Educational Computer Board. This was done after each testing sequence. The operations which each chip was asked to perform included; Abort, Help, Memory Set, Memory Display, and Block of Memory Search. This is not a complete functional test but does exercise a good portion of the device.

Charged Device Data Analysis

Fifteen devices, S/N 17-31, were stressed with the charged device ESD simulation model. Serial number 31 was taken through the test and stress sequence until it failed, in order to provide an early indication of the voltage level which would be required. It failed functionally after the -750 volt stress. The remainder of the devices were taken through the testing sequence and failed functionally as follows: -250V S/N 29, +500V S/N 20, 25, 26, 27, 30, -500V S/N 21, 22, 23, 24, 28, +750V S/N 18, -750V S/N 17, 19. Serial number 29 was pulled for failure analysis and the remainder of the parts were left in test to gain further information on input circuit degradation.

The testing was stopped after the +2250 volt stress. Leakage current failures are summarized in Figure V.G.16. This includes the input pins and pins 17 and 18. A few of the other pins failed at voltage levels of 1750 and greater. The output pins were more susceptible than the I/O pins. A printout of the average value of leakage current for each pin is shown in Figure V.G.16a. The leakage current failures do not provide all of the information required to understand the variation in pin sensitivity. The leakage current on pin 10 of serial number 30 is shown in Figure V.G.17. The current is erratic and measures 4 nA after the +2250 volt stress. This pin was electrically open when measured at this time.

Ten devices were electrically measured and the condition of the inputs and of pins 17 and 18 are shown in Figure V.G.17a. The primary failure mode of the inputs is an electrical open condition. The two I/O pins developed excess leakage current.

The variations in circuit layout are shown in Figures V.G.18 through V.G.22. Figure V.G.18 shows the standard input circuit. Figure V.G.19 shows the input configuration used for the clock, pin 15. Figure V.G.20

shows the standard output configuration. Figure V.G.21 shows the standard input/output configuration. Figure V.G.22 shows the configuration used for pins 17 and 18. These outputs have sink transistors but no source transistor. The input is the standard configuration.

All devices were visualy examined and further documentation was performed on serial numbers 20 and 22. Inputs are shown in Figures V.G.23 through V.G.26. Figure V.G.23 shows five inputs on serial number 22 that are all electrically open. Figure V.G.24 shows an open on pin 10 of serial number 22. Figure V.G.25 shows damage on pins 12 and 13. Pin 12 is open and pin 13 is shorted to ground. Figure V.G.26 shows a short on pin 15. Typical output damage is shown for pin 7 on S/N 20 in Figure V.G.27. Damage on pins 17 and 18 occurred on the current sink transistors (Figures V.G.28 and V.G.29). This was junction damage drain to body or drain to source (ground).

These parts were found to have inputs that were sensitive to stress due to damage created in the polysilicon interface between the bond pad and the input resistor. Pin 15 was the most sensitive to stress. This pin had a polysilicon stripe parallel to the protect resistor. This polysilicon was connected to ground and it also went beneath the bond pad metallization. The ground metallization represents a large capacitance and causes this pin to be readily damaged by the charged device model stress.

Two of the I/O pins, 17 and 18, were sensitive to stress. These had fewer contacts than the other I/O pins and the output pins. The more contact area the less sensitive a pin was to stress. This made the output pins the next most sensitive and the remainder of the I/O pins the least sensitive.

Human Body Discharge Data Anaylysis

Fifteen devices, S/N 2 through 16, were stressed with the human body ESD simulation test method. Serial number 2 was taken through the test and stress sequence until it failed. It failed functionally at -1250 volts. The remainder of the devices were taken through the testing sequence and failed functionally as follows: -1250V S/N 13, -2250 S/N 11, 15 and 16, -2500V S/N 14, +2750 S/N 3, 4, 5, 8 and 9, -2750V S/N 7, 10 and 12, +3000V S/N 6. The parts were removed from further stress as they failed. Leakage increases followed a pattern similar to that seen on the charged device models except that pin 15 was not damaged on any of the devices. The configuration with the ground metallization away from the interface polysilicon is not as susceptible as the other inputs to the human body ESD simulation.

Figure V.G.30 shows the leakage currents with the corresponding pin numbers and functions after the -2250 volt stress. Several inputs are leaky and pin 17 is leaky. This was found to be true on other parts as shown in Figure V.G.31. Input pins 10, 12, 13, 21, 23, 24 and 25 showed opens and/or leakage. Input pin 22 which is the same layout as the other 7 inputs did not have apparent damage. It appears that the inputs that are

the closest to output or I/O pins are more susceptible to damage. This makes 10 and 12 the most susceptible, 21 and 25 the next most susceptible and 22, 23 and 24 the least susceptible. This conclusion agrees with the electrical data. Pin 15 was not susceptible to stress. Pin 17 developed leakage current due to the fact that there was only one connection on the sink transistor. Pin 18 had multiple connections to the sink transistor and it was not damaged. The output and other I/O pins also were not damaged.

Photos of the type of damage that occurred is shown in Figures V.G.32 and V.G.33. Figure V.G.32 shows opens on pins 10 and 12. Figure V.G.33 shows slight visible damage on pins 22 and 23.

These devices had above average tolerance to ESD stress. The input configuration used allowed leakage to develop to the ground metallization and opens developed in the polysilicon.

The difference between the two test methods was evident on this device. The reason is that the package capacitance is a large factor for the charged device model and is not a factor for the human body simulation.

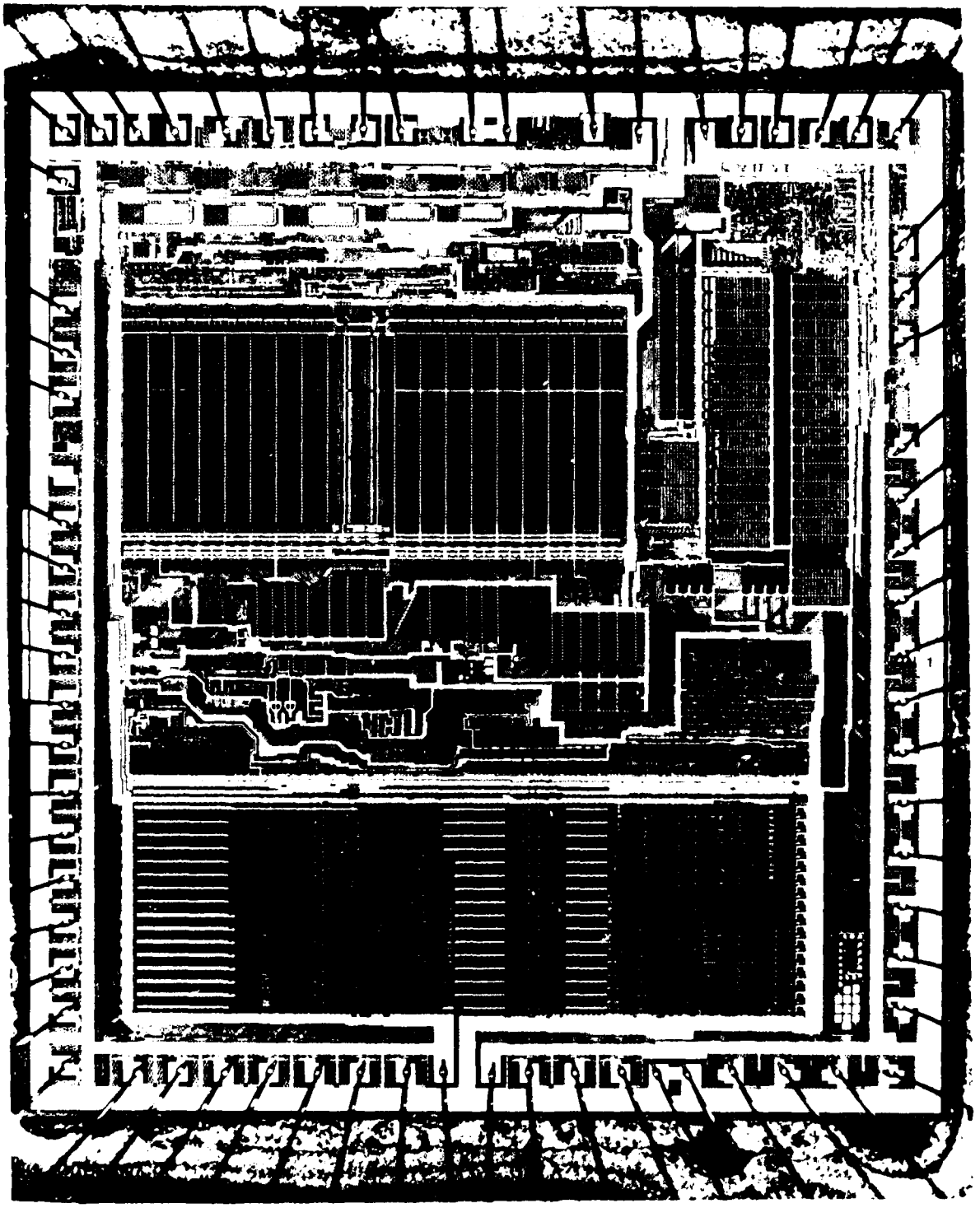


Figure V.G.1 - Overall Die Photograph

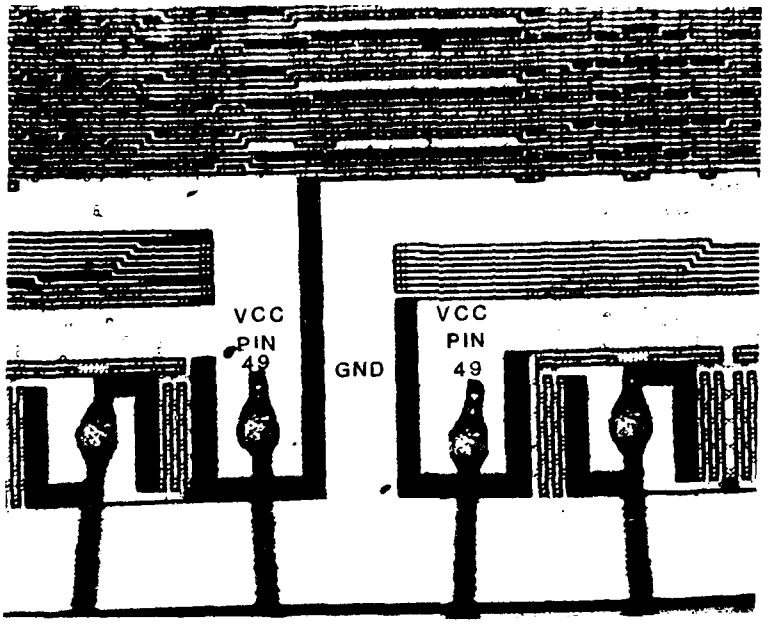


Figure V.G.2 - VCC Bond Pad and GND Metallization

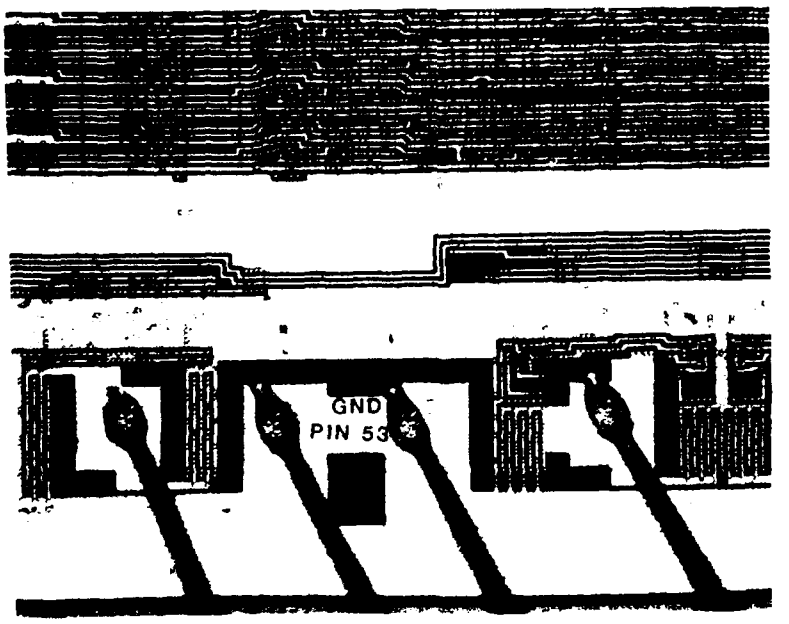


Figure V.G.3 - GND Bond Pad

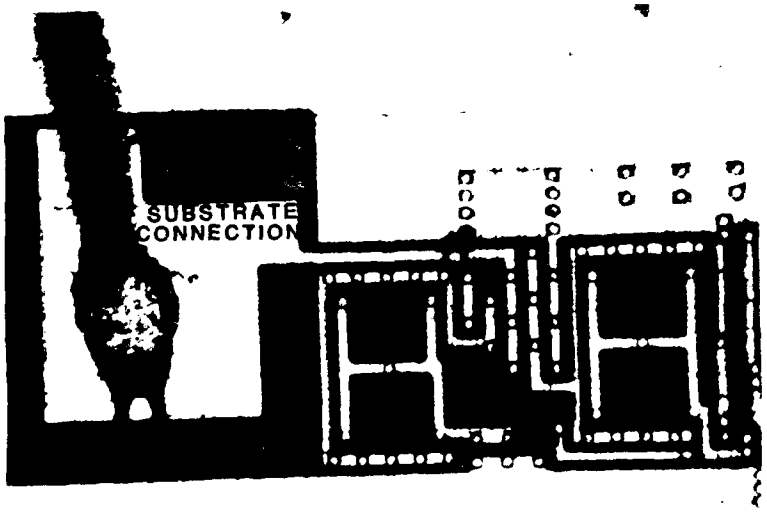


Figure V.G.4 - Substrate Connection

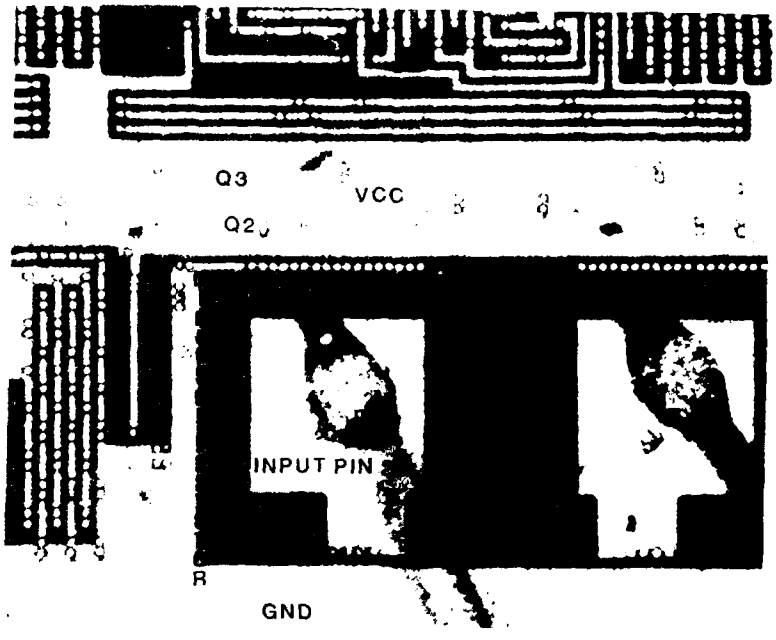


Figure V.G.5 - Pin 21 Input

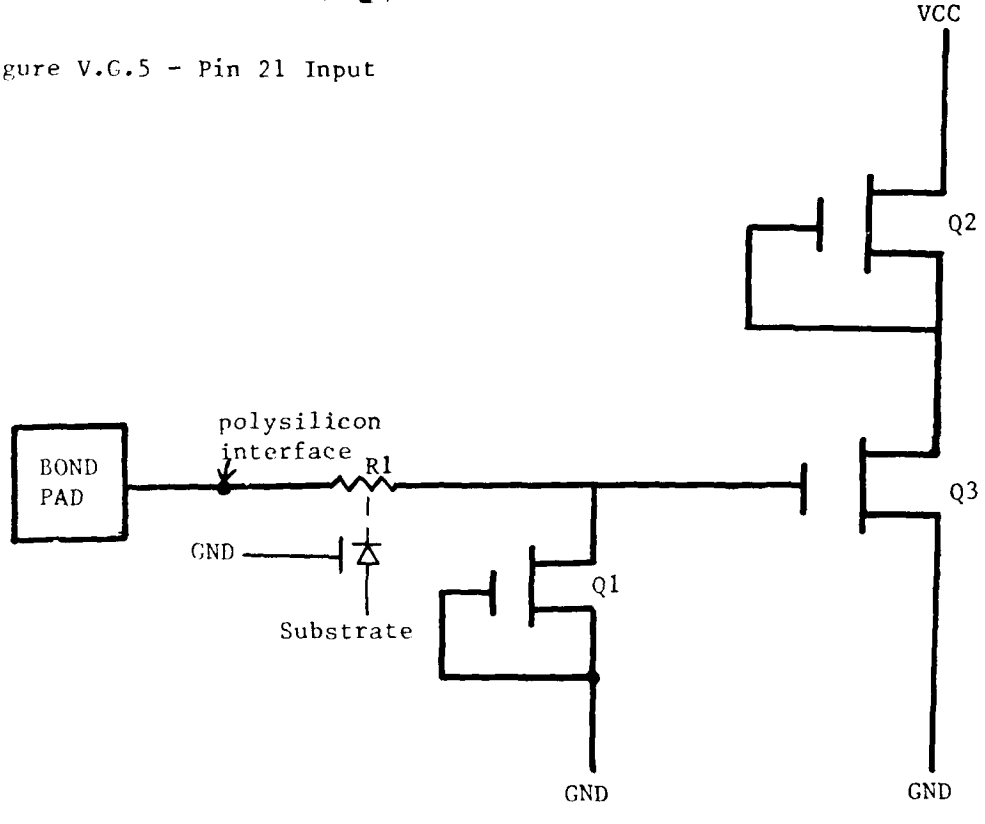


Figure V.G.5a - Input Schematic

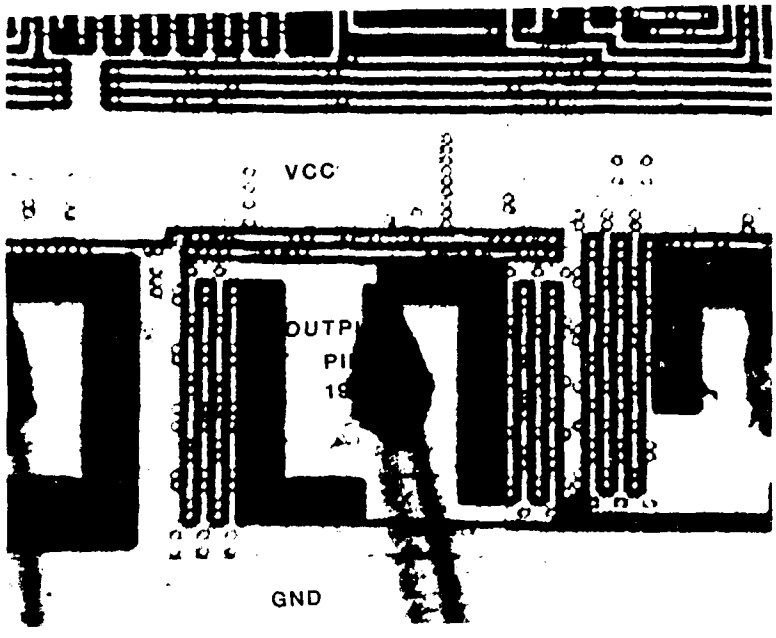


Figure V.G.6 - Pin 19 Output

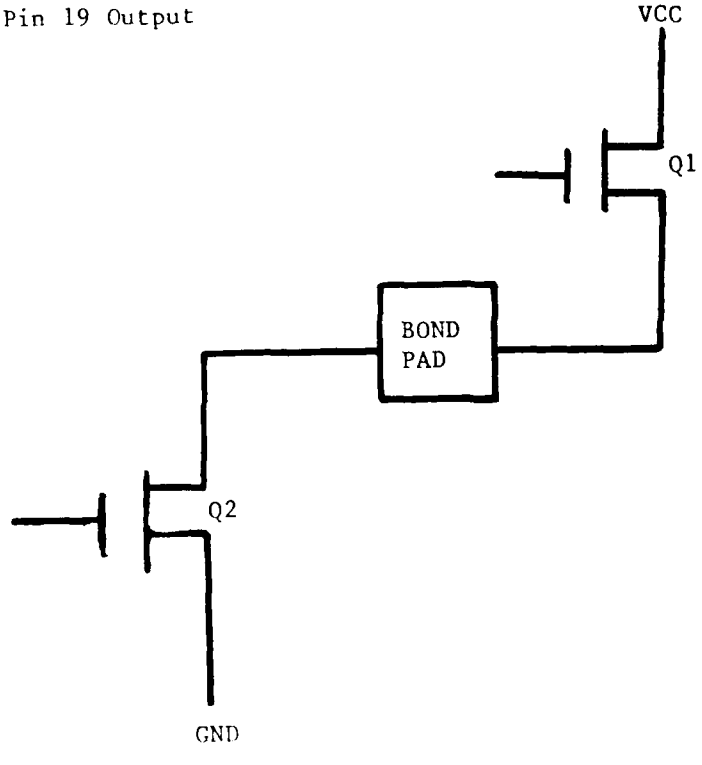


Figure V.G.7 - Output Schematic

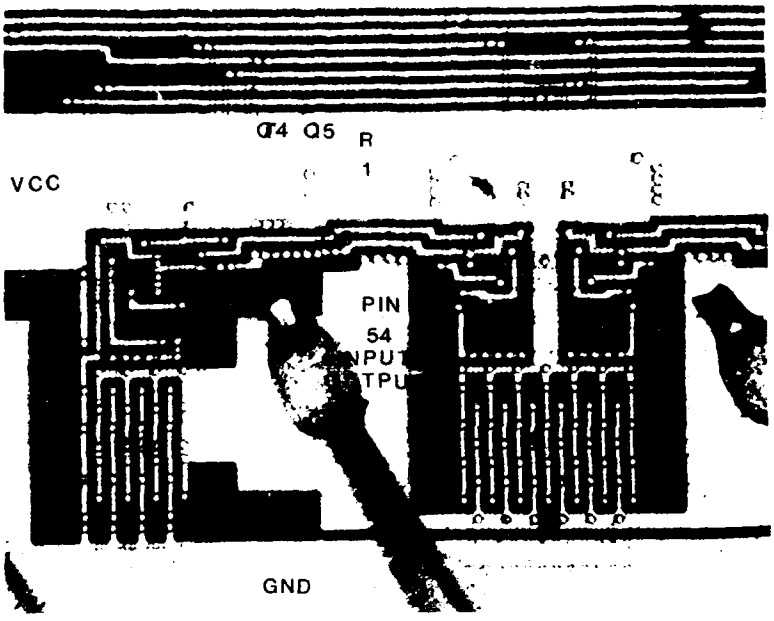


Figure V.C.8 - Pin 54 Input/Output

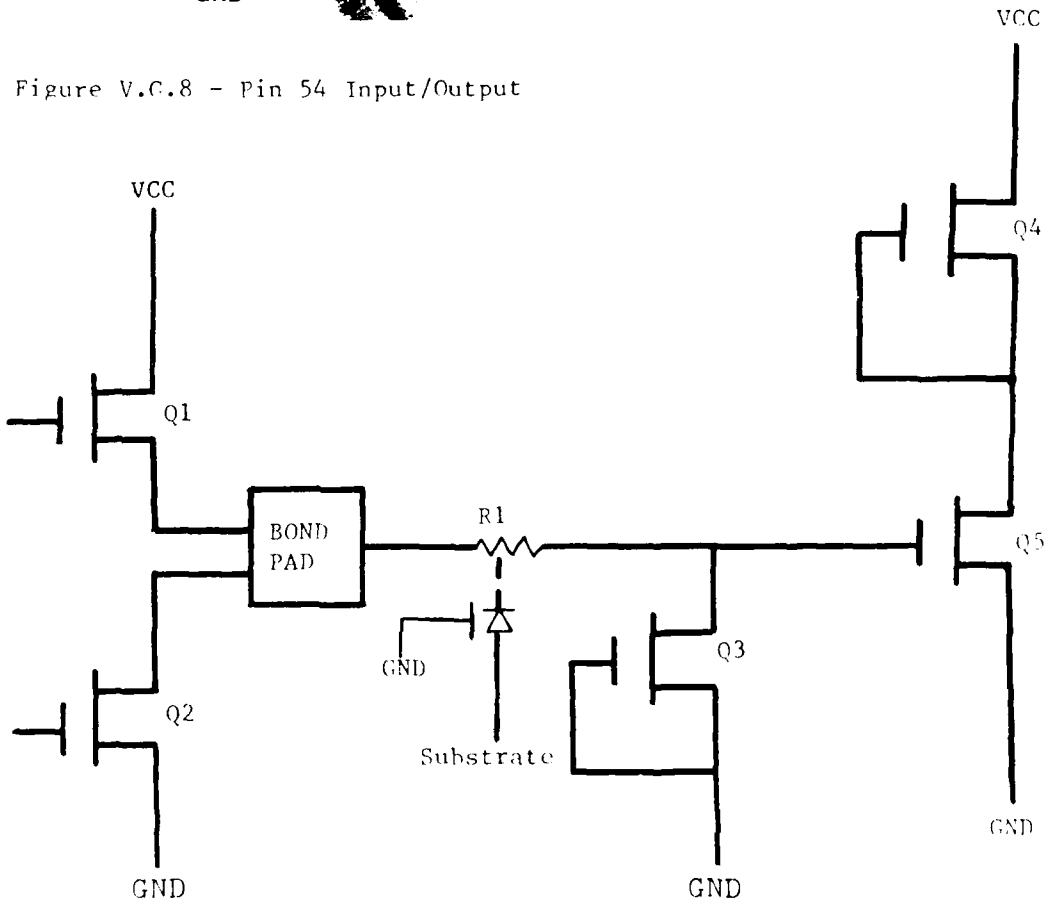
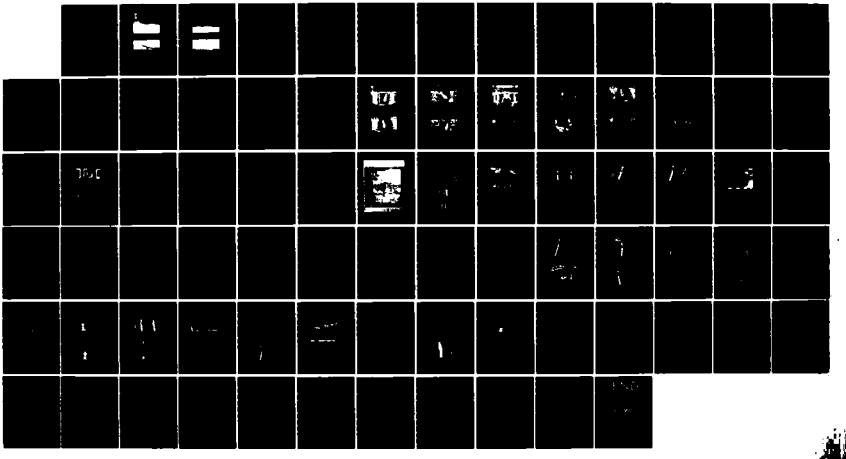
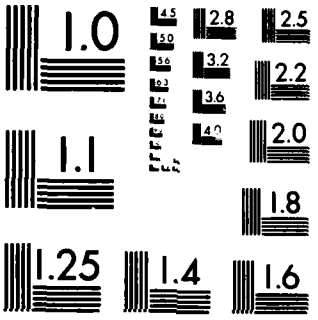


Figure V.C.9 - Input/Output Schematic

AD-A150 333 EOS (ELECTRICAL OVERSTRESS) PROTECTION FOR VLSI (VERY 3/3
LARGE SCALE INTEGRA..(U) MARTIN MARIETTA AEROSPACE
DENVER CO D D WILSON ET AL. SEP 84 MCR-84-506
UNCLASSIFIED RADC-TR-84-183 F30602-82-C-0111 F/G 9/1 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

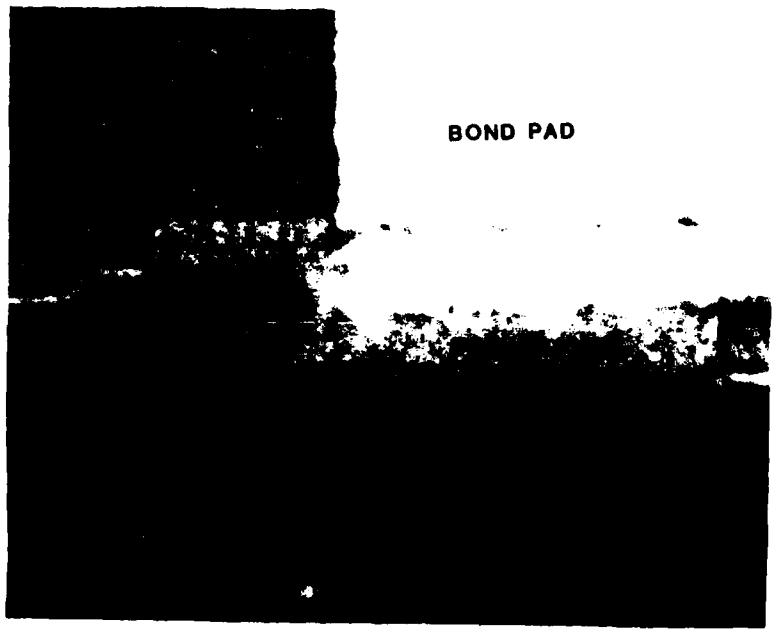


Figure V.G.10 - Top View of Section Through Input

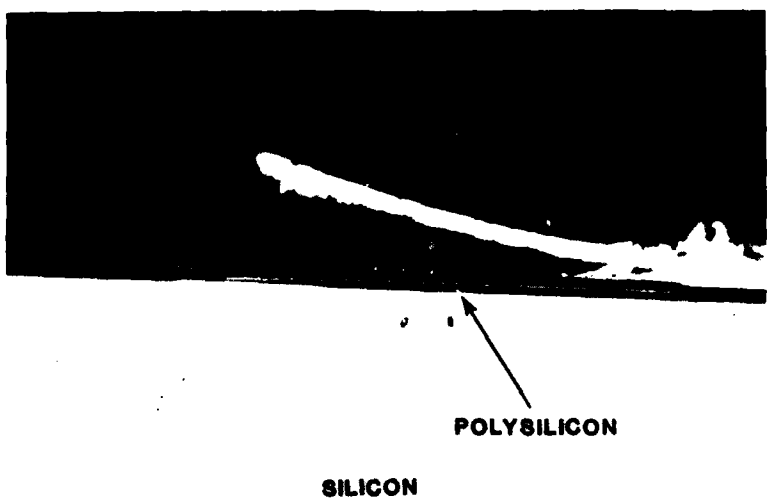


Figure V.G.11 - Side View of Section Through Input

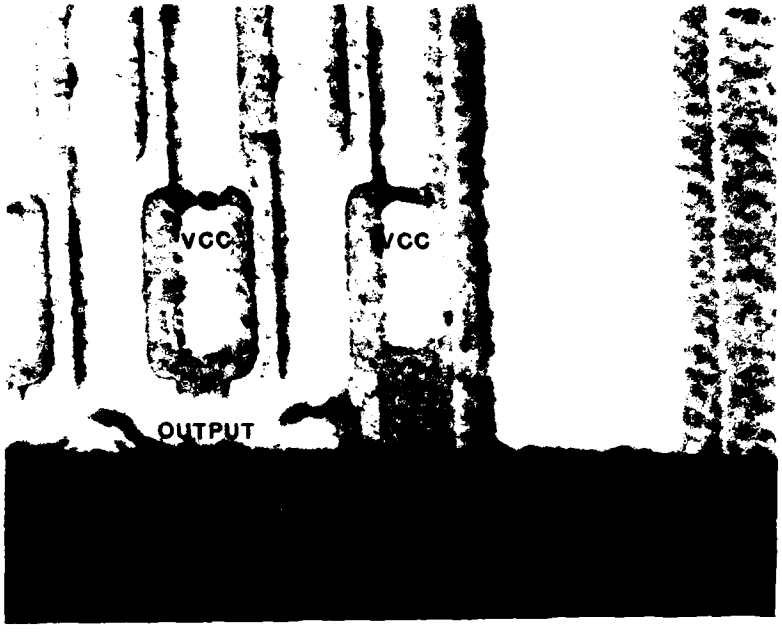


Figure V.G.12 - Top View of Section Through Input

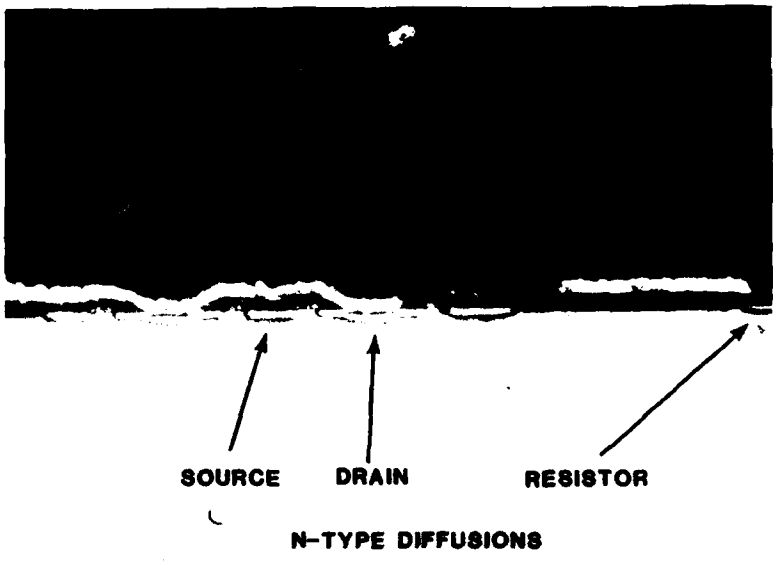


Figure V.G.13 - Side View of Section Through Input

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:22 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,13,14,15,16			
	NDV - - - - - -	903.6PA	--	1.000MA
	NDV - - - - - -	567.9PA	--	1.000MA
	NDV - - - - - -	610.7PA	--	1.000MA
	NDV - - - - - -	503.6PA	--	1.000MA
	NDV - - - - - -	396.4PA	--	1.000MA
	NDV - - - - - -	500.0PA	--	1.000MA
	NDV - - - - - -	432.1PA	--	1.000MA
	NDV - - - - - -	382.1PA	--	1.000MA
	NDV - - - - - -	510.7PA	--	1.000MA
	NDV - - - - - -	2.550NA	--	1.000MA
	NDV - - - - - -	2.854NA	--	1.000MA
	NDV - - - - - -	2.675NA	--	1.000MA
	NDV - - - - - -	4.675NA	--	1.000MA
	NDV - - - - - -	3.607NA	--	1.000MA
	NDV - - - - - -	1.800NA	--	1.000MA
	NDV - - - - - -	3.832NA	--	1.000MA
	NDV - - - - - -	1.825NA	--	1.000MA
	NDV - - - - - -	2.021NA	--	1.000MA
	NDV - - - - - -	3.404NA	--	1.000MA
	NDV - - - - - -	2.793NA	--	1.000MA
	NDV - - - - - -	2.896NA	--	1.000MA
	NDV - - - - - -	2.779NA	--	1.000MA
	NDV - - - - - -	2.907NA	--	1.000MA
	NDV - - - - - -	2.675NA	--	1.000MA
	NDV - - - - - -	2.864NA	--	1.000MA
	NDV - - - - - -	2.754NA	--	1.000MA
	NDV - - - - - -	2.696NA	--	1.000MA
	NDV - - - - - -	2.796NA	--	1.000MA
	NDV - - - - - -	2.711NA	--	1.000MA
	NDV - - - - - -	2.911NA	--	1.000MA
	NDV - - - - - -	2.961NA	--	1.000MA
	NDV - - - - - -	2.761NA	--	1.000MA
	NDV - - - - - -	3.661NA	--	1.000MA
	NDV - - - - - -	3.564NA	--	1.000MA
	NDV - - - - - -	3.621NA	--	1.000MA
	NDV - - - - - -	3.007NA	--	1.000MA
	NDV - - - - - -	3.000NA	--	1.000MA
	NDV - - - - - -	2.511NA	--	1.000MA
	NDV - - - - - -	2.646NA	--	1.000MA
	NDV - - - - - -	2.689NA	--	1.000MA
	NDV - - - - - -	3.257NA	--	1.000MA
	NDV - - - - - -	3.486NA	--	1.000MA
	NDV - - - - - -	639.3PA	--	1.000MA
	NDV - - - - - -	628.6PA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:22 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,13,14,15,16			
	NDV - - - - - -	1.239NA	--	1.000MA
	NDV - - - - - -	1.471NA	--	1.000MA
	NDV - - - - - -	1.500NA	--	1.000MA
	NDV - - - - - -	1.461NA	--	1.000MA
	NDV - - - - - -	1.554NA	--	1.000MA
	NDV - - - - - -	1.389NA	--	1.000MA
	NDV - - - - - -	1.575NA	--	1.000MA
	NDV - - - - - -	1.357NA	--	1.000MA
	NDV - - - - - -	1.421NA	--	1.000MA
	NDV - - - - - -	1.354NA	--	1.000MA
	NDV - - - - - -	1.346NA	--	1.000MA
	NDV - - - - - -	1.318NA	--	1.000MA
	NDV - - - - - -	1.207NA	--	1.000MA
	NDV - - - - - -	1.393NA	--	1.000MA
	NDV - - - - - -	1.193NA	--	1.000MA
	NDV - - - - - -	1.321NA	--	1.000MA
	NDVR - - - - - -	2.879NA	--	1.000MA
	NDVR - - - - - -	2.175NA	--	1.000MA
	NDVR - - - - - -	2.057NA	--	1.000MA
	NDVR - - - - - -	1.804NA	--	1.000MA
	NDVR - - - - - -	1.775NA	--	1.000MA
	NDVR - - - - - -	1.729NA	--	1.000MA
	NDVR - - - - - -	2.039NA	--	1.000MA
	NDVR - - - - - -	1.900NA	--	1.000MA
	NDVR - - - - - -	1.832NA	--	1.000MA
	NDVR - - - - - -	1.335UA	--	1.000MA
	NDVR - - - - - -	1.844UA	--	1.000MA
	NDVR - - - - - -	1.584UA	--	1.000MA
	NDVR - - - - - -	14.57UA	--	1.000MA
	NDVR - - - - - -	10.99UA	--	1.000MA
	NDVR - - - - - -	2.330UA	--	1.000MA
	NDVR - - - - - -	16.10UA	--	1.000MA
	NDVR - - - - - -	2.198UA	--	1.000MA
	NDVR - - - - - -	2.353UA	--	1.000MA
	NDVR - - - - - -	10.62UA	--	1.000MA
	NDVR - - - - - -	1.952UA	--	1.000MA
	NDVR - - - - - -	1.865UA	--	1.000MA
	NDVR - - - - - -	1.534UA	--	1.000MA
	NDVR - - - - - -	1.503UA	--	1.000MA
	NDVR - - - - - -	1.548UA	--	1.000MA
	NDVR - - - - - -	1.381UA	--	1.000MA
	NDVR - - - - - -	1.129UA	--	1.000MA
	NDVR - - - - - -	1.273UA	--	1.000MA
	NDVR - - - - - -	1.418UA	--	1.000MA
	NDVR - - - - - -	1.788UA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:22 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,13,14,15,16				
	NDVR - - - - - -	2.040UA	--	1.000MA
	NDVR - - - - - -	2.199UA	--	1.000MA
	NDVR - - - - - -	1.583UA	--	1.000MA
	NDVR - - - - - -	14.33UA	--	1.000MA
	NDVR - - - - - -	14.42UA	--	1.000MA
	NDVR - - - - - -	17.28UA	--	1.000MA
	NDVR - - - - - -	5.111UA	--	1.000MA
	NDVR - - - - - -	5.378UA	--	1.000MA
	NDVR - - - - - -	3.169UA	--	1.000MA
	NDVR - - - - - -	2.726UA	--	1.000MA
	NDVR - - - - - -	2.535UA	--	1.000MA
	NDVR - - - - - -	9.574UA	--	1.000MA
	NDVR - - - - - -	15.24UA	--	1.000MA
	NDVR - - - - - -	7.146NA	--	1.000MA
	NDVR - - - - - -	3.064NA	--	1.000MA
	NDVR - - - - - -	11.56NA	--	1.000MA
	NDVR - - - - - -	11.59NA	--	1.000MA
	NDVR - - - - - -	11.75NA	--	1.000MA
	NDVR - - - - - -	11.60NA	--	1.000MA
	NDVR - - - - - -	12.50NA	--	1.000MA
	NDVR - - - - - -	12.10NA	--	1.000MA
	NDVR - - - - - -	11.50NA	--	1.000MA
	NDVR - - - - - -	11.23NA	--	1.000MA
	NDVR - - - - - -	10.81NA	--	1.000MA
	NDVR - - - - - -	11.32NA	--	1.000MA
	NDVR - - - - - -	11.68NA	--	1.000MA
	NDVR - - - - - -	11.41NA	--	1.000MA
	NDVR - - - - - -	14.93NA	--	1.000MA
	NDVR - - - - - -	14.02NA	--	1.000MA
	NDVR - - - - - -	15.72NA	--	1.000MA
	NDVR - - - - - -	14.61NA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:31 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,29,30			
	NDV - - - - - -	832.1PA	--	1.000MA
	NDV - - - - - -	678.6PA	--	1.000MA
	NDV - - - - - -	500.0PA	--	1.000MA
	NDV - - - - - -	482.1PA	--	1.000MA
	NDV - - - - - -	517.9PA	--	1.000MA
	NDV - - - - - -	382.1PA	--	1.000MA
	NDV - - - - - -	489.3PA	--	1.000MA
	NDV - - - - - -	475.0PA	--	1.000MA
	NDV - - - - - -	375.0PA	--	1.000MA
	NDV - - - - - -	3.379NA	--	1.000MA
	NDV - - - - - -	3.111NA	--	1.000MA
	NDV - - - - - -	3.011NA	--	1.000MA
	NDV - - - - - -	4.386NA	--	1.000MA
	NDV - - - - - -	2.971NA	--	1.000MA
	NDV - - - - - -	1.946NA	--	1.000MA
	NDV - - - - - -	4.143NA	--	1.000MA
	NDV - - - - - -	1.954NA	--	1.000MA
	NDV - - - - - -	1.839NA	--	1.000MA
	NDV - - - - - -	3.768NA	--	1.000MA
	NDV - - - - - -	3.896NA	--	1.000MA
	NDV - - - - - -	4.371NA	--	1.000MA
	NDV - - - - - -	4.854NA	--	1.000MA
	NDV - - - - - -	4.836NA	--	1.000MA
	NDV - - - - - -	4.807NA	--	1.000MA
	NDV - - - - - -	4.900NA	--	1.000MA
	NDV - - - - - -	5.507NA	--	1.000MA
	NDV - - - - - -	5.436NA	--	1.000MA
	NDV - - - - - -	4.711NA	--	1.000MA
	NDV - - - - - -	5.179NA	--	1.000MA
	NDV - - - - - -	5.921NA	--	1.000MA
	NDV - - - - - -	6.768NA	--	1.000MA
	NDV - - - - - -	5.443NA	--	1.000MA
	NDV - - - - - -	6.132NA	--	1.000MA
	NDV - - - - - -	4.446NA	--	1.000MA
	NDV - - - - - -	3.979NA	--	1.000MA
	NDV - - - - - -	3.507NA	--	1.000MA
	NDV - - - - - -	2.839NA	--	1.000MA
	NDV - - - - - -	2.386NA	--	1.000MA
	NDV - - - - - -	2.186NA	--	1.000MA
	NDV - - - - - -	2.725NA	--	1.000MA
	NDV - - - - - -	3.911NA	--	1.000MA
	NDV - - - - - -	3.768NA	--	1.000MA
	NDV - - - - - -	1.189NA	--	1.000MA
	NDV - - - - - -	407.1PA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:31 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,29,30			
	NDV - - - - - -	1.300NA	--	1.000MA
	NDV - - - - - -	1.236NA	--	1.000MA
	NDV - - - - - -	18.79NA	--	1.000MA
	NDV - - - - - -	8.393NA	--	1.000MA
	NDV - - - - - -	1.311NA	--	1.000MA
	NDV - - - - - -	1.461NA	--	1.000MA
	NDV - - - - - -	1.207NA	--	1.000MA
	NDV - - - - - -	1.439NA	--	1.000MA
	NDV - - - - - -	1.189NA	--	1.000MA
	NDV - - - - - -	1.311NA	--	1.000MA
	NDV - - - - - -	1.332NA	--	1.000MA
	NDV - - - - - -	1.054NA	--	1.000MA
	NDV - - - - - -	1.339NA	--	1.000MA
	NDV - - - - - -	1.064NA	--	1.000MA
	NDV - - - - - -	1.325NA	--	1.000MA
	NDV - - - - - -	1.111NA	--	1.000MA
	NDVR - - - - - -	2.957NA	--	1.000MA
	NDVR - - - - - -	2.121NA	--	1.000MA
	NDVR - - - - - -	1.768NA	--	1.000MA
	NDVR - - - - - -	1.764NA	--	1.000MA
	NDVR - - - - - -	1.611NA	--	1.000MA
	NDVR - - - - - -	1.450NA	--	1.000MA
	NDVR - - - - - -	1.614NA	--	1.000MA
	NDVR - - - - - -	1.446NA	--	1.000MA
	NDVR - - - - - -	1.418NA	--	1.000MA
	NDVR - - - - - -	47.42UA	--	1.000MA
	NDVR - - - - - -	39.81UA	--	1.000MA
	NDVR - - - - - -	31.70UA	--	1.000MA
	NDVR - - - - - -	28.98UA	--	1.000MA
	NDVR - - - - - -	11.51UA	--	1.000MA
	NDVR - - - - - -	2.710UA	--	1.000MA
	NDVR - - - - - -	16.84UA	--	1.000MA
	NDVR - - - - - -	2.035UA	--	1.000MA
	NDVR - - - - - -	1.775UA	--	1.000MA
	NDVR - - - - - -	10.14UA	--	1.000MA
	NDVR - - - - - -	64.59UA	--	1.000MA
	NDVR - - - - - -	76.56UA	--	1.000MA
	NDVR - - - - - -	77.73UA	--	1.000MA
	NDVR - - - - - -	78.36UA	--	1.000MA
	NDVR - - - - - -	78.32UA	--	1.000MA
	NDVR - - - - - -	79.00UA	--	1.000MA
	NDVR - - - - - -	79.12UA	--	1.000MA
	NDVR - - - - - -	79.79UA	--	1.000MA
	NDVR - - - - - -	80.65UA	--	1.000MA
	NDVR - - - - - -	82.15UA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:31 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,29,30			
	NDVR - - - - - -	85.53UA	--	1.000MA
	NDVR - - - - - -	97.66UA	--	1.000MA
	NDVR - - - - - -	110.6UA	--	1.000MA
	NDVR - - - - - -	105.4UA	--	1.000MA
	NDVR - - - - - -	68.00UA	--	1.000MA
	NDVR - - - - - -	52.20UA	--	1.000MA
	NDVR - - - - - -	28.10UA	--	1.000MA
	NDVR - - - - - -	19.61UA	--	1.000MA
	NDVR - - - - - -	4.500UA	--	1.000MA
	NDVR - - - - - -	2.895UA	--	1.000MA
	NDVR - - - - - -	5.966UA	--	1.000MA
	NDVR - - - - - -	32.39UA	--	1.000MA
	NDVR - - - - - -	30.86UA	--	1.000MA
	NDVR - - - - - -	24.82NA	--	1.000MA
	NDVR - - - - - -	2.082NA	--	1.000MA
	NDVR - - - - - -	11.85NA	--	1.000MA
	NDVR - - - - - -	11.40NA	--	1.000MA
	NDVR - - - - - -	55.04NA	--	1.000MA
	NDVR - - - - - -	32.25NA	--	1.000MA
	NDVR - - - - - -	12.95NA	--	1.000MA
	NDVR - - - - - -	11.80NA	--	1.000MA
	NDVR - - - - - -	11.79NA	--	1.000MA
	NDVR - - - - - -	12.55NA	--	1.000MA
	NDVR - - - - - -	12.52NA	--	1.000MA
	NDVR - - - - - -	14.04NA	--	1.000MA
	NDVR - - - - - -	13.80NA	--	1.000MA
	NDVR - - - - - -	13.89NA	--	1.000MA
	NDVR - - - - - -	22.86NA	--	1.000MA
	NDVR - - - - - -	22.99NA	--	1.000MA
	NDVR - - - - - -	21.66NA	--	1.000MA
	NDVR - - - - - -	19.01NA	--	1.000MA

Figure V.G.14 - Average Leakage Current at Initial Electrical Test (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:51 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,14,15,16				
	NDV - - - - - -	2.588NA	--	1.000MA
	NDV - - - - - -	8.478UA	--	1.000MA
	NDV - - - - - -	12.81NA	--	1.000MA
	NDV - - - - - -	43.68UA	--	1.000MA
	NDV - - - - - -	12.79UA	--	1.000MA
	NDV - - - - - -	86.36UA	--	1.000MA
	NDV - - - - - -	23.47NA	--	1.000MA
	NDV - - - - - -	19.04NA	--	1.000MA
	NDV - - - - - -	8.231NA	--	1.000MA
	NDV - - - - - -	3.538NA	--	1.000MA
	NDV - - - - - -	3.958NA	--	1.000MA
	NDV - - - - - -	3.585NA	--	1.000MA
	NDV - - - - - -	5.823NA	--	1.000MA
	NDV - - - - - -	4.658NA	--	1.000MA
	NDV - - - - - -	2.681NA	--	1.000MA
	NDV - - - - - -	57.38NA	--	1.000MA
	NDV - - - - - -	2.731NA	--	1.000MA
	NDV - - - - - -	2.819NA	--	1.000MA
	NDV - - - - - -	20.13NA	--	1.000MA
	NDV - - - - - -	3.650NA	--	1.000MA
	NDV - - - - - -	3.750NA	--	1.000MA
	NDV - - - - - -	3.642NA	--	1.000MA
	NDV - - - - - -	3.662NA	--	1.000MA
	NDV - - - - - -	3.538NA	--	1.000MA
	NDV - - - - - -	3.650NA	--	1.000MA
	NDV - - - - - -	3.608NA	--	1.000MA
	NDV - - - - - -	3.477NA	--	1.000MA
	NDV - - - - - -	3.581NA	--	1.000MA
	NDV - - - - - -	3.542NA	--	1.000MA
	NDV - - - - - -	3.650NA	--	1.000MA
	NDV - - - - - -	3.788NA	--	1.000MA
	NDV - - - - - -	3.508NA	--	1.000MA
	NDV - - - - - -	4.558NA	--	1.000MA
	NDV - - - - - -	4.404NA	--	1.000MA
	NDV - - - - - -	4.488NA	--	1.000MA
	NDV - - - - - -	3.885NA	--	1.000MA
	NDV - - - - - -	3.785NA	--	1.000MA
	NDV - - - - - -	3.354NA	--	1.000MA
	NDV - - - - - -	3.423NA	--	1.000MA
	NDV - - - - - -	3.535NA	--	1.000MA
	NDV - - - - - -	3.900NA	--	1.000MA
	NDV - - - - - -	4.227NA	--	1.000MA
	NDV - - - - - -	1.442NA	--	1.000MA
	NDV - - - - - -	29.84UA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:51 WITH THE 3260 TEST SYSTEM

AIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,14,15,16			
	NDV	2.100NA	--	1.000MA
	NDV	2.015NA	--	1.000MA
	NDV	2.415NA	--	1.000MA
	NDV	2.696NA	--	1.000MA
	NDV	2.392NA	--	1.000MA
	NDV	2.008NA	--	1.000MA
	NDV	2.219NA	--	1.000MA
	NDV	2.219NA	--	1.000MA
	NDV	2.000NA	--	1.000MA
	NDV	2.281NA	--	1.000MA
	NDV	1.946NA	--	1.000MA
	NDV	2.181NA	--	1.000MA
	NDV	2.000NA	--	1.000MA
	NDV	2.100NA	--	1.000MA
	NDV	2.085NA	--	1.000MA
	NDV	1.946NA	--	1.000MA
	NDVR	14.00NA	--	1.000MA
	NDVR	12.98UA	--	1.000MA
	NDVR	42.75NA	--	1.000MA
	NDVR	90.68UA	--	1.000MA
	NDVR	28.88UA	--	1.000MA
	NDVR	173.9UA	--	1.000MA
	NDVR	80.75NA	--	1.000MA
	NDVR	65.75NA	--	1.000MA
	NDVR	30.21NA	--	1.000MA
	NDVR	967.9NA	--	1.000MA
	NDVR	1.298UA	--	1.000MA
	NDVR	1.133UA	--	1.000MA
	NDVR	8.275UA	--	1.000MA
	NDVR	6.442UA	--	1.000MA
	NDVR	1.377UA	--	1.000MA
	NDVR	15.70UA	--	1.000MA
	NDVR	1.306UA	--	1.000MA
	NDVR	1.402UA	--	1.000MA
	NDVR	6.201UA	--	1.000MA
	NDVR	1.358UA	--	1.000MA
	NDVR	1.302UA	--	1.000MA
	NDVR	1.088UA	--	1.000MA
	NDVR	1.055UA	--	1.000MA
	NDVR	1.096UA	--	1.000MA
	NDVR	990.1NA	--	1.000MA
	NDVR	820.5NA	--	1.000MA
	NDVR	913.0NA	--	1.000MA
	NDVR	1.016UA	--	1.000MA
	NDVR	1.240UA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:51 WITH THE 3260 TEST SYSTEM

AIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,14,15,16				
	NDVR	- - - - - -	1.404UA	--	1.000MA
	NDVR	- - - - - -	1.513UA	--	1.000MA
	NDVR	- - - - - -	1.109UA	--	1.000MA
	NDVR	- - - - - -	8.070UA	--	1.000MA
	NDVR	- - - - - -	7.990UA	--	1.000MA
	NDVR	- - - - - -	9.553UA	--	1.000MA
	NDVR	- - - - - -	3.166UA	--	1.000MA
	NDVR	- - - - - -	3.270UA	--	1.000MA
	NDVR	- - - - - -	1.994UA	--	1.000MA
	NDVR	- - - - - -	1.760UA	--	1.000MA
	NDVR	- - - - - -	1.665UA	--	1.000MA
	NDVR	- - - - - -	5.417UA	--	1.000MA
	NDVR	- - - - - -	8.791UA	--	1.000MA
	NDVR	- - - - - -	9.377NA	--	1.000MA
	NDVR	- - - - - -	160.3UA	--	1.000MA
	NDVR	- - - - - -	12.23NA	--	1.000MA
	NDVR	- - - - - -	12.09NA	--	1.000MA
	NDVR	- - - - - -	12.15NA	--	1.000MA
	NDVR	- - - - - -	14.03NA	--	1.000MA
	NDVR	- - - - - -	12.48NA	--	1.000MA
	NDVR	- - - - - -	11.97NA	--	1.000MA
	NDVR	- - - - - -	12.38NA	--	1.000MA
	NDVR	- - - - - -	11.99NA	--	1.000MA
	NDVR	- - - - - -	11.88NA	--	1.000MA
	NDVR	- - - - - -	11.92NA	--	1.000MA
	NDVR	- - - - - -	12.18NA	--	1.000MA
	NDVR	- - - - - -	11.98NA	--	1.000MA
	NDVR	- - - - - -	14.91NA	--	1.000MA
	NDVR	- - - - - -	14.09NA	--	1.000MA
	NDVR	- - - - - -	15.03NA	--	1.000MA
	NDVR	- - - - - -	14.45NA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:58 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,30			
	NDV - - - - - -	629.8UA	--	1.000MA
	NDV - - - - - -	240.2UA	--	1.000MA
	NDV - - - - - -	26.20UA	--	1.000MA
	NDV - - - - - -	234.2UA	--	1.000MA
	NDV - - - - - -	106.8UA	--	1.000MA
	NDV - - - - - -	236.2UA	--	1.000MA
	NDV - - - - - -	226.6UA	--	1.000MA
	NDV - - - - - -	349.0UA	--	1.000MA
	NDV - - - - - -	113.0UA	--	1.000MA
	NDV - - - - - -	5.277NA	--	1.000MA
	NDV - - - - - -	4.181NA	--	1.000MA
	NDV - - - - - -	78.73UA	--	1.000MA
	NDV - - - - - -	4.592NA	--	1.000MA
	NDV - - - - - -	238.9UA	--	1.000MA
	NDV - - - - - -	167.7UA	--	1.000MA
	NDV - - - - - -	479.1UA	--	1.000MA
	NDV - - - - - -	472.4UA	--	1.000MA
	NDV - - - - - -	157.5UA	--	1.000MA
	NDV - - - - - -	159.5UA	--	1.000MA
	NDV - - - - - -	4.138NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	5.484NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	6.435NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	6.165NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	5.484NA	--	1.000MA
	NDV - - - - - -	5.454NA	--	1.000MA
	NDV - - - - - -	6.769NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	6.523NA	--	1.000MA
	NDV - - - - - -	6.677NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	4.815NA	--	1.000MA
	NDV - - - - - -	5.812NA	--	1.000MA
	NDV - - - - - -	78.74UA	--	1.000MA
	NDV - - - - - -	157.5UA	--	1.000MA
	NDV - - - - - -	128.4NA	--	1.000MA
	NDV - - - - - -	2.992NA	--	1.000MA
	NDV - - - - - -	157.5UA	--	1.000MA
	NDV - - - - - -	4.627NA	--	1.000MA
	NDV - - - - - -	934.5UA	--	1.000MA
	NDV - - - - - -	689.9UA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:58 WITH THE 3260 TEST SYSTEM

AIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,30				
	NDV - - - - - -	78.73UA	--	1.000MA
	NDV - - - - - -	66.61NA	--	1.000MA
	NDV - - - - - -	78.75UA	--	1.000MA
	NDV - - - - - -	9.919NA	--	1.000MA
	NDV - - - - - -	9.335NA	--	1.000MA
	NDV - - - - - -	4.569NA	--	1.000MA
	NDV - - - - - -	78.73UA	--	1.000MA
	NDV - - - - - -	6.100NA	--	1.000MA
	NDV - - - - - -	1.942NA	--	1.000MA
	NDV - - - - - -	1.846NA	--	1.000MA
	NDV - - - - - -	1.973NA	--	1.000MA
	NDV - - - - - -	1.669NA	--	1.000MA
	NDV - - - - - -	3.031NA	--	1.000MA
	NDV - - - - - -	1.819NA	--	1.000MA
	NDV - - - - - -	5.681NA	--	1.000MA
	NDV - - - - - -	3.204NA	--	1.000MA
	NDVR - - - - - -	629.8UA	--	1.000MA
	NDVR - - - - - -	315.0UA	--	1.000MA
	NDVR - - - - - -	78.76UA	--	1.000MA
	NDVR - - - - - -	314.9UA	--	1.000MA
	NDVR - - - - - -	157.5UA	--	1.000MA
	NDVR - - - - - -	236.2UA	--	1.000MA
	NDVR - - - - - -	314.9UA	--	1.000MA
	NDVR - - - - - -	393.7UA	--	1.000MA
	NDVR - - - - - -	157.5UA	--	1.000MA
	NDVR - - - - - -	25.95UA	--	1.000MA
	NDVR - - - - - -	20.57UA	--	1.000MA
	NDVR - - - - - -	95.63UA	--	1.000MA
	NDVR - - - - - -	13.93UA	--	1.000MA
	NDVR - - - - - -	317.4UA	--	1.000MA
	NDVR - - - - - -	318.2UA	--	1.000MA
	NDVR - - - - - -	567.3UA	--	1.000MA
	NDVR - - - - - -	473.3UA	--	1.000MA
	NDVR - - - - - -	158.2UA	--	1.000MA
	NDVR - - - - - -	240.0UA	--	1.000MA
	NDVR - - - - - -	37.23UA	--	1.000MA
	NDVR - - - - - -	130.3UA	--	1.000MA
	NDVR - - - - - -	57.99UA	--	1.000MA
	NDVR - - - - - -	142.0UA	--	1.000MA
	NDVR - - - - - -	61.85UA	--	1.000MA
	NDVR - - - - - -	144.6UA	--	1.000MA
	NDVR - - - - - -	76.03UA	--	1.000MA
	NDVR - - - - - -	159.4UA	--	1.000MA
	NDVR - - - - - -	60.96UA	--	1.000MA
	NDVR - - - - - -	66.45UA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress (Cont.)

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2250V STRESS
ON 10 DEC 83 AT 12:58 WITH THE 3260 TEST SYSTEM

AIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	LIMITS MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,30				
	NDVR - - - - - -	84.91UA	--	1.000MA
	NDVR - - - - - -	170.5UA	--	1.000MA
	NDVR - - - - - -	94.95UA	--	1.000MA
	NDVR - - - - - -	84.49UA	--	1.000MA
	NDVR - - - - - -	115.5UA	--	1.000MA
	NDVR - - - - - -	27.36UA	--	1.000MA
	NDVR - - - - - -	14.18UA	--	1.000MA
	NDVR - - - - - -	88.41UA	--	1.000MA
	NDVR - - - - - -	159.5UA	--	1.000MA
	NDVR - - - - - -	158.7UA	--	1.000MA
	NDVR - - - - - -	3.102UA	--	1.000MA
	NDVR - - - - - -	174.8UA	--	1.000MA
	NDVR - - - - - -	16.56UA	--	1.000MA
	NDVR - - - - - -	944.8UA	--	1.000MA
	NDVR - - - - - -	866.0UA	--	1.000MA
	NDVR - - - - - -	78.76UA	--	1.000MA
	NDVR - - - - - -	78.75UA	--	1.000MA
	NDVR - - - - - -	78.77UA	--	1.000MA
	NDVR - - - - - -	53.63NA	--	1.000MA
	NDVR - - - - - -	102.4NA	--	1.000MA
	NDVR - - - - - -	83.13NA	--	1.000MA
	NDVR - - - - - -	78.79UA	--	1.000MA
	NDVR - - - - - -	291.8NA	--	1.000MA
	NDVR - - - - - -	17.82NA	--	1.000MA
	NDVR - - - - - -	25.51NA	--	1.000MA
	NDVR - - - - - -	17.59NA	--	1.000MA
	NDVR - - - - - -	16.93NA	--	1.000MA
	NDVR - - - - - -	55.55NA	--	1.000MA
	NDVR - - - - - -	26.62NA	--	1.000MA
	NDVR - - - - - -	86.17NA	--	1.000MA
	NDVR - - - - - -	35.28NA	--	1.000MA

Figure V.G.15 - Average Leakage Current after +2250 Volt Stress (Cont.)

Number of Failures at Pin Locations

10	12	13	15	17	18	21	22	23	24	25	Voltage
			13			1					+750
1				5							-750
	1			12						1	+1000
							1				-1000
		1		13		3			1		+1250
					1	5	3				-1250
					3						+1500
2					8	6					-1500
					10						+1750
					12						-1750
		2					5	1	3		+2000
	2	3									-2000
2	2	4	13	13	12	6	5	1	3	1	+2250

Figure V.G.16 - CD Stress, Cumulative Leakage Failures

(Total of 13 parts)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C N750V STRESS
ON 17 NOV 83 AT 08:27 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE		LIMITS MINIMUM	MAXIMUM
		PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,30				
			PIN		FUNCTION	
****	NDV	- - - - - - -	15	1.024mA	INPUT	-- 1.000mA
	NDV	- - - - - - -	22	1.735NA		-- 1.000mA
	NDV	- - - - - - -	25	9.507UA		-- 1.000mA
	NDV	- - - - - - -	24	1.319UA		-- 1.000mA
	NDV	- - - - - - -	23	19.10NA		-- 1.000mA
	NDV	- - - - - - -	13	3.123NA		-- 1.000mA
	NDV	- - - - - - -	12	44.29NA		-- 1.000mA
	NDV	- - - - - - -	21	609.3UA		-- 1.000mA
	NDV	- - - - - - -	10	78.74UA		-- 1.000mA
	NDV	- - - - - - -	28	3.219NA	INPUT	-- 1.000mA
	NDV	- - - - - - -	27	3.058NA	OUTPUT	-- 1.000mA
	NDV	- - - - - - -	26	2.727NA		-- 1.000mA
	NDV	- - - - - - -	20	4.012NA		-- 1.000mA
	NDV	- - - - - - -	19	2.746NA		-- 1.000mA
	NDV	- - - - - - -	6	1.738NA		-- 1.000mA
	NDV	- - - - - - -	9	3.219NA		-- 1.000mA
	NDV	- - - - - - -	7	1.715NA		-- 1.000mA
	NDV	- - - - - - -	8	1.773NA		-- 1.000mA
	NDV	- - - - - - -	11	3.104NA		-- 1.000mA
	NDV	- - - - - - -	29	3.738NA		-- 1.000mA
	NDV	- - - - - - -	30	4.231NA		-- 1.000mA
	NDV	- - - - - - -	31	4.569NA		-- 1.000mA
	NDV	- - - - - - -	32	4.750NA		-- 1.000mA
	NDV	- - - - - - -	33	4.281NA		-- 1.000mA
	NDV	- - - - - - -	34	4.600NA		-- 1.000mA
	NDV	- - - - - - -	35	5.015NA		-- 1.000mA
	NDV	- - - - - - -	36	5.046NA		-- 1.000mA
	NDV	- - - - - - -	37	4.323NA		-- 1.000mA
	NDV	- - - - - - -	38	4.612NA		-- 1.000mA
	NDV	- - - - - - -	39	5.600NA		-- 1.000mA
	NDV	- - - - - - -	40	6.265NA		-- 1.000mA
	NDV	- - - - - - -	41	5.246NA		-- 1.000mA
	NDV	- - - - - - -	42	5.715NA		-- 1.000mA
	NDV	- - - - - - -	43	4.000NA		-- 1.000mA
	NDV	- - - - - - -	44	3.612NA		-- 1.000mA
	NDV	- - - - - - -	45	3.173NA		-- 1.000mA
	NDV	- - - - - - -	46	2.646NA		-- 1.000mA
	NDV	- - - - - - -	47	1.985NA		-- 1.000mA
	NDV	- - - - - - -	48	2.015NA		-- 1.000mA
	NDV	- - - - - - -	50	2.277NA		-- 1.000mA
	NDV	- - - - - - -	51	3.362NA		-- 1.000mA
	NDV	- - - - - - -	52	3.331NA	OUTPUT	-- 1.000mA
	NDV	- - - - - - -	18	2.012NA	I/O	-- 1.000mA
	NDV	- - - - - - -	17	414.0UA	I/O	-- 1.000mA

Figure V.G.16a - CD Stress, Average Leakage Current Values

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C N750V STRESS
ON 17 NOV 83 AT 08:27 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE		LIMITS MINIMUM	MAXIMUM
		PIN		FUNCTION		
	NDV - - - - - - -	5	1.112NA	I/O	--	1.000MA
	NDV - - - - - - -	4	1.381NA	↑	--	1.000MA
	NDV - - - - - - -	3	14.25NA		--	1.000MA
	NDV - - - - - - -	2	7.462NA		--	1.000MA
	NDV - - - - - - -	1	1.296NA		--	1.000MA
	NDV - - - - - - -	64	1.108NA		--	1.000MA
	NDV - - - - - - -	63	1.250NA		--	1.000MA
	NDV - - - - - - -	62	1.062NA		--	1.000MA
	NDV - - - - - - -	61	1.277NA		--	1.000MA
	NDV - - - - - - -	60	1.054NA		--	1.000MA
	NDV - - - - - - -	59	1.150NA		--	1.000MA
	NDV - - - - - - -	58	1.069NA		--	1.000MA
	NDV - - - - - - -	57	1.054NA		--	1.000MA
	NDV - - - - - - -	56	1.177NA		--	1.000MA
	NDV - - - - - - -	55	1.015NA		--	1.000MA
	NDV - - - - - - -	54	1.223NA	I/O	--	1.000MA

PIN AVERAGE OF SERIAL NUMBERS:
17,18,19,20,21,22,23,24,25,26,27,28,30

Figure V.G.16a - CD Stress, Average Leakage Current Values (Cont.)

NDVR reading	Voltage
1	0
20	-500
7	+750
40	-750
45	-1000
31	+1250
88	-1250
88	-1500
145	+1750
4	-1750
278	-2000
4	+2250

Figure V.G.17 - CD Leakage Current on S/N 30, Pin 10 (Nanoamps)

Pin Number

10	12	13	15	17	18	21	22	23	24	25	Electrical Condition
7	8	6	4			6	4	5	7	7	Open
2	1	2	6	9	9	3	4	2	2	1	Leaky
1	1	2		1	1	1	2	3	1	2	Normal

Figure V.G.17a- CD Stress, Failure Summary

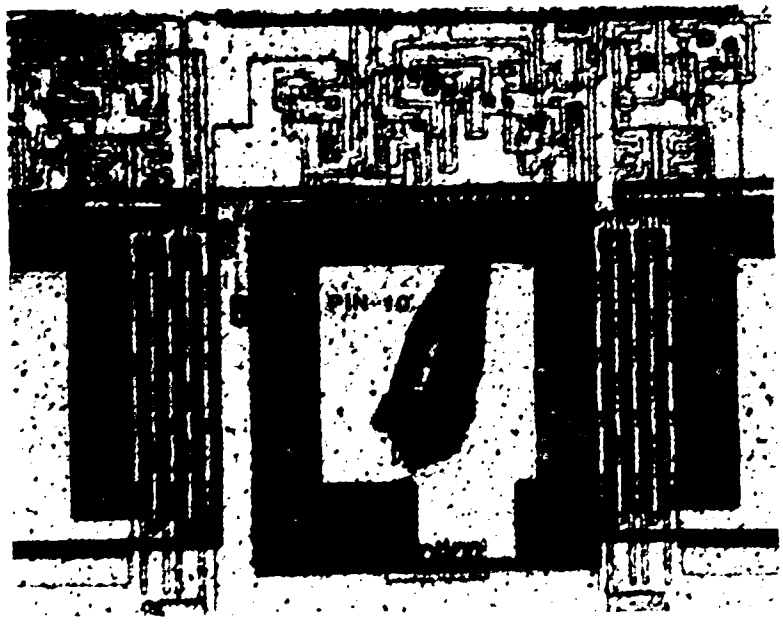


Figure V.G.18 - Pin 10 Input

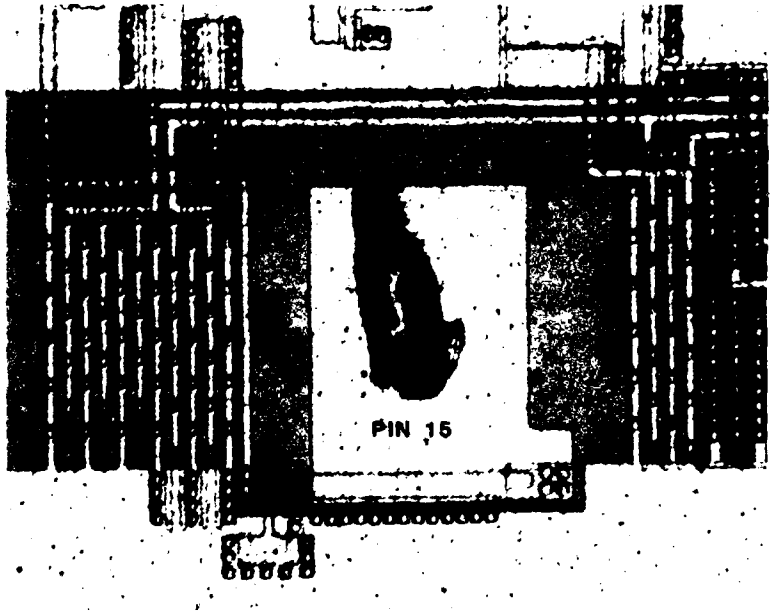


Figure V.G.19 - Pin 15 Clock Input

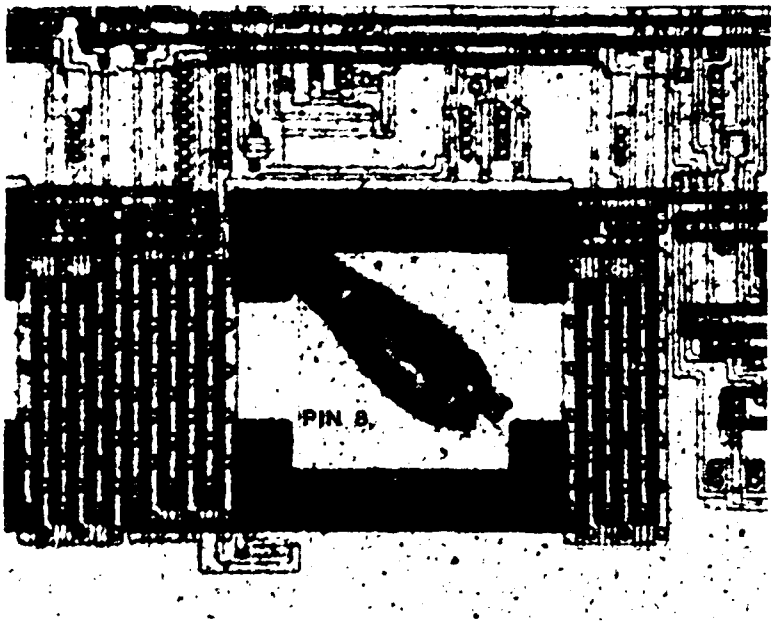


Figure V.G.20 - Pin 8 Output

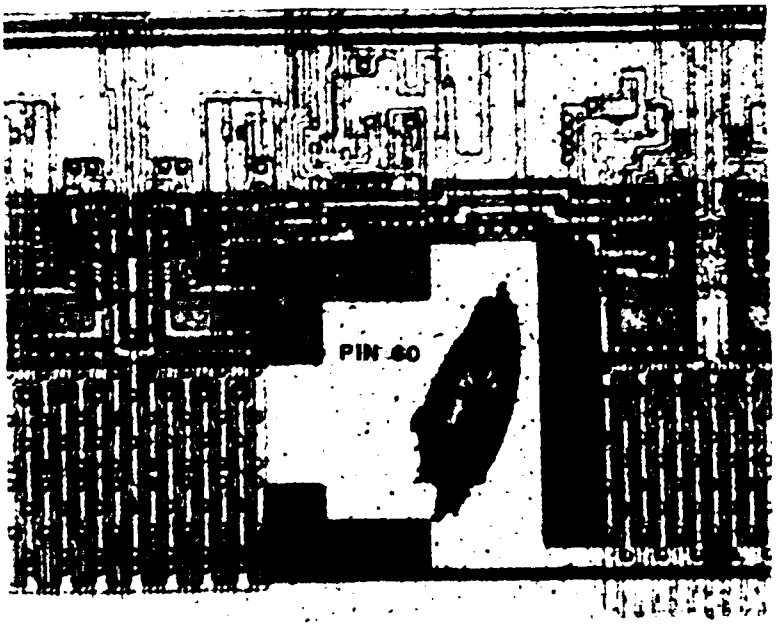


Figure V.G.21 - Pin 60 Input/Output

Figure V.G.22 - Pin 17 and 18 Input/Output

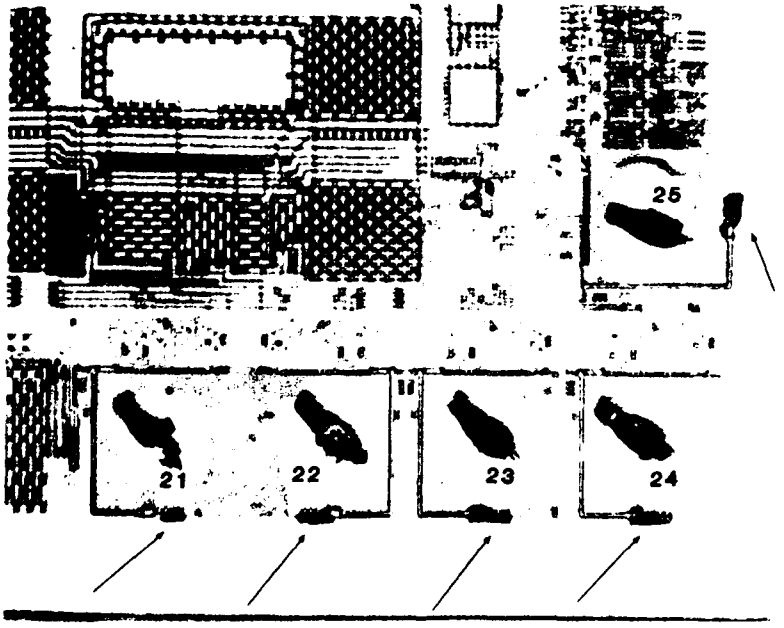


Figure V.G.23 - CD Stress, Damage at the Inputs

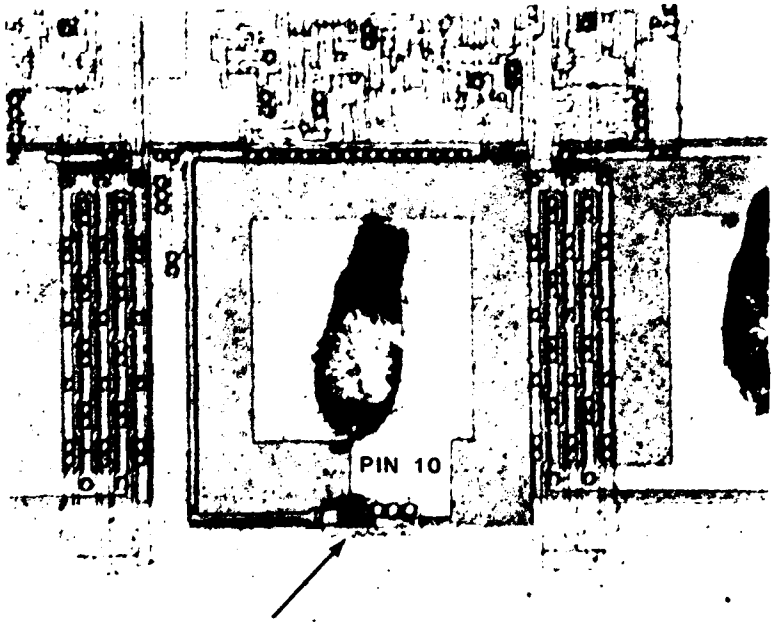


Figure V.G.24 - CD Stress, Damage at Pin 10 Inputs

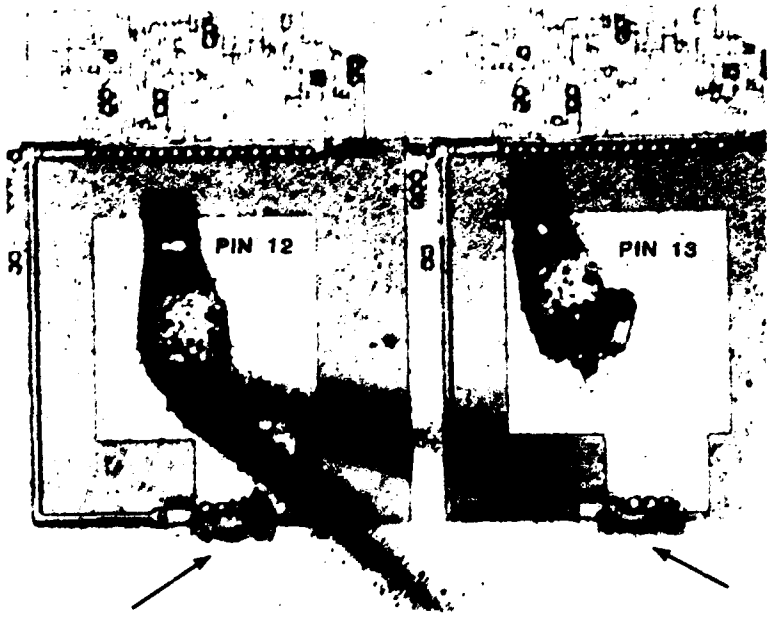


Figure V.G.25 - CD Stress, Damage at Pin 12 and 13

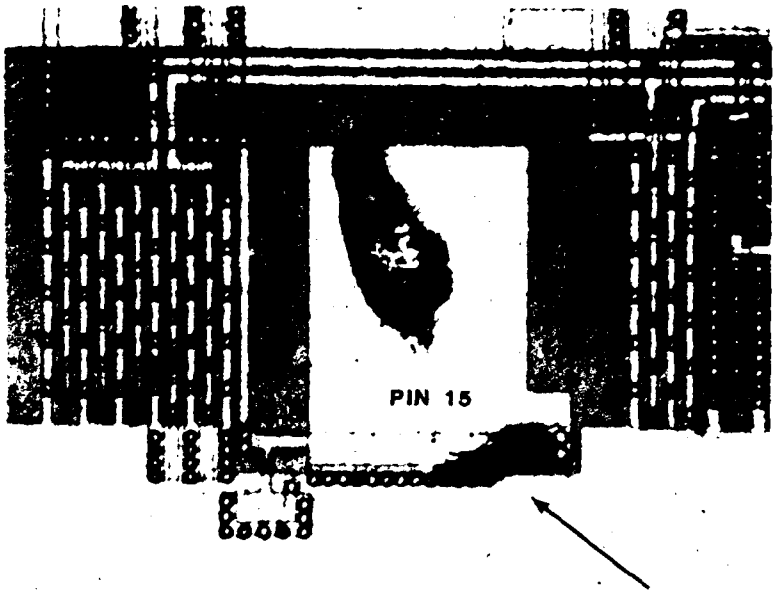


Figure V.G.26 - CD Stress, Damage on Pin 15

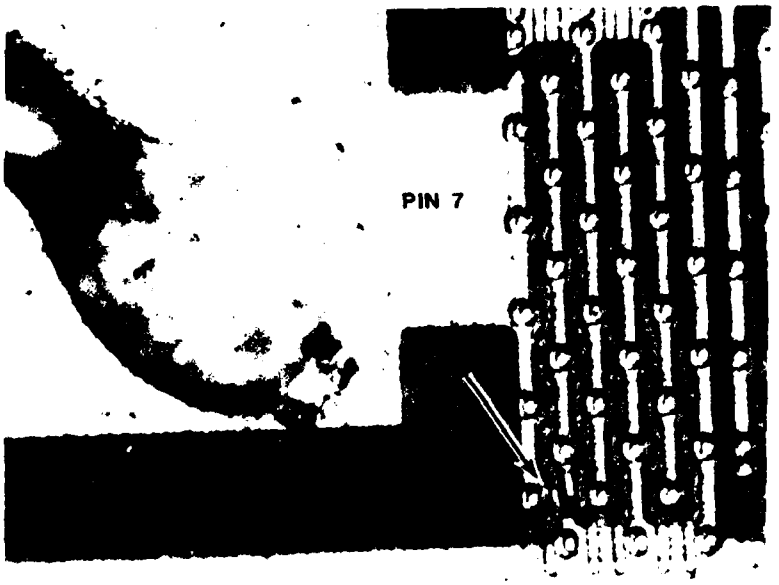


Figure V.G.27 - CD Stress, Short on Pin 7 Output

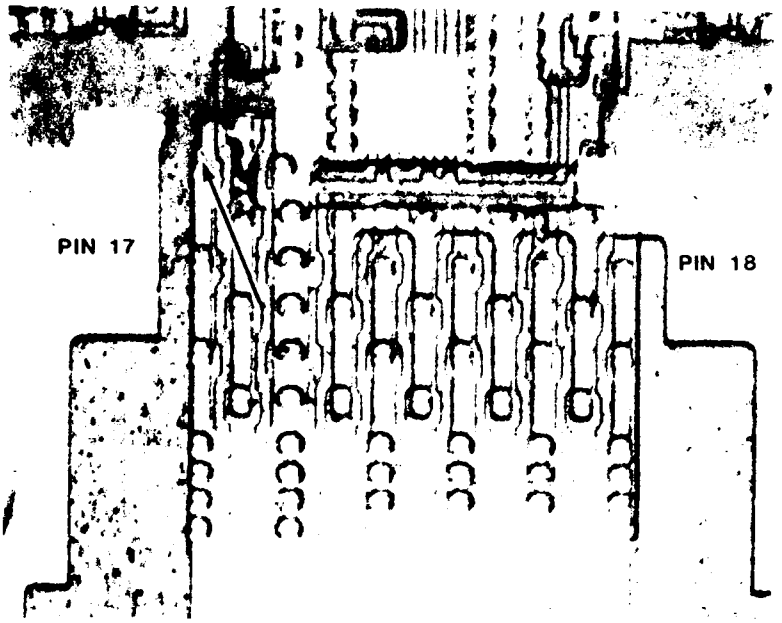


Figure V.G.28 - CD Stress,Pin 17 is Open to the Output Section and Pin 18 has Leakage Current

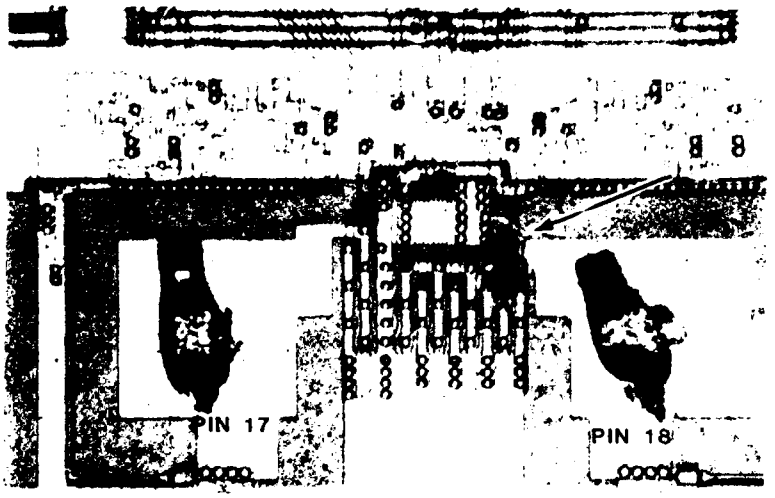


Figure V.G.29 - CD Stress Pin, 17 Has Leakage Current and Pin 18 is Open to the Output Section

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :153 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C N2250V STRESS
ON 13 DEC 83 AT 06:45 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		PIN	MEASURED VALUE	FUNCTION	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,14,15,16						
	NDV	- - - - - - -	15	2.115NA	INPUT	--	1.000MA
	NDV	- - - - - - -	22	7.976UA		--	1.000MA
	NDV	- - - - - - -	25	10.83NA		--	1.000MA
	NDV	- - - - - - -	24	40.48UA		--	1.000MA
	NDV	- - - - - - -	23	12.21UA		--	1.000MA
	NDV	- - - - - - -	13	30.63UA		--	1.000MA
	NDV	- - - - - - -	12	20.73NA		--	1.000MA
	NDV	- - - - - - -	21	12.99NA		--	1.000MA
	NDV	- - - - - - -	10	7.473NA		--	1.000MA
	NDV	- - - - - - -	28	3.412NA	INPUT	--	1.000MA
	NDV	- - - - - - -	27	3.450NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	26	3.442NA		--	1.000MA
	NDV	- - - - - - -	20	5.288NA		--	1.000MA
	NDV	- - - - - - -	19	4.346NA		--	1.000MA
	NDV	- - - - - - -	6	2.442NA		--	1.000MA
	NDV	- - - - - - -	9	72.70NA		--	1.000MA
	NDV	- - - - - - -	7	2.388NA		--	1.000MA
	NDV	- - - - - - -	8	2.477NA		--	1.000MA
	NDV	- - - - - - -	11	26.04NA		--	1.000MA
	NDV	- - - - - - -	29	3.388NA		--	1.000MA
	NDV	- - - - - - -	30	3.469NA		--	1.000MA
	NDV	- - - - - - -	31	3.392NA		--	1.000MA
	NDV	- - - - - - -	32	3.369NA		--	1.000MA
	NDV	- - - - - - -	33	3.296NA		--	1.000MA
	NDV	- - - - - - -	34	3.369NA		--	1.000MA
	NDV	- - - - - - -	35	3.358NA		--	1.000MA
	NDV	- - - - - - -	36	3.246NA		--	1.000MA
	NDV	- - - - - - -	37	3.304NA		--	1.000MA
	NDV	- - - - - - -	38	3.327NA		--	1.000MA
	NDV	- - - - - - -	39	3.392NA		--	1.000MA
	NDV	- - - - - - -	40	3.596NA		--	1.000MA
	NDV	- - - - - - -	41	3.231NA		--	1.000MA
	NDV	- - - - - - -	42	4.342NA		--	1.000MA
	NDV	- - - - - - -	43	4.204NA		--	1.000MA
	NDV	- - - - - - -	44	4.254NA		--	1.000MA
	NDV	- - - - - - -	45	3.665NA		--	1.000MA
	NDV	- - - - - - -	46	3.512NA		--	1.000MA
	NDV	- - - - - - -	47	3.154NA		--	1.000MA
	NDV	- - - - - - -	48	3.154NA		--	1.000MA
	NDV	- - - - - - -	50	3.288NA		--	1.000MA
	NDV	- - - - - - -	51	3.742NA		--	1.000MA
	NDV	- - - - - - -	52	4.000NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	18	1.173NA	I/O	--	1.000MA
	NDV	- - - - - - -	17	109.8UA	I/O	--	1.000MA

Figure V.G.30 - HBD Stress, Average Leakage Currents with Pin Numbers and Functions

FILE UID :153 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C N2250V STRESS

ON 13 DEC 83 AT 06:45 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	PIN	MEASURED VALUE	FUNCTION	LIMITS MINIMUM	LIMITS MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,14,15,16						
	NDV	5	1.688NA	I/O	--	1.000MA
	NDV	4	1.927NA	↑	--	1.000MA
	NDV	3	1.808NA		--	1.000MA
	NDV	2	2.665NA		--	1.000MA
	NDV	1	1.815NA		--	1.000MA
	NDV	64	1.927NA		--	1.000MA
	NDV	63	1.892NA		--	1.000MA
	NDV	62	1.846NA		--	1.000MA
	NDV	61	1.942NA		--	1.000MA
	NDV	60	1.715NA		--	1.000MA
	NDV	59	1.946NA		--	1.000MA
	NDV	58	1.654NA		--	1.000MA
	NDV	57	1.869NA		--	1.000MA
	NDV	56	1.781NA		--	1.000MA
	NDV	55	1.712NA		--	1.000MA
	NDV	54	1.885NA	I/O	--	1.000MA

Figure V.G.30 - HBD Stress, Average Leakage Currents with Pin Numbers and Functions (Cont.)

PIN NUMBERS

10	12	13	15	17	18	21	22	23	24	25	ELECTRICAL CONDITION
5	6					3				2	OPEN
		2		5		1		1	2	2	LEAKY
5	4	8	10	5	10	6	10	9	8	6	NORMAL

Figure V.G.31 - HBD Stress, Failure Summary

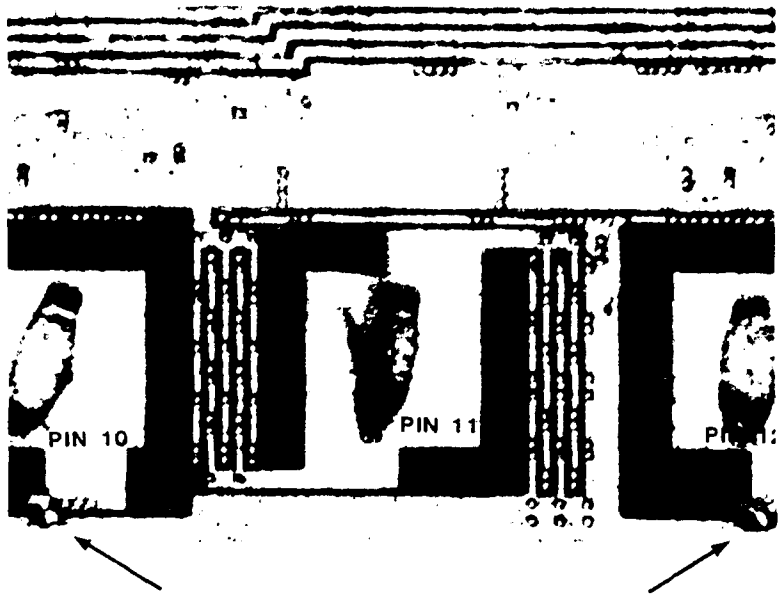


Figure V.G.32 - HBD Stress, Damage on Pins 10 and 12

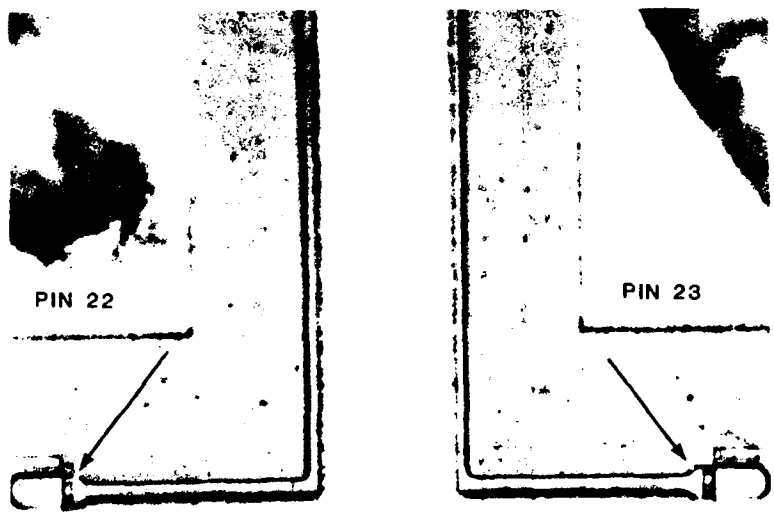


Figure V.G.33 - HBD Stress, Damage on Pins 22 and 23

H. Part H Analysis

This device is a 16-bit Microprocessor manufactured using HMOS. This is an N-channel, depletion load, silicon gate process. There are two polysilicon layers and one metallization layer. The minimum polysilicon width was about 2.5 microns and the minimum metallization width was about 3.5 microns. This was in a 40 pin dual-in-line ceramic package.

An overall die photograph is shown in Figure V.H.1. VCC is pin 40 and is on the left side of the figure. There are two ground connections, pins 1 and 20. Between VCC, pin 40, and pin 1 there is a bond pad and a wire which goes to substrate. A similar connection is made between pins 20 and 21.

The VCC bond pad is shown in Figure V.H.2. This metallization traverses the perimeter of the die to make contact with each of the inputs and outputs. It also connects to the central sections of the die. It connects to numerous n+ source diffusions.

The ground pads are shown in Figures V.H.3 and V.H.4. This metallization traverses the perimeter of the die just inside of the VCC metallization.

An input circuit is shown in Figure V.H.5 and the corresponding schematic is shown in Figure V.H.6. The input resistance measures 700 ohms. At the connection between the metallization and the diffused resistor is a polysilicon square. This is likely for ESD protection to reduce the chance of metal fusing into the silicon. The VCC metallization lays over the edge of the input resistor and produces a gated diode to substrate. The gate dielectric breakdown was about 33 volts. The input resistor to substrate and the transistor junction breakdowns were 18 volts.

An output structure is shown in Figure V.H.7 and the corresponding schematic is shown in Figure V.H.8.

The same type of output configuration is used on combination I/O pins, however a different input is used. An I/O pin is shown in Figure V.H.9 and the schematic is shown in Figure V.H.10.

In this case the input section is connected directly to a polysilicon gate. All of the outputs are the same electrically however there are three separate layouts.

Microsections were performed and the construction of the devices examined. Figure V.H.11 shows a transistor cross-section. The n-type diffusion was about 0.45 microns, the polysilicon was about 0.5 microns thick, and the metallization was about 1.0 micron thick. The oxide between the polysilicon and the silicon was 0.9 microns thick and the oxide between the polysilicon and the metallization was 1.1 microns thick.

Electrical Testing

Electrical data was taken on each of the stressed parts and the control part at each iteration during the testing. If the parts did not have a leakage failure, the data was not printed except at the initial, +500, +1000, +1500, +2000, etc., voltage levels. In addition to the leakage current information by serial number the average leakage current at each voltage level for each pin was calculated. These data are shown in Figures V.H.12 and V.H.13. Figure V.H.12 is the initial averages and Figure V.H.13 is the averages following the -2250 volt stress.

The readings taken on the Tektronix 3260 ATE were the input current leakage of each pin with respect to VCC and GND which were connected together. The readings were taken at +3 volts (NDV) and +10 volts (NDVR). This provided information on interface circuit damage. One additional measurement should have been made to ensure continuity. The failure mode which developed on several of the inputs was opens rather than shorts and this was not easily identifiable in this test.

Functional testing was performed on an SDK-86 System Design kit. This was done after each testing sequence. The operations which each chip was asked to perform included; system reset, addition, and subtraction. This is not a complete functional test but does exercise a good portion of the device. A more complete functional test was used initially and at the end of the test. This included transferring control to a terminal, modifying and reading memory and transferring control back to the keyboard. It was found that if devices passed the first functional they would pass the latter functional and if they failed the first they would fail the latter.

Charged Device Data Analysis

Fifteen devices, S/N 17 - 31, were stressed with the charged device ESD simulation model. Serial number 31 was taken through the test and stress sequence until it failed in order to provide an early indication of the voltage level which would be required. It failed functionally after the +2000 volt stress. The remainder of the devices were taken through the testing sequence and failed functionally as shown in Figure V.H.14. Serial number 25 was pulled for failure analysis and the remainder of the parts were left in test to gain further information on input circuit degradation.

The testing was stopped after the +2500 volt stress. Leakage current failures are summarized in Figure V.H.15. This includes input pins 17, 18, 19, 21, 22, 23, and 33, output pins 25, 26, and 32 and I/O pins 5, 14, 16, and 39. The measurement used to compile this table was a curve tracer reading at 10 volts after the final stress. This is in agreement with the pin averages for leakage current which was taken on the Tektronix 3260. Figure V.H.16 shows the average values after the +2500 volt stress. These can be compared to the initial averages shown in Figure 12.

To understand the variation in sensitivities the failure modes and the layouts need to be understood. Figures V.H.17 - V.H.25 show the layouts.

Figure V.H.17 - V.H.19 show input/output layouts. The I/O in Figure V.H.19 is pin 5 which was very susceptible to the charged device stress but not to the human body simulation. Two output pins are shown in Figures V.H.20 and V.H.21. Pins 25 and 26 in Figure V.H.21 failed open during the charged device testing. These pins did not develop leakage current. Figure V.H.22 shows output pin 32 and input pin 33. Figures V.H.23 - V.H.25 show input pin layouts. Pin 21 in Figure V.H.25 was one of the most susceptible pins to stress.

Failure analysis found the cause for the increased sensitivity of certain pins to be the physical layout. The damage on several inputs is shown in Figures V.H.26 through V.H.30. The distance between adjacent n+ diffusions determined the sensitivity. Pins 18 and 19 were the least sensitive, followed by pins 22 and 23, and pin 21 was the most sensitive.

Additional damage which occurred on the inputs is shown in Figures V.H.31 and V.H.32. Figure V.H.31 shows a breakdown which occurred between pin 22 and VCC. Two opens occurred on this pin. The close spacing between the polysilicon and the VCC metallization caused breakdowns to occur as shown in Figure V.H.32. This pin was not shorted or leaky when measured.

Pins 25 and 26 were found to fail open as shown in Figure V.H.33. Mechanical probing found these transistors to have normal junction characteristics. The opens are likely due to these outputs being forced to interface with shorted inputs during the functional test.

Pins 32 and 33 developed leakage current due to their physical layout. This was the only output which failed due to leakage current. These pins are shown in Figures V.H.34 and V.H.35.

The other pin that failed consistently was I/O pin 5. This pin had gate oxide failures as shown in Figures V.H.36 and V.H.37. The large ground contact beside the input gate caused this part to be susceptible to the CD stress but not the HBD stress. The ground metallization capacitance would discharge through this pin and rupture the gate oxide.

These parts were very tolerant to ESD stress. Slight variations in the layout could improve this further.

Human Body Discharge Data Analysis

Fifteen devices, S/N 2 through 16, were stressed with the human body ESD simulation test method. Serial number 2 was taken through the test and stress sequence first. It was taken through the -2250 volt level with no functional or leakage problems. The remainder of the devices were taken through the testing sequence and failed functionally as follows: +2750V S/N 11, +4500V S/N 10, and -5000V S/N 14. These were the only three parts that failed the functional test. The parts were removed from further stress as they failed. Leakage increases followed a pattern similar to that seen on the charged device models except that pin 5 was not damaged on

any of the devices. The configuration with the ground metallization beside the input gate does not create an input that is more sensitive to the human body ESD simulation.

Figure V.H.38 shows the leakage current averages after the +5000 volt stress for the 3 volt reverse bias situation. Pins 17, 18, 19, 21, 22, 23, 32 and 33 exhibited leakage increase. These are all inputs except for pin 32.

The electrical condition of 13 parts as measured on a curve tracer are shown in Figure V.H.39. The leakage in this case was measured at 1 volt reverse bias. There were no opens measured for these parts.

The leakage current increases were created by similar situations on these parts as compared to the charged device group parts. Figures V.H.40 through V.H.42 show examples. The physical layout variations cause the same pins and pin combinations to be susceptible to damage. Pin 21 was the most susceptible followed by pins 32 and 33.

These devices were found to be the most tolerant to ESD stress of any group tested. The combination of no current path available to the outside from the substrate and possibly the polysilicon interface material created this condition. A minor change on pin 21 and 33 could further decrease this sensitivity.

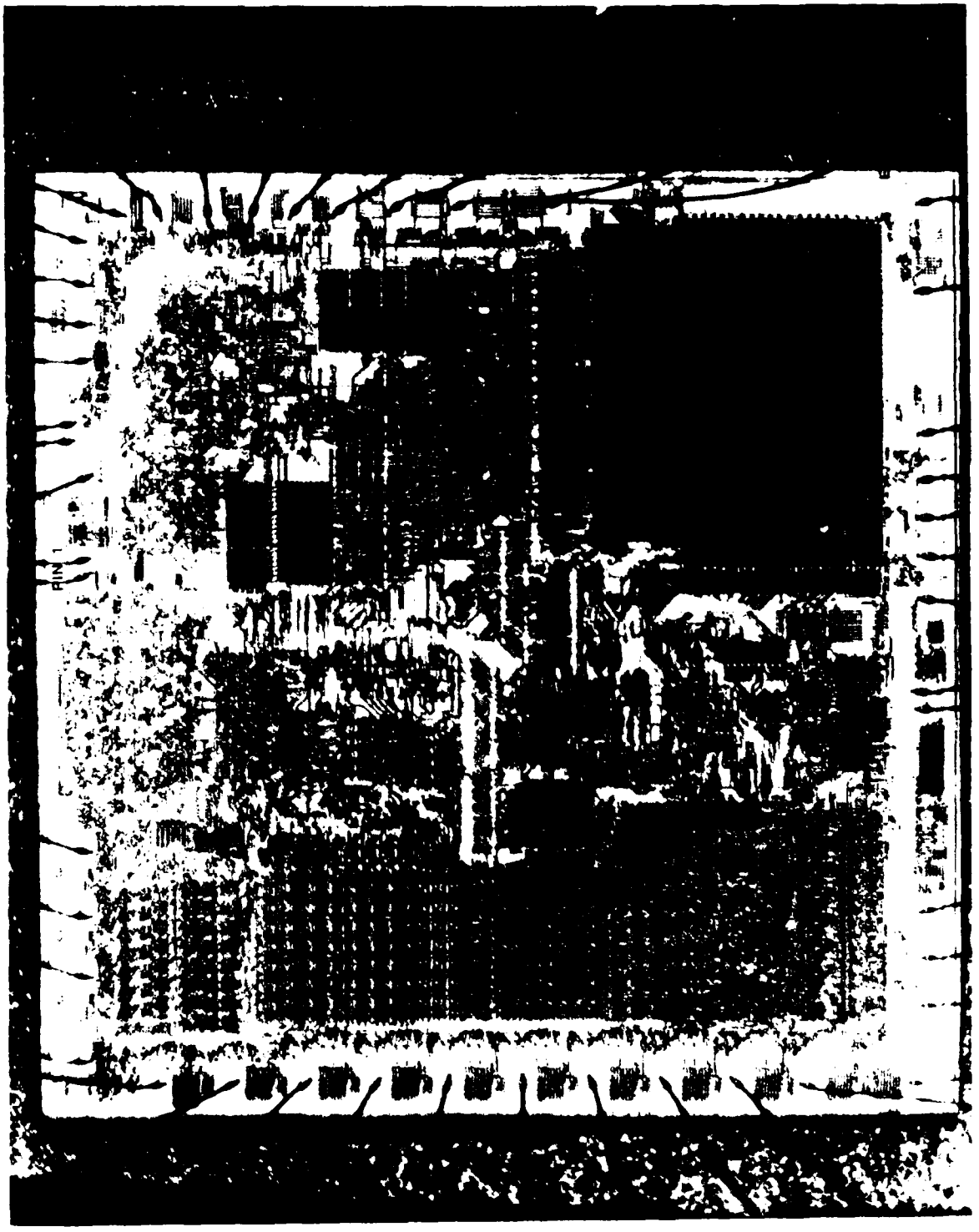


Figure V.H.1 - Overall Die Photograph

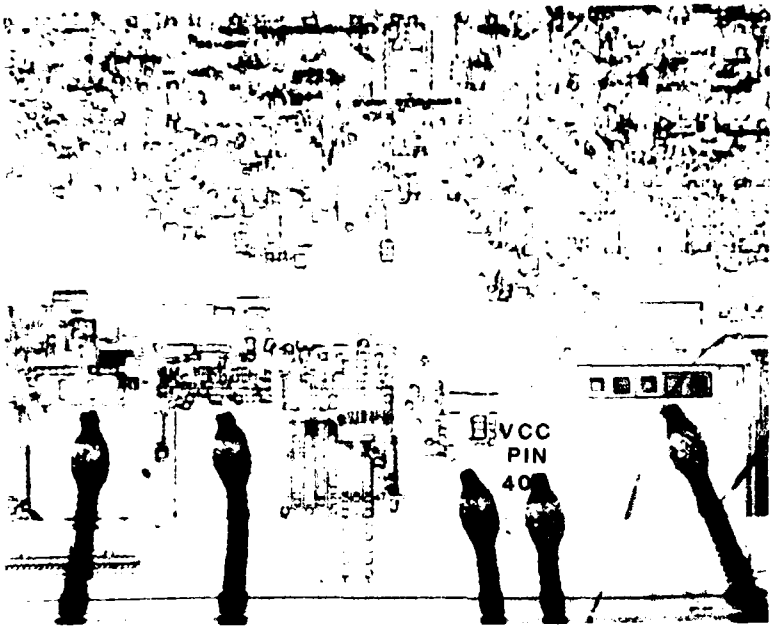


Figure V.H.2 - VCC Bond Pad

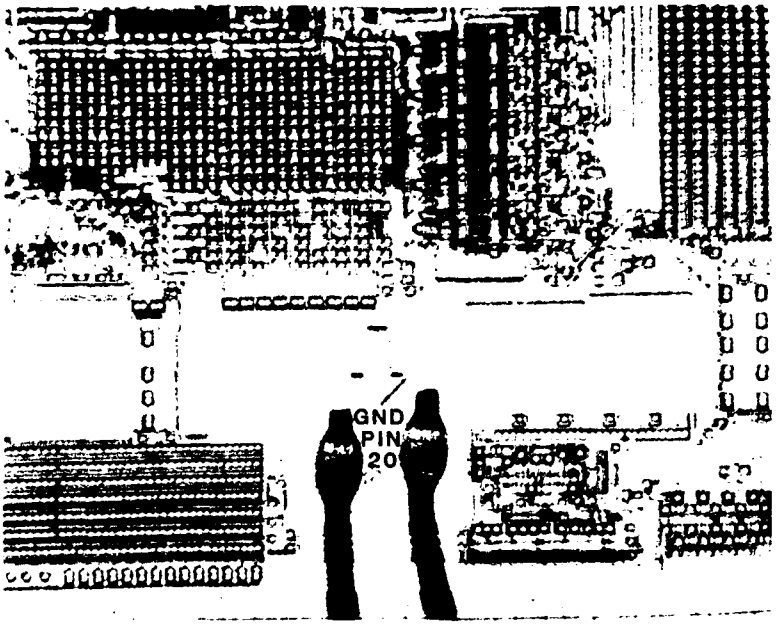


Figure V.H.3 - GND Bond Pad, Pin 20

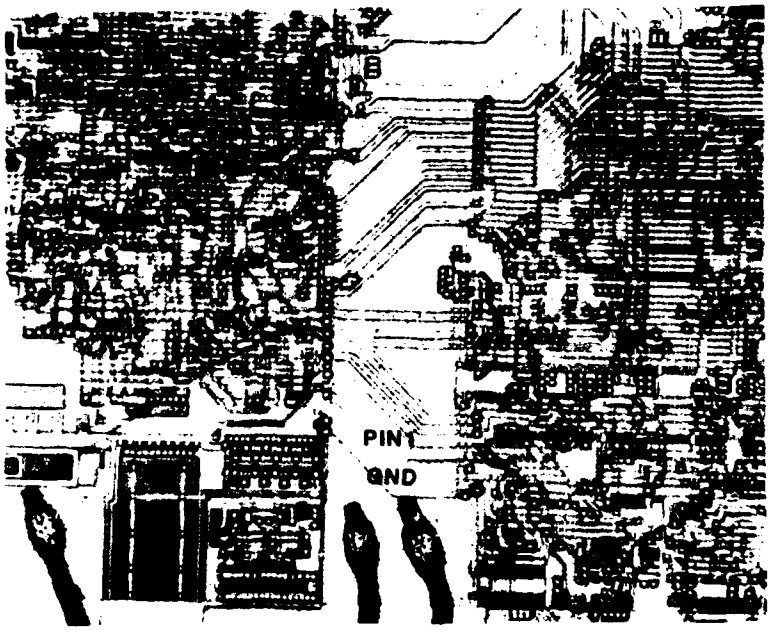


Figure V.H.4 - GND Bond Pad, Pin 1

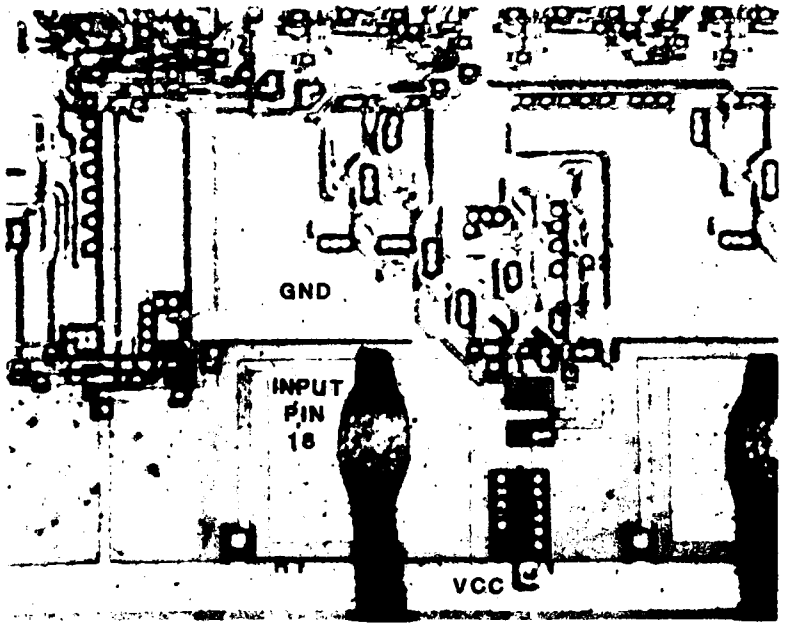


Figure V.H.5 - Pin 18 Input

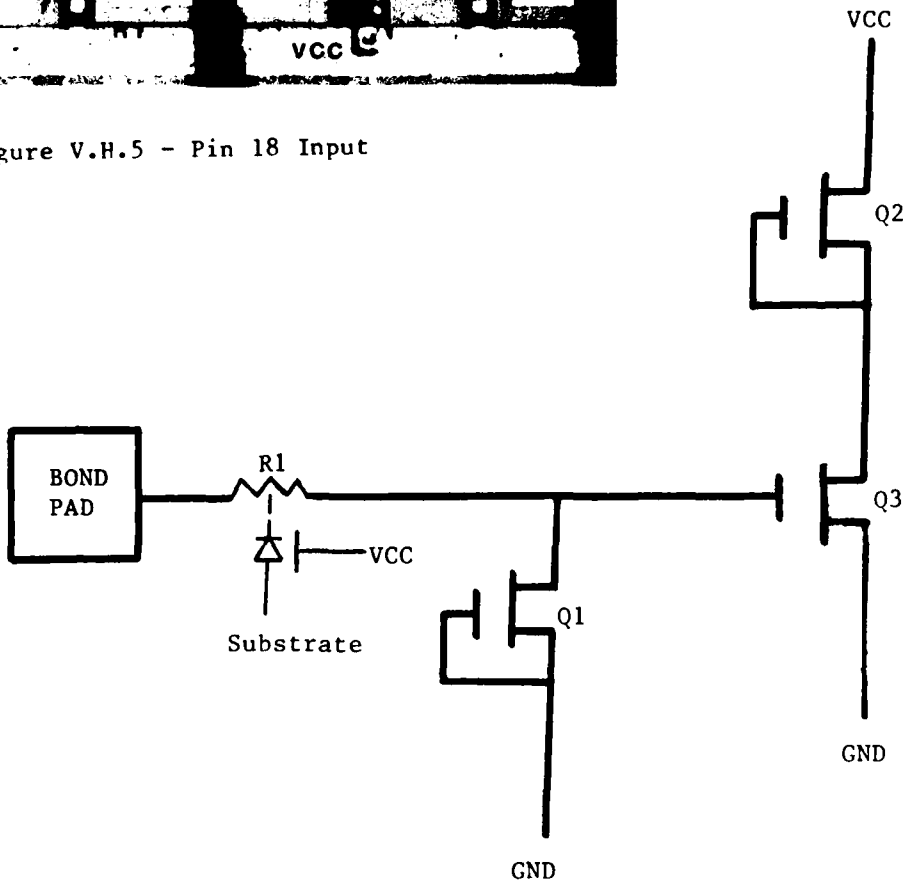


Figure V.H.6 - Input Schematic

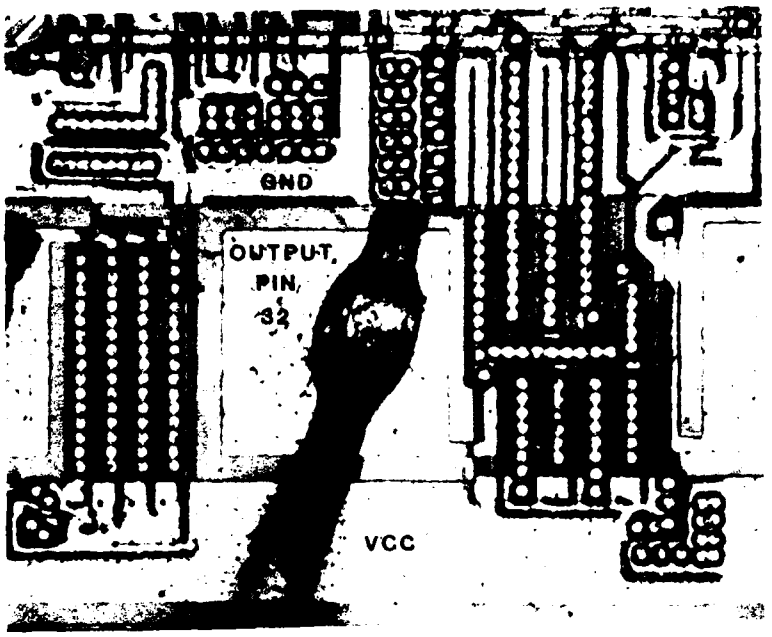


Figure V.H.7 - Pin 32 Output

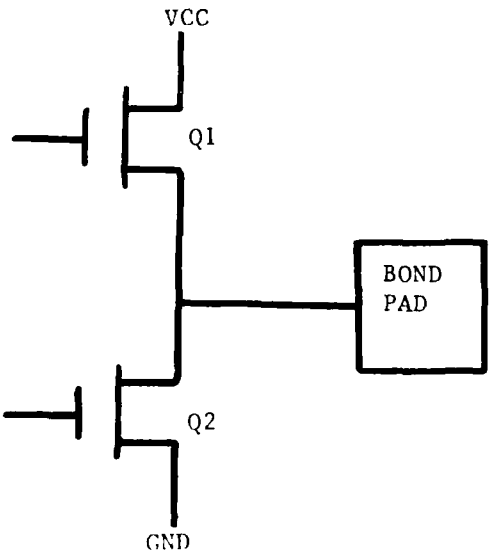


Figure V.H.8 - Output Schematic

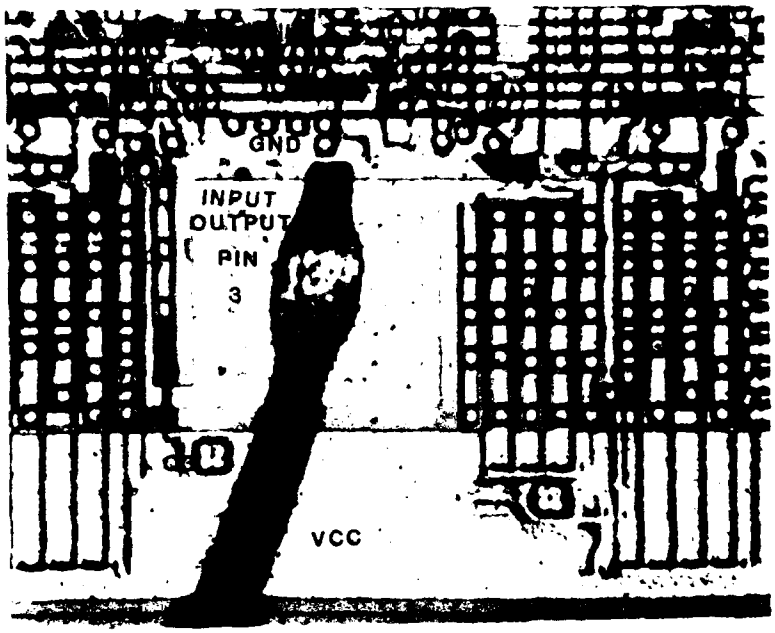


Figure V.H.9 - Pin 3 Input/Output

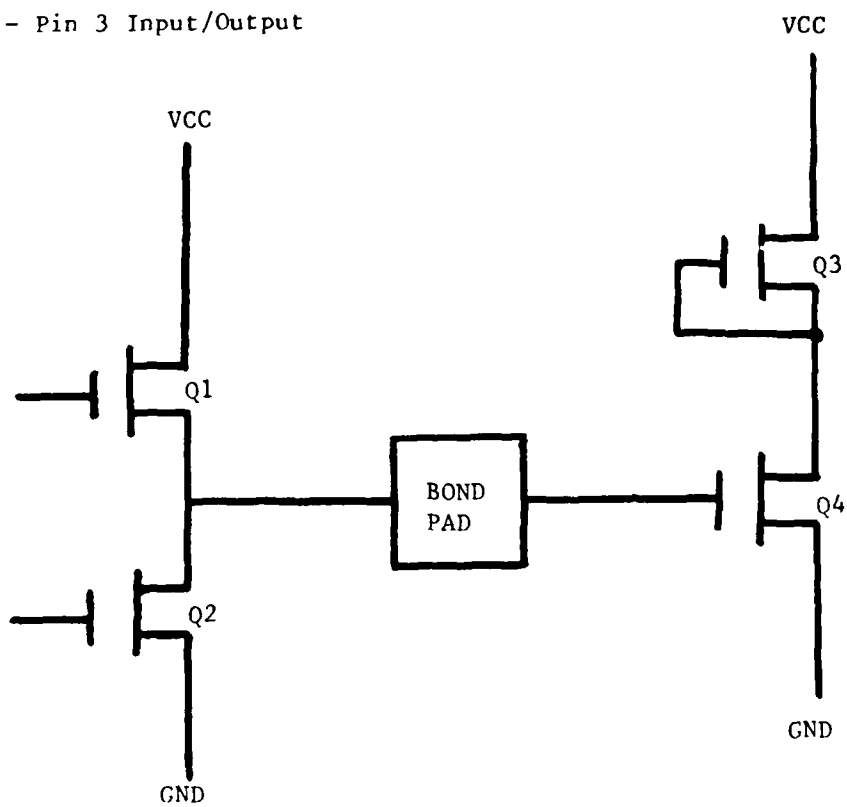


Figure V.H.10 - Input/Output Schematic

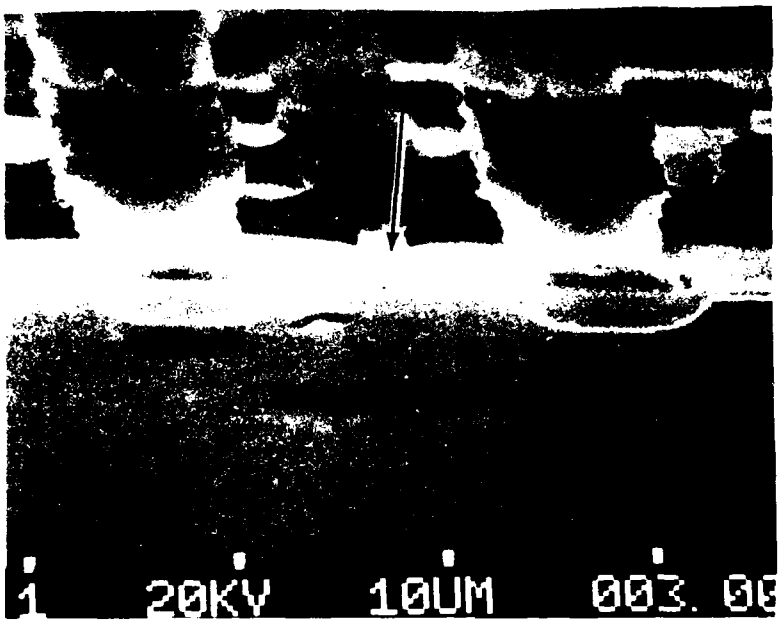


Figure V.H.11 - Transistor Cross-Section

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION MRTN EXAMINATION 41

FILE UID :152 NUMBER = 00010000
TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 1815 WITH THE 32bC TEST S

CASE	TEST TYPE	MEASURED VALUE	LIMIT MINIMUM	LIMIT MAXIMUM

PIN AVERAGE OF SERIAL NUMBERS:
1,1,2,3,5,5,7,8,9,10,11,12,13,14,15,16

		PIN		FUNCTION		
NDV	- - - - - -	21	1.315NA	INPUT	--	1.000MA
NDV	- - - - - -	17	503.1PA	INPUT	--	1.000MA
NDV	- - - - - -	18	540.6PA	INPUT	--	1.000MA
NDV	- - - - - -	19	659.0PA	INPUT	--	1.000MA
NDV	- - - - - -	22	468.7PA	INPUT	--	1.000MA
NDV	- - - - - -	23	671.9PA	INPUT	--	1.000MA
NDV	- - - - - -	31	526.5UA	I/O	--	1.000MA
NDV	- - - - - -	33	1.056NA	INPUT	--	1.000MA
NDV	- - - - - -	24	1.050NA	OUTPUT	--	1.000MA
NDV	- - - - - -	30	550.0UA	I/O	--	1.000MA
NDV	- - - - - -	25	928.1PA	OUTPUT	--	1.000MA
NDV	- - - - - -	26	803.1PA	OUTPUT	--	1.000MA
NDV	- - - - - -	28	818.8PA	OUTPUT	--	1.000MA
NDV	- - - - - -	29	584.4PA	OUTPUT	--	1.000MA
NDV	- - - - - -	32	781.3PA	OUTPUT	--	1.000MA
NDV	- - - - - -	27	621.9PA	OUTPUT	--	1.000MA
NDV	- - - - - -	34	803.1PA	OUTPUT	--	1.000MA
NDV	- - - - - -	16	200.0NA	I/O	--	1.000MA
NDV	- - - - - -	15	759.4PA	I/O	--	1.000MA
NDV	- - - - - -	14	834.4PA	I/O	--	1.000MA
NDV	- - - - - -	13	659.4PA	I/O	--	1.000MA
NDV	- - - - - -	12	38.25NA	I/O	--	1.000MA
NDV	- - - - - -	11	637.5PA	I/O	--	1.000MA
NDV	- - - - - -	10	793.8PA	I/O	--	1.000MA
NDV	- - - - - -	9	618.8PA	I/O	--	1.000MA
NDV	- - - - - -	8	753.1PA	I/O	--	1.000MA
NDV	- - - - - -	7	800.0PA	I/O	--	1.000MA
NDV	- - - - - -	6	643.8PA	I/O	--	1.000MA
NDV	- - - - - -	5	871.9PA	I/O	--	1.000MA
NDV	- - - - - -	4	621.9PA	I/O	--	1.000MA
NDV	- - - - - -	3	921.9PA	I/O	--	1.000MA
NDV	- - - - - -	2	743.8PA	I/O	--	1.000MA
NDV	- - - - - -	39	784.4PA	I/O	--	1.000MA
NDV	- - - - - -	38	771.9PA	OUTPUT	--	1.000MA
NDV	- - - - - -	37	784.4PA	OUTPUT	--	1.000MA
NDV	- - - - - -	36	771.9PA	OUTPUT	--	1.000MA
NDV	- - - - - -	35	871.9PA	OUTPUT	--	1.000MA
NDV	- - - - - -		4.750NA		--	1.000MA
NDV	- - - - - -		2.250NA		--	1.000MA
NDV	- - - - - -		1.500NA		--	1.000MA
NDV	- - - - - -		2.875NA		--	1.000MA
NDV	- - - - - -		1.750UA		--	1.000MA
NDV	- - - - - -		2.125NA		--	1.000MA

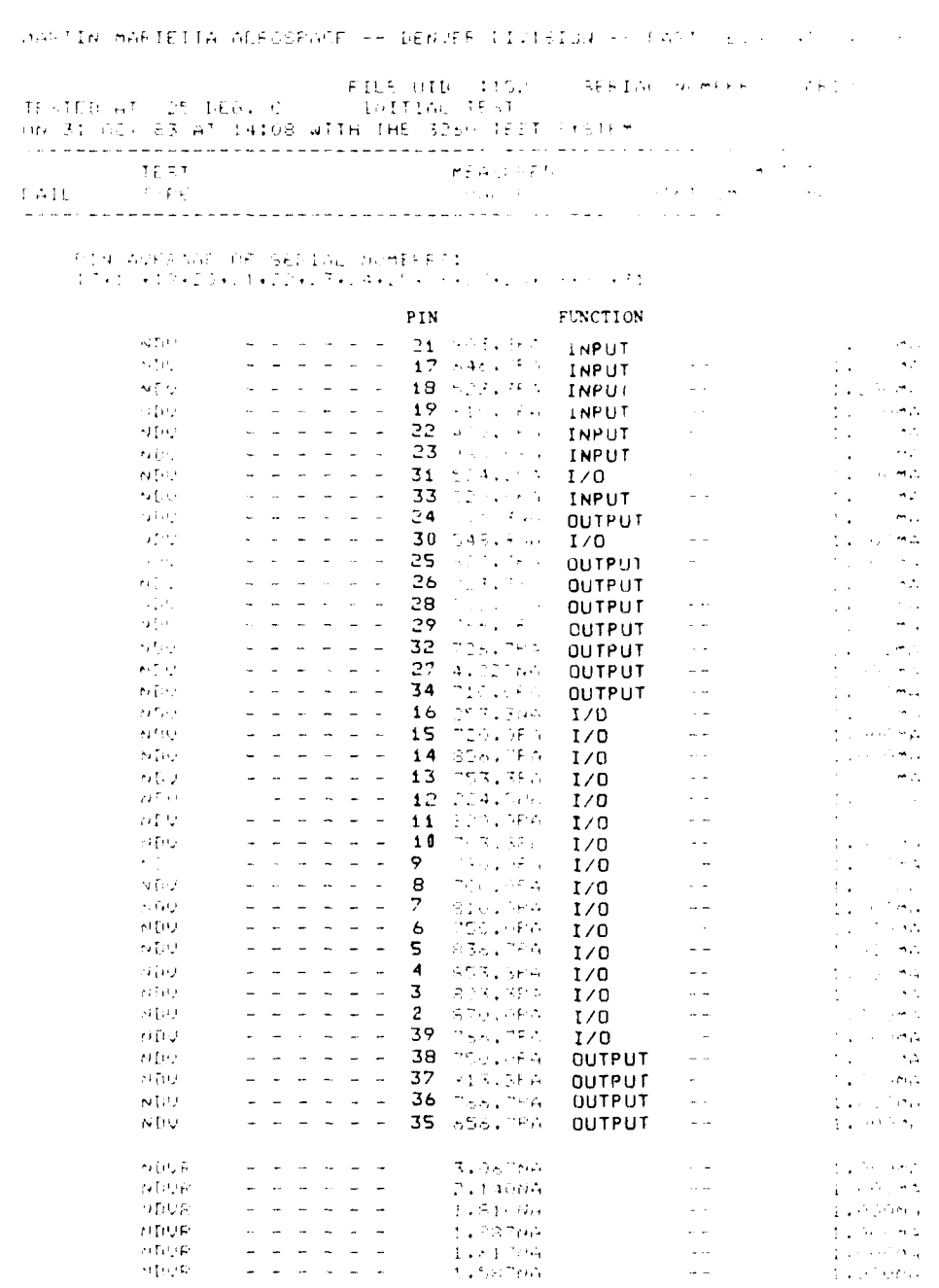
Figure V.H.12 - Average Leakage Currents at Initial Test

FILE UID :152 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 13:50 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 1,1,2,3,5,6,7,8,9,10,11,12,13,14,15,16			
****	NDVR - - - - - - -	1.097MA	--	1.000MA
	NDVR - - - - - - -	3.688NA	--	1.000MA
	NDVR - - - - - - -	11.58UA	--	1.000MA
****	NDVR - - - - - - -	1.104MA	--	1.000MA
	NDVR - - - - - - -	10.23NA	--	1.000MA
	NDVR - - - - - - -	5.925NA	--	1.000MA
	NDVR - - - - - - -	3.706NA	--	1.000MA
	NDVR - - - - - - -	3.447NA	--	1.000MA
	NDVR - - - - - - -	14.46NA	--	1.000MA
	NDVR - - - - - - -	3.275NA	--	1.000MA
	NDVR - - - - - - -	2.506NA	--	1.000MA
	NDVR - - - - - - -	286.6NA	--	1.000MA
	NDVR - - - - - - -	4.066NA	--	1.000MA
	NDVR - - - - - - -	3.034NA	--	1.000MA
	NDVR - - - - - - -	2.813NA	--	1.000MA
	NDVR - - - - - - -	58.61NA	--	1.000MA
	NDVR - - - - - - -	2.637NA	--	1.000MA
	NDVR - - - - - - -	2.484NA	--	1.000MA
	NDVR - - - - - - -	2.331NA	--	1.000MA
	NDVR - - - - - - -	3.391NA	--	1.000MA
	NDVR - - - - - - -	2.337NA	--	1.000MA
	NDVR - - - - - - -	2.656NA	--	1.000MA
	NDVR - - - - - - -	3.003NA	--	1.000MA
	NDVR - - - - - - -	3.897NA	--	1.000MA
	NDVR - - - - - - -	3.668NA	--	1.000MA
	NDVR - - - - - - -	3.441NA	--	1.000MA
	NDVR - - - - - - -	4.086NA	--	1.000MA
	NDVR - - - - - - -	3.284NA	--	1.000MA
	NDVR - - - - - - -	3.897NA	--	1.000MA
	NDVR - - - - - - -	2.722NA	--	1.000MA
	NDVR - - - - - - -	1.819NA	--	1.000MA

Figure V.H.12 - Average Leakage Currents at Initial Test (Cont.)



PIN	FUNCTION
21	INPUT
17	INPUT
18	INPUT
19	INPUT
22	INPUT
23	INPUT
31	I/O
33	INPUT
24	OUTPUT
30	I/O
25	OUTPUT
26	OUTPUT
28	OUTPUT
29	OUTPUT
32	OUTPUT
27	OUTPUT
34	OUTPUT
16	I/O
15	I/O
14	I/O
13	I/O
12	I/O
11	I/O
10	I/O
9	I/O
8	I/O
7	I/O
6	I/O
5	I/O
4	I/O
3	I/O
2	I/O
39	I/O
38	OUTPUT
37	OUTPUT
36	OUTPUT
35	OUTPUT

Figure V.H.12 - Average Leakage Currents at Initial Test (Cont.)

FILE UID :152 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C INITIAL TEST
ON 31 OCT 83 AT 14:08 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE	L I M I T S MINIMUM	MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,25,26,27,28,29,30,31			
****	NDVR - - - - - - -	1.024MA	--	1.000MA
	NDVR - - - - - - -	1.810NA	--	1.000MA
	NDVR - - - - - - -	141.0UA	--	1.000MA
****	NDVR - - - - - - -	1.024MA	--	1.000MA
	NDVR - - - - - - -	7.766UA	--	1.000MA
	NDVR - - - - - - -	2.928UA	--	1.000MA
	NDVR - - - - - - -	1.063UA	--	1.000MA
	NDVR - - - - - - -	875.2NA	--	1.000MA
	NDVR - - - - - - -	24.70NA	--	1.000MA
	NDVR - - - - - - -	1.213UA	--	1.000MA
	NDVR - - - - - - -	255.9NA	--	1.000MA
	NDVR - - - - - - -	2.383UA	--	1.000MA
	NDVR - - - - - - -	671.2NA	--	1.000MA
	NDVR - - - - - - -	464.4NA	--	1.000MA
	NDVR - - - - - - -	371.4NA	--	1.000MA
	NDVR - - - - - - -	1.511UA	--	1.000MA
	NDVR - - - - - - -	150.3NA	--	1.000MA
	NDVR - - - - - - -	128.7NA	--	1.000MA
	NDVR - - - - - - -	143.7NA	--	1.000MA
	NDVR - - - - - - -	114.5NA	--	1.000MA
	NDVR - - - - - - -	95.47NA	--	1.000MA
	NDVR - - - - - - -	105.6NA	--	1.000MA
	NDVR - - - - - - -	198.4NA	--	1.000MA
	NDVR - - - - - - -	251.3NA	--	1.000MA
	NDVR - - - - - - -	173.1NA	--	1.000MA
	NDVR - - - - - - -	126.4NA	--	1.000MA
	NDVR - - - - - - -	323.8NA	--	1.000MA
	NDVR - - - - - - -	140.8NA	--	1.000MA
	NDVR - - - - - - -	319.3NA	--	1.000MA
	NDVR - - - - - - -	351.0NA	--	1.000MA
	NDVR - - - - - - -	3.633NA	--	1.000MA

Figure V.H.12 - Average Leakage Currents at Initial Test (Cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :152 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C N2250V STRESS
ON 13 DEC 83 AT 06:28 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE		LIMITS MINIMUM		MAXIMUM
			PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,13,14,15,16				
			PIN	FUNCTION			
	NDV	- - - - - -	21 29.95NA	INPUT	--		1.000MA
	NDV	- - - - - -	17 19.48NA	INPUT	--		1.000MA
	NDV	- - - - - -	18 13.94NA	INPUT	--		1.000MA
	NDV	- - - - - -	19 14.90NA	INPUT	--		1.000MA
	NDV	- - - - - -	22 11.18NA	INPUT	--		1.000MA
	NDV	- - - - - -	23 6.446NA	INPUT	--		1.000MA
	NDV	- - - - - -	31 526.1UA	I/O	--		1.000MA
	NDV	- - - - - -	33 7.332NA	INPUT	--		1.000MA
	NDV	- - - - - -	24 2.114NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	30 548.6UA	I/O	--		1.000MA
	NDV	- - - - - -	25 2.011NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	26 2.057NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	28 1.839NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	29 1.989NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	32 16.55NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	27 1.914NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	34 1.843NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	16 3.171NA	I/O	--		1.000MA
	NDV	- - - - - -	15 2.171NA	I/O	--		1.000MA
	NDV	- - - - - -	14 1.807NA	I/O	--		1.000MA
	NDV	- - - - - -	13 1.968NA	I/O	--		1.000MA
	NDV	- - - - - -	12 2.429NA	I/O	--		1.000MA
	NDV	- - - - - -	11 1.950NA	I/O	--		1.000MA
	NDV	- - - - - -	10 1.879NA	I/O	--		1.000MA
	NDV	- - - - - -	9 1.786NA	I/O	--		1.000MA
	NDV	- - - - - -	8 1.914NA	I/O	--		1.000MA
	NDV	- - - - - -	7 1.739NA	I/O	--		1.000MA
	NDV	- - - - - -	6 1.954NA	I/O	--		1.000MA
	NDV	- - - - - -	5 1.804NA	I/O	--		1.000MA
	NDV	- - - - - -	4 1.907NA	I/O	--		1.000MA
	NDV	- - - - - -	3 1.907NA	I/O	--		1.000MA
	NDV	- - - - - -	2 1.839NA	I/O	--		1.000MA
	NDV	- - - - - -	39 1.964NA	I/O	--		1.000MA
	NDV	- - - - - -	38 1.714NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	37 2.046NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	36 1.743NA	OUTPUT	--		1.000MA
	NDV	- - - - - -	35 1.725NA	OUTPUT	--		1.000MA
	NDVR	- - - - - -	127.2NA		--		1.000MA
	NDVR	- - - - - -	128.1NA		--		1.000MA
	NDVR	- - - - - -	50.62NA		--		1.000MA
	NDVR	- - - - - -	51.59NA		--		1.000MA
	NDVR	- - - - - -	54.05NA		--		1.000MA
	NDVR	- - - - - -	23.60NA		--		1.000MA

Figure V.H.13 - Average Leakage Currents after -2250 volts

FILE UID :152 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C N2250V STRESS

ON 13 DEC 83 AT 06:28 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,10,11,12,13,14,15,16				
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	30.95NA	--	1.000MA
	NDVR	- - - - - - -	10.77UA	--	1.000MA
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	10.72NA	--	1.000MA
	NDVR	- - - - - - -	8.771NA	--	1.000MA
	NDVR	- - - - - - -	7.846NA	--	1.000MA
	NDVR	- - - - - - -	7.621NA	--	1.000MA
	NDVR	- - - - - - -	150.6NA	--	1.000MA
	NDVR	- - - - - - -	7.707NA	--	1.000MA
	NDVR	- - - - - - -	7.107NA	--	1.000MA
	NDVR	- - - - - - -	15.76NA	--	1.000MA
	NDVR	- - - - - - -	9.971NA	--	1.000MA
	NDVR	- - - - - - -	7.707NA	--	1.000MA
	NDVR	- - - - - - -	7.307NA	--	1.000MA
	NDVR	- - - - - - -	9.196NA	--	1.000MA
	NDVR	- - - - - - -	7.454NA	--	1.000MA
	NDVR	- - - - - - -	7.039NA	--	1.000MA
	NDVR	- - - - - - -	7.211NA	--	1.000MA
	NDVR	- - - - - - -	7.643NA	--	1.000MA
	NDVR	- - - - - - -	7.164NA	--	1.000MA
	NDVR	- - - - - - -	7.168NA	--	1.000MA
	NDVR	- - - - - - -	7.386NA	--	1.000MA
	NDVR	- - - - - - -	7.886NA	--	1.000MA
	NDVR	- - - - - - -	7.689NA	--	1.000MA
	NDVR	- - - - - - -	7.771NA	--	1.000MA
	NDVR	- - - - - - -	7.904NA	--	1.000MA
	NDVR	- - - - - - -	7.664NA	--	1.000MA
	NDVR	- - - - - - -	8.014NA	--	1.000MA
	NDVR	- - - - - - -	7.268NA	--	1.000MA
	NDVR	- - - - - - -	6.843NA	--	1.000MA

Figure V.H.13 - Average Leakage Currents after -2250 volts (cont.)

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :152 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C N2250V STRESS
ON 13 DEC 83 AT 06:33 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE	MEASURED VALUE			LIMITS MINIMUM		MAXIMUM
		PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,26,27,28,29,30					
		PIN		FUNCTION			
	NDV	21	847.1UA	INPUT	--		1.000MA
	NDV	17	420.4NA	INPUT	--		1.000MA
	NDV	18	150.4NA	INPUT	--		1.000MA
	NDV	19	74.77NA	INPUT	--		1.000MA
	NDV	22	315.4UA	INPUT	--		1.000MA
	NDV	23	389.2NA	INPUT	--		1.000MA
	NDV	31	525.2UA	I/O	--		1.000MA
	NDV	33	381.5UA	INPUT	--		1.000MA
	NDV	24	1.938NA	OUTPUT	--		1.000MA
	NDV	30	550.3UA	I/O	--		1.000MA
	NDV	25	1.512NA	OUTPUT	--		1.000MA
	NDV	26	1.519NA	OUTPUT	--		1.000MA
	NDV	28	1.596NA	OUTPUT	--		1.000MA
	NDV	29	1.492NA	OUTPUT	--		1.000MA
****	NDV	32	1.024MA	OUTPU	--		1.000MA
	NDV	27	5.612NA	OUTPUT	--		1.000MA
	NDV	34	1.496NA	OUTPUT	--		1.000MA
	NDV	16	195.3NA	I/O,	--		1.000MA
	NDV	15	1.581NA	I/O	--		1.000MA
	NDV	14	78.73UA	I/O	--		1.000MA
	NDV	13	1.592NA	I/O	--		1.000MA
	NDV	12	250.9NA	I/O	--		1.000MA
	NDV	11	1.542NA	I/O	--		1.000MA
	NDV	10	1.538NA	I/O	--		1.000MA
	NDV	9	1.496NA	I/O	--		1.000MA
	NDV	8	1.496NA	I/O	--		1.000MA
	NDV	7	1.542NA	I/O	--		1.000MA
	NDV	6	1.519NA	I/O	--		1.000MA
****	NDV	5	1.024MA	I/O	--		1.000MA
	NDV	4	1.665NA	I/O	--		1.000MA
	NDV	3	1.635NA	I/O	--		1.000MA
	NDV	2	1.550NA	I/O	--		1.000MA
	NDV	39	1.581NA	I/O	--		1.000MA
	NDV	38	1.438NA	OUTPUT	--		1.000MA
	NDV	37	1.662NA	OUTPUT	--		1.000MA
	NDV	36	1.400NA	OUTPUT	--		1.000MA
	NDV	35	1.331NA	OUTPUT	--		1.000MA
****	NDVR		1.024MA		--		1.000MA
	NDVR		2.309UA		--		1.000MA
	NDVR		685.2NA		--		1.000MA
	NDVR		267.7NA		--		1.000MA
	NDVR		319.4UA		--		1.000MA
	NDVR		3.567UA		--		1.000MA

Figure V.H.13 - Average Leakage Currents after -2250 volts (cont.)

FILE UID :152 SERIAL NUMBER - VARIOUS

TESTED AT 25 DEG. C N2250V STRESS
ON 13 DEC 83 AT 06:33 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		MEASURED VALUE	LIMITS MINIMUM	MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,26,27,28,29,30				
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	552.0UA	--	1.000MA
	NDVR	- - - - - - -	143.0UA	--	1.000MA
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	29.47NA	--	1.000MA
	NDVR	- - - - - - -	1.777UA	--	1.000MA
	NDVR	- - - - - - -	531.0NA	--	1.000MA
	NDVR	- - - - - - -	435.5NA	--	1.000MA
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	775.6NA	--	1.000MA
	NDVR	- - - - - - -	142.5NA	--	1.000MA
	NDVR	- - - - - - -	838.1NA	--	1.000MA
	NDVR	- - - - - - -	311.1NA	--	1.000MA
	NDVR	- - - - - - -	78.97UA	--	1.000MA
	NDVR	- - - - - - -	183.2NA	--	1.000MA
	NDVR	- - - - - - -	439.2NA	--	1.000MA
	NDVR	- - - - - - -	70.73NA	--	1.000MA
	NDVR	- - - - - - -	61.20NA	--	1.000MA
	NDVR	- - - - - - -	68.30NA	--	1.000MA
	NDVR	- - - - - - -	54.71NA	--	1.000MA
	NDVR	- - - - - - -	45.88NA	--	1.000MA
	NDVR	- - - - - - -	51.34NA	--	1.000MA
****	NDVR	- - - - - - -	1.024MA	--	1.000MA
	NDVR	- - - - - - -	125.7NA	--	1.000MA
	NDVR	- - - - - - -	83.56NA	--	1.000MA
	NDVR	- - - - - - -	62.52NA	--	1.000MA
	NDVR	- - - - - - -	163.8NA	--	1.000MA
	NDVR	- - - - - - -	73.62NA	--	1.000MA
	NDVR	- - - - - - -	172.8NA	--	1.000MA
	NDVR	- - - - - - -	186.0NA	--	1.000MA
	NDVR	- - - - - - -	6.427NA	--	1.000MA

Figure V.H.13 - Average Leakage Currents after -2250 volts (cont.)

CUMULATIVE FUNCTIONAL FAILURES	VOLTAGE LEVEL
1	-1500
2	+1750
3	+2000
5	-2000
6	+2250
10	-2250
13	+2500

Figure V.H.14 - CD Stress,
Functional Failure Summary

OPEN CONDITION	LEAKAGE CURRENT CONDITION	PIN NUMBER
	12	5
	1	14
	1	16
	2	17
	1	18
	1	19
	12	21
2	4	22
	1	23
5	0	25
4	0	26
	12	32
	10	33
	1	39

Figure V.H.15 - CD Stress, Failure Summary,
Post + 2500 Volt Stress

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :152 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P2500V STRESS
ON 13 DEC 83 AT 06:37 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		PIN	MEASURED VALUE	FUNCTION	LIMITS MINIMUM	LIMITS MAXIMUM
	PIN AVERAGE OF SERIAL NUMBERS: 17,18,19,20,21,22,23,24,26,27,28,29,30						
	NDV	- - - - - -	21	859.5UA	INPUT	--	1.000MA
	NDV	- - - - - -	17	71.81UA	INPUT	--	1.000MA
	NDV	- - - - - -	18	19.09UA	INPUT	--	1.000MA
	NDV	- - - - - -	19	9.083UA	INPUT	--	1.000MA
	NDV	- - - - - -	22	315.6UA	INPUT	--	1.000MA
	NDV	- - - - - -	23	4.611UA	INPUT	--	1.000MA
	NDV	- - - - - -	31	527.3UA	I/O	--	1.000MA
	NDV	- - - - - -	33	647.5UA	INPUT	--	1.000MA
	NDV	- - - - - -	24	2.812NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	30	552.5UA	I/O	--	1.000MA
	NDV	- - - - - -	25	1.592NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	26	1.400NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	28	1.600NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	29	1.492NA	OUTPUT	--	1.000MA
****	NDV	- - - - - -	32	1.024MA	OUTPUT	--	1.000MA
	NDV	- - - - - -	27	5.446NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	34	1.519NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	16	188.4NA	I/O	--	1.000MA
	NDV	- - - - - -	15	1.442NA	I/O	--	1.000MA
	NDV	- - - - - -	14	68.92UA	I/O	--	1.000MA
	NDV	- - - - - -	13	1.492NA	I/O	--	1.000MA
	NDV	- - - - - -	12	249.0NA	I/O	--	1.000MA
	NDV	- - - - - -	11	1.565NA	I/O	--	1.000MA
	NDV	- - - - - -	10	1.481NA	I/O	--	1.000MA
	NDV	- - - - - -	9	1.469NA	I/O	--	1.000MA
	NDV	- - - - - -	8	1.519NA	I/O	--	1.000MA
	NDV	- - - - - -	7	1.508NA	I/O	--	1.000MA
	NDV	- - - - - -	6	1.569NA	I/O	--	1.000MA
****	NDV	- - - - - -	5	1.024MA	I/O	--	1.000MA
	NDV	- - - - - -	4	1.681NA	I/O	--	1.000MA
	NDV	- - - - - -	3	1.558NA	I/O	--	1.000MA
	NDV	- - - - - -	2	1.581NA	I/O	--	1.000MA
	NDV	- - - - - -	39	78.73UA	I/O	--	1.000MA
	NDV	- - - - - -	38	1.535NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	37	1.577NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	36	1.450NA	OUTPUT	--	1.000MA
	NDV	- - - - - -	35	1.377NA	OUTPUT	--	1.000MA
****	NDVR	- - - - - -		1.024MA		--	1.000MA
	NDVR	- - - - - -		89.58UA		--	1.000MA
	NDVR	- - - - - -		79.32UA		--	1.000MA
	NDVR	- - - - - -		25.38UA		--	1.000MA
	NDVR	- - - - - -		319.3UA		--	1.000MA
	NDVR	- - - - - -		12.61UA		--	1.000MA

Figure V.H.16 - CD Stress, Leakage Current Averages After the +2500 Volt Stress

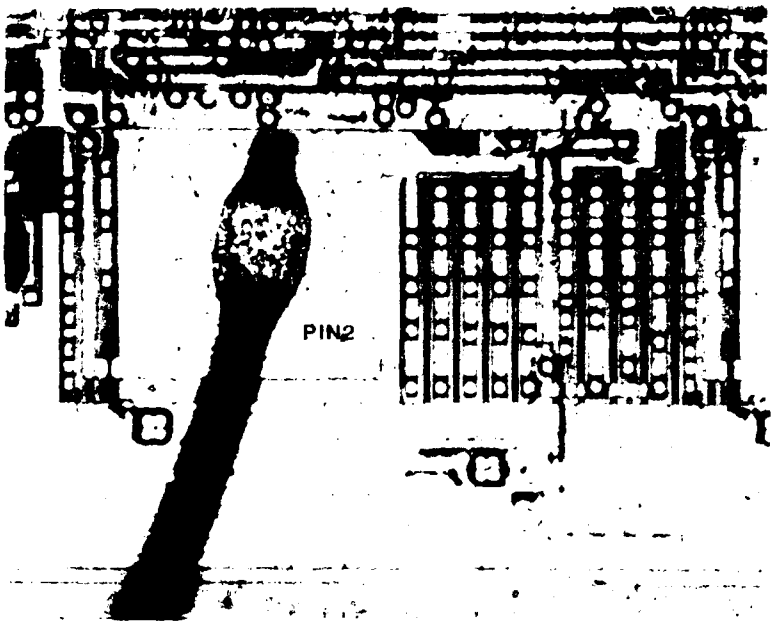


Figure V.H.17 - Pin 2 Input/Output

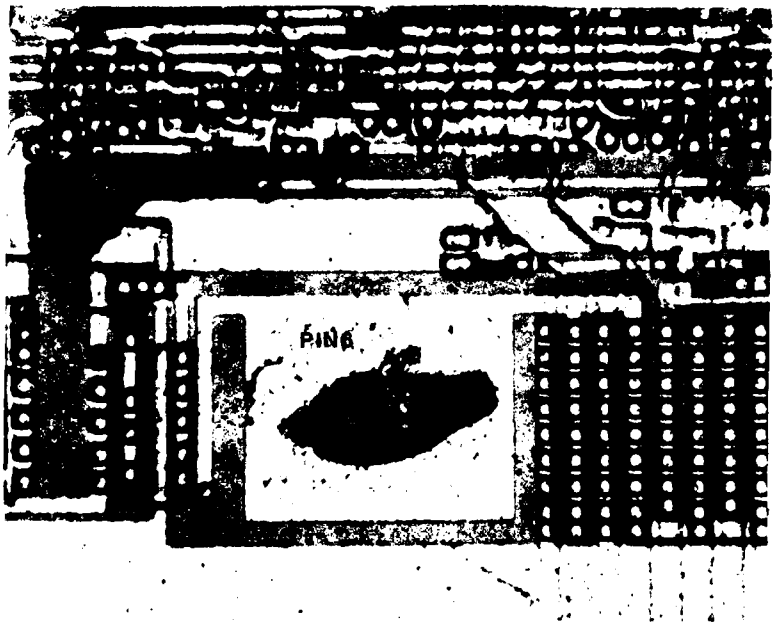


Figure V.H.18 - Pin 6 Input/Output

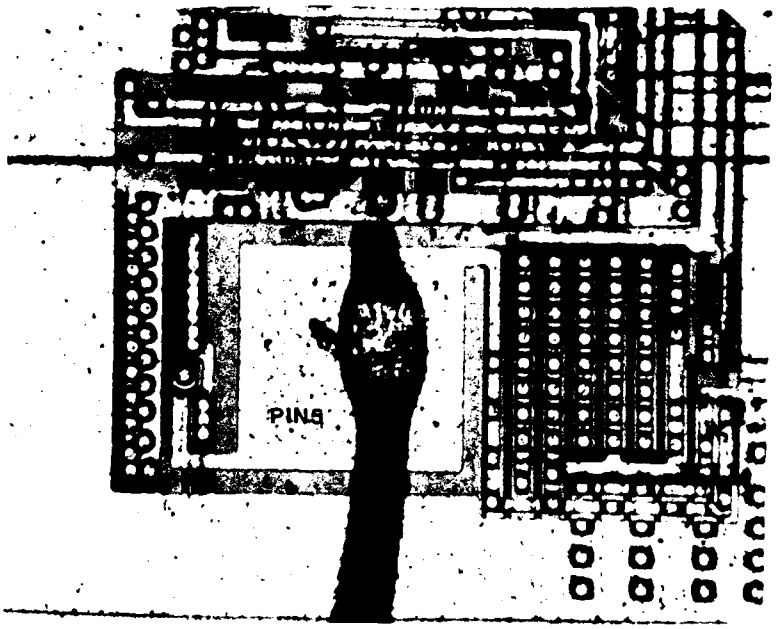


Figure V.H.19 - Pin 5 Input/Output

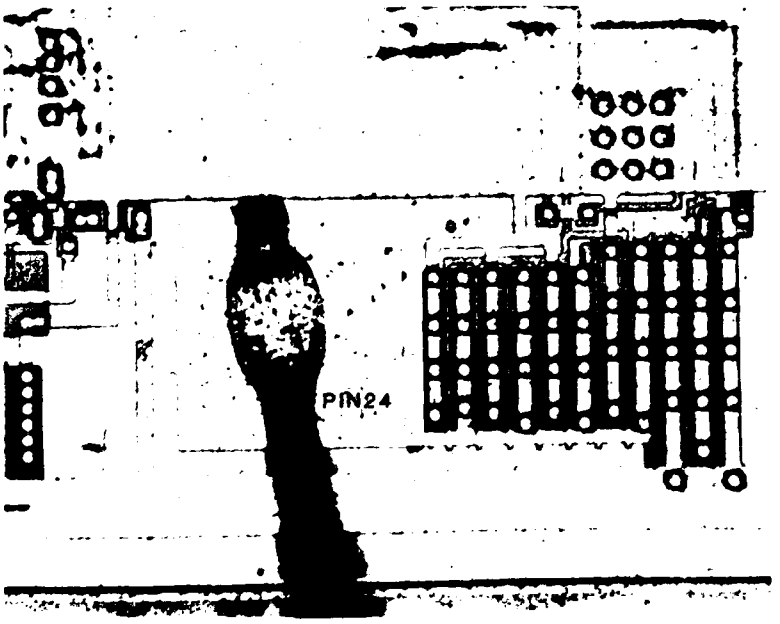


Figure V.H.20 - Pin 24 Output

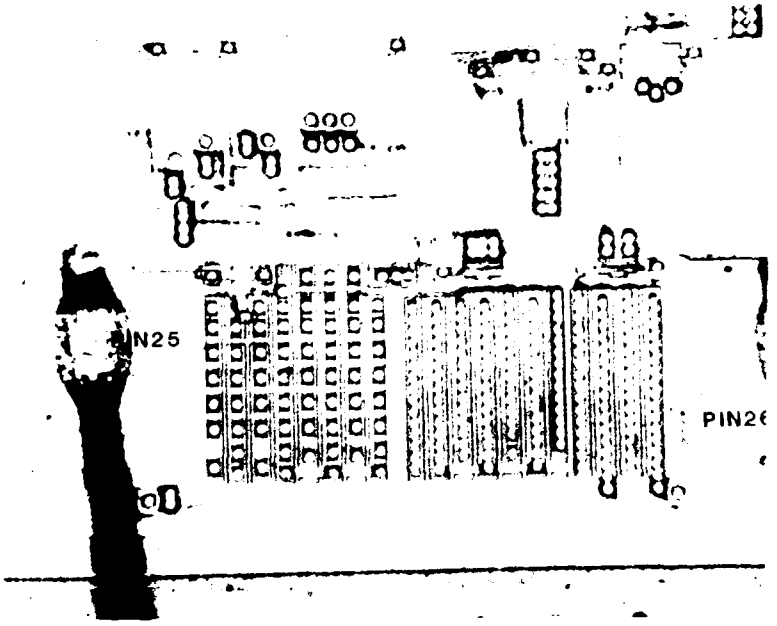


Figure V.F 21 - Output Pin 25 and 26

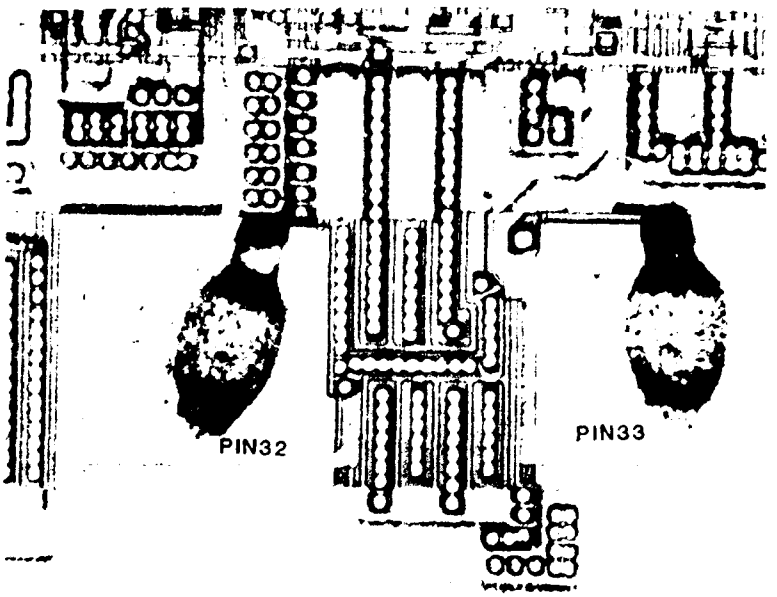


Figure V.H.22 - Output Pin 32 and Input Pin 33

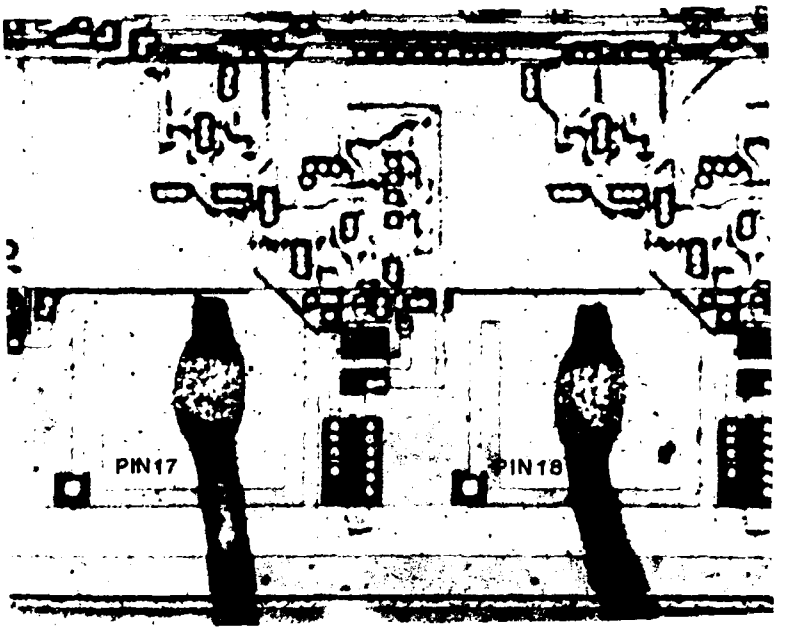


Figure V.H.23 - Input Pins 17 and 18

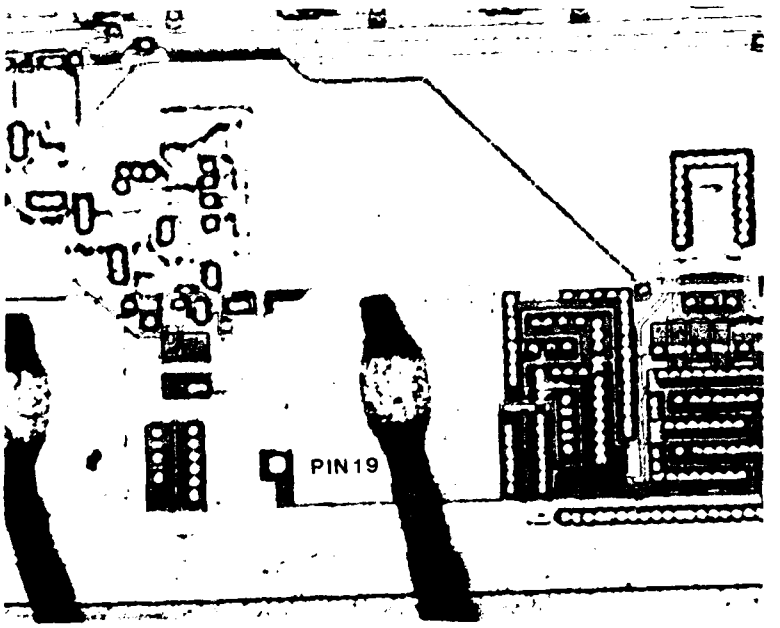


Figure V.H.24 - Pin 19 Input

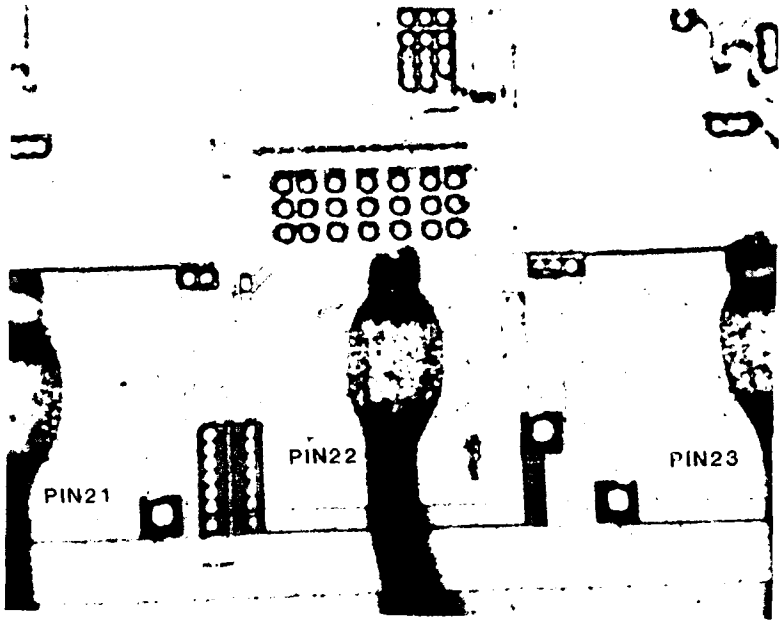


Figure V.H.25 - Pin 21, 22 and 23 Inputs

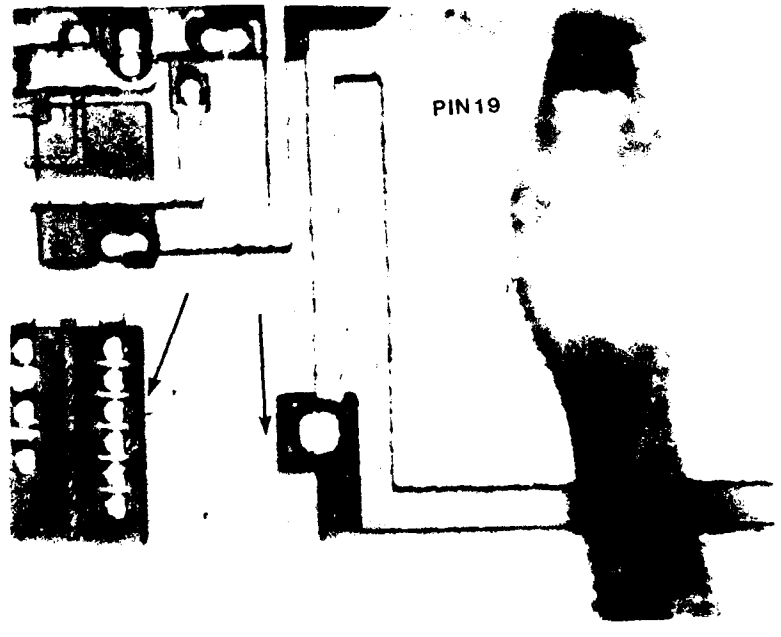


Figure V.H.26 - CD Stress, Electrical Damage from Pin 19 to Ground

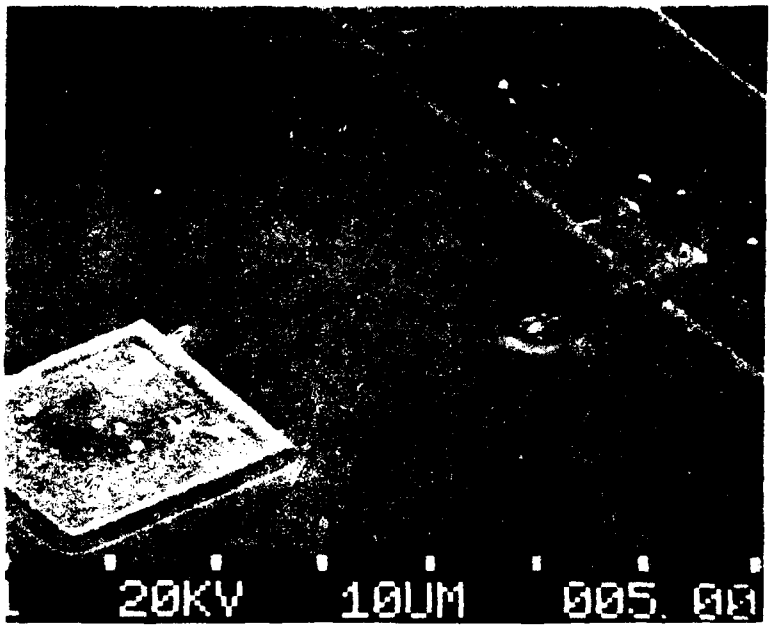


Figure V.H.27 - CD Stress, SEM Micrograph of Pin 19 Damage

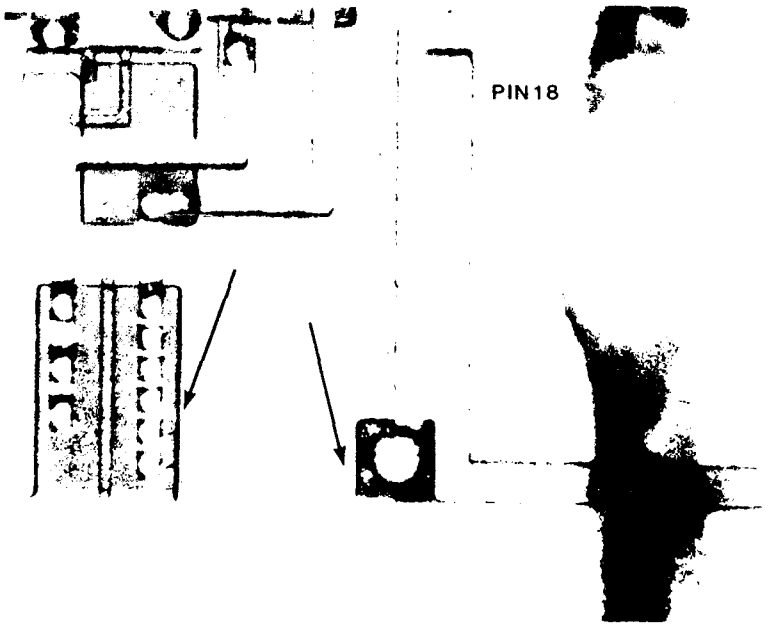


Figure V.H.28 - CD Stress, Pin 18 Degradation

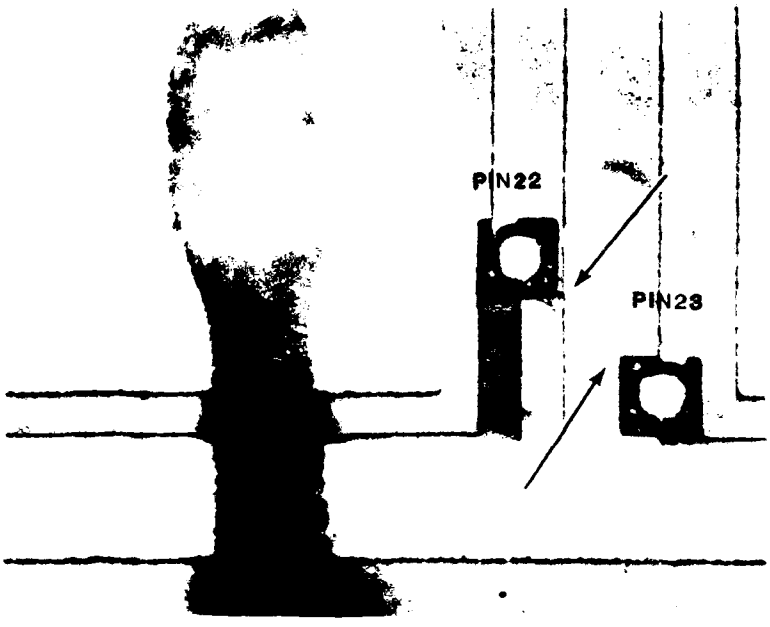


Figure V.H.29 - CD Stress, Pin 22 and Pin 23 Degradation

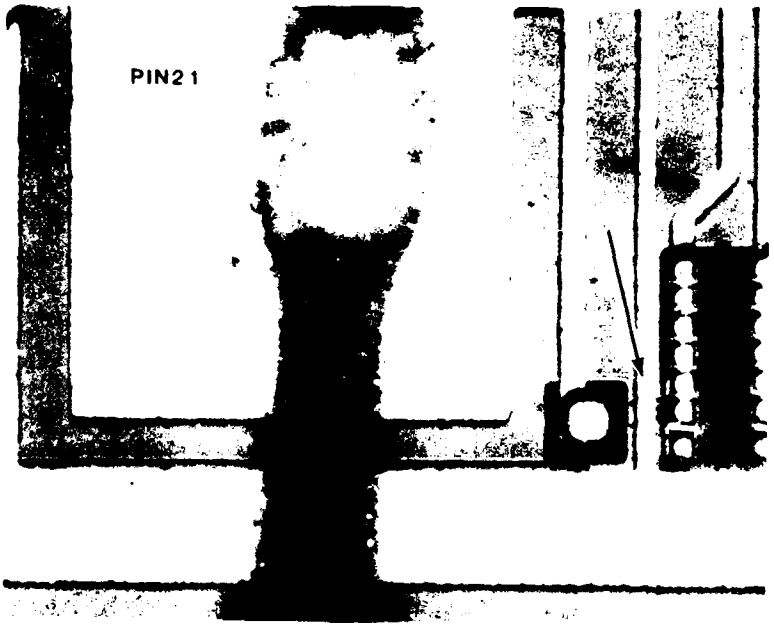


Figure V.H.30 - CD Stress, Pin 21 Damage

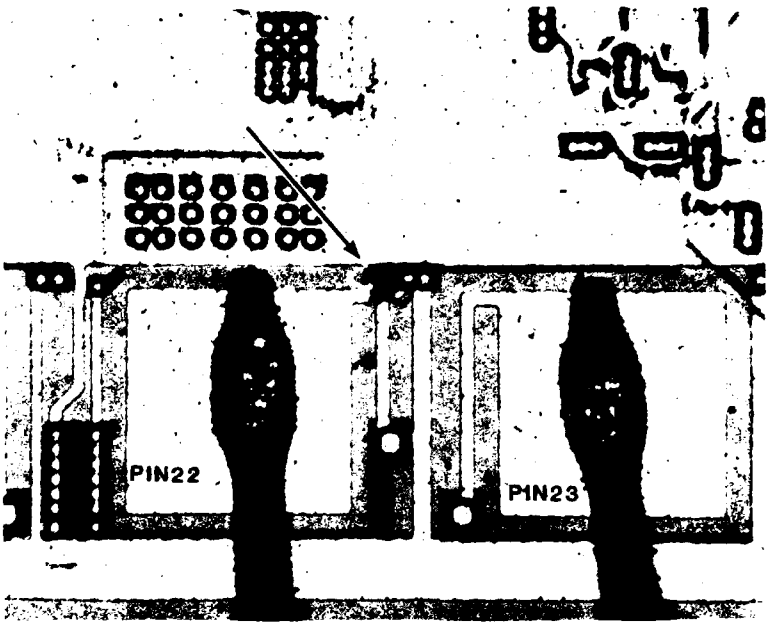


Figure V.H.31 - CD Stress, Open Metallization on Pin 22

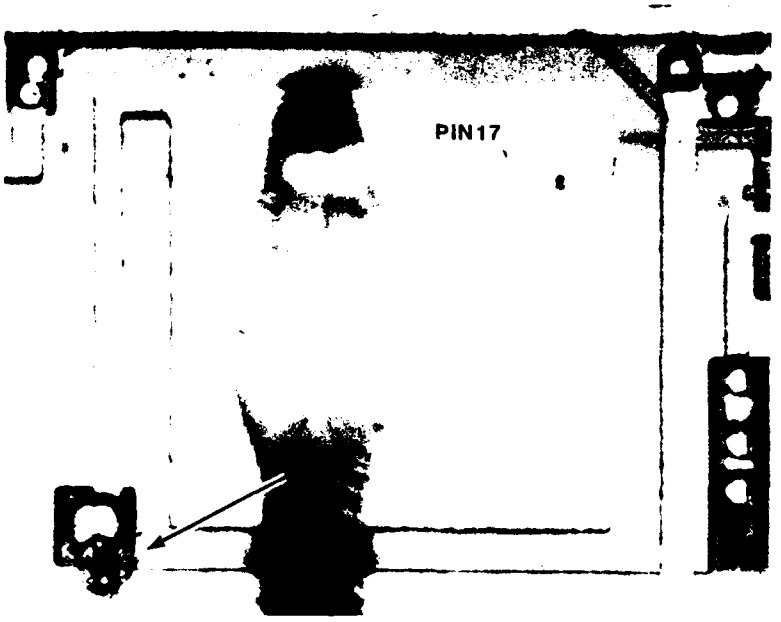


Figure V.H.32 - CD Stress, Pin 17 Shorted to Ground

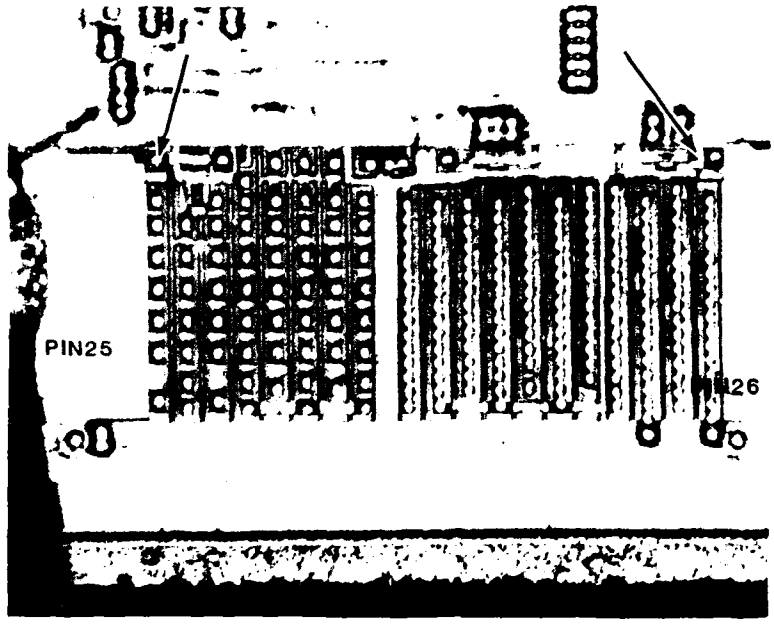


Figure V.H.33 - CD Stress, Opens on Pins 25 and 26

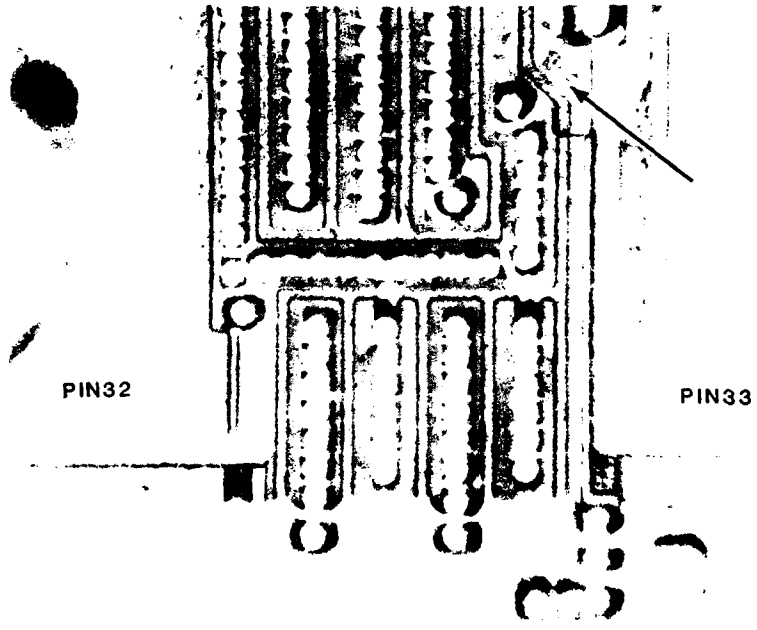


Figure V.H.34 - CD Stress, Damage Between Pins 32 and 33

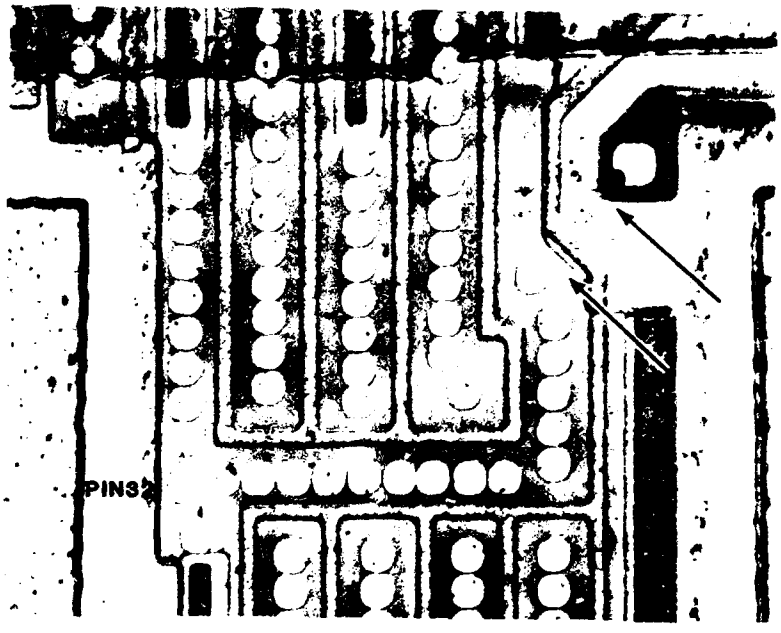


Figure V.H.35 - CD Stress, Same View as Previous Photo with Aluminum Stripped

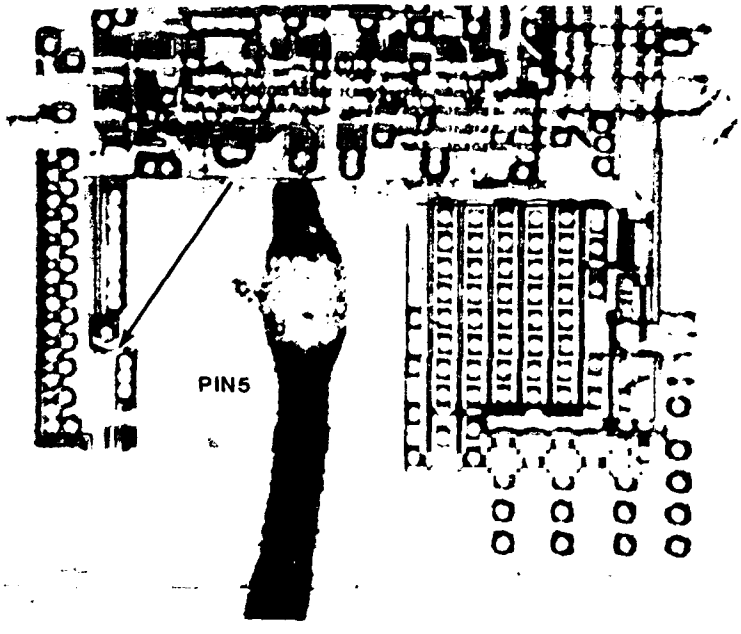


Figure V.H.36 - CD Stress, Pin 5 with Arrow Indicating *Location of Damage Site*

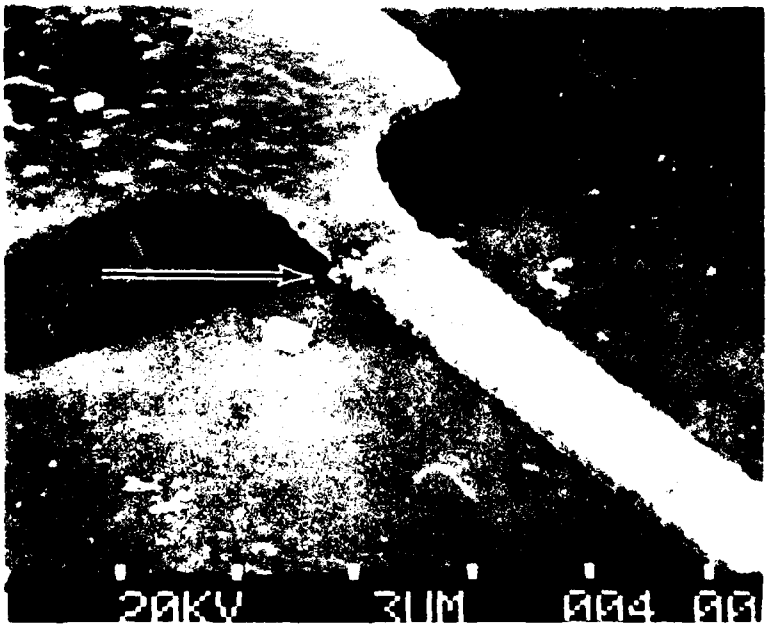


Figure V.H.37 - CD Stress, Pin 5 Polysilicon Breakdown Site

MARTIN MARIETTA AEROSPACE -- DENVER DIVISION -- PARTS EVALUATION LAB

FILE UID :152 SERIAL NUMBER - VARIOUS
TESTED AT 25 DEG. C P5000V STRESS
ON 17 DEC 83 AT 12:24 WITH THE 3260 TEST SYSTEM

FAIL	TEST TYPE		PIN	MEASURED VALUE	FUNCTION	LIMITS MINIMUM	LIMITS MAXIMUM
PIN AVERAGE OF SERIAL NUMBERS: 3,4,5,6,7,8,9,12,13,14,15,16							
	NDV	- - - - - - -	21	908.7UA	INPUT	--	1.000MA
	NDV	- - - - - - -	17	113.7NA	INPUT	--	1.000MA
	NDV	- - - - - - -	18	186.7NA	INPUT	--	1.000MA
	NDV	- - - - - - -	19	52.45NA	INPUT	--	1.000MA
	NDV	- - - - - - -	22	3.697UA	INPUT	--	1.000MA
	NDV	- - - - - - -	23	3.667UA	INPUT	--	1.000MA
	NDV	- - - - - - -	31	525.6UA	I/O	--	1.000MA
	NDV	- - - - - - -	33	1.152UA	INPUT	--	1.000MA
	NDV	- - - - - - -	24	1.554NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	30	547.7UA	I/O	--	1.000MA
	NDV	- - - - - - -	25	1.404NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	26	1.192NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	28	1.367NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	29	1.108NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	32	92.51UA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	27	1.258NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	34	6.387NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	16	18.50NA	I/O	--	1.000MA
	NDV	- - - - - - -	15	25.20NA	I/O	--	1.000MA
	NDV	- - - - - - -	14	1.263NA	I/O	--	1.000MA
	NDV	- - - - - - -	13	1.225NA	I/O	--	1.000MA
	NDV	- - - - - - -	12	1.800NA	I/O	--	1.000MA
	NDV	- - - - - - -	11	1.288NA	I/O	--	1.000MA
	NDV	- - - - - - -	10	1.188NA	I/O	--	1.000MA
	NDV	- - - - - - -	9	1.225NA	I/O	--	1.000MA
	NDV	- - - - - - -	8	1.154NA	I/O	--	1.000MA
	NDV	- - - - - - -	7	1.208NA	I/O	--	1.000MA
	NDV	- - - - - - -	6	1.233NA	I/O	--	1.000MA
	NDV	- - - - - - -	5	1.229NA	I/O	--	1.000MA
	NDV	- - - - - - -	4	1.263NA	I/O	--	1.000MA
	NDV	- - - - - - -	3	1.254NA	I/O	--	1.000MA
	NDV	- - - - - - -	2	1.279NA	I/O	--	1.000MA
	NDV	- - - - - - -	39	1.421NA	I/O	--	1.000MA
	NDV	- - - - - - -	38	1.292NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	37	1.350NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	36	1.154NA	OUTPUT	--	1.000MA
	NDV	- - - - - - -	35	1.108NA	OUTPUT	--	1.000MA
	NDVR	- - - - - - -		999.9UA		--	1.000MA
	NDVR	- - - - - - -		457.5NA		--	1.000MA
	NDVR	- - - - - - -		1.324UA		--	1.000MA
	NDVR	- - - - - - -		234.7NA		--	1.000MA
	NDVR	- - - - - - -		53.52UA		--	1.000MA
	NDVR	- - - - - - -		48.97UA		--	1.000MA

Figure V.H.38 - HBD Stress, Leakage Current Averages After the +5000 Volt Stress

LEAKAGE CURRENT	PIN NUMBER
13	21
6	22
5	23
5	32
2	33

Figure V.H.39 - HBD Stress, Leakage Current Failure Summary

(13 Parts Total)

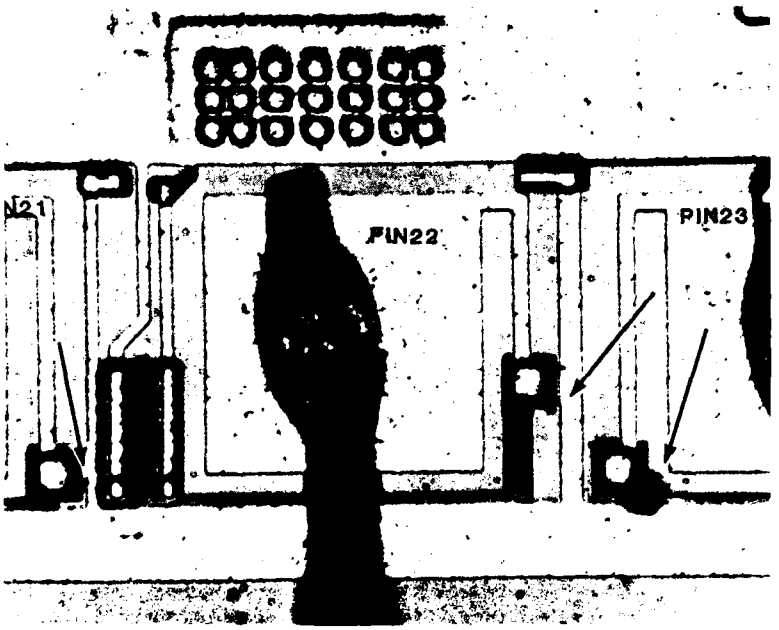


Figure V.H.40 - HBD Stress, Damage on Pins 21, 22, and 23

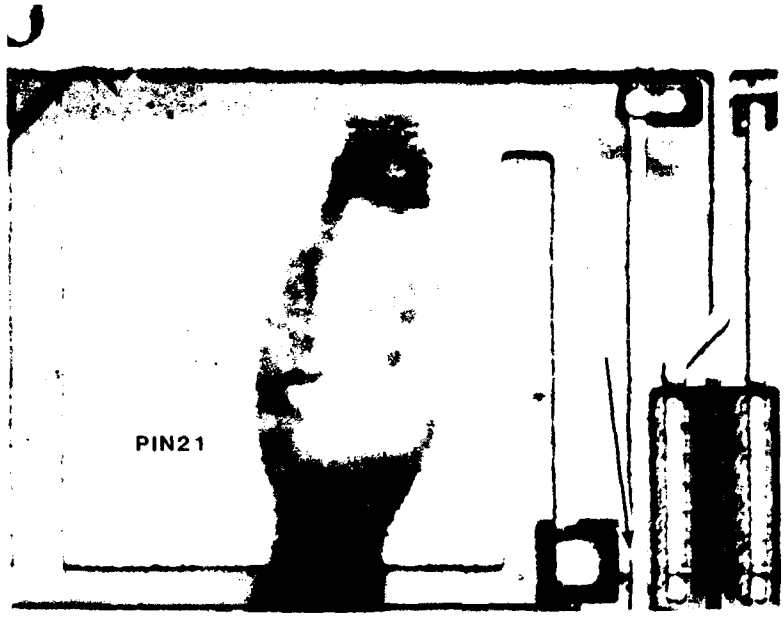


Figure V.H.41 - HBD Stress, Damage on Pin 21

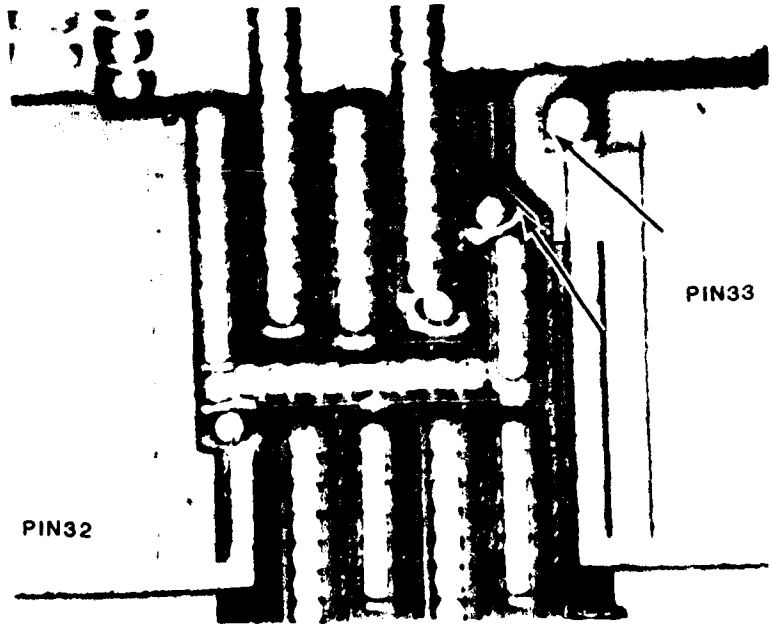


Figure V.H.42 - HBD Stress, Damage on Pins 32 and 33

VI. PROTECTION SCHEME ANALYSIS

A wide variation in the effectivenesss of protection schemes was experienced during this study. Analysis of the variations within each group of devices was included in the previous section. This section will discuss the variations between groups, the effect of reduction in dimensions, and recommendations for modifications or improvements.

Figure VI-1 shows the voltage range at which parts were removed from test for all eight groups of devices and for both types of stress. Examination of this figure reveals a number of conditions. With the exception of Part D, parts always failed at a lower level for the charged device model. There was not always the same relationship between the level of the charged device failures and the human body failures. The two groups which had the best tolerance to the HBD stress did have the best tolerance to the CD stress, however, the other parts did not follow this pattern. Part G was very sensitive to the CD stress but was relatively high in tolerance to the human body stress. This is due to the significant effect of the package size on the CD stress. The Part G devices were in the largest package and had the highest capacitance to ground. This created a much higher stress for the same voltage level.

A more quantitative display of the data in the above figure is provided in Figures VI-2 through VI-8. These figures show comparisons of the cumulative failures by manufacturer, by technology, and by functional type.

One manufacturer had two device types in this study. These were Part E and Part H and are shown in Figure VI-2. Similar trends are shown for both devices with the Part H being the more tolerant. These were the two best protection networks found in this study. The major difference was a polysilicon pad between the bond pad metallization and the diffused resistor on Part H. This reduced the development of leakage current. The basic layout was a diffused n-type resistor connected to a thin oxide transistor which had its gate and source connected to ground. The low sensitivity was due to the lack of a return current path due to the resistor being in a diffusion connected to substrate (internal connection only). Note that all devices did not fail during the human body model testing.

Figure VI-3 shows the summary for the four NMOS devices. This includes the devices shown in Figure VI-2 and also Part G and Part B. The four NMOS devices have substrate bias generators and diffused input protect resistors. These resistors measure 650 ohms for Part B, 550 ohms for Part E, 900 ohms for Part G, and 700 ohms for Part H. Part B has the most elaborate input protect network and includes a thick oxide metal gate transistor to VCC or VSS, and a field plate diode to the substrate. Part G failed at a lower level for the charged device model than Part B but Part B is still the weakest NMOS protection system as shown by the human body model. Part B received a lower stress for the charged device model than Part G for the physical reasons discussed previously.

Part E has a thin oxide polysilicon transistor to VSS and Part G and H have thin oxide polysilicon transistors to ground (VSS and ground are essentially the same). Part G and Part H have polysilicon interfaces between the bond pad metallization and the diffused resistor. There is a major difference in this polysilicon interface that makes Part H less susceptible to damage. The polysilicon on Part G is like a resistor between the diffusion and the metallization and tends to fail open. The polysilicon on Part H is sandwiched between the metallization and the diffused resistor contact and does not fail open. This figure shows a wide range of sensitivity and it indicates the type of protection which should be used. The thin oxide field plate on Part B should be removed and the distance between the source and drain on the thick oxide transistor should be increased. This increase would create a situation similar to that seen on the less sensitive inputs on Part H. The gate appears to provide no benefit since if it were removed the input would be more similar to the less sensitive Part H or Part E.

Figure VI-4 shows the cumulative failures for the two microprocessors. These were discussed in the last section.

Figure VI-5 shows the cumulative failures for the two CMOS devices. It is evident that these parts did poorly in the sensitivity testing. Both devices utilized polysilicon input resistors which created a weak system. In addition Part F had numerous different layouts and aluminum/polysilicon crossovers. Polysilicon resistors are not recommended for complex circuit input networks.

Figure VI-6 shows the cumulative failures for the two low power Schottky devices. Part D is more tolerant to stress and it appears that this is size related. The Schottky diode was much larger on Part D and consequently it was not as sensitive to stress. For the human body model the base-collector junction failed on Part D before the Schottky junction. This produced the higher voltage levels seen in Figure VI-6 for the human body stress. The charged device stress produced failure in the Schottky junction on both devices but Part D failed at a higher level. The recommendations for Schottky technology devices include increasing the size of the Schottky contact and/or placing the input base-collector junction between the input contact and the Schottky reverse bias protection diode.

Figure VI-7 shows the cumulative failures for the two RAM, I/O, Timers. Part A is CMOS and Part E is NMOS. The CMOS had the polysilicon input resistors and was sensitive to stress.

Figure VI-8 shows the cumulative failures for the two RAMs. Part F had the polysilicon input resistors and Part B had the close spaced thick oxide transistor and the field plate diode. The sensitivity variations are due to reasons previously discussed.

A number of the conventional schemes that are available have been seen on the devices in this study. The literature search found a number of other possibilities which are summarized below:

1. "Multiple I/O Protection with Single Protective Device" S. Chen, S. Park, R. Wong, IBM Tech. Disclosure Bulletin; September 1980.

   Rather than conventional protection devices on each input, this article discusses using a depletion or enhancement transfer device on each input with their gates tied back to a common protective device.

2. "Voltage Programmable Protect Circuit" C. Hoffman and F. Wiedman, IBM Tech. Disclosure Bulletin, March 1980.

   A protect circuit is described for an electrically programmable read-only memory which allows a high voltage to be placed on a pin for programming, but limits the voltage level at that pin during normal usage by a protect diode with a gate over it to allow reverse bias breakdown voltage control.

3. "Floating Plate Protective Device" Y. S. Huang, IBM Tech. Disclosure Bulletin, April 1977.

   This article discusses a floating capacitor design which has a large capacitor above a diffusion which is connected to the input metallization. Via a second diffusion this capacitor is normally isolated but if an excessive voltage is present on an input then the capacitor is connected into the circuit and absorbs the extra charge.

4. "Voltage Breakdown Characteristics of Close Spaced Aluminum Arc Gap Structures on Oxidized Silicon" F. Hickernell and J. Crawford, Reliability Physics Symposium 1977.

   Arc gap structures were investigated as possible input protection networks. They have the advantage of being a nondestructive voltage limiting structure that can limit the voltage to 300 to 400 volts.

These ideas are a few that are being or have been considered for device protection against transients.

Additional ideas that could improve protection networks and be compatible with VLSI processing have been thought of during this work. Two of these are tungsten contact to the silicon and a deep insulator grown around the input protect resistor.

The tungsten contact would alleviate the aluminum silicon interdiffusion problem by acting as a barrier similar to the polysilicon interface. It should have less of a tendency to open with stress. It can also be useful in the remainder of the circuit by being the barrier contact to shallow source and drain diffusions and it can be selectively deposited on the polysilicon to reduce the effective resistance. This idea seems practical and could provide improved circuit performance as well as decreased sensitivity to stress.

A deep insulator grown on either side of the input resistor would force the current to flow through the diffused resistor or break down the junction in the bulk. This should provide an input that protects the sensitive gates as well as not degrading itself due to this stress.

The sections for each of the eight devices discussed the ESD sensitivity variations for the various pins on a given part. The preceding section discussed the sensitivity variations between the different groups. The following will discuss the variations by physical characteristics. These physical characteristics include, conductor cross-sectional area, junction area, dielectric thickness, conductor spacing, junction electrical breakdown characteristics, overall device layout, physical construction and packaging.

These physical characteristics are discussed here and are related to the failures which occurred.

Conductor cross-sectional area was seen to be a problem on devices with polysilicon input resistors. These were devices A, F, and G. This was a significant failure mode on Part Types A and G. Part Type A has a polysilicon cross-sectional area of 1.6 microns squared and Part Type G has a polysilicon cross-sectional area of 2.2 microns squared. The average voltage failure level for the human body simulation stress was about twice as high on Part Type G as on Part Type A. There were oth failure modes involved on both parts but the relationship between the voltage failure level and the cross-sectional area of the polysilicon does appear to be significant. For the charged device testing other factors override this one, eg. package size.

Junction area was significant on the two Schottky devices. It is not considered to be the significant factor in the other device failures, however, the spacing and shape of the diffusions were shown to be significant as discussed in-depth previously. The significance is again evident for the human body simulation but is not the controlling factor for the charged device test.

The base-collector junction failed on Part Type D. The width of the contact to the base was 13 microns. The Schottky diode failed on Part Type C. The width of the contact was 9 microns. Part Type D with a contact width of 13 microns failed at about twice the voltage level of Part Type C. The Schottky diode did not fail due to this stress on Part Type D because of its large, 39 micron, width.

Dielectric thickness was a significant factor in the failures on Part Types A, B, and F. These failures were, on Part A, polysilicon to polysilicon breakdown between closely spaced stripes on the same level, and polysilicon layer to layer shorts. On Part B, this was a thin oxide dielectric breakdown. On Part F there were polysilicon to overlying metallization and polysilicon to underlying silicon shorts. The thicknesses involved were: Part A poly to poly = 0.1 microns, Part B thin

oxide estimated to be 500 Angstroms, Part F poly to metal and poly to silicon both 0.5 microns. The lowest failure levels occurred on Part F. This is believed to be due to oxide defects rather than to the nominal dielectric thickness. The thin dielectric on Part A was a major cause for the relatively low failure levels. As discussed, routing changes could alleviate this. The dielectric failures on Part B were due to the thin oxide structure utilized. Quantitative comparison of the oxide thicknesses to failure level provides little information.

Conductor spacing was a significant factor on Part A due to close polysilicon spacing as mentioned above. A routing change could correct this.

Junction electrical breakdown characteristics were measured on each of the eight devices. A listing of the breakdown voltage looking into the input for each device is given here. Part A = 30VDC, Part B = 22 VDC, Part C = 28 VDC, Part D = 20 VDC, Part E = 28 VDC, Part F = 25 VDC, Part G = 22 VDC, Part H = 18 VDC. Other factors override these in controlling ESD sensitivity.

Overall device layout was seen to be an important factor which determined device sensitivity. The layouts which were analyzed included: metallization pattern, diffusion spacing and shape, and polysilicon patterns. Two effects were evident related to the metallization. Points which were connected to large metallization areas showed sensitivity to the CD stress. This created failure mode and stress level sensitivity differences in Parts D, G and H. On Part D the failure mode was a different junction for the human body stress than for the charged device stress due to a large ground metallization connected to one junction. This junction failed for the CD stress because it received a larger stress. Parts G and H had specific pins which were much more sensitive to the CD stress due to metallization layout. The second effect was longer metallization runs decreased sensitivity. This was seen on Parts B and C. This is due to a distributed capacitance and/or inductance effect.

Diffusion spacing and shape was an important factor on Parts B, E, and H. It was found that the pin or pins that failed had closer spacing and corners between adjacent n+ diffusions. Quantitatively this spacing was: Part B = 2 microns, Part E = 26 microns, and Part H = 5 microns. The failure levels for E and H were much higher than for B, however Part H was higher than Part E. This indicates that spacing is important but more important for Part H was likely the polysilicon interface pad between the metallization and the silicon.

The effect of the physical construction and packaging on the device sensitivities is the last area to be discussed. All devices analyzed were in CERDIPs. There are two effects that likely occurred, however, they are not the controlling factor for sensitivity. These two effects are a decrease in sensitivity due to the longer lead frame lengths on the large packages and an increase in capacitance to ground for the charged device stress due to the additional area on these larger devices.

Recommendations

This study has shown how device sensitivities vary with the type of stress applied and with pin to pin physical differences.

An important result is the demonstration of the similarities and differences in device damage and sensitivity between the charged device simulation and the human body simulation. The charged device simulation produces damage at a lower level to pins that are connected to large expanses of metallization. An understanding of this effect could result in a reduced sensitivity to ESD at IC design by appropriate metallization layout.

The charged device test method has been shown to produce results which are consistent with ESD stress failures and it is recommended for the simulation of ESD on integrated circuits.

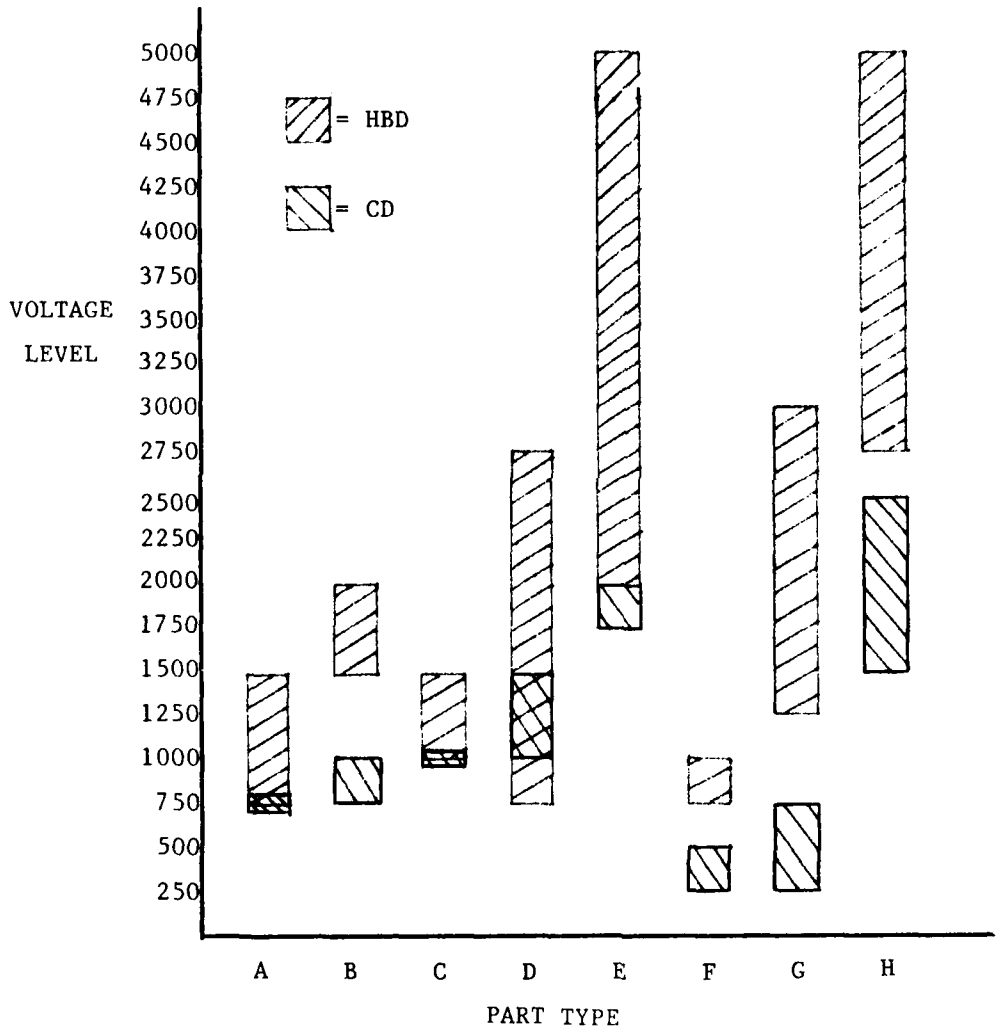


Figure VI-1 - Failures by Voltage Level For Each Part And For Both The Charged Device And Human Body ESD Models.

VOLTAGE	PART E	PART H
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		14
-2250		11
+2250		7
-2000		6
+2000	14	4
-1750	4	
+1750	1	2
-1500		1
+1500		
-1250		
+1250		
-1000		
+1000		
-750		
+750		
-500		
+500		
-250		
+250		

CHARGED DEVICE MODEL

VOLTAGE	PART E	PART H
-5000		3
+5000		
-4750	11	
+4750		
-4500	9	
+4500		2
-4250	8	
+4250		
-4000	7	
+4000		
-3750	5	
+3750	3	
-3500		
+3500		
-3250		
+3250	2	
-3000		
+3000		
-2750		
+2750		1
-2500		
+2500		
-2250		
+2250		
-2000		
+2000	1	
-1750		
+1750		
-1500		
+1500		
-1250		
+1250		
-1000		
+1000		
-750		
+750		
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-2 - Cumulative Failures for the Parts from Manufacturer A

VOLTAGE	B	E	G	H
-5000				
+5000				
-4750				
+4750				
-4500				
+4500				
-4250				
+4250				
-4000				
+4000				
-3750				
+3750				
-3500				
+3500				
-3250				
+3250				
-3000				
+3000				
-2750				
+2750				
-2500				
+2500				14
-2250				11
+2250				7
-2000				6
+2000		14		4
-1750		4		
+1750		1		2
-1500				1
+1500				
-1250				
+1250				
-1000				
+1000	15			
-750			15	
+750	8		12	
-500			11	
+500			6	
-250			1	
+250				

PART TYPE

CHARGED DEVICE MODEL

VOLTAGE	B	E	G	H
-5000				3
+5000				
-4750		11		
+4750				
-4500		9		
+4500				2
-4250		8		
+4250				
-4000		7		
+4000				
-3750		5		
+3750		3		
-3500				
+3500				
-3250				
+3250		2		
-3000				
+3000			15	
-2750			14	
+2750			11	1
-2500			6	
+2500				
-2250			5	
+2250				
-2000	15			
+2000	14	1		
-1750				
+1750	7			
-1500				
+1500	2			
-1250			2	
+1250				
-1000				
+1000				
-750				
+750				
-500				
+500				
-250				
+250				

PART TYPE

HUMAN BODY MODEL

Figure VI-3 - Cumulative Failures for the NMOS Devices

VOLTAGE	PART G	PART H
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		14
-2250		11
+2250		7
-2000		6
+2000		4
-1750		
+1750		2
-1500		1
+1500		
-1250		
+1250		
-1000		
+1000		
-750	15	
+750	12	
-500	11	
+500	6	
-250	1	
+250		

CHARGED DEVICE MODEL

VOLTAGE	PART G	PART H
-5000		3
+5000		
-4750		
+4750		
-4500		
+4500		2
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000	15	
-2750	14	
+2750	11	1
-2500	6	
+2500		
-2250	5	
+2250		
-2000		
+2000		
-1750		
+1750		
-1500		
+1500		
-1250	2	
+1250		
-1000		
+1000		
-750		
+750		
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-4 - Cumulative Failures for the Two Microprocessors

VOLTAGE	PART F	PART A
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		
-1750		
+1750		
-1500		
+1500		
-1250		
+1250		
-1000		
+1000		
-750		15
+750		5
-500		
+500	15	
-250	8	
+250	4	

CHARGED DEVICE MODEL

VOLTAGE	PART F	PART A
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		
-1750		
+1750		
-1500		15
+1500		5
-1250		4
+1250		
-1000	15	
+1000		2
-750	9	1
+750	5	
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-5 - Cumulative Failures for the Two CMOS Devices

VOLTAGE	PART C	PART D
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		
-1750		
+1750		
-1500		
+1500		14
-1250		10
+1250		
-1000	15	2
+1000	3	
-750		
+750		
-500		
+500		
-250		
+250		

CHARGED DEVICE MODEL

VOLTAGE	PART C	PART D
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		12
-2500		
+2500		8
-2250		
+2250		4
-2000		
+2000		
-1750		
+1750		
-1500		
+1500	15	
-1250		
+1250	5	
-1000		
+1000	3	
-750		
+750		2
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-6 - Cumulative Failures for the Two Schottky Devices

VOLTAGE	PART A	PART E
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		14
-1750		4
+1750		1
-1500		
+1500		
-1250		
+1250		
-1000		
+1000		
-750	15	
+750	5	
-500		
+500		
-250		
+250		

CHARGED DEVICE MODEL

VOLTAGE	PART A	PART E
-5000		
+5000		
-4750		11
+4750		
-4500		9
+4500		
-4250		8
+4250		
-4000		7
+4000		
-3750		5
+3750		3
-3500		
+3500		
-3250		
+3250		2
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		1
-1750		
+1750		
-1500	15	
+1500	5	
-1250	4	
+1250		
-1000		
+1000	2	
-750	1	
+750		
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-7 - Cumulative Failures for the Two RAM, I/0, Timers.

VOLTAGE	PART B	PART F
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000		
+2000		
-1750		
+1750		
-1500		
+1500		
-1250		
+1250		
-1000		
+1000	15	
-750		
+750	8	
-500		
+500		15
-250		8
+250		4

CHARGED DEVICE MODEL

VOLTAGE	PART B	PART F
-5000		
+5000		
-4750		
+4750		
-4500		
+4500		
-4250		
+4250		
-4000		
+4000		
-3750		
+3750		
-3500		
+3500		
-3250		
+3250		
-3000		
+3000		
-2750		
+2750		
-2500		
+2500		
-2250		
+2250		
-2000	15	
+2000	14	
-1750		
+1750	7	
-1500		
+1500	2	
-1250		
+1250		
-1000		15
+1000		
-750		9
+750		5
-500		
+500		
-250		
+250		

HUMAN BODY MODEL

Figure VI-8 - Cumulative Failures for the Two RAMs

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RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

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