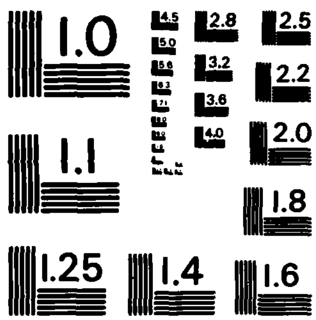
AD-A147 798 LIFE CYCLE COST MODEL FOR VERY HIGH SPEED INTEGRATED CIRCUITS(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF SYSTEMS AND LOGISTICS E A LONG SEP 84 1/3

UNCLASSIFIED AFIT/GLM/LSM/84S-39 F/G 14/1 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

LIFE CYCLE COST MODEL FOR VERY

HIGH SPEED INTEGRATED CIRCUITS

THESIS

E. Andrew Long
Captain, USAF

AFIT/GLM/LSM/84S-39

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

2

AFIT/GLM/LSM/84

LIFE CYCLE COST MODEL FOR VERY

HIGH SPEED INTEGRATED CIRCUITS

THESIS

E. Andrew Long
Captain, USAF

AFIT/GLM/LSM/84S-39

Approved for public release; distribution unlimited

The contents of the document are technically accurate, and no sensitive items, detrimental ideas, or deleterious information are contained therein. Furthermore, the views expressed in the document are those of the author(s) and do not necessarily reflect the views of the School of Systems and Logistics, the Air University, the United States Air Force, or the Department of Defense.

AFIT/GLM/LSM/84S-39

LIFE CYCLE COST MODEL FOR VERY HIGH SPEED INTEGRATED CIRCUITS

THESIS

Presented to the Faculty of the School of Systems and Logistics

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Logistics Management

E. Andrew Long, B.S.

Captain, USAF

September 1984

Preface

The purpose of this study was to use existing cost models for microcircuits, hardware, and logistics support to estimate and analyze life cycle costs (LCC) for insertion of Very High Speed Integrated Circuit (VHSIC) technologies into future avionics systems. The impact of VHSIC on the LCC of avionics systems is relatively unknown. Therefore, a need existed for a cost estimating model that can estimate LCC for various technologies, designs, and layout configurations of VHSIC chips.

A LCC model spanning the life cycle phases of a typical avionics system was developed using RCA PRICE (Programmed Review of Information for Costing and Evaluation) cost models. First, PRICE M (Microcircuit) was used to estimate the development and production costs of VHSIC technology. Next, PRICE H (Hardware) estimated integration and test costs for assembling VHSIC chips on to printed circuit boards (PCB) and assembling PCBs into the finished system. Finally, PRICE L (LCC) provided operations and maintenance costs for the deployed system. The representative avionics system was a digital synthetic aperature radar (SAR) processor. The VHSIC factors examined were 1) chip technology and design, 2) fabrication yields, 3) substrate type, 4) the use of computer-aided-design (CAD), and 5) maintenance level.

All results of this study apply only to the memory-intensive SAR processor used as the insertion model. The major cost drivers are chip fabrication yields, level of maintenance, and the use of silicon-on-saffire rather than bulk silicon chip substrates. Design related items such as the use of CAD in the chip design process, and the use of gate array rather than custom chip layouts make negligible difference. For systems similar to the SAR processor, VHSIC planners should emphasize chip fabrication yields and maintenance support concepts. VHSIC chip design and substrate type can be important although they appear to be system dependent.

In performing the research, modeling, and writing of this study, I have had a great deal of help from others. I am indebted to Major R.C. Byler, my faculty advisor, who guided me toward the research objective. Also, I wish to thank Lieutenant Colonel Harold W. Carter of the AFIT Engineering School who provided many hours of patient help in interpreting and understanding the insertion model and VHSIC technologies. A word of thanks is also owed to Lieutenant Colonel John A. Long, and Mr. Daniel V. Ferens for their assistance during the LCC modeling stages. Finally, I wish to thank the gifted and extremely competent typist who prepared this report, Mrs. Carol Y. Long, my loving wife. I would not be graduating but for her understanding and dedicated work.

E. Andrew Long

Table of Contents

Page

List of Figures

List of Tables

Page

AFIT/GLM/LSM/84S-39

Abstract

The Very High Speed Integrated Circuit (VHSIC) technology program is forecast to have a profound impact on performance, reliability, and cost of future avionics systems. An important question is "how do VHSIC design fabrication and support concepts impact life cycle cost (LCC) of a host system?" To answer this question, an insertion model representative of future avionics systems is selected and LCCs are obtained for various chip designs and layout configurations which implement this model. Five factors affecting VHSIC chips are examined with respect to LCC of a digital synthetic aperture radar processor. These factors are 1) chip technology and design, 2) fabrication yields, 3) substrate type, 4) the degree to which computer-aided-design (CAD) methods are used, and 5) maintenance level. Of these factors, the greatest impact to LCC is chip fabrication yields. The least effect on LCC is the degree to which CAD methods are used. The remaining factors fall between these two.

LIFE CYCLE COST MODEL FOR VERY

HIGH SPEED INTEGRATED CIRCUITS

I. Introduction

In today's complex defense environment, great emphasis is placed on the development and acquisition of weapon systems and weapon system subassemblies that provide the most for each dollar (19:2-16). The Very High Speed Integrated Circuit (VHSIC) Program is a Department of Defense (DoD) effort to provide a new generation of integrated circuits (IC) which will include higher throughput, smaller size, lower weight, reduced volume, lower power consumption, increased availability, and potentially lower cost (3). However, the cost of VHSIC technology is an area of considerable uncertainty in 1984 (27:338).

If Program Managers and planners are to have a reasonable basis for assessing potential costs of VHSIC insertion, managers need a modeling technique to estimate life cycle cost (LCC) for VHSIC chips and VHSIC brassboard designs — prototype hardware design using VHSIC designed chips.

Problem Statement

A need exists for a cost estimating model that can estimate and analyze LCC for VHSIC gate array designs (off-the-shelf multipurpose design) and VHSIC custom designs (unique application design) as a function of technology, design parameters, production parameters, and logistic support concepts of VHSIC chips and VHSIC brassboard designs.

Background

Acclaimed as the most ambitious and probably the most important federal program since space exploration, the DoD VHSIC program is administered and monitored by all three services (38:203).

Beginning in the mid 1980s, vastly more complex and capable semiconductor integrated circuits (IC) will flow from the program. They will be designed specifically to handle military tasks such as detecting, recognizing and classifying targets through background clutter. They will be used in new systems or retrofitted into existing ones. Bulky blackboxes will be reduced to the size of one or two chips or a single circuit board. Fault-tolerance, with built-in test capabilities and self repair circuit redundancy, will improve weapon system reliability and reduce operating and support costs. Based upon the commercial Very Large Scale Integration (VLSI) development of ICs characterized by high density, low cost, high reliability, standard chip sets, and self diagnostics, VHSIC applications will additionally concentrate on military considerations of radiation hardness, thermal tolerance, and 50 to 100 times greater throughput rate (21:48-50, 4).

The price of VHSIC technology is an area of considerable uncertainty in 1984. The VHSIC program (launched in 1979 for 225 million dollars) is projected to cost over a half billion dollars (1981 constant dollars) when fully completed in 1987. The Pentagon has added 300 million dollars to the FY 1984-89 budget to reduce contractor risk for using new equipment — Computer Aided Design (CAD) and Computer Aided Manufacturing (CAM) -- and to increase manufacturing yield (percentage of chips in a given process that perform to specification). According to Edith W. Martin, Deputy Under Secretary of Defense for Research and Advanced Technology, these additional investments are intended to reduce the cost of VHSIC logic chips from 4000 to 5000 (1983 constant) dollars apiece in 1984-85 to less than 500 dollars each by 1987 (27:338). However, Westinghouse (one of six VHSIC prime contractors) estimates the cost per logic chip in 1987 to be over 1000 (1983 constant) dollars (3). These projections differ by a factor of two in the estimated cost of a VHSIC logic chip in 1987. The extent of this variation makes credible and accurate cost estimates difficult for systems likely to use VHSIC technology. Hence, the absence of a credible cost estimating technique to predict VHSIC LCC could deter Program Managers from seriously considering a VHSIC based design, because the DoD Acquisition Improvement Program places the responsibility for evaluating, quantifying, and budgeting technological risks on Program Managers (15:11).

Research Objective

Recently, Aeronautical Systems Division (ASD) Advanced Air-to-Surface Missile (AASM) system, Project Office indicated a need for a model to estimate and analyze LCC for brassboard designs using gate array design VHSIC chips, custom design VHSIC chips, or a mix of gate array and custom VHSIC design chips. However, as part of a separate effort, ASD/ACCR has begun a ten month effort to develop a

VHSIC Cost Estimating Relationship (CER) model to estimate VHSIC chip development and production costs. This project is scheduled for completion in June, 1984. Therefore, the objective of this thesis is not to develop a new cost estimating model, but instead to use existing models that can be modified or implemented directly to estimate and analyze LCC for insertion of VHSIC Phase 1 technology. (The reader is referred to Chapter II for a detailed discussion on the objectives and purpose of VHSIC Phase 1 technology).

Research Questions

The following research questions are posed to guide the research toward the stated objective:

1. What is LCC modeling, and how does it apply to DoD and the Air Force?
2. What are the cost estimating techniques used for LCC modeling?
3. Are there models currently available that estimate LCC for integrated circuits and how is access obtained to these models and their documentation?
4. What are the objectives of the VHSIC Program and VHSIC Phase 1 technology?
5. How can an existing model or a combination of existing models be implemented to estimate and analyze LCC for insertion of VHSIC Phase 1 technology?
6. What type of insertion model is needed to characterize the capabilities of VHSIC Phase 1 technology?
7. What are the data that must be collected and in what format must the data be collected?
8. Where can these data be collected and what are limitations for collecting these data?
9. How sensitive is the insertion model's LCC to changes in VHSIC chip technology, chip design, chip fabrication yields, and logistics support concepts?

Overview

A literature review of LCC modeling, cost estimating techniques, and the DoD VHSIC program is presented in Chapter II. Chapter III presents the methodologies for VHSIC insertion and LCC modeling. In addition, this chapter describes a process model for determining VHSIC fabrication yields. A LCC model is developed in Chapter IV by combining functional relationships of three separate models into the major phases of life cycle costing (development, production, and support). Chapter V provides derivation of the primary input data to the LCC model. Specific attention is given to those inputs relating to the main areas explored in this study. Data sources and assumptions are fully explained to establish data validity. The outputs of the LCC model after processing the data described in Chapter V are presented and analyzed in Chapter VI. Chapter VII gives general conclusions drawn from the findings in Chapter VI, and recommendations for further study are made. Two appendices are attached which describe all input data and output data in detail. A complete summary of all data input to and output from the LCC model is provided in Appendix A and B respectively.

Assumptions, Limitations, and Strengths

Numerous assumptions are made with regard to 1) development and production of VHSIC chips, 2) development and production of hardware, 3) development and support of software, and 4) deployment and support of VHSIC systems. These assumptions are identified throughout this study at locations where most appropriate and applicable to facilitate understanding and validity of this work.

The results of this study are limited in accuracy for the following reasons:

1. Some data parameters required by the LCC model are unavailable. Many companies consider data on fabrication yields of integrated circuits as proprietary. Moreover, to keep this study unclassified, data for the synthetic aperture radar processor presented in Chapter III are sketchy, and the derived quantities of logic gates and memory bits are approximate.

2. The LCC modeling methodology presented in Chapter III and the LCC model described in Chapter IV have not been tested or validated against real systems implemented with VHSIC technology. Thus, the model is more conceptual than real.

Because of these limitations, the reader is cautioned against placing too much reliance on the cost results given in Chapter VI. However, the model results presented are important for two reasons. First, with one exception (5), no other LCC model for VHSIC insertion exists. Second, the relative comparison of costs for the areas studied are indicative of where emphasis should be placed when using VHSIC to implement military avionics systems. For instance, with the average VHSIC fabrication yields less than .5% (34:18), the results of this study suggest that profound LCC savings can be obtained by increasing overall yields to just 1%. Another example is the use of CAD to assist in the design of VHSIC chips. Over the life cycle of the system, cost is relatively insensitive to the use of chip-level CAD. However, the level of maintenance (organization versus depot) has a large impact on LCC. Thus, chip designers and potential users of VHSIC technology should concentrate on improving fabrication yields and give close attention to support concepts.

II. Literature Review

A literature review of regulations, manuals, directives, and other publications was accomplished to answer the following research questions:

1. What is LCC modeling, and how does it apply to DoD and the Air Force?

2. What are the cost estimating techniques used for LCC modeling?

3. Are there models currently available that estimate LCC for integrated circuits, and how is access obtained to these models and their documentation?

4. What are the objectives of the VHSIC Program and VHSIC Phase 1 technology?

LCC Defined

LCC, as defined in Air Force Regulation (AFR) 800-11, is:

> .... the total cost of an item or system over its full life. It includes the cost of acquisition, ownership, (operation, maintenance, support, etc.) and, where applicable, disposal (9:1).

Acquisition cost includes the cost of research, development, test, and evaluation (RDT&E) and production/procurement of the end item. In addition, acquisition costs include the initial investments required to establish a product support capability (support equipment, initial spares, technical data, facilities, training). Ownership cost (operating and support costs) includes the cost of operation, maintenance, and follow-on logistics support of the end item and its support systems (23:3-4).

LCC Models

LCC models cover the entire cost spectrum from design, development and acquisition, operating and support and ultimate equipment disposal (24:2.1). The concept of life cycle costing is not new. According to Blanchard, industries, businesses, government agencies, institutions, and individuals have been dealing with development, production, and support cost for years. However, these costs were viewed in a fragmented manner with very little attention directed toward overall cost of a system (2:1).

Within the DoD, the evolution of LCC models began in the early 1960s because of an increasing concern over the consequences of competitive procurement without regard to LCC (20:1-6). In the early 1970s, a shift from the independent consideration of development, production, and support costs to considering total cost growth took place within DoD. Today, LCC modeling is one of the keys in DoD management (25:4).

Characteristics and Deficiencies of LCC Models. There are many LCC models available. Some LCC models are general purpose analytical tools while others meet the needs of a specific program or type of analysis. The AFSC/AFLC LCC Working Group has defined eight separate categories of models:

1. Accounting Model. A set of equations used to aggregate components of support costs, including costs of manpower and material to a total or subtotal of LCC.

2. Economic Analysis Model. A model that considers the time value of money, specific program schedules and investigates the question of investing money in the near future to reduce costs in the more distant future.

3. Cost Estimating Relationship Model. An equation relating LCC or some portion of LCC directly to parameters that describe the design, performance, or operating environment of a system.

4. Reliability Improvement Cost Model. An equation that reflects the cost for improving equipment reliability.

5. Level of Repair Analysis Model. A model that determines a minimum cost maintenance policy from among a set of policy options for a specific piece of equipment.

6. Maintenance Manpower Planning Model. A model that evaluates the cost impact of alternative maintenance manpower requirements or the effects of alternative equipment designs on maintenance manpower requirements.

7. Inventory Management Model. A model that determines a set of spare part stock levels that is optimal for a specific system.

8. Warranty Model. A model that assesses the relative costs of having the government do in-house maintenance versus having this maintenance performed by contractors under warranty (7:6-7).

For each of these eight categories of LCC models, the following are desired characteristics of these models:

1. Completeness. LCC models must include all elements of LCC appropriate to the decision issue under considerations.

2. Sensitivity. LCC models must be sensitive :he specific design or program parameters under study to resolve LCC deficiencies between alternatives.

3. Validity. LCC models are an abstraction of the real world and some judgement is required with respect to validity of cost estimates.

4. Availability of input data. LCC models should use data that are readily available at a low cost and have a high level of validity (32:8.16-8.17).

However, according to AFSC/AFLC LCC Working Group, LCC models commonly have these four deficiencies:

1. They are not sensitive to design and performance such as accuracy, speed, range and early trade-off decisions.

2. They are too complex. In many cases LCC models have a large number of parameters that obscure a small number of parameters that are more relevant to LCC. In addition, the definitions of these parameters are not clear.

3. Frequently, the requirements for input data cannot be accomplished, because these data are not available, are expensive to collect, or lack validity.

4. Some LCC models are not sensitive to wear-induced failures (7:8-12).

Generally, a LCC model must be oriented to a narrow range of application to be useful for analysis of a specific design issue. According to the AFSC/AFLC LCC Working Group, general purpose models tend to be inadequate for specific design applications because:

> .... they lack resolution with respect to specific decision issues, do not reflect characteristics of peculiar equipment types, require data in formats that are too extensive or are not compatible with formats of available data (7:4).

<u>Applicability to DoD</u>. Depending on the intended use, LCC is a budgeting technique, a procurement technique (design-to-cost) and a management technique (acquisition consideration and trade-off tool) (12:2-3). As a budgeting technique, the research and development and production estimates of new systems play an important role in the DoD Five Year Defense Plan (FYDP) and the President's budget. Invalid cost predictions can result in an unbalanced, unrealistic FYDP, and loss of credibility with Congress (25:4, 19:12-16).

A second use of LCC is in the support of DoDD 5000.28 Design-to-Cost (DTC) program. DoDD 5000.28 defines DTC as:

> A management concept wherein rigorous cost goals are established during development and the control of systems costs (acquisition, operating and support) is achieved by practical trade-offs between operational capability, performance, cost, and schedule. Cost, as a key design parameter, is addressed on a continuing basis and is an inherent part of the development and production process (11:2).

The purpose of this program is to ensure that the developed system will have the lowest possible LCC consistent with performance and schedule requirements. Specifically, the OSD began to realize that operating and support (O&S) costs were making up the majority of the total cost on a weapons system. Moreover, OSD realized that higher O&S costs were primarily the result of the greater weapon system complexity which tended to increase performance but decrease reliability. The result of this program was a major transition from emphasis on designing for unit production to an emphasis for total LCC (1:1-2).

Finally, LCC is used to support Air Staff and Secretary of Defense reviews of new weapon system programs (10:41). A memorandum in December 1971 from OSD advised all services that parametric cost estimates and analysis for each weapon system in the acquisition cycle were to be incorporated into Defense System Acquisition Review Council (DSARC) presentations. This memorandum was followed in January 1972 y a memorandum that established a Cost Analysis Improvement Group (CAIG) within the OSD. The OSD (CAIG) was directed to review cost estimates presented to the DSARC and develop uniform criteria to be used by all DoD units making cost estimates. DoDD 5000.4 formally established the OSD (CAIG) as the main advisor on cost to the DSARC in June 1974 (25:4-5). Specifically, DoDD 5000.4 directs the OSD (CAIG) to:

1. Establish criteria, standards, and procedures concerning the preparation of cost estimates to the DASRC and CAIG;
2. Develop useful methods for formulating cost uncertainty/cost risk information for DSARC review; and

3. Work with DoD components to determine relevant costs for DSARC consideration and to develop techniques for identifying and projecting these costs (19:A-9).

Cost Estimating Techniques

The three most common estimating techniques used for LCC modeling are:

1. Parametric estimation which uses mathematical processes such as regression analysis to develop cost estimating relationships;

2. Analogy estimation which predicts the cost of a new system by comparison of differences between an existing system and the new system; and

3. Engineering estimation which relies on detail analysis of the system being developed (24:3-1, 14:465, 23:6-10).

Parametric Estimation. Parametric cost techniques were pioneered by RAND corporation in the late fifties and early sixties. This technique provides fairly accurate estimates of system costs during initial phases of system development. This approach uses output explanatory variables (physical or performance parameters such as weight, throughput rate, density) to predict cost since these parameters can be estimated early in systems development. These estimates are typically at an aggregate level and use historical information on similar systems (25:6). Thus parametric cost estimates are made by developing cost estimating relationships (CER) from cost data, physical characteristics, and operating parameters of existing weapons systems (16:6).

CERs are mathematical equations that describe the cost of an item as a function of n independent physical or performance variables (X_j) and a set of p constant coefficients (a_j), and are denoted as follows:

$$C = f(X_1, X_2, \ldots X_n; a_1, a_2, \ldots a_p) \quad (25:9)$$

To be useful, CERs should have the following characteristics:

1. All relationships describe aspects of reality which are relevant to the problem;
2. The variables in the relationship are observable;
3. The results should be repeatable with same input values;
4. The number of parameters should be small to make statistical estimation possible; and
5. They should be easy to apply (25:10, 24:3.3).

Although CERs are used to predict costs of new or developing systems, they have limitations. They should not be applied to radically new systems because there will be little prior knowledge to base estimates upon. In addition, since CERs are developed from minimal data, periodic adjustments are required for changes in economic trends, design, and maintenance policy (24:3.3-3.4). Finally, since each CER is prepared for a specific purpose at a particular time in a system's acquisition cycle, the development of an all-purpose CER probably is not possible (23:7).

Analogy Estimation. In this technique an existing system is identified similar in design and/or operational environment to the new system. The cost of the new system is estimated by taking the cost of the old system and adjusting it to account for differences between the two systems. This method precludes many of the negative aspects of

CERs. However, this approach relies heavily on expert opinion to determine the similarities and differences between systems and to assess the magnitude of their differences. Because opinions are likely to vary among experts, documentation of the assumptions and rationale is extremely important (24:3.6-3.7, 23:6-7).

Engineering Estimation. The engineering or "grass roots" method relies on the availability of detailed information about the system under development. This method is considered to be the most complex of the cost estimating techniques (14:153-157, 25:6, 24:3.8). It requires the use of all the costs associated with the elements of the developing system. When combined, the cost of the final product is obtained (14:153-157). This method has the advantage of being able to be tailored to a specific system. If accomplished properly, the engineering method will yield the most accurate results. However, the level of detail required for this method makes it very difficult and expensive to use, and by the time intricate data is available, it is usually too late to influence crucial design and support decisions (24:3.8, 23:8). According to Fox, an additional drawback is that as cost estimates for elements of the weapon system pass through succeeding levels of management, the estimates run the risk of becoming inflated through failure to identify the subjective contributions of managers at each level (14:157).

According to Long, most LCC cost estimates are accomplished using a combination of the three estimating techniques (parametric, analogy, engineering) discussed. In the conceptual phase and the early portion of the demonstration/validation phase of a program the parametric technique is most often used. As the program progresses and more data becomes available, the analogy and engineering technique predominate (23:39-40).

Existing Models That Estimate LCC For Integrated Circuits

An extensive review of literature on LCC modeling and numerous personal interviews with experts in the discipline of LCC modeling and cost analysis revealed that few models are currently available which deal specifically with estimating LCC of integrated circuits (5, 7, 8, 13, 17, 20, 23, 31, 39). Moreover, because VHSIC technology is in the developmental phase, these models should be parametric. The following models represent efforts to derive parametric cost estimates for avionics and/or integrated circuits.

1. ALPOSII (Avionics Laboratory Operating and Support Cost Model).

   This model predicts the life cycle operations and support costs of the Air Force avionics equipments, which includes logistics support, spares, support equipment, and training costs. The model is based on CERs developed from historical costs of 128 Avionics LRUs. AFWAL has this model on the CDC 6600 System (17:40).

2. Microcircuit LCC model.

   This model is coded in FORTRAN IV for the Honeywell 6000 computers. The program contains nonstandard conventions for the Honeywell compiler. It consists of a main routine and several subroutines that parametrically estimate chip costs for all phases of LCC. Printouts of all phases as well as total LCC cost are provided (5:79-80).

3. PRICE M (Programmed Review of Information for Costing and Evaluation - Microcircuit).

   Like PRICE L, PRICE M is owned and controlled by RCA. This model estimates development and production costs for custom microcircuit chips. It can be used in conjunction with

PRICE H (Hardware Model) to estimate the cost of integrated circuitry of the finished product level. ASD/ACCC has access to PRICE M on UNINET (30).

4. PRICE H (Programmed Review of Information for Costing and Evaluation - Hardware Cost Estimating).

   The RCA PRICE H model uses parametric information (unit weight, volume, type of electronics) to compute unit acquisition costs. Although normally used for estimating costs of line-replaceable unit (LRU) level items, the Avionics Laboratory at Wright-Patterson AFB, Ohio (AWAL/AAAS-2) has successfully used PRICE H to analyze hardware acquisition costs. ASD/ACCC has access to PRICE H on UNINET (13:1).

5. PRICE L (Programmed Review of Information for Costing and Evaluation - Life Cycle Cost).

   PRICE L is a parametric model owned and controlled by RCA. This model estimates the life cycle costs of a wide variety of electro-mechanical or mechanical systems. It provides ways of tailoring analyses to fit a wide variety of maintenance concepts and supply systems which can be custom designed for specific programs and user organizations. Like PRICE M and PRICE H, ASD/ACCC has access to this model on UNINET (17:21).

<u>VHSIC Program Description</u>

As discussed earlier, LCC modeling includes all phases of a system's acquisition and development. Therefore, modeling VHSIC life cycle costs requires an understanding of VHSIC technology and the VHSIC Program. This portion of the literature review describes VHSIC technology and outlines DoD strategy for development and acquisition of it. Finally, the performance and maintainability impacts on defense system of VHSIC application are examined.

Definitions. The following definitions apply to terms used to describe VHSIC technology:

1. Integrated Circuit (IC) - an interconnected array of active and passive elements integrated with a single semiconductor substrate or deposited on the substrate by a continuous series of compatible processes.

2. Chip - a circuit integrated on a small piece of semiconductor material that is capable of performing from a small to a significant number of functions.

3. Gate - a group of active and passive elements capable of performing a single logic function.

4. Level of Integration - number of gates per chip or IC. ICs are categorized according to level of integration as follows (18:369-374):

Category	No. of Gates Per Chip
Large Scale Integration (LSI)	100 - 1,000
Very Large Scale Integration (VLSI)	1,000 or more

Program Organization and Objectives. The VHSIC Program was launched in June 1979 to be accomplished over a six year period, through four distinct phases and under the management control of the Office of Under Secretary of Defense for Research and Development and administered by all three services (Figure 1) (31:29). Phase 0, 1, and 2 will be carried out consecutively, while Phase 3 will occur parallel with Phases 0, 1, and 2 (Figure 2) (36:4-7).

Phase 0: Technology Definition. This phase (March 1980 to March 1981) was dedicated entirely to concept definition and managing the process of technological evolution (1:18, 14:4). Many believe that Phase 0 was one of the more astute moves in the VHSIC Program, because

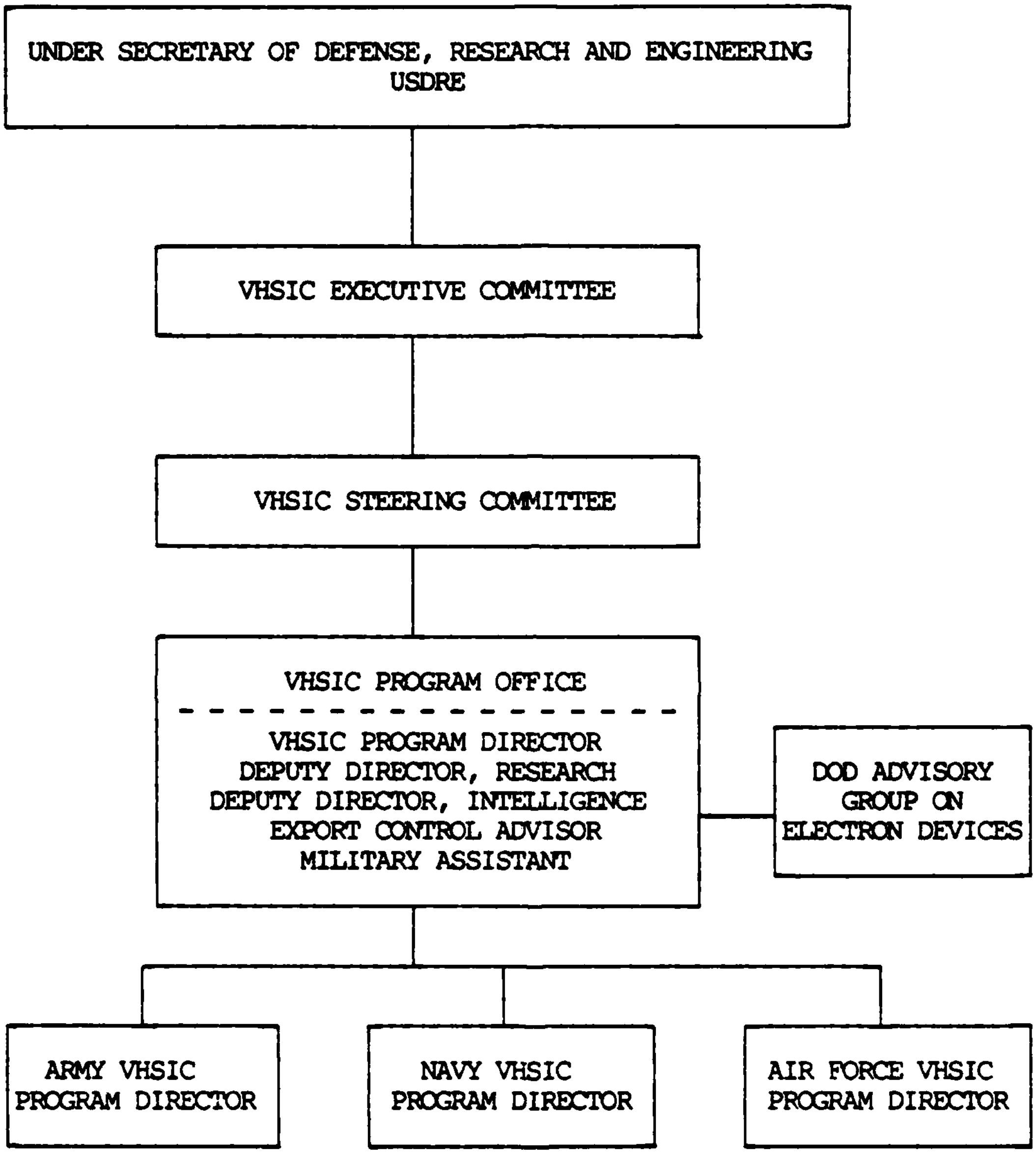
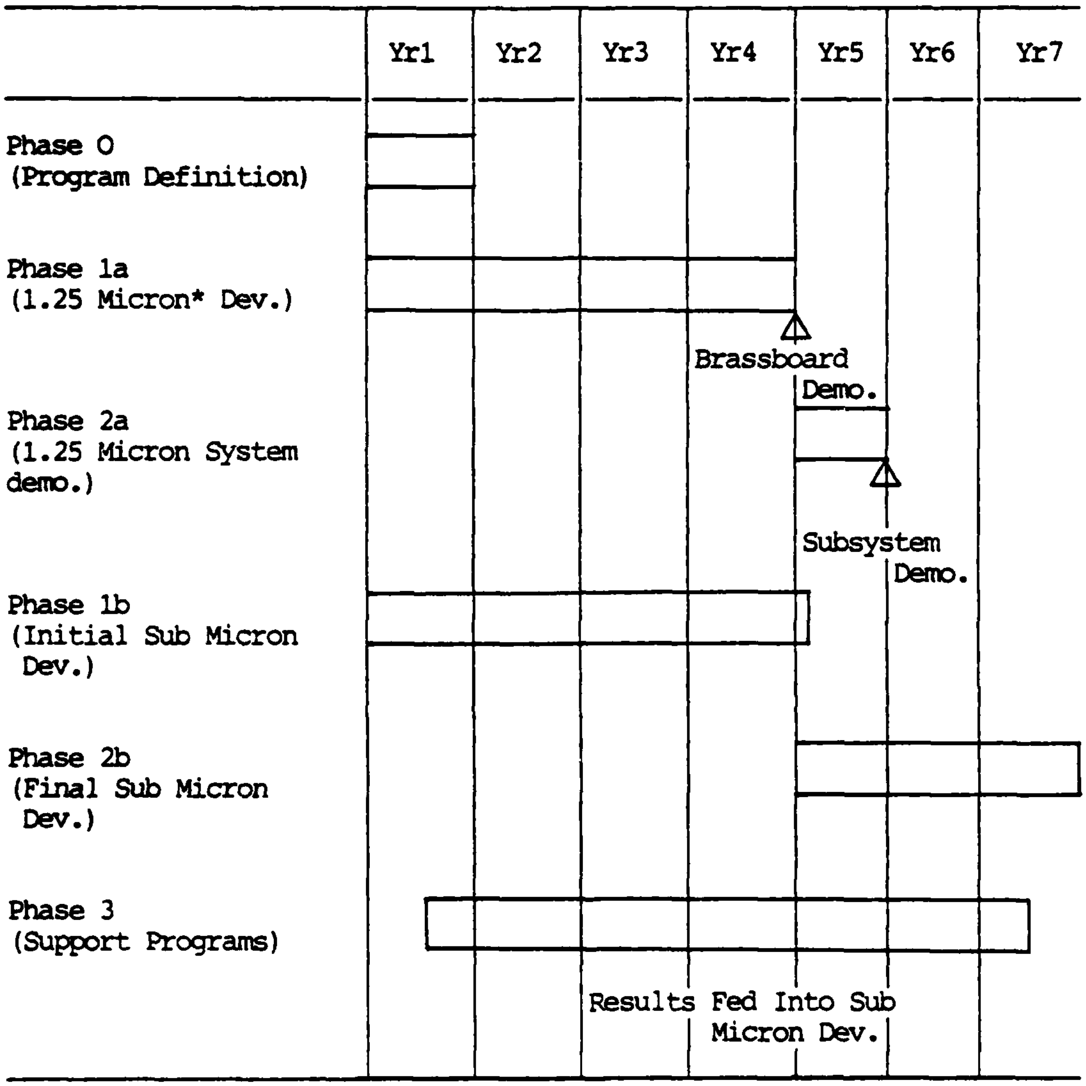


Figure 1. VHSIC Management Structure (31:29)



*one micron = one millionth of a meter or 40 millionths of an inch

Figure 2: VHSIC Program Schedule (36:7)

it planned the technological growth that was to follow (4:18, 21:77-79, 36:5). A key aspect addressed in Phase 0 contracts was the requirement for VHSIC coordinators to define and describe procedures for making VHSIC components available to all other DoD contractors and government laboratories. In addition, there is a special clause in all Phase 0 contracts which requires the primes to provide second sources for all hardware and software developed under this program. Finally, this phase provided plans for rapidly introducing VHSICs into DoD systems (36:6).

Phase 1: Technology Development. As shown in Figure 2, Phase 1 is divided into two parallel efforts. Phase 1a will develop complete electronic brassboard subsystems within three years of start. These brassboards will include VHSIC chips and modules with a minimum clock rate of 25 MHz and a functional-throughput-rate (FTR) of 5 X 10^{11} gate-H_z/cm^2 (clock rate times gate density). Density goals were set as a product of the number of gates per square centimeter of chip area and the operating speed of the gates which are more realistic measures of IC utility for military applications (21:48). Phase 1b consists of initial efforts to extend 1a technology to devices with minimum feature sizes (line width/spacing) of 1.25 microns compared to the 3 to 5 micron sizes being achieved prior to Phase 1 (21:51). In addition, these efforts include high resolution lithography and replication techniques, substrate improvements, metalization reliability, Computer-Aided-Design (CAD) techniques and systems consideration (36:6).

Phase 2: Technology Demonstration. Similarly, Phase 2 is divided into two parallel programs -- Phase 2a which will provide subsystem demonstrations of Phase 1a brassboards, and Phase 2b which continues the Phase 1b submicrometer development effort (36:6-7). The end goal of Phase 2 is to achieve FTR of 1 x 10^{13} gate-H_z/cm^2 (approximately 20-fold improvement over Phase 1) and feature sizes of 0.5 microns dimensions if possible, or at least 0.8 micron sizes. To illustrate these dimensions, if a map of the entire United States were printed using .5-micron-wide lines on 20 inch wide paper, it would be possible to show every individual street in the country (4:18, 21:51). This miniaturization will culminate in a systems-on-a-chip device capable of incorporating up to one million transistors (31:9).

Phase 3: Technology Support. Phase III, the VHSIC Support Program (Figure 2) runs parallel to the main program efforts. Unlike Phase 1 and Phase 2 contracts (large, vertically integrated efforts with each contractor covering all aspects of VHSIC development), Phase 3 contracts consist of many smaller short term contracts (two or three years in length) designed to encourage the participation of universities and small businesses in key technology areas that feed into Phase 1 and Phase 2 (36:7, 21:54). According to Larry W. Sumney, (former VHSIC Program Director and now Executive Director of the Semiconductor Research Corporation), these efforts will:

> .... focus on high resolution lithographic equipment and processing technology; advanced architecture and design concepts for reducing custom fabrication; increasing chip utilization and improving system reliability through fault tolerance and system testability through on-chip testing; advanced CAD techniques; improved silicon materials and fabrication processes; analytical

methods for determination of substrate and fabrication methods induced defects at the submicron level; methods for improving radiation, thermal and mechanical stress tolerance; establishment of design standards and interface requirements; new device, gate and circuit structures; techniques for documentation and methods for improved simplified utilization and testing (36:8).

VHSIC Application

New breeds of military equipment are emerging that are designed to collect, analyze and rapidly disseminate tactical information to identify enemy forces, select critical targets, and precisely deliver munitions. The selective, timely, and precise delivery of munitions and armaments produce a force multiplication factor intended to reduce any numerical disadvantage that US military forces might face in future conflict. This multiplication factor depends upon development of equipments that make intensive use of signal processing and data analysis. Moreover, they must be lightweight, compact, reliable, low power, and relatively inexpensive (36:7). These attributes uniquely characterize the military application for VHSIC.

Performance. The IC performance levels can be characterized by the functional throughput rate (FTR) defined as the product of the number of logic gates on the chip and their switching rate. A typical advanced commercial microprocessor contains 6,000 to 8,000 logic gates on a 7.5 mm square chip with a FTR of about 7×10^{10} gate-H_z/cm^2. By comparison (see Table 1), several types of military equipment require that throughput rates be increased by two orders of magnitude or more. This increase can be achieved by increasing circuit density, circuit speed, and total active area per chip (36:10, 33:46, 22:114).

TABLE I

Throughput Rates in Millions of Operations Per Second (36:10)

Equipment	Current Best	to	VHSIC
Programmable A/J Communications	10	to	500
Optical Surveillance Equipment	100	to	2,000
Radar Processor	50	to	1,000
Missile Sensors and Guidance	2	to	50
Acoustic Processors	100	to	1,000
Airborne Early Warning Systems	100	to	3,000

Current aircraft systems cannot afford to devote more weight, power, volume, or cooling to electronic systems. For example, the total processing load for avionics in next generation aircraft systems has been estimated at 3×10^9 operations per second. A throughput rate of this magnitude is not feasible using contemporary military IC technology (36:8-10).

The FTR targeted by the VHSIC Program translate into improvements for critical military equipments. The following represent a few examples:

1. Digital signal processing for target classification and requisition used in surveillance radar and air-to-surface missiles.

2. Acoustic signal processing used for target identification in submarines and aircraft.

3. Time and frequency dispersion for command, control and communication (21:48, 36:13-14).

Reliability and Maintainability. Due to the increasing complexity of military electronic systems, the failure rate for aircraft avionics has increased to the point that the unscheduled maintenance of electronics has become the major cause of operational downtime (6:90-91). One solution to the complexity problem for military electronics is the VHSIC Program. Rapid improvements can be expected as large assemblies of components are reduced to a single chip, as mission functions are integrated into programmable processors, and as military systems achieve a level of commonality in chip usage (21:77-79). Because of the high geometric resolution demanded by VHSIC, additional area will be available on VHSIC chips for implementing self-repair and built-in-test functions that will increase reliability and simplify maintenance (21:48-69). The ultimate goal is to create an interface with maintenance personnel that demands less skill to restore a failed system to operational status (36:17).

Air Force Management of VHSIC Application. To sustain the objectives previously discussed, DoD attention is being focused beyond acquisition of performance characteristics to that of achieving an affordable product (36:15). The impact of VHSIC technology goes beyond the cost of the product. The costs of VHSIC chips are small relative to the aggregate cost of product qualification, acceptance testing, packaging, documentation, special test equipment, logistics and operational support, and life cycle cost of the host system.

The Air Force VHSIC Program Office (AFWAL/AAD) at Wright Patterson AFB, Ohio is studying ways to introduce VHSIC technology into weapon system design. They are working to establish requirements for demonstration of VHSIC insertion in the launch and leave guided bomb, the MIL STD 1750 A Computer, the ALQ 131 Signal Processor, the modular avionics study, and the common signal processor (4:18). In addition, they will analyze the results, evaluate impact on weapon system performance and determine life cycle costs. The feasibility of improving software development tools will be studied to raise software productivity to a level commensurate with the design flexibility expected from VHSIC products. User requirements for interface to system level computer aided design will be determined and functional design specification produced. Finally, they will identify issues in supportability, testability, reliability, and maintainability that are influenced by VHSIC technology (3).

Summary of LCC Modeling and VHSIC Technology

This literature review has examined concepts and techniques for LCC modeling and has overviewed the DoD VHSIC Program and VHSIC technology.

LCC Modeling. The LCC literature examined DoD policy and requirements for LCC estimates. In addition, it investigated the characteristics, strengths, and deficiencies of estimating techniques used in LCC modeling. The AFSC/AFLC LCC Working Group Study was very useful in identifying and categorizing the basic types of LCC models and their characteristics and disadvantages. In addition, this study made clear that a wide spectrum of LCC models exist and that each model has unique characteristics for assessing specific types of LCC issues. Therefore, the limitations and assumptions of a model should be thoroughly understood before it is applied.

The literature authored by Long, May, McNichols, and Fox provided additional insight to LCC modeling by describing and analyzing cost estimating techniques and how they relate to various phases of program development. Specifically, Long, May, and McNichols indicate that parametric cost estimating techniques are best predictors of cost in the early phases of a program, because they are based on physical and performance parameters rather than detailed engineering data. However, as design progresses and detailed engineering data becomes available, Fox, May, and Long suggest that analogy and engineering estimates are better cost predictors. Hence, LCC modeling is an iterative process that depends on estimating techniques that become more exact as data becomes more detailed.

VHSIC Program and Technology. The VHSIC literature examined the structure and objectives of the VHSIC Program. In addition, it investigated the characteristics and features of VHSIC technology. The literature authored by Sumney, Reed, and Brannon described the organization and objectives of the VHSIC Program. In addition, it highlighted many of the planned and projected application of VHSIC technology.

The literature authored by Klass, Sumney, and Schlag described the performance objectives and characteristic features of VHSIC technology.

Specifically, this literature detailed current approaches for the design and manufacturing of VHSIC chips, and it compared performance estimates for VHSIC technology to existing state-of-the-art for large scale integrated circuits.

III. Methodology

This chapter describes the methods that will be used to answer the following research questions:

1. How can an existing model or combination of existing models be implemented to estimate and analyze LCC for insertion of VHSIC Phase 1 technology?

2. What type of insertion model is needed to implement and characterize VHSIC Phase 1 technology?

3. What are the data that must be collected and in what format must the data be collected?

4. Where can these data be collected and what are the limitations for collecting these data?

5. How sensitive is the insertion model's LCC to changes in VHSIC chip technology, chip design, chip fabrication yields, and logistics support concepts?

This research adheres to the following steps to address the areas of model selection, data collection, data formatting, and LCC sensitivity analysis:

1. Select LCC model or models and determine how they will be used for this study.

2. Select an insertion model that can be designed using gate array and custom designed VHSIC Phase 1 chips.

3. Collect VHSIC Phase 1 density data for each technology and fabrication yields for each technology.

4. Format VHSIC chip data to implement the insertion model for each technology and design type.

5. Format hardware parametric data to implement the insertion model.

6. Perform LCC sensitivity analysis for areas of interest.

Research questions one and two will be answered from the literature review of Chapter II. Question three will be addressed by examining the input data requirements of the selected LCC model or models. Question four will be answered from the literature review of Chapter II and interviews with experts in the area of microcircuit design and engineering. These experts are available through the Air Force VHSIC Program Office and the AFIT School of Electrical Engineering. Finally, question five will be addressed by reviewing and analyzing output data of the LCC model.

Modeling Methodology

Three models will be used for this research study. They are the following RCA PRICE (Programmed Review of Information for Costing and Evaluation) models:

1. PRICE M Model. This model estimates the cost for development and production of both custom and gate array designed integrated circuits.

2. PRICE H Model. This model estimates the cost for electro-mechanical hardware, development, production, and integration and test.

3. PRICE L Model. This model estimates the cost for supporting hardware during its operational life.

These models were selected because the PRICE M model is the only available model reviewed that is robust enough to model VHSIC technology. Moreover, PRICE M, PRICE H, and PRICE L can be used to develop a complete LCC of VHSIC insertion from chip development through logistics support. Table II shows how these models will be used in this study.

TABLE II

Use of PRICE Models

Model	How Used
PRICE M (Micro-circuit)	To estimate development and production costs of the VHSIC Phase 1 chip technologies. To perform sensitivity analysis on design and production variables.
PRICE H (Hardware)	To estimate integration and test (I&T) costs for assembling chips onto Printed Circuit Boards (PCB). To estimate I&T costs for assembling complete brassboards.
PRICE L (LCC)	To provide LCC projections of the insertion model using different technologies, chip designs, and support costs.

PRICE M MODEL. PRICE M is a parametric model designed to provide estimates for development and production costs of microcircuit chips.

Input parameters are determined by physically describing the VHSIC chip. A wide range of chips can be processed through a number of input parameters including chip dimension, number of pins, number of gates or transistors, type of packaging, CAD sophistication, and amount of new design. Other significant parameters include fabrication yields and development and production schedules. PRICE M offers a number of features such as interactive data changes, technology improvement rate tables, and automatic schedule calculation that provide versatility for examining the impact of cost by varying input parameters (30).

An important feature of PRICE M is the ability to operate in conjunction with the PRICE H to estimate the costs of integrated circuitry at the finished product level.

PRICE H. PRICE H is a parametric model that is used extensively in DoD to estimate avionics and space system costs. It has been particularly useful in developing relative costs of competitive systems (13:1).

PRICE H has been designed to estimate costs with a minimal amount of hardware information. This feature makes it an excellent tool for cost estimation of programs in the conceptual stages of development.

Inputs to PRICE H cover a wide range of systems. Since all products have weight and size, these parameters are used as the principal descriptors for electro-mechanical items. Electronic components are characterized by their componentry (mode 1), or they can be treated as purchased items using mode 3. In this study, PRICE M is used to model the cost of VHSIC chip development and production. The total cost of development and production are then introduced to PRICE H via mode 3. Chassis and circuit boards are treated as government furnished equipment (GFE). They are presented to PRICE H as mode 4, GFE items. Software development costs (estimated using an algorithm developed by Carter) are represented in PRICE H as a throughput item, mode 8. Integration and test of the VHSIC chips onto circuit boards, and integration and test of circuit boards, software, and chassis into a line replaceable unit (LRU) are accomplished using mode 5, integration and test mode, of PRICE H.

Finally, the average unit cost for a LRU is input to mode 7 to calibrate complexity functions for mode 1. Mode 1 is then used to build a hardware file for PRICE L (28).

PRICE L Model. The PRICE Life Cycle Cost model (PRICE L) provides a methodology for computing support costs for a variety of systems. Like PRICE M, it can operate in conjunction with the PRICE H model. The major advantage of the PRICE H and PRICE L methodology is the ability to assess the LCC effects of design changes, while the hardware is still in the concept development stages (24:1). PRICE L inputs are limited to factors for the equipment's employment, deployment, maintenance policy and levels of support capability, equipment and maintenance locations, and total number of years to be considered. All other inputs are developed by the PRICE H model (mode 1). PRICE L is exercised in conjunction with the PRICE H model through a real-time interactive terminal which facilitates sensitivity analysis.

During the use of the PRICE H mode 1, the user can request the system to generate a LCC data file consisting of all the LCC input variables. Alternatively, a PRICE L data file can be created directly to input the governing parameters. In this study both procedures are used. All input values except MTBF, LRU production cost, cost of engineering, and nonrecurring production costs are generated by mode 1. Finally, the PRICE-generated data can be modified before or during the life cycle cost exercise.

In this study, primary values developed by mode 1 for input to PRICE L hardware file include:

1. Cost of LRU and module test equipment.
2. LRU and module checkout time.
3. MTTR for all repairable assemblies.
4. Floor space for test equipment and storage volume for spares.

In addition, PRICE L incorporates constant "Global" values that can be changed to represent various maintenance and supply organizations. Three theaters of deployment and multi-year specification of equipment deployment and employment capability permit realistic modeling of overseas organizations sending work back to CONUS depots and planned levels of operation for each year.

Finally, the "Maintenance Concept" file has 28 standard maintenance concepts stored within the model, of which 19 can be selected for examination during any run. Further, the model will determine the most cost-effective support configuration, accompanied by an assessment of the relative cost-effectiveness of the other candidate configurations. Therefore, PRICE L can be used to determine the most cost-effective support configurations (29).

VHSIC Insertion Model

The insertion model chosen for this study is an airborne synthetic aperture radar (SAR) digital processor. A very top level characterization of a SAR digital processor is presented here. The reader is referred to Carter to gain further insight into SAR systems (5:30-38). The SAR processor described here is used to demonstrate the modeling methodology that will be described later in this chapter.

Table III shows the assumed requirements for a SAR processor that will mount in a typical military tactical aircraft.

TABLE III

Requirements for an Example SAR Processor (5:31)

Item	Requirement
Resolution	5 feet range, 7 feet azimuth
Collection mode	Stripmap
Processing mode	5 nm range by 7 nm azimuth in slant plane
Range of radar	50 nm
Altitude of radar	30,000 feet
Speed of processor	Real-time
MTBF of processor	As calculated from the VHSIC chips and other components in the SAR processor

The processor receives digital data at high speed from the radar transmitter/receiver unit, converts that data to an image, and displays the image on a CRT. Only the SAR processor is characterized and costed in this study.

Further, no attempt is made to present a complete, detailed working design. The design is carried out to a level sufficient to get an idea of the number of chips, PCBs, and chassy dimensions needed to implement a SAR processer.

Figure 3 diagrams the major functional steps in a SAR processor using the polar format method described by Carter (5:31).

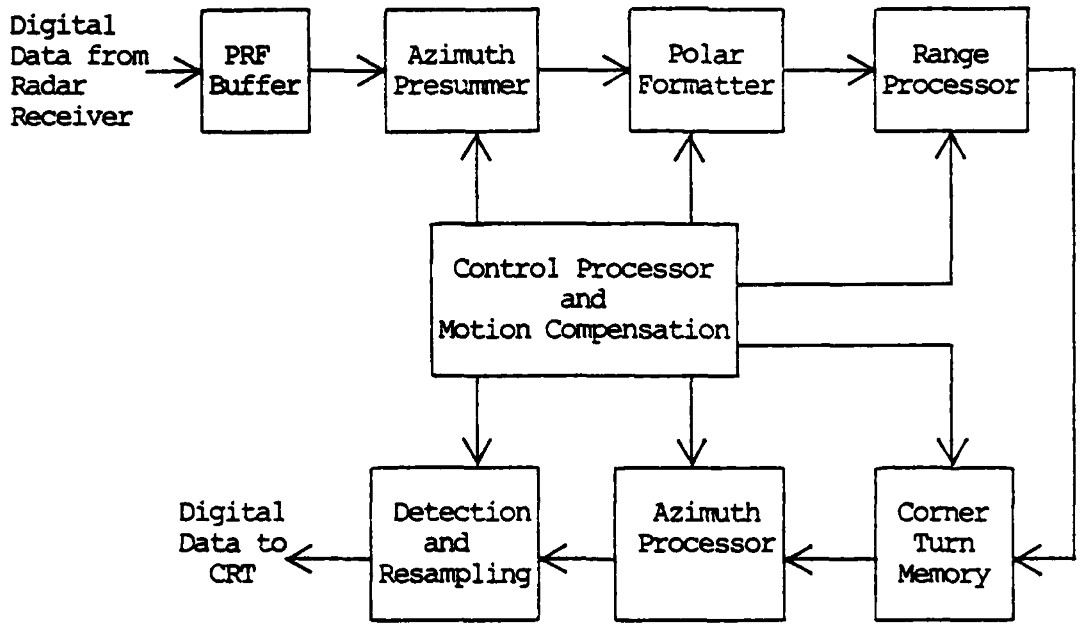


Figure 3. SAR Image Processing Functional Design (5:31)

PRF Buffer

The PRF buffer must slow the incoming radar data arriving at the input to the processor at a rate of 150 megasamples per second (Msps) to at least 1.79 Msps. The size of the PRF buffer is a function of the number of samples per pulse. Carter estimates the samples per pulse to be 9122.41 (5:35). The length of the PRF buffer is approximately twice the length of one pulse of data to permit simultaneous reading and writing of memory. The PRF buffer is about 0.219 Mbits in size (5:32-35).

Azimuth Presummer

The azimuth presummer is basically a low-pass digital filter. Since radar processing is required to be at a real-time rate, the azimuth presummer processing rate is the same as the PRF output buffer rate (1.79 Msps) times the operations per sample (5:35). Therefore, the azimuth presummer processing rate is about 17.9 million operations per second (Msps). The output of the azimuth presummer is the same as the input rate in the worst case. Approximately 10,000 gates are needed to implement this function (5:35).

Polar Formatter

The polar formatter is implemented with a two-dimensional (2-D) resampler. This function performs continuous data sampling and operates at the same speed as the azimuth presummer. In addition, it contains a memory to implement the 2-D resampler from two 1-D resamplers. Carter assumes this function operates over a 5-nm by 7-nm area at 5-ft range by 7-ft azimuth resolution oversampled by 1.5 inches in each direction which corresponds to 83 million samples (5:36). However, only a fraction (maximum 10%) of this data needs to be stored at any given time. Hence, the polar formatter is roughly 100 Mbits in memory size and requires approximately 16,000 logic gates (5:36).

Range Processor

The range processor is a 1-D Fast Fourier Transform (FFT) which compresses each range line. Approximately 10,000 logic gates and very little memory are required (5:36).

Azimuth Buffer Memory

A corner-turn memory is required to hold the radar data for the azimuth processor. This memory is capable of holding 5-nm by 7-nm patch that requires approximately 83 million (20 bit) words or 1660 Mbits of memory (5:36).

Azimuth Processor

Like the range processor, the azimuth processor is a 1-D FFT which compresses each azimuth line. Approximately 10,000 logic gates and no memory are required (5:36).

Image Detector

The radar data is now fully compressed but each sample is in complex form. The image detection process resamples the output data before it is sent to the CRT. Very little memory is involved, and the complexity of the circuitry is low (close to 5,000 gates) (5:37).

Control and Motion Compensation Processor

Control of the radar processor and the calculation of motion compensation parameters are performed by a high speed general purpose computer. Carter estimates 12 Mbits of memory and 100,000 gates are required to implement this general purpose computer (5:37).

Table IV summarizes the operation rate and memory size of the major subsystems in the SAR processor. Entries under "Technology" indicate VHSIC Phase 1 technologies that can be used to implement a particular function.

TABLE IV

Speed and Gate Complexity of SAR (5:38, 37:35-38)

Function	Max OP Rate	Memory Size	Number of Gates	Technology
Signal Processor				
PRF Buffer	150 Msps	.219 Mbits	Negligible	BIPOLAR*
Azimuth Presummer	17.9	Negligible	10,000	BIPOLAR
Polar Formatter	17.9	100 Mbits	16,000	BIPOLAR*
Range Processor	17.9		10,000	BIPOLAR*
Azimuth Buffer/ Memory	17.9	1660 Mbits	Negligible	CMOS/Bulk, NMOS
Azimuth Processor	17.9	Negligible	10,000	BIPOLAR, CMOS/SOS
Image Detection	17.9	Negligible	5,000	BIPOLAR, CMOS/SCS
Control Processor				
Control & Motion Compensation	2.0	12 Mbits	100,000	BIPOLAR*, CMOS/SOS, CMOS/BULK

*BIPOLAR Triple diffusion (3D)/Schottky transition logic (STL) or BIPOLAR Integrated Schottky logic (ISL)/Current mode logic (CML)

Hardware

The following assumptions are taken from Walker for the SAR Processor PCBs and chassis:

1. All PCBs are Air Transport Racking (ATR) standard.

2. PCBs are constructed of epoxy glass for military environments.

3. Chip packages are surfaced mounted with leads on 20 mil centers.

4. Maximum of 200 watts per board.

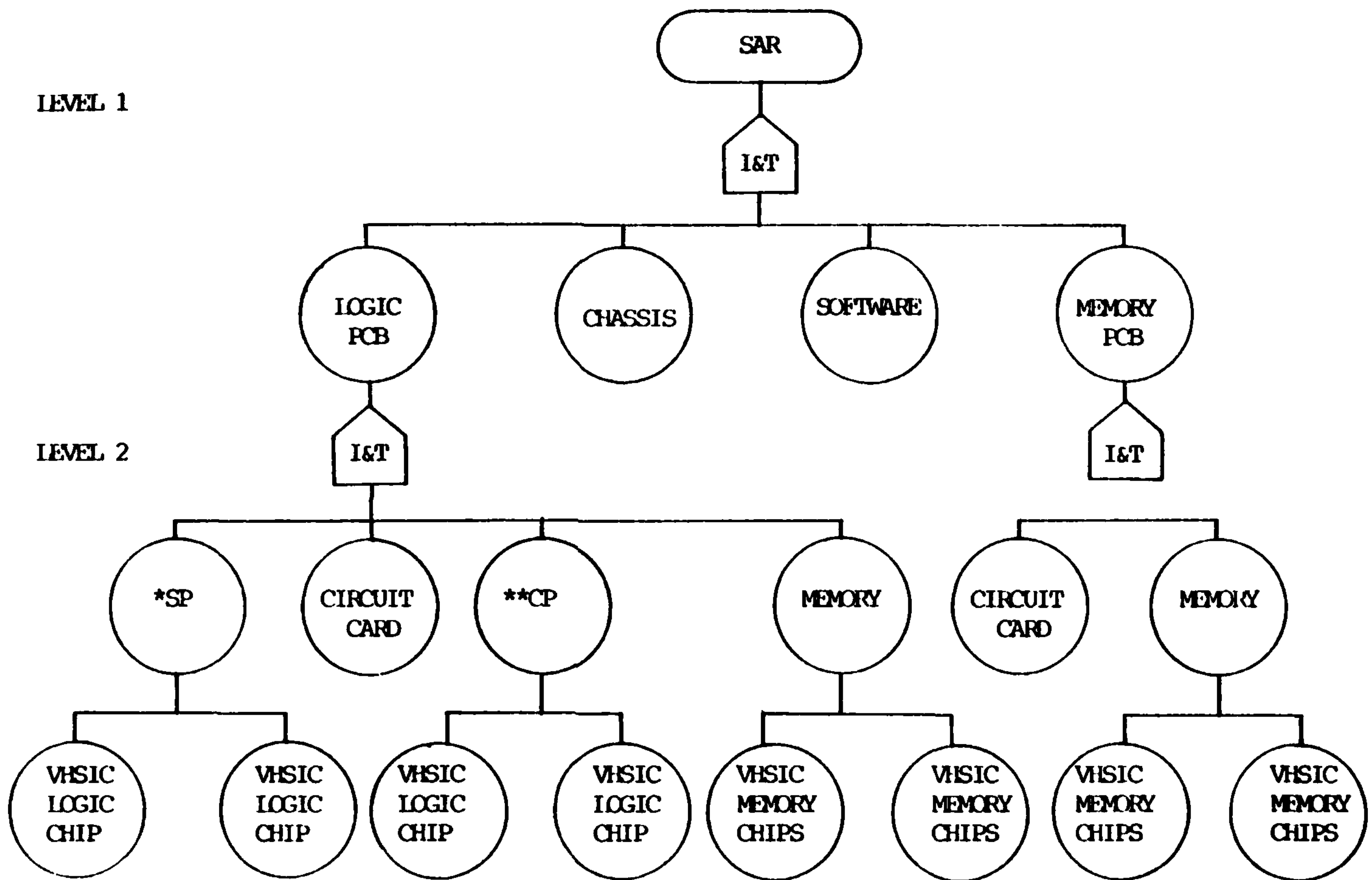
5. Single chip packages mounted on both sides of the PCBs.

6. Chassis are constructed of aluminum for military environments (39).

SAR Equipment Breakdown Structure and LCC Modeling Methodology

Figure 4 diametrically represents the equipment breakdown structure (EBS) for VHSIC chips, hardware, and software necessary to implement the SAR processor. Also, it depicts the integration and test (I&T) requirements at each level of assembly. Figure 5 diagrams the modeling methodology that will be used to estimate LCC of the EBS presented in Figure 4.

As shown in Figure 5, outputs from PRICE M (total development costs and total production costs) for each VHSIC chip technology, design, and function are input to PRICE H as mode 3, purchase items. PRICE H will contain two subsystem I&T files and one system I&T file. Outputs (weight of structure, weight of electronics, average unit production cost) of mode 5 I&T of the SAR are inputs for mode 7.



*SP - Signal Processor
**CP - Control Processor

Figure 4. Equipment Breakdown Structure (EBS) of SAR Processor.

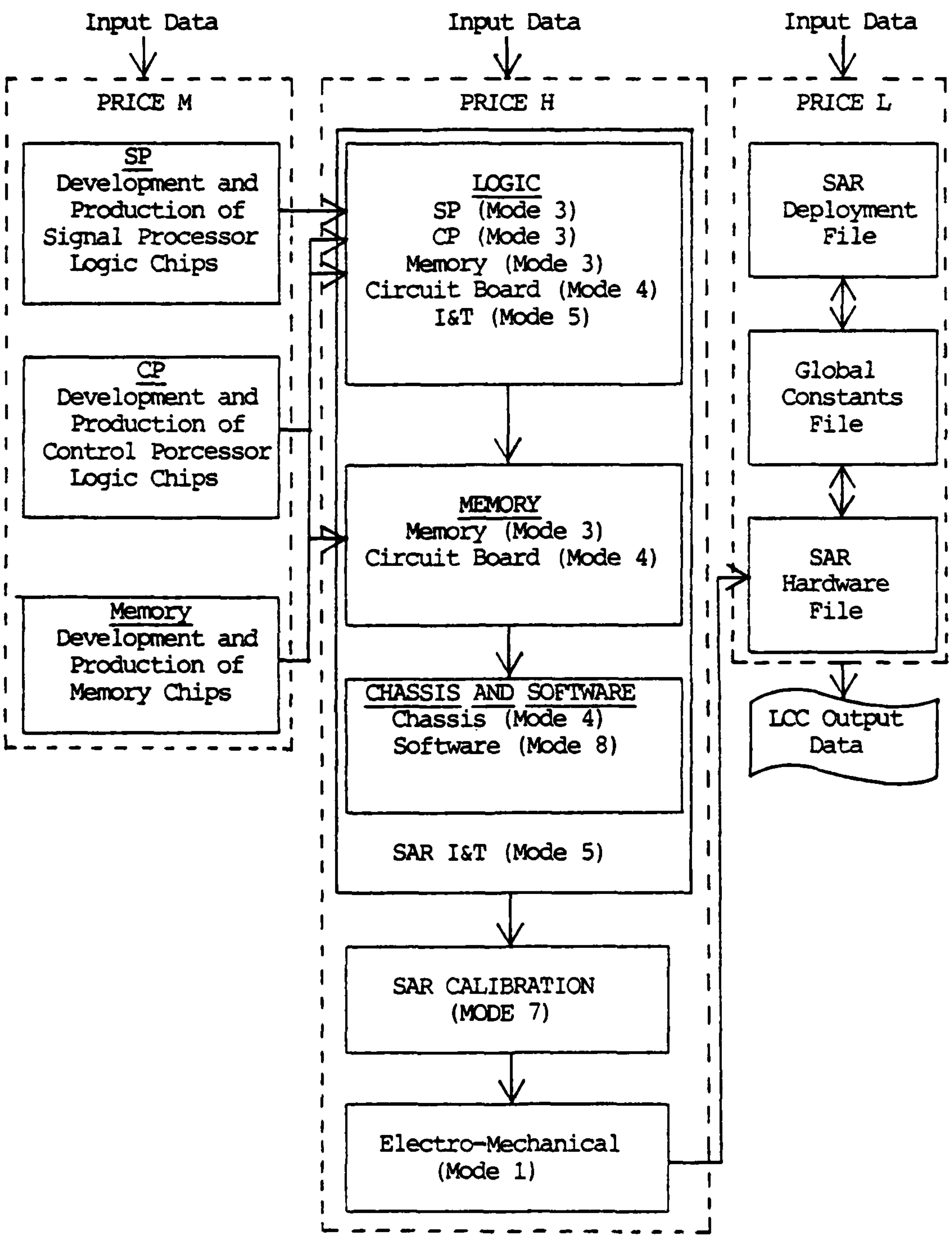


Figure 5. LCC Modeling Methodology for SAR EBS

The ECRIP mode involves running PRICE H backwards to determine complexity factors (indices that describe complexity for parameters such as design, engineering, and manufacturing) for electronics and mechanical structure when unit production costs are known. All inputs except complexity factors are input to mode 7; the output is complexity factors calculated by the model which are then used to characterize the SAR as a mode 1 electro-mechanical item. Finally, mode 1 is used to develop a LCC hardware file of the level 1 SAR processor which is one of two input files for PRICE L (28:7.1).

The second PRICE L input file is the deployment file for the SAR processor which is developed according to the following assumptions made by the author for SAR deployment:

1. SAR processors are installed into one thousand tactical aircraft of which 690 are at five CONUS bases, 170 are at three European bases, and 140 are at two Asian bases.

2. All SAR processors average 46 hours per month operating time.

3. One maintenance depot facility located in CONUS.

4. All SAR processors have fifteen years operational life.

5. Supply facilities are located at each organization.

6. Two level maintenance concept (organization and depot) is used.

7. Equipment locations and average operating life of the SAR processor remain constant throughout the program.

The "Global" file contains program constants that describe labor rates, shipping rates, cost to maintain supply items, travel time for items in the supply pipeline, and repair percentage at each maintenance level.

Finally, PRICE L provides a summary output of each of the three LCC phases (development, production, and logistics support). The development and production costs come primarily from PRICE M and PRICE H and the support costs are produced by PRICE L.

Data Collection

An extensive review of electronics literature and numerous interviews with experts in the area of integrated circuits design and engineering indicates that density data for each of the VHSIC Phase 1 technologies are available and that it can be formatted as parametric input to PRICE M (3, 4, 5, 8, 21, 22, 26, 33, 34, 35, 36, 37, 39). Likewise, data for hardware configuration is also available and can easily be formatted for parametric input to PRICE H (36).

However, due to its proprietary sensitivity, data for fabrication yields are not available. Therefore, estimates of fabrication yields are obtained from an adaption of a fabrication process model presented by Carter. This model contains equations and algorithms that estimate fabrication yields for chips based on type of substrate used, wafer size, and the size of the chip die (5: 26-28, 43-51).

Fabrication Yields Model

The process model for fabricating packaged integrated circuits is depicted in Figure 6. VHSIC chips are expected to be fabricated in this manner. The "Die Prep" function includes wafer scribe, probe test, and visual inspection. The circuit probe yield (CPYLD) is the percentage of VHSICs which pass functional testing during this process (34: 2.18).

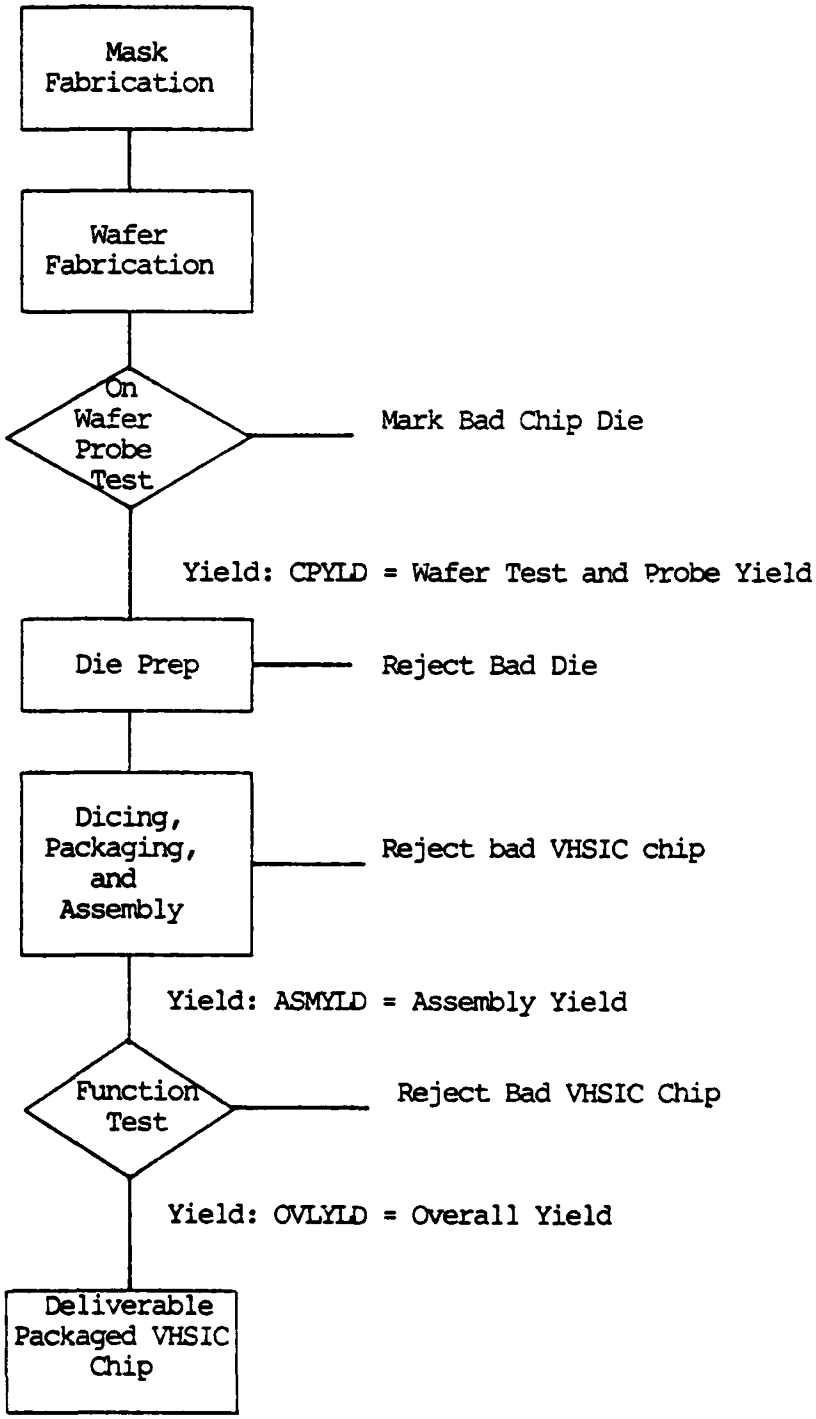


Figure 6. Process Model for Fabrication of Package VHSIC Chips. (30: 7.10, 5:25-28)

The assembly function includes breaking, packaging, and lead bonding. Assembly yield (ASMYLD) is the percentage of VHSIC chips which pass wafer dicing, packaging, bonding, and functional tests. Overall yield (OVLYLD) is the percentage of chips which pass production acceptance tests and is the product of CPYLD and ASMYLD (30:2.18). For purposes of this study, fabrication yields for development and production are assumed to be the same.

CPYLD is obtained from two equations that relate substrate type and wafer size to an estimated wafer test and probe yield. For silicon on saffire (SOS) wafers, the CPYLD equation is:

$$CPYLD_{SOS} = 4.1 \times 10^{-4} (r^2/c^2) \qquad (1)$$

where

r = radius of wafer in inches

c = edge dimension of chip die in inches (5:49)

and for bulk silicon wafers, the CPYLD equation is:

$$CPYLD_{bs} = 11.2 \times 10^{-4} (r^2/c^2) \qquad (2)$$

where

r and c have the same meaning as in equation 1 (5:49)

ASMYLD is defined by the following equation:

$$\text{ASMYLD} = \{.8/(1 + 3.0 \times 10^{-4}c^2)\}(.735) \qquad (3)$$

where

c = chip die area in mils (5: 50-51).

The reader is advised to refer to Carter for derivations of equations 1, 2, and 3 (5:49-51).

Sensitivity Analysis

Of the many characteristics of VHSIC that could be studied with respect to the SAR processor insertion model described earlier in this chapter, only five are selected for sensitivity analysis. They are the effects on LCC of chip technology and design, fabrication yields, substrate type, computer-aided-design (CAD), and level of maintenance. Each of these five areas will be analyzed with respect to four basic cases. These cases are depicted in Table V.

The memory portion of the SAR processor is implemented only in custom chips, because VHSIC Phase 1 does not have a gate array designed memory chip.

The areas selected for sensitivity analysis (except level of maintenance) are areas identified by the Second Tri-Service Workshop on Manufacturing Technology Program Planning for VHSIC technology as areas requiring manufacturing technology emphasis (34:2-6).

TABLE V

Basic Cases for LCC Sensitivity Analysis of Sar Processor

	Chip Design		
Case	Signal Processor	Control Processor	Memory
1	Custom	Custom	Custom
2	Gate Array	Gate Array	Custom
3	Custom	Gate Array	Custom
4	Gate Array	Custom	Custom

Finally, LCC sensitivity analysis will only be performed on the most expensive case and least expensive case; assuming LCC for the remaining two cases will fall somewhere between for all five areas studied.

Methodology Summary

The LCC model for VHSIC insertion will be accomplished using three cost models (PRICE M, PRICE H, AND PRICE L). These models will be used to estimate costs for each of the LCC phases of an example avionics system (SAR Processor). Finally, sensitivity analysis of five areas will be accomplished for the most and least expensive of the four basic cases to determine their effects on LCC.

IV. A VHSIC System Life Cycle Cost Model

This chapter presents mathematical expressions for a LCC model which is oriented towards VHSIC Phase 1 technology. The development and production portions of this model are adapted from functional relationships presented in the PRICE M and PRICE H models for integrated circuit development and production and system hardware development and production. Software development cost equations are adapted from a cost model presented by Carter (5:6-28). Finally, expressions for the logistic support phase are taken from the PRICE L model.

The complete code for algorithms and mathematical expressions used in the PRICE models are proprietary. Hence, they are not available for review. However, RCA PRICE does provide abbreviated procedures and equations for review by the user. The equations for development, production, and logistics support presented here are taken from these abbreviated procedures and equations to demonstrate how variables are used in this study.

The LCC model introduced in this chapter is based on the following scenario. Consider an aircraft digital avionics system which undergoes three phases (development, production, and deployment and support) in its life cycle.

During development three activities occur. First, the system is designed. Second, as a part of systems design, VHSIC chips are designed, fabricated, tested, and used to implement the third activity which is to assemble and checkout a prototype implementation of the system.

In the production phase, the system design is finalized, a preproduction prototype is built and tested, and the production of all deployed systems is accomplished. In this study, all systems fabricated during the production phase have the same fabrication cost.

Finally, in the support phase, all consumables for the life of the program (assumed to be 15 years) are purchased at the beginning of the deployment and support phase. The logistics support scenario centers around printed circuit boards as the basic repairable module. A two-level logistics base is assumed (organization and depot) with supply and maintenance locations at each base. One thousand systems are deployed to three theaters (CONUS, Europe, and Asia). In essence, the PRICE L model replicates standard logistics support concepts used in the Air Force today. Fortunately, the model is robust enough to be adaptable via input data to accommodate maintenance concepts envisioned for VHSIC Phase 1 technologies.

Development Costs

Three cost equations comprise the development costs. They are:

1. VHSIC chip development and prototype fabrication costs from the PRICE M model (30);
2. System prototype design, fabrication, integration, and test costs from the PRICE H model (28); and
3. Software development costs from the Carter model (5).

mathematically

$$\text{development costs} = \sum_{i=1}^{3} DC_i \qquad (4)$$

where

DC_1 = Total cost of VHSIC chip design and prototype fabrication.

DC_2 = Total costs for system hardware design, prototype fabrication, and integration and test. In addition, these costs include the integration and test cost of prototype VHSIC chips.

DC_3 = Total cost of software design, code, and test.

<u>Development Integrated Circuit Cost (DC_1)</u>.

$$DC_1 = \sum_{i=1}^{PROTOS1} CSPEC_i + CDES1_i + CSYS1_i + CPMGTi_1 + CDAT1_i + CPROTO1_i \quad (5)$$

where

PROTOS1 = Number of development prototypes for each VHSIC chip of type i.

$CSPEC_i$ = Cost of functional and detailed chip specification of chip type i. The specification cost for a VHSIC chip is a function of:

1. The number of gates on the chip (GATES), or the number of transistors (XSTRS) on the chip;

2. The percent of each chip which is repeated design (DESRPT); and

3. System specification level (SPLTFM) which describes the specification level imposed on the design. In this study SPLTFM=1.8, the PRICE M default value for military specifications.

4. Engineering complexity (ECMPLX) factor which describes the scope of the development effort and available resources;

5. Development calibration index (DINDEX) which relates past performance to new products; and

6. Escalation control (ESC) variable which defines cost escalation factors. In this study, ESC=0 which specifies constant year dollars in the PRICE M model.

7. Development cost multiplier (DMULT) which is used to customize specification, system, project management, prototype, and data costs to a particular user environment. For purposes of this study, DMULT=1, the PRICE M default value.

8. Level of chip specification engineering (SPEC) which is used to customize chip specification cost. This study uses the PRICE M default value of 1 (30:7.2).

$CDES1_i$ = Cost of chip design commencing with the specification and ending with a pattern generation tape for VHSIC chip type i. The design cost for each chip is a function of:

1. Gates or XSTRS;

2. Percent of new library circuit cells (NEWCEL) to be designed;

3. DESRPT; and

4. Design specification level (DPLTFM) of the designing organization. This study uses DPLTFM=1.8, the PRICE M default value for military organizations.

5. The degree of computer aided design (CADFAC) used in the chip development;

6. Number of design/prototype/test iterations (ITERAT) needed to meet chip specification;

7. ECMPLX;

8. DINDEX;

9. ESC; and

10. Level of chip design engineering (DESIGN) used to customize chip design cost. For this study, DESIGN=1, the PRICE M default value (30:7.5).

$CSYS1_i$ = Cost of system engineering for chip type i.

$CSYS1_i$ is further defined to be:

$$CSYS_i = (CSPEC_i + CDES1_i)SE \qquad (6)$$

where

SE = Systems engineering factor which is a function of:

1. ECMPLX; and

2. DINDEX.

$CPMGT1_i$ = Program management and control cost for chip type i.

$CPMGT1_i$ is further defined as follows:

$$CPMGT1_i = (CSPEC_i + CDES1_i + CSYS1_i)PM \quad (7)$$

where

PM = Project management factor which is a function of:

1. ECMPLX; and

2. DINDEX (30:7-8).

$CDAT1_i$ = Cost for documentation, deliverable drawings and reports for chip type i.

$CDAT1_i$ is further defined to be:

$$CDAT1_i = (CDES1_i + CSPEC_i + CSYS1_i = CPMGT1_i)DF \quad (8)$$

where

DF = Data factor which is a function of:

1. ECMPLX; and

2. DINDEX (30:7-9).

$CPROTO1_i$ = The cost of prototype fabrication for chip type i. The prototype cost is a function of:

1. PROTOS1;

2. Length dimension of the chip die in mils (LENGTH);

3. Width dimension of the chip die in mils (WIDTH);

4. Number of pins on the packaged chip (PINS); and

5. ITERAT (30:7.10).

<u>Development System Design Cost (DC_2).</u>

$$DC\ 2 = CDRAFT + CDES2 + CSYS2 + CPMGT2 + CDAT2 + CPROTO2 + CTTEQ1 \quad (9)$$

where

CDRAFT = Cost of manufacturing drawings, data lists, specifications, and incorporation of engineering changes in drawings. Development drafting is a function of:

1. Electronics manufacturing complexity (MCPLXE). This is an empirical factor which represents a products producibility. MCPLXE is a function of componentry, packaging, density, manufacturability, testing and power dissipation.

2. Structural/mechanical manufacturing complexity (MCPLXS). This empirical factor represents structural producibility for reliability requirements associated with operating environments.

3. Year of technology (YRTECH). This variable freezes technology to a specified year. In this study, YRTECH=1983.

4. Unique new electronic design (NEWEL). This variable indicates the level of engineering design effort for integration of electronics into a system or subsystem.

5. Unique new mechanical/structural design (NEWST) required. This input indicates the level of engineering design effort for integration of structural items into a system or subsystem.

6. Designed operating environment (PLTFM) which is the specification level that describes the intended operating environment and reliability requirements for each system. PLTFM=1.8, the PRICE H default value for military environments.

7. Month/year of start of development (DSTART);

8. Month/year of completion of first prototype not including field tests (DFPRO);

9. Month/year development completed (DLPRO); and

10. Number of prototype units chargeable to development effort (PROTOS1); number of government furnished equipment prototypes chargeable to development (PROTOS2); number of prototype systems to be integrated and tested during development (PROTOS3).

11. ESC; and

12. Development cost multiplier (DMULT). In this study, the DMULT variable is used to input VHSIC chip development costs from PRICE M.

13. Level of draft requirements for the development phase (DDRAFT). DDRAFT=1, the default value for PRICE H (28:19.1-19.13).

CDES2 = Cost of laboratory experimental work, design and development engineering, and requisition engineering.

CDES2 is further defined to be:

$$CDES2 = (CDRAFT)DF \tag{10}$$

where

DF = Design/drafting factor which is a function of:

1. DFPRO;

2. DLPRO;

3. ESC;

4. DMULT; and

5. A constant factor controlling the level of developmental engineering design (DDSIGN). In this study, DDSIGN=1, the default value (28:19.12).

CSYS2 = The cost of converting performance requirements into design specifications.

CSYS2 is further defined as follows:

$$CSYS2 = (CDRAFT + CDES2)SE2 \tag{11}$$

where

SE2 = Systems engineering factor which is a function of:

1. DFPRO;
2. DLPRO;
3. ESC; and
4. DMULT (28:19-13).

CPMGT2 = The cost of program management and control which includes travel expenses, computer operations, reports, and quality assurance.

CPMGT2 is further defined to be:

$$CPMGT2 = (CDRAFT2 + CDES2)PM2 \tag{12}$$

where

PM2 = Project Management factor which is a function of:

1. DFPRO;
2. DLPRO;
3. ESC; and
4. DMULT (28:19-13).

CDAT2 = Documentation cost for manuals, lists, reports, and drawings.

CDAT2 is defined further as follows:

$$CDAT2 = (CDRAFT2 + CDES2 + CSYS2)DF2 \tag{13}$$

where

DF2 = Data factor which is a function of:

1. DFPRO;

2. DLPRO;

3. DMULT; and

4. Level of data requirements for the development phase (DDATA). In this study, DDATA=1, the default value.

CPROTO2 = Development cost for prototypes including material, labor, overhead, integration and testing. Prototype cost is a function of:

1. MCPLXE;

2. MCPLXS;

3. YRTECH;

4. PROTOS1;

5. PROTOS2;

6. PROTOS3;

7. ESC;

8. DMULT; and

9. Prototype adjustment factor (PRMULT). In this study, PRMULT=1, the PRICE H default value (28:19.15).

CTTEQ1 = Cost of all special tools and test equipment (not capital equipment) and any refurbishment. Tooling and test equipment cost is a function of:

1. MCPLXE;

2. MCPLXS;

3. YRTECH;

4. PROTOS1;

5. PROTOS2;

6. PROTOS3;

7. DFPRO;

8. ESC; and

9. DMULT (28:19.18).

Software Development Cost (DC_3).

$$DC_3 = DOSC + DSSC \tag{14}$$

where

DOSC = Cost of software used operationally by the prototype system and the production system.

DSSC = Support software cost for the prototype system and production system.

Operational and support software costs are further defined as:

$$DOSC = (DNOW)(DCOL) + DCOP \tag{15}$$

where

DNOW = Total number of lines of operational code specifically written for the development system and production system. This includes discarded code as the system evolves.

DCOL = Average cost of operational software per line written.

DCOP = Total cost of purchased software used operationally in the prototype system and production system.

$$DSSC = (DNSW)(DCSL) + DCSP \tag{16}$$

where

DNSW = Total number of lines of support code written for the prototype system and production system. This includes analysis, simulation, and system software.

DCSL = Average cost of support software per line written.

DCSP = Total cost of purchased support software in support of the prototype system and the production system.

Production Costs

Production costs are the sum of five cost equations.

They are:

1. VHSIC chip production costs from PRICE M (30);
2. Production system design, fabrication, integration and test from PRICE H (28);
3. Special test equipment costs from PRICE L (29);
4. Cost of initial spares at all supply locations from PRICE L (29); and
5. Cost to enter spares into the supply system from PRICE L (29).

mathematically

$$PC_i = \sum_{i=1}^{5} PC_i \qquad (17)$$

where

PC_1 = Total cost of VHSIC chip production.

PC_2 = Total cost of system hardware design, fabrication, integration and test during the production phase. In addition, this cost includes the integration and test cost of all VHSIC chips.

PC_3 = Total acquisition cost of special test equipment and support equipment.

PC_4 = Total cost of initial spares (chips, PCB, and SAR) at all supply locations for all theaters.

PC_5 = Total cost to enter and catalog spare items into the supply system.

VHSIC Chip Production Cost (PC_1).

$$PC_1 = AUC1_i (QTY1_i) \qquad (18)$$

where

$AUC1_i$ = Average unit production cost of VHSIC chip type i. Average unit cost is a function of:

1. Number of production units (QTY1) to be fabricated and delivered in the production period;
2. LENGTH;
3. WIDTH;
4. PINS; and
5. Production specification level (PROFAC) which describes the manufacturing specifications of the chip. In this study PROFAC=8, the PRICE M default value for military manufacturing specifications.
6. Type of package (PKGFAC) in which the VHSIC chip is assembled, tested, and delivered; and
7. Percentage of VHSIC chips that pass production acceptance tests (OVLYLD).

OVLYLD is further defined to be:

$$OVLYLD = (CPYLD) \quad (ASMYLD) \qquad (19)$$

where

CPYLD = Wafer test and probe yield for chip type i.

ASMYLD = Assembly and test yield for VHSIC chip type i.

8. Number of mask levels needed to fabricate the chip;
9. Chip substrate factor (SUBFAC) which describes the type of substrate used; and
10. Manufacturing calibration index (MINDEX) which relates past experience to new products.

$QTY1_i$ = Number of VHSIC chips to be fabricated and delivered in the production period (30:7.11-7.14).

<u>Production System Design and Fabrication Cost (PC_2)</u>.

$$PC_2 = CDRAFT2 + CDES3 + CPMGT3 + CDAT3 + CPROD1 + CTTEQ2 \qquad (20)$$

where

CDRAFT = Production drafting costs for drawings, data lists, specifications, and incorporation of engineering changes into drawings. Production drafting is a function of:

1. MCPLXE;

2. MCPLXS;

3. YRTECH;

4. NEWEL;

5. NEWST;

6. PLTFM;

7. ESC; and

8. Production cost multiplier (PMULT). In this study, PMULT=1, the PRICE H default value.

9. Production draft multiplier (PDRAFT). In this study, PDRAFT=1, the PRICE H default value (28:19.25).

CDES3 = Cost of production engineering and laboratory experimental work. Production design is a function of:

1. MCPLXE;

2. MCPLXS;

3. YRTECH;

4. PLTFM;

5. ESC;

6. PMULT; and

7. Production design multiplier (PDSIGN) PDSIGN = 1, the default value in this study.

CPMGT3 = Cost of program management and control which includes travel expenses, computer operations, reports, and quality assurance.

CPMGT3 is further defined to be:

$$CPMGT3 = (CDRAFT2 + CDES3)PM3 \qquad (21)$$

where

PM3 = Project management factor which is a function of:

1. Month/year that production cycle starts (PSTART); and

2. Month/year of completion of production (PEND) (28:19.29).

CDAT3 = Documentation cost for technical manuals, lists, reports, and drawings.

CDAT3 is defined as:

$$CDAT3 = (CDRAFT3 + CDES3)DF3 \qquad (22)$$

where

DF3 = Data factor which is a function of:

1. PSTART;

2. PEND;

3. ESC; and

4. PMULT (28:19-30).

CPROD1 = Manufacturing costs to include material, labor, setup, overhead, and quality control. Manufacturing costs are a function of:

1. MCPLXE;

2. MCPLXS;

3. YRTECH;

4. QTY1;

5. Quantity of GFE items (QTY2);

6. I&T quantity (QTY3);

7. Weight of structure in pounds (WS);

8. Weight of equipment in pounds (WT);

9. Envelope volume of an item in cube feet (VOL);

10. Level of integration and test requirements for electronics (INTEGE);

11. Level of integration and test requirements applicable to structural items (INTEGS);

12. Number of systems or subsystems required for integration to the next higher assembly level (QTNHA); and

13. Economic base year (YRECON). In this study, YRECON = 1984.

14. ESC; and

15. PMULT (28:19.31-19.32).

CTTEQ2 = Tooling and test equipment needed to support production. Tooling and test equipment is a function of:

1. WS;
2. WE;
3. MCPLXS;
4. MCPLXE;
5. YRTECH;
6. PSTART;
7. QTY1;

8. QTY2;

9. QTY3;

10. PEND;

11. ESC; and

12. PMULT (28:19.33).

Special Test Equipment Cost (PC_3).

$$PC_3 = \sum_{i=1}^{3} OD_i \sum_{i=1}^{3} DD_i(CFIM) + \sum_{i=1}^{3} DD_i(CFIP) \tag{23}$$

where

OD_i = Number of organization level maintenance locations for each theater i.

DD_i = Number of depot level maintenance locations for each theater i.

CFIM = The cost to develop and produce a test set capable of fault isolating to the module level (PCB) and test the LRU (SAR) after the module has been removed and replaced.

CFIP = The cost to develop and produce a test set capable of fault isolating to a faulty part (VHSIC chip) and would support fault isolation to the module level (29:9.5).

Initial Spares Cost (PC_4).

$$PC_4 = (CUP/RNU)^{EUP} + (CMP/RNM)^{EMP} + (CPP/RNP)^{EPP} + \{(CPPE)(FPE)\} \tag{24}$$

where

EUP = PRICE L improvement factor used to adjust the average cost of an LRU in production.

EMP = PRICE L improvement curve for modules to adjust the average cost of a module in production.

EPP = PRICE L improvement curve for parts to adjust the average cost of a part in production.

CUP = Average unit production cost of an LRU. This value is calculated by PRICE H.

CMP = Average cost of modules in production. This value is calculated by PRICE H.

CPP = Average cost of a single part in production. This value is derived from PRICE M AUC1 of each type i chip.

CPPE = Average cost of a part which is replaced only in the installed equipment.

FPE = Fraction of parts (VHSIC chips) replaced at equipment. This value is zero for this study.

RNU = Production quantity of LRUs. This variable has same value as PRICE H QTY1.

RNM = Reference quantity of complete sets of unique modules.

RUP = Reference quantity of complete sets of unique parts (29:9.5).

<u>Cost to Enter Spares Into Supply (PC_5)</u>.

$$PC_5 = \{(PODF)(PP)(FNSP) + P + \{\sum_{i=1}^{3} ED_i(EE)\}\}CEN \quad (25)$$

where

PODF = Parts overlap discount factor. PODF = 1 for this study.

PP = Quantity of part types per LRU.

FNSP = Percentage of parts that are not stock listed.

P = Quantity of module types per LRU.

ED_i = Number of equipment locations for theater i.

EE = Number of LRUs per equipment location.

CEN = Cost to enter item in the supply system (29:9.6).

Logistics Support Costs

Logistics support costs in PRICE L are the sum of six subcosts. They are:

1. Support of support equipment support;
2. Supply support;
3. Supply administration support;
4. Manpower support;
5. Contractor support; and
6. Supply-spare storage and shipping costs (29:9.4).

mathematically

$$\text{Logistics Support Cost} = \sum_{i=1}^{6} LSC_i \qquad (26)$$

where

LSC_1 = Cost to maintain and support the support equipment of a program.

LSC_2 = Cost for procurement of Balanced Consumed Spares (LRUs, modules, parts).

LSC_3 = Cost to retain new items in the supply system over the life of the program.

LSC_4 = Cost of labor required for operating and maintaining equipment over the life of the program.

LSC_5 = Cost of contractor depot level repair for LRU maintenance. This cost is not included in this study.

LSC_6 = Cost of supply-spares storage, support equipment storage, and shipping.

Cost to Maintain Support Equipment (LSC_1).

$$LSC_i = PC_3(PCTS) \tag{27}$$

where

PCTS = Support equipment annual upkeep fraction. In this study, PCTS=.10, the PRICE L default value.

Procurement of Balanced Consumed Spares (LSC_2).

The unit costs are derived in the same manner as PC_4, but lot-buy quantities are smaller. Thus, balanced consumed spaces have a higher unit cost (29:6.7).

Supply Administration Cost (LSC_3).

$$LSC_3 = \{(PODF)(PP)(FNSP) + P + (\sum_{i=1}^{3} ED_2(EE))\}(CAD)(\sum_{i=1}^{3} ODS_i) \tag{28}$$

where

CAD = Annual cost to maintain an item in the supply system.

ODS_i = Number of organization level supply locations for each type i theater.

Manpower Cost (LSC_4).

$$LSC_4 = (NRA)(CUE, CUO, CUD)(TRE)$$

for unscheduled maintenance (29)

or

$$(SMF)(OTF)(CUE, CUO, CUD)$$

for scheduled maintenance (30)

where

NRA = Number of repair actions.

CUE = Cost per man-hour at equipment.

CUO = Cost per man-hour at organization.

CUD = Cost per man-hour at depot.

TRE = On equipment MTTR, hours.

SMF = Fraction of equipment operating time that manpower is assigned at the equipment level on a scheduled basis. In this study, SMF=0, the default value.

OTF = On time fraction or operating hours per month.

Contractor Depot Cost (LSC_5).

This cost is not represented in this study.

Supply-Space Storage and Shipping Costs (LSC_6).

$$
\begin{aligned}
LC_6 = {} & (CFTO2,\ CFTD2)(FTSQF) + (CFTO2,\ CFTD2)(FTSQP) \\
& + (CFTO2,\ CFTD2)(FTSQC) + (CFTO3,\ CFTD3)(CUBEU) \\
& + (CFTO3,\ CFTD3)(CUBEM) + (CFTO3,\ CFTD3)(CUBEP) \\
& + (WU,\ WM,\ WP)\left(\sum_{i=1}^{3} CDID_2\right)
\end{aligned} \tag{31}
$$

where

CFTO2 = Support equipment space cost (dollars/square feet/month at organization level.

CFTD2 = Support equipment space cost (dollars/square feet/month) at depot level.

FTSQF = Floor space occupied by an LRU test set.

FTSQP = Floor space occupied by a module test set.

FTSQC = Floor space occupied by LRU checkout test set at organization maintenance facility.

CFTO3 = Supply space cost (dollar/square feet/month) at organization level.

CFTD3 = Supply space cost (dollar/square feet/month) at depot level.

CUBEU = LRU storage volume.

CUBEM = Module storage volume.

CUBEP = Part storage volume.

WU = LRU weight in pounds.

WM = Module weight in pounds.

WP = Part weight in pounds (29:9.8).

$CDID_i$ = Cost to ship from organization to depot for theater i.

<u>Spares Cost and Placement</u>

Determining the quantities and types of spares to support a mission is a crucial aspect in LCC analysis. The ultimate goal is to insure an acceptable operational readiness rate with minimum quantity of spares and their related logistics costs.

Spares requirements computed in PRICE L are categorized and defined as follows:

1. Initial Spares. Initial spares (ISPARE) are LRUs, modules, and parts needed to fill the supply pipelines at the beginning of a program. They are manufactured and procured concurrently with primary equipment, and their costs are based on combined quantities of initial spares and primary mission equipment.

   In this study, initial spare LRUs and modules are considered repairable throughout the life of the program.

mathematically

$$ISPARE = MSPARE + CK(MSPARE)^{1/2} + Z \qquad (32)$$

where

MSPARE = Mean quantity of spares.

Mean quantity of spares is further defined as:

$$MSPARE = (ADFAC)(BSQTY) \quad (33)$$

where

ADFAC = Adjustment factor.

Adjustment factor is further defined as:

$$AFAC = (ED)(OTF)(OA) \quad (34)$$

where

$$OA = (MTBF/OTF)/(MTBF/OTF) + TDOWN.$$

where

TDOWN = Downtime.

Downtime is further defined to be a function of:

1. TRE;
2. Days of supply at equipment level (DOSE);
3. Days of supply at organization for repairable items (DOSOR); and
4. Days of supply at intermediate for repairable items (DOSIR). Although intermediate level maintenance is not used in this study, DOSIR is used to reflect pipeline time between organization and depot.
5. Days of supply at depot (DOSDR).

where

BSQTY = Basic supply quantity.

Basic supply quantity is further defined to be:

$$BSQTY = (DDR)(DOS) \tag{35}$$

where

DDR = Daily demand rate.

Daily demand rate is defined to be a function of:

1. Daily failure rate (DFR)

where

DFR = {(24 HOURS)(EE)(RATIO)}/MTBF.

where

RATIO = A multiplier used to adjust MTBF per theater. In this study, RATIO=1.

2. Maintenance actions at each maintenance facility.

DOS = Days of supply for respective supply locations.

CK = Safety stock coefficient for LRUs (CKU), modules (CKM), and parts (CKP) for each organization level. In this study, CK values are PRICE L default values.

Z = Stock roundup factor computed for LRUs (ZU), modules (ZM), and parts (ZP) for each organizational level. In this study, ZU values are PRICE L default values.

2. Balance Consumed. Balance consumed spares are required when initial spare quantities (ISPARE) are not sufficient to cover all scrap for the duration of the program (29:6.7). As mentioned, ISPAREs are procured at the beginning of the deployment and are sufficient to fill pipelines in accordance with the number of authorized days of supply.

If LRUs or modules are scrapped, PRICE L computes total life cycle consumption of LRUs and modules. From these subtotals are subtracted respective ISPARE quantities. This balance then becomes the balanced consumed quantities. For parts, ISPAREs plus balanced consumed spares equals the total life cycle spares requirements.

The assignments of LRU, module, and part spares are as follows:

1. Parts are stocked at the location where repairs are accomplished to the piece-part (FIP). In this study, parts are stocked at depot (FIPD).

2. Modules are stocked at the location where the LRU is repaired by replacing modules. In this study, modules are replaced at equipment (FIME) and repaired at organization (FIPO).

3. LRUs are stocked at organization supply (ODS) to replace LRUs removed from equipment (29:6.10).

LCC Model Summary

The LCC model presented in this chapter is composed of functional relationships from each of the three cost models used in this study. These relationships are combined in the form of mathematical expressions to represent the three basic phases of an avionics system LCC. The expressions given here are intended to illustrate how variables are used and not portray actual CERs.

V. LCC Input Data

The Second Tri-Service Workshop on Manufacturing Technology (MT) Program Planning for VHSIC Technology has identified 12 characteristics of VHSIC Phase 1 technology needing MT programs (34:7). The workshop has determined these programs essential if "VHSIC is to remain on schedule for system technology insertion" (34:2). This study investigates four of these 12 areas. They are the effects on LCC of chip technology and design, fabrication yields, substrate type, and computer-aided-design. In addition, a fifth area, maintenance level, is studied. Each of these areas must be narrowed to factors that can be quantified and used as parametric inputs to the PRICE M, PRICE H, and PRICE L models. Parametric inputs are defined as numerical inputs which characterize the components (VHSIC chips, hardware, software etc.) and logistics support concepts for the four basic cases of the insertion model (SAR processor) introduced in Chapter III.

The LCC model developed in the last chapter has more than 200 parametric input variables. Initial values assigned to these variables describe the four basic cases of the insertion model. These initial values are termed default values. This chapter details the derivations and assumptions for default values that characterize VHSIC chips, hardware design and layout, and logistics support. However, some default values such as complexity factors taken from the RCA PRICE User's Manuals are not discussed here (28, 29, 30). These defau . values along with those presented in this chapter are summarized in Appendix A. Finally, Appendix B describes variations made to default values for sensitivity analysis of the five areas previously mentioned.

VHSIC Phase 1 Chip Densities and Chip Size by Technology and Function

This section provides data for the densities of VHSIC chips, their size, power requirement, number of pins, number of unique cells, and the number of chips and PCBs needed to implement each SAR processor function presented in Chapter III.

Gate Densities for Logic Chips. The gate densities for VHSIC Phase 1 chips by technology are shown in Table VI for custom designed chips and Table VII for gate array designed chips. Data for gates/mil^2 for custom chips are derived from data for gates/mm^2 taken from Sumney (37:36-38). Entries under "Gates/mil^2" are gotten by multiplying gates/mm^2 by 6.4516 X 10^{-4}. Cells/mil^2 are obtained by multiplying gates/mil^2 by 5 to get the devices/mil^2. Then devices/mil^2 are divided by 6, the number of devices/cell, to get cells/mil^2. Next, assuming 85% useable cell area per chip, devices/cell are multiplied by .85 to get useable cells/mil^2 (5:40-41). Finally, data for gates/mil^2 for gate array chips are taken from Blasingame. These data assume 80% cell utilization for gate array designed chips (3).

Cell Densities for Memory Chips

The memory cell densities for static Random Access Memory (RAM) chips are shown in Table VIII. Data entered under "Bits/mil^2" are taken from Blasingame (3). Assuming one bit per cell, then cells/mil^2 are equal to bits/mil^2 (5:40).

TABLE VI

Gate Densities for Custom Chips by Technology (5:41, 37:36-38)

Technology	Gates/mm^2	Gates/mil^2	Cells/mil^2
BIPOLAR 3D/STL	390	.2516	.1782
CMOS/SOS	400	.2581	.1828
NMOS	570	.3677	.2605
BIPOLAR ISL/CML	480	.3097	.2194
CMOS/Bulk	558	.3596	.2547

TABLE VII

Gate Densities for Gate Array Chips as a Function of Technology (3)

Technology	Gates/mil^2	Cells/mil^2
CMOS/Bulk	.1488	.1240
BIPOLAR 3D/STL	.1740	.1449

TABLE VIII

Cell Densities for Memory Chips as a Function of Technology
(5:40, 37:36-38, 3, 18:274)

Technology	Bits/mil^2	Cells/mil^2
CMOS/Bulk (Static RAM)	1.309	1.309
NMOS (Static RAM)	1.652	1.652

Calculation of Chip Size and Number of Chips per Function. This section partitions the SAR processor into the number of logic and memory chips of appropriate sizes. The total logic and memory requirements are summarized in Table IV of Chapter III.

Nearly 51,000 gates of high speed logic are needed to implement the signal processor portion, and approximately 100,000 gates of slower logic are required to implement the control processor. The logic naturally divides between two chip types, a fast signal processor chip and a slower control processor chip.

Assuming 15% of the area of an integrated circuit chip is devoted to nonuseable area (benching pads, border area, chip test points, etc.) and using data from Table VI, chip dimensions are derived as shown in Tables IX, and X for signal processor chips and Tables XI and XII for control processor chips (5:40). Due to current fabrication yields for VHSIC Phase 1 technologies, chip dies with edge dimensions of larger than 350 mils are not economically feasible (3). Therefore, entries under "Gates/Chip (K)" are based upon edge dimension of 350 mils or less. The column entitled "Edge Dimension (mils)" gives the side dimensions for chips of each technology. The edge dimensions in Tables X and XII assume 80% useable cells per chip (3). Other data, "Watts/Chip" and "Pins/Package", are based on these dimensions. Finally, entries under "Unique Cells" are based on assumptions taken from Demarco that 85% of the cells for custom chips are unique design, and 50% of the cells for gate array chips are unique design (8:1027-1030).

TABLE IX

Custom Chip Sizes as a Function of Technology for Signal Processor (5:38, 36:36-37, 35:52-54, 8:1027-1030)

Technology	Gates/ Chip (K) (GATES)	Edge Dimensions (mils) (LENGTH,WIDTH)	Watts/ Chip	Pins/ Package (PINS)	Unique Cells*
BIPOLAR 3D/ STL	25.5	345.31	6.9	180	18062
BIPOLAR ISL/CML	25.5	311.24	4.0	180	18066
CMOS/Bulk	25.5	188.83	.71	180	18061
CMOS/SOS	25.5	340.93	1.7	180	18061
NMOS	25.5	285.63	2.8	180	18065

*Assume 85% of Cells on Each Chip are Unique

TABLE X

Gate Array Chip Sizes as a Function of Technology for Signal Processor (3, 5:40, 36:36-37, 35:52-54, 8:1027-1030)

Technology	Gates/Chip (K) (GATES)	Edge Dimension (Mils)* (LENGTH,WIDTH)	Watts/Chip	Pins/ Package (PINS)	Unique Cells+
CMOS/ Bulk	10.2	283.98	Negligible	148	5004
BIPOLAR 3D/STL	10.2	262.61	Negligible	148	5080

*Assume 80% Useable Cells Per Chip.
+Assume 50% of Cell on Each Chip are Unique.

TABLE XI

Custom Chip Sizes as a Function of Technology for Control Processor (5:38, 3, 36:36-37, 8:1027-1030, 35:52-54)

Technology	Gates/ Chip (K) (GATES)	Dimensions (mils) (LENGTH, WIDTH)	Watts/ Chip	Pins/ Package (PINS)	No. of Unique Cells*
BIPOLAR 3D/STL	25	341.90	6.8	180	17707
BIPOLAR ISL/CML	25	308.17	3.9	180	17711
CMOS/Bulk	25	285.99	.70	180	17708
CMOS/SOS	25	337.57	1.6	180	17707
NMOS	25	282.82	2.7	180	17711

*Assume 85% of Cells on Each Chip are Unique.

TABLE XII

Gate Array Chip Sizes as a Function of Technology for Control Processor (5:40, 36:36-37, 35:52-54, 8:1027-1030)

Technology	Gates/Chip (K) (GATES)	Edge Dimension (Mils)* (LENGHT,WIDTH)	Watts/Chip	Pins/ Pakcage (PINS)	Unique Cells+
CMOS/Bulk	10.0	281.18	Negligible	148	4906
BIPOLAR 3D/STL	10.0	260.02	Negligible	148	4980

*Assume 80% Useable Cells per Chip.

+Assume 50% of Cells on Each Chip are Unique.

The amount of memory required for the SAR processor is high, 1762 Mbits in the signal processing portion and 12 Mbits in the control processor part. Table XIII gives chip sizes by technology to implement the signal processor and control processor memory functions. The densities given in Table VIII are used to determine edge dimensions. Also, these dimensions are based on assumptions that all memory chips are limited to 64K bits/chip and that 15% of the total chip area is devoted to nonuseable area (3, 5:42). Like logic chips, data for "Pins/Package" and "Watts/Chip" are based on the chip's edge dimensions. Entries under "Transistors/Chip" are obtained by multiplying 64 by 1024 to get the number of bits/chip and then multiplying this product by 6 to get the number of transistors per chip (5:42). Finally, data for "Unique Cells" are based on the assumption that 15% of the cells for a custom designed memory chip are unique design (8:1027-1030).

Table XIV shows the number of custom and gate array designed chips needed to implement each SAR processor function. Entries in this table are based on the number of gates per chip given in Tables IX, X, XI, XII and transistors per chip given in Table XIII.

Calculation of the Number of PCBs. By combining the data in Tables IX, X, XI, XII, XIII, and XIV, and the hardware assumptions made in Chapter III, the mix of PCBs that make up the SAR processor is shown in Table XV. Note that the same number of PCBs are needed for both memory technologies. However, due to lower power requirements and better dependability for CMOS/Bulk technology, only CMOS/Bulk memory chips are used in this study (37:35).

TABLE XIII

Memory Chip Sizes as a Function of Technology for Signal Processor and Control Processor (5:42, 3, 35:52-54, 8:1027-1030)

Tech.	Bits/ Chips (K)	Edge Dimensions (Mils) (LENGTH, WIDTH)	Watts/ Chip	Pins/ Package (PINS)	Transistors/ Chip (XSTRS)	Unique Cells*
CMOS/ Bulk	64	223.75	.5	42	393,216	9831
NMOS	64	199.18	.5	32	393,216	9831

*Assume 15% of Cells on Each Chip are Unique.

TABLE XIV

Chips Per SAR Processor Function

SAR PROCESSOR - CUSTOM CHIPS

Signal Processor		Control Processor	
Logic	Memory	Logic	Memory
2	26,886	4	184

SAR PROCESSOR - GATE ARRAY CHIPS (LOGIC CHIPS ONLY)

Signal Processor	Control Processor
10.2K	10K
5	10

TABLE XV

Quantity and Composition of PCBs as a Function of Memory Chip Size

Memory Chip Size (mil X mil)	Number of VHSIC Chips on Each Board	
223.75 X 223.75	Board 1 6 Custom Logic or 15 GA Logic 270 Memory	Boards 2-68 0 Logic 400 Memory
199.18 X 199.18	Board 1 6 Custom Logic or 15 GA Logic 270 Memory	Boards 2-68 0 Logic 400 Memory

Calculation of VHSIC Fabrication Yields

Tables XVI and XVII provide fabrication yields for custom signal processor chips and control processor chips respectively by technology and substrate type. Likewise, Table XVIII and XIX show fabrication yields for gate array signal processor chips and control processor chips by technology and substrate types. Finally, Table XX provides fabrication yields for memory chips by technology and substrate type. All fabrication yields are calculated using equation 1 or 2 with wafer diameter size of five inches and chip die sizes given in Tables IX, X, XI, XII, and XIII. Data entries for "Mask Levels" are taken from Blasingame and Oldham (3, 26).

TABLE XVI

Custom Chip Fabrication Yields by Technology for Signal Processor (5:52, 3, 18:13-17, 26:111-128)

Technology	Substrate (SUBFAC)	CPYLD	ASMYLD	OVLYLD	Mask Levels (MSKLVL)
BIPOLAR 3D/STL	Bulk Silicon	.0587	.0431	2.53×10^{-3}	5
BIPOLAR ISL/CML	Bulk Silicon	.0723	.0196	1.42×10^{-3}	7
CMOS/BULK	Bulk Silicon	.0839	.0266	1.9×10^{-3}	5
CMOS/SOS	Silicon-on Saffire	.0220	.0162	3.6×10^{-3}	3
NMOS	Bulk Silicon	.0858	.0231	1.98×10^{-3}	5

TABLE XVII

Custom Chip Fabrication Yields by Technology for Control Processor (3, 5:43-52, 8:13-17, 111-128)

Technology	Substrate (SUBFAC)	CPYLD	ASMYLD	OVLYLD	Mask Levels (MSKLVL)
BIPOLAR 3D/STL	Bulk Silicon	.0598	.0440	2.63×10^{-3}	5
BIPOLAR ISL/CML	Bulk Silicon	.0737	.0199	1.47×10^{-3}	7
CMOS/BULK	Bulk Silicon	.0856	.0230	1.97×10^{-3}	5
CMOS/SOS	Silicon-on-Saffire	.0225	.0167	3.76×10^{-4}	3
NMOS	Bulk Silicon	.0875	.0235	2.06×10^{-3}	5

TABLE XVIII

Gate Array Chip Fabrication Yields by Technology for Control Processor
(5:43-52, 3)

Technology	Substrate (SUBFAC)	CPYLD	ASMYLD	OVLYLD	Mask Levels (MSKLVL)
CMOS/Bulk	Bulk Silicon	.0885	.0238	2.10×10^{-3}	5
BIPOLAR 3D/STL	Bulk Silicon	.1035	.0276	2.85×10^{-3}	7

TABLE XIX

Gate Array Chip Fabrication Yields by Technology for Signal Processor
(5:43-52, 3, 35:52-54)

Technology	Substrate (SUBFAC)	CPYLD	ASMYLD	OVLYLD	Mask Levels (MSKLVL)
CMOS/Bulk	Bulk Silicon	.0868	.0233	2.03×10^{-3}	5
BIPOLAR 3D/STL	Bulk Silicon	.1015	.0271	2.75×10^{-3}	7

TABLE XX

Custom Chip Fabrication Yields by Technology for Memory
(5:43-52, 3, 18:13-17, 26:111-128)

Technology	Substrate (SUBFAC)	CPYLD	ASMYLD	OVLYLD	Mask Levels (MSKLVL)
CMOS/ BULK	Bulk Silicon	.1398	.0367	5.13×10^{-3}	5
NMOS	Bulk Silicon	.1764	.0456	8.04×10^{-3}	5

Parametric Input Data for Design, Reliability, and Logistics Support

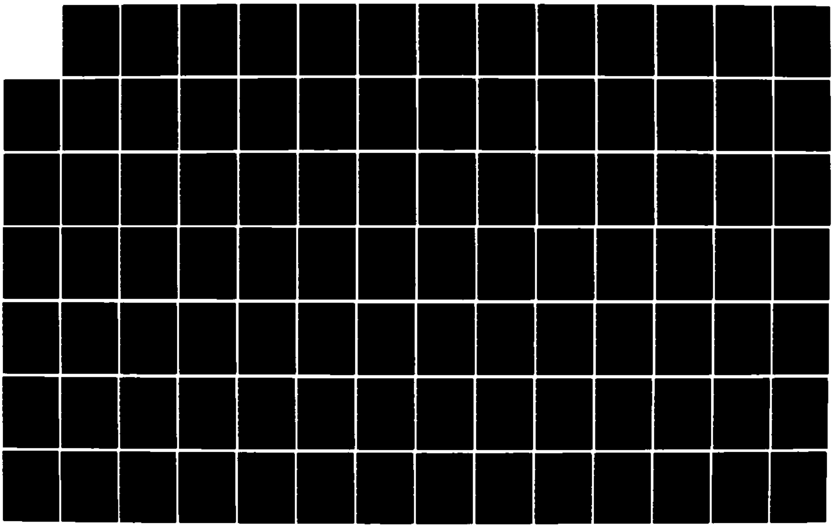
Now that chip sizes for the SAR processor have been characterized, the number of chips per function established, and expected fabrication yields determined, these data can be translated to parametric inputs that describe the SAR processor's design, reliability, and logistics support.

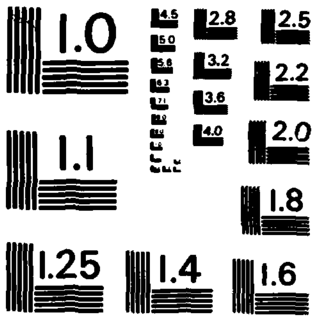
CAD and MTBF as a Function of Chip Size and/or Design. The size and/or design of VHSIC chips impact the cost of the SAR processor in three primary ways. First, smaller chips increase the number of PCBs needed to implement a system. For this study, 68 PCBs are required to implement the SAR processor.

Second, the SAR processor is impacted by chip design. The cost to design VHSIC chips is dependent upon two primary factors. One factor is whether the layout of the chip is a custom design or a gate array design. Custom designed chips require more time to layout. The other factor is whether CAD systems are used in the design and layout of each chip. The

AD-A147 798 LIFE CYCLE COST MODEL FOR VERY HIGH SPEED INTEGRATED CIRCUITS(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF SYSTEMS AND LOGISTICS E A LONG SEP 84 2/3

UNCLASSIFIED AFIT/GLM/LSM/84S-39 F/G 14/1 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

average time in man-months to design custom VHSIC chips is shown in Table XXI. Likewise, the average time in man-months to design gate array VHSIC chips is depicted in Table XXII. The values given in these tables are man-months to design a 10,000 gate logic chip or a 64K memory chip (5:54-56). Data under the entry "Cells not in Circuit Library" assume the more extensive the use of CAD, the fewer the number of cells requiring original design (8:1027-1030).

TABLE XXI

Estimated Man-Months to Design Custom Chips By Use of CAD
(5:38-56, 8:1027-1030)

CAD		Man Months to Design Chip*		
Use of CAD (CADFAC)	Cells Not in Circuit Library (NEWCEL)	Signal Processor	Control Processor	Memory
Very Little**	85%	46	45	2
Some+	50%	31	30	1
Extensive	5%	15	15	1

*Start of development (DSTRT) to date the Pattern Generation Tape is delivered (PSTRT).

**Default for logic chips (CADFAC=.8).

+Default for memory chips (CADFAC=1.0).

TABLE XXII

Estimated Man-Months to Design Gate Array Chips by Use of CAD (5:38-56, 5:1027-1030)

CAD		Man-Months to Design Chip*	
Use of CAD (CADFAC)	Cells Not in Circuit Library (NEWCEL)	Signal Processor	Control Processor
Very Little	85%	12	12
Some	50%	6	6
Extensive**	5%	3	3

*Start of development (DSTRT) to date the Pattern Generation Tape is delivered (PSTRT)

**Default for logic chip (CADFAC=1.2)

Finally, MTBF is affected by chip size and design. In this study, an assumption is made that the MTBF of VHSIC chips is a function of the complexity of chip design (39). Failure rates per chip per 1000 hours for chips in their useful life are given in Table XXIII. Notice that for the most complex designed chip (custom logic chips) the failure rate is equal to the DoD VHSIC Phase 1 Request for Proposal (RFP) failure rate of .006 failures per 1000 hours per chip (3, 5:53). Thus, the SAR processor MTBF is primarily a function of the number of VHSIC chips on each PCB and the number of PCBs in each SAR processor.

Further, other assumptions are that a chip package has a failure rate of 1 X 10^{-3} failures per 1000 hours and an unstuffed PCB with connectors has a failure rate of 1.7 X 10^{-3} failures per 1000 hours (39).

TABLE XXIII

Technology Mixes Considered for Each PCB in Determining the Effects of Chip Technology and MTBF on SAR Processor Cost (5:53-54, 39, 3, 37:36-38)

	Technology		Layout Method		Board MTBF*		
Case	Signal Processor	Control Processor	Design/ Number of Chips	Design/ Number of Chips	1 (Logic & Memory)	2-68 (Memory)	SAR MTBF**
1	BIPOLAR 3D/STL	CMOS/Bulk	Custom/2	Custom/4	2720 hrs	1684 hrs	510 hrs
2	BIPOLAR 3D/STL	CMOS/Bulk	Gate Array/5	Gate Array/10	3405 hrs	1684 hrs	530 hrs
3	BIPOLAR 3D/STL	CMOS/Bulk	Custom/2	Gate Array/10	3315 hrs	1684 hrs	528 hrs
4	BIPOLAR 3D/STL	CMOS/Bulk	Gate Array/5	Custom/4	3237 hrs	1684 hrs	526 hrs

*Assume:
$\lambda = .2 \times 10^{-3}/1000$ hours for memory chips and gate array chips.
$\lambda = 6.0 \times 10^{-3}/1000$ hours for custom logic chips.
$\lambda = 10^{-3}/1000$ hours for chip package.
$\lambda = 1.7 \times 10^{-3}/1000$ hours for unstuffed circuit boards with connectors.

**$\lambda = 1.0/1000$ hours for chassis, cables, blackplanes, etc.

Since the MTBF for each PCB is the reciprocal of the sum of the failure rates for each component part, and given that the MTBF for all PCBs is the reciprocal of the sums of each PCB, the MTBF for the logic and memory PCBs are as shown in Table XXIII. Finally, this study assumes a failure rate of 1.0 failures per 1000 hours for the rest of the SAR processor (cables, chassis, backplane, etc.) (5:53-54). Therefore, the total MTBF for the SAR processor for each of the four cases studies are as shown in Table XXIII.

Chip Technology. Table XXIII also shows the technology mixes and layout configurations used in this study. Only the signal processor and control processor are considered here, because memory chips were restricted earlier to CMOS/Bulk technology and custom layout. Like memory chips, the control processor chips are restricted to CMOS/Bulk technology due to the lower power requirements for this VHSIC technology (37:35). Similarly, the signal processor chips are limited to Bipolar technology because of the high FTRs for this technology (37:35). The number of chips needed for each layout method are obtained from Table IX and X for the signal processor and Tables XI and XII for the control processor.

Maintenance Levels. Tables XXIV and XXV give the parametric input data used to analyze the impact on LCC for various fractions of failures which are repaired at organization level and depot level. In both tables, the author assumes that 95% of all faulty SAR processors can be fault isolated to the module level (PCBs) and repaired at equipment with the remaining 5% repaired at depot. Data in Table XXIV, the default case for this study, assume 95% of the faulty PCBs are repaired at

TABLE XXIV

Level of Maintenance (95% of PCBs Repaired at Organization)

Maintenance	Case 1	Case 2	Case 3	Case 4
Fraction of SARs Repaired at Equipment (FUE)	.95	.95	.95	.95
Fraction of PCBs Repaired at Organization (FMO)	.95	.95	.95	.95
Fraction of Removed PCBs Repaired at Depot (FMD)	.05	.05	.05	.05

TABLE XXV

Level of Maintenance (5% of PCBs Repaired at Organization)

Maintenance	Case 1	Case 2	Case 3	Case 4
Fraction of SARs Repaired at Equipment (FUE)	.95	.95	.95	.95
Fraction of Removed PCBs Repaired at Organization (FMO)	.05	.05	.05	.05
Fraction of Removed PCBs Repaired at Depot (FMD)	.95	.95	.95	.95

organization with the remaining 5% repaired at depot. Conversely, data in Table XXV assume 5% of the faulty PCBs are repaired at organization with the remaining 95% repaired at depot.

The reader should note that these tables do not include costs for software maintenance or changes. However, one would expect that as software changes occur, new chips with changed firmware would be mounted on PCBs at depot and sent to organizations for assembly into SAR processors. Removed PCBs would then be sent to depot for firmware modification. However, this feature is not modeled in this study.

Hardware. Tables XXVI and XXVII describe dimensions and weight for chassis and circuit boards respectively. The chassy dimensions are based on 68 PCBs that are spaced 10/32 inches apart. In addition, a space (5" X 10" X 28") is reserved for the power supply. These dimensions are included for weight and volume of the chassy. This study does not model the cost of the power supply. The circuit board dimensions and volume are taken from data for ATR standard circuit boards (39). These data for chassy and PCB dimensions and weight are used in PRICE H for assessing integration and test costs. As mentioned in Chapter III, all hardware items except chip packages are represented in this study as GFE items. PRICE M includes the cost of chip packages in the unit production cost of chips. Finally, Table XXVIII depicts package types used in this study and the dimensions and volume of each.

Logistics Support Data. Table XXIX provides current AFLC labor and shipping rates, supply administration and support costs, and travel times for logistics support of spares (13:4).

TABLE XXVI

Parametric Data for Chassis (GFE Item) (5:57, 39)

CHASSY					
Quantity Next Higher Assembly (QTYNHA)	Dimensions	Volume (ft^3) (VOL)	Weight/ ft^3	Weight of Structure (WT)	Number Required (QTY2)
1	11" X 10" X 28"	1.94	34.5 lb	66.9 lbs	1000

TABLE XXVII

Parametric Data for Circuit Cards (GFE Item) (39, 28:4.14, 28:22.1)

CIRCUIT CARDS					
Logic PCB (QTYNHA)	Memory PCB (QTYNHA)	Volume (ft^3) (VOL)	Weight/ ft^3	Weight of Structure (WT)	Number Required (QTY2)
1	1	.0052	110	.572	68,000

TABLE XXVIII

Parametric Data for Chip Packages (39, 35:53)

PACKAGED CHIP					
Package Dimensions (In)	Volume (ft^3)	Weight (lbs)/ In^2	Weight (lbs)	Chip Type	Package Type (PKGFAC)
.5 X .5	1.8×10^{-4}	.013	.005	Memory-CMOS/Bulk	Pin Grid
.5 X .5	1.8×10^{-4}	.013	.005	Memory-NMOS	Pin Grid
1.85 X 1.45	2.1×10^{-4}	.013	.0349	Custom Logic Chips	Pin Array
1.1 X 1.1	8×10^{-6}	.013	.01573	Gate Array-Logic	Flat Pack

TABLE XXIX

AFLC Labor, Supply, and Shipping Rates and Supply Time (13:4)

Description	Rate or Time
Base level labor rate (CUO):	$29.00/hour
Depot level labor rate (CUD):	$41.00/hour
Packing and shipping rate (CONUS) (CDFD, CDID, CDIO):	$ 3.13/lb
Packing and shipping rate (overseas) (CDFD, CDID, CDIO):	$ 6.00/lb
Cost to enter item into supply system (CEN):	$1,200.00
Annual cost to maintain item in supply system (CAD):	$150.00
Supply time to CONUS bases (DOSDR, DOSIR):	10 days
Supply time to overseas bases (DOSDR, DOSIR):	15 days

Data Summary

The parameters and default values defined and reflected in the tables of this chapter are parametric inputs to the PRICE M, PRICE H, and PRICE L models which constitute the LCC model in this study. In addition to a description of each variable, the derivation and source of each were presented.

VI. LCC Output Data and Analysis

The results produced by the LCC model for each set of default values as described in Chapter V and Appendix A and changes to these values as given in Appendix B are presented in this chapter. Finally, the actual computer outputs which have been edited for readability are presented in Appendix B.

Impact of Chip Technology and Design on the SAR Processor's LCC

The variation of LCC due to signal processor and control processor chip technology and design is slight (3.9%) for the technology and design mixes examined. As shown in Table XXX, this variation comes primarily from development costs. This result should not be surprising since of the 26,076 VHSIC chips in the SAR processor, only six of them (two signal processor chips and four control processor chips) are investigated here with regard to chip technology and design. Recall that the only memory chip technology studied is CMOS/Bulk with custom design. In the worst case, the cost of the six logic chips represents only 1.1% of the total cost of all the chips in the SAR processor.

If one considers only the unit production cost (UPC) of logic chips (Table XXXI), the cost to implement the signal processor with custom chips is 26% higher than for gate array designed chips for Bipolar 3D/STL technologies. However, the cost to implement the control processor with gate array chips is 38% higher than with custom designed chips for CMOS/Bulk technology. Interestingly, the UPC to implement the signal processor and control processor functions with gate array designed chips is 8% higher than custom designed chips for Bipolar 3D/STL and CMOS/Bulk technologies. However, when all other costs are considered as shown in Table XXX, the total LCC of the SAR processor is slightly less using gate array designed logic chips.

TABLE XXX

LCC of the SAR Processor as a Function of Chip Technology and Design

Chip Technology		Costs*				
Signal Processor	Control Processor	Design	Dev. ($1.00)	Prod. ($1.00)	Support ($1.00)	Total LCC ($1.00)
BIPOLAR 3D/STL	CMOS/ Bulk	Custom	$425116.	$8617886.	$6852052.	$15895054.
BIPOLAR 3D/STL	CMOS/ Bulk	Gate Array	76675.	8581926.	6636718.	15295319.
BIPOLAR 3D/STL	CMOS/ Bulk	Custom/ Gate Array	251752.	8586153.	6659221.	15497126.
BIPOLAR 3D/STL	CMOS/ Bulk	Gate Array/ Custom	250066.	8583960.	6680172.	15514198.

*Costs are per SAR Processor in 1984 constant dollars based on default values for the four basic cases studied.

TABLE XXXI

Comparison of UPCs of Logic and Memory Chips by Technology and Design

Chip Technology	Design/Gates		Design/ Transistors	Unit Production Cost Per Chip ($1.00)*		
	Signal	Control	Memory	Signal	Control	Memory
BIPOLAR 3D/STL	Custom/ 25.5K	Custom/ 25K	-	$2047.60	$1801.38	-
BIPOLAR 3D/STL	GA/+ 10.2K	GA/ 10.0K	-	650.64	584.74	-
BIPOLAR ISL/CML	Custom/ 25.5K	Custom/ 25K	-	2144.01	1922.85	-
CMOS/ Bulk	Custom/ 25.5K	Custom/ 25K	Custom/ 393216	1082.53	981.20	$282.15
CMOS/ Bulk	GA/ 10.2K	GA/ 10.0K	-	603.78	542.15	-
CMOS/ SOS	Custom/ 25.5K	Custom/ 25.0K	-	2932.45	2662.42	-
NMOS	Custom/ 25.5K	Custom/ 25.0K	Custom/ 393216	1278.85	1305.14	288.72

*Costs are per chip in 1984 constant dollars based on default values for development and production of VHSIC chips.

+Gate Array

Impact of Substrate Type on the SAR Processor's LCC and UPC of Chips

As shown in Table XXXII, only custom designed chips are used for this LCC analysis, because the VHSIC Phase 1 program is not developing a gate array designed chip using SOS substrate (3). The use of SOS

TABLE XXXII

LCC of the SAR Processor as a Function of the Substrate Type for Signal Processor and Control Processor Functions

Technology				Costs*			
Substrate	Signal Processor	Control Processor	Design	Development Cost ($1)	Production Cost ($1)	Support Cost ($1)	Total Cost ($1)
SOS	CMOS/SOS	CMOS/SOS	Custom	$425116.	$8626670.	$6859115.	$15910901.
Bulk Silicon	BIPOLAR 3D/ STL	CMOS/Bulk	Custom	425116.	8617886.	6852052	15895054.

*Costs are per SAR processor in 1984 constant dollars.

substrate for signal processor and control processor chips results in a LCC of $15.91 million (1984 constant dollars) which is slightly higher (.063%) than the same SAR processor implemented with bulk silicon chips. However, only six of the 27,076 chips which make up the SAR processor have SOS substrates. Therefore, a better analysis of the cost differences between SOS and bulk silicon substrates can be obtained by comparing UPCs presented in Table XXXI. Both the signal processor and control processor functions implemented with CMOS/SOS chips are 171% higher than the same functions implemented with CMOS/Bulk chips.

Impact of Maintenance Level on LCC of the SAR Processor

Table XXXIII shows the LCCs of the SAR processor as a function of maintenance level for each of the four cases examined. These costs are a function of the percent of PCB repairs accomplished at organization and percent of PCB repairs accomplished at depot. Data presented in this table are based on the assumption that 95% of all SAR faults are isolated to the module level and repaired on-line (maintenance accomplished without removal from host system). The remaining 5% are repaired at depot.

Lower LCCs result when 95% of the PCBs are repaired at base level rather than depot level for the deployment scenario used in this study. Further, for all cases examined, LCCs for 95% of PCB repairs at organization level are approximately 12% less than 95% of PCB repairs at depot level. Figure 7 shows the percent of LCC difference between repairing 95% of PCB failures at the organization versus repairing only 5% of the PCB failures at organization for each of the four cases studied.

TABLE XXXIII

LCC of the SAR Processor as a Function of Maintenance Level

Percent of PCBs Repaired at Organization*	Percent of PCBs Repaired at Depot*	SAR Design	Costs** Dev. (1.00)	Prod. ($1.00)	Support ($1.00)	Total LCC ($1.00)
95	5	Case 1	$425116.	$8617886.	$6852052.	$15895054.
5	95	Case 1	425116.	8806682.	8525410.	17757208.
95	5	Case 2	76675.	8581926.	6636718.	15295319.
5	95	Case 2	76675.	8778374.	8236005.	17091054.
95	5	Case 3	251752.	8586153.	6659221.	15497126.
5	95	Case 3	251752.	8782600.	8265754.	17300106.
95	5	Case 4	250066.	8583960.	6680172.	15514198.
5	95	Case 4	250066.	8780406.	8292071.	17322543.

*Data based on the assumption that 95% of all repairs to SAR processors are fault isolated to module and repaired on-line.

**Costs are per SAR processor in 1984 constant dollars based on default values for the four basic cases studied.

Impact of CAD on LCC of the SAR Processor

As depicted in Table XXXIV, CAD analysis is limited to the most expensive default case (case one) and the least expensive default case (case two). The methods of this analysis assume that the remaining two cases (cases three and four) fall somewhere between case one and case two. Further, only signal processor chips and control processor chips are analyzed. Memory chips, being of regular architecture, show little variability in design man-hours whether or not CAD is used (8:1027-1030).

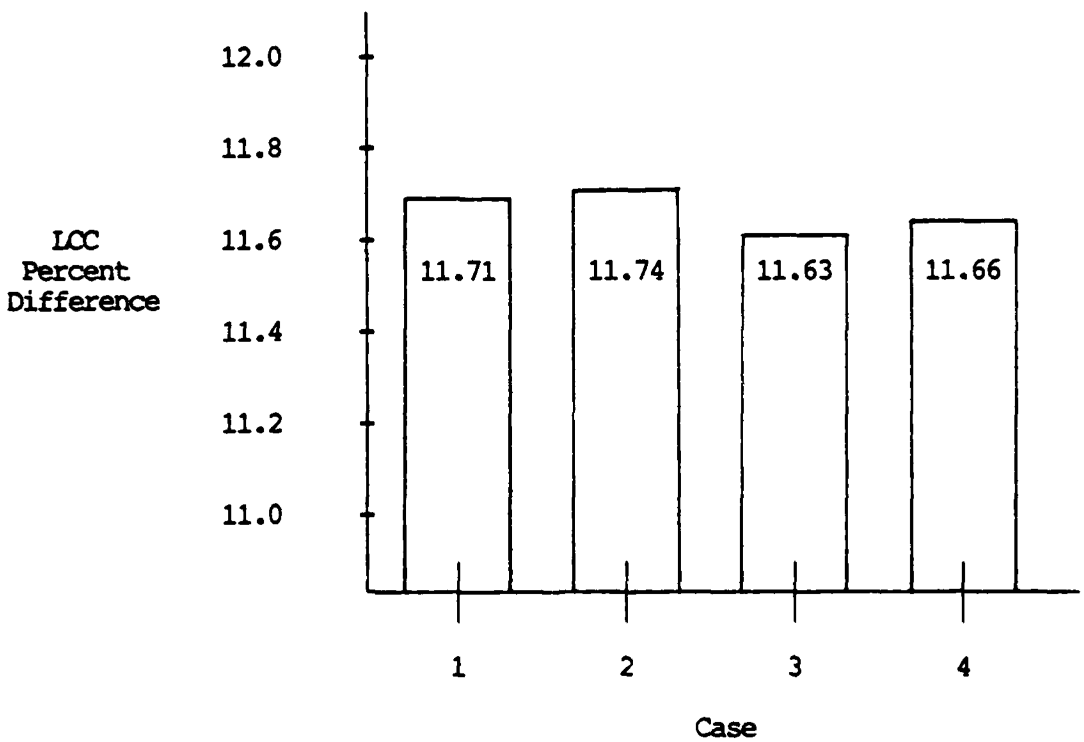


Figure 7. Percent Difference of the SAR Processor's LCC as a Function of 95% of PCB Faults Repaired at Organization Versus 95% Repaired at Depot

The LCC of the SAR processor differs by no more than 1.3% for custom

The LCC of the SAR processor differs by no more than 1.3% for custom designed chips and .065% for gate array designed chips regardless of the use of CAD. The greatest contribution of CAD studied in this analysis shortened the design man-hours by a factor of 3 to 1 for custom designed chips and 4 to 1 for gate array designed chips over very little use of CAD. Finally, memory chips for both cases are custom design with some CAD.

TABLE XXXIV

LCC of the SAR Processor as a Function of the Amount of CAD Used in the Design of the Signal Processor and Control Processor Chips

		Costs*			
Use of CAD	SAR Design	Dev. ($1.00)	Prod. ($1.00)	Support ($1.00)	Total LCC ($1.00)
Very Little	Case 1	$425116.	$8617886.	$6852052.	$15895054.
Some	Case 1	312310.	8617886.	6852052.	15782248.
Extensive	Case 1	241386.	8617886.	6852052.	15711324.
Very Little	Case 2	89435.	8586387.	6636718.	15312540.
Some	Case 2	81626.	8586387.	6636718.	15304731.
Extensive	Case 2	76675.	8581926.	6636718.	15295319.

*Costs are per SAR processor in 1984 constant dollars.

Impact of Overall Chip Fabrication Yields on the SAR Processor's LCC

Of all the variables examined in this study, fabrication yields show the greatest impact on the LCC of the SAR processor. Table XXXV shows LCCs as a function of overall fabrication yields for all SAR processor functions. Fabrication yield analysis is limited to default cases one

TABLE XXXV

LCC of the SAR Processor as a Function of Overall Chip Fabrication Yield for All SAR Functions

		Costs**			
Overall Yields for all Chip Functions	SAR Design	Dev. $1.00)	Prod. ($1.00)	Support ($1.00)	Total LCC ($1.00)
L.E. .5%*	Case 1	$425116.	$8617886.	$6852052.	$15895054.
1	Case 1	425116.	7136849.	5678963.	13240928.
5	Case 1	425116.	3887658.	3106643.	7419417.
10	Case 1	425116.	2051432.	1652646.	4129194.
L.E. .5%*	Case 2	76675.	8581926.	6636718.	15295319.
1	Case 2	76675.	7106528.	5500957.	12684160.
5	Case 2	76675.	3870883.	3011346.	6958904.
10	Case 2	76675.	2044579.	1602762.	3720016.

*Default yields.

**Costs are per SAR processor in 1984 constant dollars.

and two, because these two cases have the highest and lowest total LCC for the four default cases examined (Table XXX). The methods of this analysis are based on assumptions that changes in LCC for cases three and four fall somewhere between these cases. Figure 8 graphically shows the decrease in the SAR processor's LCC as overall fabrication yields increase from less than .5% to 10%. Note that fabrication yields can affect LCCs by over a factor of 4 for both cases.

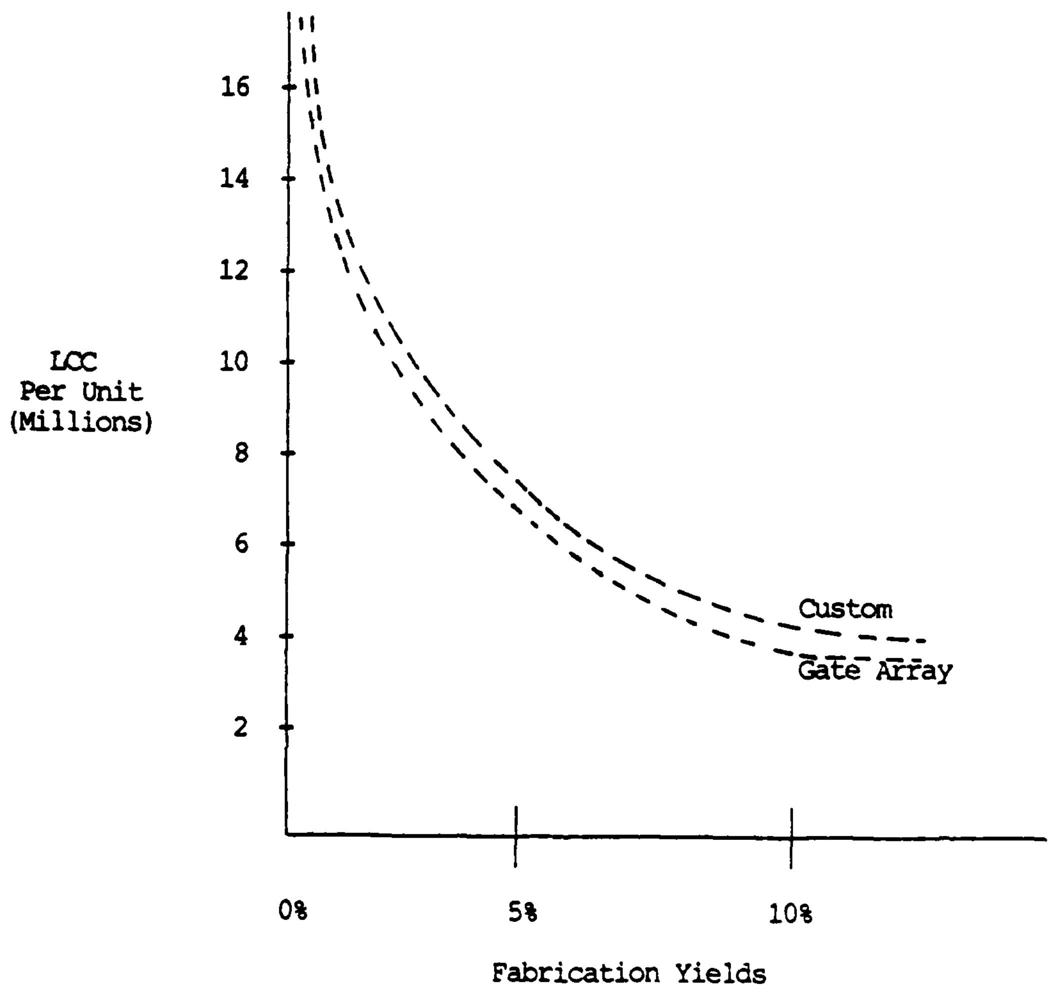


Figure 8. LCC of SAR Processor as a Function of Overall Fabrication Yields

Finally, Figure 9 shows the percent difference for the SAR processor's LCC as overall fabrication yields improve from less than .5% to over 10%.

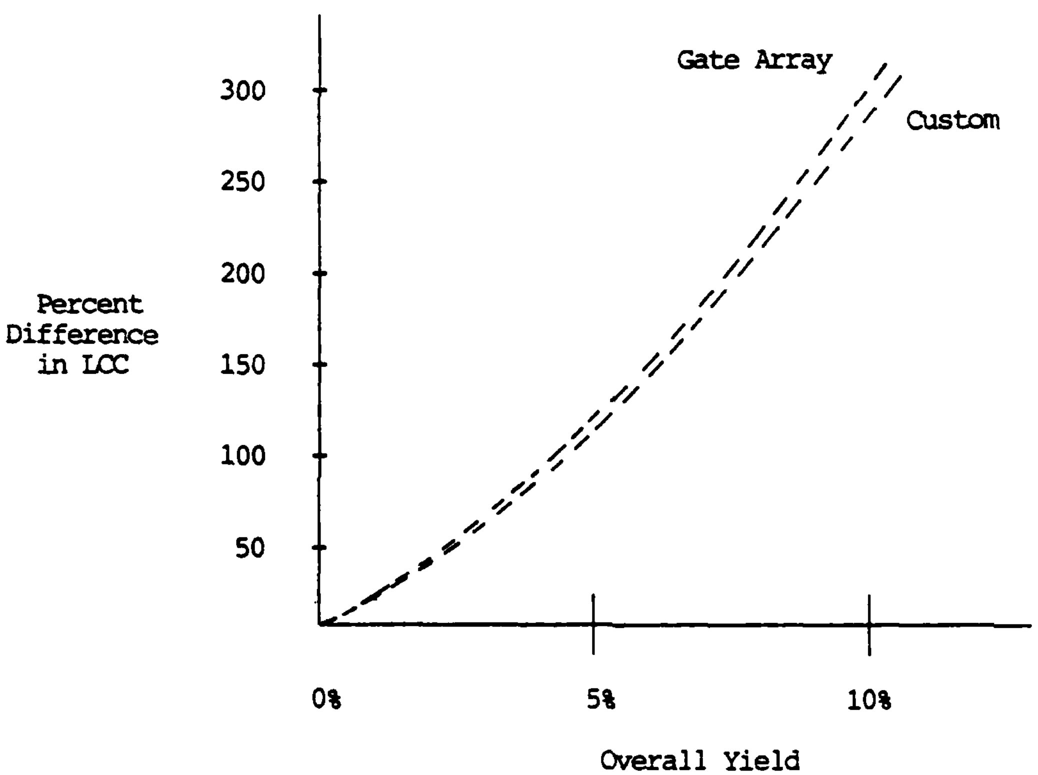


Figure 9. Percent Difference in LCC as Overall Fabrication Yields Improve

Analysis Summary

This chapter has presented LCC output data and analysis for chip technology and design mixes of the four cases studied. In addition, sensitivity analysis of output data was accomplished to determine the impact of substrate type, maintenance level, amount of CAD, and overall chip fabrication yield on the SAR processor's LCC. Conclusions drawn from the findings of this analysis are presented in Chapter VII.

VII. Summary, Recommendations, and Conclusions

This chapter summarizes findings of the analysis accomplished in Chapter VI. In addition, recommendations are made for further study of 1) the methods given in Chapter III, 2) uses for the LCC model developed in Chapter IV, and 3) the input data given in Chapter V and Appendix A. Finally, a brief conclusion is presented.

Summary of Findings

Of the factors examined in this study with respect to LCCs of a memory-intensive avionics system, the major cost drivers are chip fabrication yields, level of maintenance, and the use of silicon-on-sapphire rather than bulk silicon chip substrates. Other factors which make negligible difference in the LCCs are design-related items such as the use of computer-aided-design in the chip design process, and the use of gate array rather than custom chip layouts. Moreover, LCCs vary slightly regardless of which VHSIC Phase 1 technology is used to implement the logic functions (signal processor and control processor) of the memory-intensive SAR processor.

This study investigated only five of the many factors that can impact LCCs. Analysis of these factors indicate that they can impact LCCs by anywhere from 2 to 4 times. Improving chip fabrication yield rates are the largest single contributor to lowering LCCs.

Recommendations

The following are recommendations for further study of the methods used in this study.

1. Refine the LCC model presented in Chapter III to better represent development and support costs of software. For instance, software change costs should be included in the support phase. The software cost model used here is very top-level and provides a broad representation of software costs. RCA PRICE has a software LCC model (PRICE S) that might be used for this purpose.

2. Improve the chip fabrication yield model to represent improvements for yield rates as experience is gained. For example, chip assembly yields should improve in the production phase over the yields obtained in the development phase. Further, VHSIC chip fabrication is significantly more complex than for current technology such as Very Large Scale Integrated Circuits (34). The chip fabrication yield model should be refined to reflect this complexity.

The following are recommendations for further study of the use of the LCC model.

1. Much of the data in this study was obtained from other models (reference Chapter III) or educated opinions of experts (3, 5, 8, 39). When better empirical data are available, the input data used in this study should be refined.

2. Consider other insertion models besides the SAR processor. Because the SAR processor is memory-intensive and requires a large number of of chips, it is not representative of other avionics systems being studied for VHSIC insertion by the Air Force VHSIC Program Office (3, 4:18-22).

3. Use the LCC model to compare LCCs of one or more avionics system using conventional integrated circuits with the same systems using VHSIC Phase 1 chips.

4. Use the LCC model and insertion model presented here to compare LCC for VHSIC Phase 1 technology with VHSIC Phase 2 technology.

5. Study factors which contribute to LCCs other than those analyzed in Chapter IV. For example, this study assumed that PCBs are not scrapped at depot. But undoubtedly some PCBs will be condemned which could have a significant effect on LCCs.

Conclusion

The VHSIC program is a large and important undertaking by DoD which will lead to vastly improved avionics systems for the Air Force. This study presented a LCC model which was used to examine some of the factors impacting LCCs of an avionics system implemented with VHSIC Phase 1 technology. Only the future can validate the conclusions reached here.

Appendix A: Description of Input Data for LCC Model

This appendix contains a complete description of every parametric input variable used in the PRICE M, PRICE H, and PRICE L models. In addition, the derivation of every variable not discussed in Chapter V is provided here.

The definition of each part of Table XXXVII used here to describe default input variables is as follows:

1. Variable Name. The names appearing in this column are symbolic variables which were described in Chapter IV. Generally, these variable names are the same as ones presented in the PRICE M, PRICE H, and PRICE L User's Manuals. However, in some instances where duplications occur between models, alpha numeric prefixes or suffixes are added for clarity. For example, the input variable, production quantity (QTY), is used as a symbolic variable in the PRICE M and PRICE H models. To distinguish their differences, QTY1 represents the PRICE M input variable for production quantity of VHSIC chips, QTY2 is the PRICE H, mode 4 quantity of GFE purchased items, and QTY3 represents the PRICE H, mode 5 I&T quantity.

2. Value. Entries in this column are input values for each of the four default cases described in Chapter III.

3. ij. When a variable refers to chip-related factors, then the value for ij refers to chip type and design i and technology type j. For instance, $ASMYLD_{11}$ refers to a custom designed signal processor chip using Bipolar 3D/STL technology. Table XXXVI provides a description for each of the remaining ij factors.

4. Case. Entries in this column indicate the default cases for which the variables in column one are applicable. For example, 1,3 means that the variable in column one is input for default cases 1 and 3.

5. Model/File Name or Mode. Entries in this column show the LCC models and their associated input files or modes for which the input variable is used as input. For instance, "M" represents

PRICE M; "H/1, 3, 4, 5, or 7" refers to PRICE H, mode 1, mode 3, mode 4, mode 5, or mode 7; and "L/Hardware, Global or Deployment" indicates PRICE L, Hardware file, Global file, or Deployment file.

TABLE XXXVI

Description of ij Factors

i	j	Factor Description
1		Signal Processor, Custom Design
2		Control Processor, Custom Design
3		Signal Processor, Gate Array Design
4		Control Processor, Gate Array Design
5		Memory, Custom Design
	1	BIPOLAR 3D/STL Technology
	2	BIPOLAR ISL/CML Technology
	3	CMOS/Bulk Technology
	4	CMOS/SOS Technology
	5	NMOS Technology

6. Source. This column provides bibliography citations, text references, or description of the source for each variable given in column two.

TABLE XXXVII

Default Values for All Input Variables

Variable Name	Value	ij	Case	Model/ File or Mode	Source
AFSA=AF Supply Administration Control	1	00	All	L/Global	29:7.18, 9.6
AUC1=Purchased Unit Cost	$ 2,047.60	11	1,3	H/3	PRICE M Output
AUC1	$ 650.64	31	2,4	H/3	PRICE M Output
AUC1	$ 981.20	23	1,4	H/3	PRICE M Output
AUC1	$ 542.15	43	2,3	H/3	PRICE M Output
AUC1	$ 282.15	53	All	H/3	PRICE M Output
ASMYLD = Assembly Yield	.0431	11	1,3	M	Tbl. XVI, Eq. 3
ASMYLD	.0196	12	N/A	M	Tbl. XVI, Eq. 3
ASMYLD	.0266	13	N/A	M	Tbl. XVI, Eq. 3
ASMYLD	.0162	14	N/A	M	Tbl. XVI, Eq. 3
ASMYLD	.0231	15	N/A	M	Tbl. XVI, Eq. 3
ASMYLD	.0440	21	N/A	M	Tbl. XVII Eq. 3
ASMYLD	.0199	22	N/A	M	Tbl. XVII Eq. 3

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ASMYLD	.0230	23	1.4	M	Tbl. XVII Eq. 3
ASMYLD	.0167	24	N/A	M	Tbl.XVII, Eq. 3
ASMYLD	.0235	25	N/A	M	Tbl.XVII, Eq. 3
ASMYLD	.0233	33	N/A	M	Tbl.XIX, Eq. 3
ASMYLD	.0271	31	2,4	M	Tbl.XIX, Eq. 3
ASMYLD	.0238	43	2,3	M	Tbl.XVIII, Eq. 3
ASMYLD	.0276	41	N/A	M	Tbl.XVIII, Eq. 3
ASMYLD	.0367	53	All	M	Tbl. XX, Eq. 3
ASMYLD	.0456	55	N/A	M	Tbl. XX, Eq. 3
AUCOST = Average Unit Cost	$ 7,686,000	00	All	H/7	PRICE H, Mode 5 Output
CAD = Annual Cost to Maintain	$150.00	00	All	L/Global	Tbl. XXIX
CADFAC = CAD Factor	.8	11	1,3	M	Tbl. XXI, 8:1029
CADFAC	.8	12	N/A	M	Tbl. XXI, 8:1029

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CADFAC	.8	13	N/A	M	Tbl. XXI, 8:1029
CADFAC	.8	14	N/A	M	Tbl. XXI, 8:1029
CADFAC	.8	15	N/A	M	Tbl. XXI, 8:1029
CADFAC	.8	21	N/A	M	Tbl. XXI, 8:1029
CADFAC	.8	22	N/A	M	Tbl XXI, 8:1029
CADFAC	.8	23	1,4	M	Tbl. XXI, 8:1029
CADFAC	.8	24	N/A	M	Tbl. XXI, 8:1029
CADFAC	.8	25	N/A	M	Tbl. XXI, 8:1029
CADFAC	1.2	33	N/A	M	Tbl. XXII, 8:1029
CADFAC	1.2	31	2,4	M	Tbl. XXII, 8:1029
CADFAC	1.2	43	2,3	M	Tbl. XXII, 8:1029
CADFAC	1.2	41	N/A	M	Tbl. XXII, 8:1029
CADFAC	1.0	53	All	M	Tbl. XXI, 8:1029
CADFAC	1.0	55	N/A	M	Tbl. XXI 8:1029

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CCOU = Cost of LRU Checkout Test Set	$ 4,970,700	00	All	L/Hardware	PRICE H Mode 1, Output
CDDI = Cost to Ship from Depot to Intermediate	0	N/A	All	L/Global	Tbl.XXIX
CDFD = Cost to Ship from Factory to Depot. Dollars/ Pound/Trip	$3.13 (CONUS) $6.00 (Europe) $6.00 (Asia)	N/A	All	L/Global	Tbl. XXIX
CDID = Cost to Ship from Intermediate to Depot. Dollars/ Pound/Trip	$3.13 (CONUS) $6.00 (Europe) $6.00 (Asia)	N/A	All	L/Global	Tbl. XXIX
CDIO = Cost to Ship from Intermediate to Organization. Dollars/Pound/Trip	$3.13 (CONUS) $6.00 (Europe) $6.00 (Asia)	N/A	All	L/Global	Tbl. XXIX
CDOI = Cost to Ship from Organization to Intermediate. Dollars/Pound/Trip	0	N/A	All	L/Global	29:7.12
CEN = Cost to Enter an Item into the Supply System.	$ 1,200	N/A	All	L/Global	Tbl. XXIX
CEND = Cost of Engineering Development	$425,116,000	N/A	1	L/Hardware	PRICE M Output

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CEND	$ 76,675,000	N/A	2	L/Hardware	PRICE M Output
CEND	$251,752,000	N/A	3	L/Hardware	PRICE M Output
CEND	$250,066,000	N/A	4	L/Hardware	PRICE M Output
CFIM = Cost of LRU Test Set	$ 1,244,268	N/A	All	L/Hardware	PRICE H, Mode 1 Output
CFIP = Cost of Module Test Set	$ 3,803,676	N/A	All	L/Hardware	PRICE H, Mode 1 Output
CMP = Average Cost of Module in Production	$ 113,000	N/A	All	L/Hardware	PRICE H, Mode 1 Output
CMR = Contractor Cost for Module Repair	$ 5,068.03	N/A	1	L/Hardware	PRICE H, Mode 1 Output
CPE = Nonrecurring Production Costs	$ 4,374,000	N/A	1	L/Hardware	PRICE H, Mode 5 Output
CPE	$ 152,000	N/A	2	L/Hardware	PRICE H, Mode 5 Output
CPE	$ 4,378,000	N/A	3	L/Hardware	PRICE H Mode 5 Output

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CPE	$ 4,373,000	N/A	4	L/Hardware	PRICE H Mode 5 Output
CPF = Cost-Process Factor	.89	N/A	All	H/1	28.67
CPP = Average Cost of a Part in Production	$282.15	N/A	All	L/Hardware	PRICE H, Mode 1 Output
CPPE = Equipment Repair Part Cost	$282.15	N/A	All	L/Hardware	PRICE H, Mode 1 Output
CPYLD = Wafer Test and Probe Yield	.0587	11	1,3	M	Tbl. XVI, Eq. 2
CPYLD	.0723	12	N/A	M	Tbl. XVI, Eq. 2
CPYLD	.0839	13	N/A	M	Tbl. XVI, Eq. 2
CPYLD	.0220	14	N/A	M	Tbl. XVI, Eq, 1
CPYLD	.0858	15	N/A	M	Tbl. XVI, Eq. 2
CPYLD	.0598	21	N/A	M	Tbl. XVII, Eq. 2
CPYLD	.0737	22	N/A	M	Tbl. XVII, Eq. 2
CPYLD	.0856	23	1,4	M	Tbl. XVII, Eq. 2

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CPYLD	.0225	24	N/A	M	Tbl. XVII, Eq. 1
CPYLD	.0875	25	N/A	M	Tbl. XVII, Eq. 2
CPYLD	.0868	33	N/A	M	Tbl. XIX, Eq. 2
CPYLD	.1015	31	2,4	M	Tbl. XIX, Eq. 2
CPYLD	.0885	43	2,3	M	Tbl.XVIII, Eq. 2
CPYLD	.1035	41	N/A	M	Tbl.XVIII, Eq. 2
CPYLD	.1398	53	All	M	Tbl. XX, Eq. 2
CPYLD	.1764	54	N/A	M	Tbl. XX, Eq. 2
CUBEM = Module Storage Volume	.0052	N/A	All	L/Hardware	Tbl. XXVII
CUBEP = Part Storage Volume	.0002	N/A	All	L/Hardware	Tbl.XXVIII
CUBEU = LRU Storage Volume	1.94 ft^3	N/A	All	L/Hardware	Tbl. XXVI
CUD = Cost per Man-hour at Depot	$41.00	N/A	All	L/Global	Tbl. XXIX

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CUE = Cost per Man-hour at Equipment	$29.00	N/A	All	L/Global	Tbl.XXIX
CUO = Cost per Man-hour at Organization	$29.00	N/A	All	L/Global	Tbl.XXIX
CUP = Cost of an LRU in Production	$7,686,000	N/A	1	L/Hardware	PRICE H, Mode 5 Output
CUP	$7,687,000	N/A	2,3	L/Hardware	PRICE H, Mode 5 Output
CUP	$7,685,000	N/A	4	L/Hardware	PRICE H, Mode 5 Output
CUR = Contractor Cost for LRU Repair	$133,940.78	N/A	All	L/Hardware	PRICE H, Mode 5 Output
DCOL = Average Cost Per Line of Operational Software	$25.00	N/A	All	Software	5:99
DCOP = Cost of Purchased Software	$10,000	N/A	All	Software	5:109
DCSL = Average Cost Per Line of Support Software	$25.00	N/A	All	Software	5:99, 109

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DCSP = Total Cost of Purchased Support Software	$10,000	N/A	All	Software	5:99
DD = Number of Depot Maintenance Locations	1	N/A	All	L/Deployment	Assumed
DDS = Number of Depot Level Supply Locations	1	N/A	All	L/Deployment	Assumed
DESRPT = Design Repeat	.15	11	1,3	M	30:7.3
DESRPT	.15	12	N/A	M	30:7.3
DESRPT	.15	13	N/A	M	30:7.3
DESRPT	.15	14	N/A	M	30:7.3
DESRPT	.15	15	N/A	M	30:7.3
DESRPT	.15	21	N/A	M	30:7.3
DESRPT	.15	22	N/A	M	30:7.3
DESRPT	.15	23	1,4	M	30:7.3
DESRPT	.15	24	N/A	M	30:7.3
DESRPT	.15	25	N/A	M	30:7.3
DESRPT	.50	33	N/A	M	30:7.3

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DESRPT	.50	31	2,4	M	30:7.3
DESRPT	.50	43	2,3	M	30:7.3
DESRPT	.50	41	N/A	M	30:7.3
DESRPT	.85	53	All	M	30:7.3
DESRPT	.85	55	N/A	M	30:7.3
DFPRO = Data First Prototype Complete	187 (Jan 1987)	N/A	All	H/1	PRICE M
DI = Number of Intermediate Maintenance Locations	0	N/A	All	L/Deployment	Assumed
DINDEX = Design Index	8.5	11	1,3	M	30:2.9
DINDEX	8.5	12	N/A	M	30:2.9
DINDEX	8.5	13	N/A	M	30:2.9
DINDEX	8.5	14	N/A	M	30:2.9
DINDEX	8.5	15	N/A	M	30:2.9
DINDEX	8.5	21	N/A	M	30:2.9
DINDEX	8.5	22	N/A	M	30:2.9

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DINDEX	8.5	23	1,4	M	30:2.9
DINDEX	8.5	24	N/A	M	30:2.9
DINDEX	8.5	25	N/A	M	30:2.9
DINDEX	6.0	33	N/A	M	30:2.9
DINDEX	6.0	31	2,4	M	30:2.9
DINDEX	6.0	43	2,3	M	30:2.9
DINDEX	6.0	41	N/A	M	30:2.9
DINDEX	8.0	53	All	M	30:2.9
DINDEX	8.0	55	N/A	M	30:2.9
DIS = Number of Intermediate Level Supply Locations	0	N/A	All	L/Deployment	Assumed
DLPRO = Development Complete	687 (June 1987)	N/A	All	H/Mode 1	PRICE M Output
DMULT = Development Cost Multiplier	43,804.45	N/A	1,3	H/Mode 3	PRICE M Output
DMULT	1,332.534	N/A	2,4	H/Mode 3	PRICE M Output

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DNOW = Lines of Operational Code	200,000	N/A	All	Software	5:99, 111
DNSW = Lines of Support Software Written for the Prototype System	275,000	N/A	All	Software	5:99, 111
DOSDR = Days of Supply at Depot	10	N/A	All	L/Global	Tbl.XXIX
DOSIC = Days of Supply at Intermediate (Consumables)	0	N/A	All	L/Global	Tbl.XXIX
DOSIR = Days of Supply at Intermeidate (Repairables)	10 (CONUS) 15 (Europe) 15 (Asia)	N/A	All	L/Global	Tbl. XXIX
DOSOC = Days of Supply at Organization (Consumables)	0	N/A	All	L/Global	Assumed
DOSOR = Days of Supply at Organization (Repairables)	0	N/A	All	L/Global	Assumed

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DPLTFM = Design Platform	1.8	00	All	M	30:2.9
DSTART = Development Start	183 (Jan 1983)	N/A	All	H/1	Assumed
DSTRT = Development Start	183 (Jan 1983)	N/A	All	M	Assumed
ECMPLX = Engineering Complexity	2.3	N/A	All	H/1	28:6.6
ECMPLX = Engineering Complexity	3.0	11	1,3	M	30:7.4
ECMPLX	3.0	12	N/A	M	30:7.4
ECMPLX	3.0	13	N/A	M	30:7.4
ECMPLX	3.0	14	N/A	M	30:7.4
ECMPLX	3.0	15	N/A	M	30:7.4
ECMPLX	3.0	21	N/A	M	30:7.4
ECMPLX	3.0	22	N/A	M	30:7.4
ECMPLX	3.0	23	1,4	M	30:7.4
ECMPLX	3.0	24	N/A	M	30:7.4
ECMPLX	3.0	25	N/A	M	30:7.4
ECMPLX	1.9	33	N/A	M	30:7.4
ECMPLX	1.9	31	2,4	M	30:7.4
ECMPLX	1.9	43	2,3	M	30:7.4

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ECMPLX	1.9	41	N/A	M	30:7.4
ECMPLX	2.5	53	All	M	30:7.4
ECMPLX	2.5	55	N/A	M	30:7.4
ED = Number of Equipment Locations	690 (CONUS) 170 (Europe) 140 (Asia)	N/A	All	L/Deployment	Assumed
EDS = Number of Equipment Level Supply Locations	0	N/A	All	L/Deployment	Assumed
EE = LRUs per Equipment Location	1	N/A	All	L/Hardware	PRICE H, Mode 5 Output
EMP = Improvement Curve for Modules	.945	N/A	All	L/Hardware	PRICE H, Mode 1 Output
EPP = Improvement Curve for Parts	.972	N/A	All	L/Hardware	PRICE H, Mode 1 Output
ESC = Escalation	0	N/A	All	M H/3	30:2.5, 28:4.49
EUP = Improvement Curve for LRUs	.89	N/A	All	L/Hardware	PRICE H, Mode 1 Output
FMD = Fraction of Modules Repaired at Depot	.05	N/A	All	L/Global	Assumed

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
FMI = Fraction of Modules Repaired at Intermediate	0	N/A	all	L/Global	Assumed
FMO = Fraction of Modules Repaired at Organization	.95	N/A	All	L/Global	Assumed
FNSP = Fraction of Nonstandard Parts	.5	N/A	All	L/Hardware	PRICE H, Mode 1 Output
FTSQC = Floor Space LRU Checkout Set	4.02 ft^2	N/A	All	L/Hardware	PRICE H, Mode 1, Output
FTSQF = Floor Space LRU Test Set	10.06 ft^2	N/A	All	L/Hardware	PRICE H, Mode 1 Output
FTSQP = Floor Space for Module Test Set	30.74	N/A	All	L/Hardware	PRICE H, Mode 1 Output
FUE = Fraction of Units Repaired at Equipment	.95	N/A	All	L/Global	Assumed
FUI = Fraction of Units Repaired at Intermediate	0	N/A	All	L/Global	Assumed

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
FUO = Fraction of Units Repaired at Organization	0	N/A	All	L/Global	Assumed
GATES = Number of Gates per Chip	25,500	11	1,3	M	Tbl. IX
GATES	25,500	12	N/A	M	Tbl. IX
GATES	25,500	13	N/A	M	Tbl. IX
GATES	25,500	14	N/A	M	Tbl. IX
GATES	25,500	15	N/A	M	Tbl. IX
GATES	25,000	21	N/A	M	Tbl. XI
GATES	25,000	22	N/A	M	Tbl. XI
GATES	25,000	23	1,4	M	Tbl. XI
GATES	25,000	24	N/A	M	Tbl. XI
GATES	25,000	25	N/A	M	Tbl. XI
GATES	10,200	33	N/A	M	Tbl. X
GATES	10,200	31	2,4	M	Tbl. X
GATES	10,000	43	2,3	M	Tbl. XII
GATES	10,000	41	N/A	M	Tbl. XII
INTEGE = Next Higher Assembly Integration Factor for Electronics	.5	11	All	H/3,5	28:4.46, 8.4
INTEGE	.5	12	All	H/3,5	28.4.46,8.4
INTEGE	.5	13	All	H/3,5	28:4.46,8.4

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
INTEGE	.5	14	All	H/3,5	28:4.46,8.4
INTEGE	.5	15	All	H/3,5	28:4.46,8.4
INTEGE	.5	21	All	H/3,5	28:4.46,8.4
INTEGE	.5	22	All	H/3,5	28:4.46, 8.4
INTEGE	.5	23	All	H/3,5	28:4.46, 8.4
INTEGE	.5	24	All	H/3,5	28:4.46, 8.4
INTEGE	.5	25	All	H/3,5	28:4.46, 8.4
INTEGE	.5	33	All	H/3,5	28:4.46, 8.4
INTEGE	.5	31	All	H/3,5	28:4.46, 8.4
INTEGE	.5	43	All	H/3,5	28:4.46, 8.4
INTEGE	.5	44	All	H/3,5	28:4.46, 8.4
INTEGE	.4	53	All	H/3,5	28:4.46, 8.4
INTEGE	.4	55	All	H/3,5	28:4.46, 8.4
INTEGS = Next Higher Integration Factor for Structural Items	0	N/A	All	H/3,1	28:4.46, 8.4

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
INTEGS	.5	N/A	All	H/4,5	28:4.46, 4.51, 9.3
ITERAT = Design and Prototype Iterations	2	11	1,3	M	8:1029, 30:4.17
ITERAT	2	12	N/A	M	8:1029, 30:4.17
ITERAT	2	13	N/A	M	8:1029, 30:4.17
ITERAT	2	14	N/A	M	8:1029, 30:4.17
ITERAT	2	15	N/A	M	8:1029, 30:4.17
ITERAT	2	21	N/A	M	8:1029, 30:4.17
ITERAT	2	22	N/A	M	8:1029, 30:4.17
ITERAT	2	23	1,4	M	8:1029, 30:4.17
ITERAT	2	24	N/A	M	8:1029, 30:4.17
ITERAT	2	25	N/A	M	8:1029, 30:4.17
ITERAT	0	33	N/A	M	8:1029, 30:4.17
ITERAT	0	31	2,4	M	8:1029, 30:4.17

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ITERAT	0	43	2,3	M	8:1029, 30:4.17
ITERAT	0	41	N/A	M	8:1029, 30:4.17
ITERAT	1	53	All	M	8:1029, 30:4.17
ITERAT	1	55	N/A	M	8:1029, 30:4.17
LENGTH = Length Dimension of Chips in Mils	345.31	11	1,3	M	Tbl.IX
LENGTH	311.24	12	N/A	M	Tbl.IX
LENGTH	188.83	13	N/A	M	Tbl.IX
LENGTH	340.93	14	N/A	M	Tbl.IX
LENGTH	285.63	15	N/A	M	Tbl.IX
LENGTH	341.90	21	N/A	M	Tbl.XI
LENGTH	308.17	22	N/A	M	Tbl.XI
LENGTH	285.99	23	1,4	M	Tbl.XI
LENGTH	337.57	24	N/A	M	Tbl.XI
LENGTH	282.82	25	N/A	M	Tbl.XI
LENGTH	283.98	33	N/A	M	Tbl.X
LENGTH	262.61	31	2,4	M	Tbl.X
LENGTH	281.18	43	2,3	M	Tbl.XII
LENGTH	260.02	41	N/A	M	Tbl.XII

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
LENGTH	223.75	53	All	M	Tbl.XIV
LENGTH	199.18	55	N/A	M	Tbl.XIV
MCPLXE = Manufacturing Complexity of Electronics Items	9.053	00	All	H/3	39, 28:4.47, 8.4
MCPLXE	0	N/A	All	H/4	28:4.47, 9.4
MCPLXE	11.730	N/A	All	H/1	PRICE H, Mode 7 Output
MCPLXS = Manufacturing Complexity of Structural Items	0	N/A	All	H/3	28:4.47, 8.4
MCPLXS	5.3	N/A	All	H/4	28:4.47, 9.4
MCPLXS	8.217	N/A	All	H/1	PRICE H, Mode 7 Output
MINDEX = Manufacturing Index	14	11	1,3	M	30:2.14, 39
MINDEX	14	12	N/A	M	30:2.14, 39
MINDEX	14	13	N/A	M	30:2.14, 39
MINDEX	14	14	N/A	M	30:2.14, 39

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
MINDEX	14	15	N/A	M	30:2.14, 39
MINDEX	14	21	N/A	M	30:2.14, 39
MINDEX	14	22	N/A	M	30:2.14, 39
MINDEX	14	23	1,4	M	30:2.14, 39
MINDEX	14	24	N/A	M	30:2.14, 39
MINDEX	14	25	N/A	M	30:2.14, 39
MINDEX	7	33	N/A	M	30:2.14, 39
MINDEX	7	31	2,4	M	30:2.14, 39
MINDEX	7	43	2,3	M	30:2.14, 39
MINDEX	7	41	N/A	M	30:2.14, 39
MINDEX	13	53	All	M	30:2.14, 39
MINDEX	13	55	N/A	M	30:2.14, 39
MSKLVL = Mask Levels	5	11	1,3	M	Tbl.XVI
MSKLVL	7	12	N/A	M	Tbl.XVI

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
MSKLVL	5	13	N/A	M	Tbl.XVI
MSKLVL	3	14	N/A	M	Tbl.XVI
MSKLVL	5	15	N/A	M	Tbl.XVI
MSKLVL	5	21	N/A	M	Tbl.XVII
MSKLVL	7	22	N/A	M	Tbl.XVII
MSKLVL	5	23	1,4	M	Tbl.XVII
MSKLVL	3	24	N/A	M	Tbl.XVII
MSKLVL	5	25	N/A	M	Tbl.XVII
MSKLVL	5	33	N/A	M	Tbl.XIX
MSKLVL	7	31	2,4	M	Tbl.XIX
MSKLVL	5	43	2,3	M	Tbl.XVIII
MSKLVL	7	41	N/A	M	Tbl.XVIII
MSKLVL	5	53	All	M	Tbl.XX
MSKLVL	5	55	N/A	M	Tbl.XX
MTBF = Mean Time Between Failure (Hours)	510	00	1	L/Hardware	Tbl.XXIII
MTBF	530	00	2	L/Hardware	Tbl.XXIII
MTBF	528	00	3	L/Hardware	Tbl.XXIII
MTBF	526	00	4	L/Hardware	Tbl.XXIII
NEWCEL = New Cell	.85	11	1,3	M	Tbl.XXI

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
NEWCEL	.85	11	1,3	M	Tbl.XXI
NEWCEL	.85	12	N/A	M	Tbl.XXI
NEWCEL	.85	13	N/A	M	Tbl.XXI
NEWCEL	.85	14	N/A	M	Tbl.XXI
NEWCEL	.85	15	N/A	M	Tbl.XXI
NEWCEL	.85	21	N/A	M	Tbl.XXI
NEWCEL	.85	22	N/A	M	Tbl.XXI
NEWCEL	.85	23	1,4	M	Tbl.XXI
NEWCEL	.85	24	N/A	M	Tbl.XXI
NEWCEL	.85	25	N/A	M	Tbl.XXI
NEWCEL	.05	33	N/A	M	Tbl.XXII
NEWCEL	.05	31	2,4	M	Tbl.XXII
NEWCEL	.05	43	2,3	M	Tbl.XXII
NEWCEL	.05	41	N/A	M	Tbl.XXII
NEWCEL	.50	53	All	M	Tbl.XXI
NEWCEL	.50	55	N/A	M	Tbl.XXI
NEWEL = New Electronics	.3	N/A	All	H/5	28:4.51, 10.1
NEWEL	.5	N/A	All	H/1	28:6.6
NEWST = New Structure	.3	N/A	All	H/5	28:4.51, 10.1

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
NEWST	.1	N/A	All	H/1	28:6.5
OD = Number of Organization Level Maintenance Locations	5 (CONUS) 3 (Europe) 2 (Asia)	N/A	All	L/Deployment	Assumed
ODS = Number of Organization Level Supply Locations	5 (CONUS 3 (Europe) 2 (Asia)	N/A	All	L/Deployment	Assumed
OTF = On-time Fraction (Hours/ Month)	46 (CONUS) 46 (Europe) 46 (Asia)	N/A	All	L/Deployment	Assumed
OVLYLD = Overall Fabrication Yields	2.53×10^{-3}	11	1,3	M	Tbl.XVI Eq. 19
OVLYLD	1.42×10^{-3}	12	N/A	M	Tbl.XVI Eq. 19
OVLYLD	1.9×10^{-3}	13	N/A	M	Tbl.XVI Eq. 19
OVLYLD	3.6×10^{-3}	14	N/A	M	Tbl.XVI Eq. 19
OVLYLD	1.98×10^{-3}	15	N/A	M	Tbl.XVI Eq. 19
OVLYLD	2.63×10^{-3}	21	N/A	M	Tbl.XVII Eq. 19
OVLYLD	1.47×10^{-3}	22	N/A	M	Tbl.XVII Eq. 19

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
OVLYLD	1.97×10^{-3}	23	1,4	M	Tbl.XVII Eq. 19
OVLYLD	3.76×10^{-4}	24	N/A	M	Tbl.XVII Eq. 19
OVLYLD	2.06×10^{-3}	25	N/A	M	Tbl.XVII Eq. 19
OVLYLD	2.03×10^{-3}	33	N/A	M	Tbl.XIX Eq. 19
OVLYLD	2.75×10^{-3}	31	2,4	M	Tbl.XIX Eq. 19
OVLYLD	2.10×10^{-3}	43	2,3	M	Tbl.XVIII Eq. 19
OVLYLD	2.85×10^{-3}	41	N/A	M	Tbl.XVIII Eq. 19
OVLYLD	5.13×10^{-3}	53	All	M	Tbl. XX Eq. 19
OVLYLD	8.04×10^{-3}	55	N/A	M	Tbl. XX Eq. 19
P = Number of Module Types	68	N/A	All	L/Hardware	Tbl.XXIII
PEND = Production Complete	994 (Sept 1994)	N/A	All	H/1.7	PRICE M Output
PFAD = First Article Delivery	188 (Jan 1988)	N/A	All	H/1,7	PRICE M Output
PINS = Number of Pins	180	11	1,3	M	Tbl.IX

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PINS	180	12	N/A	M	Tbl.IX
PINS	180	13	N/A	M	Tbl.IX
PINS	180	14	N/A	M	Tbl.IX
PINS	180	15	N/A	M	Tbl.IX
PINS	180	21	N/A	M	Tbl.XI
PINS	180	22	N/A	M	Tbl.XI
PINS	180	23	1,4	M	Tbl.XI
PINS	180	24	N/A	M	Tbl.XI
PINS	180	25	N/A	M	Tbl.XI
PINS	148	33	N/A	M	Tbl.X
PINS	148	31	2,4	M	Tbl.X
PINS	148	43	2,3	M	Tbl.XII
PINS	148	41	N/A	M	Tbl.XII
PINS	42	53	All	M	Tbl.XIII
PINS	32	55	N/A	M	Tbl.XIII
PKGFAC = Packaging Factor	2.4	11	1,3	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	12	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	13	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	14	N/A	M	Tbl.XXVIII 30:2.15

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PKGFAC	2.4	15	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	21	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	22	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	23	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	24	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	25	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	1.7	33	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	1.7	31	2,4	M	Tbl.XXVIII 30:2.15
PKGFAC	1.7	43	2,3	M	Tbl.XXVIII 30:2.15
PKGFAC	1.7	41	N/A	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	53	All	M	Tbl.XXVIII 30:2.15
PKGFAC	2.4	55	N/A	M	Tbl.XXVIII 30:2.15
PLTFM = Specification Level	1.8	All	All	H/1,3,4,5	28:4.46, 8.4, 4.52

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PMULT = Production Multiplier	0	All	All	H/3	28:4.49, 8.5
PP = Number of Part Types	3	N/A	All	L/Hardware	PRICE H, Mode 1, Output
PROFAC = Production Factor	8	00	All	M	30:2.13
PROTOS1 = Chip Prototype Quantity	2	11	1,3	M, H/3	Tbl.XIV
PROTOS1	2	12	N/A	M, H/3	Tbl.XIV
PROTOS1	2	13	N/A	M, H/3	Tbl.XIV
PROTOS1	2	14	N/A	M, H/3	Tbl.XIV
PROTOS1	2	15	N/A	M, H/3	Tbl.XIV
PROTOS1	4	21	N/A	M, H/3	Tbl.XIV
PROTOS1	4	22	N/A	M, H/3	Tbl.XIV
PROTOS1	4	23	1,4	M, H/3	Tbl.XIV
PROTOS1	4	24	N/A	M, H/3	Tbl.XIV
PROTOS1	4	25	N/A	M, H/3	Tbl.XIV
PROTOS1	5	33	N/A	M, H/3	Tbl.XIV
PROTOS1	5	31	2,4	M, H/3	Tbl.XIV
PROTOS1	10	43	2,3	M, H/3	Tbl.XIV
PROTOS1	10	41	N/A	M, H/#	Tbl.XIV

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PROTOS1	27,070	53	All	M, H/3	Tbl.XIII, Tbl.XXIV
PROTOS1	27,070	55	N/A	M, H/3	Tbl.XIII, Tbl.XXIV
PROTOS2 = Number of GFE Equipment Items	68 (Circuit Boards)	00	All	H/4	Tbl.XXIII
PROTOS2	1 (Chassis)	N/A	All	H/4	Tbl.XXVI
PROTOS3 = Number of Prototype LRUs Requiring I&T	1 (SAR)	N/A	All	H/5	Tbl.XXVI
PSTART = Production Start	787 (July 1987)	N/A	All	H/1	PRICE M Output
PSTRT = Production Start (Chip Fabrication)	687 (June 1987)	11	1,3	M	Assumed
PSTRT	687	12	N/A	M	Assumed
PSTRT	687	13	N/A	M	Assumed
PSTRT	687	14	N/A	M	Assumed
PSTRT	687	15	N/A	M	Assumed
PSTRT	587 (May 1987)	21	N/A	M	Assumed
PSTRT	587	22	N/A	M	Assumed
PSTRT	587	23	1,4	M	Assumed

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PSTRT	587	24	N/A	M	Assumed
PSTRT	587	25	N/A	M	Assumed
PSTRT	983 (Sept 1983)	33	N/A	M	Assumed
PSTRT	983	31	2,4	M	Assumed
PSTRT	184 (Jan 1984)	43	2,3	M	Assumed
PSTRT	184	41	N/A	M	Assumed
PSTRT	584 (May 1984)	53	All	M	Assumed
PSTRT	584	55	N/A	M	Assumed
PTSTRT = Prototype Start (Chip Development)	1086 (Oct 1986)	11	1,3	M	Assumed
PTSTRT	1086	12	N/A	M	Assumed
PTSTRT	1086	13	N/A	M	Assumed
PTSTRT	1086	14	N/A	M	Assumed
PTSTRT	1086	15	N/A	M	Assumed
PTSTRT	986 (Sept 1986)	21	N/A	M	Assumed
PTSTRT	986	22	N/A	M	Assumed
PTSTRT	986	23	N/A	M	Assumed
PTSTRT	986	24	N/A	M	Assumed
PTSTRT	986	25	N/A	M	Assumed

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
PTSTRT	383 (March 1983)	33	N/A	M	Assumed
PTSTRT	383	31	2,4	M	Assumed
PTSTRT	383	43	2,3	M	Assumed
PTSTRT	383	41	N/A	M	Assumed
PTSTRT	183 (Jan 1983)	53	All	M	Assumed
PTSTRT	183	55	N/A	M	Assumed
QTY1 = Production Quantity (Chips)	2000	11	1,3	M, H/3	Tbl.IX, Tbl.XV
QTY1	2000	12	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	2000	13	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	2000	14	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	2000	15	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	4000	21	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	4000	22	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	4000	23	1,4	M, H/3	Tbl.IX, Tbl.XV
QTY1	4000	24	N/A	M, H/3	Tbl.IX, Tbl.XV

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
QTY1	4000	25	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	5000	33	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	5000	31	2,4	M, H/3	Tbl.IX, Tbl.XV
QTY1	10,000	43	2,3	M, H/3	Tbl.IX, Tbl.XV
QTY1	10,000	41	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY1	27,070,000	53	All	M, H/3	Tbl.IX, Tbl.XV
QTY1	27,070,000	55	N/A	M, H/3	Tbl.IX, Tbl.XV
QTY2 = Quantity of GFE Items	68,000 (Circuit Boards)	N/A	All	H/4	Tbl.XXVII, Tbl.IX
QTY3 = I&T Quantity	1,000 (SAR Units)	N/A	All	H/5	Tbl.XXVI
QTYNHA = Quantity Next Higher Assembly	2	11	1,3	H/3	Tbl.XIV
QTYNHA	5	31	2,4	H/3	Tbl.XIV
QTYNHA	4	23	1,4	H/3	Tbl.XIV
QTYNHA	10	43	2,3	H/3	TBL.XIV

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
QTYNHA	270 (PCB 1) 400 (PCB 2-68)	53	All	H/3	Tbl.XIV
QTYNHA	1 (Circuit Cards)	N/A	All	H/4	Tbl.XXVII
QTYNHA	1 (Chassis)	N/A	All	H/4	Tbl.XXVI
QTYNHA	1 (PCB 1)	N/A	All	H/5	Tbl.XIV
QTYNHA	67 (PCB 2-68)	N/A	All	H/5	Tbl.XIV
QTYNHA	1 (SAR I&T)	N/A	All	H/5	Tbl.XIV
RNM = Reference Quantity for Modules	1000	N/A	All	L/Hardware	PRICE H, Mode 1 Output
RNP = Reference Quantity for Parts	1000	N/A	All	L/Hardware	PRICE H, Mode 1 Output
RNU = Reference Quantity for LRUs	1000	N/A	All	L/Hardware	PRICE H, Mode 1 Output
SPLTFM = System Platform	1.8	00	All	M	30:2.9
SUBFAC = Substrate Factor	4.0	11	1,3	M	30:2.14

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
SUBFAC	4.0	12	N/A	M	30:2.14
SUBFAC	1.5	13	N/A	M	30:2.14
SUBFAC	2.5	14	N/A	M	30:2.14
SUBFAC	3.0	15	N/A	M	30:2.14
SUBFAC	4.0	21	N/A	M	30:2.14
SUBFAC	4.0	22	N/A	M	30:2.14
SUBFAC	1.5	23	1,4	M	30:2.14
SUBFAC	2.5	24	N/A	M	30:2.14
SUBFAC	4.0	25	N/A	M	30:2.14
SUBFAC	4.0	33	N/A	M	30:2.14
SUBFAC	1.5	31	2.4	M	30:2.14
SUBFAC	4.0	43	2,3	M	30:2.14
SUBFAC	1.5	41	N/A	M	30:2.14
SUBFAC	1.5	53	All	M	30:2.14
SUBFAC	3.0	55	N/A	M	30:2.14
TC = LRU Checkout Time at Organization	1.76	N/A	All	L/Hardware	PRICE H, Mode 1 Output
TF = LRU MTTR	1.76	N/A	All	L/Hardware	PRICE H, Mode 1 Output

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
TMO = Module MTTR	3.56	N/A	All	L/Hardware	PRICE H, Mode 1 Output
VOL = Volume	2.1×10^{-4}	N/A	1,3	H/3	Tbl.XXVIII
VOL	8×10^{-6}	N/A	2,4	H/3	Tbl.XXVIII
VOL	.0052	N/A	All	H/4	Tbl.XXVII
VOL	1.94	N/A	All	H/1	Tbl.XXVI
WECF = Electronics Weight/Ft^3	119.98	N/A	All	H/1	Tbl.XXVI
WIDTH = Width Dimensions of Chips in Mils	345.31	11	1,3	M	Tbl.IX
WIDTH	311.24	12	N/A	M	Tbl.IX
WIDTH	188.83	13	N/A	M	Tbl.IX
WIDTH	340.93	14	N/A	M	Tbl.IX
WIDTH	285.63	15	N/A	M	Tbl.IX
WIDTH	341.90	21	N/A	M	Tbl.XI
WIDTH	308.17	22	N/A	M	Tbl.XI
WIDTH	285.99	23	1,4	M	Tbl.XI
WIDTH	337.57	24	N/A	M	Tbl.XI
WIDTH	282.82	25	N/A	M	Tbl.XI
WIDTH	283.98	33	N/A	M	Tbl.X

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
WIDTH	262.61	31	2,4	M	Tbl.X
WIDTH	281.18	43	2,3	M	Tbl.XII
WIDTH	260.02	41	N/A	M	Tbl.XII
WIDTH	223.75	53	All	M	Tbl.XIII
WIDTH	199.18	55	N/A	M	Tbl.XIII
WM = Module Weight	2.57	00	All	L/Hardware	PRICE H Mode 1, Output
WP = Part Weight	.0349	00	All	L/Hardware	Tbl.XXVIII
WS - Structure Weight (Lbs)	572 (Circuit Card)	N/A	All	H/4	Tbl.XXVII
WT = Total Weight (Lbs)	241.36	N/A	All	H/1	PRICE H, Mode 3 Output
WT	.0349	11	1,3	H/3	Tbl.XXVIII
WT	.0157	31	2,4	H/3	Tbl.XXVIII
WT	.572 (Circuit Card)	N/A	All	H/4	Tbl.XXVII
WT	.0349	23	1,4	H/3	Tbl.XXVIII
WT	.0157	43	2,3	H/3	Tbl.XXVIII
WT	.005	53	All	H/3	Tbl.XXVIII

TABLE XXXVII

Default Values for All Input Variables (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
WT	66.9	N/A	All	H/4	Tbl.XXVI
XSTRS = Number of Transistors	393,216	53	All	M	Tbl.XIII
XSTRS	393,216	55	N/A	M	Tbl.XIII
YD = Years in Development Phase	4.5	N/A	All	L/Hardware	PRICE H, Mode 1 Output
YP = Years in Production Phase	7.25	N/A	All	L/Hardware	PRICE H, Mode 1
YRECON = Year of Economics	1984	N/A	All	All	Assumed
YRTECH = Year of Technology	1983	N/A	All	All	Assumed

Appendix B: LCC Output Data

This appendix contains five sections of computer output data which are analyzed in Chapter VI. Section 1 gives the output data which are results from the input of all default values presented in Appendix A. Similarily, Sections 2, 3, 4, and 5 give the value changes to default input variables and present output data used for analysis of the impact on LCCs of maintenance level, substrate type, use of CAD, and overall chip fabrication yields respectively. Each run of the LCC model gives the costs for one set of input for one case. Changes to default values for each area of sensitivity analysis are given with output data. Finally, the definition of each part of the table used here to describe changes to default input variables is the same as given in Appendix A.

Output for all chip costs by design and technology are provided first. Next, outputs for each of the four default cases is given. Finally, changes to the default input variables for sensitivity analysis of interest areas and their outputs are provided.

Section 1

Output Data for Default Values

These outputs are results from the input of all default values given in Appendix A for the four basic cases studied. The first output presented are chip costs. Then outputs for each of the four default cases are given beginning with default Case 1 and ending with default Case 4.

TITLE: SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (ij=11)

COSTS

UNIT PRODUCTION COST($ 1.00)		2047.60
PROGRAM COST ($ 1000.)		
ENGINEERING		
CHIP SPECIFICATION	34824.	
CHIP DESIGN	124158.	
SYSTEMS	10025.	
PROJECT MGMT	7238.	
DATA	3116.	
SUBTOTAL ENGINEERING	179360.	
MANUFACTURING		
PROTOTYPE	28.	
PRODUCTION	4095.	
SUBTOTAL MANUFACTURING	4123.	
TOTAL PROGRAM COST	183483.	

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(46)	OCT 86
PROTOTYPE	NOV 86	(4)	FEB 87*
ENG TEST	MAR 87*	(1)	MAR 87*
ITERATIONS	APR 87*	(3)	JUN 87*
		(54)	

	START		END PRE-PROD		FINISH	
PRODUCTION	JUN 87	(3)	AUG 87*	(10)	JUN 88*	(13)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (ij=12)

COSTS

UNIT PRODUCTION COST($ 1.00)		2144.01
PROGRAM COST ($ 1000.)		
ENGINEERING		
CHIP SPECIFICATION	34824.	
CHIP DESIGN	124158.	
SYSTEMS	10025.	
PROJECT MGMT	7238.	
DATA	3116.	
SUBTOTAL ENGINEERING	179360.	

MANUFACTURING

MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	4288.
SUBTOTAL MANUFACTURING	4316.
TOTAL PROGRAM COST	183676.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(46)	OCT 86
PROTOTYPE	NOV 86	(4)	FEB 87*
ENG TEST	MAR 87*	(1)	MAR 87*
ITERATIONS	APR 87*	(3)	JUN 87*
		(54)	

	START		END PRE-PROD		FINISH	
PRODUCTION	JUN 87	(3)	AUG 87*	(11)	JUL 88*	(14)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (ij=13)

COSTS

UNIT PRODUCTION COST($ 1.00)	1082.53

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	34824.
CHIP DESIGN	124158.
SYSTEMS	10025.
PROJECT MGMT	7238.
DATA	3116.
SUBTOTAL ENGINEERING	179360.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	2165.
SUBTOTAL MANUFACTURING	2193.
TOTAL PROGRAM COST	181553.

SCHEDULE						
DEVELOPMENT	START			FINISH		
DESIGN	JAN 83		(46)	OCT 86		
PROTOTYPE	NOV 86		(4)	FEB 87*		
ENG TEST	MAR 87*		(1)	MAR 87*		
ITERATIONS	APR 87*		(3)	JUN 87*		
			(54)			

	START		END PRE-PROD		FINISH	
PRODUCTION	JUN 87	(3)	AUG 87*	(11)	JUL 88*	(14)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (ij=14)

UNIT PRODUCTION COST($ 1.00) 2932.45

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	34824.
CHIP DESIGN	124158.
SYSTEMS	10025.
PROJECT MGMT	7238.
DATA	3116.
SUBTOTAL ENGINEERING	179360.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	5865.
SUBTOTAL MANUFACTURING	5893.
TOTAL PROGRAM COST	185252.

SCHEDULE						
DEVELOPMENT	START			FINISH		
DESIGN	JAN 83		(46)	OCT 86		
PROTOTYPE	NOV 86		(4)	FEB 87*		
ENG TEST	MAR 87*		(1)	MAR 87*		
ITERATIONS	APR 87*		(3)	JUN 87*		
			(54)			

	START		END PRE-PROD		FINISH	
PRODUCTION	JUN 87	(3)	AUG 87*	(12)	AUG 88*	(15)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-NMOS (ij=15)

COSTS

UNIT PRODUCTION COST($ 1.00) 1278.85

PROGRAM COST ($ 1000.)

ENGINEERING		
CHIP SPECIFICATION	34824.	
CHIP DESIGN	124158.	
SYSTEMS	10025.	
PROJECT MGMT	7238.	
DATA	3116.	
SUBTOTAL ENGINEERING	179360.	
MANUFACTURING		
PROTOTYPE	28.	
PRODUCTION	2558.	
SUBTOTAL MANUFACTURING	2586.	
TOTAL PROGRAM COST	181945.	

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(46)	OCT 86
PROTOTYPE	NOV 86	(4)	FEB 87*
ENG TEST	MAR 87*	(1)	MAR 87*
ITERATIONS	APR 87*	(3)	JUN 87*
		(54)	

	START		END PRE-PROD		FINISH	
PRODUCTION	JUN 87	(3)	AUG 87*	(11)	JUL 88*	(14)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS 1984

ESCALATION 0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (ij=31)

COSTS

UNIT PRODUCTION COST($ 1.00) 650.64

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	1862.
CHIP DESIGN	1720.
SYSTEMS	370.
PROJECT MGMT	247.
DATA	104.
SUBTOTAL ENGINEERING	4303.

MANUFACTURING						
PROTOTYPE			32.			
PRODUCTION			3253.			
SUBTOTAL MANUFACTURING			3285.			
TOTAL PROGRAM COST			7588.			

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(3)	MAR 83
PROTOTYPE	APR 83	(4)	JUL 83*
ENG TEST	AUG 83*	(1)	AUG 83*
ITERATIONS	- *	(0)	- *
		(8)	

	START		END PRE-PROD		FINISH	
PRODUCTION	SEP 83	(3)	NOV 83*	(12)	NOV 84*	(15)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (ij=33)

COSTS

UNIT PRODUCTION COST($ 1.00) 603.78

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	1862.
CHIP DESIGN	1720.
SYSTEMS	370.
PROJECT MGMT	247.
DATA	104.
SUBTOTAL ENGINEERING	4303.
MANUFACTURING	
PROTOTYPE	32.
PRODUCTION	3019.
SUBTOTAL MANUFACTURING	3051.
TOTAL PROGRAM COST	7354.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(3)	MAR 83
PROTOTYPE	APR 83	(4)	JUL 83*
ENG TEST	AUG 83*	(1)	AUG 83*
ITERATIONS	- *	(0)	- *
		(8)	

	START		END PRE-PROD		FINISH	
PRODUCTION	SEP 83	(3)	NOV 83*	(13)	DEC 84*	(16)

SUPPLEMENTAL INFORMATION
YEAR OF ECONOMICS 1984
ESCALATION 0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (ij=21)

COSTS

UNIT PRODUCTION COST($ 1.00)		1801.38
PROGRAM COST ($ 1000.)		
ENGINEERING		
CHIP SPECIFICATION	34440.	
CHIP DESIGN	123067.	
SYSTEMS	9887.	
PROJECT MGMT	7144.	
DATA	3075.	
SUBTOTAL ENGINEERING	177613.	
MANUFACTURING		
PROTOTYPE	28.	
PRODUCTION	7206.	
SUBTOTAL MANUFACTURING	7234.	
TOTAL PROGRAM COST	184847.	

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(45)	SEP 86
PROTOTYPE	OCT 86	(4)	JAN 87*
ENG TEST	FEB 87*	(1)	FEB 87*
ITERATIONS	MAR 87*	(3)	MAY 87*
		(53)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 87	(3)	JUL 87*	(12)	JUL 88*	(15)

SUPPLEMENTAL INFORMATION
YEAR OF ECONOMICS 1984
ESCALATION 0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML(ij=22)

COSTS

UNIT PRODUCTION COST($ 1.00)		1922.85
PROGRAM COST ($ 1000.)		
ENGINEERING		
CHIP SPECIFICATION	34440.	
CHIP DESIGN	123067.	
SYSTEMS	9887.	
PROJECT MGMT	7144.	

DATA	3075.
SUBTOTAL ENGINEERING	177613.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	7691.
SUBTOTAL MANUFACTURING	7720.
TOTAL PROGRAM COST	185332.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(45)	SEP 86
PROTOTYPE	OCT 86	(4)	JAN 87*
ENG TEST	FEB 87*	(1)	FEB 87*
ITERATIONS	MAR 87*	(3)	MAY 87*
		(53)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 87	(3)	JUL 87*	(13)	AUG 88*	(16)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (ij=23)

COSTS

UNIT PRODUCTION COST($ 1.00) 981.20

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	34440.
CHIP DESIGN	123067.
SYSTEMS	9887.
PROJECT MGMT	7144.
DATA	3075.
SUBTOTAL ENGINEERING	177613.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	3925.
SUBTOTAL MANUFACTURING	3953.
TOTAL PROGRAM COST	181566.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(45)	SEP 86
PROTOTYPE	OCT 86	(4)	JAN 87*
ENG TEST	FEB 87*	(1)	FEB 87*
ITERATIONS	MAR 87*	(3)	MAY 87*
		(53)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 87	(3)	JUL 87*	(12)	JUL 88*	(15)

SUPPLEMENTAL INFORMATION
YEAR OF ECONOMICS 1984
ESCALATION 0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (ij=24)

COSTS
UNIT PRODUCTION COST($ 1.00) 2662.42

PROGRAM COST ($ 1000.)	
ENGINEERING	
CHIP SPECIFICATION	34440.
CHIP DESIGN	123067.
SYSTEMS	9887.
PROJECT MGMT	7144.
DATA	3075.
SUBTOTAL ENGINEERING	177613.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	10650.
SUBTOTAL MANUFACTURING	10678.
TOTAL PROGRAM COST	188291.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(45)	SEP 86
PROTOTYPE	OCT 86	(4)	JAN 87*
ENG TEST	FEB 87*	(1)	FEB 87*
ITERATIONS	MAR 87*	(3)	MAY 87*
		(53)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 87	(3)	JUL 87*	(14)	SEP 88*	(17)

SUPPLEMENTAL INFORMATION
YEAR OF ECONOMICS 1984
ESCALATION 0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-NMOS (ij=25)

COSTS
UNIT PRODUCTION COST($ 1.00) 1305.14

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	34440.
CHIP DESIGN	123067.
SYSTEMS	9887.
PROJECT MGMT	7144.
DATA	3075.
SUBTOTAL ENGINEERING	177613.
MANUFACTURING	
PROTOTYPE	28.
PRODUCTION	5221.
SUBTOTAL MANUFACTURING	5249.
TOTAL PROGRAM COST	182862.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(45)	SEP 86
PROTOTYPE	OCT 86	(4)	JAN 87*
ENG TEST	FEB 87*	(1)	FEB 87*
ITERATIONS	MAR 87*	(3)	MAY 87*
		(53)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 87	(3)	JUL 87*	(12)	JUL 88*	(15)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (ij=41)

COSTS

UNIT PRODUCTION COST($ 1.00) 584.74

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	1837.
CHIP DESIGN	1696.
SYSTEMS	364.
PROJECT MGMT	244.
DATA	103.
SUBTOTAL ENGINEERING	4244.
MANUFACTURING	
PROTOTYPE	32.
PRODUCTION	5847.
SUBTOTAL MANUFACTURING	5879.

TOTAL PROGRAM COST 10123.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(3)	MAR 83
PROTOTYPE	APR 83	(4)	JUL 83*
ENG TEST	AUG 83*	(1)	AUG 83*
ITERATIONS	- *	(0)	- *
		(8)	

	START		END PRE-PROD		FINISH	
PRODUCTION	JAN 84	(3)	MAR 84*	(14)	MAY 85*	(17)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS 1984

ESCALATION 0.00*

TITLE: CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (ij=43)

COSTS

UNIT PRODUCTION COST($ 1.00) 542.15

PROGRAM COST ($ 1000.)

ENGINEERING	
CHIP SPECIFICATION	1837.
CHIP DESIGN	1696.
SYSTEMS	364.
PROJECT MGMT	244.
DATA	103.
SUBTOTAL ENGINEERING	4244.
MANUFACTURING	
PROTOTYPE	32.
PRODUCTION	5421.
SUBTOTAL MANUFACTURING	5453.
TOTAL PROGRAM COST	9697.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(3)	MAR 83
PROTOTYPE	APR 83	(4)	JUL 83*
ENG TEST	AUG 83*	(1)	AUG 83*
ITERATIONS	- *	(0)	- *
		(8)	

	START		END PRE-PROD		FINISH	
PRODUCTION	JAN 84	(3)	MAR 84*	(15)	JUN 85*	(18)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS 1984

ESCALATION 0.00*

TITLE: VHSIC MEMORY CHIP-NMOS (ij=55)

```
 COSTS
   UNIT PRODUCTION COST($ 1.00)                         288.72

   PROGRAM COST ($      1000.)
     ENGINEERING
       CHIP SPECIFICATION               13340.
       CHIP DESIGN                      33574.
       SYSTEMS                           2969.
       PROJECT MGMT                      2731.
       DATA                              1161.
     SUBTOTAL ENGINEERING               53775.

     MANUFACTURING
       PROTOTYPE                         1681.
       PRODUCTION                     7815689.
     SUBTOTAL MANUFACTURING           7817369.
   TOTAL PROGRAM COST                 7871144.

 SCHEDULE
   DEVELOPMENT          START                      FINISH
     DESIGN             JAN 83          (  1)      JAN 83
     PROTOTYPE          FEB 83          (  8)      SEP 83*
     ENG TEST           OCT 83*         (  1)      OCT 83*
     ITERATIONS         NOV 83*         (  6)      APR 84*

                                        ( 16)
                        START         END PRE-PROD              FINISH
   PRODUCTION           MAY 84    (  3)  JUL 84*       (105)    APR 93*  (108)

 SUPPLEMENTAL INFORMATION
   YEAR OF ECONOMICS      1984
   ESCALATION             0.00*
```

TITLE: VHSIC MEMORY CHIP-CMOS/BULK (ij=53)

```
 COSTS
   UNIT PRODUCTION COST($ 1.00)                         282.15

   PROGRAM COST ($      1000.)
     ENGINEERING
       CHIP SPECIFICATION               13340.
       CHIP DESIGN                      33574.
       SYSTEMS                           2969.
       PROJECT MGMT                      2731.
       DATA                              1161.
     SUBTOTAL ENGINEERING               53775.

     MANUFACTURING
       PROTOTYPE                         2029.
       PRODUCTION                     7637761.
```

SUBTOTAL MANUFACTURING	7639790.
TOTAL PROGRAM COST	7693564.

SCHEDULE

DEVELOPMENT	START		FINISH
DESIGN	JAN 83	(1)	JAN 83
PROTOTYPE	FEB 83	(8)	SEP 83*
ENG TEST	OCT 83*	(1)	OCT 83*
ITERATIONS	NOV 83*	(6)	APR 84*
		(16)	

	START		END PRE-PROD		FINISH	
PRODUCTION	MAY 84	(3)	JUL 84*	(122)	SEP 94*	(125)

SUPPLEMENTAL INFORMATION

YEAR OF ECONOMICS	1984
ESCALATION	0.00*

SAR 1 OUTPUT DATA: BASELINE CONFIGURATION

PURCHASED ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR (CASE 1)			
TOTAL COST	179388.	4095.	183483.
CIRCUIT CARD (CASE 1)			
TOTAL COST	-	-	-
CONTROL PROCESSOR (CASE 1)			
TOTAL COST	177641.	3925.	181566.
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	557.	76180.	76737.
LOGIC PCB I&T (CASE 1)			
TOTAL COST	52.	840.	892.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	7.	16.
DESIGN	32.	23.	55.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	80.	83.
DATA	1.	30.	31.
SUBTOTAL(ENG)	49.	139.	189.
MANUFACTURING			
PRODUCTION	-	688.	688.
PROTOTYPE	3.	-	3.

TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	357585.	84200.	441786.
SUBTOTAL(MFG)	357588.	84901.	442489.
TOTAL COST	357638.	85040.	442678.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	357633.	84925.	442558.
CENTER	357638.	85040.	442678.
TO	357644.	85173.	442817.

****
* SYSTEM WT 2.13 SYSTEM WS 0.57 *
* SYSTEM SERIES MTBF HRS. 2720 AV SYSTEM COST 85 *
****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	55247.	7561619.	7616866.
MEMORY PCB I&T (ALL CASES)			
TOTAL COST	164.	34680.	34844.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	7.	10.	17.
DESIGN	24.	36.	60.
SYSTEMS	3.	-	3.
PROJ MGMT	7.	2262.	2269.
DATA	2.	814.	816.
SUBTOTAL(ENG)	43.	3122.	3165.
MANUFACTURING			
PRODUCTION	-	31136.	31136.
PROTOTYPE	110.	-	110.
TOOL-TEST EQ	11.	422.	434.
PURCH ITEMS	55247.	7561619.	7616866.
SUBTOTAL(MFG)	55368.	7593177.	7648545.
TOTAL COST	55411.	7596299.	7651710.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	55394.	7592515.	7647908.
CENTER	55411.	7596299.	7651710.
TO	55433.	7600473.	7655906.

****

* SYSTEM WT	2.57	SYSTEM WS	0.57	*
* SYSTEM SERIES MTBF HRS.	1684	AV SYSTEM COST	113	*

****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CHASSIS (ALL CASES)			
TOTAL COST	-	-	-
SOFTWARE DEVELOPMENT (ALL CASES)			
TOTAL COST	11895.	-	11895.

SYSTEM COST SUMMARY

SAR I&T (CASES 1 & 3)

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SAR I&T (CASES 1 & 3)			
TOTAL COST	172.	4409.	4581.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412833.	7645819.	8058651.
SUBTOTAL(MFG)	412975.	7681851.	8094826.
TOTAL COST	413221.	7685747.	8098968.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413183.	7681220.	8094403.
CENTER	413221.	7685747.	8098968.
TO	413272.	7690807.	8104079.

****

* SYSTEM WT	241.36	SYSTEM WS	105.80	*
* SYSTEM SERIES MTBF HRS.	510	AV SYSTEM COST	7686	*

****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425116.	7685747.	8110863.

LCC OF SAR PROCESSOR, DEFAULT CASE 1

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SAR1.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	7552234	***	7977350
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1027530	6789418	7816948
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	425116	8617886	6852052	15895054

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

PURCHASED ITEM

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR (CASE 2)			
TOTAL COST	4335.	3253.	7588.
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
CONTROL PROCESSOR (CASE 2)			
TOTAL COST	4276.	5421.	9697.
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	557.	76180.	76737.
LOGIC PCB I&T (CASE 2)			
TOTAL COST	45.	932.	977.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	8.	8.	17.
DESIGN	27.	30.	57.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	93.	95.
DATA	1.	35.	36.
SUBTOTAL (ENG)	42.	166.	209.
MANUFACTURING			
PRODUCTION	-	754.	754.
PROTOTYPE	2.	-	2.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	9168.	84855.	94023.
SUBTOTAL (MFG)	9170.	85621.	94791.
TOTAL COST	9213.	85787.	95000.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	9209.	85688.	94897.
CENTER	9213.	85787.	95000.
TO	9218.	85897.	95115.

```
**************************************************************************
* SYSTEM  WT                 2.16         SYSTEM  WS              0.57  *
* SYSTEM SERIES MTBF HRS.    3405         AV SYSTEM COST           86   *
**************************************************************************
```

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	55247.	7561619.	7616866.
MEMORY PCB I&T (ALL CASES)			
TOTAL COST	164.	34680.	34844.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	7.	10.	17.
DESIGN	24.	36.	60.
SYSTEMS	3.	-	3.
PROJ MGMT	7.	2262.	2269.
DATA	2.	814.	816.
SUBTOTAL(ENG)	43.	3122.	3165.
MANUFACTURING			
PRODUCTION	-	31136.	31136.
PROTOTYPE	110.	-	110.
TOOL-TEST EQ	11.	422.	434.
PURCH ITEMS	55247.	7561619.	7616866.
SUBTOTAL(MFG)	55368.	7593177.	7648545.
TOTAL COST	55411.	7596299.	7651710.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	55394.	7592515.	7647908.
CENTER	55411.	7596299.	7651710.
TO	55433.	7600473.	7655906.

```
*************************************************************************
* SYSTEM  WT                     2.57        SYSTEM  WS           0.57  *
* SYSTEM SERIES MTBF HRS.        1684        AV SYSTEM COST       113   *
*************************************************************************
```

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CHASSIS (ALL CASES)			
TOTAL COST	-	-	-
SOFTWARE DEVELOPMENT (ALL CASES)			
TOTAL COST	11895.	-	11895.

SYSTEM COST SUMMARY

SAR I&T (CASE 2)

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SAR I&T (CASE 2)			
TOTAL COST	157.	5002.	5159.

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	6.	16.
DESIGN	33.	23.	56.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	80.	83.
DATA	1.	30.	31.
SUBTOTAL(ENG)	50.	140.	190.
MANUFACTURING			
PRODUCTION	-	693.	693.
PROTOTYPE	3.	-	3.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	182533.	83358.	265891.
SUBTOTAL(MFG)	182536.	84064.	266600.
TOTAL COST	182586.	84204.	7710888.
SUBTOTAL(MFG)	64554.	7682950.	7747505.
TOTAL COST	64780.	7687088.	7751867.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	64744.	7682654.	7747397.
CENTER	64780.	7687088.	7751867.
TO	64829.	7692006.	7756835.

```
****************************************************************************
* SYSTEM  WT                241.38              SYSTEM  WS            105.80  *
* SYSTEM SERIES MTBF HRS.   530                 AV SYSTEM COST        7687    *
****************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
FIELD SUPPORT	0.	0.	0.
FIELD TEST	0.	0.	0.
SOFTWARE	11895.	0.	11895.
OTHER	0.	0.	0.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
76675.	7687088.	7763762.

LCC OF SAR PROCESSOR, DEFAULT CASE 2

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SAR2.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	76675	7553395	***	7630070
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	990409	6574227	7564636
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	76675	8581926	6636718	15295319

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

PURCHASED ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR (CASE 3)			
TOTAL COST	179388.	4095.	183483.
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
CONTROL PROCESSOR (CASE 3)			
TOTAL COST	4276.	5421.	9697.
MEMORY CHIP (ALL CASES)			
TOTAL COST	557.	76180.	76737.
LOGIC PCB I&T (CASE 3)			
TOTAL COST	53.	861.	914.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	7.	17.
DESIGN	32.	24.	56.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	82.	85.
DATA	1.	31.	32.
SUBTOTAL(ENG)	50.	143.	193.
MANUFACTURING			
PRODUCTION	-	706.	706.
PROTOTYPE	3.	-	3.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	184220.	85697.	269918.
SUBTOTAL(MFG)	184224.	86415.	270639.
TOTAL COST	184273.	86558.	270831.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	184269.	86441.	270709.
CENTER	184273.	86558.	270831.
TO	184280.	86693.	270973.

```
**********************************************************************
* SYSTEM  WT                    2.15      SYSTEM  WS            0.57  *
* SYSTEM SERIES MTBF HRS.       3315      AV SYSTEM COST        87    *
**********************************************************************
```

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	55247.	7561619.	7616866.
MEMORY PCB I&T (ALL CASES)			
TOTAL COST	164.	34680.	34844.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	7.	10.	17.
DESIGN	24.	36.	60.
SYSTEMS	3.	-	3.
PROJ MGMT	7.	2262.	2269.
DATA	2.	814.	816.
SUBTOTAL(ENG)	43.	3122.	3165.
MANUFACTURING			
PRODUCTION	-	31136.	31136.
PROTOTYPE	110.	-	110.
TOOL-TEST EQ	11.	422.	434.
PURCH ITEMS	55247.	7561619.	7616866.
SUBTOTAL(MFG)	55368.	7593177.	7648545.
TOTAL COST	55411.	7596299.	7651710.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	55394.	7592515.	7647908.
CENTER	55411.	7596299.	7651710.
TO	55433.	7600473.	7655906.

****

* SYSTEM WT	2.57	SYSTEM WS	0.57	*
* SYSTEM SERIES MTBF HRS.	1684	AV SYSTEM COST	113	*

****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CHASSIS (ALL CASES)			
TOTAL COST	-	-	-
SOFTWARE DEVELOPMENT (ALL CASES)			
TOTAL COST	11895.	-	11895.

SYSTEM COST SUMMARY

SAR I&T (CASES 1 & 3)

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SAR I&T (CASES 1 & 3)			
TOTAL COST	172.	4416.	4589.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	42.	89.
DESIGN	156.	146.	301.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2727.	2746.
DATA	6.	986.	993.
SUBTOTAL(ENG)	247.	3900.	4147.
MANUFACTURING			
PRODUCTION	-	35579.	35579.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	493.
PURCH ITEMS	239468.	7647316.	7886783.
SUBTOTAL(MFG)	239610.	7683372.	7922981.
TOTAL COST	239857.	7687273.	7927129.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	239819.	7682742.	7922560.
CENTER	239857.	7687273.	7927129.
TO	239908.	7692336.	7932243.

****
* SYSTEM WT 241.37 SYSTEM WS 105.80 *
* SYSTEM SERIES MTBF HRS. 528 AV SYSTEM COST 7687 *
****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
251752.	7687273.	7939024.

LCC OF SAR PROCESSOR, CASE 3

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SAR3.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	528	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	251752	7557621	***	7809373
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	990410	6596717	7587127
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1992	1992
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1712	1712
TOTAL COST	251752	8586153	6659221	15497126

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9928

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.412	0.000	0.000
LOAD FACTOR	0.380	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	322
BALANCE CONSUMED	664.41	0.00	4361.441

PURCHASED ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR (CASE 4)			
TOTAL COST	4335.	3253.	7588.
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
CONTROL PROCESSOR (CASE 4)			
TOTAL COST	177641.	3925.	181566.
MEMORY CHIPS (ALL CASES)			
TOTAL COST	557.	76180.	76737.
LOGIC PCB I&T (CASE 4)			
TOTAL COST	53.	846.	899.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	6.	16.
DESIGN	33.	23.	56.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	80.	83.
DATA	1.	30.	31.
SUBTOTAL(ENG)	50.	140.	190.
MANUFACTURING			
PRODUCTION	-	693.	693.
PROTOTYPE	3.	-	3.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	182533.	83358.	265891.
SUBTOTAL(MFG)	182536.	84064.	266600.
TOTAL COST	182586.	84204.	266790.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	182581.	84088.	266669.
CENTER	182586.	84204.	266790.
TO	182592.	84338.	266930.

****
* SYSTEM WT 2.14 SYSTEM WS 0.57 *
* SYSTEM SERIES MTBF HRS. 3237 AV SYSTEM COST 84 *
****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	55247.	7561619.	7616866.
MEMORY PCB I&T (ALL CASES)			
TOTAL COST	164.	34680.	34844.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	7.	10.	17.
DESIGN	24.	36.	60.
SYSTEMS	3.	-	3.
PROJ MGMT	7.	2262.	2269.
DATA	2.	814.	816.
SUBTOTAL(ENG)	43.	3122.	3165.
MANUFACTURING			
PRODUCTION	-	31136.	31136.
PROTOTYPE	110.	-	110.
TOOL-TEST EQ	11.	422.	434.
PURCH ITEMS	55247.	7561619.	7616866.
SUBTOTAL(MFG)	55368.	7593177.	7648545.
TOTAL COST	55411.	7596299.	7651710.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	55394.	7592515.	7647908.
CENTER	55411.	7596299.	7651710.
TO	55433.	7600473.	7655906.

```
*************************************************************************
* SYSTEM  WT               2.57         SYSTEM  WS           0.57  *
* SYSTEM SERIES MTBF HRS.  1684         AV SYSTEM COST       113   *
*************************************************************************
```

GFE ITEM

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CHASSIS (ALL CASES)			
TOTAL COST	-	-	-
SOFTWARE DEVELOPMENT (ALL CASES)			
TOTAL COST	11895.	-	11895.

COST SUMMARY

SAR I&T (CASE 4)

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SAR I&T (CASE 4)			
TOTAL COST	174.	4401.	4575.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	157.	144.	301.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2725.	2745.
DATA	6.	986.	992.
SUBTOTAL (ENG)	249.	3895.	4144.
MANUFACTURING			
PRODUCTION	-	35554.	35554.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	237780.	7644977.	7882757.
SUBTOTAL (MFG)	237922.	7681008.	7918929.
TOTAL COST	238171.	7684903.	7923074.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	238133.	7680376.	7918508.
CENTER	238171.	7684903.	7923074.
TO	238222.	7689962.	7928184.

```
**************************************************************************
* SYSTEM  WT                  241.36        SYSTEM  WS           105.80  *
* SYSTEM SERIES MTBF HRS.     526           AV SYSTEM COST       7685    *
**************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
250066.	7684903.	7934969.

LCC OF SAR PROCESSOR, DEFAULT CASE 4

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SAR4.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	526	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	250066	7555651	***	7805717
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	990187	6617654	7607841
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2000	2000
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1718	1718
TOTAL COST	250066	8583960	6680172	15514198

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9926

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.453	0.000	0.000
LOAD FACTOR	0.382	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	323
BALANCE CONSUMED	667.21	0.00	4377.300

Section 2

Input Data and Output Data for Maintenance Level Analysis

The case, 95% of all PCBs are repaired at organization, is the default case. For this case, 5% of removed PCBs are repaired at organization; 95% of removed PCBs are repaired at depot.

Table XXXVIII gives value changes to default input variables for analysis of maintenance level.

TABLE XXXVIII

Changes to Default Values for Analysis of Maintenance Level

Variable Name	Value	ij	Case	Model/ File or Mode	Source
FMO	.05	00	All	L/Global	Assumed
FMD	.95	00	All	L/Global	Assumed

SYSTEM COST SUMMARY, DEFAULT CASE 1

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412833.	7645819.	8058651.
SUBTOTAL(MFG)	412975.	7681851.	8094826.
TOTAL COST	413221.	7685747.	8098968.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413183.	7681220.	8094403.
CENTER	413221.	7685747.	8098968.
TO	413272.	7690807.	8104079.

```
*************************************************************************
* SYSTEM  WT                   241.36        SYSTEM  WS         105.80  *
* SYSTEM SERIES MTBF HRS.      510           AV SYSTEM COST     7686    *
*************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425116.	7685747.	8110863.

LCC OF SAR PROCESSOR CASE 1, 95% OF ALL PCB REPAIRS AT DEPOT

GLOBAL FILENAME: GLOB.05
LIFE CYCLE FILENAME: SAR1.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	7552234	***	7977350
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1216326	8463918	9680244
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	640	640
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	2052	2052
TOTAL COST	425116	8806682	8525410	17757208

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	0.622	0.000	0.000
LOAD FACTOR	0.021	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	43	32
BALANCE CONSUMED	687.59	170.84	223.103

SYSTEM COST SUMMARY, DEFAULT CASE 2

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	6.	16.
DESIGN	33.	23.	56.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	80.	83.
DATA	1.	30.	31.
SUBTOTAL(ENG)	50.	140.	190.
MANUFACTURING			
PRODUCTION	-	693.	693.
PROTOTYPE	3.	-	3.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	182533.	83358.	265891.
SUBTOTAL(MFG)	182536.	84064.	266600.
TOTAL COST	182586.	84204.	7710888.
SUBTOTAL(MFG)	64554.	7682950.	7747505.
TOTAL COST	64780.	7687088.	7751867.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	64744.	7682654.	7747397.
CENTER	64780.	7687088.	7751867.
TO	64829.	7692006.	7756835.

```
***********************************************************************
* SYSTEM  WT                  241.38        SYSTEM  WS          105.80  *
* SYSTEM SERIES MTBF HRS.     530           AV SYSTEM COST      7687    *
***********************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
76675.	7687088.	7763762.

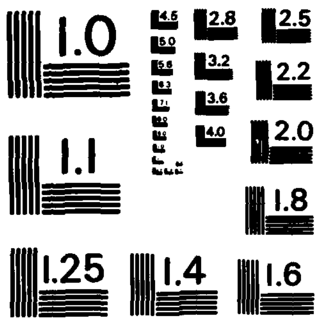
AD-A147 798 LIFE CYCLE COST MODEL FOR VERY HIGH SPEED INTEGRATED CIRCUITS(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF SYSTEMS AND LOGISTICS E A LONG SEP 84 3/3

UNCLASSIFIED AFIT/GLM/LSM/84S-39 F/G 14/1 NL

END

FILMED

DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

LCC OF SAR PROCESSOR CASE 2, 95% OF PCB REPAIRES AT DEPOT

GLOBAL FILENAME: GLOB.05
LIFE CYCLE FILENAME: SAR2.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	76675	7553395	***	7630070
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1186857	8174613	9361470
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	616	616
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1976	1976
TOTAL COST	76675	8778374	8236005	17091054

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	0.598	0.000	0.000
LOAD FACTOR	0.020	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	43	31
BALANCE CONSUMED	661.63	162.88	214.615

SYSTEM COST SUMMARY, DEFAULT CASE 3

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	42.	89.
DESIGN	156.	146.	301.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2727.	2746.
DATA	6.	986.	993.
SUBTOTAL (ENG)	247.	3900.	4147.
MANUFACTURING			
PRODUCTION	-	35579.	35579.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	493.
PURCH ITEMS	239468.	7647316.	7886783.
SUBTOTAL (MFG)	239610.	7683372.	7922981.
TOTAL COST	239857.	7687273.	7927129.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	239819.	7682742.	7922560.
CENTER	239857.	7687273.	7927129.
TO	239908.	7692336.	7932243.

```
***************************************************************************
* SYSTEM  WT                241.37          SYSTEM  WS           105.80  *
* SYSTEM SERIES MTBF HRS.   528             AV SYSTEM COST       7687    *
***************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
251752.	7687273.	7939024.

LCC OF SAR PROCESSOR CASE 3, 95% OF ALL PCB REPAIRS AT DEPOT

GLOBAL FILENAME: GLOB.05
LIFE CYCLE FILENAME: SAR3.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	528	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	251752	7557621	***	7809373
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1186857	8204353	9391210
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	618	618
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1983	1983
TOTAL COST	251752	8782600	8265754	17300106

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9928

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	0.601	0.000	0.000
LOAD FACTOR	0.020	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	43	31
BALANCE CONSUMED	664.41	163.62	215.496

SYSTEM COST SUMMARY, DEFAULT CASE 4

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	157.	144.	301.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2725.	2745.
DATA	6.	986.	992.
SUBTOTAL(ENG)	249.	3895.	4144.
MANUFACTURING			
PRODUCTION	-	35554.	35554.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	237780.	7644977.	7882757.
SUBTOTAL(MFG)	237922.	7681008.	7918929.
TOTAL COST	238171.	7684903.	7923074.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	238133.	7680376.	7918508.
CENTER	238171.	7684903.	7923074.
TO	238222.	7689962.	7928184.

```
***************************************************************************
* SYSTEM WT                241.36        SYSTEM WS             105.80  *
* SYSTEM SERIES MTBF HRS.  526           AV SYSTEM COST        7685    *
***************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
250066.	7684903.	7934969.

LCC OF SAR PROCESSOR CASE 4, 95% OF ALL PCB REPAIRS AT DEPOT

GLOBAL FILENAME: GLOB.05
LIFE CYCLE FILENAME: SAR4.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	526	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	250066	7555651	***	7805717
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1186633	8230661	9417294
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	620	620
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1990	1990
TOTAL COST	250066	8780406	8292071	17322543

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9926

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	0.603	0.000	0.000
LOAD FACTOR	0.020	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	43	31
BALANCE CONSUMED	667.21	164.37	216.383

Section 3

Input Data and Output Data for Substrate Type Analysis

The bulk silicon substrate case (case 1) is the default case.

Table XXXIX gives value changes to default input variables for substrate analysis.

TABLE XXXIX

Changes to Default Values for Substrate Analysis

Variable Name	Value	ij	Case	Model/ File or Mode	Source
AUC1	2932.45	14	1	H/3	PRICE M Output
AUC1	2662.42	24	1	H/3	PRICE M Output

PURCHASED ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR-CMOS/SOS (CASE 5:SUBSTRATE ANALYSIS)			
TOTAL COST	179388.	5865.	185253.
CIRCUIT CARD (CASE 1)			
TOTAL COST	-	-	-
CONTROL PROCESSOR-CMOS/SOS (CASE 5:SUBSTRATE ANALYSIS)			
TOTAL COST	177641.	10650.	188291.
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	557.	76180.	76737.
LOGIC PCB I&T (CASE 1)			
TOTAL COST	52.	840.	892.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	10.	7.	16.
DESIGN	32.	23.	55.
SYSTEMS	3.	-	3.
PROJ MGMT	3.	80.	83.
DATA	1.	30.	31.
SUBTOTAL(ENG)	49.	139.	189.
MANUFACTURING			
PRODUCTION	-	688.	688.
PROTOTYPE	3.	-	3.
TOOL-TEST EQ	1.	12.	13.
PURCH ITEMS	357585.	92695.	450281.
SUBTOTAL(MFG)	357589.	93396.	450984.
TOTAL COST	357638.	93535.	451173.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	357633.	93420.	451053.
CENTER	357638.	93535.	451173.
TO	357644.	93668.	451312.

****
* SYSTEM WT 2.13 SYSTEM WS 0.57 *
* SYSTEM SERIES MTBF HRS. 2720 AV SYSTEM COST 94 *
****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CIRCUIT CARD (ALL CASES)			
TOTAL COST	-	-	-
MEMORY CHIPS CMOS/BULK (ALL CASES)			
TOTAL COST	55247.	7561619.	7616866.
MEMORY PCB I&T (ALL CASES)			
TOTAL COST	164.	34680.	34844.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	7.	10.	17.
DESIGN	24.	36.	60.
SYSTEMS	3.	-	3.
PROJ MGMT	7.	2262.	2269.
DATA	2.	814.	816.
SUBTOTAL(ENG)	43.	3122.	3165.
MANUFACTURING			
PRODUCTION	-	31136.	31136.
PROTOTYPE	110.	-	110.
TOOL-TEST EQ	11.	422.	434.
PURCH ITEMS	55247.	7561619.	7616866.
SUBTOTAL(MFG)	55368.	7593177.	7648545.
TOTAL COST	55411.	7596299.	7651710.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	55394.	7592515.	7647908.
CENTER	55411.	7596299.	7651710.
TO	55433.	7600473.	7655906.

****
* SYSTEM WT 2.57 SYSTEM WS 0.57 *
* SYSTEM SERIES MTBF HRS. 1684 AV SYSTEM COST 113 *
****

GFE ITEM

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
CHASSIS (ALL CASES)			
TOTAL COST	-	-	-
SOFTWARE DEVELOPMENT (ALL CASES)			
TOTAL COST	11895.	-	11895.

SYSTEM COST SUMMARY

DATE 13-JUL-84 TIME 16:14 (184170) FILENAME: SARIT.13

SAR I&T (CASES 1 & 3)

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
SAR I&T (CASES 1 & 3)			
TOTAL COST	172.	4409.	4581.

SYSTEM COST SUMMARY

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412833.	7654314.	8067146.
SUBTOTAL(MFG)	412975.	7690346.	8103321.
TOTAL COST	413221.	7694241.	8107463.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413183.	7689714.	8102897.
CENTER	413221.	7694241.	8107463.
TO	413272.	7699301.	8112573.

****

* SYSTEM WT	241.36	SYSTEM WS	105.80	*
* SYSTEM SERIES MTBF HRS.	510	AV SYSTEM COST	7694	*

****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
FIELD SUPPORT	0.	0.	0.
FIELD TEST	0.	0.	0.
SOFTWARE	11895.	0.	11895.
OTHER	0.	0.	0.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425116.	7694241.	8119358.

LCC OF SAR PROCESSOR CASE 1,SOS SUBSTRATE ANALYSIS

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SAR5.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	7560091	***	7985207
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1028457	6796481	7824938
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	425116	8626670	6859115	15910901

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

Section 4

Input Data and Output Data for CAD Analysis

The CAD case for custom design, case 1 (little CAD) and the case for gate array design, case 2 (extensive CAD) are the default cases. Output data for chip costs are presented first which are followed by LCC output data for cases 1 and 2.

Table XL gives value changes to default input variables for little, some, and extensive CAD.

TABLE XL

Changes to Default Values for Little, Some, and Extensive CAD Analysis

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CADFAC	1.2	11	1	M	Extensive CAD
CADFAC	1.2	23	1	M	Extensive CAD
CADFAC	1.0	11	1	M	Some CAD
CADFAC	1.0	23	1	M	Some CAD
CADFAC	1.0	31	2	M	Some CAD
CADFAC	1.0	43	2	M	Some CAD
CADFAC	.8	31	2	M	Little CAD
CADFAC	.8	43	2	M	Little CAD
DESRPT	.15	11	1	M	Extensive CAD
DESRPT	.15	23	1	M	Extensive CAD

TABLE XL

Changes to Default Values for Little, Some, and Extensive CAD Analysis (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
DESRPT	.15	11	1	M	Some CAD
DESRPT	.15	23	1	M	Some CAD
DESRPT	.5	31	2	M	Some CAD
DESRPT	.5	43	2	M	Some CAD
DESRPT	.5	31	2	M	Little CAD
DESRPT	.5	43	2	M	Little CAD
DMULT	21305.431	11	1	H/3	PRICE M Output
DMULT	21924.429	23	1	H/3	PRICE M Output
DMULT	29980.465	11	1	H/3	PRICE M Output
DMULT	30943.488	23	1	H/3	PRICE M Output
DMULT	2098.8568	31	2	H/3	PRICE M Output
DMULT	1242.0917	43	2	H/3	PRICE M Output
DMULT	3307.2052	31	2	H/3	PRICE M Output
DMULT	1957.3919	43	2	H/3	PRICE M Output
ITERAT	0	11	1	M	Extensive CAD

TABLE XL

Changes to Default Values for Little, Some, and Extensive CAD Analysis (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ITERAT	0	23	1	M	Extensive CAD
ITERAT	1	11	1	M	Some CAD
ITERAT	1	23	1	M	Some CAD
ITERAT	1	31	2	M	Some CAD
ITERAT	1	43	2	M	Some CAD
ITERAT	2	31	2	M	Little CAD
ITERAT	2	43	2	M	Little CAD
NEWCEL	.05	11	1	M	Extensive CAD
NEWCEL	.05	23	1	M	Extensive CAD
NEWCEL	.50	11	1	M	Some CAD
NEWCEL	.50	23	1	M	Some CAD
NEWCEL	.50	31	2	M	Some CAD
NEWCEL	.50	43	2	M	Some CAD
NEWCEL	.85	31	2	M	Little CAD
NEWCEL	.85	43	2	M	Little CAD

CAD ANALYSIS FOR SIGNAL PROCESSOR AND CONTROL PROCESSOR CHIPS

PROGRAM COST ($ 1000.)

TITLE	ENGINEERING	PROTOTYPE	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (CAD ANALYSIS-EXTENSIVE)	87221.	29.	4095.	91345.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (CAD ANALYSIS-EXTENSIVE)	87221.	29.	4288.	91538.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (CAD ANALYSIS-EXTENSIVE)	87221.	29.	2165.	89415.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (CAD ANALYSIS-EXTENSIVE)	87221.	29.	5865.	93115.
SIGNAL PROCESSOR VHSIC CHIP-NMOS (CAD ANALYSIS-EXTENSIVE)	87221.	29.	2558.	89807.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA: CAD ANALYSIS-LITTLE)	10722.	37.	3253.	14013.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (GA: CAD ANALYSIS-LITTLE)	8017.	37.	3019.	11073.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (CAD ANALYSIS-EXTENSIVE)	86020.	29.	7206.	93254.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (CAD ANALYSIS-EXTENSIVE)	86020.	29.	7691.	93740.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (CAD ANALYSIS-EXTENSIVE)	86020.	29.	3925.	89974.
CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (CAD ANALYSIS-EXTENSIVE)	86020.	29.	10650.	96699.
CONTROL PROCESSOR VHSIC CHIP-NMOS (CAD ANALYSIS-EXTENSIVE)	86020.	29.	5221.	91269.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA: CAD ANALYSIS-LITTLE)	10575.	37.	5847.	16459.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (GA: CAD ANALYSIS-LITTLE)	10575.	37.	5421.	16033.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (CAD ANALYSIS-SOME)	122748.	28.	4095.	126871.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (CAD ANALYSIS-SOME)	122748.	28.	4288.	127064.

TITLE	ENGINEERING	PROTOTYPE	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (CAD ANALYSIS-SOME)	122748.	28.	2165.	124941.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (CAD ANALYSIS-SOME)	122748.	28.	5865.	128641.
SIGNAL PROCESSOR VHSIC CHIP-NMOS (CAD ANALYSIS-SOME)	122748.	28.	2558.	125334.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA: CAD ANALYSIS-SOME)	6793.	35.	3253.	10081.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (GA: CAD ANALYSIS-SOME)	6793.	35.	3019.	9847.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (CAD ANALYSIS-SOME)	121418.	29.	7206.	128653.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (CAD ANALYSIS-SOME)	121418.	29.	7691.	129139.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (CAD ANALYSIS-SOME)	121418.	29.	3925.	125372.
CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (CAD ANALYSIS-SOME)	121418.	29.	10650.	132097.
CONTROL PROCESSOR VHSIC CHIP-NMOS (CAD ANALYSIS-SOME)	121418.	29.	5221.	126668.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA: CAD ANALYSIS-SOME)	6699.	35.	5847.	12582.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (GA: CAD ANALYSIS-SOME)	6699.	35.	5421.	12156.

SYSTEM COST SUMMARY CAD ANALYSIS-SOME (CASE 1)

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	300027.	7645819.	7945845.
SUBTOTAL(MFG)	300169.	7681851.	7982020.
TOTAL COST	300415.	7685747.	7986163.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	300377.	7681220.	7981597.
CENTER	300415.	7685747.	7986163.
TO	300466.	7690807.	7991273.

****
* SYSTEM WT 241.36 SYSTEM WS 105.80 *
* SYSTEM SERIES MTBF HRS. 510 AV SYSTEM COST 7686 *
****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
312310.	7685747.	7998058.

LCC OF SAR PROCESSOR CASE 1 (CAD ANALYSIS-SOME)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SCADS.LI
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	312310	7552234	***	7864544
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1027530	6789418	7816948
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	312310	8617886	6852052	15782248

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

SYSTEM COST SUMMARY CAD ANALYSIS-EXTENSIVE (CASE 1)

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	229103.	7645819.	7874922.
SUBTOTAL(MFG)	229245.	7681851.	7911096.
TOTAL COST	229491.	7685747.	7915239.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	229453.	7681220.	7910673.
CENTER	229491.	7685747.	7915239.
TO	229542.	7690807.	7920349.

```
*************************************************************************
* SYSTEM  WT                 241.36          SYSTEM  WS        105.80  *
* SYSTEM SERIES MTBF HRS.    510             AV SYSTEM COST    7686    *
*************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
241386.	7685747.	7927134.

LCC OF SAR PROCESSOR,CASE 1 (CAD ANALYSIS-EXTENSIVE)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SCADE.LI
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	241386	7552234	***	7793620
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	1027530	6789418	7816948
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	241386	8617886	6852052	15711324

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

SYSTEM COST SUMMARY CAD ANALYSIS-SOME (CASE 2)

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	42.	54.	96.
DESIGN	140.	188.	328.
SYSTEMS	19.	-	19.
PROJ MGMT	18.	2855.	2874.
DATA	7.	1039.	1046.
SUBTOTAL (ENG)	226.	4136.	4362.
MANUFACTURING			
PRODUCTION	-	36001.	36001.
PROTOTYPE	125.	-	125.
TOOL-TEST EQ	14.	477.	491.
PURCH ITEMS	69366.	7646474.	7715839.
SUBTOTAL (MFG)	69505.	7682950.	7752456.
TOTAL COST	69731.	7687088.	7756818.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	69695.	7682654.	7752348.
CENTER	69731.	7687088.	7756818.
TO	69780.	7692006.	7761786.

****

* SYSTEM WT 241.38 SYSTEM WS 105.80 *

* SYSTEM SERIES MTBF HRS. 530 AV SYSTEM COST 7687 *

****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
81626.	7687088.	7768713.

LCC OF SAR PROCESSOR,CASE 2 (GA:CAD ANALYSIS-SOME)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SCDS.GLI
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	81626	7557856	***	7639482
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	990409	6574227	7564636
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	81626	8586387	6636718	15304731

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

SYSTEM COST SUMMARY CAD ANALYSIS-LITTLE (CASE 2)

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	42.	54.	96.
DESIGN	140.	188.	328.
SYSTEMS	19.	-	19.
PROJ MGMT	18.	2855.	2874.
DATA	7.	1039.	1046.
SUBTOTAL(ENG)	226.	4136.	4362.
MANUFACTURING			
PRODUCTION	-	36001.	36001.
PROTOTYPE	125.	-	125.
TOOL-TEST EQ	14.	477.	491.
PURCH ITEMS	77175.	7646474.	7723648.
SUBTOTAL(MFG)	77314.	7682950.	7760265.
TOTAL COST	77540.	7687088.	7764627.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	77504.	7682654.	7760157.
CENTER	77540.	7687088.	7764627.
TO	77589.	7692006.	7769595.

****
* SYSTEM WT 241.38 SYSTEM WS 105.80 *
* SYSTEM SERIES MTBF HRS. 530 AV SYSTEM COST 7687 *
****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
89435.	7687088.	7776522.

LCC OF SAR PROCESSOR CASE 2 (GA:CAD ANALYSIS-LITTLE)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: SCDL.GLI
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	89435	7557856	***	7647291
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	990409	6574227	7564636
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	89435	8586387	6636718	15312540

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

Section 5

Input Data and Output Data for Chip Fabrication Yield Analysis

Overall yields for cases 1 and 2 are the default values for yield analysis. Output data for chip costs are presented first which are followed by LCC output data for cases 1 and 2.

Tables XLI, XLII, and XLIII depict value changes to default input variables for 1%, 5%, and 10% yield analysis respectively.

TABLE XLI

Changes to Default Values for 1% OVLYLD Analysis

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ASMYLD	.1	11	1	M	Assumed for 1%
ASMYLD	.1	23	1	M	Assumed for 1%
ASMYLD	.1	31	2	M	Assumed for 1%
ASMYLD	.1	43	2	M	Assumed for 1%
ASMYLD	.1	53	1,2	M	Assumed for 1%
AUC1	$901.50	11	1	H/3	PRICE M Output
AUC1	$405.75	23	1	H/3	PRICE M Output
AUC1	$351.60	31	2	H/3	PRICE M Output
AUC1	$405.75	43	2	H/3	PRICE M Output

TABLE XLI

Changes to Default Values for 1% OVLYLD Analysis (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
AUC1	$233.26	53	1,2	H/3	PRICE M Output
CPYLD	.1	11	1	M	Assumed for 1%
CPYLD	.1	23	1	M	Assumed for 1%
CPYLD	.1	31	2	M	Assumed for 1%
CPYLD	.1	43	2	M	Assumed for 1%
CPYLD	.1	53	1,2	M	Assumed for 1%
DMULT	99494.176	11	1	H/3	PRICE M Output
DMULT	109452.25	23	1	H/3	PRICE M Output
DMULT	2465.8703	31	2	H/3	PRICE M Output
DMULT	109452.25	43	2	H/3	PRICE M Output
DMULT	8.837650	53	1,2	H/3	PRICE M Output
OVLYLD	.01	11	1	M	1% Yield
OVLYLD	.01	23	1	M	1% Yield
OVLYLD	.01	31	2	M	1% Yield
OVLYLD	.01	43	2	M	1% Yield
OVLYLD	.01	53	1,2	M	1% Yield

TABLE XLII

Changes to Default Values for 5% *OVLYLD* Analysis

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ASMYLD	.224	11	1	M	Assumed for 5%
ASMYLD	.224	23	1	M	Assumed for 5%
ASMYLD	.224	31	2	M	Assumed for 5%
ASMYLD	.224	43	2	M	Assumed for 5%
ASMYLD	.224	53	1,2	M	Assumed for 5%
AUC1	$411.00	11	1	H/3	PRICE M Output
AUC1	$212.75	23	1	H/3	PRICE M Output
AUC1	$199.20	31	2	H/3	PRICE M Output
AUC1	$212.75	43	2	H/3	PRICE M Output
AUC1	$125.78	53	1,2	H/3	PRICE M Output
CPYLD	.224	11	1	M	Assumed for 5%
CPYLD	.224	23	1	M	Assumed for 5%
CPYLD	.224	31	2	M	Assumed for 5%
CPYLD	.224	43	2	M	Assumed for 5%

TABLE XLII

Changes to Default Values for 5% OVLYLD Analysis (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CPYLD	.224	53	1,2	M	Assumed for 5%
DMULT	218233.58	11	1	H/3	PRICE M Output
DMULT	208743.83	23	1	H/3	PRICE M Output
DMULT	4352.4096	31	2	H/3	PRICE M Output
DMULT	208743.83	43	2	H/3	PRICE M Output
DMYLT	16.389492	53	1,2	H/3	PRICE M Output
OVLYLD	.05	11	1	M	5% Yield
OVLYLD	.05	23	1	M	5% Yield
OVLYLD	.05	31	2	M	5% Yield
OVLYLD	.05	43	2	M	5% Yield
OVLYLD	.05	53	1,2	M	5% Yield

TABLE XLIII

Changes to Default Values for 10% OVLYLD Analysis

Variable Name	Value	ij	Case	Model/ File or Mode	Source
ASMYLD	.316	11	1	M	Assumed for 10%
ASMYLD	.316	23	1	M	Assumed for 10%
ASMYLD	.316	31	2	M	Assumed for 10%
ASMYLD	.316	43	2	M	Assumed for 10%
ASMYLD	.316	53	1,2	M	Assumed for 10%
AUC1	$317.00	11	1	H/3	PRICE M Output
AUC1	$170.50	23	1	H/3	PRICE M Output
AUC1	$129.40	31	2	H/3	PRICE M Output
AUC1	$ 98.20	43	2	H/3	PRICE M Output
AUC1	$ 64.96	53	1,2	H/3	PRICE M Output
CPYLD	.316	11	1	M	Assumed for 10%
CPYLD	.316	23	1	M	Assumed for 10%
CPYLD	.316	31	2	M	Assumed for 10%
CPYLD	.316	43	2	M	Assumed for 10%

TABLE XLIII

Changes to Default Values for 10% OVLYLD Analysis (Continued)

Variable Name	Value	ij	Case	Model/ File or Mode	Source
CPYLD	.316	53	1,2	M	Assumed for 10%
DMULT	282946.37	11	1	H/3	PRICE M Output
DMULT	260470.67	23	1	H/3	PRICE M Output
DMULT	6700.1546	31	2	H/3	PRICE M Output
DMULT	4354.3788	43	2	H/3	PRICE M Output
DMULT	31.734456	53	1,2	H/3	PRICE M Output
OVLYLD	.10	11	1	M	10% Yield
OVLYLD	.10	23	1	M	10% Yield
OVLYLD	.10	31	2	M	10% Yield
OVLYLD	.10	43	2	M	10% Yield
OVLYLD	.10	53	1,2	M	10% Yield

YIELD ANALYSIS SP, CP AND MEMORY CHIPS (1%, 5%, AND 10%)

PROGRAM COST ($ 1000.)

TITLE	ENGINEERING	PROTOTYPE	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-1%)	179360.	28.	1803.	181191.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-1%)	179360.	28.	1376.	180764.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-1%)	179360.	28.	862.	180249.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-1%)	179360.	28.	1432.	180819.
SIGNAL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-1%)	179360.	28.	1048.	180436.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-1%)	4303.	32.	1758.	6093.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-1%)	4303.	32.	1346.	5681.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-5%)	179360.	28.	822.	180210.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-5%)	179360.	28.	677.	180064.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-5%)	179360.	28.	442.	179829.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-5%)	179360.	28.	661.	180048.
SIGNAL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-5%)	179360.	28.	540.	179927.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-5%)	4303.	32.	996.	5331.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-5%)	4303.	32.	746.	5081.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-10%)	179360.	28.	634.	180021.

TITLE	ENGINEERING	PROTOTYPE	PRODUCTION	TOTAL COST
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-10%)	179360.	28.	536.	179924.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-10%)	179360.	28.	354.	179741.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-10%)	179360.	28.	512.	179899.
SIGNAL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-10%)	179360.	28.	433.	179820.
SIGNAL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-10%)	4303.	32.	647.	4982.
SIGNAL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-10%)	4303.	32.	554.	4889.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-1%)	177613.	28.	3304.	180945.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-1%)	177613.	28.	2575.	180216.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-1%)	177613.	28.	1623.	179264.
CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-1%)	177613.	28.	2652.	180293.
CONTROL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-1%)	177613.	28.	2227.	179868.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-1%)	4244.	32.	3254.	7530.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-1%)	4244.	32.	2493.	6769.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-5%)	177613.	28.	1550.	179191.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-5%)	177613.	28.	1298.	178939.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-5%)	177613.	28.	851.	178492.

TITLE	ENGINEERING	PRPTOTYPE	PRODUCTION	TOTAL COST
CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-5%)	177613.	28.	1256.	178897.
CONTROL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-5%)	177613.	28.	1173.	178814.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-5%)	4244.	32.	1872.	6147.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-5%)	4244.	32.	1404.	5680.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR 3D/STL (YIELD ANALYSIS-10%)	177613.	28.	1203.	178844.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR ISL/CML (YIELD ANALYSIS-10%)	177613.	28.	1032.	178673.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (YIELD ANALYSIS-10%)	177613.	28.	682.	178323.
CONTROL PROCESSOR VHSIC CHIP-CMOS/SOS (YIELD ANALYSIS-10%)	177613.	28.	978.	178619.
CONTROL PROCESSOR VHSIC CHIP-NMOS (YIELD ANALYSIS-10%)	177613.	28.	939.	178580.
CONTROL PROCESSOR VHSIC CHIP-BIPOLAR STL (GA:YIELD ANALYSIS-10%)	4244.	32.	1141.	5417.
CONTROL PROCESSOR VHSIC CHIP-CMOS/BULK (GA:YIELD ANALYSIS-10%)	4244.	32.	982.	5257.
VHSIC MEMORY CHIP-NMOS (YIELD ANALYSIS-1%)	53775.	1681.	7397475.	7452930.
VHSIC MEMORY CHIP-CMOS/BULK (YIELD ANALYSIS-1%)	53775.	2029.	6314254.	6370057.
VHSIC MEMORY CHIP-NMOS (YIELD ANALYSIS-5%)	53775.	1681.	3617787.	3673243.
VHSIC MEMORY CHIP-CMOS/BULK (YIELD ANALYSIS-5%)	53775.	2029.	3404992.	3460795.
VHSIC MEMORY CHIP-NMOS (YIELD ANALYSIS-10%)	53775.	1681.	1868391.	1923846.
VHSIC MEMORY CHIP-CMOS/BULK (YIELD ANALYSIS-10%)	53775.	2029.	1758493.	1814297.

COST SUMMARY CASE 1, YIELD ANALYSIS 1%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL (ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412833.	6317773.	6730605.
SUBTOTAL (MFG)	412975.	6353805.	6766780.
TOTAL COST	413221.	6357701.	6770922.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413183.	6353179.	6766361.
CENTER	413221.	6357701.	6770922.
TO	413272.	6362754.	6776025.

```
***********************************************************************
* SYSTEM WT                  241.36          SYSTEM WS          105.80  *
* SYSTEM SERIES MTBF HRS.    510             AV SYSTEM COST     6358    *
***********************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425116.	6357701.	6782817.

LCC OF SAR PROCESSOR (CASE 1:YIELD ANALYSIS-1%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S1Y1.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	6248102	***	6673218
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	850625	5616329	6466954
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	425116	7136849	5678963	13240928

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

COST SUMMARY CASE 1, YIELD ANALYSIS-5%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL (ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412833.	3406537.	3819370.
SUBTOTAL (MFG)	412975.	3442570.	3855545.
TOTAL COST	413221.	3446465.	3859687.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413183.	3441943.	3855125.
CENTER	413221.	3446465.	3859687.
TO	413272.	3451519.	3864790.

```
************************************************************************
* SYSTEM  WT                  241.36         SYSTEM  WS        105.80  *
* SYSTEM SERIES MTBF HRS.     510            AV SYSTEM COST    3446    *
************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425116.	3446465.	3871582.

LCC OF SAR PROCESSOR (CASE 1:YIELD ANALYSIS-5%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S1Y5.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	3388439	***	3813555
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	461097	3044009	3505106
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	425116	3887658	3106643	7419417

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

COST SUMMARY CASE 1, YIELD ANALYSIS-10%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	48.	41.	89.
DESIGN	155.	145.	300.
SYSTEMS	17.	-	17.
PROJ MGMT	20.	2724.	2744.
DATA	6.	985.	992.
SUBTOTAL(ENG)	246.	3896.	4142.
MANUFACTURING			
PRODUCTION	-	35556.	35556.
PROTOTYPE	128.	-	128.
TOOL-TEST EQ	15.	478.	492.
PURCH ITEMS	412832.	1759756.	2172587.
SUBTOTAL(MFG)	412974.	1795789.	2208763.
TOTAL COST	413220.	1799685.	2212905.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	413182.	1795162.	2208344.
CENTER	413220.	1799685.	2212905.
TO	413271.	1804738.	2218009.

****

* SYSTEM WT	241.36	SYSTEM WS	105.80	*
* SYSTEM SERIES MTBF HRS.	510	AV SYSTEM COST	1800	*

****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
425115.	1799685.	2224800.

LCC OF SAR PROCESSOR (CASE 1:YIELD ANALYSIS-10%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S1Y10.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	510	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	425116	1772023	***	2197139
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	241287	1590012	1831299
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	2062	2062
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1772	1772
TOTAL COST	425116	2051432	1652646	4129194

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9924

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.811	0.000	0.000
LOAD FACTOR	0.394	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	118	18	332
BALANCE CONSUMED	687.60	0.00	4515.019

COST SUMMARY CASE 2,YIELD ANALYSIS 1%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	42.	54.	96.
DESIGN	140.	188.	328.
SYSTEMS	19.	-	19.
PROJ MGMT	18.	2855.	2874.
DATA	7.	1039.	1046.
SUBTOTAL (ENG)	226.	4136.	4362.
MANUFACTURING			
PRODUCTION	-	36001.	36001.
PROTOTYPE	125.	-	125.
TOOL-TEST EQ	14.	477.	491.
PURCH ITEMS	64415.	6318598.	6383012.
SUBTOTAL (MFG)	64554.	6355074.	6419629.
TOTAL COST	64780.	6359212.	6423991.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	64744.	6354778.	6419521.
CENTER	64780.	6359212.	6423991.
TO	64829.	6364130.	6428959.

```
***************************************************************************
* SYSTEM  WT                   241.38           SYSTEM  WS        105.80  *
* SYSTEM SERIES MTBF HRS.      530              AV SYSTEM COST    6359    *
***************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
76675.	6359212.	6435886.

LCC OF SAR PROCESSOR CASE 2 (YIELD ANALYSIS-1%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S2Y1.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	76675	6248503	***	6325178
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	819903	5438466	6258369
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	76675	7106528	5500957	12684160

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

COST SUMMARY CASE 2 YIELD ANALYSIS 5%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST ($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	42.	54.	96.
DESIGN	140.	188.	328.
SYSTEMS	19.	-	19.
PROJ MGMT	18.	2855.	2874.
DATA	7.	1039.	1046.
SUBTOTAL (ENG)	226.	4136.	4362.

MANUFACTURING			
PRODUCTION	-	36001.	36001.
PROTOTYPE	125.	-	125.
TOOL-TEST EQ	14.	477.	491.
PURCH ITEMS	64415.	3407264.	3471679.
SUBTOTAL (MFG)	64554.	3443742.	3508296.
TOTAL COST	64780.	3447878.	3512658.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	64744.	3443444.	3508188.
CENTER	64780.	3447878.	3512658.
TO	64829.	3452797.	3517625.

```
************************************************************************
* SYSTEM  WT                 241.38          SYSTEM  WS          105.80  *
* SYSTEM SERIES MTBF HRS.    530             AV SYSTEM COST      3448    *
************************************************************************
```

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
76675.	3447878.	3524553.

LCC OF SAR PROCESSOR CASE 2 (YIELD ANALYSIS-5%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S2Y5.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	76675	3388156	***	3464831
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	444605	2948855	3393460
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	76675	3870883	3011346	6958904

OPERATIONAL AVAILABILITY 0.9997   OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

COST SUMMARY CASE 2 YIELD ANALYSIS 10%

TOTAL COST, WITH INTEGRATION COST

PROGRAM COST($ 1000)	DEVELOPMENT	PRODUCTION	TOTAL COST
ENGINEERING			
DRAFTING	42.	54.	96.
DESIGN	140.	188.	328.
SYSTEMS	19.	-	19.
PROJ MGMT	18.	2855.	2874.
DATA	7.	1039.	1046.
SUBTOTAL(ENG)	226.	4136.	4362.
MANUFACTURING			
PRODUCTION	-	36001.	36001.
PROTOTYPE	125.	-	125.
TOOL-TEST EQ	14.	477.	491.
PURCH ITEMS	64415.	1760096.	1824511.
SUBTOTAL(MFG)	64554.	1796573.	1861128.
TOTAL COST	64780.	1800710.	1865490.

COST RANGES	DEVELOPMENT	PRODUCTION	TOTAL COST
FROM	64744.	1796276.	1861020.
CENTER	64780.	1800710.	1865490.
TO	64829.	1805629.	1870458.

****

* SYSTEM WT	241.38	SYSTEM WS	105.80	*
* SYSTEM SERIES MTBF HRS.	530	AV SYSTEM COST	1801	*

****

THRU-PUT COSTS	DEVELOPMENT	PRODUCTION	TOTAL COST
SOFTWARE	11895.	0.	11895.
TOTAL THRU-PUT COST	11895.	0.	11895.

TOTAL COST, WITH THRU-PUT COSTS

DEVELOPMENT	PRODUCTION	TOTAL COST
76675.	1800710.	1877385.

LCC OF SAR PROCESSOR CASE 2 (YIELD ANALYSIS-10%)

GLOBAL FILENAME: GLOB.95
LIFE CYCLE FILENAME: S2Y10.LC
DEPLOYMENT FILENAME: SAR.DP

MTBF	530	MTTR-LRU	1.8	MOD TYPES/LRU	68	LRUS/EQUIP	1
RATIO (1)	1.00	-MODULE	3.6	PART TYPES/LRU	3	LRU FAIL ALLOW	0
RATIO (2)	1.00						
RATIO (3)	1.00						

PROGRAM COST	DEVELOPMENT	PRODUCTION	SUPPORT	TOTAL
EQUIPMENT	76675	1769814	***	1846489
SUPPORT EQUIPMENT	***	38037	57055	95092
SUPPLY	***	232643	1540271	1772914
SUPPLY ADMIN.	***	85	1745	1830
MANPOWER	***	***	1985	1985
CONTRACTOR SUPPORT	***	***	0	0
OTHER	0	***	1706	1706
TOTAL COST	76675	2040579	1602762	3720016

OPERATIONAL AVAILABILITY 0.9997 OPERATIONAL READINESS 0.9930

SUPPORT EQUIPMENT	ORG	INT	DEPOT
NUMBER OF SETS	10	0	0
UTILIZATION	11.371	0.000	0.000
LOAD FACTOR	0.379	0.000	0.000

SUPPLY	UNITS	MODULES/TYPE	PARTS/TYPE
INITIAL	114	17	321
BALANCE CONSUMED	661.63	0.00	4345.692

Bibliography

1. Bennett, John J. "Comment," Defense Management Journal, 12: 1-4 (January 1976).

2. Blanchard, Benjamin S. Logistics Engineering and Management. Englewood Cliffs NJ: Prentice-Hall, Inc., 1978.

3. Blasingame, John M. "Very High Speed Integrated Circuits (VHSIC)," Program Management Review Presented to ASD/CC, VHSIC Program Office, Wright-Patterson AFB OH, September 1983. Unnumbered.

4. Brannon, Phil. "VHSIC - Can It Clear the Third Hurdle?" Journal of Electronic Defense, 6: 18-22 (November 1983).

5. Carter, Harold. Preliminary Investigation of the Life Cycle Costs of a Digital Avionics Processor Using Very High Speed Integrated Circuits. Student Research Report, No. 0460-81. Air Command and Staff College, Maxwell AFB AL, June 1981 (AD-B057 618).

6. Coleman, Herbert J. "Weapons Maintainability Guidance Sought by GAO," Aviation Week and Space Technology, 116: 90-91 (16 February 1981).

7. Collins, Dwight E. Analysis of Available Life Cycle Cost Models and Actions Required to Increase Future Model Applications. Technical Report ASD-TR-75-25. Joint AFSC/AFLC Commanders' Working Group on Life Cycle Cost, Wright-Patterson AFB OH, December 1974 (AD-A014 772).

8. Demarco, Anthony and W. Kenneth Witzgall. "The Economics of Choosing a Custom Microcircuit Approach," Proceedings of the IEEE 1983 National Aerospace and Electronics Conference NAECON. 1027-1031. IEEE Press, New York, 1983.

9. Department of the Air Force. Life Cycle Cost Management Program. AFR 800-11. Washington: HQ USAF, 22 February 1978.

10. Department of Defense. Major System Acquisition Process. DoD Directive 5000.2. Washington: Government Printing Office, 1983.

11. Department of Defense. Major System Acquisition Process. DoD Directive 5000.28. Washington: Government Printing Office, 1975.

12. Earl, Don. "Techniques for a Multifaceted Discipline," Defense Management Journal, 12: 38-47 (January 1976).

13. Ferens, Daniel V. "Preliminary Life Cycle Analysis for the Solid State Phased Array Antenna and VHSIC Processor." Report to AFWAL/CC. Avionic Laboratory, Wright-Patterson AFB OH, 1983.

14. Fox, Ronald J. Arming America. Cambridge: Harvard University Press, 1974.

15. Gordon, Harvey. Acquisition Improvement Program (AIP). Second Year-End Report. Acquisition Improvement Program Steering Group, Defense Systems Management College, Fort Belvoir VA, May 1983.

16. Guerra, Joel A., et al. An Operating and Support Cost Model for Avionics Automatic Test Equipment. MS thesis, LSSR 21-79B. School of Systems and Logistics, Air Force Institute of Technology (AU), Wright-Patterson AFB OH, September 1979 (AD-A075 586).

17. Hunt, Saadia Y. "Life Cycle Cost Models Reference Guide." Report to Directorate of Cost Analysis, Comptroller. Wright-Patterson AFB OH, April 1983.

18. Kabaservice, Thomas P. Applied Microelectronics. St Paul: West Publishing Co., 1978.

19. Kennerly, David H. "The Winds of Reform," Time, 121 (59): 12-30 (7 March 1983).

20. Kernan, John E., and Lavern J. Menker. Life Cycle Cost Procurement Guide. Joint AFSC/AFCC Commander's Working Group on Life Cycle Cost ASD/ACL, Wright-Patterson AFB OH, July 1976.

21. Klass, Philip J. and B. Elson. "Technical Survey: Very High Speed Integrated Circuits," Aviation Week and Space Technology, 114: 48-85 (16 Feburary 1981).

22. Klass, Philip J. "Retrofit Sought for High-Speed Circuits," Aviation Week and Space Technology, 117: 114-115 (21 September 1981).

23. Long, John A. Life Cycle Costing in a Dynamic Environment. PhD dissertation. School of Industrial and Systems Engineering, Ohio State University, Columbus OH, 1983 (AD-A133 023).

24. May, Thomas E. Operating and Support Cost Estimating, A Primer. Report to Directorate of Cost Analysis, Comptroller, ASD/ACCL, Wright-Patterson AFB OH, May 1982.

25. McNichols, Gerald R. On the Treatment of Uncertainty in Parametric Costing. PhD dissertation. School of Engineering and Applied Science, George Washington University, Washington DC, February 1976 (AD-A022 153).

26. Oldham, William G. "The Fabrication of Microelectronic Circuits," Scientific American, 237 (3): 111-128 (September 1977).

27. "Pentagon Mulls VHSIC Applications," Aero Space Daily, 11: 338 (August 1983).

28. PRICE Hardware Reference Manual, Revision 3. RCA PRICE SYSTEMS, Cherry Hill NJ, January 1982.

29. PRICE Life Cycle Cost Reference Manual, Revision 2. RCA PRICE SYSTEMS, Cherry Hill NJ, May 1983.

30. PRICE Microcircuit Reference Manual, Revision 3. RCA PRICE SYSTEMS, Cherry Hill NJ, March 1984.

31. Reed, Ronald P. Long Range Logistics Planning for Very High Speed Integrated Circuit Components. MS thesis, NPS-54-81-021. Naval Post Graduate School, Monterey CA, December 1981 (AD-A115 181).

32. Scherrer, John D. Life Cycle Costing - QMT-353. Unpublished course material. Air Force Institute of Technology, School of Systems and Logistics, Wright-Patterson AFB OH, September 1976.

33. Schlag, Jay. "Technologies and Design Tools in Microelectronics," Journal of Electronic Defense, 6: 46-49 (November 1983).

34. "Second Tri-Service Workshop On Manufacturing Technology Program Planning for VHSIC Technology." Final Report. Air Force Wright Aeronautical Laboratory, Materials Laboratory, Manufacturing Technology Division, Wright-Patterson, AFB OH, 14-15 October 1982.

35. Speicher, Patricia S. and Eugene C. Blackburn. "VHSIC Contractors Face Packaging Challenges," Hybrid Circuit Technology, 1: 51-55 (January 1984).

36. Sumney, Larry W. VHSIC and Defense Technology. Unpublished Program Description. Director, VHSIC Program, Office of Under Secretary of Defense for Research and Development, Washington DC, October 1980.

37. Sumney, Larry W. "VHSIC: A Status Report," IEEE Spectrum, 12: 34-39 (December 1982).

38. "Technology - A Quick Switch for Military Uses," Science News, 123: 203 (26 March 1983).

39. Walker, John. "VHSIC Insertion into the APG-66 PSP," Presentation to the USAF Scientific Advisory Board. Westinghouse Defense And Electronic Systems Center, Baltimore MD, August 1982.

VITA

Captain Enzo A. Long was born on 1 September 1947 in Clovis, New Mexico. He graduated from Clovis High School in 1966 and attended New Mexico State University from which he received the degree of Bachelor of Science in Mathematics in 1974. Upon graduation, he received a commission in the USAF through the ROTC program. His Air Force assignments have included a total of six years as Minuteman ICBM Crew Member, Wing Evaluator, and Missile Operations Instructor at Minot AFB, North Dakota and Vandenberg AFB, California. His last assignment prior to entering the School of Systems and Logistics in 1983 was Chief, Central Data Facility for the Ground Launch Cruise Missile (GLCM) Initial Operational Test and Evaluation Test Team at Dugway Proving Ground, Utah.

Permanent address: 913 West Yucca Drive
Clovis, New Mexico 88101

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) AFIT/GLM/LSM/84S-39	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION School of Systems and Logistics 6b. OFFICE SYMBOL (If applicable) AFIT/LS	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code) Air Force Institute of Technology Wright-Patterson AFB, Ohio 45433	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code)	10. SOURCE OF FUNDING NOS. PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT NO.
11. TITLE (Include Security Classification) See Box 19	

12. PERSONAL AUTHOR(S)
Enzo A. Long, B.S., Captain, USAF

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Yr., Mo., Day)	15. PAGE COUNT
MS Thesis	FROM ______ TO ______	1984 September	240

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB. GR.	Life Cycle Costs, Integrated Circuits, Semiconductors, Very High Speed Integrated Circuits (VHSIC) Microcircuits, Chips (Electronics)
15	05		

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Title: LIFE CYCLE COST MODEL FOR VERY HIGH SPEED INTEGRATED CIRCUITS

Thesis Chairman: Rodney C. Byler, Major, USAF

Approved for public release: IAW AFR 190-1.
11 Sept 84
Dean for Research and Professional Development
Air Force Institute of Technology (ATC)
Wright-Patterson AFB OH 45433

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code)	22c. OFFICE SYMBOL
Rodney C. Byler, Major, USAF	513-255-5023	AFIT/LSM

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

The Very High Speed Integrated Circuit (VHSIC) technology program is forecast to have a profound impact on performance, reliability, and cost of future avionics systems. An important question is: "how do VHSIC design fabrication and support concepts impact life cycle cost (LCC) of a host system?" To answer this question, an insertion model representative of future avionics systems is selected and LCCs are obtained for various chip designs and layout configurations which implement this model. Five factors affecting VHSIC chips ~~are examined~~ with respect to LCC of a digital synthetic aperture radar processor. These factors are: (1) chip technology and design; (2) fabrication yields; (3) substrate type; (4) the degree to which computer-aided-design (CAD) methods are used; and (5) maintenance level. Of these factors, the greatest impact to LCC is chip fabrication yields. The least effect on LCC is the degree to which CAD methods are used. The remaining factors fall between these two.

Originator-supplied Keywords include: Semiconductors, Microcircuits, and Chips (Electronics).

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

END

FILMED

1-85

DTIC