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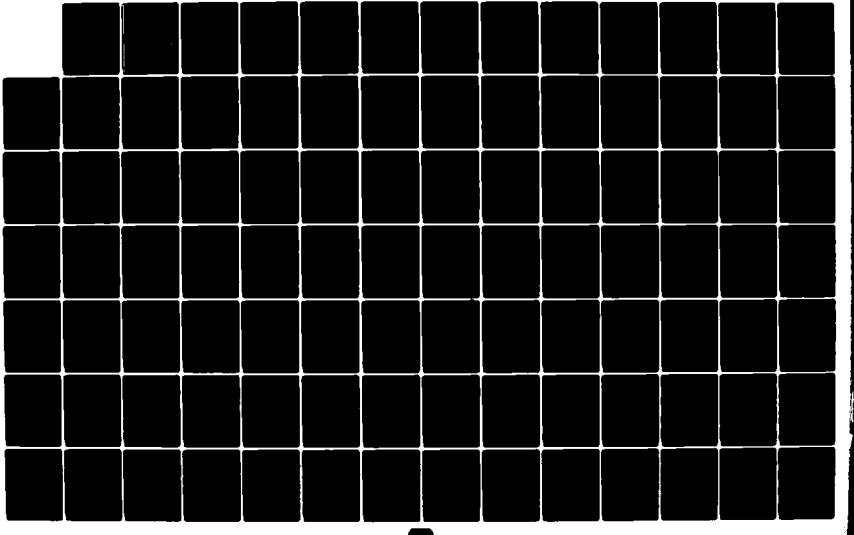

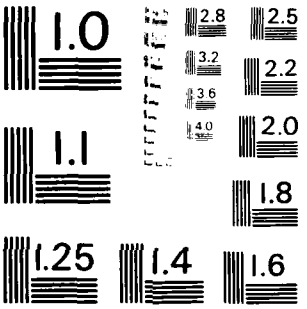

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ZERO-IF RECEIVER STUDY

FINAL TECHNICAL REPORT

CDRL NO. A003

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ZERO-IF RECEIVER STUDY

CONTRACT NO. DAAK80-81-C-0154

REVISED EDITION

PREPARED BY

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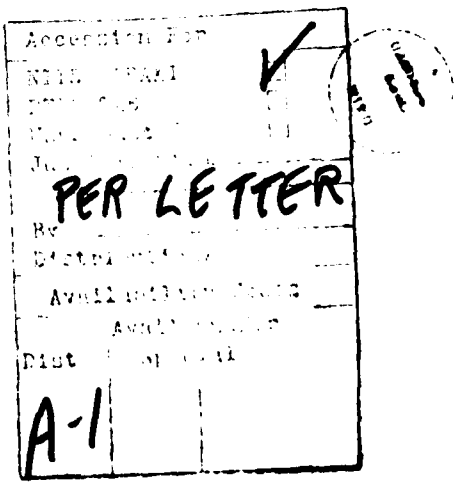

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Section 1

INTRODUCTION

The Zero-IF Receiver Study was performed to design and fabricate a breadboard model of a Zero-IF receiver with both analog and digital techniques. The value of this Zero-IF architecture will be fully realized when the low frequency circuits inherent in a Zero-IF system are reduced to one or two LSI circuits. In today's LSI technology, in which complete synthesizer subsystems may be integrated on a single chip (less voltage controlled oscillator and crystal reference), the receiver becomes the transceiver subassembly that has the greatest need for unique size reduction techniques. This Zero-IF technique, when applied to the design of small hand-held FM transceivers, offers distinct advantages with respect to size and weight reduction. Not only can the "IF" and demodulator be integrated, but this receiver architecture places reduced requirements on the receiver preselector filters.

In typical available transceivers, the receiver occupies one-third or less of the volume of the transceiver. The rest of the package contains a synthesizer and transmitter. Hand-held transceivers normally employ relatively low-power transmitters (five watts or less) because of practical battery limitations. These transmitters, therefore, are relatively small and are not the major size limiting subassemblies of hand-held transceiver systems. The larger portions of the receiver are normally the receiver preselector and the IF crystal filter.

A Zero-IF receiver design is basically a form of superheterodyne design in which the receiver local oscillator operates at the same frequency as the RF signal. For a frequency modulation system based on the Zero-IF principle, all of the gain and signal processing after mixing is accomplished at audio frequencies. The RF gain required is only that necessary to maintain noise figure for desired receiver sensitivity. The primary advantage of this type of design is that the majority of receiver gain and subsequent signal demodulation and signal processing are done at audio frequencies. With today's integrated circuit technology, much of this audio circuitry can be converted to digital circuitry and processed with highly producible large scale integration (LSI); this leads to lower cost receiver-transmitter designs. Other advantages for this type of receiver design are as follow:

- No stringent attenuation requirements on the RF section of the receiver to meet the image response requirement of a conventional design.
- Synthesizer-controlled, variable-frequency oscillator (VFO) can function directly as both the receiver local oscillator and as the transmitter exciter without changing frequency. Only modulation must be introduced to perform the transmit function.

In a Zero-IF receiver system, the local oscillator signal is at the same frequency as the incoming RF signal. Therefore, the preselector provides no attenuation of the local oscillator signal. The problem of high local oscillator radiation in a Zero-IF system is solved through the use of high reverse isolation RF amplifier design techniques. The local oscillator attenuation achieved with these RF amplifiers, when added to that of the double-balanced mixers, will reduce the local oscillator radiation to less than -73 dBm.

Both the analog and digital Zero-IF breadboard met or exceeded all of its performance goals and the other program objectives.

Section 2

TECHNICAL OBJECTIVES AND PROGRAM REQUIREMENTS

The objective of the Zero-IF Receiver Study was to fabricate a breadboard model of a Zero-IF receiver to illustrate the feasibility and performance of this design concept. Initially, a complete receiver system was designed, breadboarded, and tested with a phase-locked-loop (PLL) Zero-IF demodulator. After the successful completion of this effort, a digital demodulator was designed and fabricated. The digital demodulator was fabricated on a sub-chassis that plugged into the original PLL receiver. During this study, emphasis was placed on FM Zero-IF demodulator techniques, however, a complete receiver was fabricated to demonstrate what performance could be achieved with a Zero-IF system and to compare these results with a conventional superhetrodyne receiver such as the AN/PRC-68. The preselector, RF ampilfier, and mixer circuits were of a conventional design such as that used on many ITT programs. The deliverable breadboard uses a signal generator as a local oscillator.

2.1 DESIGN SPECIFICATIONS AND PROGRAM DESCRIPTION

The Zero-IF receiver breadboard was designed to meet the specifications shown below in Table 2.1-1. These specifications were considered design goals inasmuch as the Zero-IF system represents a novel approach to receiver design. Each was met or exceeded.

Table 2.1-1. Zero-IF Specifications (Design Goals)

Sensitivity (10 dB SINAD)	-113 dBm
Adjacent Channel Rejection	70 dB
Selectivity (6 dB down)	> 16 kHz
Spurious Responses	-60 dB
Local Oscillator Radiation	<-73 dBm

This program resulted in the development and demonstration of both an analog and digital demodulation systems.

2.2 TECHNICAL APPROACH

At the beginning of the program, a complete Zero-IF receiver was designed. The demodulator section used a PLL demodulator. This receiver was tested and met the goals set for it. The PLL demodulator section was then put aside, and a digital demodulator was designed. The receiver was again tested, and again met the goals set

for it. Figure 2.2-1 is a general block diagram of the breadboarded receiver. It consists of the receiver front end, IF filters, IF Amplifiers, the demodulator, and audio circuits.

2.2.1 Preselector Filters

The block labeled as number 1 in Figure 2.2-1 represents the preselector filters. The requirements of the preselector filters for a Zero-IF receiver are similar to the requirements of the filters for an up-converter. That is, the filters need only be designed to suppress third-order mixing products to ensure sufficient attenuation for all order products. These filters usually have a bandwidth of one half octave. Therefore, only three filters are required to cover the 30 to 88 MHz band. Several versions of RF band filters were checked out. A combination low pass and high pass was chosen because a band-pass filter yielded undesirable component values. In addition, the low pass - high pass combination is more desirable for future transceiver applications in which the transmit path includes only the low pass filter. Figure 2.2.1-1 is a block diagram of the preselector. In the figure, the switches shown represent PIN diodes which are controlled by the band select switch on the front panel of the radio. Note on the schematic, page A-2 of Appendix A, each filter has a PIN diode on both its input and its output. A -15 Vdc level is forced on the PIN diodes when a particular band is not desired. This dc level causes the diode to be reverse biased and, therefore, effectively no signals are passed in that particular band. The selected band, on the other hand, has a +11 Vdc level forced on it because the voltage divider consists of the 10 K and 1.5 K resistors. The positive dc level forward biases the diodes on the selected band, thereby enabling the signals in this band to be passed on to the RF gain/attenuator stage. Tables 2.2.1-1 through 2.2.1-3 are lists of the filter responses for the three bands - 30-43 MHz, 43-62 MHz, and 62-88 MHz. Figures 2.2.1-2 through 2.2.1-4 are plots of the data.

2.2.2 RF Amplifier and RF AGC Circuits

The block labeled as number 2 in Figure 2.2-1 represents the RF amplifier and RF AGC circuits. These circuits contain two hybrid amplifiers (Part numbers QBH-102 and QBH-104 from Q-bit Corp.) and a PIN diode attenuator. Figure 2.2.2-1 is a block diagram of the RF Amplifier attenuator board. Schematics of these circuits can be found in Appendix A. Page A-3 is a schematic of the RF amplifier and attenuator, while Page A-4 is a schematic of the RF attenuator control logic. Each amplifier has 12 dB of gain. The PIN diode attenuator has 48 dB of attenuation and is controlled by the baseband AGC circuits. Table 2.2.2-1 shows the amount of attenuation of each step for three different frequencies. Without this attenuator, the maximum on-channel input signal that the receiver can handle without distortion is -40 dBm. With the addition of this circuit and the RF gain control, the receiver is able to operate with signals up to 0 dBm. It has been designed in a bridge-T configuration which maintains a good VSWR (better than 2:1) for all levels of attenuation. This is most impor-

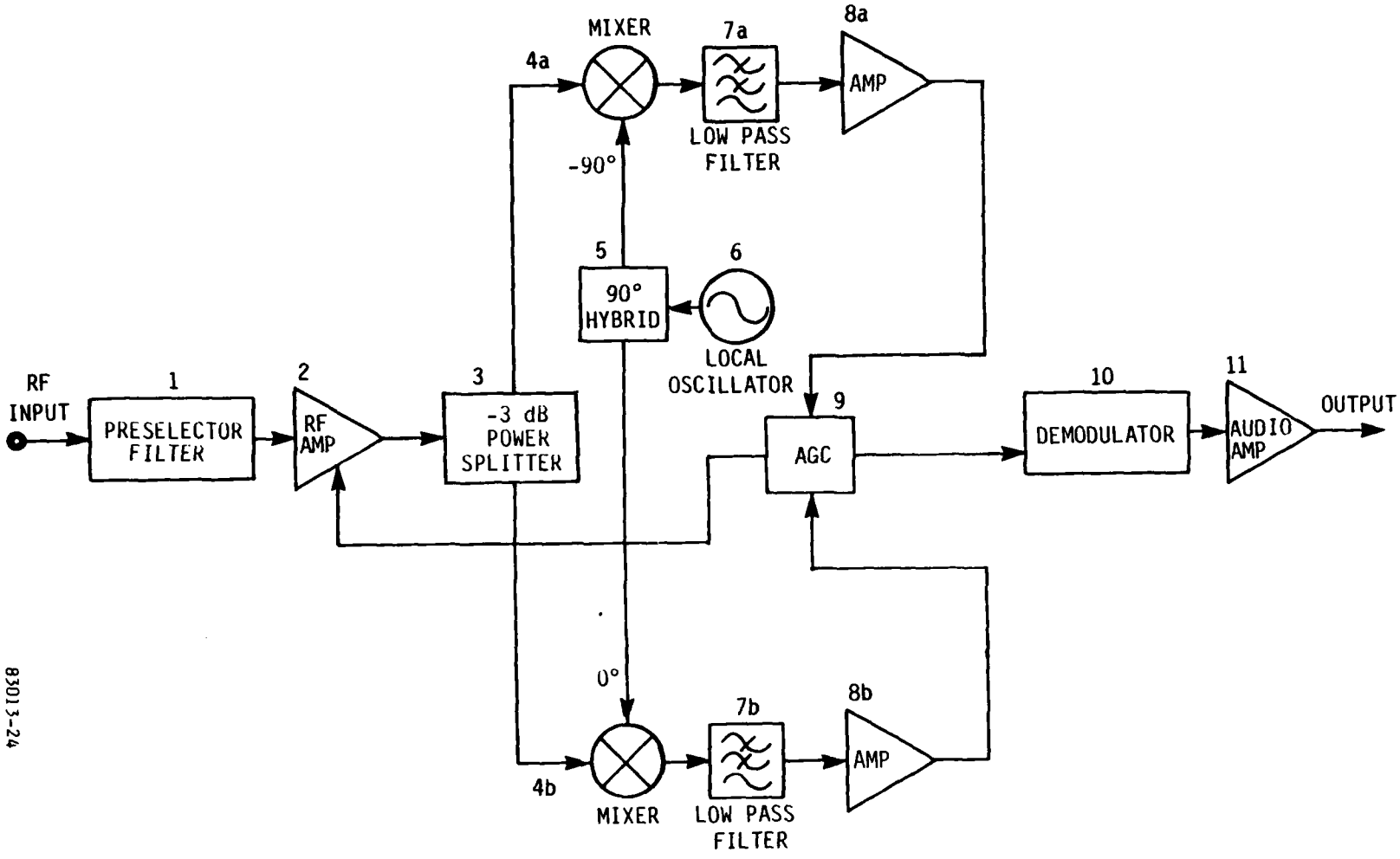


Figure 2.2-1. Breadboard Block Diagram

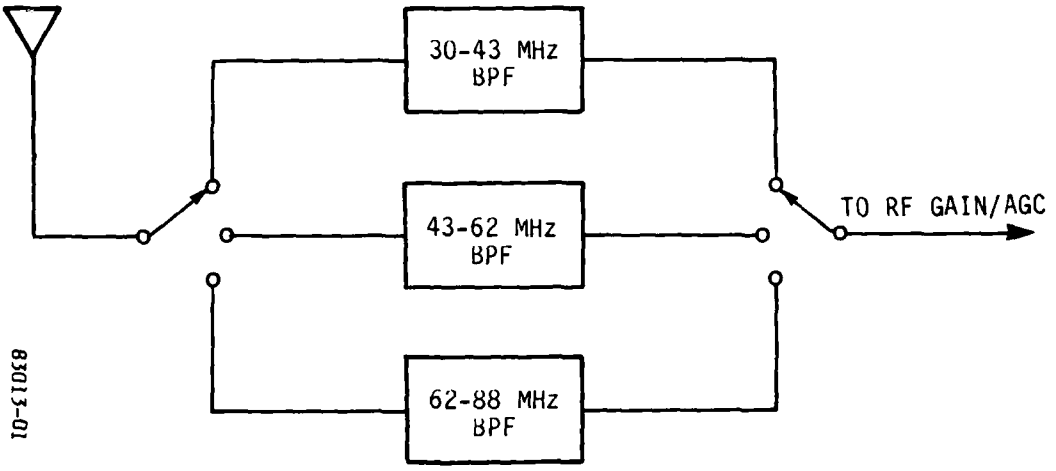


Figure 2.2.1-1. Block Diagram of Preselector Bandpass Filters

Table 2.2.1-1. 30-43 MHz Preselector Filter Response

Frequency (MHz)	Filter Response (dB)
3.000	-46.80
7.000	-41.80
12.000	-48.70
18.000	-55.20
22.000	-25.30
27.000	-4.00
32.000	-1.30
36.000	-1.50
41.000	-1.30
46.000	-6.70
51.000	-18.70
56.000	-34.50
60.000	-46.40
65.000	-40.80
69.000	-41.40
74.000	-44.90
84.000	-47.40
89.000	-50.30
94.000	-53.40
98.000	-56.80
103.000	-60.60
107.000	-64.60
112.000	-66.40

Table 2.2.1-2. 43-66 MHz Preselector Filter Response

Frequency (MHz)	Filter Response (dB)
3.000	-49.60
8.000	-42.20
12.000	-41.80
18.000	-46.80
23.000	-56.60
27.000	-51.30
32.000	-28.00
36.000	-8.70
41.000	-1.20
46.000	-1.00
51.000	-1.40
56.000	-1.40
61.000	-1.00
65.000	-1.30
70.000	-5.50
74.000	-13.50
79.000	-22.20
84.000	-31.00
89.000	-41.70
94.000	-62.50
98.000	-48.80
103.000	-46.40
108.000	-46.00
112.000	-46.50

Table 2.2.1-3. 62-88 MHz Preselector Filter Response

Frequency (MHz)	Filter Response (dB)
3.000	-54.40
8.000	-46.20
12.000	-44.10
17.000	-44.70
22.000	-49.50
27.000	-65.60
32.000	-44.80
36.000	-39.30
41.000	-39.10
46.000	-38.20
51.000	-17.60
56.000	-5.20
61.000	-1.10
65.000	-1.20
70.000	-1.60
74.000	-1.50
79.000	-1.20
84.000	-1.10
89.000	-1.50
93.000	-2.60
99.000	-7.60
103.000	-16.40
108.000	-26.10
112.000	-38.80

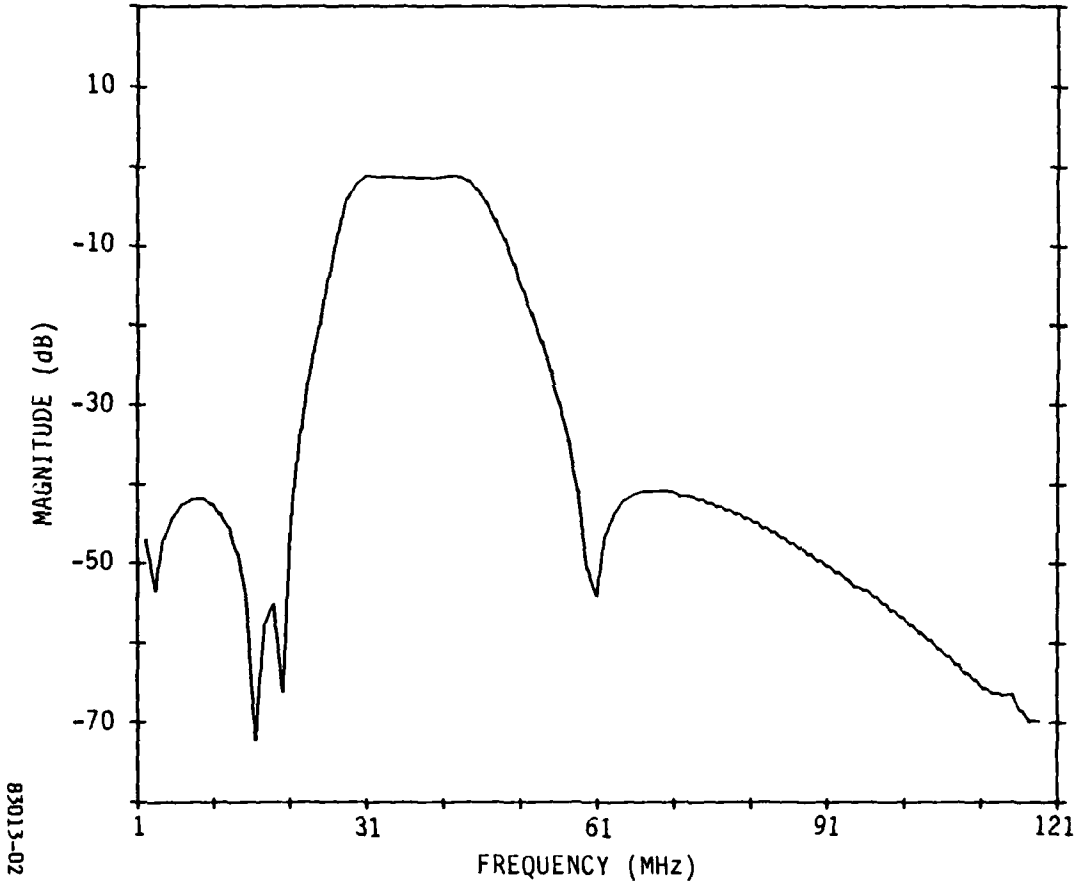


Figure 2.2.1-2. Zero-IF Preselector Filter Band 1

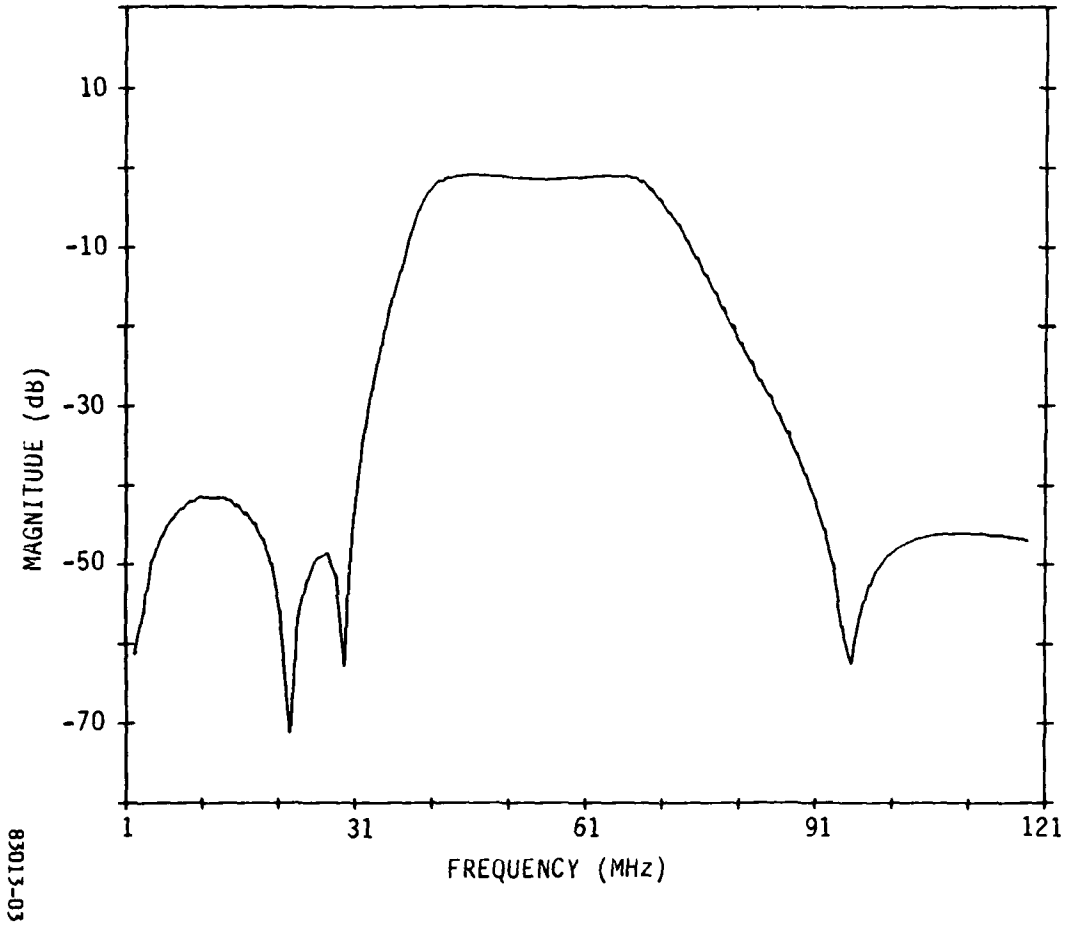


Figure 2.2.1-3. Zero-IF Preselector Filter Band 2

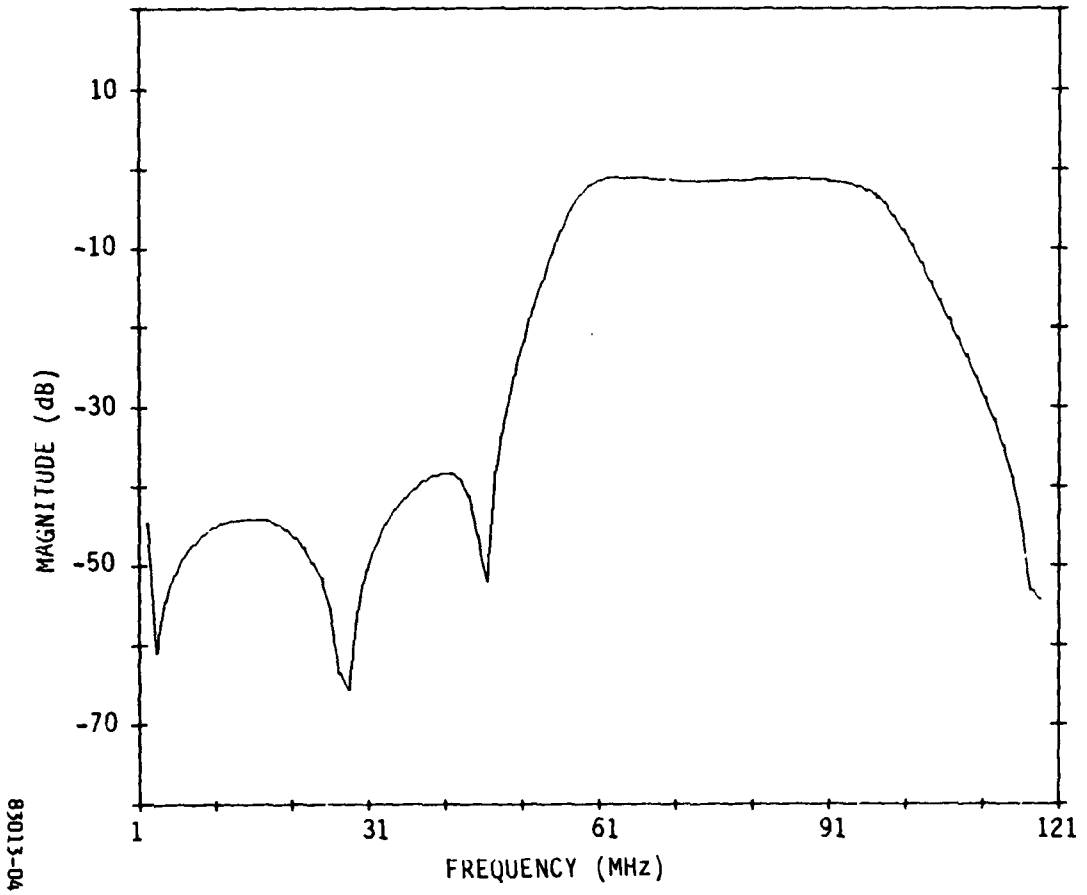


Figure 2.2.1-4. Zero-IF Preselector Filter Band 3

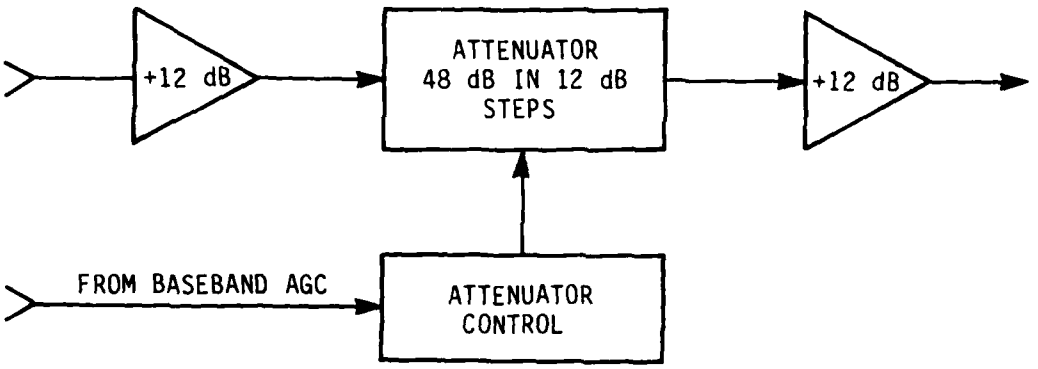


Figure 2.2.2-1. Block Diagram of RF Amplifier Attenuator Board

tant at the 0 dB attenuation setting because any loss under low signal conditions will add to the noise figure of the receiver. The attenuator control logic controls the PIN diode attenuator. It is an extension of the baseband AGC circuit and consists of a shift register which steps the PIN diode attenuator in four 12 dB steps. This process does not begin until the baseband AGC reaches its maximum attenuation and, therefore, the receiver noise figure is not degraded except at high signal inputs where noise figure is not a concern. For more detail on how this circuit operates, see section 2.2.7.

Table 2.2.2-1. RF Amplifiers with PIN Diode Attenuator

Conditions: -20 dBm input from HP8640 signal generator and output terminated by 50 ohm load of Boonton RF voltmeter.

Attenuation Step	30 MHz		59 MHz		88 MHz	
	Output Level (dBm)	Amount of Atten. (dB)	Output Level (dBm)	Amount of Atten. (dB)	Output Level (dBm)	Amount of Atten. (dB)
0	2.9	-	2.7	-	2.6	-
1	-9.4	12.3	-9.6	12.3	-9.6	12.2
2	-21.6	24.5	-21.8	24.5	-21.6	24.2
3	-33.0	35.9	-32.4	35.1	-30.8	33.4
4	-44.0	46.9	-43.5	46.2	-40.0	42.6

2.2.3 Signal Splitter Circuit

The blocks labeled 3, 4a and 4b in Figure 2.2-1 comprise the signal splitter circuit. The signal splitter circuit consists of a power splitter and two mixers. The primary concern was to match signal amplitude and phase in the two signal paths. A Merrimac (PDS-20-50) power splitter and two Mini-Circuits (MCLSBL-1) mixers are the parts selected for this circuit. Figure 2.2.3-1 is a block diagram of the splitter/mixer circuit. A schematic of this circuit can be found on page A-5 of the Appendix. In the circuit, the -3 dB power splitter (block 3) splits the desired signal into two in-phase signals. These signals are then mixed with the two quadrature signals from the local oscillator circuit described in section 2.2.4. The output of each mixer (blocks 4a and 4b) is a baseband signal along with a signal whose frequency is twice the local oscillator frequency. The undesired signal, that signal which is at twice the local oscillator frequency, is then filtered out using the baseband filter described in section 2.2.5.

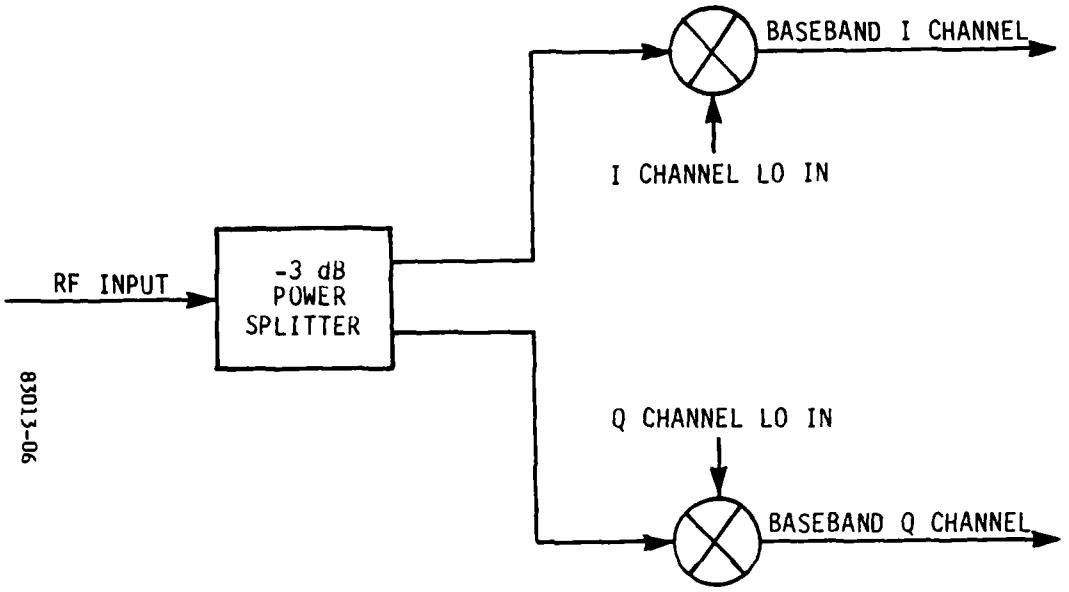


Figure 2.2.3-1. Block Diagram of Splitter/Mixers

2.2.4 Quadrature LO Circuit

The block labeled number 5 in Figure 2.2-1 is a 90 degree power splitter/combiner. This is an off-the-shelf part which is used to provide the two quadrature local oscillator (LO) signals. Block number 6 represents an RF signal generator external to the breadboard which is used as the LO. By running the LO through the splitter/combiner, two quadrature signals are generated that are then supplied to the mixers shown in the schematic of the signal splitter circuit on page A-5 of the Appendix. An Anzac part (JH-131) was selected to perform the function of block number 5.

2.2.5 Baseband Filter

The channel bandwidth is defined by the baseband filters. The baseband filters are passive with a cutoff frequency of 8 kHz. In Figure 2.2-1, they are represented by blocks 7a and 7b. The schematic for this circuit can be found on page A-6 in the Appendix. note that these filters are seven-pole filters. It was necessary to use a seven-pole filter in order to achieve an adjacent channel attenuation of 70 dB. The component values for these filters were carefully calculated and the final circuit is composed of close tolerance parts (one percent) selected to be as close as possible to the calculated values so that both filters are identical. Table 2.2.5-1 shows the frequency response of this circuit. Figure 2.2.5-1 is a plot of this data.

2.2.6 Low-Noise Amplifier

The blocks labeled as numbers 8a and 8b in Figure 2.2-1 represent the low noise amplifier for each channel. Figure 2.2.6-1 is a block diagram of the circuit. A schematic can be found on page A-7 in Appendix A. The first stage of the low-noise amplifier is a 1:40 step-up transformer. A low-noise op-amp follows the transformer. The frequency response of this circuit was adjusted to decrease the noise bandwidth. The modifications consisted of adjusting the compensation capacitor on the first amplifier and adjusting the feedback (gain) of the second active filter stage. Note the power supply lines are also filtered. Figure 2.2.6-1 is a block diagram of the low noise amplifier. Table 2.2.6-1 is a table of the frequency response of this circuit. Figure 2.2.6-2 is a plot of the data.

2.2.7 Baseband AGC

The block labeled as number 8 in Figure 2.2-1 represents the baseband AGC circuits. As shown in the schematic on page A-8 of the Appendix, the baseband AGC circuits are made up of a digital step attenuator followed by a compression amplifier. The digital step attenuator switches in or out attenuation in 6-dB steps, depending on the rectifier/detector circuitry. When all eight steps (48 dB) are switched on, a "carry out" bit goes to the RF attenuator control logic. When the rectifier/detector indicates more attenuation is necessary, the RF attenuation is used in the same manner. When the

Table 2.2.5-1. Channel Filter Frequency Response

Frequency (Hz)	Amplitude Response Channel 1 (dB)	Amplitude Response Channel 2 (dB)
5	-1.2	-1.3
10	-1.5	-1.6
50	-1.4	-1.5
100	-1.4	-1.5
500	-1.4	-1.5
1 K	-1.2	-1.3
2 K	-.6	-.7
3 K	0	-.1
4 K	0	0
5 K	-.4	-.5
6 K	-1.2	-1.3
7 K	-1.7	-1.8
7.5 K	-1.5	-1.6
8 K	-1.5	-1.6
8.5 K	-1.7	-1.8
9 K	-2.7	-3.3
9.5 K	-4.7	-5.4
10 K	-7.8	-7.7
10.5 K	-9.8	-10.7
11 K	-13.5	-14.2
12 K	-18.6	-18.9
13 K	-22.8	-23.3
14 K	-26.6	-27.3
15 K	-30.6	-31.3
20 K	-46.6	-46.9
25 K	-63.2	-53
27.9 K	-70.4	-80.5
29 K	-77.4	-76.8
31 K	-72.6	-72.5
32.6 K	-71.4	-71.5
35 K	-71.5	-71.5
40 K	-76.3	-76.3
45 K	-81.6	-81.5

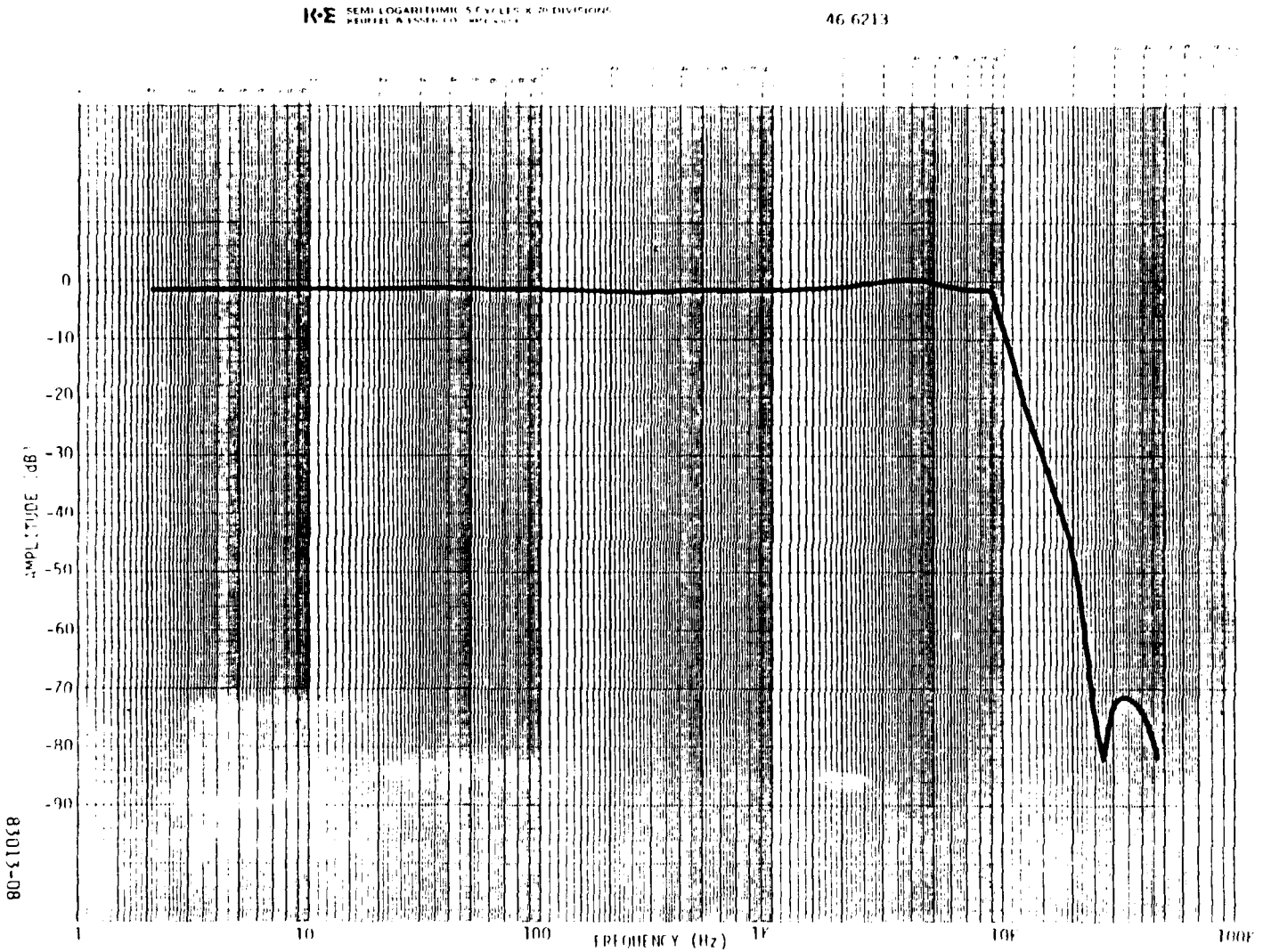


Figure 2.2.5-1. Frequency Response of Baseband Filter

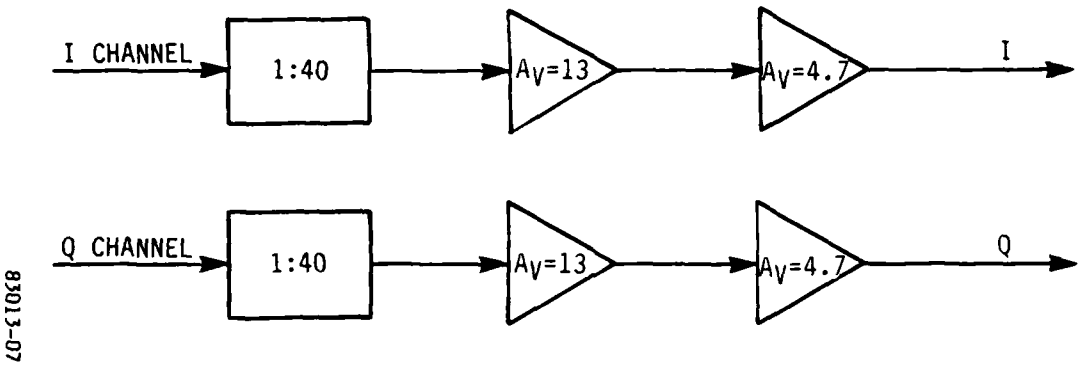


Figure 2.2.6-1. Block Diagram of the Low-Noise Amplifier

Table 2.2.6-1. Frequency Response Zero-IF Receiver Low Noise Amp Input Voltage = 3 mV_{rms}.

Frequency (Hz)	Output Voltage (V_{rms})	dB (1 kHz)
5	6.1	-.5
10	6.3	-.3
50	6.4	-.1
100	6.4	-.1
400	6.5	0
1K	6.5	0
2K	6.4	-.1
3K	6.3	.3
4K	6.2	.5
5K	5.9	-1.0
6K	5.6	-1.4
7K	5.2	-2.0
8K	4.9	-2.6
9K	4.4	-3.5
10K	4.2	-4.0
15K	2.8	-7.6
20K	2.0	-10.4
30K	1.75	-15.7
50K	.195	-30.6

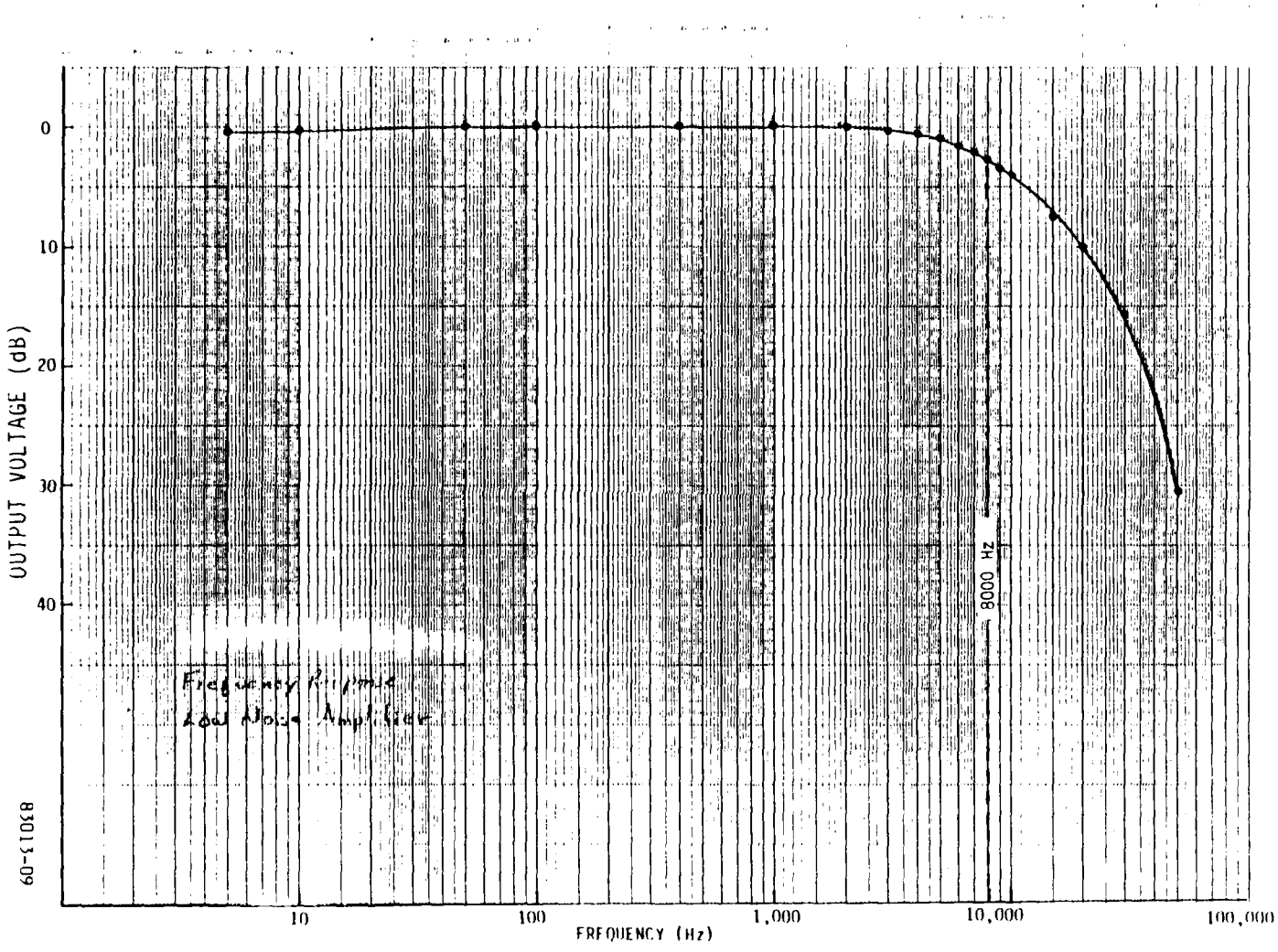


Figure 2.2.6-2. Low Noise Amplifier Frequency Response

rectifier/detector indicates less attenuation is necessary, attenuation is switched off in exactly the reverse order that it was switched on. In other words, if a starting point of no attenuation on is used, the least significant bit of attenuation is switched in and more as necessary. When less attenuation is needed, the most significant bit that was switched in is then switched out down to the least significant bit. The attenuation control logic also disables itself whenever the rectifier/detector indicates more attenuation is necessary and all attenuation is switched on, or whenever the indication is for less attenuation and all attenuation is switched off. Furthermore, the rectifier/detector has a window of 18 dB to ensure that the AGC circuit does not bounce between two steps of attenuation. In addition, the compression amplifier provides a constant level output for the variances that will occur with signal level variances not exactly equal to one step of attenuation. Overall, the AGC circuits provide 116 dB of attenuation, 48 dB at RF and 48 dB at baseband in step attenuation with 20 dB in the compression amplifier. Figure 2.2.7-1 is a block diagram of this circuit.

2.2.8 Demodulator

Block number 9 in Figure 2.2-1 represents the demodulator. Section 3 is a discussion on the analog demodulator. Section 4 covers the digital demodulator. Please refer to these sections for information on the demodulation processes.

2.2.9 Audio Circuits

The final section contains the audio circuit, which is represented by block number 10 in Figure 2.2-1. As shown in the schematic on page A-11 of the appendix, the audio circuits are made up of a low-pass, high-pass filter and a speaker amplifier. The filter section creates a bandpass (3 dB) from 350 Hz to 3 kHz, and the speaker amplifier delivers 1/2 Watt to an 8-ohm speaker. A block diagram of the audio circuit board is shown in Figure 2.2.9-1. Table 2.2.9-1 is a set of frequency response data for this circuit. Figure 2.2.9-2 is a plot of the data. Table 2.2.9-2 is a set of data showing the distortion of the audio filters.

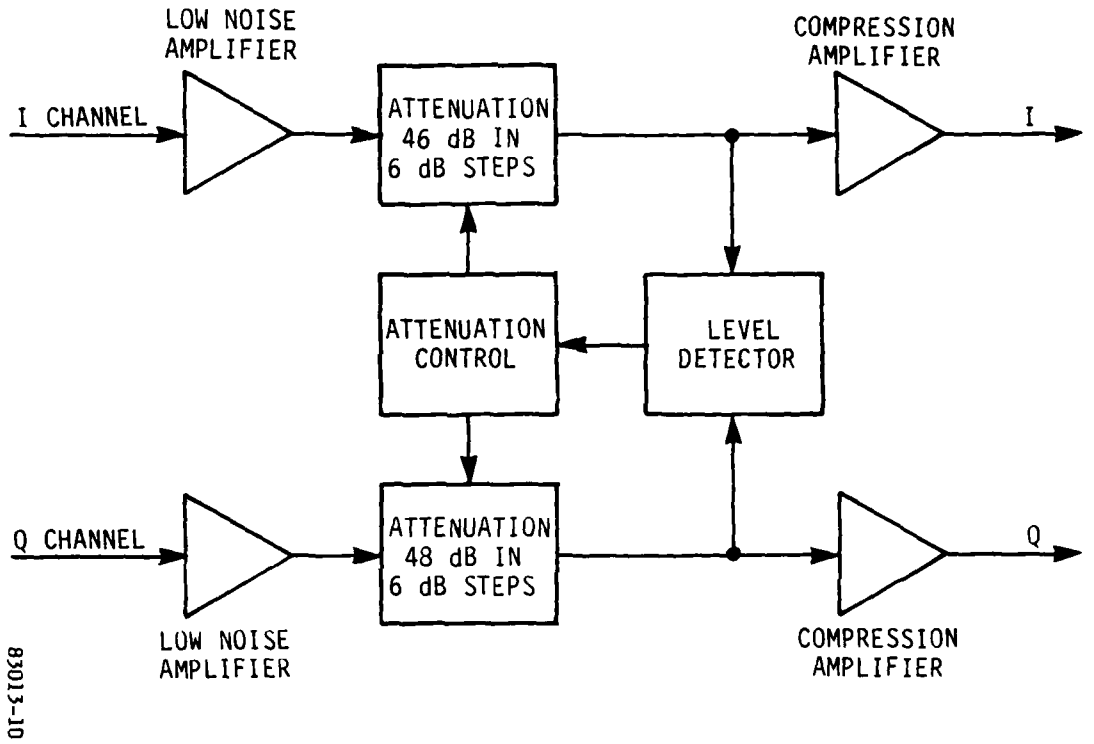


Figure 2.2.7-1. Block Diagram of Baseband AGC

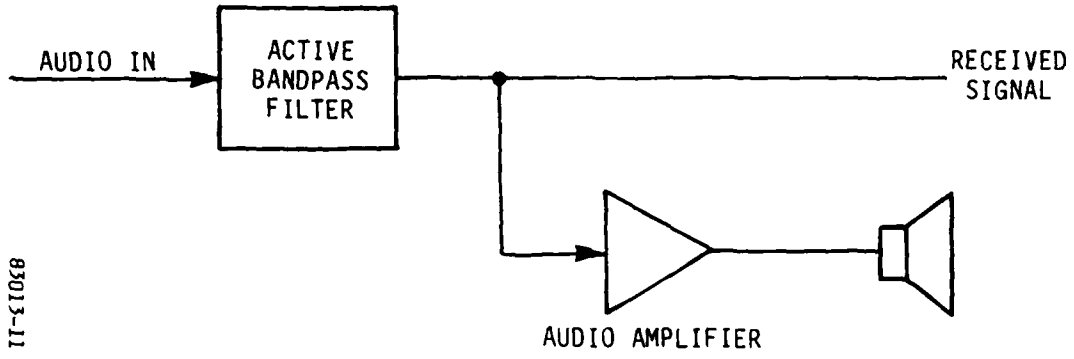


Figure 2.2.9-1. Block Diagram of Audio Circuits

Table 2.2.9-1. Frequency Response of Audio Filters
Input Voltage = 0.66 mV_{rms},

Frequency (Hz)	Output Voltage (V_{rms})	dB
5	0.72 mV	-68.9
10	2.26 mV	-58.9
20	11.0 mV	-45.2
30	27 mV	-37.4
40	52 mV	-31.7
50	84 mV	-27.5
60	0.125	-24.1
70	0.17	-21.4
80	0.23	-18.8
90	0.295	-16.6
100	0.362	-14.8
120	0.54	-11.4
150	0.82	-7.7
175	1.075	-5.4
200	1.32	-3.6
300	1.875	-0.6
400	2.00	-0.0
500	2.00	-0.0
1K	1.95	-0.2
2K	1.875	-0.6
3K	1.55	-2.2
4K	1.06	-5.5
5K	0.74	-8.6
6K	0.51	-11.7
7K	0.38	-14.4
8K	0.29	-16.8
9K	0.23	-18.8
10K	0.185	-20.7
15K	0.085	-27.4
20K	0.051	-31.7
30K	0.026	-37.7

Table 2.2.9-2. Percent of Distortion of Audio Filters

Output Frequency	THD (%)
300 Hz	0.245
1K Hz	0.158
3K Hz	0.044

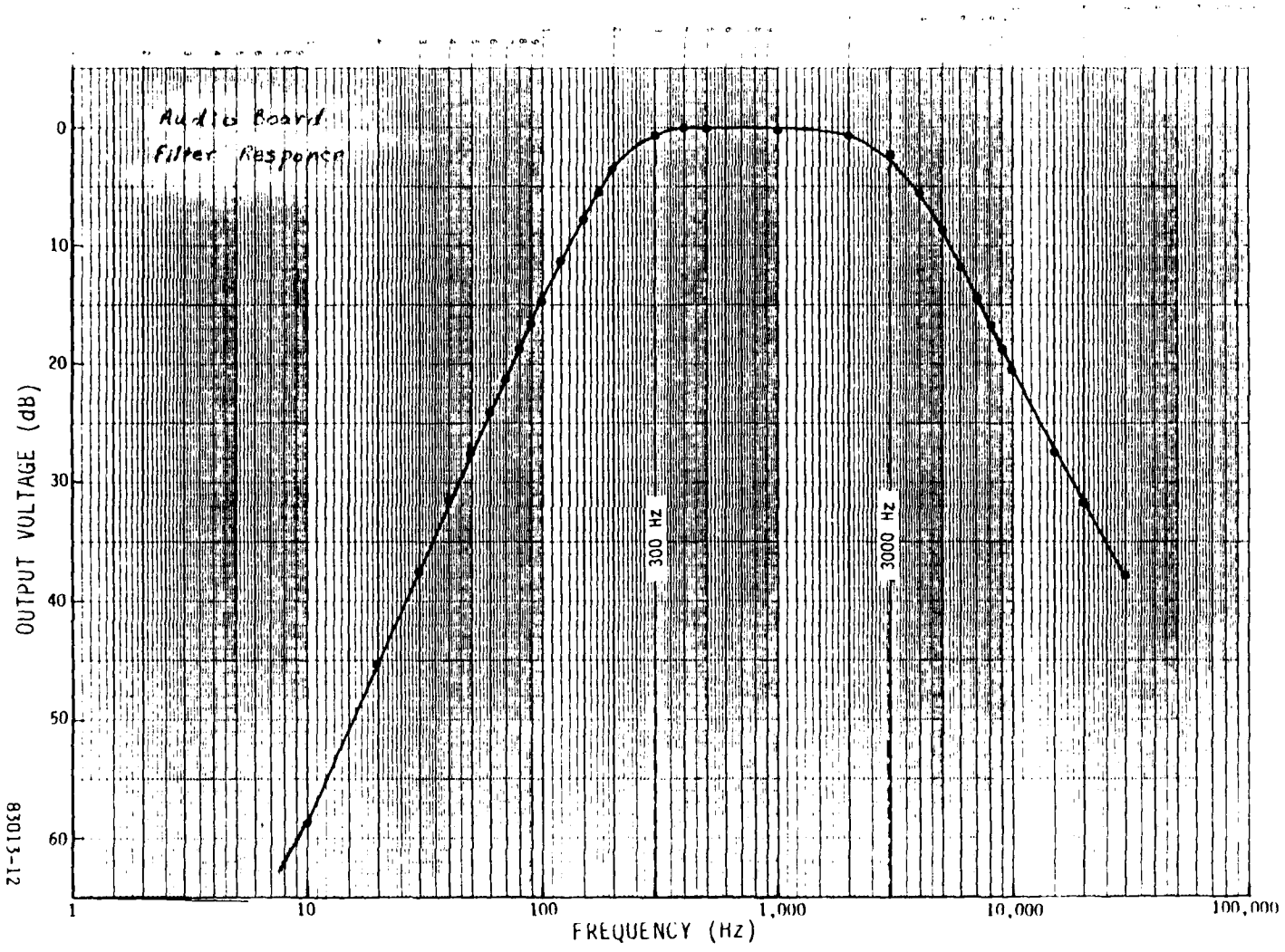


Figure 2.2.9-2. Zero-IF Receiver Audio Board Filter Response

Section 3

ANALOG DEMODULATOR

In an FM demodulation system using the Zero-IF concept, the RF carrier and double-sideband modulation spectrum are linearly translated to zero IF frequency by an asynchronous local oscillator (at the same frequency of the RF carrier). This causes the lower sideband of the RF signal to be folded over exactly on top of the upper sideband at the IF frequency. This folding of the RF spectrum requires some form of novel processing to demodulate the overlapping baseband information.

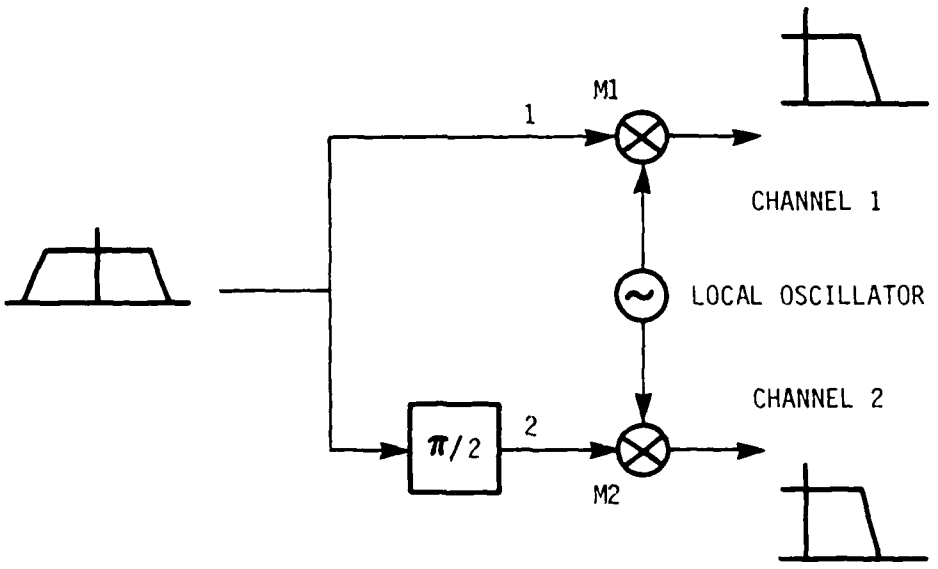
This superposition of sidebands can be resolved by using two quadrature baseband IF channels, each covering the frequency range of zero (dc) to half the original RF channel bandwidth. See Figure 3-1. A decision as to the original position of the RF signal relative to the local oscillator reference can be made by comparing the phase of the signals in the two channels. When the frequency modulated RF signal is higher in frequency than the local oscillator, the two signal phasors at points (1) and (2) will be rotating faster than the local oscillator reference phase. When they are translated to baseband by the local oscillator, which affects both in a similar way, the signal in channel (1) will lead that in channel (2) by $\pi/2$ radians. When the RF signal is lower in frequency than the local oscillator, the two RF phasors (1) and (2) are rotating slower than the local oscillator reference and, therefore, channel (1) will lag channel (2) by $\pi/2$ radians.

The two quadrature baseband signals are then filtered to remove the upper sideband of the mixing process (approximately twice the local oscillator frequency) and to define the noise bandwidth of the receiver.

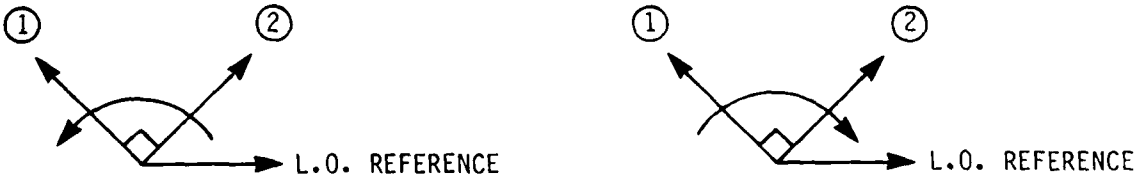
A frequency discriminator is connected to the output of these two filtered baseband channels; this produces a dc voltage with a magnitude proportional to the frequency that the slowly moving RF carrier has deviated from the local oscillator and a polarity determined by the relative phase of the two baseband channels.

Originally, a sine-cosine frequency discriminator was proposed for the Zero-IF receiver study. The sine-cosine demodulator is a classical design that is relatively easy to analyze and understand. Figure 3-2 is a block diagram of the sine-cosine demodulator. It consists of two differentiators, two linear four-quadrant multipliers, and a summing network.

The operation of this sine-cosine discriminator can be visualized by considering the RF carrier to be initially higher than the local oscillator frequency by $\delta\omega$. Figure 3-2 shows an instantaneous view of these signals. Note that channel (1) leads channel (2). The output from differentiator (1) is equal to channel (2), but



(A) Filter Bandwidths



RF SIGNAL HIGHER IN FREQUENCY THAN L.O.

RF SIGNAL LOWER IN FREQUENCY THAN L.O.

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(B) Phasor Diagrams

Figure 3-1. Filter Bandwidth and Phasor Diagram

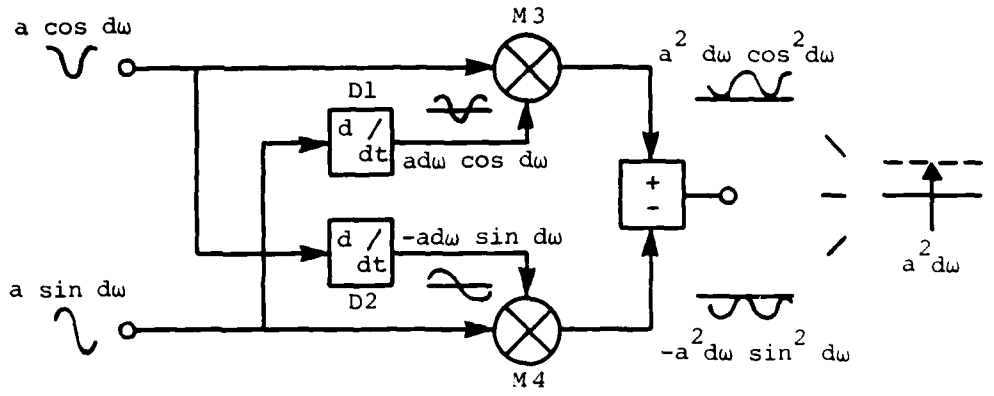

Figure 3-2. Demodulator Output (Positive Output)

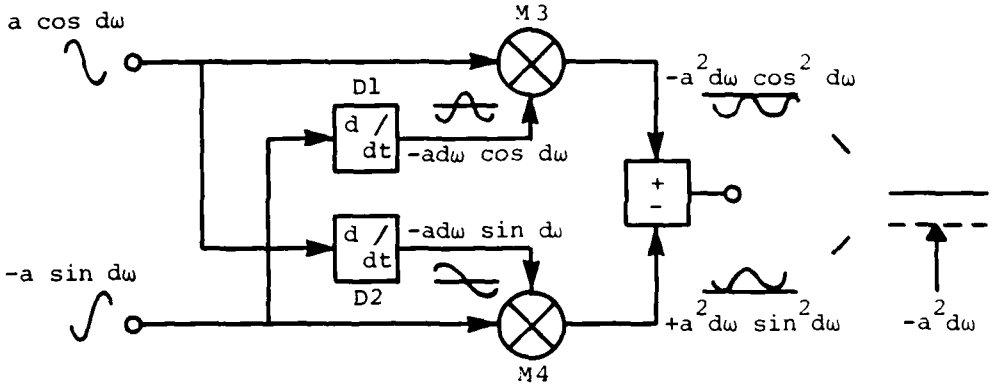

Figure 3-3. Demodulator Output (Negative Output)

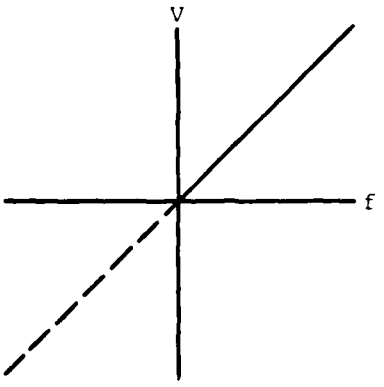

Figure 3-4. Discriminator Characteristic

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is phase shifted by $\pi/2$ with amplitude proportional to its frequency ($\delta\omega$). The output of differentiator (2) is similar. Multiplier M3 linearly multiplies its two inputs to produce an output at twice the input frequency which has an amplitude linearly proportional to the original input frequency ($\delta\omega$). The amplitude also depends upon the square of the original input signal level (a). Multiplier M4 produces a similar output of opposite polarity, lagging in phase by $\pi/2$.

Figure 3-2 shows that the combination of the two waveforms produces a dc voltage ($\cos^2 \delta\omega + \sin^2 \delta\omega = 1$) of amplitude proportional to $\delta\omega$, the original input frequency (difference frequency of RF and local oscillator) and to the square of the input amplitude. Figure 3-3 shows that the RF carrier is lower in frequency than the local oscillator by $\delta\omega$; the frequencies in the two channels are the same as in the previous case, but channel (2) now leads channel (1). The circuit performs as before, but it now generates a negative dc voltage. Figure 3-4 shows the complete discriminator characteristic.

Using these techniques to construct a practical FM receiver, it is necessary to include some means of maintaining a constant audio output level for widely varying input RF levels. An automatic gain control (AGC) circuit could be implemented at either RF or baseband. To minimize power consumption, the latter is preferred. Although this is an FM system, limiting amplifiers are not acceptable because the differentiators will produce spikes with amplitudes dependent only upon the slew-rate of the square waves (from the limiters) and not their frequency. This demodulation scheme is completed by adding a post-detection filter after the summer; the filter's sole function is to define the output noise bandwidth and not to reconstruct the modulation (Figure 3-5).

Although the sine-cosine demodulator is practically feasible, it was abandoned for the Phase-Locked-Loop (PLL) approach for analog demodulation at the beginning of the program. The PLL system was designed and breadboarded because it requires less accurate phase and amplitude balance between the I and Q channels and, because it is a feedback system, it has slightly better performance at low signal-to-noise ratios.

3.1 PHASE-LOCKED-LOOP DEMODULATOR

The phase-locked-loop (PLL) demodulator is actually quite similar to the sine-cosine demodulator. Figure 3.1-1 is a simplified block diagram of both the sine-cosine and PLL demodulators. Both demodulators cross multiply both channels by the derivative of the other channel. The Sine-Cosine demodulator derives this differentiated signal directly with a differentiator circuit, much as that used in analog computers. The PLL demodulator uses an indirect approach.

This is a Type 1 PLL, which consists of one integrater in the loop, which is the voltage controlled oscillator (VCO). The reference signal for this PLL is a free-running oscillator, at the same nominal frequency of the VCO. The mixed output of the VCO and the free-running

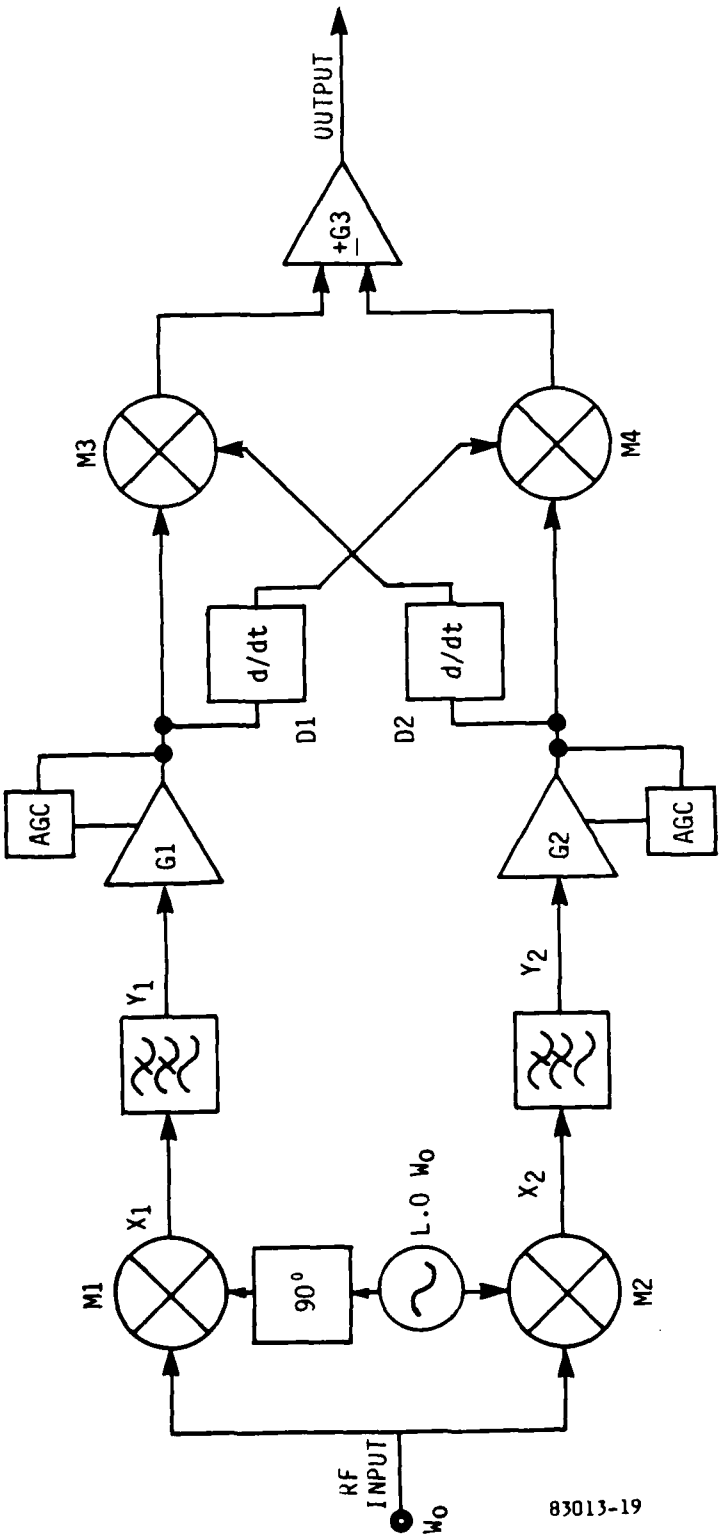

Figure 3-5. Basic Zero-IF System

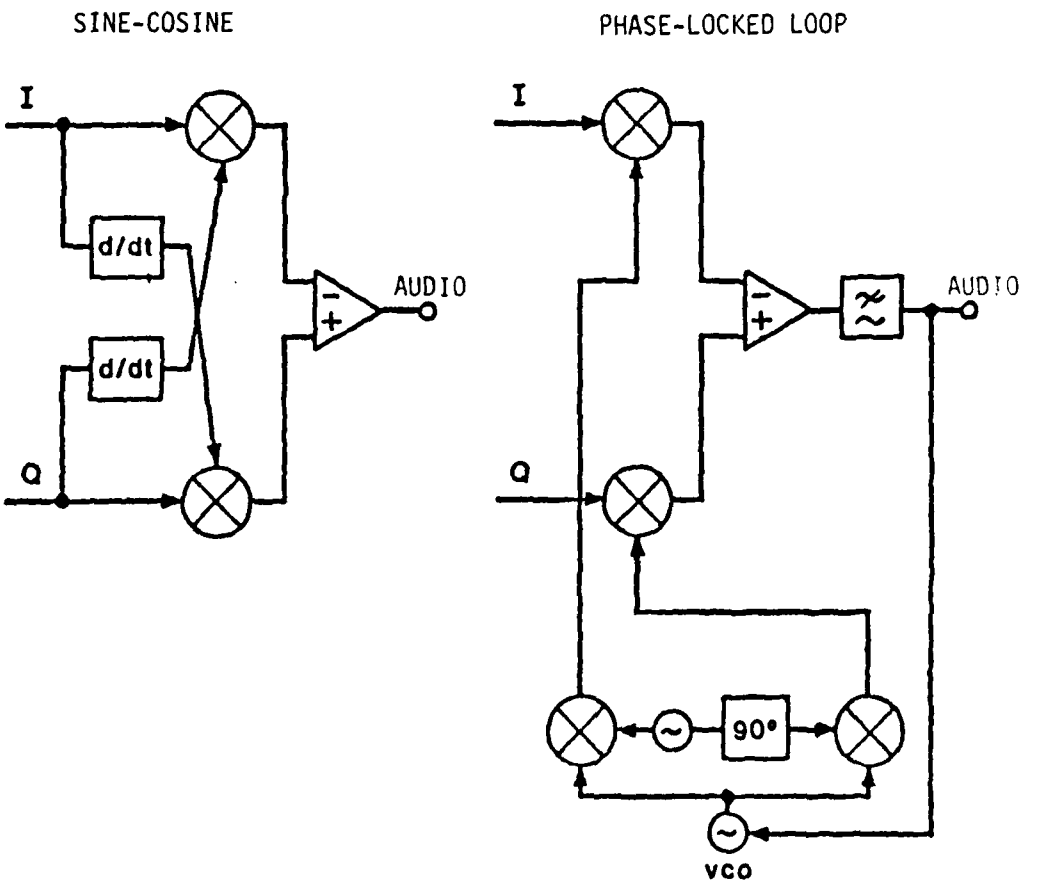

Figure 3.1-1. Analog Demodulators

oscillator with no modulation and no frequency error is a dc level. If modulation or a frequency error exists, these outputs are the derivatives of the I and Q channels as in the sine-cosine demodulator.

The PLL is a Type I (1 integrater) second order (2 poles) PLL. The characteristics of the desired response were derived by using techniques presented by Gardner in Phaselock Techniques, using the following equations.

ζ (PLL loop damping ratio) = 1

B_i (channel bandwidth) = 16 kHz

D (modulation index) = 1.66

ω_n(min) (min PLL natural frequency) =

$$\left(\frac{\pi B_i}{D+1}\right)\left[1 - 2\zeta^2 + \sqrt{(1-2\zeta)^2 + 1 + \frac{4D^2}{\pi^2}}\right]^{1/2}$$

or ω_n (min) = 103,555 radian

Figure 3.1-2 is a Bode plot of the open loop gain of the *phase-locked-loop demodulator.*

3.2 ANALYSIS OF PHASE-LOCKED-LOOP DEMODULATOR

Figure 3.2-1 is a general block diagram of the PLL demodulator. For analysis purposes, each of six mixers or multipliers are assumed to be ideal four quadrant linear multipliers. The following mathematical analysis describes the operation of the Zero-IF phased-locked-loop demodulator. As shown in Figure 3.2-1, the frequency modulated input signal is given by

$$S = A_c \text{COS}\left(\omega_c t + \frac{\Delta\omega}{\rho} \text{ SIN } \rho t\right)$$

where

A_c is the amplitude of the signal,

ω_c is the carrier frequency,

$\Delta\omega$ is the peak deviation, and

ρ is the frequency of the modulating audio signal.

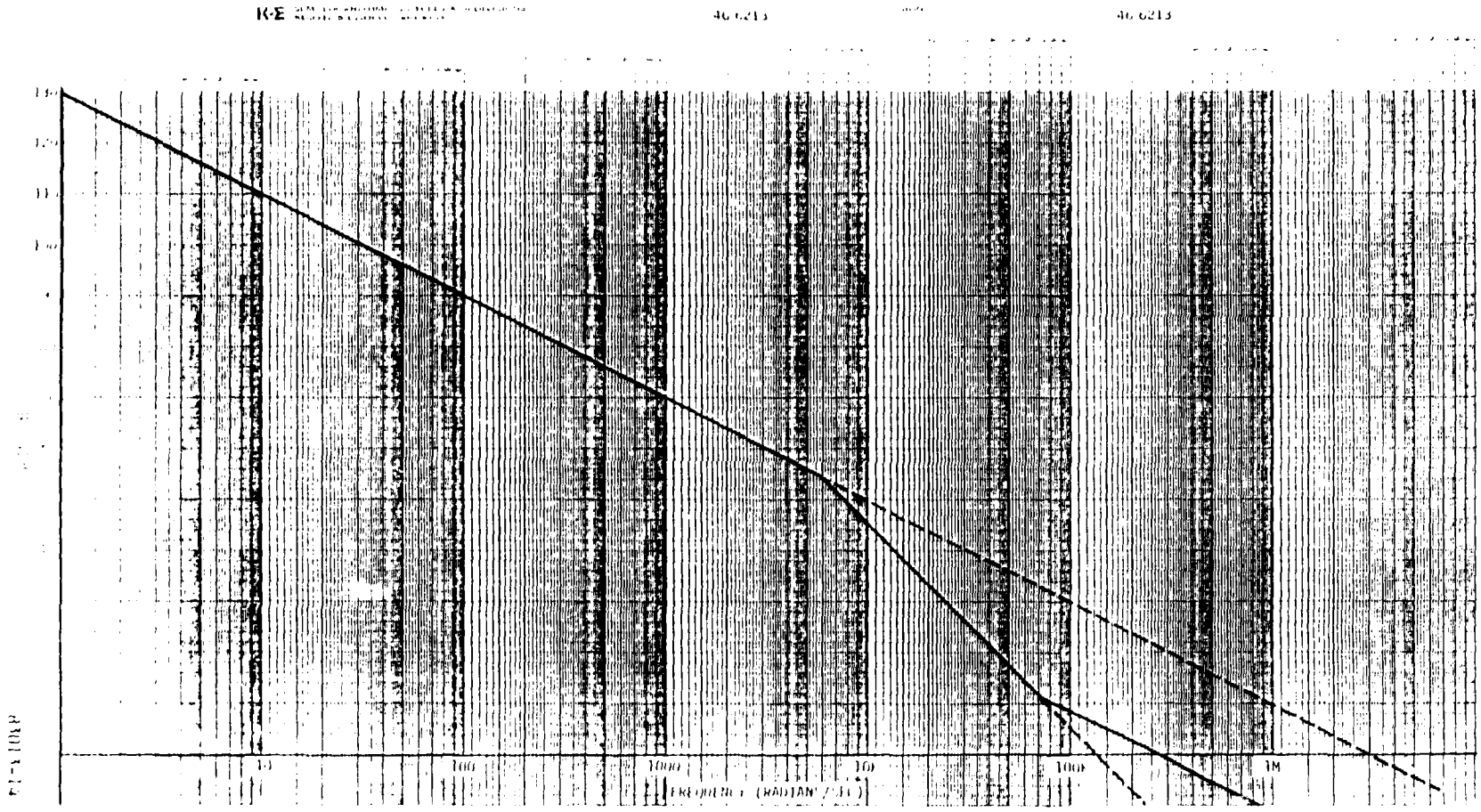

Figure 3.1-2. Bode Plot Zero-IF PPL Demodulator (2nd Order)

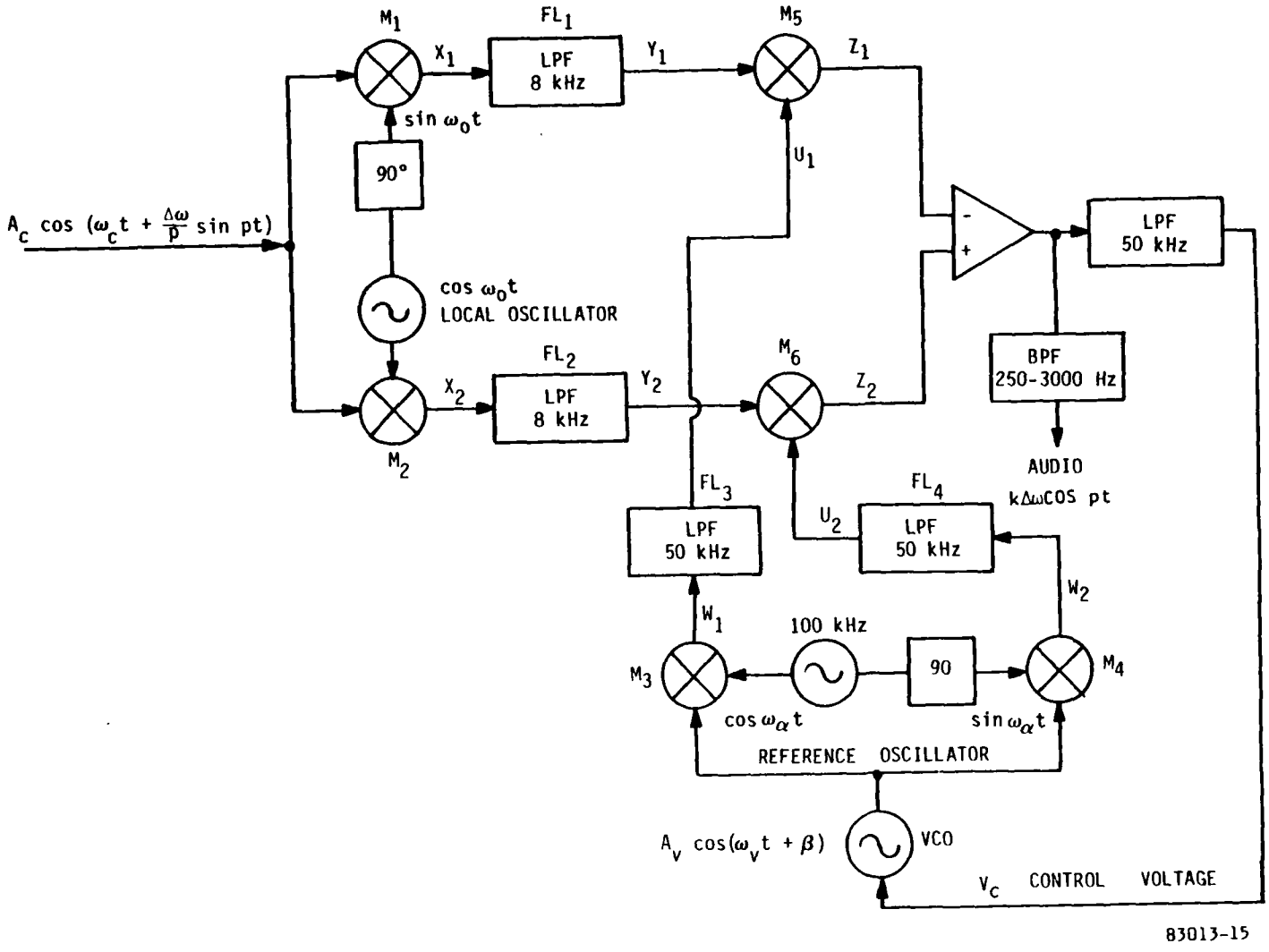

Figure 3.2-1. Zero-IF Phase-Locked-Loop Processor

The signal is converted to baseband by mixing with the local oscillator in mixers M_1 and M_2. Baseband signals X_1 and X_2 are in phase quadrature because of the 90° phase shift provided in the local oscillator signal applied to M_1.

X_1 is given by

$$X_1 = A_c \text{SIN}\omega_o t \ \text{COS}\ (\omega_c t + \frac{\Delta\omega}{\rho}\ \text{SIN}\ \rho t)$$

where

ω_o is the frequency of the local oscillator.

Expansion yields

$$X_1 = \frac{Ac}{2}\text{SIN}(\omega_o t + \omega_c t + \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t) + \frac{Ac}{2}\text{SIN}(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t)$$

and

$$X_2 = \frac{Ac}{2}\text{COS}(\omega_o t + \omega_c t + \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t) + \frac{Ac}{2}\text{COS}(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t)$$

The lowpass filters, FL_1 and FL_2, remove the sum products of X_1 and X_2 and at the output of the filters, the baseband signals are given by

$$Y_1 = \frac{Ac}{2}\text{SIN}(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t)$$

$$Y_2 = \frac{Ac}{2}\text{COS}(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}\text{SIN}\ \rho t)$$

These two quantities are the inputs labeled I and Q on the schematic on page A-9. Let the output of the voltage controlled oscillator (VCO) shown on the schematic on page A-10 be

$$V = A_v \text{COS}(\omega_v t + \beta)$$

where

β is the phase,

ω_v is the frequency of the VCO, and

A_v is the amplitude.

The signals, W_1 and W_2, are quadrature baseband signals derived from mixers M_3 and M_4 by mixing the quadrature components of the reference oscillator with the output signal of the VCO.

$$W_1 = \frac{Av}{2}COS(\omega_\alpha t + \omega_v t + \beta) + \frac{Av}{2}COS(\omega_\alpha t - \omega_v t - \beta)$$

$$W_2 = \frac{Av}{2}SIN(\omega_\alpha t + \omega_v t + \beta) + \frac{Av}{2}SIN(\omega_\alpha t - \omega_v t - \beta)$$

The lowpass filters, FL_3 and FL_4, remove the sum products and U_1 and U_2 result.

$$U_1 = \frac{Av}{2}COS(\omega_\alpha t - \omega_v t - \beta) \text{ and}$$

$$U_2 = \frac{Av}{2}SIN(\omega_\alpha t - \omega_v t - \beta).$$

U_1 and U_2 are the outputs of the circuit shown on the schematic on page A-11 of the appendix. The baseband signals Z_1 and Z_2 are the result of mixing Y_1 and U_1 in M_5 and Y_2 and U_2 in M_6. These mixers are shown on page A-10. Z_1 is given by

$$Z_1 = \frac{AcAv}{4}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t)COS(\omega_\alpha t - \omega_v t - \beta)$$

$$Z_1 = \frac{AcAv}{4}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t + \omega_\alpha t - \omega_v t - \beta)$$

$$+ \frac{AcAv}{4}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t - \omega_\alpha t - \omega_v t + \beta).$$

Similarly,

$$Z_2 = \frac{AcAv}{8}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t + \omega_\alpha t - \omega_v t - \beta)$$

$$- \frac{AcAv}{8}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t - \omega_\alpha t + \omega_v t + \beta).$$

At the output of the voltage comparator

$$Z_2 - Z_1 = -\frac{AcAv}{4}SIN(\omega_o t - \omega_c t - \frac{\Delta\omega}{\rho}SIN\ \rho t - \omega_\alpha t + \omega_v t + \beta)$$

The last equation is the SIN of the phase error in the phase-locked loop. For a locked condition, the argument must be zero and

$$\beta = \frac{\Delta\omega}{\rho}\text{SIN } \rho t - \omega_o t + \omega_c t + \omega_\alpha t - \omega_v t$$

The VCO is an integrator and the phase of the VCO signal is the integral of the control line voltage, V_{C_0}; therefore,

$$V_c = k\frac{\partial\beta}{\partial t}$$

where

k is a constant describing the VCO.

V_c is then

$$V_c = k\Delta\omega\text{COS } \rho t - \omega_o + \omega_c + \omega_\alpha - \omega_v$$

The recovered audio signal is the first term of the last equation and is the output labeled VCO control on page A-10. The remaining terms are dc components and are used for AFC as shown by the AFC output shown on page A-10.

The recovered audio signal is independent of the level of the input signal, S, and only dependent on $\Delta\omega$ which are the requirements for a demodulated FM signal.

3.3 ANALOG ZERO-IF RECEIVER BREADBOARD

The analog receiver developed under the original contract with CECOM uses a PLL circuit for demodulation. As indicated, the PLL approach was chosen over the sine-cosine demodulator because of its reduced sensitivity to phase and amplitude mismatch between the two channels. Figure 3.3-1 is a block diagram of the analog Zero-IF receiver. It consists of three major sub-assemblies, the RF circuits, baseband circcuits and analog demodulator, each discussed previously. As shown later, the RF circuits and basebands circuits are identical to the digital zero-IF receiver. The breadboard model has only two front panel controls, volume and preselector band selector. The preselector bands are

1) 30-43 MHz
2) 43-62 MHz
3) 62-88 MHz

The breadboard also includes a rear panel 50 ohm jumper between the output of the preselector and the input of the RF amplifier. This jumper may be removed to evaluate the receiver at frequencies other than 30 to 88 MHz. The RF circuits will provide reasonable performance from 20 to 200 MHz.

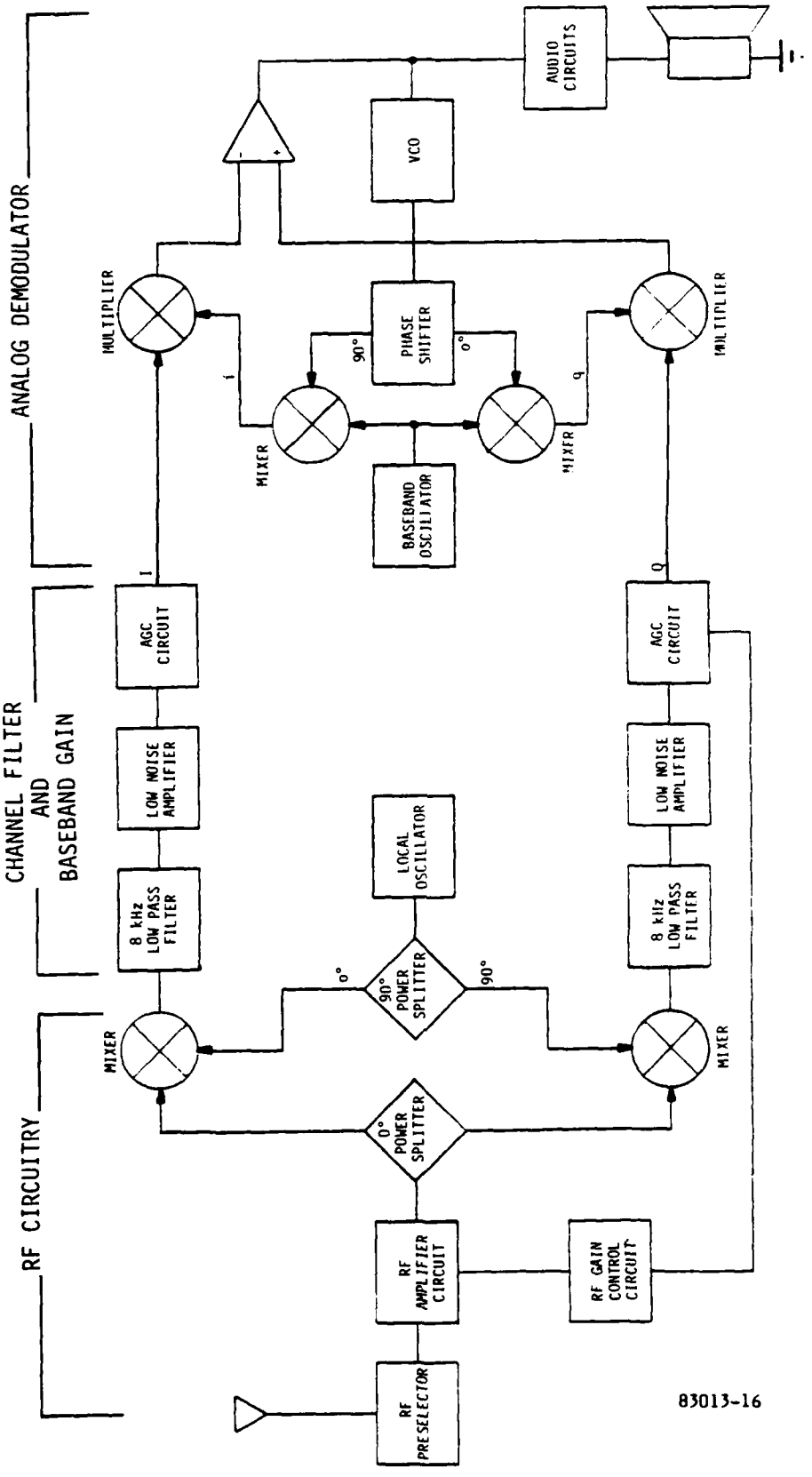

Figure 3.3-1. Zero-IF Receiver Block Diagram

3.4 TEST RESULTS - ANALOG ZERO-IF RECEIVER

This analog Zero-IF receiver breadboard was formally tested on July 29, 1982. The test data is shown below. The results of these tests demonstrate excellent performance. The goals for the various parameters are based on the performance achieved by the AN/PRC-68. The paragraph numbers are referenced to the test plan.

4.0 RECEIVER TEST PROCEDURE DATA SHEETS FOR ZERO-IF RECEIVER STUDY

4.1 a) Unit: Zero-IF Receiver Breadboard

4.2 b) Tested by: _____
Date: _____

4.3 c) Witnessed by: _____

4.4 Test Data

4.4.1 Sensitivity

Test Frequency	RF Level For 10 dB SINAD	Goal
30 MHz	-118 dBm	<-113 dBm
43 MHz	-120 dBm	<-113 dBm
59 MHz	-120 dBm	<-113 dBm
62 MHz	-120 dBm	<-113 dBm
87.975 MHz	-120 dBm	<-113 dBm

4.4.2 Audio Distortion

Modulation Frequency	Measured Distortion	Goal
300 Hz	3.1 % THD	<10% THD
1 kHz	3.2 % THD	<10% THD
3 kHz	3.8 % THD	<10% THD

4.4.3 Audio Frequency Response

Level of demodulated one 1 kHz tone 1.65 Vrms. 1.5 Vrms ±20%

Frequency of -3 dB Points

Upper -3 dB	3200 Hz	3000 Hz ± 20%
Lower -3 dB	215 Hz	250 Hz ± 20%
Ripple	0.3 dB	<2 dB

4.4.4 AGC Range

RF Signal Level (dBm)	Audio Output Level (Vrms)	Audio SINAD (dB)
-110	1.65	22.8
-100	1.65	28.5
-90	1.65	29.2
-80	1.66	28.8
-70	1.67	30.0
-60	1.66	29.6
-50	1.66	29.7
-40	1.65	29.5
-30	1.66	29.6
-20	1.66	29.6
-10	1.66	29.5
0	1.66	18.4

4.4.5 Spurious Response

LO Freq. (MHz)	10 dB SINAD LEVEL (dBm)	Spurious Frequency (MHz)	Required Spurious Level (dBm)	Spurious Rejection (dB)	Goal (dBs is dB above Sensitivity)
30	-116	60	-10	106	>60 dBs
43	-118.5	86	-28.5	90	>60 dBs
62	-120	124	-18.5	101.5	>60 dBs

4.4.6 LO Radiation

Frequency	Level At Antenna Port	Goal
30 MHz	<-100 dBm	<-73 dBm
59 MHz	<-100 dBm	<-73 dBm
87.975	-99 dBm	<-73 dBm

4.4.7 Receiver Selectivity

Signal Generator #2 = 116.5 dBm (10 dB SINAD) +5 dB = -111.5 dBm

Frequency of Signal Generator #1	Level of Signal Generator #1	Rejection (dB) (Gen #1 - Gen #2)
49.0 MHz	-11.5 dBm	100
54.0 MHz	-11.5 dBm	100
58.0 MHz	-15.5 dBm	96
58.8 MHz	≈ -20.0 dBm	≈ 91.5
58.9 MHz	-25 dBm	86.5
58.95 MHz	-13.0 dBm	98.5
58.975 MHz	-19.0 dBm	92.5
59.025 MHz	-18.0 dBm	93.5
59.050 MHz	-17.5 dBm	94.0
59.1 MHz	≈ -20.0 dBm	≈ 91.5
59.2 MHz	≈ -20.0 dBm	≈ 91.5
60 MHz	-13.0 dBm	98.5
64 MHz	-11.0 dBm	100.5
69 MHz	-7.5 dBm	104.0

Section 4

DIGITAL DEMODULATOR

The most significant advantage of digital demodulation of FM signals is that digital integrated circuit technology is well established. This means that a complete demodulator could be fabricated on a single chip, requiring a minimum number of external components. As such, this chip would form the heart of a small, low cost transceiver system. Every Zero-IF demodulation technique involves using an inphase (I) and a quadrature (Q) channel because the lower sideband is folded over on top of the upper sideband. To extract the modulation and to eliminate the beat frequency between the local oscillator and input frequency these two channels (I and Q) are necessary.

There are various approaches to digital demodulation of Zero-IF signals, each using different algorithms and having different advantages and disadvantages. Each approach, however, does require that the baseband channels be converted to a sequence of binary number pairs by an A to D converter. Then, each binary number represents an I and Q sample value. The three most promising methods for digital demodulation of Zero-IF FM signals are as follows:

1. Arctan look-up table

2. Complex multiplication of (I + jQ) and a unit reference vector. (Vector Processor)

3. Zero crossing system that requires additional baseband channels.

After the I and Q signals have been digitized, the signal may be demodulated by any of these three approaches.

Using the Arctan look-up approach, the instantaneous voltages of the I and Q channels are represented by two numbers. A ROM look-up table is used to determine the log of the absolute value of these numbers and the signs (+ or -) are stored. After finding the logs, these numbers are subtracted, smaller from larger, which amounts to dividing the amplitude of the two signals. Information as to which signal was larger is also stored. Now, by taking an antilog of this number, the result is I ÷ Q (or Q ÷ I). The phase of the demodulated signal is determined by finding the arctan of this quotient with another look-up table. This results in a number describing the phase angle between 0 and 45 degrees. This information is expanded to a full 360°, based on the sign of the I and Q channels and which was larger. The desired FM demodulation results when successive samples of the phase information are subtracted, which is in essence a discrete differentiation. The FM output, still digitized, is passed through an D/A converter and is lowpass filtered, this provides an analog demodulated FM signal that may be amplified to drive a speaker or earphone.

The vector processor approach is an alternate method, which does not require any division or log look-up tables. Instead it uses a sequence of a and b digital pairs representing the rectangular coordinates of a unit phasor. These correspond to the rotation of a unit phasor in predetermined angular increments. This sequence of a and b digital phasor values is multiplied with the I and Q values to obtain the equivalent of the actual phasor at the instant of the sample. When equality is reached, the phasor angle value, which is the address to a ROM with the a and b values, is stored. This method, in effect, replaces the division operation with two multiplications and an add operation. As in the arctan look-up table approach, successive samples must be subtracted to produce the desired FM demodulated signal.

Neither of these digital frequency demodulation methods use feedback or limiting and, therefore, AM noise contributes to the detected signal-to-noise and a threshold detection problem exists. However, digital feedback techniques can be applied to the baseband signals to improve the threshold performance.

The zero crossing approach uses limiting amplifiers. This approach eliminates the need for AGC circuits but reduces the phase-change sampling from continuous to four per cycle. This reduction of sampling time reduces the ultimate SINAD to about 30 dB. If a cleaner signal is desired, this method could be modified to create more sample points with additional channels. This technique is similar to a conventional pulse counting FM detector. It has the FM improvement factor, but suffers from reduced zero crossings in the Zero-IF architecture.

Each of these three approaches represent a viable solution to digital demodulation of Zero-IF FM signals, each with its own particular advantages and disadvantages. Table 4-1 is a summary of these tradeoffs.

4.1 VECTOR PROCESSOR

The digital demodulator approach chosen for the Zero-IF receiver study was the vector processor approach, chosen because it readily lends itself to large scale integration while still providing good performance.

Figure 4.1-1 is a block diagram of the Vector Processor Zero-IF Digital Demodulator. The two sample-and-hold circuits sample the I and Q channels at a periodic rate. These two samples are then digitized by the two analog-to-digital converters. The outputs of two A/D converters represent a complex number of the form I + jQ.

In order to extract the frequency modulation signal from I + jQ, it is first necessary to calculate the absolute phase of the signal as a function of I + jQ at the instant in time when the sample-and-hold circuits sample the I and Q baseband channels. This is accomplished by converting I + jQ to polar coordinates. The result of this conversion is the instantaneous amplitude and phase information.

Table 4-1. Digital Demodulation Techniques

Approach	Advantages	Disadvantages
1. Look-up Table	• Good voice performance	• No FM threshold
	• Relatively easy to implement	• Not easily integrated
	• Proven concept	• Not-optimum for data
	• Low risk	
2. Vector Processor	• Fairly easy to integrate	• No FM threshold
	• Good voice performance	• Not-optimum for data
		• Requires microsecond speed multiplication
3. Zero Crossing	• FM threshold	• Degrades ultimate SINAD
	• Eliminate AGC	
	• Good data performance	

The block labeled as d/dt in Figure 4.1-1 takes the derivative of the phase with respect to time; this provides a frequency or FM output as a digital number. The d/dt function is accomplished by subtracting successive samples of the phase. A digital-to-analog converter then provides an analog voltage that drives a conventional audio amplifier and speaker.

4.2 EXPLANATION OF VECTOR PROCESSOR

The primary function of the Vector Processor portion of the digital demodulator is the rectangular to polar conversion of the I and Q signals. This conversion must be done every 25 microseconds (40 kHz sampling rate). To perform this conversion at a high speed, a novel approach is used. Figure 4.2-1 is a block diagram of the vector processor and Figure 4.2-2 is a flow chart of digital demodulation using a vector processor. The operation of the vector processor is summarized as follows.

STEP 1: The I and Q channels are split into two paths on board 1 of the vector processor (See page A-13).

STEP 2: Continuing on board 1, one path determines if the amplitude of I and the amplitude of Q is positive or negative. This information is used later.

STEP 3: The remaining paths take the absolute value (magnitude) of I and Q.

STEP 4: I and Q are converted from an analog to a digital signal (sample and hold, than A to D) and sent to board 2 of the vector processor (page A-14).

STEP 5: I and Q are tested to see which has the greater magnitude. The lesser is now called b. This magnitude information is used later.

STEP 6: The lesser value is sent to a magnitude comparator and the greater value to a multiplier.

STEP 7: A Johnson counter from board 4 (page A-16) addresses a lookup table which stores the tangent of an angle, d, for d = 0 thru 45 degrees. The greater of I and Q is multiplied by the tangent from the lookup table. This becomes a.

STEP 8: Now a and b are tested to see which has the greater magnitude.

If a < = b go to step 9a
If a > b go to step 9b
This magnitude information is sent to board 4.

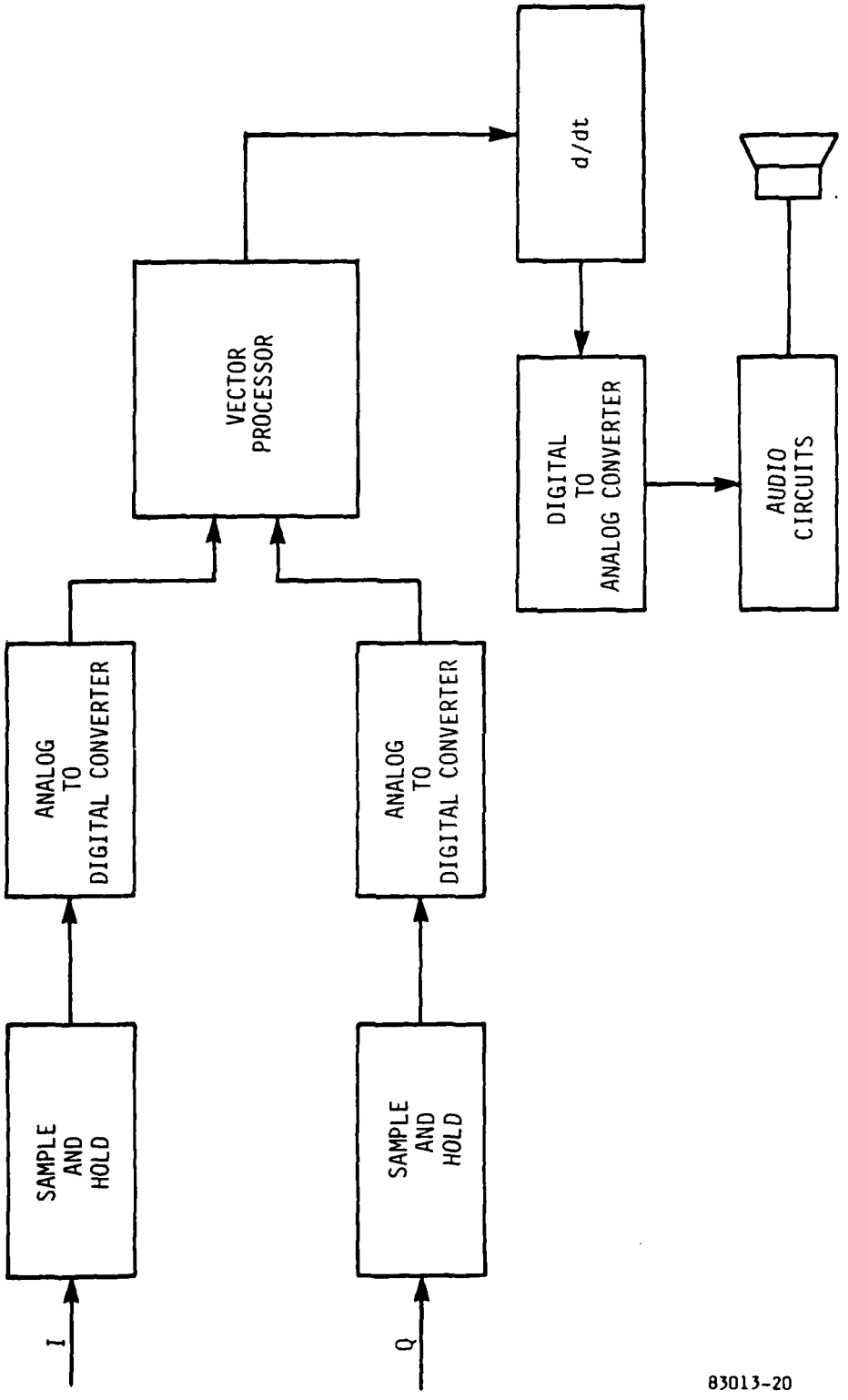

Figure 4.1-1. Zero-IF Digital Demodulator Block Diagram

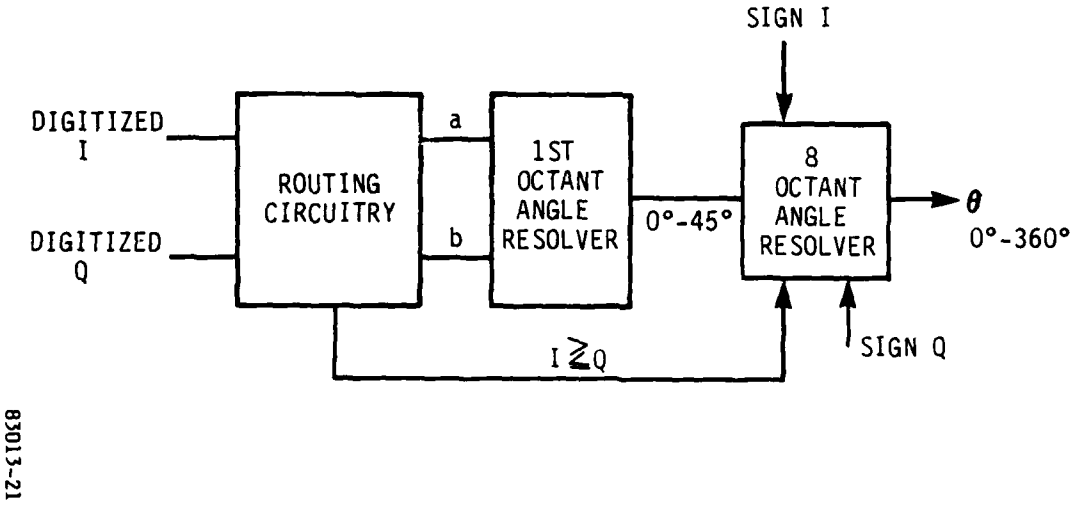

Figure 4.2-1. Vector Processor Block Diagram

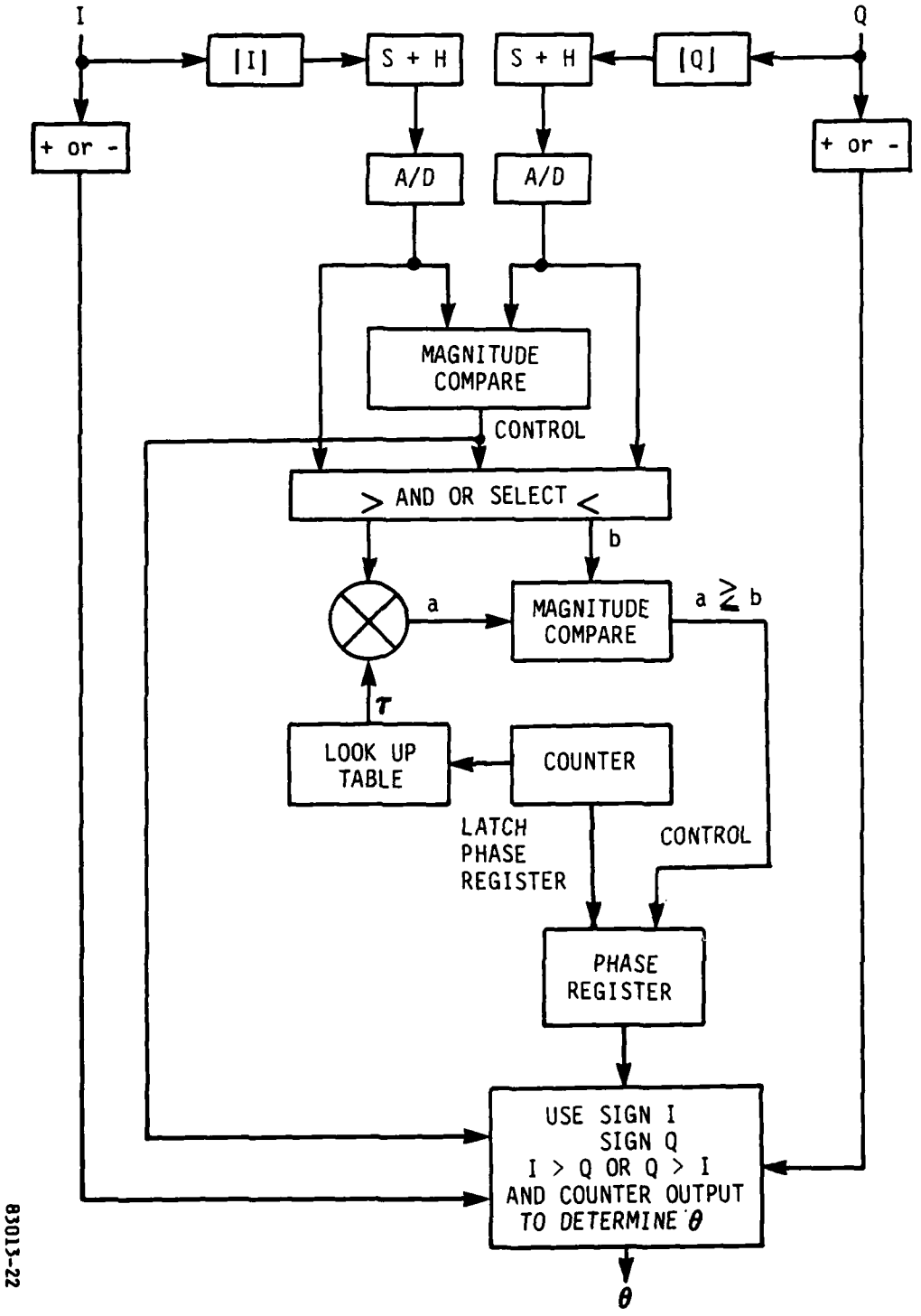

Figure 4.2-2. Vector Processor Flow Chart

STEP 9a: Store a "1" in the current test bit position of the phase register on board 4. Go to step 10.

STEP 9b: Store a "0" in the current test bit position of the phase register on board 4. Go to step 10.

STEP 10: Let the counter move one count to the next least significant bit. If the bit just tested was the least significant bit, latch the phase register output. Go to step 11. If not, multiply the greater of I and Q again by the lookup table output. Go to step 8.

STEP 11: The output of 10 is ϕ, an angle in the first octant (I and Q are both positive with I greater than Q). This angle plus the output of step 2 and step 5, which define the eight octants, results in θ, which is the instantaneous phase of the incoming signal.

On board 3 (page A-15), the output θ is then differentiated by subtracting successive samples of the phase information. A digital-to-analog converter then provides an analog voltage that drives an audio amplifier and speaker.

4.3 DIGITAL ZERO-IF RECEIVER

The digital receiver developed under the add on contract with CECOM uses a vector processor for digital demodulation. As indicated, the vector processor approach to digital demodulation was chosen over the Arctan lookup table and zero crossing approaches because of its good performance and ease of integration. Figure 4.3-1 is a block diagram of the digital Zero IF receiver. As can be seen by comparing this figure with the figure of the analog receiver (Figure 3.3-1), the RF and baseband gain circuitry are the same. This enables the digital demodulator and analog demodulator circuit cards to be interchanged in the deliverable breadboard. This change can be accomplished by merely removing one set of circuit cards and replacing them with the other set.

4.4 TEST RESULTS: DIGITAL ZERO-IF RECEIVER

The Digital Zero-IF receiver was formally tested on March 25, 1982. The test data is shown below. The results of these tests show good performance. the goals for the various parameters were met or exceeded in every case. The paragraph numbers are in reference to paragraphs in the test procedure.

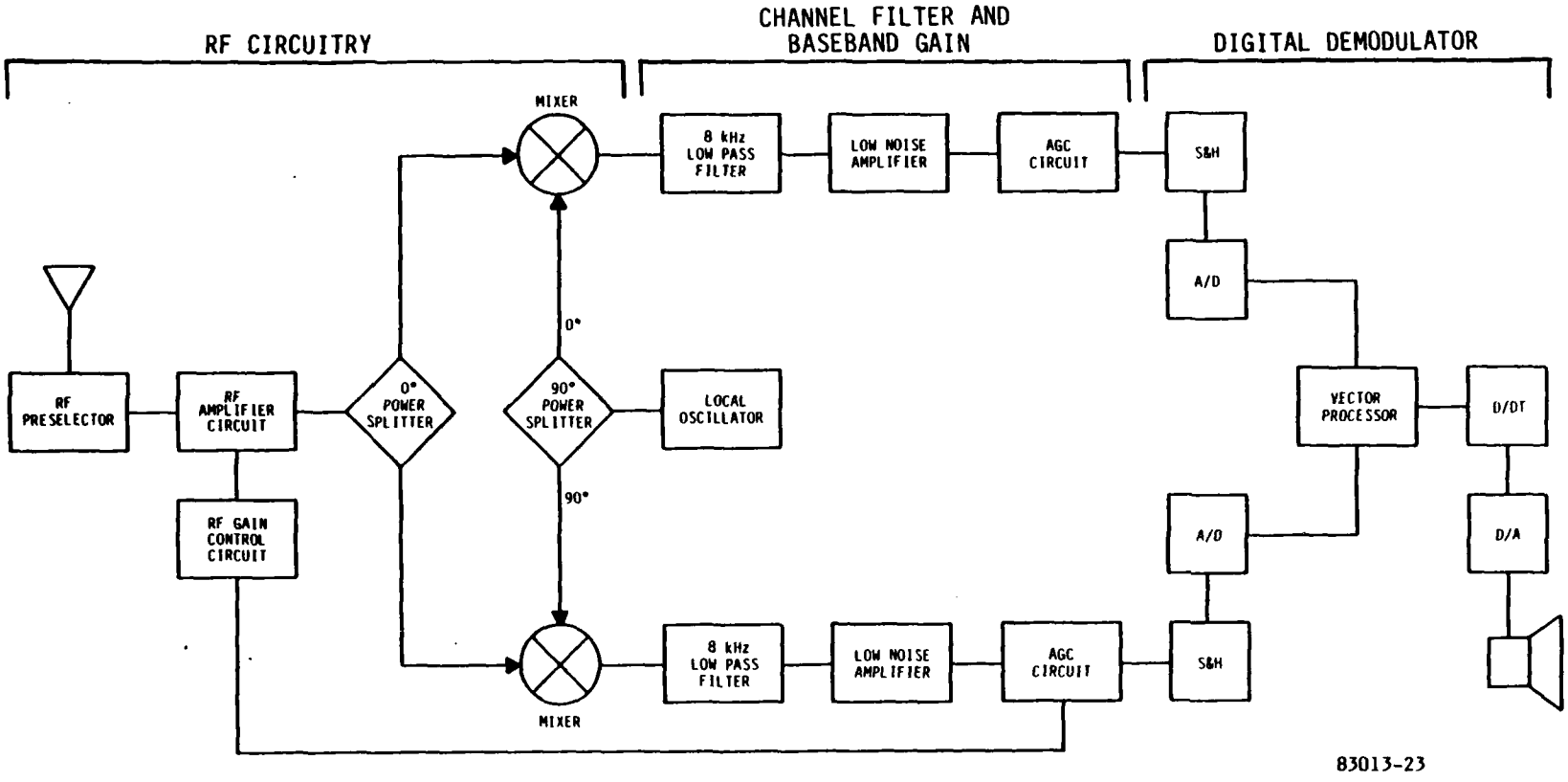

Figure 4.3-1. Digital Zero-IF Receiver Block Diagram

4.0 RECEIVER TEST PROCEDURE DATA SHEETS FOR ZERO IF RECEIVER STUDY.

4.1 a) Unit: Zero IF Receiver Breadboard

4.2 b) Tested by: _____
Date: _____

4.3 c) Witnessed by: _____

4.4 Test Data

4.4.1 Sensitivity

Test Frequency	Measured SINAD	Goal
30 MHz	-117 dBm	<-113 dBm
43 MHz	-119 dBm	<-113 dBm
59 MHz	-119 dBm	<-113 dBm
62 MHz	-119 dBm	<-113 dBm
87.975 MHz	-120 dBm	<-113 dBm

4.4.2 Audio Distortion

Modulation Frequency	Measured Distortion	Goal
300 Hz	4.3 % THD	<10% THD
1 kHz	2.6 % THD	<10% THD
3 kHz	2.2 % THD	<10% THD

4.4.3 Audio Frequency Response

Level of demodulated one kilohertz tone is 0.7 Vrms.

Frequency of -3 dB Points		Goal
Upper -3 dB	2.4K Hz	3000 Hz ± 20%
Lower -3 dB	215 Hz	250 Hz ± 20%
Ripple	0.4 dB	<2 dB

4.4.4 AGC Range

RF SIGNAL LEVEL	AUDIO LEVEL (Vrms)	AUDIO SINAD (dB)
-110 dBm	0.72	27
-100 dBm	0.72	30.8
-90 dBm	0.72	31.5
-80 dBm	0.72	32.0
-70 dBm	0.72	32.0
-60 dBm	0.72	31.4
-50 dBm	0.72	32.0
-40 dBm	0.72	31.0
-30 dBm	0.72	31.5
-20 dBm	0.72	31.8
-10 dBm	0.72	30.6
0 dBm	0.72	22.4

4.4.5 Spurious Response

LO Freq. (MHz)	10 dB SINAD LEVEL (dBm)	Spurious Frequency (MHz)	Required Spurious Level (dBm)	Spurious Rejection (dB) B-A	Goal (dBs is dB above Sensitivity)
30	-118.5	60	-27.5	+91.0	>60 dBs
43	-119.0	86	-27.0	+92.0	>60 dBs
62	-114.0	124	-40	+74	>60 dBs

4.4.6 LO Radiation

Frequency	Level at RF I/O	Goal
30 MHz	<-90 dBm	<-73 dBm
59 MHz	<-98 dBm	<-73 dBm
87.975	<-92 dBm	<-73 dBm

4.4.7 Receiver Selectivity

Signal Generator #2 = -114 dBm (10 dB SINAD) +5 dB = -109 dBm

Frequency of Signal Generator #1	Level of Signal Generator #1	Rejection (dB) (Gen #1 - Gen #2)
49.0 MHz	-10 dBm	99
54.0 MHz	-10 dBm	99
58.0 MHz	-10 dBm	99
58.8 MHz	-20 dBm	89
58.9 MHz	-12 dBm	97
58.95 MHz	-20 dBm	89
58.975 MHz	-29 dBm	80
59.025 MHz	-30 dBm	79
59.050 MHz	-21 dBm	88
59.1 MHz	-13 dBm	96
59.2 MHz	-20 dBm	89
60 MHz	-10 dBm	99
64 MHz	-9 dBm	100
69 MHz	-8 dBm	101

Section 5

CONCLUSIONS AND RECOMMENDATIONS

The Zero-IF Receiver Study Program has resulted in a breadboard receiver that demonstrates excellent performance for both the analog and digital demodulators. The breadboard shows that Zero-IF is a viable technology for receiver systems. Both the analog and digital demodulators may be integrated into an LSI. The digital system is well suited to the universal gate array approach currently used in ITT-A/OD's SINCGARS-V system. A preliminary analysis indicated that the digital demodulator could be implemented in the standard 400 gate array and mounted in a chip carrier package less than one-half inch square. Similarly, the AGC circuits may be integrated in either I^2L, bipolar or CMOS linear arrays. The CMOS array would consume the least amount of power, but the bipolar offers the lowest 1/f noise. I^2L offers a compromise between the other two.

Integrating these receiver subsystem into an LSI promises to provide the necessary components for the design of small, low cost, low power radio system. The Zero-IF approach is extremely well suited to hand-held radio applications that do not require a narrow band receiver preselector. The Zero-IF architecture has no image frequency and a preselector is only required to eliminate spurious responses. The Zero-IF spurious responses are far removed from the desired channel, which permits the use of a fairly broad preselector. Elimination of a narrow band preselector, either PIN diode switched or varactor tuned, significantly reduces the size and cost of a receiver systems.

The Zero-IF architecture, however, is not limited to hand-held FM receivers. For high performance applications, a narrow band preselector may be included, with a corresponding increase in size and cost. Additionally, ITT-A/OD has demonstrated that the Zero-IF concept can be used for amplitude modulated systems and preliminary analysis shows that any form of modulation can be handled by a Zero-IF system.

The Zero-IF technique is not limited only to receiver subsystems. ITT-A/OD has demonstrated an FM modulator that is essentially a Zero-IF FM receiver in reverse. As in the case of the receiver, the greatest advantage of this approach is to integrate these circuit functions into one or more LSI circuits.

The ITT Corporation, through efforts at the Aerospace/ Optical Division and Standard Telecommunications Laboratories in England, is devoted to continued development of Zero-IF architecture. The first commercial ITT product using the Zero-IF system is an ultra-miniature radio pager that has been sold in England to British Telecom. Shortly, these pagers will be sold in selected areas in the United States through Tandy Corporation's Radio Shack outlets for a price of $99.95, which attests to the value of Zero-IF architecture to produce small, low-power, low-cost radio equipment.

Section 6

OPERATIONAL INSTRUCTIONS

The Zero-IF breadboard is a complete receiver system less power supplies and local oscillator.

6.1 TEST EQUIPMENT REQUIREMENTS

The following equipment is either required or optional for evaluating the Zero-IF breadboard:

Quantity	Description	Remarks
2	15 Volt Power Supplies	(2A)
2	RF Signal Generators	(30-88 MHz)
1	Distortion Analyzer	
1	Oscilloscope	(optional)

6.2 POWER SUPPLY CONNECTIONS

Connect the two 15-volt power supplies as follows:

A. Connect +15 volt line to +15 volt power supply.
B. Connect ground to ground lug on +15 volt power supply.
C. Connect -15 volt line to -15 volt power supply.
D. Connect ground to ground (+ terminal) on -15 volt power supply.

CAUTION: Double check connection to be sure the right line is going to the right power supply or else damage may occur to radio. DO NOT EXCEED $\pm$ 15 Vdc.

6.3 SIGNAL GENERATOR CONNECTIONS

Connect the two signal generators as follows:

A. Set generator "1" to 10 dBm RF output.
B. Turn off modulation on generator "1".
C. Set frequency of generator "1" to 35 MHz.
D. Connect to local oscillator input through a 50 Ω coax cable.
E. Set generator "2" to -70 dBm RF output.
F. Set modulation frequency to 1000 Hz on generator "2".
G. Set deviation to 5 kHz on generator "2".
H. Connect generator "2" to preselector input through a 50 Ω coax cable.

6.4 RECEIVER POWER-UP

To operate the receiver, do the following:

A. Set preselector switch to low.
B. Turn volume control down
C. Turn both power supplies on
D. Slowly increase volume control until the demodulated signal can be heard.

6.5 SINAD MEASUREMENTS

To measure the ultimate SINAD of the receiver, do the following:

A. Connect distortion analyzer to received signal output via a 50-ohm coax cable.
B. Turn distortion analyzer on.
C. Set function switch to set level.
D. Set meter range knob to 0 on dB range.
E. Set sensitivity switch to 0 on dB scale.
F. Set frequency range to X100.
G. Set frequency dial close to 10 as possible at pointer.
H. Turn meter range switch clockwise until the meter begins to come up.
I. Fine tune frequency for maximum deflection and highest meter range setting possible using the fine and coarse adjustment.
J. Read ultimate SINAD and record the level.

6.6 RECEIVER POWER-DOWN

After completing the SINAD or other additional tests, do the following:

A. Disconnect distortion analyzer.
B. Turn both power supplies off simultaneously.
C. Turn off both RF generators.
D. Disconnect test equipment from radio.

6.7 CONVERSION FROM ANALOG TO DIGITAL DEMODULATION

A. Be sure power is off.
B. Remove the baseband multipliers board and the baseband oscillator and VCO board (Part Nos. 31174-107 and 31174-108). This can be accomplished by removing the two Phillips head screws that are securing each board to standoffs and pulling the boards out of the connectors (J8 and J9).
C. Insert the two digital subchassis boards A15 and A16 into connectors J8 and J9, respectively.

D. Place the digital subchassis on top of the three tall standoffs. Use a No. 4 screw, flat washer, and lock washer at each standoff to secure the subchassis onto the breadboard.
E. Insert the four digital demodulator boards into the four connectors. Part Nos. 31174-111, 31174-112, 31174-113, and 31174-114 fit into connector Nos. J10, J11, J12 and J13, respectively.
F. Secure each board to the subchassis in the same manner that the analog democulator boards were secured. Use two sets of screw, a flat washer, and a lock washer for each board.
G. Follow the procedure for turn on, and the receiver will operate with a digital demodulator.

6.8 CONVERSION FROM DIGITAL TO ANALOG DEMODULATION

A. Be sure power is off.
B. Remove the four digital demodulator boards from the digital demodulator subchassis. This can be accomplished by removing the two Phillips head screws that are securing each board to standoffs and pulling the board out of the connector.
C. Remove the three Phillips head screws that are holding the subchassis in place.
D. Lift the subchassis out of the breadboard.
E. Remove the screws holding the wire harness boards in the breadboard and remove the boards.
F. Place the subchassis out of the way.
G. Place the baseband multipliers board (Part No. 31174-107) into connector J8.
H. Place the baseband oscillator and VCO board (Part No. 31174-108) into connector J9.
I. Secure the boards in the same manner that the digital demodulator boards were secured into the subchassis. Use two sets of a screw, flatwasher, and lock washer for each board to secure the boards onto the breadboard.
J. Follow the procedure for turn on and the receiver will operate with an analog demodulator.

Section 7

DIGITAL ZERO-IF COMPUTER SIMULATION

This program simulates the Zero-IF receiver architecture and calculates the distortion (SINAD) of the system. Two modulated sine waves, ninety degrees out of phase, represent the I and Q channels. They are sampled and converted from analog to digital. Each signal is then sent through a simulated phase detector. Once the phase of the I and Q channels are calculated, the difference between samples is calculated. This difference calculation simulates the differential process necessary for FM demodulation. The SINAD is then calculated with the formula (S+N+D/N+D).

Included in this program is the ability to change the number of A to D and phase quantization bits, along with changing the sampling rate. Insight can be gained into some of the limitations of the system. The program also provides a check for the hardware performance. Large variations between the program simulation and hardware results can be detected and subsequently corrected. This raises the confidence level for both the hardware and the software simulation.

The performance goals for the hardware were set at 35 dB ultimate SINAD, which provides ample voice recognition. Assuming a 40-kHz sampling rate, the goals can be achieved by using six bits quantization for the A to D converter and three bits in 45° phase quantization. The simulation calculated a 38.7 dB SINAD for these input parameters.

Currently, the hardware has eight A to D and seven phase quantization bits. The ultimate SINAD of the hardware measures 32 dB SINAD. The simulation calculates a 51 dB SINAD for the same conditions. This difference can be explained by the fact that the simulation does not consider phase or amplitude errors in the I and Q channels. Typically, up to 1 dB channel imbalance and a deviation of up to two degrees from phase quadrature is present in the hardware. The value of the simulation lies in the fact that it defines the operational capability of the digital circuits only. The results of this is that the hardware performance is not limited by the digital demodulator but by the analog circuits ahead of this demodulator. The fact that the digital system is actually capable of a better ultimate SINAD than that which is required explains why the ultimate SINAD of the digital system is the same as the analog system. That is, both are limited not by the demodulators but by the phase and amplitude imbalance of the analog circuits ahead of the demodulator.

A listing of this program can be found in the back of the Appendix.

APPENDIX

SCHEMATIC DIAGRAMS,

PARTS LIST,

COMPUTER SIMULATION

LISTING,

AND

FUNCTIONAL DESCRIPTION

OF

THE ZERO-IF RECEIVER

APPENDIX

SCHEMATIC DIAGRAMS,

PARTS LIST,

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LISTING,

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FUNCTIONAL DESCRIPTION

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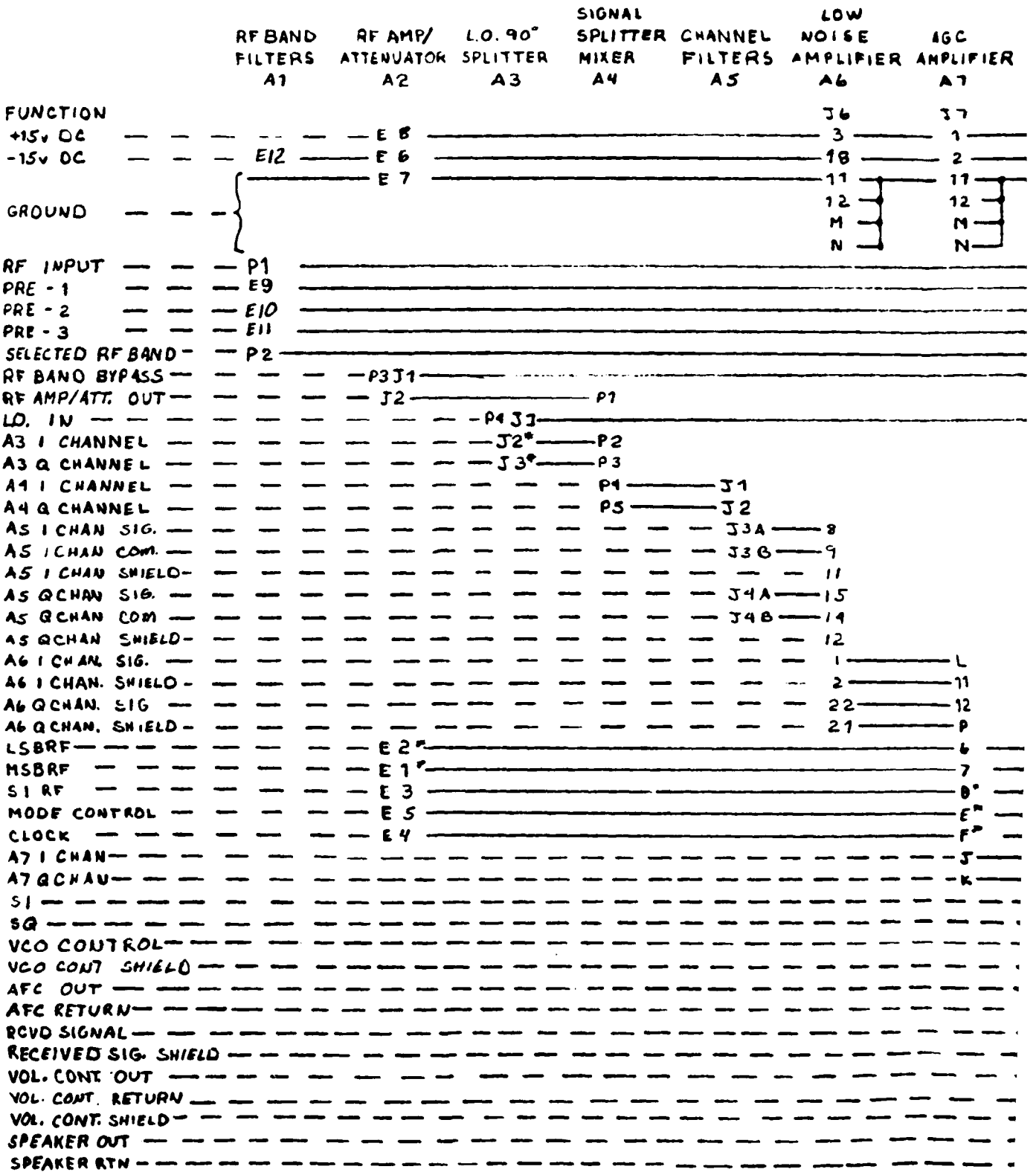
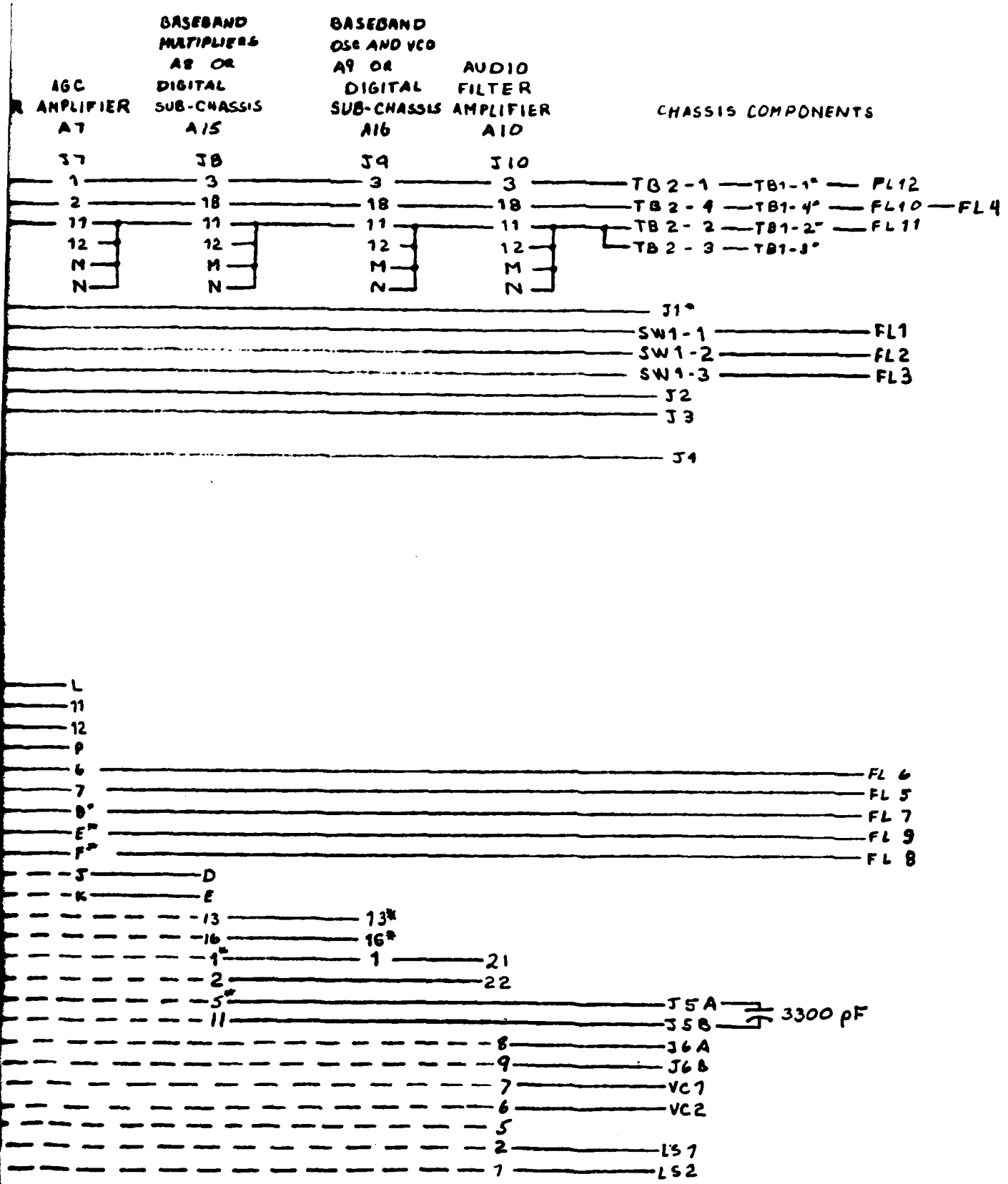
THE ZERO-IF RECEIVER

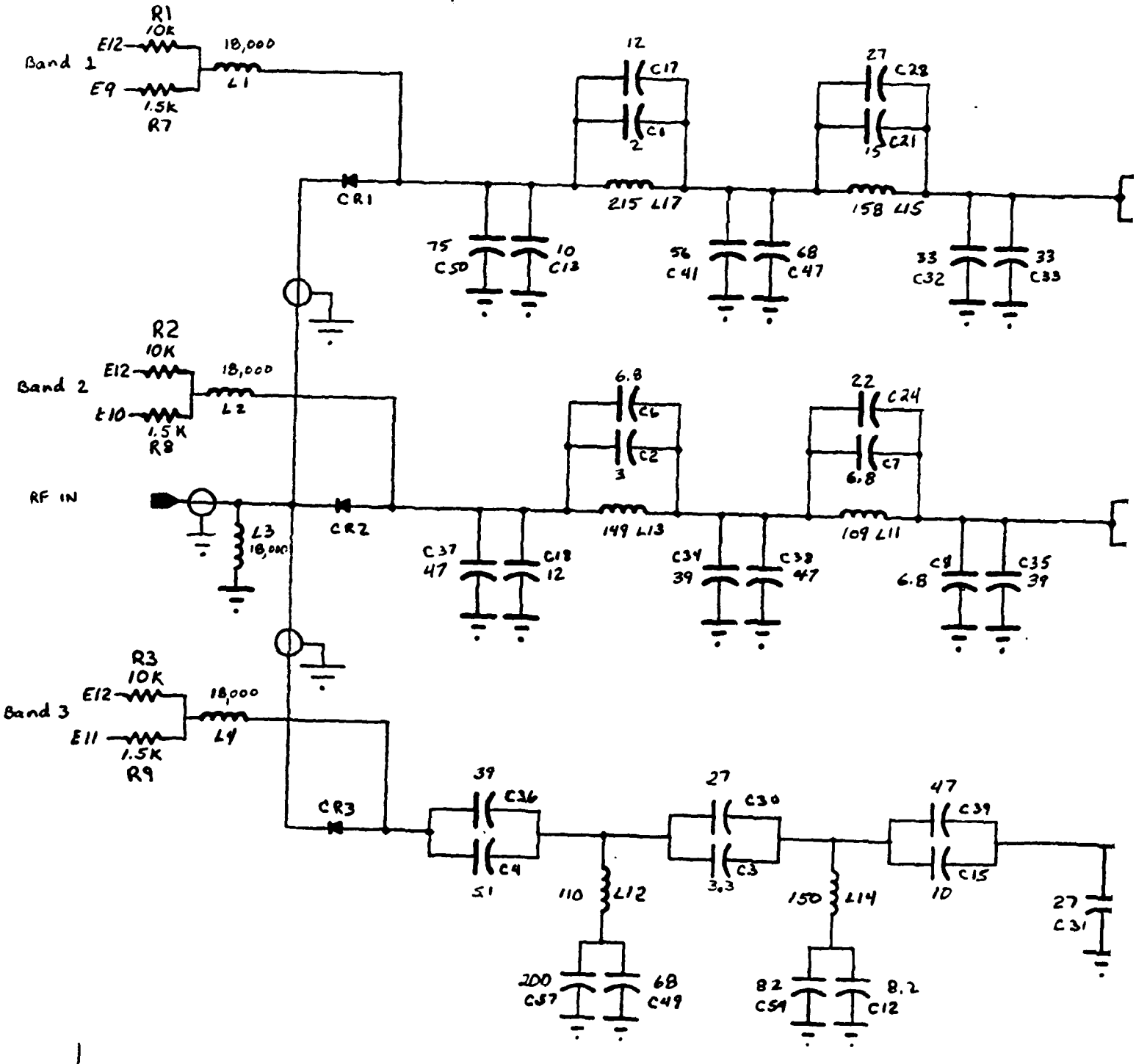


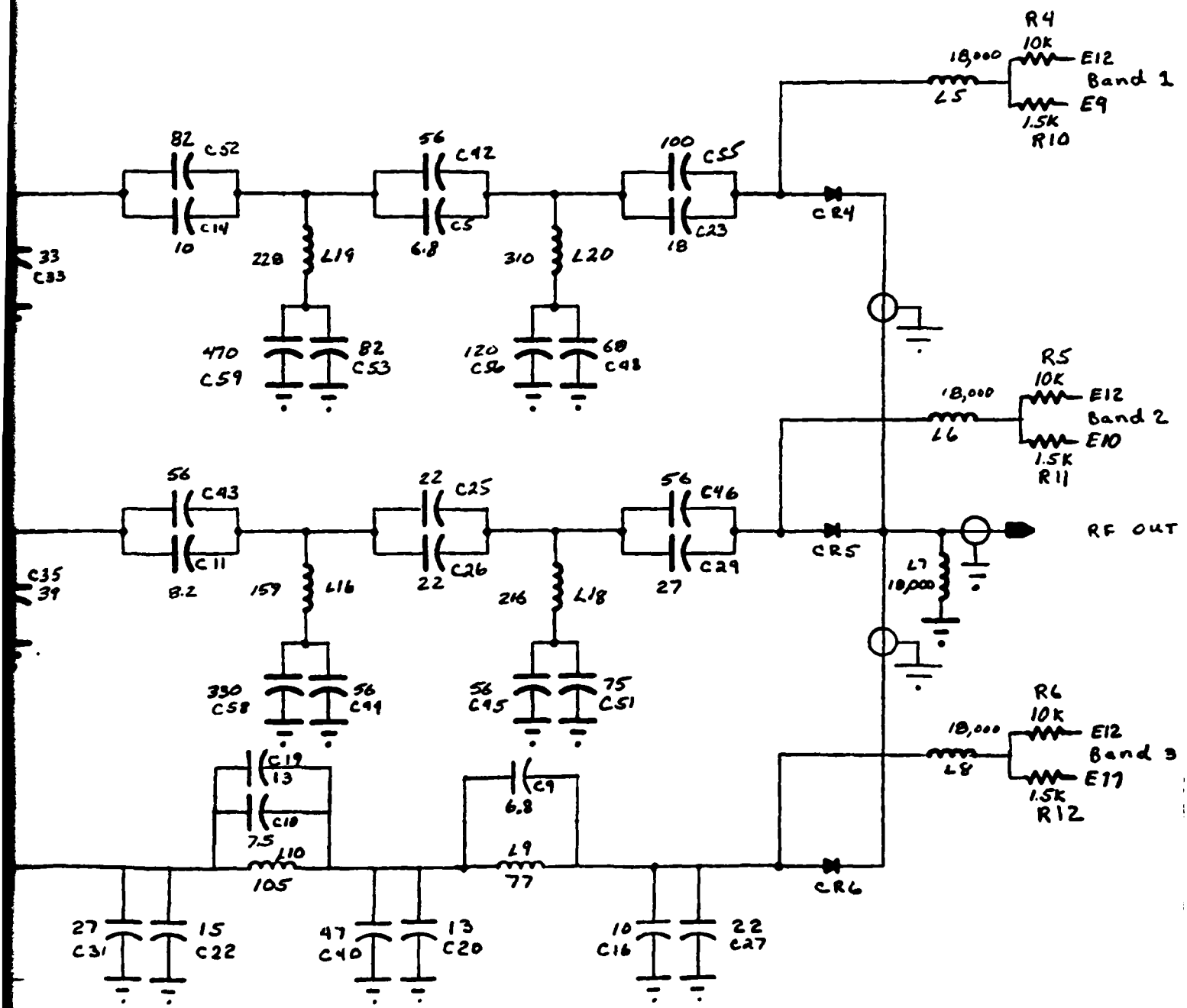
NOTES 1) * DENOTES SIGNAL SOURCE



SCHEMATIC: ZERO-IF CHASSIS WIRING DIAGRAM

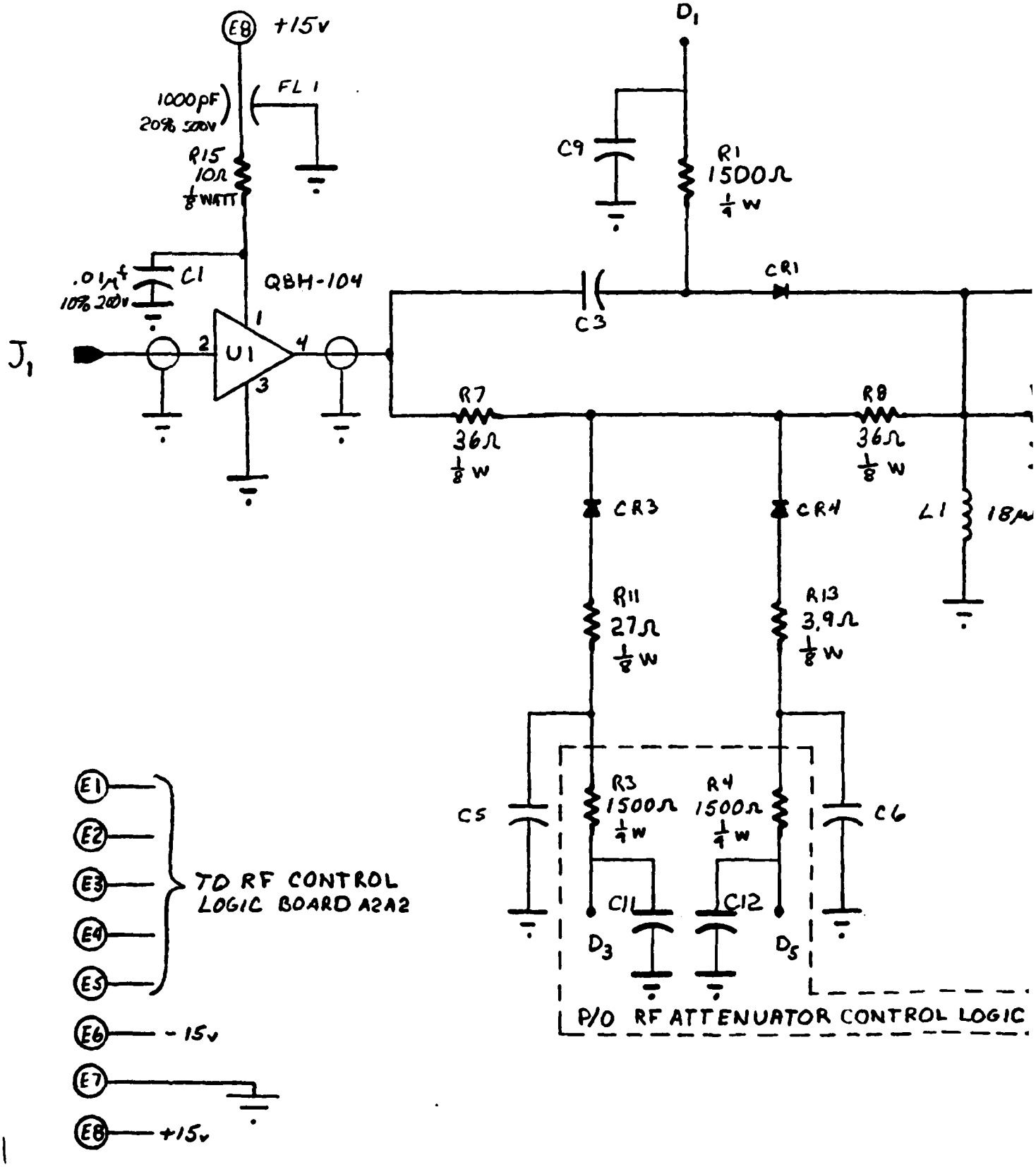
NOTE: 1) ALL CAPACITOR VALUES ARE IN PICOFARADS AND ALL INDUCTORS ARE IN NANOHENRYS
2) ALL 10K RESISTORS ARE ¼ WATT, 5%
3) ALL 1.5K RESISTORS ARE ¼ WATT, 5%
4) ALL FEEDTHRUS ARE 1500 PF
5) ALL CAPACITORS ARE 500V AND 10%
6) ALL DIODES ARE MA47047

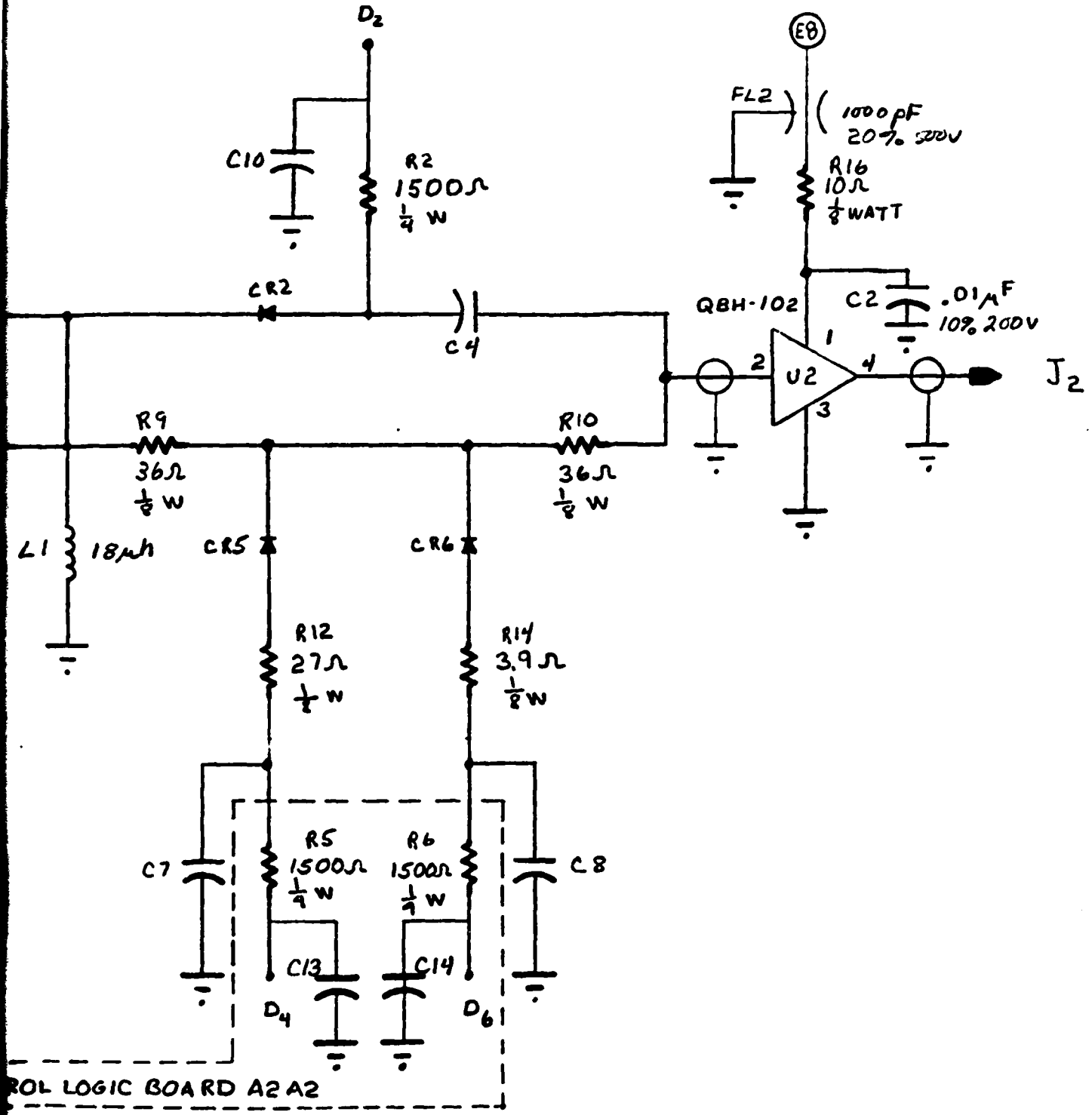




SCHEMATIC: ZERO-IF PRESELECTOR BAND FILTERS

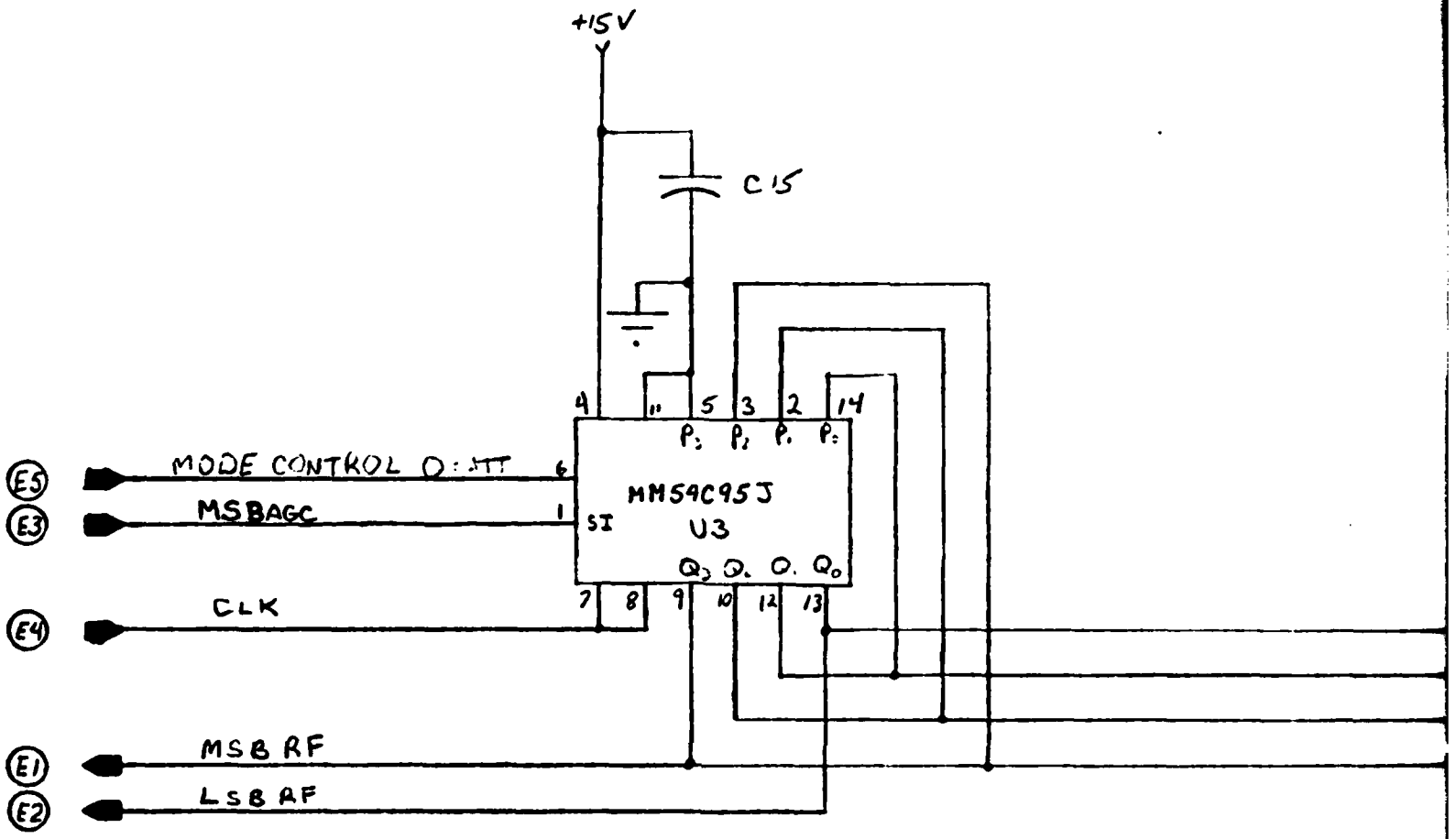
2) ALL RESISTORS ARE 5% TOLERANCE
3) CAPACITORS C3-C8 ARE ALL 1800 PF 10% 50V
4) CAPACITORS C9-C14 ARE ALL 1000 PF 20% 1000V

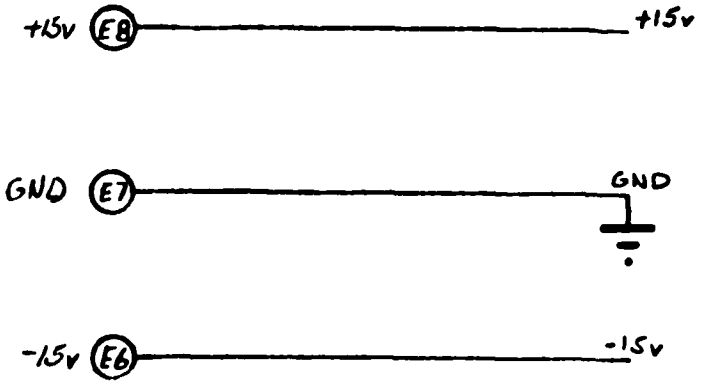


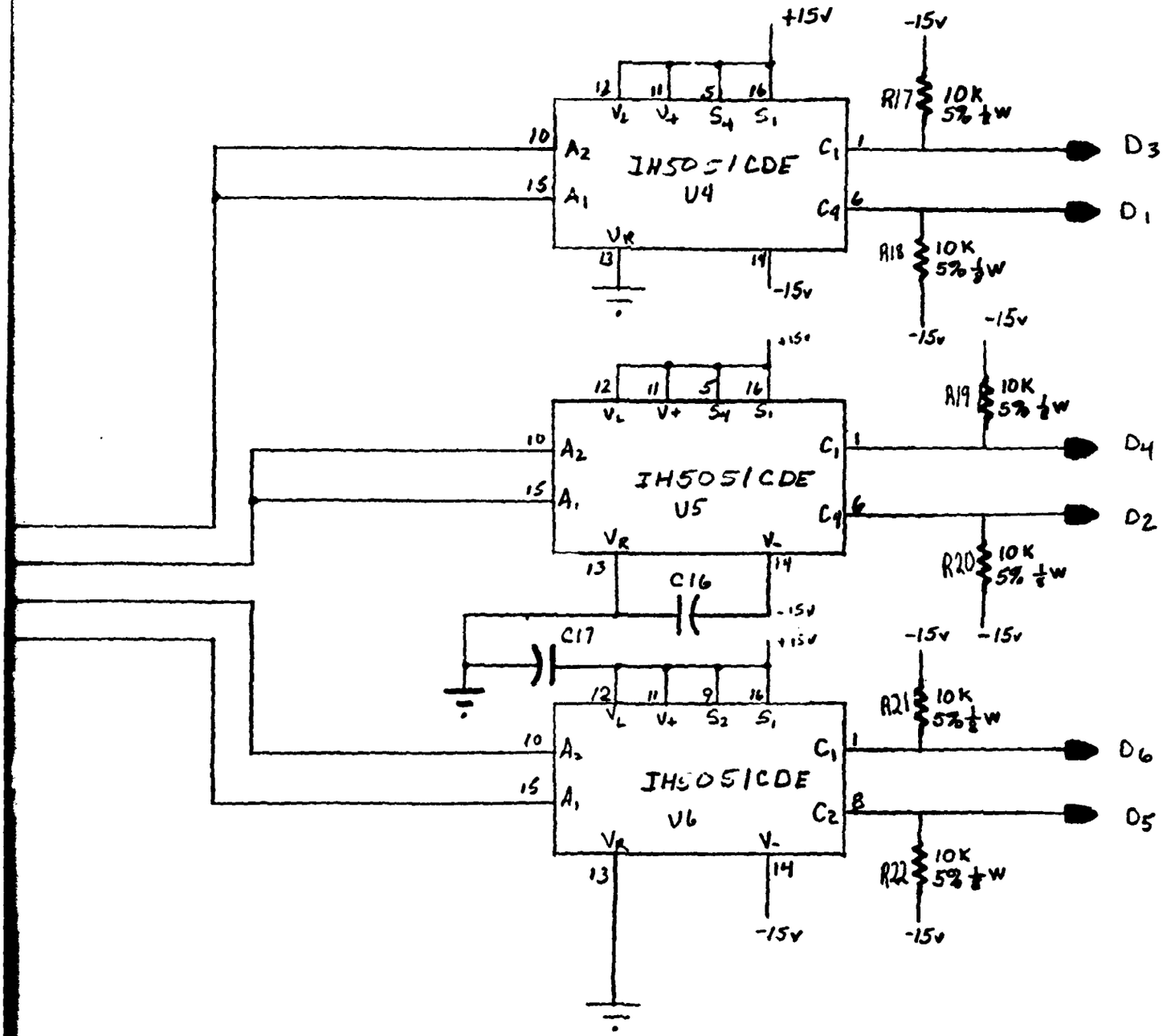


SCHEMATIC: ZERO-IF RF AMPLIFIER/ATTENUATOR

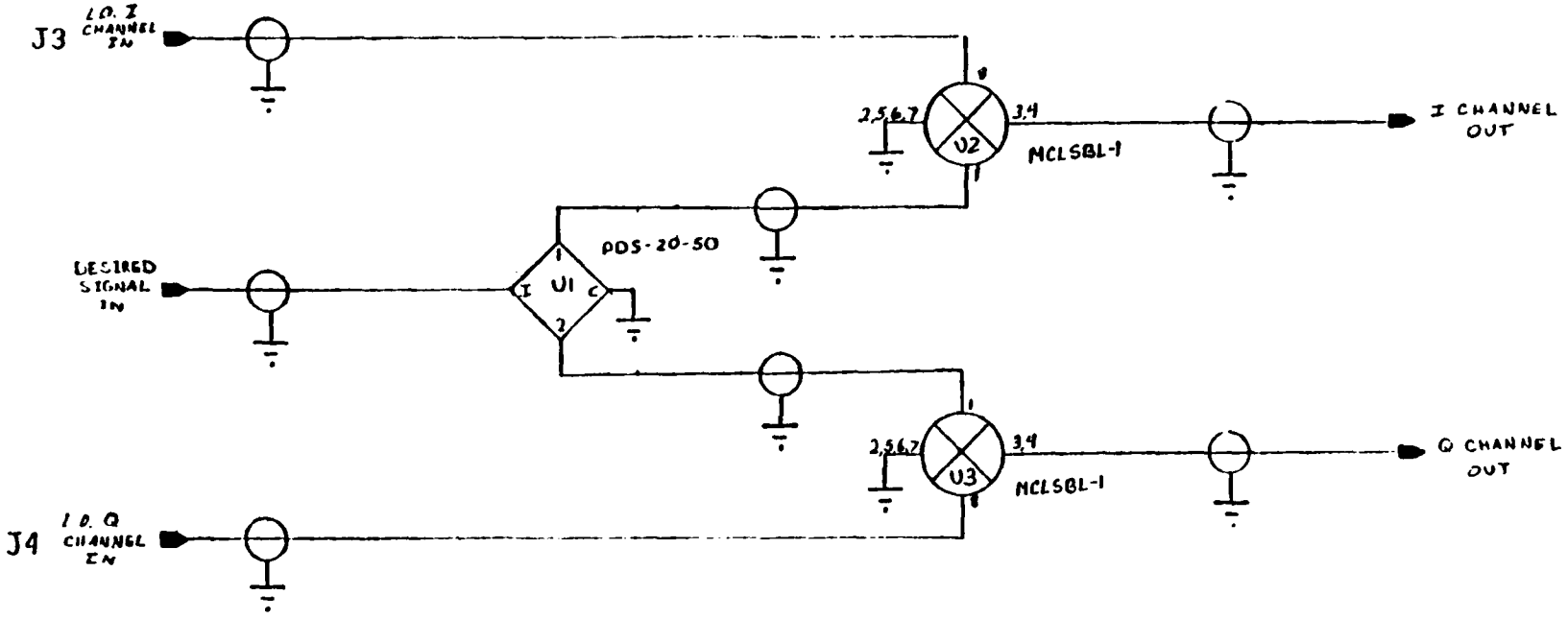
NOTES 1) ALL CAPACITORS ARE .022μF 10% 100V.







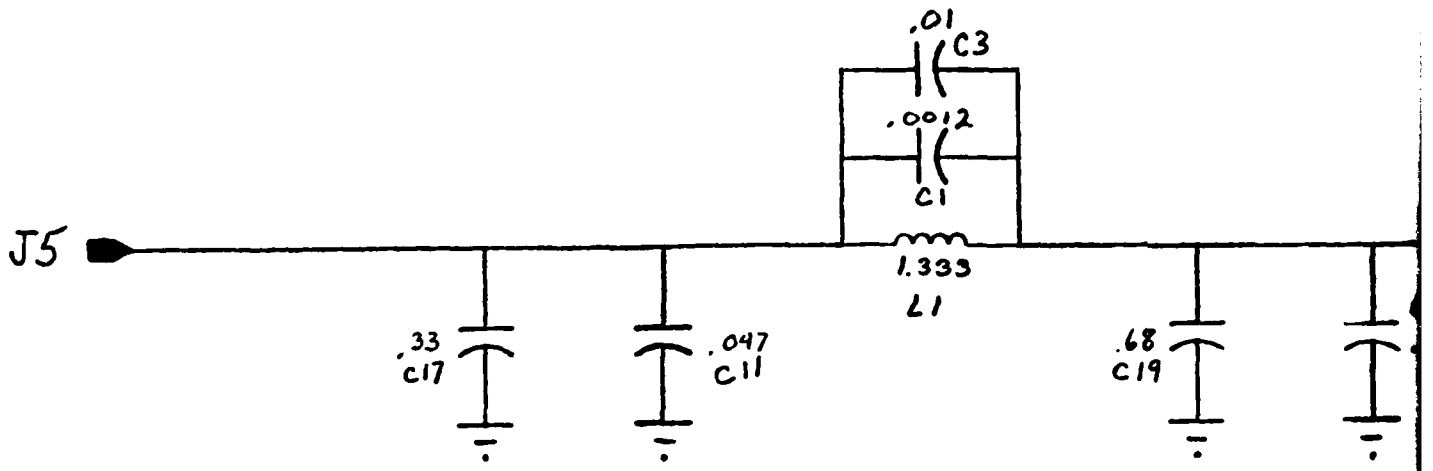
SCHEMATIC: ZERO-IF RF ATTENUATOR CONTROL LOGIC



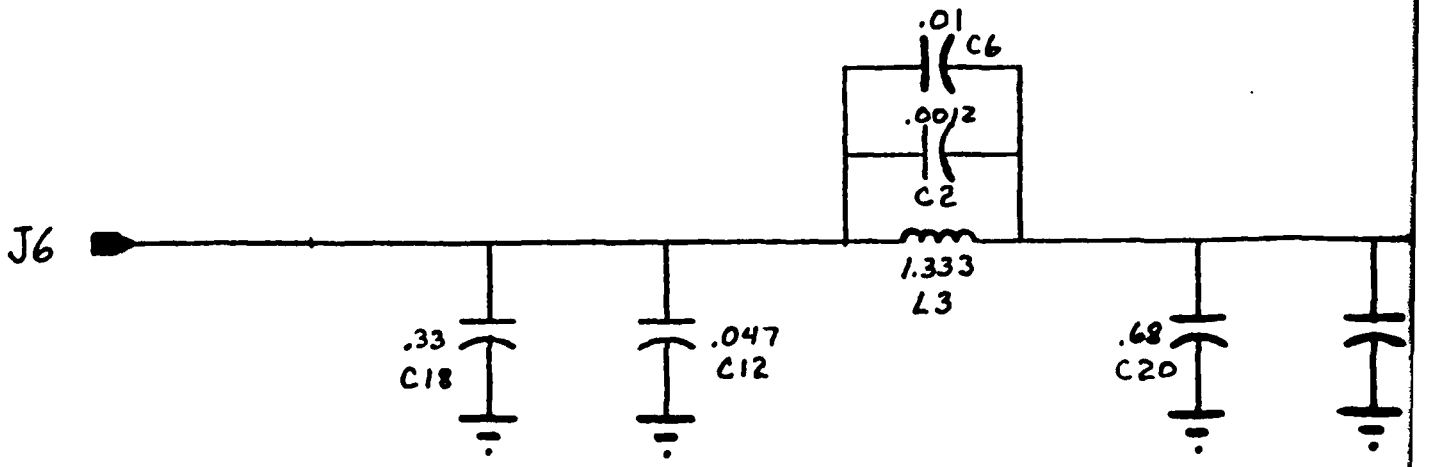
SCHEMATIC: ZERO-IF SPLITTER/MIXER

NOTES: 1) ALL CAPACITOR VALUES ARE IN MICROFARADS
2) ALL INDUCTOR VALUES ARE IN MILLIHENRYS
3) ALL CAPACITORS ARE 30V 1%

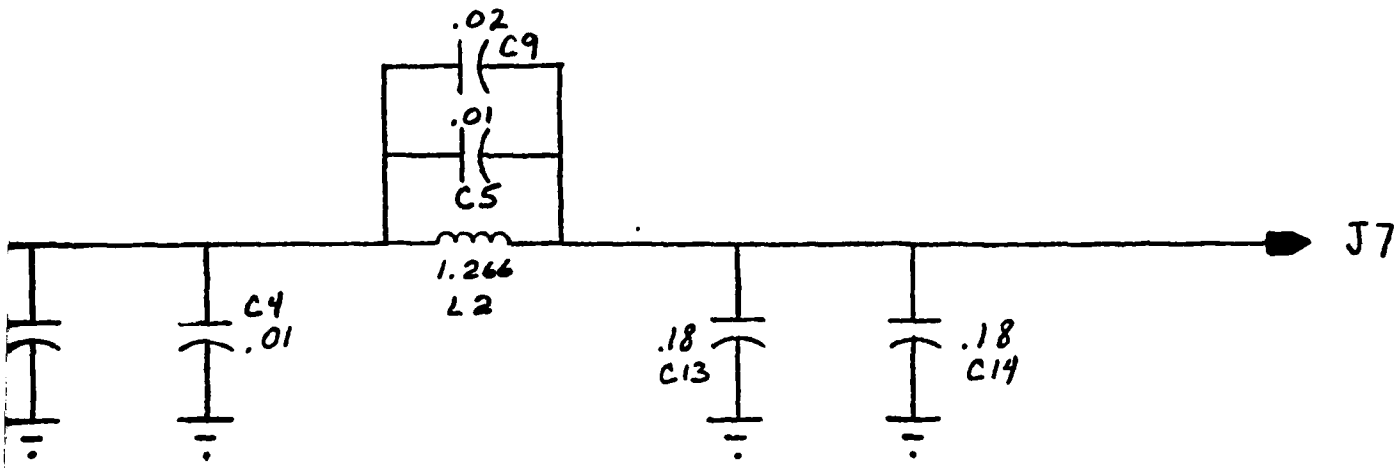
I CHANNEL



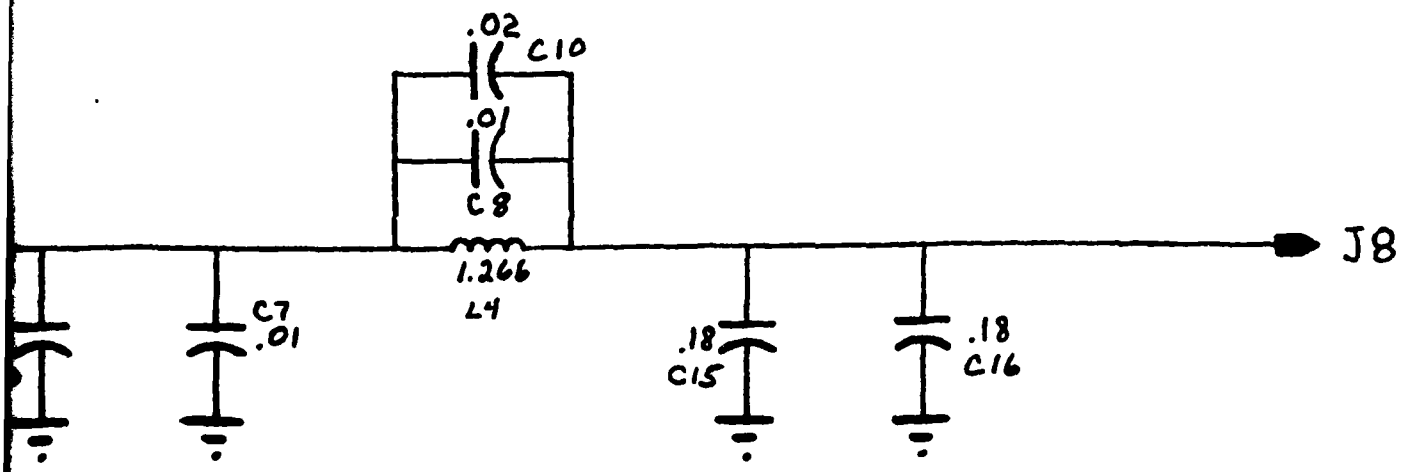
Q CHANNEL



I CHANNEL

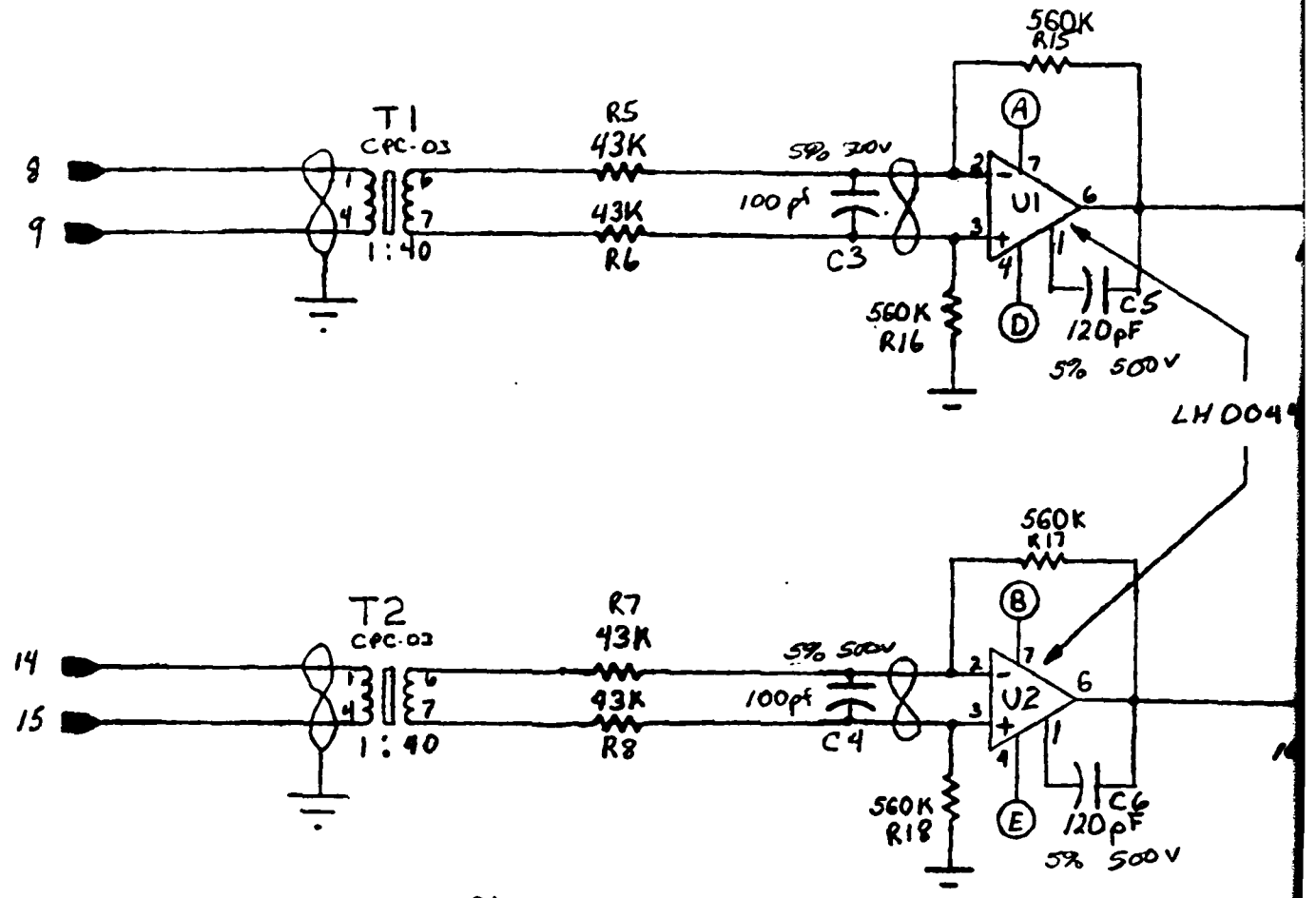


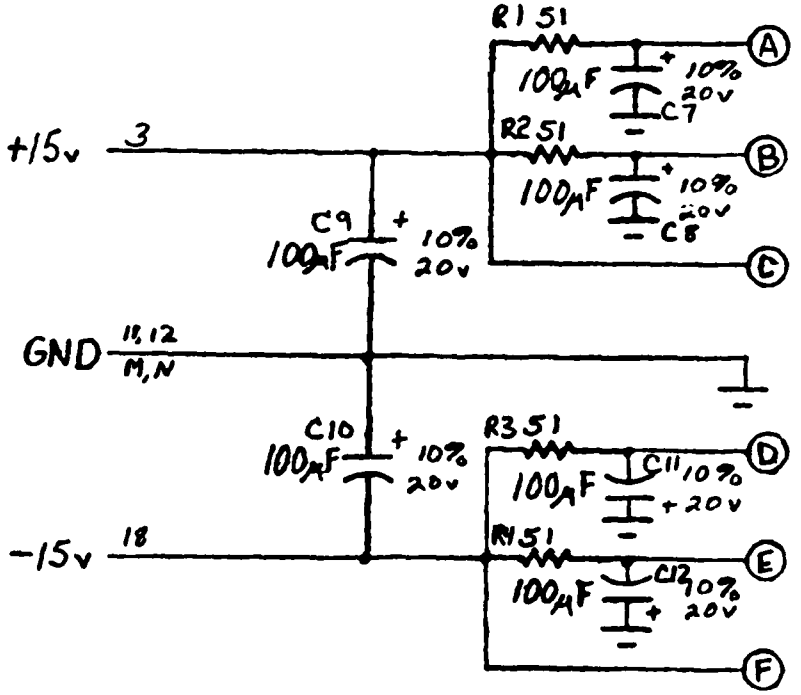
Q CHANNEL

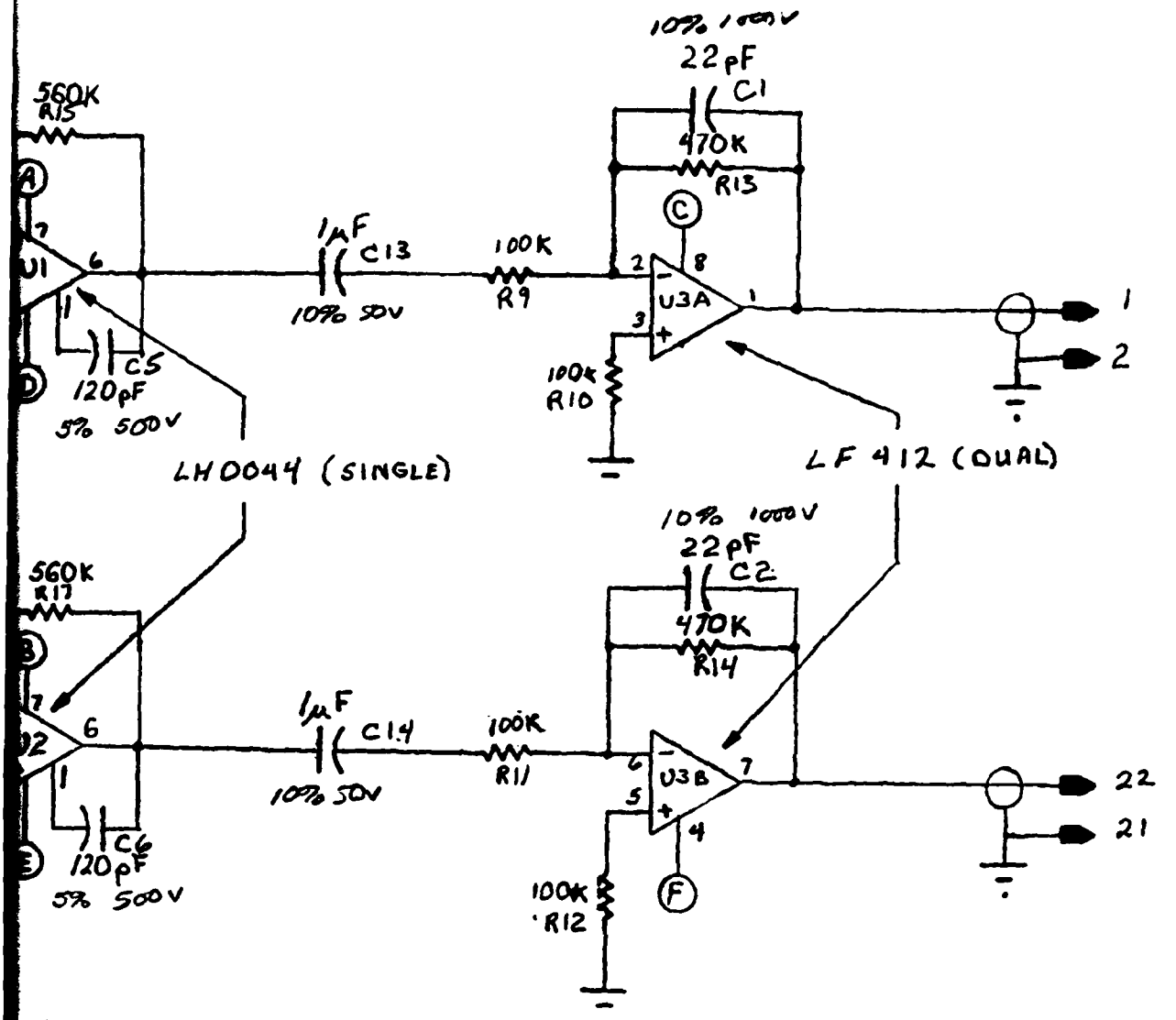


SCHEMATIC: ZERO-IF BASEBAND FILTERS

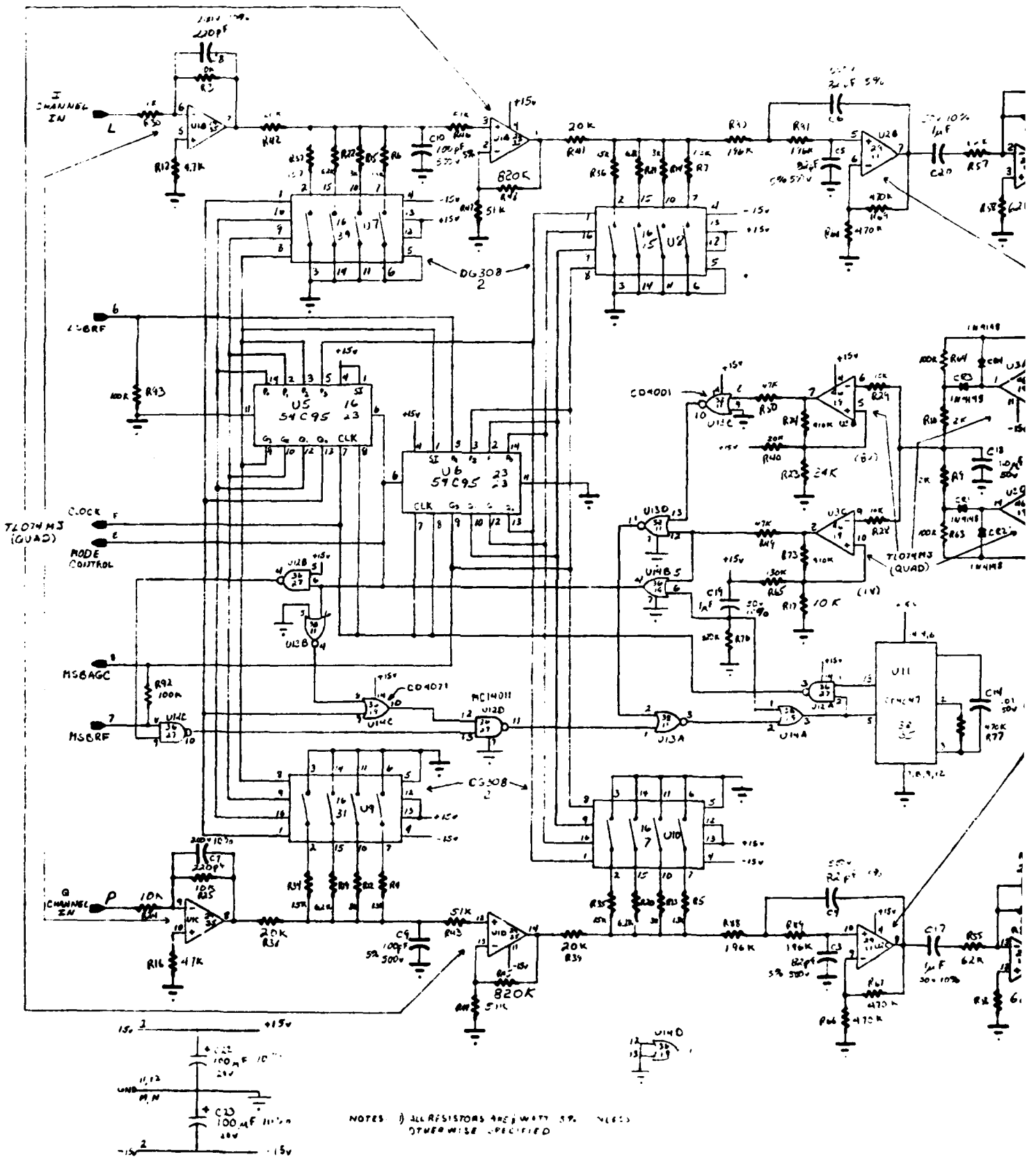
NOTES: 1) CIRCLED LETTERS INFER COMMON POINTS
2) ALL RESISTORS ARE ¼ WATT 5%
3) ALL RESISTOR VALUES GIVEN IN OHMS

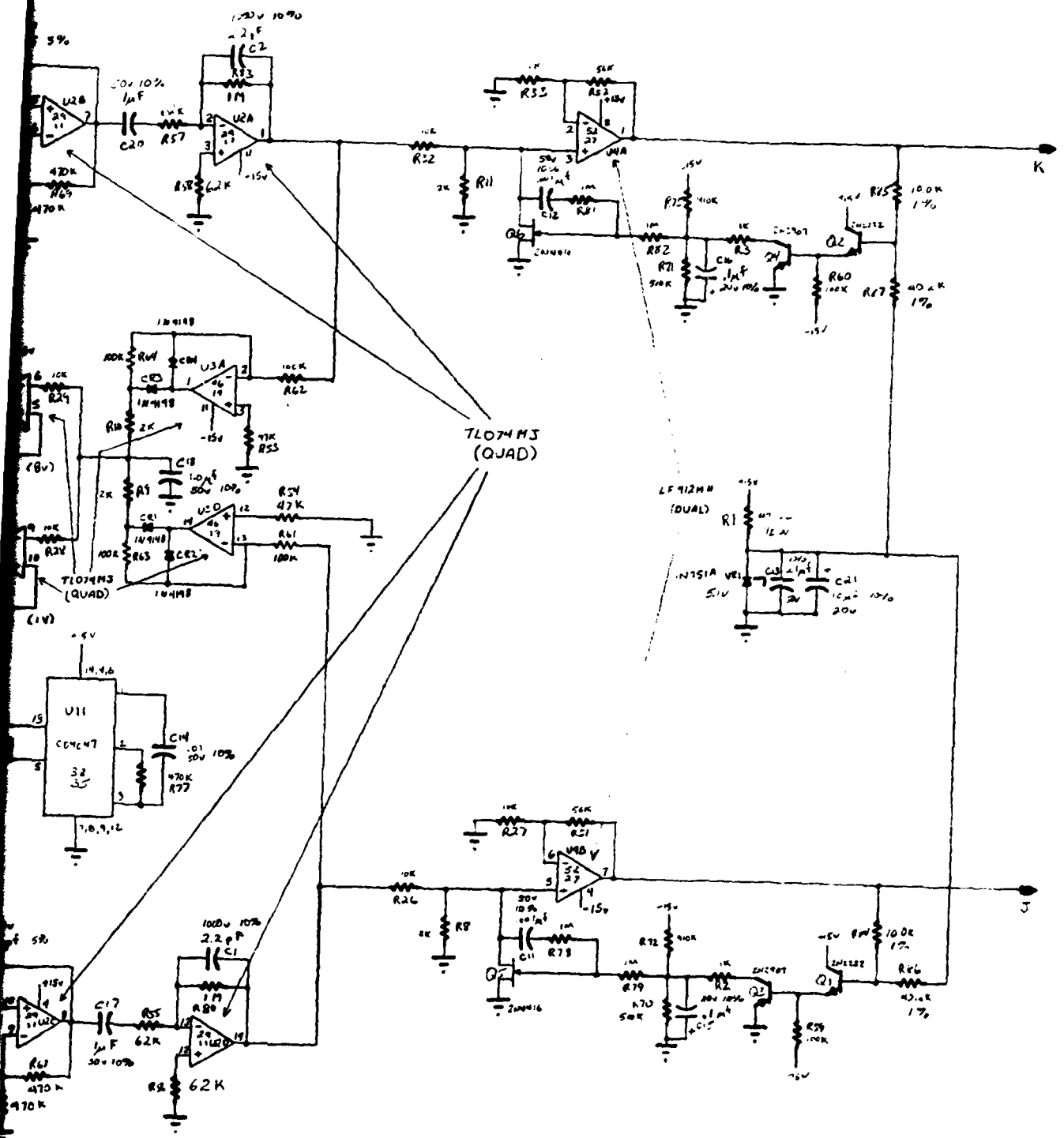




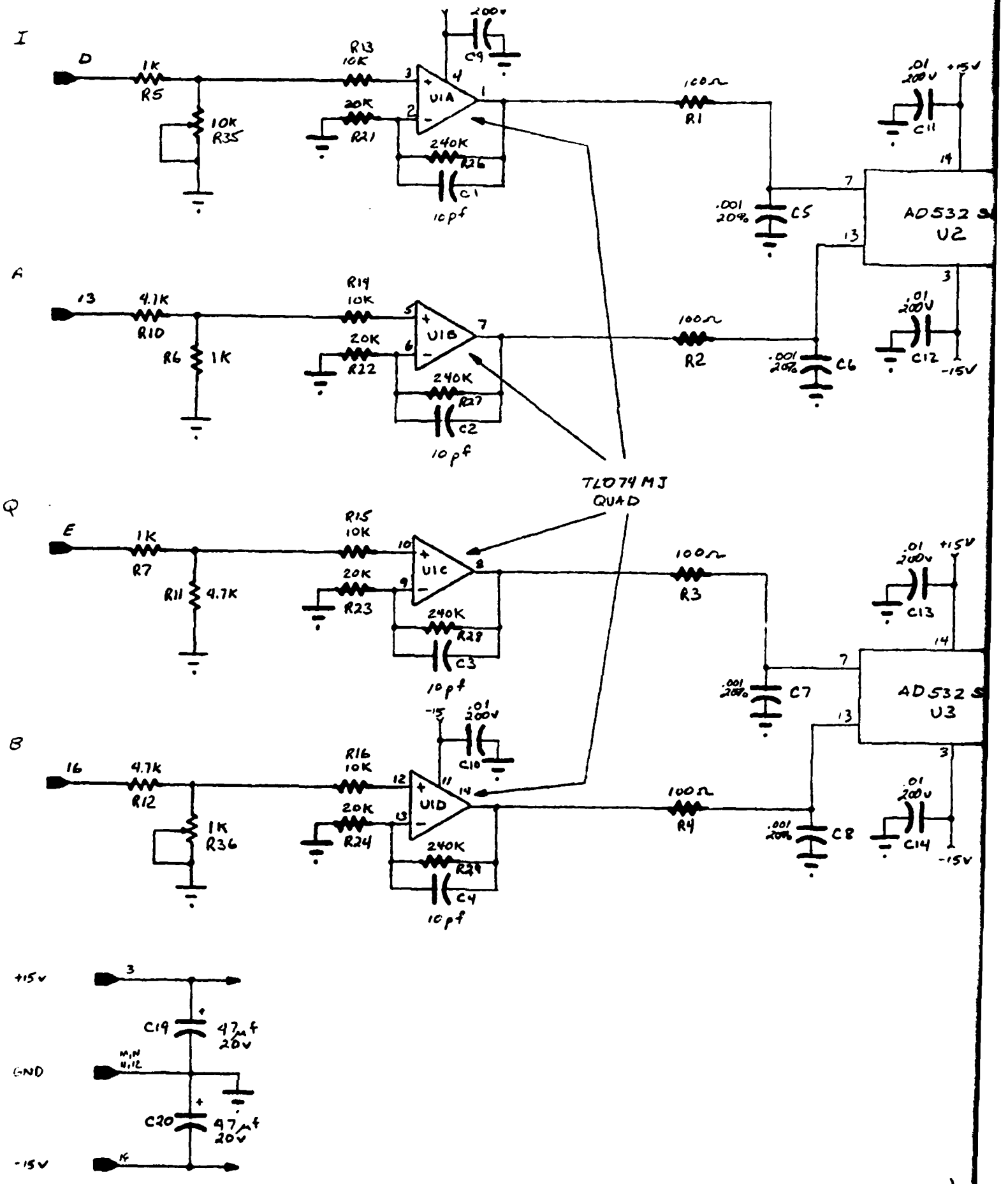


SCHEMATIC: ZERO-IF LOW NOISE AMPLIFIER

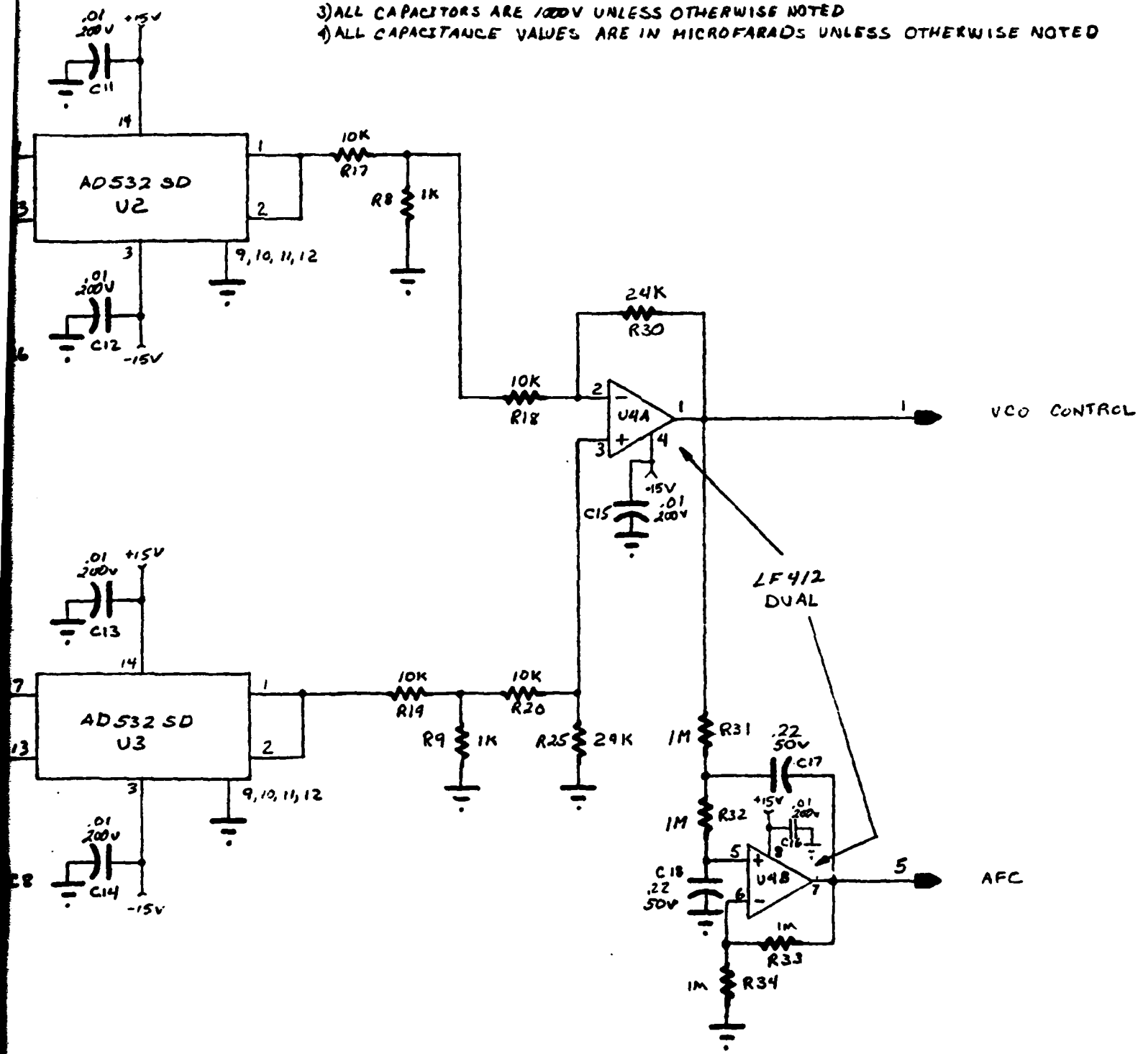

I CHANNEL IN
Q CHANNEL IN
DG308
TL074MJ (QUAD)
CD4001
CD4071
MC14011
MSBAGC
MSBRF
CLOCK
MODE CONTROL
820K
20K
196K
10K
24K
NOTES 1) ALL RESISTORS ARE ¼ WATT 5% UNLESS OTHERWISE SPECIFIED



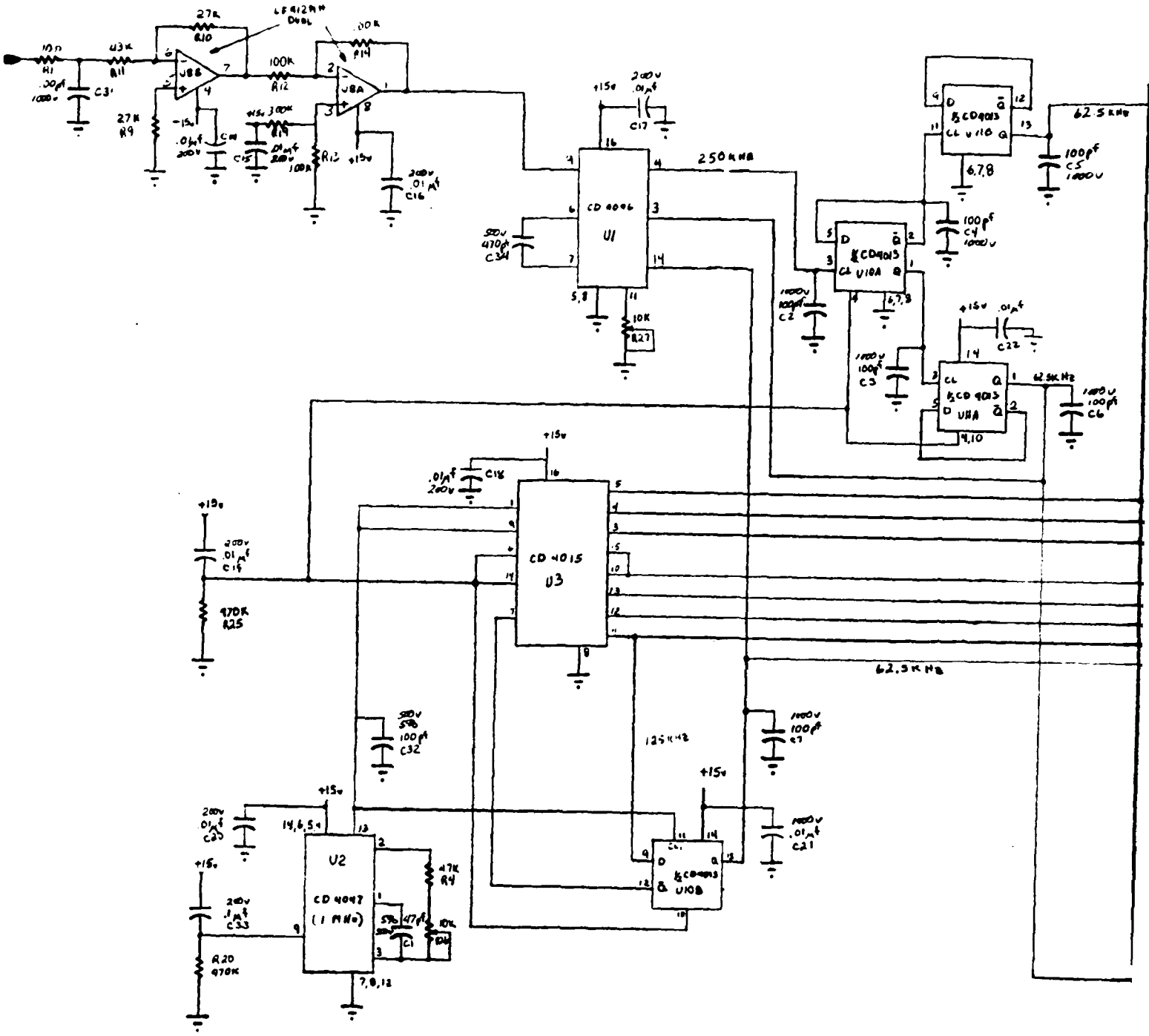
SCHEMATIC: ZERO-IF BASEBAND AGC


I
D
1K
R5
10K
R35
R13
10K
20K
R21
200v
C9
U1A
240K
R26
C1
10pf
100Ω
R1
.01
200v
+15v
C11
14
7
.001
20%
C5
AD532 S
U2
13
3
.01
200v
C12
-15v
A
13
4.1K
R10
R6
1K
R19
10K
20K
R22
U1B
240K
R27
C2
10pf
100Ω
R2
.001
20%
C6
TL074 MJ
QUAD
Q
E
1K
R7
R11
4.7K
R15
10K
20K
R23
U1C
240K
R28
C3
10pf
100Ω
R3
.01
200v
+15v
C13
14
7
.001
20%
C7
AD532 S
U3
13
3
.01
200v
C14
-15v
B
16
4.7K
R12
1K
R36
R16
10K
20K
R24
U1D
240K
R29
C4
10pf
-15v
.01
200v
C10
100Ω
R4
.001
20%
C8
+15v
3
C19
47μf
20v
GND
MIN
W.12
C20
47μf
20v
-15v
K

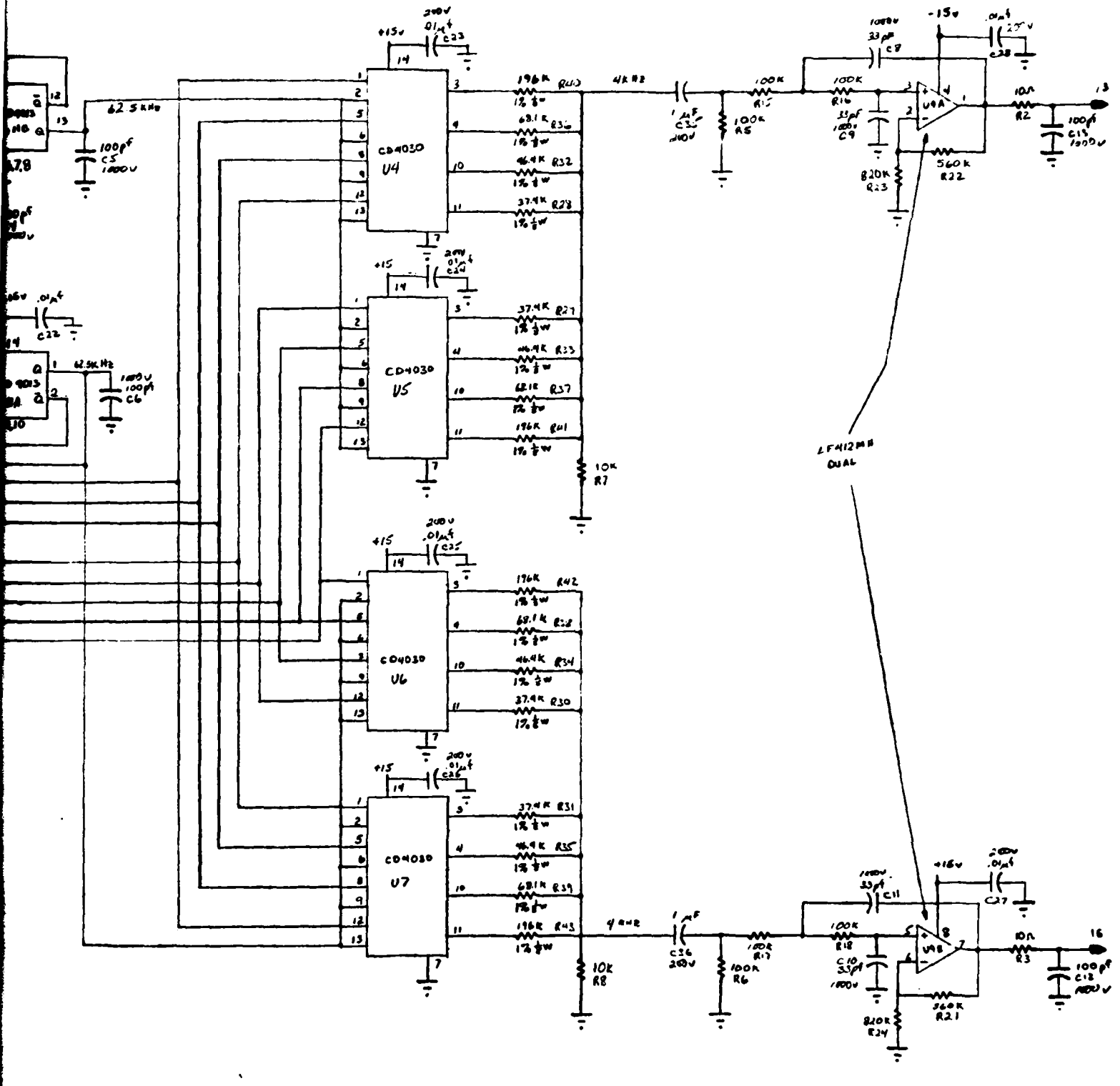
NOTES: 1) ALL RESISTORS ARE ¼W, 5%
2) ALL CAPACITORS ARE 10% TOLERANCE UNLESS OTHERWISE NOTED
3) ALL CAPACITORS ARE 100V UNLESS OTHERWISE NOTED
4) ALL CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED



SCHEMATIC: ZERO-IF BASEBAND MULTIPLIERS



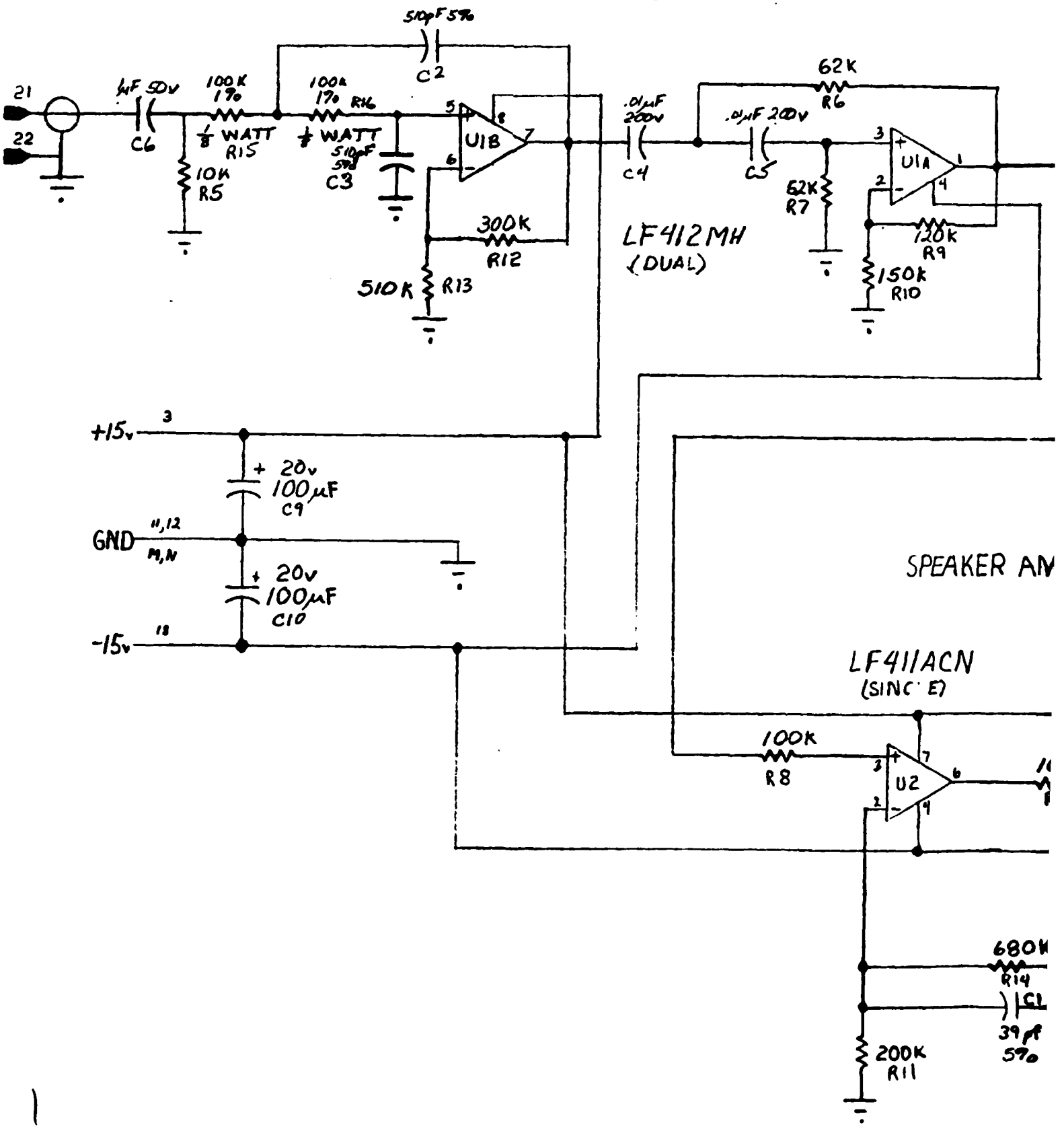
NOTES 1) ALL RESISTORS ARE ¼ W 5%, UNLESS OTHERWISE NOTED
2) ALL CAPACITORS ARE 10% TOLERANCE UNLESS OTHERWISE NOTED
3) ALL INDUCTORS ARE 20% TOLERANCE PART # MS75054-1

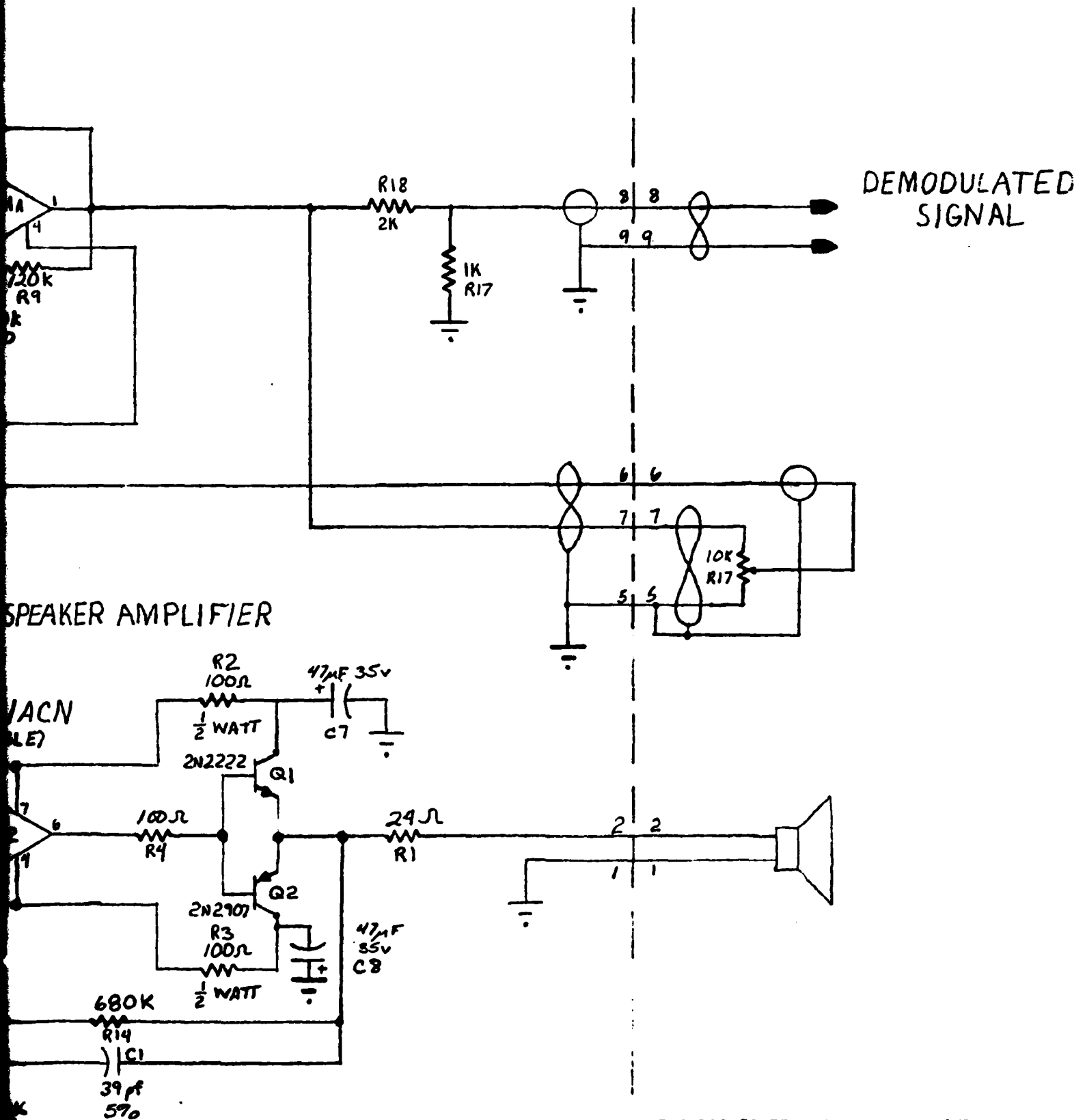


SCHEMATIC: ZERO-IF BASEBAND OSCILLATOR AND VCO

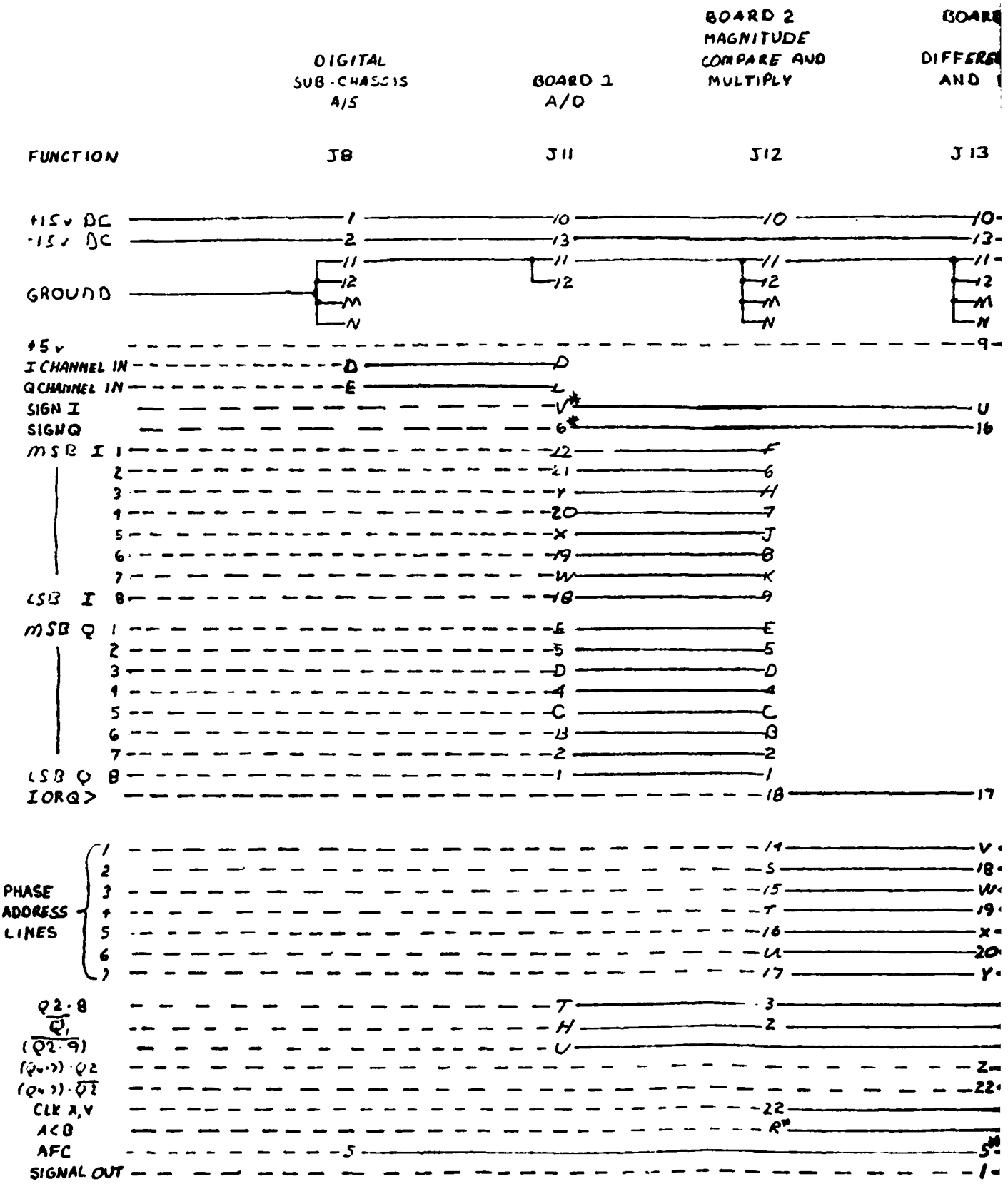
NOTES 1) ALL RESISTORS ARE 5% ¼ WATT UNLESS OTHERWISE NOTED
2) ALL CAPACITORS ARE 10%, 50V UNLESS OTHERWISE NOTED
3) COMPONENTS ON THE RIGHT OF DASHED LINE MOUNTED OFF BOARD

AUDIO FILTERS

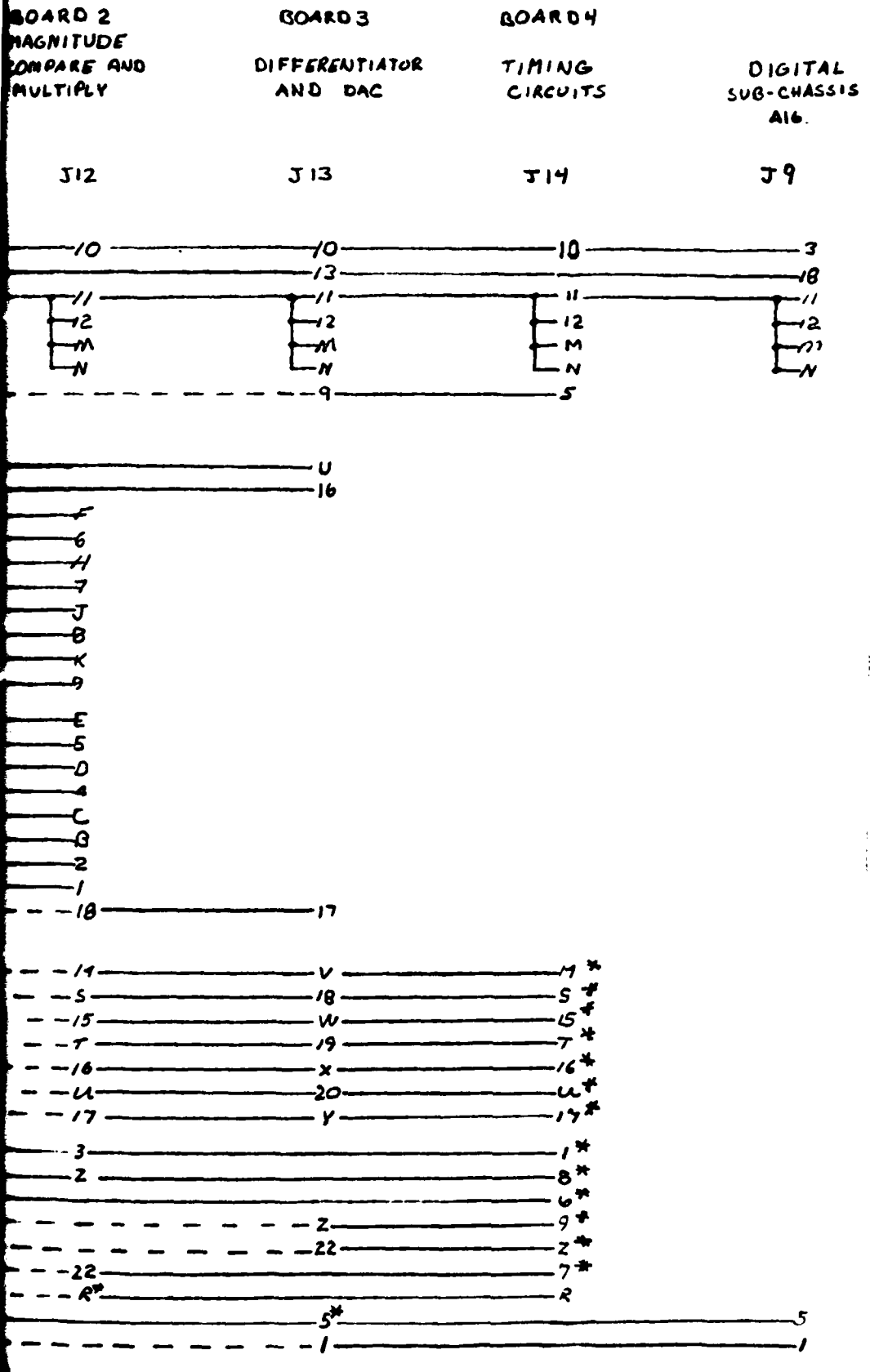




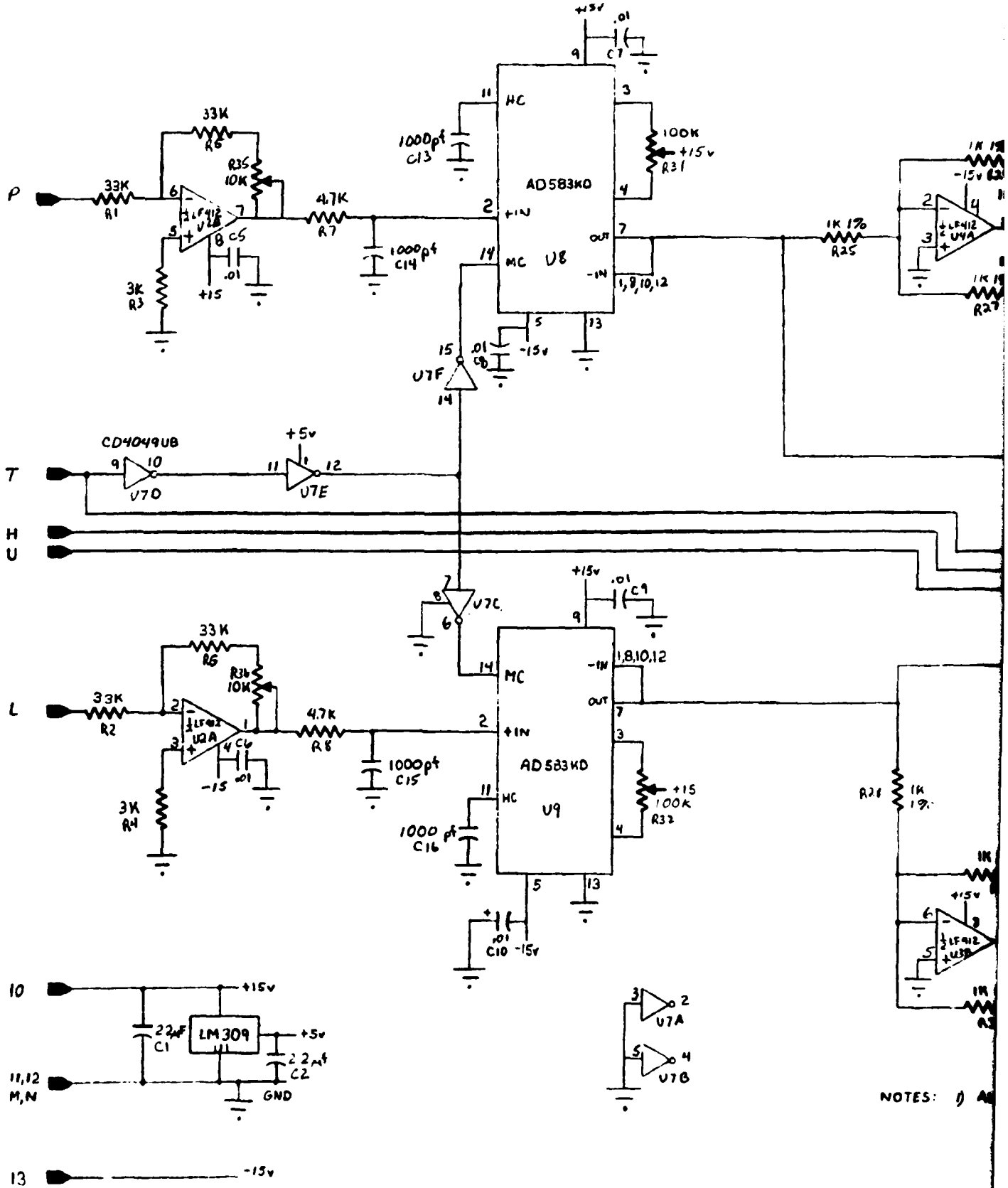
SCHEMATIC: ZERO-IF AUDIO FILTERS AND SPEAKER AMP

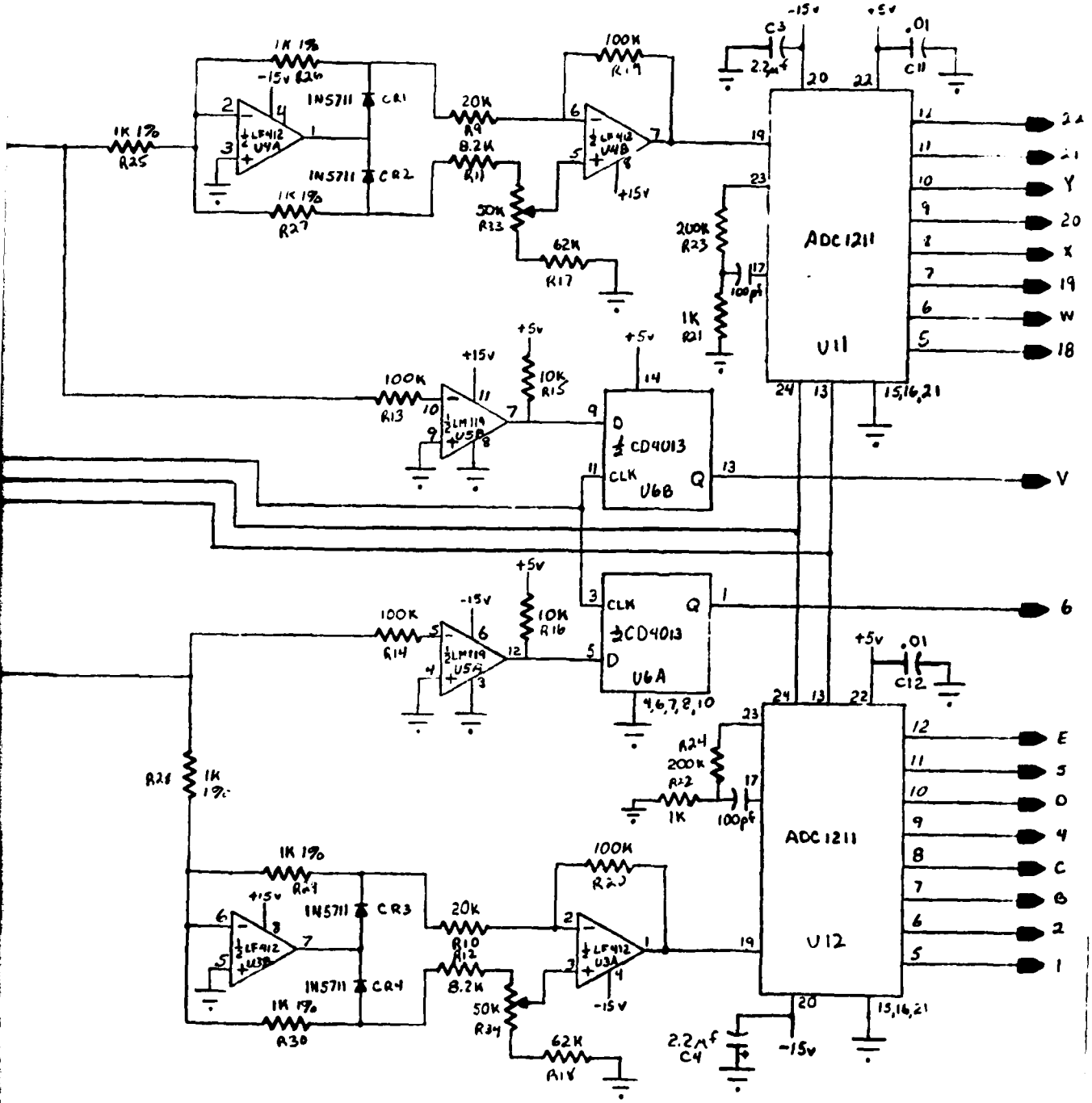


* DENOTES SIGNAL SOURCE



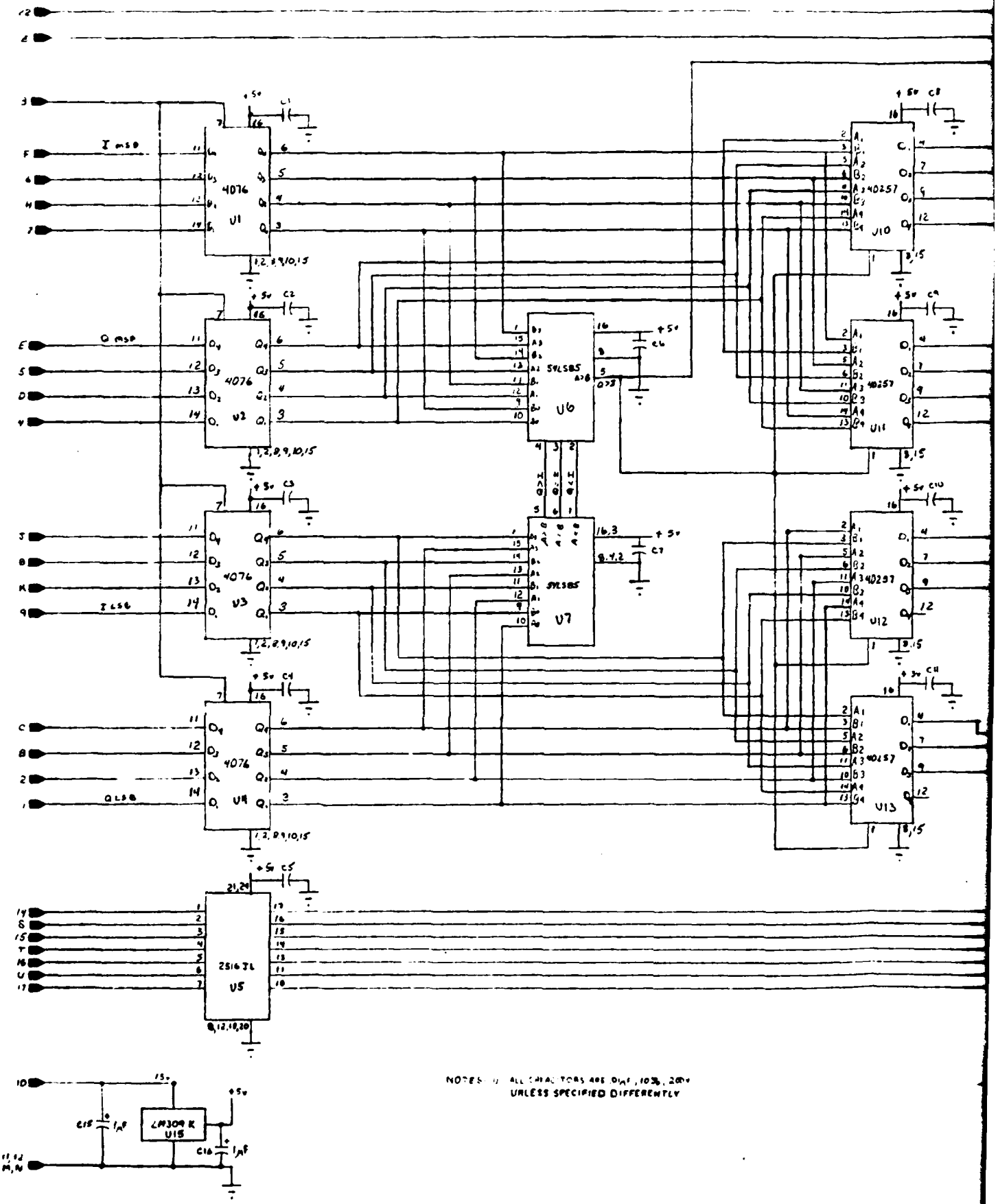
SCHEMATIC: ZERO-IF DIGITAL SUB-CHASSIS WIRING DIAGRAM


P
33K R1
33K R6
R36 10K
½ LF412 U2B
4.7K R7
1000pf C14
3K R3
.01 C5
+15
AD583KD
U8
1000pf C13
100K R31
+15v
-15v
.01 C8
U7F
1K 1% R25
½ LF412 U4A
T
CD4049UB
U7D
+5v
U7E
H
U
U7C
+15v
.01 C9
L
33K R2
33K R5
R36 10K
½ LF412 U2A
4.7K R8
1000pf C15
3K R4
.01 C6
-15
AD583KD
U9
1000 pf C16
+15 100K R32
.01 C10 -15v
R28 1K 1%
1K
10
11,12 M,N
13
+15v
22µF C1
LM309
+5v
22µf C2
GND
U7A
U7B
-15v
NOTES: 1)

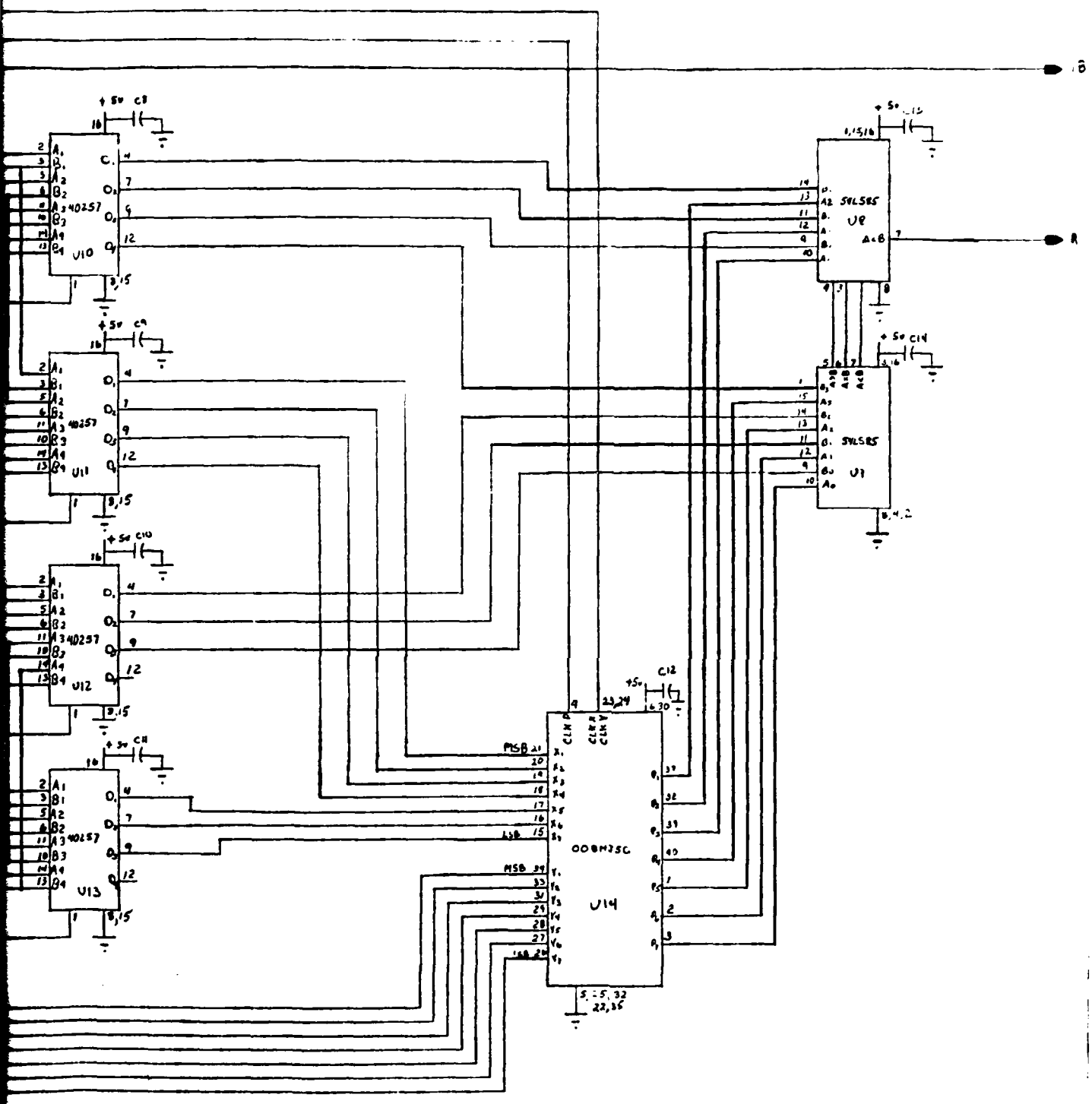


NOTES: 1) ALL RESISTORS ARE $\frac{1}{8}$ WATT, 5%

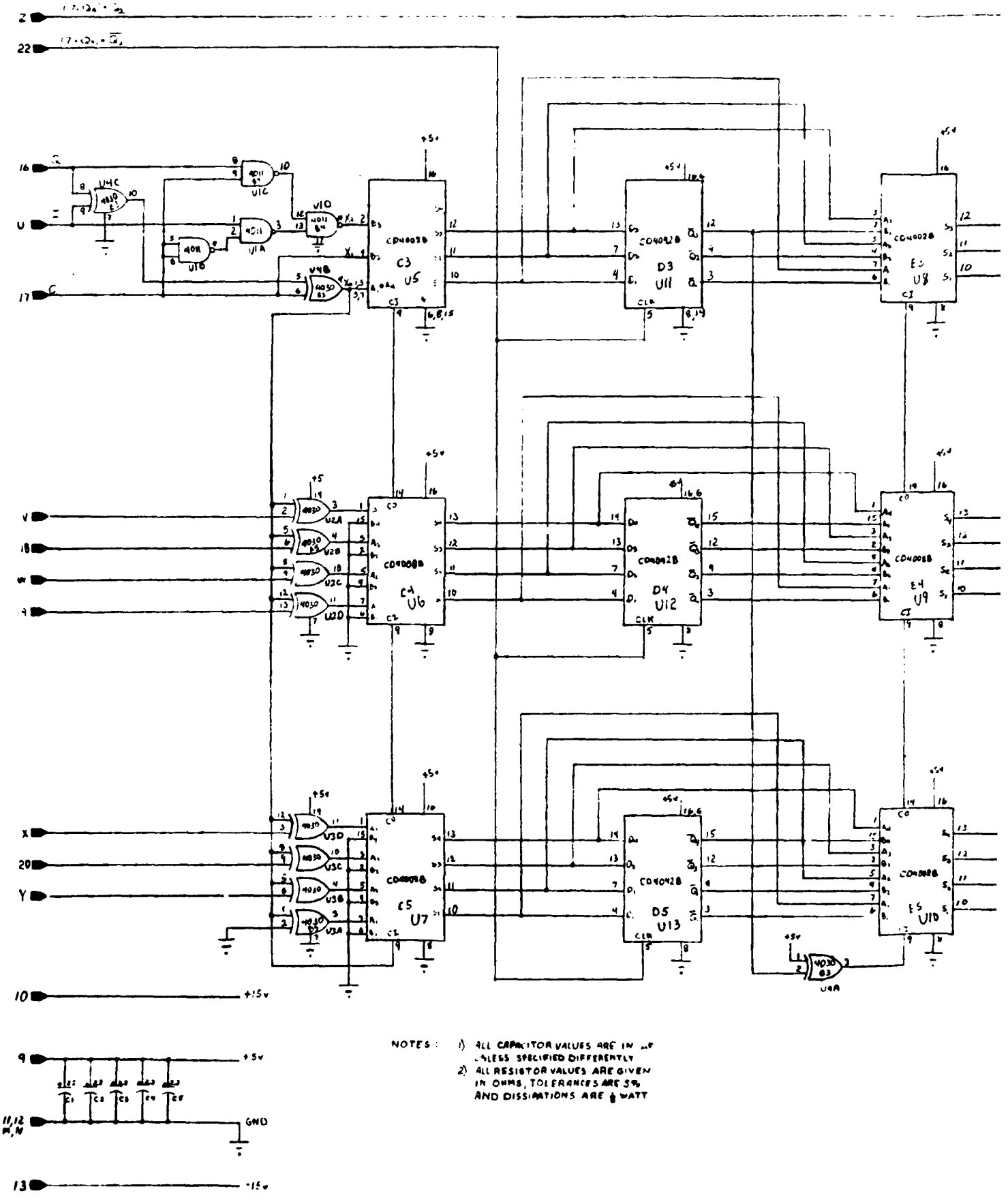
SCHEMATIC: ZERO-IF SAMPLE AND HOLD AND A TO D



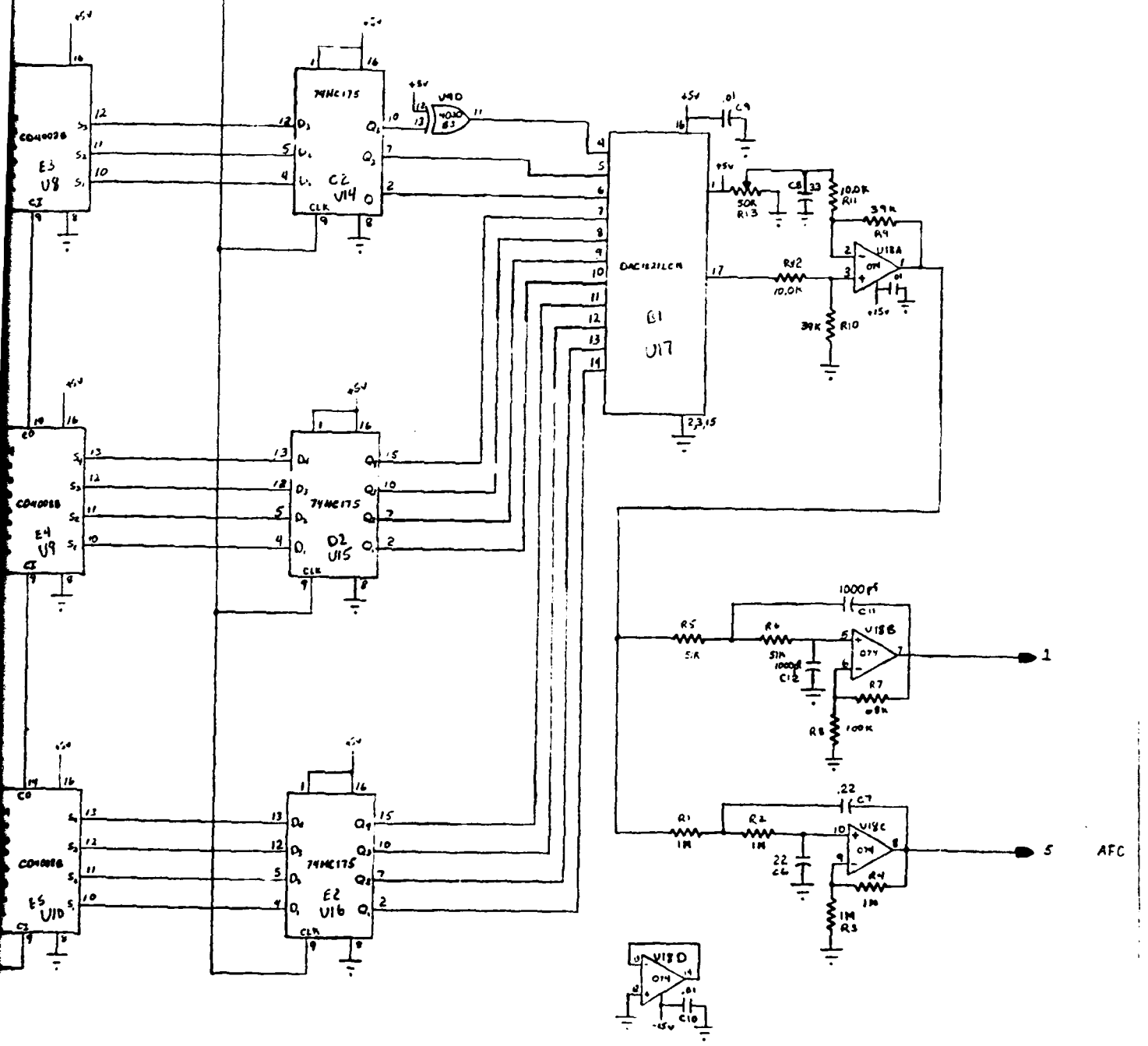
NOTES: 1) ALL CAPACITORS ARE 0.1μF, 10%, 20V+ UNLESS SPECIFIED DIFFERENTLY



SCHEMATIC: ZERO-IF MAGNITUDE COMPARE AND MULTIPLY



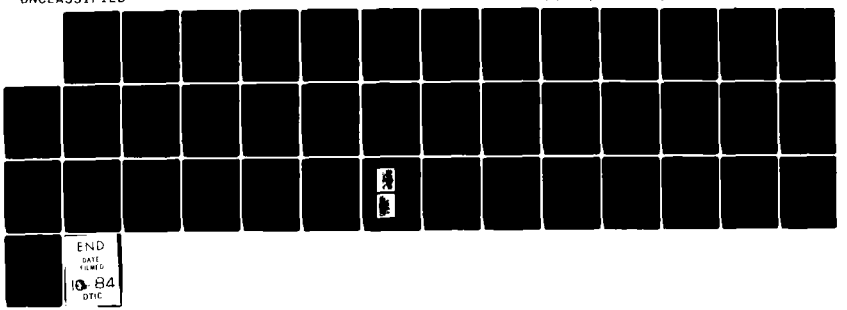
NOTES:
1) ALL CAPACITOR VALUES ARE IN μF UNLESS SPECIFIED DIFFERENTLY
2) ALL RESISTOR VALUES ARE GIVEN IN OHMS, TOLERANCES ARE 5% AND DISSIPATIONS ARE ¼ WATT



SCHEMATIC: ZERO-IF DIFFERENTIATOR AND DAC

AD-A145 694 ZERO-IF RECEIVER STUDY REVISION(U) ITT AEROSPACE/OPTICAL DIV FORT WAYNE IND E J NEYENS ET AL. 10 JUN 83 ITT-A/OD-31174A003 DAAK80-81-C-0154 2/2

UNCLASSIFIED F/G 17/2.1 NL



END
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10-84
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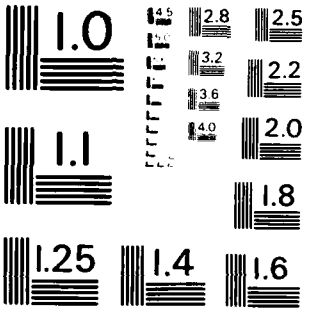
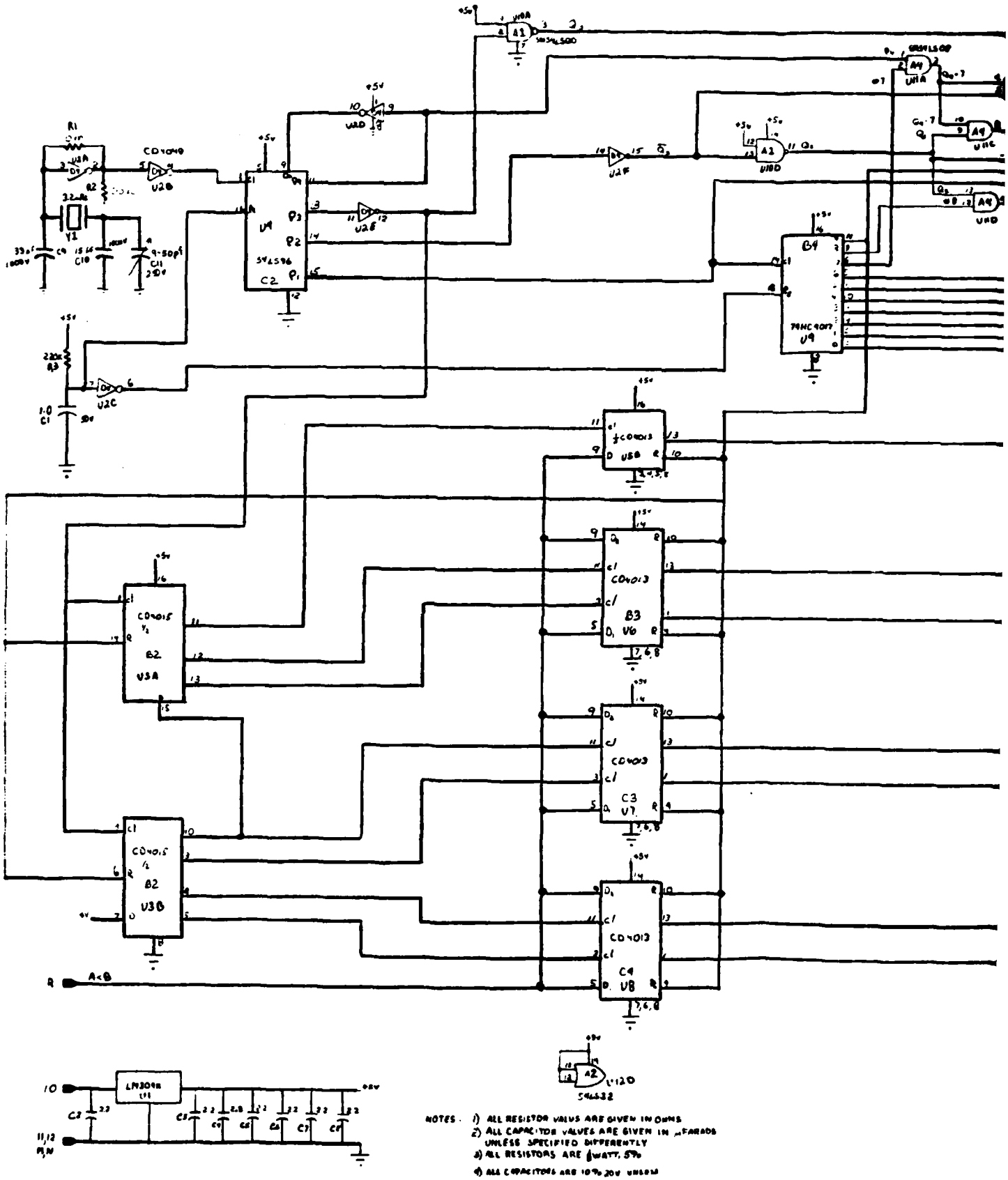
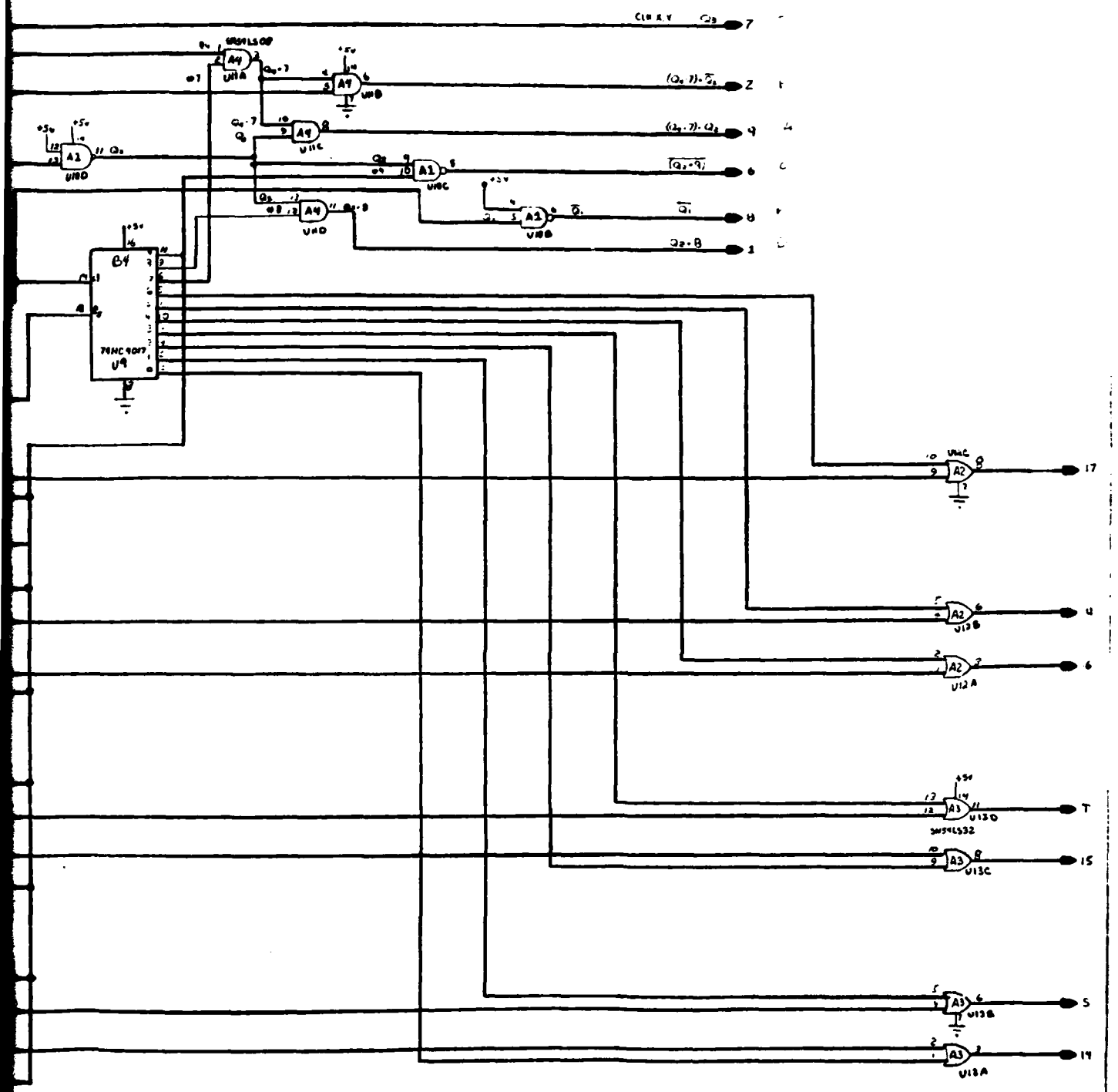


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A


R1
CD4049
U2B
32.4k
Y1
33pf
C9
15pf
C10
9-50pf
C11
250v
U4
74LS96
C2
U2A
U2D
U2F
U2E
U2C
220k
R3
1.0
C1
50v
U1A
U1B
U1C
U1D
B4
74HC4017
U9
CD4013
B3
U6
CD4015
B2
U5A
U5B
C3
U7
C4
U8
A<B
LM309K
U11
U12D
74LS32
NOTES:
1) ALL RESISTOR VALUES ARE GIVEN IN OHMS
2) ALL CAPACITOR VALUES ARE GIVEN IN μFARADS UNLESS SPECIFIED DIFFERENTLY
3) ALL RESISTORS ARE ¼WATT, 5%
4) ALL CAPACITORS ARE 10% 20V UNLESS SPECIFIED DIFFERENTLY



SCHEMATIC: ZERO-IF DIGITAL TIMING CIRCUITS

FORT WAYNE
AEROSPACE / OPTICAL DIVISION

BID PARTS LIST

PREPARED BY D. J. Schwarz

DATE 3-22-83

COMPLETE INFORMATION BLOCKS ON FIRST SHEET ONLY

ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Chassis Part # 31174-100				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	5			Vector P/N R644	Board Edge Connector						Vector
2	4			502070-3	BNC to SMC Bulkhead Connector						ITT
3	2			31-010	BNC Bulkhead Insulating Connector						Amphenol
4	12				Capacitive Feedthrough						
5	2				Terminal Strip 4 Pin						
6	16				Solder Lugs						
7	10				Metal Standoff 1/2"						
8	15				Metal Standoff 5/8"						
9	1			JH-131	90° Power Splitter						Anzac
10	2				Cable Assembly W1→W4						
11	2				Twisted Shielded Pair 14"						
12	1			12-1852	Speaker						Radio Shack
13	1				Potentiometer 10K						
14	1				3-position Switch						
15	1				Capacitor 3300 pf						
16	1			8006125	BNC Jumper						ITT
17	4				#4 Screw, Panhead 5/8"						
18	37				#4 Screw, Flathead 1/4"						
19	24				#4 Screw, Panhead 1/2"						
20	14				#4 Flat Washer						
21	10				#4 Lock Washer						
22	10				#4 Nut						
23	25				#6 Screws, Panhead 1/4"						
24	33				#6 Screws, Flathead						
25	4				#6 Lock Washers						
26	4				#6 Nuts						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Rcvr Chassis Part #31174-100				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
27	19				#6 Flat Washer						
28	25				LED Sockets						
29	2				Knobs						
30	3				Metal Standoff 1-1/2"						
31	2				Double Banana Plugs						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A1 Preselector Part # 31174-101				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	12				Capacitive Feed Through Stand Off						
2	6				Capacitive Stand Off						
3	6				Resistor 10 kΩ R1→R6						
4	6				Resistor 1.5kΩ R7→R12						
5	6			MA47047	PIN Diode CR1→CR6						Microwave Assoc.
6	8				Inductor 18,000 nh L1→L8						
7	1				Inductor 77 nh L9						
8	1				Inductor 105 nh L10						
9	1				Inductor 109 nh L11						
10	1				Inductor 110 nh L12						
11	1				Inductor 149 nh L13						
12	1				Inductor 150 nh L14						
13	1				Inductor 158 nh L15						
14	1				Inductor 159 nh L16						
1[illegible]	1				Inductor 215 nh L17						
[illegible]	1				Inductor 216 nh L18						
17	1				Inductor 228 nh L19						
18	1				Inductor 310 nh L20						
19	1				Chip Capacitor 2 pf C1						
20	1				Chip Capacitor 3 pf C2						
21	1				Chip Capacitor 3.3 pf C3						
22	1				Chip Capacitor 5.1 pf C4						
23	5				Chip Capacitor 6.8 pf C5-C9						
24	1				Chip Capacitor 7.5 pf C10						
25	2				Chip Capacitor 8.2 pf C11, C12						
26	4				Chip Capacitor 10 pf C13→C16						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A1 Preselector Part # 31174-101				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
27	2				Chip Capacitor 12 pf C17, C18						
28	2				Chip Capacitor 13 pf C19, C20						
29	2				Chip Capacitor 15 pf C21, C22						
30	1				Chip Capacitor 18 pf C23						
31	4				Chip Capacitor 22 pf C24→C27						
32	4				Chip Capacitor 27 pf C28→C31						
33	2				Chip Capacitor 33 pf C32, C33						
34	3				Chip Capacitor 39 pf C34→C36						
35	4				Chip Capacitor 47 pf C37→C40						
36	6				Chip Capacitor 56 pf C41→C46						
37	3				Chip Capacitor 68 pf C47→C49						
38	2				Chip Capacitor 75 pf C50, C51						
39	3				Chip Capacitor 82 pf C52→C54						
40	1				Chip Capacitor 100 pf C55						
41	1				Chip Capacitor 120 pf C56						
42	1				Chip Capacitor 200 pf C57						
43	1				Chip Capacitor 330 pf C58						
44	1				Chip Capacitor 470 pf C59						
45	2			RG316	Coaxial Cable 3"						
46	2				Coaxial Cable Connectors SMC						
47	4			CA50034	Coaxial Tube 1.5"						Precision Tube

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A2 RF Amplifier Attenuator Part #31174-102				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			QBH-104	RF Amplifier U1						Q-Bit
2	1			QBH-102	RF Amplifier U2						Q-Bit
3	6				Resistor 1500Ω R1→R6						
4	4				Resistor 36Ω R7-R10						
5	2				Resistor 27Ω R11,R12						
6	2				Resistor 3.9Ω R13,R14						
7	6			MA47047	PIN Diode CR1-CR6						Microwave Assoc.
8	5				Capacitor .01 µf C1→C4						
9	6				Capacitor .001 µf C5→C8						
10	1				Inductor 15 µh L1						
11	4			CA50034	Coaxial Tube 1/2"						Precision Tube
12	2				Bulkhead Connectors SMC						
13	8				Capacitive Standoff						
14	1			MM54C95J	Shift Register						National
15	3			IH5051CDE	Low Resistance Dual SPDT Switch						Intersil
16	6				Resistor 10K R1-R6						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A3 Splitter Mixer Part # 31174-103				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			PDS-20-50	0° Splitter U1						Merrimac
2	2			MCL-SBL-1	RF Mixer U2,U3						Mini Circuits Lab
3	2				Bulkhead Connectors SMC						
4	4			CA50034	Coaxial Tube 2"						Precision Tube
5	3				90° Cable Connectors SMC						
6	3			RG316	Coaxial Cable 8"						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A4 8 kHz Low Pass Filters Part # 31174-104				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	2				Inductor 1.333 mh L1,L3						
2	2				Inductor 1.266 mh L2,L4						
3	2				Capacitor .0012 µf C1,C2						
4	6				Capacitor .01 µf C3-C8						
5	2				Capacitor .02 µf C9,C10						
6	2				Capacitor .047 µf C11,C12						
7	4				Capacitor .18 µf C13-C16						
8	2				Capacitor .33 µf C17,C18						
9	2				Capacitor .68 µf C19,C20						
10	4				Bulkhead Coaxial Connector SMC						

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DATE 3-22-83

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A5 Low Noise Amplifier Part # 31174-105				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION			UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	2			CPC-03	Transformers	40:1	T1,T2						TRW
2	2				Capacitor	22 pf	C1,C2						
3	2				Capacitor	100 pf	C3,C4						
4	2				Capacitor	120 pf	C5,C6						
5	6				Capacitor	100 µf	C7→C12						
6	4				Resistor	51Ω	R1→R4						
7	4				Resistor	43K	R5→R8						
8	4				Resistor	100K	R9→R12						
9	2				Resistor	470K	R13,R14						
10	4				Resistor	560K	R15→R18						
11	2				Capacitor	1 µf	C13,C14						
12	2			LH0044	Single Low Noise OP AMP		U1,U2						National
13	1			LF412	Dual OP AMP		U3						National
14	2				Twisted Shielded Pair 3"								
15	2				Coaxial Cable 8"								

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DATE 3-22-83

COMPLETE INFORMATION BLOCKS ON FIRST SHEET ONLY

ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A6 AGC Circuit Part # 31174-106				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	3			TL074MJ	Quad OP AMP U1-U3						Texas Instruments
2	1			LF412MH	Dual OP AMP U4						National
3	2			MM54C95J	Shift Register U5,U6						National
4	4			DG308CJ	Analog Switch U7-U10						Siliconix
5	1			CD4047	Multivibrator U11						RCA
6	1			MC14011	Quad NAND Gate U12						Motorola
7	1			CD4001	Quad NOR Gate U13						RCA
8	1			CD4071	Quad OR Gate U14						RCA
9	1				Resistor 470Ω R1						
10	2				Resistor 1K R2,R3						
11	4				Resistor 1.3K R4→R7						
12	4				Resistor 2K R8→R11						
13	4				Resistor 3K R12→R15						
14	3				Resistor 4.7K R16→R18						
15	5				Resistor 6.2K R19→R22						
16	1				Resistor 6.8K R23						
17	10				Resistor 10K R24→R33						
18	4				Resistor 15K R34→R37						
19	5				Resistor 20K R38→R42						
20	6				Resistor 51K R43,44,46,47						
21	4				Resistor 47K R49,R50,R53,R54						
22	2				Resistor 56K R51,R52						
23	4				Resistor 62K R55→R58						
24	6				Resistor 100K R59→R64,R92,R93						
25	1				Resistor 130K R65						
26	5				Resistor 470K R66→R69,R77						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A6 AGC Circuit Part # 31174-106				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
27	2				Resistor 510K R70,R71						
28	4				Resistor 910K R72→R75						
29	1				Resistor 820K R76						
30	6				Resistor 1M R78→R83						
31	2				Precision Resistor 10.0K R84,R85						
32	2				Precision Resistor 40.2K R86,R87						
33	4				Precision Resistor 196K R88→R91						
34	2				Capacitor 2.2 pf C1,C2						
35	4				Capacitor 82 pf C3→C6						
36	2				Capacitor 220 pf C7,C8						
37	2				Capacitor 100 pf C9,C10						
38	2				Capacitor .001 µf C11,C12						
39	2				Capacitor .01 µf C13,C14						
40	2				Capacitor .1 µf C15,C16						
41	4				Capacitor 1 µf C17→C20						
42	1				Capacitor 10 µf C21						
43	2				Capacitor 100 µf C22,C23						
44	4			1N4148	Diode CR1→CR4						
45	1			1N751A	Zener Diode VR1						
46	2			2N2222	Transistor Q1,Q2						Motorola
47	2			2N2907	Transistor Q3,Q4						Motorola
48	2			2N4416	Transistor Q5,Q6						Siliconix
49	2				Resistor 820K R45,R48						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A7 Baseband Multiplier Part # 31174-107				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION		UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			TL074MJ	Quad OP AMP	U1						Texas Instruments
2	2			AD532SD	Internally Trimmed Multiplier	U2,U3						Analog Devices
3	1			LF412MH	Dual OP AMP	U4						National
4	4				Resistor 100Ω	R1→R4						
5	5				Resistor 1K	R5→R9						
6	3				Resistor 4.7K	R10→R12						
7	8				Resistor 10K	R13→R20						
8	4				Resistor 20K	R21→R24						
9	1				Resistor 24K	R25						
10	4				Resistor 240K	R26→R29						
11	1				Resistor 100K	R30						
12	4				Resistor 1M	R31→R34						
13	4				Capacitor 10 pf	C1-C4						
14	4				Capacitor .001 µf	C5→C8						
15	8				Capacitor .01 µf	C9→C16						
16	2				Capacitor .22 µf	C17,C18						
17	2				Capacitor 47 µf	C19,C20						
18	1				Potentiometer 10K	R35						
19	1				Potentiometer 1K	R36						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A8 Baseband VCO & Oscillator Part 31174-108				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION		UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			CD4046AE	Phase Locked Loop							RCA
2	1			CD4047AE	Multivibrator	U2						RCA
3	1			CD4015AE	Shift Register (Dual 4-bit)	U3						RCA
4	4			CD4030A3	Quad Exclusive OR	U4→U7						RCA
5	2			LF412MH	Dual OP AMP	U8,U9						National
6	2			CD4013BE	Dual D Flip Flop	U10,U11						RCA
7	2				Resistor 10Ω	R2,R3						
8	1				Resistor 4.7K	R4						
9	2				Resistor 10K	R5,R6						
10	2				Resistor 1K	R7,R8						
11	2				Resistor 27K	R9,R10						
12	1				Resistor 43K	R11						
13	3				Resistor 100K	R12→R14						
14	4				Resistor 270K	R15→R18						
15	1				Resistor 300K	R19						
16	2				Resistor 470K	R20,R25						
17	2				Resistor 560K	R21,R22						
18	2				Resistor 820K	R23,R24						
19	2				Potentiometer 10K	R26,R27						
20	1				Capacitor 47 pf	C1						
21	15				Capacitor 100 pf	C2→C13,						
						C29→C32						
22	15				Capacitor .01 µf	C14→C28						
23	1				Resistor 100Ω	R1						
24	1				Capacitor .1 µf	C33						
25	1				Capacitor 470 pf	C34						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A8 Baseband VCO & Oscillator Part 31174-108				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
26	2				Capacitor 1 µf C35,C36						
27	2				Capacitor 100 µf C37,C38						
28	4				Precision Resistor 37.4K R28→R31						
29	4				Precision Resistor 46.4K R32→R35						
30	4				Precision Resistor 68.1K R36→R39						
31	4				Precision Resistor 196K R40→R43						
32	2				Inductor 470 µh L1,L2						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A9 Audio Board Part # 31174-109				

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION		UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			LF412MH	Dual OP AMP	U1						National
2	1			LF411ACN	Single OP AMP	U2						National
3	1			2N2222	Transistor	Q1						Motorola
4	1			2N2907	Transistor	Q2						Motorola
5	1				Resistor 24Ω	R1						
6	3				Resistor 100Ω	R2÷R4						
7	1				Resistor 10K	R5						
8	2				Resistor 62K	R6,R7						
9	1				Resistor 100K	R8						
10	1				Resistor 120K	R9						
11	1				Resistor 150K	R10						
12	1				Resistor 200K	R11						
13	1				Resistor 390K	R12						
14	1				Resistor 510K	R13						
15	1				Resistor 680K	R14						
16	2				Precision Resistor 100K	R15,R16						
17	1				Capacitor 39 pf	C1						
18	2				Capacitor 510 pf	C2,C3						
19	2				Capacitor 0.1 µf	C4,C5						
20	1				Capacitor 1 µf	C6						
21	2				Capacitor 47 µf	C7,C8						
22	2				Capacitor 100 µf	C9,C10						
23	1				Resistor 1K	R17						
24	1				Resistor 2K	R18						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Digital Demod, Sub Chassis Part # 31174-110				(6)

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	2			4112-4	Vector Boards						Vector
2	4			R644	Board Edge Connector						Vector
3	8				#4 Screw, Panhead 1/2"						
4	16				#4 Flat Washer						
5	16				#4 Lock Washer						
6	8				#4 Nut						
7	8				Metal Standoff 1/4"						
8	16				#4 Screw 1/4"						
9					Epoxy Glass Sheet .01"						
10	2				Nylon Clamps						
11	2				#8 Screw Panhead 1/2"						
12	2				#8 Flat Washer						
13	2				#8 Lock Washer						
14	2				#8 Nut						

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A10 Sample and Hold A/D Part # 31174-111				(2)

ITEM NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	4				Capacitor 2.2 μF (C1-C4)						
2	8				Capacitor .01 μF (C5-12)						
3	4				Capacitor 1000 pF (C13-16)						
4	2				Resistor 33K (R1,2)						
5	2				Resistor 3K (R3,4)						
6	2				Resistor 33K (R5,6)						
7	2				Resistor 4.7K (R7,8)						
8	2				Resistor 20K (R9,10)						
9	2				Resistor 8.2K (R11,12)						
10	2				Resistor 100K (R13,14)						
11	2				Resistor 10K (R15,16)						
12	2				Resistor 62K (R17,18)						
13	2				Resistor 100K (R19,20)						
14	2				Resistor 1K (R21,22)						
15	2				Resistor 200K (R23,24)						
16	6				Precision Resistor 1K (R25-30)						
17	4			IN5711	Diode (CR1-24)						
18	4			7633FW503	Potentiometer 100K (R31-34)						Bourns
19	2			8633FW103	Potentiometer 10K (R35,36)						Bourns
20	1			LM309K	5V Regulator (U1)						National
21	3			LF412MH	Dual OPAMP (U2-4)						National
22	1			LM119J	Dual Comparator (U5)						National
23	1			CD4013BE	Dual D Flip-Flop (U6)						RCA
24	1			CD4049UBE	Hex Inverter (U7)						RCA
25	2			AD583KD	Sample and Hold (U8,9)						Analog Devices
26	2			ADC1211HCD	Analog to Digital Converter (U11,12)						National

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A11 Mag. Compare and Multiply Part # 31174-112				(3)

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	14				Capacitor 0.1 µF (C1-14)						
2	2				Capacitor 1 µF (C15-16)						
3	4			CD4076BE	Quad D Latch (U1-4)						RCA
4	1			2516JL-45	EPROM (U5)						Texas Inst.
5	4			SN54LS85J	Magnitude Comparator (U6-9)						Texas Inst.
6	4			CD40257BE	AND OR Select (U10-13)						RCA
7	1			008HJ5C	Multiplier (U14)						TRW
8	1			LM309K	5V Regulator (U15)						National
9	1			5012B	Heat Sink						Aavid Eng.

ITT FW D120 (REV 9/78)

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A12 Differentiator and DAC Part # 31174-113				(4)

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	5				Capacitor 2.2 µF (C1-5)						
2	2				Capacitor .22 µF (C6-7)						
3	1				Capacitor 3.3 µF (C8)						
4	2				Capacitor .01 µF (C9,10)						
5	2				Capacitor 1000 pf (C11,12)						
6	4				Resistor 1MΩ (R1-4)						
7	2				Resistor 51KΩ (R5,6)						
8	2				Resistor 39K (R9,10)						
9	2				Precision Resistor 10K (R11,12)						
10	1			7633FW503	Potentiometer 50K (R13)						Bourns
11	1				Resistor 68K (R7)						
12	1				Resistor 100K (R8)						
13	1			CD4011BE	Quad NAND Gate (U1)						RCA
14	3			CD4030BE	Quad XOR Gate (U2-4)						RCA
15	3			CD4008BF	4-Bit Adder (U5-10)						RCA
16	6			CD4042BE	Quad D Latch (U11-13)						RCA
17	3			MC74HC175	Quad D Flip-Flop (U14-16)						Motorola
18	1			DAC1221LCN	12-Bit D to A Converter (U17)						National
19	1			TL074MJ	Quad OPAMP (U18)						Texas Inst.

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ASSEMBLY NO.	DESCRIPTION	QTY	BID NUMBER	BID COMPLETION DATE	ENGINEERING CONTACT
	Zero-IF Receiver Board A13 Timing Circuits Part # 31174-114				(5)

NO.	QTY/GROUP G1	QTY/GROUP G2	MAKE-BUY CODE	PART NUMBER	DESCRIPTION	UNIT COST	EXTENDED COST	MIL	HI REL	COMM	VENDOR
1	1			LM309K	5V Regulator (U1)						National
2	1			CD4049UB	Hex Inverter (U2)						RCA
3	1			CD4015BE	Dual 4-Bit Shitf Register (U3)						RCA
4	1			SN54LS96J	5-Bit Shift Register (U4)						Texas Inst.
5	4			CD4013BE	Dual D Flip-Flop (U5-8)						RCA
6	1			MC74HC4017	Decade Counter (U9)						Motorola
7	1			JAN3.2000	3.2 MHz Crystal Oscillator (Y1)						JAN
8	1			SN54LS00J	Quad NAND Gate (U10)						Texas Inst.
9	1			SN54LS08J	Quad AND Gate (U11)						Texas Inst.
10	2			SN54LS32J	Quad OR Gate (U12,U13)						Texas Inst.
11	1				Resistor 10M (R1)						
12	1				Resistor 510Ω (R2)						
13	1				Resistor 220K (R3)						
14	1				Capacitor 1 µF (C1)						
15	7				Capacitor 2.2 µF (C2-8)						
16	1				Capacitor 33 pF (C9)						
17	1				Capacitor 15 pF (C10)						
18	1			JMC9376	Variable Capacitor 9-50 pF (C11)						Johanson

```
      IMPLICIT REAL*8 (A-H,O-Z)
      IMPLICIT INTEGER*4 (I-N)
      INTEGER*4 IND(6)
      REAL *8 ADTS(6)
      INTEGER*4 NPHA(9),KADA(9)
      INTEGER*4 KATD
      COMPLEX*8 SL(5),HK(5),YK(5),ET(5,5),U(5),YK1(5),ETJ,CXMJ
      COMPLEX*8 SUMJ,XMJC,DTSC,TDXC,DDTSC,TTDXC
      COMPLEX*8 TJ1(5),CTMJ,SUMT,TJ(5)
      DIMENSION SRMJ(20),SR(20)
      COMMON /RAND/IIO,III
C
C     ZERO IF SIMULATION PROGRAM
C
C     INPUT VARIABLES:
C     DF = FM FREQUENCY DEVIATION
C     FOD = CARRIER FREQUENCY OFFSET DIFFERENCE
C     TAI = I CHANNEL PHASE OFFSET
C     TAQ = Q CHANNEL PHASE OFFSET
C     TRC = TIME CONSTANT FOR MODULATION FILTER
C     DTS = A/D SAMPLING RATE
C     KAD = NUMBER OF A/D BITS FOR I AND Q SIGNALS
C     NPH = NUMBER OF PHASE QUANTIZATION LEVELS
C     ND = NUMBER OF DATA SAMPLES
C     VARN = VARIANCE OF NOISE MODULATION
C
      WRITE(1,1)
1     FORMAT(1X,'SIN WAVE RUN')
C     IP=1 THEN DEBUG PRINTOUT.
C     IP=1
      IP=0
      IIO=1
C     DF (KHZ)
C     FOD (KHZ)
C     TAI (RADIANS)
C     TAQ (RADIANS)
      DF=5.0
      FOD=0.0
      TAI=0.0
      TAQ=0.0
      WRITE(1,503)DF,FOD,TAI,TAQ
503   FORMAT(1X,'DF=',E12.4,2X,'FOD=',E12.4,2X,
     1'TAI=',E12.4,2X,'TAQ=',E12.4)
C     TRC (MILLISEC)
      TRC=0.053
      VARN=1.0
      NPHA(1)=2
      NPHA(2)=4
      NPHA(3)=8
      NPHA(4)=16
      NPHA(5)=32
      NPHA(6)=64
      NPHA(7)=128
      NPHA(8)=256
      NPHA(9)=512
      KADA(1)=2
      KADA(2)=4
      KADA(3)=6
      KADA(4)=8
      KADA(5)=12
      KADA(6)=16
      KADA(7)=10
      KADA(8)=11
      KADA(9)=12
C
      ADTS(1)=.05
      ADTS(2)=.05
      ADTS(3)=.025
      ADTS(4)=.0125
      ADTS(5)=.00625
      IND(1)=2000
      IND(5)=2000
      IND(3)=2000
      IND(2)=2000
      IND(4)=2000
C
C
C
C
```

```
      DO 2000 I1=1,1
      DTS=ADTS(I1)
      ND=IND(I1)
      WRITE(1,504)TRC,VARN,ND,DTS
504   FORMAT(1X,'TRC=',E12.4,1X,1X,'VARN=',
     1E12.4,1X,'ND=',I5,1X,'DTS=',E12.4)
      DO 1999 I2=6,8
      NPH=NPHA(I2)
      DO 1998 I3=1,2
      KAD=KADA(I3)
      WRITE(1,999)NPH,KAD
999   FORMAT(1X,'NPH=',I5,5X,'KAD=',I5)
      TMJ1=0.0D0
      PIE=4.0D0*DATAN(1.0D0)
      PIE2=8.0D0*DATAN(1.0D0)
      DCXM1=0.0D0
      EDC1=0.0D0
      SM21=0.0D0
      SE21=0.0D0
      XMDC1=0.0D0
      ETA1=0.0D0
      DO 101 IZ=1,20
      SR(IZ)=0.0D0
      SRMJ(IZ)=0.0D0
101   CONTINUE
C
C
C
C
C
C     4 POLE BUTTERWORTH LOW PASS FILTER
C     CHARACTERISTICS FB(3 DB POINT)=5KHZ
C     SL1,SL2,SL3,SL4 ARE THE LHP POLE LOCATIONS
C     FOR THE FILTER.   HK1,HK2,HK3,HK4 ARE THE
C     COMPLEX PARTIAL FRACTION EXPANSION COEFFICIENTS.
C
C
C
      FB=4.0D0
      WRITE(1,571)FB
571   FORMAT ('FB=',2X,F10.3)
      WB=2.0D0*PIE*FB
      SL(1)=(-0.3827,0.9239)
      SL(2)=(-0.9239,0.3827)
      SL(3)=(-0.9239,-0.3827)
      SL(4)=(-0.3827,-0.9239)
      HK(1)=(-0.4619,0.1913)
      HK(2)=(0.4619,-1.1151)
      HK(3)=(0.4619,1.1151)
      HK(4)=(-0.4619,-0.1913)
C
C
C
C
C     FM=1KHZ SINEWAVE
C
      FM=1.013
C
       BETA = DATAN(PIE*FM*DTS)
C     BETA =0.0
C
C
C
C     DELAY CALCULATIONS FOR 4-POLI
C
C     BUTTERWORTH FILTER
C
      W=FM/FB
      SUMD=0.0
      DO 400 I=1,4
      SGL=REAL(SL(I))
      GL=AIMAG(SL(I))
      TDL=SGL/(SGL*SGL+(W-GL)*(W-GL))
      SUMD=TDL+SUMD
400   CONTINUE
      TDL=-SUMD/WB
      IF(IP.EQ.1)WRITE(1,401)TDL
```

```
401   FORMAT('TDL=',E20.8)
C
C
      DTSC=CMPLX(SNGL(DTS),0.0)
      DO 30 I=1,4
C     MULTIPLY BY WB TO UNNORMALIZE POLES
      DDTSC=SL(I)*DTSC*WB
      HK(I)=HK(I)*WB
C
       DO 20 J=1,4
      IF(J.EQ.I)ET(I,J)=CEXP(DDTSC)
      IF(J.NE.I)ET(I,J)=(0.0,0.0)
      IF(IP.EQ.1)WRITE(1,19)ET(I,J),I,J
19    FORMAT('ET=(',E20.8,',',E20.8,')',5X,'I=',I2,5X,'J=',I2)
20    CONTINUE
      YK1(I)=(0.0,0.0)
      U(I)=(1.0,0.0)
      TJ1(I)=(0.0,0.0)
C
C
30    CONTINUE
C
C
C
C
      DO 100 I=1,ND
      XTJ=(I-1)*DTS
C     GENERATE I AND Q SIGNAL
      TMJ=DSIN(PIE2*FM*XTJ)
        TMJT=DSIN(2*PIE*FM*XTJ-BETA)
      IF(IP.EQ.1)WRITE(1,602)TMJ
602   FORMAT(1X,'TMJ=',E20.8)
      PTJ=(DF/FM)*(1.0D0-COS(PIE2*FM*XTJ))
      ARG=PIE2*FOD*XTJ+PTJ
      XIJ=DCOS(ARG+TAI)
      YQJ=1.0D0*DSIN(ARG+TAQ)
      IF(IP.EQ.1)WRITE(1,506)XIJ,YQJ
506   FORMAT(1X,'XIJ=',E12.4,5X,'YQJ=',E12.4)
C
C     DEMODULATION OF I AND Q SIGNALS
C
C     A/D QUANTIZATION OF I AND Q SIGNALS
      IXJ=KATD(XIJ,1.0D0,KAD)
      LQJ=KATD(YQJ,1.0D0,KAD)
      IF(IP.EQ.1)WRITE(1,507)IXJ,LQJ
507   FORMAT(1X,'IXJ=',I6,5X,'LQJ=',I6)
C     ESTIMATE OF PHASE USING VECTOR METHOD
C
      MI=IABS(IXJ)
      MQ=IABS(LQJ)
      IPK=2.D0**KAD
      IF(IP.EQ.1)WRITE(1,505)IPK,MI,MQ,NPH
505   FORMAT(1X,'IPK=',I4,2X,'MI=',I5,2X,'MQ=',I5,2X,'NPH=',I5)
      CALL VEPAC(MI,MQ,NPH,KAD,ETA)
      IF(IP.EQ.1)WRITE(1,502)ETA
502   FORMAT(1X,'ETA=',E12.4)
      THETA=ETA
C     TEST I AND Q CHANNELS FOR PHASE QUADRANT
      IF(IXJ.GT.0)GO TO 200
      ETA=PIE+THETA
      IF(LQJ.GT.0)ETA=PIE-THETA
      GO TO 201
200   ETA=PIE2-THETA
      IF(LQJ.GT.0)ETA=THETA
201   CONTINUE
      IF(IP.EQ.1)WRITE(1,501)ETA
501   FORMAT(1X,'ETA=',E12.4)
      DELTA=ETA-ETA1
      IF(DABS(ETA-ETA1).LT.PIE)GO TO 210
      IF(ETA.GT.ETA1)DELTA=DELTA-PIE2
      IF(ETA.GT.ETA1)GO TO 210
      DELTA=DELTA+PIE2
210   CONTINUE
      XMJ=DELTA/(PIE2*DF*DTS)
      IF(IP.EQ.1)WRITE(1,213)XMJ
213   FORMAT('XMJ=',E20.8)
```

```
      ETA1=ETA
C
CC
C     LOW-PASS FILTERING OF DIFFERENCE
C     SIGNAL USING 4-POLE BUTTERWORTH FILTER.
CC
CC
CC
C
      DO 230 IJ=1,4
      ETJ=(0.0,0.0)
C
C
      DO 220 JJ=1,4
      ETJ=ET(IJ,JJ)*YK1(JJ)+ETJ
220   CONTINUE
      IF(IP.EQ.1)WRITE(1,221)ETJ
221   FORMAT('ETJ=(',E20.8,',',E20.8,')')
C
CC
C
      XMJC=CMPLX(SNGL(XMJ),0.0)
      YK(IJ)=XMJC*HK(IJ)+ETJ
      IF(IP.EQ.1)WRITE(1,222)YK(IJ)
222   FORMAT('YK=(',E20.8,',',E20.8,')')
230   CONTINUE
      IF(IP.EQ.1)WRITE(1,231)
231   FORMAT('230 LOOP COMPLETED')
C
CC
CC
CC
C     LOW-PASS FILTERING OF REFERENCE
C     SIGNAL TO COMPARE WITH LOW-PASS FILTERED
C     DIFFERENCE SIGNAL.
CC
C
      DO 330 IJ=1,4
      ETJ=(0.0,0.0)
C
C
      DO 320 JJ=1,4
      ETJ=ET(IJ,JJ)*TJ1(JJ)+ETJ
320   CONTINUE
C
C
      TMJC=CMPLX(SNGL(TMJT),0.0)
      TJ(IJ)=TMJC*HK(IJ)+ETJ
330   CONTINUE
CC
CC
C
      SUMJ=(0.0,0.0)
      SUMT=(0.0,0.0)
C
CC
C
      DO 240 IJ=1,4
      YK1(IJ)=YK(IJ)
      IF(IP.EQ.1)WRITE(1,242)YK1(IJ)
242   FORMAT('YK1=(',E20.8,',',E20.8,')')
      TJ1(IJ)=TJ(IJ)
      SUMJ=U(IJ)*YK(IJ)+SUMJ
      SUMT=U(IJ)*TJ(IJ)+SUMT
240   CONTINUE
      IF(IP.EQ.1)WRITE(1,241)
241   FORMAT('240 LOOP COMPLETED')
C
CC
C
      TMJX=REAL(SUMT)*DTS
      XMJ=REAL (SUMJ)*DTS
C     WRITE(1,620)XTJ,TMJT,TMJX
C20   FORMAT(1X,'XTJ=',E12.4,4X,'TMJT=',E12.4,4X,'TMJX=',E12.4)
      IF(IP.EQ.1)WRITE(1,211)SUMJ
211    FORMAT('SUMJ=('E20.8,',',E20.8,')')
C
C     CALCULATE ESTIMATE OF MEAN
C     FOR DEMODULATED DATA TO CORRECT
C     FOR DC OFFSETS
C
```

```
      NMX=20
      NMX1=NMX-1
      CALL SFTR(XMJ,SR,NMX)
      XMDC=(XMJ-SR(NMX))/FLOAT(NMX)+XMDC1
      XMDC1=XMDC
C     XMJP=XMJ-XMDC
      XMJP=XMJ
      IF(IP.EQ.1)WRITE(1,150)XMDC,XMJ,TMJ,SR(NMX)
150   FORMAT(1X,'XMDC=',E20.8,5X,'XMJ=',E20.8,5X,'TMJ=',E20.8,
     15X,'SR(NMX)=',E20.8)
C
C     CALCULATE ERROR DIFFERENCE
C
160     EXM=XMJP-TMJX
      IF(IP.EQ.1)WRITE(1,153)XMJP,TMJX,EXM
153   FORMAT('XMJP=',E20.8,5X,'TMJX=',E20.8,5X,'EXM=',E20.8)
C     GO TO 100
C
C     CALCULATE MEAN AND VARIANCE OF
C     MODULATION VARIABLES FOR SIGNAL
C     PLUS DISTORTION TO DISTORTION RATIO
C
      IF(I.LT.NMX  )GO TO 100
      NI=I-NMX1
      XNI=FLOAT(NI)
      XNI1=FLOAT(NI-1)
      IF(IP.EQ.1)WRITE(1,302)XNI
302   FORMAT(1X,'XNI=',E20.8)
      DCXM=XMJP/XNI+XNI1*DCXM1/XNI
      DCXM1=DCXM
      EDC=EXM/XNI+XNI1*EDC1/XNI
      EDC1=EDC
      XM2=XMJP**2
      SM2=XM2/XNI+XNI1*SM21/XNI
      EM2=EXM**2
      SE2=EM2/XNI+XNI1*SE21/XNI
      SM21=SM2
      SE21=SE2
100   CONTINUE
      WRITE(1,303)FM
C
303   FORMAT('FM=',F10.4)
C
C
C
C     GO TO 175
C
C     CALCULATE (S+D)/D RATIO
C
      VARM=SM2-(DCXM**2)
      VARE=SE2-(EDC**2)
      WRITE(1,301)VARM,VARE
301   FORMAT(1X,'VARM=',E20.8,5X,'VARE=',E20.8)
      SDR=10.0D0*DLOG10(VARM/VARE)
      WRITE(1,300)SDR
300   FORMAT(1X,'SDR(DB)=',E20.8)
175   CONTINUE
      WRITE(1,998)
998   FORMAT(1H1)
1998  CONTINUE
1999  CONTINUE
2000  CONTINUE
C
C
C
```

```
C
C
      STOP
      END
      SUBROUTINE GRV(XM,SG,XV,YV)
C
C     THIS SUBROUTINE GENERATES TWO INDEPENDENT GAUSSIAN RANDOM VARIABLES
C
C     SG = DESIRED STANDARD DEVIATION OF GRV
C     XM = DESIRED MEAN OF GRV
      IMPLICIT REAL*8 (A-H,O-Z)
      IMPLICIT INTEGER*4 (I-N)
      COMMON /RAND/IIO,II1
      PIE2=8.0D0*DATAN(1.0D0)
      CALL RANDU(IIO,II1,YD1)
      IIO=II1
      Z=SG*DSQRT(-2.0D0*DLOG(1.0D0-YD1))
      CALL RANDU(IIO,II1,YD2)
      IIO=II1
C     WRITE(1,10)YD1,YD2
10    FORMAT(1X,'YD1=',E12.5,5X,'YD2=',E12.5)
      PHI=PIE2*YD2
      XV=Z*DCOS(PHI)
      YV=Z*DSIN(PHI)
      RETURN
      END
      FUNCTION KATD(X,A,K)
C
C     X=ANALOG SIGNAL WITH MEAN = ZERO
C     A = MAX LEVEL FOR A/D CONVERTER
C     K = NUMBER OF BITS QUANTIZATION INCLUDING SIGN
C     OUTPUT IS DISCRETE DECIMAL LEVEL, NOT BINARY
C
      IMPLICIT INTEGER*4 (I-N)
      REAL*8 X,A,S
      INTEGER*4 KATD
      K2=2**(K-1)
      S=2.0D0*A/(2.0D0**K)
      KX=(X+A)/S
      KATD=KX-K2
      RETURN
      END
      SUBROUTINE VEPAC(IX,JY,NX,KAD,A)
C
C     THIS SUBROUTINE CALCULATES THE VECTOR PHASE
C     ANGLE FROM THE INPHASE AND QUADRATURE
C     SIGNAL COMPONENTS.
C     SIGNAL COMPONENTS
C     IX=MAGNITUDE OF SIGNAL COMPONENT
C     JY=MAGNITUDE OF QUADRATURE SIGNAL COMPONENT
C     NX=NUMBER OF PHASE RESOLUTION CELLS IN 90 DEGREES
C     A=ANGLE (IN RADIANS) CALCULATED FROM IX AND JY SIGNALS
C
      IMPLICIT REAL*8 (A-H,O-Z)
      IMPLICIT INTEGER*4 (I-N)
      INTEGER*4 KATD
      PIE=4.0D0*DATAN(1.0D0)
      DPHI=PIE/(2.0D0*NX)
      IPK=2.0D0**(KAD-1.0D0)
      AIPK=IPK
      IZT=(AIPK**2.0D0)*DPHI/2.0D0
      NX1=NX+1
C     WRITE(1,200)DPHI,IPK,IZT,NX1
200   FORMAT(1X,'DPHI=',E12.4,2X,'IPK=',I5,2X,'IZT=',I5,2X,
     1'NX1=',I5)
      DO 100 I=1,NX1
      PHI=FLOAT(I-1)*DPHI
      AI=DCOS(PHI)
      BI=DSIN(PHI)
      JAI=KATD(AI,1.0D0,KAD)
      JBI=KATD(BI,1.0D0,KAD)
C     WRITE(1,1)JAI,JBI
1     FORMAT(1X,'JAI=',I6,5X,'JBI=',I6)
      JZT=JAI*JY-JBI*IX
      IF(JZT.LT.IZT)GO TO 101
100   CONTINUE
101   CONTINUE
      A=PHI
      RETURN
      END
      SUBROUTINE RANDU(IX,IY,YFL)
      IMPLICIT REAL*8 (A-H,O-Z)
```

```
      IMPLICIT INTEGER*4 (I-N)
C
      IY=IX*INTL(65539)
      IF(IY.GE.0)GO TO 6
      IY=IY+INTL(2147483647)+INTL(1)
6     YFL=IY
      YFL=YFL*.4656613D-09
      RETURN
      END
      SUBROUTINE SFTR(X,SR,NL)
C
C     THIS SUBROUTINE PERFORMS A SHIFT REGISTER
C     OPERATION.  X IS THE NEWEST INPUT VARIABLE,
C     SR IS THE SHIFT REGISTER ARRAY,  NL IS THE
C     LENGTH OF THE SHIFT REGISTER.
C
C
      REAL*8 X,H1,H2,SR
      INTEGER*4 NL,I,NL1
      DIMENSION SR(20)
      IF(IP.EQ.1)WRITE(1,10)NL
10    FORMAT('NL=',I5)
      NL1=NL-1
      H1=SR(1)
      DO 100 I=1,NL1
      H2=SR(I+1)
      SR(I+1)=H1
      H1=H2
100   CONTINUE
      SR(1)=X
      RETURN
      END
```

FUNCTIONAL DESCRIPTION OF THE ZERO-IF RECEIVER

INTRODUCTION

The Zero-IF receiver built under the Zero-IF receiver study contract for the US Army is designed to operate in the 30-88 MHz band receiving an FM signal with 5 kHz peak deviation. It can receive signals as strong as 0 dBm and as weak as -118 dBm. The following is a description of how the receiver works.

RF Circuits

An RF signal is input to the radio via J1 on the back panel of the chassis. It then passes through connector P1 which mates with J1 and is input to the preselector filters. This connection is shown on the chassis wiring diagram (page A-1 of the appendix) in the line labeled RF input. One of the three bands in the preselector (page A-2 of the appendix) is selected by turning the band select switch located on the front panel of the radio. The three channels are labeled as L, M, and H. Of course, these letters stand for low, middle and high band. If the signal is within the passband of the selected filter it will continue onto the RF amplifier/attenuator stage. If the signal is not within the passband of the selected filter it will be attenuated and effectively the radio will behave as if no signal was received. In this way, the preselector can be thought of as a tuner.

Band selection is accomplished in the circuit through the use of PIN diodes. Each of the bands has a dc voltage applied to it. This voltage is provided by two control inputs. One control input (E12 on the schematic) provides -15 volts for all 3 bands. The band which is selected will have +15 volts connected to its other control input (E9, E10, or E11) causing current to flow through the voltage divider of the 10K and 1.5K resistors. A +11 volt dc level is then applied to the PIN diode, forward biasing it, and allowing the RF signal to pass. The bands which are not selected have the -15 volt level on their diodes, reverse biasing them, causing an open circuit for the RF signal.

The RF signal then leaves the preselector filters board via P2 and enters J2. J2 is connected to J3 by a jumper on the back panel of the radio. J3 connects to P3 J1 and the signal enters the RF amplifier/attenuator board. The jumper between J2 and J3 can be removed and by connecting an antenna to J3, signals outside the 30-88 MHz band can be received. The RF parts should provide good performance between 20 and 200 MHz.

The RF amplifier/attenuator board is a two section board. One section contains the RF amplifiers and the PIN diode variable attenuator pad, while the other section contains the attenuator pad control logic.

The signal is first amplified by an RF amplifier U1 (page A-3 of the appendix) and then enters the attenuator pad. The attenuator pad is used to control the RF level coming into the receiver.

It has five different settings. The settings are 0, 12, 24, 36, and 48 dB of attenuation. As the RF level increases, the baseband AGC circuits control the level of the signal entering the demodulator. After the baseband AGC's attenuation is exhausted, stronger signals could cause clipping and degrade the SINAD. When the baseband AGC indicates that more attenuation is necessary, the shift register U3 in the attenuator control logic (page A-4 of the appendix) is strobed and one step of RF attenuation is turned on. If the baseband AGC indicates that there is too much attenuation and the RF attenuator has some attenuation on, the shift register is strobed again, and one step of RF attenuation is turned off.

The attenuator uses analog switches to turn the individual steps on and off. In the 0 dB of attenuation setting, D1 and D2 are on while D3 through D6 are off. This allows the signal to pass through the upper branch of the circuit (see the schematic on page A-3) by forward biasing the PIN diodes. In the 12 dB of attenuation setting, D1 is turned off and D3 is turned on. All other points remain the same. If 24 dB of attenuation is required, D2 is turned off and D4 is turned on. For 36 dB of attenuation D5 is turned on, and 48 dB of attenuation is achieved by turning on D6. At the full attenuation setting (48 dB), two diodes are off (D1 and D2) and four diodes are on (D3 through D6). The RF signal leaves the attenuator pad and enters the amplifier U2. The RF signal is amplified by 12 dB and leaves this board and enters the signal splitter/mixer board as shown on the chassis wiring diagram. The local oscillator (LO) signal is supplied by an RF signal generator. It enters the radio via J4 on the back panel of the radio. It then enters the local oscillator 90 degree splitter (LO splitter). The LO signal is then split into two signals, one in phase with the LO and one 90 degrees out of phase (in quadrature) with the LO. These two signals are then input to the signal splitter/mixer board.

The signal splitter/mixer board receives the signal from the RF amplifier/attenuator board and inputs it to the 0° power splitter U1 (page A-5 of the appendix). This part splits the received signal into two signals identical in phase and amplitude. These two signals each proceed to the RF input of a mixer (U2 or U3). The LO input on each mixer is connected to one of the two LO signals coming onto this board. The received signals are then mixed with the LO signals. The output of the mixers is a baseband signal along with an RF frequency at twice the LO frequency. These two signals are then input to the baseband channel filters board. It should be noted that the two baseband signals are identical except that they are 90 degrees out of phase. They can be referred to as the in-phase and quadrature signals; hence, the names I and Q channels.

Baseband Circuits

The baseband channel filters board (page A-6 of the appendix) consists of two (one for each channel) seven pole passive element filters. These filters are low pass with a cut off frequency of 8 kHz. These filters provide 70 dB of attenuation at 25 kHz which is the adjacent channel. After the signal is filtered here, it continues on to the low noise amplifier board.

The low noise amplifier board (page A-7 of the appendix) is designed to give small signal gain without adding noise from active devices. Both channel signals go through a transformer, T1 and T2. These transformers are arranged such that they are a 1:40 step up. Their outputs then go to U1 and U2. These are very low input noise op amps. They provide 22 dB of gain. The signal then goes to a filtering and gain stage, U3, which has another 13 dB of gain. After this stage the channel signals proceed to the automatic gain control board from Pins 1 and 22 to L and 12 respectively as shown on the chassis wiring diagram.

The automatic gain control (AGC) board (page A-8 of the appendix) is designed to amplify small signals and to attenuate large signals. This is accomplished through the use of a digital step attenuator. The major components of the attenuator are the two shift registers U5 and U6, and the four analog switches U7 through U10.

The detector is made of the four op amps in U3. This circuit half-wave rectifies each channel signal and sums the two together. This produces a dc level. This dc level is compred with two reference levels, one being a low threshold and the other a high threshold. When the dc level from the rectifiers is between the two thresholds, the amount of attenuation set in the attentuator is correct. If the dc level is higher than the high threshold, the control logic causes the attenuator to increase the amount of attenuation. If the dc level is too low, the control logic causes the attenuator to decrease the amount of attenuation.

Whenever a change in attenuation is necessary, the control logic enables the clock, U11. The clock causes the shift registers to shift in or out attenuation. The direction of shift is determined by the mode control line. When the control logic causes this line to go to a high state, the attenuator will switch out attenuation with the clock. If the mode control line is in a low state, the attenuation will switch in attenuation with the clock. When the proper amount of attenuation is reached, the control logic once again disables the clock. The clock only runs when an attenuation change is needed. This helps reduce the amount of digital noise generated in this circuit.

The analog switches are used to provide the attenuation. As each switch is closed, attenuation is provided by the voltage divider set up with the 20K ohm resistors R38 and R42 or R39 and R41. Note that the switches are wired in parallel so that each channel receives the same amount of attenuation. Also, starting from the zero attenuation setting, the swtiches U8 and U10 are used first, then U7 and U9 followed by the RF attenuation circuit.

The RF attenuation circuit is an extension of the baseband AGC circuit. The clock, the most significant bit from the AGC circuit (MSBAGC), and the mode control lines all are inputs to the RF attenuation circuit. The detector still functions the same after the baseband AGC is used up. The least significant bit from the RF (LSBRF)

stage and the most significant bit from the RF (MSBRF) stage are fed back to the baseband AGC circuit. The MSBRF is an overflow protection bit which, when high, disables the clock if the detector indicates more attenuation is necessary. This is to prevent the clock from running and the circuits from trying to add in more attenuation when there is none available. The LSBRF is used to tell the baseband AGC that all RF attenuation is off. Therefore, if less attenuation is necessary the baseband AGC must turn off some of its own attenuation.

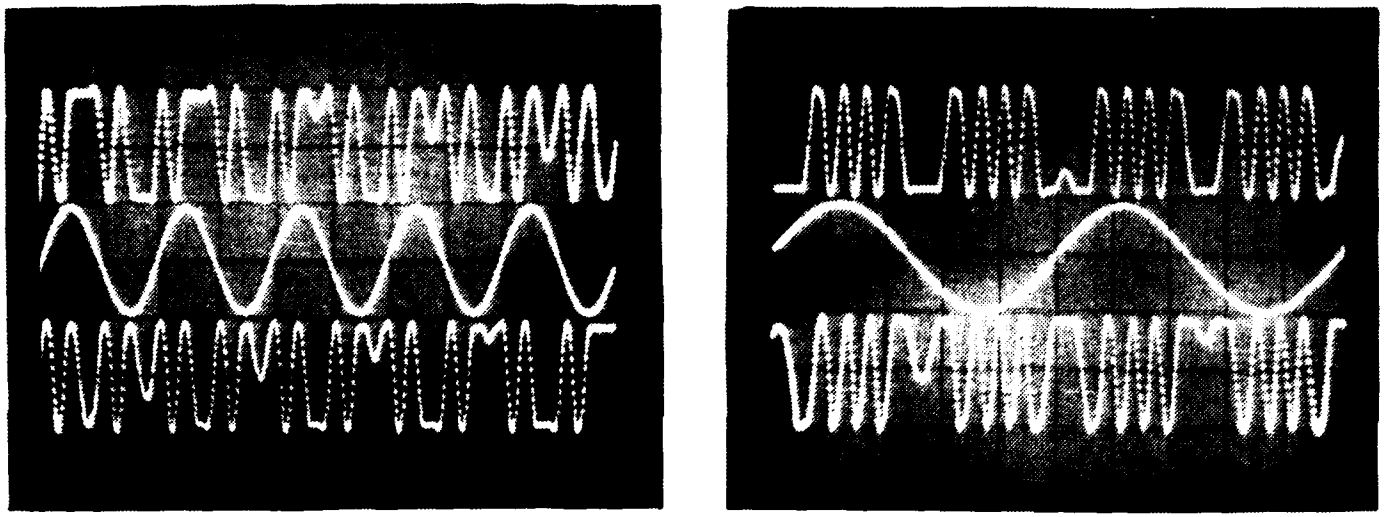
A compression amplifier (U4A, U4B) follows the AGC circuitry in each channel. The purpose of the compression amp is twofold. First, it smooths out the bumps caused by switching in and out different steps of attenuation. Secondly, it provides a constant amplitude signal out for the demodulator. The key element in the compression amplifier is the n-channel FET (Q5 and Q6) in each. The FET is used as a variable resistor. The amount of attenuation can then be varied by changing the voltage on the gate. This is included in the closed loop feedback to the op amps (U4A and U4B) along with the capacitors and resistors which set the attack and release time constants.

The output of the compression amplifier is shown in Figure 1. The center trace in these pictures is the modulation impressed on the RF carrier. The upper and lower traces are the outputs of each channel. Note that the channel signals are identical except that they are 90 degrees out of phase. Also note, as the modulation crosses zero, both channel signals undergo a 180 degree phase shift. This corresponds to the reversal of the direction of rotation of the phasor as described in Section 3. Notice too that for lower modulation frequencies, the channel signals have more cycles of phase than for higher modulation frequencies. This corresponds to the longer time between zero crossings for lower modulation frequencies, and therefore the phasor rotates in each direction for a longer period of time.

The AGC output pins are J and K of J6. The signals are input to the demodulator through connector J7 pins D and E. Both demodulators use these two pins for their input. The analog demodulator boards plug directly into the chassis connectors J7 and J8. The digital demodulator subchassis jumper boards also plug directly into these connectors for digital demodulation as shown on the chassis wiring diagram.

Analog Demodulator

As explained in Section 3, the analog demodulation process used in the Zero-IF receiver is a phase-locked loop (PLL) demodulator. The major advantage of this approach is that it is not sensitive to amplitude and phase matching of the I and Q signals. This translates to the circuit being able to more completely eliminate the deviation tones from the demodulated output.



Modulation Tone = 1 kHz
Vertical = 1 volt/div.
Horizontal = 0.5 msec/div.

Modulation Tone = 400 Hz
Vertical = 1 volt/div.
Horizontal = 0.5 msec/div.

Figure 1. I and Q Channel Signals with the Modulation Impressed on the RF Carrier

The PLL demodulator used in the Zero-IF receiver is very similar to an ordinary PLL circuit. Figure 2 is a block diagram of an ordinary PLL circuit. A signal enters the loop at A and is input to the phase detector. The phase detector output is then input to a low pass filter (LPF). The demodulated signal is at the output of the LPF. This signal is also input to a VCO as the control voltage. The VCO output is then fedback to the other input of the phase detector, completing the loop.

Figure 3 shows that the Zero-IF PLL demodulator is different from the ordinary (PLL) demodualtor in that it has two channels in the feedback path. Two feedback channels must be supplied because there are two input channels. The feedback signals represent the mixed output of the VCO and the baseband oscillator. If there is no modulation on the received carrier and no frequency error exists, the output of the baseband oscillator and VCO mixers is a dc level. If modulation or frequency error exists, these outputs are the derivatives of the I and Q channels.

The I and Q signals enter the phase detector (page A-9 of the appendix) which is implemented as two analog multipliers (U2 and U3). The other input to each multiplier is the filtered output of the baseband mixers. The multiplier outputs are then subtracted one from the other in an op amp (U4A). The result from this subtraction is the error voltage in the PLL. As it was shown mathematically in Section 3, the error voltage is the desired demodulator signal. The error voltage is sent to the audio circuits for filtering and is the control voltage input (page A-10 of the appendix) for the VCO (U1).

The control voltage for the VCO passes through two op amps (U8A and U8B). These op amps provide a level shift for the VCO control voltage so that the VCO frequency will vary linearly with voltage 20 kHz about its nominal frequency (250 kHz). The VCO output is input to the clock of a D type flip flop (U10A) which is connected in the standard manner for division by two. Both outputs of this flip flop are input to the clocks of two more D type flip flops (U11A and U11B) which are also connected to divide by two. This results in a nominal frequency of 62.5 kHz which varies higher and lower by 5 kHz out of the flip flops. Figure 4 is a timing diagram showing the results of this division. Note how the two final outputs (Q_{D2} and Q_{D3}) are 90 degrees out of phase. This insures that the two signals generated by this circuit are also 90 degrees out of phase. These two signals are input one to each baseband mixer (U4, U5, and U6, U7). The other input to both baseband mixers is the free running baseband oscillator. This oscillator (U2) operates at 1 MHz and is divided down to 62.5 kHz (a division of 16) by the shift register (U3) and flip flop (U10B). The mixer inputs driven by this result are in phase. The baseband mixer outputs are two IF signals, like those shown in Figure 1, which are 90 degrees out of phase. These signals are also the derivatives of the I and Q signals. This is obvious because the VCO is an integrator in a feedback path, therefore the VCO effectively differentiates the I and Q signals.

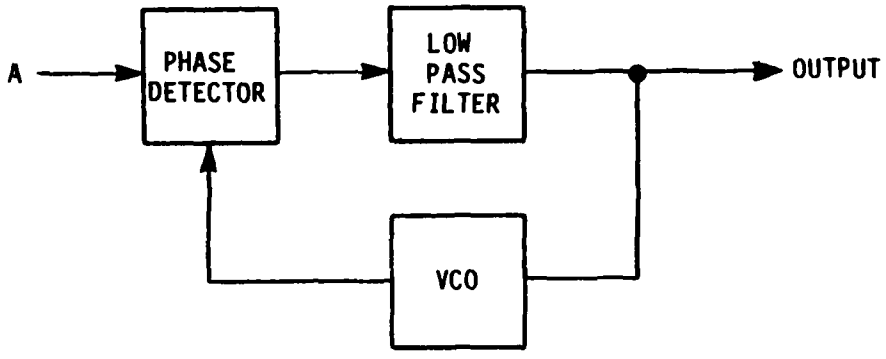


FIGURE 2: Basic PLL Circuit

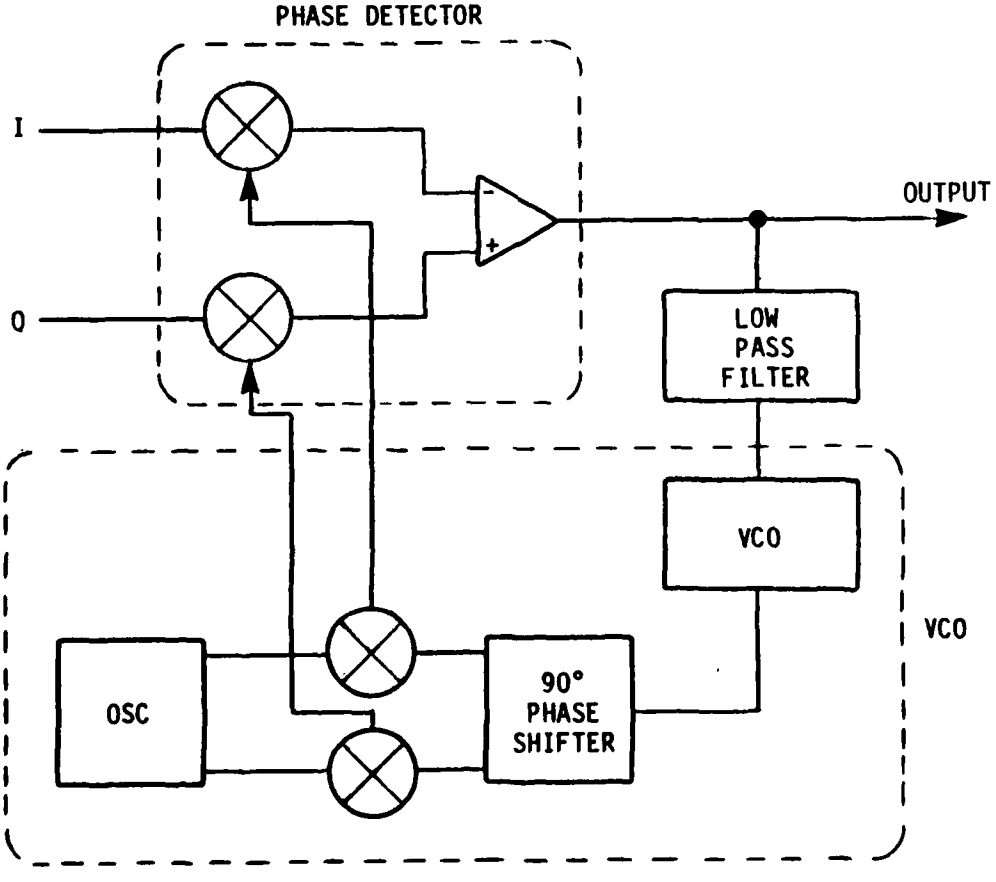


FIGURE 3: Zero I.F PLL Demodulator

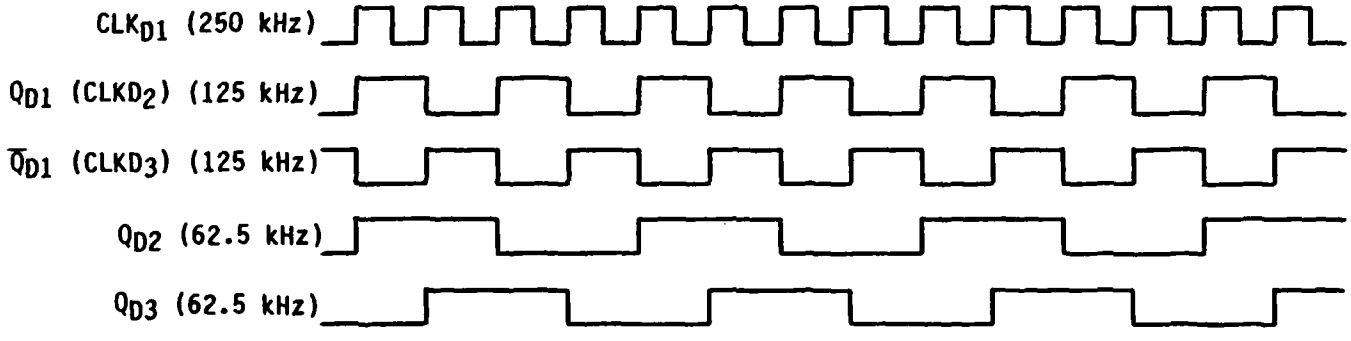


FIGURE 4: Timing Diagram for Zero I.F.
Receiver Divide by 4 Circuit

The baseband mixer outputs then pass through 50 kHz low pass filters (U9A, U9B). The filtered output is fed back to the baseband multipliers board (page A-9 of the appendix). Here they pass on the phase detector, completing the loop.

The baseband multiplier (phase detector) outputs are always in phase with each other. Each output is the product of two signals whose frequency varies from 0 to 5 kHz. Therefore, the output signal of each multiplier varies from 0 to 10 kHz. The output signals also have another component. This component is the error voltage for each particular phase detector. The error voltage represents the amount of phase error present between the two signals that are input to the multiplier. It varies plus or minus depending on the amount the phase of the two input signals is away from 90 degrees. These two error voltage signals are identical except that they are 180° out of phase. Subtracting the two phase detector outputs yields the error voltages added together and the remainder of the signals canceling out. This error voltage represents the desired demodulated signal.

The output error voltage from each phase detector is dependent on the magnitude of the phase difference between the two input signals. When the two input signals are 90 degrees out of phase, the output error voltage is zero. As the two signals vary from 90 degrees out of phase, the error voltage will vary about zero volts linearly. Figure 5 is a graph of the error voltage versus the difference in phase of the two input signals. The two zero crossings represent the possibility of either input signal leading the other at any instant in time. As the modulation passes through zero crossings, the phase detector bounces from working on one slope to the other because the input signals exchange roles leading in phase.

For the case of no modulation with a beat frequency, the phase detector outputs are a frequency of twice the beat frequency riding on a dc level. The output frequencies are in-phase, while the dc levels are of opposite polarity. Subtracting the phase detector outputs yields the dc level only. This dc level directly represents the beat frequency. When the magnitude of the beat frequency is small, the dc level is small. When the magnitude of the beat frequency is large, the dc level is large. When modulation is present, the instantaneous carrier deviation can be analyzed as a beat note. The carrier deviation changes with time, following the modulation causing a change in the instantaneous beat note. These changes cause a varying dc level which actually is the demodulated signal. If the LO and the received carrier are at the same frequency, the demodulated signal will vary above and below zero volts. When they are not at the same frequency the demodulated signal will vary above and below the dc level caused by the beat note. The dc level is eliminated from the demodulate signal by the high pass filter in the audio circuits (U1A on the schematic on page A-11 of the appendix).

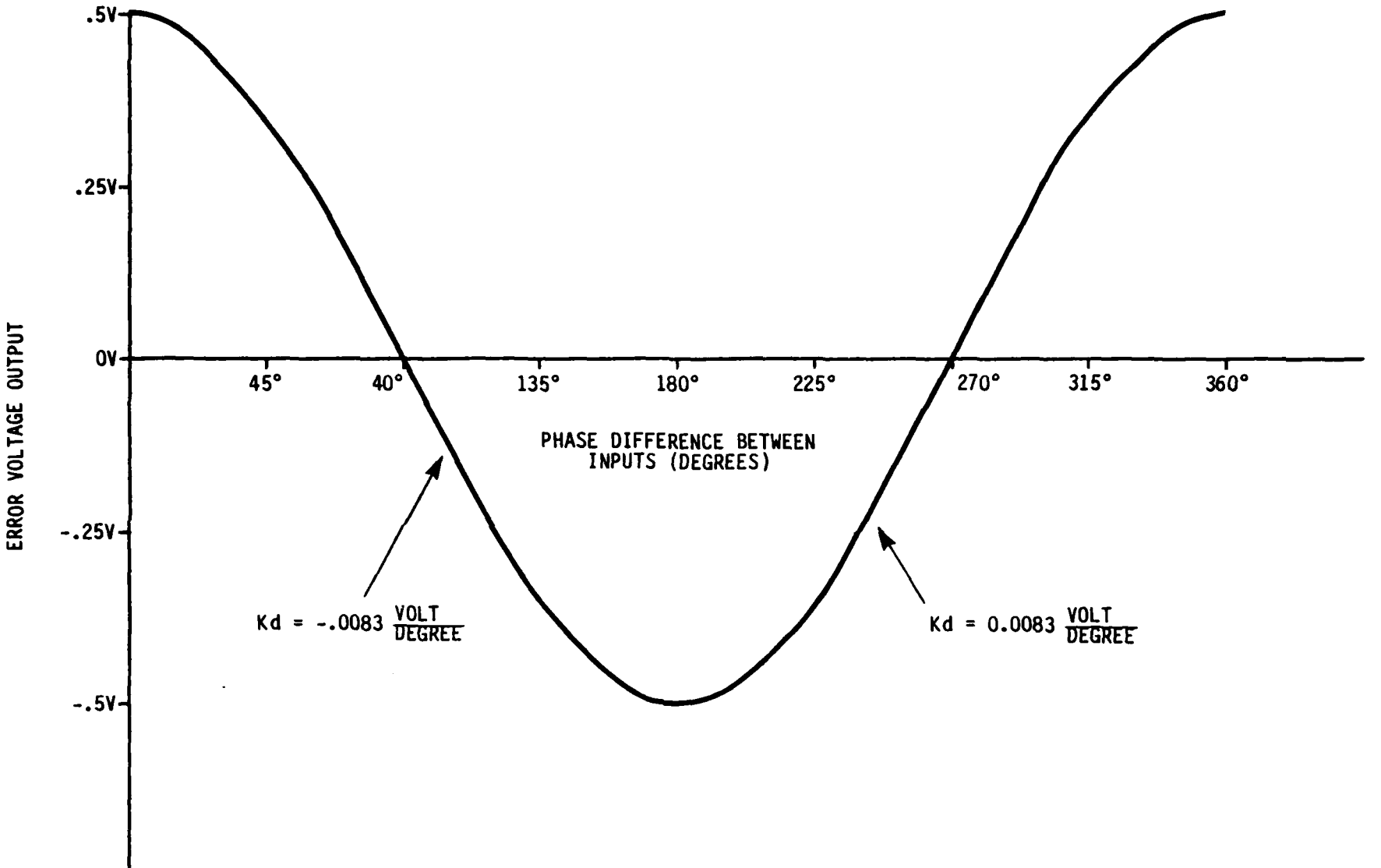


FIGURE 5: Plot of Phase Detector Error Voltage vs. Difference in Phase of Input Signals

The error voltage drives the VCO and is the demodulated output as described previously. By changing the frequency of the VCO with the error voltage the same beat frequency is generated in the feedback loop. This frequency will be phase locked to the received signal inputs. The phase error away from 90 degrees crates the dc level which keeps the VCO on the proper frequency. Thus, the loop is complete. This dc level can also be used for automatic frequency control (AFC). By low pass filtering the output (cutoff frequency of 1 to 2 Hz), the dc level can be separated and fed back to the LO. By recognizing this as a tuning signal, the LO frequency may be adjusted to draw its operating frequency closer to the received carrier. Switching around the multiplier input connections will change the polarity of the AFC signal and nothing else.

Digital Demodulator

As explained in Section 4, the digital demodulation process used in the Zero-IF receiver is the vector processor. The vector processor uses the successive approximation technique in finding the absolute phase of a sample. It then differentiates by subtracting successive samples. To avoid the necessity of very high speed logic, the vector processor uses the pipeline technique for data manipulation.

SECTION 1

Section 1 of the pipeline receives the output of the AGC circuit and samples the signal by the sample and holds ICs U8 and U9 (page A-13 of the appendix). Comparators U5A and U5B check the sign of the sample. This information is stored in the latches U6A and U6B for use in the next section of the pipeline. The signal is next input to a full wave rectifier U3A and U3B, and U4A and U4B. The rectified channel signals are then input to the Analog to Digital converters, U11 and U12. The output of the Analog to Digital converters is sent to the magnitude compare and multiply circuit (page A-14 of the appendix) as shown on the digital subchassis wiring diagram (page A-12 of the appendix) and latched. This is the end of Section 1 of the pipeline.

SECTION 2

Section 2 begins by comparing the magnitudes of the samples of the two channel signals in U6 and U7. The information received here does two things. First it is sent to the end of this section as an information bit and second, it is used to direct the greater of the two samples to the multiplier U14, and the lesser to a second magnitude comparator U8 and U9. The word that went to the multiplier is multiplied by the tangent of 22.5 degrees. The multiplier output is sent to the second magnitude comparator. The magnitude comparator output is sent to the phase register (page A-16 of the appendix) on the digital timing circuits board.

The phase register (U5B, U6, U7, U8, U9, U12 and U13) is capable of representing any angle between 0 and 45 degrees to within 0.351 degrees. It is used to find the phase angle of the signal at the instant the sample was taken. It uses the successive approximation technique to accomplish this. First, the phase register is set to 22.5 degrees by U9. This information passes to an EPROM on the magnitude compare and multiply board. The EPROM is a look up table storing the tangent of the angles from 0 through 45 degrees. The tangent of 22.5 degrees is sent to the multiplier. After multiplication, the second magnitude comparator sends a signal to the phase register. If the multiplier output is less than the lesser of the two samples, the 22.5 degree bit is saved. If the multiplier output is greater than the lesser sample, the 22.5 degree bit is thrown out.

Next, the 11.25 degree bit is used. If the 22.5 degree bit was saved, the EPROM will be addressed with 33.75 degrees, if not, the EPROM will be addressed with 11.25 degrees. The tangent is again sent to the multiplier, the multiplier outputs to the comparator, and the comparator outputs to the phase register. The next least significant bit is used until all seven bits are used. When this process is finished, a seven bit word representing the phase of the sample in 45 degrees is on the output of the phase register.

Besides going to the EPROM, the phase register output also goes to the differentiator and DAC (Digital to Analog Converter) circuit (page A-15 of the appendix) as shown on the subchassis wiring diagram. Here the phase register output, the first magnitude compare bit and the sign bits from the first section of the pipeline are combined to represent the phase of the sample for 0 through 360 degrees. The previous word is then subtracted from this word in U8, U9, and U10. The subtraction output is latched in U14, U15, and U16. This is the end of the second section of the pipeline.

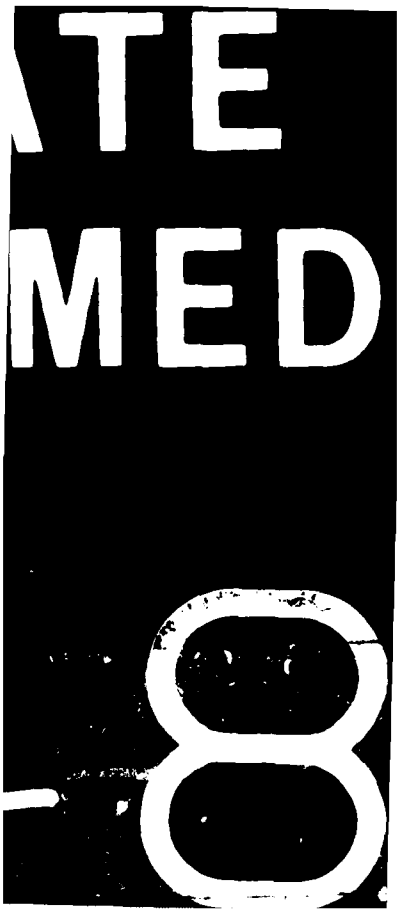
SECTION 3

Section 3 of the pipeline latches the phase register output into the previous sample register U11, U12, and U13. It also contains the DAC. The DAC outupt is then held for one sample period. The DAC output is input to two filters. One filter is a 3100 Hz low pass. The output of this filter is sent to the audio circuit. The other filter is a 0.75 Hz lowpass. The output of this filter is sent to J5 on the back panel of the radio as the AFC signal.

Audio Circuits

The audio circuits in the Zero-IF receiver (page A-11 of the appendix) are very basic. The first element of the audio circuits is a 300 Hz-3000 Hz bandpass filter. The filter is made up of an active two pole 3000 Hz lowpass (U1B) and an active two pole 300 Hz high pass (U1A) filter. The output of this filter is attenuated by R18

and R17 and sent to the desired signal output which is connected to J6 on the back panel of the radio. The desired signal output can be used to measure the performance of the radio. The filter output is also sent to the volume control and on to the speaker amplifier. The speaker amplifier drives the speaker with 400 milliwatts rms of power.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