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STINGER POST HYBRID SIMULATION: DESIGN DESCRIPTION AND USERS' MANUAL

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Development of a hybrid simulation for the Stinger POST Missile System was completed during this task. A comprehensive users' manual is presented through this report. Descriptions of the analog models, electronics breadboard assembly, control logic, digital program, interfaces, diagnostic capabilities, and operation sequences are provided.

PREFACE

This technical report was prepared by the Electrical and Computer Engineering Department of the School of Engineering, The University of Alabama in Huntsville (UAH). The project documented in this report was directed by T. N. Long and was staffed by T. A. Palmer, D. A. Hall and T. N. Long. The work was performed through delivery order number 0003, contract number DAAH01-82-D-A008; Dr. N. A. Kheir, Principal Investigator. Dr. M. M. Hallum, III, Chief, Systems Evaluation Branch, Army Missile Laboratory, U.S. Army Missile Command, was technical monitor. Mr. D. H. Dublin of the Systems Evaluation Branch provided technical coordination.

The authors wish to acknowledge the valuable contributions of personnel from the various organizations, including MICOM, Georgia Institute of Technology Engineering Experiment Station and General Dynamics, that have participated in development of the Stinger POST hybrid simulation. Since development spanned a period of over three years, it is difficult to acknowledge each contributor individually. So, apology is due for any oversight of contributors on the "background" page.

The technical viewpoints, opinions, and conclusions expressed in this report are those of the authors and do not necessarily express or imply policies or positions of the U. S. Army Missile Command.

BACKGROUND

This project was originally directed by personnel from the Georgia Institute of Technology Engineering Experiment Station (GITEES), and V. Grimes, of MICOM, provided technical coordination. C. Barnett initially directed the GITEES project which was staffed by T. Long, D. McKinley, and R. Murray. GITEES personnel defined configurations, partitioning, and interfaces and participated in hardware development. The guidance electronics breadboard assembly was provided by General Dynamics (GD), [1] and the gyroscope models were obtained from GD personnel working papers. D. Curry, of MICOM, developed and maintained the digital program under the direction of V. Grimes. Analog models were implemented and maintained by K. Hall, T. Adams, and R. Robinson of MICOM. UAH staff members P. Pritchett, R. Burt and D. Hall participated in target modelling efforts, [3]. Midway through development, T. Long undertook GITEES project direction responsibilities, R. Burt joined the GITEES staff, and D. Dublin began technical coordination for MICOM. During this period, implementation was completed and the simulation was made operational. Toward the end of the development cycle, P. Pritchett joined the GITEES staff and T. Long joined the UAH staff. During this final period, P. Pritchett participated in target modelling, R. Burt upgraded configurations of the guidance electronics, and UAH personnel developed diagnostic capabilities, maintained guidance electronics hardware, maintained simulation operation, and began simulation validation.

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ABBREVIATIONS

A	Amplifier
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
C	Servo-Set Potentiometer
CCA	Circuit Card Assembly
CCMV	Counter-Coutermeasure Verification
CDC	Control Data Corp.
CM	Comparator
D	Divider
DAC	Digital to Analog Converter
DDS	Digital Display System
DFG	Diode Function Generator
DIP	Dual In-Line Package
EAI	Electronic Associates Inc.
EBA	Electronic Breadboard Assembly
EM 0	Emulation Mode 1
EM 1	Emulation Mode 2
EM 2	Emulation Mode 3
ETSG	Electronic Target Signal Generator
F	Diode Function Generator
FF	Flip - Flop
FOV	Field of View
GD/P	General Dynamics - Pamona
HISC	Hybrid Interface Signal Conditioner
HP	Hewlett Packard
HS	Hand Set Potentiometer
I	Integrator
IC	Integrated Circuit
IFOV	Instantaneous Field of View
I/O	Input/Output
IR	Infra-Red
J	Jack
K	Function Relay
L	Limiter
LED	Light Emitting Diode
M	Multiplier
MVFG	Multi-Variable Function Generator
PB	Push Button
PCP	Prototype Control Probe
POST	Passive Optical Seeker Technique
S	Analog Switch
SGC	Static Gain Curve
TAG	Target Adaptive Guidance
TGxx	Output Logic Trunk
TGxxx	Green Analog Trunk
TOxx	Input Logic Trunk
TP	Test Point
TRxxx	Red Analog Trunk
U	Integrated Circuit
UV	Ultra-Violet
µP	Microprocessor

1.0 INTRODUCTION

Development of the Stinger-POST hybrid simulation was completed during performance of the task documented by this report. Subsequently, the intent of this report is to provide a comprehensive description of the simulation. It should contain most of the information required for effective and efficient operation.

Stinger POST is a small, shoulder launched missile. It has a dual spectrum (infra-red and ultra-violet) seeker which scans its field of view in a rosette fashion. Energy from a source is focused on its detector through the use of two counter-rotating mirrors annd a set of lenses. The mirrors also form the seeker's gyroscope. Stinger POST is an "intelligent" missile with two microprocessors in its electronics section. The electronics maintain tracking with the gyroscope and maintain guidance with the wing servo-mechanism. The missile has only a single wing-set which requires a rolling airframe. Since the missile is so small, it carries a very small warhead. Accordingly, it must score a "hit" on a target in order to record a "kill".

The Stinger POST hybrid simulation provides a high-fidelity, real-time simulation of the missile system. It can be used to predict test flight performance and analyze the flight afterwards. A variety of targets can be modelled with flares included. The simulation can also be used to evaluate the contributions of individual parameters or to generate engagement boundaries for the composite system.

A block diagram of simulation partitioning is presented in Figure 1. Guidance electronics functions are duplicated by an Electronics Breadboard Assembly (EBA). Interface functions are accomplished in the Hybrid Interface Signal Conditioner (HISC). The gyroscope motoring models, gyroscope dynamics model, target models, and wing servomechanism model are implemented on an EAI-781 analog computer. Target intensity profiles and drift profiles are contained in multi-variable function generators (MVFGs). And, scenario control, target calculations, and airframe modelling are performed by a CDC-6600 digital computer system.

The report is partitioned similar to the way that the simulation is partitioned. Section 2.0 describes the control logic which resides on the logic portion of an EAI-781 analog computer. Section 3.0 details the analog models. These include the gyroscope motoring models, gyroscope model, target models, and wing servo model; all reside primarily on the EAI-781. Section 4.0 reviews the EBA. It is identical to the seeker's electronics except for the fact that it is in discrete component form. The digital program, which runs on the CDC 6600, is discussed in Section 5.0. The interfaces are reviewed in Section 6.0 with the HISC and trunking stations being the principal areas reviewed. Then in Section 7.0, diagnostic capabilities are described. These include diagnostic techniques for the EBA, diagnostic tools implemented on the EAI-781 control console, and test routines developed on the CDC 6600. And finally, in Section 8.0, usage sequences are detailed. This includes initialization, tailoring, and operation sequences.

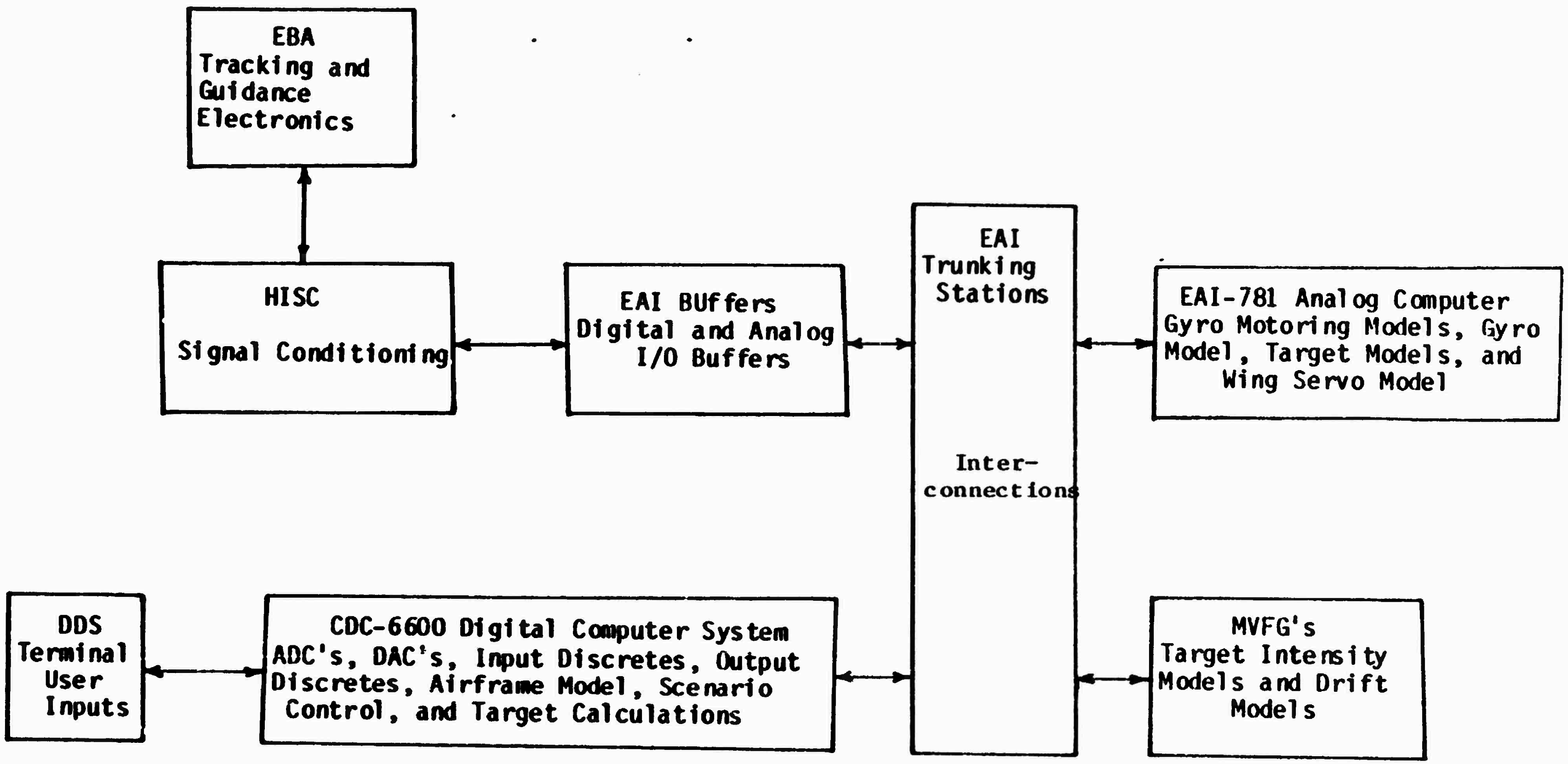

Figure 1 Stinger POST Hybrid Simulation Partitioning

2.0 CONTROL LOGIC

Simulation operation is controlled primarily by the digital program, which operates on the CDC 6600 computer. It is controlled by the operator through the Real Time Digital Display System (DDS). Logic signals transferred between the CDC 6600 and EAI-781 logic panel via a digital input/output system are used to execute the control. Combinational logic on the logic panel generates control signals used by the analog circuits, EBA, and digital program.

Most of the control logic functions are illustrated in Figure A-1 in Appendix A. Flip-flop FF000 is used to enable operation of the simulation. When it is enabled and Input Logic Trunk T015 is sent "high", a "handshaking" initialization signal is sent back to the digital program via Output Logic Trunk TG15. The equation for this function is presented as Equation 1 in Table 1. In words, the CDC 6600 receives an "all initialized" signal after it has sent its "initialize" signal and the "enable simulation" flip-flop has been set.

The equations presented in Table 1 represent the functional requirements. Actual implementation on the control logic panel is different in many cases since only AND and NAND gates are available. Examining Equation 2, a "gyro operate" signal is generated if the "all initialized" signal is generated <u>or</u> the "force gyro operate" flip-flop is set. The inverted output (negative logic) is used because integrators on the EAI 781 require a "low" to begin operation.

For Equation 3, a "gyro look angle integrator operate" signal is generated if there is a "gyro operate" signal <u>and</u> the "disable track loop" push-button has <u>not</u> been set.

For Equation 4, a "preliminary launch" signal is generated if "all initialized," "uncage EBA," <u>and</u> "launch" signals have been generated <u>and</u> the "stop" <u>and</u> "abort simulation" signals are <u>absent</u>.

For Equation 5, the "launch operate" signal is simply the inverse of Equation 4.

For Equation 6, a negative logic "roll resolver operate" signal is generated if the "launch" signal is generated <u>or</u> the "force roll resolver operate" flip-flop is set.

For Equation 7, a negative logic "roll resolver integrator operate" signal is generated if the "preliminary launch" signal is generated <u>or</u> the "force roll resolver operate" flip-flop is set.

For Equation 8, a "wing servo operate" signal is generated if the "force wing servo operate" push-button is set <u>or</u> the "bore clear" signal is generated.

For Equation 9, a "cage EBA" is present if the "all initialized <u>and</u> uncage EBA" signal has <u>not</u> been generated <u>and</u> the "force uncage" flip-flop has <u>not</u> been set.

For Equation 10, a "launch EBA" signal is generated if the "preliminary launch" signal is present <u>or</u> if the "force EBA launch" flip-flop is set.

For Equation 11, the "turn on oscillograph" signal is generated if the "enable oscillograph" push-button has been set <u>and</u> the "run oscillograph" signal has been generated.

For Equation 12, the "abort" signal is essentially the same as the "abort simulation" signal.

And for Equation 13, the "clear EBA" signal simply passes through the logic panel without going through any gates.

Some of flip-flops and push-buttons mentioned above were added for diagnostic purposes. Their use will be described further in Section 7.0. Others will be described in Section 3.0 with the analog description. Additionally, there are a few logic components which have not been included in Figure A-1. Some serve diagnostic purposes and others are integral parts of models; they too will be described in later sections.

$$\mathrm{ALLINI} = \mathrm{INITLZ} \cdot \mathrm{ENSIM} \tag{1}$$

$$\mathrm{GYROOP} = \overline{\mathrm{ALLINI} + \mathrm{FGYROP}} \tag{2}$$

$$\mathrm{GLAIOP} = \overline{\overline{\mathrm{GYROOP}} \cdot \overline{\mathrm{DISTRK}}} \tag{3}$$

$$\mathrm{PLNCH} = \mathrm{ALLINI} \cdot \mathrm{UNCAGE} \cdot \mathrm{LAUNCH} \cdot \overline{\mathrm{STOP}} \cdot \overline{\mathrm{ABSIM}} \tag{4}$$

$$\mathrm{LNCHOP} = \overline{\mathrm{PLNCH}} \tag{5}$$

$$\mathrm{RROP} = \overline{\mathrm{LAUNCH} + \mathrm{FRROP}} \tag{6}$$

$$\mathrm{RRINOP} = \overline{\mathrm{PLNCH} + \mathrm{FRROP}} \tag{7}$$

$$\mathrm{WSRVOP} = \mathrm{ENWSRV} + \mathrm{BORCLR} \tag{8}$$

$$\mathrm{CAGEBB} = \overline{\mathrm{FUNCAG}} \cdot \overline{(\mathrm{ALLINI} \cdot \mathrm{UNCAGE})} \tag{9}$$

$$\mathrm{LNCHBB} = \mathrm{PLNCH} + \mathrm{FBBLCH} \tag{10}$$

$$\mathrm{OSCON} = \mathrm{ENOCSC} \cdot \mathrm{RUNOSC} \tag{11}$$

$$\mathrm{ABORT} = \mathrm{ABSIM} \tag{12}$$

$$\mathrm{CLRBB} = \mathrm{CLRBB} \tag{13}$$

Table 1 Control Logic Equations

3.0 Analog Models

3.1 Introduction

The analog models reside primarily on the EAI-781 analog computer. They include the gyroscope motoring models, gyroscope dynamics model, target models, and wing servo model. Some models also use multivariable function generators (MVFC's). They are accessed by the EAI-781 via the trunking stations. The analog schematics are presented in Appendix A and programs (data sets) for function generators are presented in Appendix B.

3.2 Gyroscope Motoring Models

It was determined that it would be adequate to simply present the EBA with reference signals defined by a spin rate profile. This would simplify the simulation without jeopardizing its ability to model system performance. Subsequently, the motoring loops were left open, spin profiles were defined, and the EBA drive signals were left unused.

The simplified gyroscope motoring models are presented in Figures A-2 and A-3 of Appendix A. Resolver R500 and R530 (Figure A-2) produce the sines and cosines of the primary and secondary spins respectively. They are placed into operation by FF440. Primary spin rate is determined by integrator I032 and servo-set potentiometer C051. The initial condition for I032 is determined by C150. Its value, I, defines the pre-launch spin rate. The upper value, F, on the limiter L112 defines the final post-launch spin rate. The value, R, on C100 defines the rate at which the spin rate is ramped from pre-launch to post-launch. Scaling, in Hertz, for the output of I032 is 200 (100V = 200 Hz).

Secondary spin rate is directly proportional to the primary rate and is defined by the value, S, of C052. "-S" is used since the secondary rotates in a direction opposite of the primary.

Rectangular coordinates of the instantaneous field-of-view (IFOV) in the rosette scan are developed using Amplifier A112. and A132. Figure 2 illustrates the horizontal and vertical components of the primary and secondary optical vectors which are summed to form the IFOV. Conventions were chosen based on the physical relationships of magnets and coils in the seeker head. The summation equations are given in Equation 14 and Equation 15 respectively.

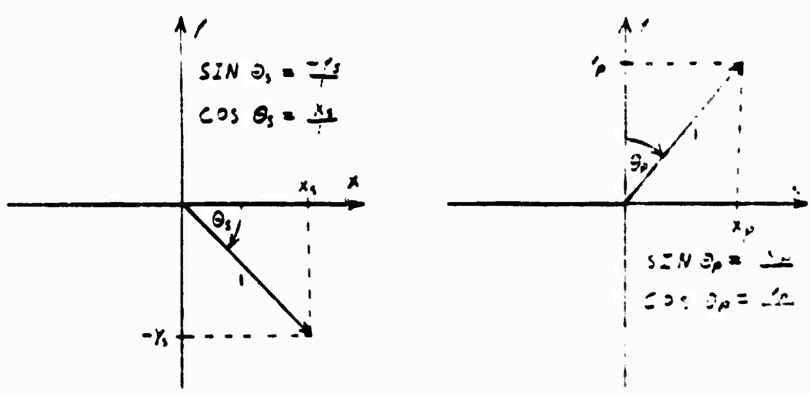

Figure Rosette Optical Vector Components

$$XROST = .5\ (SINUPT + COSUST) \quad (14)$$

$$YROST = .5\ (COSUPT - SINUST) \quad (15)$$

R510 (Figure A-3) produces the sine and cosine of roll. Control logic for the resolver is discussed in Section 2. Roll rate is developed in the digital program and transferred via a DAC through Red Trunk TR552. FF040 and FF221 are diagnostic tools that will be discussed in Section 7. Since roll is in a direction which is negative with respect to the chosen convention, it is subtracted from primary and secondary spin before the signals are sent to the EBA as reference signals. For the secondary signal, this is done in R530 (Figure A-2). The output, R531, is used as the Secondary Reference Coil and is defined by Equation 16.

$$XPRIM2 = SINUPT \cdot COSPT - COSUPT \cdot SINPT \quad (16)$$

Equation 16 is a quadrature representation of Equation 17.

$$XPRIM2 = SIN(\omega_p t - \dot{\rho} t) \quad (17)$$

where ωp = secondary spin rate (rad/sec)
$\dot{\rho}$ = roll rate (rad/sec)
t = time.

It should be noted that the subscript "p" represents prism which is the same as secondary. The subscript "s" is similarly used to represent spin which is the same as primary. This use of "s" and "p" is quite often confusing when examining the primary and secondary gyro reference signals.

Roll is subtracted from the primary in R510 (Figure A-3). Its outputs are defined by Equation 18 and Equation 19.

$$XPRIM3 = SINUST \cdot SINPT + COSUST \cdot COSPT \quad (18)$$

$$YPRIM3 = SINUST \cdot COSPT - COSUST \cdot SINPT \quad (19)$$

Equation 18 and Equation 19 are quadrature representations of Equation 20 and Equation 21 respectively.

$$XPRIM3 = COS(\omega_s t - \dot{\rho} t) \quad (20)$$

$$YPRIM3 = SIN(\omega_s t - \dot{\rho} t) \quad (21)$$

where ωs = primary spin rate (rad/sec).

The summation of -.1060(XPRIM3) and -.1696(YPRIM3) by A231 is used to adjust the phase of primary reference signal presented to the EBA, which in turn determines system phasing. A complete discussion of system phasing is presented in Section 8.3.

3.3 Gyroscope Model

The basic gyroscope model is presented in Figures A-4 through A-6 [1]. Three basic equations are modeled. The first two are the basic dynamics equations of elevation (θ) and azimuth (Ψ). They are presented in Equation 22 and Equation 23 respectively.

$$\ddot{\theta}_G = -(D_G/J_G)\dot{\theta}_G - (I_G/J_G)\omega_s\dot{\Psi}_G + (K_m/J_G)\dot{\sigma}(\sin\omega_s t)f(|\beta_z|) + (D_G/J_G)\dot{\Psi}_{GD} \quad (22)$$

$$\ddot{\Psi}_G = -(D_G/J_G)\dot{\Psi}_G + (I_G/J_G)\omega_s\dot{\theta}_G - (K_m/J_G)\dot{\sigma}(\cos\omega_s t)f(|\beta_y|) - (D_G/J_G)\dot{\theta}_{GD} \quad (23)$$

where:

$\dot{\theta}_G$, $\dot{\Psi}_G$ = projections of gyro spin axis precession rate in the X-Z (elevation) and X-Y (azimuth) planes respectively (degree/second)
D_G = viscous damping (ft-lb-sec)
J_G = gyro transverse moment of inertia (slug-ft^2)
I_G = gyro polar moment of inertia (slug-ft^2)
K_m = gyro gain (ft-lb-sec)
$\dot{\sigma}$ = seeker tracking rate signal (deg/sec)
β_Y, β_Z = projection of the look angle in the X-Z and X-Y planes respectively (deg)
$\dot{\theta}_{GD}$, $\dot{\Psi}_{GD}$ = projections of the g-dependent drift velocity in the X-Z and X-Y planes respectively (deg/sec)
$f(|\beta_z|)$, $f(|\beta_y|)$ = physical cage coil precessibility functions.

The third equation is a representation of the cage coil signal which is returned to the EBA. It is presented in Equation 29 with Equation 24 through Equation 28 being intermediate equations.

$$\beta_z = \Psi_G - \Psi_M + \theta Q' \quad (24)$$

$$\beta_y = \theta_G - \theta_M - \Psi R' \quad (25)$$

$$\beta_{TACT} = \sqrt{\beta_y^2 + \beta_z^2} \quad (26)$$

$$\beta_{TACT} \cos(\omega_s t - \phi_B) = \beta_y \cos \omega_s t + \beta_z \sin \omega_s t) \quad (27)$$

$$FBTCC = f(\beta_{TACT}) \quad (28)$$

$$ECAGE = [FBTCC \cdot \omega_s \cdot \beta_{TACT}]\cos(\omega_s t - \phi_B) \quad (29)$$

where:

θ_M, Ψ_M = projections of missile center line in the X-Z (pitch) and X-Y (yaw) planes respectively (deg)

$\theta Q'$, $\Psi R'$ = empirical body-rate/gyro-rate look angle components (deg)

β_{TACT} = total look angle (deg)

$\beta_{TACT}COS(\omega_s t - \phi_B)$ = real, spin frequency modulated look angle signal

ϕ_B = phase modulation factor

FBTCC = physical cage coil amplitude function

ECAGE = real, spin frequency modulated cage coil signal

A correlation between schematic variables and equation variables is presented in Table 2.

$\dot{\theta}_G$, $\dot{\Psi}_G$	= THEG1, PSIG1
$COS\omega_s t$, $SIN\omega_s t$	= COSUST, SINUST
$f(\lvert\beta_z\rvert)$, $f(\lvert\beta_y\rvert)$	= FBZ, FBY
θ_{GD}, Ψ_{GD}	= THG1DR, PSG1DR
β_y, β_z	= BY, BZ
$\dot{\delta}$	= PRECMD
ω_s	= US = FS
θ_G, Ψ_G	= THEG, PSIG
θ_M, Ψ_M	= PITCH, YAW
$\theta Q'$, $\Psi R'$	= THEG1Q, PSIG1Q
β_{TACT}	= BTACT

Table 2
Gyroscope Equation/Schematic Variable Relations

Examining Figure A-4, precession is presented to the gyro model by the EBA via TR502. Multiplier M343 and M344 scale the precession signals, used by the elevation and azimuth channels respectively, by the precessibility functions. Tables B-1 and B-2 in Appendix B contain the data for these functions. A plot of the functions is presented in Figure B-1. A detailed explanation of these functions, along with additional gyro analyses, is presented in Reference [2]. M124 and M134 demodulate the precession signal in elevation and azimuth respectively. The combined inputs to I020 and I030 represent $-\ddot{\theta}_G$ and $-\ddot{\Psi}_G$ respectively. Each input can be identified as a term from Equation 22 and Equation 23. The outputs then represent $\dot{\theta}_G$ and $\dot{\Psi}_G$. I210 and I220 are diagnostic tools used for tailoring and static gain curve generation. They are discussed further in Section 7.3.8.

In Figure A-5, θ_G and Ψ_G are developed by I010 and I022 respectively. In addition to inputs $\dot{\theta}_G$ and $\dot{\Psi}_G$, TG551 and TG552 can be used to impart gyro rates from the digital program for diagnostic purposes. C012 and C102 can be used to define constant initial pointing angles. They are useful for tailoring and diagnostics. Pointing angles, θ_G and Ψ_G, are sent to ADC's for the digital program via TR521 and TR522 respectively. Control logic for I010 and I022 is discussed in Section 2.0. A011 and A023 are used to develop the look angles in elevation and azimuth respectively. Body angles are subtracted from gyro pointing angles in their respective planes to derive the true planar look angles. Body pitch and yaw angles are received from DAC's via TR540 and TR541 respectively. The terms from A031 and A021 are empirically derived components of body and gyro pitch and yaw rates. They were derived in an effort to make the analytical model match the physical device. M103 and M104 then begin the process of developing total look angle and M125 and M143 begin the process of modulating the cage coil signal at the primary spin frequency.

In Figure A-6, a real, spin frequency modulated look angle signal is produced by A122. Its amplitude is then scaled by the other components in the figure to develop the cage coil signal, which is sent to the EBA via TR441. It is multiplied by the spin rate term at M123. Then it is multiplied by another term, which represents the physical electrical design of the cage coil, at M133. The total look angle, which is finally developed at Square-rooter 105, is used to drive the function which defines that term. Data for the function can be found in Table B-3 of Appendix B. A plot of the function is presented in Figure B-2.

Additionally in Figure A-6, comparator CM450 is used to inform the digital program when the maximum possible gyro look angle has been exceeded. That valve, FOVL, is defined by C543. The discrete signal is transmitted via the TG13.

The gyro drift terms, which are presented to I020 and I030 in Figure A-4, are illustrated in Figure A-14. Data for the function generators are listed in Table B-4 (Radial Drift) and Table B-5 (Tangential Drift) in Appendix B. A detailed explanation of the radial and tangential drift models can be found in Reference [2].

3.4 Target Models

Initial simulation design envisioned use of an Electronic Target Signal Generator (ETSG). Delays in its development led to the design of a simple square, logical target on the EAI-781. Its purpose was to drive the simulation so that simulation development could be expedited. However, it worked so well that other geometric targets were developed on the EAI-781. This, coupled with continuing ETSG problems, led to the abandonment of the ETSG and the sole use of targets implemented on the analog computer.

Targets are modeled on the EAI-781 by using equations to define regions of space. As the IFOV scans the rosette pattern, target equations determine whether the point is within or outside the boundaries of the respective target. If it is within, a logic output gates an analog switch to present an intensity function to the summation amplifier for the particular spectral channel. If the IFOV is outside the boundary, the switch is left open with no input being provided to the summation.

The word "target" refers to each individual source which may be summed to develop a composite signal for each channel. Four sources are available for the infrared (IR) channel. They are a circle (point source), a rectangle (body), a triangle (plume), and a square (flare). Three sources are available for the ultra-violet (UV) channel. They are a circle, a rectangle, and a square. However, only one boundary is defined for both the IR and UV circles; only one boundary is defined for the rectangles; and only one boundary is defined for the squares. This is possible due to the fact that each boundary defines a target which presents two coincident spectral sources.

Using comparators to generate boundaries for targets means that rectangular pulses are produced. This is due to the fact that the IFOV is defined by a point. Figure 3 illustrates the process by which a pulse is generated as a "point" IFOV scans across a circular target. However, the optics in an actual seeker are such that the IFOV has a definite size (blur size) that was designd into the system. Figure 4 illustrates the pulse generation process that occurs in an actual seeker. The pulse that results from this true convolution process is notably different from the rectangular pulse.

The validity of using rectangular pulses with the Stinger POST EBA is quite acceptable though. This is due to the fact that the 2nd order filters in its pre-amp circuits well represent only the energy contained in the pulse. The pre-amps are rather insensitive to pulse shape. However, a bias in target size must be added to compensate for differences in pulse width. This bias was determined empirically by adjusting the size of a point source (circle) target until the pulse width matched that measured during an actual seeker head test. The difference between the theoretical and empirical sizes of a point source is used as the bias for all target size calculations.

The basic target shapes (except flares) all have a single point (key point) in common when they are used in a composite target. Figure 5 shows an example target shape and its key point. This permits the calculation of only one error signal to define the position of the composite target within the rosette pattern. Additionally, target position and orientation in the pattern are relative. Target motion and changes in orientation can be modeled by pattern offsets (Figure 6) and rotation (Figure 7) of the pattern respectively.

Figure A-7 shows the circuitry that performs the translation and rotation functions. Target error signals in elevation and azimuth, relative to the center of the rosette, are calculated in the digital program. They are presented to the analog model through DAC's via TG402 and TG401 respectively. FF450, Handset Potentiometer HS134, HS135, Function Relay K050, and K051 are used for manual control of target position. The rotation (target orientation) angle is calculated similarly and presented via TG411. Translations in elevation and azimuth are performed in A223 and A233, respectively, using the rosette signals from Figure A-2 and the error signals. R550 performs the rotation function. Equations for the translated and rotated rosette signals are presented in Equation 30 and Equation 31.

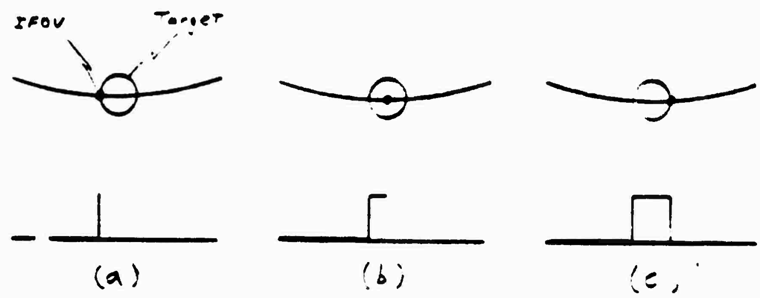

Figure 3 Generation of Detector Signal with Logic

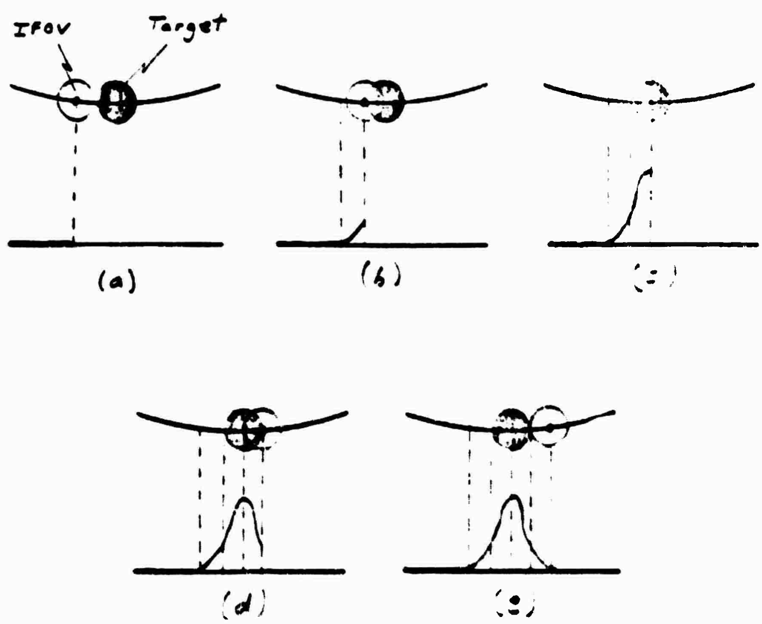

Figure 4 Convolution of IFOV and Source with a Real Detector

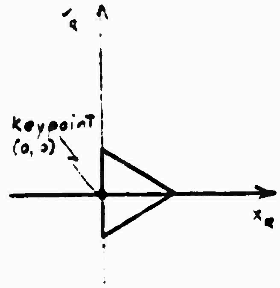

Figure 5 Basic Target Shape with Keypoint

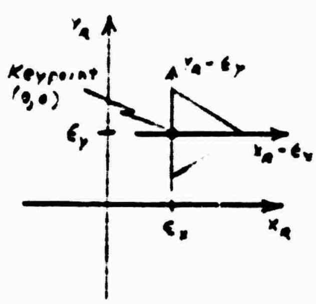

Figure 6 Target Translation

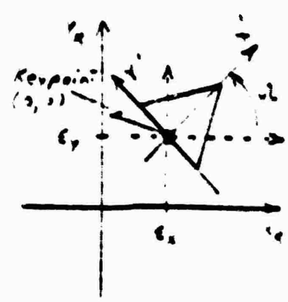

Figure 7 Target Translation and Rotation

$$X' = (Y_R - \varepsilon_y)\sin\Omega + (X_R - \varepsilon_x)\cos\Omega \tag{30}$$

$$Y' = (Y_R - \varepsilon_y)\cos\Omega - (X_R - \varepsilon_x)\sin\Omega \tag{31}$$

where X_R, Y_R = normalized IFOV position in elevation and azimuth respectively

X', Y' = normalized, translated and rotated IFOV position in elevation and azimuth respectively

ε_y, ε_y = composite target error signals, relative to the center of the rosette pattern, in elevation and azimuth respectively

Ω = composite target orientation angle (deg).

Table 3 presents a correlation between schematic variables and equation variables.

X_R, Y_R	= XROST, YROST
X', Y'	= XPRIMR, YPRIMR
ε_x, ε_y	= EPSIZT, EPSIYT
Ω	= THR
$(X_R - \varepsilon_x)$, $(Y_R - \varepsilon_y)$	= XNEW, YNEW

Table 3 Target Equation/Schematic Variable Relations

3.4.1 Circles (Point Sources)

Circle generation circuitry is presented in Figure A-8 in Appendix A. The equation for a circle is presented in Equation 32.

$$(X')^2 + (Y')^2 = r^2 \tag{32}$$

M335 and M345 form $(X')^2$ and $(Y')^2$ respectively. A342 performs the summation of the two. Therefore, the output of A342 represents the radius$^{(r)}$ squared of a circle defined by the instantaneous location of the IFOV. It is important to remember that, effectively, translation and rotation relative to the rosette scan pattern has already been performed with the circuitry illustrated in Figure A-7. Circle radius is defined in the digital program, sent to a DAC, and presented to the model via TR412. It is presented to CM250 along with the output of A342. The inverted output of CM250 is high if the radius of the circle defined by the effective position of the IFOV is less than the radius of the target. In other words, the inverted output is high as the IFOV passes through the region of the target. Equation 33 is true for this condition and represents the operation of CM250.

$$PCSQO - RCSQ \leq 0 \quad \text{or} \quad RCSQ \leq PCSQO \tag{33}$$

where PCSQO = target radius squared (rad^2)

$RCSQ = (X')^2 + (Y')^2$.

The shaded area shown in Figure 8 represents the region where $(X')^2 + (Y')^2 < r^2$.

In Figure A-8, C551, C343, and C350 are used for scaling matching. K251, HS144 and FF440 are used to allow manual control of target size.

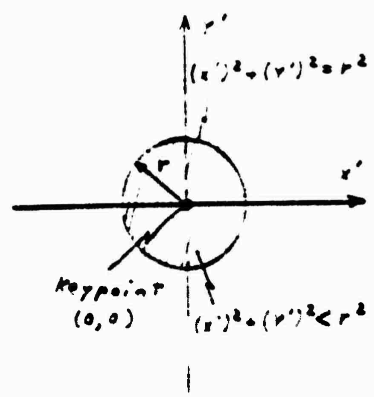

Figure 8 Circle $(x')^2 + (Y')^2 \leq r^2$

The intensity functions for IR and UV are contained in Diode Function Generator (DFG) F101 and F111 respectively. They are a function of range which is input from the digital program via a DAC and TG412. They are gated into their respective detector summations by analog switch (S) 020 and S401 respectively. S020 and S401 are controlled by the inverted output of CM250. HS145, K010, K401, and FF251 are used to allow manual control of intensity.

The contents of F101 and F111 represent a particular target and are changed for each new target. Therefore, representative programs are not presented in this report but will be presented in following validation reports. Additionally a complete discussion on the use of the circular target in the modeling of a composite target is presented in Reference [3].

3.4.2 Rectangle (Body)

Rectangle region generation circuitry is presented on the lower portion of Figure A-9 in Appendix A. The region of the rectangle is defined by the intersection of four regions of space. These four regions are represented by Equation 34 and Equation 35 where each equation defines the intersection of the two regions

$$- RL \leq X' \leq 0 \tag{34}$$

$$- WR/2 \leq Y' \leq WR/2 \tag{35}$$

where: RL = rectangle length (rad)

WR = rectangle width (rad).

Again, it is important to remember that, effectively, translation and rotation has already been performed with the circuitry illustrated in Figure A-7 (X' and Y').

Rectangle length and width are presented to the model by the digital program via DACs and TR542 and TR543 respectively. The inverted output of CM251 is logic high for $X' \leq 0$; the output of CM 031 is logic high for $X' \geq RL$; the output of CM040 is logic high for $Y' \geq -WR/2$; and, the output of CM041 is logic high for $Y' \leq WR/2$. The output of And Gate (AND) 3B then represents the intersection of these four outputs (regions) and defines the region of the rectangle.

A graphical representation of the region is shown in Figure 9.

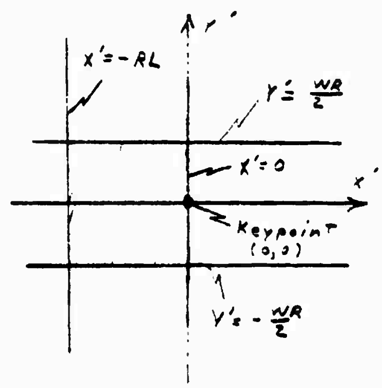

Figure 9 Rectangle $(RL \leq X' \leq 0) \cap (-WR/2 \leq Y' \leq WR/2)$

Note that the keypoint is offset to one side with a particular initial orientation defined for the rectangle. Since the rectangle is used to represent an aircraft body, provisions must be made to properly mate it to a plume model (triangle). Comparing this offset and orientation to the triangle's offset and orientation shown in the next section reveals how the mating is achieved.

An aircraft body has both IR and UV spectral content. Therefore, the output of AND3B is used to gate two intensity functions (See Figure A-13 in Appendix A). AND3B controls S011 and S050 for the IR and UV summation inputs respectively. The functions are stored on Multi-Variable Function Generators (MVFGs). Aspect angle and range are generated by the digital program and transferred to the model via DACs and TG400 and TG412 respectively. They are then presented to the IR MVFG via TG301 and TG300 respectively, and to the UV MVFG via TG213 and TG212 respectively. The IR MVFG output is received via TR320; the UV MVFG output is received via TG222. Again, representative MVFG programs are not presented in this report but will be presented in following validation reports, and a rectangle usage discussion can be found in Reference [3].

FF431, K431, K421, HS125, and HS115 in Figure A-9 are used to allow manual control of rectangle length and width. FF251, K240, K011, and HS145 in Figure A-13 are used to allow manual control of intensity.

3.4.3 Triangle (Plume)

Triangle region generation circuitry is presented on the upper portion of Figure A-9 in Appendix A. The region of the triangle is defined by the intersection of three regions of space. These three regions are represented by Equation 36 and Equation 37. Equation 37 represents the intersection of two regions.

$$X' \geq 0 \tag{36}$$

$$[(-W/L)X' + W] \leq Y' \leq [(W/L)X' - W] \tag{37}$$

where: W = half width of isoceles triangle base (rad)

L = isoceles triangle length from center of base (rad).

Again, it is important to remember that, effectively, translation and rotation has already been performed with the circuitry illustrated in Figure A-7 (X' and Y').

The triangle is isoceles in shape. The half width of its base and its length, measured from the center of its base, are presented to the model by the digital program via DACs and TG410 and TG403 respectively. The output of CM251 is logic high for $X' \geq 0$. This determines the first region. Divider (D) 304 produces W/L and M314 then produces $-(W/L)X'$. A400 performs a summation to produce $(W/L)X' - W$, and CM431 generates a logic high when $(W/L)X' - W - Y' \geq 0$. Subsequently, this output determines the second region $[Y' \leq (W/L)X' - W]$. A401 also produces $-(W/L)X'$ and is a result of the developmental process. It feeds CM410 which generates a logic high when $(W/L)X' - W + Y' \geq 0$. The third region $[Y' \geq -(W/L)X' + W]$ is determined by this output. ANDOG performs the intersection of the three regions to define the region of the triangle.

A graphical representation of the region is shown in Figure 10.

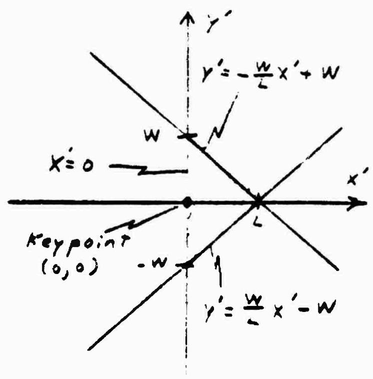

Figure 10 Triangle - [X' ≥ 0] [(-(W/L)X' + W) ≤ Y' ≤ ((W/L)X' - W)]

Note the location of its keypoint and its orientation. The triangle is used to represent an aircraft plume, and provisions have been made to properly mate it to the body (rectangle) model. Comparing the offsets and orientations of the two reveals how the mating is achieved.

An aircraft plume primarily has only IR spectral content which implies the need for only one intensity function. However, that one function is rather complex with an intensity gradient being distributed over the plume. Circuitry illustrated in Figure A-10 of Appendix A provides a two-slope, linear gradient function.

A452 sums three components to generate the composite gradient. C503 first generates a dc level for the plume.

D324 generates -X'/L while A442 and L121 are used to insure 0 ≤ X'/L ≤ 1. A450 then generates 1 - X'/L, which is the first normalized linear gradient. It is illustrated in Figure 11, and it is scaled by C502.

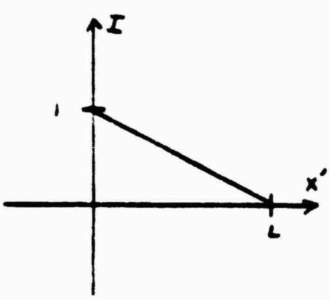

Figure 11 First Linear Plume Gradient

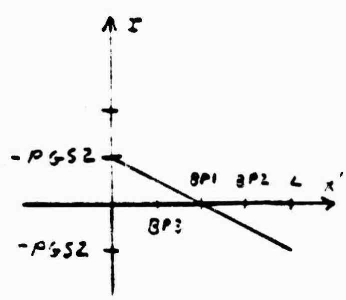

Figure 12 Second Linear Linear Plume Gradient

A432 takes the output of A450 and adds a value, PGS2, to generate 1-PGS2-X'/L, which is the second normalized linear gradient. It is illustrated in Figure 12. However, to form a breakpoint in the composite two-slope gradient, S431 and AND3A are used to gate the second gradient. CM200 and C511 (PBP) are used to define the normalized breakpoint with a logic high being generated if PBP-X'/L $\geq$ 0 (X'/L $\leq$ PBP). C501 scales the second gradient.

PBP is generally chosen so that the composite model is represented by case (a) in Figure 13. However, case (b) or case (c) can be generated if other breakpoints are chosen. Reference [3] includes a program to determine potentiometer settings for chosen configurations. CM210, C523 and TG400 (Aspect Angle) can be used to make the breakpoint a function aspect angle also.

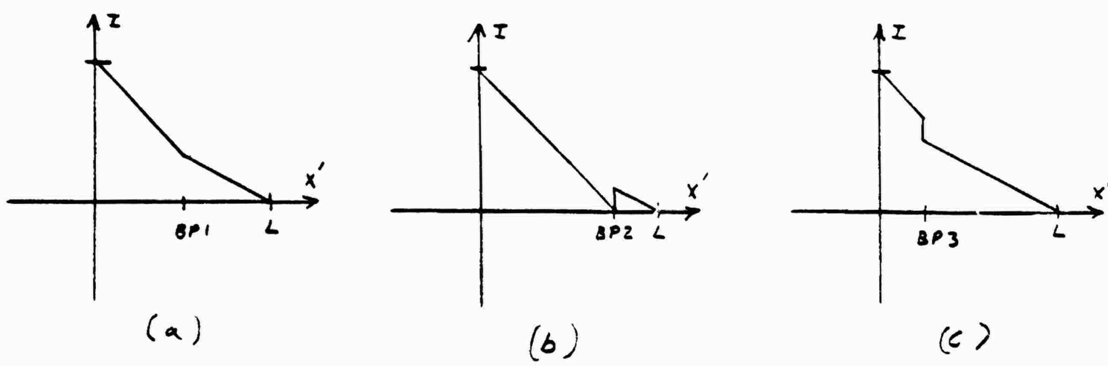

Figure 13 Composite Plume Gradient as Function of Breakpoint

The composite gradient model is scaled by an intensity function, which is a function of range and aspect angle, before the result is gated into the IR detector summation amplifier. The function resides in an MVFG. Aspect angle (TG400) and range (TG412) is provided to the MVFG via TG211 and TG210 respectively. Its output is received via TG220, and the scaling is performed by M355. Again, representative MVFG programs are not presented in this report but will be presented in following validation reports, and a triangle usage discussion can be found in Reference [3].

Gating is performed by the output of the triangle region generation circuitry (ANDOG) from Figure A-9 and A-240. FF441 and K250 are used to allow manual control of plume intensity if desired.

3.4.4 Flare

Flare region generation circuitry is presented in Figure A-11 in Appendix A. The flare is modeled as a square (Figure 14) and is a simplified form of a rectangle. However, since a flare separates from the composite target model during a flight, independent positioning must be performed for the flare. Independent elevation and azimuth error signals, relative to the center of the rosette pattern, are presented to the model by the digital program via DAC's and TR400 and TR402 respectively. A413 subtracts the azimuth error signal from X_R, and A403 subtracts the elevation error signal from Y_R. The result is a new translated set of axes (Figure 15).

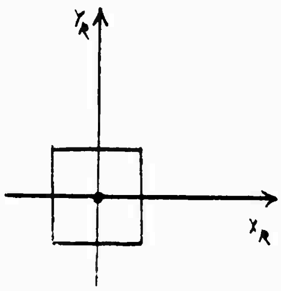

Figure 14 Square (Flare) Region

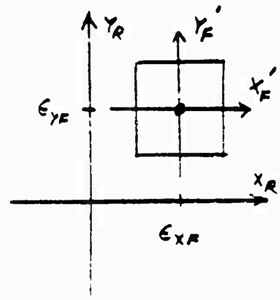

Figure 15 Translated Square (Flare)

The translation is represented by Equation 38 and Equation 39.

$$X'F = X_R - \varepsilon xF \tag{38}$$

$$Y'F = Y_R - \varepsilon yF \tag{39}$$

where: X'F, Y'F = translated flare axes

$\varepsilon_x F$, $\varepsilon_y F$ = azimuth and elevation flare error signals relative to rosette pattern center (rad)

Rotation circuitry is not required though since its size is always about as small as a point source.

Like the rectangle, the square is defined by the intersection of four regions of space. These four regions are represented by Equation 40 and Equation 41. The intersection of two regions is defined by each equation.

$$-FLSZ/2 \leq X'F \leq FLSZ/2 \tag{40}$$

$$-FLSZ/2 \leq Y'F \leq FLSZ/2 \tag{41}$$

where FLSZ = flare size (rad)

X'F is presented to CM000 and CM420 while Y'F is presented to CM211 and CM430. Flare size remains constant during a flight, so it is defined by C553. FLSZ/2 is then presented to CM000 and CM211, and -FLSZ/2 is presented to CM420 and CM430. The output of CM000 is a logic high for X'F $\geq$ -FLSZ/2; the inverted output of CM420 is "high" for X'F $\leq$FLSZ/2; the output of CM211 is "high" for Y'F $\geq$-FLSZ/2; and, the inverted output of CM430 is "high" for Y'F$\leq$ FLSZ/2. The output of AND1G then represents the intersection of the four outputs (regions) and defines the region of the square. A graphical representation of the flare region is in Figure 16.

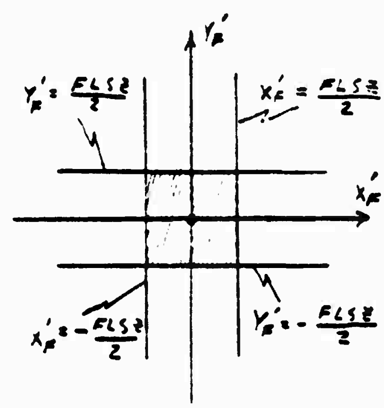

Figure 16 Flare-(-FLSZ/2 $\leq$ XF $\leq$ FLSZ/2)$\cap$(-FLSZ/2 $\leq$ Y'F $\leq$ FLSZ/2)

AND5G is used to gate the flare on or off under external control. Utilizing AND6B, AND6C, and AND3C, flare circuitry is turned on by the digital program via T002. AND3C is the final output that initiates the flare's intensity profile model. And, FF231 and FF411 perform diagnostic functions.

Flare IR and UV intensity functions are illustrated in Figure A-12 in Appendix A. I411, C223, and C233 are combined to simply form a timer. It is put into operation by a logic low from AND3C, illustraed in Figure A-11. The timer drives F120 which contains the time dependent flare profile. Its output is then scaled by a range and azimuth dependent function which resides in a MVFG. The digital program provides the flare model with the range to the flare and aspect via DACs and TR403 and TG400 respectively. They are then sent to the MVFG via TG302 and TG303 respectively. Its output is received via TR322, and M325 performs the actual scaling. The resulting intensity function is then gated by the output of the flare logic circuitry (AND5G) and S000. This output represents the IR spectral output of the flare.

The UV spectral output of a flare is generally short lived and can be modeled directly from the IR spectral output. Therefore, the output of A003 is gated by S010 and CM010. The inverted output of CM010 simply shuts off the signal after a present amount of time determined by C541. Time is provided to CM010 by the flares master timer (I411). The output of S010 then represents the UV spectral output of the flare.

3.4.5 Integrated Detector Signals

The composite detector signals are developed by A451 and A252, illustrated in Figure A-13 in Appendix A. A451 sums the individual contributions from the target models, and its output, the simulated IR detector signal, is sent to the EBA via TR440. C250 scales the circle input; C252 scales the rectangle input; C301 scales the noise input; and, C251 scales the triangle input. The flare input comes from A033, illustrated in Figure A-12, and its input is scaled by C032. The other inputs to A033 allow for the addition of more flares. L150 limits A033 to a value between -100V and +100V. System saturation occurs at ±125V.

Similar to the IR channel, A252 performs the UV summation, and its output is sent to the EBA via TR452. C300 scales the noise input; C342 scales the rectangle input; and, C253 scales the circle input. The flare input comes from A211 (Figure A-12), and its input is scaled by C453. Its limiting is performed by L130.

3.5 Wing Servomechanism Model

The wing servomechanism used in Stinger/POST is unchanged from that of Stinger. Its transfer function is presented in Figure 17, and its EAI-781 model is illustrated in Figures A-15 and A-16 in Appendix A. The model is hybrid in nature, employing large percentages of both analog and logic components. This is necessary because the wing servomechanism is a single oscillating wing set. Subsequently the system is roll dependent.

The wing servo model is rather complex, but there is only one input and one output. Wing command (δc) is developed by the EBA and presented to the model via the Hybrid Interface Signal Conditioner (HISC - See Section 6.2) and TR501. Its output, wing incidence, is used by the digital program. It is received via TR520 and an ADC.

The model is maintained by MICOM personnel who manage the Analog Computer Room. They possess design information and diagnostic tools. Since the design is essentially the same as a previous model used for Stinger, a high degree of confidence has been developed in the model. Documentation of impulse response, step response, etc. is used in the event of failures in the model. Of the EAI-781 models, it has the greatest failure rate. However, MICOM personnel are quite adept at diagnosing and correcting any failures that occur in the model.

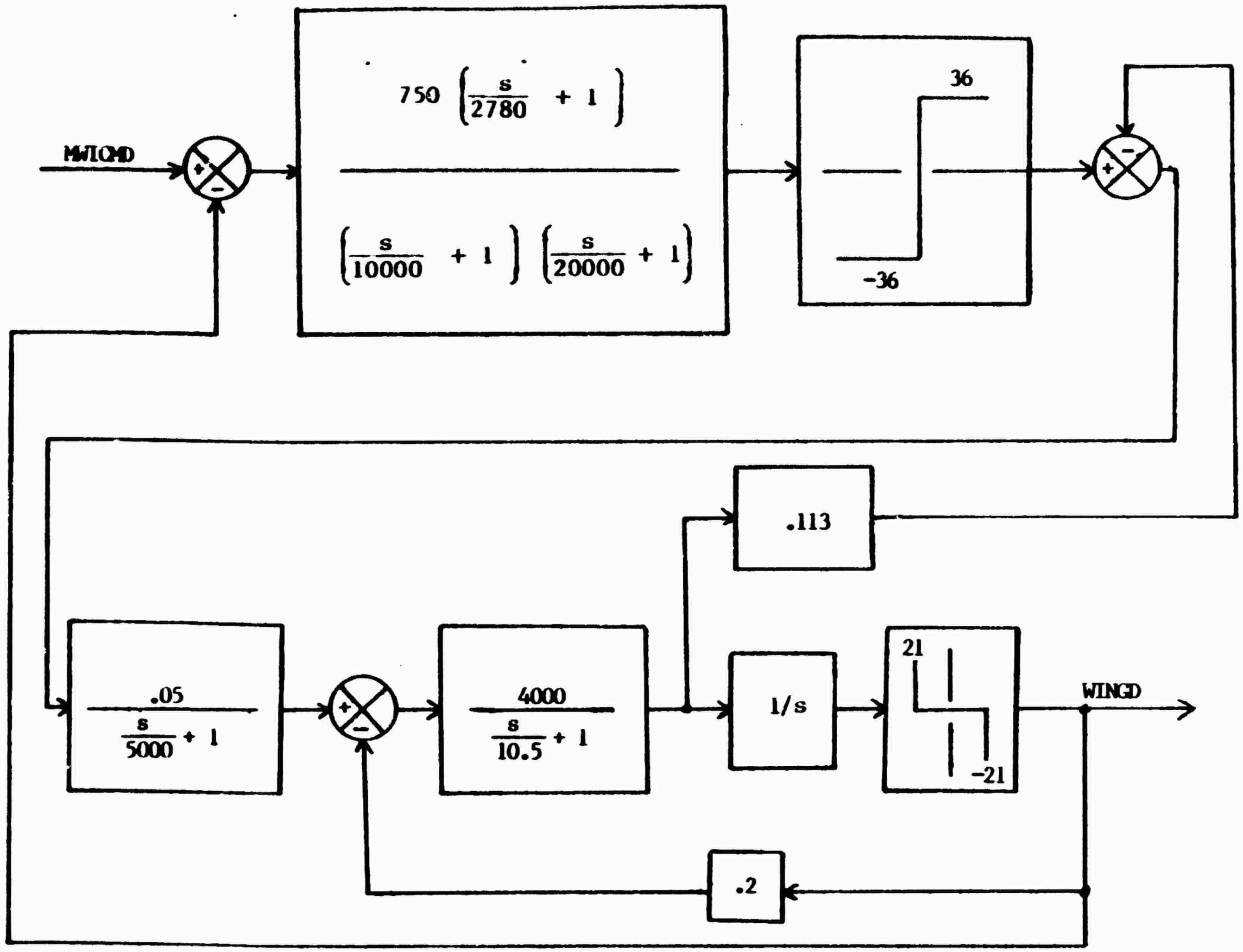

Figure 17 Wing Servomechanism Transfer Function

3.6 Function Generators

There are two types of function generators used in the simulation with the analog models described in the previous sections. The most simple type is the Diode Function Generator (DFG). It provides a single function of one variable with 16 break points. The DFG is an integral component of the EAI-781. The first three data sets presented in Appendix B are for DFG's.

Multi-Variable Function Generators (MVFGs) are separate from the EAI-781 and must be accessed via trunking stations. Depending upon the chosen mode, four one-variable functions, two two-variable functions, one three-variable function, or two one-variable and one two-variable functions can be provided by one MVFG. MVFGs are accessed via the trunking stations in pairs. The modes and possible configurations for a pair of MVFGs are presented in Table 4 and Table 5 respectively. The last two data sets presented in Appendix B are for MVFGs.

Mode	Description
1	Four functions of one variable each
2	Two functions of two variables each
3	Two functions of one variable each and one function of two variables.
4	One function of three variables.

Table 4 MVFG Modes

Mode	Function Number	Argument Number	Trunking Station Address: Argument	Trunking Station Address: Function	Output Hole
1	1	1	X V208	V210 $F_1(x)$	1
	2	1	Y V209	V211 $F_1(y)$	2
	3	1	Z V20A	V212 $F_1(z)$	3
	4	1	W V20B	V213 $F_1(w)$	4
	5	1	X V208	V214 $F_2(x)$	5
	6	1	Y V209	V215 $F_2(y)$	6
	7	1	Z V20A	V216 $F_2(z)$	7
	8	1	W V20B	V217 $F_2(w)$	8
2	1	1	X V208	V210 $F_1(x,y)$	1
		2	Y V209		
	2	1	Z V20A	V212 $F_1(z,w)$	3
		2	W V20B		
	3	1	X V208	V214 $F_2(x,y)$	5
		2	Y V209		
	4	1	Z V20A	V216 $F_2(z,w)$	7
		2	W V20B		
3	1	1	X V208	V210 $F_1(x)$	1
	2	1	Y V209	V211 $F_1(y)$	2
	3	1	Z V20A	V212 $F_1(z,w)$	3
		2	W V20B		
	4	1	X V208	V214 $F_2(x)$	5
	5	1	Y V209	V215 $F_2(y)$	6
	6	1	Z V20A	V216 $F_2(z,w)$	7
		2	W V20B		
4	1	1	X V208	V210 $F_1(x,y,z)$	1
		2	Y V209		
		3	Z V20A		
	2	1	X V208	V214 $F_2(x,y,z)$	5
		2	Y V209		
		3	Z V20A		

Table 5 MVFG Trunking Station Patching

4.0 ELECTRONICS BREADBOARD ASSEMBLY (EBA)

The Electronics Breadboard Assembly (EBA) is a collection of seven circuit card assemblies (CCAs) mounted on a motherboard within a frame. One CCA is used to aid diagnostics. It serves as an interface between the motherboard and front panel and controls the display circuitry on the front panel. The other six cards contain circuitry which closely duplicates that used by a Stinger POST guidance assembly. However, the six cards primarily use off-the-shelf, dual-in-line package (DIP) integrated circuits (ICs). An actual guidance assembly uses basic IC chips, mounted on printed substrates, to form hybrid microcircuit wafers.

The EBA is designed to perform three primary functions. First it has circuitry to maintain the speed of the gyroscope's primary and secondary mirrors. However, since operation of this circuitry is seldom critical to overall system performance, it has been bypassed. A primary speed profile with a constant relative secondary speed has been defined at the EAI-781. The second function is to maintain gyroscope tracking of a target in space. The EBA processes IR and UV detector signals, primary and secondary reference signals, and a cage coil signal to develop a precession signal to perform this function. The third function is to maintain missile guidance. A wing command signal is developed from the precession, cage coil, and reference signals to perform this function.

Through the course of development of the hybrid simulation, several hardware and firmware programs used by microprocessors on CCA#4 and CCA#5 have evolved with the Stinger POST program. Hardware descriptions can be found through a large number of General Dynamics-Pamona (GD/P) documents. The most useful sources of information are the GD/P schematics of the EBA and Reference [4]. That reference describes the major EBA signals of the configuration first received at MICOM. However, EBA hardware changes have been performed in two stages at MICOM to match two revision levels. Descriptions of these changes are due to be published shortly in a final report for project A 3125 of the Georgia Institute of Technology Engineering Experiment Station. Firmware configurations have generally been a function of individual flight tests. A detailed outline of firmware configurations will be presented in an upcoming University of Alabama in Huntsville final report on Stinger POST hybrid simulation validation.

Use of the EBA in the simulation is best understood by examining its interface to the simulation. The hybrid interface signal conditioner described in Section 6.2 is used to perform the interface function. Additionally, detailed interface signal descriptions can be found in Reference [2]. Some of this information is classified as confidential and is not repeated in this report for that reason.

EBA failures were a frequent occurrence throughout the course of simulation development. It was received with several problems that were diagnosed and corrected. And, the need to frequently examine signals on various CCA's led to a large number of the failures. Subsequently several diagnostic capabilities were developed for the EBA. They are described in Section 7.2.

5.0 DIGITAL PROGRAM

The digital program is executed in real-time on a CDC 6600 large scale computer. It includes simulation executive control, the airframe model and target processing calculations. An operator executes the program through a station in the Digital Display System (DDS).

Executive control of the simulation is performed by the digital program. It first schedules all resources to be used by the simulation. Then after execution begins, the logical sequence of events of the simulated missile flight is directed by the program. The sequence is controlled with the assistance of the control logic on the EAI-781, (See Section 2.0). Control bits are output to the EAI-781 via a common block (*OD1S2), and status bits are received via a common block (*ID1S2). Common blocks are discussed in more detail in the interface section (Section 6.4).

The airframe model is contained in the digital program, and it is almost identical to the one used for the Stinger simulations. It models the motion of a rolling missile under single oscillating wing set control. Equations of motion for the model can be found in Reference [5]. Additionally, a detailed description of the airframe model and the complete digital program is currently being prepared by MICOM personnel.

Target processing calculations are performed to determine target location within the seeker's FOV and target size. In the current configuration, the program must only perform calculations for the "key point" (See Section 3.4) of the composite target and for the flare. Early in the simulation development cycle, it was anticipated that calculations would be required for a larger number of targets and that a Direct Cell would be required to transfer data. At that time, a timing study of the program's slow and fast loops was performed. That study and another discussion of the digital program can be found in Reference [6]. However, the relaxed requirements for the current configuration allows adequate time for good stability.

Both the airframe model and the target processing section require information from the analog models (Section 3.0) and generate information used by the analog models. The program interfaces with the models via ADC's and DAC's. Actual communication from and to the ADC's and DAC's is performed via common blocks (*ADC1 and *DAC1 respectively). Again, section 6.4 has an additional discussion on the role of common blocks as an interface tool.

The digital program was also used to develop diagnostic programs for the simulation. Portions of the main digital program have been extracted to build the programs described in Section 7.4.

6.0 INTERFACES

6.1 Introduction

The Stinger POST hybrid simulation contains a large number of interfaces. A layout of simulation components and their interconnections, is presented in Figure 18. Signal conditioning and support hardware required by the EBA are discussed in Section 6.2. Trunking stations are described in Section 6.3, and the interface between the digital program and the rest of the simulation is discussed in Section 6.4.

6.2 Hybrid Interface Signal Conditioner (HISC)

The Hybrid Interface Signal Conditioner (HISC) was designed to serve as an interface between the EBA and the rest of the simulation. When it was designed, the interface was much more complicated due to the fact that an Electronic Target Signal Generator (ETSG) was planned for use as a target source by the simulation. However, the development of targets on the EAI-781 and abandonment of the ETSG resulted in a greatly simplified interface. Subsequently, much of the HISC's circuitry has been bypassed and will not be discussed. Descriptions of each of the HISC's circuit cards will be presented in Sections 6.2.1 through 6.2.6.

6.2.1 Power Card

The power supply card provides regulated voltages to the other cards. Its schematic is presented in Figure C-1 in Appendix C, and its layout is presented in Figure C-7. Regulator (R)1 provides +15V from a 20V input; R2 provides -15V from -20V; R3 provides +5V from +8V; and, R4 provides -5V from -8V. The regulated voltages are available at the power supply card's front panel and are made available to all other cards in the HISC via the back-plane wiring. Back-plane wiring is presented in Figure 19 and a sketch of front view is presented in Figure 20.

6.2.2 Analog In Card

The Analog In card receives the differential analog signals originating from the trunking stations' analog buffers. Its schematic and layout are presented in Figure C-2 and Figure C-8 respectively. Five receivers are currently implemented on the card. Each receiver consists of two stages built from one LM747. The first stage inverts the input signal with respect to HISC common. The second stage then sums analog common with the inverted signal and inverts that result with respect to HISC common. The final receiver output is a clean, accurate, buffered signal.

The differential inputs come from the back-plane connector (A9). The receiver outputs are routed to the front panel. Gyro reference, secondary reference, and cage coil are the signals needed by the EBA. They are available at Jack (J) 3, J6, and J2 respectively. X-rosette (J4) and Y-rosette (J5) are the rectangular coordinates of the IFOV in the rosette pattern and are available for diagnostic purposes.

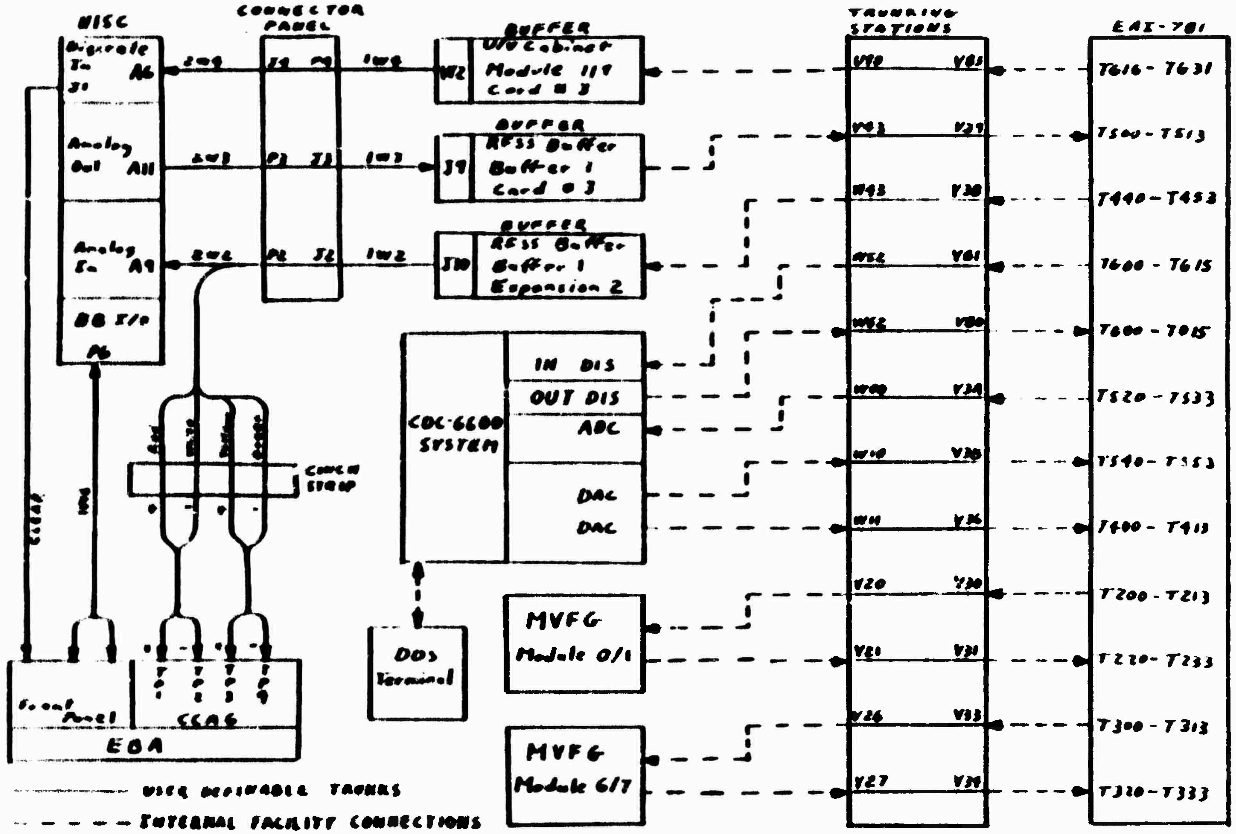

Figure 18 Stinger POST Simulation Interconnections

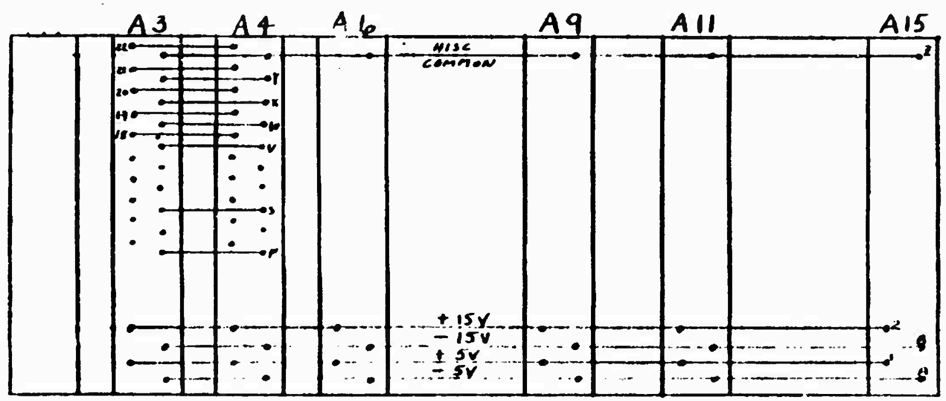

Figure 19 HISC Back-Plane Wiring

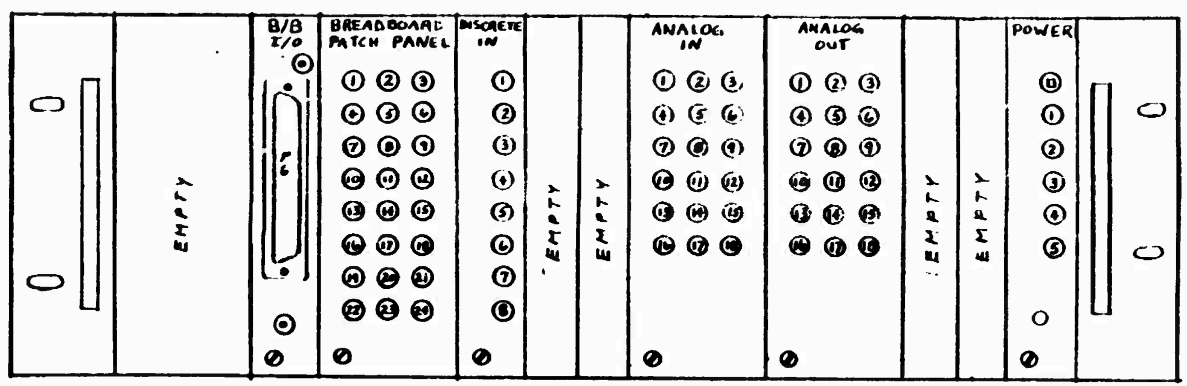

Figure 20 HISC Front View

6.2.3 Discrete In Card

The Discrete In card receives the differential logic signals originating from the trunking stations' digital buffers. Its schematic and layout are presented in Figure C-3 and Figure C-9 respectively. SN75108's are used as the receiving end of a transmitter/receiver pair. Three signals are received which are used to control the EBA. They are "cage," "launch," and "clear". "Cage" and "launch" are routed directly to the card's front panel at J2 and J3 respectively. The "clear" signal controls a normally-open, single-throw miniature relay. It grounds the "EBA clear" line when a logic high is received. The clear line from the EBA must be plugged into J1 on the card's front panel for proper operation.

A fourth signal, which controls operation of the oscillograph, is received by the card. The "oscillograph operate" signal is routed to J4. A jumper is then required between J4 and J7. This permits the signal to control a normally-open, single-throw minature relay. It closes the remote operate line when a logic high is received. The remote operate lines and differential inputs are received via the back-plane connector (A6).

6.2.4 Breadboard Patch Panel Card

The Breadboard Patch Panel card serves two purposes. It is first used to route signals from the front panel to the back-plane wiring via connector A4. Signals used by the EBA which pass through this card include launch, test, AGC freeze, cage, cage coil, gyro reference, secondary reference, precession, guidance command, and signal ground. The card's schematic and layout are presented in Figure C-4 and C-10 respectively.

A second purpose of the card is to perform necessary scaling for two signals. The cage coil signal must be multiplied by a factor of two before it is presented to the EBA. This is required to prevent saturation of the cage coil signal in the EAI system. A two-stage amplifier, built with an LM747 (U7), performs the scaling. The input comes from J11 on the front panel and the output goes to the back-plane connector (A4), pin W.

The EBA's guidance command output is also scaled to insure against saturation in the EAI system. It is multiplied by a factor of .8 with a similar two-stage amplifier (U2). The input comes from connector A4, pin P, and the output is routed to J18.

6.2.5 Breadboard I/O Card

The Breadboard I/O card serves several purposes. Its schematic and layout are presented in Figure C-5 and Figure C-11 respectively. The card's primary purpose is to route all EBA/HISC interface signals through a connector on the card's front panel. A wiring list for the connector and its cable is presented in Table C-1 in Appendix C. Several signals are simply routed through the card from the back-plane connector (A3) to the front connector (P6). These signals on the back-plane are connected directly between the Breadboard I/O and Breadboard Patch Panel cards.

A scaling circuit is also implemented on the card. The EBA's precession output must be multiplied by a factor of .5 to prevent saturation in the EAI system. The two-stage amplifier is built with an LM747(U2). Its input comes from pin 3 of the front panel connector, and its output goes to pin 19 on A3.

Several logic functions are also performed on the card. A normally-open, single-throw minature relay (U5) and an AND gate (1/4 of U1) are used to perform the caging function. A logic high cage signal from A3, pin 20, causes the relay contacts to close. This routes the "buffered cage coil" signal back to the EBA via its "cage in" line. When the cage signal is "low," the line is left open. This action performs the caging function.

The timer start line is controlled by two miniature relays (U7 and U8) and two AND gates (1/2 of U1). With the current configuration, the "test" input from A3, pin 21, should always remain grounded. A logic high on the "launch" line (A3, pin 22) causes the contacts on the normally-closed, single-throw relay (U8) to open. Otherwise the timer start line is connected to ground through relay U7. This action performs the pre-launch/post-launch function.

For the present configuration, U6 and the remaining AND gate in U1 are not necessary. However, the "test" and "AGC freeze" lines from A3, pin 21, and A3, pin 7, should always remain "grounded".

6.2.6 Analog Out Card

The schematic and layout for the Analog Out card are presented in Figure C-6 and Figure C-12 respectively. In the current configuration, the card serves only one purpose. It routes the "precession" and "guidance command" signals from its front panel to the back-plane connector (A11). The signals have already been buffered by the scaling circuits. Four buffers are also available on the card to route signals to the EAI system if desired for diagnostic purposes.

6.2.7 Miscellaneous Hardware, Patching, and Cabling

Original design envisioned a multi-purpose simulation and anticipated changes throughout the development cycle. Subsequently, the modular design of the HISC occurred. The modular design requires that certain signals be "patched" between the modules via the front panels. This "patching" can be found in Table 13 in Section 8.2.

The power supply that supplies the HISC also provides +20V and -20V to the EBA. A "star" common is employed with the HISC, EBA, and their associated test and recording equipment. A single copper bar provides the common for all of this equipment. It is important to note that the common lines for the EBA are connected to the black connector for the positive supply and the red connector for the negative supply.

A sketch of the cabinet with the EBA, HISC, Power Supplies and oscillograph is presented in Figure 21. Interconnections associated with this equipment are detailed in Figure 13. The "clear" line, between J1 of the Discrete In module and the EBA, and the cable (1W6), between the Breadboard I/O module and the EBA, have already been noted in the above sections. Discrete In, Analog In, and Analog Out cables have also been referenced. The wiring list for the Discrete In cable is presented in Table C-2 in Appendix C. The Analog In and Analog Out cables are identical and are detailed in Table C-3.

Original simulation design included detector signal pre-amplifiers in the HISC. However, noise and AGC switching considerations prompted their movement to CCA#6 in the EBA. Subsequently, differential detector signals from the EAI system are "broken out" at the connector plate and routed to CCA#6. They are first routed to a cinch connector strip on the connector plate though. Coaxial cables are then used to route the signals to CCA#6. These interconnections can be seen in Figure 18 also.

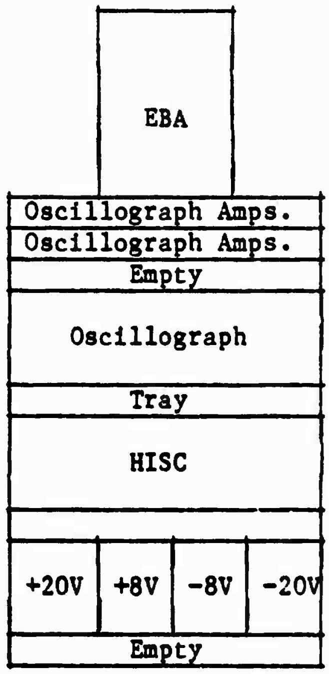

Figure 21 Physical Configuration of the Stinger POST Simulation Cabinet

6.3 Trunking Stations

Examination of Figure 17 reveals that all interconnections for the hybrid simulation facility are completed in the trunking stations. Each interconnection is called a "trunk". Listings for the trunks used by the Stinger POST hybrid simulation are detailed in Appendix D. Table 6 serves as a guide to locate specific trunk listings in Appendix D.

Table	Source	Destination
D-1	CDC 6600 DAC(1)	EAI-781
D-2	CDC 6600 DAC(2)	EAI-781
D-3	EAI-781	HISC
D-4	EAI-781	CDC 6600 ADC(1)
D-5	EAI-781	MVFG (0,1)
D-6	MVFG (0,1)	EAI-781
D-7	EAI-781	MVFG (6,7)
D-8	MVFG (6,7)	EAI-781
D-9	HISC	EAI-781
D-10	EAI-781 Logic	HISC
D-11	EAI-781 Logic	CDC 6600 In. Dis.
D-12	CDC 6600 Out. Dis.	EAI-781 Logic

Table 6 Guide to Trunk Listings in Appendix D

6.4 Common Blocks

Common blocks are used as an interface between the digital program and the hybrid simulation system. In Fortran programs, common blocks are used to conveniently transfer variables between subroutines containing the given common blocks. Variables are sent to the DACs and Output Discretes and received from the ADCs and Input Discretes via these common blocks. *ADC1, *IDIS2, *DAC1, and *ODIS2 communicate with the ADCs, Input Discretes, DACs and Output Discretes respectively. These blocks, with their variables, can be identified in the portion of the program listing presented in Figure 22. It is important to note that variables 1-16 of *DAC1 are used to supply DAC(1) while variables 17-32 are used to supply DAC(2). The JAM, ON command in the listing prompts the immediate transfer of the particular DAC variable as soon as it is calculated.

```
MAIN        74/74    OPT=1                              FTNH 4.2+81294

      PROGRAM MAIN(INPUT=65,OUTPUT=65,TAPE5=INPUT,TAPE6=OUTPUT,TAPE1=
     1 513,SYMBOL,HFILE)
      INTERRUPT(I=1,R=130,T=200,P=200)
      COMMON/*ALC1/1,CWIDATA,THEG,PSIG,PHII,SPHII,CPHII
      COMMON/*IDIS2/3,INDIS
      JAM,CN
      COMMON/*DAC1/2,YAWC,LRFO,WRKC,6,RPO,FPIO,BGDOTO
     1   ,ALPHAO,UFIC,DUPIO,VPO,WPO,RFICHO,RYAWO,SIGDYO
      COMMON/*JAC1/17,EPF10,SIGDZO,LYF10,RNGF10,
     1 23,FCLJO,PITCHO,CEO,EYTO,EPTO,LTRO,WTRO,TRPO,RANGEO,
     2   JPC
      COMMON/*OLIS2/3,OUTDIS
      JAM,CFF
```

Figure 22 Common Blocks Used for the Interface Between the Digital Program and the Simulation Hardware

7.0 DIAGNOSTIC CAPABILITIES

7.1 Introduction

The complexity of the Stinger POST hybrid simulation made it imperative that a number of diagnostic capabilities to be developed. Some capabilities are independent of the simulation while others are integral parts. Frequent failures of the EBA made it the first target for diagnostic aids. Section 7.2 describes trouble-shooting hints, techniques, tools, and procedures for the EBA. Section 7.3 reviews the diagnostic tools that have been built into the EAI-781 models. These tools aid one to conveniently test the analog models and much of the simulation hardware. The main closed-loop digital program has also been used to develop diagnostic open-loop and closed-loop programs. These are discussed in Section 7.4.

7.2 EBA Diagnostic Capabilities

Frequent failures of the EBA, due to both its design and the necessity to often probe for signals on CCAs, made it imperative to develop diagnostic techniques for the EBA. Section 7.2.1 describes test routines developed on the Tektronix 8002 microprocessor development system, and Section 7.2.2 describes the use of the HP-1615A logic analyzer as an anlaysis tool. However, some problems can be diagnosed through tailoring, by observation, or by trouble shooting with an oscilloscope. Some possible checks are listed in Table 7.

1. +15V (J6 - front panel), -15V (J8), and +10V (J78) Regulators
2. 5 MHz Clock (J77)
3. Activity on all data lines (J67-J74)
4. Gyro Reference (J10)
5. Digital 256 X Gyro Reference (J60)
6. Secondary Reference (J13)
7. Digital 256 X Secondary Reference (J62)
8. IR Predetect (J5) and/or UV Predetect (J20)
9. IR Preamp (TP7 - CCA#6) and/or UV Preamp (TP5 - CCA#6)
10. CFAR Indicate (J56)
11. Relative position of Predetect between CFAR's for on-axis target
12. Digital 1024 X Cage Coil (J64)
13. Cage state (front panel LED), and Launch state (J61)
14. User generated Cage Coil (J32), and subsequent look angle logic (front panel LED)
15. Precession for off-axis target (J31)
16. Proper AGC action (AGC word-front panel)
17. Valid (Table 8) CCA#4 word (front panel display)
18. Valid (Table 9) CCA#5 word (front panel display)
19. Relative position of IR Predetect (J5) and LT CMD (TP8-CCA#4)
20. Relative position of LT CMD and TE (TP7 -CCA#4)

Table 7 20 Simple EBA Operation Checks

Word	Status
91	Caged
90	91: Target Not in FOV
11	Pre-Launch
10	11: Target Not in FOV
51	Post-Launch
50	51: Target Not in FOV
41	51: $\dot{\sigma}$ Blanking
40	41: Target Not in FOV

Table 8 Valid CCC#4 Words

Word	Status
00	No Acquisition
01	00: Type 1 Forced
80	Flare Mode
81	80: Type 1 Forced
C0	IR Acquisition
C1	C0: Type 1 Forced
E0	UV Acquisition
E1	E0: Type 1 Forced

Table 9 Valid CCC#5 Words

7.2.1 Tektronix 8002a Test Programs for the EBA

A microprocessor (μP) development system has been used to develop and execute several programs to insure proper operation of the EBA and to diagnose problems that may occur in the EBA. The programs were written and debugged using a Tektronix 8002a system with full RCA 1802 microprocessor emulation capabilities. They are executed using the 8002a in its iteractive emulation mode (EM 1) with the prototype control probe (PCP) connected to the appropriate CCA in the EBA. The CCA's μP is replaced by the PCP. In this mode, 1802 input/output (I/O) commands are routed from/to the EBA via the PCP. This permits memory to be shared between the EBA memory and the 8002a program memory in 128_{10} byte blocks. For execution, most of the programs require parameters to be passed to the program. To accomodate this need, memory locations $FFF0_{16}$-$FFFF_{16}$ have been reserved for control parameters which may be defined using the 8002a PATCH or EXAM commands as described in the 8002a System Reference Manual [7]. However, through the use of command files, the user interface has been reduced to a minimum, and only a few system level inputs are required. The theory and instructions for use of each diagnostic program are described in the following sections. Appendix E contains all diagnostic software flowcharts, command file listings, and program listings.

7.2.1.1 Transfer of EBA PROM Memory to 8002a Memory

This program transfers memory, byte-by-byte, from PROMs located on CCA #5 to the 8002a system's program memory. The program also fetches each PROM memory byte a second time and compares it to the first byte in RAM. Any differences cause a termination; otherwise, the program continues until the last address of PROM has been transferred. The program assumes that the PROM starting location is 0000_{16}. The last PROM address to be transferred and the starting address of 8002a RAM to be used for storage are passed as control parameters.

To simplify use of the program, a chain (command) file has been written to pass the control parameters and execute the program. The sequence for using the program follows with user entries underscored.

SYSTEM CONFIGURATION
Drive 0: 1802 v3.3 system files
Drive 1: INS1TX, INS2TX, XFERMF;0 files
PCP: CCA#5 μP

INSTRUCTIONS
INS1TX/1
INS2TX/1 (last EBA PROM address) (first 8002a RAM address)
ex: INS2TX/1 07FF E000

PROGRAM OUTPUTS

1. "AA" will be displayed on the front panel "W5 WRITE" display if the transfer was successful (may be "xA" in some cases).
2. "EE" will be displayed on the "W5 WRITE" display if an error was discovered in the transfer (also may be "xE").
3. The "Q" line (front panel, pin 57) will be a logic high if the transfer was successful.
4. The "Q" line will oscillate at about a 50% duty cycle if an error was discovered in the transfer.

7.2.1.2 Verification of EBA PROM Memory Against 8002a Diskette File

This program verifies the contents of EBA PROM memory on CCA #5 against a previously saved diskette file. Such a file can be developed using the program documented in the previous section. The program assumes the PROM memory starts at 0000_{16}. The first address of 8002a RAM to be used to store the file and the name of the file are passed as control parameters. The program does a byte-by-byte comparison of the file (as loaded in RAM) to PROM memory. It exits if there are any differences or continues until all locations have been checked.

Again, a command file has been written to pass the control parameters and execute the program. The operation sequence follows with user entries underscored.

SYSTEM CONFIGURATION
Drive 0: 1802 v3.3 system files, (file for verification)
Drive 1: INS1VF, INS2VF, VFILE;0 files
PCP: CCA #5 μP

INSTRUCTIONS
INS1VF/1
INS2VF/1 (verification file) (last EBA PROM address) (first 8002a RAM address)

PROGRAM OUTPUTS

1. "AA" will be displayed on "W5 WRITE" display if verification was successful.
2. "EE" will be displayed on "W5 WRITE" display if an error was found.
3. The "Q" line (front panel, pin 57) will be logic high if verification was successful.
4. The "Q" line will oscillate at about a 50% duty cycle if an error was discovered.

7.2.1.3 EBA Synthesized Error Signal DACs Tests

This program outputs either a fixed value or a sinusoidal wave at a user specified frequency to either the Ex, Ey, or both $\dot{\sigma}$ error DAC channels. The program may be used to check the DAC operation, type I/II filter operation, and synthesized error amplifier performance. For the sinusoidal wave portion of the program, the sine table used for error calculations on CCA #4 is used in order to better simulate actual error output.

The sequence for using the program follows. Again, user entries are underscored, and a chain file has been written to pass the control parameters and execute the program.

SYSTEM CONFIGURATION
Drive 0: 1802 v3.3 system files
Drive 1: INS1ER, INS2ER, EROUTA;0 files
PCP: CCA#4 μP

INSTRUCTIONS
INS1ER/1
INS2ER/1 (type: I=00, II=FF) (frequency: Hex) (channel: X and Y = 0, X = 1, Y = 2) (output: fixed = 0, sine = 1) (fixed level: Hex)

PROGRAM OUTPUTS
1. The "Q" line ('FOV VALID' test point on CCA #4) will oscillate at a 50% duty cycle if a parameter error was detected.

7.2.1.4 Automatic Gain Control (AGC) Tests

This program tests the IR and UV Automatic Gain Control (AGC) circuitry on CCA#6. The program outputs a user selected bit pattern to the flip-flops and analog switches which control the IR and UV AGC action on CCA #6 via CCA#5. The bit pattern is toggled with 00_{16} so that individual bits in the flip-flops and gain steps can be checked for correct operation. The rate at which the bits are toggled is user defined also.

Again, a chain file has been written to pass the output byte and the delay factor to the program. The sequence for using the program follows with user entries underscored.

SYSTEM CONFIGURATION
    Drive 0: 1802 v3.3 system files
    Drive 1: INS1AGC, INS2AGC, AGCOUT;0 files
    PCP: CCA#5 μP

INSTRUCTIONS
    INS1AGC/1
    INS2AGC/1 (output byte: Hex) (delay factor: Hex)

PROGRAM OUTPUTS
1. The byte is written to the "W5 WRITE" display as it is being written to CCA #6.
2. The "Q" line (front panel, pin 57) will toggle at the same rate as the output byte.

7.2.1.5 EBA RAM Memory Tests

This program tests RAM memory located on CCA#4 or CCA#5. The program writes a series of bit patterns (00_{16}, 55_{16}, AA_{16}, FF_{16}) to RAM, reads the location, and compares the result to the pattern written. If the bytes are the same, the next location is tested. If a bad location is found, the program halts. The bad location and the bit pattern which failed to test properly may be examined by the user.

Again, a chain file has been written to load and execute the program. The sequence for running the program follows with user entries underscored.

SYSTEM CONFIGURATION
    Drive 0: 1802 v3.3 system files
    Drive 1: INS1MT,METS;0 files
    PCP: CCA#4 μP or CCA#5 μP

INSTRUCTIONS
    INS1MT/1

PROGRAM OUTPUTS
1. The "Q" line ("FOV VALID" test point for CCA#4 - pin 57, front panel for CCA#5) on the respective CCA will be logic high if the test was a success.
2. The "Q" line will oscillate at a 50% duty cycle if the test failed.
3. For CCA#5, the "W5 WRITE" display will display either an "FF," "AA," "55," or "00" if that pattern failed to test properly.

7.2.2 HP-1615A Logic Analyzer Test Techniques

Realisticly, the HP-1615A is probably the most important tool required for EBA maintenance. It can record and store 256 words with a maximum total of 24 bits each. It records a word with each clock signal received. Additionally, six qualifier inputs can be received to qualify the clock signal. An important concept to remember is that the qualifying bits must reach their chosen steady-state status before the clock input is received. Here it may be important to choose whether to clock on the clock signal's positive or negative transition.

For use of the HP-1615A with the EBA and its RCA-1802 microprocessors, it is mandatory that the timing diagram (Figure 23) of the 1802 [8] is thoroughly understood. Again, the most important task is to find a signal that can be used to clock the 1615A. Examination of Figure 23 reveals that all 1802 signals are in a steady state condition during the low-to-high transition of the TPB signal. Subsequently it is generally advisable to use TPB as a clock signal when working with the 1615A. Other signals can then be used as "qualifiers" for the clock when defining the conditions required for the collection of data.

The "menu" type operation of the 1615A makes it relatively easy to use. Two principal areas must be defined by the user after the probes have been attached to a circuit. First, the conditions of the trace must be defined. This includes the clock, qualifier, and trigger considerations discussed above. Second, the format of the output must be specified. The 1615A allows the user to observe the collected data in a large number of formats. The data can also be written to a printer (HP-IB required).

The 1615A is particularly useful with three of the CCA's. CCA#4 contains a μP. Subsequently, it is often desirable to observe its program during execution. After attaching the probes to the data and address lines, and clocking on TPB, each cycle of the 1802 can be observed. Specific words can be chosen as a trigger to begin a trace. This permits one to begin looking at specific chosen points in the program. Data which is read/written from/to a particular I/O device (CDP 1852) or DAC (AD7524) can be isolated also. While still looking at the data lines, the clock signal can be "qualified" with the chip select signals for that device. The 1615A is also useful for looking at the counters in the phase-lock-loops (MC14520) on CCA#4.

CCA#5 also contains a μP. Again, it is often desirable to observe its program during execution and data read/written from/to particular I/O devices. Additionally, the 1615A is very useful for looking at the thresholds on CCA#5 during EBA operation.

CCA#6 does not have a μP, but its AGC action is controlled by the one on CCA#5. Checking operation of the latches (MC14175) and analog switches (DG 201) used to perform AGC action is greatly simplified by use of the 1615A.

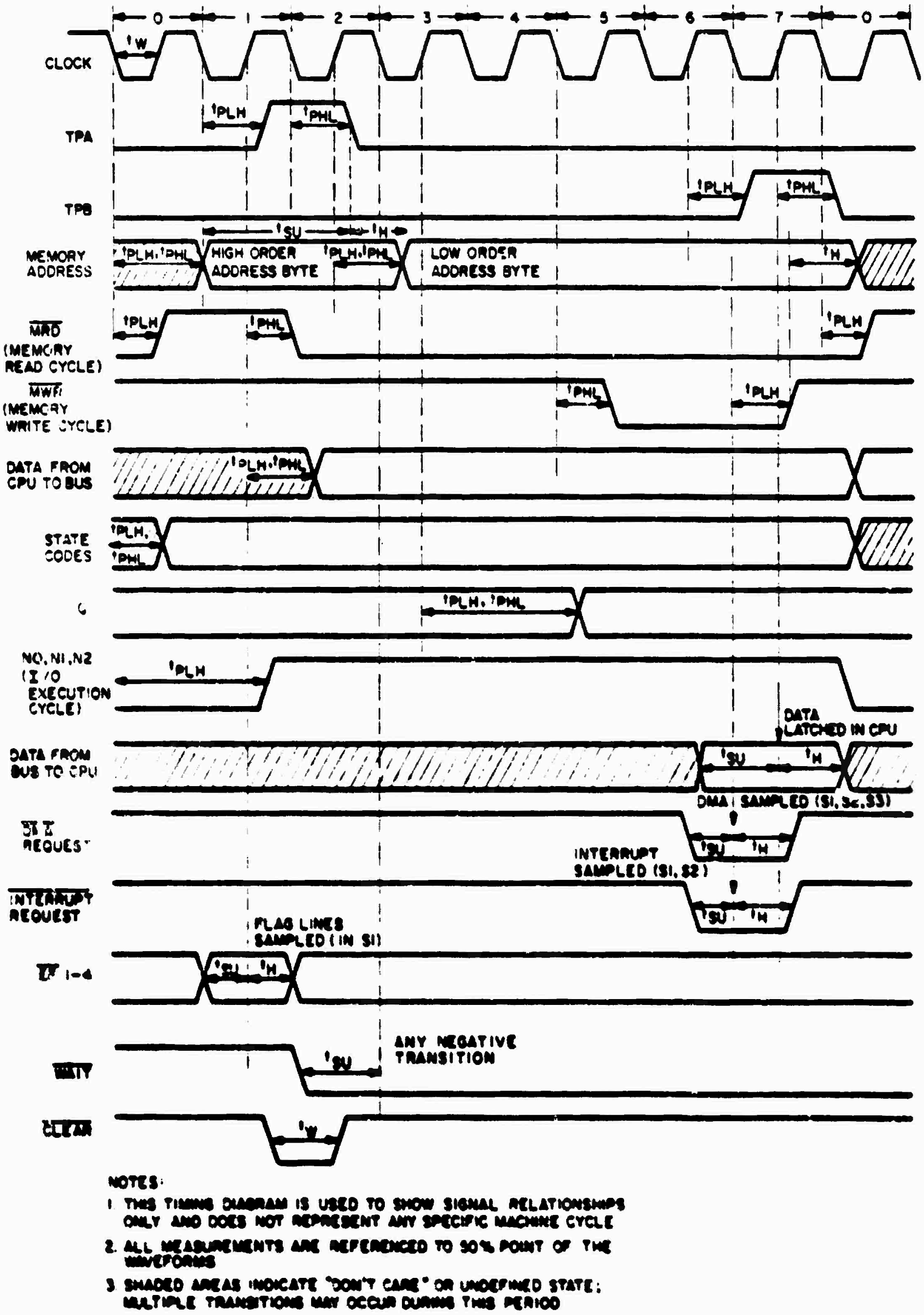

Figure 23 RCA 1802 Timing Diagram

7.3 Analog Control Panel Diagnostic Functions

Much of the simulation hardware can be tested with the aid of diagnostic tools built into the analog models on the EAI-781. Some of the tools are used to allow the user to control certain model parameters independent from simulation control. Some are instrumental in tailoring.

A number of the capabilities were discussed in Section 2.0 (Control Logic) and are illustrated in Figure A-1 in Appendix A. FF220 forces the EBA into the "uncaged" states and FF041 forces the "launched" state. PB002 enables operation of the oscillograph. And, PB003 forces the wing servo model into operation.

Specific functions will be discussed in Sections 7.3.1 - 7.3.8. Tables 10 - 12 provide a summary of flip-flops, push-buttons, and hand-set potentiometers that make up most of the analog control panel diagnostic functions.

Flip-Flop #	Description
000	Enable Analog and Recorders
001	-
010	Force Rate Gyro Operate
011	(Static Test)
020	(Part of Wing Servo)
021	(Part of Wing Servo)
030	-
031	-
040	Force Handset Roll Rate (HS104)
041	Force Launch
050	-
051	Force Roll Resolver Operate
200	Abort Real-Time
201	Activate Static Gain Integrators
210	-
211	-
220	Force Uncage
221	Force Zero Roll
230	Force Handset Flare Positioning (HS105, HS114)
231	Force Flare #1 Operation
240	-
241	-
250	Force Normalized Flare Intensity History
251	Force Handset Target Intensity (HS145)
400	Enable Rosette
401	Select UV Display
410	-
411	Disable Flare #1 Ignition
420	-
421	-
430	Force Handset Triangle Sizing (HS115, HS125)
431	Force Handset Rectangle Sizing (HS115, HS125)
440	Force Handset Circle Sizing (HS144)
441	Disable Triangle Gradient
450	Force Handset Target Positioning (HS134, HS135)
451	Display Synchronization

Table 10 Analog Control Panel Flip-Flop Assignments

PB#	Description
000	-
001	Open Tracker Loop
002	Enable Oscillograph
003	Force Wing Servo Operate

Table 11 Analog Control Panel Push-Button Assignments

Handset Pot #	Description
104	Roll Rate
105	Flare Position-Azimuth (FF230)
114	Flare Position-Elevation (FF230)
115	Target Width (FF431)
124	-
125	Target Length (FF431)
134	Target Position - Azimuth (FF450)
135	Target Position - Elevation (FF450)
144	Circle Size (FF#440)
145	Target Intensity (FF#251)
154	-
155	-

Table 12 Analog Control Panel Handset Potentiometer Assignments

7.3.1 Roll Control

Roll rate can be placed under user control as shown in Figure A-3. The roll resolver (R510) can be forced into operation by setting FF051. FF221 and K241 combine to insure zero roll when FF221 is set. And, FF040 and K041 combine to permit the user to define a constant roll rate when FF040 is set. HS104 can then be used to define that rate.

7.3.2 Gyroscope

The gyroscope model (Figures A-5 and A-6) can be forced into operation by setting FF010. I010 (θg) and I022 (Ψg) can be independently placed into initial condition, though, by setting PB001. Constant, open-loop look angles can then be defined by placing values on C012 (θg) and C102 (Ψg). These functions are important in tailoring and can be used to develop specific cage coil signals.

7.3.3 Target Position

Constant target positions within the rosette pattern can be defined by the user via FF450, K050, K051, HS134, and HS135 (illustrated in Figure A-7). When FF450 is set, positioning control is switched from the trunk inputs to the hand-set potentiometers. HS134 can be used to position the target in azimuth, and HS135 can be used to position it in elevation.

7.3.4 Circle Size and Intensity

Circle parameters of size and intensity can be defined by the user (illustrated in Figure A-9). When FF440 is set, HS144 controls circle size via K251. When FF251 is set, HS145 defines a constant intensity in both the IR and UV channels via K010 and K401 respectively.

7.3.5 Triangle and Rectangle Size and Intensity

Triangle and rectangle size can be defined by the user (illustrated in Figure A-9). When FF430 is set, HS125 controls the length of the triangle and HS115 controls its width. When FF431 is set, HS125 and HS115 also respectively control the length and width of the rectangle.

Triangle intensity (illustrated in Figure A-10) can be defined to include its gradient and be a function of range and aspect angle, to be uniform and a function of range and aspect angle, or to be a constant value. Setting FF441 forces a constant value via K250. Otherwise, the entire intensity model remains in effect. The gradient model can be disabled by setting C501=C502=0.0 and C503 equal to some value. The value of C503 then determines the level of the uniform intensity.

Rectangle intensities (illustrated in Figure A-13) can also be controlled by the user. Setting FF251 enables the user to set constant intensity values with HS145 via K011 in the IR channel and K250 in the UV channel.

7.3.6 Flare Position, Size and Intensity

Constant flare positions (illustrated in Figure A-11) within the rosette pattern can also be defined by the user. When FF230 is set, positioning control is switched from the trunk inputs to HS105 and HS114. HS105 can used to position the flare in azimuth via K030, and HS114 can be used to position it in elevation via K031.

Since flare size remains constant during a simulated flight, its size is already user definable. C553 defines this simulation variable.

FF231 can be used to independently force the flare into operation. And, FF411 can be used to disable ignition of the flare intensity profile by the digital program. When FF250 is set, the normalized intensity profile is multiplied (via K000) by a constant, instead of the range dependent function.

7.3.7 X-Y Display

The intensity input to the X-Y Display is driven by either the composite IR signal or the composite UV signal (illustrated in Figure A-13). The result is a visual representation of the individual spectral composite target within the rosette pattern. While FF401 is left unset, the IR source is displayed. The UV source is displayed via K040 when FF401 is set. A bias for the display can be set with the aid of C302 and A101. The relative target-to-rosette intensity can be controlled by the value set on C302.

7.3.8 Static Gain Curves

Static Gain Curves are used to characterize the EBA's response to a particular target. With the simulation, they represent a graphical record of a target model's validity. Subsequently, a more detailed static gain curve discussion will be presented in the next report in this series of tasks (Simulation Validation). However, a brief explanation of the method used to generate static gain curves will be presented here.

After forcing the gyroscope into operation (FF010), "opening the tracker loop" (PB001), and defining a zero look angle (C012=C102=0.0), static gain curves can be generated with the use of FF201, K200, I210, K201, and I220 (illustrated in Figure A-4). Additionally, the EBA must be uncaged (FF220). Then, using the techniques described in sections 7.3.4 - 7.3.6, the target model to be characterized must be defined by the user.

The actual curves are generated by plotting the output of either I210 or I220 against the target's position within the rosette pattern in either elevation (HS135) or azimuth (HS134) respectively. While FF201 is left unset, I210's output represents θg and I220's output represents ψg. When FF201 is set and C203 and C221 are set to 1.0, the outputs of I210 and I220 are filtered representations of $\dot{\theta} g$ and $\dot{\psi} g$ respectively. It is important to remember that these outputs are a direct measure of the EBA's precession signal in response to the particular target.

7.4 Digital Display System (DDS) Diagnostic Routines

Two digital diagnostic programs, which can be executed from a Digital Display System (DDS) terminal, are available to the simulation user. With these programs, OLOOP1 CYCLE 2 and OLOOP1 CYCLE 3, it is possible to exercise the simulation under a variety of known conditions. This permits one to evaluate the "health" of the simulation or assists one in the diagnosis and repair of occasional simulation failures. Both programs are "user friendly" and require a minimum number of inputs from the operator. When each of the programs is either initialized or halted, the operator is presented with a "menu" of options. However, it is important to insure that the Initialization and Tailoring Sequences outlined in Section 8.0 have been performed before attempting to use these programs.

The first program, OLOOP1 CYCLE 2, is designed to model a simple, nonmaneuvering, closed-loop flight. Its flowchart is presented in Figure F-1 in Appendix F. Both tracking and guidance loops are closed with this program. The operator can specify the initial conditions (missile and target) and target characteristics. Initial conditions include range to target, missile body angle, missile body rate, and target azimuth. Target characteristics include rate, crossing angle, body dimensions, plume dimensions and flare drop rate. A detailed operation sequence is presented in Appendix F.

OLOOP1 CYCLE 3 differs from the first program in that it only closes the loop around the tracker. Its flow chart is presented in Figure F-2. A standard, circular (point source) target should be used for all tests with this program. Options 0 through 5 enable evaluation of the simulation's ability to acquire a target with or without an initial pointing error. Options 6 through 11 are used to check track rate performance. And, options 12 through 15 are used to evaluate the effects of range closure and accelerations.

With this program, as soon as an option is chosen, Real-Time execution begins. New options can then be chosen and implemented during program execution. This permits the evaluation of a variety of steady-state and transient conditions.

8.0 SIMULATION USAGE SEQUENCES

8.1 Introduction

Use of the Stinger POST hybrid simulation can be divided into three stages. The first is the initialization stage. A sequence for initialization is presented in Section 8.2. Tailoring is the second stage of usage. Tailoring must be checked and/or adjusted to insure proper operation of the simulation. The operation sequence for tailoring is presented in Section 8.3. Actual operation of the simulation is the third stage of usage and should only be attempted after the initialization and tailoring sequences have been completed. The operation sequence is presented in Section 8.4.

8.2 Initialization Sequence

I. Check with Analog Computer Room personnel to insure that the following activities have been completed.

   A. Mount the proper analog and logic boards on the EAI-781.
   B. Connect the proper trunk lines.
   C. Successfully complete a static check of the system.

II. Initialize the Display System to display the composite rosette/target representation.

   A. Set the following push-buttons (in order)
      1. Trace Selector: I
      2. Input: 20
      3. Trace Selector: II
      4. Input: 21
      5. Cross Plot: I
   B. Adjust the intensity setting on the display to the desired level.

III. Initialize the EBA, HISC, and oscilloscope.

   A. Check to insure that the EBA and HISC power switches are off.
   B. Turn on all four power supply switches (located at the bottom of the simulation hardware cabinet), and check to insure that the two variable supplies are set to 8 volts.
   C. Verify that the HISC is patched as outlined in Table 13.
   D. Turn on the HISC (located directly above the power supplies).
   E. Turn on the EBA (located on top of the cabinet) and check to insure that neither ammeter exceeds 1 Amp.
   F. Set the EBA switches as indicated in Table 14.
   G. Turn on the Tektronix oscilloscope.
   H. Connect X10 probes to "CH 2" of each of the oscilloscope's amplifier modules.
   I. Set the DISPLAY MODE and TRIGGER SOURCE switches of each module to "CH 2".

J. Set the GAIN of both amplifiers to 5V/DIV and select "DC" coupling.
K. Turn the time base adjustment fully counter-clockwise and select "AUTO" MODE, "DC" COUPLING, and "INT" SOURCE.
L. Set the oscilloscope VERT MODE to "RIGHT," the TRIGGER SOURCE to "LEFT," and choose "NON STORE" trace.
M. Connect the left "CH 2" probe to Ex (TP1 on EBA CCA#4) and the right "CH 2" probe to E_y (TP4 on CCA#4).

IV. Initialize the EAI-781 control console.

A. Check to insure that PWR and PP push-buttons are "on".
B. Set the following push-buttons:
   1. Select System: DVM and ADR
   2. Clock: 10^6
   3. Analog Time Scale: M and SEC
   4. Analog Mode: IC
   5. Logic Mode: R
   6. Slave: MSL and HYB
C. Set FF 400.
D. Poll FF 451 "on" and "off" until rosette pattern appears on X-Y display (0-5 pollings may be required).

V. Check (via the PACER 100 Control Console) to insure that simulation trucks are connected as indicated in Table 15.

From		To		
Module	Pin No.	Module	Pin No.	Signal[1]
Discrete In A	2	B.B.P.P. *	4	Cage Command
Discrete In A	3	B.B.P.P.	1	Launch Command
Discrete In A	4	Discrete In A	7	Oscillograph Control
Analog In	Cage	B.B.P.P.	11	Cage Coil
Analog In	Gyro	B.B.P.P.	12	Gyro Reference
Analog In	Sec	B.B.P.P.	13	Secondary Reference
B.B.P.P.	18	Analog Out	2	Wing Command
B.B.P.P.	15	Analog Out	3	Precession
HISC Power	PWR/GND	B.B.P.P.	2	Test Command
HSIC Power	PWR/GND	B.B.P.P.	3	AGC Freeze Command
HISC Power	PWR/GND	Analog Out	SIG GND	Differential Gnd
HISC Power	PWR/GND	Analog Out	5	Empty
HISC Power	PWR/GND	Analog Out	6	Empty
HISC Power	PWR/GND	Analog Out	7	Empty

* Breadboard Patch Panel.

Table 13
HISC Patching Instructions for Stinger/POST Configuration

Title	Position
Power	ON
Cage/Uncage	UNCG
LAUNCH	POST
FOV	ENBL
AGC	ENBL
Type Track	Normal

Table 14
EBA Switch Settings For Initialization

ADDRESS	DESTINATION
W10	V3B
W11	V36
W00	V3A
U90	V83
V30	V24
V31	V25
V33	V26
V34	V27
V81	W52
V80	W62
V38	W43
V39	V43

Table 15
Analog Room Trunks For Stinger POST Simulation Configuration

VI. Initialize an IR Point Source (Circle) target.
   A. Set FF251 and F440.
   B. Adjust HS 145 to a fully clockwise position.
   C. Set C250 to .1000
   D. Set C251, C301, C252, C032, C453, C300, C342, and C253 to 0.0000.
   E. Adjust HS144 (circle size) to yield an output which represents a point source.

8.3 Tailoring Sequence

I. Check to insure that the initialization sequence has been performed correctly.

II. Tailor Scan Phase.
   A. Set FF220, FF221, FF041, FF010 and PB001.
   B. Set C012 and C102 to 0.0000.
   C. Adjust the left DIP switch atop CCA#4 to a setting (approximately $C2_{16}$ - MSB at bottom) which yields the smallest pattern of "dots" on the oscilloscope.
   D. Perform corrective maintenance if the resulting DIP setting varies over 2 or 3 bits from its previous setting.

III. Tailor Track Phase.
   A. Check to insure that scan phase tailoring has been performed.
   B. Set FF450.
   C. Initialize strip chart recorder #2 (right side).
      1. Zero channels 1 and 2 in the center of their respective scales.
      2. Set channel 1 and 2 scales to 2.0V/line.
      3. Set "STOP," "LC," and "X.01" on speed control.
   D. Adjust HS134 to +0.2500 and HS135 to 0.0000, and check to insure that the circle on the X-Y display is to the right.
   E. Set strip chart speed to "200" for approximately 4 seconds and then "STOP."
   F. Adjust HS134 to -0.2500, and check to insure that the circle is to the left.
   G. Repeat Step E.
   H. Adjust HS134 to 0.0000 and HS 135 to -0.2500, and check to insure that the circle is to the bottom.
   I. Repeat Step E.
   J. Adjust HS135 to +0.2500, and check to insure that the circle is to the top.
   K. Repeat Step E.
   L. Compare the strip chart trace to Figure 24.
   M. If a strip chart offset occurs in one plane while the circle location is adjusted in the other plane (Figure 25) adjust the right DIP switch atop CCA#4 (approximately EA_{16} - MSB at bottom).
   N. Repeat Steps D-M until the strip chart trace matches figure 24.
   O. Perform corrective maintenance if the resulting DIP setting varies over 3 or 4 bits from its previous setting.
   P. Unset FF450.

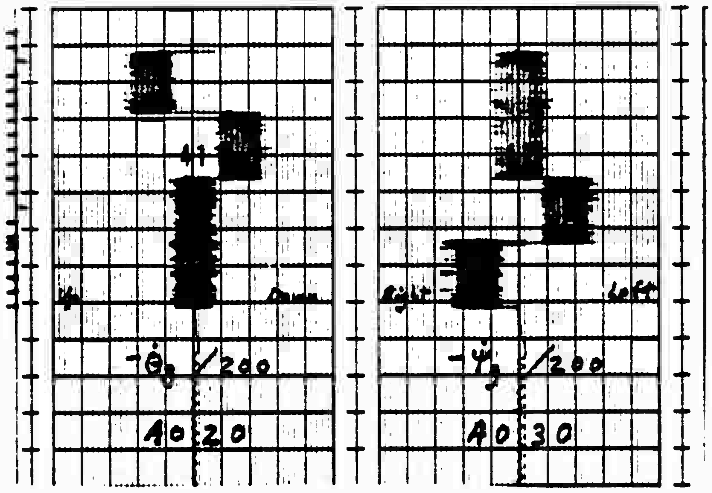

Figure 24 Strip Chart Trace of $-\dot{\theta}g$ and $\dot{\Psi}g$ With Correct Phase Tailoring.

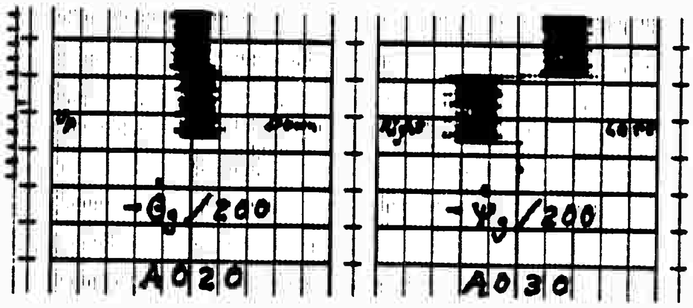

Figure 25 Strip Chart Trace of $-\dot{\theta}g$ and $\dot{\Psi}g$ With Phase Tailoring Out By One Bit.

IV. Check the Guidance Circuitry.

- A. Set C012 to +0.3000.
- B. Unset FF221.
- C. Set FF040, FF051, and PB003.
- D. Set HS104 to a value equal to -.0180 x (roll rate in Hertz).
- E. Monitor J26 on the EBA with the oscilloscope.
- F. Perform corrective maintenance if a roll rate signal is not present at J26.
- G. Check Wing Servo operation by observing A440 with an oscilloscope at the EAI-781.
- H. Set C012 to 0.0000.
- I. Unset FF040, FF051, FF220, FF221, FF041, FF010, PB001, and PB003.

V. Tailor Signal-to-Noise Ratio (SNR)

A. Set C250 and C253 to 0.0000.

B. Set the EBA AGC word switch to IR AGC.

C. Check to insure that the EBA AGC word display reads approximately FF.

D. Set C301 to a value which generates the required amount of IR noise as indicated by the AGC word. Note that the output is scaled to .44 db/step as indicated by Figure 26.

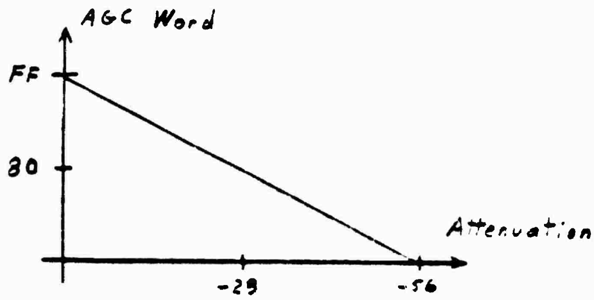

Figure 26 AGC Word Scaling

E. Using the OLOOP1 CYCLE3 program (described in Section 7.4), set the target in the center of the FOV at a range equal to the launch range of the flight to be modeled. An operations sequence for this procedure is presented in Appendix F.

F. Set C250 to a value which generates the required amount of IR signal as indicated by the AGC word.

G. Set the EBA AGC word switch to UV AGC.

H. Check to insure that the display reads approximately FF.

I. Set C300 to a value which generates the required amount of UV noise.

J. Set C253 to a value which generates the required amount of UV signal.

VI. Tailor System Guidance Phase.

A. Using OLOOP1 CYCLE3, begin tracking a target, and continuously move the target back and forth in azimuth.

B. Using an oscilloscope at the EAI 781, compare the phase of R510 ($-\sin \dot{\rho}$ t) and TR501 (δc) while the target is moving to the left.

C. If a phase difference occurs, set C230 and C231 subject to Equation 42 and Equation 43 respectively.

$$C230 = \sin \phi/5 \qquad (42)$$

$$C231 = \cos \phi/5 \qquad (43)$$

where: ϕ = system phase compensation (degrees).

If the resulting value of ϕ differs more than 10 degrees from 212°, perform corrective maintenance on the system.

D. Check Scan and Track Phase tailoring.

E. Repeat Steps C and D if phase words required a change.

F. Check phasing for target motion in other directions as indicated in Table 16.

Direction Target Motionon	Signal In Phase With δ c	
Right	SIN ρ	(A430)
Left	- SIN ρ	(R510)
Up	COS ρ	(A431)
Down	- COS ρ	(R513)

Table 16 Target Motion and System Phasing Relationships

8.4 Operation Sequence

I. Call Computer Control to bring the DDS terminal "on line".

II. Enter user ID, Password, etc., on DDS terminal.

III. Access file space and make ready digital portion of hybrid simulation.

  A. Modify digital routines as required.

  B. Recompile.

  C. Save in permanent space new modifications.

IV. Check to determine if initialization and tailoring sequences have been completed.

V. Verify that adequate resources are available (core space, trunks, etc.) and status schedule those resources needed for run(s).

VI. Begin the hybrid simulation operation by executing DIRSS.

VII. ENTER GO TO START will appear on screen.

VIII. Insure that recorders are scaled correctly and in "remote" mode.

IX. Type "GO" and press the SEND key. A delay will be experienced as pre-run calculations are performed.

X. READY FOR REAL TIME will appear on the screen. At this point, any parameter desired to be monitored on the DDS terminal can be entered. After these are entered, type "GO" and press SEND key.

XI. If adequate resources are not available, program will delay and recycle to point where READY FOR REAL TIME will once again appear on screen. If this occurs, repeat starting at Step X.

XII. If all was ready, the simulation proceeds under EXECUTIVE control of the real time operating system and follows the logical sequence of events simulating missile flight.

XIII. Following end (either normal or aborted) of simulated flight, END OF REAL TIME appears on screen. Enter "GO" to print/plot resulting data.

9.0 CONCLUSIONS AND RECOMMENDATIONS

The Stinger POST simulation has reached a usable level of development. Diagnostic capabilities and configuration enhancements have yielded a good degree of reliability. Validation has been completed for a couple of test flights and will be presented in the next final report in this series of tasks, which will be completed soon.

There are still several minor tasks that could be completed to improve the reliability and testability of the simulation. Some of the tasks are related to the need to remove excess items left in the simulation during the development process. Review of the control logic would find several circuits that could be simplified. And, the HISC could be simplified to just four circuit cards. Extra lines in the HISC cables could be used to transfer several more diagnostic signals between the EBA and the EAI-781. Additionally, extra components in two extra flare models could be used to develop more diagnostic capabilities at the EAI-781. Alternately though, they could easily be incorporated into the simulation if the need for extra flares arises.

An important diagnostic improvement recommendation is for development of a system of function relays and flip-flops to send chosen (by flip-flop) signals to the EAI-781 system oscilloscope. Including δ_c and sinϕ or cosϕ in such a system would greatly simplify checking system phasing.

A minor change should be made to the simulation to improve validity. The square flare models should be changed to circles. Extra components from the extra flare models could be used for this purpose.

Aside from these recommendations, little needs to be done to improve the usability of the simulation. However, additional validation needs to be completed for the simulation. The extent of additional validation needed is subject to discussion though. Regardless, the Stinger POST hybrid simulation has been developed into a reliable, high fidelity simulation.

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APPENDIX A
EAI-781 Model Schematics

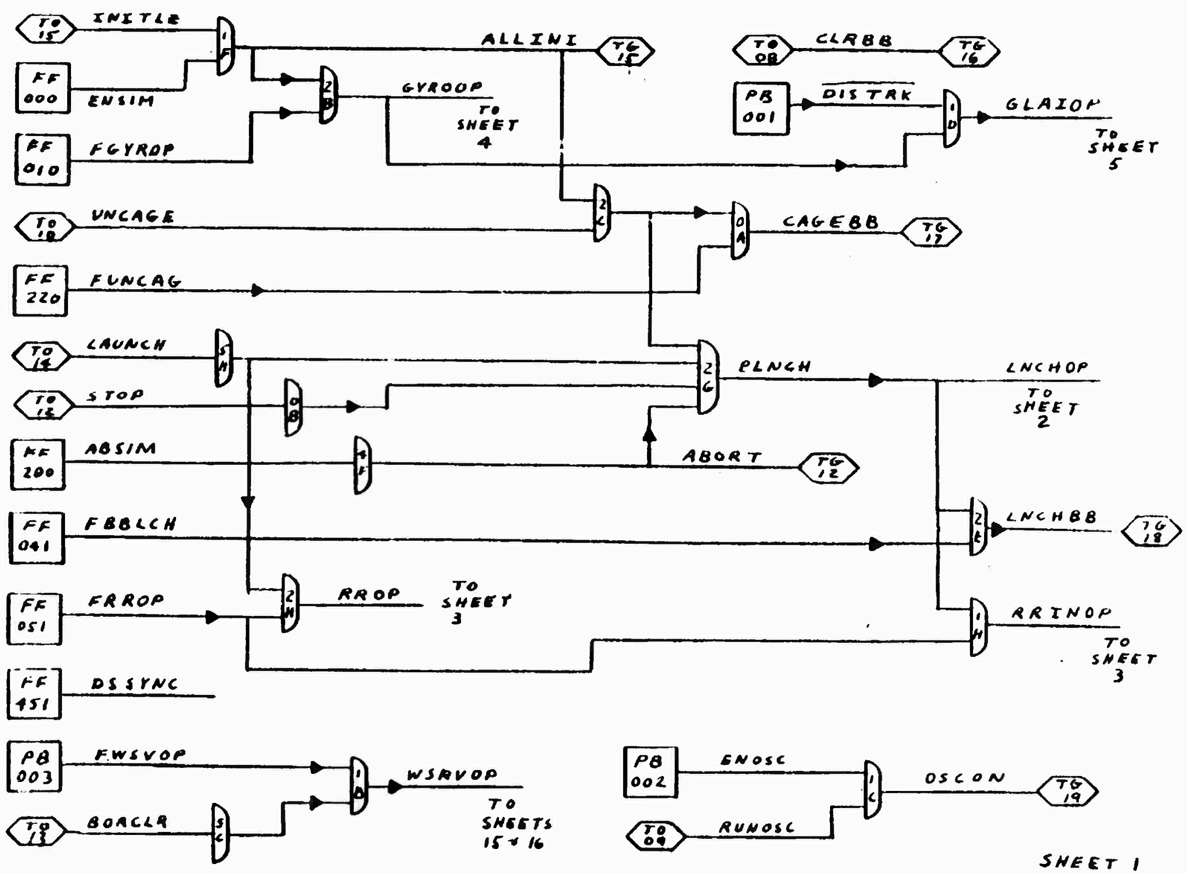
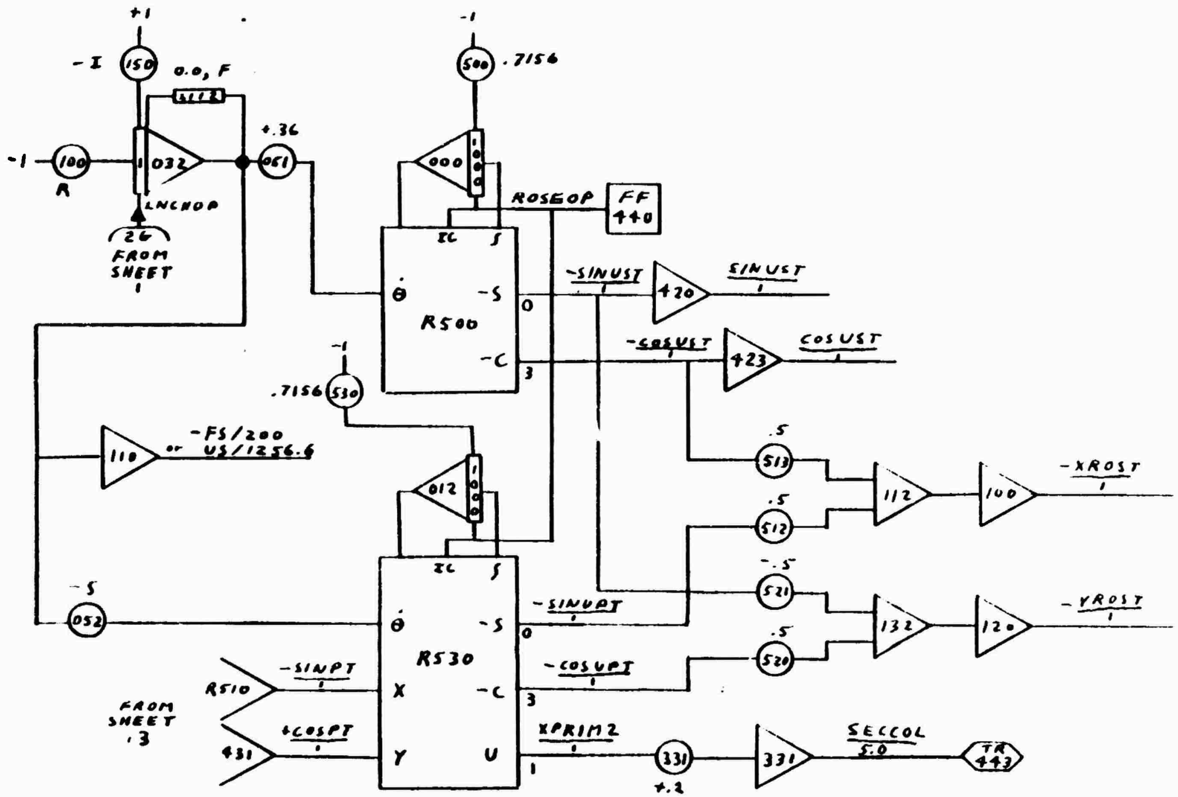


Figure A-1 Simulation Control Logic



SHEET 2

F'gure A-2 Primary Gyro Motor, Secondary Gyro Motor, Rosette, and Secondary Reference Coil

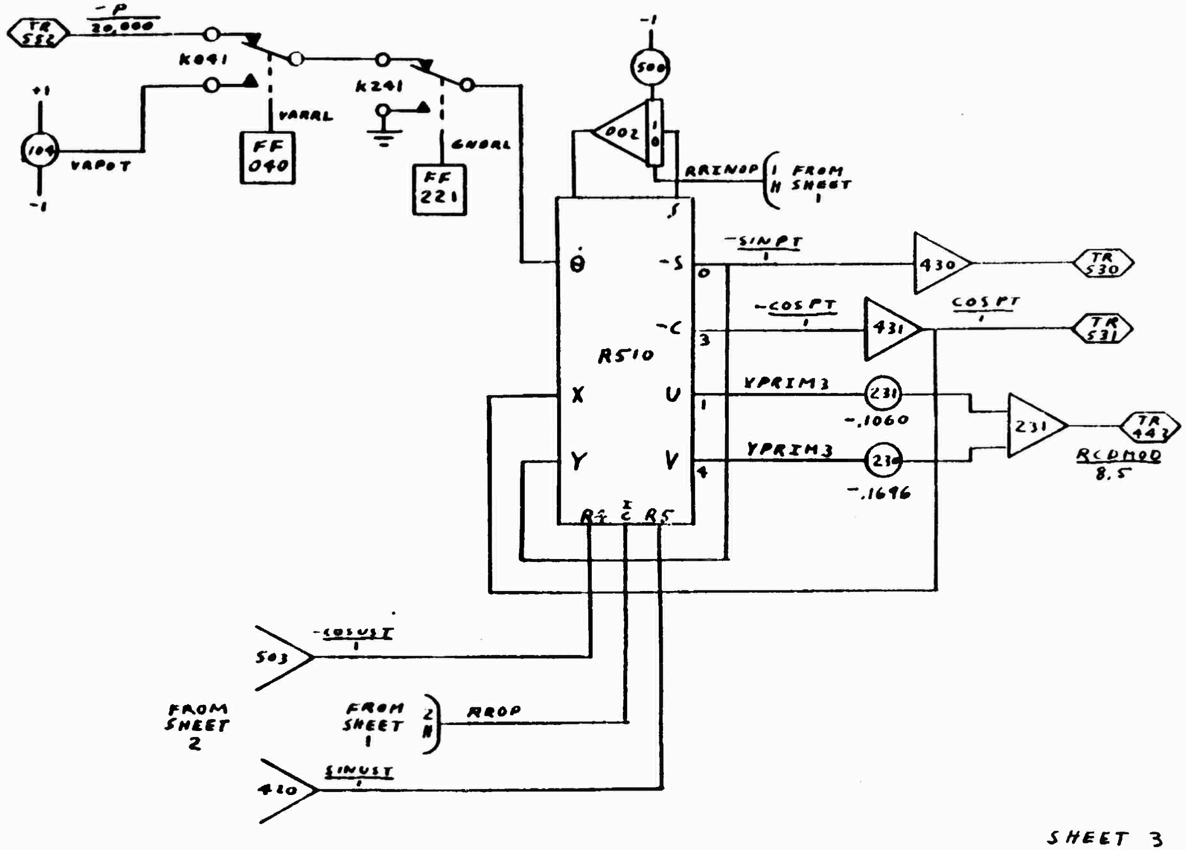


Figure A-3 Roll and Primary Reference Coil

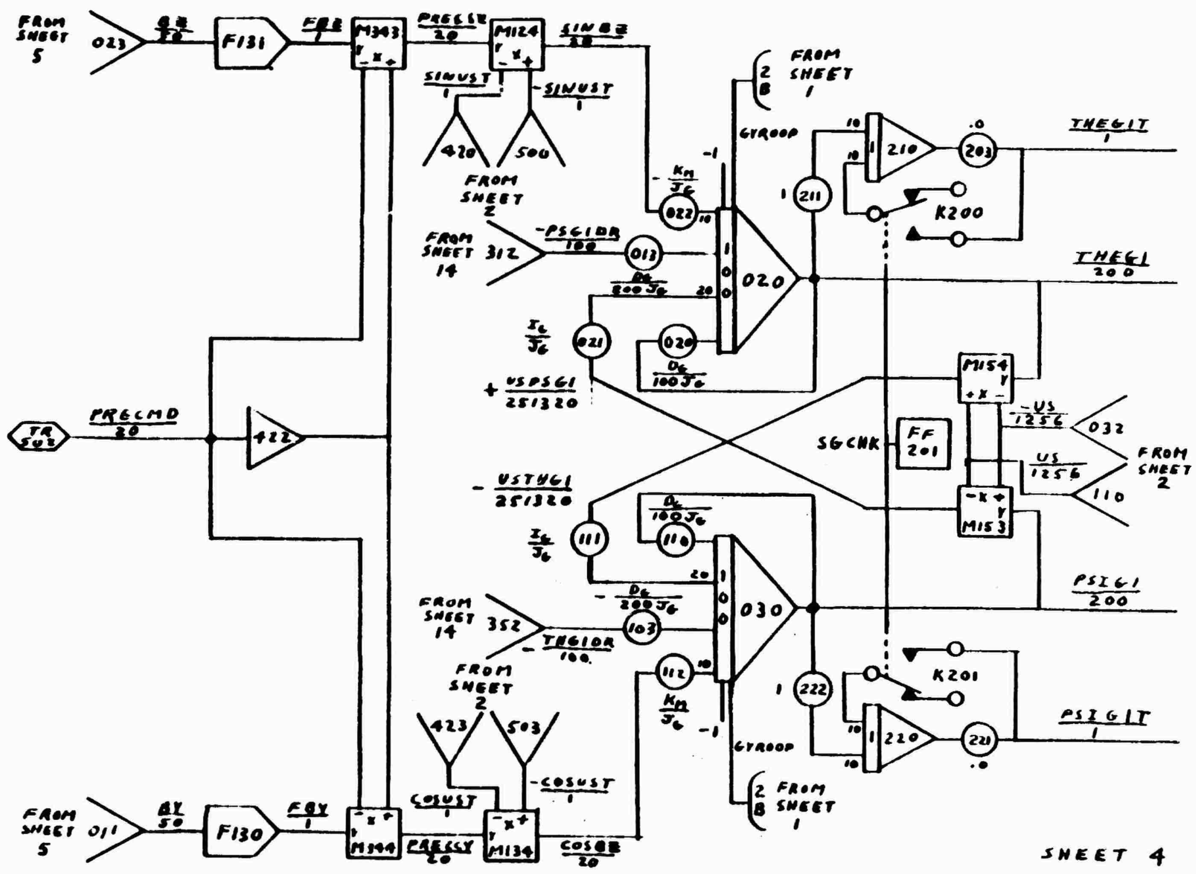


Figure A-4 Gyroscope (1 of 3)

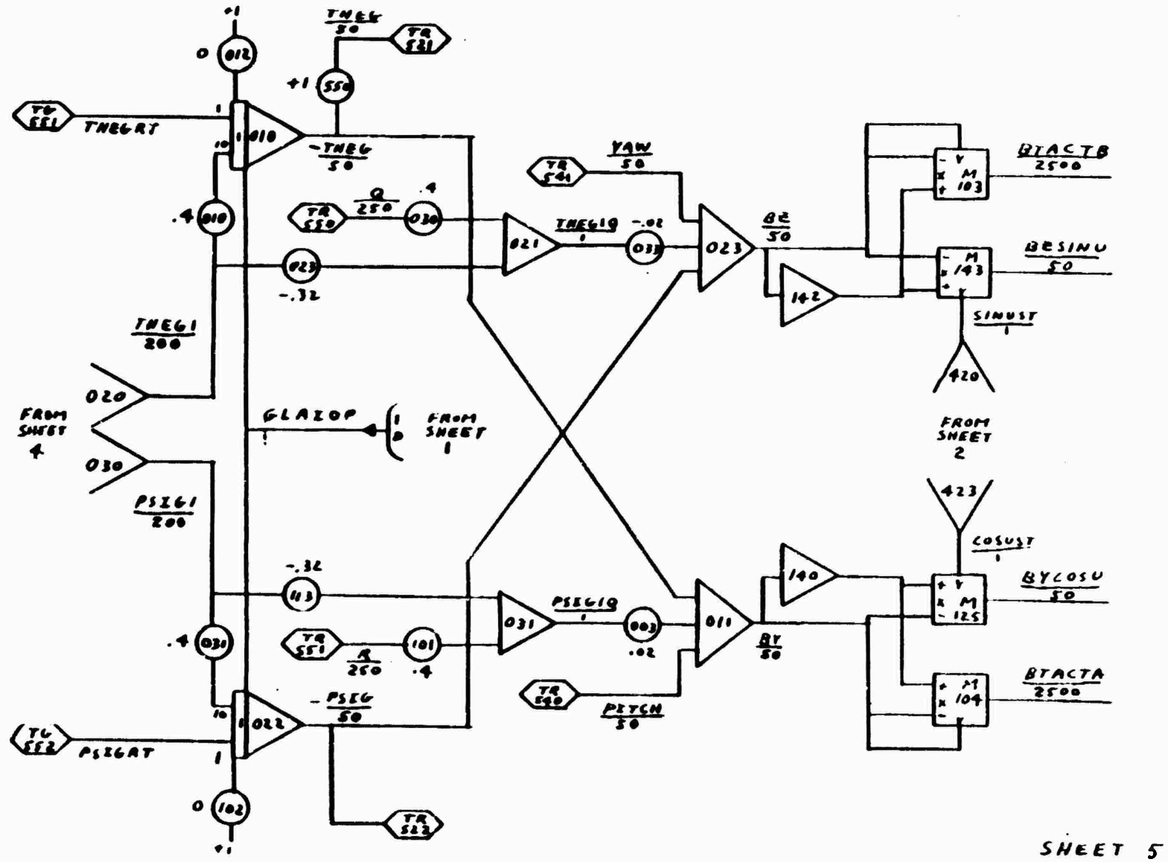


Figure A-5 Gyroscope (2 of 3)

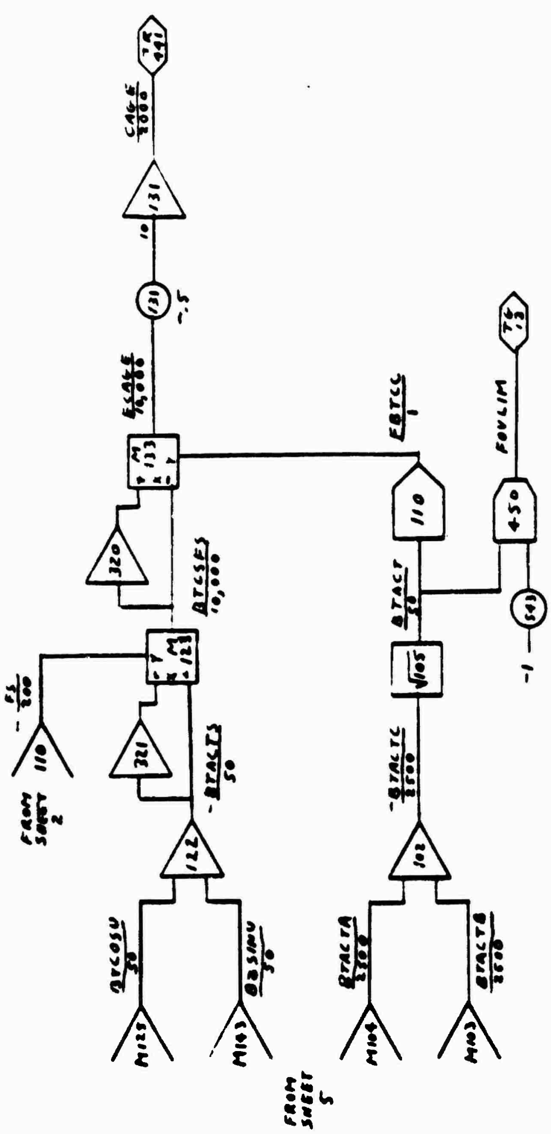


Figure A-6 Gyroscope (3 of 3)

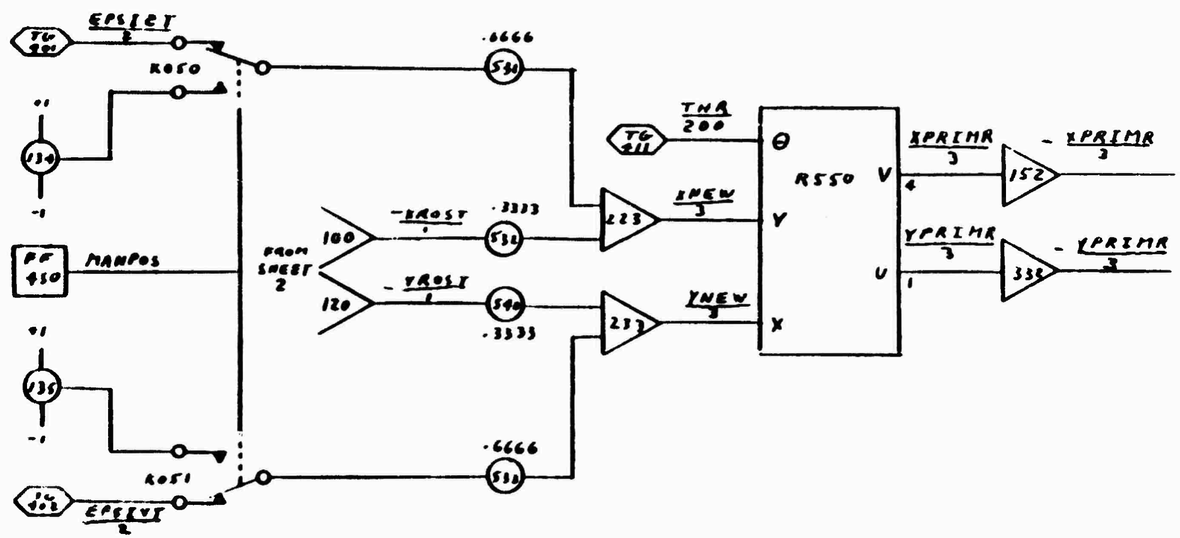
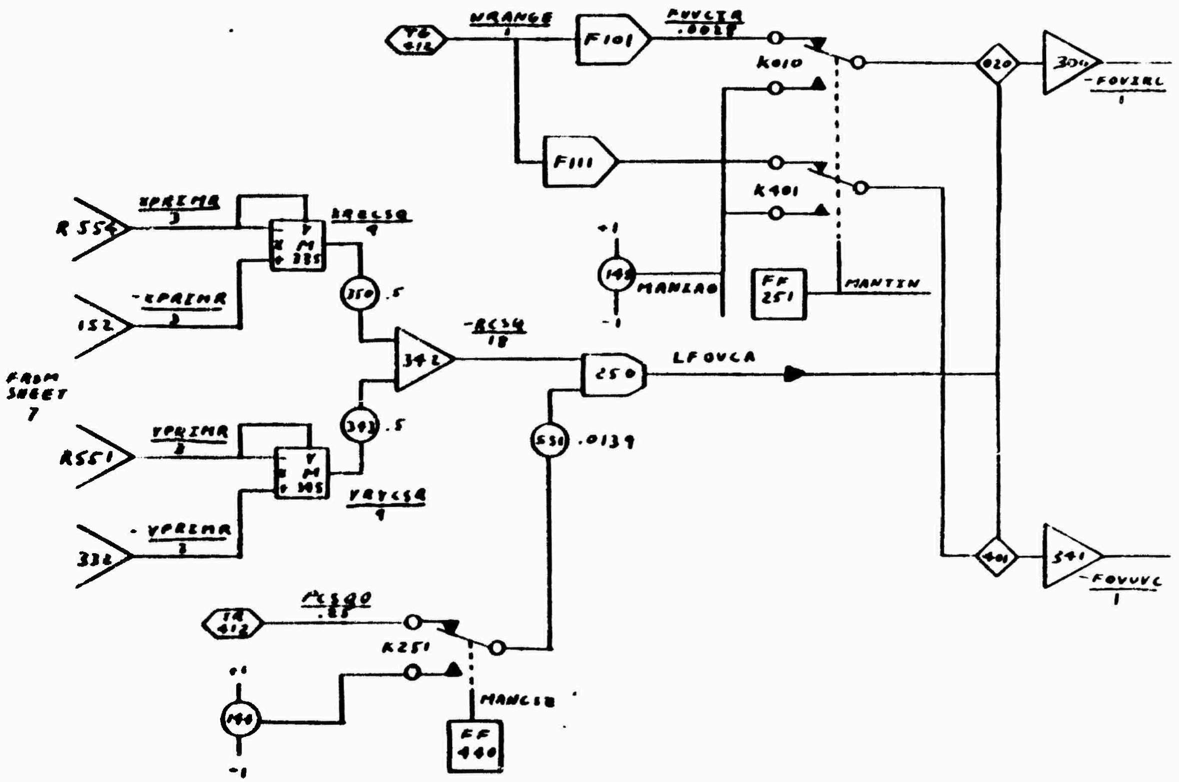


Figure A-7 Target Rotation and Positioning



SHEET 8

Figure A-8 Circle (Point Source) Logic and Intensities

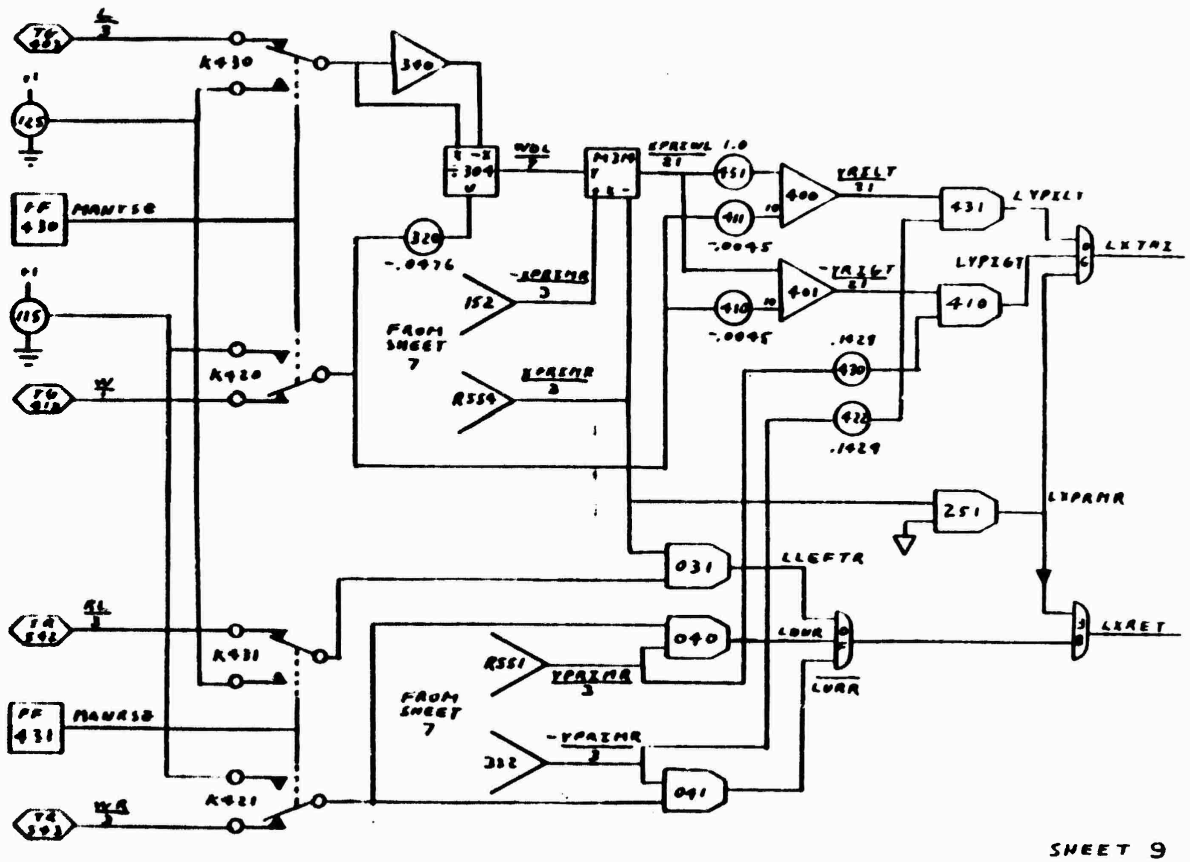


Figure A-9 Triangle (Plume) and Rectangle (Body) Logic

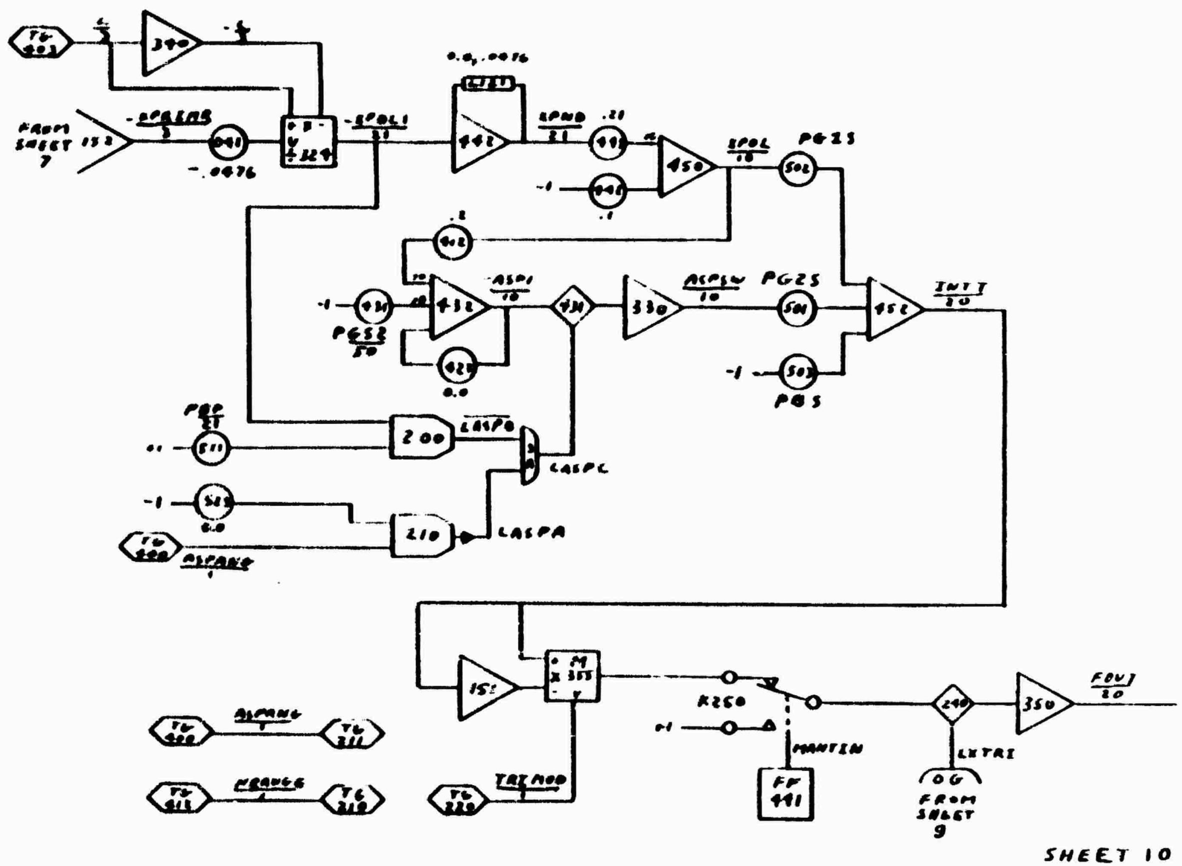


Figure A-10 Triangle (Plume) Intensity

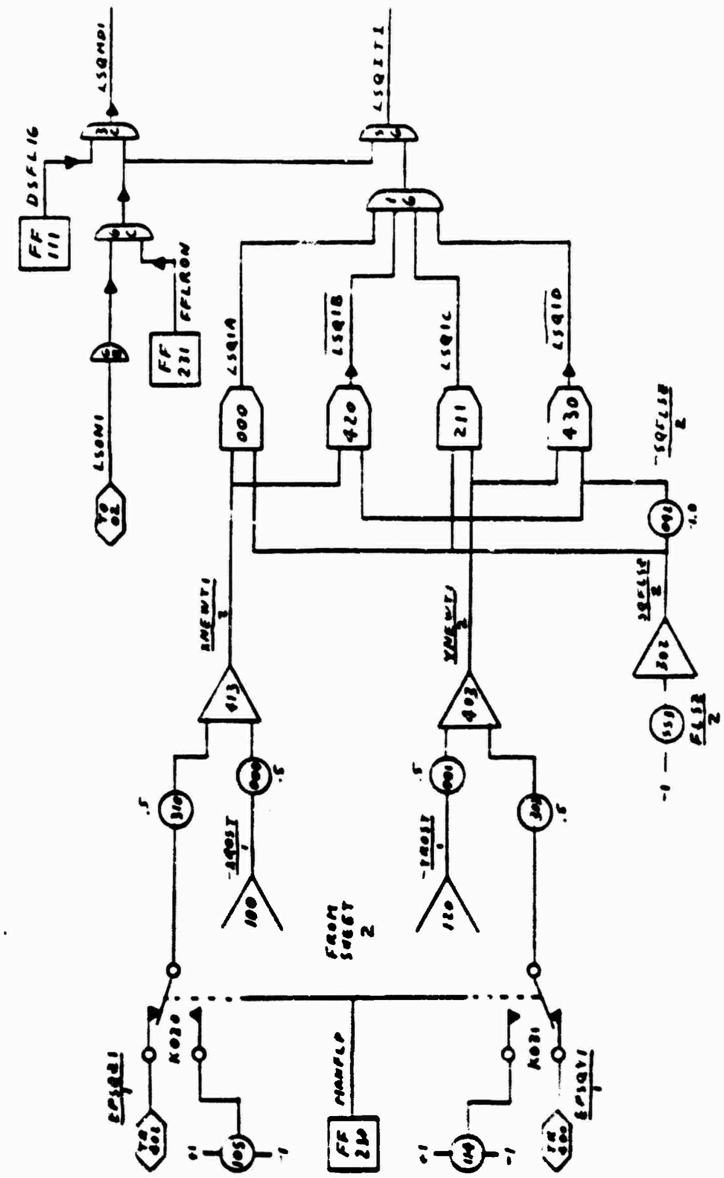
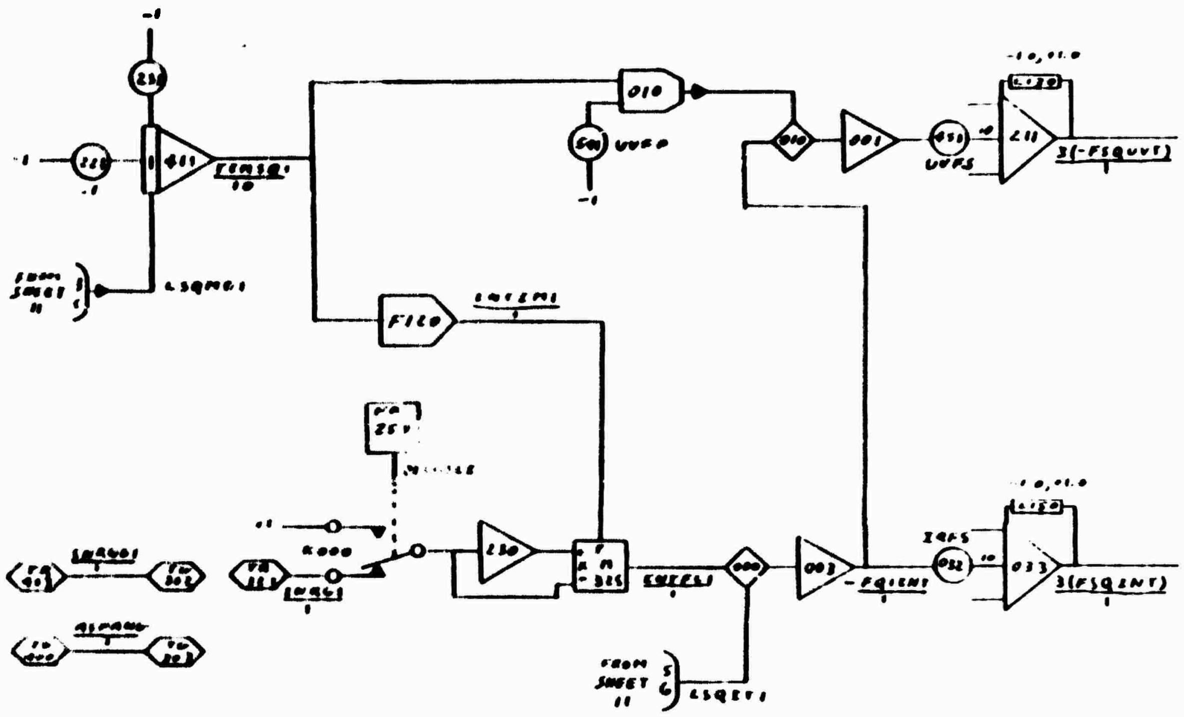


Figure A-11 Flare Logic



SHEET 12

Figure A-12 Flare Intensities

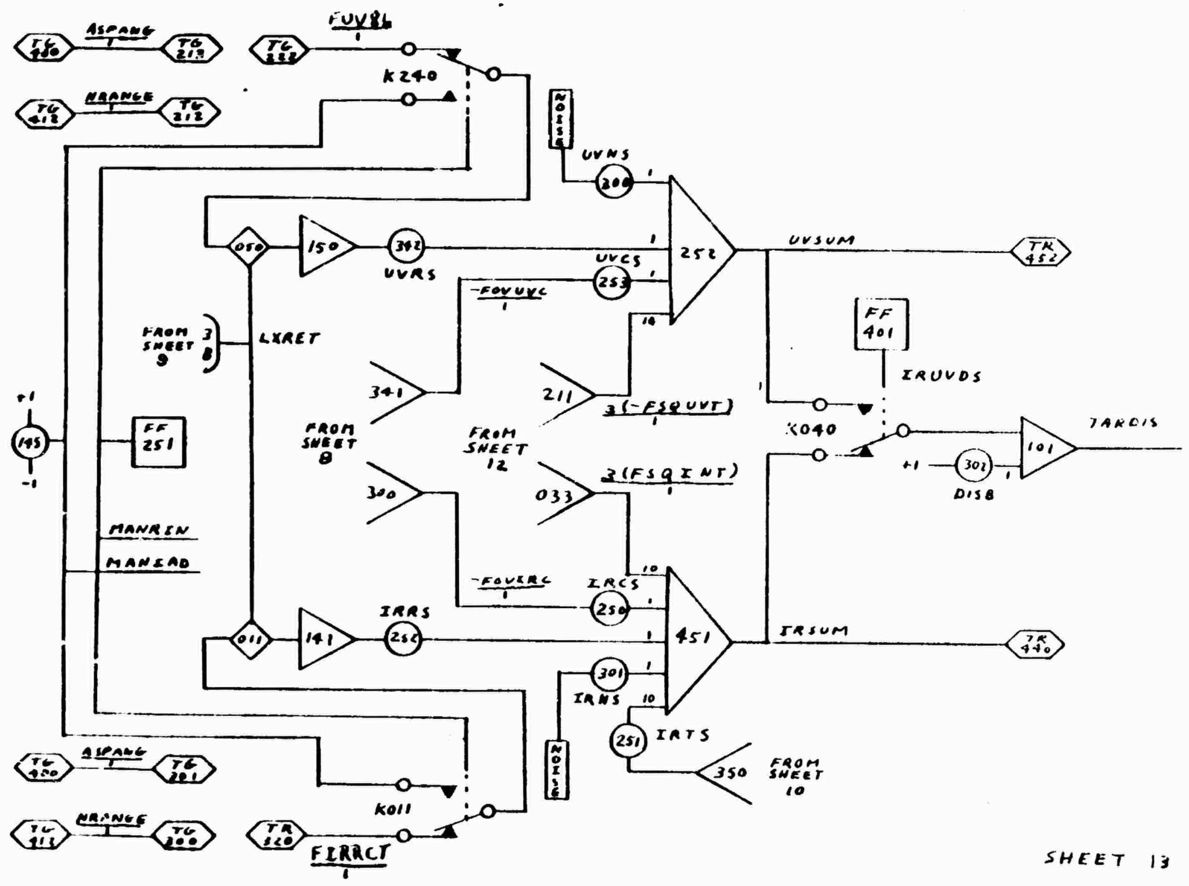


Figure A-13 Rectangle (Body) Intensity and Composite Detector Signals

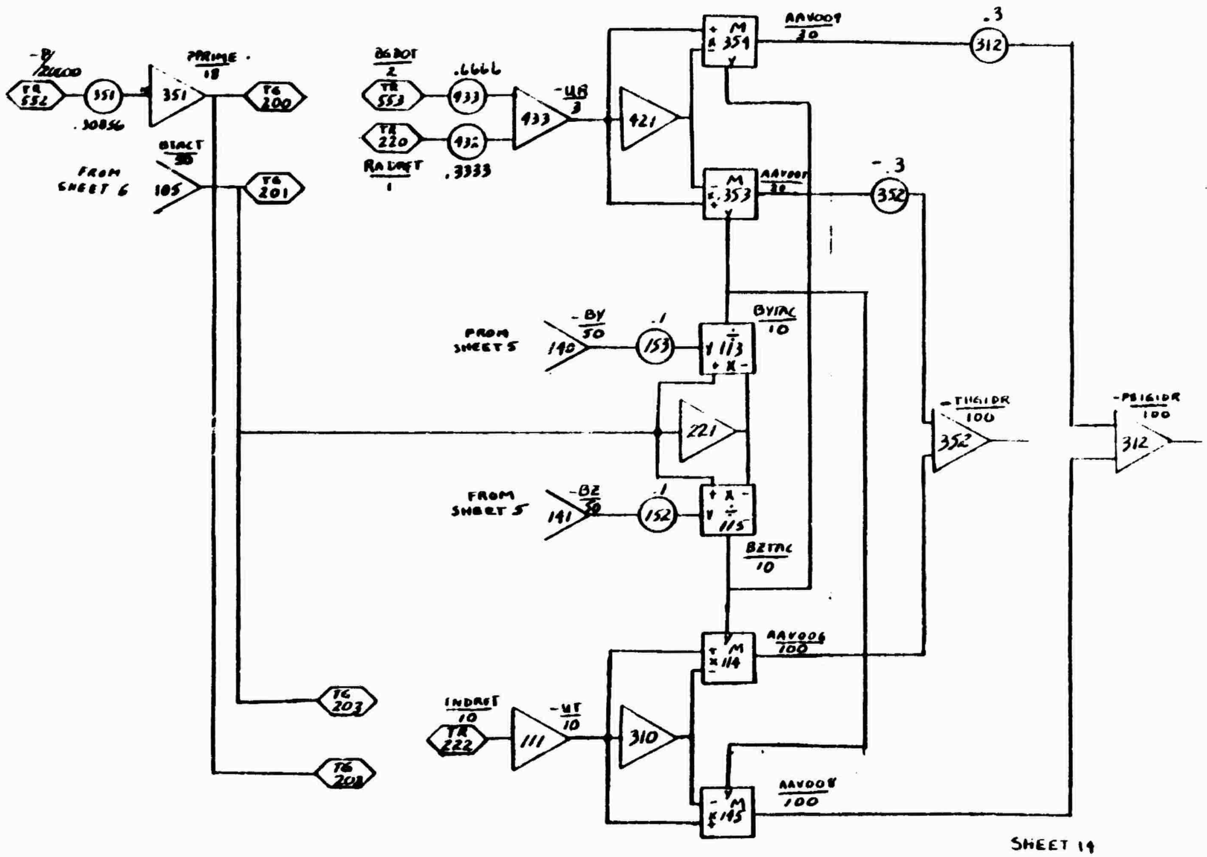


Figure A-14 Gyroscope Drift

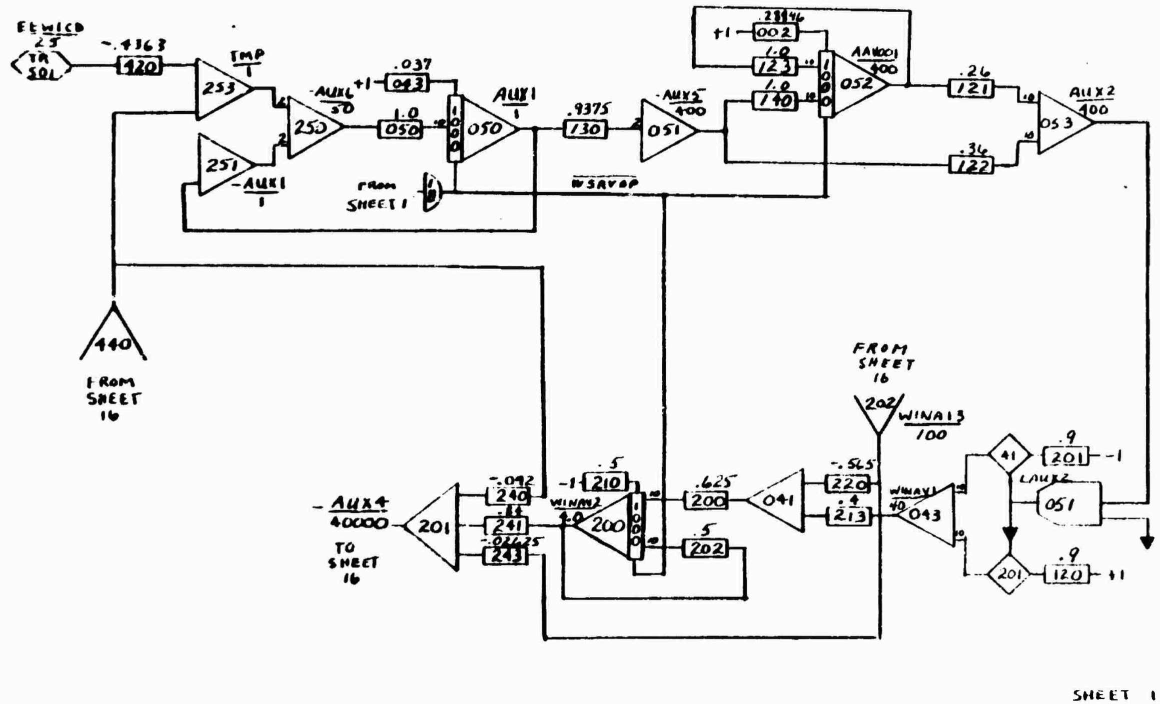


Figure A-15 Wing Servomechanism (1 of 2)

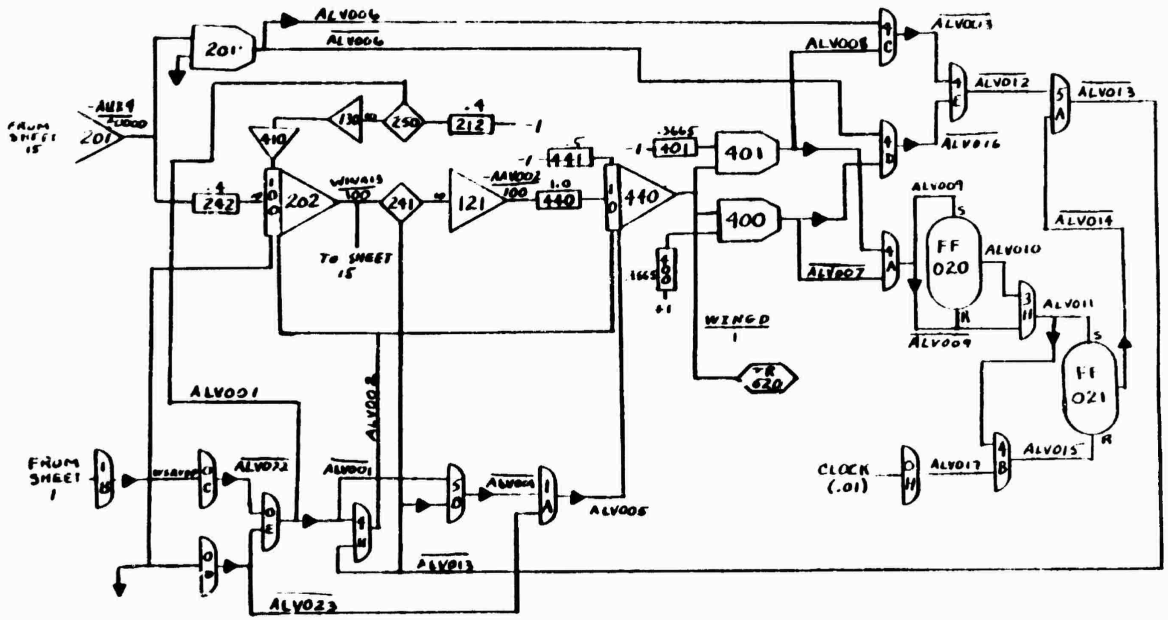


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Figure A-16 Wing Servomechanism (2 of 2)

APPENDIX B

Function Generator Data

	NAME	UNITS	NO. BPTS
FUNCTION	FABSBZ		
VARIABLE			
1	BZ		15

		BZ	FABSBZ	INDEX
		-.50000E+02	.85300E+00	1
		-.34000E+02	.85300E+00	2
		-.30000E+02	.89000E+00	3
		-.24000E+02	.92000E+00	4
		-.18000E+02	.95500E+00	5
		-.12000E+02	.97900E+00	6
		-.60000E+01	.99500E+00	7
		.00000E+00	.10000E+01	8
		.60000E+01	.99500E+00	9
		.12000E+02	.97900E+00	10
		.18000E+02	.95500E+00	11
		.24000E+02	.92000E+00	12
		.30000E+02	.88000E+00	13
		.34000E+02	.85300E+00	14
		.50000E+02	.85300E+00	15

END OF FUNCTION TABLE

Table B-1 Precessibility in Elevation Function Data (FABSBY)

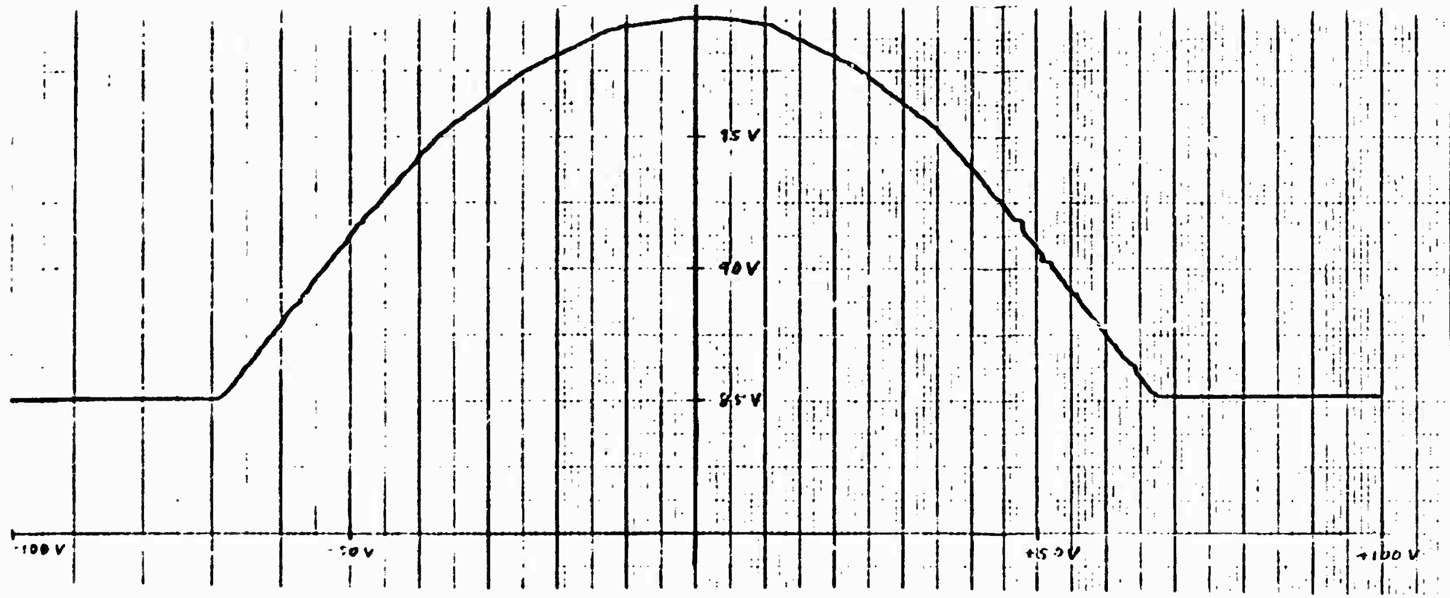

Figure B-1 Plot of Precessibility Function Data (FABSBY or FABSBZ)

	NAME	UNITS	NO. BPTS
FUNCTION	FABSBY		
VARIABLE			
1	BY		15

		BY	FABSBY	INDEX
		-.50000E+02	.85300E+00	1
		-.34000E+02	.85300E+00	2
		-.30000E+02	.88000E+00	3
		-.24000E+02	.92000E+00	4
		-.18000E+02	.95500E+00	5
		-.12000E+02	.97900E+00	6
		-.60000E+01	.99500E+00	7
		.00000E+00	.10000E+01	8
		.60000E+01	.99500E+00	9
		.12000E+02	.97900E+00	10
		.18000E+02	.95500E+00	11
		.24000E+02	.92000E+00	12
		.30000E+02	.88000E+00	13
		.34000E+02	.85300E+00	14
		.50000E+02	.85300E+00	15

END OF FUNCTION TABLE

Table B-2 Precessibility in Azimuth Function Data (FABSBZ)

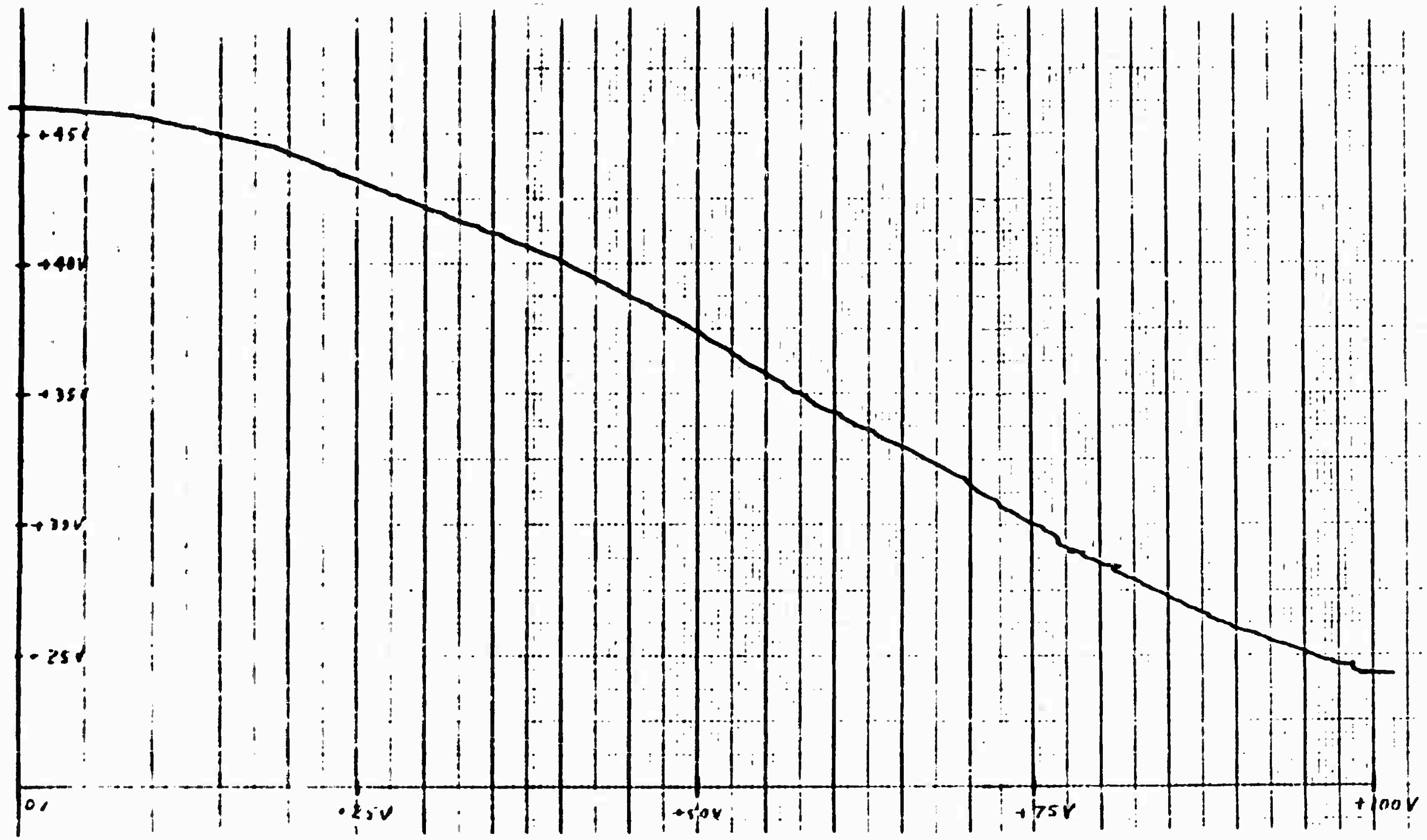

Figure B-2 Plot of Cage Coil Physical Scaling Data (BTCC)

	NAME	UNITS	NO. BPTS
FUNCTION	BTCC		
VARIABLE			
1	BTACT		11

		BTACT	BTCC	INDEX
		.00000E+00	.46250E+00	1
		.50000E+01	.45750E+00	2
		.10000E+02	.44540E+00	3
		.15000E+02	.42420E+00	4
		.20000E+02	.40300E+00	5
		.25000E+02	.37610E+00	6
		.30000E+02	.34350E+00	7
		.35000E+02	.31710E+00	8
		.40000E+02	.29460E+00	9
		.45000E+02	.25920E+00	10
		.50000E+02	.24040E+00	11

END OF FUNCTION TABLE

Table B-3 Cage Coil Physical Scaling Data (BTCC)

	NAME	UNITS	NO. BPTS
FUNCTION	RDLDRF		
VARIABLE			
1	PPRIME		5
2	BTACT		19

	BTACT	PPRIME	RDLDRF	INDEX
	.00000E+00	-.10000E+00	.60000E-01	1, 1
		.70000E+01	.60000E-01	2, 1
		.10500E+02	.75000E-01	3, 1
		.14000E+02	.12000E+00	4, 1
		.18000E+02	.15000E+00	5, 1
	.50000E+01	-.10000E+00	.19000E+00	1, 2
		.70000E+01	.24000E+00	2, 2
		.10500E+02	.27000E+00	3, 2
		.14000E+02	.31000E+00	4, 2
		.18000E+02	.35500E+00	5, 2
	.60000E+01	-.10000E+00	.40000E+00	1, 3
		.70000E+01	.44500E+00	2, 3
		.10500E+02	.48000E+00	3, 3
		.14000E-02	.53000E+00	4, 3
		.18000E+02	.57000E+00	5, 3
	.80000E+01	-.10000E+00	.59500E+00	1, 4
		.70000E+01	.62000E+00	2, 4
		.10500E+02	.64000E+00	3, 4
		.14000E+02	.64000E+00	4, 4
		.18000E+02	.60000E-01	5, 4
	.10000E+02	-.10000E+00	.60000E-01	1, 5
		.70000E+01	.75000E-01	2, 5
		.10500E+02	.12000E+00	3, 5
		.14000E+02	.15000E-00	4, 5
		.18000E+02	.19000E+00	5, 5
	.12000E+02	-.10000E+00	.24000E+00	1, 6
		.70000E+01	.27000E+00	2, 6
		.10500E+02	.31000E+00	3, 6
		.14000E+02	.35500E-00	4, 6
		.18000E+02	.40000E+00	5, 6
	.14000E+02	-.10000E+00	.44500E+00	1, 7
		.70000E+01	.48000E+00	2, 7
		.10500E+02	.53000E+00	3, 7
		.14000E+02	.57000E+00	4, 7
		.18000E+02	.59500E-00	5, 7
	.16000E+02	-.10000E+00	.62000E+00	1, 8
		.70000E+01	.64000E+00	2, 8
		.10500E+02	.64000E+00	3, 8
		.14000E+02	.60000E-01	4, 8
		.18000E+02	.60000E-01	5, 8
	.18000E+02	-.10000E+00	.75000E-01	1, 9
		.70000E+01	.11000E+00	2, 9
		.10500E+02	.14500E-00	3, 9
		.14000E+02	.18000E+00	4, 9
		.18000E+02	.23000E+00	5, 9
	.20000E+02	-.10000E+00	.26000E+00	1, 10
		.70000E+01	.29000E+00	2, 10

Table B-4 Radial Drift Data (RDLDRF - 1 of 2)

	.10500E+02	.34000E+00	3, 10
	.14000E+02	.37500E+00	4, 10
	.18000E+02	.41000E+00	5, 10
.22000E+02	-.10000E+00	.44500E+00	1, 11
	.70000E+01	.48000E+00	2, 11
	.10500E+02	.51000E+00	3, 11
	.14000E+02	.52500E+00	4, 11
	.18000E+02	.52500E+00	5, 11
.24000E+02	-.10000E+00	.52000E+00	1, 12
	.70000E+01	.52000E+00	2, 12
	.10500E+02	.55000E-01	3, 12
	.14000E+02	.55000E-01	4, 12
	.18000E+02	.70000E-01	5, 12
.26000E+02	-.10000E+00	.10000E+00	1, 13
	.70000E+01	.13000E+00	2, 13
	.10500E+02	.16500E+00	3, 13
	.14000E+02	.21000E+00	4, 13
	.18000E+02	.24500E+00	5, 13
.28000E+02	-.10000E+00	.27000E+00	1, 14
	.70000E+01	.31000E+00	2, 14
	.10500E+02	.35000E+00	3, 14
	.14000E+02	.37500E+00	4, 14
	.18000E+02	.40000E+00	5, 14
.30000E+02	-.10000E+00	.43000E+00	1, 15
	.70000E+01	.44500E+00	2, 15
	.10500E+02	.43500E+00	3, 15
	.14000E+02	.41000E+00	4, 15
	.18000E+02	.35500E+00	5, 15
.32000E+02	-.10000E+00	.35500E+00	1, 16
	.70000E+01	.45000E-01	2, 16
	.10500E+02	.45000E-01	3, 16
	.14000E+02	.60000E-01	4, 16
	.18000E+02	.90000E-01	5, 16
.34000E+02	-.10000E+00	.12000E+00	1, 15
	.70000E+01	.15000E+00	2, 17
	.10500E)02	.18000E+00	3, 17
	.14000E+02	.21000E)00	4, 17
	.18000E+02	.23500E+00	5, 17
.36000E+02	-.10000E+00	.27000E+00	1, 18
	.70000E+01	.29500E+00	2, 18
	.10500E+02	.33000E+00	3, 18
	.14000E+02	.35000E+00	4, 18
	.18000E+02	.36000E+00	5, 18
.50000E+02	-.10000E+00	.23500E-00	1, 19
	.70000E+01	.22000E-00	2, 19
	.10500E+02	.21000E+00	3, 19
	.14000E+02	.70000E-01	4, 19
	.18000E+02	.70000E-01	5, 19

END OF FUNCTION TABLE

Table B-4 (Cont'd) Radial Drift Data (RDLDRF-2 of 2)

	NAME	UNITS	NO. BPTS
FUNCTION	TNGDRF		
VARIABLE			
1	PPRIME		5
2	BTACT		19

	BTACT	PPRIME	TNGDRF	INDEX
	.00000E+00	-.10000E+00	.00000E+00	1, 1
		.70000E+01	.00000E+00	2, 1
		.10500E+02	-.10000E+00	3, 1
		.14000E+02	-.20000E+00	4, 1
		.18000E+02	-.20000E+00	5, 1
	.50000E+01	-.10000E+00	-.20000E+00	1, 2
		.70000E+01	-.25000E+00	2, 2
		.10500E+02	-.30000E+00	3, 2
		.14000E+02	-.40000E+00	4, 2
		.18000E+02	-.45000E+00	5, 2
	.60000E+01	-.10000E+00	-.50000E+00	1, 3
		.70000E+01	-.60000E+00	2, 3
		.10500E+02	-.65000E+00	3, 3
		.14000E+02	-.75000E+00	4, 3
		.18000E+02	-.80000E+00	5, 3
	.80000E+01	-.10000E+00	-.90000E+00	1, 4
		.70000E+01	-.10000E+01	2, 4
		.10500E+02	-.11000E+01	3, 4
		.14000E+02	-.11000E+01	4, 4
		.18000E+02	.00000E+00	5, 4
	.10000E+02	-.10000E+00	.00000E+00	1, 5
		.70000E+01	-.10000E+00	2, 5
		.10500E+02	-.20000E+00	3, 5
		.14000E+02	-.20000E+00	4, 5
		.18000E+02	-.20000E+00	5, 5
	.12000E+02	-.10000E+00	-.25000E+00	1, 6
		.70000E+01	-.30000E+00	2, 4
		.10500E+02	-.40000E+00	3, 6
		.14000E+02	-.45000E+00	4, 6
		.18000E+02	-.50000E)00	5, 6
	.14000E+02	-.10000E+00	-.60000E+00	1, 7
		.70000E+01	-.65000E+00	2, 7
		.10500E+02	-.75000E+00	1, 7
		.14000E+02	-.80000E+00	4, 7
		.18000E+02	-.90000E+00	5, 7
	.16000E+02	-.10000E+00	-.10000E+01	1, 8
		.70000E+01	-.11000E+01	2, 8
		.10500E+02	-.11000E+01	3, 8
		.14000E+02	.00000E+00	4, 8
		.18000E+02	.00000E+00	5, 8
	.18000E+02	-.10000E+00	-.10000E+00	1, 9
		.70000E+01	-.20000E+00	2, 9
		.10500E+02	-.25000E+00	3, 9
		.14000E+02	-.35000E+00	4, 9
		.18000E+02	-.35000E+00	5, 9
	.20000E+02	-.10000E+00	-.40000E+00	1, 10
		.70000E+01	-.50000E+00	2, 10

Table B-5 Tangential Drift Data (TNGDRF-1 of 2)

	.10500E+02	-.55000E+00	3, 10
	.14000E+02	-.65000E+00	4, 10
	.18000E+02	-.75000E+00	5, 10
.22000E+02	-.10000E+00	-.90000E+00	1, 11
	.70000E+01	-.12000E+01	2, 11
	.10500E+02	-.14000E+01	3, 11
	.14000E+02	-.17500E+01	4, 11
	.18000E+02	-.22000E+01	5, 11
.24000E+02	-.10000E+00	-.27000E+01	1, 12
	.70000E+01	-.27000E+01	2, 12
	.10500E+02	.00000E+00	3, 12
	.14000E+02	.00000E+00	4, 12
	.18000E+02	-.10000E+00	5, 12
.26000E+02	-.10000E+00	-.20000E+00	1, 13
	.70000E+01	-.30000E+00	2, 13
	.10500E+02	-.35000E+00	3, 13
	.14000E+02	-.35000E+00	4, 13
	.18000E+02	-.40000E+00	5, 13
.28000E+02	-.10000E+00	-.55000E+00	1, 14
	.70000E+01	-.70000E+00	2, 14
	.10500E+02	-.90000E+00	3, 14
	.14000E+02	-.12000E+01	4, 14
	.18000E+02	-.15000E+01	5, 14
.30000E+02	-.10000E+00	-.19000E+01	1, 15
	.70000E+01	-.24000E+01	2, 15
	.10500E+02	-.31000E+01	3, 15
	.14000E+02	-.39000E+01	4, 15
	.18000E+02	-.51000E+01	5, 15
.32000E+02	-.10000E+00	-.51000E+01	1, 16
	.70000E+01	.00000E+00	2, 16
	.10500E+02	.00000E+00	3, 16
	.14000E+02	-.10000E+00	4, 16
	.18000E+02	-.20000E+00	5, 16
.34000E+02	-.10000E+00	-.30000E+00	1, 15
	.70000E+01	-.40000E-00	2, 17
	.10500E)02	-.45000E+00	3, 17
	.14000E+02	-.60000E)00	4, 17
	.18000E+02	-.90000E+00	5, 17
.36000E+02	-.10000E+00	-.11000E+01	1, 18
	.70000E+01	-.14000E+01	2, 18
	.10500E+02	-.17500E+01	3, 13
	.14000E+02	-.23000E+01	4, 18
	.18000E+02	-.30000E+01	5, 13
.50000E+02	-.10000E+00	-.40000E+01	1, 19
	.70000E+01	-.52000E+01	2, 19
	.10500E+02	-.66000E+01	3, 19
	.14000E+02	-.86000E+01	4, 19
	.18000E+02	-.86000E+01	5, 19

END OF FUNCTION TABLE

Table B-5 (Cont'd) Tangential Drift Data (TNGDRF-2 of 2)

APPENDIX C

HISC Documentation

- Schematics
- Circuit Card Layouts
- Wiring Lists

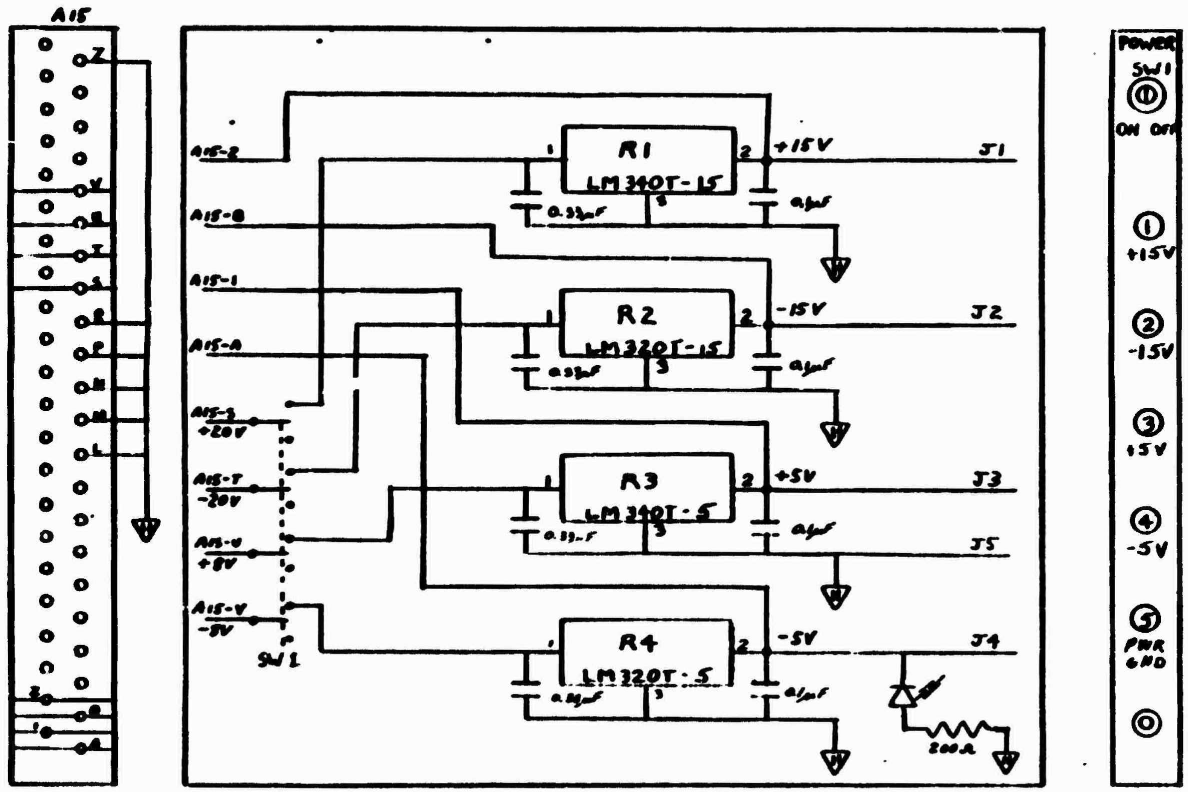

Figure C-1 Power Supply Module

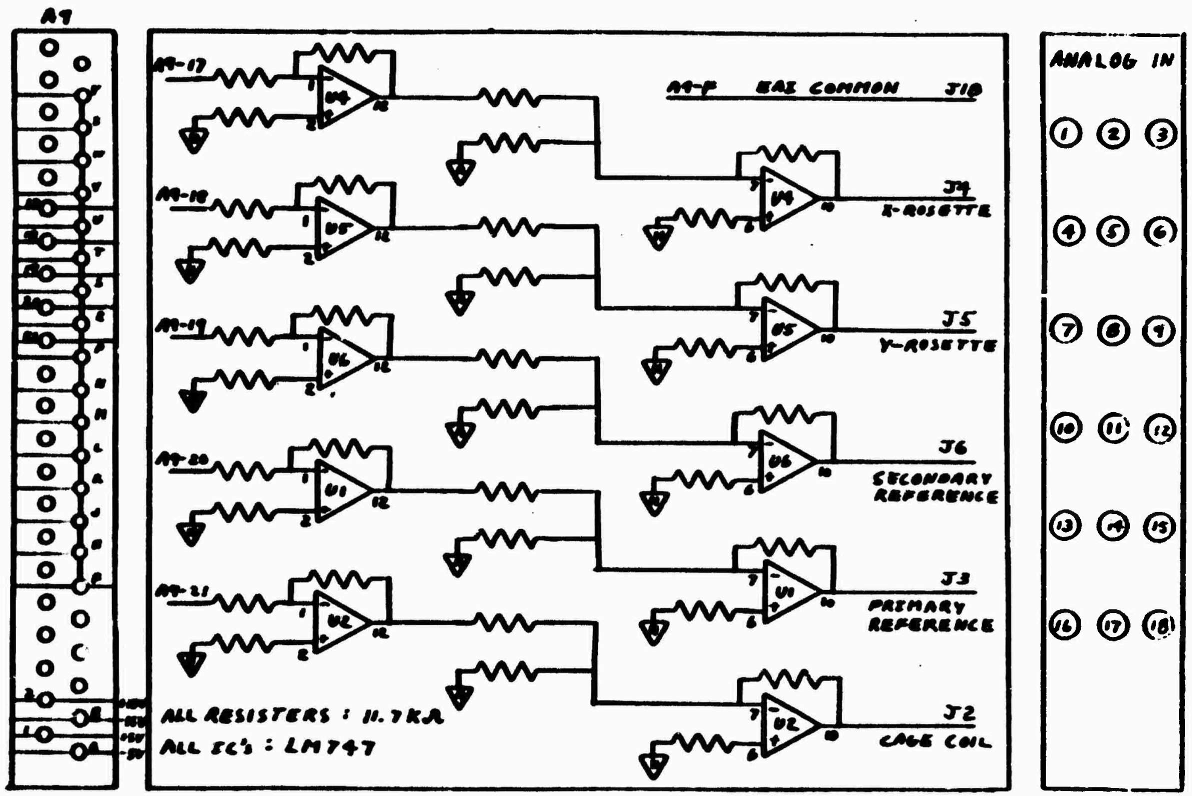

Figure C-2 Analog in Module

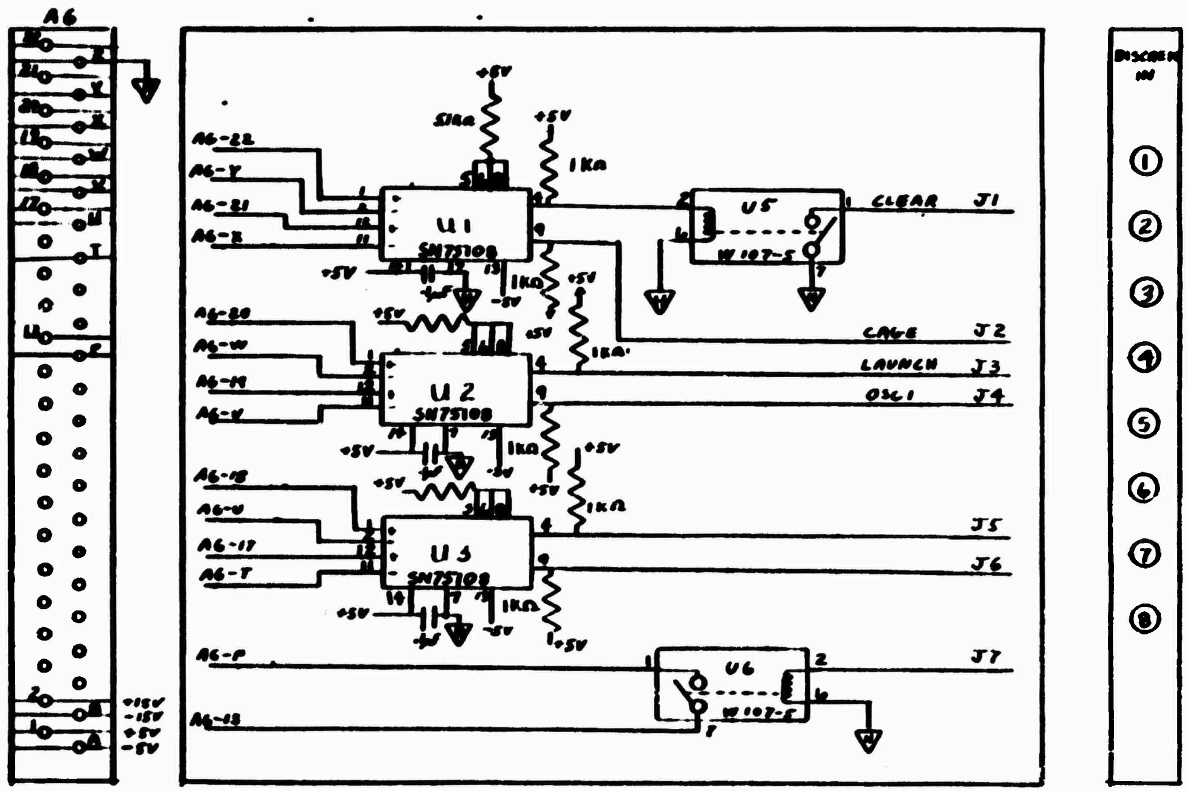

Figure C-3 Discrete In Module

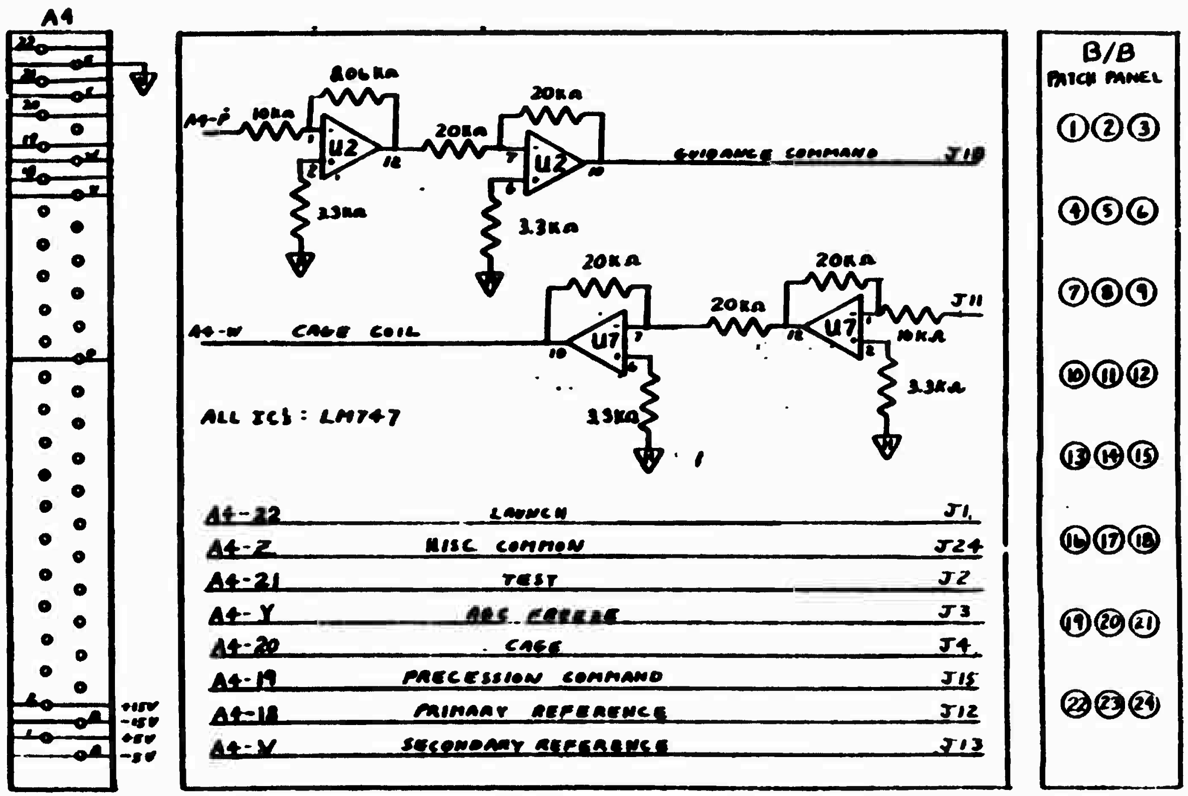

Figure C-4 Breadboard Patch Panel Module

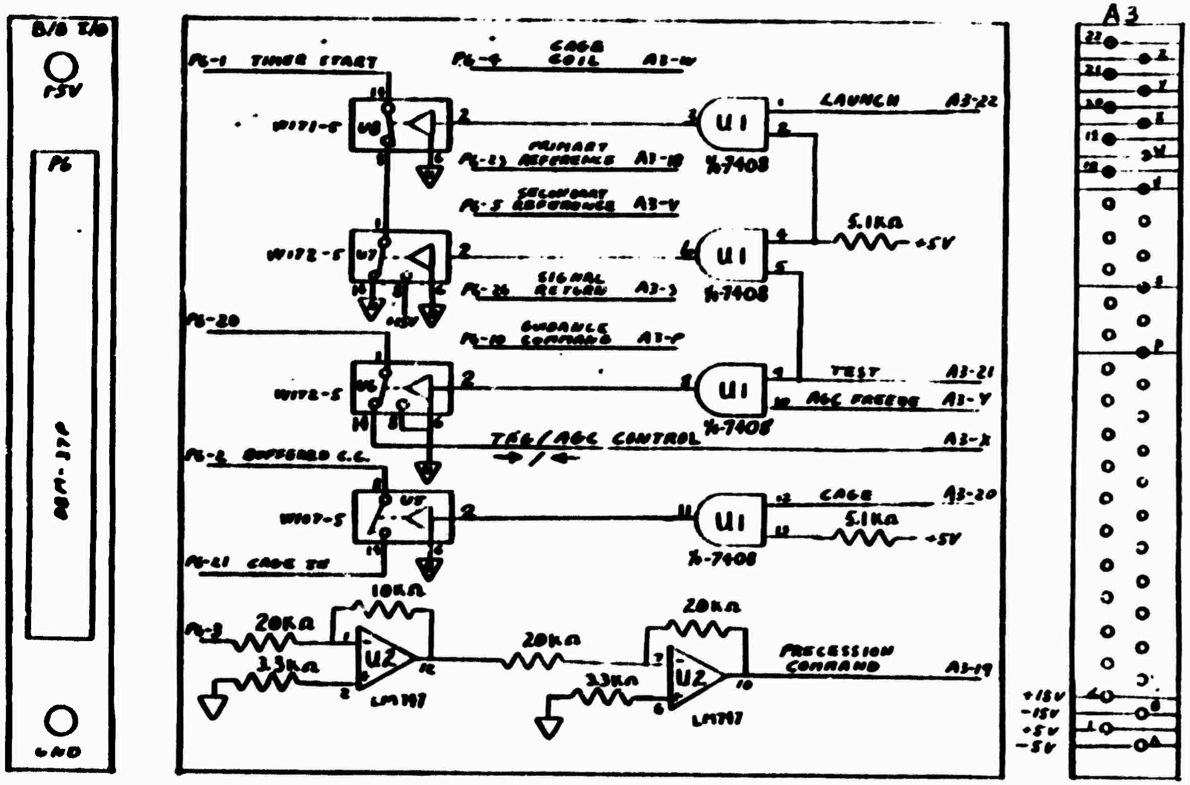

Figure C-5 Breadboard I/O Module

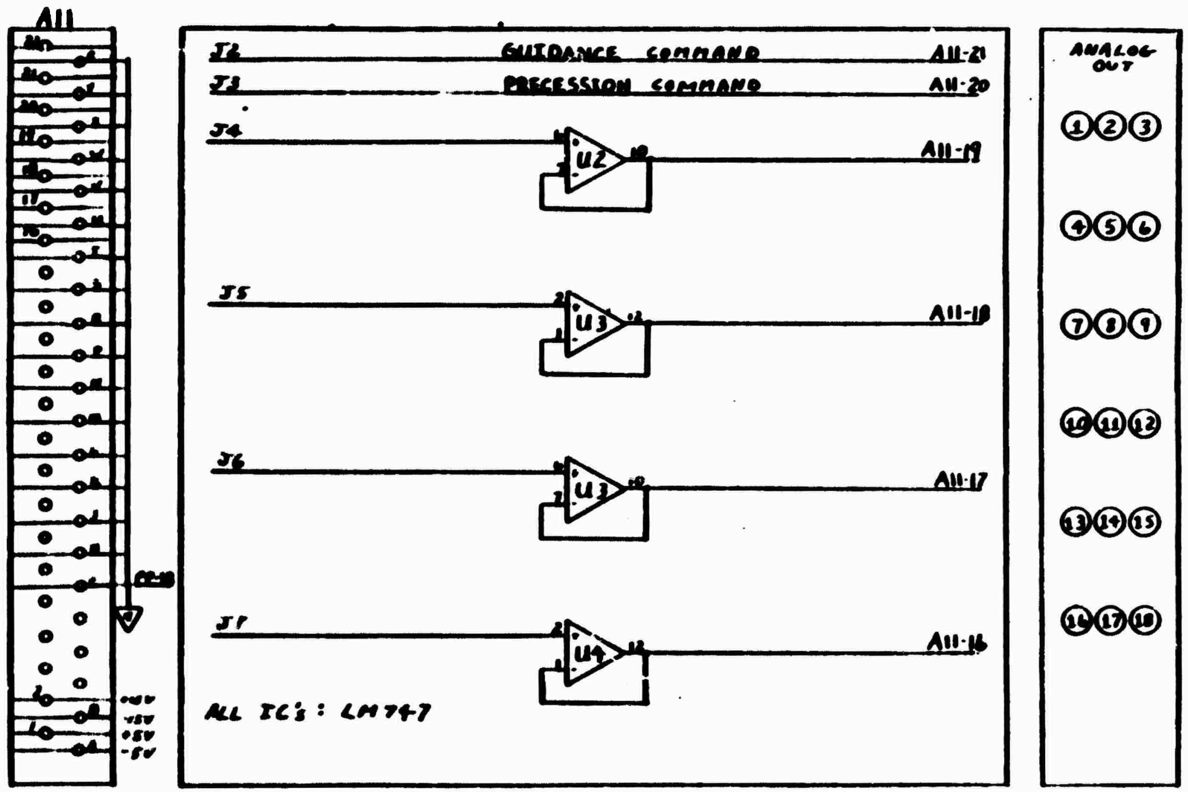

Figure C-6 Analog Out Module

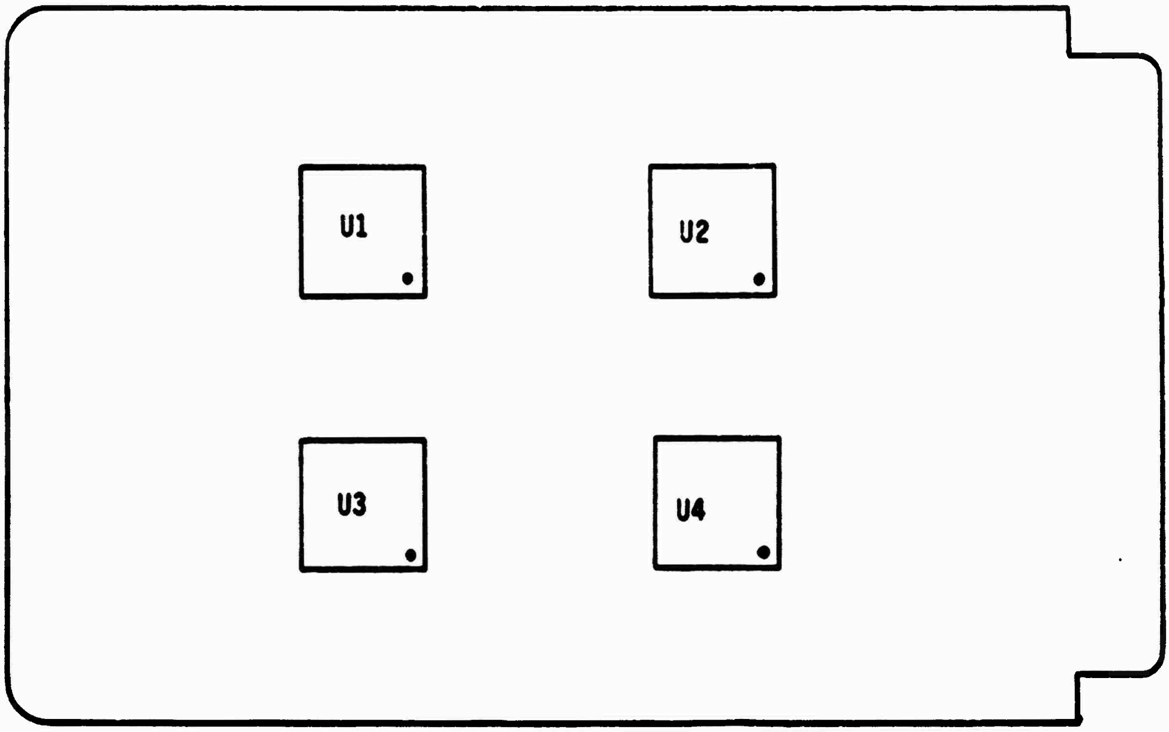

Figure C-7 Power Supply Card Layout

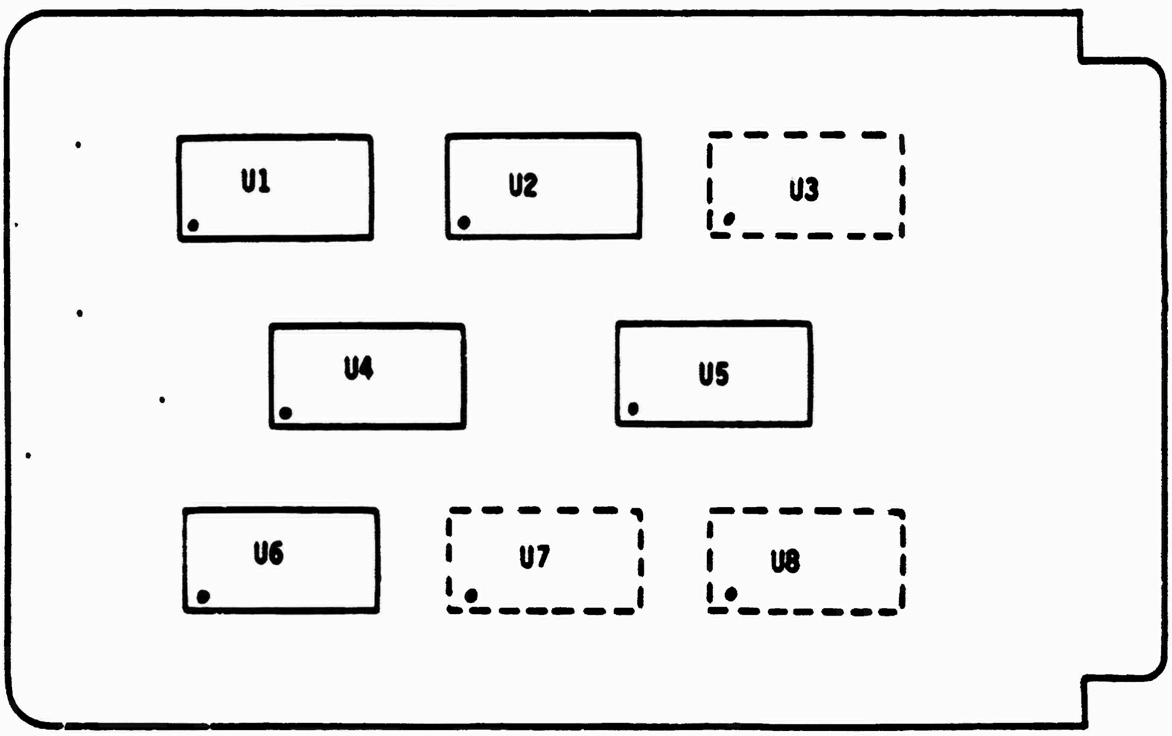

Figure C-8 Analog In Card Layout

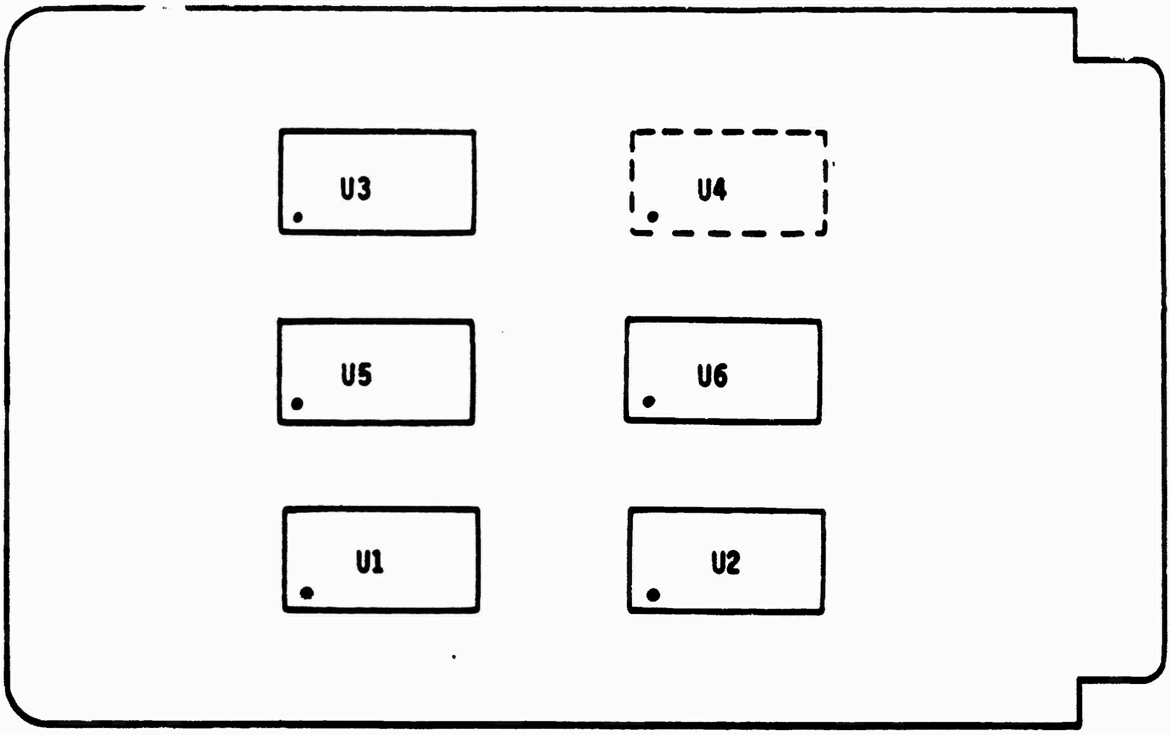

Figure C-9 Discrete In Card Layout

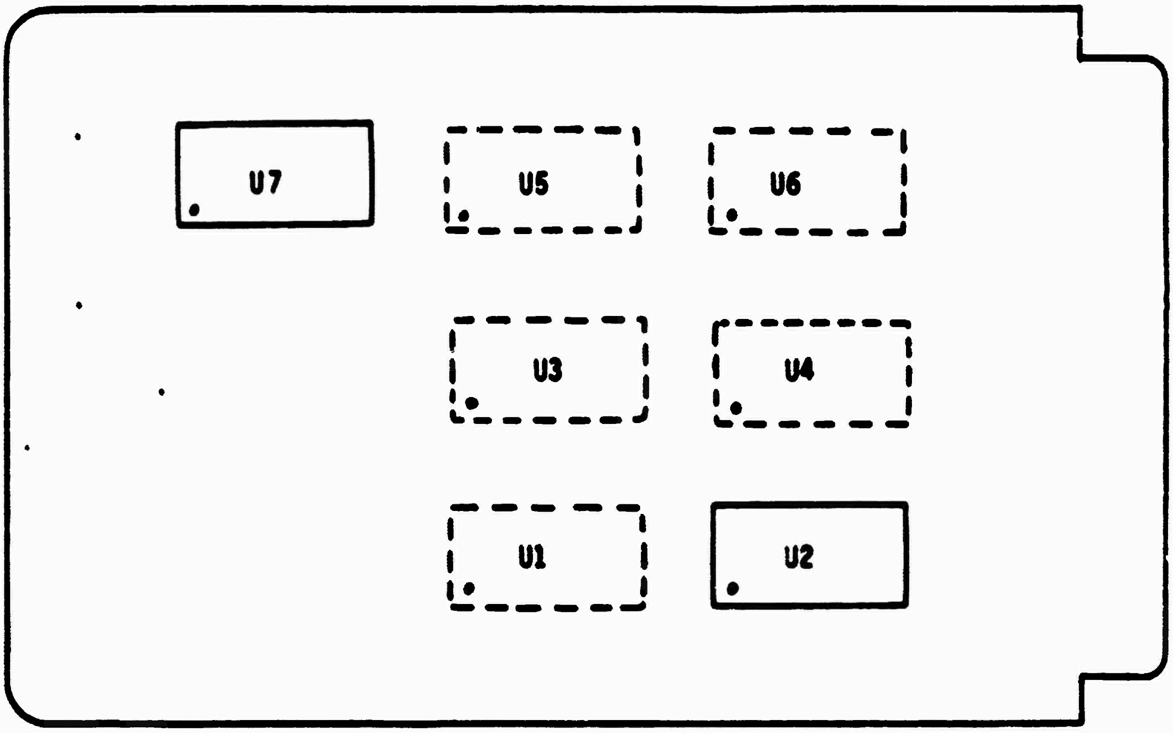

Figure C-10 Breadboard Patch Panel Card Layout

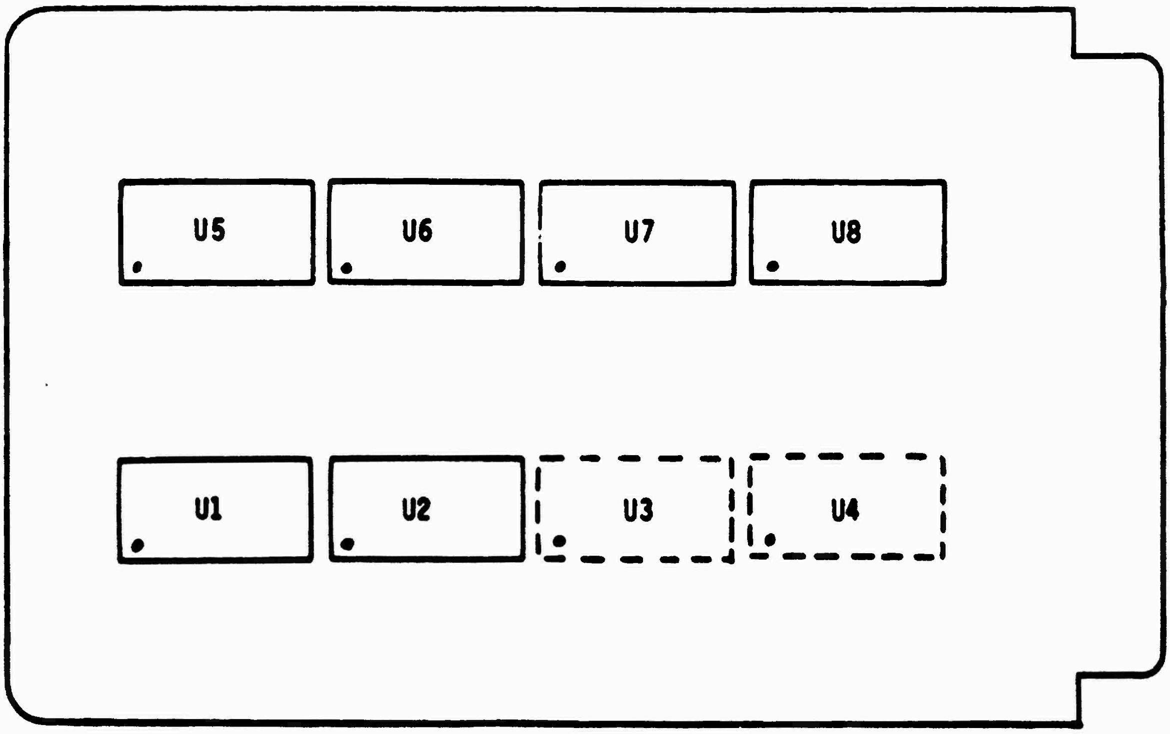

Figure C-11 Breadboard I/O Card Layout

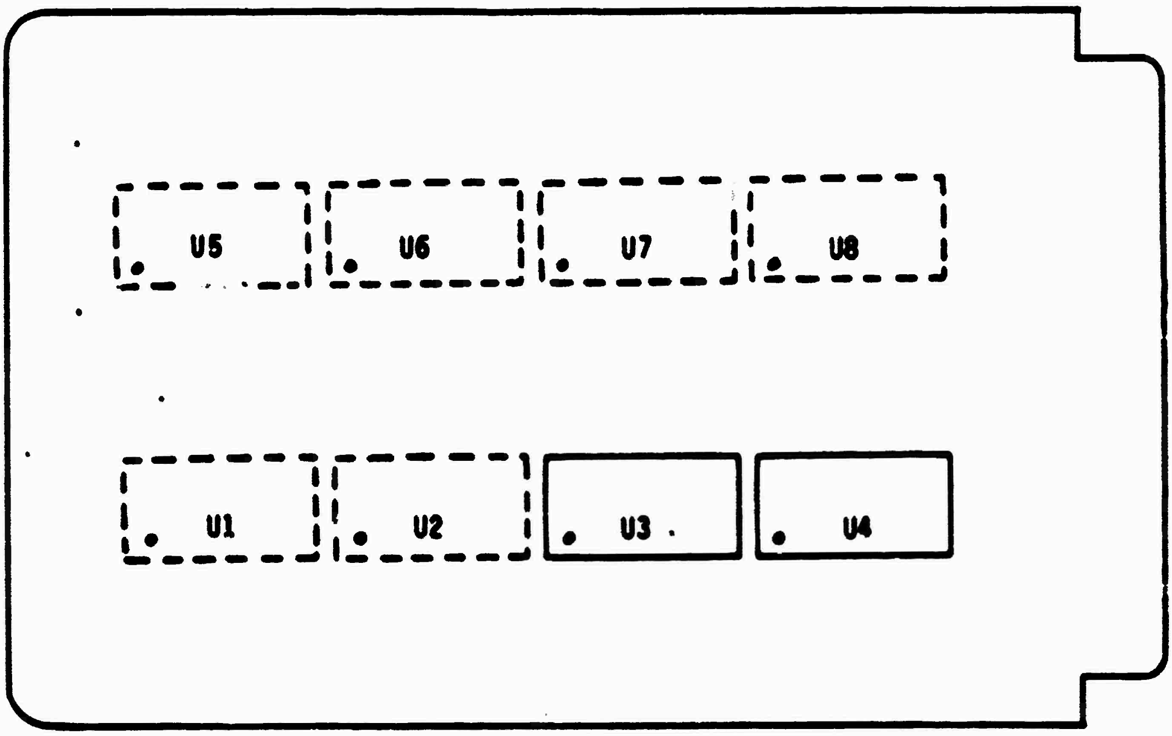

Figure C-12 Analog Out Card Layout

Signal	HISC Connector Pin No.	Cable 1W6 Connector Pin No.	Connector Pin No.	Breadboard Connector Pin No.	Front Pin No.
Precession Coil	P6 - 3	S6 - 3	P98 - 34	J98 - 34	31
Cage Coil	4	4	30	30	32
Sec. Reference	5	5	12	12	13
UV Preamp	6	6	8	8	16
Signal Return 1	7	7	28	28	1
Gyro Drive	9	9	16	16	33
IR AGC 1	13	13	20	20	40
Precession Return	22	22	36	36	42
Gyro Reference	23	23	26	26	10
IR Preamp	24	24	4	4	2
Preamp Return	25	25	24	24	21
Secondary Drive	28	28	14	14	36
IR AGC 2	32	32	10	10	42
Timer Start	1	1	P99 - 6	J99 - 6	76
Buffered Cage Coil	2	2	10	10	18
Signal Return 3	8	8	30	30	3
Guidance Command	10	10	36	36	26
UV Preamp/Pulse Amp	11	11	4	4	14
TE Pulses/IR Threshold	12	12	28	28	43
TAG/AGC Control	20	20	26	26	19
Cage-In	21	21	P75	None	75
Wing Erect Control	27	27	P99 - 34	J99 - 34	48
IR Preamp/ Pulse Amp	29	29	24	24	29
+ Wing Erect/ UV Threshold	30	30	14	14	47
Audio/Sync Filter	31	31	12	12	27

Table C-1 EBA/HISC Cable (1W6) Wiring List

SIGNAL	CABLE 1W4			CABLE 2W4		
OUTDIS #	U90 Edge #	Wire Color	Connector P4 Pin #	Connector J4 Pin #	Wire Color	A6/A7 Pin #
0 + *	1	White	1	1	White	A6-22
0 -	A	Green	20	20	Green	A6-Y
1 +	D	Blue	2	2	Blue	A6-21
1 -	4	White	21	21	White	A6-X
2 +	B	Red	3	3	Red	A6-20
2 -	2	Orange	22	22	Orange	A6-W
3 +	C	Blue	4	4	Blue	A6-19
3 -	3	Green	23	23	Green	A6-V
4 +	F	Black	5	5	Black	A6-18
4 -	6	White	24	24	White	A6-U
5 +	H	Green	6	6	Green	A6-17
5 -	11	Yellow	25	25	Yellow	A6-T
6 +	J	Red	7	7	Red	A6-16
6 -	8	Brown	26	26	Brown	A6-S
7 +	K	Green	8	8	Green	A6-15
7 -	9	Black	27	27	Black	A6-R
8 +	P	Brown	9	9	Brown	A7-22
8 -	13	Green	28	28	Green	A7-Y
9 +	U	Red	10	10	Red	A7-21
9 -	17	Black	29	29	Black	A7-X
10 +	R	Blue	11	11	Blue	A7-20
10 -	14	Black	30	30	Black	A7-W
11 +	S	Orange	12	12	Orange	A7-19
11 -	15	Black	31	31	Black	A7-V
12 +	V	Brown	13	13	Brown	A7-18
12 -	18	Black	32	32	Black	A7-U
13 +	Z	Blue	14	14	Blue	A7-17
13 -	22	Red	33	33	Red	A7-T
14 +	W	Black	15	15	Black	A7-16
14 -	19	Yellow	34	34	Yellow	A7-S
15 +	X	Green	16	16	Green	A7-15
15 -	20	Red	35	35	Red	A7-R

* twisted pairs

Table C-2 Discrete Cable (1W4) Wiring List

Signal Analog #	Cable 1W2 or 1W3 EAI Connector Pin #	Wire Color	Connector J2 or J3 Pin #	Cable 2W2 or 2W3 Connector P2 or P3 Pin #	Wire Color	A9 or A11 Pin #
0+	1-A	Yellow	1	1	Yellow	22
0-	1-C	Red	20	20	Red	Y
1+	1-L	Red	2	2	Red	21
1-	1-N	White	21	21	White	X
2+	1-U	Blue	3	3	Blue	20
2-	1-X	Black	22	22	Black	W
3+	1-B	Brown	4	4	Brown	19
3-	1-E	Red	23	23	Red	V
4+	1-M	Black	5	5	Black	18
4-	1-R	Green	24	24	Green	U
5+	1-W	Blue	6	6	Blue	17
5-	1-Y	Red	25	25	Red	T
6+	2-A	Green	7	7	Green	16
6-	2-C	Red	26	26	Red	S
7+	2-L	Black	8	8	Black	15
7-	2-N	White	27	27	White	R
8+	2-U	Black	9	9	Black	14
8-	2-X	Brown	28	28	Brown	P
9+	2-B	Orange	10	10	Orange	13
9-	2-E	Red	29	29	Red	N
10+	2-M	Yellow	11	11	Yellow	12
10-	2-R	Black	30	30	Black	M
11+	2-W	Red	12	12	Red	11
11-	2-Y	Black	31	31	Black	L
12+	3-A	Green	13	13	Green	10
12-	3-C	White	32	32	White	K
13+	3-L	Green	14	14	Green	9
13-	3-N	Yellow	33	33	Yellow	J
14+	3-U	Brown	15	15	Brown	8
14-	3-X	Green	34	34	Green	H
15+	3-B	Green	16	16	Green	7
15-	3-E	Blue	35	35	Blue	F

Table C-3 Analog Cables (1W2 and 2W2 or 1W3 and 2W3) Wiring List

Note: All cables are shielded twisted pair cables. All shields are tied together at J2 or J3 and connected to pin 37 of J2 or J3 respectively. Pin 37 of P2 or P3 and all shields at P2 or P3 are tied together and connected to common.

APPENDIX D

Trunk Listings

Source DAC(1)	Variable/Unit: Scale Factor	Trunk W 10	Trunk V 3B	Destination	Variable/Scaling
MDAC (0)	Empty				
MDAC (1)	YAWO/rad:1.146	W101	V3B1	TR541	YAW/50 deg
MDAC (2)	LRRO/rad:19.1	W102	V3B2	TR542	RL/3 deg
MDAC (3)	WRRO/rad:19.1	W103	V3B3	TR543	WR/3 deg
MDAC (4)	Empty				
MDAC (5)	RPO/rad/sec:.22918	W105	V3B5	TR551	R/250 deg/sec
MDAC (6)	PPIO/rad/sec:.00286	W106	V3B6	TR552	P/-20,000 deg/sec
MDAC (7)	BGDOTO/none:.5	W107	V3B7	TR553	BGDOT/2
MDAC (8)	ALPHAO/rad:2.865	W108	V3B8	TG540	same/20 deg
MDAC (9)	UPIO/ft/sec:.000333	W109	V3B9	TG541	same/3000 ft
MDAC (10)	DUPIO/ft/sec^2:.0005	W10A	V3BA	TG542	same/2000 ft/sec^2
MDAC (11)	VPO/ft/sec:.001	W10B	V3BB	TG543	same/1000 ft/sec
MDAC (12)	WPO/ft/sec:.001	W10C	V3BC	TG550	same/1000 ft/sec
MDAC (13)	RPTCHO/rad/sec:1.146	W10D	V3BD	TG551	same/50 deg/sec
MDAC (14)	RYAWO/rad/sec:1.146	W10E	V3BE	TG552	same/50 deg/sec
MDAC (15)	SIGDYO/rad/sec:1.0	W10F	V3BF	TG553	same/1 rad/sec

Table D-1 CDC 6600 DAC(1) Outputs to EAI-781

Source DAC(2)	Variable/Unit: Scale Factor	Trunk W11	Trunk V36	Destination	Variable/Scaling
MDAC (0)	EPF10/rad:57.3	W110	V360	TR400	EPSQY1/1 deg
MDAC (1)	SIGDZO/rad/sec:1.0	W111	V361	TR401	same/1 rad/sec
MDAC (2)	EYF10/rad:57.3	W112	V362	TR402	EPSQZ1/1 deg
MDAC (3)	RNGF10/none:1.0	W113	V363	TR403	SNRNG1/1
MDAC (4)	Empty				
MDAC (5)	Empty				
MDAC (6)	RCSQO/rad^2:13132.0	W116	V366	TR412	PCSQO/1.25 deg^2
MDAC (7)	PITCHO/rad:1.146	W117	V367	TR413	PITCH/50 deg
MDAC (8)	CEO/none:1.0	W118	V368	TG400	ASPANG/1
MDAC (9)	EYTO/rad:28.648	W119	V369	TG401	EPSIZT/2 deg
MDAC (10)	EPTO/rad:28.648	W11A	V36A	TG402	EPSIYT/2 deg
MDAC (11)	LTRO/rad:19.1	W11B	V36B	TG403	L/3 deg
MDAC (12)	WTRO/rad:57.3	W11C	V36C	TG410	W/1 deg
MDAC (13)	TRPO/rad:.2864	W11D	V36D	TG411	THR/200 deg
MDAC (14)	RANGEO/none:1.0	W11E	V36E	TG412	NRANGE/1
MDAC (15)	QPO/rad:.22918	W11F	V36F	TG413	Q/250 deg/sec

Table D-2 CDC 6600 DAC(2) Outputs to EAI-781

Source	Variable/Scaling	Trunk V 38	Trunk W 43	Destination HISC	Variable
TR440	Empty				
TR441	CAGE/2000	V381	W431	A9-21	Cage Coil
TR442	RCDMOD/8.5	V382	W432	A9-20	Gyro Reference
TR443	SECCO1/5	V383	W433	A9-19	Secondary Reference
TR450	XROSET/1	V384	W434	A9-17	X-Rosette
TR451	YROSET/1	V385	W435	A9-18	Y-Rosette

Table D-3 EAI-781 Outputs to HISC

Source	Variable/Scaling	Trunk V3A	Trunk W00	Destination	Variable/Unit: Scale Factor
TR520	WINGD/1 rad	V3A0	W000	ADC S/H (0)	DWIDATA/rad:1.0
TR521	THEG/50 deg	V3A1	W001	ADC S/H (1)	THEG/rad:.8726
TR522	PSIG/50 deg	V3A2	W002	ADC S/H (2)	PSIG/rad:8726
TR523	PT/200 deg	V3A3	W003	ADC S/H (3)	PHII/rad:3.49
TR530	SINPT/1	V3A4	W004	ADC S/H (4)	SPHII/none:1.0
TR531	COSPT/1	V3A5	W005	ADC S/H (5)	CPHII/none:1.0

Table D-4 EAI-781 Outputs to CDC 6600 ADC(1)

Source	Variable/Scaling	Trunk V30	Trunk V20	Destination	Variable
TG200	PPRIME/18	V308	V208	MV00	X(IN)
TG201	BTACT/50	V309	V209	MV00	Y(IN)
TG202	PPRIME/18	V30A	V20A	MV00	Z(IN)
TG203	BTACT/50	V30B	V20B	MV00	W(IN)
TG210	MRANGE/1	V30C	V20C	MV01	X(IN)
TG211	ASPANG/1	V30D	V20D	MV01	Y(IN)
TG212	MRANGE/1	V30E	V20E	MV01	Z(IN)
TG213	ASPANG/1	V30F	V20F	MV01	W(IN)

Table D-5 EAI-781 Outputs to MVFG (0,1)

Source	Variable	Trunk V21	Trunk V31	Destination	Variable/Scaling
MV00	F1(X,Y)	V210	V310	TR220	RADRFT/1
MV00	F1(Z,W)	V216	V316	TR222	TNDRFT/1
MV01	F1(X,Y)	V218	V318	TG220	TRIMOD/1
MV01	F1(Z,W)	V21E	V31E	TG222	FUV86/1

D-6 MVFG (0,1) Outputs to EAI-781

Source	Variable/Scaling	Trunk V33	Trunk V26	Destination	Variable
TG300	MRANGE/1	V338	V268	MV06 X(IN)	X(IN)
TG301	ASPANG/1	V339	V269	MV06 Y(IN)	Y(IN)
TG302	SMRNG1/1	V33A	V26A	MV06 Z(IN)	Z(IN)
TG303	ASPANG/1	V33B	V26B	MV06 W(IN)	W(IN)

Table D-7 EAI-781 Outputs to MVFG (6,7)

Source	Variable	Trunk V27	Trunk V34	Destination	Variable/Scaling
MV06	F1(X,Y)	V270	V340	TR320	FIRRCT/1
MV06	F1(Z,W)	V276	V346	TR322	FLRINT/1

Table D-8 MVFG (6,7) Outputs to EAI-781

Source HISC	Variable	Trunk V43	Trunk V39	Destination	Variable/Scaling
A11-22	Empty				
A11-21	Wing Command	V431	V391	TR501	EEWICD/25
A11-20	Precession	V432	V392	TR502	PRECMD/20

Table D-9 HISC Outputs to EAI-781

Source	Variable	Trunk V83	Trunk U90	Destination HISC	Variable
TG16	CLRBB	V830	U900	A6-22,Y	Clear
TG17	GAGEBB	V831	U901	A6-21,X	Cage
TG18	LNCHBB	V832	U902	A6-20,W	Launch
TG19	OSCON	V833	U903	A6-19,V	Run Oscillograph

Table D-10 EAI-781 Logic Outputs to HISC

Source	Variable	Trunk V81	Trunk W52	Destination	Variable
TG12	ABORT	V81C	W52C	IDS SENSE LINE (12)	INDIS
TG13	FOVLIM	V81D	W52D	IDS SENSE LINE (13)	INDIS
TG14	Empty				
TG15	ALINIT	V81F	W52F	IDS SENSE LINE (15)	INDIS

Table D-11 EAI-781 Logic Outputs to CDC 6600 Input Discretes

Source	Variable	Trunk W62	Trunk V80	Destination	Variable
ODS Control Line 0	OUTDIS				Empty
ODS Control Line 1	OUTDIS				Empty
ODS Control Line 2	OUTDIS	W622	V802	TO2	LSON1
ODS Control Line 3	OUTDIS				Empty
ODS Control Line 4	OUTDIS				Empty
ODS Control Line 5	OUTDIS				Empty
ODS Control Line 6	OUTDIS				Empty
ODS Control Line 7	OUTDIS				Empty
ODS Control Line 8	OUTDIS	W628	V808	T08	CLEAR
ODS Control Line 9	OUTDIS	W629	V809	T09	RUNOSC
ODS Control Line 10	OUTDIS	W62A	V80A	T010	UNCAGE
ODS Control Line 11	OUTDIS				Empty
ODS Control Line 12	OUTDIS	W62C	V80C	T012	STOP
ODS Control Line 13	OUTDIS	W62D	V80D	T013	BORECLR
ODS Control Line 14	OUTDIS	W62E	V80E	T014	LAUNCH
ODS Control Line 15	OUTDIS	W62F	V80F	T015	INITLZ

Table D-12 CDC 6600 Logic Output Discretes to EAI-781

APPENDIX E

Tektronix 8002a EBA Diagnostic Programs
(Flowcharts, Command Files, and Program Listings)

- PROM Memory to 8002a Memory Transfer
- PROM Memory Verification Against 8002a Diskette File
- Synthesized Error Signal DACs' Tests
- Automatic Gain Control (AGC) Tests
- RAM Memory Tests

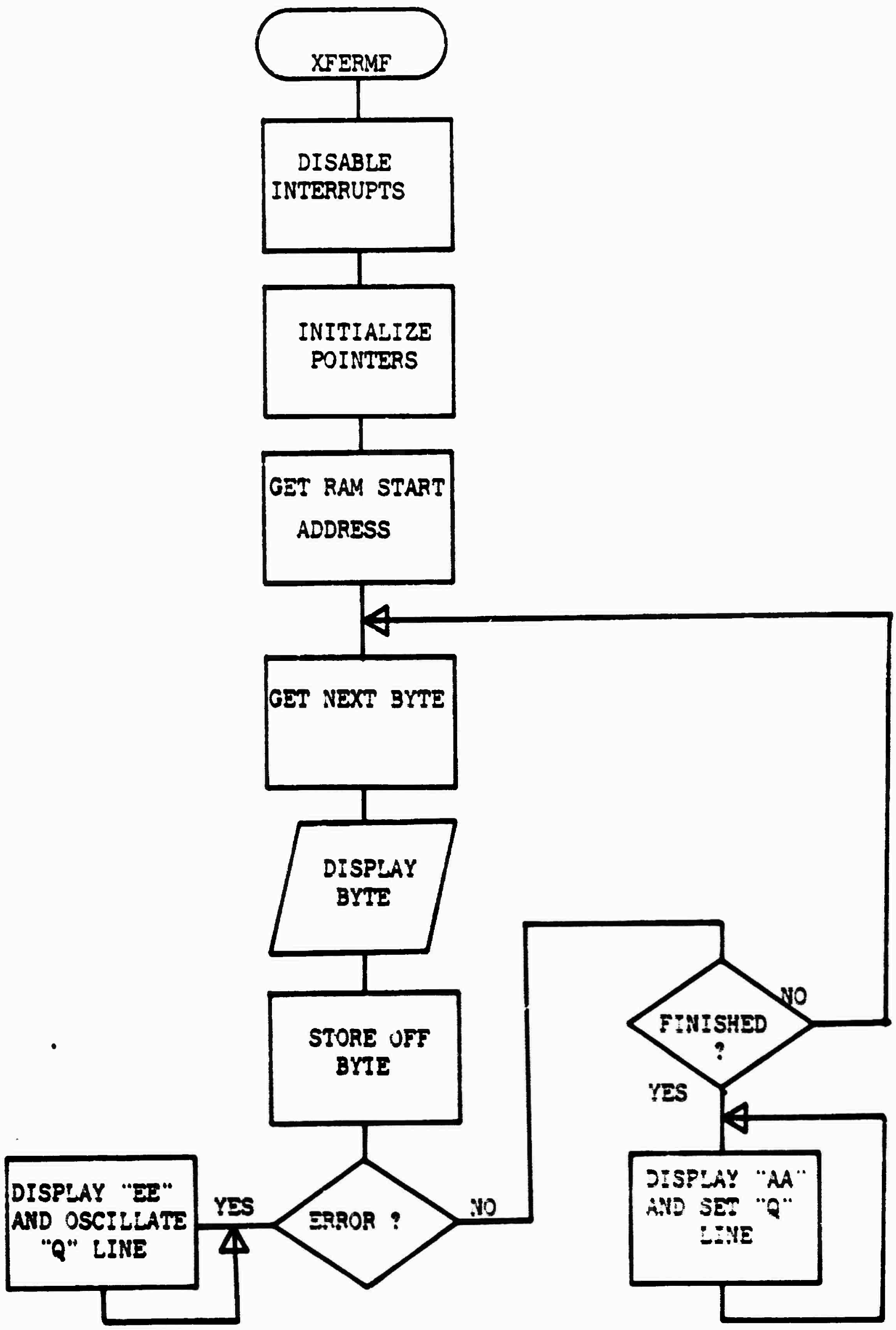

Figure E-1 EBA PROM Memory to 8002a Memory Transfer Diagnostic Program

```
* THIS IS A ROUTINE TO TRANSFER
* FROM MEMORY FROM THE BREAD BOARD
* TO THE 8002a. TO RUN THE FROGRAM
* THE FOLLOWING FARAMETERS MUST BE
* FASSED TO THE FROGRAM
*
*  1> THE LAST ADDRESS OF THE FROM
*     TO BE COFIED
*  2> THE FIRST ADDRESS OF RAM TO
*     BE COFIED TO
*
* TO PASS THE ARGUMENTS,TYFE THE
* FOLLOWING:
*
* INS2TX/1 [LAST ADD FROM] [FIRST ADD RAM]
*
* "INS2TX"-ROUTINE TO PASS ARGUMENTS AND
* EXECUTE "XFERMF;0/1".
*
PATCH FFFC $1$2
LOAD XFERMF;0/1
EM 1
DEB
RES
* TRANSFER NOW ACTIVE
GO 8000
```

```
;THIS ROUTINE TRANSFERS THE CONTENTS OF THE PROMS ON WAFER #5 TO AN AREA
;IN MEMORY, WITH AN AUTOMATIC VERIFICATION SEQUENCE, FOR TRANSFERRAL TO A
;DISK FILE. THE FOLLOWING PARAMETERS MUST BE PASSED BY THE USER:
;
;       MEMORY ADDRESS              PARAMETER
;       --------------              ----------------------------------
;         FFFC                      THE LAST ADDRESS OF ROM (BREADBOARD)
;                                   ROUTINE PROGRAM
;         FFFE                      FIRST ADDRESS OF RAM TO COPY ROMS TO
;
;THE ROUTINE RETURNS WITH THE FOLLOWING IF THE VERIFICATION WAS A SUCCESS:
;       1) "AA" IS DISPLAYED ON "HS WRITE" AND "IR ABC" DISPLAY PANELS, MAY
;               BE "XA" IN SOME DEGENERATE CASES (OK THOUGH)
;       2) THE Q LINE WILL BE SET AT A CONSTANT 5 VOLTS. THIS MAY BE MONITORED
;               ON PIN 57 OF THE BREADBOARD FRONT PANEL
;
;THE ROUTINE ASSUMES THAT THE FIRST ADDRESS OF ROM IS 0000. THE PROMS TO BE
; VERIFIED AGAINST SHOULD BE IN WAFER #5 PROM SLOTS
;
        ORG     8000H
BGN     DIS                     ;DISABLE ALL INTERRUPTS
        BYTE    00H
        LDI     #0FAH
        PLO     RA
        LDI     #00
        PHI     R4
        PLO     R4
        REQ                     ;RESET Q-LINE
        SEX     R4              ;INITIALLY 0000,ROM POINTER
        LDI     #0FFH
        PHI     R1
        PHI     R2
        PHI     RA
        LDI     #0FEH           ;R1=FFFE
        PLO     R1              ;R1 IS THE RAM BUFFER AREA POINTER
        LDI     #0FCH           ;R2=FFFC
        PLO     R2              ;R2 IS THE LAST ADDRESS OF THE ROM ROUTINE
        LDN     R1
        PHI     R3              ;R3 WILL POINT TO  SPECIFIED RAM ADDRESS FOR TRANSFER
        INC     R1
        LDN     R1
        PLO     R3              ;R3 POINTS TO FIRST BYTE OF RAM BUFFER
READ    SEX     R4              ;ROM POINTER
        LDX
WRITE   OUT     7               ;DISPLAY ON "HS WRITE"
        DEC     R4
        STR     R3              ;STORE BYTE TO RAM LOCATION R3
VERIF   LDN     R3              ;VERIFY CORRECT BYTE
        SM
        BNZ     ERR
        BNF     ERR
        LDI     #00
        ADI     #00             ;CLEAR DF FLAG
        LDI     #0FCH
        PLO     R2
        SEX     R2
        GHI     R4
        SM
        BNZ     ZERO
        BNF     ZERO
        INC     R2
        GLO     R4
        SM
        BNZ     ZERO
```

```
        SHL
        BNZ     ZERO
        BNF     ZERO
        BR      FINE
ZERO    LDI     #00H
        ADI     #00
        INC     R1
        INC     R3      ;NOT DONE YET POINT TO NEXT LOCATION
        INC     R4
        BR      READ
FINE    SEX     R0
OUTS    OUT     7
        BYTE    0AAH    ;OUTPUT BYTE OT WS DISPLAY
        SEQ             "WS WRITE" DISPLAY WILL HAVE "AA" IF SUCCESSFUL VERIFY
        OUT     2       ;SO WILL "UV AGC"
        BYTE    0AAH    ;TO UV AGC
        BR      OUTS    ;LOOP FOREVER (Q SET,SUCCESS)
ERR     SEX     R4
        GHI     R4
        STR     RA      ;FFFA=MSB OF BAD ADDRESS
        INC     RA
        GLO     R4
        STR     RA      ;FFFB=LSB OF BAD ADDRESS
ER1     SEX     R0
        SEQ             ;Q=50% DUTY CYCLE IF NOT SUCCESSFULL
        NOP
        NOP
        NOP
        SEX     R4      ;POINT TO BAD BYTE
        OUT     3       ;UV AGC=BAD BYTE
        DEC     R4
        SEX     R0
        OUT     2       ;"UV AGC" DISPLAYS "EE" IF NOT SUCCESSFULL
        BYTE    0EEH    ;ERROR MESSAGE
        OUT     7       ;SO DOES "WS WRITE"
        BYTE    0EEH
        REQ
        BR      ER1
        END     BGN
```

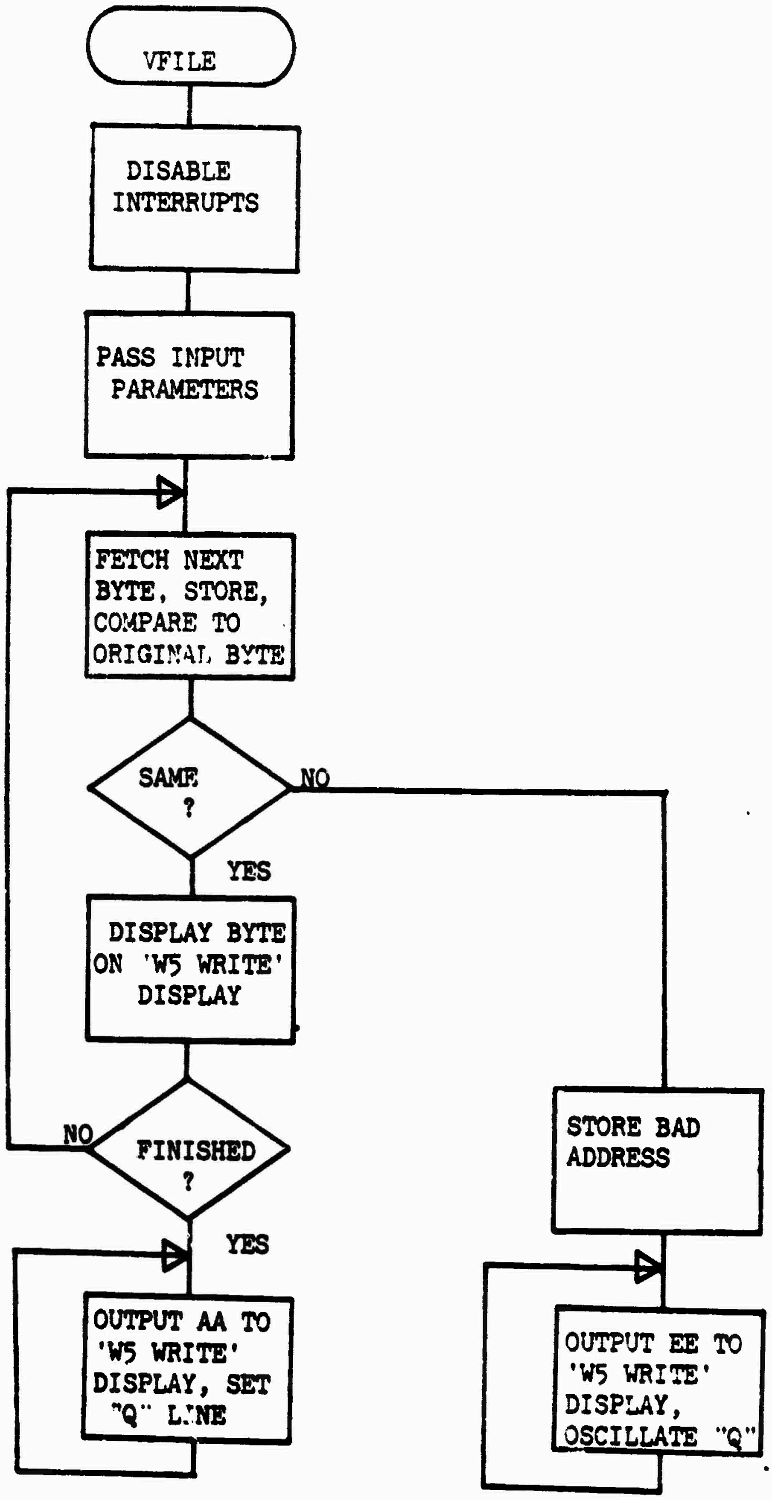

Figure E-2 EBA PROM Memory Verification Against 8002a Diskette File Diagnostic Program

```
* THIS IS A ROUTINE WHICH VERIFIES AN
* EXISTING DISK FILE AGAINST THE CON-
* TENTS OF THE PROMS  IN THE WAFER #5
* PROM SOCKETS. THE PROGRAM REQUIRES
* THE EMULATOR TO BE ATTACHED TO  THE
* PROCESSOR SOCKET OF WAFER 5.
* THE FOLLOWING PARAMETERS MUST BE PAS-
* SED TO THE PROGRAM:
* 1> FILE NAME OF EXISTING FETCH FILE
*     TO VERIFY AGAINST
* 2> LAST ADDRESS OF PROM TO BE CHECKED
* 3> FIRST ADDRESS OF RAM TO VERIFY
*
* TO PASS THESE ARGUMENTS, TYPE:
* INS2VF/1 [NAME] [LST ADD] [FIRST ADD RAM]
```

```
* "INS2VF" VERIFY FILE ROUTINE
FETCH $1
PATCH FFFC $2$3
LOAD VFILE;0/1
EM 1
DEB
RES
* VFILE;0 NOW EXECUTING
[illegible] 3000
```

```
;THIS ROUTINE CHECKS PROMS AGAINST THE CONTENTS OF A DISK FILE FOR USE
;WITH THE STINGER/POST BREADBOARD WAFERS #4 AND #5. THE FETCH FILE CON-
;TAINING THE OBJECT CODE TO BE VERIFIED SHOULD BE LOADED AT AN ADDRESS
;ABOVE 9000H. THE FOLLOWING PARAMETERS MUST BE PASSED:
;
;       MEMORY ADDRESS              PARAMETER
;
;       --------------              ------------------------------------
;         FFFC                      THE LAST ADDRESS OF ROM (BREADBOARD)
;                                   ROUTINE TO WHICH THE DISK FILE IS TO
;                                   BE COMPARED (07FF=W5,03FF=W4)
;         FFFE                      FIRST ADDRESS OF RAM WHERE DISK FETCH
;                                   FILE IS LOCATED
;
;THE ROUTINE RETURNS WITH THE FOLLOWING IF THE VERIFICATION WAS A SUCCESS:
;     1> "AA" IS DISPLAYED ON "WS WRITE" AND "IR AGC" DISPLAY PANELS, MAY
;              BE "XA" IN SOME DEGENERATE CASES (OK THOUGH)
;     2> THE Q LINE WILL BE SET AT A CONSTANT 5 VOLTS. THIS MAY BE MONITORED
;              ON PIN 57 OF THE BREADBOARD FRONT PANEL
;
;THE ROUTINE ASSUMES THAT THE FIRST ADDRESS OF ROM IS 0000. THE PROMS TO BE
; VERIFIED AGAINST SHOULD BE IN WAFER #5 PROM SLOTS
;
        ORG     8000H
BGN     DIS             ;DISABLE ALL INTERRUPTS
        BYTE    00H
        LDI     #0FAH
        PLO     RA
        LDI     #00
        PHI     R4
        PLO     R4
        REQ             ;RESET Q-LINE
        SEX     R4      ;INITIALLY 0000,ROM POINTER
        LDI     #0FFH
        PHI     R1
        PHI     R2
        PHI     RA
        LDI     #0FEH   ;R1=FFFE
        PLO     R1      ;R1 IS THE RAM BUFFER AREA POINTER
        LDI     #0FCH   ;R2=FFFC
        PLO     R2      ;R2 IS THE LAST ADDRESS OF THE ROM ROUTINE
        LDN     R1
        PHI     R3      ;R3 WILL POINT TO  SPECIFIED RAM ADDRESS FOR TRANSFER
        INC     R1
        LDN     R1
        PLO     R3      ;R3 POINTS TO FIRST BYTE OF RAM BUFFER
READ    SEX     R4      ;ROM POINTER
        LDX
WRITE   OUT     7       ;DISPLAY ON "WS WRITE"
        DEC     R4
VERIF   LDN     R3      ;VERIFY CORRECT BYTE
        SM
        BNZ     ERR
        BNF     ERR
        LDI     #00
        ADI     #00     ;CLEAR DF FLAG
        LDI     #0F
        PLO     R2
        SEX     R2
        GHI     R4
        SM
        BNZ     ZERO
        BNF     ZERO
        INC     R2
        GLO     R4
```

```
         SM
         BNF     ZERO
         BR      FINE
ZERO     LDI     #00H
         ADI     #00
         INC     R1
         INC     R3      ;NOT DONE YET POINT TO NEXT LOCATION
         INC     R4
         BR      READ
FINE     SEX     R0
OUT5     OUT     7
         BYTE    0AAH    ;OUTPUT BYTE OT WS DISPLAY
         SEQ             "WS WRITE" DISPLAY WILL HAVE "AA" IF SUCCESSFUL VERIFY
         OUT     2       ;SO WILL "UV AGC"
         BYTE    0AAH    ;TO UV AGC
         BR      OUT5    ;LOOP FOREVER (Q SET,SUCCESS)
ERR      SEX     R4
         GHI     R4
         STR     RA      ;FFFA=MSB OF BAD ADDRESS
         INC     RA
         GLO     R4
         STR     RA      ;FFFB=LSB OF BAD ADDRESS
ER1      SEX     R0
         SEQ             ;Q=50% DUTY CYCLE IF NOT SUCCESSFULL
         NOP
         NOP
         NOP
         SEX     R4      ;POINT TO BAD BYTE
         OUT     3       ;UV AGC=BAD BYTE
         DEC     R4
         SEX     R0
         OUT     2       ;"UV AGC" DISPLAYS "EE" IF NOT SUCCESSFULL
         BYTE    0EEH    ;ERROR MESSAGE
         OUT     7       ;SO DOES "WS WRITE"
         BYTE    0EEH
         REQ
         BR      ER1
         END     BGN
```

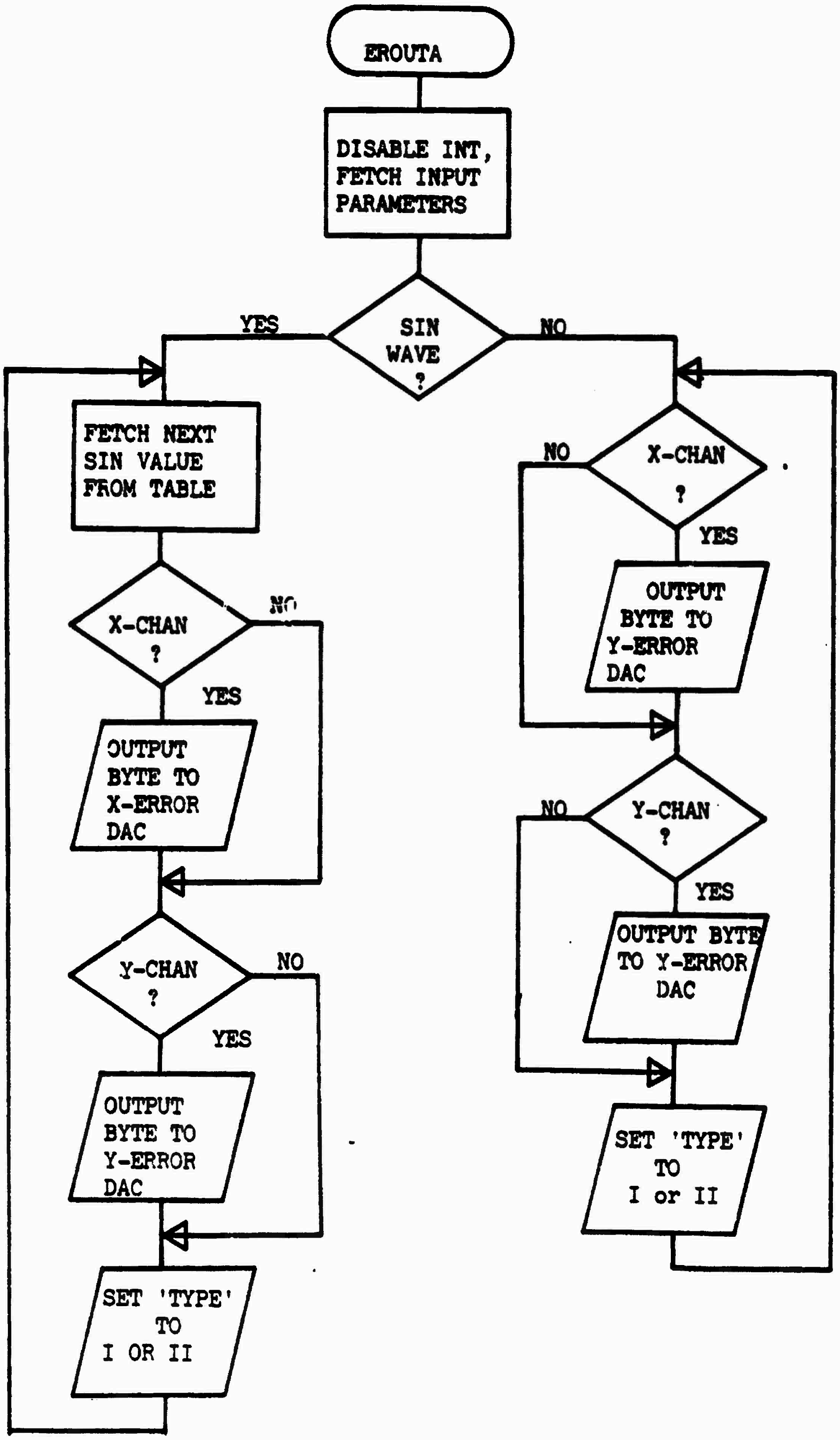

Figure E-3 EBA Synthesized Error Signal DACs Tests Diagnostic Program

```
* THIS IS A WAFER 4 DAC CHECK PROGRAM
* WRITTEN TO :
*    A) OUTPUT A FIXED VALUE TO BOTH
*       X AND Y CHANNELS
* OR B) OUTPUT A SINUSOIDAL WAVE AT A
*       PRESET FREQUENCY TO ONE OR BOTH
*       THE CHANNELS
*
* IN ORDER TO RUN THE PROGRAM, THE FOLLOWING
* DATA SHOULD BE ENTERED (DELIMITED BY SPACES)
*  [TYPE (0/1)] [FREQUENCY FACTOR] [CHANNELS (0=X&Y,1=X,2=Y)]
*  [00=FIXED OUTPUT VALUE,01=SIN CURVE] [VALUE OF FIXED OUTPUT]
*
* TO PASS THE ARGUMENTS TYPE:
*       INS2ER [ARG] [ARG] [ARG] [ARG] [ARG]
*

* "INS2ER"-ROUTINE TO PASS ARGUMENTS AND EXECUTE
*             "EROUTA;0/1"
PATCH FFFB $1$2$3$4$5
FETCH SINTAB/1
LOAD EROUTA;0/1
DEB
EM 1
RES
* "EROUTA;0/1" NOW EXECUTING
GO 0400
```

```
;THIS ROUTINE OUTPUTS VALUE(S) TO THE X AND/OR Y ERROR DEC  CHANNELS
;OF THE BREADBOARD. THE OUTPUTS MAY BE MONITORED AT THE TEST  POINTS
;ON WAFER #4. THE USER MUST PASS PARAMETERS TO THE PROGRAM AS FOLLOWS:
;          MEMORY LOCATION          BYTE DEFINITION
;          ---------------          ---------------
;             FFFB                  "TYPE" BYTE,0=I,1=II
;             FFFC                  SIN WAVE PERIOD SCALING (0=SHORT,1=LONG)
;             FFFD                  00=X AND Y CHANNELS,01=X CHANNEL,02=Y CHANNEL
;             FFFE                  00=FIXED VALUE OUTPUT,01=SIN WAVE OUTPUT
;             FFFF                  FIXED VALUE TO OUTPUT (00-FF)
;
;THE USER SHOULD ALSO FETCH "SINTAB" BEFORE EXECUTING THE PROGRAM
;
        ORG     0400H
        DIS             ;DISABLE INTERRUPTS
        BYTE    00H
        LDI     #00     ;ZERO OUT REGISTERS
        PLO     R1
        PLO     R2
        PLO     R3
        PLO     R4
        PLO     R5
        PLO     R6
        PLO     R7
        PHI     R1
        PHI     R2
        PHI     R3
        PHI     R4
        PHI     R5
        PHI     R6
        PHI     R7
        LDI     #0FFH   ;PUT FF IN HIGH PART OF REGISTERS
        PHI     R5      ;TO POINT TO PROGRAM PARAMS IN HIGH MEMORY
        PHI     R6
        PHI     R9
        PHI     R2
        PHI     R3
        PLO     R2      ;R2 POINTS TO BYTE TO OUTPUT TO ERROR DAC(S)
        PLO     R7      ;R7 WILL BE THE SIN TABLE BYTE COUNTER
        LDI     #0FEH
        PLO     R6
        LDI     #0FDH
        PLO     R5
        LDI     #0FCH
        PLO     R3      ;R3=FFFC,R5=FFFD,R6=FFFE,R7=FFFF
        LDI     #0FBH
        PLO     R9      ;R9 (FFFB) POINTS TO "TYPE SWITCH" (0=I,1=II)
        LDI     #03H
        PHI     R4      ;R4 (0300) POINTS TO SIN TABLE (FROM FETCH FILE "SINTAB")
BGN     SEX     R9      ;POINTS TO TYPE SWITCH
        OUT     6       ;OUTPUTS [FFFB] TO PORT 6 (SETS TYPE)
        DEC     R9      ;STILL POINTS TO FFFB
        SEX     R0
        LDN     R5      ;0 IF X AND Y CHANNELS USED
        BZ      XNY
        SDI     01H
        BZ      JUSX    ;1 IF JUST X CHANNEL USED
        BR      JUSY    ;MUST BE Y CHANNEL ONLY
JUSY    LDN     R6      ;FIXED VAL=00,SIN=01
        BZ      FIXD    ;GO IF FIXED OUTPUT REQUESTED
        SDI     01H
        BNZ     ERROR   ;IF NOT 1 OR 0
SINO    SEX     R4      ;SIN WAVE OUTPUT TO Y CHANNEL
        LDN     R3      ;DELAY FACTOR (00-FF) CHANGES PERIOD OF SIN WAVE
```

```
        PLO     R8      ;PUT VAL INTO R8
LP1     OUT     2       ;OUTPUT SIN TO Y CHANNEL
        DEC     R4      ;POINT TO SAME BYTE
        SEX     R9
        OUT     6       ;REFRESH "TYPE" SWITCH
        DEC     R9      ;POINT TO SAME BYTE
        SEX     R4      ;BACK TO SIN TABLE POINTER
        GLO     R8      ;DELAY
        BZ      NEXTS
        DEC     R8
        BR      LP1
NEXTS   INC     R4      ;POINT TO NEXT SIN VALUE
        LDN     R3      ;GET DELAY BACK INTO R8
        PLO     R8
        DEC     R7      ;SIN TABLE COUNTER
        GLO     R7
        BZ      RE7     ;RESTORE SIN POINTER TO 0300
        BR      LP1
RE7     LDI     #03H
        PHI     R4
        LDI     #00
        PLO     R4
        LDI     #0FFH
        PLO     R7      ;RESTORE DEC COUNTER
        LDN     R3      ;GET DELAY AGAIN
        PLO     R8
        BR      LP1     ;STARTS COUNT BYTE OF SIN TABLE OVER
FIXO    LDN     R2      ;FIXED VALUE OUTPUT,R2 POINT TO BYTE TO OUTPUT
        SEX     R2      ;POINTS TO BYTE TO OUT
LP2     OUT     2       ;OUTS BYTE TO Y
        DEC     R2      ;POINT TO SAME BYTE
        SEX     R9
        OUT     6       ;REFRESH "TYPE"
        DEC     R9
        SEX     R2
        BR      LP2     ;LOOP FOREVER
JUSX    LDN     R6      ;SAME AS BEFORE
        BZ      FIX1
        SDI     01H
        BNZ     ERROR
SIN1    SEX     R4      ;SIN TABLE
        LDN     R3      ;DELAY
        PLO     R8
LP3     OUT     1       ;X SIN OUT
        DEC     R4      ;POINT TO SAME BYTE
        SEX     R9
        OUT     6
        DEC     R9
        SEX     R4
        GLO     R8      ;CHECK DELAY
        BZ      NEXTT   ;GET NEXT BYTE IF THROUGH
        DEC     R8
        BR      LP3
NEXTT   INC     R4
        LDN     R3
        PLO     R8
        DEC     R7
        GLO     R7
        BZ      RF7
        BR      LP3
RF7     LDI     03H
        PHI     R4
        LDI     00
        PLO     R4
        LDI     0FFH
        [illegible] [illegible]7
```

```
        LDN     R3
        PLO     R8
        BR      LP3
FIX1    LDN     R2          ;BYTE TO OUTPUT (AT FFFBH)
        SEX     R2
LP4     OUT     1
        DEC     R2          ;POINT TO SAME BYTE
        SEX     R9
        OUT     6
        DEC     R9
        SEX     R2
        BR      LP4         ;LOOP
XNY     LDN     R6          ;SAME AS BEFORE EXCEPT BOTH CHANNELS
        BZ      FIX2
        SDI     01H
        BNZ     ERROR
SIN2    SEX     R4          ;SIN TABLE POINTER
        LDN     R3          ;DELAY
        PLO     R8          ;XFER TO R8
LP5     OUT     1           ;OUT X
        DEC     R4
        OUT     2           ;OUT    Y
        DEC     R4
        GLO     R8
        SEX     R9
        OUT     6
        DEC     R9
        SEX     R4
        BZ      NEXTU
        DEC     R8          ;DEC COUNT
        BR      LP5
NEXTU   INC     R4
        LDN     R3
        PLO     R8
        DEC     R7
        GLO     R7
        BZ      RG7
        BR      LP5
RG7     LDI     03H
        PHI     R4
        LDI     00
        PLO     R4
        LDI     0FFH
        PLO     R7
        LDN     R3
        PLO     R8
        BR      LP5
FIX2    LDN     R2          ;BYTE TO OUT
        SEX     R2
LP6     OUT     1
        DEC     R2
        OUT     2           ;OUT X AND Y
        DEC     R2
        SEX     R9
        OUT     6
        DEC     R9
        SEX     R2
        BR      LP6         ;FOREVER
ERROR   SEQ     ;50% DUTY CYCLE ON Q LINE IF ERROR (SHOULD MONITOR)
        NOP
        NOP
        REQ
        NOP
        NOP
        BR      ERROR
```

```
        ORG     0000H
        DIS
        BYTE    00H
        LDI     00
        PLO     R1
        PLO     R2
        PLO     R3
        PLO     R4
        PHI     R1
        PHI     R2
        PHI     R3
        PHI     R4
        LDI     0FAH            ;00FA=START LOC MSB
        PLO     R5              ;R5=00FA
        LDN     R5              ;GET START LOC MSB
        PHI     R1
        INC     R5
        LDN     R5              ;GET START LOC LSB
        PLO     R1              ;R1 IS CURRENT LOCATION POINTER
        LDI     0FEH            ;00FE   IS MSB OF BAD LOCATION OF FOUND
        PLO     R2
        LDI     0FCH            ;00FC IS THE LAST ADDRES MSB
        PLO     R6              ;INTO R6
BGN     LDI     0FFH
        STR     R1
        LDN     R1
        SDI     0FFH
        BNZ     ERRF
        LDI     00
        ADI     00

        LDI     0AAH
        STR     R1
        LDN     R1
        SDI     0AAH
        BNZ     ERRA
        LDI     00
        ADI     00

        LDI     55H
        STR     R1
        LDN     R1
        SDI     55H
        BNZ     ERR5
        LDI     00
        ADI     00

        LDI     00H
        STR     R1
        LDN     R1
        SDI     00H
        BNZ     ERRO
        LDI     00
        ADI     00

        INC     R1
        SEX     R6
        GHI     R1
        SM                      ;CHECK IF LAST ADDRES MSB

        BNZ     MORE
        INC     Ra
        GLO     R1
        [illegible]
```

```
        BNZ     MORE            ;CHECK IF LAST ADDRESS LSB
        BR      TEND

MORE    LDI     00
        ADI     00
        LDI     OFCH
        PLO     R6              ;RESTORE LAST ADDRESS POINTER
        BR      BGN

ERRF    SEX     RO
        GHI     R1
        STR     R2
        INC     R2
        GLO     R1
        STR     R2
ERRF1   OUT     7
        BYTE    OFFH
        SEQ
        NOP
        NOP
        REQ
        BR      ERRF1

ERRA    SEX     RO
        GHI     R1
        STR     R2
        INC     R2
        GLO     R1
        STR     R2
ERRA1   OUT     7
        BYTE    OAAH
        SEQ
        NOP
        NOP
        REQ
        BR      ERRA1

ERRS    SEX     RO
        GHI     R1
        STR     R2

        INC     R2
        GLO     R1
        STR     R2
ERRS1   OUT     7
        BYTE    O55H
        SEQ
        NOP
        NOP
        REQ
        BR      ERRS1

ERRD    SEX     RO
        GHI     R1
        STR     R2
        INC     R2
        GLO     R1
        STR     R2
ERRD1   OUT     7
        BYTE    [illegible]
```

```
                NOP
                NOP
                REQ
                BR        ERR01

TEND            SEX       R0
                OUT       7
                BYTE      88H
                SEQ
                NOP
                NOP
                BR        TEND
                END       BGN
```

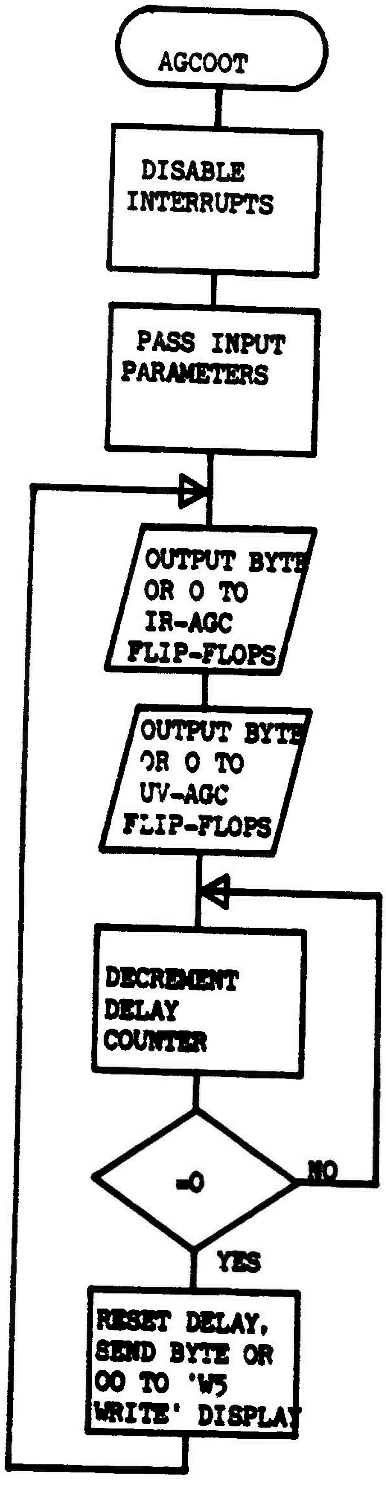

Figure E-4 EBA Automatic Gain Control (AGC) Tests Diagnostic Program

```
* THE 1802 SYSTEM DISK SHOULD BE IN DRIVE 0
*
* THIS IS AN AGC WORD OUTPUT AND FLIP-FLIP PROGRAM
* ITS MAIN USE IS TO OUTPUT A BINARY WORD TO THE
* AGC FLIP-FLOPS ON WAFER 6 AND TOGGLE THE BITS WITH 0
*
* THE FOLLOWING PARAMETERS MUST BE PASSED TO THE PROGRAM
*       A) THE BYTE (IN 2 DIGIT HEX CODE) TO OUTPUT
*       B) THE DELAY FACTOR (2 DIG HEX CODE) OR DUTY CYCLE BYTE
*
* TO PASS THESE ARGUMENTS ENTER THE FOLLOWING COMMAND
*
*       INS2AGC/1 [BYTE] [DELAY]
*

PATCH 00FE $1$2
LOAD AGCOUT;0/1
DEB
EM 1
RES
GO 0000
```

```
;THIS ROUTINE OUTPUTS A KNOWN VALUE TO THE AGC LATCHES ON WAFER 6
;AND TOGGLES THIS VALUE WITH 00 AT A RATE SET BY THE USER.
;THE FOLLOWING PARAMETERS MUST BE SET BY THE USER:
;
;   MEMORY LOCATION           PARAMETER
;   ---------------           ---------------------------------
;     00FF                    LOCATION OF BYTE TO OUTPUT
;     00FE                    LOCATION OF TOGGLE RATE (0=FAST,FF=SLOW)
;
;THE FOLLOWING OUTPUTS ARE GIVEN TO THE USER
;    1> THE BYTE, AS IT IS OUTPUT TO THE LATCHES, IS ALSO SENT TO THE
;       "WS WRITE" DISPLAY
;    2> THE Q LINE WILL TOGGLE +5 AND 0 VOLTS (PIN 57,FRONT PANEL) AS THE
;       BYTE IS TOGGLED ON FLIP FLOPS
;
        ORG     0000H
        DIS
        BYTE    00H
        LDI     00H
        PHI     R1
        PHI     R2
        PHI     R3
        PHI     R4
        PHI     R5
        PHI     R6
        PHI     R7
        PLO     R1
        PLO     R2
        PLO     R3
        PLO     R3
        PLO     R4
        PLO     R5
        PLO     R6
        PLO     R7
BGN     LDI     0FFH
        PLO     R3              ;R3 POINTS TO THE BYTE TO OUTPUT
                                ;AT 0FFH
        LDI     0FEH            ;0FEH IS THE LOCATION OF THE DEC
        PLO     R5              ;R5 POINTS TO DEC BYTE
        LDN     R5              ;GET BYTE
        PLO     R4              ;STORE INTO R4.0
LOOP    SEX     R3              ;BYTE TO OUTPUT
        SEQ                     ;SET Q LINE HIGH
        OUT     2               ;OUTPUT TO IR AGC FFS
        DEC     R3              ;POINTS TO SAME BYTE
        OUT     7               ;OUTPUT BYTE TO WS WRITE DISPLAY
        DEC     R3              ;POINTS TO SAME BYTE
        OUT     3               ;OUT TO UV AGC FFS
        DEC     R3              ;POINTS TO SAME BYTE
        GLO     R4              ;TEST DECREMENT COUNTER
        BZ      OLOOP           ;GO IF FINISHED
        DEC     R4              ;ELSE DECREMENT AND LOOP
        BR      LOOP
OLOOP   LDI     0FEH            ;LOCATION OF COUNT
        REQ                     ;RESET Q LINE (=0)
        PLO     R5              ;R5 POINTS TO DEC BYTE
        LDN     R5              ;GET COUNT IN [D]
        PLO     R4              ;PUT BACK INTO R4
LOOP1   SEX     R0              ;[PC]=[X]
        OUT     2               ;OUTPUT 00 TO IR AGC FFS
        BYTE    00H
        OUT     3               ;OUTPUT 00 TO UV AGC FFS
        BYTE    00H
        OUT     7               ;OUTPUT 00 TO WS WRITE DISPLAY
```

```
BYTE    00H
GLO     R4          ;CHECK COUNTER
BZ      LOOP        ;GO IF DONE
DEC     R4          ;ELSE DEC COUNTER
BR      LOOP1       ;AND LOOP
END     BGN
```

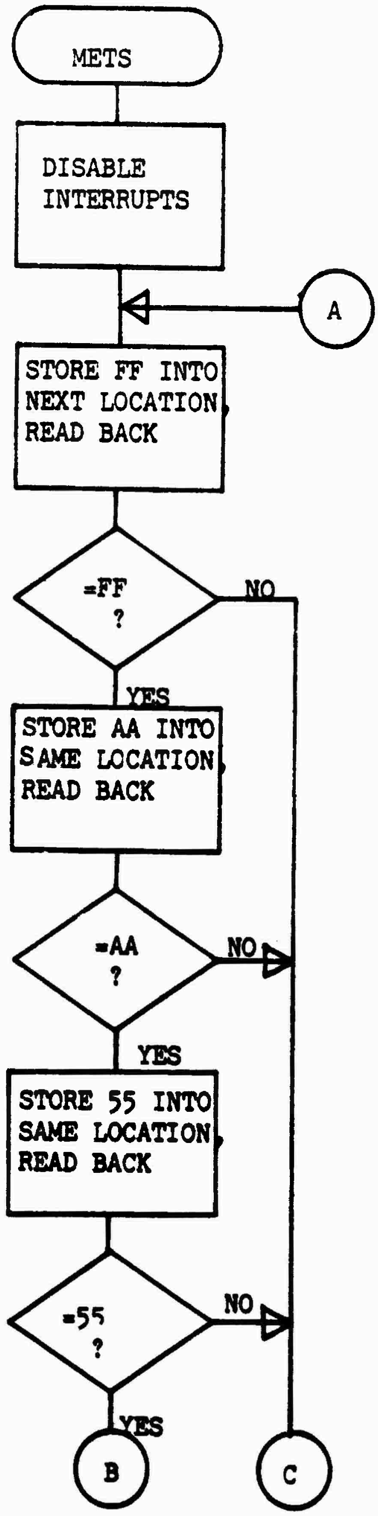

Figure E-5 EBA RAM Memory Tests Diagnostic Program (1 of 2)

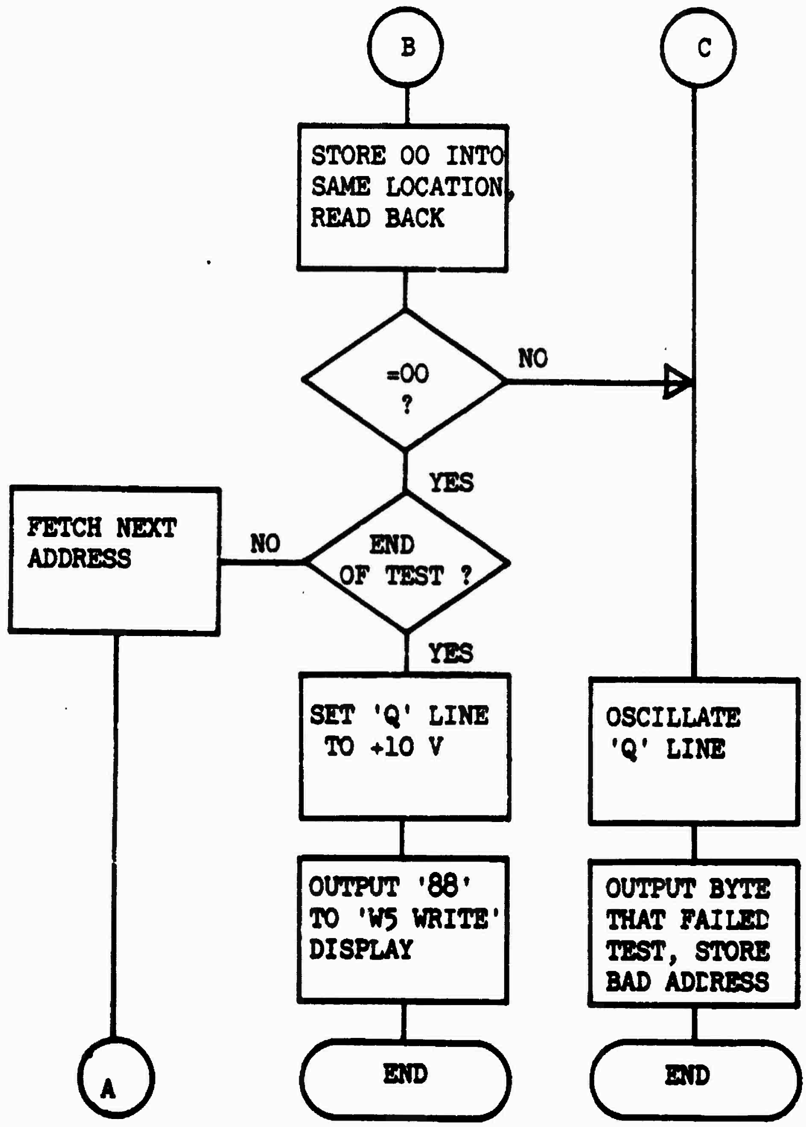

Figure E-5 (Cont'd) EBA RAM Memory Tests Diagnostic Program (2 of 2)

```
* THIS ROUTINE IS USED TO CHECK THE
* BREADBOARD'S ON BOARD MEMORY FOR
* FAULTY LOCATIONS. THE PROGRAM
* REQUIRES NO USER PARAMETERS
* THE Q LINE (PIN 57 OF B/B FRONT
* PANEL) MAY BE MONITORED TO SEE
* WHETHER A BAD LOCATION WAS FOUND.
*
* THE BAD ADDRESS CAN BE SEEN BY
* EXAMINING [OOFE] AND [OOFF] FOR
* THE MSB AND LSB OF THE BAD LOCATION
* IF THE TEST WAS A SUCCESS:
*    1> THE Q LINE (P 57,FRONT PANEL)
*       WILL BE AT "1"
*    2> AN "88" WILL BE ON THE "W5
*       WRITE" DISPLAY
* IF THE TEST WAS A FAILURE:
*    1> THE Q LINE WILL BE OSCILLATING
*       AT ABOUT 50% DUTY CYCLE
*    2> THE "W5 WRITE" WILL DISPLAY
*       AN "FF","AA","55","00"
*
*
*
LOAD METS;0/1
EM 1
DEB
RES
GO 0000
```

```
; THIS IS A ROUTINE TO TEST THE BREADBOARD
; MEMORY (2000-207F). NO PARAMETERS NEED
; TO BE PASSED.
;
; THE PROGRAM RETURNS THE ADDRESS OF ANY
; BAD LOCATION AT [OOFE] [OOFF] (MSB,LSB)
; ,DISPLAYS THE BAD TEST PATTERN, IF ANY,
; AND (1) SETS Q LINE IF EVERYTHING OK,
;  OR (2) TOGGLES Q LINE (50%) IF NO GOOD
;         LOCATION FOUND
;
        ORG     0000H
        DIS
        BYTE    00H
        LDI     00
        PLO     R1
        PLO     R2
        PLO     R3
        PLO     R4
        PHI     R1
        PHI     R2
        PHI     R3
        PHI     R4
        LDI     #20H     ;20=START LOCATION MSB
        PHI     R1
        LDI     #00H
        PLO     R1       ;R1 IS CURRENT LOCATION POINTER
        LDI     OFEH     ;OOFE   IS MSB OF BAD LOCATION OF FOUND
        PLO     R2
BGN     LDI     #OFFH    ;STORE (11111111) BINARY
        STR     R1
        LDN     R1
        SDI     #OFFH    ;SEE IF FF STILL THERE
        BNZ     ERRF     ;GO IF BAD LOCATION
        LDI     00       ;CLEAR CARRY
        ADI     00

        LDI     #OAAH    ;SAME WITH (10101010) BINARY
        STR     R1
        LDN     R1
        SDI     OAAH
        BNZ     ERRA
        LDI     00
        ADI     00

        LDI     #055H    ;AGAIN WITH (01010101) BINARY
        STR     R1
        LDN     R1
        SDI     55H
        BNZ     ERR5
        LDI     00
        ADI     00

        LDI     #00H     ;LAST WITH (00000000) BINARY
        STR     R1
        LDN     R1
        SDI     00H
        BNZ     ERRO
        LDI     00
        ADI     00

        INC     R1
        GLO     R1
        SDI     #07FH    ;SEE IF LAST ADDRESS
```

```
        BZ      TEND
        BNZ     MORE

MORE    LDI     00
        ADI     00          ;CLEAR CARRY
        BR      BGN

ERRF    SEX     RO          ;HERE IF (11111111) NOT GOOD
        GHI     R1          ;SAVE BAD ADDRESS
        STR     R2          ;INTO [FE] [FF]
        INC     R2
        GLO     R1
        STR     R2
ERRF1   OUT     7           ;OUTPUT BAD BYTE TO
        BYTE    #OFFH       ;"WS WRITE" DISPLAY
        SEQ                 ;SET Q LINE =1
        NOP
        NOP
        REQ                 ;RESET Q LINE=0 (50%)
        BR      ERRF1

ERRA    SEX     RO          ;SAME FOR (10101010)
        GHI     R1
        STR     R2
        INC     R2
        GLO     R1
        STR     R2
ERRA1   OUT     7
        BYTE    0AAH
        SEQ
        NOP
        NOP
        REQ
        BR      ERRA1

ERR5    SEX     RO          ;SAME FOR (01010101)
        GHI     R1
        STR     R2

        INC     R2
        GLO     R1
        STR     R2
ERR51   OUT     7
        BYTE    055H
        SEQ
        NOP
        NOP
        REQ
        BR      ERR51

ERRO    SEX     RO          ;AGAIN FOR (00000000)
        GHI     R1
        STR     R2
        INC     R2
        GLO     R1
        STR     R2
ERRO1   OUT     7
        BYTE    00H
        SEQ
        NOP
        NOP
        REQ
```

```
BR          ERR01

TEND        SEX         R0          ;HERE IF ALL OK
OUT         7           ;"W5 WRITE"="88"
BYTE        88H
SEQ                     ;Q LINE STAYS HIGH
NOP
NOP
BR          TEND
END         BGN
```

APPENDIX F

DDS Diagnostic Routines

- OLOOP1 Cycle 2 Flowchart
- OLOOP1 Cycle 3 Flowchart
- Operation Sequence

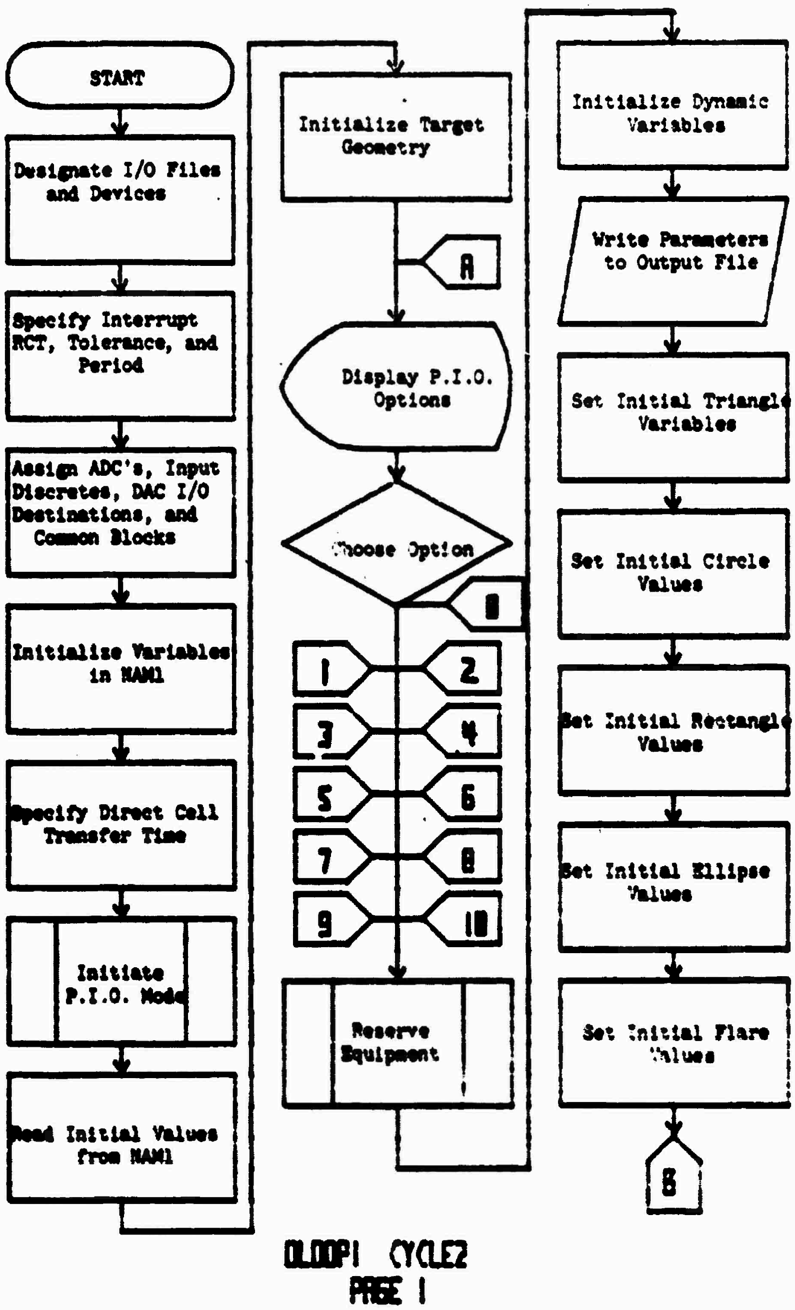

Figure F-1 OLOOP1 Cycle 2 Flowchart (1 of 7)

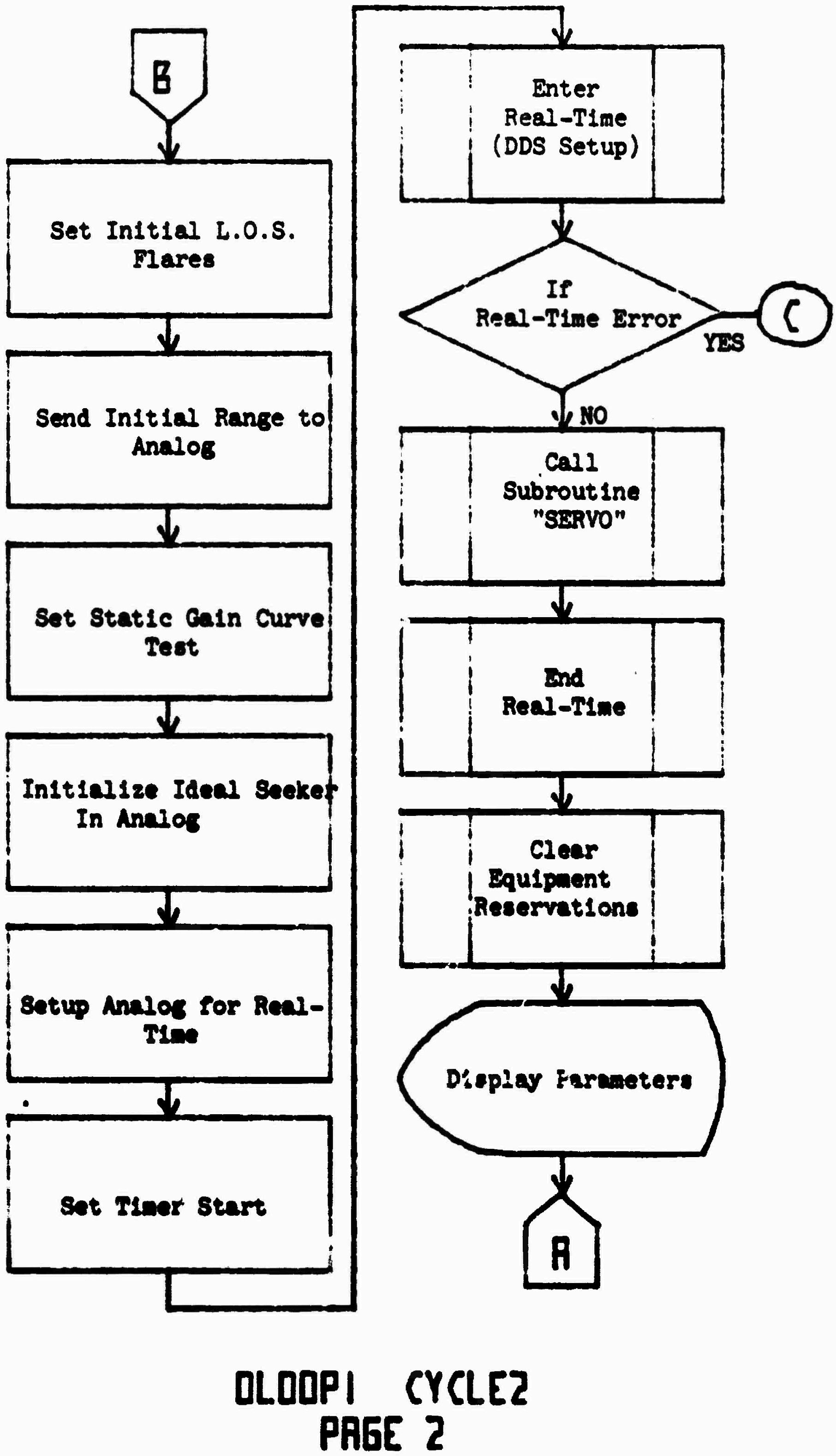

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (2 of 7)

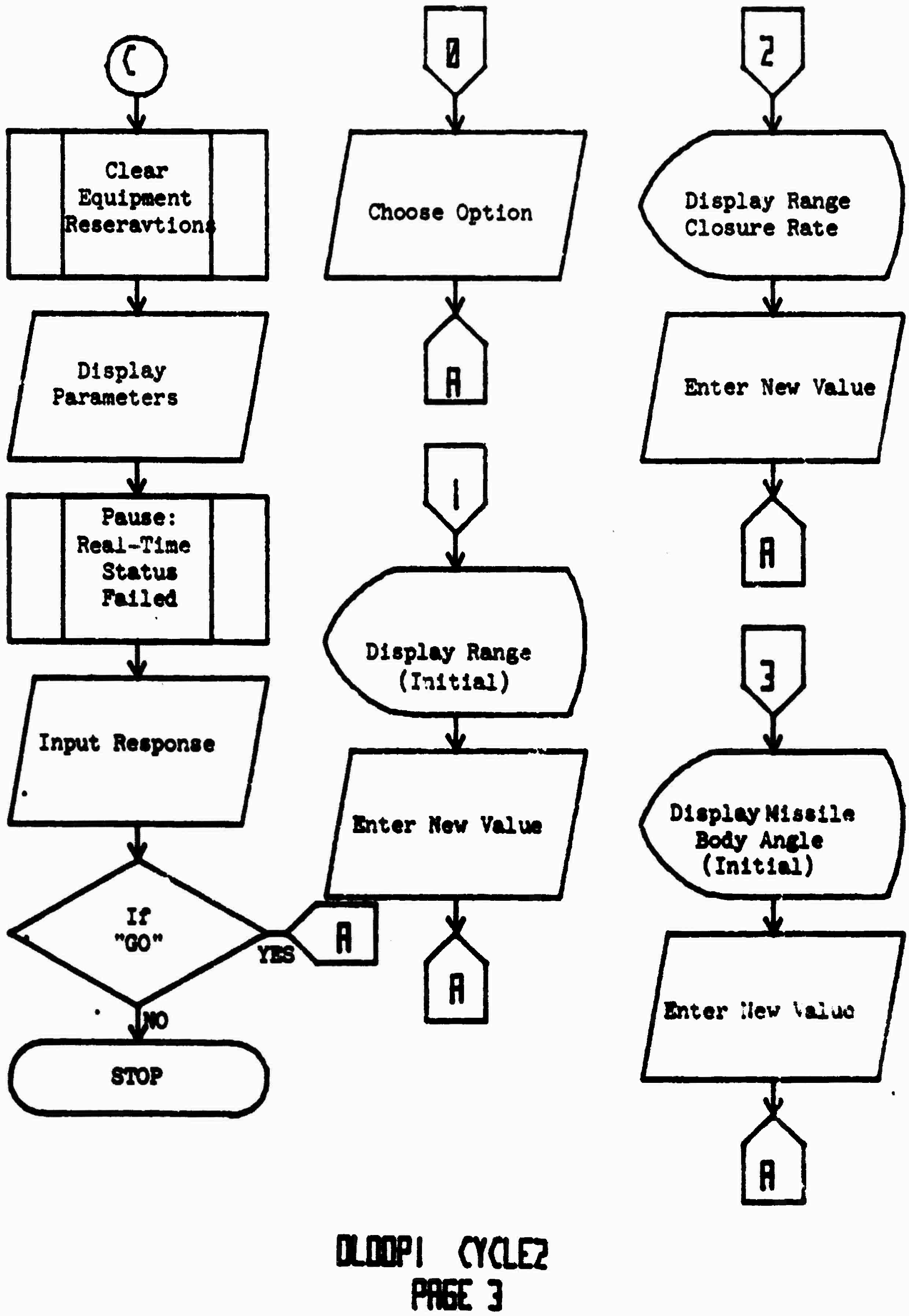

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (3 of 7)

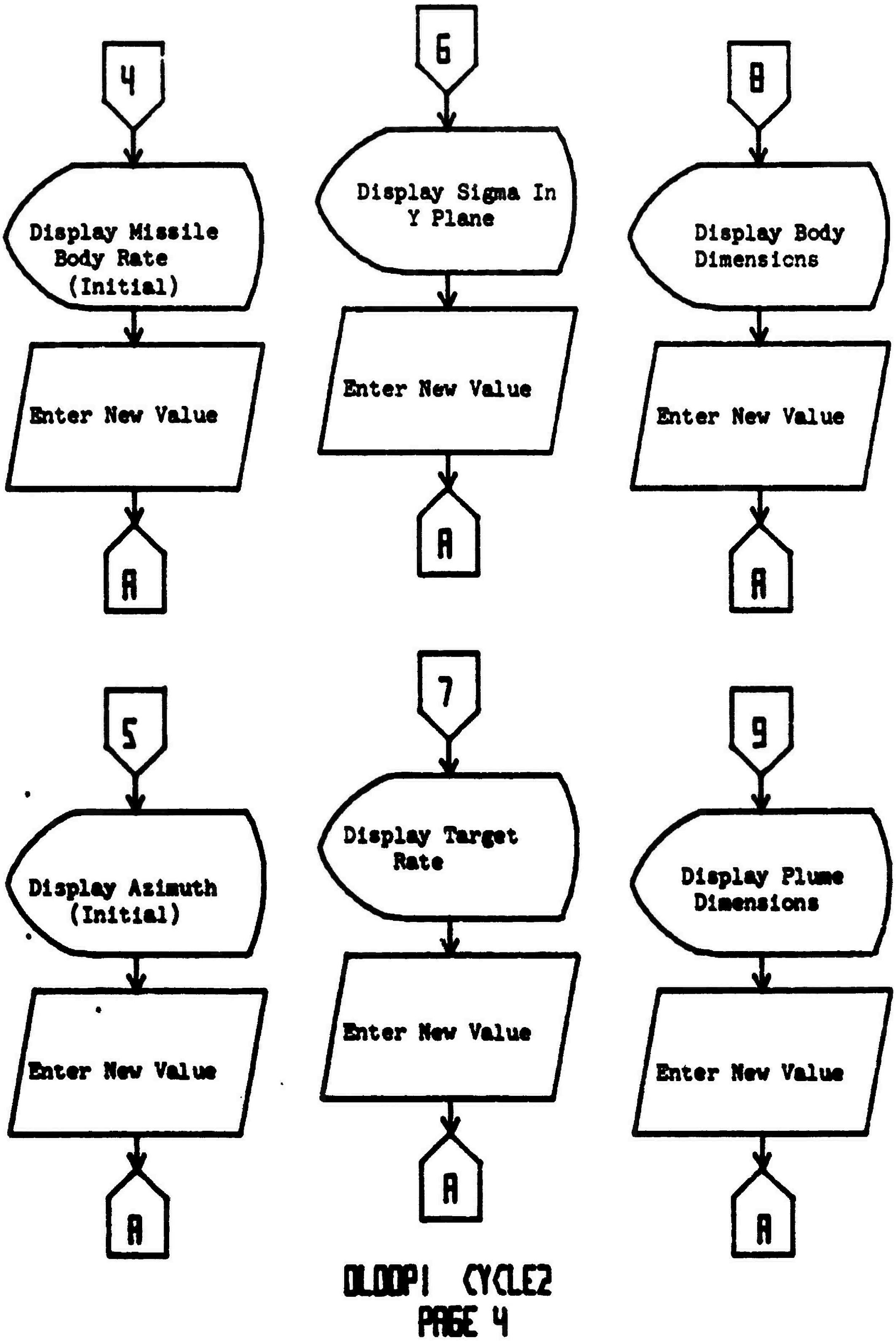

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (4 of 7)

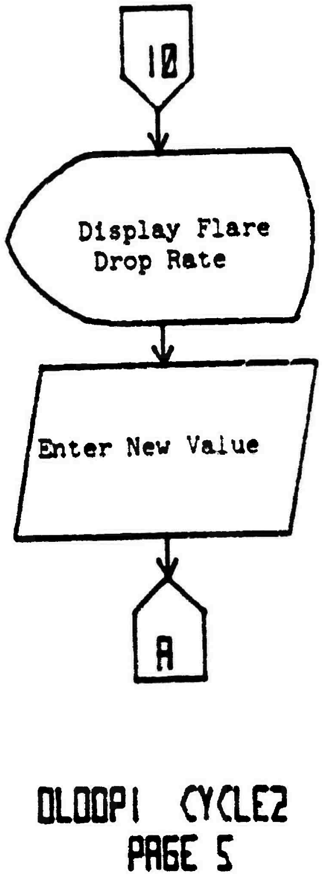

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (5 of 7)

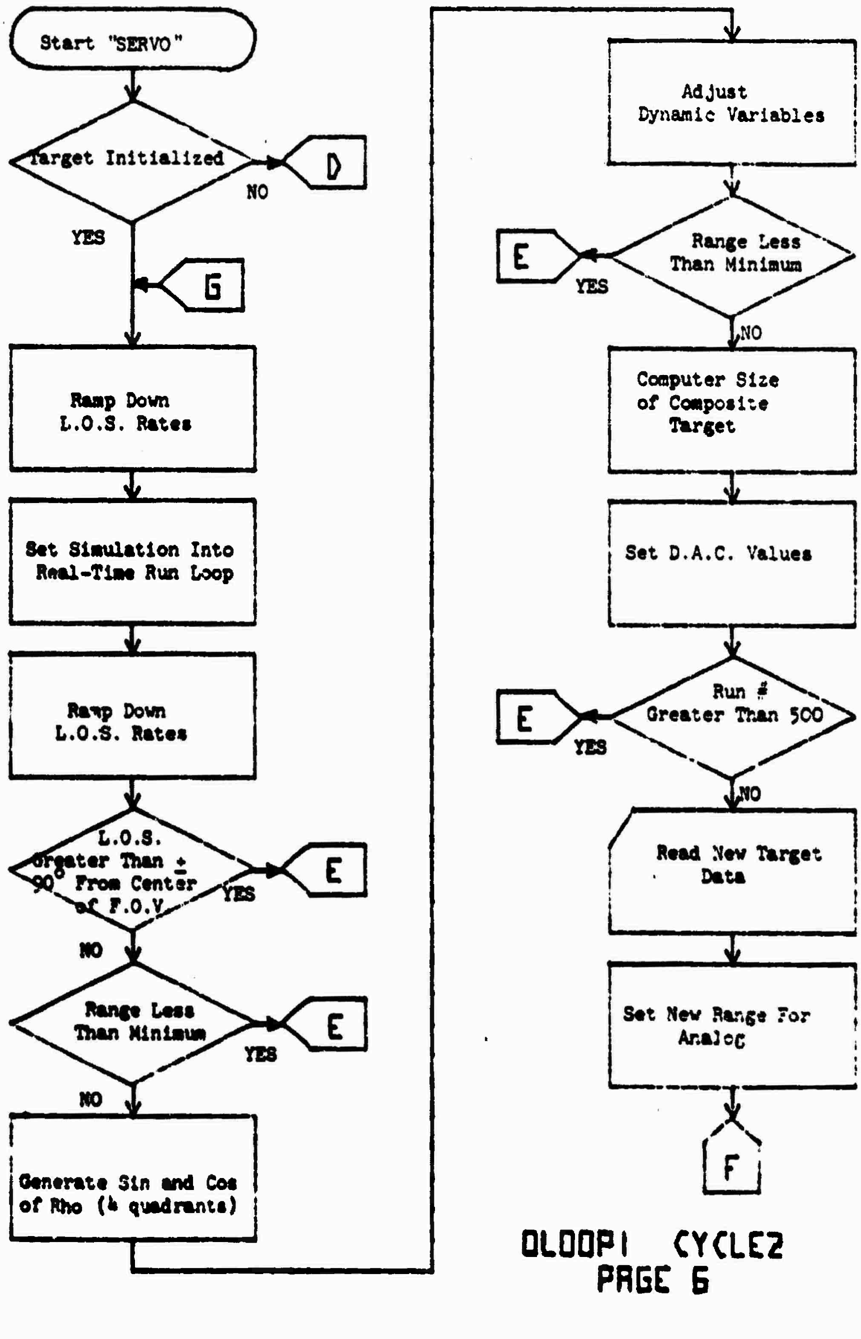

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (6 of 7)

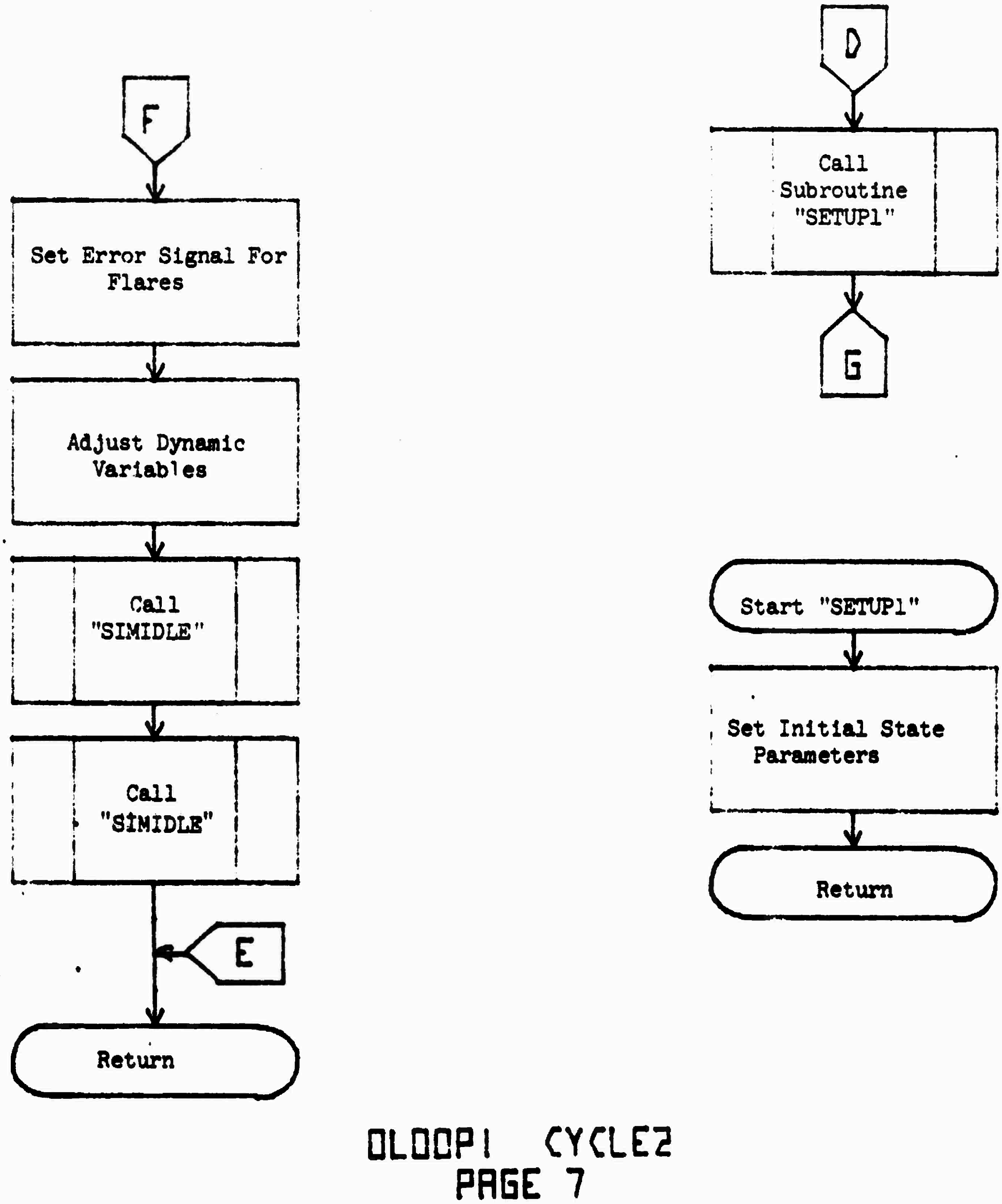

Figure F-1 (Cont'd) OLOOP1 Cycle 2 Flowchart (7 of 7)

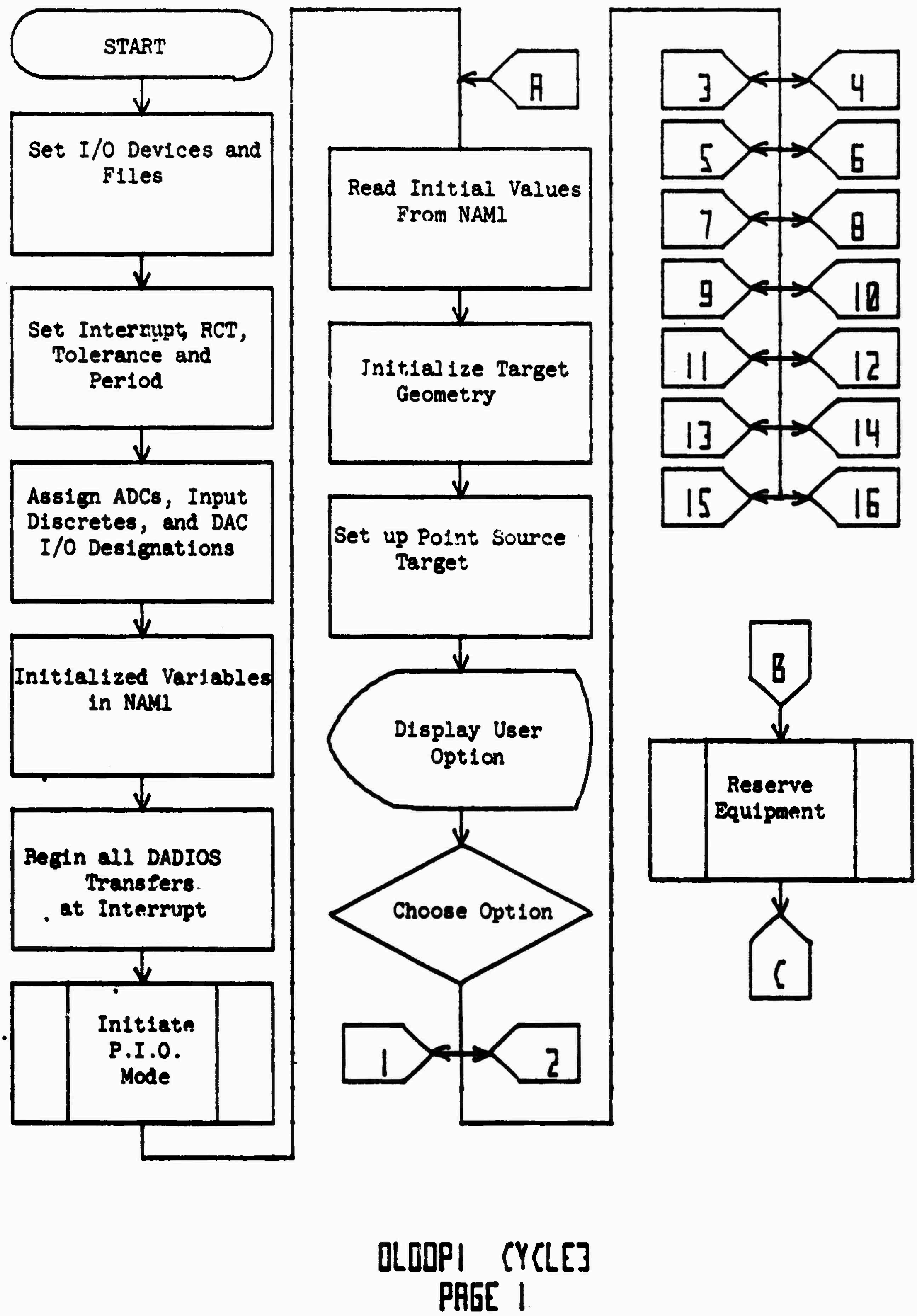

Figure F-2 OLOOP1 Cycle 3 Flowchart (1 of 5)

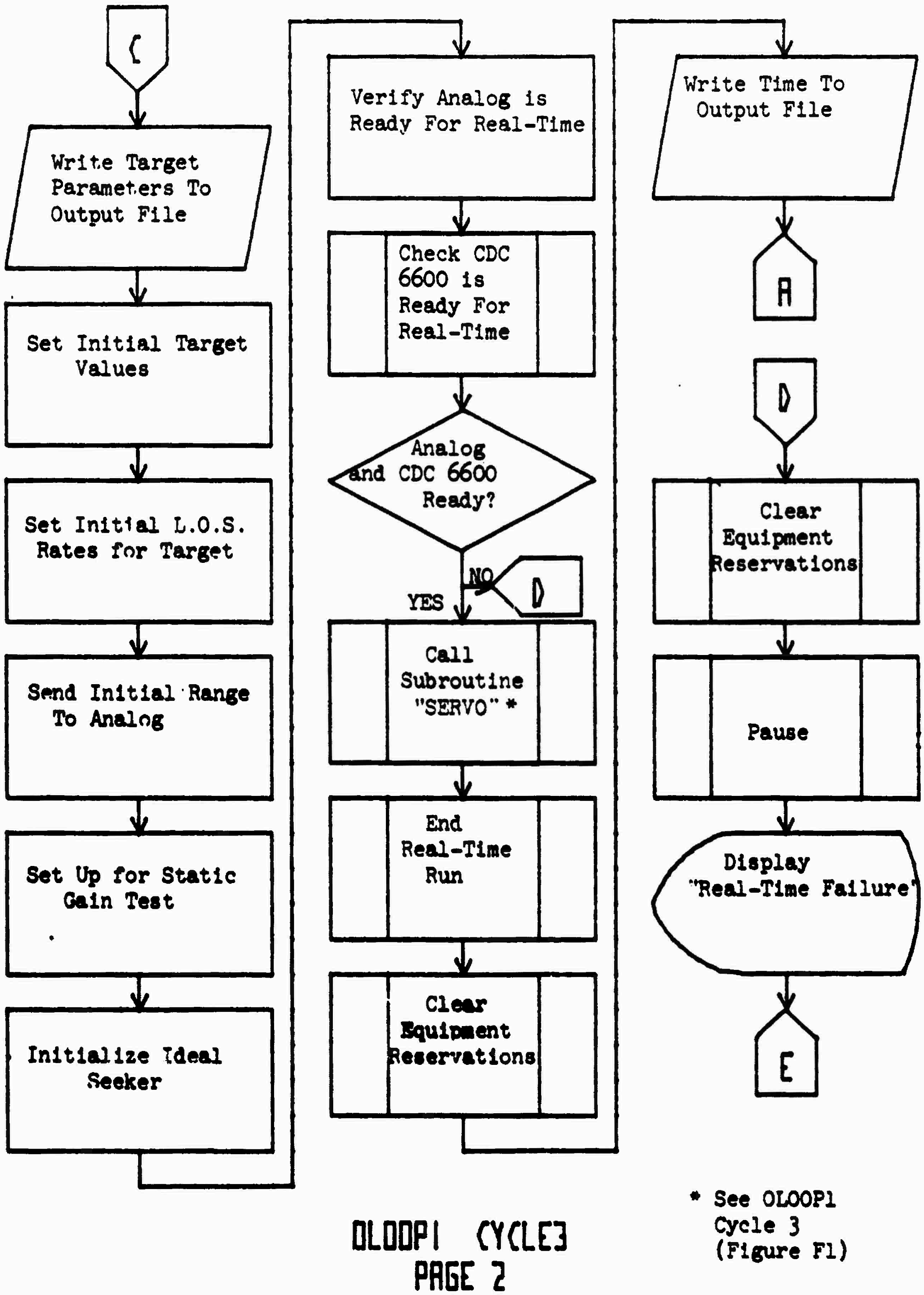

Figure F-2 (Cont'd) OLOOP1 Cycle 3 Flowchart (2 of 5)

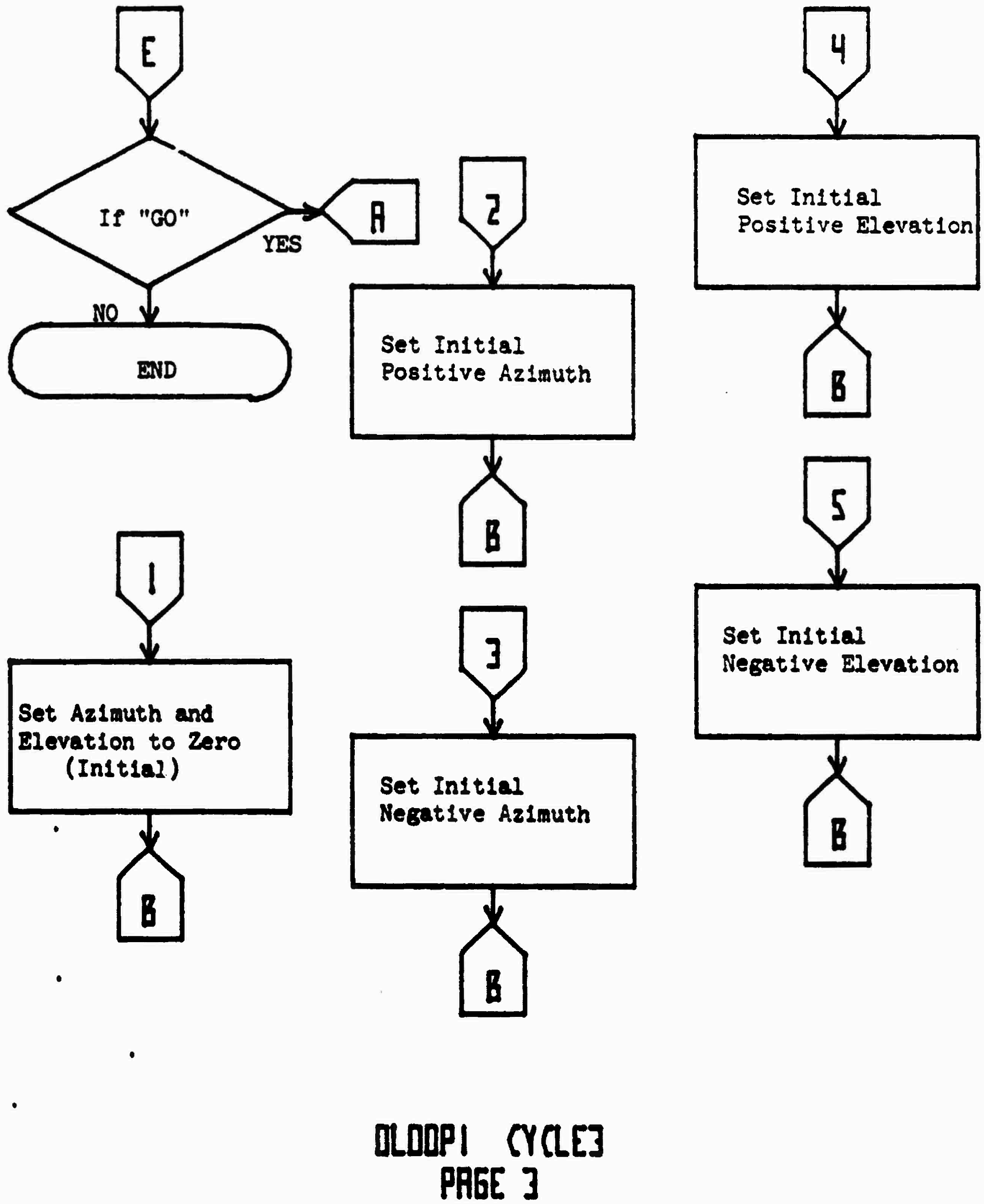

Figure F-2 (Cont'd) OLOOP1 Cycle 3 Flowchart (3 of 5)

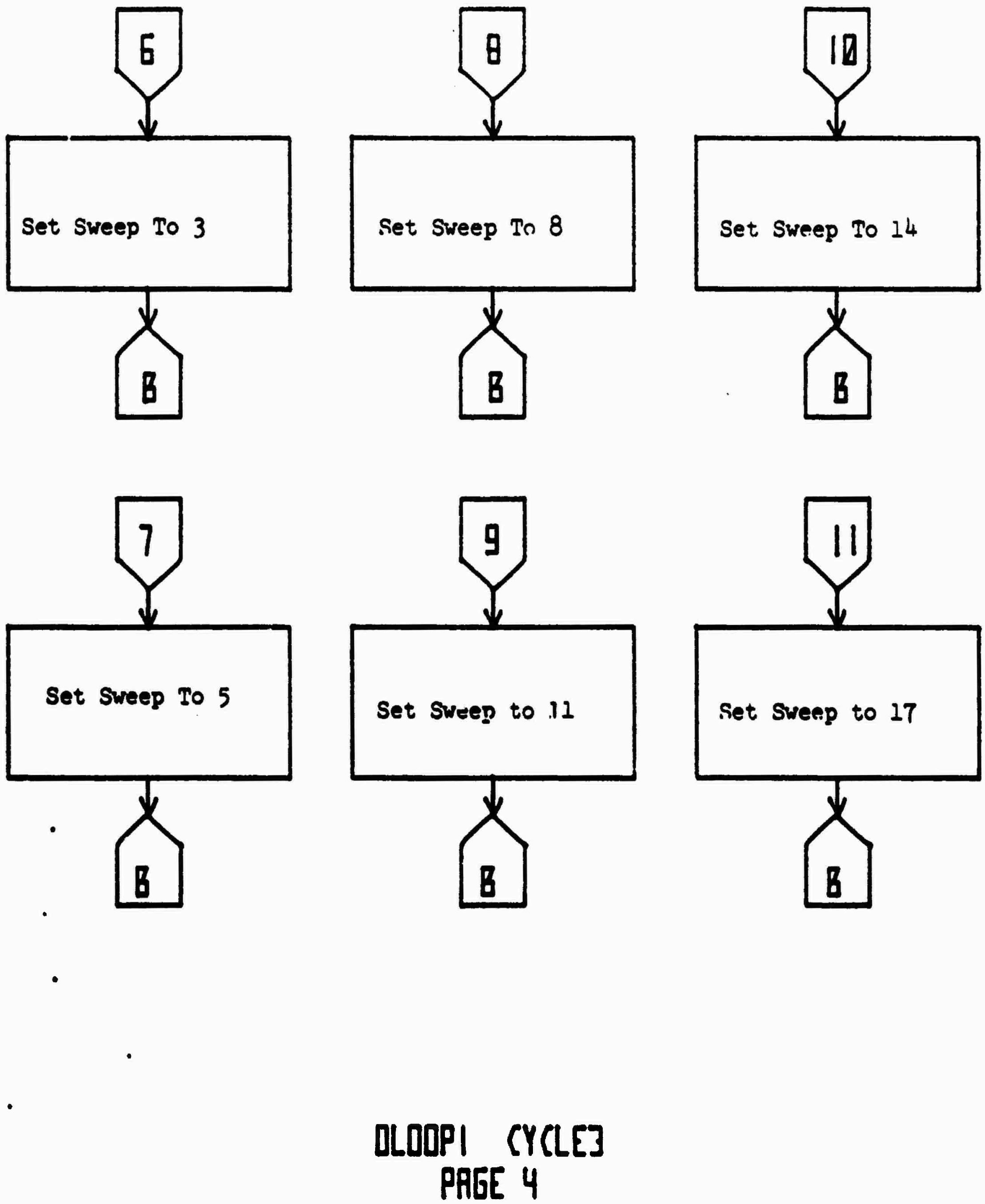

Figure F-2 (Cont'd) OLOOP1 Cycle 3 Flowchart (4 of 5)

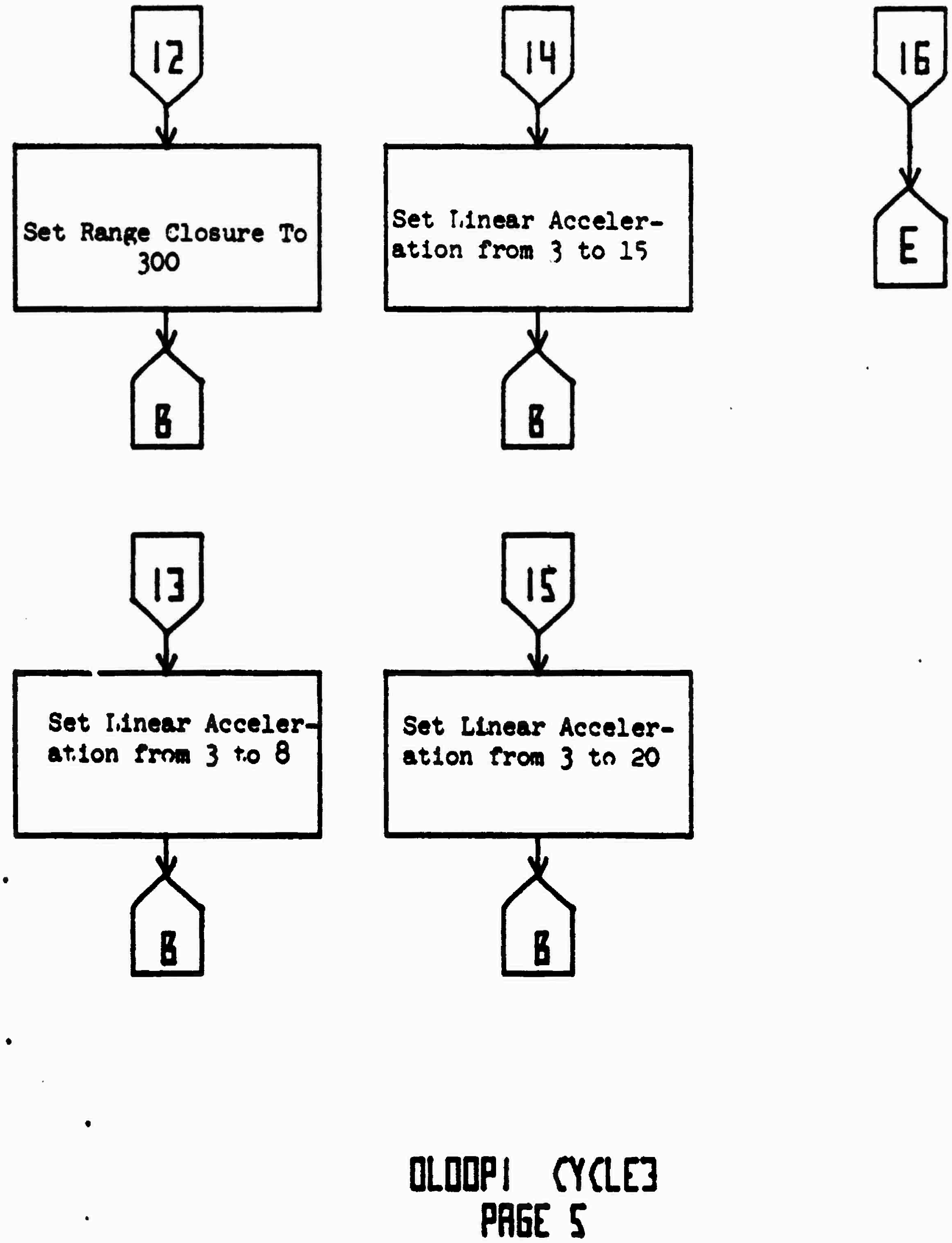

Figure F-2 (Cont'd) OLOOP1 Cycle 3 Flowchart (5 of 5)

DDS Diagnostic Routines Operation Sequence

I. Call the DDS operator via the intercom system.

1. Press "CALL".
2. Press "1".
3. Press "6"; LED should flash. The console operator will answer.
4. Holding the button on the inside of the phone receiver ask the operator to bring terminal #56 "on line."
5. When the operator acknowledges, press "HANG UP".

II. DDS Terminal will display - ACTIVE AND NOT BUSY.

1. Press "SEND".
   Terminal will display - ENTER USERNAME, PASSWORD, ACCOUNT NUMBER.
2. Enter-username, password, account number; press "SEND".
   Terminal will display - TRANSMIT NO CLASSIFIED MATERIAL.
3. Press "SEND".
   Terminal will display - PRIMARY COMMAND SET.
4. Type P; press "SEND".
5. Enter - ATTACH, lfn, pfn, ID=Acct. file, CY=X

   where:

   lfn = name of the local file to be used,
   pfn = name of the permanent file cataloged in memory (i.e. OLOOP1),
   Acct. file = the code name of the users cataloged files (DHXXXP), and
   X = cycle number from 1 to 5 (use #2 or #3).

   Press "SEND".
6. Type $J; press "SEND".
7. Enter-lfn,Y

   where:

   Y = lowest "control point available for direct" as displayed on screen.

   Press "SEND".

   Terminal will flash one message and then display-JOB CONTROL REPERTORY

8. Press "SEND".

   The terminal will display
   - TYPE P THEN TYPE 0, 2, 1 when the compiler is finished.

9. Press "SEND".
10. Type P; press "SEND".
11. Type 0,2,1; press "SEND".

   a. For OLOOP1 Cycle 2 the terminal will display initial missile and target parameters. The user as the option to change any one of these by following these steps:

      1. Press "SKIP" twice; enter number of parameter you want to change; press "SEND".
      2. Enter new value; press send. If you enter 11, the computer will go into real-time operation.

   b. For OLOOP1 Cycle 3, the terminal will display a set of scenarios previously programmed. To initiate a run, execute the following steps:

      1. Press "SKIP" twice.
      2. Enter number coinciding with desired scenario; press "SEND".

12. Unless the program aborts itself, the user must do so. This is accomplished by setting FF200 at the EAI 781 control-consols.
13. When you are finished, perform the following steps.
14. Type $$; press "SEND".
15. Type DROP; press "SEND".
16. If you want to attach another file, return to Step 4.
17. Type $T; press "SEND".
18. Press "SEND".

Terminal will display - A STATION LOGICALLY OFF.

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