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VOLUME II

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ADVANCED ULTRA-VIOLET (UV) AIRCRAFT FIRE DETECTION SYSTEM VOLUME II - SYSTEM HARDWARE DESIGN, SOFTWARE DESIGN, AND TEST

GENERAL DYNAMICS/FORT WORTH DIVISION
P.O. BOX 748
FORT WORTH, TEXAS 76101

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Thomas A. Hogan
THOMAS A. HOGAN, Project Engineer
Fire Protection Branch
Fuels and Lubrication Division
Aero Propulsion Laboratory

Robert G. Clodfelter
ROBERT G. CLODFELTER, Chief
Fire Protection Branch
Fuels and Lubrication Division
Aero Propulsion Laboratory

FOR THE COMMANDER

Robert D. Sherrill
ROBERT D. SHERRILL, Chief
Fuels and Lubrication Division
Aero Propulsion Laboratory

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Volume I - System Description and Flight Test
Volume III - Ground Support Equipment (GSE) For System Checkout

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this program was to utilize ultra-violet (UV) radiation technology to provide advanced means of detecting fire hazards more reliably and more rapidly than current thermally activated continuous cable type system. This volume, Volume II, of three volumes provides detail information on the development, circuit/software design and qualification testing of the system component.

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FOREWORD

The work reported herein was performed in accordance with Air Force Contract F33615-77-C-2029 under the direction of the Fire Protection Branch (AFWAL/POSH) of the Fuels and Lubrication Division, Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 2348, Task 01, Work Unit 02, with Mr G.T. Beery and Mr T.A. Hogan, AFWAL/POSH, as Project Engineers.

This report is the result of utilizing ultra-violet (UV) radiation technology in the development and flight testing of an advanced aircraft fire detection system.

The contractor was General Dynamics, Fort Worth Division, Fort Worth, Texas. Mr. R.J. Springer, Program Manager, directed the efforts of P.H. Lang, W.B. Kirk, B.B. Witte, D.C. Nelson, and J. Phillips. The overall effort was under the supervision of Mr. C.E. Porcher, Manager, Propulsion and Thermodynamics Section. Graviner Ltd./HTL Industries, General Dynamics subcontractor, accomplished the design, fabrication, environmental testing and support for the flight test phase of the program. Graviner/HTL's efforts were directed by Mr. S.P. Robinson who was supported by P.H. Sheath and D.J.V. Smith. Sacramento Air Logistics Command (SM-ALC) provided the F-111 aircraft and support for the flight test phase of the program. Mr B.W. Nichols, SM-ALC Engineering, coordinated the flight testing at McClellan Air Force Base.

This report describes the results of work conducted during the period of 15 December 1977 to 26 October 1981.

This is Volume II of three volumes. Volume I describes the overall work of the program which includes the results of the flight test phase. Volume II contains a description and details of the system circuit and software design. Volume III contains a description and details of the Ground Support Equipment (GSE) which is used as a fault diagnostic maintenance tool.

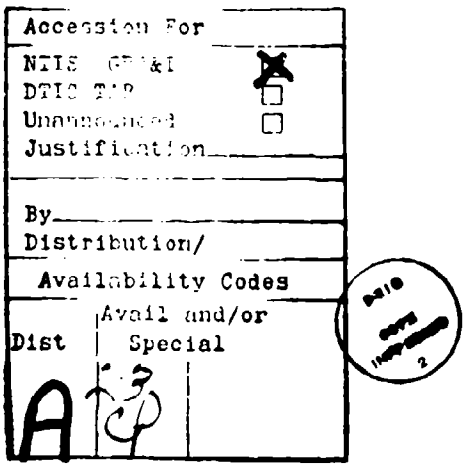

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SUMMARY

Analysis and details that include the electrical circuit, power supply, microprocessor boards, and logic cards were completed for each component in the system. In addition a software program was completed that included initialization, processing of adjacency and absent head information, software assembly listings, instruction summaries for the RCA 1802 microprocessor, and the COSMAC Level 2 assembly language of the microprocessor. A qualification test was completed after the design and fabrication of the system components.

1.0 INTRODUCTION

1.1 Microprocessor Selection

The trade study determined that the design should be based on the use of a microprocessor. Microprocessor evaluations determined that the RCA 1802 microprocessor would best provide the needs of the system requirements. The CMOS design, low power consumption, and low immunity to noise were the primary features for the selection of the 1802 for the UV fire detection system.

1.2 Microprocessor Integration

The integration of the microprocessor into the system design provides the flexibility and programmability needed to meet the high reliability requirements of this program.

2.0 COMPONENT DESIGN

2.1 Detectors

The main design constraints of the sensor heads arose from the requirement to use the proven Graviner D6100 UV cell with its associated UV test emitter, to withstand the environmental conditions of a military aircraft engine installation and to be as small and lightweight as possible. Physical characteristics are shown on Figures 2-1, 2-2 and on Installation Schematics Figures 2-3 and 2-4.

Within these design constraints the configurations developed and shown on drawings 53522-011 and 53521-012 are probably close to and optimum. (References 2-1 and 2-2.)

The designs are based on the assumption of production quantities that would justify expenditure on tooling for pressed steel case-work but the sensor assemblies used during this program were fabricated without tooling to simulate the proposed production design.

The photocell and protective quartz dome are mounted on a thin steel retainer with a fillet of silicone potting compound. This assembly is then spot welded to the case. In early development samples, some difficulties were experienced with emitter glass envelopes cracking during low temperature tests but this was later overcome by incorporating a resilient rubber compound coating prior to emitter assembly.

The simple mounting base is intended for use with a variety of aircraft brackets which might be necessary to provide appropriate viewing directions in an engine installation.

The assembly meets the required life of 10,000 hours at 250°C with the exception of the electrical connector, which has a life limited by the manufacture to 1000 hours at 250°C.

2.2 Component Design - Computer Control Unit

2.2.1 Construction

System A and System B electronic circuitry is contained in mechanically identical racking. General Assembly drawings 53813-203 and 53813-204 show pictorially the systems' construction. (References 2-3 and 2-4.) Physical characteristics are shown on Figure 2-5.

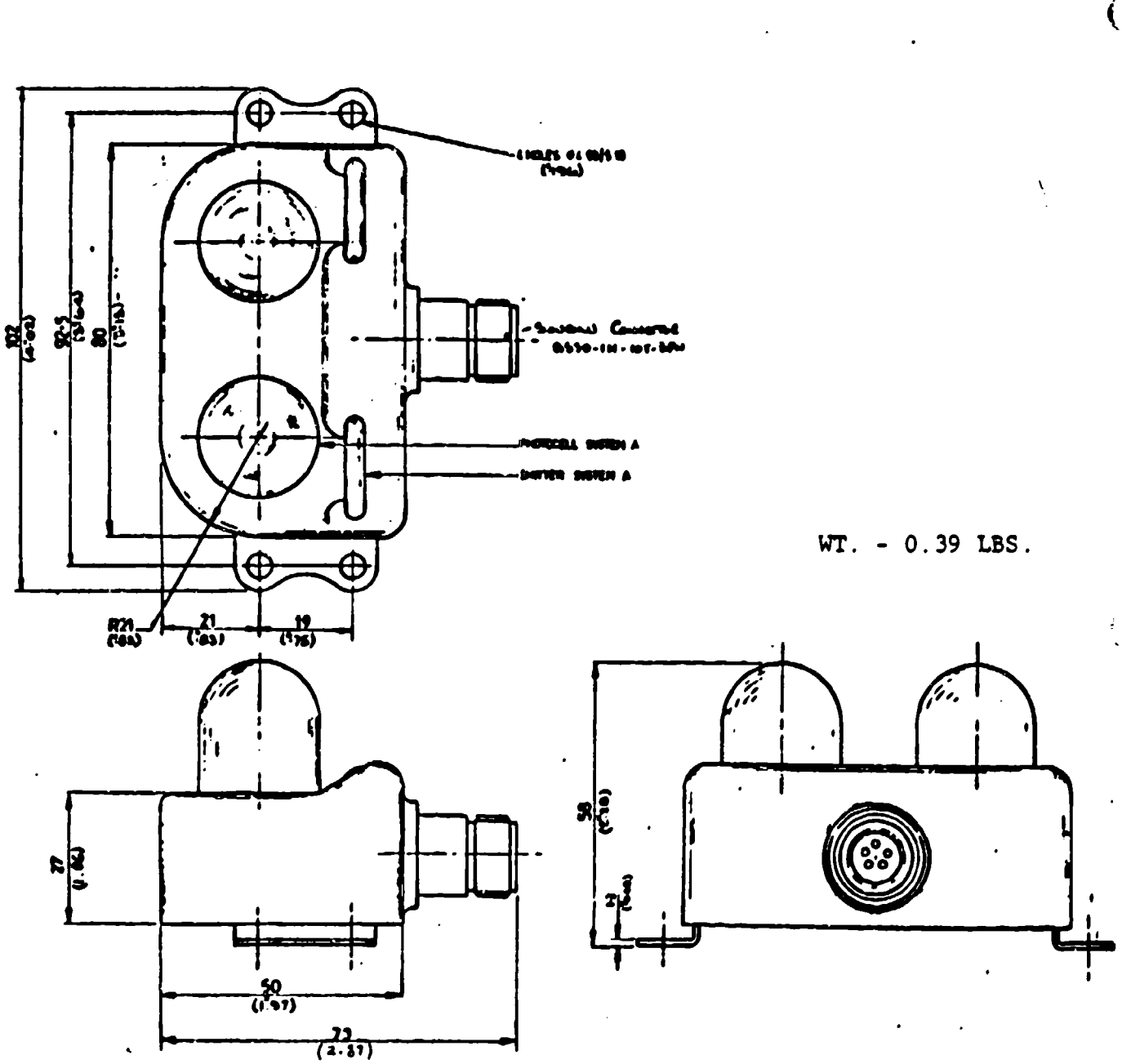

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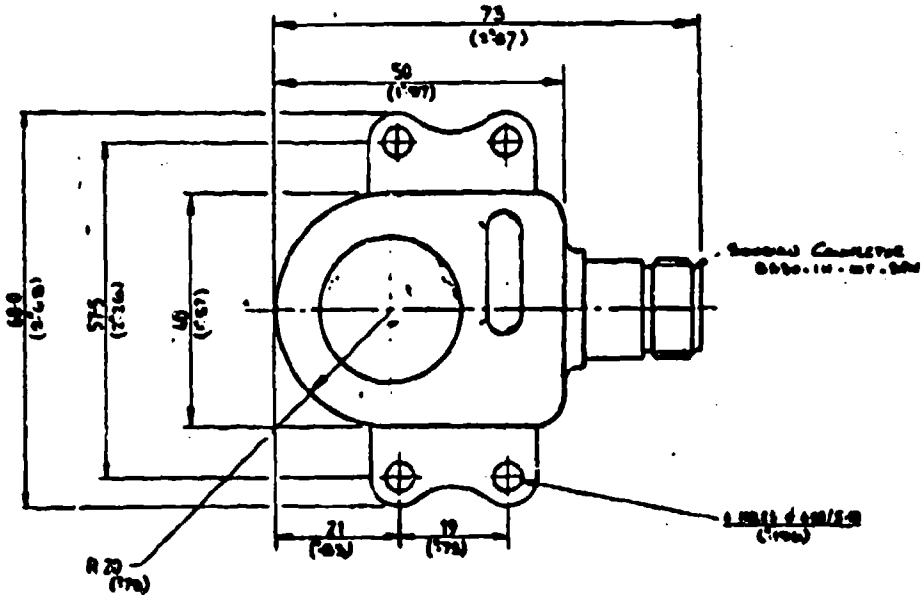
FIGURE 2-1 UV DETECTOR DUAL HEAD



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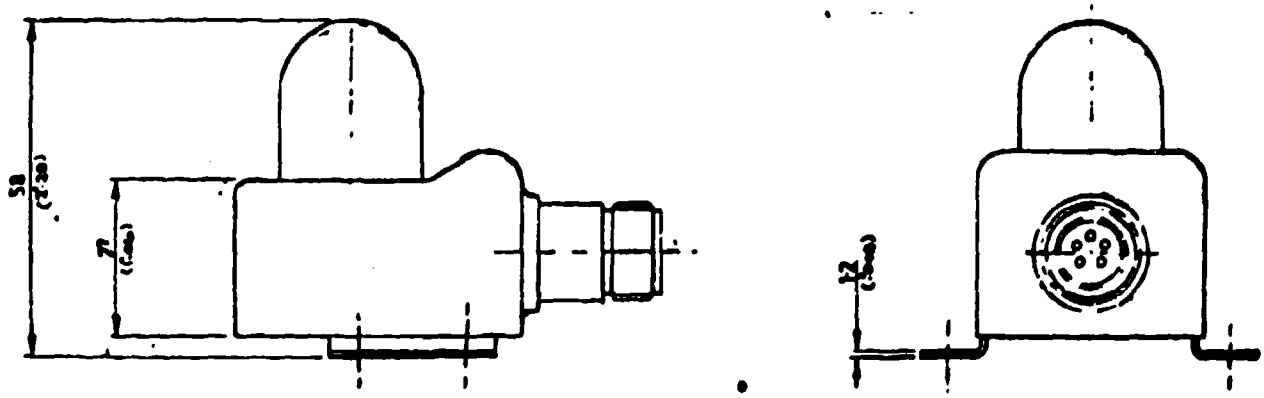


FIGURE 2-2 UV DETECTOR SINGLE HEAD

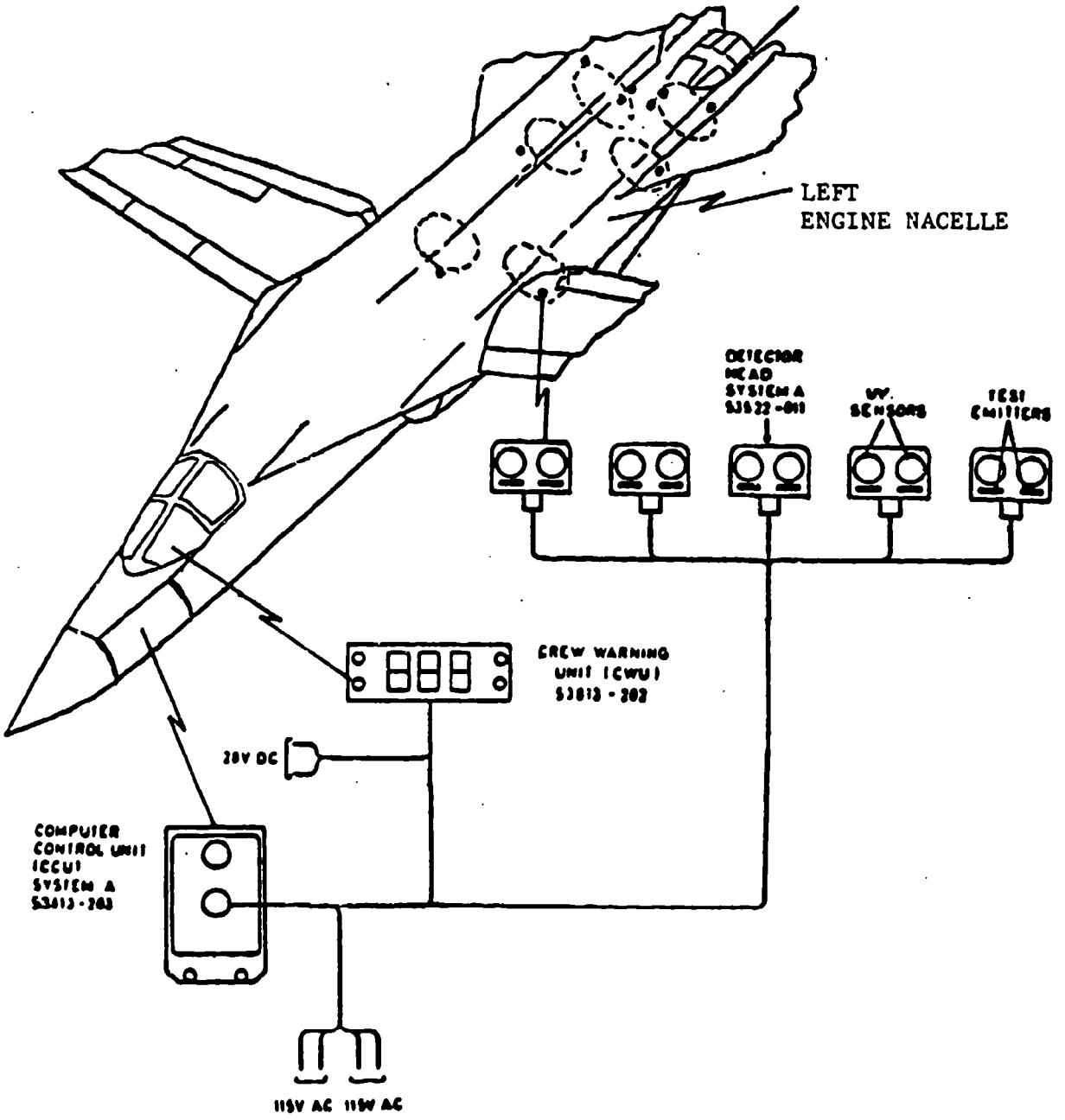


FIGURE 2-3 SYSTEM 'A' INSTALLATION SCHEMATIC

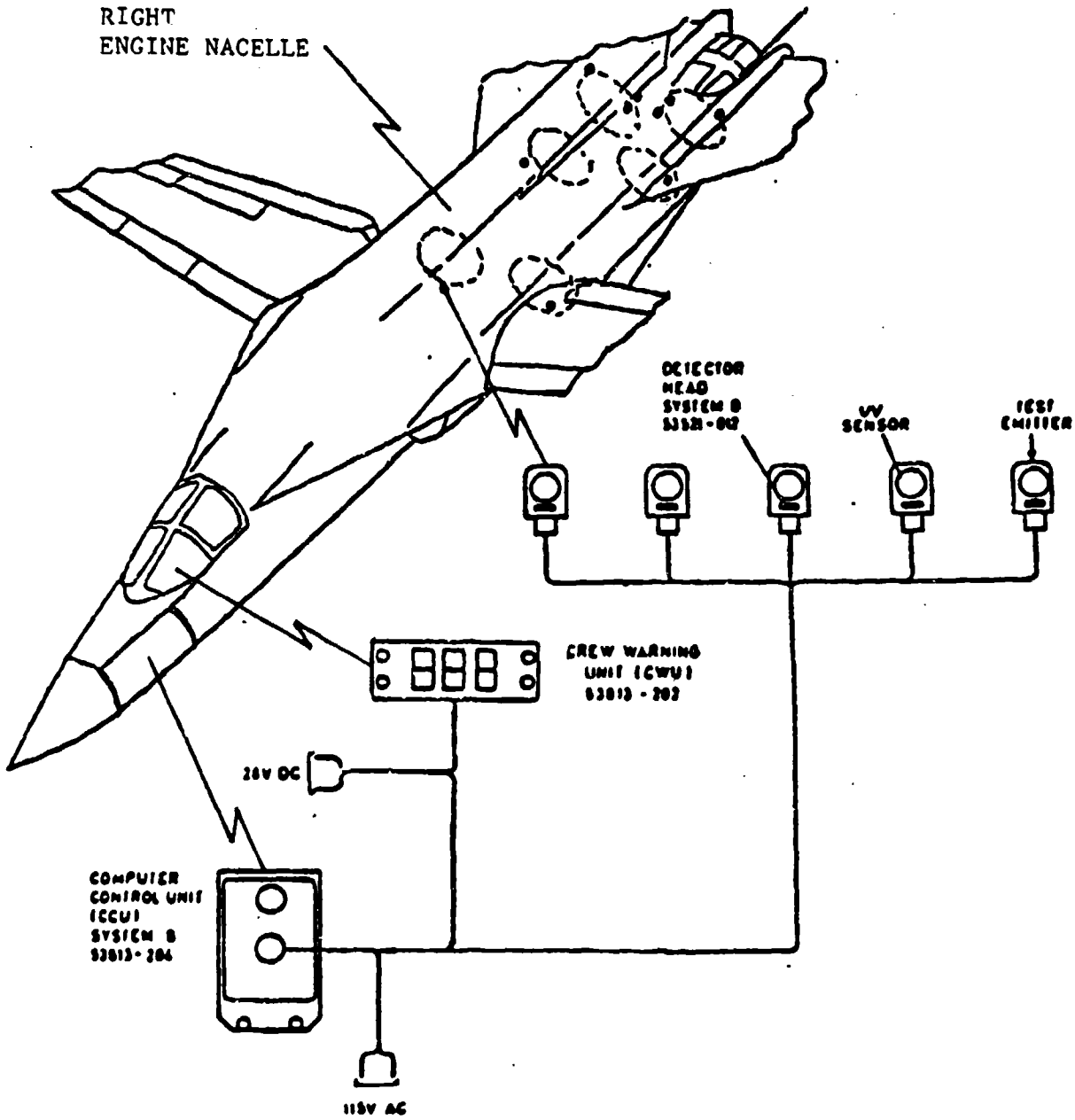


FIGURE 2-4 SYSTEM 'B' INSTALLATION SCHEMATIC

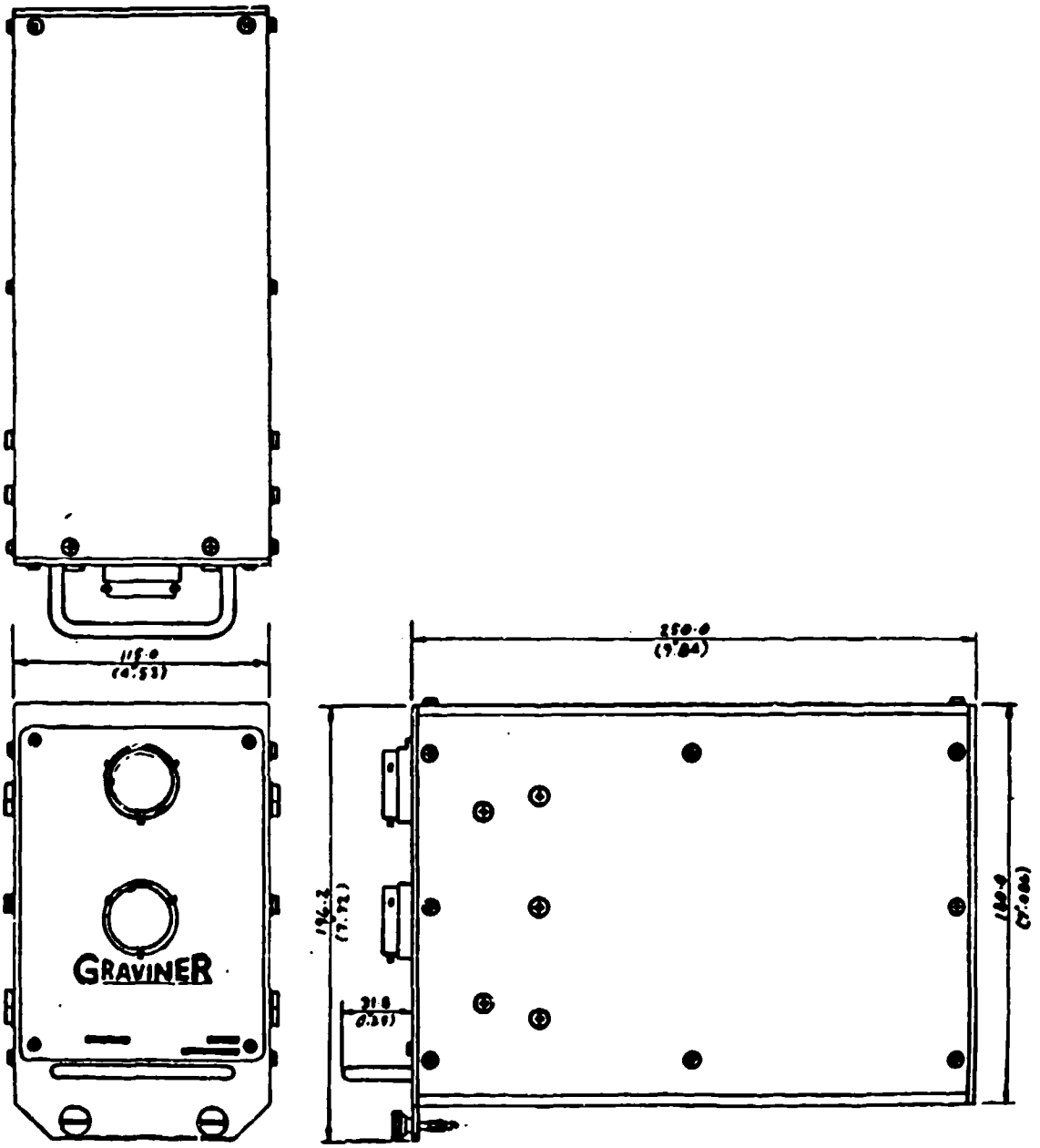


FIGURE 2-5 COMPUTER CONTROL UNIT

The essential features of both systems are as follows:

a) It is a box construction consisting of formed top, bottom and side panels, with two similar cast end plates. The rear panel has on its external face indented locating slots to ensure correct positioning of the units in the aircraft racking and on its internal face it contains guides to ensure location and adequate fixing for the printed circuit boards.

The front panel has mounted through it, two captive knurl headed screws to provide fixing to the aircraft racking. Two circular electrical multipin connectors are mounted through the front panel. One, termed on the front panel label the 'aircraft plug', routes to the electronics power and signals from detectors and also carries the signals to the crew warning unit (CWU). The second connector, termed the GSE plug, is utilized when the system is interrogated by ground support equipment and is not normally used when the aircraft is operational.

Internally, the box contains a cross member which acts to make the construction more rigid. To this are attached the printed circuit board guides.

b) Within the box a mother board printed circuit card acts to connect the various parts of the control unit electronics together. On the mother board are mounted connectors which mate with the cable harness connected to the two circular connectors, and to the daughter board connectors. The mother board also houses the transformer for the systems' power supply requirements.

c) A filter board is mounted on the front panel, close to the aircraft plug such that incoming power can be filtered.

d) The printed circuit cards contained within the units are interconnected via the mother board, and consist of, in the case of System A, a common logic card, two microprocessor cards, two head drive cards, a master logic card and a slave logic card. In the case of System B, the unit contains a common logic card, a microprocessor card, a head drive card, a master logic card and a battery card which is braced such that the mass of batteries does not cause vibration problems. Each card edge connector is polarized such that boards cannot be incorrectly located within the boxes.

2.2.2 Circuit Description

A block diagram of the CCU is shown in Figure 2-6. This is shown to give a general appreciation of the way the CCU printed boards interface with each other. Circuit description is essentially on a board by board basis. Reference is made to the CCU circuit diagram 53813-203CD (System A) or 53813-204CD (System B), for a clearer understanding of the way cards are interconnected. (References 2-5 and 2-6.)

2.2.2.1. Drive Supply Card

(Circuit diagram 43761-143-CD) - Reference 2-7

The drive supply card consists of a 320v DC stabilized supply, a 5.6v and a 5v DC stabilized supply, 8 head drive circuits, an emitter drive circuit and a low voltage detection reference.

2.2.2.1.1. 320v DC Supply

The AC voltage from the transformer's secondary winding No.1 is rectified via the bridge rectifier D1, D2, D3 and D4 and smoothed by C1. C31 is a radio frequency suppression capacitor. This voltage is then stabilized to 320v DC by means of a series feedback regulator. D12 and R6 provide a reference voltage for the emitter of TR3. R9 and R11 potentially divide the output voltage which feeds the base of TR3. As the output voltage increases, TR3 base rises above the reference voltage and TR3 starts to conduct. This in turn clamps the base of TR2 and the output voltage . D16 protects TR2 from exceeding its reverse voltage rating. The base drive to TR2 is provided by a constant current source generated by TR1. D9 and R1 set up a reference voltage for the base of TR1. R4 sets up a constant current in the emitter lead of TR1. Hence a constant current is developed in the collector of TR1. The 320v DC supply powers the head drive circuits and the emitter drive circuits.

2.2.2.1.2. 5.6v and 5v DC Supply

The AC voltage from the transformer's secondary winding No. 2 is rectified via the bridge rectifier D5, D6, D7 and D8 and smoothed by C3. C2 is a radio frequency suppression capacitor. This voltage is then stabilized to 5.6v via an emitter follower regulator. A reference voltage at the base junction of TR4 is set up by R7 and the combined forward voltages of D13, D14 and D15. R8 sets up a constant current in the emitter lead of TR4. This in turn sets up a constant current in the collector lead which supplies zener diode, D17, and base drive to TR5. D17 provides a reference voltage (6.2v) at the base junction of TR5 causing the emitter of TR5 to provide a 5.6 volt output. C4 smooths this voltage and acts as an energy store for sudden surges in current. D18 protects TR5 base emitter junction from exceeding its reverse voltage rating when supply is switched off.

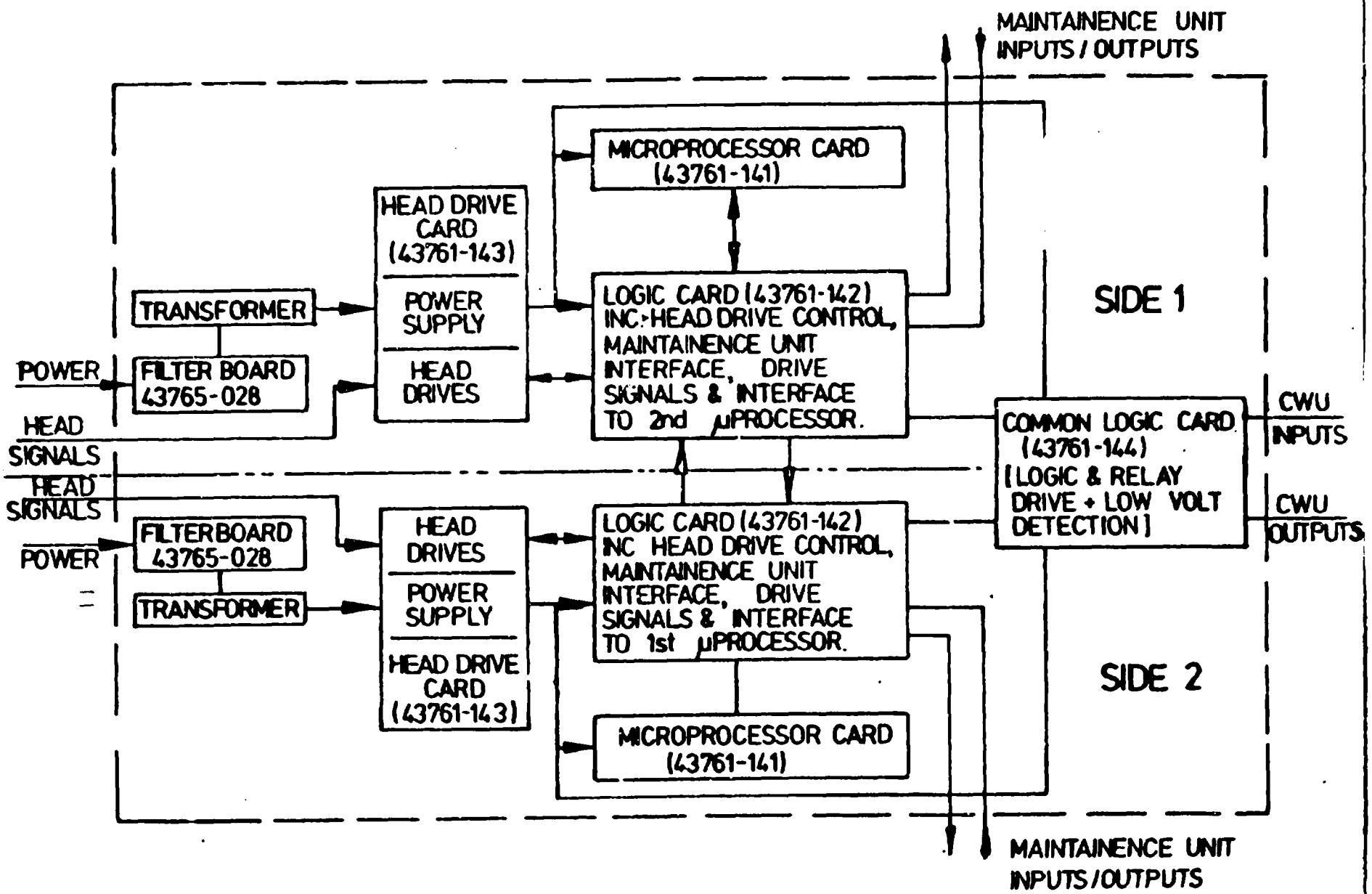


FIGURE 2-6 COMPUTER CONTROL UNIT BLOCK DIAGRAM

Two further supplies are generated from this voltage via D19 and D20. The 5.6v supplies power to the common output logic card. The 5.6v supply via D20 powers all logic and microprocessor devices except the RAM which is powered via D19. This ensures that the RAM is isolated in the event of supply failure or disconnection. In this case the RAM is powered by a separate battery pack as detailed in Section 2.2.2.6.

2.2.2.1.3. Low Voltage Detection

This circuit monitors the rectifier voltage of the transformers No. 2 secondary winding. The voltage is potentially divided by D10,R2,R3 and R71. The voltage across R3 is fed to the common logic card. This circuit provides an early warning signal to the microprocessor that the supply is fa ling as detailed in Section 2.2.2.4.4.2.

2.2.2.1.4.. Head Drive Circuit

The head drive circuit is designed to enable one side of the photocell to be common with the 0v line. Thereby, minimizing the amount of wiring required in the aircraft and control unit. The head circuit consists of four sections:

i) The Detector Current Sensor,
ii) Head Turn Off Time Control Circuit. (not part of the drive supply card)
iii) Head Turn Off
iv) Current Limit Circuit

Circuit description relates to head drive 1 consisting of transistors TR6, 7 and 14 with associated components.

2.2.2.1.4.1. The Detector Current Sensor

The head current sensor PNP transistor TR14, which in standby mode is biased off. When the supply is switched on the capacitance across the leads to the photocell charges up via R32. R72 and C23 are designed to charge up at a slower rate than R32, R and the lead capacitance therefore reverse biasing the base emitter junctions of TR14 and holding it off. D38 protects the base emitter junction of TR14 from exceeding its reverse voltage rating.

When UV is present at the photocell it will conduct causing current to be drawn through R, R32, R72 and the emitter base junction of TR14. TR14 conducts and current flows through R24 and R25. C5 reduces the radio frequency interference generated when the current sensor circuit is operating. The voltage across R25 is coupled via C9 to the head turn off timing control circuit on the logic card.

2.2.2.1.4.2. Head Turn off Time Control Circuit

The head turn off timing circuit is described in Section 2.2.2.3.5.

2.2.2.1.4.3. Head Turn Off

The output from the logic card feeds the base junction of TR7. R13 is a pull down resistor to ensure TR7 does not turn itself ON due to collector base leakage current. A 5 volt signal from the logic card causes TR7 to turn ON. The potential divider chain, R12 R20 then clamps the base of TR6 to approximately 15v. TR6 acts as an emmitter follower, therefore the voltage across the photocell is reduced to approximately 15v allowing the photocell to deionize. At the end of the timing period the signal from the logic card returns to 0v. TR7 turns off allowing TR6 to be turned on by R12 returning the photocell voltage to 320v.

2.2.2.1.4.4. Current Limit Circuit

If the head lead becomes short circuit to ground, TR14 turns hard ON and an output pulse is passed to the logic card. TR7 turns on and the voltage across the photocell drops to approximately 15v. At the end of the head time off period TR7 turns off allowing TR6 to turn on, but as TR14 is being held hard on excessive current is being drawn through R80. When the voltage developed across the base emitter junction of TR6 and R80 equals the combined forward voltages of D25 and D55 no further increase in TR6 base drive occurs, and hence the current is limited. D47 isolates the head circuit from seeing negative going spikes.

2.2.2.1.5. Emitter Drive Circuit

The emitter drive circuit is designed so that a maximum of 8 emitters can be powered at one time. The emitters are connected in parallel to minimize aircraft and control unit wiring. The circuit consists of three parts:

i) Time Sharing 350v Switch.
ii) Emiter Enable Circuit (Head Test)
iii) Emitter Verify Circuit.

2.2.2.1.5.1. Time Sharing 350v Switch

The voltage to the emitter enable circuit is controlled by the time share switch. The timeshare signal from the logic card (at pin 8) is a square wave. When the output is high TR30 turns on via a base current limiting resistor R4 (on logic card), this holds TR32 off. TR31 is turned on by R62 and 350v DC is supplied to the emitter enable circuit. When the output of the logic card goes low, TR30 turns off and TR32 turns ON via R61 pull up resistor.R62 and R63 potentially divides the 350v supply clamping the base of TR31 to approximately 154v. The emitters, which require greater then 90v to strike, will therefore turn off. R60 is a pull down leakage current resistor for TR30 emitter base junction.

2.2.2.1.5.2. Emitter Enable Circuit

Under standby condition i.e. emitter off, the head test input (pin 9) from the logic card is low (0v). TR34 is, therefore, turned ON via R65 pull up resistor. R64 and R66 potentially divide the voltage from the time share switch which clamps the base of TR33 to approximately 25v when TR21 emitter voltage is high and approximately 1v when it is low. TR33 is an emitter follower and 25v or 1v is fed to the emitters (connected at pin 15) via a current limiting resistor R69.

When the head test input goes high, the emitter of TR34 is held at 5v.

Because the pull up resistor R65 is supplied from the 5v power supply, TR34 turns off and TR33 turns on via pull up resistor, R64. The voltage at the emitter TR33 will then follow the voltage at TR31 emitter which changes from 350v to 15v in sympathy with the time share input. D37 protects TR33 from exceeding its reverse voltage rating when it turns off.

2.2.2.1.5.3. Emitter Verify

The circuit monitors the output voltage to the emitters so that the microprocessor can confirm when the emitters are on.The output voltage from TR33 is potentially divided by R67 and R68. The junction of these resistors feeds the base of TR35. When the emitter line voltage is high (350v), there is sufficient voltage at the base of TR35 to turn it ON. The collector of TR35 goes low which feeds the EF3 (NOT) input of the microprocessor card. When the output goes low TR35 turns off and the output is pulled up via R70 to the 5v line. Because the lead capacitance tends to hold the emitters on for a short period after the emitter circuit has been switched off, it is necessary to discharge this capacitance.

2.2.2.2. Microprocessor Boards

(Circuit diagram reference 43761-141CD) - Reference 2-8

The microprocessor card houses a CMOS microprocessor (IC1) CDP 1802 CD and CMOS memory consisting of 3K bytes of read only memory (ROM) and 256 bytes of random access memory (RAM). All other integrated circuits contained on the card are CMOS to ensure high noise immunity and low power consumption. The ROM consists of 6 IC's, IC5 - IC10 each being UV erasible 512 word 8 bit configured parts, IM 6654MJG, manufactured by Intersil. RAM is formed by IC2 and IC3 configured as 256 bit by 4 manufactured by RCA, part number CDP 1822CD.

Memory is arranged such that ROM resides between locations H'0000' and H'0BFF' and RAM resides between locations H'0C00' and H'0CFF'. This is controlled by IC4 (CDP1859CD) which latches and decodes address line information as further described.

The microprocessor issues the address on to the data bus in two bytes. Firstly, the upper byte, whose correct presence is defined by a timing pulse TPA whose negative edge is used to latch the address into the 4 bit latch/decoder IC4 via its clock input (CK). At the time immediately after the falling edge of TPA, the address A11, A10, A9 and A8 have been latched into IC4 via address line A3 to A0. The truth table of IC4 shows that A8 and A9 and their compliments are provided as latched outputs while A10 and A11 are decoded into 1 of 4 format such that when the true address is present, the appropriate chip enable is driven to a '0' state. Therefore, the CE (NOT) lines act to select between M'0000' and M'03FF' when CE0 (NOT) is true, between M'0400' and M'07FF', when CE1 (NOT) is true and between H'0800' amd H'0BFF', when CE2 (NOT) is true, i.e. between 0 and 1K byte, 1K byte and 2K bytes or between 2K bytes and 3k bytes.

The latched outputs A9 and A9 (NOT) serve to further decode the address. When the address is in the lower half of the required 1K byte range (i.e. between 0 and 512) then A9 (NOT) is at logic '1' and A9 is at logic'0'thus selecting from the upper bank of ROM (IC5, IC7, and IC9) since the E2 (NOT) input of the IM 6654 requires a '0' signal to be selected. The latched A8 line from IC4 is connected to all ROM A8 inputs.

ROM's IM6654 will latch internally on the address lines at the occurrence of a negative going edge on E1 (NOT) only if the chips S1 (NOT) line is held low. Because of this it is necessary to create a suitable signal to input as an E1 (NOT)control at a time when all required inputs are available on the address bus.

This is done by delaying the TPA pulse for two system clock cycles and utilizes IC13 to effect the delay. The crystal (XTAL) output from the microprocessor is used to act as a clock pulse into the first stage divider of IC13. The data input to this divider is the TPA pulse. Initially, when the system is switched on, both Q outputs of IC13 are reset, caused by a control signal provided to the reset inputs. At this first occurrence of TPA, a '1' is clocked through to the output of the first stage of IC13. A second clock pulse occurring at the clock input transfers this '1' level through to the second stage output which is connected to all ROM E1 (NOT) inputs. The advent of a third clock pulse causes a negative going edge at E1 (NOT) as required for latching of address lines into the ROM. This occurs approximately 1.5 clock cycles after the negative going edge of TPA has occurred and at a time when the lower order address byte has been issued by the microprocessor and has become stable on

the address bus. If the chip has been selected at the time the E1 (NOT) line input changes from a '1' to a '0' state, then the address lines A0 - A8 and chip enable line c2 (NOT) are latched into the ROM causing the selected location to place its contents in the MRD output of the microprocessor such that the ROM cannot be enabled on to the data bus during a memory write cycle. During this time the EN (NOT) line is held high thus disabling the CE (NOT) outputs to a deselected '1' state.

Address line decoding for the 256 bytes of RAM is effected by the nand gate of IC11 and D type flip flops of IC12 whose Q output is initially set to a '1' switch on by coupling the clear line to the set input of IC12 via an inverting buffer of IC11. Since the address range of the RAM is OC00 to OCFF, the two inputs to the and gate are used to detect the presence of a '1' level on address lines A10 and A11 (A3 and A2 during the upper byte address cycle). When both A10 and A11 are present the output of the nand gate goes to a '0' state. TPA signal is inverted by an invert gate of IC11 such that a positive edge will occur at the clock input of IC12 at the time TPA goes low. The result of which is that the output of the nand gate is latched on to the Q output of IC12 . A '0' Q output is then used as a chip enable for the RAM and CS1 (NOT) of ICS2 and 3 are connected to IC12's Q line. When this line is low RAM becomes selected and data is passed to, or stored from the data bus according to the state of the R/W (read/write) line and selected address on lines A0 - A7. The input lines I1 - I4 and output lines O1 - O4 are linked together on to the data bus and direction of data flow is controlled by the microprocessor timing logic via the MWR (NOT) line.

The CS2 line of RAM's IC3 and IC4 is a second chip select line which must be maintained at a '1' level while the system is running. This line is used to ensure that RAM does not receive any incorrect data when the system is powered up or shut down. This is further covered under Section 2.2.2.4.4.2 as are the functions of D_1, D_2, D_{12} and the separate power supply to RAM via VDD RAM.

The microprocessor timing is set by a crystal (XL) with appropriate loading C1 and C2 and bias resistor R1, as defined by the manufacturer. Design frequency is 2MHZ and was chosen based on the needs of the system. The operate frequency is limited by the working voltage and temperature range. The working voltage was chosen as 5V to suit the needs of the ROM. The design frequency gives adequate margin when the system operates at 85°C that allows sufficient time to execute all required system functions and allows memory components to run well inside their timing restraints. In addition, the relatively low operate frequency holds microprocessor power consumption to a low level.

Data bus lines D0 to D7 are connected to ground via pull down resistors R2 to R9 such that on power up and power down, data lines return to known states. This helps ensure that incorrect data is not passed to RAM, which would corrupt data held for GSE read out.

Resistor R10 and R11 act as pull up resistors for the two flag lines EF1 (NOT) and EF2 (NOT).

The microprocessor WAIT line is connected to VDD via the motherboard also CK IN and CK OUT are connected together via the motherboard,and all these connections are designed to facilitate board testing.

All other remaining microprocessor inputs and outputs, namely DMA IN (NOT), INT(NOT), SC0, SC1, EF1 (NOT) to EF4(NOT), TPA, TPB, N0, N1, N2, CLR (NOT) and Q lines act as control or timing outputs or inputs as described in subsequent sections.

Capacitors C3 to C7 are filter capacitors placed strategically around the pcb to reduce effects of supply borne transients or induced pickup.

2.2.2.3 Logic Card

(Circuit diagram reference 43761-142 CD (Master) - Reference 2-9
or 43761-148 CD (Slave) - Reference 2-10

The logic card can be sectioned into several areas having well defined functions to perform. They are power up, reset circuitry, input and output control, interrupt timimg, head drive timing and control input data buffering and output data buffering.

2.2.2.3.1. Power up, Reset Circuit

To ensure correct system operation when power is first applied the circuit must be in a known state. Essentially all important microprocessor regis..rs must be reset to zero, output ports must be cleared such that transient conditions do not appear at the CWU and some system flip flop registers must be set to a known state.

R1 and C1 form a time delay function and act in conjunction with R2, R3 and two buffer sections of IC2. When power is first applied, C1 is discharged. Via the pot chain divider of R2 and R3 the buffer input (pin 5 of IC20) is held at OV resulting in the clear line, CLR (NOT), output at pin 2 of IC20 being held

low. Note that since the resistor R3 of the pot divider chain is connected to the CLR (NOT) line, the pot divider is initially zero volt referenced.

The general requirement of the system is that the CLR (NOT) line should be held low for a short period of time to ensure correct reset of the above mentioned functions. As R1 causes C1 to charge up, the threshold of buffer input pin 5 is reached such that its output now changes to a '1' state (5V level). The clear line follows this transition which is speeded up by the fact that the divider chain R2 and R3 is now 5V line referred effecting a schmitt trigger action. The transition effects the removal of the clear state from all attached circuits.

Buffer input pin 7 of IC20 is also connected to the clear line such that via its output, pin 6 and diode D1, output port IC12 is initially cleared. The action of CS2 input on the output port IC12 is discussed in section 2.2.2.4.

2.2.2.3.2. Data bus Lines

Data bus lines connected to the microprocessor (external to the pcb) are connected to output port IC12, input ports IC14, IC15 and IC17 and to outputs of IC6 and IC10.

2.2.2.3.3. Data bus Control

Data being input to, or output from the microprocessor via the data bus lines is controlled by decode chip IC13 which itself is controlled by timing and output signals generated by the microprocessor. Lines N0, N1 and N2 are input lines to the decoder chip which contain encoded data as to the required port (input or output) to or from which data is to be passed. IC13 decodes the N lines and, its outputs are connected to chip enable lines of various input and output ports or act as clock lines. CKA and CKB inputs of IC13 are connected to TPA and TPB outputs of the microprocessor controlling the duration that IC13 outputs remain active.

2.2.2.3.4. Interrupt Timing

The system requires for correct operation an interrupt signal which occurs once every 832us. This signal is sent to the microprocessor's INT (NOT) (interrupt) input causing an interrupt software program to be executed.

To generate the timing signal the microprocessor's own timing pulse, TPB, is used. This pulse occurs every 4us with a crystal frequency of 2MHZ.

The circuit involved is IC1 and IC2.

The timing pulse TPB is connected to the clock input of IC1 (pin 1). With the EN line connected to VDD the counter chip causes TBP pulse to be divided by 16 at its output (pin 6). Thus, at this point a square wave of 64us period is observed. This waveform is applied to the enable (EN) input of the second counter stage of IC1. With the clock input (CK) connected to VSS the chip acts to increment the counter on the negative transition of the incoming signal.

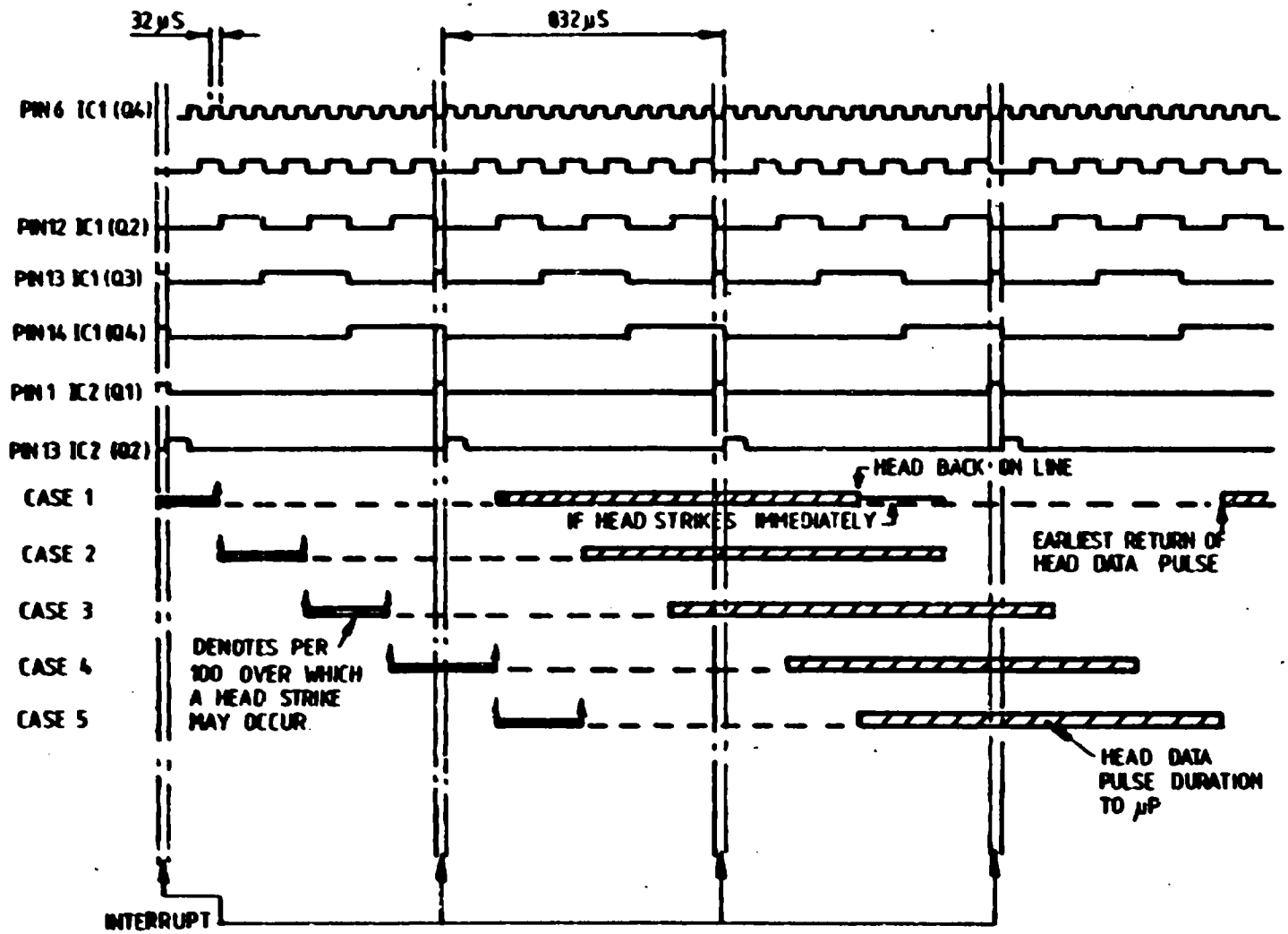
The following operation is then discussed in conjunction with Figure 2-7.

Q3 output of IC1, by the divider action of IC1 is caused to change state on negative transitions of the previous binary divide stage, resulting in the pulse train shown. When Q4 output is low the positive transition of Q3 has no effect on the output Q (pin 1) of IC2, since at the transition the data input to IC2 at pin 5 (Q4 of IC1) is zero. When Q4 output is high, the positive transition of Q3 will cause a change of state at IC2 pin 1 to a '1'. The data input at pin 9 of IC2 is now at '1' level, consequently, at the next positive transition of this D type flip flop's clock input a '1' will be transferred to its Q output (pin 13.) As can be seen from the timing diagram, this occurs 32us later.

Pin 13 of IC2 acts as a reset input to the second stage of the divider chain of IC1, and one D type section of IC2. Because the D input at pin 9 of IC2 is now returned to '0' by this reset action, then on the next positive transition of Q4 (pin 6) of IC1, the reset pulse is removed.

This cycle is repeated as shown by the timing diagram such that the Q output (pin 1) of IC2 is low for 800 us and high for 32us. Q (pin 2) of IC2 is the compliment of this and consequently applies a negative going edge to the INT (NOT) input of the microprocessor once every 832us. As can be seen this interrupt pulse is self resetting after being sustained for 32us. The timing of the microprocessor hardware and software is such that this interrupt pulse is always recognized before it has time to return to the standby state.

At power up the output states of ICS 1 and 2 are random which can cause an initial incorrect timing of the interrupt pulse. However, since the software program does not enable interrupt pulses to be recognized for some milliseconds after power up, the required synchronization has time to occur.



INTERRUPT & HEAD DATA TIMING DIAGRAM

FIGURE 2-7

2.2.2.3.5. Head Drive Control Circuit

The eight head drive circuits described under Section 2.2.2.3.1. each require individual control such that at the occurence of a strike, the head is starved of voltage for a 2ms period. ICS 3 - 10 and ICS 18 and 19 are responsible for head drive control and buffering on to the data bus for access by the microprocessor.

Circuit description considers one control section associated with head 1.Active components are R5, R32, IC18 nand gate (with output pin 3), R43, IC3 NOR set/reset flip flop (with Q output pin 2), IC4 binary counter and IC6 transmission gate output pin 1 of which is connected to the data bus line D0.

Under standby conditions the set/reset flip flop has its Q output (pin 2 IC3) at a '1' state since the last input would have been a set input.

Consequently, the reset input of the binary counter would be disabled and the clock pulse input at pin 1 (derived from the timing block) would have no effect. The output (pin 3) of the and gate is dependant on the input at pin 1. This, the time share signal is high ('1') for 167mS and low ('0') for 167mS repetitively. Therefore, R32 acting as the base current drive to TR7 of the head drive circuit controls whether the head is on line or off line.

When head 1 strikes, a pulse is developed across R5 due to the differentiating action of the combination of C9 (on the head drive card) and R5. This pulse acts as a reset pulse to the set/reset flip flop, causing its Q output to change to a '0' state. At this time the time share input to the and gate (pin 1) is high (which it had to be to allow a strike to occur initially). The resulting '0' state now existing on pin 2 of the nand gate causes its output to go to a '1' state, the result of which is that the striking head is starved of voltage.

The duration that the head is starved of voltage is a function of the operation of the binary counter IC4. The counter is clocked by pin 12 (Q2) of IC1, a pulse which occurs once every 256mS as shown on the timing diagram Figure 2.7.

Again, with reference to the timing diagram, when a strike has occurred the reset input R (pin 7, IC4) is released allowing the CK input to cause the counter to count.

When eight CK pulses (low to high transitions) have elapsed Q4 output of the binary divider goes high. Since this output is connected as the set input of the set/reset flip flop the effect is to cause the binary divider to be reset and to restore the head back to an on line status. Since one clock pulse is normally 256us, then it follows that the head has been off line for 2048us or just over 2mS.

The timing diagram shows that this software is subject to some variation due to the uncertainty of when the head will strike with respect to the fixed timing intervals of the clocking pulse.

The timing diagram shows the 5 cases which can occur indicating the range of strike time between clock pulse events, the result of which is that head 'off time' can vary between 1.92mS and 2.24mS.

The Q3 output of the binary counter is used to act as an indication to the microprocesor that a head has fired. This Q3 output is fed to a transmission gate which controls Q3 access to the data bus, the control line of which is conected to output 7 (07) of IC13. Head status is available to the microprocessor by executing a command on INPUT PORT 7.

To ensure correct interpretation of the incoming data, the timing of the circuit and manipulation of the data is critical.

Again, with reference to the timing diagram it can be seen that the Q3 output (which indicates a head strike to the data bus) can occur in such a way as to either be true at one or two successive interrupts. The interrupt marker causes the interrupt program to input the head status data to the microprocessor, thus it could be that the system interprets one strike as two events if the event happens to "straddle" two interrupt markers.

As shown by case 1, when the head returns to an on line status Q3 output cannot return to a state showing a second strike event until just before the fifth interrupt event. For this case and all other cases it is proven that two separate head strikes on one head cannot be observed by two consecutive interrupt markers. As a result the software program is written so as to disregard as false, a second pulse if two consecutive strikes occur.

2.2.2.3.6. DMA and Control Data Parameters

Direct Memory Access (DMA) is utilized in the design to pass relevant data from one processor to the other. This data includes a byte of information containing parity bits and various

status bits, to be discussed under the heading, Software. In addition each processor transmits to the second processor a byte containing the status of each head such that the receiver can make appropriate logic decisions.

DMA transfer is used such that the important task of observing fire conditions (termed the "gathering phase") is not interrupted. DMA causes the transfer of the above data directly to the receiving processors memory and is virtually unseen by the normal interrupt program. To guarantee that the data is received correctly the hardware associated with the DMA function is duplicated in such a way that if one of the receivers is faulty it can be identified.

The circuitry associated with the DMA activity is essentially IC15, 16, 17, 22 and 23 and associated components.

The transfer of data is effected by the sending microprocessor, the result of which is that the required level to be transmitted appears at the receiving logic card via the DMA DATA IN line (pin 53 on the edge connector). A clock pulse is required to initiate the receiving processors DMA mechanism. The clock pulse is generated by the sending processor and appears at pin 17 of the receiver logic card designated DMA DATA CK IN.

The DMA DATA IN logic level is buffered and separated by two buffers of IC21. The outputs of both buffers are connected, one to each of the two input ports IC15 and IC17 associated with DMA transfer both being connected to the 0 input.

The remaining inputs to the two DMA input ports are:

bit 1 (I1) = master/slave initialization bit.
bit 2 (I2) = port identity bit.
bit 3 (I3) = third level adjacency bit.
bit 4,5,6, (I4,I5,I6) = second level adjacency bit.
bit 7 (I7) = first level adjacency bit.

Master slave initialization bit is required to ensure that at switch on the software takes a path such that the time share for side 1 and side 2 of the system functions in antiphase to each other. The only difference between logic cards 43761-142 (Master) and 43761-148 (Slave) is in the setting of the master/slave bit, master is recognized as being connected to a '1' level and slave as being connected to a '0' level.

The port identity bit I2 is connected to VDD on IC15 input and to VSS on IC17 input. This is to enable the processor to recognize that it is correctly receiving data from both input ports.

The function of bits I3, to I7 are considered in detail in Appendix A-1.

Each bit of transmitted data is transmitted twice and the receiving input ports are arranged by hardware means such that the data is passed alternately via IC15 and IC17.

Since two bytes of information are to be transferred twice, it follows that 32 separate DMA transfers occur requiring 32 memory locations in the receiver memory map.

When a DMA data transfer is intiated by the sending processor the required logic level is placed on the DMA DATA IN line. When it subsequently initiates a clock pulse at the DMA DATA CK IN the following events occur.

R40 connected to the DMA DATA CK IN line acts as a load resistor to the transmitting circuit which in the non sending mode is in a tri-state high impedance mode. The incoming high level pulse is differentiated by C2 and R29 and then, via isolating diode D5 and associated bias resistor R31, is connected to the C (clock) input of IC16.

The used half of IC16, a D type flip flop, functions with its D input connected to its Q output, i.e. such that it operates in a divide by two mode.

Assuming that Q of IC16 is initially '1', then at the event of a positive transition on its C input, the Q output changes to a '1' state, thus IC15's CS2 input (chip select) becomes enabled. At the same time IC15's CK input has changed from a '1' to a '0' level. The transition causes the data on lines I0 to I7 to be latched into the port and a low level on the service request output SR(NOT) to occur.

SC0 and SC1 are outputs from the processor which indicate whether the processor is performing a fetch, execute, interrupt or DMA activity, when carrying out a DMA activity
SC0 = 0 and SC1 = 1.

At the moment SR (NOT) goes low, the state of the system is not a DMA cycle, as a result the NOR gate connected to SC0 and SC1 (IC22 and IC23) cause a '1' state at pin 2 of IC23. Thus, the output (pin 3, IC23) of the NOR gate changes to a high level ('1'). A '1' level now exists at pin J of IC23, and since the SR (NOT) of IC17 has not been set to '0' then pin 6 of IC23 is a '0'. As a result of the transition of SR (NOT) from a '1' to a '0' level pin 4 of IC23 changes to a '0'. This signal is transferred to the microprocessor on its DMA IN (NOT) input which it recognizes as a request to DMA information into its memory. The internal logic of the microprocessor waits until the next system execute cycle has been completed and then suspends normal processor operation for one system cycle such that DMA may be executed. On doing so, the state code SC0 = 0 and SC1 = 1 is applied to the NOR logic gates of IC22 and IC23 resulting in pin 11 of IC23 changing from a '0' state to a '1' state. With the condition CS1 and CS2 at '1' status the input data is enabled onto the data bus and subsequently due to logic action within the processor is stored at a defined memory location.

At the completion of the cycle the SC0 and SC1 state revert to the code defining the next 'fetch' phase of operation, resulting in IC23 pin 11 output changing to a '0' state. The internal logic of the input port uses this transition to reset the SR (NOT) output to a '1' standby state, However, due to the finite delay between CS1 going negative and the reset of the SR output a condition exists at inputs 1 and 2 of IC23 whereby a second transient '1' pulse can occur. This race condition would activate incorrectly another DMA request at the microprocessor. To eliminate this timing problem, small capacitors are connected between IC23 pin 3 and ground and similarly between IC23 pin 3 and ground, namely C10 and C11. This short time delay effected by the gate output impedance in conjunction with the capacitor is sufficiently long to eliminate the effects of the reset delay propagation time of the input ports service request flip flop.

A second DMA DATA CK IN pulse would then have the effect of causing data to be input via IC17 due to the toggling action of IC16.

Because the program software needs to know the status of the master/slave bit of the input data before a DMA activity takes place, the hardware is arranged such that this data may be input by alternative means.

A second path to initiate the DMA process is included using an initializing clocking pulse derived from pin 6 of decoder chip IC13. This output is differentiated by C3 and R30, then via isolating diode D4 is applied to the C input of IC16 in similar manner to the DMA DATA CK IN input. By executing an output instruction to port 1 (which does not physically exist) a 2.75us active clock pulse is produced initiating DMA activity.

2.2.2.3.7. Input Data Buffer

Input data is received by the data bus from three sources:

1) Via IC6 and 7 which is head status data, as previously described.

2) By ports IC15 and IC16 acting in DMA mode, as previously described.

3) By IC14.

IC14 is a hex inverter/buffer with tri state output and is used to pass six control signals to the microprocessor. When its OD input is high ('1') its outputs are in high impedance mode, when the OD output is low input data is inverted and accesses the data bus. When an input instruction on input port 3 is executed by the microprocessor program, pin 7 of IC13 goes high for 2.75us and via the inverting buffer of IC22 enables the data output onto the data bus.

The six input control signals are as follows:

a) D5 input gives the microprocessor the status of the fire test switch. D5 receives this signal via the circuit involving R28, R25 and D2. When the fire test button is in a standby state a OV level exists at the fire test input to the logic card (edge connector pin 1). D2 is then forward biased taking current through R25 and off card resulting in D5 input to IC14 being at approximately 0.6 volts. When a fire test is requested the FIRE TEST input to the card will be at 7 volts. D2 now acts to block the 7V signal and the pull up resistor R25 serves to pull the D5 input to a '1' level.

b) D2 input gives the microprocessor access to the status of the fault test switch. The fault test input at pin 2 of the logic card edge connector is 0v in standby mode and at 7v when the fault test button is depressed. Associated components R27, D3 and R22 act in similar manner to that described for fire test input.

c) Inputs D1, D3, D4, and D6 of IC14 are associated with GSE (ground support equipment) operation. All four inputs are tied by pull up resistors to the system VDD rail by R21, R33, R24 and R26 respectively. In normal operating conditions, i.e. when GSE is not connected, the four GSE inputs to the logic card are open circuit, therefore, D1, D3, D4 and D6 present logic level '1's to the IC14.

The four GSE inputs allow the CCU operation to be controlled by the ground support equipment. Combinations of logic levels applied to these inputs select different programs for running. These programs are initialized by resetting the system causing the software program to interrogate the four GSE inputs and subsequently to run the required program.

System reset is effected by discharging C1 through D6 from the GSE RESET input at pin 41 of the logic card edge connector.

The above inputs are connected to the data bus via IC14 Q outputs as follows:

Input	Connected to	Data Bus
GSE 1		bit 0
FAULT SWITCH		bit 1
GSE 3		bit 2
GSE 2		bit 3
FIRE SWITCH		bit 4
GSE 4		bit 5

2.2.2.3.8. Output Data Buffer

Output data buffering (and latching) is effected by IC11, 12, 20 and 21. IC12's inputs are connected to the data bus. Data being latched into the port is controlled by CS1, CS2 and CK inputs. The mode input of IC12 is connected to VDD to characterize the device as an output port. With CS1 permanently connected to VSS the chip select has only to be satisfied by CS2 = 1 for data bus information to be latched into the ports outputs at the next occurence of a CK pulse. The microprocessor selects this output by an output instruction to port 4 which causes decoder chip IC13 to issue a 2.75us pulse at pin 12. This output is connected to IC12's CS2 input. The microprocessor then issues the required data to the data bus and timing pulse TPB which is connected as the CK input to IC12, effects the data latch.

The eight outputs from output port 4 (IC12) all have pull up load resistors connected (R13 to R20). Port bit operation is as follows:

O7 output (pin 12). This output is the time share output, a square wave pulse train generated by the system program. The time share waveform has a period of 334mS, 167mS high and 167mS low.

The time share waveform is fed via a buffer stage of IC21 and R4 to the head drive card which is then utilized to control high

voltage at the heads. The time share output is also fed via IC11's 'D' input and H output, this chip acts as a buffer to its input signals. With END input tied permanently to VDD input data is buffered directly to its output at H. This line is connected to a flag input on the opposite side microprocessor card (EF2)(NOT) and is used for monitoring.

O6 output (pin 19) and O4 (pin 15). These outputs , GSE2 and GSE 1, are each buffered by a buffer of IC21 and are connected to the CCU GSE plug. Both outputs transmit signals to the ground support equipment as confirmation of execution or at completion of execution of required program as dictated by the GSE I/P control lines.

When the system runs a fire detection program, software caused the GSE 1 line to follow the time share signal and the GSE 2 line to be at a '1' state onlu during when a head test is being performed. This operation is further described under the heading "Software".

O5 output (pin 7). This output is buffered by a buffer of IC21 the output of which controls power to the emitter via the head drive card as described in Section 2.2.2.1.

O3 output (pin 15) is an output called INHIBIT OUT. This signal is used as an inhibit signal on the common logic card; under standby conditions this output is at Ov. O3 is connected to the ENC input of IC11 which with a Ov on its input causes output 6 to be high impedance. When O3 changes to a '1' output, data at IC11's C input is transferred to the G output. Because C is connected to VSS, a change at G from high impedance to a 'O' state will occur. This output is also cross connected to the second microprocessor via the processor cards EF1 (NOT) input and is used by the software program. Further operation of the inhibit function is described in Section 2.2.2.4. and in the section headed "Software".

O2 output (pin 7). This output is the FIRE output which in standby conditions is at Ov, and at Fire conditions changes to a '1' state. The output is fed to the common logic card described in Section 2.2.2.4.

O1 output (pin 6). This output is the FAULT output which in standby conditions is at Ov. When a fault is issued the output changes to a '1' state. This output is fed to the common logic card as described in Section 2.2.2.4.

O0 output (pin 4). This output is termed DMA DATA OUT. Onto this output is loaded data to be transferred to the second microprocessor. IC11 acts as a buffer. With ENB connected to VDD, data at F follows data at B. The DMA DATA OUT line is then connected to DMA DATA CLOCK IN on the second microprocessor.

DMA DATA CK OUT at pin 19 of the logic card edge connector is derived via a buffering section of IC11 from a decoded output of IC13, which acts as the clock output for DMA data. DMA DATA CK OUT is connected to the second microprocessor as DMA DATA CK IN (see CCU circuit diagram 53813-203CD). (Reference 2-5.)

IC11 buffering also acts as a device to eliminate effects of differences in supply voltage of each microprocessor. IC11 allows level shifting to occur by connecting its VDD terminal to the positive supply of the processor recieving data and the VCC terminal to the positive supply of the processor sending data. Note all four outputs of IC11 are cross connected to the second microprocessor circuit.

The Q line output from the microprocessor is connected to a buffer on the logic card, this path is via edge connector pin 32 and buffer input pin 9 of IC20. The buffered output is connected to edge connector pin 33 and is termed GSE DATA. This line is connected to the GSE plug on the CCU and is used to transfer serial data from the processor memory to the ground support equipment.

2.2.2.3.9. Filtering

Capacitors C4 to C9 are connected in strategic positions across the power supply lines to filter out unwanted spurious supply borne signals and noise elements.

2.2.2.4. Common Logic Card (System A)

(Circuit diagram reference 43761-144CD) - Reference 2-11

The common logic card for a system A (dual microprocessor system) consists of three independent circuits.

a) Logic associated with fire and fault indication.
b) Driver circuits to energize output relays.
c) Circuitry which performs buffering and level shifting as inputs from the CWU.
d) Circuitry which detects impending switch off of power to the system.
e) Filtering circuitry.

2.2.2.4.1. Fire and Fault Logic

Fire and fault logic is determined by IC1, 2 and 4 and associated components.

Power for IC1, 2 and 4 is obtained by "ORING" both microprocessors 5.6v supply rails. Note that the circuit diagram refers to 'A' 5.6v and B' 5.6v refering to Side A and Side B of an 'A' type system.

D1 and D2 perform the power supply "ORING" function which is necessary such that if one procesor side power supply fails for any reason, the common logic card will still be capable of logic decisions based on the remaining good 5.6v rail.

As described in section 2.2.2.3.8, fire and fault inputs (for both sides A and B) are in the '0' state in standby conditions. The inhibit inputs for both sides are in a high impedance mode.

Consider the inputs to IC1, with (A) FIRE OUT at '0' pin 8 of IC1 via the inverter will be at '1'. The second input to this NAND gate at pin 9 will be '1' because (A) INHIBIT IN is high impedance and R11 acts as a pull up resistor. Consequently, NAND output pin 10 will normally be at '0'.

Similarly, considering (B) FIRE OUT and (B) INHIBIT IN input to IC2, pin 10 of IC2 will normally be in the '0' state.

NAND gate output, pin 4 of IC4 will therefore normally be at a '1'. This NAND gate of IC4 acts to effectively AND together fire conditions from both sides of the system.

When a fire is indicated by A FIRE OUT and B FIRE OUT both input pins 5 and 6 of IC4 will change to a '1' state causing the ouput pin 4 to change to a '0' state. If, however, only one FIRE OUT changes to a '1' state the AND logic is not satisfied and pin 4 of IC4 stays at a standby '1' state.

Fault logic is similar to that of FIRE logic, (A) FAULT OUT and (B) FAULT OUT under standby conditions cause '0' level inputs at pins 1 and 2 of IC4, therefore with no fault condition present, pin 3 of IC4 is at a '1' level. For a '0' output on pin 2 of IC4 both microprocessor FAULT OUT lines must signal a '1' (fault) level.

If one side of the system is shut off by the second side the AND fire and fault logic must effectivley change to OR. In the event of a side shut down by the second side, that second side will issue a '1' level at the inhibit output of port 4 on the logic card, which causes a change from high impedance to a '0' state on (A) or (B) INHIBIT IN line of the common logic card.

Take the example where side A processor has caused side B to shut down and caused (B) INHIBIT IN to change to a '0' state (Note that (B) INHIBIT IN is an input from side A logic card port 4 as can be seen from CCU circuit diagram). With (B) INHIBIT IN now changed to a '0' state pin 10 and pin 11 of IC2 will be to a '1' state.

The occurence of a FIRE condition ('1') at (A) FIRE OUT now causes pin 4 of IC4 to change to a '0' state. Similarly, the occurence of a FAULT condition (1) at (A) FAULT OUT now causes pin 3 of IC4 to change to a '0' state, effectively changing the gates function from AND to OR.

An identical logical operation is performed if side B causes side A to shut down, in that only B FIRE or FAULT lines need to change state to effect a transition at the output NAND gates of IC4.

2.2.2.4.2. Logic Drive and Output Circuit

From section 2.2.2.4.1., in the event of a fire condition IC4 pin 4 changes from a '1' state to a '0' state, and in the event of a fault IC4 pin 3 changes from a '1' to a '0' state.

2.2.2.4.2.1. Fault Condition

With no fault condition TR2 receives base current drive through R19 which in turn enables base current drive through TR3 via R27 and the conducting TR2. TR4 will also be switched on since its base current will flow through R29 and the conducting TR3. With TR4 switched on RLA will be energized via the 28v supply rail which feeds the logic driver stage.

With relay RLA normally energized at standby relay contacts RLA 1 and RLA 2 are open. Isolating diodes D14 and D15 are commoned together by their cathodes to comprise the fault drive output to the CWU. The isolating diodes are included such that relay contacts may be checked individually by GSE via the check points lines at edge connector pins 36 and 34.

When a fault condition occurs TR2 will turn off, TR3 turn on and TR4 turn off causing RLA to de-energize issuing a fault condition to the CWU.

2.2.2.4.2.2. Fire Condition

With no fire condition, TR1 receives base drive via R20 turning TR1 on. With TR1 collector developing only its saturation voltage base current supplied by R25 to TR5 is diverted through TR1 thus TR5 is switched off. Under standby conditions, i.e. with the fault state at standby TR6 will be switched on as TR3 is normally on.

When a fire input occurs TR1 will switch off causing R25 to feed base current to TR5. With TR5 and TR6 on RLB will energize via TR7 emitter base junction causing TR7 to switch on passing its collector load current through R34 to ground.

TR7 acts as a sensing circuit used to pass a confirmation signal back to the microprocessor indicating that the fire condition has successfully been initiated. With TR7 off, i.e. no fire condition, current flows from the A side VDD rail via R7, D3 and R34 and from the B side VDD rail via R8,D4 and R34 to ground. With R7 and R8 each 100k and R34 at 2.7K the anodes of D3 and D4 will be approximately one diode drop above the 0v rail. This FIRE TEST VERIFY and is connected to EF4 (NOT) input on the microprocessor card. For the second side the signal at D4 anode is taken via R2 to its EF4 (NOT) input on the microprocessor card.

When a fire signal is issued by the system TR7 turns on, connecting TR7 collector to the 28v rail. This reverse biases D3 and D4 causing R7/R1 and R8/R2 combinations to act as a pull up resistor on the microprocessor flag inputs. Therefore, when a fire condition occurs microprocessor EF4 (NOT) inputs change from a '0' to a '1' state.

2.2.2.4.2.3. Fault Override

With the series connections of TR5 and TR6, if a fire condition is being indicated a subsequent fault condition causing TR6 to switch off will make the fire condition at the CWU clear and indicate a fault condition, i.e. a fault condition overrides a fire condition.

2.2.2.4.3. Inputs from CWU

The CWU (as described in section 2.3) effects closure of a switch to the 28v rail if the fire test button is depressed and closure of a second switch to the 28v rail if the fault test button is depressed.

The fire and fault test inputs are routed to the FIRE TEST I/P and FAULT TEST I/P on the common logic cards.

With neither test button depressed both transistors TR8 and TR9 are switched off and both the FAULT TEST and FIRE TEST lines fed to the logic board, are at 0v.

When the fire test button is depressed R39 passes current because pin 22 of the common logic card edge connector is conneced to 28v at the CWU. D16, a 7.5v zener diode clamps the voltage level at the base of TR9, which, with R37, acts as an emitter follower stage. The voltage at TR9 emitter is then approximately 7 volts. Similarly, when the fault test button is depressed, a change of voltage from 0v to about 7 volts occurs at TR8 emitter.

Components C12 and C13 in conjunction with R39, R41, D16 and D17 act to eliminate interference entering the circuit via the cable connectors from the CWU.

2.2.2.4.4. Low Supply Voltage Detection

2.2.2.4.4.1. The Need For Low Voltage Detection

Low voltage detection is required to ensure correct operation of the system in the event of short duration loss of power and to ensure that memory data is not corrupted as discussed in section 2.2.2.2.

2.2.2.4.4.2. Operation of Low Voltage Detection Circuit

The circuit consists essentially of the quad comparator IC3 and associated components. The battery card (described in section 2.2.2.6.) supplies, under full charge conditions, a 4 volt power source to pin 26 of the common logic card edge connector.

(A) VDD RAM is a 5v input supply from the head drive card, this supply is fed via D18 as the supply voltage to the comparator IC3. Similarly (B) VDD RAM is fed via D19 to the comparator supply input. Operation is then such that if A supply fails the comparator continues to function due to the sustained presence of B supply, and vice versa. The battery input is connected directly to the comparator VDD input but high current does not flow from the VDD RAM line (at 5V) to the battery (4V) because a blocking diode is included on the battery card output line (See section 2.2.2.6.).

D18 and D19 are included such that in the absence of the battery (in production, since the battery card feature in for flight trials purposes only) VDD of IC3 receives current from either A side or B side VDD RAM supplies.

D7 clamps the battery voltage to 7.5V in the event of an open circuit battery, protecting the comparator and components which it controls.

Detection occurs seperately for side A and side B of system A, operation of which is identical, the following describes the operation of Side A low voltage detection.

Resistor chain R5 and R6 acts as a potential divider reference voltage which is fed to the inverting input, pin 4, of the quad comparator, this voltage is 1.25 volts. The non inverting input pin 5 of IC3 is connected to the low voltage detection arm of the bridge on the head drive card. (See circuit diagram 43761-143 CD) Under normal conditions the voltage is greater than 1.25 volts.

The potential divider chain of D10,R2, R3,and R71 on the head drive card is set such that the voltage at the R2, R3 and R71 node is 1.25 volts when the unregulated supply voltage (at D10 anode) is 8.1 volts.

At this unregulated voltage the 5V regulator on the head drive card functions correctly, however to obtain a voltage of 8.1 volts implies that the 115V supply has fallen below 85 volts A.C., this in turn affects the high voltage to the heads, below this supply voltage heads may not fire correctly. The action of the low voltage detection circuit eliminates this unwanted condition.

At normal conditions with Pin 5 of IC3 greater than 1.25 volts the collector transistor output at pin 2 of IC3 will be off.

A second low voltage detection circuit is that formed by the potential divider of R23 and R24 which feeds comparator inputs, pins 9 and 11. The Inverting inputs of these two comparators are connected to the 1.25V reference point. This detection network acts to detect the presence of the 28V supply. When the 28V supply is present the voltage at R23/R24 node is greater than 3 volts. Under all normal fluctuations of the supply rail, therefore, the transistor outputs at pins 13 and 14 of IC3 will be switched off.

IC3 pin 4 output is connected to IC3 pin 2 output both having a common pull up resistor R13. With both output transistors switched off, R13 causes the CS2 line, connected to these outputs to be at VDD RAM voltage.

If the 115V A.C. supply drops below 85 volts the voltage at pin 5 of IC3 will drop below 1.25 volts causing the output state of the comparator to change, a 0V condition will now exist at the CS2 line.

Alternatively if the 28V supply falls below approximately 8 volts, pin 9 of IC3 will now be less than 1.25 volts causing the output state of the comparator, pin 14 to change, again an 0V condition will result on the CS2 line.

Therefore, either a drop in AC line voltage or a loss of the 28v supply voltage causes the CS2 line to change from a '1' state to a '0' state.

Capacitor C2 ensures that VDD RAM voltage stays high for sufficient time for the correct comparator operation i.e. so that the comparator reference voltage is held high for a short period after the VDD RAM regulator input has dropped such that correct regulator is not taking place.

Assuming that the system has just been switched off, CS2 will change from a '1' state to a '0' state. As VDD RAM voltage collapses the VDD input to IC3 will be powered via the battery input. The VDD line now has battery voltage which is also fed to RAM memory on the microprocessor card, thus maintaining memory content. The change of state of CS2 to a '0' via D1 state disables the CS2 input of RAM memory on the microprocessor card, a change which must occur before the supply voltage drops out of range of that specified for correct operation of the microprocessor chip. For the system design the CS2 change of state to a '0' level occurs approximately 2mS before the 5v supply rail (VDD) begins to drop out of regulation.

The action of CS2 changing state also has effects on the logic card (see circuit diagram). The CS2 line via D1 of the logic card, causes the power-on reset capacitor to be discharged when CS2 changes to a '0' state, holding the CLR line at a reset state during the power-off period.

When power is restored to the system the following sequence of events occurs: VDD RAM line voltage will change from battery voltage to its normal running voltage level. At the same time, dependant on how quickly supply voltage on AC and DC supplies builds up, CS2 line will change to a '1' state. This will cause D1 on the logic card to become reverse biased allowing the power-on reset circuit to function. Subsequent removal of the reset condition causes D2 on the microprocessor card to become reverse biased and R12 causes CS2 to be pulled to a '1' level allowing RAM memory to become enabled.

This sequence of events ensures that all timing and initialization needs of the system are met.

2.2.2.4.5. Filtering Circuit

Diode D8 is an energy absorbing zener diode which clips incoming high voltage spikes. To keep power dissipation of D8 to safe limits yet allow all voltage requirements of the logic drive circuit to be met a fusible resistor of 15 ohm impedance is included in series with the 28v supply rail.

Diode D11 in series with the positive supply rail cuts off any effects of high negative voltage excursions on the 28v supply line.

Capacitors C3 to C11, C14 and C15 are active in reducing unwanted circuit interference.

2.2.2.5. Common Logic Card (System B)

(Circuit diagram reference 43761-146CD) - Reference 2-12

System B common logic card uses the same pcb as that for System A with minor amendments. The amendments are to make links at comparator IC3 such that the B side low voltage line detection circuitry is inactive, and to eliminate a NAND gate package (IC2 on System A common logic card) and associated resistors.

With the of IC2, operation of the fire and fault logic is as if A side has effected an inhibit on B side logic gating.

All other functions are as per System A common logic card description.

2.2.2.6. Battery Card

(Circuit component reference 43761-140CD) - Reference 2-13

The battery card is resident in System B only. It consists of two independant battery circuits suppling, in the case of Battery A output, power to System A common logic card battery input. This is performed by a connecting wire in the system harness on the aircraft installation.

Battery B supplies power to System B common logic card Battery input via the CCU mother board.

The battery cells B1 to B6 are sealed nickel cadmium cells with a 240mAH rating. A trickle charge current is fed to the cells via either D1 and R1 for cells B1 - B3 or D2 and R2 for cells B1 - B6. Isolating diodes D3 and D4 then pass battery current to the common logic card and RAM on the microprocesor card.

Design of the battery card was based on an average flight envelope of one and a half hours. Thus, to ensure that sufficient charge is stored during this period a relatively high trickle current is necessary. To attain this, a 240maH rating battery had to be used to ensure that over the operating temperature range the maximum allowable trickle current was not exceeded. The design ensures that a battery will supply the comparator on the common logic card and the RAM on the microprocessor card for 8 hours after a normal flight envelope.

It should be noted that the battery card is included only for flight trails and has an operating temperature range limited to -30° to +45°.

2.2.2.7. Filter Board

(Circuit diagram Ref: System A 43765-028, System B 43765-029) - References 2-14 and 2-15.
It is necessary for the control unit to meet the conducted emission, susceptability and transient requirements of MIL-STD-461A and MIL-STD-704A. This is acheived by three filter networks on the filter board for System A and two filter networks on the filter board for System B. To minimize the radiated emission effect of the incoming supply leads, the filter boards are mounted as close to the plug as possible.

There are two 115v filters on System A, and one 28v DC filter. The 115v filters are designated 115vA and 115vB. The components that make up 115vA are R1, D1, D2, D3 and D4 (transient voltage suppressors) R1,R3 and C2. D1 and D2 clip the incoming transient voltage on one half cycle to approximately 350v peak and D3 and D4 clip the voltage on the following half cycle. R1 provides some source impedance for the transient voltage suppressors to limit the current flowing during the transients. R1 is a fusible resistor which will blow if the circuit exceeds a constant

current of approximately 0.65A. R3 and C2 act as a radio frequency suppressor. Similarly, components D5, D6, D7, D8, R2, R4 and C3 make up the 115vB filter. The 28v filter is made up of three components on the filter board. L1 and L2 slow up incoming and outgoing current transients, and C1 suppresses incoming voltage spikes. Further filtering of the 20v DC supply is carried out on the common logic card as discussed in Section 2.2.2.4. Similarly, System B has the same filter with the exception of 115vB which is not required.

2.3. Crew Warning Unit(CWU)

(Circuit diagrams ref. 53813-202-CD) - Reference 2-16

The Crew Warning Unit gives visual indication if either a fire or a fault is detected on either of the aircrafts engine fire detection systems.

2.3.1. Construction

General assembly drawing 53813-202A shows the units construction which is contained in a rectangular box made from stainless steel. The front panel is (2") high x (6") wide, and is retained to the box by means of two screws. On the front panel are six switch/indicator assemblies mounted in three groups of two. The outer two groups are indicators and the inner groups are switches. There are also four pillars mounted on this panel which support a circuit board and the remaining components. The switch indicator assemblies are connected to the circuit board and to a square flange bayonet recepticle by means of P.T.F.E. wire. This recepticle is bolted to the inside of the bottom of the box by means of four screws. The cable harness is of sufficient length to allow the four panel assemblies to be removed from the box to enable any necessary repairs.

The indications are of the sunlight readable type to MIL-S-22885/90 and the legends "FIRE" and "FIRE DET-FAIL" are only visible when illuminated. As these indication/switches are not of the waterproof type it is necessary to have drainage holes on each corner of the bottom of the box.

The unit is mounted in the aircraft by means of four DZUS fasteners, two on each side of the front panel.

The unit has a natural polished finish apart from the front panel which is painted matt black, and has an overall size of 6" wide x 1.75" high x 5" deep. The approximate weight of the unit is 600g.

2.3.2. Circuit Description

The crew warning unit performs three functions:

i) Fire and fault indication.
ii) Fire and fault test.
iii) CCU reset.

2.3.2.1. Fire and Fault Indication

For increased reliability, LP1 - LP4 are wires in parallel and provide the left engine "FIRE" indication when supplied by a 24 volt signal from the common logic card in the left engines control unit. Similarly, LP5 - LP8 provide the left engine "FIRE DET FAIL" indication.

LP9 - LP12 provide the right engine "FIRE DET FAIL" indication when supplied by 24 volt signals from the common logic card in the right engines control unit. Similarly, LP13 - 16 provide the right engine "FIRE DET FAIL" indication.

2.3.2.2. Fire and Fault Test

There are two test button facilities "FIRE DET TEST" and "FAIL IND TEST". The first test button "FIRE DET TEST" is a two pole normally open momentary action switch S1. When the switch is depressed, S1a contacts close and supply 24volts to the fire test input on both common logic cards via D1 and D2 isolation diodes. This action energizes the test emitters as detailed in Section 3.4.3.2., and both FIRE indicators light.

The second test button "FAIL IND TEST", is also a two pole normally open momentary action switch, S2. When the switch is depressed, S2a contacts close and supply 24v to the fault test input on both common logic cards via D3 and D4 isolation diodes. This action generates a fault as described in Section 3.4.3.2., and both "FAIL IND TEST" indicators light.

The 24v that supplies these switches is filtered to minimize radio frequency pick-up. D5 is a reverse voltage protection diode. L1 suppresses the radio frequency currents and C1 decouples the radio frequency voltages.

2.3.2.3. Control Unit Reset

The "FIRE DET TEST" and "FAIL IND TEST" [illegible] switch provides a second function. When the control units [illegible] a fault mode it is necessary to reset them. This can be achieved by depressing these switches in a particular sequence as described in Volume I . S2b connects control line 2 to 0v and S1b connects control line 2 to control line 1. Control lines 1 and 2 feed to both control units as shown in installation drawing 222004. (Reference 2-17)

3.0 SOFTWARE DESIGN

An overview of the software system is given in para. 3.1 followed by more detailed discussion of the software segments.

3.1. Overview of Software

The system software resident in 3K bytes of ROM memory serves to control timing functions of the system, to process and act on fire data and to effect many system tests designed to prove the integrity of the system.

The assembled program listings are contained in Appendix A-2, all software description refers to the relevant program and should be read in conjunction with the system flow diagram 53813-203 and 204 FD. (Reference 3-1)

Program structure is such that the majority of functions occur under interrupt control due to the time dependant nature of the system requirements.

3.1.1 Software Component Programs

A cyclic operation occurs after the INITIALIZATION program has been completed, in which the two sides of the system (if System A) are synchronized and all required registers and memory locations are set to initial values.

After initialization the BACKGROUND program is entered, the primary function of which is to carry out tests to prove that ROM memory is not corrupt. This program is interrupted at intervals of 832 us to carry out the INTERRUPT program.

The interrupt program has two phases, GATHER and PROCESS, both are responsible for system timing. During the gather phase the sides time share is high and at each interrupt event the main function is to obtain head data. This phase lasts for 167ms.

On completion of the gather phase the time share changes to a low level and the PROCESS phase commences, this also lasts for 167ms.

At each interupt event during the process phase, system timing and system interrupts are monitored.

The FIRE program is responsible for processing the head data and computing if a fire or fault condition is to be set or reset. The fire program is executed after the gather phase of the interrupt program and is entered from the background program. Consequently the fire program is interrupted every 832 us meanwhile background operation is suspended. Upon fire program completion background operation resumes.

The final major element of the software is the GSE program which is executed upon command of the remote test equipment.

3.1.2 Program Development

All programs were edited and assembled using an RCA development system apart from the fire program and parts of the GSE program which were compiled using a tie to a main frame computer.

Main frame written program was debugged in the same medium and then combined with the remaining program which was then debugged using the RCA development system and associated emulator.

3.1.3 Program Instructions and Language

Appendix A-3 contains a summary of the instruction set and their function of the 1802 microprocessor.

Appendix A-4 summarizes the level 2 assembly language used in the listing of the fire and part of GSE program.

3.1.4 RAM Memory Allocation

Fig. 3-1 maps the useage of memory locations in the RAM area between locations OCOO and OCFF.

3.1.5 Register Allocation

Fig.3-2 shows the major useage of microprocessor registers.

3.1.6 Flags and Interrupt Data

The major memory locations utilized for flags and input data is shown in Table3-1 where individual bit useage is identified.

3.2. Initialization Program

The function of the initialization program is to set registers and memory locations such that upon entry to background, interrupt and fire programs, correct program operation occurs.

The second main function of the initialization program is to cause correct start up and phasing of the two processor sides if the system is A type.

3.2.1. Memory Locations and Register Initialization

At start up interrupts are disabled (line 4) and program control is moved to register P7 (line 10) Power-on reset causes program counter R0 to be reset to H'0000' and program runs from this program step under control of R0. Operation must be moved away from R0 control because the DMA capability utilized by the hardware required R0 to act as a memory pointer to which data is being passed.

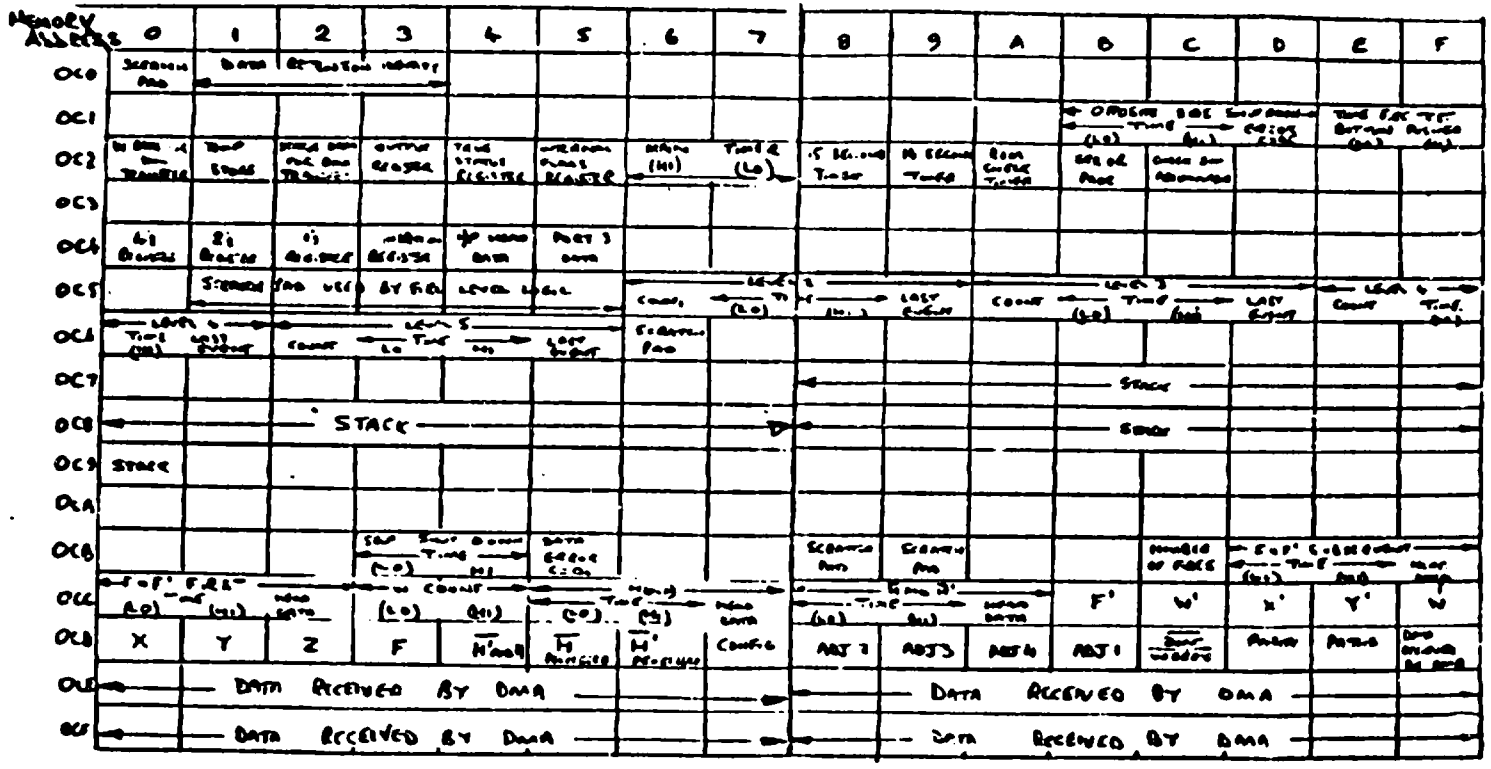


FIGURE 3-1 RAM MEMORY MAP

REGISTER	USEAGE
R0	DMA Memory Pointer
R1	Interrupt Program
R2	Stack Pointer
R3	Background Program
R4	Used By Interrupt Program
R5	Lower Half Used As Interrupt Timer Upper Half Used As Temporary Store In Interrupt Program
R6	Used By DMA Program
R7	Initialization & GSE Program
R8	Used As Subroutine Pointer
R9	Used As Subroutine Pointer
RA	Used By Fire Program
RB	Used By Fire Program
RC	Pointer To ROM For Background Program
RD	Used By GSE Program
RE	Used By Fire Program
RF	Used By Fire Program

FIGURE 3-2 REGISTER ALLOCATION

TABLE 3-1
MEMORY LOCATION USEAGE

MEMORY LOCATION	IDENTITY	BIT ALLOCATION 7	6	5	4	3	2	1	0
OC22	DMA Status Register	-	-	-	-	Rom Check Data	H' Data	Parity 1	Parity 2
OC23	Output Status Register	Time Share	GSE 1	Head Test	GSE 2	Inhibit	Fire	Fault	DMA Data
OC24	True Status Register					Inhibit	Fire	Fault	
OC25	Internal Flags Register	Fire Button (High)	Test Flag	Fire Button (low)	Other Proce- ssor Dead	Rom Check	Head Test	Fault Button	Enter Fire Program
OC45	Port 3 Data	-	-	GSE 4 I/P	Fire Button	GSE 2 I/P	GSE 3 I/P	Fault Button	GSE 1 I/P

Registers are initialized for pointing to RAM memory locations specifically R0, the DMA pointer, R2, R5, RA and RF (lines 12 - 15).

At this point, program operation determines whether it is to run the fire program or under control of GSE. The hardware input, bit 5 of port 3 called GSE 4 INPUT, is set to a '1' if GSE is disconnected and '0' if GSE is connected and active. Program steps at lines 18 to 20 determine the GSE status. If GSE program is to be run a jump to the separately described GSE program occurs.

A fire program will automatically occur if GSE is not connected.

Program then determines whether it has data retained in memory from a previous flight. To perform this, three locations are allocated to storage of an identity pattern. On start-up, all RAM locations will be in a random bit pattern if the battery is not holding RAM supply voltage up. By setting the three locations to a bit pattern, A5,A5,A5, the program can determine whether the memory should be reset.

If data has been retained from a previous flight and memory not read out (and subsequently reset) by the GSE then the pattern A5,A5,A5 will exist at locations OC01, OC02 and OC03.

The program at lines 21 to 43 check for the A5,A5,A5 pattern, if confirmed the memory is not reset. If not confirmed, the program utilizes a subroutine RMTAR, described in Section 3.2.4. to test and reset to zero all locations of the volatile memory (note that this reset function serves to reset the main timer at location OC26 and OC27). Subsequently, locations OC01 - OC03 are all set to contain bit pattern A5.

The initialization program then sets the H(OLD) location OCC7 to H'FF' indicating at this stage that all heads in the system are good. Subsequent head tests and fire program will then modify this location according to the aircraft configuration and number of heads utilized within that configuration.

Program lines 44 to 50 effect zeroing of memory locations referred to on the memory map as W,X,Y,Z,W',X',Y',F and F'. These locations are used by the fire program and are further described in Section 3.5.

The processor side now needs to know whether it is to act as a master or slave processor. The purpose of this hardware input is to enable software to set the operation of the two sides such that they are functioning in anti-phase, i.e. while say, side 1 is in the gather phase, side 2 will be in the process phase.

To input the hardware status of the master/slave bit, which is resident on DMA input ports, it is necessary to effect a

bootstrap DMA operation and then to run software checks on the input data. This operation is performed between lines 51 and 71 and is identical to that described in Section 3.5.1.1.

The configuration data of the DMA ports i then stored at location OCD7 and is called the configuration yte (lines 72 to 74).

For correct operation of its first pass it must appear to the fire program that DMA data has been received from the second processor. To effect this the low bits of memory locations OCDF to OCE6 must be set to 1,1,0,0,1,1,0 and 0 respectively. This is effected between lines 75 and 79.

At line 80 che program looks to see if the inhibit line into it has been flagged high by the second side. This operation is included here to eliminate the possibility of the return to a functional state of one side after its power lines have been interrupted. This is necessary because the system cannot reconfigure tc a two sided system once one side has exhibited a fault condition. Therefore, if a system started with both sides functional, and then say side 2 failed due to a power supply interruption, side 1 would reconfigure to a single sided system and raise its inhibit flag line. In the unlikely event of side 2 being repowered while side 1 is still running, the software of lines 80 and 81 ensure that the side runs into a latching fault LACHFL routine, effectively running in a passive loop.

Timer constraints explained in Section 3.4.3.3. are then loaded to memory locations OC28,OC29, and OC2A (lines 87 to 89). This is followed by clearing memory locations OC20 to OC25, locations used by the gather phase of the interrupt program (lines 91 and 92).

Line 93 sets parity bits for transfer by DMA activity as discussed in Section 3.4.4.

3.2.2. Start up Timing

Assuming that the system is A type, it is necessary to ensure that both sides are synchronized in a manner so that one side will issue its time share high (allowing hardware to pass high voltage to the heads) and the second side will issue its time share low (such that its heads are off line). Subsequent timing of the two sides operation is then accomplished by the interrupt program.

What must be taken into account is the fact that both sides may differ slightly in the time taken to reach a given point in the program. This difference is a function of the tolerance of components associated with the "power-on reset" circuit and tolerance of the crystal and hence the system clock.

Program execution between lines 96 and 145 takes the above timing discrepancies into account, operation of which is as follows:

When program execution of say, side 1 reaches line 96 a hardware flag is output on the time share output line of port 4. This flag output is also directly connected as a flag input to the second side on its EF2 (NOT) input. Conversely, the EF2 (NOT) flag input to side . signals the status of side 2 processors time share line.

Allowance is made for the possible delay of the second side reaching the point where it issues a flag '1' level on its time share line. A time delay is built into the program, throughout which a check to see whether the EF2 (NOT) input has changed state. If the time delay times out (approximately 6 seconds later) before side 2 issued EF2 (NOT) = 1 then the second side is inhibited. Lines 98 and 99 load the delay constant to the timer and program jumps to line 110 to execute the delay. After each instruction the status of the EF2 (NOT) flag is checked. If it changes state the delay program is terminated by a jump to label HALF.

If the delay program times out it is presumed that the second side has failed to start (or that the system is type B). This results in the logging of an error code to a location reserved for codes which effect shut down of the second processor. The time of shut down is also logged. Locations used are OC1B and OC1D.

Assume again that correct start up of both sides has occurred then the slower side, on entry to the time delay program, will immediately exit from same because the quicker side has issued a time share '1' flag and is at this time executing a delay sequence. At the moment the slowest side issues a high time share output, synchronization has been achieved and both sides proceed to the next step by determining at line 103 whether they are master or slave. If the side is master, program jumps to label GO on line 128.

If the side is slave, the time share line must be reset to '0' i.e. heads off line (at line 107).

3.2.3. Further Housekeeping Requirements

Further housekeeping requirements for correct entry to the fire and interrupt programs must then occur. Line 108 sets R0 to OCFF, because subsequently the slave side goes directly (via the background program) to the fire program, this program expects to see OCFF in R0 as if a DMA transfer has taken place in the previous gather phase. Because at this time no prior gather phase has taken place for the slave side, it must be simulated. A flag is then set in the internal flags register, OC25 such that the fire program is immediately entered via the background program described in Section 3.3.

Program execution has now reached label GO at line 128. At this point the interrupt program counter R1 is loaded with the start address of the interrupt program (H'0606').

Register R2, the stack pointer, (described in Section 3.4) is initialized to point at stack memory location 0C90 and R5 and R6 are initialized to suit the needs of the interrupt program.

It is necessary to process the configuration byte before entry to the fire program. This is effected by setting the address of the program ADJSET in R9 and then executing a subroutine call at line 136, the resultant parity checksum generated by ADJSET is stored at 0CDA by line 137.

After enabling interrupts to occur (line 138) program control is passed to R3 and execution resumes via the background program.

3.2.4 Ram Test and Reset Routine

This subroutine is called by the initialization program and the GSE program. Its function is to perform a test on all random access memory locations and then to reset them all to zero.

Program listing is shown from line 146 of the initialization program.

Entry to the program is at line 149, all locations are checked by loading AA to each, followed by reading them back to the accumulator and executing a check to ensure that the write operation was correctly performed. This is repeated by writing 55 to each location. Failure to respond correctly to the test results in the loading of a fault identity and a jump to the LACHFL routine.

Following the above test all memory locations are reset to zero and the program control is returned to the calling program.

3.3. Background Program

The background (or main) program performs a continuously cycling test on the content of the read only memory, thus ensuring that at all times, all program steps are correct. This is necessary particularly in the case of routines that are not flexed in the course of normal operation or when FIRE or FAULT buttons are pressed, for example LACHFL.

In effect this program is split into 12, 256 byte pages. Each page is checked individually by adding all bytes together, the resultant byte (ignoring all carries) is then compared with a checksum stored in a convenient area of the memory. Failure to check out correctly causes the side to shut itself down.

As a confidence check the second side allows a given time for the primary side to carry out the check (and vice versa). The second side, as part of the interrupt program, down counts a register. If the counter reaches zero before the primary side indicates (via DMA transfer) that the operation has been completed on all ROM a fault condition is issued by the second side and effects a shut down of the faulty side by issuing a high on its inhibit line.

The background program is functional only when head data is being gathered, i.e. when time share of the side is high, and the program operation allows only one page to be checked per gather phase.

Further operation of the background program is to control the entry to the fire program.

3.3.1. Background Program Operation

On entry to the background from the initialization program, a register is set up pointing to RAM, this pointer is initially set to OCOO, i.e. 1 byte above the highest program bit (OBFF), this occurs on lines 0010 and 0013.

A memory location is assigned to act as an accumulator for ongoing result of the addition of each memory byte within the page being checked. This memory location is OC2C.

A check to determine whether time share is high or low is then carried out at lines 14 and 15, the check is carried out once, i.e. on entry to the background program from initialization and allows immediate transfer to the fire program if the side is slave.

The same check is then carried out at lines 17 and 18 as part of the cyclic operation of the program.

To ensure that only one page of memory is checked per gather phase the check at line 19 is included.The interrupt timer R5 (0) which counts down from H'C8' at the start of the gather phase, to H'13' at completion. Checking for the R5 (0) value being less than H'C0' gives a window of eight interrupt occurrences for the page check to be started. Because the page check will take more than eight interrupt periods, only one page is verified per gather phase.

The test at line 19, if passed, leads to the checking of a page of ROM. The accumulator at OC2C is then rezeroed. (line 22).

Program lines 23 to 26 get each ROM byte as pointed to by the pointer and adds them into the accumulator. At the completion of the page the resultant accumulator value is compared with the check sum values stored at memory locations 0800 to 0808.

Location 0800 points to page 0 checksum, up to location 080B which points to page B checksum. The fact that the lower byte value of the memory location is the same as the page number is utilized by the program to access the checksum value (line 28 and 29). Lines 30 and 31 execute the checksum comparison with the page accumulator, failure to compare correctly results in the loading of a fault identity and a jump to the LACHFL routine (line 48).

With the page correctly checked, the page pointer is initialized to the next page below or if zero page has just been checked, back to page B. (lines 32 to 36)

Program continues by returning to the label HELIUM by this time the interrupt counter is below H'C0' and no new page of program is checked. Instead program jumps to line 49 where it wants to see the occurrence of a flag which allows it to proceed to the fire program. This flag (bit 0 of 0C25) is set by the interrupt program at the completion of the gather phase (line 146 of gather phase interrupt program). When the flag line is set, program proceeds at line 51 where parting bits of the DMA status register are loaded before passing program control to R7 which is the fire program pointer.

At the occurrence of subsequent gather phases the next page of ROM is checked as pointed to by the high byte of the ROM counter. When the check at line 34 indicates that all pages have been checked program jumps to line 38. A flag is set at bit 3 of the internal flags register at location 0C25 which is used as an indication that the ROM check has successfully been completed.

Program then repeats RAM checking from page B to page 0, in a continuous cycle.

3.4 Interrupt Program

3.4.1 Interrupt Program Common to Gather and Process Phases

The interrupt program is responsible for timing of the two phases of operation, i.e.gather and process phases.
The phases are so called because during gather, head data is being input to the system and during the process phase the received data is being processed by the fire program.

The interrupt program also performs logical operations on the head data as it is received and is also responsible for transfering data to the output port from the output register. This data is loaded to the output register at various points throughout the background and fire program, there will therefore in most cases be a finite delay (less than 832 microsecs) betwen an output state being requested and being executed.

The program is entered at line 72 of the gather phase listing of the interrupt program. Register R2 is pointing to a stack in memory such that on entry a new free area of stack is made available by operation at line 72. The T register (which contains the X and P pointer register values immediately after the interrupt event) is then saved in the stack, another free area is made available and the value of the accumulator (D) and the carry flag (DF) are also saved in the stack.

At lines 78 to 80 a memory location is pointed to which is to save the new state of the 8 heads available as input port 7. Memory location 0C44 is the location used. Instruction on line 83 effects the storage of the head data.

The program next checks to determine whether the test flag is set. The test flag is set by the last interrupt of the process phase when it computes that 15 seconds has elapsed since the last head test. If this flag is set the effect of program lines 87 to 94 is to set the output port 4 with FIRE = 1, INHIBIT = 1, HEAD TEST = 1. This is copied from the output status register, however the true status register does not have FIRE = 1 and INHIBIT = 1 because the real condition is that a fire does not exist the output is only as a response to a test condition.

At this time the internal flags register is also copied to R4(1).

The head test output at '1' causes the emitters at the detectors to fire such that during this gather phase a large number of pulses is input to memory allowing the fire program to verify quality of heads.

The fire and inhibit line outputs at '1' level allows the output relay to operate, in fact due to the speed of software operation, a signal at EF4(NOT)input will change state and be verified before the mechanical contact has time to change over. The result of verification is to immediately set inhibit and fire outputs back to zero.

Line 96 of the program checks to see whether the result of the output to fire and inhibit lines has resulted in the feedback check path to EF4(NOT) changing state.

If the change has occurred and the test flag was set it is reset and the fire and fault signals returned to zero (if a true fire was not existing at the time the test was performed). To verify this, reference is made to the true status register, operation of this conditional reset is documented between lines 183 and 198.

The EF4(NOT) line will also be indicating a fire condition at the output if a true fire exists or if the opposite processor is conducting a test on the output circuit, these conditions are tested between lines 172 and 182. If the conditions are met then

program operation continues at line 99, otherwise the EF4(NOT) line has been raised in response to a hardware circuit failure and the side is shut down by entering a fault code and branching to LACHFL.

If the condition at line 96 is such that no return signal at EF4(NOT) has been received then this is conditional on whether a test had been initiated. If the test had not been initiated, then no high signal would be expected and program continues at line 99. If however a test had been initiated and no response has occurred, several reasons exist for this. They are that the fault output is set, and because in the hardware of the common logic card fault over rides fire, no return confirmation will occur. Or because the second sides inhibit line is raised. Failure to meet these conditins indicates that the lack of response to the test is a function of hardware failure and a fault is issued via the LACHFL routine. If the conditions are met operation contines at line 99.

At line 99 the interrupt timer, which controls the duration of the time share period is decremented.

At line 104 it is determined whether the time share line is high or low and program divides accordingly.

3.4.2 Gather Phase Program

If at line 104 time share is low the gather phase program starting at line 107 is executed. The head data stored at OC44 is processed in the manner described in section 3 of Appendix A-1 such that the FOURS, TWOS and ONES COUNT is generated, this is peformed (lines 108 to 129) in such a way that when all three registers are full no overflow occurs.

FOURS, TWOS and ONES data is stored at locations OC40, OC41 and OC42.

The data so stored can represent up to a maximum of 7 counts in one gather phase, i.e. if bit 0 of each location is set to a '1' the head 1 has gathered a minimum of 7 strikes in the gather phase. At each occurrence of the interrupt program during the gather phase the three locations are updated according to the latest data available from the heads.

On completion of the head data processing the program determines whether the gather phase is complete by looking at the count in the interrupt timer counter (line 131). If the count has reached D'13' then the number of interrupts since the start of the gather phase has been 200 (the interrupt counter was initially set to D'213'). As each interrupt is 832 microsecs apart it follows that the total length of the gather phase is 832 x 200 microsecs ie 166.4 mS.

If the count has not decremented to D'13' program returns to background operation.

If the gather phase is complete, operation determines firstly whether the completed phase was one where a head test was carried out, i.e. with emitter struck. The head test line of the output register is looked at (line 133 to 137) if high the last phase was a head test.

Program operation then verifies whether the emitter circuit has fired, this is carried out by observing the EF3(NOT) status.

Two conditions then exist, if the head test was requested, the EF3(NOT) line should give a positive verification, program execution jumps to line 148 and the EF3(NOT) line is checked. If the verification shows that the emitters had not received a strike initiating voltage a fault code is loaded and a jump to the LACHFL routine occurs. This is necessary as the system would otherwise be unaware of the status of heads (lines 164 and 165). If the flag line shows that emitters do have a strike voltage applied, the head test line (and the GSE 2 line which mimics it) is reset at line 157.

A short delay of approximately 160 micro secs is then initiated at line 159. When this times out a further check is carried out to determine whether the emitters have cleared in response to line 157. The delay is necessary to ensure that head circuit capacitance does not influence the result of the test at line 161 where again the emitter voltage is examined. If for any reason (i.e. a hardware failure) the emitter voltage remains high a fault identity is loaded and a jump to the LACHFL routine occurs.

If no head test was requested during the last gather phase, program continues at line 138 at which the emitter line EF3(NOT) is checked. Program expects to find that the emitter line voltage is low, however if the flag indicates that it is high (due to a hardware failure) then a fault identity is loaded and a jump to the LACHFL routine occurs.

Program operation has now reached line 140 at which the interrupt timer is reloaded to a count of 213 ready for timing of the next process phase. The time share output (and GSE1 output which mimics it) is reset to zero such that the heads are taken off line ready for the process phase (lines 142 to 145).

Before returning to the background program, the fire program flag is set (bit 0 of memory location 0C25), this enables the background program to pass control to the fire program as explained in Section 3.3.

Exit from the interrupt program commences at line 66 where the statuses D, DF, and T are recalled from the stack and reloaded appropriately ready for the return to the program that was interrupted (at line 71).

3.4.3 Process Phase Program

The process phase program starts at line 66 of the listing titled "Process Phase Interrupt Program"

The primary function of this program segment is to perform and monitor timing functions of the system. The program ensures that the duration of the process phase is correct and monitors the second side to ensure that it is effecting correct timing of the gather phase.

At line 66 the first check is to determine whether the second side is functional, this is executed by checking the internal flags register which has previously been duplicated to register 4.

3.4.3.1 Process Phase Operation for a Currently Fault Free System A

The program contines at line 70 and commences to carry out timing checks on the second sides time share output.

The gathering and processing sides will both be decrementing their respective interrupt times at the rate of one per interrupt event. When the gather side decrements to a count of 13, at which stage it changes its time share output from '1' to '0', the process phase interrupt timer should also contain approximately 13, errors will exist due to component tolerances. If the process phase timer decrements to zero before the gather phase time share changes from '1' to a '0' state, then the timing is sufficiently in error for the side acting in process mode to effect the shut down of the second side.

Program at line 70 checks to determine whether the interrupt timer has reached 0, if it has program jumps to line 192.

The internal flags register is checked to see if the second side is already inhibited, if not it up dates the register and loads an inhibit flag to the true status register (line 196). An error code is then loaded to the location (OC1D) defining the reason for a second side shut down and the time at which the event took place is copied from the main timer counter to locations OC1B and OC1C (lines 197 to 203).

The output register at OC23 is then copied with an inhibit flag which is subsequently output to hardware at the next entry to the interrupt program (line 204 and 205). A jump to the program segment which is functional only at the completion of the process phase then occurs (Section 3.4.3.3.)

If the interrupt timer has not decremented to zero the time share status of the second side is checked to determine whether it has changed to a zero.

If a change of the second side from a gather to a process phase

is indicated, program continues at the segment which is functional at the completion of the process phase (section 3.4.3.3.)

If no change of the second side from gather to process is indicated, program continues by handing control to the DMA program explained in section 3.4.4.
On return from the DMA program the interrupt program is exited via the status restoration path explained in section 3.4.2.

3.4.3.2. Process Phase Operation for a Faulty System A or a System B

Operation in the process phase is identical for a faulty second side and a system B. In both cases at some time previously bit 4 of the internal flags register has been set high. The result of the test at line 68 is then to cause program to jump to line 188.

When one processor side is off (or not included as the system B case) timing control is effected by the good side. To perform this the interrupt timing register is checked to determine if the process phase is completed (line 189). Time out occurs similarly to the gather phase when the register has decremented to D'13'. If time out has not occurred, program control returns to the background program via the exit route which reinstates saved conditions. If the time out has occurred a jump at line 190 to line 75 is effected.

3.4.3.3 Program Operation at Completion of the Process Phase

After the last interrupt has occurred in the process phase, i.e. when the interrupt timer has decremented to D'13', program will be routed to the listing from line 75.

The first step is to set the time share output to a '1' (and to set its mimic GSE 1), this is performed between lines 75 and 80 where the new data is first copied to the output address register before being output to hardware.

The interrupt timer is then re-initialized to a count of 214 ready for the next gather phase.

Lines 83 to 96 process bit 3 of location OC25, the RAM check status bit. This bit will periodically be set to '1' by the successful completion of all RAM memory locations. The bit is transferred, by masking, to bit 3 of the location involved in DMA transfer i.e. OC22. At the same time the flag at bit 3 of OC25 is reset such that another successful RAM check will re issue the flag.

Lines 98 to 100 then reset the head test and fault status bits of the output register to zero, new data is then copied in at the commencement of the next interrupt.

The condition of the fault and fire buttons are then tested to determine if a test is requested. The button status' are input at line 103 and masked to eliminate unwanted data on this input port, the result is stored at R5 (1). The fault flag is then copied into the flags register and the output register. Operation (between lines 107 and 120) is such that if the button was previously depressed and is now clear the flag and output register condition is cleared.

Line 121 to 131 perform the same function for the fire button, the flags register and the output register is set or reset accordingly. However in this instance the fire button results in raising the head test bit of the output address register to a '1'. This in turn causes the emitters to be active on all subsequent gather phases while the fire button is being depressed. The result therefore is that a fire condition is initiated at the CWU as a result of the emitter stimulus. In this way a test of the system logic is performed.

In the case of the fault test the fault lamp being illuminated at the CWU is only a check on common logic hardware.

When the fire test button is pressed, the time of depression is logged in memory locations OC1E and OC1F by copying the main timer content. This is carried out such that GSE can compute event times with respect to the time that the fire test button is depressed. With the pilot directive that the absolute time of the fire test must be recorded during pre-flight checks, a method of relating events during flight to real time exists.

Line 143 then effects the output of fault line and head test line requirements according to the demands of the test buttons.

At line 144 the memory location which contains the ROM check timer is decremented and checked to determine whether it is zero. This function acts as a check on the second side and is a race against the successful completion of the ROM check. For example side 1 will perform a ROM check every 12 time share periods at the end of which a flag is DMA transferred to side 2 to state that the test has been completed. On receipt the fire program resets the ROM timer to a high value. If the timer times out before the next receipt a fault is indicated implying that side 1 has not completed the test in the time specified.

At line 149, if the ROM timer has decremented to zero, program jumps to line 209 where a check to determine whether the second side is already logged as faulty is carried out. If not lines 210 to 218 outputs an inhibit to the output and true status registers and stores a fault code and time of fault at locations OC1B to OC1D. If the fault condition is new or not, program continues at line 219 where the inhibit condition is stored in the output register for subsequent output at the next entry to the interrupt program.

A similar procedure to the ROM check race is used to check that the second side is performing a head test every 15 seconds.

The counter at location 0E29 is decremented at the completion of the process phase. If it times out before the occurrence of the second side's head test a fault condition is initiated. When the second sides head test is performed the DMA status transmitted reflects this and the fire program re-initializes the counter (see Section 3.3.2.2)

Line 150 to 153 decrements the 16 second counter and checks for zero content. If the count is zero a jump to line 223 occurs. A check is carried out to determine if a fault has previously been initialized by this route, if not flags are set at bit 4 of the internal flags register and bit 3 of the true status register. An error code and time of error is then loaded to locations 0C1B to 0C1D (lines 226 - 234). At line 235, if the fault condition is new or not an inhibit bit is loaded to the output register.

Program next jumps to line 154 at which the timer responsible for setting a head test at 15 second periods is decremented. The timer (at location 0C28) is then checked for zero content.

If the timer has timed out at line 158 the timer is reset to its initial value.

The main timer is then incremented at lines 158 to 166 taking into account the fact that the counter is two locations wide and incrementing the high byte if overflow from the low byte occurs.

Note that the main timer is incremented once every 15 seconds thus all data events are recorded against 15 second markers.

At lines 167 to 177, to prepare the next gather phase for a head test, bit 2 of the internal flags register, the head test bit is set. The output register head test bit and its mimic GSE 2 is also set to '1'.

The internal flags register test flag (bit 6) is then set to 1 at line 178 to 182. The new output register status is then output at line 184 causing hardware to pass a high voltage to the emitters.

At line 185 whether the 15 second period was completed or not, R6 is loaded with requirements of the DMA program (section 3.4.4.). The process phase is completed by returning to the background program via the exit routine at line 66 of the gather phase program where saved conditions are reinstated.

3.4.4 DMA Program

The DMA program takes data from memory locations 0C20 and 0C22 and transfers it out serially via bit '0' of the output port.

The required sequence of events is to set or reset bit '0' according to the data bit being transmitted. An output instruction to port 1 which acts as a clock pulse effects data latch into, and initiates DMA operation of the second side. The cycle repeats until all data is transmitted. Each data bit is transmitted twice, the two memory locations OC20 and OC22 are reset as the transmission occurs.

Only one DMA operation occurs on each event of the process phase of the interrupt program, since 16 data bits are transmitted twice, 32 interrupts occur after Q is set by the fire program before all data is transferred.

On entry to the DMA subroutine which occurs during each pass through the process phase, the status of the Q bit is first checked. DMA transfer will only occur if the Q bit is set, as dictated by the Fire program (section 3.5) if not set, control returns to the calling program.

Register R6, previously set at the last pass through the process phase to H'0110', is used to determine whether the data bit is being transmitted for the first or second time and to count the number of bits transmitted. Bit '0' of R6(1) is at '1' if the bit being transmitted is first pass and at '0' if second pass Bit 4 of R6(1) is used to indicate if both bytes have been transfered Because 16 transfers per data byte occurs, R6(0) is initially set at H '10' and is used to determine when all bits have been transfered twice.

When Q becomes set by the fire program, the DMA program which samples the Q line at each pass, through the process phase, proceeds to line 16. At this point R8 is set to be used as pointer to the output register and two locations from which data is to be output (OC23, OC22, and 0C20 respectively).

At first entry, R6(1) bit 0 is at '1' and program continues at line 20 where R6(1) bit 0 is reset. At line 22 and 23 bit 0, the data transfer port of the output register, is cleared to '0' and at lines 24 and 25 the low bit of location OC22 is copied to the output register.

Program steps 26 and 27 then output the data bit which is subsequently clocked into the second side by an output instruction to port 1. Decrementing R6(0) at line 28 indicates that one transfer of the current byte at OC22 has taken place. With R6(0) now at H 'OF' program jumps to the exit segment of the interrupt program.

On the next entry to the DMA program bit '0' of R6(1) is now zero and from line 19 program jumps to line 42. At this point R6(1) bit '0' is reset to '1' and the data at OC22 is shifted such that the next bit for transfer is now resident at bit '0' position.

The branch from line 46 to 26 now initiates the second transfer of the first bit which is still stored at bit 0 of the output port. Register R6 is decremented before exit from the interrupt program occurs.

At the third and fourth entry to the DMA program the second bit of location OC22 is output. This is repeated until all bits of OC22 have been transferred, at this time when the test at line 30 occurs R6 (0) is zero. A check at line 31 determines if both bytes have been transferred. If bit 4 of R6(1) is low as at this time it is set to a '1' along with bit '0' of R6 (1), R6(0) is re-initialized to enable the next 16 data transfers to be counted (lines 33 to 35).

The memory location now to be transferred serially out is OC20, this is first moved to OC22 from which the transfer will occur. (lines 36 and 37).

Subsequent entries to the DMA program cause the second data byte to be output in similar manner as the first until at line 30 the test again shows that R6(0) is zero. As this pass the test at line 32 shows that both data bytes have been output and program jumps to line 39, at which R6 is re-initialized and the Q output reset such that no further DMA activity can occur. The DMA program exit then occurs, and all subsequent entries cause no data transfer until the next fire program issues Q = 1.

3.5. Fire Program

The main function of the fire program is to process head data obtained from the last gather phase of the interrupt program resulting in the indication of fire or fault conditions.

Data may be fire data or data indicating the status of heads if the last gather phase was coincident with a head test.

The supplied data is processed as per the requirements of Volume I, Section 4.

The general method by which this data is processed is outlined in Appendix A-1.

Subordinate functions carried out by the fire program are:

a) Recording the time at which a fire event occurred.
b) Recording the adjacency area in which the fire condition occurred.
c) Recording the time at which the fire reset occurred.

d) Recording the time at which heads fail to respond to head tests.
e) Recording how close the system comes to indicating a fire condition in terms of the number of successive gates filled by 4 or more pulses.
f) Recording the number of fire events.

Program listing for fire program is carried out in level 2 assembler a language peculiar to RCA. A summary of commands are contained in Appendix A-4.

Fire program listing is split into three segments named UNPACK, RENEW and FSET. These three programs call up three subroutines, ADJPR, ADJSET and HEADS.

3.5.1. Program Segment UNPACK

The program execution is dependant on whether the system is running as a System A or System B. (Note System A operation with a failed side is effectivley a System B)

Upon entry to the program access to the internal flags register at OC25 and detemines whether the second side is functional.

3.5.1.1. UNPACK With Both Sides Functional

If both sides are functioning correctly.

If data has been passed from the second side during the last gather phase then the register R0, used as the pointer for DMA data should be set to OCFF, this is checked by the program. If incorrect data has not been correctly received and a fault identity is loaded. Two reasons for this exist:

Firstly, due to some failure of the receiving processor, the second may have initiated an inhibit. Program looks at the status of its EF1 (NOT) flag, if set (='1') then the second processor has initiated a side shut down. As a result a branch to the fault latch routine (LACHFL) occurs.

If EF1(NOT) = 0 no inhibit has occurred and due to failure to send data the second side is inhibited by jumping to program at NYOFF1. Program route in UNPACK is followed for a failed side and is discussed in Section 3.5.1.2.

At line 90, the data pointer (R0) is reset to OCDF ready to receive data at the next gather phase via DMA activity.

Program operation then checks that received data is via the two separate input channels of the logic card DMA circuitry. This it does by checking the port identity bit of the received data (referred to as X bit on flow diagram).

The check is carried out on memory locations OCDF and OCEO. Data at location OCDF should be as a result of one DMA port, data at OCEO should be as a result of the second DMA port. The hardware is wired such that the port identity bit is '0' at one input port and at '1' on the second. The logic check at line 95 compares the two bits. If different, operation continues at label PS2. If incorrect a fault label is loaded and program executes a self shut down by LACHFL routine.

Further checks on received DMA data are carried out on the parity bits which are transmitted prior to any good data. Low bits of OCDF, OCEO, OCE1 and OCE2 should be 0,0,1,1 respectively. Lines 101 and 102 check for this compliance, failure causes program to pass to NYOFF1.

It is also essential to prove the hardwire linking configuration of the DMA ports which identify the adjacency set information to the program. It was essential to use two ports in the design such that verification could be achieved. This check is carried out at lines 105 to 111 by comparing memory locations OCDF and OCEO after inputed data and port identity has been masked off. The master/slave bit setting is also included in the check. Incorrect configuration results in a fault identity loading and jump to LACHFL routine.

Because of the need to include at the DMA ports a port identity bit it became necessary to eliminate one of the adjacency bits. Referring to the adjacency table of Section 9 of the report in Appendix A-1, it can be seen that by utilizing the 4th order bit only two adjacency set configurations are lost. However, it was evident that the set identified by 111111XX is desirable as this is the only case when a single headed system can be implemented. The second lost configuration identified by 011111XX is effectivley duplicated by the configurtion 110100XX.

Since without the fourth identity bit it is possible to identify the case 11111 as being unique, the program checks for this condition. To preserve the adjacency program written for 6 bits the 5 bit data is converted to 6 bits before being stored to memory location OCD7. Lines 113 to 120 check for the fourth order case and store the configuration data to the appropriate location.

The DMA received data from side 2, at locations OCF0 to OCFE is only contained in the lowest order bit of ech byte. It is then necessary to unpack the status byte and the byte (H') containing either head data or the byte (W') containing the head test data. Note that the dash notation refers to the data received from the second microprocessor to distinguish it from that of the prime.

Lines 122 to 142 unpacks this data and reconfigures it to two single bytes. Unpacked data is stored at scratch pad locations OCB8 and OCB9.

3.5.1.2. UNPACK With One Side Faulty (Or System B operation)

The jump to program label NYOFF1 occurs due to a detected failure. Program at line 214 logs the status of the second processor at its internal flags register (bit 4 of OC25). Also true status and output status registers OC23 and OC24 are updated with inhibit flags set at bit 3 position.

Because program still requires the aircraft configuration data at the two DMA ports, it must "bootstrap" this information into memory. The hardware allows this to be effected by executing an OUT 2 instruction as described in Section 2.2.2.3.6. The configuration is inputed twice allowing delays such that data is transferred correctly (lines 221 to 224).

Program execution then checks for correct port identity, correct duplication of configuration bytes and checks for fourth order adjacency bit before storing the data, in similar manner to that of Section 3.3.1.1.

If correct data is not received from the second processor, the register containing W',X',Y', as described in Section 10 of Appendix A-1. must be set to zero to ensure correct operation of the fire program. The H' register must also be set to an all faulty status. This operation is effected between lines 250 and 254.

Subroutine HEADS is then called. This processes received head condition data.

3.5.2. Program Segment RENEW

The main function of this program segment is to update all registers associated with computation of fire conditions or all registers associated with head status dependant on whether the last gather phase gathered fire data or was a head test.

Program operation commences with a check on whether the second processor is successfully carrying out its own check on ROM content. The result of a successful check by the second processor is to initialize a flag bit in its status register which is subsequently transferred across by DMA activity. Lines 156 to 165 determine whether the status bit has previously been set by the second processor. If yes, the countdown ROM timer is preset to its initial count down value.

Further operation is dependant on whether received DMA data was W' or H' type. This is checked at lines 166 to 169 by observing bit 3 of the received status byte which is '0' if W' and '1' if H' gather function.

3.5.2.1. RENEW if W' Type Data

If the received data (now unpacked and resident at scratch pad location OCB8) is fire data, the registers W',X' and Y' must be updated. This operation is carried out after the jump from line 169 to NYOFF4 at line 196.

W' X' and Y' information is contained at location OCCC, OCCD and OCCE respectively. This data has to be shifted such that the last gather phase W' moves to X' etc. i.e. W' ---> X', X' ---> Y' and Y' is lost. This function is performed by lines 196 to 202.

3.5.2.2. RENEW if H' Type

If the received data was H' type, program continues at line 173. Firstly, it acknowledges the receipt of H' data by presetting the counter at OC29 to its initial down count value (line 174 to 176).

The H' data is then processed by the ADJPR subroutine described in Section 3.5.3.6.3. and then by subroutine HEADS.

At this point whether the system is A or B type all H' and W' data has been correctly processed according to the requirements of Appendix A-1.

Program action now concentrates on processing data from the last gather phase of its own side i.e. on W and H type data. NYOFF5 at line 262 is the point from which this is carried out.

Again dependant on whether data is W or H type two different routes are taken. The sides own internal flags register is interrogated to determine this at lines 263 to 264. The data about to be processed is that contained at the FOURS register location (OC40).

3.5.2.3. RENEW if W Types

The fire register F at OCD4 determines whether a fire is to be set. If a fire condition is existing, the fire indication remaining on is dependant on whether the new data received is such that at least two pulses per gate are being received as per the requirement stated in Volume I. Therefore, a fire condition for a head remains if the logic condition F AND 2's or 4s is satisfied. This result is stored for DMA transfer to the second side at location OC20 (to be received by side 2 as W' information) and as W information.

Similarly, to W' data, W is processed by updating registers containing X,Y and Z data (as defined in Section 10 of Appendix A-1.)

Registers W, X,Y and Z are at locations OCCF, OCD1, OCD2 and OCD3 respectively.

Data W moves to X etc., i.e. W-->X, X-->Y, Y-->Z and Z is lost.

The above processing is carried out at lines 327 to 340.

3.5.2.4. RENEW if H Type

If the last gather phase for its own side was a head test, H is processed according to program starting at line 277. Initially, a check is carried out to determine whether the new head status data H has differed from the previous H data (obtained 15 seconds previously).

The previous head status data is stored at location OCC7 and is termed H0. It determines whether a change of status has occurred when logic operation of lines 279 to 283 are performed. If the status has changed the new status is loaded to location OCC7 and the time of this change is logged at OCC5 and OCC6 by copying the main timer value to these registers. In this way the time of the last head failure can be identified.

The H data is also stored at OC20 for subsequent DMA transfer (see lines 290 and 291).

H data is subsequently processed by subroutines ADJPR and HEADS and ADJSET described in Sections 3.5.3.7.3., 3.5.3.7.2., and 3.5.3.7.1. according to lines 292 to 315.

The check sum figure generated through the ADJSET subroutine is then checked against the previously stored checksum at OCD2. If the new check sum differs according to lines 317 to 322 a fault code is generated and program jumps to LACHFL.

At the completion of the caps segment of the program a flag is set to allow the process phase of the interrrupt program to transfer data by DMA activity. The flag set is by raising the Q line output high and is performed at such a time that all data to be transferred has been loaded to locations OC20 and OC22.

3.5.3. Program Segment FSET

The main function of this section of the fire program is to calculate whether a fire condition should be set or reset according to all the data available.

Data logging functions are also performed.

Program FSET commences at line 356.

3.5.3.1. W COUNT Register

The initial operation performed by FSET is to update the memory location OCC3 and OCC4, termed the W count register. This register acts as a counter to store all occasions when a head has registered four or more head strikes in one time share period.

Each bit of the W register indicates if a particular head has received 4 or more strikes in the last gather phase. For each '1' level in the W register the W COUNT register is incremented unless that is it is already full, (corresponding to approximately 65000 gates). This incrementing is only performed if the received data is not as a result of a head test.

Program implementation of the above is shown between lines 359 and 384.

3.5.3.2. Fire Level Logging

For a System A a fire condition is achieved when 6 consecutive gates (3 on each side of the system) are filled. A record is made of how near to this fire condition the system gets. For example, 5 consecutive gates may fulfil the fire condition but the 6th be clear. This is termed 5th fire level. The program treats the 6 gates W or Z,X,Y, and W',X' and Y' as a window, thus if say W,Y and X' were indicating filled gates (with 4 pulses) a 3rd level fire condition is registered.

When a fire level is detected the time that the event took place along with the head indicating the fire level is recorded.

This program is skipped if the current data being processed is as a result of a head test.

Memory locations OC51 to OC55 and OC66 are used as scratch registers for this program while locations OC56 to OC65 contain the stored data, according to the RAM memory chart, Figure 3-1.

This operation is fulfilled by program lines 386 to 444.

3.5.3.3. Calculations of Fire Conditions

Fire set and reset conditions are calculated from line 450 onwards. With reference to Section 10 of Appendix A-1., initially FL (termed in the software listing as the reset condition byte) is generated. Program lines 450 to 458 are responsible for this function.

Fire generation conditions according to the logic of Section 10 of Appendix A-1. are calculated between lines 462 and 502. This results in scratch pad register OCB8 containing all zeros if the fire is to be reset otherwise a fire condition is to be set or sustained.

3.5.3.4. Fire Condition Logging and Outputting to Hardware

If no fire condition is indicated the outputting program is skipped, When a fire condition is indicated by software the time and the adjacency set which caused the fire condition are logged. The program is arranged such that the occurence of the first fire and its start time is logged at locations OCC0, OCC1 and OCC3.

The end of the event is recorded at locations OCBD, OCBE and OCBF. This procedure enables the duration of the fire event to be determined. To identify whether multiple fire events have taken place the memory location OCBC is used to store the number of fire events that have occurred. These operations above are carried out between lines 511 and 528 of the program.

The completed fire, or no fire, condition is then output to port 4 at line 535.

The fire condition is also saved at output status and true status memory locations.

3.5.3.5. Reverse Adjacency Processing

To enable the head data to be utilized in determining the next F register, the head data which has been adjacency procesed has to be unprocessed. This is performed as described in Section 11 of Appendix A-1.

The reverse adjacency processing is carried out between lines 547 and 564.

3.5.3.6. Housekeeping and DMA RAM Checks

At the completion of the fire program various resetting and checking operations are carried out between lines 576 and 589.

The FOURS, TWOS and ONES registers (memory locations OC40, OC41 and OC42) are reset to zero at lines 567 and 568. This is to enable correct operation of the next gather phase.

The memory locations OCDF to OCFE which receive DMA data, are also exercised to prove their correct operation. This is carried out by loading a pattern of H'AA' into each location and then checking that this write condition was successful This is repeated with a pattern of H'55' to prove that each bit is capable of being set to '1' or '0'. Failure to respond correctly to the tests results in the loading of a fault identification and a branch to LACHFL routine.

The DMA memory locations are then reset to zero and the DMA pointer register R0 is set ready for the next DMA transfer.

Program operation then returns to the background program, pointed to by R3, at line 596.

3.5.3.7. Subroutines

3.5.3.7.1. ADJSET Subroutine

This subroutine is used to create the adjacency forms ADJ1, ADJ2, ADJ3 and ADJ4 as required by sections 5,6,7, and 8 of Appendix A-1. These forms are created from the configuration byte at locations OCD7 and stored at locations OCD8, OCD9, OCDA and OCDB.

A checksum generated through the program and is used to check that correct processing of the configuration data has been performed.

The ADJSET subroutine is shown between lines 602 and 668 of the fire program.

3.5.3.7.2. HEADS Subroutine

This subroutine is used to determine whether the number of heads in the system are sufficient to satisfy the adjacency set requirements. If a fire area has no ability to detect fire conditions the result of the computation (.NOT.H').AND.(.NOT.H) will be non zero. This non zero result is used to indicate a fault condition. This fault condition is copied to the true status register and output register. The fault is then copied to hardware by the next interrupt program. HEADS program is performed between lines 679 and 706.

3.5.3.7.3. Subroutine ADJPR

This subroutine is used to process the received head data W,W',H or H', condensing the individual head status into adjacency format. This is performed in accordance with Section 11 of Appendix A-1.

Program operation is performed between lines 714 and 735.

3.5.3.7.4. Subroutine LACHFL

This subroutine is called by the fire program and other programs of the system.

Its essential function is to shut down its own operation. Entry to the routine is performed with the accumulator containing the fault identity code of the function calling the LACHFL routine.

A list of codes generated before entry to the LACHFL routine are documented in Figure 3-3.

The routine saves this error code at location OCB5 along with the time (related to the main program timer) that the failure occurred at locations OCB3 and OCB4.

The interrupt routine is disabled on entry to the program.

Output code H'42' is passed to output port 4 before going into a loop, effectively stopping program operation. This output code raises the hardware GSE2 line high and issues a fault line high to the common logic circuit.

Program operation is performed between lines 747 and 768.

FAULT IDENTITIES

Self Shut Down Mode:

Identity	Description
01	No return path from o/p relay
02	Faulty common logic (alarm return permanently high)
03	No emitter operation (or return path)
04	Permanent emitter operation (or return path)
05	No emitter reset when reset by program
20	Error at RAM check
24	Bad DMA ROM check
25	Different Paths Check
28	No good paths
29	X bits of two DMA ports not different
30	Left configuration different from right configuration
A7	Being inhibited by opposite side
D1	Bad sum check byte
F9	X bits of two DMA ports not different
FF	Fault at ROM check.

Opposite side shut down mode:

Identity	Description
80	Opposide side time share did not set at initilization
81	Opposite side time share time out incorrect
82	Opposite side not confirmed ROM check complete
83	Opposite side not confirmed 15 second head test

FIGURE 3-3 FAULT IDENTITIES

3.6 GSE Interface Program

The GSE program acts interactively with external ground support equipment which is detailed in a separate report.

The GSE program is entered if at start up the GSE 4 input line on port 3 is found to be at '1' at line 18 of the initialization program. The three GSE inputs, 1, 2 and 3 then determine which program is to be run. With three inputs eight programs are available.

Programs written in the system software are headed:

1) Idle
2) Output Data
3) RAM Retention Part A
4) RAM Retention Part B
5) Common Logic Check
6) ROM Test
7) ROM Test and Reset
8) Board Test Routine

On entry to the GSE program the status of port 3 is input and all unwanted bits masked off such that only the three inputs, GSE 1, 2 and 3 are remaining (lines 15 to 17). A series of tests between lines 18 and 26 then determine which test is to be run according to the setting of GSE inputs 1, 2 and 3.

Completion of each test requested of the CCU results is confirmation by appropriately setting the GSE 1 and 2 output lines. This enables the connected ground support equipment to determine if the test has been passed or failed.

3.6.1 Idle Program

The idle routine has no specific function to perform, it is merely a convenient state to leave the system in when no function is being performed. Program operation starts at line 27. At line 28 the GSE 1 and 2 output lines are both set high by an output instruction. Program then runs into a loop at line 29.

3.6.2 Output Data Program

This program is responsible for transmitting out the contents of the RAM memory for analysis by the GSE. All memory locations are transmitted in ASCII format at a rate of 300 baud.

The program from line 61 uses two subroutines, a delay routine called DELAY and a routine called out which outputs ASCII characters via the Q line which acts as the serial output port.

Register 6 acts as a pointer to RAM memory from which data is to be output. This is initialized to OC00 at lines 61 to 65. Start addresses of the two subroutines are then loaded to registers 8 and 9 at lines 67 to 70.

The computer card in the ground support equipment expects to see a string of characters which define where the following data is to be loaded. The string !M4400 is a statement that the memory contents of the CCU are to be stored from a starting address of 4400.

Lines 71 to 79 load sequentially the above string in ASCII equivalent, by executing the OUT subroutine the character is transmitted on the Q line.
Lines 80 to 82 cause a space character to be transmitted 24 times, this causes the printer of the GSE to be set correctly to print the data as it is transmitted simultaneous with its storage to memory.

Program between lines 83 and 107 cause each CCU RAM memory byte, starting as address OC00, to be converted into ASCII format and transmitted.

A carriage return character is then transmitted, this is recognized by the GSE computer card as the conclusion of data transfer.

The GSE 1 line is raised to a '1' indicating that the program sequence has been completed (line 111) and a loop function is executed at line 112.

3.6.2.1 Subroutines of Data Program

The ASCII characters, output at 300 baud, consist of a high level start bit, 7 data bits, an even parity bit and two stop bits. This requires that each bit be held high or low on the Q line for 3ms. The delay subroutine at lines 144 to 148 executes a 3ms delay before returning to the calling program.

On entry to the OUT subroutine, at line 115, registers are initialized R3(0) acts as a bit counter. The Q line is set for 3ms, this is the start bit. At line 121 a check is carried out to determine if all data bits of the ASCII character have been transmitted. If not, the next bit is shifted into the carry register (lines 122 to 124) and dependant on the bit being '0' or '1' the Q output is reset or set and the 3ms delay activated. Note that at line 126, register 1 is incremented if the next data bit is a '1'. This register acts to accumulate of the number of '1's' transmitted.

When the test at line 121 determines that all bits have been transmitted program jumps to line 131, at which R1 is used to recall if an odd or even number of '1''s have been transmitted (lines 131 to 133).

If even the Q line is set, if odd, the Q line is reset and the 3ms delay is initiated, thus performing parity transmission.
Two stop bits (zero's) are then transmitted by resetting Q and executing two 3ms delays (lines 138 to 140).

Control then returns to the calling program.

3.6.3 RAM Retention Program (Part A)

This program is designed to run in conjunction with Part B (Section 3.6.4). Its function is to set up a data pattern in memory which is checked by Part B. The mode of use is to set the data pattern and subsequently switch system power off. On power up Part B then checks if the data pattern has correctly been saved by the battery back up and its associated control hardware.

Part A serves to set the data pattern H'00' at location OCOO H'01' at location OC01 etc. up to H'FF' at location OCFF.

Program execution starts at line 30 and is completed by setting GSE 1 output to a '1' level at line 35 before entering a loop at line 36.

3.6.4 RAM Retention Program (Part B)

This program serves to check the bit pattern set in memory by Part A (Section 3.6.3). It does so by adding all memory location contents together (disregarding overflow) the resultant figure is then checked against a checksum.
Program execution starts at line 37. Lines 40 to 42 get and add all memory data bytes together storing the accumulated figure at R6(0). When all bytes have been added, the result is compared with the checksum at line 44.

If the check is good (i.e. the memory pattern is the same as that set by the program of section 3.6.3) both GSE 1 and 2 output lines are set to '1' before a loop is executed at line 48.

If the check shows an error, only the GSE 1 output line is set to a '1' (line 49) before a loop is executed.

3.6.5 Common Logic Program

The common logic program acts in conjunction with the ground support equipment to test the logic block of the common logic card. The test is designed to flex the fire and inhibit lines

individually such that it can be proved that in normal operation a fire condition is only indicated when both sides set their respective outputs. The output conditions on GSE 1 and 2 lines enable GSE to determine what part of the common logic program is being executed.

At program entry, a bootstrap operation on the DMA port is carried out to access the master/slave bit. At line 10, if the side is slave, execution of a 2 second delay occurs at lines 21 and 22.
If the side is master, the following sequence of events takes place.

1) Issue a time share, fire and GSE 2 output to port 4 (line 11) and execute a delay for 400ms (lines 12 and 13).

2) Reset fire and GSE 2 outputs and set inhibit and GSE 1 outputs (line 14) and execute a 400 ms time dealy (lines 16 and 17).

3) Reset inhibit and time share lines, and set GSE 1 and 2 outputs (line 18) then execute a loop at line 19.

If the side was slave, after the completion of the two second time delay (line 23) the master sides time share t is repeatedly sampled until it is reset after execution of the above steps (lines 22 and 23). When this occurs the slave side also executes the sequence of steps 1, 2 and 3.

3.6.6 ROM Check Program

The ROM check program is that run in the backgound program, as described in section 3.3.

The ROM check set up program sets data correctly for entry into the background program. The time share bit of the output register must be set to a '1' (line 30 and 31) because the background program will only execute ROM check if the phase is gather. Furthermore it will only carry out ROM check if if the interrupt timer R5(0) has a count above H'CO', therefore line 32 stores H'FF' to R5(0). Entry to the background program occurs at line 35.

3.6.7 Board Test Program

The board test program listed from line 150 of the GSE program is used to fault find boards and does not interact with the ground support equipment or the normal operation of the CCU.

4.0 TESTING

4.1 Functional Tests

Functional testing of the component parts of the system was carried out in accordance with the following Graviner Quality Control Data Sheets, which form Appendix No. B-1 to this report.

Detector Unit Types 53522-011 and 53521-012

Q. Data Sheet No. Q.5304. Issue A

Paragraphs 5.2., 5.2.1., 5.3., 5.4.1., 5.4.2. and 5.5.

Applicable limits, Type 3 as paragraph 5.6. of Q.5304, appropriate at and between the declared extremes of operating temperatures.

Crew Warning Unit Type 53813-202

Q. Data Sheet No. Q.5308 Issue C

Paragraphs 4.3.2, 4.3.3, 4.3.4, 4.3.5, 4.3.6, 4.3.7, 4.3.8, 4.3.9 and 4.8.

Applicable limits, Type 3 as paragraph 8 of Q.5308, appropriate at and between the delcared extremes of operating temperature.

System A. Control Unit Type 53813-203

Q. Data Sheet No. Q.5309 Issue A

Paragraphs 4.1, 4.2.1, 4.2.2, 4.4, 4.5, 4.7.3, 4.7.4, 4.7.5, 4.7.6, 4.8.3.1, 4.8.3.2, 4.8.6.2, 4.8.6.3, 4.8.9, 4.8.10, 4.9.2, 4.9.3, 4.9.4, 4.9.5, 4.10.2, 4.10.3, 4.10.4, 4.10.5, 4.11.3.2, 4.11.3.3, 4.11.3.5, 4.11.6, 4.11.7.1, 4.12.10.2 and 4.12.10.3.

Applicable limits, Type 3 as Appendix 1 of Q.5309, appropriate at and between the declared extremes of operating temperature.

System B. Control Unit Type 53813-204

Q. Data Sheet No. Q.5310 Issue A

Paragraphs 4.1, 4.2.1, 4.2.2, 4.4, 4.5, 4.7.3, 4.7.4, 4.8.3.1, 4.8.6.2, 4.8.6.3, 4.8.8, 4.8.9, 4.9.2, 4.9.3, 4.10.2, 4.10.3, 4.10.4, 4.10.5, 4.11.3.2, 4.11.6, 4.11.7.1, 4.12.6.2 and 4.12.6.3.

Applicable limits, Type 3 as Appendix 1 of Q.5310, appropriate at and between the declared extremes of operating temperature.

4.2 Qualification Test Plan

The Qualification Test Plan is incorporated as ATS No. 52, Issue 5 which forms Appendix B-2 to this report.

A separate test plan has been formulated for Electromagnetic Interference with is incorporated as Appendix B-3 to this report.

4.3 Qualification Tests

4.3.1 Samples for Test

The following samples were supplied for testing:

Crew Warning Unit Type 53813-202
Serial Nos. 100 and 101

Computer Control Unit Type 53813-203
Serial Nos. 100 and 101

Computer Control Unit Type 53813-204
Serial Nos. 100 and 101

Dual U.V. Detectors Type 53522-011
Serial Nos XP1, XP2, XP6 and XP7

Single U.V. Detector Type 53521-012
Serial Nos. ENV, XP1, XP2 and XP5.

4.3.2 Approval Tests

The following tests only, of ATS No. 52 were carried out:

4.3.2.1 Weight (ATS 52 Para. 4.1.1)

The weights of a representative sample of components submitted for approval testing were checked and recorded as follows:

C.W.U. Type 53813-202	S/No. 100	0.581 Kg.
C.C.U. Type 53813-203	S/No. 101	3.699 Kg.
Detector Type 53522-011	S/No. XP2	0.142 Kg.
	S/No. ZP7	0.156 Kg.
Detector Type 53521-012	S/No. XP2	0.099 Kg.

4.3.2.2 Size (ATS 52 Para. 4.1.2)

The dimensions of all samples submitted for approval testing was checked against the relevant drawings and were found to be satisfactory.

4.3.2.3 Visual Examination (ATS 52 Para. 4.1.3)

All samples submitted for approval testing were examined for correctness of marking, workmanship, visible defects, and were found to be satisfactory.

4.3.2.4 Center of Gravity (ATS 52 Para. 4.1.4)

The center of Gravity of the following items of equipment was established using the knife edge method and is shown in Figure Nos. 4-1, 4-2, 4-3, 4-4, and 4-5.

C.W.U. Type 53813-202	S/No. 101
C.C.U. Type 53813-203	S/No. 100
C.C.U. Type 53813-204	S/No. 100
Detector Type 53522-011	S/No. XP6
Detector Type 53521-012	S/No. XP1

4.3.2.5 Voltage Supplies (ATS 52 Para. 4.2.1)

The component parts of the system were operated from power supplies in accordance with MIL-STD 704A, Equipment Category B, Emergency supply condition.

A.C. Voltage Limits	102 volts 380 Hz to 124 volts 420 Hz
D.C. Voltage Limits	16 to 29 volts

4.3.2.6 Voltage Transients (ATS 52 Para. 4.2.1)

The effect of the following voltage transients on the system has been established.

Voltage	Duration
190	0.10 second
174	0.40 second
139	4.00 seconds
137	5.00 seconds

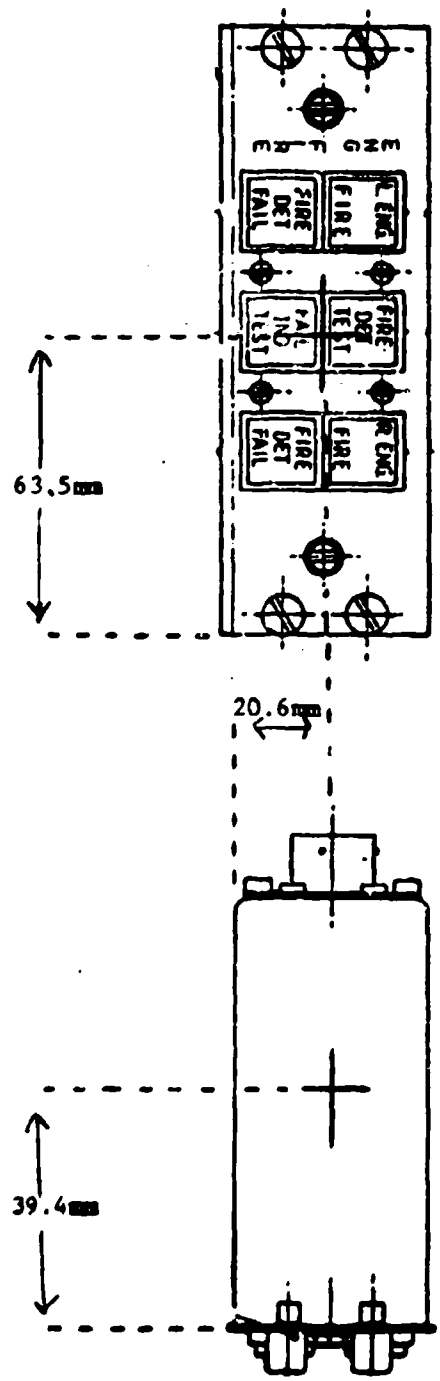


FIGURE 4-1 CREW WARNING UNIT TYPE 53813-202 CENTER OF GRAVITY

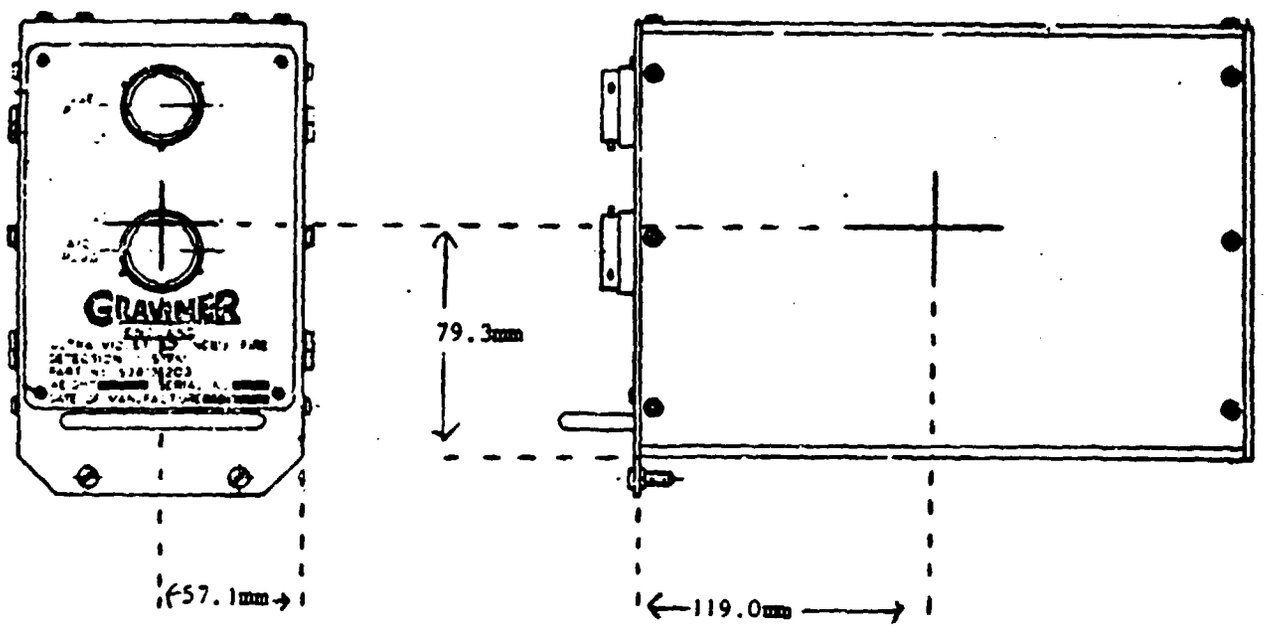


FIGURE 4-2 SYSTEM A CONTROL UNIT TYPE 53813-203 CENTER OF GRAVITY

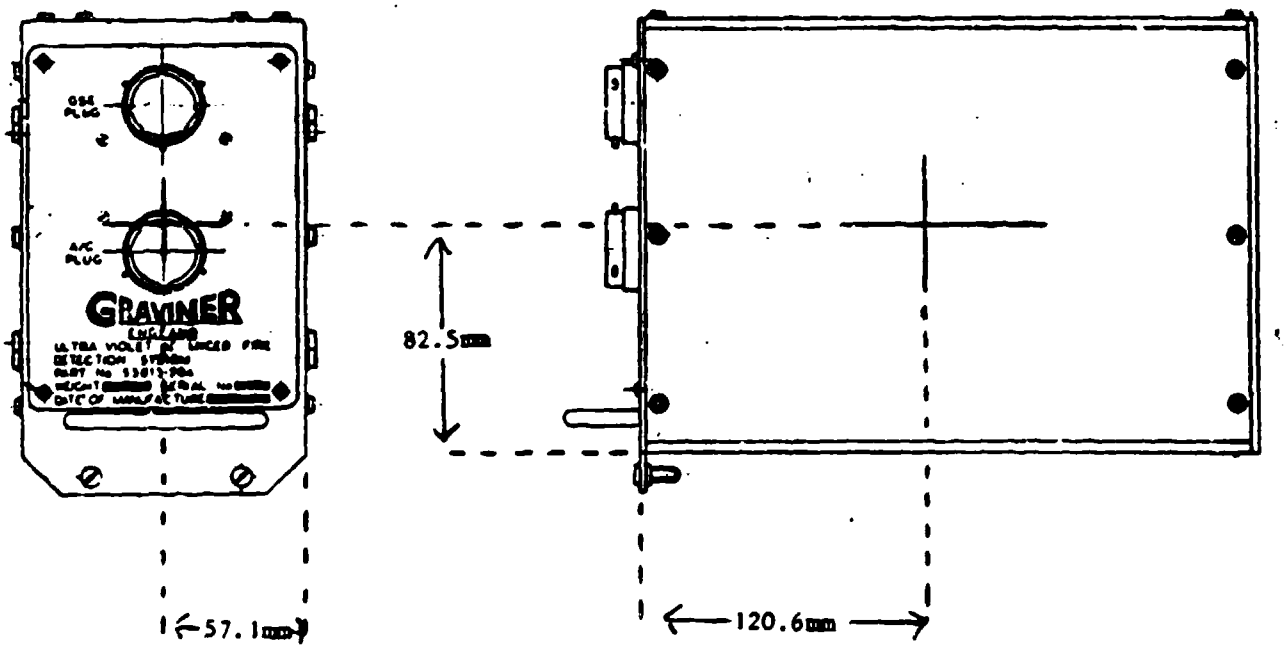


FIGURE 4-3 SYSTEM B CONTROL UNIT TYPE 53813-204 CENTER OF GRAVITY

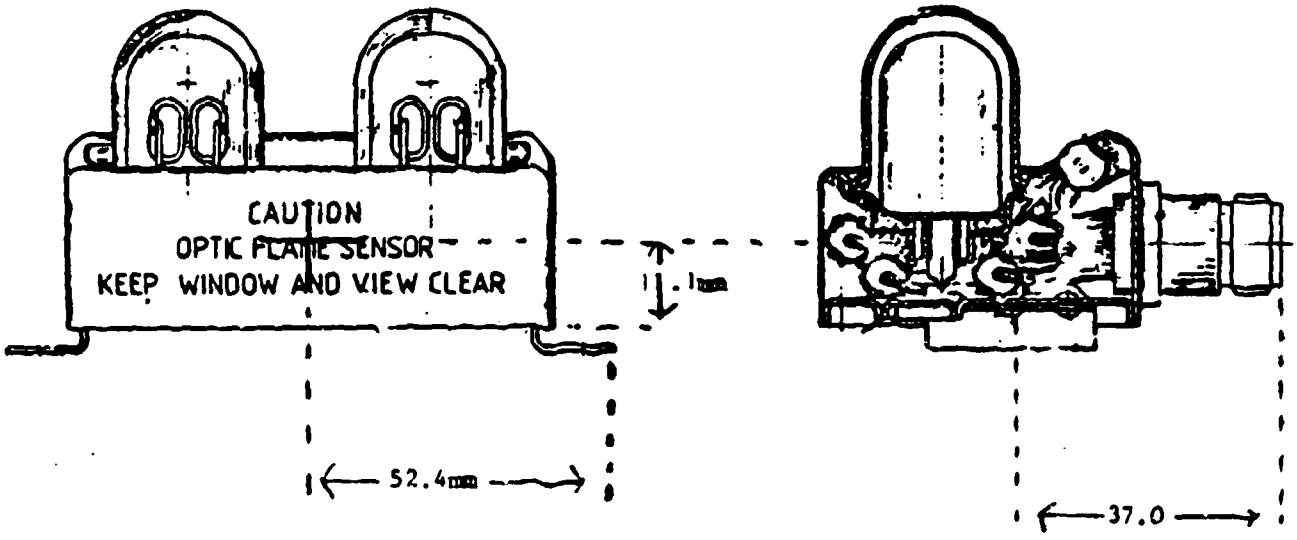


FIGURE 4-4 DETECTOR UNIT TYPE 53522-011 CENTER OF GRAVITY

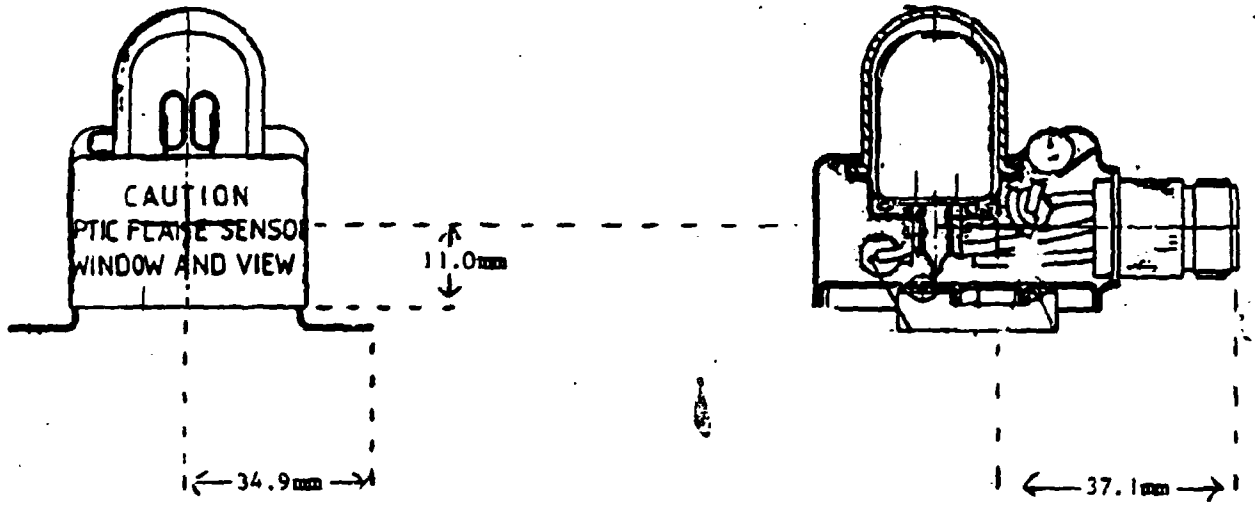


FIGURE 4-5 DETECTOR TYPE 53522-012 CENTER OF GRAVITY

Testing was carried out in accordance with MIL-STD-704A and the results of the tests are recorded in Lucas Aerospace Report No. LM80876. Appendix 5 (AED.ENV.480550) which forms Appendix B-3 to this report.

4.3.2.7 Supply Interruption (ATS 52 Para. 4.2.1)

The effect of Supply Interruption to the system has been established. Testing was carried out in accordance with MIL-STD-704A and the results of the tests are recorded in Lucas Aerospace Report LM 80876 Appendix B-3 (AED.ENV 480550).

4.3.2.8 Insulation Resistance (ATS 52 Para. 4.2.2)

Insulation Resistance Tests were carried out where necessary during approval testing as follows:

C.C.U. 30 volts d.c. between all unearthed terminal pin and case. (Leakage current not to exceed 1.5 uA)

The insulation resistance measured at all times exceeded 20 Megohms.

C.W.U. 500 volts d.c. between all unearthed terminal pins and case.

The insulation resistance measured at all times exceeded 20 Megohms.

Detector Unit. 500 volts d.c. between all unearthed terminal pins and case.

The insulation resistance measured at all times exceeded 20 Megohms.

4.3.2.9 Electromagnetic Interference (ATS 52 Para. 4.2.3)

The system has been tested to comply with the Electromagnetic Interference requirements of MIL-STD-461.

This work was carried out by Lucas Aerospace and the results of the tests are recorded in Lucas Aerospace Report No. LM 80876 which forms Appendix B-3 to this report.

4.3.2.10 Chattering Relay Test

The following test was carried out as a requirement of General Dynamics, using the following equipment:

System 'A' C.C.U. Type 53813-203 Serial No. 100
System 'B' C.C.U. Type 53813-204 Serial No. 100
C.W.U. Type 53813-207 Serial No. 100

and using the test configuration as shown on Figure 4-6.

Transient Impulse Susceptibility

No change in indications, malfunctions or degradation of performance shall be indicated in any equipment and/or its load when exposed to an impulse type electromagnetic field generated by a type MS25271 (or an acceptable equivalent) when wired for continuous operation with a switch in series with the positive side of the line from a 28V D.C. power source. No. suppression components (shielding, diodes etc.) shall be attached to the relay or its wiring. The unshielded positive lead leaving the switch shall be laid over three side of the test sample and then connected to the relay. The unshielded return lead from the relay shall be taped to, and in parallel with, input power leads, signal leads and interconnecting leads. The total length of each external wiring harness paralleled with the relay circuit shall not be less than 60 inches. The 28V input shall be reversed and the test repeated.

Equipment Used

System cableform as used for EMC testing refer to EMC report for details. Cableform wiring as per drawing Z22004.

Relay Type (NATO Stock No. 5945 92 192)
Elliot HF 1201 C00

Control Unit System A (53813-203) Serial No. 100
Control Unit System B (53813-204) Serial No. 100
Crew Warning Unit (53813-202) Serial No. 100

Test Performed

The equipment was arranged as per Test set up and relay wiring diagrams.

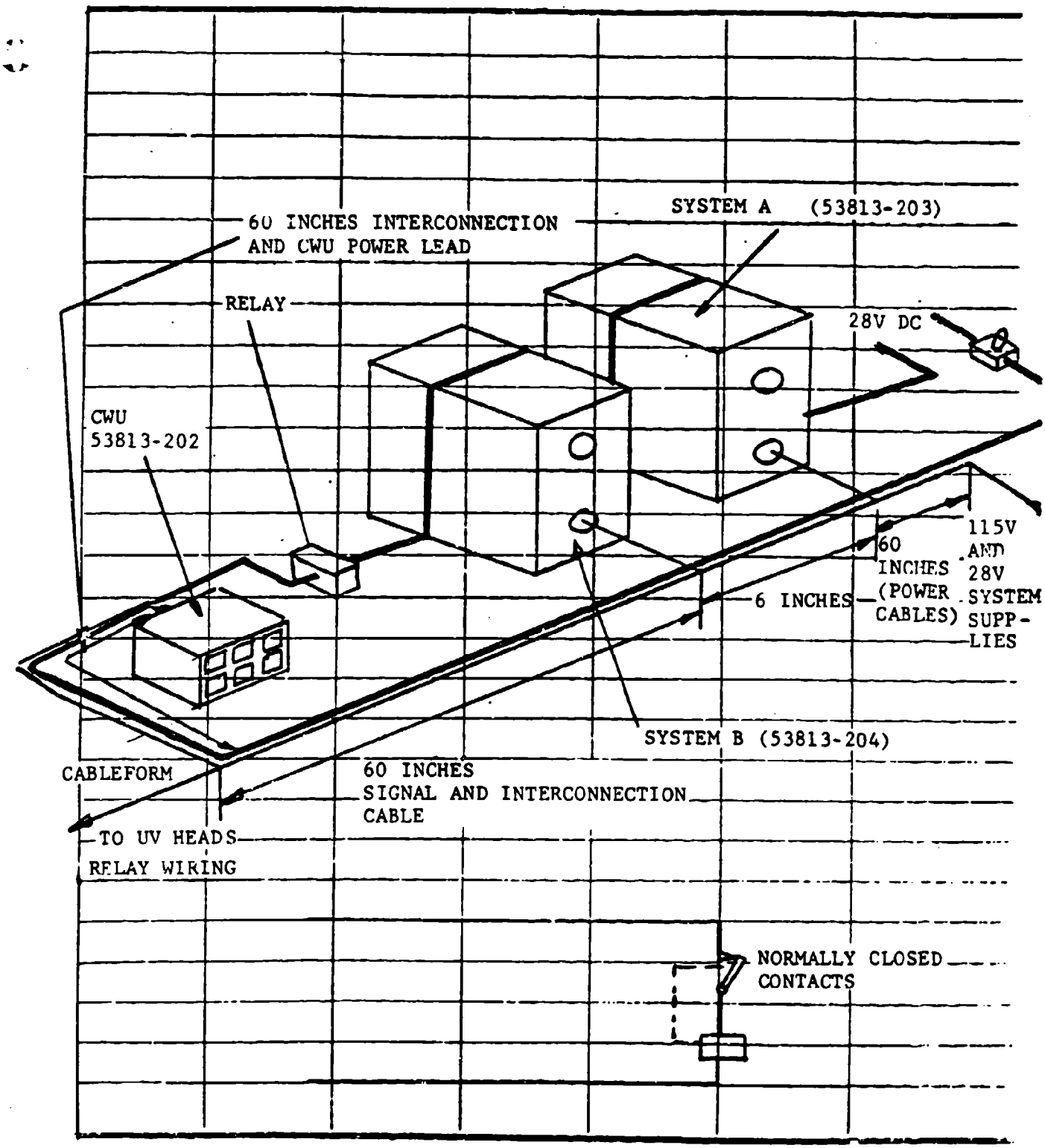


FIGURE 4-6 CHATTERING RELAY TEST SET-UP

With the system power switched on the control units were observed to function as per respective Q data sheets paragraphs 4.3.1 and 4.3.2.

The chattering relay supply was switched on and again paragraphs 4.3.1 and 4.3.2 of Q data sheet were carried out, namely

(1) Depression of fire push button and observing that both L.ENG and R.ENG fire lamps operated correctly.

(2) Depression of FAIL IND Test button on C.W.U. and observing that FIRE DETECT FAIL lamps functioned correctly. Correct operation of GSE1 and GSE2 lids on GSE control unit was also observed.

At no time during the test did the system show false indications, malfunction or become degraded.

The chattering relay supply was then switched off, the 28V supply reversed and the test repeated. Again no false indication, malfunction or degradation of the system was observed.

Conclusion

The system passed the chattering relay test.

4.3.2.11 Response and Reset Time (ATS 52 Paras. 4.3.2 and 4.3.3)

System 'A' comprising, C.C.U. Type 53813-203, S/No. 100, C.W.U. Type 53813-202, S/No. 101 and Dual Detector Type 53522-011, S/No. XP6 was subjected to Response and Reset Time test as follows:

The response time of the system was measured when the detector was exposed to a U.V. source at a distance of four feet.

The reset time of the system was measured when the U.V. source was removed from the view of the detector.

Exposure	Response Time	Reset Time
1	1.23 seconds	0.84 second
2	1.25 seconds	0.85 second
3	1.28 seconds	0.95 second

System 'B' comprising C.C.U. Type 53813-204, S/No. 100, C.W.U. Type 53813-202, S/No. 101 and Single Detector Type 53521-012, S/No. ENV was subjected to the response and reset time tests as previously described with the following results:

Exposure	Response Time	Reset Time
1	1.12 seconds	0.79 second
2	1.01 seconds	0.86 second
3	1.14 seconds	0.87 second

4.3.2.12 High Temperature (ATS 52 Para. 4.4.1)

System 'A' comprising C.C.U. Type 53813-203, S/No. 101, C.W.U. Type 53813-202, S/No. 100 and Fuel Detector Type 53522-011 fitted with fly leads (No Serial Number) was subjected to the high temperature requirements of MIL-STD-810C, Method 501.1, Procedure 1 modified as follows:

Detector - 24 hours exposure to 260°C
C.W.U. - 48 hours exposure to 71°C
C.C.U. - Not tested.

System response and reset with the detector at 260°C was as follows:

Exposure	Response Time	Reset Time
1	1.35 seconds	0.952 second
2	1.15 seconds	0.832 second
3	1.26 seconds	0.911 second

The results of functional tests conducted on the C.W.U. at 71°C are recorded in Table No. 1.

System 'B' comprising C.C.U. Type 53813-204, S/No. 101, C.W.U. Type 53813-202, S/No. 100 and Single Detector Type 53521-012 fitted with fly leads (No Serial Number) was subjected to the high temperature requirements of MIL-STD-810C, Method 501.1, Procedure 1 modified as follows:

Detector - 24 hours exposure to 260°C
C.W.U. - As previously tested
C.C.U. - Not tested.

System response and reset with the detector at 260°C was as follows:

Exposure	Response Time	Reset Time
1	1.24 seconds	0.928 second
2	1.06 seconds	0.878 second
3	1.08 seconds	0.870 second

4.3.2.13 Low Temperature (ATS 52 Para. 4.4.2)

System 'A' comprising C.C.U. Type 53813-203, S/No.101, C.W.U. Type 53813-202, S/No. 101 and Dual Detector Type 53522-011, S/No. XP6 was subjected to the low temperature requirements of MIL-STD-810C, Method 502.1, Procedure 1 and was exposed to a temperature of -54°C for a period of 24 hours.

System response and reset at -54°C was as follows:

Exposure	Response Time	Reset Time
1	1.804 seconds	0.907 second
2	1.253 seconds	0.908 second
3	1.183 seconds	0.939 second

The results of functional tests carried out on the C.W.U. and the C.C.U. at -54°C are recorded in Table Nos. 2 and 3 respectively.

System 'B' comprising C.C.U. Type 53813-204, S/No. 101, C.W.U. Type 53813-202, S/No. 101 and Single Detector Type 53521-012, S/No. ENV was subjected to the low temperature requirements of MIL-STD-810C, Method 502.1, Procedure 1 and was exposed to a temperature of -54°C for a period of 24 hours.

System response and reset at -54°C was as follows:

Exposure	Response Time	Reset Time
1	0.842 second	0.774 second
2	0.861 second	0.752 second
3	0.494 second	0.879 second

The results of functional tests carried out on the C.C.U. at -54°C are recorded in Table No. 4.

4.3.2.14 Altitude (ATS 52 Para. 4.4.4)

Dual Detector Type 53522-011, Serial No. XP6 and Single Detector Type 53521-012, Serial No. ENV were subjected to the altitude requirements of MIL-STD-810C, Method 500.1, Procedure 1 and was exposed tc altitude pressures equivalent to 70,000 feet (1.33 in Hg) and -1000 feet (30.12 in Hg) for periods of 1 hours each.

Throughout the test the detectors were connected to their respective C.C.U. and C.W.U.

System response and reset times after the altitude test were as follows:

Detector Type 53522-011, S/No. XP6

Exposure	Response Time	Reset Time
1	1.26 seconds	0.843 second
2	1.27 seconds	0.932 second
3	1.26 seconds	0.791 second

Detector Type 53521-012, S/No. ENV

Exposure	Response Time	Reset Time
1	0.95 second	0.826 second
2	0.89 second	0.724 second
3	0 93 second	0.664 second

4.3.2.15 Acceleration (ATS 52 Para. 4.4.10)

System A, C.C.U. Type 53813-203, Serial No. 100 and System B, C.C.U. Type 53813-204 (with battery card), S/No. 100. C.W.U. Type 53813-202, S/No. 101, Detector Type 53522-011, S/No. XP6 and Detector Type 53521-012,S/No. ENV were subjected to the acceleration requirements of MIL-STD-810C, Method 513.2, Procedure 1.

Acceleration levels of 25.5g were applied in each of three mutually perpendicular planes, in both forward and reverse directions and were held for a period of 60 seconds in each direction.

On completion of acceleration testing functional tests were conducted in accordance with the relevant Q.data sheet, the results of which are recorded in Tables No.s 5, 6, 7 and 8 (Appendix B-6).

4.3.2.16 Vibration (ATS 52 Para. 4.4.13)

The following items of equipment were subejcted to the following vibration tests:

Crew Warning Unit

Crew Warning Unit Type 53813-202, Serial No. 101 was subejcted to a resonance search in accordance with Specification MIL-STD-810C; Method 514.2-2, Procedure 1; Curve J of Figure 514.2-2 and to random vibration in accordance with Specification MIL-STD-810C; Method 514.2, Procedure 1A; Figures 514-2-11A and 514-2-2A.

Computer Control Unit

The units, Computer Comtrol Unit Type 53813-203, Serial No. 100 (System A); Type 53813-204; Serial No. 100 (System B with Battery Card), were subjected to a resonance search in accordance with Specification MIL-STD-810C, Method 514.2.2, Procedure 1, Curve J of Figure 514.2.2; to random vibration in accordance with Specification MIL-STD-810C, Method 515.2, Procedure 1A, Figures 515-2-11A and 514-2-2A.

Detector Units

Detector Unit Type 53522-011, Serial No. XP6 and Detector Unit Type 53521-012, Serial No. ENV were subjected to a resonance search in accordance with MIL-STD-810C, Method 514.2, Procedure 1, Curve G of Figure 514.2-2 and to random vibration in accordance with MIL-STD-810C, Method 514.2, Procedure 1A, Figures 514.2-11A and 514.2-2A.

All items of equipment functioned satisfactorily during and after vibration testing and the results of functional tests are recorded in Table Nos. 9-20 inclusive (Appendix B-6).

This test work was carried out by E.M.I. Electronics Limited, Feltham, Middlesex, and the details of the vibration tests, including equipment axes, frequency ranges, vibration levels, resonance search results, are fully reported in E.M.I. report No. ENV 2739 which forms Appendix B-4 to this report.

4.3.2.17 Acoustic Vibration (ATS 52 Para. 4.4.14)

Dual Detectors Type 53522-011, S/Nos. XP1 and XP7, Single Detector Type 53521-012, S/Nos. XP1 and XP5 were subjected to the acoustic vibration requirements of MIL-STD-810C, Method 515.2, Procedure 1.

The units were exposed to an overall sound pressure level of 154 dB measured using three Bruel and Kjaer Type 4135 microphones for a period of 30 minutes.

Functional tests were carried out before and after testing and the results are recorded in Table No. 21 (Appendix B-6).

This test work was carried out by British Aerospace, Dynamics Group, Hatfield, Hertfordshire.

Report No. ETR 2297, Test House Certificate A.W. 117 which forms Appendix B-5 to this report.

4.3.2.18 Mechanical Shock (ATS 52 Para. 4.4.12)

C.W.U. Type 53813-202, S/No. 101; System A. C.C.U. Type 53813-203, S/No. 100; System B C.C.U. Type 53813-204, S/No. 100· Detector Unit Type 53522-011, S/No. XP6 and Detector Unit Type 53521-012, S/No. ENV; were subjected to the mechanical shock requirements of MIL-STD-810C, Method 516.2, Procedure 1.

Each item of equipment was subjected to a total of 18 shock pulses of 20.0g for a duration of 11.0 milliseconds. Three (3) shocks in each of 3 mutually perpendicular planes in both forward and reverse directions.

Functional tests were carried out after shock testing and the results are recorded in Table Nos. 22, 23, 24 and 25 (Appendix B-6).

4.3.2.19 Flame Sensitivity (ATS 52 Paras. 4.3.2 and 4.3.3)

System A, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-203, Serial No. 100 and Dual Detector Type 53522-011 without Serial number fitted with fly leads was subjected to the flame sensitivity test as follows:

The detector unit was exposed to the radiation from a 5" diameter pan fire containing JP-4 aviation fuel at a distance of 4 feet.

The system indicated "Fire" after exposure to the flame. The "Fire" indication continued when half of the flame radiation was blocked from view of the detector and the system indicated "Fire Out" upon removal of the fire radiation source.

System response and reset times were measured at the system supply voltage extremes with the following results.

System A

System Supply Voltages	16.0v D.C. 102v. 380Hz		29.0v D.C. 124v 420 Hz	
	Response Time	Reset Time	Response Time	Reset Time
	1.31 seconds	0.80 second	1.256 seconds	1.41 seconds
	1.50 seconds	1.04 seconds	1.117 seconds	0.90 second
	1.23 seconds	1.57 seconds	1.111 seconds	1.0 second

System B, comprising C.W.U. Type 53813-202,Serial No. 100; C.C.U. Type 53813-204, Serial No. 100 and Detector Unit Type 53521-012 with Serial number fitted with fly leads, was subjected to the flame sensitivity test as previcusly described with the following results:

System B

System Supply Voltages	16.0v D.C. 102v 380 Hz		29.0v D.C. 124v 420 Hz	
	Response Time	Reset Time	Response Time	Reset Time
	0.764 second	0.579 second	0.986 second	0.715 second
	0.836 second	0.821 second	0.910 second	0.654 second
	0.856 second	0.776 second	0.876 second	0.751 second

4.3.2.20 Exposure to Flame (ATS 52 Para. 4.5.3)

System A, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. TYpe 53813-203, Serial No. 100; Detector Unit Type 53522-011, Serial No. XP7; Detector Unit Type 53522-011 without Serial number and filled with fly leads, was subjected to the "Exposure to Flame Test" as follows:

The detector without serial number and 6" of wiring was immersed in a 6" x 1100°C Flame.

Detector Serial No. XP7 was positioned so as to detect the flame but was not immersed in it.

The 6" x 1100°C Flame was supplied from a burner as detailed in Figure No. 2 of TSO-C79.

The detector was immersed in the flame for a period of 5 minutes.

The system indicated a "Fire" when exposed to the flame and continued to indicate for the entire 5 minutes exposure.

After the 5 minute exposure the flame was extinguished and the system indicated "Fire Out".

The nature of the test did not permit system response times to be recorded.

System B, comprising C.W.U. Type 53813-202, Serial No. 100; C.C.U. Type 53813-204, Serial No. 100; Detector Type 53521-012, Serial No. XP3; Detector Type 53521-012, without serial number and fitted with fly leads, was subjected to the "Exposure to Flame" test as previously described.

The system indicated a "Fire" when exposed to the flame and continued to indicate for the entire 5 minute exposure.

After the 5 minute exposure the flame was extinguished and the system indicated "Fire Out".

It should be noted that during these tests a 270 kilohm resistor was incorporated into the emitter lines of the detectors which were immersed in the flame.

REFERENCES

2-1 Graviner Ltd. Drawing; UV Detector Dual Head; No. 53522-011-I.D., Rev. H.

2-2 Graviner Ltd. Drawing; UV Detector I.D. (Single Head); No. 53521-012-ID, Rev. H.

2-3 Graviner Ltd. Drawing; Control Unit for Ultra-Violet Advanced Fire Detection System, System A; No. 53813-203GA, Rev. E.

2-4 Graviner Ltd. Drawing; Control Unit for Ultra Violet Advanced Fire Detection System, System B; No. 53813-204GA, Rev. E.

2-5 Graviner Ltd. Drawing; Circuit Diagram for Ultra Violet Advanced Fire Detection System A; No. 53813-203-CD, Rev. A.

2-6 Graviner Ltd. Drawing; Circuit Diagram for Ultra Violet Advanced Fire Detection System B; No. 53813-204-CD, Rev. A.

2-7 Graviner Ltd. Drawing; Drive/Supply Card; No. 43761-143-C.D., Rev. G.

2-8 Graviner Ltd. Drawing; Microprocessor Card; No. 43761-141-CD, Rev. B.

2-9 Graviner Ltd. Drawing; Logic Card - Master for F-111 Application Only; No. 43761-142-C.D., Rev. F.

2-10 Graviner Ltd. Drawing; Logic Card - Slave for F-111 Application Only; No. 43761-148-CD, Rev. D.

2-11 Graviner Ltd. Drawing; Common Output Logic Card; No. 43761-144-C.D., Rev. H.

2-12 Graviner Ltd. Drawing; Common Output Logic Card, System B; No. 43761-146-CD, Rev. F.

2-13 Graviner Ltd. Drawing; Battery Supply Card; No. 43761-140-C.D., Rev. B.

2-14 Graviner Ltd. Drawing; Filter Board System A; No. 43765-028-CD, Rev. C.

2-15 Graviner Ltd. Drawing; Filter Board System B; No. 43765-029-CD, Rev. C.

2-16 Graviner Ltd. Drawing; Circuit Diagram of Crew Warning Unit; No. 53813-202-CD, Rev. D.

2-17 Graviner Ltd. Drawing; Advanced Fire Detection System Wiring; No. Z22004, REv. D.

3-1 Graviner Ltd. Drawing; Flow Diagram for Ultra Violet Advanced Fire Detection System; No. 53813-203/204-F.D., Rev. B.

APPENDIX A-1

PROCESSING OF ADJACENCY AND ABSENT HEADS INFORMATION

GRAVINER REPORT

TITLE	PROCESSING OF ADJACENCY AND ABSENT HEADS INFORMATION FOR THE ADVANCED AIRCRAFT FIRE DETECTION SYSTEM
AUTHOR/S	N.J.B. Young
NUMBER & DATE	R.242. 29th. January 1979

Checked by N.J.B Young

Approved by

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3. L.Fernando
4. A.R.Brown
5. R.L.Farquhar.
6. N.J.B.Young

PROCESSING OF ADJACENCY AND ABSENT HEADS INFORMATION FOR THE ADVANCED AIRCRAFT FIRE DETECTION SYSTEM

SUMMARY

The microprocessor systems fire and fault routines must allow for adjacency and for the possibility of installations with less than 8 pairs of heads. Earlier proposals for the scope of the system were not regarded as satisfactory by General Dynamics.

This report investigates the adjacency concept and describes a particular package which allows for 4 levels of adjacency and for up to 7 heads being absent. The suggested package has been designed to meet the current and anticipated future requirements of General Dynamics and to supersede the proposals of the interim report (D.840, 26th June 1978).

GR

CONTENTS

1. ADJACENCY CONCEPT

The system contains two microprocessors, A and B, each associated with one side of each pair of (up to) 8 U.V. heads (numbered 1, 2, ...). If there is no adjacency, any head may "see" a fire (a definition of "see" in this sense will be given later) and a fire condition for pair 1 is:-

A1 sees a fire and B1 sees a fire

or, briefly, A1 and B1

This fire condition is reset when both A1 and B1 cease to declare a fire

These rules are modified by adjacency. Let us declare the pairs 1 and 2 to be adjacent. Then the fire condition for this adjacency set becomes:-

((A1,A2), taken together see a fire) and ((B1, B2), taken together see a fire).

and the reset condition is that all four heads cease to declare a fire.

Having given an explanation of adjacency we now state some axioms.

a) Adjacency is the same for the A and B sides of the system. If pairs 1, 2 and 6 (say) form an adjacency set we write (126)

b) Adjacency is commutative.

(1 2) ⇔ (2 1)

c) Adjacency of adjacency sets is equivalent to adjacency of their members.

(1 2) (3 4) ⇔ (1 2 3 4)

Thus adjacency is associative

(1) (23) ⇔ (1 2) (3) ⇔ (1 2 3)

We equate the adjacency set consisting of one head pair to that pair:

(1) = 1

d) Adjacency is not transitive, in the sense that

(1 2) and (2 3) $\not\Rightarrow$ (1 2 3)

We can therefore write the left hand side as (1 (2) 3), and

(1 (2) 3) $\not\Rightarrow$ (1 (2) 3) $\Leftrightarrow$ (1 2 3)

It is desirable not to have transitivity as this enables greater design flexibility.

N.B. (1 2 3) should be read as "1, 2 and 3 form an adjacency set", not "1, 2 and 3 are adjacent". Therefore

(1 2 3) $\not\Rightarrow$ (1 2)

as 1 and 2 do not form an adjacency set without 3, although 1 and 2 are adjacent. In this way we distinguish the descriptive property of "being adjacent" from the definitive logical property of forming an adjacency set.

2. DESIGN PHILOSOPHY

All the information determining the adjacencies and the number of heads for a particular aircraft system has to be hard-wired as 6 bits of a byte (whose other 3 bits are used for bit-serial data transfer and master/slave processor initialization). We then have a twin requirement that the method for encoding this information enables the widest possible range of configurations with the least amount of processing.

The design philosophy followed is to:-

a) Cope with absent heads by making them adjacent to existent heads in an aircraft configuration, and using all 6 bits to contain adjacency information.

b) Reconfigure these 6 bits into a small number of adjacency bytes which are combined with head information using logic and shift operations (avoiding branches and table look-up when possible) to give fire, reset and fault conditions.

c) Remember that when the system is used to protect a single area it is preferable on reliability grounds never to have an adjacency set consisting of a single head pair. We could then insist a priori that every adjacency set consists of at least 2 pairs, in fact

(1 5) (2 6) (3 7) (4 8)

(which will be termed "option PAIR") and that if one pair (say 4) is to be lone this can be achieved by omitting its adjacency partner (so 8 would not exist)

On the other hand we may require the system to protect two similar areas in which case we could insist that the adjacencies for 1, 2, 3 and 4 are repeated for 5, 6, 7 and 8, but that none of the first four is adjacent to any of the second four. (This will be termed "Option SPLIT")

Of course, although these options were originally designed for single area and two similar area systems respectively, they are of considerable use outside these applications. For the range of adjacencies possible see the sections below.

One of the 6 available bits will be used to choose between options PAIR and SPLIT.

2 (contd)

N.B. i) Of course, fully to use the flexibility and power of this adjacency philosophy it is necessary to adopt intelligent numbering methods. Thus

(1 8)

may not be possible, but re-numbering 8 as 5 we can achieve

(1 5)

ii) There is still the possibility of hard-wiring a single physical head pair into more than one location (to create a "ghost").
Thus:

(1 5 8)

can be achieved by wiring 5 into both 5 and 4, and using

(1 5) (4 ≡ 5 8)

Hardware requirements prevent a head being wired to more than two lines.

iii) As will be seen, the above philosophy enables relatively straightforward decoding/processing and considerable flexibility. We should note that the adjacency coding itself has a degree of redundancy (for example 4 independent pairs of head pairs may be configured as either of

Option PAIR = (15) (2 6) (3 7) (4 8)
Option SPLIT = (12) (34) (56) (78)),

that its versatility increases dramatically when one or more heads are absent (as the numbering of the missing heads provides extra degrees of freedom) and that the choice of an appropriate numbering and configuration for a particular aircraft is a skilled operation.

3. HEAD INFORMATION

(For easy reference this and later sections are summarised schematically at the end of this report).

Each U.V. tube is capable when energised of responding to incoming radiation by firing. A head firing causes the head to be de-energised for a (nominal) 2 ms recovery period and also makes available to the data bus a stretched pulse of (about) 1 ms. While in its gathering phase the microprocessor inspects the data bus 200 times at intervals of 832 μs. Each stretched pulse will therefore be seen either once or twice. A second inspection of the same pulse is ignored; three successive sightings (1's on the data bus) must correspond to two pulses.

Therefore the sequence:-

0, 1, 1, 0, 1, 1, 1, 0

is processed (by setting to 0 the second 1 of a sequential pair) to

0, 1, 0, 0, 1, 0, 1, 0

and so on.

The stretched pulses in one gathering phase may be counted. If a count of 4 or more pulses per gathering phase is achieved by any head in an adjacency set, and this requirement is satisfied for three successive gathering phases, this adjacency set is said to see a fire. (For a fire condition to be issued it is necessary that at least one adjacency set see a fire on each of the A and B sides according to all processors working). An alternative definition of "seeing a fire" is given in an appendix. If a count of less than 2 pulses in a single gathering phase is achieved a head is said to clear. (For a reset to be issued it is necessary that all heads on both of the A and B sides in all previously fire-condition adjacency sets clear).

We wish to process the information for the eight heads (1 to 8) in parallel, and associate these heads with the eight bits (7 to 0) of a byte, thus:-

3 (contd)

HEADS 1 2 3 4 5 6 7 8

BITS 7 ——— 0

The 832 μs inspection byte is processed as follows:-

Inspection and (not . last true inspection) → true inspection

(alternative equivalent Boolean expressions exist).

Pulse counting is conducted using "Ones", "Twos" and "Fours" registers, (which must of course be zefoed at the start of each processing phase) and performing arithmetic in parallel thus:-

True Inspection and Ones	→	Carry - twos
True Inspection Xor Ones	→	Ones
Carry-twos and Twos	→	Carry - fours
Carry-twos Xor Twos	→	Twos
Carry-fours or Fours	→	Fours

Thus at the end of a gathering period, the Fours register has a 1 in each position where a head has fired at least four times. We now enter a processing period.

This side also has an F ragister, which as we shall see has a 1 in each position corresponding to a head in an adjacency set, which set is thought by its processor to see a fire. We generate a new register, the W register:

Four or (Twos and F) → W

This register is to be made available to the other processor, via a DMA operation, in this form. Likewise a similar register, W', from the other processor has been received from the other side.

3 (contd)

Another register, the H register, contains a 1 in each position corresponding to a head which passed the last test and is therefore assumed to be working We make this available to the other side and have received their, H', register.

We now apply adjacency rules to these registers.

4. ADJACENCY INFORMATION

I propose the following configuration of the byte containing the adjacency information ("configuration" byte).

Bit 0 = for bit-serial data transfer, not hard-wired.
1 = master/slave initialization bit.
2 = fourth level adjacency bit.
3 = third level adjacency bit
4,5,6 = second level adjacency bits
7 = first level (OPTION PAIR = 1, SPLIT= 0)

Data Bus Bit Configuration byte

7	6	5	4	3	2	1	0
1	2nd			3	4	X	X

At each level of adjacency we consolidate relevant data in the W, W', H and H' registers and fill the cleared spaces with 0's (W,W') or 1's (H, H'). The processing is the same for the W and W' registers, and for the H and H' registers.

5. FIRST LEVEL ADJACENCY

If OPTION PAIR (bit 7 of configuration byte = 1)

(W or $\overset{\text{4 spaces}}{\underset{\text{W}}{\longleftarrow}}$) and $11110000_2 \rightarrow$ W

(H or $\overset{\text{4 spaces}}{\underset{\text{H}}{\longleftarrow}}$) or $00001111_2 \rightarrow$ H

where the superscript arrow indicates a shift in the direction shown (not ring shift).

We can now treat the two options together, with the adjacencies for 1, 2, 3 and 4 repeated for 5, 6, 7 and 8.

6. SECOND LEVEL ADJACENCY

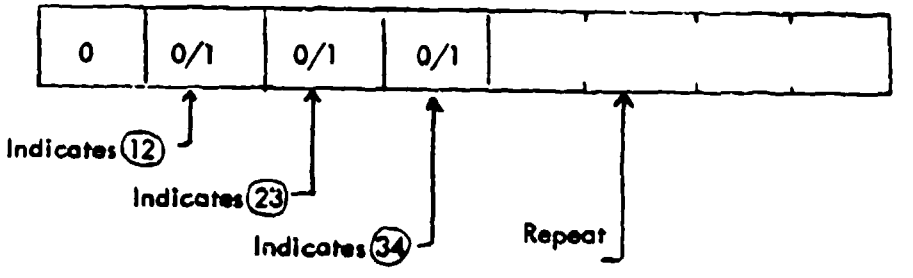
Reconfigure second level adjacency information :

Configuration and 01110000 $\longrightarrow$ Adj 2

Adj 2 or $\xrightarrow[\text{Adj 2}]{\text{4 spaces}}$ $\longrightarrow$ Adj 2

The upper and lower half-bytes of Adj 2 are identical and we describe only the processing associated with the former.

A one in a position of Adj 2 states that the corresponding head is adjacent to the head corresponding to the position on the left, this



The processing is:

W or $\overleftarrow{(W \text{ and } Adj2)}$ and not (Adj 2 and (not $\overleftarrow{Adj\ 2}$)) $\rightarrow$ W

H or $\overleftarrow{(H \text{ and } Adj\ 2)}$ or (Adj 2 and (not $\overleftarrow{Adj\ 2}$)) $\longrightarrow$ H

H now has all ones except in the first position of an adjacency set (as so far specified) none of whose heads (on its side) are working. W now has ones in the first position of an adjacency set any of whose heads (on its side) have fired sufficiently often in the last gathering phase, and in no other position.

7. THIRD LEVEL ADJACENCY

Third level adjacency may be used to declare the adjacency of lower level adjacency sets.

Take:

Adj 3 = 10001000 if third level adjacency bit = 1

Adj 3 = 00000000 " " " " " = 0,

(i.e. no third level adjacency).

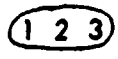
The processing is:

W or (W and Adj 3) and not Adj 3 → W

H or (H and Adj 3) or Adj 3 → H

Thus if we have the second level adjacencies

then third level adjacency can give



the relevant data being held in the head 2 (bit 6) position.

Note that third level adjacency should not be used unless the indicated second level adjacencies are declared. Failure to observe this may lead to a logical inconsistency and is forbidden.

8. FOURTH LEVEL ADJACENCY

Fourth level adjacency may be used to declare the adjacency of lower level adjacency sets.

Take:

Adj 4 = 00100010 if fourth level adjacency bit = 1

Adj 4 = 00000000 " " "" " = 0

The processing is:-

W or (W and Adj 4) and not Adj 4 → W

H or (H and Adj 4) or Adj 4 → H

Declaration of fourth level adjacency converts

Fourth level adjacency should not be used unless the indicated lower-order adjacencies are declared. Failure to observe this may lead to a logical inconsistency and is forbidden.

9. ADJACENCY TABLES

We list the permitted configuration bytes and generated adjacency sets.

Split

Configuration byte 1st	2nd	3rd	4th		Adjacency sets
0	000	0	0	XX	1 2 3 4 5 6 7 8
0	001	0	0	XX	1 2 (3 4) 5 6 (7 8)
0	010	0	0	XX	1 (2 3) 4 5 (6 7) 8
0	011	0	0	XX	1 (2 3 4) 5 (6 7 8)
0	100	0	0	XX	(1 2) 3 4 (5 6) 7 8
0	101	0	0	XX	(1 2) (3 4) (5 6) (7 8)
0	110	0	0	XX	(1 2 3) 4 (5 6 7) 8
0	111	0	0	XX	(1 2 3 4) (5 6 7 8)
0	110	1	0	XX	(1 2 3) 4 (5 6 7) 8
0	111	1	0	XX	(1 2 3 4) (5 6 7 8)
0	111	1	1	XX	(1 2 3 4) (5 6 7 8)

Pair

Configuration byte 1st	2nd	3rd	4th		Adjacency sets
1	000	0	0	XX	(1 5) (2 6) (3 7) (4 8)
1	001	0	0	XX	(1 5) (2 6) 3 7 4 8
1	010	0	0	XX	(1 5) 2 6 3 7 (4 8)
1	011	0	0	XX	(1 5) (2 6) (3 7) (4 8)
1	100	0	0	XX	(1 5 2 6) (3 7) (4 8)
1	101	0	0	XX	(1 5 2 6) 3 7 4 8
1	110	0	0	XX	1 5 (2 6) 3 7 (4 8)
1	111	0	0	XX	1 5 (2 6) (3 7) 4 8
1	110	1	0	XX	1 5 2 6 3 7 (4 8)
1	111	1	0	XX	1 5 2 6 (3 7) 4 8
1	111	1	1	XX	1 5 2 6 3 7 4 8

9 (contd)

Note that none of the above adjacencies is equivalent to

(1 2) 3 4 5 6 7 8

or

(1 2) (3 4) (5 6) 7 8

which were mentioned in the interim report (D.840, 26th. June 1978)

Also note that we have used six configuration bits but only achieved 22 configurations, some of which are equivalent.

It is clear from the table that this adjacency system enables us fully to satisfy the current requirements of General Dynamics while providing a wide class of alternative adjacency arrangements should their requirements change.

The adjacency system has the further advantages of logical straighforwardness and of repetitive structure designed to enable efficient and economical programming.

The effect of the adjacency processing on W and H bytes is shown in a table in an appendix to this report.

10. FIRE/FAULT CONDITIONS

The H, H', W and W' bytes have now been fully processed according to the adjacency rules. The W register has 1's in positions where heads of the relevant adjacency sets have fired the relevant number of times (and in no other positions). The H register is all 1's except in certain positions where all heads in the relevant adjacency set (on this side) are not working.

Therefore:-

H or H' = 11111111 = FF_{16}

unless all heads on both sides in at least one adjacency set are not working, in which case we issue a fault condition.

Under the current hardware arrangements a fault conditions overrides a fire condition, and latches. This arrangement may not be optional for future systems/installations, and there are advantages in writing the software in such a way as to enable alternatives to be implemented in hardware. The fault processing is:-

i) If all the heads in an adjacency set on both sides of the system are not working a fault is issued and this set takes no further part in deciding whether there is a fire. (It is assumed that heads fail passive).

ii) If all the heads in an adjacency set on one side of the system are not working (or are unavailable because that side is switched off or not present) then only the remaining side is considered.

Thus the complete failure of an adjacency set issues a fault but does not inhibit the processor from issuing a fire condition from other adjacency sets, though current hardware arrangements prevent the fire condition being sent to the CWU.

We combine the W and H registers by:-

W or (not H) → W

W' or ((not H') and H) → W'

noting that ' is is the first ti... ...at the processing for the two sides has differed.

10 (contd.)

We also have available the W registers for the previous three periods (now named the X, Y and Z registers) and also the similar X' and Y' (though not the Z') registers. The fire condition is to be issued by our microprocessor when it decides an adjacency set has seen a fire, on both sides, over the last three periods. As the data gathering periods for the two sides are interleaved there are of course two ways of choosing the three periods concerned, depending on which sides gathering phase starts the sequence.

We generate an F (for fire) register.

(W or Z) and X and Y $\longrightarrow$ F

If (F and W' and X' and Y') $\neq$ 0

we issue a fire condition for confirmation by the other processor, if working. Note that if this condition does nc hold and a fire condition was already signalled, we do not rescind it; the reset process is defined below.

To derive the reset condition we use another register, the FL register, defined during the previous processing phase:

(F) and (W or W' or X or X') $\longrightarrow$ FL

if the new FL = 0 we issue a reset.

The inclusion of X or X' terms allows the fire condition to be maintained if one gate period is not filled, however 2 consecutive empty gates will result in a reset condition.

Note that we have assumed both processors to be working in the above. If one is switched off or absent, the reset conditic- is altered in an obvious way.

11. ADJACENCY SET FIRE DECLARATION

FL contains a 1 for each adjacency set now declaring an unreset fire state according to this processor side. We now have to reverse the adjacency processing and generate an F register to participate in the count of 2 or 4 decisions described above.

Fourth level = FL or ($\overrightarrow{FL}$ and Adj 4) → F

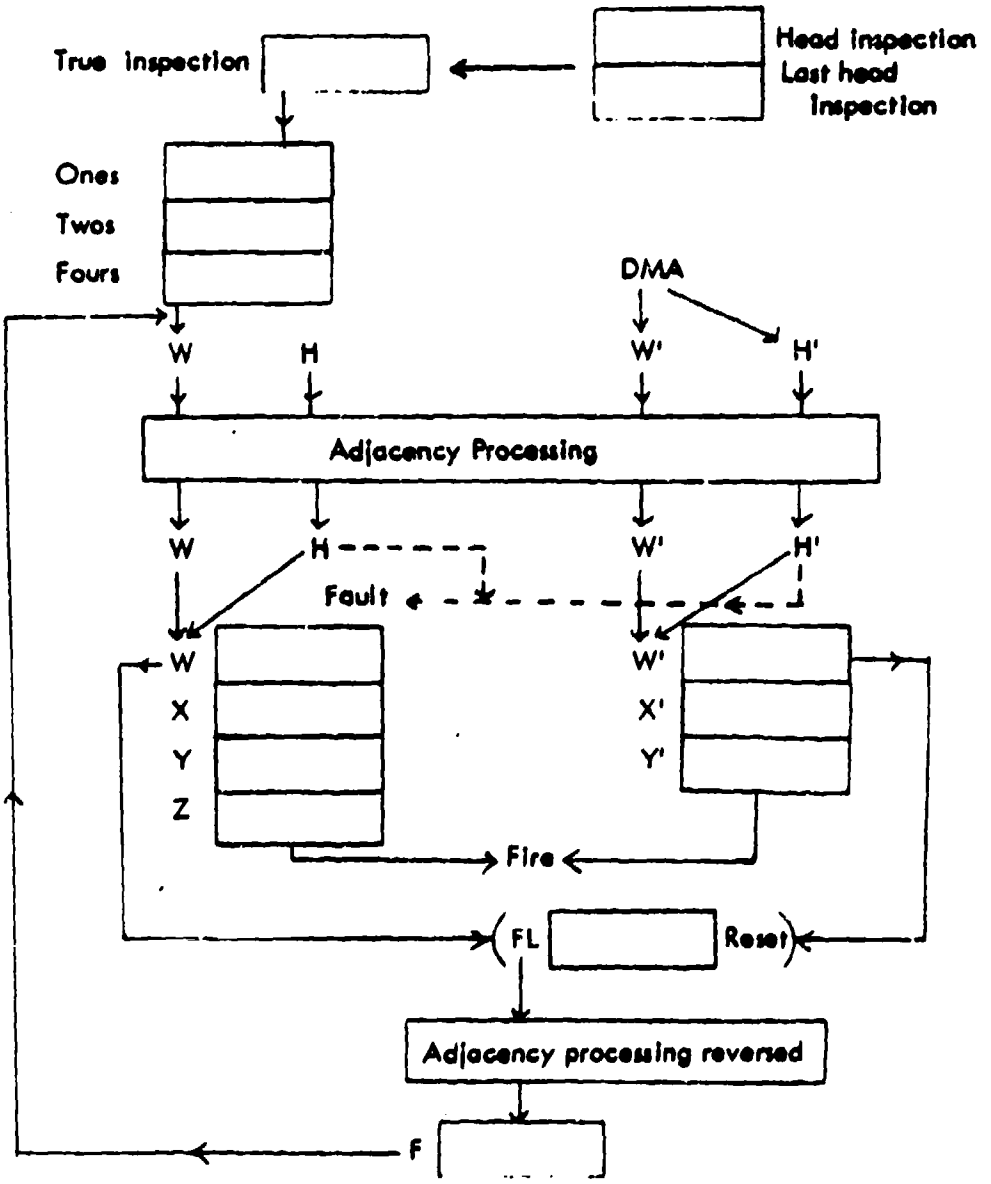
Third level = F or ($\overleftarrow{F}$ and Adj 3) → F

Second level = F or ($\overrightarrow{F}$ and Adj 2) → F

First level = If OPTION PAIR, F or $\xrightarrow[F]{4\ spaces}$ → F

Finally F has a 1 for each head in an adjacency set seeing a fire. (As a result, if a head is in two adjacency sets, its firing count requirement of 2 or 4 will be determined by either of the adjacency sets seeing a fire. This crosstalk only occurs when at least one side sees a fire, and is marginally beneficial.)

12. SCHEMATIC



APPENDIX 1

ALTERNATIVE DEFINITION OF "SEEING" A FIRE

The decision to perform the adjacency processing on the W and W' bytes implies and is implied by the definition of "seeing" a fire. We have defined this by adjacency set, requiring that for three successive gathering phases some head (not necessarily the same one) fires 4 or more times (on each of the A and B sides, according to all processors working.) An alternative and equally valid definition is to require the same head to fire 4 or more times for three successive gathering phases on side A, (and some head to do the same on side B, though by the adjacency these two heads need not belong to the same head pair.) Making this definition has implications for the probabilistic calculations of system reliabilities under different conditions, and for the methods of in-flight logging of fire and fault conditions. The change to the software is minimal however, it being necessary merely to perform the adjacency processing not on the W and W' bytes but on F and F', where these are derived from the unprocessed W, X, Y, Z, W', X', Y' bytes as

(W or Z) and X and Y → F

W and X and Y → F'

APPENDIX A-2

SOFTWARE ASSEMBLY LISTING

```
!M
0000 1              0001 ..********INITIALIZATION PROGRAMME********
0000 1              0002 STEPS=0070
0000 1              0003 ORG=0000          .. INITIALISATION PGM
0000 7100           0004 DIS. ...
0002 F800           0005 LDI=00
0004 B7             0006 PHI R7
0005 A9             0007 PLO R9
0006 F8FD           0008 LDI=FD            .. WILL CHANGE IF CODE MOVES
0008 A7             0009 PLO R7
0009 E7D7           0010 SEQ SEP R7
000B 1              0011 ORG=000B
000B F80C           0012 LDI=0C
000D B2             0013 PHI R2
000F B9             0014 PHI R9
000E F8AABF         0015 PHI R0 PHI RA PHI RF
0012 F8DFA0         0016 LDI=DF PLO RA     .. SET FOR D.M.A
0015 E9             0017 SEX R9
0016 6B             0018 INP 3             .. INPUTS GIE STATUS
0017 FA20           0019 ANI=20
0019 CA0070         0020 LBNZ STEPS
001C 19             0021 INC R9            .. R9 = 0C01
001D 72             0022 LDXA
001E F2             0023 AND
001F F01            0024 IPK
0020 F2             0025 AND       .. D NOW R9 IF 0C01   0C03 ALL R9
0021 FFA9           0026 SMI=A9
0023 32A1           0027 BZ FIRST    .. ZERO IF D A9
0025 F8A4           0028 LDI=04
0027 B9             0029 PHI R9      .. SET SUBROUTINE COUNTER
0028 F8B1           0030 LDI=B1
002A A9             0031 PLO R9
002B D9             0032 SEP R9
002C 1              0033          .. GO TO RAM TEST & RESET ROUTINE
002D F803           0034 LDI=03
002F A9             0035 PLO R9
0030 F8A9           0036 LDI=A9      .. R9 0C03
0032 73             0037 STXD
0033 73             0038 STXD
0034 73             0039 STXD
0034 1              0040          .. R9 = 0C00 AS IN 0C01 TO 0C03
0034 F8C7A9         0041 LDI=C7 PLO R9
0037 F8FFB9         0042 LDI=FF STR R9
003A 1              0043 ......SET GOOD HEADS
003A F8D3           0044 FIRST: LDI=D3
003C A9             0045 PLO R9      .. R9 0CD3
003D F8A0           0046 RETURN: LDI=A0    .. RESET W=X=Y=Z
003F 73             0047 STXD
0040 89             0048 GLO R9      .. W = X = Y
0041 FFCA           0049 SMI=CA      .. F = F
0043 3A50           0050 BNZ RETURN
0045 6C6C6C6C       0051 OUT 4 NOP NOP
0049 6C6C6C6C       0052 OUT 4 NOP NOP
004D F8DFA8AF       0053 LDI=DF PLO R8 PLO RF
0051 FE             0054 SHL RF
0052 72             0055 LDXA
0053 F2             0056 XOR
0054 FA04           0057 ANI=04
0056 1              0058          .. NON ZERO IF FAIL
0056 1              0059          .. PORT CHECK BIT OK
0057 1C11           0060 BIT BAD
```

```
0056 F829C00BD0!        LDI#29 LBR#0BD0
005B 2F!                DAK: DEC RF
005C !
005C F8B9AA!            LDI#B9 PLO RA
005F 72FAFA5A!          LDXA ANI#FA STR RA
0063 F0FAFA!            LDX ANI#FA   ..CLEARS OFF X BIT XDATA
0066 EAF3!              SEX RA XOR   .. ZERO IF L = R CONFIG
0068 326F!              BZ FIR
006A F830C00BD0!        LDI#30 LBR#0BD0
006F 0AFAFAFBAA!        FIR:LDN RA ANI#FA XRI#AA
0074 3A79F8FC5A!        BNZ YEW LDI#FC STR RA
0079 F8D7AF!            YEW:LDI#D7 PLO RF
007C 0AFAFC5F!          LDN RA ANI#FC STR RF  ..STORE CONFIG
0080 F8E6AA!            LDI#E6 PLO RA
0083 F8017373!          LDI#01 STXD STXD
0087 F8007373!          LDI#00 STXD STXD
008B F801F17373!        LDI#01 OR STXD STXD
0090 F8FEF273!          LDI#FE AND STXD
0094 F8FEF25A!          LDI#FE AND STR RA
0098 3C9F!              BN1 TOM
009A F8A7C00BD0!        FAULT: LDI#A7 LBR#0BD0  ..ERROR CODE 23 OPP SIDE IS
009F !                                          .. INHIBITING YOU
009F F80CBABB!          TOM: LDI#0C PHI RA PHI RB
00A3 F82BAA!            LDI#2B PLO RA    .. RA 0C2B
00A6 E3!                SEX RA
00A7 F80073!            LDI#00 STXD
00AA F82C73!            LDI#2C STXD    .. ROM CHECK CONSTANT
00AD F80673!            LDI#06 STXD    .. 16 SEC TIMER CONS
00B0 F80173!            LDI#01 STXD    .. 15 SEC TIMER CONS
00B3 2A2A!              DEC RA DEC RA
00B5 F80073!            LDI#00 STXD    .. CLEAR 0C20 TO 0C25
00B8 2A73737373!        DEC RA STXD STXD STXD
00BD F822AAF8025A60!    LDI#22 PLO RA LDI#02 STR RA IRX
00C4 !
00C4 !
00C4 F8A05A!            LDI#A0 STR RA
00C7 64!                OUT 4         .. SET TIME SHAPE
00C8 F800A5!            LDI#00 PLO R5    .. LOAD DELAY CONST
00CB F8FFB5!            LDI#FF PHI R5
00CE 35EA!              START: B2 DELAY   .. IF OPP T/S = 0 GOTO DELAY
00D0 !
00D0 C4C4C4C4C4!        NOP NOP NOP NOP NOP
00D5 0AFA02!            HALF:LDN RA ANI#02  .. AM I MASTER?
00D8 CA0111!            LBNZ GO
00DB F822AA!            LDI#22 PLO RA    .. IF SLAVE RESET T/S
00DE C4F0FA7F!          NOP LDX ANI#7F
00E2 5A64!              STR RA OUT 4
00E4 F8FFA0!            LDI#FF PLO R0
00E7 C0012D!            LBR EXTRA
00EA 3DD5!              DELAY: BN2 HALF
00EC 253DD5!            DEC R5 BN2 HALF
00EF 953DD5!            GHI R5 BN2 HALF
00F2 3AEA!              BNZ DELAY
00F4 F81DAA!            LDI#1D PLO RA
00F7 F89073!            LDI#90 STXD       .. STO ERROR CODE
00FA F826AB!            LDI#26 PLO RB
00FD 4B73!              LDA RB STXD     .. STO HI TIMER
00FF 0B73!              LDN RB STXD    .. STO LO TIMER
0101 F825AA!            LDI#25 PLO RA
0104 F810!              LDI#10
```

```
0106 F173:
0108 F3A2:
010A F173:
010C F3A9:
010E F193:
0110 64:
0111 :
0111 343AF306B1A1:
0117 F30CB5BEBF:
011C F3C3A5:
011E F301B4:
0122 F310A6:
0125 F330A2:
0128 F30BB9:
012B F300A3:
012E D4:
012F 5EE7:
0131 7077:
0133 F301B3:
0136 F37DA3D3:
013A C000A8:
013D F329A8:
0140 F301F1:
0142 93:
0144 7001111:
0147 :
0A00 07:
0A01 :
0A01 F3EFA9:
0A04 F3A0:
0A06 :
0A06 B9:
0A07 :
0A07 F3AA:
0A09 7A:
0A0A 9A:
0A0B 74B7:
0A0D F3AA99:
0A10 7A:
0A11 FFAA:
0A13 7ACA:
0A15 9A:
0A16 7AC0:
0A18 F3:
0A1A F330:
0A1C C00PD0:
0A1F F3A0:
0A21 B9:
0A22 F3EF:
0A24 A9:
0A25 :
0A25 F399:
0A27 7A:
0A28 3A:
0A29 7AD9:
0A2B F399:
0A2D 99:
0A2E 7A:
0A2F 7A99:
0A31 3A:

0121 OP :TXD     .. :TO OTHER PPO DEAD
0122 LDI#03
0123 OP :TXD
0124 LDI##A
0125 OP :TP P8
0126 OUT 4
0127
0128 GO: R1 :POT LDI#06 PHI P1 PLO P1  .. P1 0606
0129 LDI#0C PHI P5 PHI PE PHI PF
0130 LDI#C3 PLO P5     .. LOAD TIMER #C3
0131 LDI#01 PHI P6     .. P6 0110
0132 LDI#10 PLO P6
0133 LDI#30 PLO P2
0134 LDI#0F PHI P9
0135 LDI#00 PLO P9
0136 :EP P9
0137 :TP PE :EX P7
0138 RET. #77
0139 LDI#01 PHI P3
0140 LDI#70 PLO P3 :EP P3
0141 :POT:LBP FAULT
0142 EXTPA: LDI#25 PLO P8
0143 LDI#01 OP
0144 :TP P8
0145 LBR G0
0146 OP#=#AB0
0147 PAROT: :EP P7     .. PAM TE: : PETE: ROUTINE
0148
0149 PNTAP: LDI#FF PLO P5
0150 LDI##
0151
0152 PHI P5    .. P5 0FFF
0153
0154 AGAIN: LDI#AA
0155 :T D
0156 GLO P5
0157 BNZ AGAIN     .. NOTE AA NOT :TORED > 00
0158 LDI#AA :TP P5
0159 :EC: LDXA
0160 :MI#AA
0161 BNZ BAD
0162 GLO P5
0163 BNZ :EC
0164 BP HOP
0165 BAD: LDI#20
0166 LBR##BD0    .. TO LACHEL
0167 HOP: LDI##C
0168 PHI P5
0169 LDI#FF
0170 PLO P5
0171
0172 POUND: LDI#55
0173 :TXD
0174 GLO P5
0175 BNZ POUND
0176 LDI#55        .. 0000 NOW 55
0177 :TP P5
0178 THRO: LDXA
0179 :MI#55
017B BNZ THRO
```

```
0AF3 PS1
0AF4 BADE1
0AF6 PS1
0AF7 C41
0AF8 C41
0AF9 F3001
0AFB PS1
0AFC PS1
0AFD >AF91
0AFF >0B05
0AF1 :
0AF1 :
0000

* E+H-L-U=
```

```
0131 GLO PS
0132 BNZ THPD
0133 DEC PS
0134 NOP
0135 NOP
0136 FRTH: LDI>00   .. PS >CFF
0137 ITXD
0138 GLO PS
0139 BNZ FRTH
0130 BP BAKOT  ..RESETS ALL RAM EXCEPT >C00
0131                .. PS NOW >C00
0132 END
```

Data Sheet: DC,7306
Sheet: 5
Issue: A

```
!M
0000 :          0001  ..********BACKGROUND PROGRAMME******
0000 :          0002
0000 :          0003   .. IT CHECKS ROM CONTENTS ONE PAGE PER
0000 :          0004 ..GATHER PHASE EXCEPT AT SIZE UP
0000 :          0005
0000 :          0006 XREG=000
0000 :          0007 ROMCNT=00C
0000 :          0008 LCHFLT=00RD0
0000 :          0009 ORG=0170
0170 F80CBC:    0010 ENTRY: LDI00C PHI ROMCNT
0173 BDF82CAD:  0011 PHI XREG LDI02C PLO XREG
0177 ED:        0012 SEX XREG                          .. XREG = 002C
0178 F800AC:    0013 LDI000 PLO ROMCNT        .. ROMCNT = 0C00
017B F823ADAD:  0014 LDI027 PLO RD LDN RD
017F FA8032DA:  0015 ANI080 BZ GONIGL ..TO HERE REQ'D BY
0183 :          0016              ..SLAVE FOR GOOD START UP
0183 F823ADAD:  0017 HELIUM:LDI023 PLO RD LDN RD ..O P REG
0187 FA8032B3:  0018 ANI080 BZ HELIUM
018B 3EFFC03BCE: 0019 GLO R8 XRI0C0 BNF WAITE1
0190 F82CAD:    0020 LDI02C PLO RD
0193 F800:      0021 LDI000
0195 5D:        0022 STR XREG                  .. CLEAR RAM LOC002C
0196 2C:        0023 NEON: DEC ROMCNT
0197 0CF4:      0024 LDN ROMCNT ADD
0199 5D:        0025 STR XREG
0199 3C3A96:    0026 GLO ROMCNT BNZ NEON
019D 2D:        0027 DEC XREG
019E 9C5DAC:    0028 PHI ROMCNT STR XREG PLO ROMCNT
01A1 F800BC:    0029 LDI000 PHI ROMCNT
01A4 0CA0F5:    0030 LDN ROMCNT IRX SD
01A7 3AC9:      0031 BNZ FAULT
01A9 2D72:      0032 DEC XREG LDXA
01AB C4C4:      0033 NOP NOP
01AD 32B5:      0034 BZ ROMOK
01AF BC:        0035 PHI ROMCNT
01B0 F800AC:    0036 LDI000 PLO ROMCNT
01B3 3083:      0037 BR HELIUM
01B5 F825AD:    0038 ROMOK: LDI025 PLO XREG
01B8 F800:      0039 LDI00A
01BA F15D:      0040 OR STR XREG               .. SET ROM OK BIT
01BC :          0041                           .. THIS WILL BE TRANSMITTED
01BC :          0042                           .. TO OPP PROCESSOR VIA DMA
01BC :          0043
01BC F80CBC:    0044 LDI00C PHI ROMCNT ..REINITIALIZE
01BF BDF82CAD:  0045 PHI XREG LDI02C PLO XREG
01C3 EDF800AC:  0046 SEX XREG LDI000 PLO ROMCNT ..ROMCNT=0C00
01C7 3083:      0047 BR HELIUM
01C9 F8FFC00RD0: 0048 FAULT:LDI0FF LBR LCHFLT
01CE F825ADOD:  0049 WAITE1:LDI025 PLO RD LDN RD
01D2 FA01 32CE: 0050 ANI001 BZ WAITE1
01D6 F80CB7:    0051 GONIGL: LDI00C PHI R7
01D9 F8 ...:    0052 LDI022 PLO R7 LDN R7
01DD FA0FF80257: 0053 ANI00C ORI0.. STR R7
01E2 F8..A7F800B7: 0054 LDI005 PLO R7 LDI002 PHI R7
01E8 D7:        0055 SEP R7 ..GO TO FIRE PROG
01E9 ED3083:    0056 SEX RD BR HELIUM
01EC :          0057 ORG0A00
0A00 5CD17E7550CC44 0058 .05C.0D1.07E.075.050.0CC.044.0B3
0A07 B3:        0059
0A08 AEB31C46FFFFFF 0060 .0AE.0B3.01C.046.0FF.0FF.0FF.091
0A0F 91:        0061
0A10 :          0062
0A10 :          0063        ..THESE ARE PARITY BITS
0A10 :          0064       ..TO SUIT BACKGROUND PROG.
....            0065   END
```

```
0001 ..oooooooGATHER PHASE INTERRUPT PROGRAMMEooooooo
0002                .. REGISTER ALLOCATION:
0003
0004
0005 DMPNTR=n00     .. R0 THE DMA STACK
0006 IRCNTR=n01     .. R1 THE INTERRUPT ADDRESS
0007 ISCNTR=n02     .. R2 THE INTERRUPT STACK
0008 MPCNTR=n07     .. MAIN PROGRAMME COUNTER
0009                ..  R3 ALLOCATED
0010 IOSTAT=n04     .. R4 A WORKING REGISTER
0011                .. HI IOSTAT CONTAINS INTERNAL FLAGS INF
0012                .. LO IOSTAT CONTAINS SYS STATUS
0013                .. HI IOSTAT = OPADII
0014                .. LO IOSTAT = OPADI
0015 TIMER=n05      .. LO TIMER IS THE INTERRUPT TIMER
0016                .. IS DECREMENTED ON EVERY INTERRUPT
0017                .. HI TIMER IS USED AS A TEMP
0018                .. WORKING REGISTER.
0019 TEMP=n03       .. IS USED AS A TEMP REGISTER
0020
0021
0022 DMAPUT=n06     .. ALLOCATED FOR DMA ROUTINE
0023
0024 VREG=n08       .. VREG IS MAIN WORKING REGISTER
0025
0026
0027                .. RAM LOCATIONS (OUTPUT)
0028
0029
0030 OPMIII=n20     .. W DATA TO DMA>
0031 OPAMII=n21     .. TEMP MEM LOCATION
0032 OPAMI=n22      .. I DATA TO DMA>
0033
0034
0035 OPADP=n23      .. OUTPUT STATUS
0036                .. DATA WILL BE OUTPUTTED FROM
0037                .. THIS LOCATION
0038 OPADI=n24      .. REAL OUTPUT STATUS
0039 OPADII=n25     .. INTERNAL FLAGS INF
0040 OPAIII=n26     .. MAIN TIMER (HI) CLOCK>
0041 OPADIV=n27     .. MAIN TIMER (LO>
0042 OPADV=n28      .. 1S SEC TIMER
0043 OPADVI=n29     .. 1S SEC TIMER
0044 OPAVII=n2A     .. POM CHECK TIMER
0045                .. THE 1S SEC > THE POM CHECK
0046                .. TIMERS ARE SET WHEN INF FROM
0047                .. OPP PROCESSOR IS RECEIVED -
0048                .. BY NIGEL
0049
0050
0051                .. RAM LOCATIONS (INPUT)
0052
0053
0054 INPMIV=n40     .. 4 I REGISTER
0055 INMIII=n41     .. 3 I REGISTER
0056 INPMII=n42     .. 1 I REGISTER
0057 INPMI=n43      .. INSPECTION REGISTER
0058 INPADP=n44     .. INPUT HEAD DATA TO
0059                ..    THIS LOCATION
0060 INPADI=n4A     .. INPUT IF I PUTTON STATUS TO
```

```
0000 ;                                      .. THIS LOCATION.
0000 ;
0000 ;          LACHFL=0000DG               .. ADDRESS OF LACH FAULT PGM
0000 ;          PROCES=000010
0000 ;          ORG0000
0600 E2;        EXIT: SEX R2
0601 60;        IRX
0602 72;        LDXA
0603 7E;        SHL
0604 72;        LDXA
0605 70;        RET
0606 22;        DEC R2
0607 78;        SAV .. SAVE T
0608 22;        DEC R2
0609 73;        STXD .. SAVE D
060A 76;        SHRC
060B 73;        STXD                        .. SAVE DF
060C F844A8;    LDI INPADR PLO XREG         .. INITIALISE INPUT ADDRESS
060E ;                                      .. TO LOAD INPUT HEAD DATA
060E E8;        SEX XREG                    .. THIS STEP AGAIN MAY NOT BE NECESS
0610 ;
0610 ;                                      .. IF X HAS BEEN INITIALISED ALREADY
0610 6E;        INP 7                       .. AND HAS NOT BEEN MODIFIED.
0611 ;                                      .. TO PUT HEAD DATA AND STORE ON
0611 ;                                      .. LOCATION POINTED BY XREG
0611 ;                                      .. NOTE INPUTTING HAS TO BE DONE
0611 F8[illegible]A8;   LDI OPADII PLO XREG .. WITHIN 24 INSTRUCTION CYCLES
0614 [illegible]        LDX ANI040 DEC XREG LSZ LDI00C
061B [illegible]        OR ANI00F SHI TIMER DEC XREG
0620 [illegible]        LDX ANI0F2 STR XREG
0624 [illegible]        SHI TIMER OR STR XREG
0627 [illegible]        IRX LDXA PLO IOSTAT
062A [illegible]        LDX PHI IOSTAT
062C [illegible]        DEC XREG DEC XREG OUT 4
062E [illegible]        IRX
0630 [illegible]        BN4 SUE
                                            .. BRANCH TO SUE IF ALARM RETURN =
0632 FA40;      ANI040                      .. TEST TEST FLAG
0634 [illegible]        BNZ MARY            .. BRANCH IF TEST FLAG = 1
0636 [illegible]        DECTIM: DEC TIMER
0637 [illegible]        LDI OPADR
0639 [illegible]        PLO XREG
063A [illegible]        LDN
063B FA[illegible]      ANI0[illegible]     .. TEST TIME SHARE
063D [illegible]        LBZ PROCES
0640 ;                                      .. IF TIME SHARE = 0 DO PROCESS
0640 ;          .. ENTER FIRE ROUTINE       .. ELSE GATHER
0640 F84[illegible]     GATHER: LDI INPMI
0642 A8;        PLO XREG                    .. X = INPMI
0643 [illegible]        LDXA
0644 FBFF;      XRIOFF                      .. COMPLIMENT INS REG
0646 F2;        AND
0647 28;        DEC XREG                    .. FORM NEW INS
0648 73;        STXD
0649 F2;        AND                         .. INS AND ONES = 2'C
064A B[illegible];      PHI TIMER           .. STORE 2'C ON HI TIMER
064B 28;        DEC XREG
064C F2;        AND
064D 28;        DEC XREG                    .. 2'C AND 2'C = 4'C
064E F1;        OR                          .. 4'C OR [illegible]
064F [illegible]        STR XREG
```

```
                    0121 LDI INPMI
                    0122 PLO XPEG
                    0123 LDX
                    0124 DEC XPEG           ..  INC XOP ONE? = ONE?
                    0125 XOP
                    0126 STXD
                    0127 GHI TIMER          ..  SAVE XOP TWO ? = TWO ?
                    0128 XOP
                    0129 STR XPEG           ..  EXIT FROM FIRE ROUTINE
                    0130 GLO TIMER
                    0131 SMI 13             ..  IF INT TIME IS = 13
                    0132 BNZ EXIT           ..  BRANCH TO EXIT
                    0133 LDI OPADR
                    0134 PLO XPEG
                    0135 LDX
                    0136 ANI#20             ..  TEST EMITTER ON
                    0137 BNZ PETER          ..  IF SO BRANCH
                    0138 B3 JAMES           ..  ( X POINTS TO OPADP )
                    0139                    ..  VERIFY EMITTER ACTIVE
                    0140 RESETS: LDI 214    ..  ( THIS SHOULD BE OFF )
                    0141 PLO TIMER          ..  SET TIMER 214
                    0142 LDI#6F         .. RESET GSE 1
                    0143 AND                ..  RESET TIME SHAPE
                    0144 STR XPEG
                    0145 OUT 3              ..  NOW X POINTS TO OPADI
                    0146 NIGEL: IRX LDI#01 OR   STR XPEG
                    0147 BR EXIT
                    0148 PETER: BN3 JOHN
                    0149 DEC XPEG           ..  X = OPADP
                    0150 LDI#04             ..  D = OPADI
                    0151 AND                .. TEST HV BIT
                    0152 IRX                ..    = OPADP
                    0153 BZ RESETS          .. IF HV HAS BEEN SET BRANCH TO RESETS
                    0154 LDI#6F             .. RESET GSE 1
                    0155 AND                .. RESET EMITTER DRIVE
                    0156 STR XPEG
                    0157 OUT 3 DEC XPEG
                    0158 LDI#07
                    0159 DELAY: GHI TIMER GHI TIMER SMI#01
                    0160 BNZ DELAY
                    0161 BN3 RESETS
                    0162 LDI#05
                    0163 LBR LACHEL
                    0164 JOHN: LDI#03
                    0165 LBR LACHEL         .. VERIFY EMITTER ACTIVE
                    0166                    ..  SHOULD HAVE BEEN OFF
                    0167 JAMES: LDI#04
                    0168 LBR LACHEL         .. VERIFY EMITTER
                    0169                    ..  SHOULD HAVE BEEN ON
                    0170 JULIE: ANI#40
                    0171 BNZ JULIE          ..  TEST. TEST FLAG
                    0172 GLO IOSTAT         ..  TEST FIRE STATUS
                    0173 ANI#04
                    0174 BNZ DECTIM         ..  IF FIRE = 1 GO TO NORMAL PROGRAMM

                    0175 GLO TIMER          ..  TEST TIMER TO SEE IF IT HAS COUNT

                    0176                    ..  AT LEAST TWO INTERRUPT PERIODS
                    0177                    ..  ( IF NOT GO TO NORMAL PROGRAMME )
                    0178 LDI 209
                    0179 BM DECTIM
                    0180 PI DECTIM          ..  IF OPERATIONAL PROCESSOR HAS
```

```
06A0 :
                        0191                        ;;  INHIBITTED YOU GO TO NORMAL PROGR
06A0 F803C00BD0:        0192 LDI=02 LBR LACHFL          ;; LOAD FAULT NO.2
06A5 F833:              0193 JULIE: LDI OPADP
06A7 A9:                0194 PLO XPEG               ;; X = OPADP
06A8 E0:                0195 LDX
06A9 FAF3:              0196 ANI=F3                 ;; RESET INH/FIPE BITS ( TO ZERO)
06AB 53:                0197 STR XPEG
06AC 60:                0198 IPX
06AD 60:                0199 IPX
06AE E0:                0200 LDX                    ;; Y = OPADII
06AF FABF:              0201 ANI=BF                 ;; RESET TEST FLAG STATUS
06B1 73:                0202 STXD                   ;; X = OPADI
06B2 E0:                0203 LDX
06B3 FA0C:              0204 ANI=0C
06B5 23:                0205 DEC XPEG               ;; COPY INH/FIPE STATUS
06B6 F1:                0206 OR                     ;; TO OPADP
06B7 53:                0207 STR XPEG           ;; X = OPADP
06B8 64:                0208 OUT 4
06B9 30361:             0209 BP DECTIM
06BB F83F8A81:          0210 MARY: LDI=25 PLO XPEG
06BE F8FABF731:         0211 LDX ANI=BF STXD        ;; RESET TEST FLAG
06D2 :                  0212                        ;; BIT & DC25
06D2 F8FA021:           0213 LDX ANI=02
06D5 3B361:             0214 BNZ DECTIM
06D7 231:               0215 DEC XPEG
06D8 F8FA021:           0216 LDX ANI=02
06DB 3B361:             0217 BNZ DECTIM
06DD 3A361:             0218 BI DECTIM
06DF F801C00BD01:       0219 LDI=01 LBR LACHFL
06E4 :                  0220 END
0000

FAILURE
```

```
:M
0000 :                0001 ..●●●●●●●PROCESS PHASE INTERRUPT PROGRAMME●●●●●●●
0000 :                0002
0000 :                0003                .. REGISTER ALLOCATIONS
0000 :                0004
0000 :                0005 EXIT=#0600
0000 :                0006
0000 :                0007
0000 :                0008 DMPNTR=#00     .. R0 THE DMA STACK
0000 :                0009 IRCNTR=#01     .. R1 THE INTERRUPT ADDRESS
0000 :                0010 ISCNTR=#02     .. R2 THE INTERRUPT STACK
0000 :                0011 MRCNTR=#07     .. MAIN PROGRAMME COUNTER
0000 :                0012                ..  R7 ALLOCATED
0000 :                0013 IOSTAT=#04     .. R4 A WORKING REGISTER
0000 :                0014                .. HI IOSTAT  CONTAINS INTERNAL FLAGS INF
0000 :                0015                .. LO IOSTAT CONTAINS DEVICE STATUS
0000 :                0016                .. HI IOSTAT = OPADII
0000 :                0017                .. LO IOSTAT = OPADI
0000 :                0018 TIMER=#05      .. LO TIMER IS THE INTERRUPT TIMER
0000 :                0019                .. IS DECREMENTED ON EVERY INTERRUPT
0000 :                0020                .. HI TIMER IS USED AS A TEMP
0000 :                0021                .. WORKING REGISTER.
0000 :                0022 TEMP=#03       .. IS USED AS A TEMP REGISTER
0000 :                0023
0000 :                0024
0000 :                0025 DMAPUT=#06   .. ALLOCATED FOR DMA ROUTINE
0000 :                0026
0000 :                0027 XREG=#08       .. XREG IS MAIN WORKING REGISTER
0000 :                0028
0000 :                0029
0000 :                0030                .. RAM LOCATIONS (OUT PUT)
0000 :                0031
0000 :                0032
0000 :                0033 OPMIII=#20   .. M DATA (TO DMA)
0000 :                0034 OPAMII=#21   .. TEMP MEM LOCATION
0000 :                0035 LATCHEL=#0BDA
0000 :                0036 OPAMI=#22    .. I DATA (TO DMA)
0000 :                0037 OPADR=#23    .. OUT PUT STATUS
0000 :                0038                .. DATA WILL BE OUT PUTTED FROM
0000 :                0039                .. - THIS LOCATION
0000 :                0040 OPADI=#24    .. REAL OUT PUT STATUS
0000 :                0041 OPADII=#25   .. INTERNAL FLAGS INF
0000 :                0042
0000 :                0043 OPAIII=#26   .. MAIN TIMER LO
0000 :                0044
0000 :                0045 OPADV=#27    .. MAIN TIMER HI
0000 :                0046 OPADV=#28    .. 1S SEC TIMER
0000 :                0047 OPADVI=#29   .. 1m SEC TIMER
0000 :                0048 OPAVII=#2A   .. ROM CHECK TIMER
0000 :                0049                .. THE 1m SEC / THE ROM CHECK
0000 :                0050                .. TIMERS ARE SET WHEN INF FROM
0000 :                0051                .. OPP PROCESSOR IS RECEIVED
0000 :                0052
0000 :                0053
0000 :                0054              .. RAM LOCATIONS (IN PUT)
0000 :                0055
0000 :                0056
0000 :                0057 INPMIV=#40   .. 4TH REGISTER
0000 :                0058 INMIII=#41   .. 3RD REGISTER
0000 :                0059 INPMII=#42   .. 1ST REGISTER
0000 :                0060 INPMI=#43    .. INSPECTION REGISTER
```

```
0000 ;                  0041 INPADP=044     .. INPUT HEAD DATA TO
0000 ;                  0042                .. - THIS LOCATION
0000 ;                  0043 INPADI=045     .. INPUT TEST BUTTON STATUS TO
0000 ;                  0044                .. THIS LOCATION.
0000 ;                  0045 OPG=0A10
0310 94:                0046 PROCES: GHI IO^STAT   .. IS OTHER PROCESSOR DEAD
0311 FA10:              0047 ANI=10
0313 3A03:              0048 BNZ DEAD              .. IF SO BR TO DEAD PGM
0315 ;                  0049
0315 F8:                0050 GLO TIMER
0316 32D3:              0051 BZ INHOPP             .. IF TIMER = 00 GO TO INHOPP
0318 FD^7C^05^B0:       0052 SDI=7C LBNF=05^B0 .. BR TO DMA PGM
031D 3633:              0053 BZ SETTIM
031F C0^05^B0:          0054 LBR 05^B0
0322 F833:              0055 SETTIM: LDI OPADP  .. X = OPADP
0324 A1:                0056 PLO XPEG
0325 F830:              0057 LDI=30                .. SET TIME SHAPE BASE 1
0327 F1:                0058 OR
0328 91:                0059 STR XPEG
0329 21:                0060 OUT 4
032A F804:              0061 LDI 214           .. X = OPADI
032C A8:                0062 PLO TIMER
032D A0:                0063 IRX               .. X = OPADII
032E F808:              0064 LDI=08
0330 F2:                0065 AND
0331 B8:                0066 PHI TIMER         .. X = OPADII.STORE POM STATUS
0332 ;                  0067                   .. ON HI TIMER
0332 F8F7:              0068 LDI=F7
0334 F2:                0069 AND
0335 73:                0070 STXD              .. CLEARS POM STATUS FROM OPADII
0336 23:                0071 DEC XPEG          .. TEST FOR CLEAR IS
0337 23:                0072 DEC XPEG          ..   = OPAMI
0338 C4:                0073 NOP               .. REMOVE LATER
0339 38:                0074 SKI TIMER
033A F1:                0075 OR
033B 91:                0076 STR XPEG          .. STORE POM STATUS
033C A0:                0077 IRX
033D F8D0:              0078 LDI=D0
033F F2:                0079 AND
0340 91:                0080 STR XPEG          .. RESET MED TEST FAULT = ZERO
0341 F844^A4:           0081 LDI INPADI PLO XPEG   .. SET    INPADI TO INPUT
0344 ;                  0082                       .. FAULT - FIRE BUTTON INF
0344 68:                0083 INP 3
0345 FBFF:              0084 XRI=FF                .. COMPLEMENT
0347 FA12:              0085 ANI=12
0349 38:                0086 SKI TIMER
034A F8^4A^01:          0087 LDI OPADII PLO XPEG   .. X= FLAGS LOC
034D F800:              0088 LDI=00                .. CLEAR FAULT FIRE BUTTON
034F F2:                0089 AND                   .. STATES
0350 91:                0090 STR XPEG
0351 38:                0091 SKI TIMER
0352 FA02:              0092 ANI=02
0354 F1:                0093 OR                    .. COPY FAULT BUTTON STATES
0355 73:                0094 STXD                  .. TO FLAGS LOC
0356 ;                  0095
0356 FA02F1:            0096 ANI=02 OR         .. FAULT BUTTON OR TRU FAULT
0359 FA02:              0097 ANI=02
035B 23:                0098 DEC XPEG
035C F1:                0099 OR
035D 91:                0100 STR XPEG
```

```
                    0121 GHI TIMEP
                    0122 ANI#10
                    0123 SHL            .. COPY FIRE BUTTON STATUS
                    0124 ANI#20         .. TO FLAGS LOCATION
                    0125 OR
                    0126 STP XPEG
                    0127 IRX
                    0128 IRX
                    0129 ANI#20
                    0130 OR
                    0131 STP XPEG
                    0132 LDX ANI#20         .. IF FIRE TEST = 1
                    0133 LBZ PEACE           .. RECORD TIME ON
                    0134 LDI#26 PLO XPEG    .. LOCATION$
                    0135 LDXA PHI DMAPUT    .. 0C1E & 0C1F
                    0136 LDX PLO DMAPUT     .. ( HI & LO BYTES )
                    0137 LDI#1F PLO XPEG
                    0138 GHI DMAPUT STXD
                    0139 GLO DMAPUT STXD
                    0140 LDI#29 PLO XPEG
                    0141 LDI#00 OR STP XPEG
                    0142 PEACE: DEC XPEG DEC XPEG
                    0143 OUT 4
                    0144 PPOGRM: LDI OPAVII
                    0145 PLO XPEG
                    0146 LDX
                    0147 SM[n01
                    0148 STXD
                    0149 LBZ POWFLT
                    0150 SIXCHK: LDX
                    0151 SM[n01
                    0152 STXD
                    0153 LBZ SIXFLT
                    0154 FIFCHK: LDX
                    0155 SM[n01
                    0156 STP XPEG
                    0157 LBNZ SETPAR
                    0158 LDI 44
                    0159 STXD
                    0160 LDX
                    0161 AD[n01
                    0162 STXD
                    0163 LBNZ NOFLO
                    0164 LDX
                    0165 AD[n01
                    0166 STP XPEG
                    0167 NOFLO: DEC XPEG
                    0168 LDI#04
                    0169 OR
                    0170 STXD
                    0171 DEC XPEG
                    0172 LDI#A0         .. SET GSE 2 & EMITTER
                    0173 OR
                    0174 STXD
                    0175 LDI#04
                    0176 OR
                    0177 STP XPEG
                    0178 SETFLG: LDI OPAD11
                    0179 PLO XPEG
                    0180 LDI #40        .. SET TEST FLAG
```

```
                        0131 DF
                        0132 ITXD           .. X = OPADI
                        0133 DEC XPEG       .. X = OPADP
                        0134 OUT 4
                        0135 SETPAM: LDI#01 PHI P6
                        0136 LDI#10 PLO P6
                        0137 LBR EXIT
                        0138 DEAD: GLO TIMEP
                        0139 PHI 13
                        0140 LBZ SETTIM
                        0141 LBR EXIT
                        0142 INHOPP: LDI OPADII PLO XPEG
                        0143 LDX ANI#10
                        0144 BNZ ONE        .. X = 0C25
                        0145 LDI#10 OR ITXD    .. ITO OTHER PROCESSOR DEAD
                        0146 LDI#03 OR ITXD  .. SET INH ON TRUE LOC
                        0147 LDI#26 PLO XPEG
                        0148 LDXA PHI P6
                        0149 LDX PLO P6
                        0200 LDI#1D PLO XPEG
                        0201 LDI#31 ITXD       .. ITO EPROP CODE 31
                        0202 GHI P6 ITXD       .. ON LOC #0C1D
                        0203 GLO P6 ITXD       .. ' TIME
                        0204 ONE: LDI#23 PLO XPEG
                        0205 LDI#08 OR ITP XPEG
                        0206 LBR SETTIM
                        0207 POWFLT: LDI OPADII PLO XPEG
                        0208 LDX ANI#10
                        0209 BNZ TWO        .. X = 0C25
                        0210 LDI#10 OR ITXD    .. ITO OTHER PROCESSOR DEAD
                        0211 LDI#03 OR ITXD  .. SET INH ON TRUE LOC
                        0212 LDI#26 PLO XPEG
                        0213 LDXA PHI P6
                        0214 LDX PLO P6
                        0215 LDI#1D PLO XPEG
                        0216 LDI#32 ITXD       .. ITO EPROP CODE 32
                        0217 GHI P6 ITXD       .. ON LOC #0C1D
                        0218 GLO P6 ITXD       .. ' TIME
                        0219 TWO: LDI#23 PLO XPEG
                        0220 LDI#08 OR ITP XPEG
                        0221 LDI#2A PLO XPEG
                        0222 LBR IIXCHK
                        0223 IIXFLT: LDI OPADII PLO XPEG NOP
                        0224 LDX ANI#10
                        0225 BNZ THREE      .. X = 0C25
                        0226 LDI#10 OR ITXD    .. ITO OTHER PROCESSOR DEAD
                        0227 LDI#03 OR ITXD  .. SET INH ON TRUE LOC
                        0228 LDI#26 PLO XPEG
                        0229 LDXA PHI P6
                        0230 LDX PLO P6
                        0231 LDI#1D PLO XPEG
                        0232 LDI#33 ITXD       .. ITO EPROP CODE 33
                        0233 GHI P6 ITXD       .. ON LOC #0C1D
                        0234 GLO P6 ITXD       .. ' TIME
                        0235 THREE: LDI#23 PLO XPEG
                        0236 LDI#08 OR ITP XPEG
                        0237 LDI#2A PLO XPEG
                        0238 LBR FIFCHK
                        0239
                        0240 END
```

```
1
1M
0000 :                  0001 ..•••••••DMA PROGRAMME•••••••
0000 :                  0002 ..TRANSMIT TWO 8 BIT NUMBERS TO THE
0000 :                  0003    .. OPP PROCESSOR SERIALLY
0000 :                  0004    .. NOTE DATA ON LOCATION 0022
0000 :                  0005    .. THE PARITY STATUS DATA IS TRANSMITTED FIRST
0000 :                  0006    .. THEN THE DATA FROM LOCATION 0020
0000 :                  0007    .. IS COPYIED ON TO LOC 0022 AND  DATA
0000 :                  0008    .. WILL BE TRANSMITTED.
0000 :                  0009    .. EACH BIT WILL BE TRANSMITTED TWICE
0000 :                  0010
0000 :                  0011 .. FINALLY Q IS RESET TO INDICATE
0000 :                  0012 .. THE END OF DMA ACTIVITY.
0000 :                  0013 EXIT=0D600
0000 :                  0014 ORG0050
0050 C3D6001            0015 LBRD EXIT
0053 EA1                0016 SEX PA
0054 F823BB1            0017 LDI#23 PLO PB
0057 3AFA011            0018 BNF PA ANI#01
005A 32EE1              0019 BZ REPEAT
005C 3A1                0020 BDF SHI P6
005D FAFEB61            0021 ANI#FE PHI P6      .. RESET DMA PORT COUNTER
0060 0D1                0022 LDN PA
0061 FAFE731            0023 ANI#FE STXD
0064 7AFA011            0024 LDI#A ANI#01       .. RESET DMA BIT ON Q IF APPROP
0067 F1731              0025 OR STR PB          .. MEM LOCATION
006A 6A41               0026 REPT1 OUT 4        .. O P DATA TO PORT
006C 411                0027 OUT 1              .. TOGGLE DMA LINE
006E 3A1                0028 BDF PA
0070 7A1                0029 REQ PA
0071 3A0D0001           0030 LBNF EXIT
0075 0AFH101            0031 RETH1: GHI PA ANI #10
0078 3AF41              0032 BNZ OUT
007A F811PA1            0033 LDI#11 PHI P6      .. P6 = 110F
007D F810BA1            0034 LDI#10 PLO P6
0080 F820BA1            0035 LDI#20 PLO PB
0083 73A01              0036 LDXA IPX           .. COPY M TO T LOC
0085 B31                0037 STR PB
0086 C30A0001           0038 LBR EXIT
008A F801BA1            0039 OUT1 LDI#01 PHI P6
008D F810BA1            0040 LDI#10 PLO PA
0090 3A0D0A001          0041 BEQ LBR EXIT
0094 3AF801BA1          0042 REPEAT1 GHI PA OPI#01 PHI PA
0097 23001              0043 DEC PB LDN PB
0099 FA331              0044 SHR STR PB
009C 301                0045 IDL
009E 3A0131             0046 PB MRET
00A1 1                  0047 END
0000

: F.W.L.IIm
```

```
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 FL LOC  COSMAC CODE      LNNO SOURCE LINE
    0000                     1  ..TEMPORARY SETTING OF SYMBOLIC NAMES
    0000                     2    ..DECIMAL VALUES FOR RESET VALUES
    0000                     3     ..OR ERROR CODE NOS
    0000                     4    ..HEX VALUES ABSOLUTE ADDRESSES
    0000                     5      ..ABOVE #0C
    0000                     6    ..UNPACK
    0000                     7    NYVAL2=#DF
    0000                     8    NYVAL3=NYVAL2+4 ..TO 4TH DMA LOCN
    0000                     9    NYVAL4=47
    0000                    10      ..DECIMAL VALUE USED TO RESET
    0000                    11      ..16 SEC (INTERRUPT) COUNTER
    0000                    12    NYERR1=40 ..THIS SIDE
    0000                    13     ..BEING INHIBITED
    0000                    14    NYERR2=50 ..ADJACENCY BYTES
    0000                    15     ..CHECK ERROR
    0000                    16    NYCONF=RF
    0000                    17    NYDEPK=RF
    0000                    18    NYSCR=RA
    0000                    19    NYSTA1=RB
    0000                    20    NYCTR=RE
    0000                    21    NYMAIN=R7 ..MAIN PROGRAM COUNTER
    0000                    22    ..RENEW
    0000                    23    NYVAL5=#CA ...NOT.H'.AND..NOT.H
    0000                    24    NYVAL6=#CD ..X'
    0000                    25    NYVAL7=NYVAL6+1 ..Y'
    0000                    26    NYVAL8=#C7 ..OLD H
    0000                    27    NYVAL9=#D5 ...NOT.H PROCESSED
    0000                    28    NYVALA=#D3 ..F
    0000                    29    NYH=RF
    0000                    30    NYSUB=R9 ..SUBROUTINES' COUNTER
    0000                    31    NYADJ=RE
    0000                    32    ..FSET
    0000                    33    NYVALB=#C4 ..OLD W
    0000                    34    NYVALC=#CF ..W
    0000                    35    NYVALD=#CC ..W'
    0000                    36    NYVALF=#D4 ..H.AND..NOT.H'
    0000                    37    NYVALG=#C2 ..OLD F.AND.F'
    0000                    38    NYVALJ=#DB ..ADJ1
    0000                    39    NYW=RF ..NYW,NYH,NYDEPK,NYCONF
    0000                    40     ..ARE SAME REGR
    0000                    41    ..ADJSET
    0000                    42    NYVAL1=#B9 ..TOP SCRATCH LOCN
    0000                    43     ..LOCNS #0CB8,#0CB9 ARE SCRATCH
    0000                P   44    ..USED TO MATCH WITH INTERRUPT ROUTINE
    0000                    45    NYVAL=#0C ..UPPER BYTE OF ALL
    0000                    46     ..RAM LOCNS
    0000                    47    NYVAL0=#D7 ..LOCN OF CONFIG
    0000                    48    NYVALK=#25 ..#0C25 LOCN OF INTERNAL
    0000                    49     ..FLAGS INFO
```

AS 12/07/79

```
0000                    50    NYVALN=#2A ..#0C2A IS ROM CHECK TIMER,
0000                    51     ..#0C29 IS 16 SEC(I/R) TIMER
0000                    52    NYVALP=64 ..DECIMAL ROM CHECK RESET VAL
0000                    53    NYVALQ=#42 ..ONES COUNT
0000                    54    NYVALR=#40 ..FOURS COUNT
0000                    55    NYVALS=#26 ..MAIN TIMER (1 OF 2 BYTES)
0000                    56    NYVALT=#20 ..W/H DATA (TO DMA)
0000                    57    NYVALU=#23 ..O/P BYTE
0000                    58    NYVALW=#B5 ..LATCHED ERROR INFO
0000                    59    NYVALX=NYVAL0-1 ...NOT.H' PROCESSED
0000                    60    NYVALY=#BC ..#OF FIRES LOCN
0000                    61    NYVALZ=NYVALG-3
0000                    62    HVALA=#C4..W COUNT HI
0000                    63    HVALB=#54..COUNT STACK LEVEL 4
0000                    64    HVALD=#65..LEVEL 5 STORE
0000                    65    HVALE=#55..COUNT STACK LEVEL 5
0000$                   66    HVALF=#55
0000                    67    HVALG=HVALD-16..END OF STORES
0205                    68    ORG #205
0205                    69   ..****************************************
0205                    70   ..****************************************
0205                    71    ..UNPACK ROUTINE, PART OF FIRE ROUTINE
0205 F825AB             72    NYVALK->NYSTA1.0
0208                    73     ..POINTS TO INTERNAL FLAGS
0208 0BFA10             74    @NYSTA1.AND.B'00010000'
020B                    75     ..OTHER PROCESSOR STATUS
F   020B 3A00           76    IF &>0 GO TO NYOFF1
020D                    77     ..SHORT BRANCH TO W',X',.NOT.H'
020D                    78      ..SETTING ROUTINE
020D 80FBFF             79     R0.0 .XOR. #FF  ..ZERO FF CORRECT # 0B
F   0210 3200           80     IF=0 GO TO PS1
0212                    81    ....IF NO DATA RECD.,2CASES
0212                    82    ...EF=1,WE ARE INHIBITED
0212                    83    ...EF=0,WE MUST INHBT OTHER PROCSSR
F   0212 3C00           84     IF NEF1 GO TO NYOFF1
0214                    85     ...HERE WE ARE INHBTD
0214                    86     ...FATAL FAULT FOR THIS SIDE
0214                    87     ...BRANCH TO LATCFL
0214                    88     ...WITH ERROR CODE IN D REG
F   0214 F828C00000     89     NYERR1)LBR LACHFL
0219 F8DFA0             90    PS1:NYVAL2->R0.0
021C                    91      ...RESETS DMA PTR.
021C F8DFAF             92     NYVAL2->NYDEPK.0
021F                    93     ...POINTS AT LO BIT OF DMA DATA
021F FF                 94     SEX NYDEPK
0220 72F3FA04           95     @1.XOR.@.AND.#04
0224                    96     ...RESULT >0 IF 2 PORTS
0224                    97    ....CHECK BIT OK & DMA CRECT
F   0224 3A00           98     IF>0GO TO PS2
F   0226 F829C00000     99    #29)LBR LACHFL
```

A5 12/07/79

```
    022E 2F                    100    PS2:DEC NYDEPK
 FF 022C 72763300 72763300     101    @!/2';BDF NYOFF1;@!/2';BDF NYOFF1
 FF 0234 72763B00 72763B00     102    @!/2';BNF NYOFF1;@!/2';BNF NYOFF1
    023C                       103    ...CHECKS FOR 0011 ON LOW
    023C                       104    ...4 DMA REGS(LO BITS)
    023C F8DFAF                105    NYVAL2->NYDEPK.0
    023F F8B9AA                106    NYVAL1->NYSCR.0
    0242 72FAFA5A              107    @!.AND.B'11111010'->@NYSCR
    0246 F0FAFA                108     @.AND.B'11111010'..CLR OFF X BIT DATA
    0249 EAF3                  109    SEX NYSCR;.XOR.@
    024B                       110    ...RESULT 0 IF L=R CONFIG
 F  024B 3200                  111    IF =0 GO TO PS3
 F  024D F830C00000            112    #30;LBR LACHFL
    0252 0AFAF8FB88            113    PS3:@NYSCR.AND.#F8.XOR.B'10001000'
    0257                       114    ...CHECK FOR 4TH ORDER ADJ CASE
    0257                       115    ...ZERO IF SAME
 F  0257 3A00                  116    IF>0 GO TO PS4
    0259 F8FC5A                117    B'11111100'->@NYSCR
    025C F8D7AF                118   PS4:NYVAL0->NYDEPK.0
    025F 0AFAFC5F              119     @NYSCR.AND.#FC->@NYDEPK
    0263                       120    ...CONFIG TO LOCN
    0263 F8DFAF                121    NYVAL2->NYDEPK.0
    0266                       122   ..NOW UNPACK 1ST STATUS BYTE
    0266                       123   ......
    0266                       124    ..N.B. NYDEPK.0 HAS MAX VAL OF FF
    0266 F808AE                125    #08->NYCTR.0
    0269 1F4F76                126  NYDKL1:INC NYDEPK;@NYDEPK!/2'
    026C                       127         ..LOADS BIT INTO DF
    026C F0765A2E              128    @/2'->@NYSCR;DEC NYCTR
    0270                       129     ..TRANSFERS BIT J 'TO SCRATCH BYTE
    0270 8E                    130    NYCTR.0
    0271 3A69                  131    IF >0 GO TO NYDKL1
    0273                       132    ..NB**UNPACKED STATUS LEFT
    0273                       133     ..IN SCRATCH LOCN
    0273                       134    ..
    0273                       135    ..NOW UNPACK H'/W' DATA IN SAME WAY
    0273 2A                    136    DEC NYSCR ..POINTS TO 2ND SCRATCH LOCN
    0274 F808AE                137    #08->NYCTR.0
    0277 1F4F76                138  NYDKL2:INC NYDEPK;@NYDEPK!/2'
    027A F0765A2E              139    @/2'->@NYSCR;DEC NYCTR
    027E 8E                    140    NYCTR.0
    027F 3A77                  141    IF >0 GO TO NYDKL2
    0281                       142    ..N.B. NYDEPK.0 HAS MAX VALUE OF #FF
    0281                       143    ..**
    0281                       144    ..**
    0281                       145    ..THIS COMPLETES UNPACK ROUTINE
    0281                       146    ..WILL CONTINUE IN FIRE ROUTINE
    0281                       147    ..NB STATUS,W'/H' INFO LEFT
    0281                       148     ..IN SCRATCH
    0281                       149  ..*****************************************
```

AS 12/07/79

```
     0281                    150  ..*****************************************
     0281                    151  ..*****************************************
     0281                    152  ..*****************************************
     0281                    153    ..RENEW ROUTINE,PART OF FIRE ROUTINE
     0281                    154     ..FOLLOWS UNPACK ROUTINE
     0281                    155     ..AUTHOR THIS SECTION..NIGEL YOUNG
     0281 F82AAB             156    NYVALN->NYSTA1.0
     0284                    157     ..POINTS AT ROM CHECK TIMER
     0284 1A      !          158    INC NYSCR ..TO POINT AT DMA'D OVER
     0285                    159      ..STATUS BYTE
     0285 0AFA08             160    @NYSCR.AND.B'00001000'
     0288                    161     ..1 IF ROM CHECK COMPLETED
     0288 CEF840             162    LSZ ;NYVALP
     028B                    163     ..VALUE MUST NOT BE 0
     028B CE5B5B             164    LSZ;->@NYSTA1;->@NYSTA1
     028E                    165     ..2ND INSTRUCTION IS DUMMY FILLER
     028E 0AFA04             166    @NYSCR.AND.B'00000100'
     0291                    167     ..0 FOR W', 1 FOR H'
     0291 2A                 168    DEC NYSCR ..TO POINT AT W'/H' BYTE
F    0292 3200               169    IF =0 GO TO NYOFF4
     0294                    170  ..*****************************************
     0294                    171    ..*
     0294                    172    ..*
     0294                    173    ..H' PROCESSING
     0294 2B                 174    DEC NYSTA1
     0295                    175     ..POINTS AT 16 SEC (INTERRUPT) TIMER
     0295 F82F5B             176    NYVAL4->@NYSTA1 ..RESETS
     0298 F8D6AF             177    NYVALX->NYH.0 ..POINTS
     029B                    178     ..AT .NOT.H' LOCATION
@    029B EA                 179    SEX NYSCR
 F   029C F800A9             180    A.0(ADJPR)->NYSUB.0
 F   029F F800B9             181    A.1(ADJPR)->NYSUB.1
     02A2 D9                 182    SEP NYSUB ..CALLS ADJPR,RESULT LEFT IN
     02A3                    183     ..D REGR, NYADJ POINTS TO .NOT.DONTWOR
     02A3 EE                 184    SEX NYADJ
     02A4 FBFFF2EF73         185    .XOR.#FF.AND.0->0-'NYH
     02A9                    186     ..NYH NOW X REGR
     02A9                    187     ..POINTS AT .NOT.H
 F   02A9 F800A9             188      .0(HEADS)->NYSUB.0
 F   02AC F800B9             189       1(HEADS)->NYSUB.1
     02AF D9                 190         NYSUB ..CALLS SUBROUTINE HEADS
     02B0                    191        HEAD FAULT ISSUING SUBROUTINE
 F   02B0 C00000             192    LBR NYOFF5
     02B3                    193  ..*****************************************
     02B3                    194    ..*
     02B3                    195    ..*
     02B3                    196  NYOFF4: ..W' STORAGE
     02B3 F8CDAF             197    NYVAL6->NYH.0
     02B6 EF                 198    SEX NYH
     02B7 72732F             199    0!->0-;DEC NYH  ..X'->Y'
```

AS 12/07/79

```
     02BA 7273              200    @!->@-            ..W'->X'
     02BC 0A5F              201    @NYSCR->@NYH      ..STORE W'
F    02BE C00000            202    LBR NYOFF5
     02C1                   203  ..*****************************************
     02C1                   204    ..*
     02C1                   205    ..*
     02C1                   206  NYOFF1:
     02C1                   207    ..DEFAULT PROCESSING SETS W',X',Y'=#00,
     02C1                   208     ...NOT.H'=#FF,RAISES INHIBIT LINE, SO
     02C1                   209     ..NO MORE DMA DATA SENT
     02C1                   210    ..SET OTHER PROCESSOR TO DEAD
     02C1                   211     ..ON INTERNAL FLAGS. RAISE
@    02C1                   212     ..INHIBIT BIT ON TRU AND O/P
     02C1                   213     ..RAM LOCATION
     02C1 F82SAB            214    NYVALK->NYSTA1.0 ..INTERNAL FLAGS
     02C4 0BF9105B          215    @NYSTA1.OR.B'00010000'->@NYSTA1
     02C8 2B                216    DEC NYSTA1 ..TRU STATUS
     02C9 0BF9085B          217    @NYSTA1.OR.B'00001000'->@NYSTA1
     02CD 2B                218    DEC NYSTA1 ..O/P BYTE
     02CE 0BF9085B      @   219    @NYSTA1.OR.B'00001000'->@NYSTA1
     02D2 E7                220     SEX NYMAIN
     02D3 F8DFA0            221     NYVAL2->R0.0
     02D6 AF                222     PLO NYH
     02D7 6200C4C4          223     OUT 2,#00;NOP;NOP
     02DB 6200C4C4          224     OUT 2,#00;NOP;NOP
     02EF                   225    ...O/P TO GET A/C CONFIG
     02DF                   226     ...NOP S  FOR DELAYS
     02DF EF                227     SEX NYH
     02E0 72F3FA04          228    @!.XOR.@.AND.#04
     02E4                   229     ..RESULT NON ZERO IF
     02E4                   230    ..PORT CHECK BITS OK
F    02E4 3A00              231     IF>0 GO TO PS5
F    02E6 F8F9C00000        232    #F9;LBR LACHFL
     02EB 2F                233    PS5:DEC NYH
     02EC F8B9AA            234     NYVAL1->NYSCR.0
     02EF 72FAFA5A          235     @!.AND.B'11111010'->@NYSCR
     02F3 F0FAFA            236     @.AND.B'11111010'...CLEARS OFF
     02F6                   237     ...XBIT,DATA
     02F6 EAF3              238     SEX NYSCR;.XOR.@
     02F8                   239     ..RESULT NON ZERO IF L=R CONFIG
F    02F8 3200  $           240     IF=0 GO TO PS6
F    02FA F830C00000        241    #30;LBR LACHFL
     02FF 0AFAF8FB88        242   PS6:@NYSCR.AND.#F8.XOR.B'10001000'
     0304                   243     ..CHECK FOR 4THORDER ADJ CASE
     0304                   244     ..ZEROOIF SAME
F    0304 3A00              245     IF>0 GO TO PS7
     0306 F8FC5A            246     B'11111100'->@NYSCR
     0309 F8D7AF            247    PS7:NYVAL0->NYH.0
     030C 0AFAFC5F          248     @NYSCR.AND.#FC->@NYH..CONF TO LOCN
     0310 F8CEAFEF          249    NYVAL7->NYH.0;SEX NYH
```

A5 12/07/79

```
     0314 F800737373          250    #00->0-,0-,0-
     0319 F8D6AF              251    NYVALX->NYH.0 ...N0T.H' PROCESSED
     031C F8FF73              252    #FF->0- ..NOW POINTS AT .NOT.H
F    031F F800A9              253    A.0(HEADS)->NYSUB.0
F    0322 F800B9              254    A.1(HEADS)->NYSUB.1
     0325 D9                  255    SEP NYSUB  ..CALLS SUBROUTINE HEADS
     0326                     256     ..HEAD FAULT ISSUING SUBROUTINE
     0326                     257  ..*****************************************
     0326                     258  ..**
     0326                     259  ..COMPLETES H',W' PROCESSING/STORING
     0326                     260  ..*
     0326                     261  ..*****************************************
     0326                     262  NYOFF5: ..H PROCESSING OR W STORING
     0326 F825AB              263    NYVALK->NYSTA1.0 ..INTERNAL FLAGS
     0329 0BFA04AF            264    @NYSTA1.AND.B'00000100'->NYH.0
     032D                     265     ..EXTRACT 0 FOR W, 1 FOR H
     032D                     266     ..TEMPORARILY PUSH INTO Y/I
     032D 0EFAFB5B            267    @NYSTA1.AND.B'11111011'->@NYSTA1
     0331                     268     ..RESET
     0331                     269  ..!!!!!MUST RECHECK RESET USING
     0331                     270  ..LACHFL ROUTINE
     0331 F840AB              271    NYVALR->NYSTA1.0 ..FOURS COUNT
     0334 8F                  272    NYH.0 ..W OR H ?
F    0335 C20000              273    LBZ NYOFF7 ..LONG BRANCH IF 0
     0338                     274  ..*****************************************
     0338                     275    ..*
     0338                     276    ..*
     0338                     277    ..H PROCESSING
     0338                     278    ..FLAG ALREADY RESET
     0338 F8C7AF              279    NYVAL8->NYH.0 ..POINTS TO OLD H
     033B EF                  280    SEX NYH
     033C 0BFBFF              281    @NYSTA1.XOR.#FF  ..NEW .NOT.H
     033F F2                  282    .AND.@   ...NEW.NOT.H.AND.OLD H
F    0340 3200                283    IF=0 GO TO NYOFF8
     0342 0BF273              284    @NYSTA1.AND.@->@-
     0345 F826AA              285    NYVAL5->NYSCR.0 ..TO BYTE OF MAIN TIMER
     0348 4A730A73            286    @NYSCR!->@-;@NYSCR->@-
     034C                     287     ..RENEWS H, TIME
     034C                     288                        ..!!!!!!!!!!!!
     034C                     289  NYOFF8: ..PUT INTO DMA LOCATION
     034C F820AA              290    NYVALT->NYSCR.0 ..STORE W/H FOR DMA
     034F 0B5A                291    @NYSTA1->@NYSCR ..FOURS COUNT
     0351 F8D5AF              292    NYVAL9->NYH.0
     0354                     293     ..TO HOLD PROCESSED .NOT.H
*    0354 F8B9AA              294    NYVAL1->NYSCR.0 ..SCRATCH LOCN
     0357 0B5A                295    @NYSTA1->@NYSCR ..UNPROCESSED H
     0359 EA                  296    SEX NYSCR
*F   035A F800A9              297    A.0(ADJPR)->NYSUB.0
F    035D F800B9              298    A.1(ADJPR)->NYSUB.1
     0360 D9                  299    SEP NYSUB  ..CALLS ADJPR,RESULT LEFT
```

AS 12/07/79

```
     0361                          ..IN D REGR, NYADJ POINTS TO
     0361                          .. .NOT.DONTWORRY BYTE
     0361 EE                       SEX NYADJ
     0362 FBFFF25F                 .XOR.#FF.AND.0->0NYH
     0366 EF                       SEX NYH ..POINTS AT .NOT.H
F    0367 F800A9                   A.0(HEADS)->NYSUB.0
F    036A F800B9                   A.1(HEADS)->NYSUB.1
     036D D9                       SEP NYSUB ..CALLS SUBROUTINE HEADS,
     036E                          ..HEAD FAULT ISSUING SUBROUTINE
F    036E F800A9                   A.0(ADJSET)->NYSUB.0
F    0371 F800B9                   A.1(ADJSET)->NYSUB.1
     0374 D9                       SEP NYSUB ..CALLS ADJACENCY BYTES
     0375                          ..RESETTING PROGRAM; D REGR CONTAINS
     0375                          ..VALUE, NYADJ POINTS AT OLD VALUE OF
     0375                          ..SUM CHECK BYTE
     0375 EE                       SEX NYADJ
     0376 F3                       .XOR.0 ..SHOULD BE ZERO
F    0377 3200                     IF =0 GO TO NYOFF9
     0379                          ..OTHERWISE FATAL ERROR FOR
     0379                          ..THIS SIDE. BRANCH TO FAULT
     0379                          ..LATCHING SECTION WITH ERROR
     0379                          ..CODE NO IN D REGR
F    0379 F832C00000               NYERR2;LBR LACHFL
     037E                     ..*****************************************
     037E                          ..*
     037E                          ..*
     037E                          ..W STORAGE
     037E                     NYOFF7: ..NYSTA1 POINTS AT FOURS COUNT
     037E F8D3AF                   NYVALA->NYH.0 ..POINTS AT F
     0381 F820AA                   NYVALT->NYSCR.0 ..STORE LOCN
     0384                          ..FOR DMA ACROSS
     0384 FB60                     SEX NYSTA1;IRX ..POINTS AT TWOS
     0386 0FF2                     0NYH.AND.0(TWOS)
     0388 2B                       DEC NYSTA1
     0389 F15A                     .OR.0(FOURS)->0NYSCR
     038B                          ..STORES FOR DMA
     038B 2F2FEF                   DEC NYH;DEC NYH;SEX NYH ..POINTS AT Y
     038E 72732F                   0!->0-;DEC NYH ..Y->Z
0    0391 72732F                   0!->0-;DEC NYH ..X->Y
     0394 7273                     0!->0-         ..W->X
     0396 0A5F                     0NYSCR->0NYH
     0398                     ..*****************************************
     0398                     ..*
     0398                     ..*
     0398                     NYOFF9: ..REJOIN
     0398 7B                       SEQ ..SETTING Q ALLOWS DMA OUT
     0399                          ..TO OTHER SIDE
     0399                          ..NB NYSCR NOT RESET HERE
     0399                          ..**
     0399                          ..**
```

```
A5          12/07/79

    0399                        350    ..THIS COMPLETES RENEW ROUTINE, NOW
    0399                        351     ..ENTER FSET, FINAL PART OF FIRE ROUT
    0399                        352  ..*****************************************
    0399                        353  ..*****************************************
    0399                        354  ..*******************"*********************
    0399                        355  ..*****************************************
    0399                        356    ..FSET ROUTINE, LAST PART OF FIRE ROUT
    0399                        357     ..FOLLOWS RENEW ROUTINE
    0399                        358     ..AUTHOR THIS SECTION..NIGEL YOUNG
    0399 F8C4AEEE               359    NYVALB->NYADJ.0;SEX NYADJ
    039D                        360     ..POINTS TO LOCN OF LOGGED NONZERO W
    039D F825AF                 361    NYVALK->NYW.0
    03A0 0FFA80                 362    @NYW.AND.B'10000000'
N   03A3 CA0000                 363    LBNZ NYOFFA
    03A6                        364   ......W,X,Y,Z,W',X',Y'L LOGGING
    03A6 F8CFAF                 365       NYVALC->NYW.0
@   03A9 0F                     366       @NYW
F   03AA 3200                   367       IF=0 GO TO HB
    03AC F8C4AA                 368       HVALA->NYSCR.0
    03AF EA                     369     SEX NYSCR
F   03B0 F0FBFFC20000           370     @.XOR.#FF;LBZ HA
    03B6 2A                     371     DEC NYSCR
    03B7 72AEF0BE               372     @!->NYADJ.0;@->NYADJ.1 ..W COUNT->REG
    03BB F808AB                 373       #8->NYSTA1.0
    03BE 0F765F                 374     HST:@NYW/2'->@NYW  ..LSB TO DF
    03C1 C7                     375       LSNF ..IF 0 DONT INC
    03C2 1E0F                   376       INC NYADJ;@NYW.. COUNT 1 IF NOT 0
    03C4 2B                     377       DEC NYSTA1
    03C5 8B                     378       NYSTA1.0
    03C6 3ABE                   379       IF>0 GO@TO HST..  TOTAL OF 8 TIMES
    03C8 0F765F                 380       @NYW/2'-@NYW.. RESTORE W
    03CB 9E5A                   381       NYADJ.1->@NYSCR..REPLACE W COUNT HI
    03CD 2A                     382      DEC NYSCR..LEFT AT FIRST W COUNT
    03CE 8E5A                   383       NYADJ.0->@NYSCR..REPLACE W COUNT LO
    03D0 F80CBE                 384     HA:NYVAL->NYADJ.1 ...RESET U/BYTE TO 0
    03D3                        385   ........................
    03D3 F855AA                 386     HB:HVALF->NYSCR.0
    03D6 EA                     387       SEX NYSCR
    03D7 F80073737373730        388       #00->@-,@-,@-,@-,@-
    03DE F8FF73                 389       #FF->@-.. STACIHBSET
F   03F1 F800AF                 390       A.0(ADUP)->NYSTA1.0
F   03E4 F800BB                 391       A.1(ADUP)->NYSTA1.1..SET TO ADUP SU
    03E7 F8CCAE                 392       NYVALD->NYADJ.0..W'@LOCN.
    03EA DB                     393       SEP NYSTA1..GO TO ADUP SUB.
    03EB 1F                     394       INC NYADJ.. X'
    03EC DB                     395       SEP NYSTA1..GOSUB
    03ED 1F                     396       INC NYADJ..Y'
    03EE DB                     397       SEP NYSTA1
    03EF 1E1E                   398       INC NYADJ;INC NYADJ.... X
    03F1 DB                     399       SEP NYSTA1
```

A5 12/07/79

```
     03F2 1E
     03F3 DB
     03F4 F8CFAF
     03F7 F865FC01AF
     03FC 0F
     03FD 1F1F1F
     0400 EF
     0401 F15E
     0403 DB
F    0404 3000
     0406
     0406 D7
     0407 F854AA
     040A EA
     040B 0EF2
     040D 60
     040E F1732A
     0411 0EF2
     0413 60
     0414 F1732A
     0417 0EF2
     0419 60
     041A F1732A
     041D 0EF2
     041F 60
     0420 F173
     0422 0EF173
     0425 60
     0426 3006
     0428
     0428 F826AE
     042B F80CBB
     042E F855AA
     0431 F865AB
     0434 0A2A
F    0436 3200
     0438 EB73
     043A 4E730E732F
F    043E F0FBFF3200
     0444 F0FC015B
     0448 8BFC03AB
     044C 8BFF04AB
     0450 8BFF55
     0453 CE
     0454 3034
     0456
     0456
@    0456
     0456 F8CCAF
     0459
```

```
400          INC NYADJ.. Y
401          SEP NYSTA1
402          NYVALC->NYW.0..W LOCN.
403          HVALD+1->NYADJ.0 ..W.OR.Z (SCRATCH)
404          @NYW    .. W
405          INC NYW;ING NYW;INC NYW ...Z
406          SEX NYW
407          .OR.@->@NYADJ ...W.OR.Z
408          SEP NYSTA1
409          GO TO ADEND
410     .........SUBROUTINE ADUP
411          SEP NYMAIN
412       ADUP:HVALE->NYSCR.0
413          SEX NYSCR
414          @NYADJ.AND.@ ...NEW 5 COUNT
415          IRX   ... 5 LOCN.
416          .OR.@->@-;DEC NYSCR ...STORE & MOVE@
417@         @NYADJ.AND.@   ...NEW 4 COUNT
418@         IRX
419          .OR.@->@-;DEC NYSCR
420          @NYADJ.AND.@   ...NEW 3 COUNT
421          IRX
422          .OR.@->@-;DEC NYSCR
423          @NYADJ.AND.@   ...NEW 2 COUNT
424          IRX
425          .OR.@->@-
426          @NYADJ.OR.@->@-
427          IRX
428          GO TO ADUP-1
429     ............END OF ADUP
430       ADEND:NYVALS->NYADJ.0   ...MAIN TIMER @
431          NYVAL->NYSTA1.1   ...RESET U/BYTE TO@
432          HVALE->NYSCR.0   ... 5 COUNT
433       FIVES:HVALD->NYSTA1.0
434       HC:@NYSCR;DECNYSCR
435          IF=0 GO TO FOURS
436          ->@-'NYSTA1
437          @NYADJ!->@-;@NYADJ->@-;DEC NYADJ
438          @.XOR.#FF;IF=0 GO TO HD
439        @+1->@NYSTA1
440        HD:NYSTA1.0+3->NYSTA1.0
441       FOURS:NYSTA1.0-4->NYSTA1.0
442          NYSTA1.0-HVALG
443          LSZ
444          GO TO HC
445          ........END OF LOGGING
446       ..**
447       ..**
448     NYOFFA:NYVALD->NYW.0
449          ..POINTS TO W'
```

A5 12/07/79

```
                0459 EF              450     SEX NYW
                045A F8B9AA          451     NYVAL1->NYSCR.0 ..SCRATCH LOCN
                045D 72F1            452     @!.OR.@  ..W'.OR.X'
                045F 6060            453     IRX;IRX
                0461 F160            454     .OR.@(W);IRX
                0463 F1              455     .OR.@(X)
                0464 606060          456     IRX;IRX;IRX
                0467 F25A            457     .AND.@(F)->@NYSCR
                0469                 458      ..RESET CONDITION BYTE IN DUMMY LOCN
                0469                 459     ..**
                0469                 460     ..**
                0469                 461     ..NOW CALCULATE F
                0469 2F              462     DEC NYW ..POINTS AT Z
                046A F02F2F2F        463     @(Z);DEC NYW;DEC NYW;DEC NYW
                046E F160            464     .OR.@(W);IRX
                0470 F260            465     .AND.@(X);IRX
                0472 F2EAF1          466     .AND.@(Y).OR.@'NYSCR
                0475 2A5A            467     DEC NYSCR;->@NYSCR
              F 0477 F800A9          468     A.0(ADJPR)->NYSUB.0
              F 047A F800B9          469     A.1(ADJPR)->NYSUB.1
                047D D9              470     SEP NYSUB ..CALLS ADJPR
                047E                 471      ..RESULT LEFT AT SCRATCH LOCN
                047E                 472      ..NYADJ POINTS TO .NOT.DONTWORRY
                047E 0EF25A          473     @NYADJ.AND.@(F)->@NYSCR
                0481                 474      ..DONTWORRY PROCESSING
                0481 F8D5AF          475     NYVAL9->NYW.0
                0484                 476      ..POINTS AT .NOT.H
                0484 0FF15A          477     @NYW.OR.@(F)->@NYSCR
                0487                 478      ..F SAVED IN SCRATCH LOCN
                0487                 479     ..**
                0487                 480     ..**
                0487                 481     ..NOW CALCULATE F'
                0487 1A              482     INC NYSCR ..TO POINT AT RESET BYTE
                0488 F8CCAF          483     NYVALD->NYW.0 ..POINTS TO W'
                048B EF              484     SEX NYW
                048C 72F260          485     @!.AND.@;IRX ..W'.AND.X'
              @ 048F F2EAF15A        486     .AND.@(Y').OR.@'NYSCR->@NYSCR
              F 0493 F800A9          487     A.0(ADJPR)->NYSUB.0
              F 0496 F800B9          488     A.1(ADJPR)->NYSUB.1
                0499 D9              489     SEP NYSUB ..CALLS ADJPR
                049A                 490      ..RESULT LEFT AT SCRATCH LOCN
                049A                 491      ..NYADJ POINTS TO .NOT.DONTWORRY
                049A 0EF25A          492     @NYADJ.AND.@(F')->@NYSCR
                049D F8D4AF          493     NYVALF->NYW.0 ..POINTS TO
                04A0                 494       ..(H.AND.(.NOT.H'))
                04A0 0FF1            495     @NYW.OR.@(F')
                04A2 2A              496     DEC NYSCR ..POINTS AT F
                04A3 F25A            497     .AND.@(F'.AND.F)->@NYSCR
                04A5                 498      ..NYSCR POINTS TO FIRE CONDITION BYTE
                04A5                 499     ..**
```

AS 12/07/79

```
     04A5                          500     ..'*
     04A5 1A                       501     INC NYSCR
@    04A6 5A2A                     502     ->@NYSCR;DEC NYSCR
     04A8                          503      ..IF NO FIRE AUTOMATICALLY
     04A8                          504      ..CONTAINS #00 FOR RESET
     04A8 F825AF                   505       NYVALK->NYW.0
     04AB 0A                       506       @NYSCR
  F  04AC 3A00                     507       IF>0 GO TO POINT1
     04AE 0FFA7F5F                 508      @NYW.AND.B'01111111'->@NYW
     04B2                          509      ..RESET HEAD TEST FLAG
  F  04B2 3000                     510      GO@TO POINT4
     04B4 0FFA80                   511    POINT1:@NYW.AND.B'10000000'
  F (04B7 3A00                     512      IF >0 GO TO POINT3..DONT LOG
     04B9 F8C2AF                   513      NYVALG->NYW.0..OLD F&F' LOCN
     04BC F826AB                   514      NYVALS->NYSTA1.0..TIMER
     04BF 0F                       515      @NYW
  F  04C0 3200                     516      IF=0 GO TO LOG
     04C2 F8BFAF                   517      NYVALZ->NYW.0..2ND LOG LOCN
     04C5 0AEF73                   518    LOG:@NYSCR-@-'NYW
     04C8 4B730B73                 519      @NYSTA1!->@-;@NYSTA1->@-
     04CC F823AB                   520    POINT2:NYVALU->NYSTA1.0..O/P BYTE
     04CF 0BFA04                   521      @NYSTA1.AND.B'00000100'
  F  04D2 3A00                     522      IF >0 GO TO POINJ3
     04D4                          523      ..FIRE NOT ABOUT TO BE SET
     04D4 F8BCAB                   524      NYVALY->NYSTA1.0..# OF FIRES LOCN
     04D7 0BFFFF                   525      @NYSTA1-CFF
  F  04DA 3200                     526      IF =0 GO TO POINT3..REG. FULL
     04DC 0BFC015B                 527      @NYSTA1+#01->@NYSTA1..INCREMENT
     04E0 F8045A                   528    POINT3:B'00000100'->@NYSCR
     04E3 EA                       529@   POINT4:SEX NYSCR
     04E4 F823AB                   530     NYVALU->NYSTA1.0 ..O/P BYTE
     04E7 0BFAFBF15B               531     @NYSTA1.AND.B'11111011'.OR.@->@NYSTA1
     04EC                          532      ..SETS OR RESETS O/P FIRE CONDITION
     04EC E7                       533     SEX R7
     04ED 7177                     534     DIS,#77
     04EF EB64                     535     SEX NYSTA1;OUT 4
     04F1                          536       ..OUTPUTS
     04F1 EA                       537     SEX NYSCR
     04F2 0BFAFBF15B               538     @NYSTA1.AND.B'11111011'.OR.@->@NYSTA1
     04F7 E7                       539     SEX  R7
     04F8 7077EA                   540     RET,#77;SEX NYSCR
     04FB                          541      ..SAVES FIRE IN TRUE LOCNSALSO
     04FB                          542     ..**
     04FB                          543     ..**
     04FD                          544     ..NOW REVERSE ADJACENCY@PROCESSING
     04FB                          545     ..OF F; USE 3 REGR.'S@FOR CONVENIENCE
     04FE                          546     ..CAN USE JUST 2
     04FB 1A                       547     INC NYSCR
     04FC                          548     ..POINTS TO F.AND.F'@IN SCRATCH
     04FC F8D3AF                   549     NYVALA->NYW.0
```

```
     04FF                          550      ..POINTS TO SAVE LOCN OF0F
     04FF F8DBAE                   551     NYVALJ->NYADJ.0
     0502                          552      ..POINTS TO ADJ1
     0502                          553     ..REVERSE 1ST LEVEL ADJ PROCESSING
     0502 0AF6F6F6F6               554     0NYSCR/2/2/2/2
     0507 EEF2EAF15A               555     .AND.0'NYADJ.OR.0'NYSCR->0NYSCR
     050C                          5560    ..REVERSE 4TH LEVEL ADJ PROCESSING
     050C 2E                       5570    DEC NYADJ
     050D F6EEF2EAF15A             558     /2.AND.0'NYADJ.OR.0'NYSCR->0NYSCR
     0513                          559     ..REVERSE 3RD LEVEL ADJ PROCESSING
     0513 2E                       560     DEC NYADJ
     0514 F6EEF2EAF15A             561     #2.AND.0'NYADJ.OR.0'NYSCR->0NYSCR
     051A                          562     ..REVERSE 2ND LEVEL ADJ PROCESSING
     051A 2E                       563     DEC NYADJ
     051B F6EEF2EAF15F             564     /2.AND.0'NYADJ.OR.0'NYSCR->0NYW
     0521                          565      ..SAVES F FOR NEXT ENTRY TO FIRE ROUT0
     0521                          U66     ..NOW RESET FOURS,TWOS,ONES COUNT
     0521 F842AA                   567     NYVAL0->NYSCR.0 ..ONES0COUNT POINTER
     0524 F800737373               568     #00->0-,0-,0-
     0529                          569     ..END OF PROGRAM SECTION FSET
     0529                          570     ..WHICH COMPLETES FIRE ROUTINE
     0529                          571     ..****************************************
     0529                          572     ..****************************************
     0529                          573     ..ENDS FIRE ROUTINE
     0529                          574     ..*****************J***J*****************
     0529                          575     ..NOW CHECK DMA  RAM
     0529 EF                       5760     SEX RF
     052A F8FFAF                   577     LDI#FF;PLO0RF
     052D F8AA738F                 578     POINT:LDI#AA;STXD;GLO0RF
     0531 FFDE3A2D60               579      SMI#DE;BNZ POINT;IRX..TO POINTAT DF
F    0536 72FFAA3A00               580     REPT:LDXA;SMI#AA;BNZ WRONG
     053B 8F3A362F                 581      GLO0RF;BNZ REPT;DEC RF
     053F F855738F                 582     AGIN:LDI#55;STXD;GLO RF
     0543 FFDE3A3F60               583      SMICDE;BNZ AGIN;IRX
F    0548 72FF553A00               584     ROUND:LDXA;SMI#55;BNZ WRONG
F    054D 8F3A483000               5850     GLO0RF;BNZ ROUND;BR RIGHT
F    0552 F824C00000               586     WRONG:LDI#24;LBR LACHFL
     0557 F80CBFB0F8E2AF0          587P   RIGHT:LDI#0C;PHI RF;PHI R0;LDI#E2;PLO RF
     055E0F8007373                 588      LDI 0;STXD;STXD
     0562 F8FF7373                 589      LDI#FF;STXD;STXD
     05660                         590      ...SET 1ST 4 DMA LOCNS
     05660                         591     ..TO INDICATE FAILURE
     0566                          592      ..*******************J******J**********
     0566 F8DFA0                   5930     LDI#DF;PLO R0..RE-INITIALIZE DMA
     0569 F825AF0F                 594      LDI#25;PLO RF;LDN RF
     056D FAFE5F                   595      ANI#FE;STR RF
     0570 D3                       596     SEP R3
    00B00                          597     ORG #B00
     0B00                          598    ..****************************************
     0B00                          599      ..SUBROUTINE ADJSET,AUTHOR NIGEL YOUNG
```

```
AS          12/07/79

                                    ..CALLED BY INITIALIZATION
                                    ..AND 15 SEC  H SETTING ROUTINES
                                ADJSET:
0B00 F8D7AFAF                     NYVAL0->NYCONF.0,NYADJ.0
0B04                                ..CONFIG BYTE
0B04                              ..USE NYADJ TO POINT TO
0B04                                ..ADJACENCY BYTES
0B04                              ..NB UPPER BYTE OF REGRS
0B04                                ..MUST BE #0C
0B04 F8B9AA                       NYVAL1-NYSCR.0 ..SCRATCH
0B07                                ..PUT LOCATION INTO WHAT WILL BE X R
0B07 4EEA73                       @NYADJ!->@-'NYSCR
0B0A                              ..INCREMENTS NYADJ
0B0A                                ..DECREMENTS NYSCR (WH BECAME X REGR)
0B0A                                ..PUTS CONFIG INTO 1ST SCRATCH LOCATI
0B0A                                ..
0B0A                                ..
0B0A                              ..NOW CREATE ADJ2
0B0A                                ..CONFIG ALREADY IN D REGR
0B0A FA705A                       &.AND.B'01110000'->@NYSCR
0B0D F6F6F6F6F15E5A               &/2/2/2/2.OR>@->@NYADJ,@NYSCR
0B14                                ..ADJ2 STORED IN ITS AND DUMMY@LOCN
0B14 72F473                       @!+@->@-  ..CONFIG+ADJ2 STORED
0B17 4EFEFBFFF25A@                @NYADJ!*2.XOR.#FF.AND.@->@NYSCR
0B1D                                ..PART CALCULATION OF@DONTWORRY BYTE
0B1D 60                           IRX..REINCREMENTS TO POINT AT@SUM TOTAL
0B1E                              ..
0B1E                              ..NOW FIND ADJ3
0B1E                              ..FINDING OF ADJ3,ADJ4,ADJ1 COULD BE
0B1E                                ..WRITTEN AS COMMON@SUBROUTINE
0B1E                                ..BUT@NO@ADVANTAGE IN CODE LENGTH
0B1E@0FFA08                       @NYCONF.AND.B'00001000'->&M
                                                              @   0B21 CE
0B22 F888                         B'10001000'->&  ..ELSE SET TO VALUE
  @ 0B24 5E                       &->@NYADJ
0B25                                ..STORES ADJ3,EITHER 0 OR@SET VALUE
0B25 F473                         &+@->@-   ..SUBTOTAL
0B27 4EF15A                       @NYADJ!.OR.@->@NYSCR
0B2A                                ..PART CALCN OF DONTWORRY BYTE
0B2A 60                           IRX ..INCREMENT X REGR
0B2B                              ..
0B2B                              ..NOW FIND ADJ4 SIMILARLY
0B2B 0FFA04                       @NYCONF.AND.B'00000100'->&
0B2E CE                           LSZ
0B2F F822                         B'00100010'->&
0B31 5E                           &->@NYADJ
0B32 F473                         &+@->@-
0B34 4EF15A60                     @NYADJ!.OR.@->@NYSCR; IRX
0B38                              ..
0B38                              ..NOW FIND ADJ1 SIMILARLY
```

```
AS              12/07/79


     0B38 0FFA80            650     @NYCONF.AND.B'10000000'->&
     0B3B CE                651     LSZ
@    0B3C F80F              652     B'00001111'->&
     0B3E 5E                653     &->@NYADJ
     0B3F F473              654@    &+@->@-
     0B41                   655     ..PARTIAL SUM SAVED
     0B41                   656     ..
     0B41                   657@    ..NOW CALCULATE  .NOT.DONTWORRY
     0B41 4EF1FBFF5E        658     @NYADJ!.OR.@.XOR.#FF->@NYADJ
     0B46 1E60              659     INC NYADJ;IRX
     0B48@FA                660     &+@->& ..PARITY SUM CHECK BYTE LEFT
     0B49                   661       ..IN D REGR. X REGR LEFT POINTING AT
     0B49                   662       ..SUM SCRATCH LOCATION@WHICH ONLY
     0B49                   663       ..CONTAINS PARTIAL SUM WHICH SHOULD
     0B49                   664       ..NOT BE USED
     0B49                   665       ..NYADJ LEFT POINTING AT PARITY SUM
     0B49                   666       ..BYTE,NYPARI,LOCATION
@    0B49 D7                667     SEP NYMAIN ..RETURN
     0B4A      @            668     ..END OF@SUBROUTINE ADJSET
     0B4A                   669   ..****************************************@
@@   0B4A                   670   ..****************************************
     0B4A                   671     ..*************J***J****J*************
     0B4A                   672     ..*
     0B4A                   673     ..*
 @   0B4A                   674     ..SUBROUTINE HEADS,CALLED IN PROGRAM
     0B4A                   675       ..SECTION RENEW
      4A                    676     ..ISSUES FAULT ON HEAD FAILURE THRUOUT
     0B4A                   677       ..ANY ADJACENCY SET
     0B4A                   678     ..AUTHOR THIS SUBROUTINE..NIGEL YOUNG
     0B4A                   679   HEADS:
     0B4A                   680     ..X REGR IS NYH,POINTING AT .NOT.H
     0B4A                   681     ..ENTER HERE
     0B4A FBB9AA            682     NYVAL1->NYSCR.@ ..SCRATCH
     0B4D                   683       ..MUST ENSURE NOT OTHERWISE NEEDED
     0B4D 72FBFFF2          684     @!.XOR.#FF.AND.@
     0B51 2F2F              685     DEC NYH;DEC NYH
     0B53 5F                686     ->@NYH ..STORES (.NOT.H').AND.H
     0B54 1F                687     INC NYH
     0B55 72F25A            688     @!.AND.@->@NYSCR ..(.NOT.H').AND.(.NOT@
     0B58                   689       ..IF NOT ZERO, FAULT
@F   0B58 3200              690     IF =@ GO@TO NYOFF6 ..RETURNS
@    0B5A F8CAAF            691     NYVAL5->NYH.@
     0B5D @F                692     @NYH ..OLD VALUE OF (.NOT.H').AND.(.NO@
 F   0B5E 3A@@              693     IF >@ GO TO NYOFF6 ..DONT RENEW IF
     0B60                   694           ..ALREADY NON-ZERO
     0B60 0A73              695     @NYSCR->@-
@    0B62 F826AA            696     NYVAL5->NYSCR.@ ..TIMER
     0B65 4A730A73          697     @NYSCR!->@-;@NYSCR->@-
@    0B69                   698       ..LOGS FAULT
     0B69 F823AB            699     NYVALU->NYSTA1.@ ..O/P STATUS
```

AS 12/07/79

```
0B6C 0BF9025B          700    @NYSTA1.OR.B'00000010'->@NYSTA1
0B70 1B                701    INC NYSTA1
0B71 0BF9025B          702    @NYSTA1.OR.B'00000010'->@NYSTA1
0B75                   703     ..SAVES FAULT INTERNALLY & FOR O/P
0B75                   704    ..??NEED TO@CHECK FAULT BUTTON
0B75 D7                705 NYOFF6:SEP NYMAIN ..RETURN
0B76                   706    ..END OF SUBROUTINE HEADS
0B76                   707 ..*****************************************
0B76                   708 ..*****************************************
0B76                   709 ..
0B76                   710 ..*****************************************
0B76                   711 ..*****************************************
0B76                   712    ..SUBROUTINE ADJPR,AUTHOR NIGEL YOUNG
0B76                   713    ..CALLED FOR F,F',H,H' PROCESSING
0B76                   714 ADJPR:
0B76 F8D7AE            715    NYVAL@->NYADJ.@ ..CONFIG
0B79                   716     ..SAVES FAULT IN TRUE LOCATION ALSO
0B79                   717     ..USE NYADJ TO POINT TO ADJACENCY BYTE
0B79                   718     ..N.B. UPPER BYTE MUST BE #0C
0B79 1E                719    INC NYADJ
0B7A 4EF2FEF17360      720    @NYADJ!.AND.@*2.OR.@->@-;IRX
0B80                   721     ..PERFORMS SECOND LEVEL PROCESSING
0B80 4EF2F6F17360      722    @NYADJ!.AND.@/2.OR.@->@-;IRX
0B86                   723     ..PERFORMS THIRD LEVEL PROCESSING
0B86 4EF2FEF17360      724    @NYADJ!.AND.@*2.OR.@->@-;IRX
0B8C                   725     ..PERFORMS FOURTH LEVEL PROCESSING
0B8C 4EF2FEFEFEFEF1    726    @NYADJ!.AND.@*2*2*2*2.OR.@
0B93 7360              727      ->@-;IRX
0B95                   728     ..PERFORMS FIRST LEVEL PROCESSING
0B95                   729    ..RESULT OF ADJACENCY PROCESSING
0B95                   730     ..LEFT IN D REGISTER AND AT LOCATION
0B95                   731     ..ORIGINALLY POINTED TO BY X REGISTER
0B95                   732    ..X REGISTER RESTORED TO ENTRY CONDITI@
0B95                   733    ..NYADJ REGISTER POINTS TO
0B95                   734     .. .NOT.DONTWORRY BYTE
0B95 D7                735    SEP NYMAIN ..RETURN
0B96                   736    ..END OF SUBROUTINE ADJPR
0B96                   737 ..*****************************************
0B96                   738 ..*****************************J***********
0B96                   739 ..*****************************************
0B96                   740 ..FATAL FAULT LATCHING SECTION,LACHFL
0B96                   741    ..FOR FAULTS WHICH CLOSE DOWN THIS
0B96                   742    ..SIDE OF SYSTEM
0B96                   743    ..NOT A SUBROUTINE,BRANCHED TO WITH
0B96                   744    ..ERROR CODE NO IN D REGR
0B96                   745    ..VALUE OF P VARIES WITH ERROR
0BD0                   746    ORG@BD0
0BD0                   747 LACHFL:
0BD0 79                748    MARK ..CLOBBERS M(R2)
0BD1 E26071            749    SEX R2;IRX;DIS
```

```
A5          12/07/79

     0BD4                        750      ..DISABLES I/RUPTS,RESTORES X,P
     0BD4 2252                   751     DEC R2;->@R2
     0BD6                        752      ..RESTORES R2,SAVES ERROR CODE NO
     0BD6                        753      ..IN ITS CLOBBERED MEMORY LKCN
     0BD6 F8B5AA                 754     NYVALW->NYSCR.0
     0BD9                        755      ..LACHFL STORAGE LOCN
     0BD9 F826AF                 756     NYVALS->NYH.0
     0BDC                        757      ..BYTE@OF TIMER
     0BDC                        758     ..NYH,NYSCR CLOBBERED..DOESN'T MATTER
     0BDC EA                     759     SEX NYSCR
     0BDD 02734F730F73           760     @R2->@-;@NYH!->@-;@NYH->@-
     0BE3                        761      ..SAVES ERROR CODE NO & TIME
     0BE3 F823AA                 762     NYVALU->NYSCR.0 ..O/P BYTE
F    0BE6 F800A4                 763     A.0(LABLX)->R4.0
F    0BE9 F800B4                 764     A.1(LABLX)->R4.1
     0BEC E4D4                   765     SEX R4;SEP R4
     0BEE 6442                   766     LABLX:OUT4, #42
     0BF0 30F0                   767  NYLOOP:GO TO NYLOOP
     0BF2                        768      ..LOOPS
     0BF2                        769     ..END OF LACHFL,FATAL FAULT LATCHING R@
     0BF2                        770  ..*****************************************
     0BF2                        771  ..*****************************************
     0BF2                        772     END
     0BF2                        774  ..*****************************************
     0BF2                        775  ..*****************************************
B    0BF2                        776
     0BF2                        777     END
```

AG2 12/07/79

```
 FL LOC  COSMAC CODE      LNNO SOURCE LINE
    0000                    1    ..GSE PROGRAM
    0000                    2    ..ENTRY WITH X=R5
    0000                    3    ..P=R7, R5=0C00
    0000                    4    TEMP=#01..TEMPORARY REGISTER USED IN OB
    0000                    5    TLOC=#03..ASCII BYTE STORED AT R3
    0000                    6    RAM=#06..DATA SHIFTED FROM R6
    0000                    7    WORK=#04..R4 IS WORKING REG
    0000                    8    DELAY=#08..R8 IS DELAY ROUTINE CTR
    0000                    9    OUT=#09..R9 IS O/P ASCII CHAR ROUTINE R
 e  0000                   10     ..R4 WORKING REG
    0000                   11    CMLOG=#0757
    0000                   12    ROMCK=#0750
    0000                   13    BDTST=#0792
    0970                   14    ORG #0970
    0970 C4                15    NOP
    0971 6B                16    INP3..GET GSE STATUS
    0972 FA0D              17    ANI#0D..MASK
 F  0974 C20000            18    LBZIDLRT..IDLE ROUTINE
    0977 FF01              19    SMI#01
 F  0979 C20000            20    LBZ DATOT..DATA OUT
 F  097C FF03C20000        21    SMI #03;LBZ RMRNA..RAM RETENTION
 F  0981 FF01C20000        22    SMI #01;LBZ RMRNB..     RAM RETENTION B
    0986 FF03C20757        23    SMI #03;LBZ CMLOG..COMMON LOGIC
    098B FF01C20750        24    SMI#01;LBZ ROMCK ..ROMCHECK
 F  0990 FF03C20000        25    SMI #03;LBZ RMTR..RAM TEST&RESET
    0995 C00792            26    LBR BDTST ..BOARD TEST (MICRO P)
    0998 E7                27   IDLRT:SEX 7
    0999 6450              28     OUT 4 ,#50..SETS GSE 1&2 HIGH
    099B 3098              29    BR IDLRT..WHICH CHECKS THEM FOR LATER R
    099D F8FFA5            30   RMRNA:LDI#FF;PLO 5
    09A0 85                31   ENCOR:GLO R5
    09A1 73                32    STXD
    09A2 3AA0              33    BNZ ENCOR..LOADS 0CFF=FF TO 0C00=00
    09A4 E7                34     SEX R7
    09A5 6410              35     OUT 4,#10..RAISE GSE FLAG
    09A7 30A7              36   ME:BR ME
    09A9 F80055            37   RMRNB:LDI#00;STR5
    09AC 72                38    LDXA
 e  09AD A6                39    PLO R6..PUTS 00 AT R6(0)
    09AE 86F4A6            40   BACKTO:GLO R6;ADD;PLO R6..TEMP SUM STORE
    09B1 6085              41    IRX;GLO R5
    09B3 3AAE              42    BNZ BACKTO
    09B5 86                43   GLO R6
    09B6 FF80              44    SMI#80..CHECKSUM BIT
    09B8 E7                45    SEX R7
 F  09B9 3A00              46    BNZ FLTY..BAD CHECKSUM BRANCH
    09BB 6450              47     OUT 4,#50..RAISE GSE 1&2
    09BD 30BD              48   TIME:BR TIME
    09BF 6410              49    FLTY:OUT 4,#10..RAISE GSE 1
```

AG2 12/07/79

```
    09C1 30BD              50    FF TIME
    09C3 F80A              51   RMTR:LDI #0A
    09C5 B9                52    PHI R9
    09C6 F8B1A9D9          53    LDI #B1;PLO R9;SEP R9..RAM TEST&RESET
    09CA E7                54    SEX R7
    09CB 6410              55     OUT 4,#10..GSE 1 HIGH SIGNIFIES
    09CD                   56     ..COMPLETE
    09CD 30CD              57   SELF:BR SELF
    09CF                   58    ..N.B. IF BAD RAM TEST
    09CF                   59    ..LACHFL PUTS GSE2 HIGH
    09CF                   60    ..OUTPUT RAM TO GSE ROUTINE
    09CF F80C              61   DATOT:LDI#0C
    09D1 B6                62    PHI RAM..REGISTER DENOTED BY&
    09D2 F800              63    LDI#00..RAM=0C00
    09D4 A6                64    PLO RAM
    09D5 A4                65    PLO WORK..REG DENOTED BY
    09D6                   66    ..WORK=XX00
F   09D6 F800A9            67    A.0(OPASCI)->R9.0
F   09D9 F800B9            68    A.1(OPASCI)->R9.1
F   09DC F800A8            69    A.0(DELRT)->R8.0
F   09DF F800B8            70    A.1(DELRT)->R8.1
    09E2 F821B3            71    LDI#21;PHI TLOC
    09E5 D9                72    SEP OUT..TRANSMIT!
    09E6 F84DB3            73    LDI#4D;PHI TLOC
    09E9 D9                74    SEP OUT.."M
    09EA F834B3            75    LDI#34;PHI TLOC
    09ED D9$               76    SEP OUT.."4
    09EE F834B3D9          77     LDI#34;PHI TLOC;SEP OUT.."4
    09F2 F830B3D9          78     LDI#30;PHI TLOC;SEP OUT.."0
    09F6 F830B3D9          79     LDI#30;PHI TLOC;SEP OUT.."0
    09FA F818AD            80     LDI#18;PLO RD...SET FOR 24 SPACES
    09FD F820B3D9          81   PHS:LDI#20;PHI TLOC;SEP OUT
    0A01 2D8DCA09FD        82     DEC RD;GLO RD;LBNZ PHS
    0A06 72                83   READ:LDXA..READ LOCATION 0C00
    0A07                   84    ..AND ADVANCED
    0A07 B4                85   PHI WORK
    0A08 F6F6F6F6          86    SHR;SHR;SHR;SHR
    0A0C FCF6              87   ADI#F6
F   0A0E 3B00              88   BNF LAB 1
    0A10 FC07              89   ADI#07
    0A12 FFC6              90    LAB1:SMI#C6..CONVERT THE FOUR MOST
    0A14 B3                91          PHI TLOC..SIGNIFICANT BITS
    0A15                   92                   ..TO ASCII
    0A15 D9                93         SEP OUT..O/P ASCII BYTE
    0A16 94                94         GHI WORK
    0A17 FEFEFEFE          95     SHL;SHL;SHL;SHL
    0A1B F6F6F6F6          96     SHR;SHR;SHR;SHR
    0A1F FCF6              97       ADI#F6
F   0A21 3B00              98       BNF LAB 2
    0A23 FC07              99      ADI#07
```

AG2 12/07/79

```
     0A25 FFC6          100    LAB2:SMI#C6..CONVERT THE FOUR LEAST
     0A27 B3            101         PHI TLOC..SIGNIFICANT BITS
     0A28               102    ..TO ASCII
     0A28 D9            103     SEP OUT..O/P ASCII BYTE
     0A29 F800FE        104    LDI#00;SHL..IS DF=0
     0A2C 84            105         GLO WORK
     0A2D FC01A4        106    ADI#01;PLO WORK..CHECKSUM TO STOP G
     0A30 CB0A06        107    LBNF READ..AFTER 256 BYTE TRANSFER
     0A33 F80DB3        108    LDI#0D;PHI TLOC..LOAD CRG. RTN.
     0A36 D9            109    SEP OUT..TRANSMIT"CARRIAGE RETURN"
     0A37 F7            110    SEX R7
     0A38 6410          111     OUT 4,#10..ISSUE GSE 1 FLAG
     0A3A C00A3A        112    THIS:LBR THIS
     0A3D               113    ..O/P ASCII CHARACTER ROUTINE
     0A3D D7            114    START:SEP R7
     0A3E F808A3        115    OPASCI:LDI#08;PLO TLOC
     0A41 F800AA        116    LDI#00;PLO TEMP
     0A44 7B            117    SEQ
     0A45 D8            118    RETURN:SEP DELAY
     0A46 23            119    DEC TLOC
     0A47 83            120    GLO TLOC
F    0A48 3200          121    BZ PAREND
     0A4A 93            122    GHI TLOC
     0A4B F6            123    SHR
     0A4C B3            124    PHI TLOC
F    0A4D 3B00          125    BNF TOM
     0A4F 11            126    INC TEMP
     0A50 7A            127    REQ
     0A51 38            128    SKP
     0A52 7B            129    TOM:SEQ
     0A53 C00A45        130    LBR RETURN
     0A56 81            131    PAREND:GLO TEMP
     0A57 F6            132    SHR
F    0A58 3B00          133     BNF BILL
     0A5A 7A            134    REQ
     0A5B 38            135    SKP
     0A5C 7B            136    BILL:SEQ ...EVEN PARITY
     0A5D D8            137     SEP DELAY
     0A5E 7A            138     REQ
     0A5F D8            139     SEP DELAY
     0A60 D8            140    SEP DELAY
     0A61 C00A3D        141    LBR START
     0A64               142    ..DELAY ROUTINE
     0A64 D9            143     STR1:SEP R9
     0A65 F851          144    DELRT:LDI#51 ..FOR 300 BAUD
     0A67 FF01          145    DIL:SMI #01
     0A69 C4C4          146     NOP;NOP
     0A6B 3A67          147    BNZ DIL
     0A6D C00A64        148    LBR STR1
     0A70               149     ...BOARD TEST PROGRAM
```

AG2 12/07/79

```
    0A70                    150    ...(GSE SWITCH AT B'111'
    0792                    151    ORG#0792
    0792 F890               152    LDI#90
    0794 A2                 153    PLO R2
F   0795 F800B1B9           154    A.1(INADR)->R1.1,R9.1
F   0799 F800A1             155    A.0(INADR)->R1.0  ..INTERRUPT ADDRESS
    079C E7                 156    SEX R7
    079D 7077               157    RET,#77
F   079F F800A9             158    A.0(DALLY)->R9.0
    07A2 E561D962D9         159    SEX R5;OUT 1;SEP R9;OUT 2;SEP R9
    07A7 63D964D967D9       160    OUT 3;SEP R9;OUT 4;SEP R9;OUT 7;SEP R9
    07AD C00200             161    LBR #0200
    07B0 7A                 162   CMBAK:REQ
    07B1 F800A5             163   CIRCLE:LDI#00;PLO R5 ..TO RESET PORT
F   07B4 3400F8B155         164    B1 HAY;LDI#01;STR R5
F   07B9 3500F802F155       165   HAY:B2 BEE;LDI#02;OR;STR R5
F   07BF 3600F804F155       166   BEE:B3 SEA;LDI 4;OR;STR R5
F   07C5 3700F808F155       167   SEA:B4 DEE;LDI 8;OR;STR R5
    07CB 64                 168   DEE:OUT 4
    07CC 30B1               169    BR CIRCLE
    07CE D7                 170   PIE:SEP R7
    07CF F8A0BFAF           171   DALLY:LDI#A0;PHI RF;PLO RF;..APPROX
    07D3 2F9F3AD3           172   HONEY:DEC RF;GHI RF;BNZ HONEY
    07D7                    173    ...                          ..1 S DELAY
    07D7 30CE               174    BR PIE
    07D9                    175    ORG*.....DOES NOTHING!!
    07D9 6072FE7270         176   BYBYE:IRX;LDXA;SHL;LDXA;RET
    07DE 22782273           177   INADR:DEC R2;SAV;DEC R2;STXD  ..SAVE ACC
    07E2 7673               178    SHRC;STXD  ..SAVE DF
    07E4 F8A0BEAE7B         179   LDI#A0;PHI RE;PLO RE;SEQ
    07E9 2E9E3AE9           180   CRAZY:DEC RE;GHI RE;BNZ CRAZY ..1 SEC D
    07ED 7A30D9             181    REQ;BR BYBYE
    0200 7BD9C005F9         182    ORG#0200;SEQ;SEP R9;LBR#05F9
    05F9 7AD9C0078D         183    ORG#05F9;REQ;SEP R9;LBR#078D
    078D 7BD9C00968         184    ORG#078D;SEQ;SEP R9;LBR#0968
    0968 7AD9C00AF1         185    ORG#0968;REQ;SEP R9;LBR#0AF1
    0AF1 7BD9C007B0         186    ORG#0AF1;SEQ;SEP R9;LBRCMBAK
    0AF6                    187    ..THESE ARE SKIP THROUGH
    0AF6                    188    ..ADDRESSES TO PROVE
    0AF6                    189    ..MEMORY DECODING IS OK
```

```
L
!M
0000 ;                  0001   .. ******COMMON LOGIC TEST PROGRAMME******
0000 ;                  0002 ORG=0757
0757 E7;                0003 SEX R7
0758 6200;              0004 OUT 2,=00
075A C4C4;              0005 NOP NOP  .. AM I MASTER
075C 20;                0006 DEC R0
075D E0;                0007 SEX P0
075E F0FA02;            0008 LDX ANI=02
0761 E7;                0009 SEX R7
0762 327C;              0010 BZ SLAVE
0764 64C4;              0011 BEGIN: OUT 4,=C4  .. ISSUE T/S,FIRE & GSE 2
0766 F840B4A4;          0012 LDI=40 PHI R4 PLO R4  ..APPROX 400 MS DELAY
076A 24943A6A;          0013 DIL1: DEC R4 GHI R4 BNZ DIL1
076E 6498;              0014 OUT 4,=98  .. RESET FIRE & GSE 2, ISSUE
0770 F840B4A4;          0015 LDI=40 PHI R4 PLO R4  .. INHIBIT & GSE 1
0774 2494;              0016 DIL2: DEC R4 GHI R4
0776 3A74;              0017 BNZ DIL2  .. TIME DELAY
0778 6450;              0018 FLASH: OUT 4,=50  ..RESET INHIBIT, T/S &
077A 307A;              0019 THIS: BR THIS  ..ISSUE GSE 1 & 2
077C F8FFB4A4;          0020 SLAVE:LDI=FF PHI R4 PLO R4
0780 2494C4;            0021 DELAY:DEC R4 GHI R4 NOP .. APPROX 2 SEC DELAY
0783 3A80;              0022 BNZ DELAY
0785 3564;              0023 SELF: B2 BEGIN
0787 3085;              0024 BR SELF
0789 ;                  0025
0789 ;                  0026
0789 ;                  0027   ..******ROM CHECK SET UP******
0789 ;                  0028
0789 ;                  0029 ORG=0740  .. ROM CHECK SET U
0740 F823A5;            0030 SEVEN:LDI=23 PLO R5 ..ALL REQ'D FOR
0743 F88055;            0031 LDI=80 STR P5 ..CORRECT SET
0746 F8FFA5;            0032 LDI=FF PLO P5 ..UP TO ENTER
0749 F801B3;            0033 LDI=01 PHI R3 ..BACKGROUND PGM.
074C F870A3;            0034 LDI=70 PLO R3
074F D3;                0035 SEP R3
0750 3040;              0036 BR SEVEN ..ENTRY POINT
0752 ;                  0037 ORG=05F9
05F9 7AD9C0073D;        0038 .=7A,=D9,=C0,=07,=8D ..NOT USED IN PROG,BUT LEFT OVER
05FE ;                  0039 ORG=0AF1
0AF1 7BD9C007B0;        0040 .=7B,=D9,=C0,=07,=B0 ..FROM PREVIOUS EDITS
0AF6 ;                  0041                      ..AND MUST BE INCLUDED FOR
0AF6 ;                  0042                      ..CORRECT PARITY
0AF6 ;                  0043 END
0000

? F,H,L,U=
```

APPENDIX A-3

INSTRUCTION SUMMARY FOR 1802

Appendix A — Instruction Summary

The COSMAC instruction summary is given in Tables I and II. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation

M(R(N)) → D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

TABLE I – INSTRUCTION SUMMARY
by Class of Operation

Register Operations

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) –1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1

Memory Reference

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D;R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) + 1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) –1

Logic Operations◆◆

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		

◆NOTE THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED
◆◆NOTE THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF

Arithmetic Operations◆◆

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D, R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))-D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P)) D→DF, D, R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))-D-(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P)) D (NOT DF)→DF, D, R(P) +1
SUBTRACT MEMORY	SM	F7	D M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D M(R(P))→DF, D, R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D M(R(X))-(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D-M(R(P))-(NOT DF)→DF, D R(P) +1

Branch Instructions — Short Branch

SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38◆	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33◆	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	38◆	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1 (1 = V_{SS})	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0 (0 = V_{CC})	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1 (1 = V_{SS})	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0 (0 = V_{CC})	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1 (1 = V_{SS})	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0 (0 = V_{CC})	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1 (1 = V_{SS})	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0 (0 = V_{CC})	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1

Branch Instructions — Long Branch

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8◆	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→ R(P).1 M(R(P) +1)→ R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	C8	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→ R(P).0 ELSE R(P) +2

Skip Instructions

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SHORT SKIP (SEE NBR)	SKP	38◆	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8◆	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE

◆NOTE THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.
◆◆NOTE THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.

Control Instructions

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
IDLE	IDL	00	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE

Input–Output Byte Transfer

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

*NOTE THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED

**NOTE THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF

APPENDIX A-4

COSMAC LEVEL 2 ASSEMBLY LANGUAGE

In order to make programming easier, in Level II operations several of the op-code mnemonics can be replaced with codes that correspond to their most frequent use. Likewise, operations involving the D register can be done using D-sequence instructions. In D-sequence instructions, special characters are used instead of op-code mnemonics making D-sequence instructions similar in appearance to APL statements. (APL is a high-level programming language)

Executable Statements: Level II

Substitution Instructions. The substitutions for the op-code mnemonics fall into two forms. The mnemonics and their substitutions are listed in Table VI. The first form involves simply the use of an immediate keyword in the same way that the mnemonic was used. These keywords are IDLE, GOTO, NOGOTO, SKIP, RETURN, DISABLE, POP, PUSH, SAVE, GOSTATE, CALL, and EXIT. EXIT is treated like a first class instruction and CALL is treated like a macro call in that it is followed by an operand string. They are used to execute the standard call and return procedures. In order to use them, the registers 2 through 6 must already be set aside for the standard call and, return procedure . They can be initialized by using the Utility Program UT21 built-in subroutines, INIT1 and INIT2. (Refer to Chapter 10). The operands of CALL consist of the address of the subroutine, followed by any inline parameters that the programmer wishes to pass. EXIT has no operands.

The second form consists of the word IF followed by a space, a BRANCH keyword, another space, and the keyword GOTO. The BRANCH keywords indicate the condition on which a branch is to take place. They are Q, &=, =0, DF, PZ, GE, EF1, EF2, EF3, EF4, NQ, &>0, >0, NDF, MINUS, LESS, NEF1, NEF2, NEF3, and NEF4.

```
<immediate keyword> ::= IDLE|GOTO|NOGOTO|SKIP|RETURN
   |DISABLE|POP|PUSH|SAVE|GOSTATE|CALL|EXIT
<branch keyword> ::=Q|&=|=0|DF|PZ|GE|EF1|EF2|EF3|EF4
   |NQ|&>0|>0|NDF|MINUS|LESS|NEF1|NEF2|NEF3|NEF4
<substitution> ::= IF <branch keyword>GOTO|<immediate keyword>
```

Examples:

```
IDLE                        IDL
GOTO ADD_NUMS               BR ADD_NUMS
IF =0 GOTO BEGINNING        BZ BEGINNING
IF NEF4 GOTO END_           BN4 END_
GOSTATE R5                  SEP R5
CALL TYPE,'MESSAGE'         SEP R4
                            DC TYPE
                            DC 'MESSAGE'
PUSH X                      STXD X
POP   Y                     LDA Y
```

D-Sequence Instructions. The D-Sequence instructions consist of three parts, the load part, the manipulation part, and the storage part. What each of these parts corresponds to is listed in Table VII. Not all parts are needed in a statement. Any single part can be present or all can be present. Two parts can also be present, but if more than one part is present, the order load, manipulation, and storage part must be maintained.

The load part tells the assembler what should be loaded into the D-register. A register name followed by a .0 or .1 indicates the either the low- or high-order byte of that register should be loaded into D. A constant, identifier, or term in parentheses indicates that the value of that constant, identifier, or term should be loaded immediately into the D-register. An @ indicates that the D-register should be loaded from memory. If a register name follows the @, then the byte pointed to by that register is used. If no register name is specified, the register named by the X register used. If a " precedes the register name it indicates that the X-register should be set to point to that register. If memory is accessed and a ! ends the load part, the contents of the register used is incremented. If the @ ends the load part, a comment in parentheses may be inserted immediately (without spaces) after the @.

The manipulation part tells the assembler what is to be done with the D-register. There are 9 binary operations which can be performed and 4 unary operations. The binary operations are + (add), - (subtract), -+ (subtract and negate), +" (add with carry), -" (subtract with borrow), -+" (subtract and negate with borrow), .AND. (and), .OR. (or), and .XOR. (exclusive or). The manipulation part for the binary operations consists of the operator symbol followed without spaces by the source of the second operand. The source can be a memory location, a constant, an identifier, or a term in parentheses. If a constant, identifier, or term is used, its value is immediately used. To use the memory, an @ immediately follows the operation symbol. Immediately following the @ there is a " followed by a register name. The X-register is set to register name and the register points to the memory byte that is used. The unary operators are /2 (shift right), *2 (shift left), /2" (shift right circular) or *2" (shift left circular).

The storage part tells the assembler what to do with the contents of the D-register. All storage parts begin with -> (a minus followed by a greater than). If a register name followed by .0 or .1 follows the arrow (->), the contents are stored in the low- or high-order byte of that register. If an @ follows the arrow, the contents are stored in memory. If a register name follows the @, it points to the byte in memory where the D-register contents are to be stored. If no register name follows the @, the register specified by the X-register is used. The @ may be followed by a - indicating that the contents of the register used should be decremented. If the - is used, then the register name (if there is one) must be separated from the - by a ". The X-register is set to the register name given. If the @- is the end of the storage part, then a comment within parentheses may immediately follow the @-.

```
<load part> ::= @|@!|@<register>|'<register>|
   |@"<register>|@(<character string>)|<register>.0
   |<register>.1|<term>
<object> ::= @|'"<register>|<term>
<operator> ::= +|-|-+|+"|-"|-+"|.AND.|.OR.|.XOR.
<manipulation part> ::= <operator><object>|/2|*2|/2"|*2"
<storage part> ::= ->register>.0|->register>.1|->@<register>
   |->@-|->@-"<register>|->@-(<character string>)
<D-sequence statement> ::= <load part>|<manipulation part>
   |<storage part>|<load part><manipulation part>
   |<load part><storage part>|<manipulation part><storage part>
   |<load part><manipulation part><storage part>
```

Note that no spaces are allowed between the special characters involved or between the special characters and any identifiers or registers that are used. There is also a limit on the length of a Level II statement. It may be contain no more than thirty-nine characters.

Examples:

5->R5.0	LDI 5;PLO R5
5	LDI 5
A	LDI A
FIVE+2->R7.0	LDI FIVE;ADI 2;PLO R7
@N!->@-"N	LDA N;SEX N:STXD
.XOR.CAR_RET	XRI CAR_RET
(FIVE+SIX)->@UTILITY	LDI 11;STR UTILITY

Sample Program Illustrating D-Sequences. Fig. 13 is a repeat of Fig. 12 thefirst sample program written in Level II assembly. It illustrates the use of the D-sequence statements and substitutions.

Table VI - Level II Substitutions for Level I Mnemonics

Level I	Level II
B1	IF EF1 GOTO
B2	IF EF2 GOTO
B3	IF EF3 GOTO
B4	IF EF4 GOTO
BDF	IF DF GOTO
BGE	IF GE GOTO
BL	IF LESS GOTO
BM	IF MINUS GOTO
BN1	IF NEF1 GOTO
BN2	IF NEF2 GOTO
BN3	IF NEF3 GOTO
BN4	IF NEF4 GOTO
BNF	IF NDF GOTO
BNQ	IF NQ GOTO
BNZ	IF &>0 GOTO
	IF >0 GOTO
BPZ	IF PZ GOTO
BR	GOTO
BQ	IF Q GOTO
BZ	IF &=0 GOTO
	IF =0 GOTO
DIS	DISABLE
IDL	IDLE
LDXA	POP
NBR	NOGOTO
RET	RETURN
SAV	SAVE
SEP	GOSTATE
SKP	SKIP
STXD	PUSH
SEP R4	CALL
SEP R5	EXIT

Table VII - D-Sequence Statements

Symbol	Level I	Action
Load Part		
@	LDX	M(R(X))->D
@"N	SEX N;LDX	N->X;M(R(X))->D
@(COMMENT)	LDX ..COMMENT	M(R(X))->D
@N	LDN N	M(R(N))->D FOR N<>0
N.0	GLO N	R(N).0->D
N.1	GHI N	R(N).1->D
@N!	LDA N	M(R(N))->D;R(N)+1->R(N)
CONSTANT	LDI CONSTANT	A.0(CONSTANT)->D
@!	LDXA	M(R(X))->D;R(X)+1->R(X)
Manipulation Part		
+@	ADD	D+M(R(X))->DF,D
+@"N	SEX N;ADD	N->X;D+M(R(X))->DF,D
+CONSTANT	ADI CONSTANT	D+CONSTANT->DF,D
-@	SM	D-M(R(X))->DF,D
-@"N	SEX N;SM	N->X;D-M(R(X))->DF,D
-CONSTANT	SMI CONSTANT	D-CONSTANT->DF,D
-+@	SD	M(R(X))-D->DF,D
-+@"N	SEX N;SD	N->X;M(R(X))-D->DF,D
-+CONSTANT	SDI CONSTANT	CONSTANT-D->DF,D
+"@	ADC	D+M(R(X))+DF->DF,D
+"@"N"	SEX N;ADC	N->X;D+M(R(X))+DF->DF,D
+"CONSTANT	ADCI CONSTANT	D+CONSTANT+DF->DF,D
-"@	SMB	D-M(R(X))-NDF->DF,D
-"@"N	SEX N;SMB	N->X;D-M(R(X))-NDF->DF,D
-"CONSTANT	SMBI CONSTANT	D-CONSTANT-NDF->DF,D
-+"@	SDB	M(R(X))-D-NDF->DF,D
-+"@"N	SEX N;SDB	N->X;M(R(X))-NDF->DF,D
-+"CONSTANT	SDBI CONSTANT	CONSTANT-D-NDF->DF,D
.AND.@	AND	D.AND.M(R(X))->D
.AND.@"N	SEX N;AND	N->X;D.AND.M(R(X))->D
.AND.CONSTANT	ANI CONSTANT	D.AND.CONSTANT->D
.OR.@	OR	D.OR.M(R(X))->D
.OR.@"N	SEX N;OR	N->X;D.OR.M(R(X))->D
.OR.CONSTANT	ORI CONSTANT	D.OR.CONSTANT->D
.XOR.@	XOR	D.XOR.M(R(X))->D
.XOR.@"N	SEX N;XOR	N->X;D.XOR.M(R(X))->D
.XOR.CONSTANT	XRI CONSTANT	D.XOR.CONSTANT->D

Table VII (cont'd)

Symbol	Level I	Action
Manipulation Part		
/2	SHR	SHIFT D RIGHT NONCIRCULAR
*2	SHL	SHIFT D LEFT NONCIRCULAR
/2"	SHRC	SHIFT D RIGHT CIRCULAR
*2"	SHLC	SHIFT D LEFT CIRCULAR
Storage Part		
->N.0	PLO N	D->R(N).0
->N.1	PHI N	D->R(N).1
->@N	STR N	D->M(R(N))
->@-	STXD	D->M(R(X));R(X)-1->R(X)
->@-"N	SEX N;STXD	N->X;D->M(R(X));R(X)-1->R(X)
->@-(COMMENT)	STXD ..COMMENT	D->M(R(X));R(X)-1->R(X)

Note 1: Wherever an N appears, a register may be placed. (R followed by a hexadecimal digit or a hexadecimal constant less than 10H)

Note 2: Wherever the word constant appears, a constant or valid identifier may be placed.

Note 3: Wherever an @ appears at the end of a part (not followed by "N, N, or !), it may be replaced with @ (comment).

APPENDIX B-1

QUALITY DATA SHEETS - Q5304
Q5308
Q5309
Q5310

GRAVINER LIMITED, COLNBROOK, ENGLAND	DATA SHEET No. Q.53.4	
QUALITY CONTROL DATA SHEET	SHEET No. 1	No. OF SHEETS 12

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART A. MANDATORY REQUIREMENTS

DEFINITION

Q.53.4 becomes a master document for function performance testing of U.V. Detectors.

Performance values have been defined in compliance with "funnel" or "tiered tolerances" philosophy and form the following categories.

Type 1 - Factory or Production Acceptance Limits
appropriate at normal ambient temperature conditions.

Type 2 - Receiving Inspection or Customer Acceptance Limits
appropriate at normal ambient temperature conditions.

Type 3 - Quality or Functional Acceptance Limits
appropriate at and between the declared extremes of operating temperature.

In any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptance value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any specified test where a single value remains in the test is applicable to Type 1, 2 and 3 tests.

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GRAVINER LIMITED, COULSDON, ENGLAND.	DATA SHEET No. Q5304	
QUALITY CONTROL DATA SHEET	SHEET No. 2	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART A. RAILPORT REQUIREMENTS.

NOTE

Care should be taken not to subject personnel's eyes to U.V. radiation from emitters on Test Kit, Detector Heads, or from the Solar Lamp.

1. IDENTIFICATION

Each U.V. detector shall be given a unique serial number.

2. FREQUENCY OF TEST

The following tests shall be carried out on a 100% basis on detector assemblies.

3. SEQUENCE OF TESTS

Type 1 Tests - Paras. 5.2. -

Type 2 Tests - As defined in Users Handbook

Type 3 Tests - From Para. 5.2.

4. ACTIONS REQUIRED

All results shall be recorded against the serial number of the detector assembly and shall show the date of the test.

5. TEST DESCRIPTION

5.1. Equipment Required

Test Kit - Tool No. 697-128 with adaptor for detector head.

Solar Simulator (with 2 filters) - Tool No. 697-112

Electronic Counter with 1-100 sec. gate times.

Digital Voltmeter with 1 Kv d.c. range.

Calibrated photocell.

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TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART A. MANDATORY REQUIREMENTS.

5.1.1. Calibration of Test Equipment

The U.V. source shall satisfy the following requirements:-

When measured at the front face of the U.V. Detector, irradiance at wave length 220 nm and bandwidth less than 10 nm shall not be greater than 3×10^{-10} watts/cm^2.

Irradiance at any other wavelength between 270 and 320 nm of a bandwidth less than 10 nm shall not be greater than 10^{-7} watts/cm^2.

A 5" pan fire at a distance of 4 ft. satisfies this requirement.

The standard test emitters (type 45666-201) mounted on the test equipment (Tool No. 697-128), shall be calibrated, to give the same output response from the reference photocell, as when that photocell views the above pan fire.

Note: This calibration is additional to the pre-checking calibration required by the test procedure.

5.1.2. Test Sequence

The following tests shall be performed in sequence.

5.2. Sensitivity

The calibrated photocell shall be mounted in the Test Kit, Tool No. 697-128, the positive terminal in the A+ position. The applied voltage shall be 320V ± 5v.

The count rate from the reference photocell shall be used in conjunction with Table 1 to compute the radiation falling on the photocell, and the acceptance value for the detector head on test.

5.2.1. Sensitivity as a Function of Gas Leakage

The applied voltage of the cell on test shall be reduced to -(See 5.6.)

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TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART A. MANDATORY REQUIREMENTS.

5.2.1. Sensitivity as a Function of Gas Leakage (contd.)

The voltage to test emitter shall be switched OFF.

After a minimum period of 5 seconds, the test emitter shall be switched on.

The count rate from the detector on test shall be greater than 5 pulses/sec.

5.3. Solar Immunity

With a supply voltage of 320V ± 5V applied, the detector on test shall be exposed to a solar lamp (697-112). The electrodes of the cell shall be 2.5" ± 0.25" from the lamp filter.

The count rate shall be less than - (See para. 5.)

5.4. U.V. Emitter Test

5.4.1. Low Voltage Operation

The voltage shall be set to - (See para. 5.) The emitter shall be switched on, and the discharge of the emitter observed to occur across the narrowest gap of the electrodes, for a period of not less than 30 seconds.

5.4.2. High Voltage Operation

The applied voltage shall be set to 320V ± 5V. The emitter shall be switched on and the discharge observed to occur across the narrowest gap of the electrodes, for a period of not less than 30 seconds.

5.5. Insulation Test

The insulation between the live pins linked together, and the detector case shall be not less than 20 megohms, at 500 Volts.

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GRAVNER LIMITED, COLNBROOK, ENGLAND	DATA SHEET No. A 5304	
QUALITY CONTROL DATA SHEET	SHEET No. 5	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART A. HARDAPORT REQUIREMENTS.

5.6. Schedule of Test Limits

Test Definition	Category	Value	Unit
5.2.1.	1	280	Volts
	2	285	Volts
	3	290	Volts
5.3.	1	1.2	Pulses/sec.
	2	5	Pulses/sec.
	3	5	Pulses/sec.
5.4.1.	1	280	Volts
	2	285	Volts
	3	290	Volts

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TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART A. RANDAFORT REQUIREMENTS.

TABLE 1

CHANNEL B TEST EMITTER	PROBE ACCEPTANCE COUNT RATE (PULSE/SEC)
1.4y	68
1.3y	63
1.2y	58
1.1y	53
y	48
0.9y	43
0.8y	38
0.7y	33
0.6y	28

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GRAVINER LIMITED, COLNEBROOK, ENGLAND.	DATA SHEET No. D.5304	
QUALITY CONTROL DATA SHEET	SHEET No. 7	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART B. GRAVINER PREFERRED TESTING PROCEDURE.

1. EQUIPMENT REQUIRED

Test Kit - 697-128.
Test Kit to detector head adaptor.
Calibrated photocell
Pulse counter with 100 sec. gate times
Solar Lamp - Tool No. 697-112 and 2 filters.
D.V.M. with D.C. 1 KV range.

2. SETTING UP PROCEDURE FOR CALIBRATION

S1 and S3 to OFF.
S2 to position B.
S4 to position B+
S5 to position 3
S6 to position 1.
S8 to position OUT.
S7 to position 2.
Connect BNC 1 to pulse counter and SKT 2 to DVM.
Set counter to DC Channel A.
Set pulse counter to 100 sec. gate.
Set D.V.M. to suitable range (more than 32[illegible])
S9 to 2 mS.

3. CALIBRATION PROCEDURE

Fit calibrated photocell to test kit with positive pin to position A, when [illegible] on holder is in B position.
S1 to position ON. LP1 will illuminate. Allow 5 [illegible]utes warm up time.
D.V.M. to read 320V ± 5V, S8 to position IN.
S3 to position ON, test emitter B will illuminate.
Press reset button on pulse counter.
At the end of 100 second period, total counts will be displayed. These, [illegible] in conjunction with the calibration certificate and Table 1 ascertain the acceptance level to be used.
S3 to OFF when counts are displayed

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q5304	
QUALITY CONTROL DATA SHEET	SHEET No. 8	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART B . GRAVINER PREFERRED TESTING PROCEDURE.

4. SETTING UP PROCEDURE FOR TESTING

S1 and S3 to OFF.
S2 to position B.
S4 to position B+.
S5 to position 1.
S6 to position 1.
S8 to position OUT.
S7 to position 2.
S9 to position 2 mS.
Adaptor switches to position P/Cell and position A.
Connect adaptor to Test Kit. Connect screen clip to earthing point on test kit.
Connect head to be tested to adaptor lead. Fit head to test kit with photocell in line with emitter B. In the case of a dual head, align P/Cell A with emitter.

5. SENSITIVITY TEST

5.1. Single Head, and Channel A of Dual Head

S1 to position ON, LP1 will illuminate.
D.V.M. to read 320V ± 5V.
S8 to position IN.
S3 to ON, test emitter B will illuminate.
Press reset button on pulse counter. The counts will be recorded after 100 secs.
Refer to acceptance level from Para. 3.
S3 to OFF after counts have been recorded.

5.2. Channel B of Dual Head

Switch on Adaptor to B.
Align photocell B with test emitter B.
S3 to ON. Emitter B will illuminate.
Press reset button on pulse counter. The counts will be recorded after 100 secs.
Refer to acceptance level from Para. 3.
S3 to OFF after counts have been recorded.

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TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS
PART B. GRAVINER PREFERRED TESTING PROCEDURE.

6. SENSITIVITY AS A FUNCTION OF GAS LEAKAGE

6.1. Channel B (Dual Head)

S8 to position OUT.
S7 to position 4.
D.V.M. to read 280V ± 5V.
S8 to IN position.
S3 to ON position. Test emitter B will illuminate.
Press reset button on pulse counter. The counts over a 100 sec. period will be recorded, and must be greater than 5 pulses per second (pps).
S3 to OFF position, test emitter will extinguish.

6.2. Channel A and Single Head

Reposition head to align channel A with test emitter B.
Switch on adaptor to position A.
S3 to ON position, test emitter B will illuminate.
Press reset button on pulse counter. The counts over a 100 sec. period will be recorded, and must be greater than 5 p.p.s.
S3 to OFF position, test emitter will extinguish.
S8 to position OUT.

7. EMITTER CHECK 320V

7.1. Channel A (Dual Head) and Single Head

Adaptor switch to EMITTER position.
S7 to position 5.
D.V.M. shall read 320± 5V.
S8 to position IN.
The emitter on channel A will illuminate, and the discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.
S8 to position OUT.

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TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART B. GRAVINER PREFERRED TESTING PROCEDURE.

7.2. Channel B (Dual Head)

Adaptor switch to position B.
S8 to position IN.
The emitter on channel B will illuminate, and the discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.
S8 to position OUT.

8. EMITTER CHECK 280V

8.1. Channel B (Dual Head)

S8 to position OUT.
S7 to position 6.
D.V.M. shall read 280V $\pm$ 5V.
S8 to position IN.
The emitter on Channel B will illuminate. The discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.
S8 to position OUT.

8.2. Channel A (Dual Head) and Single Head

Switch on Adaptor to position A.
Switch S8 to position IN.
The emitter on Channel A will illuminate. The discharge shall occur across the narrowest gap of the electrodes, for a period of not less than 30 secs.
S8 to position OUT.
S1 to position OFF, LP1 will extinguish.

9. MEGGER CHECK

S6 to position 2.
Plug a 500V megger into sockets marked megger, ensure that the 'croc' clip on the yellow flylead is connected to the metal case of the head on test. The megger when energised should read more than 20 megohms.

10. SOLAR

NOTE: Care should be taken not to subject personnel eyes to light emitted by the

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10. SOLAR (contd.)

solar lamp. Slide gate on lamp to be closed before switching lamp on.

10.1. Channel A (Dual Head) and Single Head

S6 to position 1.
S8 to position OUT.
S7 to position 1.
Adaptor switch to position A and position PHOTOCELL.
Mount head to adaptor on solar lamp, with channel A nearest source.
Turn solar lamp on and allow to warm up for 5 minutes.
S1 to position ON, LP1 illuminates.
D.V.M. to read 320V ± 5V.
Place cover over head and filters.
Open slide gate on lamp.
S8 to position IN.
Press reset button on pulse counter.
The counts over a 100 sec. period will be recorded, and must be less than - (See para. 5.6.).
Close slide gate on lamp.
S8 to OUT.

10.2. Channel B (Dual Head)

Adaptor switch to position B.
Move head so that Channel B is nearest source window.
Place cover over head and filters.
Open slide gate on lamp.
S8 to position IN.
Press reset button on pulse counter.
The counts over a 100 sec. period will be recorded, and must be less than - (See para. 5.6.).
Close slide gate on lamp.
S8 to OUT.
Disconnect head from fixture.

END OF TEST

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. A 53.4	
QUALITY CONTROL DATA SHEET	SHEET No. 12	No. OF SHEETS

TITLE: DRAFT ACCEPTANCE REQUIREMENTS FOR 53521-012 AND 53522-011 HIGH TEMPERATURE U.V. DETECTORS PART B. GRAVINER PREFERRED TESTING PROCEDURE.

NOTE: If the solar lamp is turned off, a period of at least 30 minutes must elapse before it is switched back on.

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GRAVINER LIMITED. COLNBROOK. ENGLAND.	DATA SHEET No. Q 5308	
QUALITY CONTROL DATA SHEET	SHEET No. 1	No. OF SHEETS 14

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

1. DEFINITION

Q.5308 becomes a master document for functional performance testing of Crew Warning Unit.

Performance values have been defined in compliance with "funnel" or "tiered tolerances" philosophy and form the following categories.

Type 1 - Factory or Production Acceptance Limits appropriate at normal ambient temperature conditions.

Type 2 - Receiving Inspection or Customer Acceptance Limits appropriate at normal ambient temperature conditions.

Type 3 - Quality or Functional Acceptance Limits appropriate at and between the declared extremes of operating temperatures.

In any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptance value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any specified test where a single value remains in the test is applicable to Type 1, 2 and 3 tests.

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GRAVINER LIMITED. COLNBROOK. ENGLAND.	DATA SHEET No. A 5308	
QUALITY CONTROL DATA SHEET	SHEET No. 2	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART A

2. FREQUENCY OF TEST

The following tests shall be carried out at a frequency appropriate to definition.

Type 1 All units.

Type 2 It is recommended that all units "on receipt" and subsequently as defined in users procedures and schedules.

Type 3 These will be carried out as appropriate upon:

a) Initiation of production.

b) Introduction of a major modification.

c) Cessation of production for 6 months or more.

d) Introduction of new processes which may affect production standards.

e) Change of key operator.

The samples shall be selected at random from current production and shall previously have passed the production or factory Type 1 test.

In addition, sampling shall be as follows:

Up to a production rate of 100 items per year, one item is to be selected annually for non-destructive testing. For destructive testing one unit is to be selected annually.

3. ACTION REQUIRED

3.1. For Type 1 tests all results shall be recorded against the serial number of each control unit.

For Type 3 tests, an abridged test report detailing results against the serial number of each control unit is to be raised.

3.2. For Type 1 tests any failure shall be reported to the Design Authority.

For Type 3 tests control unit that fails any part of the tests shall be examined to establish the cause of failure.

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TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

3.2. cont.

An additional unit shall be taken for test and dependent on results, action will be taken to release the batch and to make amendments to inspection requirements, test requirements, production techniques or design standards as is appropriate.

4. TYPE 1. PRODUCTION ACCEPTANCE TESTS

4.1. Equipment Required for Tests

1. 0.5 A stabilised supply variable from 16v to 29v DC.
2. 0 to 30v DC digital volt meter (DVM) with minimum input resistance of 1 megohm.
3. 0 - 0.2A DC ammeter.
4. Four 3K6 2% .5w resistor.
5. 500v DC insulation tester.
6. Ohm meter.

4.2. Electrical Connections

1. Connect +ve of DC power supply via an ammeter to connector pin number 6.
2. Connect +ve of voltmeter to +ve of DC power supply.
3. Connect the -ve of DC power supply to connect pin number 5.
4. Connect a 3K6 resistor between connector pin number 9 and 5.
5. Connect a 3K6 resistor between connector pin number 10 and 5.
6. Connect a 3K6 resistor between connector pin number 11 and 5.
7. Connect a 3K6 resistor between connector pin number 12 and 5.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5308	
QUALITY CONTROL DATA SHEET	SHEET No. 4	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

4.3. Electrical Requirements

Note: The limits are given in the schedule of test limits, para. 8.0.

4.3.1. Indicator Functional Checks

Set the DC supply to 16v.

4.3.2. Connect the +ve of the supply via an ammeter to connector pin no. 1. "L ENG FIRE" should show. The current drawn should be between ------mA and------ mA. Disconnect number 1 from +ve of the supply. Indication to cancel.

4.3.3. Connect the +ve of the supply via an ammeter to connector pin no. 2. "LFIRE DET FAIL" should show. The current drawn should be between ------mA and ------mA. Disconnect pin number 2 from the +ve of the supply. Indication to cancel.

4.3.4. Connect the +ve of the supply via an ammeter to connector pin no. 3. "R ENG FIRE" should show. The current drawn should be between ------mA and------mA. Disconnect pin number 3 from the +ve of the supply. dication to cancel.

4.3.5. Connect the +ve of the supply via an ammeter to connector pin no. 4. "R FIRE DET FAIL" should show. The current drawn should be between ------mA and ------ mA. Disconnect pin number 4 from the +ve of the supply. Indication to cancel.

4.3.6. Test Switch Functional Test

Connect the -ve of the D.V.M. to connector pin number 12. Depress "FAIL IND. TEST" switch and hold. The voltage indicated on the D.V.M. should be within ------V to ------V. The current drawn should not exceed------ mA. Release switch. Voltage to equal supply. Current to drop to Zero. Disconnect DVM from pin 12.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q5308	
QUALITY CONTROL DATA SHEET	SHEET No. 5	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

4.3.7. Connect the -ve of the D.V.M. to connector pin number 11. Depress "FAIL IND. TEST" switch and hold. Voltage indicated on D.V.M. should be within ----V to ----V. The current drawn should not exceed---- mA. Release the switch. Voltage to equal supply. Current to drop to Zero. Disconnect DVM from pin 11.

4.3.8. Connect the -ve of the D.V.M. to connector pin number 10. Depress the "FIRE DET. TEST" switch and hold. Voltage indicated on the D.V.M should be within ----V to ----V. The current drawn should not exceed ---- mA. Release the switch. Voltage to equal supply. Current to drop to Zero. Disconnect DVM from pin 10.

4.3.9. Connect the -ve of the D.V.M. to connector pin number 9. Depress the "FIRE DET TEST" switch and hold. Voltage indicated on the D.V.M. should be within ----V to ----V. The current drawn should not exceed---- mA. Release the switch. Voltage to equal supply. Current to drop to Zero. Disconnect DVM from pin 9.

4.4. Set the supply to 29v and repeat tests of para. 4.3.2. to 4.3.9.

4.5. Connections for tests para. 4.6. tests.

1) Disconnect the +ve of DC power supply from connector pin number 6.

2) Disconnect the -ve of the DC power supply from connector pin number 5.

3) Connect the +ve of DC power to connector pin number 5.

4) Connect the -ve of DC power supply to connector pin number 6.

5) Connect +ve of D.V.M. to +ve of DC power supply.

6) Set DC supply to 29v.

4.6. Connect -ve of D.V.M. to connector pin 12. Depress "FAIL IND. TEST" Switch, voltage on D.V.M. should not exceed ----V. Disconnect -ve of D.V.M. from pin 12.

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TITLE :

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

4.6.1. Connect +ve of DVM to connector pin number 11. Depress "FAIL IND. TEST" switch. Voltage on DVM should not exceed ----V. Disconnect +ve of DVM from pin 11.

4.6.2. Connect +ve of DVM to connector pin number 10. Depress "FIRE DET. TEST". Voltage on DVM should not exceed ----V. Disconnect +ve of DVM from pin 10.

4.6.3. Connect +ve of DVM to connector pin number 9. Depress "FIRE DET. TEST". Voltage on DVM should not exceed ----V. Disconnect +ve of DVM from pin 9.

4.7. Connections for para 4.8 tests

1) Connect ohmmeter between connector pin number 5 and pin number 14.

4.8. Control Unit Reset Switch Tests

4.8.1. Depress and hold "FAIL IND. TEST" switch. Resistance on ohmmeter should not exceed ----ohm. Release "FAIL IND. TEST" switch.

4.8.2. Disconnect lead from pin 14 and connect to pin 7. Depress and hold "FIRE DET. TEST" and "FAIL IND. TEST" switches. Resistance on ohmmeter should not exceed ----ohm. Release "FIRE DET. TEST" and "FAIL IND. TEST" switches.

4.8.3. Disconnect lead from pin 5 and connect to pin 14. Depress and hold "FIRE DET. TEST" switch. Resistance on ohmmeter should not exceed ----ohm. Release "FIRE DET. TEST" switch.

4.9. Connections for para. 4.10. tests.

1) Remove all connections from connector.

2) Link all connector pins together.

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TITLE : ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

4.10. Insulation Test

Using the 500v DC insulation tester, the resistance measured between all connector pins and case should not be less than ---- megohms.

5. TYPE 2. CUSTOMER RECEIVING TESTS

Tests as Type 1. Para. 4.1. to 4.4.

Note: The limits are given in the schedule of test limits, para. 8.

6. TYPE 3. QUALITY AND FIELD LIMITS

Note: The limits are given in the schedule of test limits para. 8.

6.1. Non-Destructive Tests

The following tests shall be carried out.

6.2. Room Temperature Tests

Type 1 tests para. 4.1. to 4.10. and Type 1 limits apply.

6.3. High Temperature Tests +71°C

Place unit under test in an air circulating temperature chamber. Maintain temperature at +71°C for 3 hrs.
Carry out tests of para. 4.3.2. to 4.3.5. inclusive at 16v and 29v.

6.4. Low Temperature Tests -54°C

Place unit under test in a refrigerated chamber. Maintain temperature at -54°C for 3 hrs. Carry out tests of para. 4.3.2. to 4.3.5. inclusive at 16v and 29v.

6.5. Repeat room temperature tests of para. 6.2.

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TITLE:
ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART A.

6.6. Destructive Tests

The following tests shall be carried out.

6.7. Room Temperature Tests

Type 1 tests para. 4.1. to 4.10. and Type 1 limits apply.

6.8. High Temperature Tests +71°C

The control unit shall be subjected to the high temperature test requirement of MIL-STD-810C, Method 501.1. Procedure 1 for a period of 48 hours. At the end of this time the functional tests of para. 4.3.2. to 4.3.5. should be carried out at 16v and 29v.

6.9. Low Temperature -54°C

The control unit shall be subjected to the low temperature test requirements of MIL-STD-810C. Method 502.1. Procedure 1 for a period of 48 hours. At the end of this time the functional tests of para. 4.3.2. to 4.3.5. should be carried out at 16v and 29v.

7.0. Temperature Shock

The control unit shall meet the temperature shock requirements of MIL-STD-810C Method 503, Procedure 1, and shall be unaffected by rapid transfer between the following temperatures:

-54°C to +71°C.

After this test the control unit should not have sustained any mechanical damage and should meet the requirements of para. 4.1. to 4.10. and room temperature limits at 16v and 29v.

7.1. Vibration

The control unit shall meet the vibration requirements of MIL-STD-810C, Method 514.2. Procedure 1A. The unit shall be subjected to random vibration

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TITLE:
ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART A.

7.1.cont.

in each of 3 mutually perpendicular axes. The test shall be over the frequency range of 15 - 2000 Hz. at the vibration levels and test times detailed in Fig. 514.2-11A and 514.2-2A of MIL-STD-810C.

The unit shall function as required by tests of paras. 4.3.2. to 4.3.5. during and 4.1. to 4.10. after test.

8. Schedule of Tests

PARA.		TYPE 1	TYPE 2	TYPE 3
4.3.2.)				
4.3.3.)				
4.3.4.)	16v	62 mA and 81 mA	59 mA and 84 mA	59 mA and 87 mA
4.3.5.)	29v	93 mA and 112 mA	90 mA and 115 mA	90 mA and 118 mA
4.3.6.)		1.3v to 2.0	1.0v to 2.2	N/A
4.3.7.)	16v	9 mA	10 mA	N/A
4.3.8.)	29v	1.3v to 2.0	1.0v to 2.2	N/A
4.3.9.)		16 mA	17 mA	N/A
4.6.0.)				
4.6.1.)		-0.3v	-0.35v	N/A
4.6.2.)				
4.6.3.)				
4.8.1.		0.025 ohm	0.025 ohm	0.025 ohm
4.8.2.		0.050 ohm	0.050 ohm	0.050 ohm
4.8.3.		0.025 ohm	0.025 ohm	0.025 ohm
4.10.		20 megohms	20 megohms	20 megohms

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5308	
QUALITY CONTROL DATA SHEET	SHEET. No. 10	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

1. EQUIPMENT REQUIRED

DC D.V.M.

A.V.O. Model 8

0.5A 0-30v Variable DC supply.

Ohmmeter

Test Equipment FIG.1 Adapter FIG.2.

2. CONNECTIONS AND SETTINGS

2.1. SW1 and SW2 to OFF.

2.2. SW3 to POS 1

2.3. Connect DVM to DVM Terminals.

2.4. Connect AVO to AVO Terminals

2.5. Set AVO ON 0-100 mA Scale DC.

2.6. Connect Power Supply to 16-29v Terminals.

2.7. Set Supply to 16v

2.8. Turn Supply OFF.

2.9. Connect Unit to Test Set.

3. TEST PROCEDURE

3.1. Turn Power Supply Power ON, LED to Light.

3.2. Set SW2 to 1, L ENG "FIRE" to Light.

3.3. Read Current ----mA. Para. 4.3.2.

3.4. Set SW2 to 2, L.ENG FIRE TO EXTINGUISHER, Left "FIRE DET FAIL" to Light

3.5. Read Current ----mA, Para. 4.3.3.

3.6. Set SW2 to 3, Left "FIRE DET FAIL" to extinguish, R ENG FIRE to Light.

3.7. Read Current ----mA. Para. 4.3.4.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q.53.8	
QUALITY CONTROL DATA SHEET	SHEET No. 11	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

3. TEST PROCEDURE (contd.)

3.8. Set SW2 to 4, 'R.ENG FIRE' To Extinguish, "R.FIRE DET FAIL' to light.

3.9. Read current -----mA, Para. 4.3.5.

3.10. Set SW2 to OFF, 'R .FIRE DET FAIL' to extinguish.

3.11. Set SW1 to 1. Set Avo to 0-100mA range.

3.12. Depress and hold "FAIL IND TEST".

3.13. Read DVM ---- Volts and AVO -----mA, Para. 4.3.6.

3.14. Release "Fail IND TEST".

3.15. Set SW1 to 2.

3.16. Depress and hold 'FAIL IND TEST'.

3.17. Read DVM ---- Volts and AVO ---- mA, Para. 4.3.7.

3.18. Release "FAIL IND TEST".

3.19. Set SW1 to 3.

3.20. Depress and hold "FIRE DET TEST".

3.21. Read DVM ----- Volts and AVO ----- mA, Para. 4.3.8.

3.22. Release "FIRE DET TEST".

3.23. Set SW1 to 4.

3.24. Depress and hold "FIRE DET TEST".

3.25. Read DVM ----- Volts and AVO ---- mA, Para. 4.3.9.

3.26. Set SW1 to OFF.

3.27. Set Power Supply to 29v. Set Avo to 0-1A range.

3.28. Repeat Para. 3.2. to 3.26. Inclusive.

3.29. Set SW3 to 2.

3.30. Set SW1 to 1.

3.31. Depress and hold "FAIL IND TEST".

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q5308	
QUALITY CONTROL DATA SHEET	SHEET No. 12	No. OF SHEETS

TITLE:
ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

3. TEST PROCEDURE (contd.)

3.32. Read DVM ---- Volts. Para 4.6.
3.33. Release "FAIL IND TEST".
3.34. Set SW1 to 2.
3.35. Depress and hold "FAIL IND TEST".
3.36. Read DVM ---- Volts. Para. 4.6.1.
3.37. Release "FAIL IND TEST".
3.38. Set SW1 to 3.
3.39. Depress and hold "FIRE DET TEST".
3.40. Read DVM ---- Volts. Para. 4.6.2.
3.41. Release "FIRE DET TEST".
3.42. Set SW1 to 4.
3.43. Depress and hold "FIRE DET TEST".
3.44. Read DVM ---- Volts. Para. 4.6.3.
3.45. Release "FIRE DET TEST".
3.46. Set SW1 to OFF.
3.47. Set SW3 to 1.
3.48. Set Power Supply OFF.
3.49. Disconnect Unit from Test Set.
3.50. Connect ohmmeter between pin number 5 and pin number 14.
3.51. Depress and hold "FIRE DET TEST".
3.52. Read ohmmeter ---- ohm. Para. 4.8.1.
3.53. Release "FIRE DET TEST".
3.54. Disconnect ohmmeter lead from pin number 14 and connect to pin number 7.
3.55. Depress and hold "FIRE DET TEST" and "FAIL IND TEST".

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5308	
QUALITY CONTROL DATA SHEET	SHEET No. 13	No. OF SHEETS

TITLE:

ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

3. TEST PROCEDURE (cont'd.)

3.56. Read ohmmeter ---- ohms. Para 4.8.2.

3.57. Release "FIRE DET TEST" and "FAIL IND TEST".

3.58. Disconnect ohmmeter lead from pin number 5 and connect to pin number 14.

3.59. Depress and hold "FAIL IND TEST".

3.60. Read ohmmeter ---- ohms. Para 4.8.3.

3.61. Release "FAIL IND TEST".

3.62. Disconnect ohmmeter from unit.

3.63. Connect unit to Adaptor ----

3.64. Connect Megger between case of unit and lead of adaptor.

3.65. Megger insulation resistance to be ------ megohms. Para. 4.10.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. A5308	
QUALITY CONTROL DATA SHEET	SHEET No. 14	No. OF SHEETS 14

TITLE: ACCEPTANCE REQUIREMENTS FOR 53813-202 CREW WARNING UNIT
PART B. PREFERRED GRAVINER TEST PROCEDURE WITH TYPE 1 LIMITS

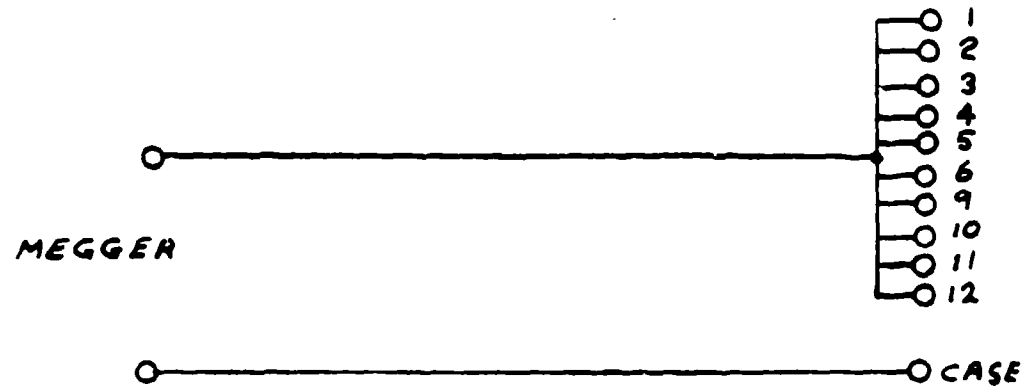

FIG 2

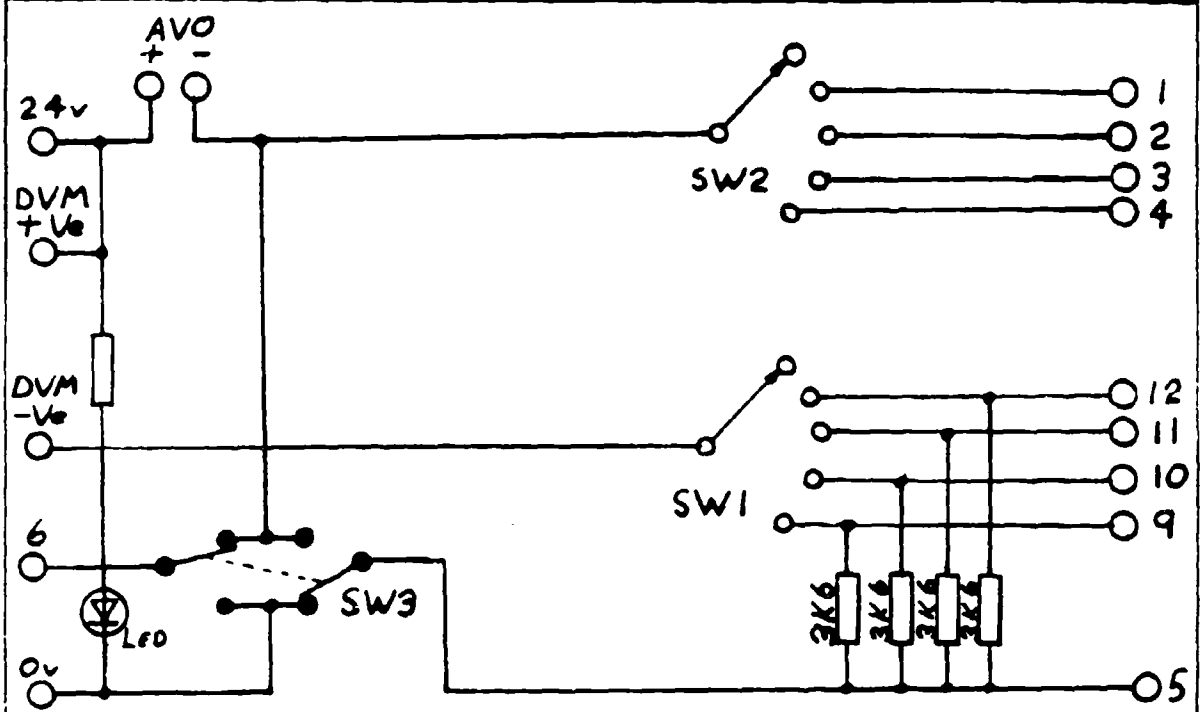

FIG 1

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET. No. 1	No. OF SHEETS 45

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

(i) Definition

Q5309 becomes a master document for function performance testing of Control Unit 53813-203.

Performance values have been defined in compliance with "funnel or tiered tolerances" philosophy and form the following categories.

Type 1 - Factory or Production Acceptance Limits appropriate at normal ambient temperature conditions.

Type 2 - Receiving Inspection or Customer Acceptance Limits appropriate at normal ambient temperature conditions.

Type 3 - Quality or Functional Acceptance Limits appropriate at and between the declared extremes of operating temperatures.

In any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependency, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptable value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any test where a single value remains in the test is applicable to Type 1, 2 and 3 tests.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 2	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

(ii) Frequency of Test

The following tests shall be carried out at a frequency appropriate to definition.

Type 1 All units.

Type 2 It is recommended that all units 'on receipt' and subsequently as defined in users procedures and schedules.

Type 3 These will be carried out as appropriate upon:-

Initiation of production.
Introduction of a major modification.
Cessation of production for three months.
Introduction of new processes which may affect production standard.
Change of key operator.

(iii) Action Required

iii(a) For Type 1 tests all results shall be recorded against Serial No. of each control unit.

For Type 3 tests an abridged test report detailing results obtained against Serial No. of each control unit is raised.

iii(b) For Type 1 tests any failures shall be reported to the Design Authority.

For Type 3 tests, any Control Unit that fails any test or part of a test shall be examined to locate the particular replaceable sub-assembly causing the malfunction.

The defective sub-assembly shall be replaced to eachof two replacement sub-assemblies, and repeat testing carried out on both items.

Subject to satisfactory results on both replacement sub-assemblies, the batch of units can be released.

A failure during re-test on either sub-assembly constitutes a failure of the whole batch, and rectification/design modification is required before the batch can be released.

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GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q5309	
QUALITY CONTROL DATA SHEET	SHEET No. 3	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

NOTES: Control Unit is referred to as CCU.
Crew Warning Unit is referred to as CWU.

1. EQUIPMENT REQUIRED FOR TESTS

Cableform as per Figure 1.

400 Hz power supply (frequency range 380 Hz to 420 Hz)
(voltage range 102V to 124V)

DC supply 2 amp (variable 16 - 30V output)

DC supply 0.5 amp (variable 3 - 4 volts output)

DC supply 0.5 amp (5.6V)

Gould storage oscilloscope OS4000 and 2 x 10 probes.

Resistance Bridge

4 AVO Model 8.

Counter timer capable of being +ve and -ve edge triggered at 5V levels resolving to 0.1 mS on count range of 100 secs.
e.g. Racal Dana 9901 and 1 x 1 probe.

Ground support control box and cable harness assembly as per Fig. 2.
Meter and Supply Switching Unit as per Fig. 12.
Head Simulation Unit as per Fig. 3.

Diode IN4001.

Crew Warning unit part number 53813-202.

Computer Card Golden River Co. GR6243.

Printer, Digitec. Part Number 6410J.

Digital Voltmeter (DC and 400 Hz capability), used in conjunction with insulated probes.

Pulse select unit as per Fig. 11 (calibrated as per Appendix 2)

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

2. CONNECTIONS

Check that all supplies are set to OFF. Connect control unit to supplies and test equipment as per Fig. 4.

3. INITIAL SETTINGS

3.1. S1A, S2A, S3 and S_4 on Meter and Supply Switing Unit to OFF. All 4 meters switch on Meter and Supply Swithing Unit to A.

3.2. Rotary switch on GSE control unit to position 6.

3.3. GSE mode switch to IN.

3.4. Date switch to A.

3.5. Computer card baud rate settings to 30 characters/sec.

3.6. All head simulation unit, F1 (fire and FA fault) switches all to off.

3.7. M1 and M2 set to 1 amp range AC.

3.8. M3 set to 1 Amp range DC.

3.9. M4 set to 10 mA range DC.

3.10. Using DVM set to 200V AC range switch on AC supply and set it to 124V 420 Hz ($\pm$ 0.5V).

3.11. Using DVM set to 50V DC switch on V_1 and set it to 29V ($\pm$0.1V).

3.12. Using DVM set to 10V DC switch on V_2 and set it to 4V ($\pm$ 0.1V).

3.13. Using DVM set to 10V DC range, disconnect positive lead to V_3 supply. Switch on V_3, set it to 5.6V ($\pm$ 0.2V). Switch off V_3 and reconnect positive lead.

3.14. Head select switch on Pulse Simulation unit to OFF.

4. TEST PROCEDURE

Notes: 1) Meter M4 should be observed at each test and unless stated otherwise should read zero current.

2) Limits of all tests are contained in Appendix 1.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4. TEST PROCEDURE (contd.)

4.1. Earthing Connections

With CCU disconnected, using resistance bridge, check resistance between CCU case and pin 15 of A/C plug, resistance to be less than-----ohms.

4.2. Preliminary Check Out (High Supply Voltages)

4.2.1. Connect A/C and GSE cable forms to CCU as per Fig. 4. Switch S4 to on. M4 should read less than --------mA.

Switch S3 to on. M3 should read less than -------- mA.

CWU left hand 'FIRE DETECT FAIL' lamp to illuminate.

4.2.2. Set S1A and S2A to on. Note, S1A and S2A should be switched within 1 second of each other. Observe that GSE 1 LEDS on side 1 and side 2 of Ground Support Control Unit (GSE CU) indicates.

M1 to indicate less than -------- mA.

M2 to indicate less than -------- mA.

M3 to indicate less than -------- mA.

M4 to indicate zero mA.

4.3. Preliminary Check Out

4.3.1. Set GSE CU mode switch to OUT, depress and release reset switch, observe that GSE 1 LEDS on GSECU flash alternately at a rate of approximately 3 per second. GSE 2 LEDS should flash alternately approximately once every 15 seconds.

Observe that CWU left hand lamps i.e. 'L ENG.FIRE' and 'FIRE DETECTOR FAIL' lamps are both extinguished.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.3.2. Depress 'FIRE DETECT TEST' push button on CWU, 'L ENG FIRE' lamp to indicate within approximately one second.

Release 'FIRE DETECT TEST' push button on CWU, 'L ENG FIRE' lamp to extinguish within approximately one second.

Depress 'FAIL IND. TEST' push button on CWU, left hand 'FIRE DETECT FAIL' lamp to show.

Release 'FAIL IND. TEST' push button on CWU, left hand 'FIRE DETECT FAIL' lamp to extinguish.

4.4. Supply Currents - Running Mode

M1 and M2 to indicate less than -------- mA.
Note: Meter needle will fluctuate in sympathy with time share. Observe average value.

M3 to indicate less than -------- mA.

M4 to indicate zero.

4.5. Supply Currents - Fire Mode

Depress and hold CWU Fire Test button, when 'L ENG FIRE' lamps show, observe meter readings.

M1 and M2 should read less than -------- mA.

M3 should read less than -------- mA.

M4 should read zero.

Release CWU fire test button.

4.6. Preliminary Check Out (Low Supply Voltages)

Set switches S1A/S2A, S3 and S4 to OFF.

Set GSE mode switch on GSECU to IN.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.6. Preliminary Check Out (Low Supply Voltages) (contd.)

Repeat 4.2 to 4.5. inclusive with power supply settings as follows:-

Using DVM set

AC supply to 102 volts 380 Hz (± 0.5V)

V1 supply to 16 volts DC (± 0.2V)

V2 supply to 3 volts DC (± 0.1V)

Repeat 4.2 to 4.6 inclusively, then set S1A/S2A, S3 and S4 to OFF.

4.7. Regulation Operation

Note: All DC voltages are measured with respect to pin 32 of monitoring points.

4.7.1. Settings (Low Supply)

Using DVM set

V1 to 28 volts DC (± 0.2V)

Set V2 to 3.6 volts DC (± 0.1V)

Set GSE mode switch on GSECU to IN.

4.7.2. Set switches S1A/S2A, S3 and S4 to ON.

4.7.3. Regulation at low supply (5.6V rail) side 1.

With DVM set at 10V range DC, check voltage at pin 12 of monitoring points. Voltage to be between -------- volts minimum and -------- volts maximum.

4.7.4. Regulation at low supply (5.6V rail) side 2.

Repeat 4.7.3. with DVM connected to pin 18 of monitoring point.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.7.5. Regulation at low supply (head supply) side 1.

BEWARE OF HIGH VOLTAGE ON THESE TERMINALS.

Set DVM on 500V DC range. Check voltage at pin 25 of monitoring point, voltage to be between -------- volts minimum and --------- volts maximum.

4.7.6. Regulation at low supply (head supply) side 2.

Repeat 4.7.5. with DVM connected to pin 39 of monitoring point.

Set switches S1A/S2A, S3 and S4 to OFF.

4.7.7. Settings (High Supply)

Using DVM set AC supply to 124V 420 Hz. Repeat 4.7.2. to 4.7.6 inclusively.

4.8. Timing Tests

4.8.1. Settings for Power Up Time Delay

With Switches S1A/S2A, S3 and S4 to OFF set

AC supply to 400 Hz 115V ($\pm$ 0.5V).

Set oscilloscope time base to 0.2 secs/cm, channel 1 and 2 amps. to 0.2V cm triggering to positive edge channel 1. Set stored trigger point to $\frac{3}{4}$ trace.

Set channel 1 and 2 to DC mode.

Set storage mode to ROLL.

Set GSE mode switch to IN.

Switch on oscilloscope and adjust it such that channel 1 trace is at mid screen and channel 2 is $\frac{1}{2}$ cm above bottom of screen.

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TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.8.2. Connections for Power Up Time Delay

Connect CH1 to terminal block monitoring point 23.
Connect CH2 probe to terminal block monitoring point 12.

All probe returns are connected to pin 32 of monitoring point.

4.8.3. Power Up Time Delay (Side 1)

4.8.3.1. With oscilloscope trigger armed switch on system power in the order S3 and S4, S1A/S2A observe waveform as per Fig. 5.

Note: If oscilloscope does not trigger, adjust trigger level in conjunction with setting S1A, S2A to off, re-arming trigger and setting S1A/S1B back to ON.

Measure time delay between rising edge of channel 1 and 2 as shown in Fig. 5.
Set S1A/S2A, S3 and S4 to OFF.

4.8.3.2. Power up Time Delay (Side 2)

Repeat 4.8.3.1. but with Channel 1 probe connected to terminal block monitoring point 41 and Channel 2 probe connected to monitoring point 18.
Remove oscilloscope probes from monitoring point.

4.8.4. Settings for Time Share Timing

Switch on timer counter.

Set GSE mode switch to OUT.

Set timer for positive edge start, positive edge stop such that 500 mS can be measured.

4.8.5. Connections for Time Share Timing

Connect timer probe to monitoring point pin 23.

Probe return connected to monitoring point pin 32.

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CKD					207				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.8.6. Side 1 Time Share

4.8.6.1. Set S1A/S2A, S3 and S4 to ON.

System to function as per 4.3.1.

4.8.6.2. Observe period of timer, time to be between --------secs. minimum and --------secs maximum.

4.8.6.3. Re-select for negative edge stop and read timer. Time to be --------secs. minimum and -------- secs. maximum.

4.8.7. Side 2 Time Share

Repeat 4.8.6. with timer probe connected to monitoring point 41.

4.8.8. Connections and settings for Self Test Timer

Connect timer probe to monitoring point pin 3.
Select timer for positive edge start, positive edge stop. Select timer range to cover a 20 second period.

4.8.9. Side 1 Self Test Timing (Period)

Observe period of timer, time to be between -------- secs. minimum and -------- secs. maximum.

4.8.10. Side 1 Self Test Timing (Duration)

Reselect timer for positive edge start, negative edge stop and observe period of timer. Time to be between -------- secs. minimum and -------- secs. maximum.

4.8.11. Side 2 Self Test Timing

Repeat 4.8.8. to 4.8.10. but with timer probe connected to monitoring point pin 6.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					208				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.8.11. Side 2 Self Test Timing (contd.)

Remove timer probe from monitoring point.

4.9. Ground Support Voltage Lines

Note: All DC voltages are monitored with respect to pin 32 of monitoring point.

4.9.1. Settings

With power on from previous test, GSE mode switch on GSECU to IN.
Depress and release reset button on GSECU.
Observe that GSE1 LEDS on side 1 and 2 light.

4.9.2. System Definition Connection

With DVM set on 10V DC range, check voltage at pin 27 of monitoring points, voltage to be between -------- volts minimum and -------- volts maximum.

4.9.3. Battery Monitoring Point

With DVM set to 10V range check voltage at pin 37 of monitoring point, voltage to be between -------- volts minimum and -------- volts maximum.

4.9.4. 115V Feeds to GSE (Side 1)

BEWARE OF HIGH VOLTAGE ON THESE TERMINALS.

Set DVM to 200V AC range and connect probes to pins 10 and 11 of monitoring point.

Observe DVM reading between -------- volts maximum and -------- volts minimum. Set S2A to OFF and observe that DVM voltage does not change.
Return S2A to ON.

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.9.5. 115V Feeds to GSE (Side 2)

BEWARE OF HIGH VOLTAGE ON THESE TERMINALS

Set DVM to 200V AC range and connect probes to pins 19 and 20 of monitoring points.

observe DVM reading, voltage to be between -------- volts maximum and -------- volts minimum.
Set S1A to OFF and observe that DVM voltage does not change.
Return S1A to ON.

4.10. Check Point Monitoring

4.10.1. Settings and Connections

Set GSE mode switch to OUT on GSECU.
Depress and release reset switch on GSECU.
Set DVM to 50 volt range DC.
Connect DVM positive to pin 28 and negative to pin 32 of monitoring point.

4.10.2. Check Point 1

DVM reading to be zero.

Depress 'FIRE DETECT TEST' push button, 'LEFT ENG. FIRE' lamp to indicate, DVM reading to be between -------- volts minimum and ;-------- volts maximum.
Release 'FIRE DETECT TEST' push button.

4.10.3. Check Point 2

Repeat 4.10.2. with DVM positive connected to pin 29 of monitoring points.

4.10.4. Check Point 3

Connect DVM to pin 35 of monitoring points.
DVM reading to be zero volts.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					21C				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.10.4. Check Point 3 (contd.)

Depress 'FAIL IND. TEST' push button, left 'FIRE DETECT FAIL' indication to show.
Observe DVM reading, voltage to be between -------- volts minimum and -------- volts maximum.

.5. Check Point 4

Repeat 4.10.4. with DVM connected to pin 36 of monitoring point.

4.11. Ground Support Controlled Tests

4.11.1. RAM Test and Reset

Set GSE Mode switch on GSECU to IN.
Depress and release reset switch on GSECU.
Observe that side 1 and side 2 GSE1 LEDS on GSECU light.

4.11.2. Common Logic Test (Functional)

Select position 4 on rotary switch, depress and release reset button.
Observe that GSE1 and 2 LEDS on GSECU flash on and off in the following sequence:

GSE 2 side 1 (ON-OFF), GSE1 side 1 (ON), GSE2 side 1 (ON).

GSE2 side 2 (ON-OFF), GSE1 side 2 (ON), GSE2 side 2 (ON).

Repeat depression and release of reset button, observe that 'L ENG.FIRE' and left hand 'FIRE DETECT FAIL' lamps do not flash on during the period that GSE LEDS are active.
Set S1A/S2A, S3 and S4 to OFF.

4.11.3. Common Logic Test (Timing)

4.11.3.1. Connections and Settings

Set oscilloscope channels 1 and 2 amps to 0.2V/cm.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					211				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.11.3.1. Connections and Settings (contd.)

Set trigger to CH1 (positive edge).

Set display mode to ROLL.

Set time base to 0.1 secs/cm.

Set "stored" trigger point to ½ trace.

Connect channel 1 probe to pin 23 of monitoring point.

Connect channel 2 probe to pin 3 of monitoring point.

Connect probe return lines to pin 32 of monitoring point.

4.11.3.2. Side 1 Timing of Common Logic Test

Set S1A/S2A, S3 and S4 to ON.
Depress and hold reset button on GSECU.
Arm oscilloscope trigger and release reset button 2 seconds later.

Waveform to be as Fig. 6.

Note: If oscilloscope does not trigger adjust trigger level in conjunction with depressions of GSECU reset switch and rearming of oscilloscope trigger.

Take measurements of t1 and t2.
Set S1A/S2A, S3 and S4 to OFF.

4.11.3.3. Side 2 Timing of Common Logic Test

Connect channel 1 probe to pin 41 of monitoring point.

Connect channel 2 probe to pin 6 of monitoring point.

Repeat 4.11.3.2.

4.11.3.4. Inter Channel Timing (Connections)

Connect channel 1 probe to pin 23 of monitoring point.

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.11.3.4 Interchannel Timing (Connections) (Contd.)
Connect channel 2 probe to pin 41 of monitoring point.
Set time base to 0.5 secs/cm. Set 'stored trigger' point to ½ scale.

4.11.3.5 Interchannel Timing
Set S1A/S2A, S3 and S4 to ON. Arm oscilloscope trigger.
Depress and hold reset button on GSECU for 5 seconds.
Release reset button on GSECU.
Waveform to be as Fig.7. take measurement t.
Remove oscilloscope probes.

4.11.4. Background Programme Test
Select position 5 on GSECU rotary switch.
Depress and release reset button.
After 5 seconds no LEDS to show on GSECU.

4.11.5. Idle Programme Test.
Select position 0 on GSECU rotary switch.
Depress and release reset button.
Observe that side 1 and side 2 GSE1 and 2 LEDS on GSECU show.

4.11.6. Data Retention Test.
Set S4 to OFF. Select position 2 on GSECU rotary switch.
Depress and release reset button.
Observe that side 1 and side 2 GSE1 LEDS on GSECU light.
Select position 3 on GSECU rotary switch, depress and release reset button.
Observe that side 1 and side 2 GSE1 and GSE2 LEDS on GSECU light.
Reselect position 2 on GSECU rotary switch, depress and release reset button.
Observe that Side 1 & 2 and GSE1 LED's on GSECU light.
Set S1A/S2A and S3 to OFF. Wait 30 seconds.
Select position 3 on GSECU rotary switch.
Set S1A/S2A and S3 to ON.
Observe that only side 1 and 2 GSE 1 LEDS on GSECU Light.

ISSUE	A								
MOD									
COMPILED	PS								
CKD									
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.11.6. Data Retention Test (contd.)

Reselect position 2 on GSECU rotary switch.
Set S4 to ON.

Depress and release reset button on GSECU. Observe that only side 1 and side 2 GSE1 LEDS on GSECU light.
Set S1A/S2A and S3 to OFF. Wait 30 seconds.

Select position 3 on GSECU rotary switch. M4 to read less than -------- mA maximum.
Set S1A/S2A and S3 to ON. Observe that side 1 and 2 GSE1 and GSE 2 LEDS on GSECU light.

4.11.7. Data Readout Test

4.11.7.1. Side 1 Test

Switch on V3 (supply to computer card).
Switch on mains power to printer.

Select position 2 on GSECU rotary switch.

Depress and release reset switch on GSECU.

Observe that side 1 and side 2 GSE1 LEDS on GSECU light.

Select position 1 on GSECU rotary switch.
Depress and hold reset switch on GSECU.
Depress and release S5.

Observe that printer prints --------.

Release reset switch on GSECU.

Printer should print as Fig. 8.

When printer stops observe that GSE1 LEDS (side 1 and 2) on GSECU light.

4.11.7.2. Side 2 Test

Repeat 4.11.7.1. test but with GSECU data switch set to 8.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					214				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q3308	
QUALITY CONTROL DATA SHEET	SHEET No. 17	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12. System Functional Tests

All fire and fault indications refer to 'L ENG.FIRE' and left hand 'FIRE DETECT FAIL' lamps on CWU.

Note: These tests are carried out using the head simulation unit referred to as HSIMU.

All references to side 1 fault and fire switches refer to System A side 1. System B fault and fire switches are not used.

4.12.1. Initialise for Functional Tests

With system still powered from previous tests, select position 6 on rotary switch of GSECU.

Set GSE mode switch to OUT.

Depress and release reset switch on GSECU. Observe that system functions as per 4.3.1.

4.12.2. Check for No Faulty Head Drive Circuits

Set all side 1 fire switches to ON. CWU fire lamp should remain off.

Set all side 1 fire switches to OFF. Set all side 2 fire switches to on. CWU fire lamp should remain OFF.

Set all side 2 fire switches to OFF.

4.12.3. 'ANDED' Head Operation

Set heads 5, 6 and 7 fault switches, sides 1 and 2 on HSIMU to ON. These to remain on for all subsequent functional tests of para. 4.12.

Note: Switch positions 0 - OFF 1 -ON.

Carry out ANDED TESTS according to sequence as follows, and observe CWU fire lamp status as shown.

ISSUE	A								
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APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.3. 'ANDED' Head Operation (contd.)

	SIDE 1 HEAD FIRE SWITCHES					SIDE 2 HEAD FIRE SWITCHES					CWU FIRE LAMP
	8	4	3	2	1	8	4	3	2	1	
1)	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	0	0	0	0
	0	0	0	0	1	0	0	0	0	1	1
	0	0	0	0	0	0	0	0	0	1	1
	0	0	0	0	0	0	0	0	0	0	0
2)	0	0	0	1	0	0	0	0	0	0	0
				1					1		1
				0					1		1
				0					0		0
3)			1					0			0
			1					1			1
			0					1			1
			0					0			0
4)		1					0				0
		1					1				1
		0					1				1
		0					0				0

ISSUE	A								
MOD									
COMPILED	PS								
CKD					216				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S CONTROL UNIT 53813-203 (SYSTEM A)

4.12.3. (contd)

	SIDE 1 HEAD FIRE SWITCHES					SIDE 2 HEAD FIRE SWITCHES					CWU FIRE LAMP
	8	4	3	2	1	8	4	3	2	1	
5)	1					0					0
	1					1					1
	0					1					1
	0					0					0
6)				0					0		0
				1					0		0
				1					1		1
				0					1		1
				0					0		0
7)					1					0	0
					1					1	1
					0					1	0
					0					0	0
8)			1					0			0
			1					1			1
			0					1			0
			0					0			0
9)		1						0			0
		1						1			1
		0						1			0
		0						0			0
10)	1						0				0
	1						1				1
	0						1				0
	0						0				0
11)		1				0					0
		1				1					1
		0				1					0
		0				0					0

Note: All unmarked positions are assumed to be "0".

ISSUE	A										
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COMPILED	PS										
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APP											

TITLE : ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.3. (Cont.)

	SIDE 1 HEAD FIRE SWITCHES						SIDE 2 HEAD FIRE SWITCHES					CWU FIRE LAMP
	8	4	3	2	1		8	4	3	2	1	
12)					1				1			0
13)			1								1	0
14)					1			1				0
15)		1									1	0
16)					1		1					0
17)	1										1	0
18)			1					1				0
19)		1							1			0
20)			1				1					0
21)	1								1			0
22)	0	0	0	0	0		0	0	0	0	0	0

Note: All unmarked positions are assumed to be '0'

4.12.4. 'ORED' Head Operation Side 1

4.12.4.1. Set all side 2 head fault switches to ON.

Depress and release GSECU reset switch and observe that CWU fault indication does not light after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

ISSUE	A									
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COMPILED	PS									
CKD					218					
APP										

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.4.2. Set side 1 head 1 fireswitch to ON.

Fire indication on CWU to show.

Set side 1 head 1 fire switch to OFF.

Fire indication on CWU to extinguish.

4.12.4.3. Repeat 4.12.2.2. for heads 2, 3, 4 and 8.

4.12.4.4. Return side 2 fault switches 1, 2, 3, 4 and 8 to OFF.

4.12.5. 'ORED' Head Operation Side 2

4.12.5.1. Set all side 1 fault switches to ON.

Depress and release GSECU reset switch, observe that CWU fault indication does not light after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

4.12.5.2. Set side 2 head 1 fire switch to ON.

Fire indication on CWU to show.

Set side 2 head 1 fire switch to OFF.

Fire indication on CWU to extinguish.

4.12.5.3. Repeat 4.12.5.2. for heads 2, 3, 4 and 8.

4.12.5.4. Return side 1 fault switches 1, 2, 3, 4 and 8 to OFF.

4.12.6. Failed Heads

Set side 1 and side 2 heads 1, 3 and 4 fault switches on H SIMU to ON.

Observe that left hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE1 (side 1 and 2) LEDS flashing on GSECU.

Set side 1 and 2 heads 1, 3 and 4 fault switches on HSIMU to OFF.
Set side 1 & 2 heads 2 & 8 fault switches on HSIMU to ON.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					2/9				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.6. Failed Heads (contd.)

Observe that left hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE2 (side 1 and side 2). LEDS flashing on GSECU.

4.12.7.

4.12.7.1. Heads 1 and 2 adjacency Set

Set all side 1 and 2 fire and fault switches to OFF.

4.12.7.2. Set GSE mode switch on GSECU to IN.

Depress and release reset button.
Left hand 'FIRE DETECT FAIL' lamp to be OFF.
Observe that side 1 and side 2 GSE1 LEDS on GSECU are lit.

Set head 1 and 2 fault switches on side 1 and side 2 to ON.

Set GSE mode switch on GSECU to OUT.

Depress and release reset button.

Left hand CWU 'FIRE DETECT FAIL' lamp should light immediately after the first occurrence of GSE2 (side 1 and 2) LEDS flashing on GSECU.

Set head 1 and 2 fault switches on side 1 and side 2 to OFF.

After the occurrence of the next flashing sequence of GSE 2 LEDS (occurring approximately once every 15 seconds) observe that left hand 'FIRE DETECT FAIL' lamp does not extinguish.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					220				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.7.3. Heads 2 and 3 Adjacency Set

Repeat 4.12.7.2. using heads 2 and 3 fault switches.

4.12.7.4. Heads 4 and 8 Adjacency

Repeat 4.12.7.2. using head 4 and 8 fault switches.

4.12.7.5. Set GSE mode switch to IN. Depress and release reset switch.
Observe that GSE1 LEDS on side 1 and side 2 of GSECU light.
'FIRE DETECT FAIL' lamp on CWU to be extinguished.

4.12.8. Sensitivity and Short Circuit Head Operation

4.12.8.1. Set Up for Side 1 Heads

Set all side 1 fault switches to OFF.

Set all side 2 fault switches to ON.

Set side 1 and 2 fire switches to OFF.

Set SIDE SELECT on pulse select unit (PSU) to side 1A.

Set HEAD SELECT switch on PSU to head 1.

Set PULSE SELECT switch on PSU to 0.

Set GSE mode switch on GSECU to OUT.

Depress and release reset switch on GSECU.

Observe that system functions as per 4.3.1.

4.12.8.2. Fire Set (Head 1, Side 1)

Note: Allow 2 seconds at each switch position before observing result on CWU.

Set PULSE SELECT switch on PSU to 1.

Observe that fire indication on CWU is not lit.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					221				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.8.2. Fire Set (Head 1, Side 1) (contd.)

Set PULSE SELECT Switch on PSU to 2.

Observe that fire indication on CWU is not lit.

Set PULSE SELECT siwtch on PSU to 3.

Observe that fire indication on CWU is not lit.

Set PULSE SELECT switch on PSU to 4.

Observe that fire indication on CWU is lit.

4.12.8.3. Short circuit (Head 1, Side 1)

Depress and hold short circuit button on sensitivity test unit.

Observe that fire indication on CWU extinguishes.

Release short circuit button on PSU.

Observe that fire indication on CWU re-lights.

4.12.8.4. Fire Reset (Head 1, Side 1)

Set PULSE SELECT switch on PSU to 3.

Observe that fire indication on CWU remains lit.

Set PULSE SELECT switch on PSU to 2.

Observe that fire indication on CWU remains lit.

Set PULSE SELECT switch on PSU to 1.

Observe that fire indication on CWU extinguishes.

Return PULSE SELECT switch on PSU to 0.
Observe that fire indication on CWU remains extinguished.

4.12.8.5. Sensitivity and Short Circuit Head Operation (Side 1, Heads 2, 3, 4, and 8)

Repeat 4.12.8.2. to 4.12.8.4. for heads 2, 3, 4 and 8 by selecting required head on HEAD SELECT switch on PSU.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					222				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.8.6. Set Up for Side 2 Heads

Set all side 2 fault switches to OFF.

Set all side 1 fault switches to ON.

Set SIDE SELECT on PSU to side 2A.

Set HEAD SELECT on PSU to head 1.

Set PULSE SELECT on PSU to 0.

4.12.8.7. Fire Set (Head 1, Side 2)

Repeat 4.12.8.2.

4.12.8.8. Short Circuit (Head 1, Side 2)

Repeat 4.12.8.3.

4.12.8.9. Fire Reset (Head 1, Side 2)

Repeat 4.12.8.4.

4.12.8.10. Sensitivity and Short Circuit Head Operation (Side 2, Heads 2,3,4, and 8)

Repeat 4.12.8.2. to 4.12.8.4. for heads 2, 3, 4 and 8 by selecting required head on HEAD SELECT switch on PSU.

4.12.8.11. Return HEAD SELECT switch on PSU to OFF.

4.12.9. 115V Power Failure

4.12.9.1. Set all side 1 and side 2 head FIRE AND FAULT switches to OFF. Depress and release reset switch on GSECU.

Observe that system is functional as per paras. 4.3.1. and 4.3.2.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					22.3				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 83813-203 (SYSTEM A)

4.12.9.2. Side 1 Power Failure

Set S1A to OFF.

Observe that GSE 1 and 2, side 1 LEDS on GSECU extinguish.

GSE 1 and 2, side 2 LEDS continue to flash as per 4.3.1.

Carry out functional test as per 4.3.2.

Set side 2, head 1 fire switch to ON.

Observe that CWU fire lamp is lit.

Set side 2, head 1 fire switch to OFF.

Observe that CWU fire lamp extinguishes.

Set S1A to ON.

Side 2, GSE 1 and 2 LEDS to continue flashing as per 4.3.1.

Side 1, GSE 2 LED to show continuous.

4.12.9.3. Set Up for Side 2 Power Failure

Set GSE mode switch on GSECU to IN.

Depress and release reset switch.

Observe that both side 1 and side 2 GSE 1 LEDS ON GSECU light.

Set GSE mode switch on GSECU to OUT.

Depress and release reset switch.

Observe that system operates as per 4.3.1.

4.12.9.4. Side 2 Power Failure

Set S2A to OFF.

Observe that GSE1 and 2 Side 2 LEDS on GSECU

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.9.4. Side 2 Power Failure (contd.)

extinguish.

GSE 1 and 2, side 1 LEDS continue to flash as per 4.3.1.

Carry out functional test as per 4.3.2.

Set side 1 head 1 fire switch to ON.

Observe that CWU fire lamp is lit.

Set side 1 head 1 fire switch to OFF.
CWU fire lamp to extinguish.
Set S2A to ON.

Side 1 GSE 1 and GSE 2 LEDS to continue flashing as per 4.3.1.

Side 2 GSE 2 LED to show continuous.

Set S1A/S2A, S3 and S4 to OFF.

4.12.10. Response to Fire

4.12.10.1. Settings and Connections

Set Channel 1 and Channel 2 amplifiers on oscilloscopes to 20V/cm.
Connect Channel 1 oscilloscope probe to side 1 ED terminal of HSIMU, and Channel 2 oscilloscope probe to side 2 ED terminal of HSIMU.

Connect probe return lines to pin 32 of monitoring point.

Connect pin 28 of monitoring point to external trigger input of oscilloscope using a X1 probe.

Set oscilloscope trigger mode to EXT. (positive edge).

Set trigger point at end of trace ensuring that end trace coincides with end of trace graticule.

Set time base to 0.2 secs/cm.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					25				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

4.12.10.1. Settings and Connections (contd.)

Set S1A/S2A, S3 and S4 to ON. Observe that system functions as per 4.3.1.

4.12.10.2. Response to Fire (Set)

Note: To ensure correct results this test should be carried out about 3 seconds after GSE 2 LEDS on GSECU on both sides 1 and 2 have flashed.

With oscilloscope trigger armed, depress and hold 'FIRE DETECT TEST' on CWU.

Note: If oscilloscope does not trigger, adjust trigger level in conjunction with repeat depressions of 'FIRE DETECT TEST' push button, and re-arming of trigger.

Waveform should be of the form of Fig. 9.
Measure fire set time t.

4.12.10.3. Response to Fire (Reset)

Note: To ensure correct results this test should be carried out about 3 seconds after GSE2 LEDS on GSECU on both sides 1 and 2 have flashed.

Select negative edge EXT trigger.

Re-arm oscilloscope trigger.

Release 'FIRE DETECT TEST' switch on CWU.

Observe oscilloscope waveform, trace to be of the form as Fig. 10.

Measure fire reset time t.

4.12.10.4. Switch Off

Set S1A, S2A, S3 and S4 to OFF. Remove oscilloscope probes. Switch off all power supplies. END OF TEST.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					226				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. 05309	
QUALITY CONTROL DATA SHEET	SHEET No. 29	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS — APPENDIX 1

Test Definition	Category	Parameter Values								Units
4.1.	1	0.2 max								Ohms
	2	0.25 max								
	3	0.3 max								
		Values at AC Supply = 124V 420 Hz V1 = 29V V2 = 4V				Values at AC Supply = 102V 380 Hz V1 = 16V V2 = 3V				
		M1	M2	M3	M4	M1	M2	M3	M4	
4.2.1.	1	-	-	140	1.25	-	-	100	1.1	mA
	2	-	-	148	1.45	-	-	106	1.3	
	3	-	-	160	1.65	-	-	115	1.55	Max.
4.2.2.	1	140	140	85	0	115	115	45	0	mA
	2	150	150	89	0	123	123	47	0	
	3	165	165	97	0	135	135	52	0	Max.
4.4.	1	121	121	75	0	100	100	42	0	mA
	2	129	129	80	0	107	107	45	0	
	3	142	142	86	0	117	117	48	0	Max.
4.5.	1	146	146	270	0	118	118	176	0	mA
	2	156	156	280	0	126	126	185	0	
	3	171	171	295	0	138	138	198	0	Max.
		Values at AC Supply = 102V 380 Hz				Values at AC Supply = 124V 420 Hz				
4.73 4.74	1	5.7 ± 0.45				5.7 ± 0.45				Volts
	2	5.7 ± 0.5				5.7 ± 0.5				
	3	5.7 ± 0.65				5.7 ± 0.65				
4.75 4.76	1	322 ± 10				322 ± 10				Volts
	2	322 ± 12				322 ± 12				
	3	322 ± 17				322 ± 17				

ISSUE	A									
MOD										
COMPILED	PS									
CKD					227					
APP										

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS (contd.) APPENDIX 1

Test Definition	Category	Parameter Values		Units
4.8.3.1. 4.8.3.2.	1	0.63 ± 0.42		Seconds
	2	0.63 ± 0.47		
	3	0.63 ± 0.52		
		Side 1	Side 2	
4.8.6.2.	1	337 ± 17	337 ± 17	mS
	2	337 ± 20	337 ± 20	
	3	337 ± 23	337 ± 23	
4.8.6.3.	1	168 ± 9	168 ± 9	mS
	2	168 ± 11	168 ± 11	
	3	168 ± 13	168 ± 13	
4.8.9.	1	14.8 ± 0.74	14.8 ± 0.74	seconds
	2	14.8 ± 0.88	14.8 ± 0.88	
	3	14.8 ± 1.03	14.8 ± 1.03	
4.8.10.	1	168 ± 9	168 ± 9	mS
	2	168 ± 11	168 ± 11	
	3	168 ± 13	168 ± 13	
4.9.2.	1	5.7 ± 0.45		Volts
	2	5.7 ± 0.5		
	3	5.7 ± 0.65		
4.9.3.	1	5.1 ± 0.6		Volts
	2	5.1 ± 0.68		
	3	5.1 ± 0.85		
4.9.4.	1	114.9 ± 0.6		Volts
	2	114.9 ± 0.7		
4.9.5.	3	114.9 ± 0.8		

ISSUE	A									
MOD										
COMPILED	PS									
CKD					228					
APP										

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-203 (SYSTEM A)

SCHEDULE OF TESTS (contd.) APPENDIX 1

Test Definition	Category	Parameter Value		Units
4.10.2. 4.10.3. 4.10.4. 4.10.5.	1 2 3	27.5 ± 0.7 27.4 ± 0.9 27.2 ± 1.2		Volts
		t1	t2	
4.11.3.2. 4.11.3.3.	1 2 3	0.39 ± 0.035 0.39 ± 0.040 0.39 ± 0.050	0.39 ± 0.035 0.39 ± 0.040 0.39 ± 0.050	seconds
4.11.3.5.	1 2 3	1.9 ± 0.5 1.9 ± 0.6 1.9 ± 0.8		seconds
4.11.6.	1 2 3	1.2 max 1.35 max 1.6 max		mA
4.11.7.1.	1) 2) 3)	GRUTIL V.4.		-
4.12.10.2	1 2 3	1.15 ± 0.1 1.15 ± 0.12 1.15 ± 0.15		seconds
4.12.10.3	1 2 3	0.68 ± 0.05 0.68 ± 0.06 0.68 ± 0.08		seconds

ISSUE	A								
MOD									
COMPILED	PS								
CKD					229				
APP									

GRAVNER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. 0.5309	
QUALITY CONTROL DATA SHEET	SHEET No. 32	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

APPENDIX 2

CALIBRATION OF PULSE SIMULATION BOX

1.0. EQUIPMENT REQUIRED FOR TESTS

28 V D.C. SUPPLY (0·5 AMP.).
2 x OSCILLISCOPE PROBES (x10)
STORAGE OSCILLISCOPE (GOULD OS 4000 OR SIMILAR)
PULSE SIMULATION BOX
NORMALLY OPEN BIAS SWITCH

2.0. CONNECTIONS

CONNECT AS PER FIG. A

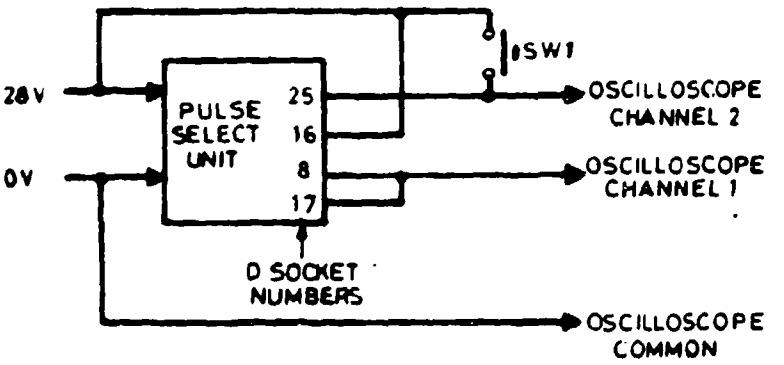


FIG. A

3.0. PULSE CHARACTERISTICS

3.1. SETTINGS

SET 28V D.C. SUPPLY TO 28V
SET CHANNEL 1 Y AMP TO 1V/cm.
SET CHANNEL 2 Y AMP TO 2V/cm.
SET TRIGGER TO CHANNEL 1 NEGATIVE EDGE.
SET "STORED TRIGGER POINT" TO 1/4 SCALE.
SET TIME BASE TO 0·1 mS/cm.
SET PULSE SIMULATION BOX PULSE SELECT SWITCH TO 4.
SET OSCILLOSCOPE STORAGE MODE TO ROLL.
SWITCH ON OSCILLOSCOPE.
SET CHANNEL 1 TRACE TO BE AT MID SCREEN.
SET CHANNEL 2 TRACE TO BE 1cm ABOVE BOTTOM OF SCREEN.

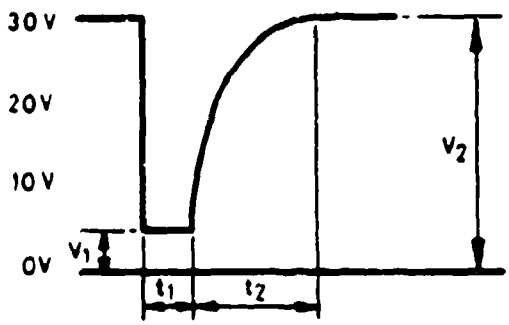
ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					230				
APP									

GRAVINER LIMITED. COLNBROOK. ENGLAND.	DATA SHEET No. Q5309	
QUALITY CONTROL DATA SHEET	SHEET No. 33	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

3.2. PULSE CHARACTERISTICS MEASUREMENT

SWITCH ON 28V SUPPLY. ARM OSCILLOSCOPE TRIGGER. REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH SW1 WHILST ADJUSTING TRIGGER LEVEL UNTIL WAVE FORM OF FIG. B IS OBSERVED. NOTE OSCILLOSCOPE SHOULD BE RE-ARMED AFTER EACH SWITCH DEPRESSION.



V1 MAX.= 10V
V_1 MIN. = 2V
V_2 MAX.= 30V
V_2 MIN. = 26V
t_1 MAX.= 300μS
t_1 MIN.= 50μS
t_2 MAX.= 800μS
t_2 MIN. = 100μS

FIG. B

WAVE FORM SHOULD BE WITHIN THE LIMITS OF FIG. B AS SHOWN.

4.0. NUMBER OF PULSES

4.1. SETTINGS

SET TRIGGER MODE TO CHANNEL 2 POSITIVE EDGE
SET TIME BASE TO 10 mS / cm.

4.2. OBSERVATION OF PULSES

ARM OSCILLOSCOPE, REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH, WHILST ADJUSTING TRIGGER LEVEL, UNTIL WAVE FORM OF FIG. C IS OBSERVED.

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					231				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET. No. 34	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

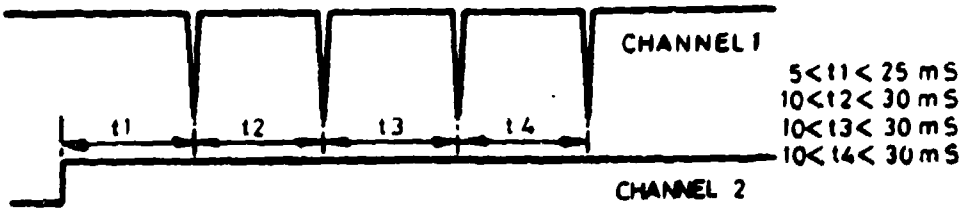


FIG. C

NOTE :- DUE TO STORAGE CHARACTERISTIC OF OSCILLOSCOPE, PULSES MAY NOT BE UNIFORM IN HEIGHT. REPEAT DISPLAYS MAY BE NECESSARY TO ENSURE THAT ALL PULSES ARE PRESENT. WAVEFORM SHOULD BE WITHIN TOLERANCES SHOWN IN FIG. C

SET PULSE SELECT SWITCH ON PULSE SIMULATION BOX TO 3. OBTAIN OSCILLOSCOPE TRACE AS PREVIOUSLY, BY DEPRESSION OF SW1.

OBSERVE THAT 3 PULSES ONLY ARE PRESENT ON THE TRACE. THE RIGHT HAND PULSE OF FIG. C SHOULD NOW BE MISSING.

SET PULSE SELECT SWITCH TO 2,1 AND 0 AND OBSERVE CORRESPONDING NUMBER OF PULSES APPEARING ON THE OSCILLOSCOPE, WHILST UTILISING BIAS SWITCH AND OSCILLOSCOPE AS PREVIOUSLY.

SWITCH OSCILLOSCOPE AND 28 V SUPPLY OFF AND REMOVE TEST CONNECTIONS TO PULSE SIMULATION BOX.

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					232				
APP									

GRAVES LIMITED, COLNBROOK, ENGLAND	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 95	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

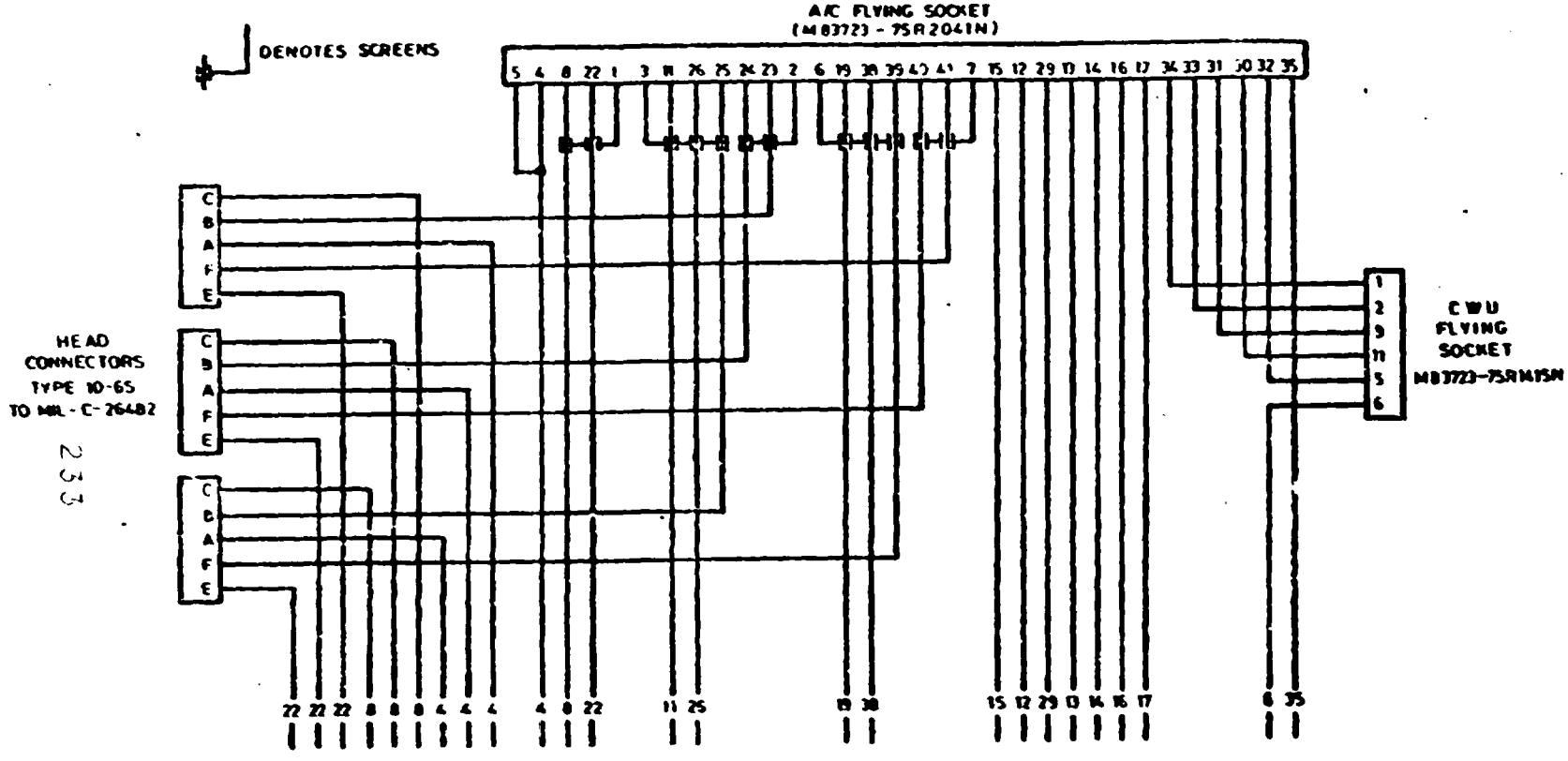


FIG. 1

ISSUE	A									
MOD										
COMPILED	P.S.									
CHD										
APP										

Gravner LIMITED, COLNBROOK, ENGLAND	SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 36	No. OF SHEETS
TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)		

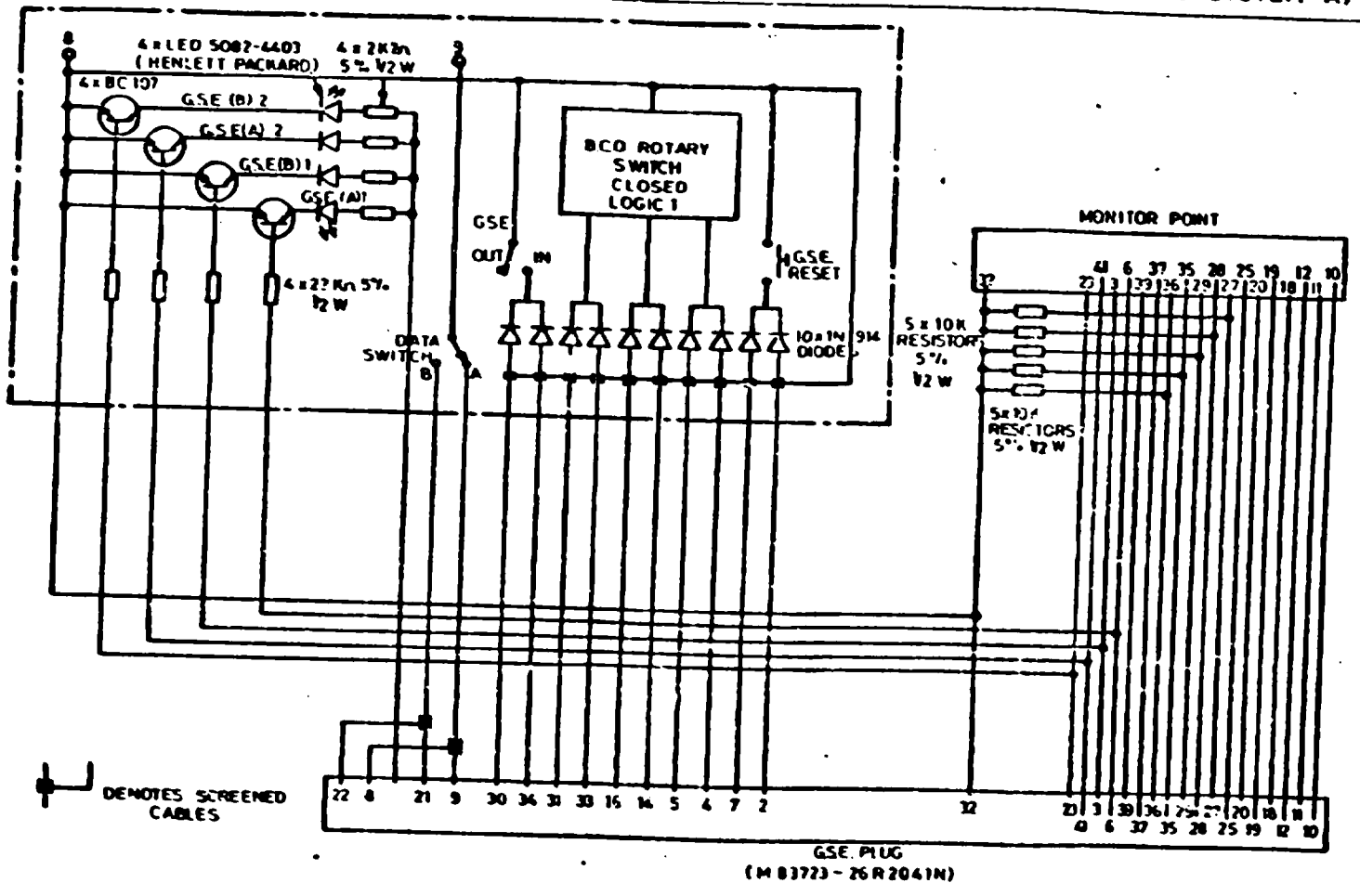
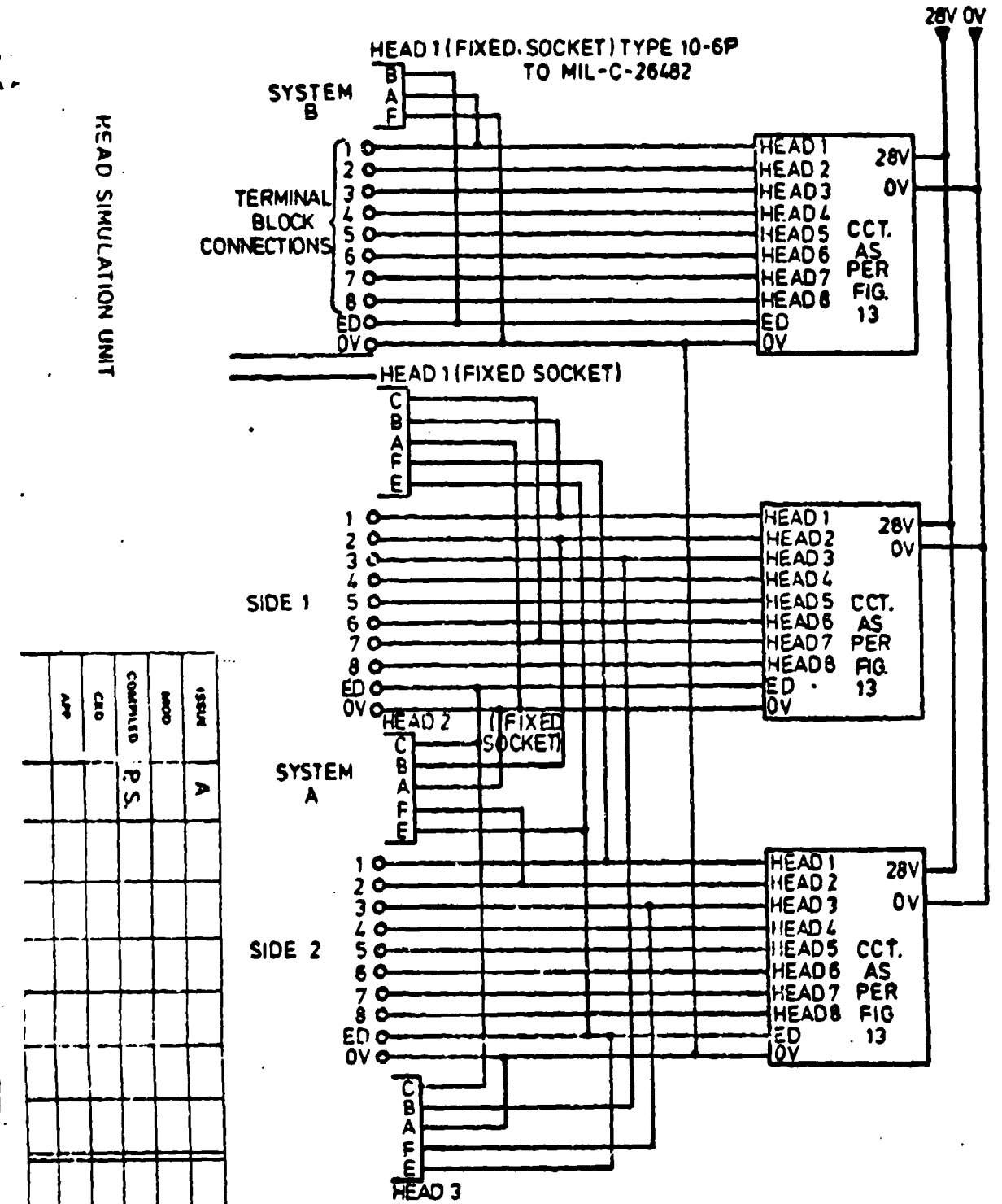
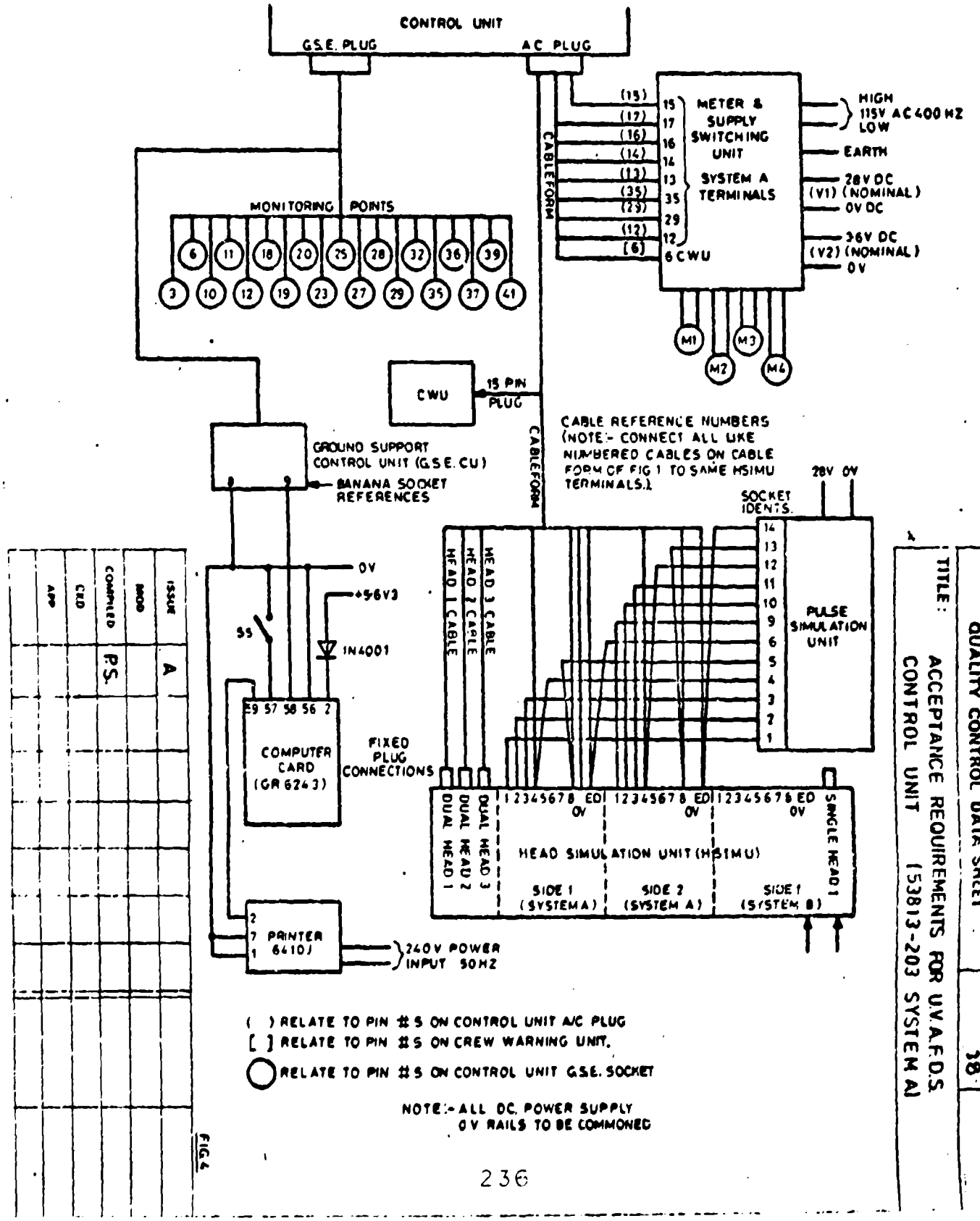


FIG. 2

GROUND SUPPORT CONTROL BOX
& CABLE HARNESS ASSEMBLY

ISSUE	A								
MOD									
COMPILED	P.S.								
CHD									
APP									


HEAD SIMULATION UNIT
HEAD 1 (FIXED SOCKET) TYPE 10-6P
TO MIL-C-26482
28V 0V
SYSTEM B
B A F
TERMINAL BLOCK CONNECTIONS
1 2 3 4 5 6 7 8 ED 0V
HEAD 1 28V
HEAD 2
HEAD 3 0V
HEAD 4
HEAD 5 CCT.
HEAD 6 AS
HEAD 7 PER
HEAD 8 FIG.
ED 13
0V
HEAD 1 (FIXED SOCKET)
C B A F E
SIDE 1
HEAD 2 (FIXED SOCKET)
SYSTEM A
SIDE 2
HEAD 3
ISSUE
MOD
COMPILED P.S.
CHD
APP
TITLE: ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT (53813-203 SYSTEM A)
QUALITY CONTROL DATA SHEET
GRAVINER LIMITED, COLNBROOK, BERKS.
DATA SHEET No. 05309
SHEET No. 37
No OF SHEETS
FIG. 3


CONTROL UNIT
G.S.E. PLUG
A.C. PLUG
CABLEFORM
METER & SUPPLY SWITCHING UNIT SYSTEM A TERMINALS
HIGH 115V AC 400 HZ LOW
EARTH
28V DC (V1) (NOMINAL)
0V DC
36V DC (V2) (NOMINAL)
0V
MONITORING POINTS
CWU
15 PIN PLUG
GROUND SUPPORT CONTROL UNIT (G.S.E. CU)
BANANA SOCKET REFERENCES
CABLE REFERENCE NUMBERS (NOTE:- CONNECT ALL LIKE NUMBERED CABLES ON CABLE FORM OF FIG 1 TO SAME HSIMU TERMINALS.)
28V 0V
SOCKET IDENTS.
PULSE SIMULATION UNIT
HEAD 1 CABLE
HEAD 2 CABLE
HEAD 3 CABLE
0V
+36V3
IN4001
SS
COMPUTER CARD (GR 6243)
FIXED PLUG CONNECTIONS
HEAD SIMULATION UNIT (HSIMU)
DUAL HEAD 1
DUAL HEAD 2
DUAL HEAD 3
SINGLE HEAD 1
SIDE 1 (SYSTEM A)
SIDE 2 (SYSTEM A)
SIDE 1 (SYSTEM B)
PRINTER 6410)
240V POWER INPUT 50HZ
( ) RELATE TO PIN #S ON CONTROL UNIT A/C PLUG
[ ] RELATE TO PIN #S ON CREW WARNING UNIT.
RELATE TO PIN #S ON CONTROL UNIT G.S.E. SOCKET
NOTE:- ALL DC. POWER SUPPLY 0V RAILS TO BE COMMONED
ISSUE
MOD
COMPILED
CKD
APP
P.S.
A
FIG 4
TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)
QUALITY CONTROL DATA SHEET
GRAVINER LIMITED COLNBROOK
DATA
SHEET No. 18
No. OF SHEETS
0 5309

GRAYMER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 39	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

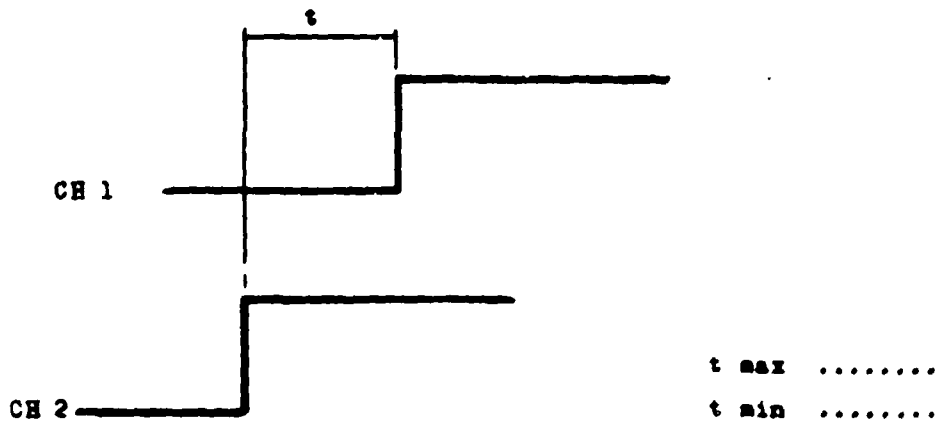


Figure 5

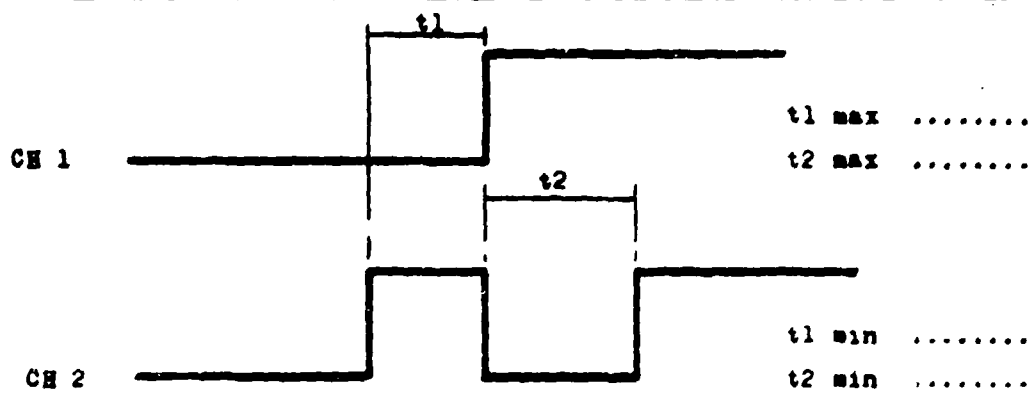


Figure 6

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					237				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

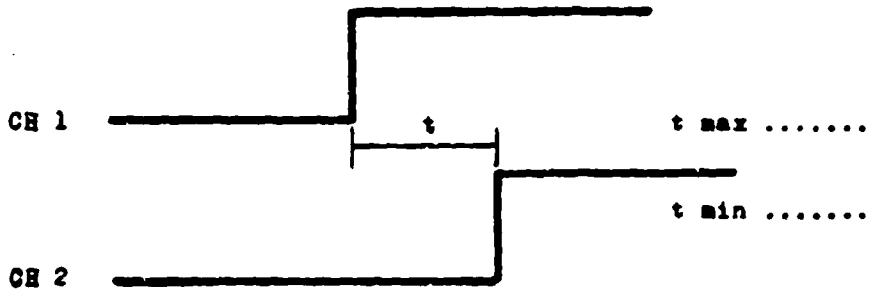


Figure 7

Figure 8

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					238				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 41	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

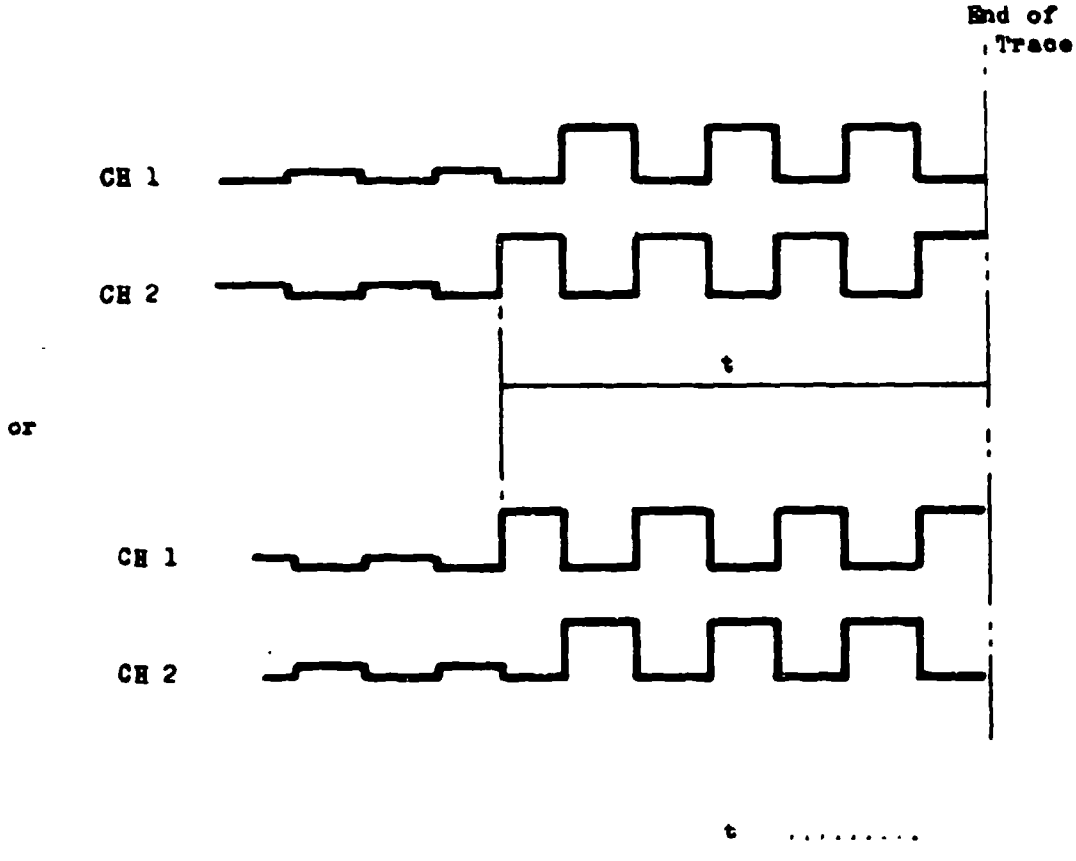


Figure 9

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					239				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)

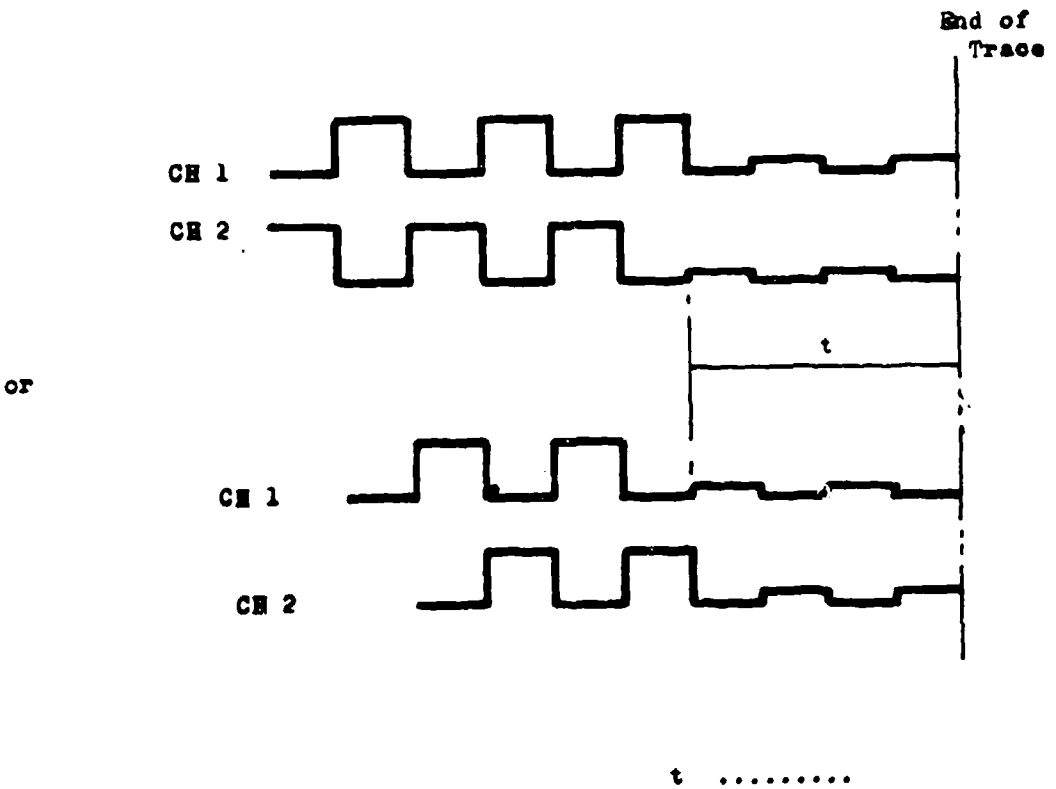
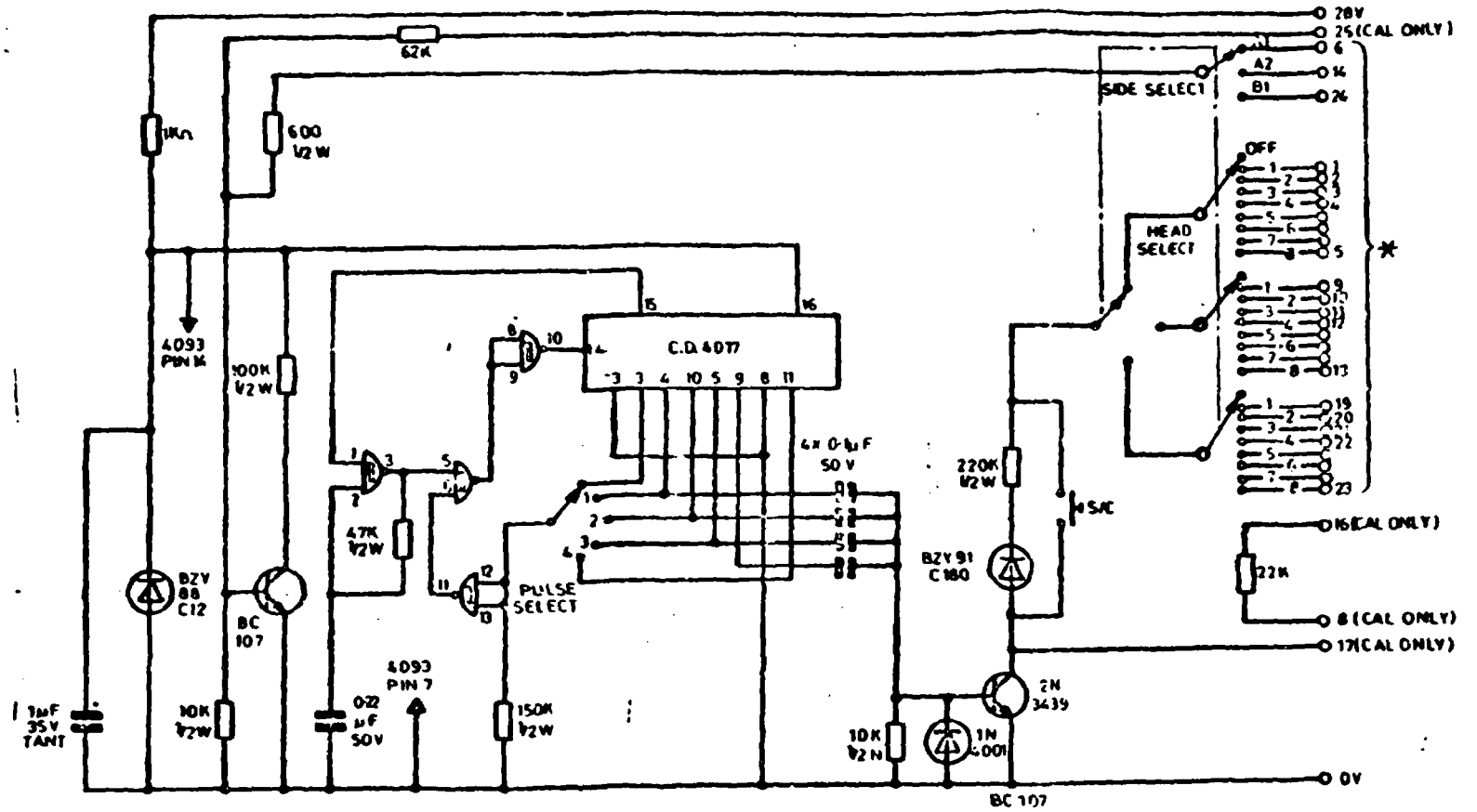


Figure 10

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					240				
APP									

GRAVINER LIMITED COLNBROOK ENGLAND	DATA SHEET No Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No 43	No OF SHEET
TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F. D.S. CONTROL UNIT (53813-203 SYSTEM A)		



CD4093 ✱ DENOTES D SOCKET CONNECTIONS

PULSE SELECT UNIT

FIG. 11

ISSUE	A
MOD	
COMPILED	P.S.
CKD	
APP	

GRAVINER LIMITED COLNBROOK ENGLAND

DATA SHEET No. Q 5309

QUALITY CONTROL DATA SHEET | SHEET No 44 | No OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.E.O.S. CONTROL UNIT (53813-203 SYSTEM A)

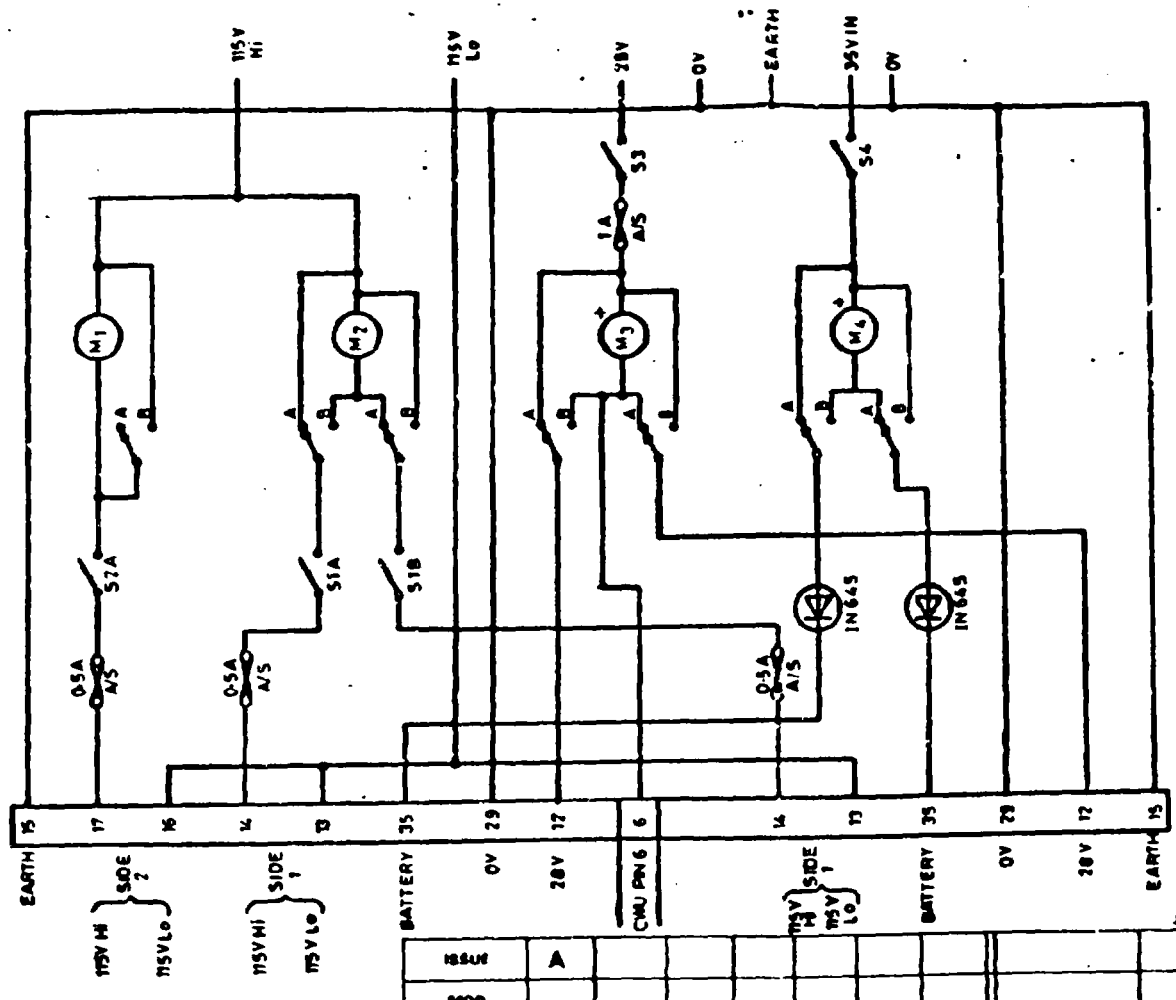
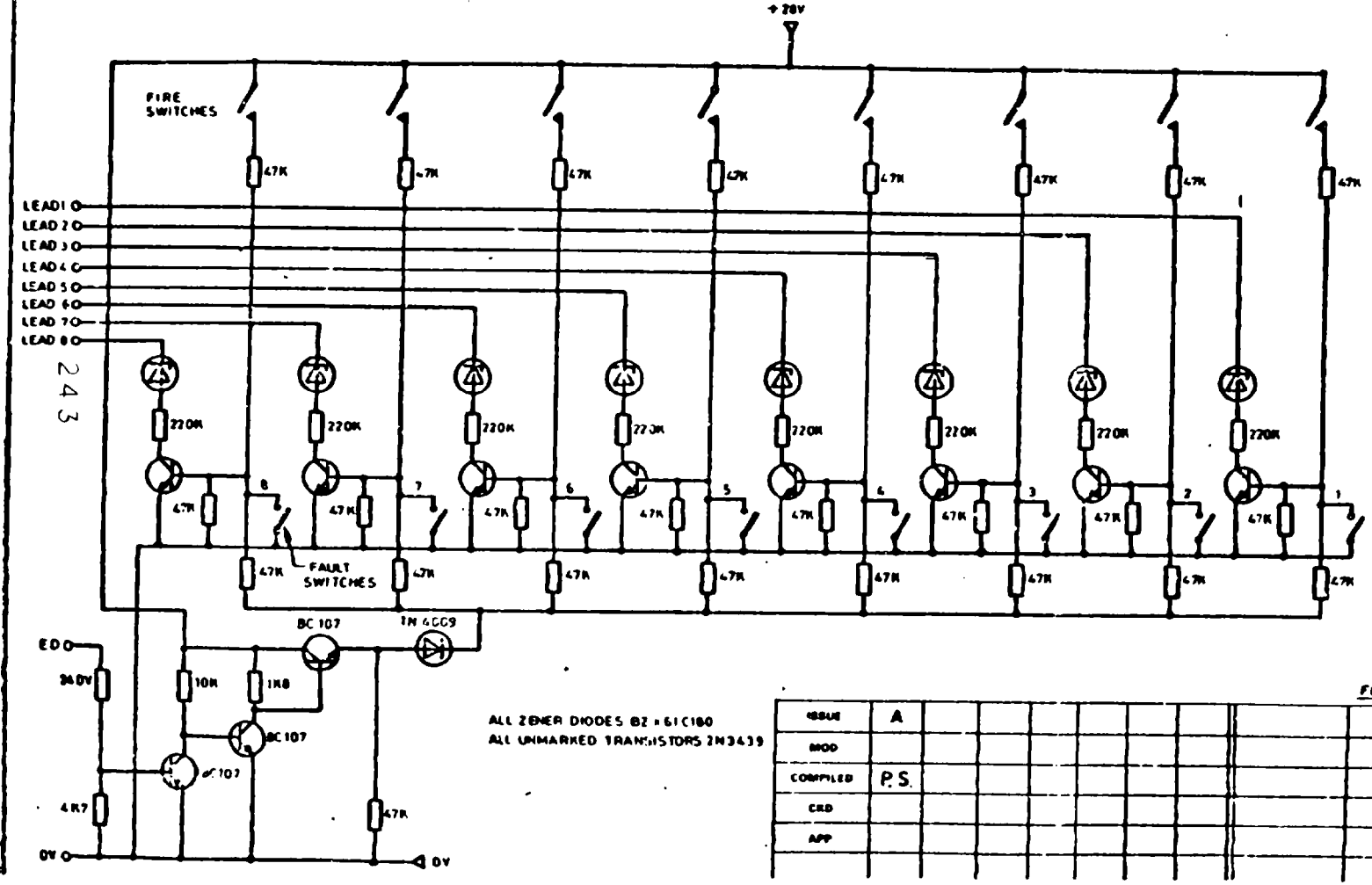


FIG. 12

CIRCUT DIAGRAM FOR METER & SUPPLY SWITCHING UNIT

ISSUE	A
MOD	
COMPILED	P.S.
CKD	
APP	

[illegible] LIMITED COLNBROOK ENGLAND	DATA SHEET No. Q 5309	
QUALITY CONTROL DATA SHEET	SHEET No. 45	No. OF SHEETS
TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-203 SYSTEM A)		



243

ALL ZENER DIODES BZ = 61C180
ALL UNMARKED TRANSISTORS 2N3439

FIG. 13

ISSUE	A
MOD	
COMPILED	P.S.
CKD	
APP	

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET No. 1	No. OF SHEETS 32

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

(1) Definition

Q 5310 becomes a master document for functional performance testing of control unit 53813-204.

Performance values have been defined in compliance with "funnel or tiered tolerances" philosophy and form the following categories.

Type 1 - Factory or Production Acceptance Limits appropriate at normal ambient temperature conditions.

Type 2 - Receiving Inspection or Customer Acceptance Limits appropriate at normal ambient temperature conditions.

Type 3 - Quality or Functional Acceptance Limits appropriate at and between the declared extremes of operating temperatures.

In any repeat of test in two geographical areas there is expected to be some difference in test results. Differences within the stated accuracy of instrumentation and those due to acceptable variances based upon time dependancy, transportation and test techniques are declared as acceptable. To meet these circumstances Type 1 limits used for Factory tests allow a smaller variation than those used for Type 2 limits by Receiving Inspection and as Customer Acceptance. These tests are carried out at normal ambient temperature conditions.

Functional limits at extremes of operating conditions are determined and declared. From time to time quality audit tests may be carried out and performance characteristics are measured for compliance with values of the approval sample which are measured at appropriate extreme conditions, particularly with respect to temperature. Type 3 limits cater for functional acceptance characteristics and allow a greater variation than Type 2 limits.

The correct acceptable value applicable to the nature of the test is detailed in a schedule and is to be selected for use as appropriate. Any test where a single value remains in the text is applicable to Type 1, 2, and 3 tests.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					245				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET No. 2	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

(ii) Frequency of Test

The following tests shall be carried out at a frequency appropriate to definition.

Type 1 All units.

Type 2 It is recommended that all units 'on receipt' and subsequently as defined in users procedures and schedules.

Type 3 These will be carried out as appropriate upon:-

Initiation of production.
Introduction of a major modification.
Cessation of production for three months.
Introduction of new processes which may affect production standard.
Change of key operator.

(iii) Action Required

iii(a) For Type 1 tests all results shall be recorded against Serial No. of each control unit.

For Type 3 tests an abridged test report detailing results obtained against Serial No. of each control unit is raised.

iii(b) For Type 1 tests any failures shall be reported to the Design Authority.

For Type 3 tests, any Control Unit that fails any test or part of a test shall be examined to locate the particular replaceable sub-assembly causing the malfunction.

The defective sub-assembly shall be replaced to each of two replacement sub-assemblies, and repeat testing carried out on both items.

Subject to satisfactory results on both replacement sub-assemblies, the batch of units can be released.

A failure during re-test on either sub-assembly constitutes a failure of the whole batch, and rectification/design modification is required before the batch can be released.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					246				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

NOTES: Control unit is referred to as CCU
Crew warning unit is referred to as CWU.

THIS TEST MUST NOT BE PERFORMED USING BATTERY CARD 43761-140 IN PLACE

For flight trial applications using battery card 43761-140 test as per Appendix 3.

1. EQUIPMENT REQUIRED FOR TESTS

Cable form as per FIG.1.

400 Hz. power supply (frequency range 380 Hz to 420 Hz)
(voltage range 102V to 124V)

D.C. supply 2 Amp (variable 16 - 30V output)

D.C. supply 0.5 Amp (variable 3 - 4 volts output)

D.C. supply 0.5 Amp 5.6V

Gould Storage Oscilloscope OS 4000 and two X10 probes.

Resistance Bridge

3 x AVO Model 8

Counter Timer capable of being +ve and -ve edge triggered at 5V levels, resolving to 0.1 mS on count range of 100 secs e.g. Racal Dana 9901 and one X1 probe.

Ground support control box and cable harness assembly as per FIG. 2.

Meter and supply switching unit as per FIG.11.

Head Simulation Unit as per FIG. 3.

Diode IN4001.

Crew Warning Unit part number 53813-202.

Computer Card, Golden River Co. GR6243,
Printer, Digitec Part Number 6410J.

Digital Voltmeter (DC and 400 Hz AC capability) used in conjunction with insulated probes.
Pulse simulation unit as per FIG. 10. (Calibrated as per Appendix 2).

ISSUE	A								
MOD									
COMPILED	pc								
CKD					247				
APP									

TITLE : ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

2. CONNECTIONS

Check that all supplies are set to OFF. Connect control unit to supplies and test equipment as per FIG. 4.

3. INITIAL SETTINGS

3.1. S1A, S1B, S2A, S3 and S4 ON, Meter and Supply Switching Unit to OFF. All 4 meter switches as , Meter and Supply switching unit to B.

3.2. Rotary switch on GSE control unit to position 6.

3.3. GSE mode switch to IN.

3.4. Data switch to A.

3.5. Computer card baud rate settings to 300 C/sec.

3.6. All head simulation unit, F1 (fire) and FA (fault) switches to OFF.

3.7. M_2 set to 1 Amp range AC.

3.8. M_3 set to 1 Amp range DC.

3.9. M_4 set to 10 mA range DC.

3.10. Using DVM set to 500v AC range switch on AC supply and set it to 124v 420 Hz ($\pm$ 0.5v).

3.11. Using DVM set to 50v DC range Switch on V_1 and set it to 29v ($\pm$ 0.2v).

3.12. Using DVM set to 10v DC range switch on V_2 and set it to 4v ($\pm$ 0.1v).

3.13. Using DVM set to 10v DC range, remove positive lead from V_3 supply. Switch on supply and set it to 5.6v DC ($\pm$ 0.1v). Switch V_3 supply off and reconnect positive lead.

3.14. Head select switch on Pulse simulation unit to OFF.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					248				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4. TEST PROCEDURE

Notes 1. Meter M_4 should be observed at each test and unless stated otherwise should read zero current.

2. Limits of all tests are contained in Appendix 1.

4.1. Earth Connections

With CCU disconnected, using resistance bridge, check resistance between CCU case and pin 15 of A/C plug, resistance to be less than ----------ohms.

4.2. Preliminary Check Out (High Supply Voltages)

4.2.1. Connect A/C and GSE cable forms to CCU as per FIG. 4.
Switch S4 to ON, M_4 should read less than --------mA.
Switch S_3 to ON, M_3 should read less than --------mA.
CWU right hand "FIRE DETECT FAIL" lamp to illuminate.

4.2.2. Switch S_{18} to ON, and observe that GSE 1 LED on Side 1 of GROUND SUPPORT CONTROL UNIT (GSECU) indicates.

M_2 to indicate less than --------mA.

M_3 to indicate less than --------mA.

M_4 to indicate zero.

4.3. Preliminary Check Out

4.3.1. Set GSECU mode switch to OUT. Depress and release reset swi tch, observe that Side 1 GSE LED begins and continues to flash after an initial off period of approximately 4 seconds. GSE 1 Side 1 LED should flash at a rate of approximately 3 per second. Side 1 GSE2 LED on GSECU should flash approximately once every 15 seconds.

Observe that CWU right hand lamps i.e. 'R ENG FIRE' and 'FIRE DETECT FAIL' lamps are both extinguished.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					249				
APP									

TITLE : ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.3.2. Depress 'FIRE DETECT TEST' push button on CWU, 'R ENG FIRE' lamp to indicate within approximately one second.
Release 'FIRE DETECT TEST' push button on CWU, 'R ENG FIRE' lamp to extinguish within approximately one second.
Depress 'FAIL IND. TEST' push button on CWU, Right hand 'FIRE DETECT FAIL' lamp to show.
Release 'FAIL IND TEST' push button on CWU, Right hand 'FIRE DETECT FAIL' lamp to extinguish.

4.4. Supply Currents - Running Mode

M_2 to indicate less than --------mA.

Note: - meter needle will fluctuate in sympathy with time share.

Observe average value.
M_3 to indicate less than --------mA
M_4 to indicate zero.

4.5. Supply Currents - Fire Mode

Depress and hold CWU Fire test button, when R ENG FIRE' lamps show observe meter readings.
M_2 should read less than --------mA.
M_3 should read less than --------mA.
M_4 should read zero.
Release CWU FIRE Test button.

4.6. Preliminary Check Out (Low Supply Voltages)

Set switches S1B, S_3 and S_4 to OFF.
Set GSE MODE Switch on GSECU to IN.
Using DVM set AC supply to 102 volts 380 Hz ($\pm$ 0.5v),
V_1 supply to 16 volts ($\pm$ 0.2v),
V_2 supply to 3 volts, ($\pm$ 0.1v).
Repeat 4.2 to 4.5 inclusively, then set S1B, S_3 and S_4 to OFF.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					2-0				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.7. Regulator Operation

Note: All DC voltages are measured with respect to pin 32 of monitoring points.

4.7.1. Settings (Low Supply)

Using DVM Set AC supply to 102V 380 Hz ($\pm$ 0.5v),
V_1 to 28 volts ($\pm$ 0.2V),
V_2 to 3.6 volts ($\pm$ 0.1v).
Set GSE Mode Switch on GSECU to IN.

4.7.2. Set Switches S1B, S_3 and S_4 to ON.

4.7.3. Regulation at Low Supply (5.6V Rail) Side 1

With DVM set at 10V range DC, check voltage at pin 12 of monitoring points. Voltage to be between --------volts minimum and -------- volts maximum.

4.7.4. Regulation at Low Supply (Head Supply) Side 1

BEWARE OF HIGH VOLTAGES ON THESE TERMINALS.

Set DVM on 500V DC range. Check voltage at pin 25 of monitoring point, voltage to be between -------- volts minimum and -------- volts maximum.
Set switches S1B, S_3 and S_4 to OFF.

4.7.5. Settings (High Supply)

Using DVM set AC supply to 124V 420 Hz.
Repeat 4.7.2. to 4.7.4. inclusively.

ISSUE	A								
MOD									
COMPILED	PS								
CKD									
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET. No. 8	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.8. Timing Tests

4.8.1. Settings for power up time delay.
With switches S1B, S_3 and S_4 set to OFF set AC supply to 400 Hz 115V.

Set oscilloscope time base to 0.2 secs/cm, channel 1 and 2 amps. to 0.2V/cm, triggering to positive edge channel 1. Stored trigger point set to $\frac{3}{4}$ trace.
Set channel 1 and 2 to DC mode.
Set storage mode to ROLL.
Switch on oscilloscope and adjust channel 1 trace to be at mid-screen.
Adjust channel 2 trace to be 1 cm above bottom of screen.
Set GSE mode switch to IN.

4.8.2. Connections for power up Time Delay

Connect CH1 probe to terminal block monitoring point 23.
Connect CH2 probe to terminal block monitoring point 12.
All probe returns are connected to pin 32 of monitoring point.

4.8.3. Power Up Time Delay (Side 1)

4.8.3.1 With oscilloscope trigger armed switch on system power in the order S_3, S_4 and S1B.

Note: If oscilloscope does not trigger, adjust trigger level in conjunction with setting S1B to OFF, re-arming trigger and setting S1B back to ON.
Observe oscilloscope waveform as per FIG. 5.
Measure time delay between rising edge of channel 1 and 2 as shown in FIG. 5.
Switch off S1B, S_3 and S_4 and remove oscilloscope probes.

4.8.4. Settings for Time Share Timing

Switch on timer counter.
Set GSE mode switch to OUT.
Set timer for positive edge start, positive edge stop such that 500 mS can be measured.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					252				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.8.5. Connections for Time Share Timing

Connect timer probe to monitoring point pin 23.
Probe return connected to monitoring point pin 32.

4.8.6. Time Share Timing

4.8.6.1. Set S_1 B, S_3 and S_4 to ON.
System to function as per 4.3.1.

4.8.6.2. Observe period of timer, time to be between --------secs. minimum and --------secs. maximum.

4.8.6.3. Reselect for negative edge stop and read timer.
Time to be between --------- secs. minimum and --------- secs. maximum.

4.8.7. Connections and Settings for Self Test Timer

Connect timer probe to monitoring point pin 3.
Select timer for positive edge start, positive edge stop.
Select timing range to cover a 20 second period.

4.8.8. Self Test Timing (Period)

Observe period of timer, time to be between --------secs. minimum and --------seconds maximum.

4.8.9. Self Test Timing (Duration)

Reselect timer for positive edge start negative edge stop and observe period of timer.
Time to be between --------secs. minimum and --------secs. maximum.
Remove timer probe connections.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					253				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.9. Ground Support Voltage Lines

Note: All DC voltages are monitored with respect to pin 32 of monitoring point.

4.9.1. Settings

With power on from previous test, set GSE Mode Switch on GSECU to IN.
Depress and release reset button on GSECU.
Observe that GSE1 LED on Side 1 of GSECU lights.

4.9.2. Battery Monitoring Point

With DVM set to 10v range DC check voltage at pin 37 of monitoring point, voltage to be between -------- volts minimum and -------- volts maximum.

4.9.3. 115V Feed to GSE

BEWARE OF HIGH VOLTAGE ON THESE TERMINALS

Set DVM to read 200V AC range and connect probes to pins 10 and 11 of monitoring point.
Observe DVM reading, voltage to be between -------- volts maximum and -------- volts minimum.

4.10. Check Point Monitoring

4.10.1. Settings and Connections

Set GSE mode switch to OUT on GSECU.
Depress and release reset switch on GSECU.
Set DVM to 50 volt range DC.
Connect DVM positive to pin 28 and negative to pin 32 of monitoring point.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					2.5.4				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.10.2. Check Point 1

DVM reading to be zero volts.
Depress 'FIRE DETECT TEST' push button, 'R ENG FIRE' lamp to indicate, DVM reading to be between -------- volts minimum and -------- volts maximum.

4.10.3. Check Point 2

Repeat 4.10.2. with DVM positive connected to pin 29 of monitoring points.

4.10.4. Check Point 3

Connect DVM to pin 35 of monitoring points.
DVM reading to be zero volts.
Depress 'FAIL IND TEST' push button, right 'FIRE DETECT FAIL' indication to show.
Observe DVM reading, voltage to be between -------- volts minimum and -------- volts maximum.

4.10.5. Check Point 4

Repeat 4.10.4. with DVM connected to pin 36 of monitoring points.

4.11. Ground Support Controlled Tests

4.11.1. RAM Test and Reset

Set GSE Mode switch on GSECU to IN.
Depress and release reset button on GSECU.
Observe that Side 1 GSE1 LED on GSECU lights.

4.11.2. Common Logic Test (Functional)

Select position 4 on rotary switch, depress and release reset button.
Observe that Side 1 GSE 1 and 2 LED's on GSECU flash ON and OFF in the following sequence.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					255				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.11.2. Common Logic Test (Functional) (contd.)

GSE 2 Side 1 (ON-OFF), GSE 1 Side 1 (ON), GSE 2 Side 1 (ON)

Repeat depression and release of reset button, observe that 'R ENG FIRE' lamp flashes in sympathy with the first flash of GSE 2. Right hand 'FIRE DETECT FAIL' lamp should remain off during the period that GSE LED's are active.
Set S1B, S_3 and S_4 to OFF.

4.11.3. Common Logic Test (Timing)

4.11.3.1. Connections and Settings

Set oscilloscope channels 1 and 2 amps. to 0.2V/cm.
Set trigger to CH1 (positive edge).
Set display mode to roll.
Set time base to 0.1 secs/cm.
Set "stored trigger point" to ½ trace.

Connect Channel 1 probe to pin 23 o. monitoring point.
Connect Channel 2 probe to pin 3 of monitoring point.
Connect probe return lines to pin 32 of monitoring point.

4.11.3.2. Side 1 Timing of Common Logic Test

Set S1B, S_3 and S_4 to ON.
Arm oscilloscope trigger.
Depress and release reset button on GSECU.
Wave form to be as FIG. 6.
Note:
If oscilloscope does not trigger, adjust trigger level in conjunction with depression of GSECU reset switch and rearming of oscilloscope trigger.
Take measurements of t_1 and t_2.
Remove oscilloscope probes.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					256				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.11.4. Background Programme Test

Select position 5 on GSECU rotary switch. Depress and release reset button. After 5 seconds no LED's to show on GSECU.

4.11.5. Idle Programme Test

Select position 0 on GSECU rotary switch.
Depress and release reset button.
Observe that side 1 GSE 1 and 2 LED's on GSECU show.

4.11.6. Data Retention Test

Set S_4 to OFF. Select position 2 on GSECU rotary switch, depress and release reset button.
Observe that side 1 GSE1 LED on GSECU lights.
Select position 3 on GSECU rotary switch, depress and release reset button.
Observe that side 1 GSE1 and GSE2 LED's on GSECU lights.
Reselect position 2 on GSECU rotary switch, depress and release reset button.
Observe that side 1 GSE1 LED on GSECU lights.
Set S1B and S_3 to OFF. Wait 30 seconds.
Select position 3 on GSECU rotary switch .
Set S1B and S_3 to ON.
Observe that only side 1 GSE1 LED on GSECU lights.
Reselect position 2 on GSECU rotary switch.
Set S_4 to ON.
Depress and release reset button on GSECU. Observe that only Side 1 GSE1 LED on GSECU lights.
Set S1B and S_3 to OFF. Wait 30 seconds.
Select position 3 on GSECU rotary switch. M4 to read between -------- mA minimum and -------- mA maximum.
Set S1B and S_3 to ON. Observe that side 1 GSE1 and GSE2 LED on GSECU light.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					257				
APP									

4.11.7. Data readout Test

Switch on V_3 (supply to computer card). Switch on mains power to printer.
Select position 2 on GSECU rotary switch.
Depress and release reset switch on GSECU.
Observe that Side 1 GSE 1 LED on GSECU lights.
Select position 1 on GSECU rotary switch.
Depress and hold reset switch on GSECU.
Depress and release S5.
Observe that printer prints --------
Release reset switch on GSECU.
Printer should print as per FIG.7.
When printer stops observe that GSE 1 LED (Side 1) on GSECU lights.

4.12. System Function Tests

All fire and fault indications refer to 'R ENG FIRE' and right hand 'FIRE DETECT FAIL' lamps on CWU.
Note:
These tests are carried out using the headsimulation unit referred to as HSIMU.

All references to Side 1 fault and fire switches refer to system B side 1. System A fault and fire switches are not used.

4.12.1. Initialise for Functional Tests

With system still powered from previous tests select position 6 on rotary switch of GSECU.
Set GSE mode switch to OUT.
Depress and release reset switch on GSECU. Observe that system functions as per 4.3.1.

4.12.2. Set side 1 head 1 fire switch to ON.
Fire indication on CWU to show.
Set side 1 head 1 fire switch to OFF.
Fire indication on CWU to extinguish.

Repeat 4.12.2. for heads 2, 3, 4, and 8.

TITLE :
ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.12.3. Failed Heads

Set side 1 heads 5, 6 and 7 fault switches on HSIMU to ON.
Set side 1 heads 1, 3 and 4 fault switches on HSIMU to ON.
Observe that right hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE 2 (side 1) LED's flashing on GSECU.
Set side 1 heads 1, 3 and 4 fault switches on HSIMU to OFF.
Set side 1 heads 2 and 8 fault switches on HSIMU to ON.
Observe that right hand 'FIRE DETECT FAIL' lamp does not light at next occurrence of GSE2 (Side 1) LED flashing on GSECU.

4.12.4. Adjacency Set Failure

4.12.4.1. Heads 1 and 2 Adjacency Set

Set side 1 heads 1, 2, 3, 4 and 8 fire and fault switches to OFF.
Set GSE mode switch on GSECU to IN.
Depress and release reset button.
Observe that side 1 GSE 1 LED on GSECU lights.
Set head 1 and 2 fault switches on side 1 to ON.
Set GSE mode switch on GSECU to OUT.
Depress and release reset button.
Right hand CWU 'FIRE DETECT FAIL' lamp should light immediately after the first occurrence of GSE 2 (Side 1) LED flashing on GSECU.
Set head 1 and 2 fault switches on side 1 to OFF.
After the occurrence of the next flashing sequence of GSE 2 LED's (occurring approximately once every 15 seconds) observe that right hand 'FIRE DETECT FAIL' lamp does not extinguish.

4.12.4.2. Heads 2 and 3 Adjacency Set

Repeat 4.12.4.1. using heads 2 and 3 fault switches.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					259				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.12.4.3. Heads 4 and 8 Adjacency Set

Repeat 4.12.4.1. using heads 4 and 8 fault switches.
Set GSE mode switch to IN. Depress and release GSE reset switch.

4.12.5. Short Circuit Head Operation

4.12.5.1. Set Up

Set system B fault switches to OFF.
Check that all system B side 1 fire switches are set to OFF.
Set SIDE SELECT switch on pulse select unit (PSU) to side 1B.
Set HEAD SELECT switch on pulse select unit to head 1.
Set PULSE SELECT switch on PSU to 0.
Set GSE mode switch on GSECU to OUT.
Depress and release reset switch on GSECU.;
Observe that system functions as per 4.3.1.

4.12.5.2. Fire Set (Head 1)

Note:
Allow 2 seconds at each switch position before observing result on CWU.
Set PULSE SELECT switch on PSU to 1.
Observe that fire indication on CWU is not lit.
Set PULSE SELECT switch on PSU to 2.
Observe that fire indication on CWU is not lit.
Set PULSE SELECT switch on PSU to 3.
Observe that fire indication on CWU is not lit.
Set PULSE SELECT switch on PSU to 4.
Observe that fire indication on CWU is lit.

TITLE: ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT 53813-204 (SYSTEM B)

4.12.5.3. Short Circuit (Head 1)

Depress and hold short circuit button on pulse simulation unit.
Observe that fire indication on CWU extinguishes.
Release short circuit button on PSU.
Observe that fire indication on CWU re-lights.

4.12.5.4. Fire Reset (Head 1)

Set PULSE SELECT switch on PSU to 3.
Observe that fire indication on CWU remains lit.
Set PULSE SELECT switch on PSU to 2.
Observe that fire indication on CWU remains lit
Set PULSE SELECT SWITCH on PSU to 1.
Observe that fire indication on CWU extinguishes.
Return PULSE SELECT switch on PSU to 0.
CWU fire indication to remain extinguished.

4.12.5.5. Sensitivity and Short Circuit Head Operation (Heads 2, 3, 4, 8)

Repeat 4.12.5.2. to 4.12.5.4. for heads 2, 3, 4 and 8 by selecting required head on HEAD SELECT switch on PSU.

4.12.5.6. Set S1B, S_3 and S_4 to OFF.
Set head select switch on PSU to OFF.

4.12.6. Response to Fire

4.12.6.1. Settings and Connections

Set channel 1 amplifier on oscilloscope to 20v/cm.
Connect channel 1 oscilloscope probe to System B side 1. ED terminal of HSIMU.
Connect probe return to pin 32 of monitoring point.
Connect pin 28 of monitoring point to external trigger input of oscilloscope, using X1 probe.

ISSUE	A								
MOD									
COMPILED	PS								
CKD									
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.12.6.1. Settings and Connections (contd.)

Set oscilloscope trigger mode to Ext. (positive edge).
Set trigger point at end of trace ensuring that end trace coincides with end of trace graticule.

Set time base to 0.1 secs/cm.
Storage mode set to ROLL.
Set S1B, S_3 and S_4 to ON. Observe that system functions as per 4.3.1.

4.12.6.2. Response to Fire (Set)

Note:
To ensure correct results this test should be carried out about 3 seconds after GSE2 LED on GSECU (side 1) has flashed.

With oscilloscope trigger armed depress and hold 'FIRE DETECT TEST' button on CWU.

Note:
If oscilloscope does not trigger, adjust trigger level in conjunction with repeat depressions of 'FIRE DETECT TEST' button, re-arming trigger between each switch depression.

Waveform shall be of the form of FIG. 8. Measure fire set time t.

4.12.6.3. Response to Fire (Reset)

Re-arm oscilloscope trigger, select negative edge EXT trigger.
Release 'FIRE DETECT TEST' switch on CWU.
Observe oscilloscope wave form, trace to be of the form of FIG. 9.

Note:
To ensure correct results this test should be carried out about 3 seconds after GSE2 LED on GSECU (side 1) has flashed.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					26.2				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

4.12.6.4. Switch Off

Set S1B, S_3 and S_4 to OFF.
Remove oscilloscope probes from monitoring points.
Switch off all power supplies.

END OF TEST

ISSUE	A								
MOD									
COMPILED	PS								
CKD					203				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. Q5310

QUALITY CONTROL DATA SHEET

SHEET No. 20 | No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-20 (SYSTEM B)

SCHEDULE OF TESTS — APPENDIX 1

Test Definition	Category	Parameter Values						Units
4.1.	1 2 3	0.2 max 0.25 max 0.3 max						Ohms
		Values at AC Supply = 124V 420 Hz V1 = 29V V2 = 4V			Values at AC Supply = 102V 380 Hz V1 = 16V V2 = 3V			
		M2	M3	M4	M2	M3	M4	
4.2.1.	1	-	140	1.25	-	100	1.1	
	2	-	148	1.45	-	106	1.3	mA
	3	-	160	1.65	-	115	1.55	Max.
4.2.2.	1	140	85	0	115	45	0	
	2	150	89	0	123	47	0	mA
	3	165	97	0	135	52	0	Max.
4.4.	1	121	75	0	100	42	0	
	2	129	80	0	107	45	0	mA
	3	142	86	0	117	48	0	Max.
4.5.	1	146	270	0	118	176	0	
	2	156	280	0	126	185	0	mA
	3	171	295	0	138	198	0	Max.
		Values at AC Supply = 102V 380 Hz			Values at AC Supply = 124 V 420Hz			
4.Z3	1	5.7 ± 0.45			5.7 ± 0.45			
	2	5.7 ± 0.5			5.7 ± 0.5			Volts
	3	5.7 ± 0.65			5.7 ± 0.65			
4.Z4	1	322 ± 10			322 ± 10			
	2	322 ± 12			322 ± 12			Volts
	3	322 ± 17			322 ± 17			

ISSUE	A									
MOD										
COMPILED	PS									
CKD					264					
APP										

GRAVINER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. Q5310

QUALITY CONTROL DATA SHEET

SHEET No. 21 | No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-20$ (SYSTEM B)

SCHEDULE OF TESTS (Contd.) APPENDIX 1

Test Definition	Category	Parameter Value	Units
4.8.6.2.	1 2 3	337 ± 17 337 ± 20 337 ± 23	mS
4.8.6.3.	1 2 3	168 ± 9 168 ± 11 168 ± 13	mS
4.8.8.	1 2 3	14.8 ± 0.74 14.8 ± 0.88 14.8 ± 1.03	seconds
4.8.9.	1 2 3	168 ± 9 168 ± 11 168 ± 13	mS
4.9.2.	1 2 3	5.1 ± 0.6 5.1 ± 0.68 5.1 ± 0.85	Volts
4.9.3.	1 2 3	114.9 ± 0.6 114.9 ± 0.7 114.9 ± 0.8	Volts
4.10.2. 4.10.3. 4.10.4. 4.10.5.	1 2 3	27.5 ± 0.7 27.4 ± 0.9 27.2 ± 1.2	Volts
4.11.3.2.	1 2 3	t1: 0.39 ± 0.035 0.39 ± 0.04 0.39 ± 0.05 t2: 0.39 ± 0.035 0.39 ± 0.04 0.39 ± 0.05	seconds
4.8.3.1.	1 2 3	0.63 ± 0.42 0.63 ± 0.43 0.63 +0.62/−0.44	seconds

ISSUE	A									
MOD										
COMPILED	PS									
CKD					264					
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GRAVINER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. Q5310

QUALITY CONTROL DATA SHEET

SHEET No. 22 | No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

SCHEDULE OF TESTS (Contd.) APPENDIX 1

Test Definition	Category	Parameter Value	Units
4.11.6.	1 2 3	1.2 max. 1.35 max. 1.6 max	mA
4.11.7.1.	1) 2) 3)	GRUTIL V.4	-
4.12.6.2.	1 2 3	0.85 ± 0.1 0.85 ± 0.12 0.85 ± 0.15	seconds
4.12.6.3.	1 2 3	0.68 ± 0.05 0.68 ± 0.06 0.68 ± 0.08	seconds

APPENDIX 3 SCHEDULE OF TESTS

4.7.	1 2	3.6 ± 0.6 3.6 ± 0.65	volts
4.9.	1 2	3.6 ± 0.6 3.6 ± 0.65	volts

ISSUE	A								
MOD									
COMPILED	PS								
CKD					200				
APP									

GRAVINER LIMITED. COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET No. 23	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

APPENDIX 3

FLIGHT TRIALS UNIT WITH BATTERY CARD

1.0. Equipment required, as per main Q. Sheet.

Additional equipment, 1 decade resistance box (100K capability) + 2 flyleads.

2.0. Connections. As per main Q Sheet.

3.0. Initial settings.

3.1. S1A, S1B, S2A, S3 and S4 on meter supply switching unit to OFF.

3.2. GSE mode switch to IN, rotary switch set to position 6.

3.3. M2 set to 1 Amp range.

3.4. M3 set to 1 Amp. range.

3.5. M4 set to 10 mA range.

3.6. Using DVM set to 500V AC range, switch on AC supply and set it to 115V 400 Hz ($\pm$ 0.5V).

3.7. Using DVM set to 50V DC range, switch on V1 and set it to 2 8V DC ($\pm$0.2V).

3.8. Insert battery card into control unit 53813-204.

4.0. Procedure.

4.1. Set S3 to ON. Observe that R. hand 'FIRE DETECT FAIL' lamp lights.

4.2. Wait for ½ hour to allow battery to charge.

4.3. Set S1B to ON.
Observe that Side 1 GSE 1 LED on GSECU lights and R. hand 'FIRE DETECT FAIL' lamp extinguishes.

4.4. Set rotary switch on GSECU to 2. Depress and release reset button on GSECU. Observe that GSE1 LED on side 1 of GSECU lights.

4.5. Set S1B and S3 to OFF.

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					267				
APP									

TITLE : ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT 53813-204 (SYSTEM B)

APPENDIX 3 (contd.)

4.6. Wait for 30 seconds then set rotary switch to position 3 and set S1B and S3 to ON.
Observe that both GSE 1 and GSE 2 LEDS on GSECU light. Set S1B and S3 to OFF.

4.7. Using DVM set to 10V range DC, connect negative lead to pin 32 of monitoring point, connect positive lead to pin 37 of monitoring point.
Meter reading to be between -------- volts minimum and -------- volts maximum.

4.8. Set decade resistance box to 100K

4.9. Connect decade resistance box between pin 32 of monitoring point and cable 18 of system B aircraft plug cable form.
Connect DVM across 100 K decade box, observe meter reading.
Reading to be between -------- volts minimum and -------- volts maximum.

4. Remove decade resistance box and flyleads.
Set all power supplies to OFF.

END OF TEST.

ISSUE	A								
MOD									
COMPILED	PS								
CKD					268				
APP									

GRAYNER LIMITED. COLNBROOK. ENGLAND.	DATA SHEET No. 0.5310	
QUALITY CONTROL DATA SHEET	SHEET. No 25	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)

APPENDIX 2

CALIBRATION OF PULSE SIMULATION BOX

1.0. EQUIPMENT REQUIRED FOR TESTS

28 V D.C. SUPPLY (0·5 AMP.).
2 x OSCILLISCOPE PROBES (x10)
STORAGE OSCILLISCOPE (GOULD OS 4000 OR SIMILAR)
PULSE SIMULATION BOX
NORMALLY OPEN BIAS SWITCH

2.0. CONNECTIONS

CONNECT AS PER FIG. A

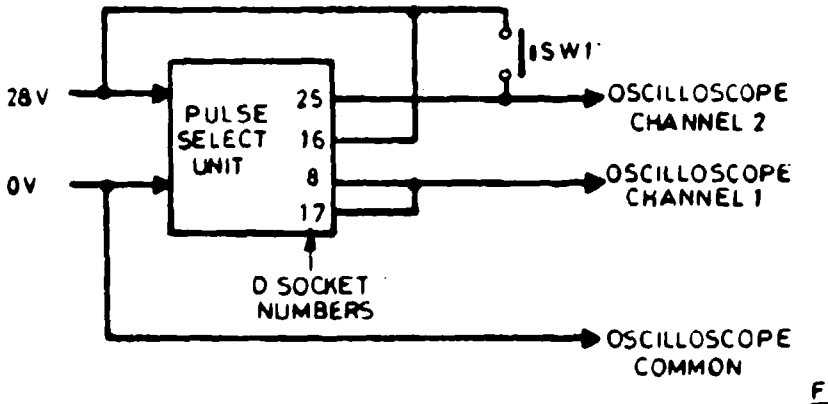


FIG. A

3.0. PULSE CHARACTERISTICS

3.1. SETTINGS

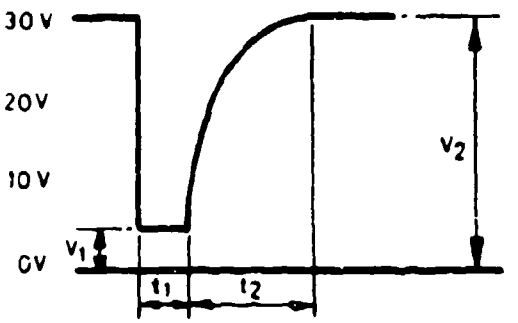
SET 28V D.C. SUPPLY TO 28V
SET CHANNEL 1 Y AMP TO 1V/cm.
SET CHANNEL 2 Y AMP TO 2V/cm.
SET TRIGGER TO CHANNEL 1 NEGATIVE EDGE.
SET "STORED TRIGGER POINT" TO 1/4 SCALE.
SET TIME BASE TO 0·1 mS/cm
SET PULSE SIMULATION BOX PULSE SELECT SWITCH TO 4.
SET OSCILLOSCOPE STORAGE MODE TO ROLL.
SWITCH ON OSCILLOSCOPE.
SET CHANNEL 1 TRACE TO BE AT MID SCREEN
SET CHANNEL 2 TRACE TO BE 1cm ABOVE BOTTOM OF SCREEN

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					6·9				
APP									

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)

3.2. PULSE CHARACTERISTICS MEASUREMENT

SWITCH ON 28V SUPPLY. ARM OSCILLOSCOPE TRIGGER. REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH SW1 WHILST ADJUSTING TRIGGER LEVEL UNTIL WAVE FORM OF FIG. B IS OBSERVED. NOTE OSCILLOSCOPE SHOULD BE RE-ARMED AFTER EACH SWITCH DEPRESSION.



V1 MAX.= 10V
V_1 MIN. = 2 V
V_2 MAX.= 30 V
V_2 MIN. = 26V
t_1 MAX.= 300µS
t_1 MIN.= 50µS
t_2 MAX.= 800µS
t_2 MIN. = 100µS

FIG. B

WAVE FORM SHOULD BE WITHIN THE LIMITS OF FIG. B AS SHOWN.

4.0. NUMBER OF PULSES

4.1. SETTINGS

SET TRIGGER MODE TO CHANNEL 2 POSITIVE EDGE
SET TIME BASE TO 10 mS / cm.

4.2. OBSERVATION OF PULSES

ARM OSCILLOSCOPE, REPEAT DEPRESSION AND RELEASE OF BIAS SWITCH, WHILST ADJUSTING TRIGGER LEVEL, UNTIL WAVE FORM OF FIG. C IS OBSERVED.

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					270				
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.

DATA SHEET No. Q 5310

QUALITY CONTROL DATA SHEET

SHEET No. 27 | No OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)

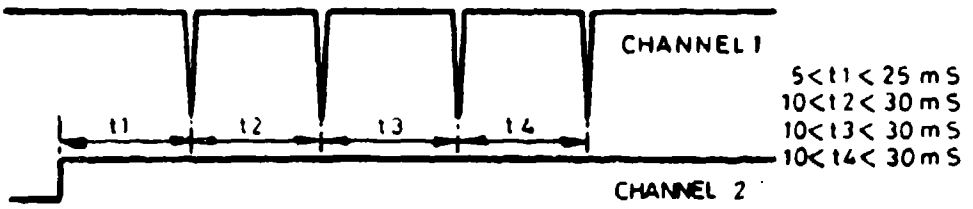


FIG. C

NOTE :- DUE TO STORAGE CHARACTERISTIC OF OSCILLOSCOPE, PULSES MAY NOT BE UNIFORM IN HEIGHT. REPEAT DISPLAYS MAY BE NECESSARY TO ENSURE THAT ALL PULSES ARE PRESENT. WAVEFORM SHOULD BE WITHIN TOLERANCES SHOWN IN FIG. C

SET PULSE SELECT SWITCH ON PULSE SIMULATION BOX TO 3. OBTAIN OSCILLOSCOPE TRACE AS PREVIOUSLY, BY DEPRESSION OF SW1.

OBSERVE THAT 3 PULSES ONLY ARE PRESENT ON THE TRACE. THE RIGHT HAND PULSE OF FIG. C SHOULD NOW BE MISSING.

SET PULSE SELECT SWITCH TO 2, 1 AND 0 AND OBSERVE CORRESPONDING NUMBER OF PULSES APPEARING ON THE OSCILLOSCOPE, WHILST UTILISING BIAS SWITCH AND OSCILLOSCOPE AS PREVIOUSLY.

SWITCH OSCILLOSCOPE AND 28 V SUPPLY OFF AND REMOVE TEST CONNECTIONS TO PULSE SIMULATION BOX.

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					271				
APP									

GRAVINER LIMITED COLNBROOK ENGLAND

DATA SHEET No 0 5310

QUALITY CONTROL DATA SHEET

SHEET No 28 | No OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.E.D.S. CONTROL UNIT (53813-204-SYSTEM B)

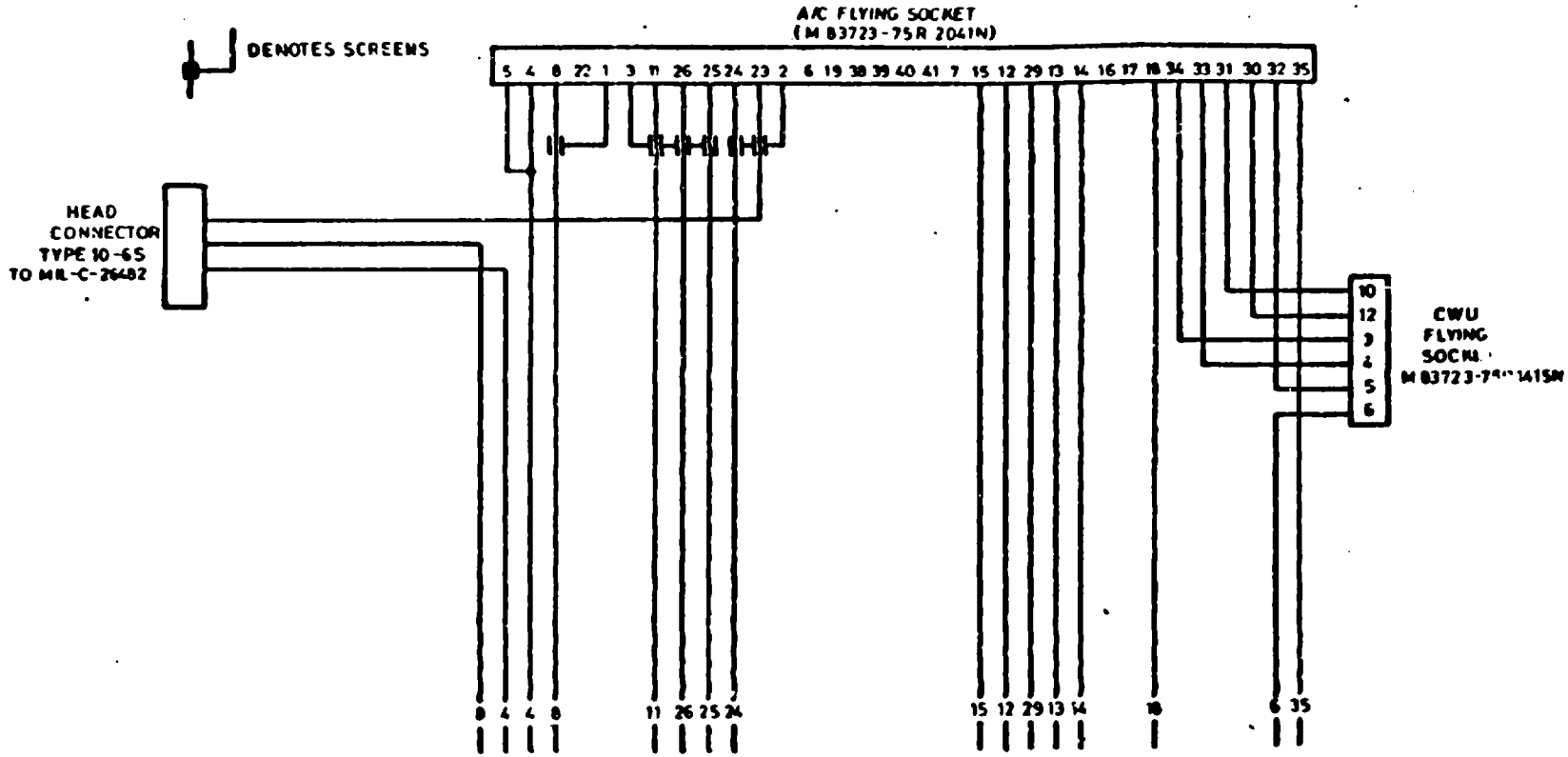


FIG. 1

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD									
APP									

GRAVIN LIMITED COLNBROOK ENGLAND		DATA SHEET No	05310
QUALITY CONTROL DATA SHEET		SHEET No 29	No OF SHEET
TITLE:	ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT (53813-204 SYSTEM B)		

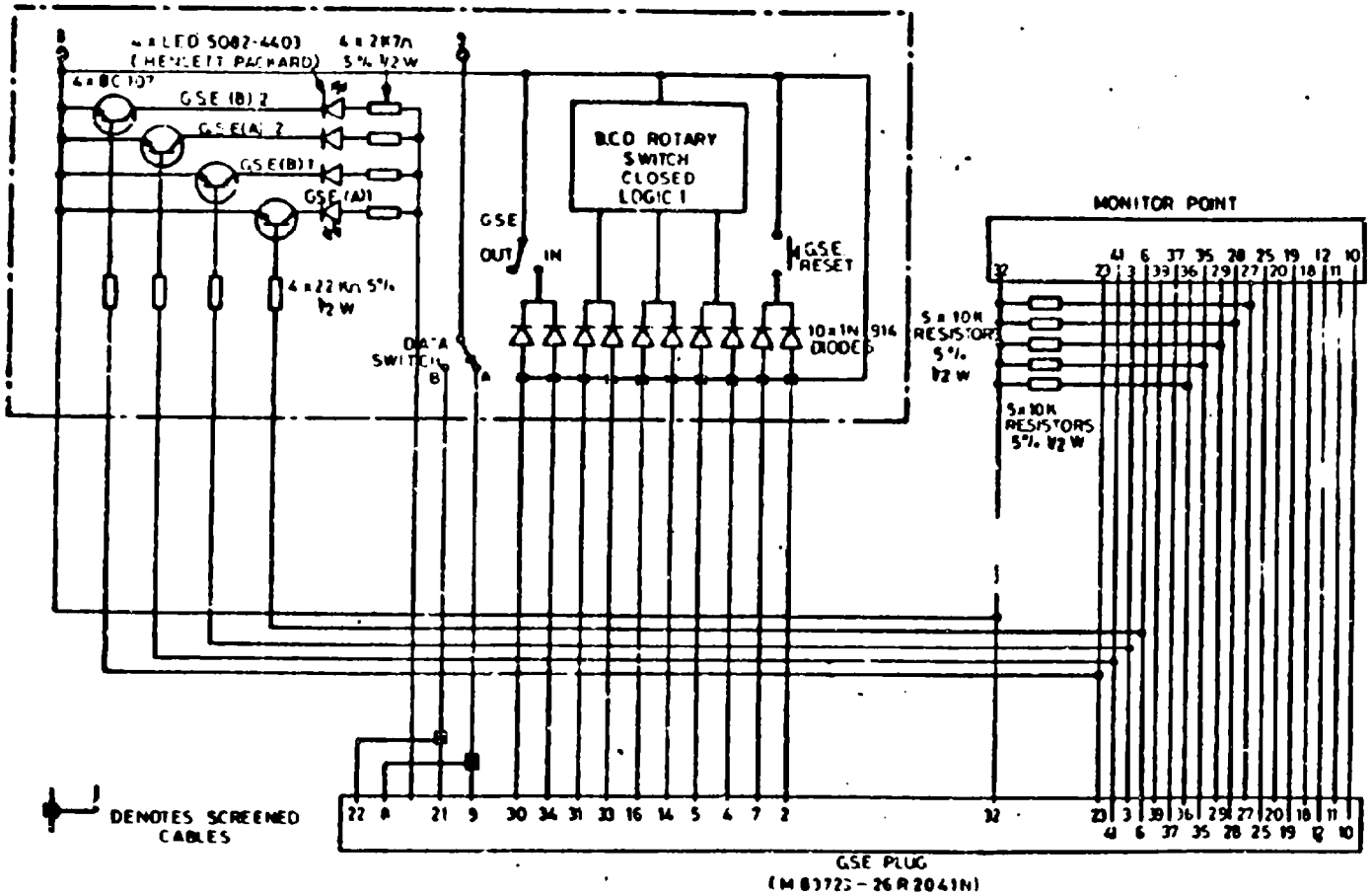
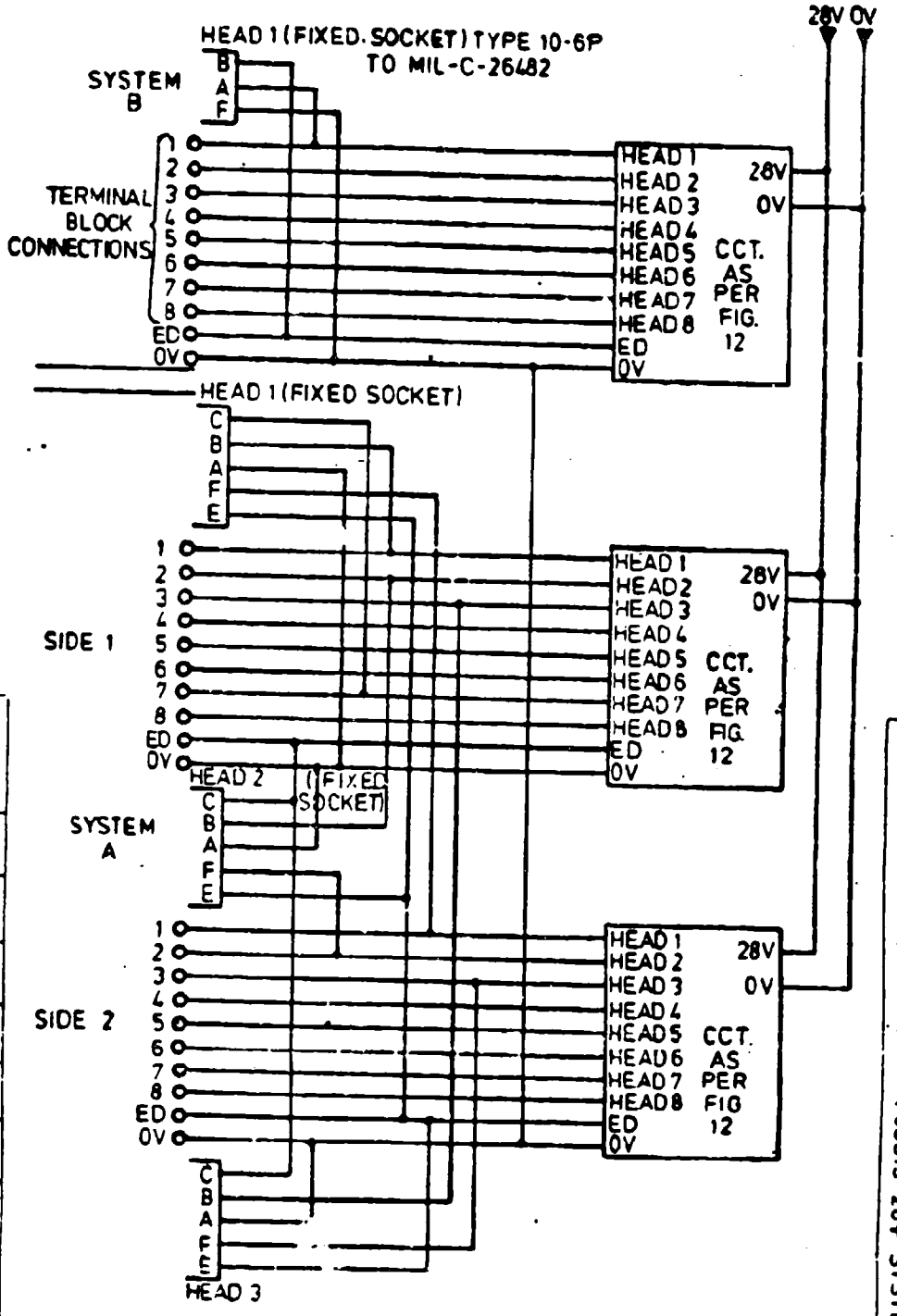


FIG. 2

GROUND SUPPORT CONTROL BOX
& CABLE HARNESS ASSEMBLY

ISSUE	A								
DRGD									
COMPILED	P.S.								
CKD									



HEAD SIMULATION UNIT

ISSUE	MOD	COMP...ED	CKD
A		P.S.	

F.S.J.

TITLE: ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT (53813-204 SYSTEM B)

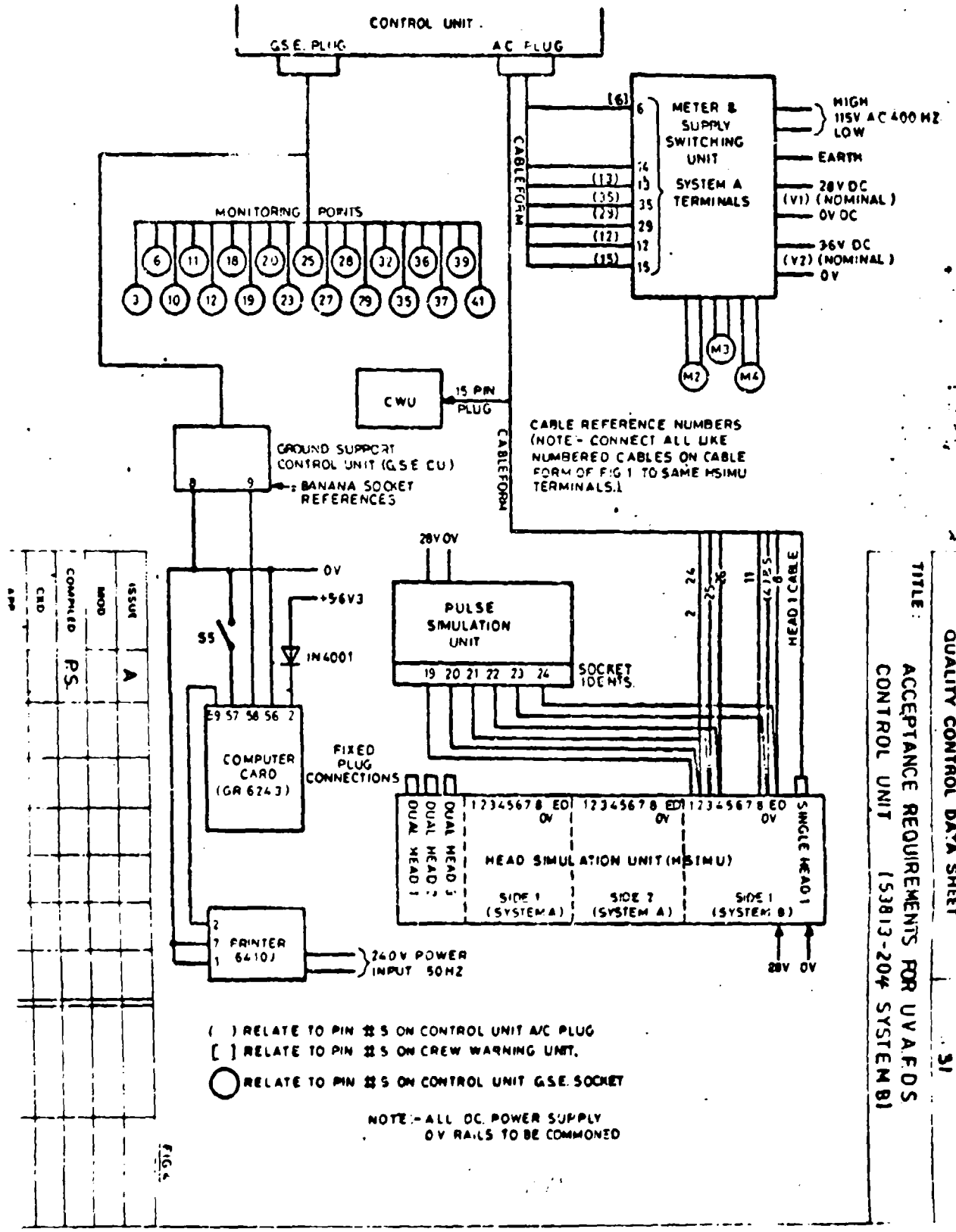
GRAVER LIMITED COLNBROOK ENGLAND

QUALITY CONTROL DATA SHEET

DATA SHEET No. 0530

SHEET No. 30

No. OF SHEETS



TITLE: ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT (53813-204 SYSTEM B)

GRANGER LIMITED COMMONDALE ENGLAND

QUALITY CONTROL DATA SHEET

DATA

SHEET No. 51

No. OF SHEETS

Q 530

LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310
QUALITY CONTROL DATA SHEET	SHEET No. 32 / No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)

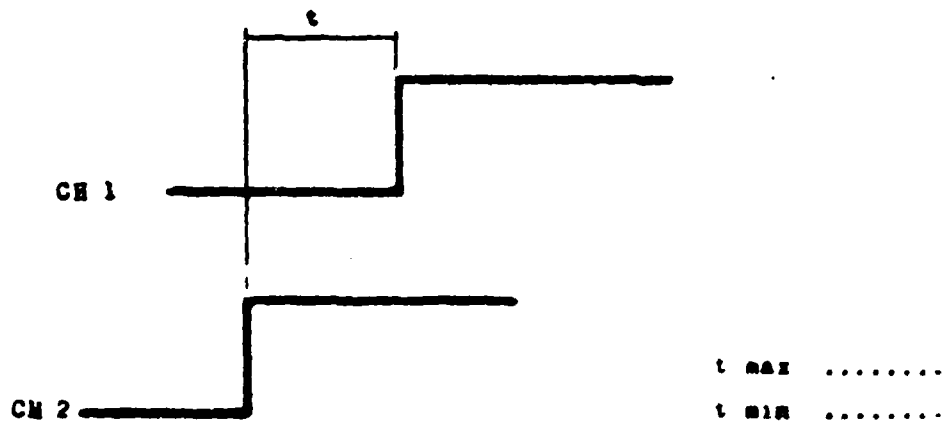


Figure 5

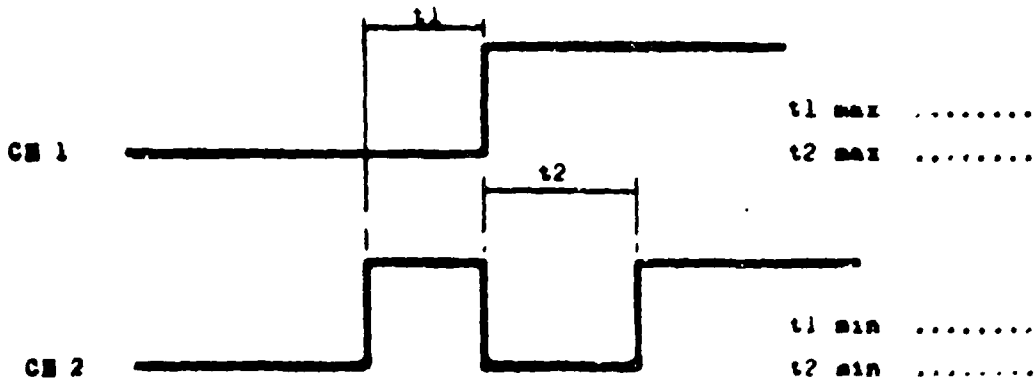


Figure 6

ISSUE	A								
MOD									
COMPILED	P.S								
CHD									
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No: Q 5310	
QUALITY CONTROL DATA SHEET	SHEET. No. 33	No. OF SHEETS

TITLE: ACCEPTANCE REQUIREMENTS FOR AFDS CONTROL UNIT (53813-204 SYSTEM B)

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->
GAUTIL V. 4
->!84400
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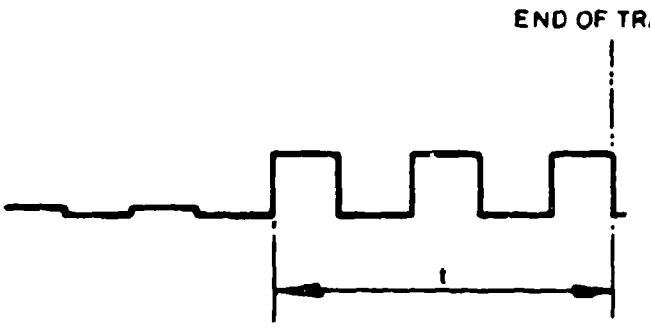
FIGURE 7

ISSUE	A								
MOD									
COMPILED	DS								
CKD									
APP									

GRAVINER LIMITED, COLNBROOK, ENGLAND.	DATA SHEET No. Q 5310	
QUALITY CONTROL DATA SHEET	SHEET No. 34	No. OF SHEETS

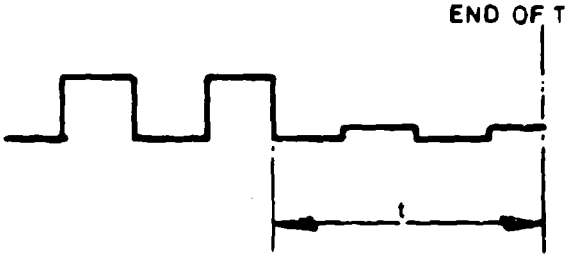
TITLE: ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)



t MAX. .....

t MIN. .....

FIG. 8



t MAX. .....

t MIN. .....

FIG. 9

ISSUE	A								
MOD									
COMPILED	P.S.								
CKD					278				
APP									

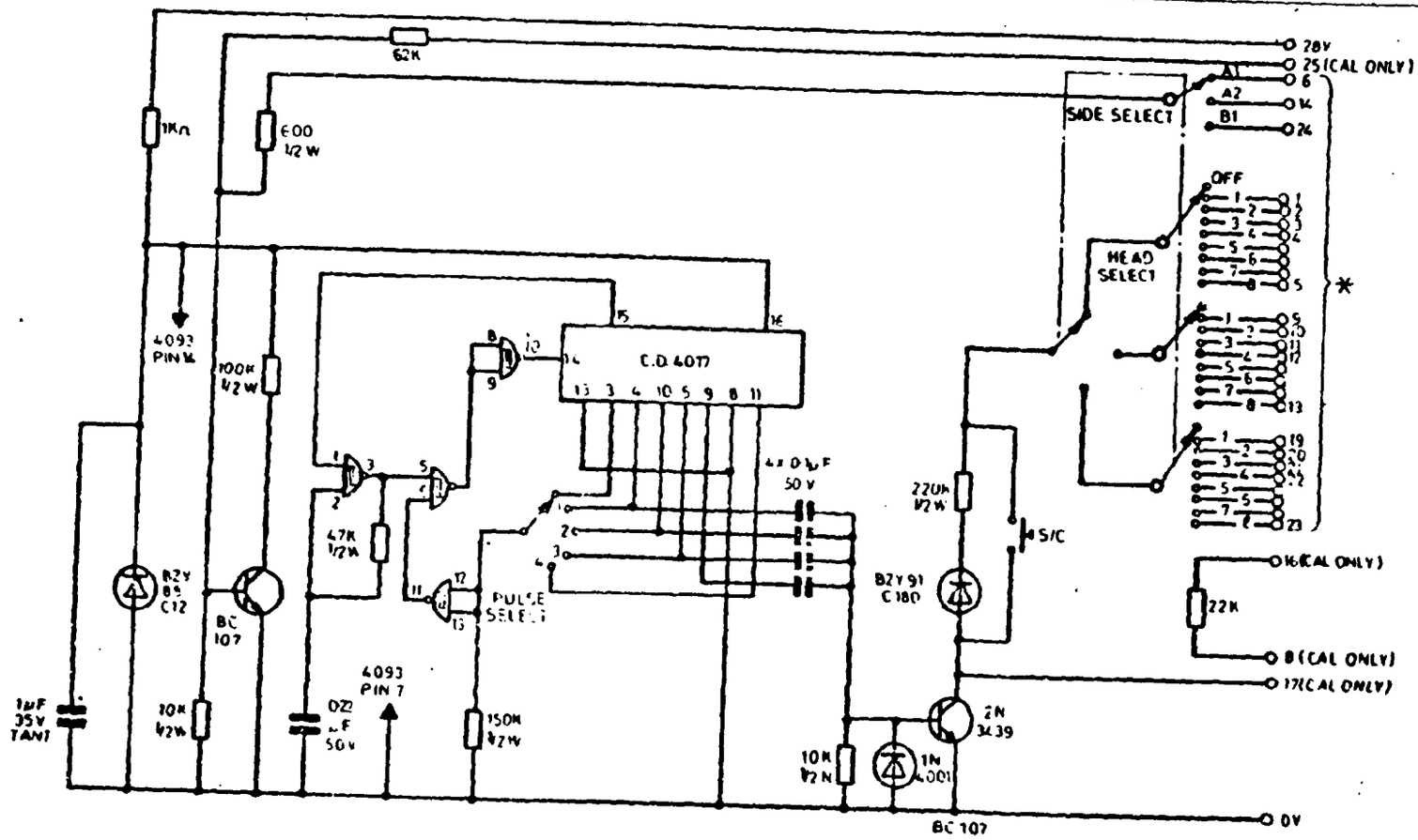
GRAVINER LIMITED CONNAUGHT ENGLAND

DATA SHEET No 0 5310

QUALITY CONTROL DATA SHEET

SHEET No 35 No OF SHEETS

TITLE ACCEPTANCE REQUIREMENTS FOR U.V.A.F D.S. CONTROL UNIT (53813-204 SYSTEM B)



CD4053 * DENOTES D SOCKET CONNECTIONS

PULSE SELECT UNIT

ISSUE	A
MOD	
COMPILED	P.S.
CKD	

FIG. 10

TITLE ACCEPTANCE REQUIREMENTS FOR U.V.A.F.D.S. CONTROL UNIT (53813-204 SYSTEM B)

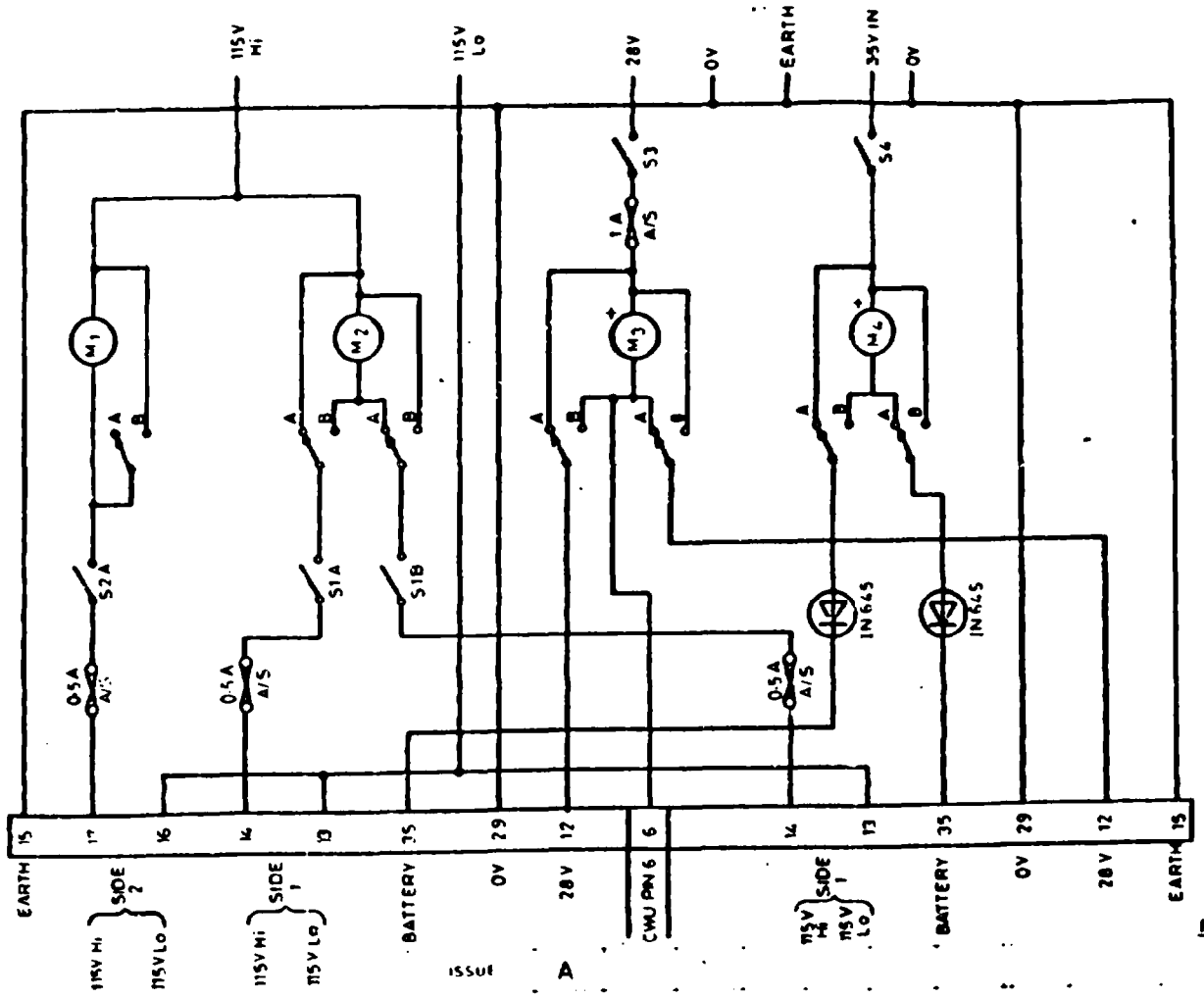
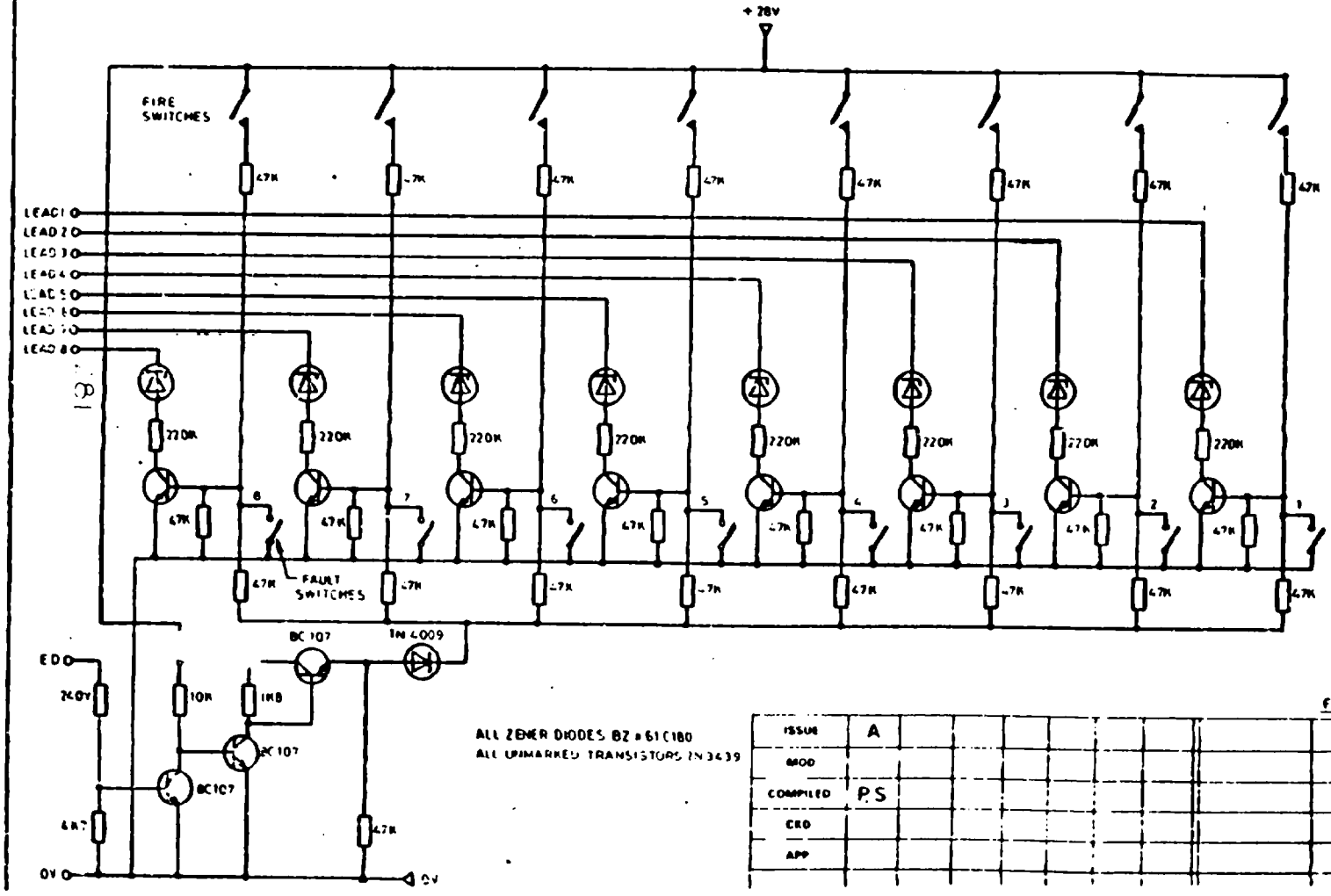


FIG. 11

CIRCUIT DIAGRAM FOR METER & SUPPLY SWITCHING UNIT

ISSUE	A
MOD	
COMPILED	P.S.
CHD	
APP	

GRAVISER LIMITED COLNBROOK ENGLAND	DATA SHEET No. 0 5310	
QUALITY CONTROL DATA SHEET	SHEET No. 37	No. OF SHEETS
TITLE: ACCEPTANCE REQUIREMENTS FOR UVAFDS CONTROL UNIT (53813-204 SYSTEM B)		



ALL ZENER DIODES BZ x 61 C180
ALL UNMARKED TRANSISTORS 2N3439

FIG. 12

ISSUE	A								
MOD									
COMPILED	P.S								
CKD									
APP									

APPENDIX B-2

APPROVAL TEST SCHEDULE ATS 52

GRAVINER LIMITED

ATS.No.52

Test Schedule
for
Ultra-Violet
Advanced Fire Detection System

85 Compiled by. R.V.enay

APPROVALS ENGINEER.

DATE. 26.5.78.

Test Schedule
for
Ultra-Violet
Advance Fire Detection System

Amendment Record

Issue No.	Page No.	Para.No.	Amendment	Date
1			Introduction	26.5.78.
2	Part 1		)	27.6.78.
	Part 2		) Revised	
	Part 3		)	
	1	4.2.1.	Added	
		4.2.2.	Added	
	2	4.3.4.	Revised	
3	Part 1		) Reference to TSO-C11(d) deleted.	11.1.79.
	Part 3		) TSO-C79 added.	
	Part 4	Para.4.5.3.	)	
4	Part 4	Para.4.4.	Revised	26.3.79.
		Para.4.6.	Test Plan added.	
5	Part 4	All	Revised	10.9.79.

CONTENTS

PART 1.

List of related documents applicable to this schedule

SOR.078104	General Dynamics. Statement of Work.
MIL-STD-810C	Environmental Test Methods.
MIL-STD-461	Electromagnetic Interference Requirements.
MIL-D-27729A	Detecting Systems, Flame and Smoke, Aircraft and Aerospace Vehicles.
MIL-W-25038B	Wire, Electrical, High Temperature and Fire Resistant. Aircraft.
TSO.C79	Fire Detectors Radiation Sensing Type
MIL-STD-704A	Electric Power Aircraft; characteristics and utilisation of.

PART 2

Description

The Ultra Violet Advanced Fire Detection System is intended for use in high performance aircraft to detect engine/nacelle fires.

The multi-channel system comprising, Computer Control Unit (C.C.U.), Crew Warning Unit (C.W.U.) and up to 8 Detector Units shall detect aircraft engine/nacelle fires within one second.

Two systems are proposed :

System 'A' shall include the following features :-

- Automatic Self Test
- Fault Discrimination Capability
- Fault Maintenance Read Out and
- Manual Confidence Test.

The simplified System 'B' shall incorporate Manual Test only.

PART 3

Test Equipment

The following test equipment shall be used where necessary to carry out the tests as detailed in Part 4 of this schedule.

Temperature and Humidity tests shall be carried out using "Montford Climatic Chamber" Type PHX73/RR/H/FFF/AUTO/CAM.
Temperature measurement shall be by "Comark Electronic Digital Thermometer with an accuracy of ± 0.1% of reading.

Altitude testing shall be carried out in "Graviner Altitude Chamber", satisfying the requirement of MIL-STD-810C, Method 50 1.1. Proc.I. Pressure levels shall be measured using suitable pressure and vacuum gauges with an accuracy of ± 2% of reading.

Sand and Dust testing shall be carried out using "Graviner Sand and Dust Chamber", satisfying the requirements of MIL-STD-810C Method 510.1. Proc.I.

Fungus Resistance Tests shall be carried out using "Hedinair Mould Growth Cabinet" satisfying the requirements of British Standard 3S.2011, Part J.

Salt, Fog testing shall be carried out using "Graviner Salt Spray Chamber", satisfying the requirements of MIL-STD-810C Method 509.1. Proc.I.

Acceleration testing shall be carried out using "Graseby Centrifuge" Type G.W.3.

Fire Resistance testing shall be carried out using a 6" x 1100°C Torch to Specification TSO C79, Figure No.2.

All pressure and vacuum gauges used shall be calibrated to the requirements of British Standard BS.1780.

All electrical instrumentation used shall be calibrated to the requirements of British Standard BS.89.

4. Approval Tests

4.1. Examination of Product

4.1.1. Weight

The weight of all system components submitted for approval testing shall be checked and recorded.

4.1.2. Size

The dimensions of all system components submitted for approval testing shall be checked to ensure conformity with the relevant drawings.

4.1.3. Visual Examination

All system components submitted for approval testing shall be examined for correctness of marking, workmanship and visible defects.

4.1.4. Centre of Gravity

The centre of gravity for each of the system components shall be established using the "knife edge method".

4.2. Electrical Tests

4.2.1. Voltage Supplies

The system shall operate from nominal 115 volt 400 Hz and 28 volt d.c. power supplies in accordance with MIL-STD-704A, Equipment Category B, Emergency supply conditions.

A.C. Voltage Limits. 102 - 124 volts. 380 - 420Hz

D.C. Voltage Limits. 16 - 29 volts.

System A

C.C.U. 115v, 400Hz and 28v.d.c.

C.W.U. 28v.d.c.

System B

C.C.U. 115v 400Hz

C.W.U. 28v.d.c.

Voltage Transients

The system shall be unaffected by exposure to the following input voltages in accordance with MIL-STD-704A.

Voltage	Duration
190	0.10 second
174	0.40 second
139	4.00 seconds
137	5.00 seconds

After the transient test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3. and the acceptance requirements of the relevant Q. Data Sheet detailed in paragraph 4.4.

Supply Interruption

The effect of voltage supply interruption to the system shall be established.

This test shall be carried out as part of Voltage Transient testing in accordance with MIL-STD-704A.

4.2.2. Insulation Resistance

C.C.U. Using a 30 volt d.c. source, the leakage current between all unearthed terminal pins and case shall not exceed 1.5 μA.

C.W.U. Using a 500 volt d.c. insulation tester the resistance measured between all unearthed connector pins and case shall not be less than 20 Megohms.

Detector Unit Using a 500 volt d.c. insulation tester the resistance measured between all unearthed connector pins and case shall not be less than 20 Megohms.

4.2.3. Electromagnetic Interference

The complete system shall be tested to comply with the electromagnetic interference requirement of MIL-STD-461.

Testing shall be carried out in accordance with "EMC Test Plan" for Ultra-Violet Advanced Fire Detection System.

4.2.4. Functional Test

4.3. Performance Tests

The following tests, paras. 4.3.2., 4.3.3., and 4.3.4. shall be carried out in accordance with MIL-D-27729A, paras. 3.11.2., 3.11.3., and 3.11.4. modified as follows :-

4.3.1. Standard Test Flame

The Standard Test Flame shall be produced by burning JP-4 fuel or 100 octane gasolene in a 5 inch diameter pan, in an environment in which the airflow does not exceed 10 feet per second.

A U.V. source with the equivalent radiation distribution and intensity may be substituted.

The U.V. source shall satisfy the following requirements :-

When measured at the front face of the detector, irradiance, at wavelength 220nm and bandwidth less than 10 nm, shall not be greater than 3×10^{-10} watts/cm^2.

Irradiance at any other wavelength between 270 and 320 nm of a bandwidth less than 10nm shall not be greater than 10^{-7} watts/cm^2.

This satisfies the requirements of a 5" pan fire at a distance of four feet.

4.3.2. Response Time

The system shall respond within 1 second when one Detector Unit is exposed to the Standard Test Flame of para. 4.3.1. at a distance of four feet while simultaneously being exposed to direct unfiltered midday (± 1 hour) sunlight, or its equivalent in U.V. spectral radiation and intensity.

The Detector Units shall be tested independently at the supply voltage extremes detailed in para. 4.2.1.

4.3.3. Reset Time

After having been exposed to the Standard Test Flame of para. 4.3.1. for a period of one minute, the flame shall be cut off from the view of the Detector Unit. The time taken for the warning to clear shall not exceed 1.5 seconds. The Detector Unit shall continuously be exposed to direct sunlight during this test. The test shall be carried out at supply voltage extremes detailed in para. 4.2.1.

4.3.4. Viewing Field

The Detector Unit shall have a viewing field of at least 80°. This shall be achieved by exposing the Detector Unit to the Standard Test Flame of para. 4.3.1. in the following attitudes and at a distance of four feet.

(a) Detector Unit on a line 40° above the flame centre viewing along a horizontal axis.

(b) Detector Unit on a line 40° below the flame centre viewing along a horizontal axis.

(c) Detector Unit on a line 40° to right of flame centre viewing along a horizontal axis.

(d) Detector Unit on a line 40° to left of flame centre viewing along a horizontal axis.

The system shall meet the response time requirements of para. 4.3.2., and shall be tested at voltage extremes detailed in para. 4.2.1.

4.3.5. False Clearing of Alarm

With the system in a warning condition after having been exposed to the Standard Test Flame of para. 4.3.1., no reset shall occur when 50% of the Test Flame is masked from the view of the Detector Unit. This test shall be carried out at supply voltage extremes detailed in para. 4.2.1.

4.4. Environmental Tests (Sequential)

Environmental tests shall be carried out, where possible, in the following sequence as defined by MIL-STD-810C, paragraph 4, Table I for Group 2 equipment, sequence (a).

Prior to any environmental testing, all equipment shall meet the Acceptance Test Requirements detailed in the following documents :-

Crew Warning Unit - Graviner Q.Data Sheet No.Q.5305.

Computer Control Unit - Graviner Q.Data Sheet No.Q.

Detector Unit - Graviner Q.Data Sheet No.Q.5304.

These tests shall also be carried out where detailed after environmental tests.

In addition to the above tests, where possible, during the following environmental tests a minimum of three fire response checks shall be carried out in accordance with paragraph 4.3.2.

These checks shall be carried out, shortly after the beginning of the test, at the mid point and just prior to completion.

4.4.1. High Temperature

The component parts of the system shall meet the High Temperature requirements of MIL-STD-810C, Method 501.1, Procedure I, and shall be unaffected by 48 hours at the following temperatures :-

Detector Unit	260°C
Computer Control Unit	85°C
Crew Warning Unit	71°C

The equipment shall be energised throughout the test. After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.2. Low Temperature

The component parts of the system shall meet the Low Temperature requirements of MIL-STD-810C, Method 502.1, Procedure I and shall be unaffected by 24 hours at a temperature of -54°C.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.3. Temperature Shock

The component parts of the system shall meet the Temperature Shock requirements of MIL-STD-810C, Method 503.1, Procedure I, and shall be unaffected by rapid transfer between the following temperatures :-

Detector Unit	260°C/-54°C/260°C
Computer Control Unit	85°C/-54°C/85°C
Crew Warning Unit	71°C/-54°C/71°C

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.4. Altitude

The component parts of the system shall meet the Altitude requirements of MIL-STD-810C, Method 500.1, Procedure I and shall be unaffected by periods of 1 hour each at pressures equivalent to 70,000 feet (1.33 in Hg) and -1000 feet (30.12 in Hg).

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.5. Temperature/Altitude

The component parts of the system shall meet the Temperature/Altitude requirements of MIL-STD-810C Method 504.1, Procedure I, for continuously operating equipment Category 6, and shall be unaffected by exposure to temperatures of -54°C to 71°C with altitudes up to 70,000 feet.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.6. Sand and Dust

The component parts of the system shall meet the Sand and Dust requirements of MIL-STD-810C, Method 510.1, Procedure I and shall be unaffected by 28 hours exposure to Sand and Dust.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.7. Humidity

The component parts of the system shall meet the Humidity requirements of MIL-STD-810C, Method 507.1, Procedure I and shall be unaffected by the following test :-

10 cycles of -

2 hours to 65°C with 95% RH
6 hours at 65°C with 95% RH
16 hours at 30°C with 85% RH

After the 240 hour test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.8. Fungus Resistance

The component parts of the system shall meet the Fungus Resistance requirements of MIL-STD-810C, Method 508.1, Procedure I. The equipment and suitable control items shall be sprayed with a mixed spore suspension containing the following cultures :-

Aspergillus niger
Aspergillus flavus
Aspergillus versicolor
Pencillium funicolosum
Chaetomium globosum

The test item shall then be stored under cyclic temperature and humidity condition to include 20 hours at 30°C and 95% RH followed by 4 hours at 25°C with 100% RH.

After 7 days the control items shall be examined and if satisfactory fungus growth is evident the test shall continue for 28 days.

After the test the equipment shall be examined for fungus growth and shall then meet the performance requirements of paras. 4.3.2. 4.3.3 and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.9. Salt Fog

The component parts of the system shall meet the Salt Fog requirements of MIL-STD-810C, Method 509.1, Procedure I and shall be unaffected by 48 hours exposure to a Salt Fog from a 5%, by weight, Sodium Chloride solution.

After exposure, to aid examination, the equipment may be washed in running water, not exceeding 38°C, and then stored at ambient conditions for 48 hours.

The equipment shall then meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.10. Acceleration

The component parts of the system shall meet the acceleration requirements of MIL-STD-810C, Method 513.2, Procedure I, and shall be unaffected by acceleration levels up to 25.5g.

Acceleration shall be applied in each of three mutually perpendicular planes, in both forward and reverse directions, and shall be held for a minimum of 60 seconds in each direction.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheets detailed in paragraph 4.4.

4.4.11. Explosive Atmosphere

Not applicable.

4.4.12. Mechanical Shock

The component parts of the system shall meet the shock requirements of MIL-STD-810C, Method 516.2., Procedure I, and shall be unaffected by shock loads of 20.0g.

The equipment shall be subjected to 18 shock pulses of 20.0g for a duration of 11.0 milliseconds. 3 shocks in each of 3 mutually perpendicular planes in both forward and reverse directions.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.13. Vibration

The component parts of the system shall meet the vibration requirements of MIL-STD-810C, Method 514.2.

The equipment shall be subjected to the vibration test comprising a Resonance Search, Functional Test and Endurance Test in each of 3 mutually perpendicular axes over the frequency range of 5-2000 Hz.

Resonance Search

The equipment shall be subjected to a sinusoidal resonance search in each of 3 mutually perpendicular axes, over the frequency range of 5-2000 Hz in accordance with MIL-STD-810C, Method 514.2 Procedure I, at the following vibration levels :-

Detector Unit

Figure 514.2-2, Curve G for equipment located in engine compartments.

5-14 Hz	0.10 inch. double amplitude
14-23 Hz	1.0g acceleration
23-90 Hz	0.036 inch. double amplitude
90-2000 Hz	15.0g acceleration.

C.C.U. and C.W.U.

Figure 514.2-2, Curve J for equipment mounted in forward fuselage.

5-14 Hz	0.10 inch. double amplitude
14-23 Hz	1.0 g acceleration
23-52 Hz	0.036 inch. double amplitude
52-2000 Hz	5.0g acceleration.

Functional and Endurance Test.

The equipment shall be subjected to random vibration in each of 3 mutually perpendicular axes over the frequency range of 15-2000 Hz in accordance with MIL-STD-810C, Method 514.2, Procedure 1A as detailed in Figures 514.2-11A and 514.2-2A at the following vibration levels :-

Equipment	Test Levels		
	Maximum P.S.D. g^2/Hz		
	Endurance 1 Hour	Performance 1 Hour	A
C.C.U. and C.W.U.	0.033	0.025	0.02
Detectors	0.33	0.25	0.04

The endurance test may be eliminated if the Functional Test is run for 3 hours.

The equipment shall meet the performance requirements of paras. 4.3.2. and 4.3.3., during the test.

On completion of the vibration test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.4.14. Acoustic Vibration

The Detector Unit shall meet the Acoustic Vibration requirements of MIL-STD-810C, Method 515.2, Procedure I and shall be unaffected by 30 minutes exposure to a sound pressure level of 150 dB.

After the test the Detector Unit shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of Q.Data Sheet No. Q.5304.

4.5. Environmental Tests (Non Sequential)

4.5.1. Fuel and Oil Immersion

The Detector Unit shall be immersed in JP-4 Fuel, DERD 2454, (MIL-T-5624G) and then allowed to drain for a period of 1 minute. No cleaning shall be accomplished prior to conducting the performance tests of paras.4.3.2. and 4.3.3.

This procedure shall be repeated for the following fluids :-

Turbine Oil	DERD 2497	(MIL-L-23699)
Hydraulic Fluid	DTD 585	(MIL-H-5606)

After the test the Detector Unit shall meet the Acceptance requirements of Q.Data Sheet No.Q.5304.

4.5.2. Rain Spray

The components parts of the system shall meet the Rain Spray requirements of MIL-STD-810C, Method 506.1., Procedure I, and shall be unaffected by a minimum of 30 minutes exposure to rain spray at the rates detailed in the specification.

After the test the equipment shall meet the performance requirements of paras. 4.3.2., 4.3.3., and Acceptance requirements of the relevant Q.Data Sheet detailed in paragraph 4.4.

4.5.3. Fire Resistance

Two Detector Units shall be used for this test. One Detector Unit, connector and 6" of wiring shall be immersed in a 6" x 1100°C flame. The other Detector Unit shall be positioned so as to detect the flame but shall not be immersed in the flame. The 6" x 1100°C flame shall be supplied by a burner as detailed in Figure No.2 of MIL-W-25038B. An equivalent burner which may be used for the test is described in Fig. No.2 of Specification TSO.C79.

The Detector Unit shall be immersed in the 6" x 1100°C flame for a period of 5 minutes.

The system shall indicate a fire within 1 second after exposure to the flame and shall continue to indicate for the entire 5 minute exposure.

After the 5 minute period the flame shall be extinguished and the system shall indicate "fire out" within 1.5 seconds.

APPENDIX B-3

1. EMI TEST PLAN

2. RADIO INTERFERENCE REPORT NO. LM 80876

E.M.I. TESTS FOR ADVANCED AIRCRAFT FIRE DETECTION SYSTEM

CONTENTS

1. FOREWORD

1.1. Testing Aims

The system to be tested consists of one Control Unit type 53813-203, one Control Unit type 53813-204, one Crew Warning Unit type 53813-202, five Dual Detectors type 53522-011, five Single Detectors type 53521-012. The tests to be performed are to demonstrate the system compliance to MIL-STD-461A, NOTICE 3, CLASS A1, and MIL-STD-704A.

1.2. Test Methods

1. CE01 Conducted Emission Power Leads 30 Hz to 20K Hz. (Performed for data purposes only).
2. CE02 Conducted Emission Signal and Control Leads 30 Hz to 20K Hz.
3. CE03 Conducted Emission Power Leads 100K Hz to 50M Hz. (Data to be collected from 14K Hz to 100K Hz for customer information).
4. CF04 Conducted Emission Signal and Control Leads 20K Hz to 50M Hz.
5. CS01 Conducted Susceptibility Power Leads 30Hz to 50Hz.
6. CS02 Conducted Susceptibility Power Leads 50K Hz to 400M Hz (Note 1)
7. CS06 Conducted Susceptibility SPIKE Power Leads.
8. RE02 Radiated Emission Electric Field 14K Hz to 10G Hz.
9. RS02 Radiated Susceptibility Magnetic Induction Field (Note 3).
10. RS03 Radiated Susceptibility Electric Field 14K Hz to 1G Hz. (Note 2)
11. Transient Acceptance to MIL-STD-704A. (Category B).
12. Chattering Relay Test (See Section 5).

NOTE 1

Signals 50K Hz - 200 M Hz Modulated on 1 K Hz sine wave (80% modulation). Signals 200 M Hz - 400 M Hz Modulated on 1 K Hz square wave (100% Modulation).

NOTE 2

Signals 50 K Hz - 200 M Hz Modulated on 1 K Hz sine wave (80% modulation). Signals 200 M Hz - 1 G Hz Modulated on 1 K Hz square wave (100% modulation).

NOTE 3

The procedures and limits of method RS02(a) and (b) shall apply except that the voltage E of part (b) shall be 400 volts across 5 ohms.

1.3. Order of Tests

a) CE03, b) CE04, c) CE01, d) CE02,

e) CS01, f) CS02, g) RS03, h) RE02.

j) Transient acceptance

k) CS06

l) RS02

m) Chattering relay test.

1.4. Test Controls

All test set ups and techniques are subject to control by MIL-STD-462, Notice 2.

2. TEST FACILITY

2.1. Test Facility for Test Methods 1 to 11

2.1.1. Tests will be performed in screened rooms. All power lines entering screened room will be filtered.

2.1.2. All test equipment will be housed in adjoining screened room for radiated tests. All power lines entering screened room will be filtered.

2.1.3. All connections between screened rooms for these tests will be made via coaxial leads and connectors or via an interconnecting screened tube.

2.1.4. Coaxial cable insertion loss graphs will be included in the test report where measurements above 100M Hz are recorded.

2.1.5. Ambient Interference Measurements

Prior to each test an ambient calibration for Conducted and Radiated Emission will be performed with the power switches on and the supply line loaded with an impedance equivalent to the system under test.

2.1.6. The test facility shall supply a list of what equipment is used in each test.

2.1.7. The test facility shall supply detailed descriptions of all test settings and methods according to MIL STD 462 guide lines.

2.2. Test Facility for Test Methods 7 and 12

2.2.1. Description of circuit used to produce pulses that are applied to A.C. Aircraft supplies for test method CS06.

2.2.1.1. The equipment used shall consist of a controlled timing current which energises a transient voltage pulse generator having a source impedance of 50 ohm. The pulse is superimposed on the supply so that it coincides with the peak of the 400 Hz waveform either positive or negative going.

2.2.2. The test facility shall supply a list of what equipment is used in each test.

2.2.3. The test facility shall supply detailed descriptions of all test set ups and methods according to MIL STD 462 guide lines.

3. CALIBRATION OF TEST EQUIPMENT

3.1. Calibration

All equipment used shall be calibrated in accordance with MIL-C-45662 at intervals of six months.

3.2. Accuracy

Frequency	When a more accurate measurement than $\pm$ 2% of the indicated frequency of the EMI Receiver is required a frequency counter will be used.
Amplitude	All amplitude measurements will be within $\pm$ 2 dB of the indicator value.

4. OPERATION OF THE SYSTEM AND OTHER INFORMATION REQUIRED IN PERFORMING THE E.M.C. TESTS

4.1. Operation of the System

4.1.1. Condition 1 STANDBY

This condition is when the UV source is switched off and the "FIRE" and "FIRE DET FAIL" indicators are not illuminated. For CE03 and RE02 a transient condition should be applied by depressing fire test switch periodically during test at a rate of at least 3 operation/ resets per octave.

4.1.2. Condition 2 FIRE

This condition is when the UV source is switched on and the "FIRE" indicators are illuminated on the crew warning unit.

4.1.3. Test Facility

In condition 1 a confidence check can be carried out by depressing the "FIRE DET TEST" switch which illuminates both "FIRE"Indicators, and depressing the "FAIL IND TEST" switch which illuminates the "FIRE DET FAIL" indicators.

4.2. Susceptibility Criteria

The criteria for Susceptibility/Non-Susceptibility will be as follows:-

Condition 1, illumination of any Crew Warning Unit "FIRE" and "FIRE DETECT FAIL" indicators.

Condition 2, cancellation of either "FIRE" indicators.

General, permanent extinction of head emitters when fire test button is depressed.

4.3. Signal and Control Leads to be measured for Conducted Emission

The following leads will be classified as signal and control leads for the Electromagnetic Compatibility Tests:

All leads from Detectors to Control Unit A.

All leads from Detectors to Control Unit B.

Lead from Crew Warning Unit Pin 1 to Control Unit A Pin 34
Lead from Crew Warning Unit Pin 2 to Control Unit A Pin 33
Lead from Crew Warning Unit Pin 9 to Control Unit A Pin 31
Lead from Crew Warning Unit Pin 11 to Control Unit A Pin 30
Lead from Crew Warning Unit Pin 10 to Control Unit B Pin 31
Lead from Crew Warning Unit Pin 12 to Control Unit B Pin 31
Lead from Crew Warning Unit Pin 3 to Control Unit B Pin 34
Lead from Crew Warning Unit Pin 4 to Control Unit B Pin 33
Lead from Control Unit A Pin 35 to Control Unit B Pin 18

The leads will be tested as a bunch. The longest cable to a dual head will be tested. The longest cable to a single head will be tested.

4.4. Power Leads to be Tested:

The following leads will be classified as power leads for the Electromagnetic Compatibility Tests:-

115V 400 Hz.	Line to Control Unit A	Pin 14
115V 400 Hz.	Neutral to Control Unit A	Pin 13
115V 400 Hz.	Line to Control Unit A	Pin 17*
115V 400 Hz.	Neutral to Control Unit A	Pin 16*
115V 400 Hz.	Line to Control Unit B	Pin 14
115V 400 Hz.	Neutral to Control Unit B	Pin 13
28V d.c.	Positive to Control Unit A	Pin 12
28V d.c.	Negative to Control Unit A	Pin 29
28V d.c.	Positive to Control Unit B	Pin 12
28V d.c.	Negative to Control Unit B	Pin 29
28V d.c.	Positive to Crew Warning Unit	Pin 6

* Not to be monitored in CE01, 02, 03, 04 Tests.

4.5. Power Lead Test for Conducted Susceptibility

All live or positives of 4.4 (with the exception of those marked *) to be tested with respect to the relevant neutral or negatives and with respect to earth or by series injection as appropriate.

All neutrals or negatives of 4.4 (with the exception of those marked *) to be tested with respect to earth or by series injection as appropriate.

4.6. Power Lead Connections for Transient Acceptance

For purpose of transient acceptance tests power cables will be linked as follows and treated as a single cable.

1) 115V 400 Hz. Line to Control Unit A Pin 14
115V 400 Hz. Line to Control Unit A Pin 17
115V 400 Hz. Line to Control Unit B Pin 14
are all linked together.

2) 115V 400 Hz. NEUTRAL to Control Unit A Pin 13
115V 400 Hz. NEUTRAL to Control Unit A Pin 16
115V 400 Hz. NEUTRAL to Control Unit B Pin 13
are all linked together.

3) 28V d.c. POSITIVE to Control Unit A Pin 12
28V d.c. POSITIVE to Control Unit B Pin 12
28V d.c. POSITIVE to crew warning unit Pin 6
are all linked together

4) 28V d.c. NEGATIVE to Control Unit A Pin 29
28V d.c. NEGATIVE to Control Unit B Pin 29
are all linked together.

4.7. Grounding

4.7.1. The Control Unit and detectors shall be bonded to the Ground plane via short brass straps or brading straps, using dagger pins and retaining screws to simulate aircraft installation.

4.7.2. Bonding between the control unit and the ground plane must be equal to or less than 2.5 milliohms DC resistance, and must be recorded as data in the report.

4.7.3. The Control Unit Pin 15 will be bonded to the Ground plane via the shortest practical length of wire.

4.7.4. The negative lead of the 28V d.c. supply will be bonded to the Ground plane from the screened room wall terminal.

4.8. Lead Length

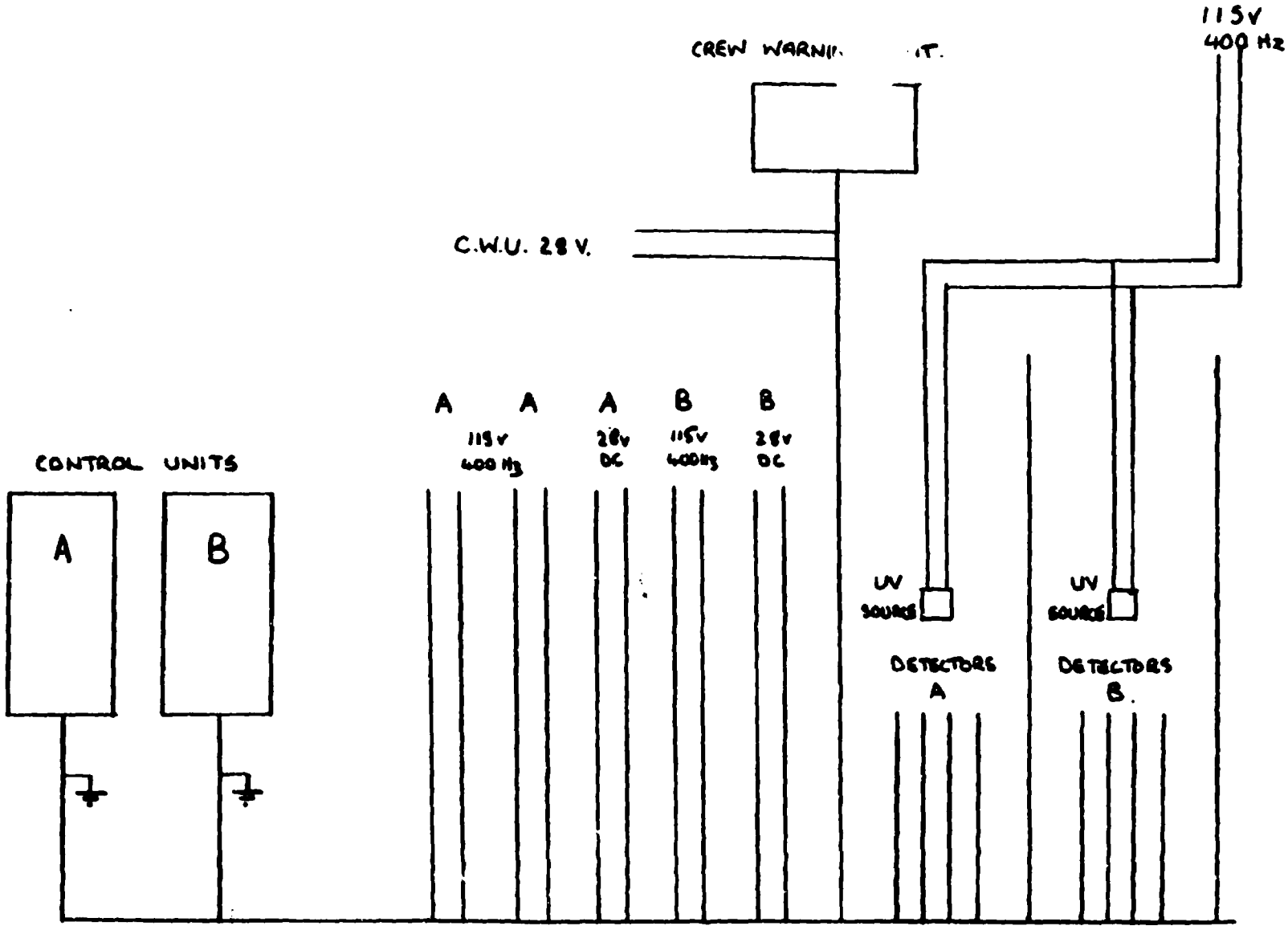
4.8.1. The screened leads from the control unit to the detectors will be 60 ft on one detector and 20 ft on the remaining four detectors for each system.

4.8.2. The leads from the control units to the crew warning unit shall be 15 ft.

4.8.3. The power leads to the control units will be a nominal 3 ft long for the conducted tests and 6 ft for radiated tests.

5.0. Chattering Relay Test

No change in indications, malfunctions or degradation in performance shall be indicated in any equipment and/or its load when exposed to an impulse type electromagnetic field generated by a type MS 25271 relay (or an acceptable equivalent) when wired for continuous operation with a switch in series with the positive side of the line from a 28V d.c. power source. No suppression components (shielding diode etc.) shall be attached to the relay or its wiring. The unshielded positive lead leaving the switch shall be laid over three sides of the test sample and then connected to the relay. The unshielded return lead from the relay shall be taped to and in parallel with input power leads, signal leads and interconnecting leads. The total length of each external wiring harness parallel with the relay circuit shall not be less than 60". The 28 volt input shall be reversed and the transient repeated.



TEST LAYOUT FIG. 1.

Lucas Aerospace
Engineering Report

Radio Interference Report No. LM 80876

GRAVINER LTD ADVANCED AIRCRAFT ENGINE

FIRE DETECTION SYSTEM.

Author P.P. Curtis Date 7-7-80
P.P. Curtis

Approved by P.D. Campbell Date 14.7.80
P.D. Campbell

Lucas Aerospace Electrical Division
Maylands Avenue Hemel Hempstead Hertfordshire England

Lucas Aerospace

Lucas Aerospace Limited
Electrical Division
Maylands Avenue
Hemel Hempstead
Hertfordshire HP2 4SP

Telephone: Hemel Hempstead 42233
Telex: 82110

TEST HOUSE CERTIFICATE

Issued Under
Defence Quality Assurance Board Approval No. 12870
Civil Aviation Authority Reference D.A.I. 1265/39

Serial No. H 1545

TO:

GRAVINER LTD
POYLE ROAD
COLNBROOK
SLOUGH SL3 OEB

CONTRACT No. 84224

RELEASE NOTE No.

File Copy

REQUIREMENTS OF CUSTOMER'S ORDER:

E.M.C. tests to MIL-STD-462 Notice 2 and MIL-STD-461A Notice 3 as detailed in Graviner Test Plan 3.3.80 Issue 4.

DESCRIPTION:

ADVANCED AIRCRAFT FIRE DETECTION SYSTEM.

REPORT: LN 80876

CERTIFICATION:

*~~Certified that tests have been carried out to the requirements of the Chief Executive, Defence Quality Assurance Board.~~

*Certified that the above mentioned ~~specimens/parts/materials~~/systems have been tested/~~examined~~ in accordance with the terms of the contract/~~order~~ applicable thereto and unless otherwise stated conform fully to the ~~standards~~/specifications quoted hereon and the requirements of the Civil Aviation Authority.
This does not guarantee the bulk of the items/~~material~~ to be of equal quality.

Date 8-5-80 Signed: [signature] 314

For and on behalf of Lucas Aerospace Ltd.

Circulation

GRAVINER 6
A.R. Sharp
File

Summary

The Graviner Advanced Aircraft Fire Detection system was tested to Test Plan 31.3.80 issue 4. The system comprised of two control units types 53813-203 and 53813-204, one Crew Warning Unit type 53813-202, five Dual Detectors type 53522-011 and five Single Detectors type 53521-012.

The tests were performed to demonstrate the system compliance to MIL-STD-461A, Notice 3, Class A1 and MIL-STD-704A.

The equipment complies with the requirements of the following tests:-

CE.01 30Hz to 20KHz Conducted Emissions Narrowband Power leads.
CE.02 30Hz to 20KHz Conducted Emissions Narrowband Signal and Control leads.
CE.03 100KHz to 50MHz Conducted Emissions Broadband and Narrowband Power leads. Condition 1 Standby, and Condition 2 fire.
RE.02 14KHz to 1GHz Radiated Emissions Broadband Condition 1 Standby.
RE.02 14KHz to 10GHz Radiated Emissions Narrowband Condition 1 Standby, and Condition 2 fire.
CS.01 Conducted Susceptibility Power leads 30Hz to 50KHz
CS.02 Conducted Susceptibility Power leads 50KHz to 400MHz
RS.03 Radiated Susceptibility 14KHz to 1GHz.

The equipment has emissions outside the specified broadband limits in the following tests:-

CE.03 Fire detect test transients.

The following leads showed transient emissions out of limit caused by the operation of the fire detect test switch on the Crew Warning Unit.

115V line Control A pin 14	7MHz, 10MHz, 15MHz and 20MHz
115V Neutral Control A pin 13	5MHz, 7MHz, 10MHz, 15MHz and 20MHz
28V dc Positive Control A	30KHz, 15KHz and 20MHz
28V dc Negative Control A	15MHz and 20MHz
115V Neutral Control B	5MHz, 7MHz, 10MHz and 15MHz
28V dc Positive Control B	7MHz, 10MHz, 15MHz and 20MHz
28V dc Negative Control B	20MHz
28V dc Positive C.W.U.	500KHz, 700KHz, 1MHz, 1.5MHz, 2.0MHz 3MHz, 4MHz, 5MHz, 7MHz, 10MHz, 15MHz 20MHz.

CE.04 20KHz to 50MHz Conducted Emissions Signal and Control leads.
Condition 1, Standby.
Bunch 1, (All leads, Detectors, Control Units, Crew Warning unit excluding Power supplies). Transient emissions caused by "detector self test check", out of limits between 450KHz and 9.5MHz.
Bunch 2, (Single detector long cable bunch). Emissions out of limit as above between 450KHz and 10.5MHz.
Bunch 3, (Dual detector long cable bunch). Emissions out of limit as above between 650KHz and 4.0MHz.

Condition 2, Fire.
Bunch 1, (All lead, detectors, Control Units, crew warning unit excluding power sup· es). Emissions caused by "detection of fire" above the limit between 450KHz and 10MHz.

Bunch 2, (Single Detector long cable bunch). Emissions out of limit as above between 500KHz and 14MHz.

Bunch 3, (Dual Detector long Cable bunch) Emissions out of limit as above between 550KHz and 8MHz.

RE.02 Radiated Emissions Electric Field 14KHz to 10GHz.

Fire Detect Transients.

The following frequencies show transient emissions out of limit caused by the operation of the fire detect test switch on the Crew Warning Unit.

20KHz, 30KHz, 45KHz, 65KHz, 80KHz, 100KHz, 150KHz, 200KHz, 1MHz, 3MHz, 4MHz, 10MHz, 40MHz and 150MHz.

Condition 2 Fire.

The radiated emissions were marginally above the limit between 14KHz and 20KHz and 5.75MHz and 6.5MHz.

The transient voltage and spike tests undertaken at Lucas Aerospace Ltd., Bradford are detailed in a separate report included within this report. See appendix No. 5.

Contents

Introduction

This report details E.M.C. tests carried out on the Graviner Ltd., Advanced Aircraft Engine Fire Detection System. The tests described herein were carried out in accordance with the Graviner Ltd., Test Plan No. 31-3-80 issue 4.

The tests described in this report were carried out at Lucas Aerospace facilities at Hemel Hempstead and Bradford.

Equipment Under Test

Ultra Violet Advanced Fire Detection Control Unit Pt. No. 53813-203
Serial No. 100.
Ultra Violet Advanced Fire Detection Control Unit Pt. No. 53813-204
Serial No. 100.
Crew Warning Unit Pt. No. 53813-202 Serial No. 100.
5 off Single Detector Units Pt. No. 53521-012.
5 off Dual Detector Units Pt. No. 53522-011.

Associated Equipment.

Aircraft cable form
Neon lights
Gnd test box.
Fibre optic cables for system warning lamps.

Test Equipment

Stoddart 91550-1 current probe Ser. No. 421/130
Stoddart 91197-1 current probe Ser. No. 218
Electro-Metrics CIG.25 impulse generator
Fairchild PCL-10 current probe + PCL10A amplifier Ser. No. 471
Electro-Metrics Antenna Selector SU125 Ser. No. 143
Fairchild RVR 25 Rod antenna and coupler Ser. No. 6-23
Fairchild BIA 25 Biconical antenna Ser. No. 6-23

Test Equipment (Cont'd)

Stoddart 93490-1 Conical log-spiral antenna.
EMCO 3103 Conical log-spiral antenna Ser. No. 2127
EMCO 3105 Double Ridged Guide Antenna Ser. No. 2091
Electro-Metrics Log periodic antnnna LA-70
Lucas manufactured mono-conical antenna
I.F.I. EFG 2 broadband antenna Ser. No. 34
Solar 6552 audio amplifier
Solar 62201A audio transformer
Solar 6512 10uF Feedthrough capacitors 9 off
Dubillier SBC 45 10uF feedthrough cpacitors 2 off
Marconi V.T.V.M. TF 2604 Ser. No. 200933/037
Marconi T.F.200 Signal Generator Ser. No. 54706/14
Marconi T.F.144H4 Signal Generator Ser. No. 53698/12
Marconi T.F. 801D/1 Signal Generator Ser. No. 53599/24
Marconi V.T.V.M. TF1041B Ser. No. JA217/484
Fairchild EMC10E Measuring Set Ser. No. 10471E
Electro-Metrics EMC25 MK III Measuring Set Ser. No. 366
Stoddart NM65T Measuring Set Ser. No. 145.
Electro-Metrics Programmer ESC 125A Ser. No. 146
Electro-Metrics X-Y plotter 125B Ser. No. 003
I.F.I. LPA Levelling pre-amplifier Ser. No. 0374942.
I.F.I. EFS1 E-Field Sensor 2 off
I.F.I. LMT Light Modulator/Transmitter 2 off
Bird 8135 termaline co-axial resistor Ser. No. 6829
Radial 6dB pad 15 watt.
I.F.I. Wideband amplifier Ser. No. 0374936
Coupling capacitors Lucas 1.0uF, 0.1uF and 0.01uF
2 off fibre optic cables
AML C203 power signal generator Ser. No. 125
AML 7050H plug-in-head 200-450MHz Ser. No. 119
AML 7051 AH plug-in-head 450-750MHz Ser. No. 104
AML 7051BH plug-in-head 750-1GHz Ser. No. 105.

Lucas high pass filter (400Hz isolation)
Lucas 25uH choke.
Texscan filters:- MOD 6LE 330AB Ser. No. 2888-1
MOD 6LE 494AB Ser. No. 2889-1
MOD 6LE 741AB Ser. No. 2890-1
MOD 6LD 1111AB Ser. No. 2891-1
Solar 7021-1 phase Shift network
Solartron 1484 True RMS voltmeter Ser. No. 137366

E.M.C. Tests General

The tests were carried out in a screened enclosure as described in the test plan. Interconnection cable assemblies simulated the actual installation and use. Leads that are screened in the normal installation were screened in the test installation. As far as possible, cables and equipments were arranged so that no shielding was interposed between the test sample, cables, and measuring antennas. All leads and cables were within 10 ± 2 cm of the edge of the ground plane and approximately 5 cm above the ground plane. Grounding of the system units was accomplished by copper braid attached to a single ground point. All the ground straps had an impedance of between 0.75 mohms and 1 mohm.

The test sample layouts are shown in appendix 1.

Screened Room Supplies

The 115V a.c. 400Hz Supplies and the 28V d.c. Supplies were brought into the screened room via filters located within the screened room walls,

E.M.C. Test CE.03

Conducted emissions Power leads 10KHz to 50MHz.

Test equipment.

a) Current probes Stoddart 91550-1 and 91197-1
b) Electro-Metrics EMC25 MK.III measuring set Ser. No. 366
c) Ten microfarad capacitors.
d) Electro-Metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.03. Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5 cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1 Fig. No. 1. The power leads which were separately measured for conducted emissions were as follows:-

115V 400Hz Line to Control Unit A Pin 14
115V 400Hz Neutral to Control Unit A Pin 13
28V d.c. Positive to Control Unit A Pin 12
28V d.c. Negative to Control Unit A Pin 29
115V 400Hz Line to Control Unit B Pin 14
115V 400Hz Neutral to Control Unit B Pin 13
28V d.c. Positive to Control Unit B Pin 12
28V d.c. Negative to Control Unit B Pin 29
28V d.c. Positive to Crew Warning Unit Pin 6

Each lead was subjected to 3 modes of test as follows:-

Condition 1. STANDBY.

Where the U.V. source is switched off and the "FIRE" and "FIRE DET FAIL" indicators were not illuminated.

Condition 1 (a).

Test samples were set as for STANDBY. A Transient condition was applied by depressing the fire test switch periodically at a rate of approximately 3 operation/resets per octave.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each power line listed in the schedule. Page nos. 1 to 9 inclusive appendix 2 detail the conducted emissions when the system was operated in conditions 1 and 1 (a).

At no frequency are there emission above the limit when the system is operated in Standby, condition 1.

When the system was operated in condition 1(a) the following above limit emissions were recorded.

Report No. LM 80876

LEAD	X-Y	PAGE NO.	FREQUENCY	dB ABOVE LIMIT
115V Line Control A		1	5.0MHz	0.5
" " " A		1	7.0MHz	5.0
" " " A		1	10.0MHz	3.5
" " " A		1	15.0MHz	3.0
" " " A		1	20.0MHz	1.0
115V Neutral Control A		2	5.0MHz	1.5
" " " "		2	7.0MHz	8.5
" " " "		2	10.0MHz	9.0
" " " "		2	15.0MHz	8.5
" " " "		2	20.0MHz	4.0
28V d.c. Positive Control A		3	30.0KHz	0.5
" " " "		3	85.0KHz	0.5
" " " "		3	15.0MHz	4.0
" " " "		3	20.0MHz	6.5
28V dc Negative Control A		4	15.0MHz	5.0
" " " "		4	20.0MHz	10.0
115V Neutral Control B		6	7.0MHz	10.0
" " " "		6	10.0MHz	12.0
" " " "		6	15.0MHz	12.0
28V dc Positive Control B		7	7.0MHz	1.0
" " " "		7	10.0MHz	0.5
" " " "		7	15.0MHz	8.0
" " " "		7	20.0MHz	5.0
28V dc Negative Control B		8	20.0MHz	2.0
28V dc Positive C.W.U.		9	500KHz	4.0
" " " "		9	700KHz	1.5
" " " "		9	1.0MHz	7.0
" " " "		9	1.5MHz	5.0
" " " "		9	2.0MHz	9.0
" " " "		9	3.0MHz	2.0
" " " "		9	4.0MHz	5.0
" " " "		9	5.0MHz	5.0
" " " "		9	7.0MHz	4.0
" " " "		9	10.0MHz	14.0
" " " "		9	15.0MHz	5.0
" " " "		9	20MHz	5.0

3/4

Page Nos. 10 to 18 inclusive app. 2 detail the power lead conducted emissions when the system is operated in condition 2 "FIRE".
The X-Y plots show that there are no emissions above the limit.

Throughout all modes of system operation there were no narrowband emissions and therefore the system meets the narrowband requirements.

EMC Test CE.04

Conducted emissions Signal and Control leads 20KHz to 50MHz.

Test equipment.

a) Current probes Stoddart 91550-1 and 91197-1
b) Electro-Metrics EMC-25 MK.III measuring set Ser. No. 366
c) Ten microFarad capacitors
d) Electro-Metrics programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.04 Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5 cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1 Fig. No. 1. The control and signal lead bunches were separately measured for conducted emissions as follows:-

Bunch 1, All leads, Detectors, Control Units, Crew Warning Unit, excluding power supplies.

Bunch 2. Single detector long cable bunch.

Bunch 3. Dual detector long cable bunch.

Each bunch was subjected to 2 modes of test as follows:-

Condition 1 STANDBY.

Where the U.V. source is switched off and the "FIRE" and "FIRE DET. FAIL" indicators were not illuminated.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results.

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each bunch listed in the schedule. Page nos. 19 to 21 app. 2 inclusive detail the conducted emissions when the system was operated in condition 1, Standby.

The X-Y plot on page 19 app. 2. Bunch 1, shows transient emissions above the limit between 450KHz and 9.5MHz. The maximum emission above the limit is 25dB between 2.3 and 2.4MHz.

Page 20 app. 2, Bunch 2, shows transient emissions above the limit between 450KHz and 11.75MHz. The maximum emission above the limit is 22dB between 2.3 and 2.4MHz.

Page 21 app. 2, Bunch 3, shows transient emissions above the limit between 600KHz and 800KHz, and between 1.2MHz and 4MHz. The maximum emission above the limit is 25dB between 2.3 and 2.4MHz.

Page nos. 22 to 24 app. 2. inclusive detail the conducted emissions when the system is operated in condition 2, Fire.

The X-Y plot on page 22, app.2, Bunch 1, shows emissions above the limit between 450KHz and 10MHz. The maximum emission above the limit is 27dB between 2MHz and 2.2MHz.

The X-Y plot on page 23, app.2, Bunch 2, shows emissions above the limit between 480KHz and 610KHz, and between 850KHz and 13MHz. The maximum emission above the limit is 20.5 dB between 2.05MHz and 2.3MHz.

The X-Y plot on page 24, app. 2, Bunch 3, shows emissions above the limit between 580KHz and 670KHz, between 1 MHz and 5MHz, at 6.6MHz and at 7.8MHz. The maximum emission occurs at 2.1MHz and is 28.5dB above the limit.

Throughout the two modes of system operation there were no narrowband emissions and therefore the system meets the narrowband requirements.

E.M.C. Test CE.01

Conducted emissions Power leads 30Hz to 20KHz.

Test Equipment.

a) Current Probe PCL-10
b) PCL 10A Amplifier for use with (a).
c) Electromagnetic Interference Meter Fairchild EMC10E
d) 10uF feedthrough capacitors
e) Electro-Metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2 test CE.01. Input power supplies were connected to the test items via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between leads, cables and the ground plane of 5cm. The length of each power supply lead between test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1, fig. No. 1. The power supply leads which were separately measured for conducted emissions were as follows:-

115V 400Hz line to Control Unit A Pin 14
115V 400Hz Neutral to Control Unit A Pin 13
28V dc Positive to Control Unit A Pin 12
28V dc Negative to Control Unit A Pin 29
115V 400Hz Line to Control Unit B Pin 14
115V 400Hz Neutral to Control Unit B Pin 13
28V dc Positive to Control Unit B Pin 12
28V dc Negative to Control Unit B Pin 29
28V dc Positive to Crew Warning Unit Pin 6.

Each lead was subjected to 2 modes of test as follows:-

Condition 1 STANDBY. 328

Where the U.V. source is switched off and the "Fire" and "Fire Det. Fail" indicators were not illuminated.

Condition 2 FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results.

The test Results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each power line listed in the schedule. Page nos. 25 to 33 app. 2 inclusive detail the conducted emissions when the system was operated in Condition 1. At no frequency were there narrowband emissions above the limit when the system was operated in Condition 1, STANDBY.

Page nos. 34 to 42 inclusive appendix 2 detail the power lead conducted emissions above the limit when the system was operated in condition 2 "FIRE". The X-Y plots show that there are no narrowband emissions above the limit.

E.M.C. Test CE.02

Conducted emissions signal and control leads 30Hz to 20KHz.

Test equipment.

a) Current Probe PCL-10
b) PCL 10A Amplifier for use with (a)
c) Electromagnetic Interference Meter Fairchild EMC10E
d) Electro-metrics Programmer ESC 25A.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CE.02. Input power supplies were connected to the test items via 10uF feedthrough capacitors bonded to the ground plane. There was a minimum separation between cables, leads and the ground plane of 5cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of one metre. The arrangements for the test are illustrated in appendix 1. Fig. No. 1. The control and signal lead bunches were separately measured fo. conducted emissions as follows:-

Bunch 1, All leads, Detectors, Control Units, Crew Warning Unit, excluding power supplies.

Bunch 2. Single Detector long cable bunch.
Bunch 3. Dual Detector long cable bunch.

Each bunch was subjected to two modes of test as follows:-

Condition 1. STANDBY.

Where the U.V. source was switched off and the "FIRE" and "FIRE DET. FAIL" indicators were not illuminated.

Condition 2. FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results.

The test results are contained in appendix 2, the appendix contains X-Y plot data of the conducted emissions on each bunch listed in the schedule. Page nos. 43 to 45 app. 2. inclusive detail the conducted emissions when the system was operated in condition 1 Standby. Page nos. 46 to 48 app. 2 inclusive detail the conducted emissions when the system was operated in condition 2 Fire. No X-Y plot shows narrowband emissions above the limit.

E.M.C. TEST RE.02

Radiated Emission 14KHz to 10GHz Electric Field.

Test equipment.

a) Test antennas 41" Rod, Bi-conical, Conical Log Antenna, Double ridged guide Antenna.
b) E.M.I. meters EMC 25 and NM65T
c) Electro-metrics programmer ESC25A
d) 10uF feedthrough capacitors.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test RE.02. Input power supplies to the test items were connected via 10uF feedthrough capacitors bonded to the ground plane.
There was a minimum separation between cables, leads and the ground plane of 5cm. The length of each power lead between the test sample and the 10uF capacitor was a minimum of two metres. The arrangements for the test are illustrated in appendix 1. Fig. nos. 2, 3, 4 and 5. The system was tested in three modes as follows:-

Condition 1. STANDBY.

Where the U.V. source has switched off and the "FIRE" and "FIRE DET. FAIL" indicators were not illuminated.

Condition 1(a).

Test samples were set up as for STANDBY. A Transient condition was applied by depressing the fire test switch periodically at a rate of approximately 3 operation/resets per octave.

Condition 2. FIRE.

Where the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

Test Results

The test results are contained in appendix 2, the appendix contains X-Y plot data of emissions in all three modes of operation.
Page 49 and 50 show the radiated broadband emissions from 14KHz to 1GHz when the system was operated in modes 1 and 1 (a).
In mode 1, Standby the only emissions above the limit occur at 15KHz and 16KHz where the levels are both 0.5 dB above the limit. There were no narrowband emissions exhibited on the X-Y plot.
In mode 1(a) the following above limit transient emissions were recorded.

X-Y PAGE NO.	FREQUENCY	dB ABOVE LIMIT
49	14KHz	3
49	20KHz	12.5
49	30KHz	13
49	45KHz	14.5
49	65KHz	15
49	80KHz	12
49	100KHz	9.5
49	150KHz	2.5
49	200KHz	8.5
49	1MHz	1.5
49	3MHz	6
49	4MHz	7
49	10MHz	5
49	40MHz	2
50	150MHz	2

Graph nos. 51 and 52 show the narrowband X-Y plot 1-10GHz for when the system was operated in "Standby". There are no narrowband emissions. The emissions above the limit shown on band 1 are broadband.

The X-Y plots on pages 53 and 54 show the radiated broadband emissions from 14KHz to 1GHz, when the system was operated in mode 2 "Fire".

The radiated emissions above the limits occur at between 14KHz and 18KHz, and 5.75MHz and 6.6MHz. The maximum emission occurred at 6.4MHz, where the level was 6dB above the limit. There were no narrowband emissions exhibited on the X-Y plot. Graph nos. 55 and 56 show narrowband X-Y plot 1-10GHz for when the system was operated in "Fire". There were no narrowband emissions. The emissions above the limit shown on band 1 are broadband.

E.M.C. Test CS.01

Conducted Susceptibility, 30Hz to 50KHz. Power leads.

Test equipment.

a) Oscillator Marconi TF 2000 & TF144/H4
b) Power Amplifier Solar 6552-1
c) Isolation Transformer Solar 6220-1A
d) 400uF capacitor
e) Marconi V.T.V.M. TF1941B
f) Solar Phase Shift network.

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CS.01. Input power supplies were connected to the test items via a 10uF feedthrough capacitor bonded to the ground plane. The arrangement for the test is shown in fig. 6. appendix 1. The system was tested in two modes of operation as follows:-

Condition 1. STANDBY.

Condition 2. FIRE.

Test Results

When the initial test results were undertaken it was found that when any d.c. lead of the system was tested in condition 1, STANDBY there were malfunctions. The malfunctions were identified by either or both the Fire warning lights illuminating. The susceptibility occurred between 3.5KHz and 50KHz.

After investigation, (both CS.01 and CS.02 test methods), the following modifications were made to the system.

1) The screen of the detector leads was in each case grounded at the control units and not as originally at the detectors.

2) The common logic cards power supply input filters in both control units were modified by including two 6.8uF capacitors between the 28V d.c. positive and negative leads to ground. See figure 1., appendix 3.

3) The drive supply cards, (two in control unit A and one in control unit B), were modified by decoupling the 10Kohm resistors R25, R27, R29, R31, R49, R51, R53, and R55 with 10,000 p.F. capacitors. See figure 2, appendix 3.

Note: After the susceptibility tests were completed the emission tests were repeated and where necessary the X-Y plots were re-plotted. The emission results given in this report are the final levels obtained after the above modifications had been engineered into the system.

With the system modified as detailed above there were no malfunctions throughout test CS.01 on any lead in either of the two modes.

E.M.C. Test CS.02

Conducted Susceptibility 50KHz to 400MHz. Power leads.

Test equipment.

a) Marconi VTVM TF 1041B
b) Marconi VTVM TF 2604
c) Solar 6512 10uF feedthrough capacitors.
d) Marconi Signal Generator TF 144H/4
e) Marconi Signal Generator TF 801D/1
f) IFI LPA1 Levvelling pre-amplifier
g) Radiall 6dB pads
h) Marconi 50 ohm load TM5582
i) Lucas coupling capacitors 1.0uF, 0.1uF, and 0.01uF
j) Lucas high pass filter (400Hz isolation)
k) IFI Wideband amplifier
l) A.M.L. C203 power signal generator
m) A.M.L. 7050H plug in head 200-450MHz
n) 25uH choke (frequency limit 1MHz)
o) Texscan Filters

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462 Notice 2, test CS.02. Input power supplies were connected to the test items via a 10uF feedthrough capacitor bonded to the ground plane. The arrangements for the test are shown in fig. 7 appendix 1. The system was tested in two modes as follows:

Condition 1. Standby.

Condition 2. Fire.

Note the susceptibility signal was modulated to Graviner Test Plan 3.3.80 issue 4 requirements.

Test Results.

After the modifications detailed in the CS.01 test were incorporated in the system there were no malfunctions throughout the CS.02 test, on any lead in either mode.

E.M.C. Test RS.03

Radiated Susceptibility 14KHz to 1GHz Electric Field.

Test equipment.

a) I.F.I. LPA 1 Levelling pre-amplifier
b) EFS.1 E-field sensors 2 off
c) IFI Light Modulator/Transmitter
d) Bird Termaline co-axial resistor.
e) IFI Wideband amplifier
f) Fibre optic cables
g) A.M.L. C203 power signal generator
h) A.M.L. Plug in heads 7050H, 7051AH, 7051BH 200MHz-1GHz
i) EMCO 3103 Con. Log. spiral antenna 100-1000MHz
j) IFI Broadband antenna 10KHz-200MHz
k) Marconi Signal Generators TF144/H, TF801/D
l) Stoddart Con. Log spiral antenna 93490-1
m) Stoddart Con. Log spiral antenna 93491-2
n) EMC 25 measuring set
o) Texscan Filters MOD 6LE 330AB, MOD 6LE 494B, MOD 6LE 741AB and MOD 6LD 1111AB

Test Schedule.

The E.M.C. test was conducted in accordance with the requirements of MIL-STD-461A Notice 3 and MIL-STD-462, Notice 2, test RS.03. Input power supplies were connected to the test [illegible] via a 10uF feedthrough capacitor bonded to the ground plane. The [illegible]ts for the test are shown in figs. 8, 9 and 10 appendix 1. The s[illegible] was tested in two modes as follows:-

Condition 1. Standby
Condition 2. Fire.

Note the susceptibility signal was modulated to Graviner Test Plan 3.3.80 issue 4 requirements.

Test results.

In condition 1, Standby there were several susceptibilities to the general E-field as follows:-

Frequency	Threshold	Malfunction
118MHz	7 v/m	Right Eng. Fire det. fail lamp illuminated.
121.5MHz	10 v/m	" " " " " " "
124MHz	10 v/m	" " " " " " "
193MHz	8.5 v/m	Left Eng. Fire det. fail lamp illuminated.
200MHz	10 v/m	" " " " " " "

At no frequencies were there malfunctions of the system when the specified E-field level was transmitted.

There was no susceptibility to the radiated E-field when the system was tested in condition 2 fire.

Conclusions

With the system modified as described in the report text, see figs. 1 and 2 appendix 3, the following test results were noted.

E.M.C. Test CE.03

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the CE.03 narrowband requirements. There were no broadband emissions above the limit when the system was operated in condition 1, STANDBY.

In condition 1(a) where transient emissions were recorded when the fire test switch was depressed and reset, there were many emissions above the broadband limits. The table in the CE.03 results details all the leads and frequencies when the transient emissions were above the limit. The major emissions above the limit are as follows:-

LEAD	X-Y PAGE NO.	FREQUENCY	dB ABOVE LIMIT
115V Neutral Control A	2	7.0MHz	8.5
" " " "	2	10.0MHz	9.0
" " " "	2	15.0MHz	8.5
28V dc Positive Control A	3	20.0MHz	6.5
28V dc Negative Control A	4	20.0MHz	10.0
115V Neutral Control B	6	7.0MHz	10.0
" " " "	6	10.0MHz	12.0
" " " "	6	15.0MHz	12.0
28V dc Positive Control B	7	15.0MHz	8.0
28V dc Positive C.W.U.	9	1.0MHz	7.0
" " " "	9	2.0MHz	9.0
" " " "	9	10.0MHz	14.0

Although the above table details emissions which are significantly above the limit, as they are of a transient nature and the repetition rate low they would not in the opniion of the Lucas Aerospace E.M.C. personnel cause a serious E.M.C. hazard.

In condition 2, Fire, there were no broadband emissions above the limit on any lead.

E.M.C. Test CE.04.

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the CE.04 narrowband requirements.

There were broadband emissions above the limit when the system was tested in condition 1, Standby as follows. Bunch 1, all leads, detectors, control units, and crew warning unit, excluding the power supplies, had emissions above the limit between 450KHz and 9.5MHz. The maximum emission occurred at between 2.3 and 2.4MHz and was 25dB above the limit.

Bunch 2, single detector long cable bunch, had broadband emissions above the limit between 450KHz and 11.75MHz. The maximum emission above the limit is 22 dB between 2.3 and 2.4MHz.

Bunch 3, dual detector long cable bunch, had broadband emissions above the limit between 600KHz and 800MHz and 1.2MHz and 4MHz. The maximum emission above the limit was 25dB between 2.3 and 2.4MHz.

There were also broadband emissions above the limit when the system was operated in condition 2, Fire, as follows.

Bunch 1, all leads, detectors, control units, and crew warning unit, excluding power supplies had emissions above the limit between 450KHz and 10MHz. The maximum emission above the limit is 27dB between 2MHz and 2.2MHz.

Bunch 2, single detector long cable bunch, had emissions above the limit between 480KHz and 610KHz, and 850KHz and 13MHz. The maximum emission above the limit is 20.5dB between 2.05MHz and 2.3MHz.

Bunch 3, dual detector long cable bunch, had emissions above the limit between 580KHz and 670KHz, 1MHz and 5MHz, and 6.6MHz and 7.8MHz. The maximum emission occurs at 2.1 MHz and is 28.5dB above the limit.

All the above out of specification broadband emissions could be a source of E.M.C. hazard if the aircraft cable layout enabled close coupling to occur between the Fire detect system wiring and leads to other systems. However from the RE.02 test results detailed in this report it would appear that the out of limit emissions are contained within the system wiring as there were no radiated emissions recorded above the limits at the above frequencies.

E.M.C. Test CE.01.

There were no narrowband emissions outside the limits recorded from any of the leads under test in either of the two modes of system operation.

E.M.C. Test CE.02.

There were no narrowband emissions outside the limits recorded from any of the bunches under test in either of the two modes of system operation.

E.M.C. Test RE.02.

There were no narrowband emissions detected during the test in the two modes of operation therefore the system complies with the RE.02 narrowband requirements.

In condition 1, Standby, there were broadband emissions marginally outside the specification limits between 14KHz and 16KHz. The maximum emission being only 0.5dB above the limit. When the system is operated in condition 1(a) transient emissions above the limit were recorded when the fire test switch was depressed and reset. The table in the RE.02 results details all out of limit transient emissions. The major emissions recorded above the limit are as follows.

X-Y PAGE NO.	FREQUENCY	dB ABOVE LIMIT
49	20KHz	12.5
49	30KHz	13
49	45KHz	14.5
49	65KHz	15
49	80KHz	12
49	100KHz	9.5
49	200KHz	8.5
49	3MHz	6
49	4MHz	2

Although the above table details emissions which are significantly above the limit, as they are of transient nature and the repetition rate low, they would not in the opinion of the Lucas Aerospace E.M.C. personnel cause a serious E.M.C. hazard.

In condition 2, Fire, there were broadband emissions above the limit between 14KHz and 18KHz, between 5.75MHz and 6.6MHz. The maximum emission occurred are 6.4MHz where the level was 6dB above the limit. It is considered by the Lucas Aerospace E.M.C. personnel that these radiated emissions would not cause an E.M.C. hazard in the aircraft installation.

E.M.C. Test CS.01.

The test was performed with the circuit and cable modifications as described earlier. There were no susceptibilities throughout the test on any lead in either of the two conditions of system operation.

E.M.C. Test CS.02.

The test was performed with the circuit and cable modifications as described earlier there were no susceptibilities throughout the test on any lead in either condition of system operation.

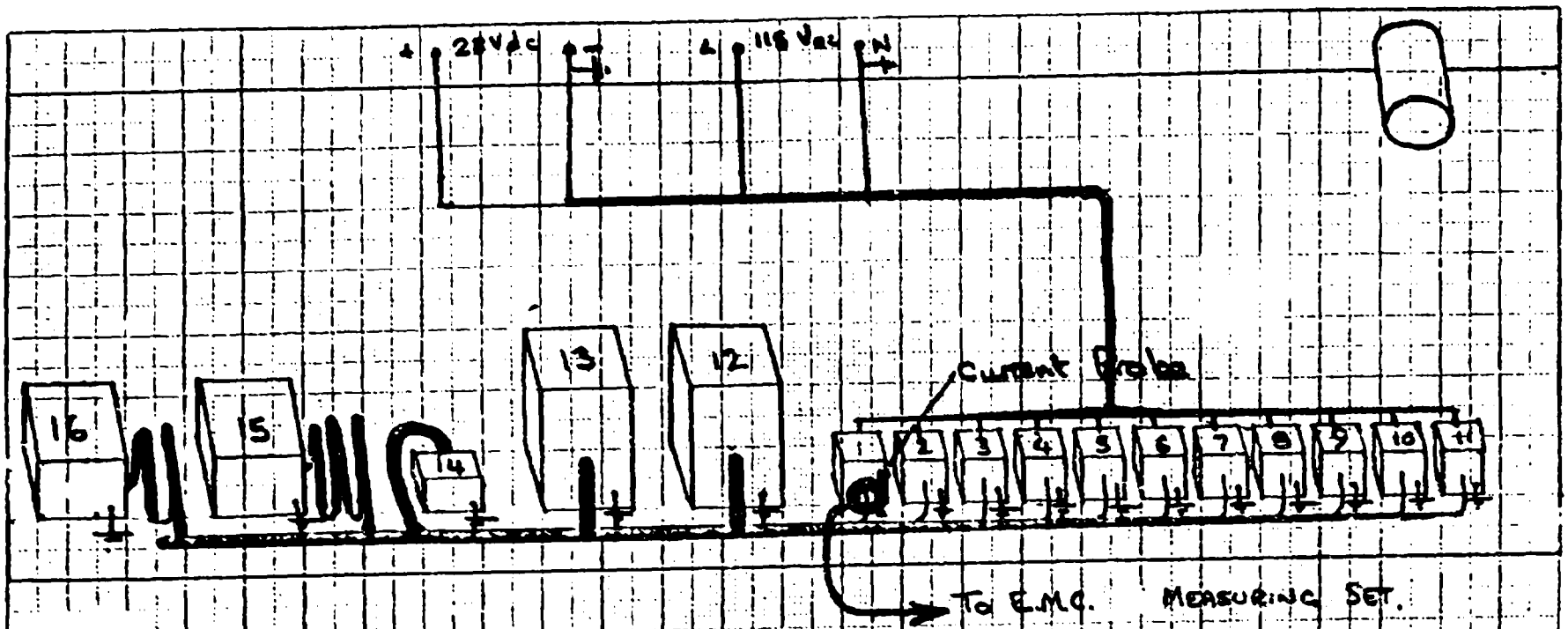
E.M.C. Test RS.03.

In condition 1, Standby, there were several frequencies as detailed in the report where the system malfunctioned, i.e. Eng. Fire detect lamps illuminated. At no frequency were there malfunctions of the system when the specified E-field level was transmitted.

The results contained in this report only apply to equipment manufactured to the same standards as that submitted for testing any deviation from these standards could invalidate these results.

Appendix 1

Test Layouts



1) 10μF Capacitor Line Control A Pin 14
2) " " " Neutral Control A Pin 13
3) " " " Line Control B Pin 17
4) " " " Neutral Control A Pin 16
5) " " " Positive Control A Pin 12
6) " " " Negative Control A Pin 29
7) " " " Line Control B Pin 14
8) " " " Neutral Control B Pin 13
9) " " " Positive Control B Pin 12
10) " " " Negative Control B Pin 29
11) " " " Positive Crew W. Unit Pin 6
12) Control Unit B
13) Control Unit A
14) Crew Warning Unit
15) Metal box containing single head detector.
16) Metal box containing double head detector.

Note:
All system units and 10μF feedthrough capacitors bonded to the ground plane via 1" copper band
Cable length from units to 10μF capacitors minimum of 1 metre.
All Cables min 5cm above the ground plane

Test Nos. CE01 / CE02
CE03 / CE04

FIGURE No 1. GRANNER FIRE DETECTION SYSTEM

A.C.T.

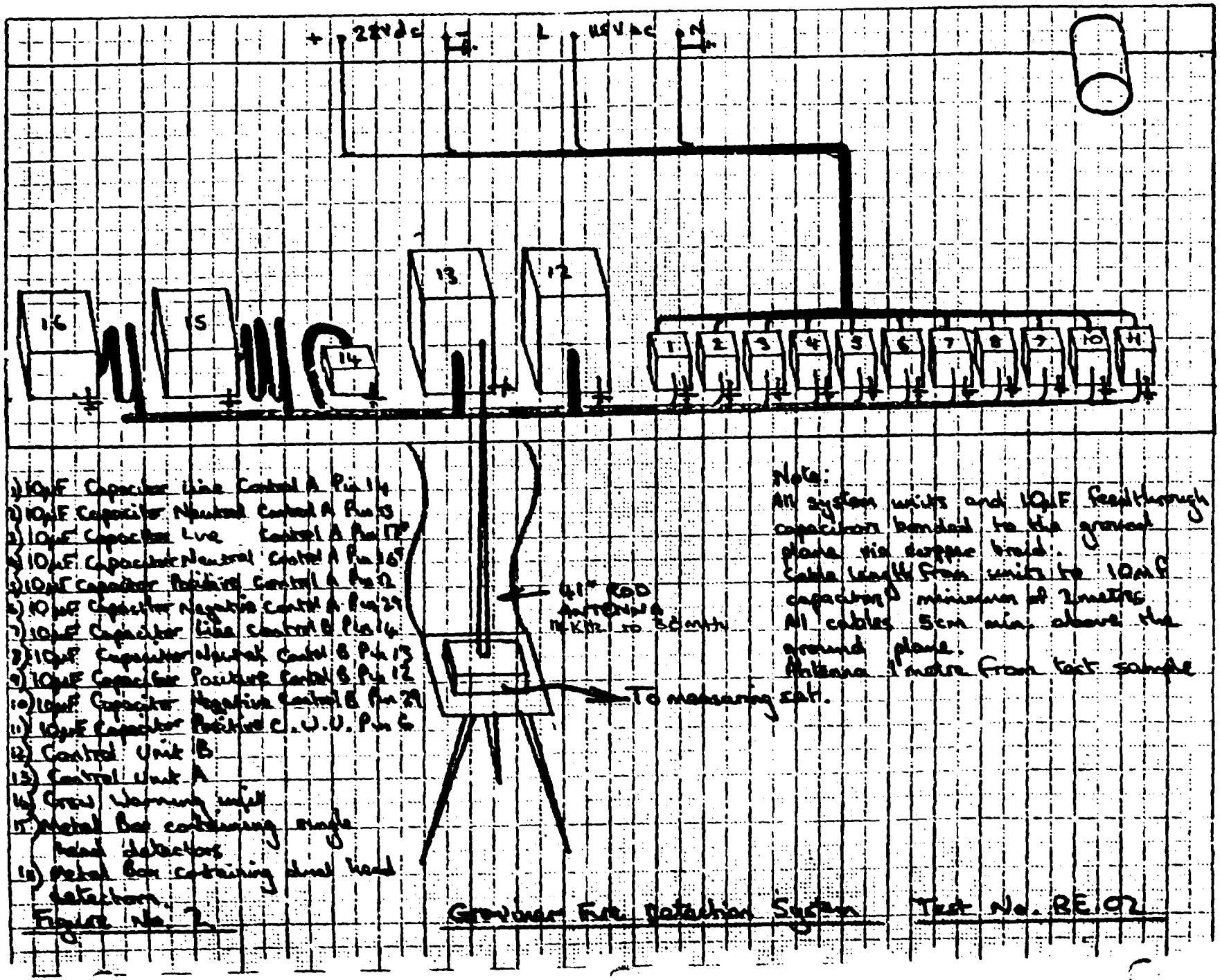
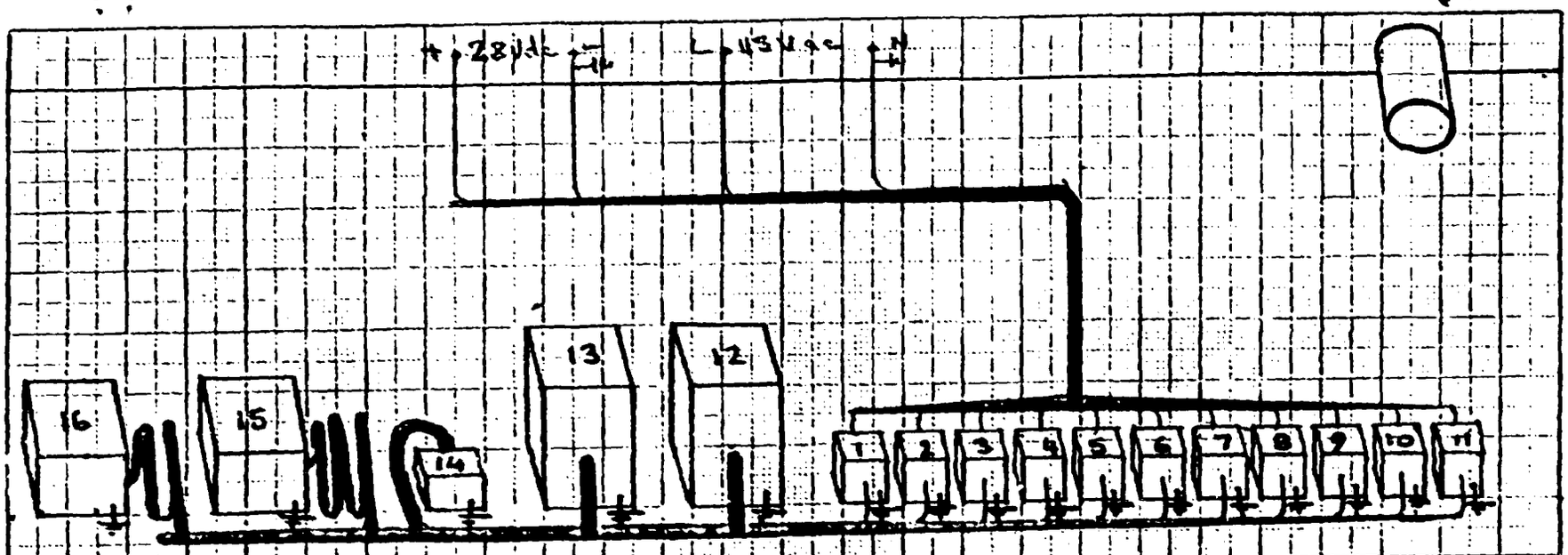


Figure No. 2

Groundwave Emn. Rotation System Test No. RE02



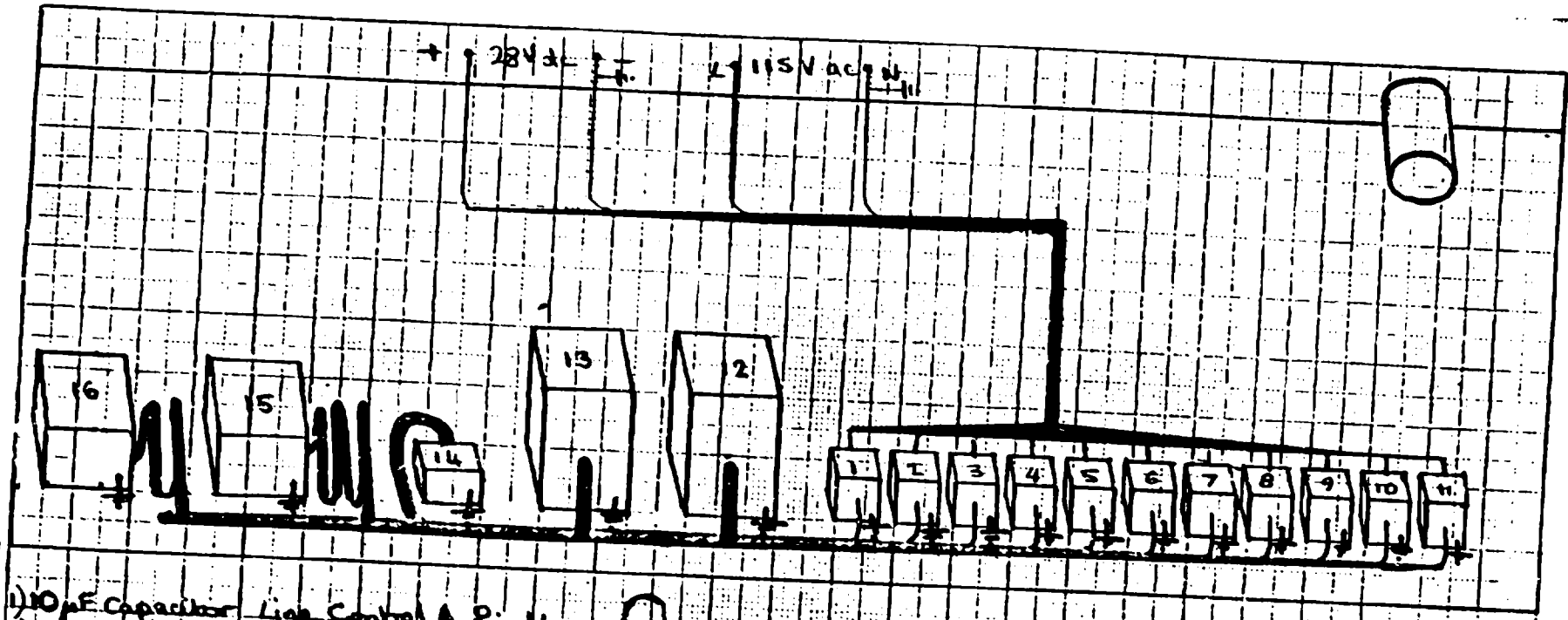
1) 10μF Capacitor Line Control A Pin 14
2) 10μF Capacitor Neutral Control A Pin 13
3) 10μF Capacitor Line Control A Pin 12
4) " " Neutral Control A Pin 16
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Line Control B Pin 14
8) " " Neutral Control B Pin 13
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 29
11) " " Positive to Up Up Pin 6
12) Control Unit B
13) Control Unit A
14) Crew Warning Unit
15) Metal Box containing single detectors
16) Metal Box containing dual detectors

Bi-con Antenna

To measuring Set.

Note:
All system units and 10μF feedthrough capacitors bonded to the ground plane via copper braid. Cable length from unit to 10μF capacitors minimum of 2 metres. All cables 5 cms min above the ground plane
Antenna 1 metre from test sample shown in a horizontal position.
Readings also taken with antenna in vertical position
Bi-con antenna measurement range 30mHz to 2GmHz

FIGURE No 3 GRAVINER FIRE DETECTION SYSTEM Test No. REC2

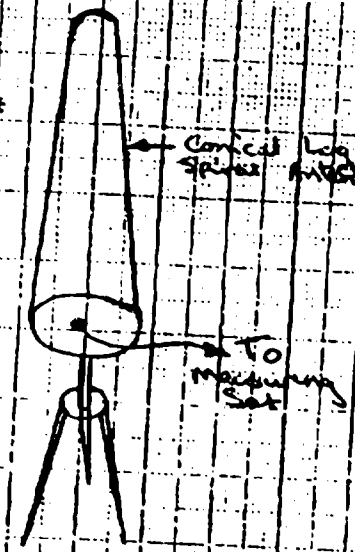


352

1) 10 μF Capacitor Line Control A Pin 14
2) " " Neutral Control A Pin 13
3) " " Line Control A Pin 17
4) " " Neutral Control A Pin 16
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Line Control B Pin 14
8) " " Neutral Control B Pin 15
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 28
11) " " Positive C.W.U. Pin 6

1. Control Unit B
2. Control Unit A
3. Crew Warning Unit
4. Metal Box containing single detectors
5. Metal Box containing twin detectors

Equip. No 4

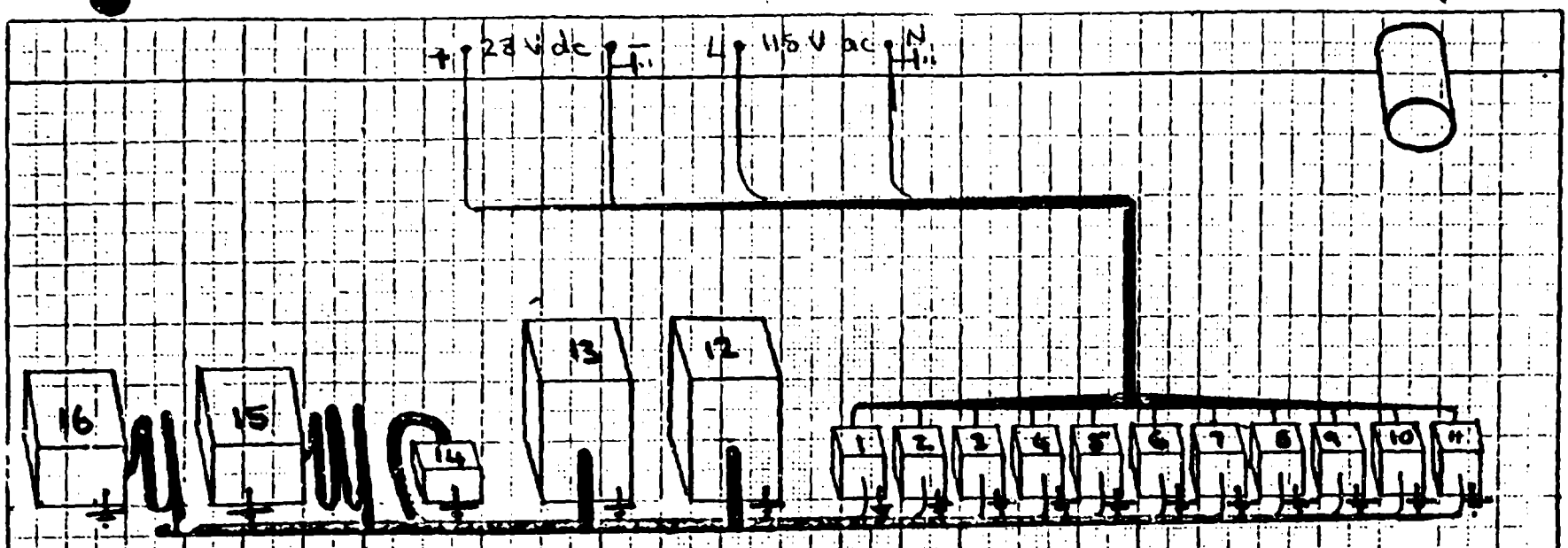


Note:-
All systems units and 10μF feedthrough capacitors bonded to the ground plane
11 ft. compact coaxial Cable length from unit to 10μF capacitors minimum of 2 metres All cables 5 cm min. above the ground plane.
Antenna 1 metre from test sample's
Conical Log Spiral antenna measurement range 200MHz to 1000MHz

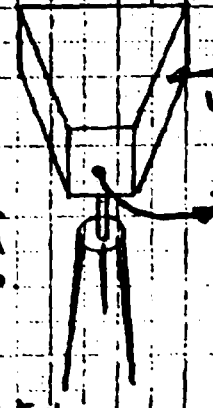
GRANINER FIRE DETECTION SYSTEM

TEST No RE 02

A.C.T.



1) 10μF Capacitor Line Control A Pin 14
2) " " Neutral Control A Pin 13
3) " " Line Control A Pin 17
4) " " Neutral Control A Pin 16
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Line Control B Pin 14
8) " " Neutral Control B Pin 13
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 29
11) " " Positive C.W.U. Pin 6
12) Control Unit B
13) Control Unit A
14) Crew Warning Unit
15) Metal Box containing Ridge detectors
16) Metal Box containing dipole detector



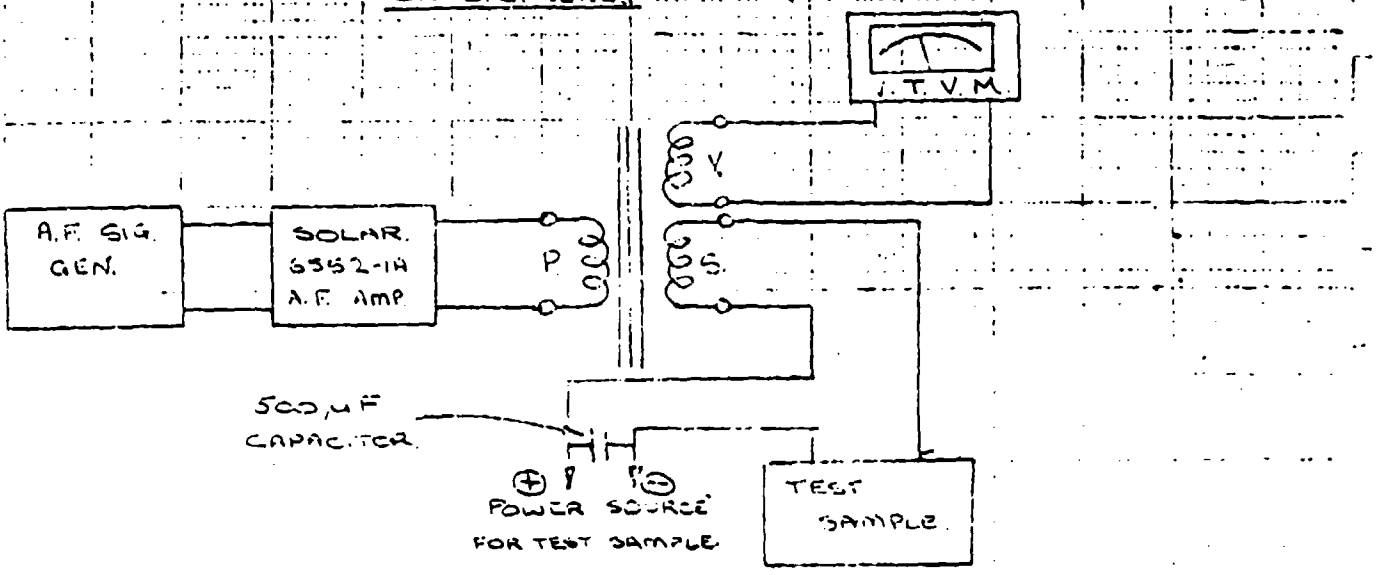
Note:-
All systems units and 10μF feed through capacitors bonded to the ground plane via copper braid. Cable lengths from unit to 10μF capacitors minimum of 2 metres. All cables 5 cm min. above the ground plane.
Antenna 1 metre from test samples shown in horizontal position measurements also taken with antenna in vertical position.
Ridge Guide antenna measurement range 1 GHz to 10 GHz.

Figure No 5 GRUMMAN FIRE DETECTION SYSTEM Test No RS.02

353

A.C.T.

INTERCONNECTING DIAGRAM FOR A.F. SUSCEPTIBILITY TESTS
ON D.C. LINES



INTERCONNECTING DIAGRAM FOR A.F. SUSCEPTIBILITY TESTS
ON A.C. LINES

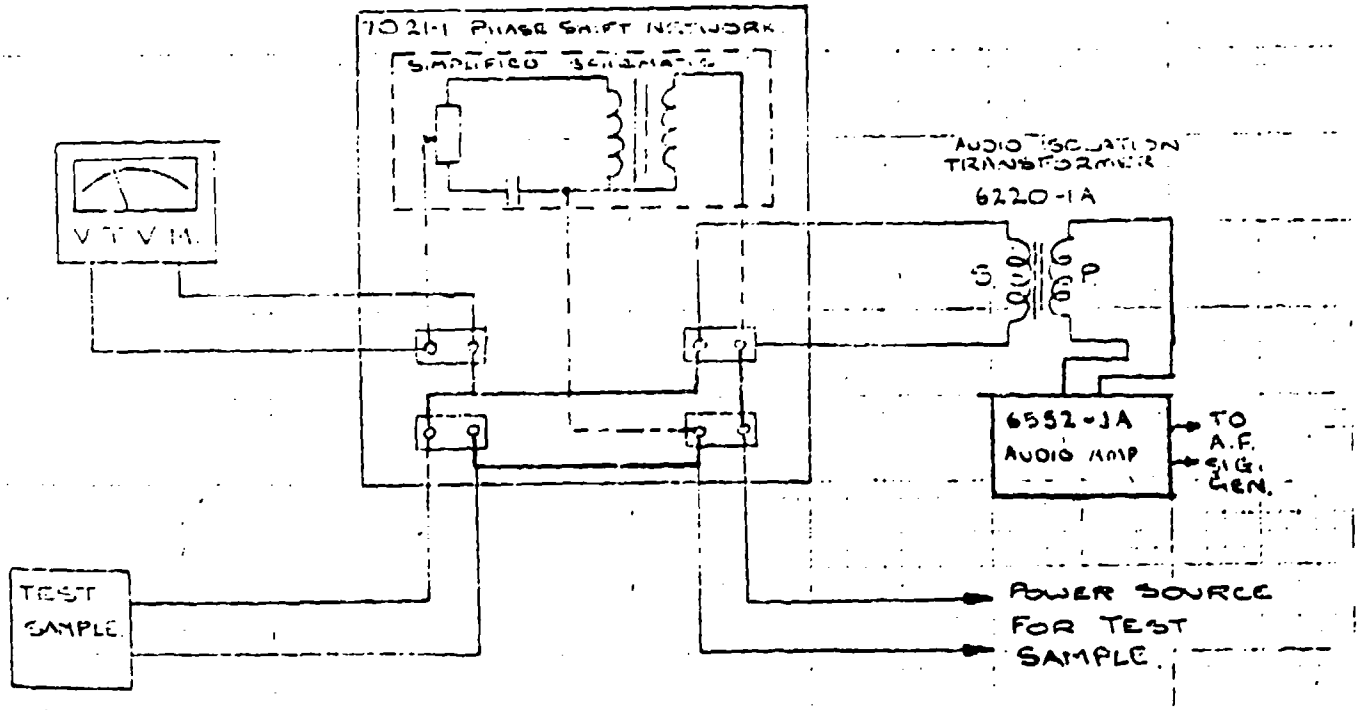
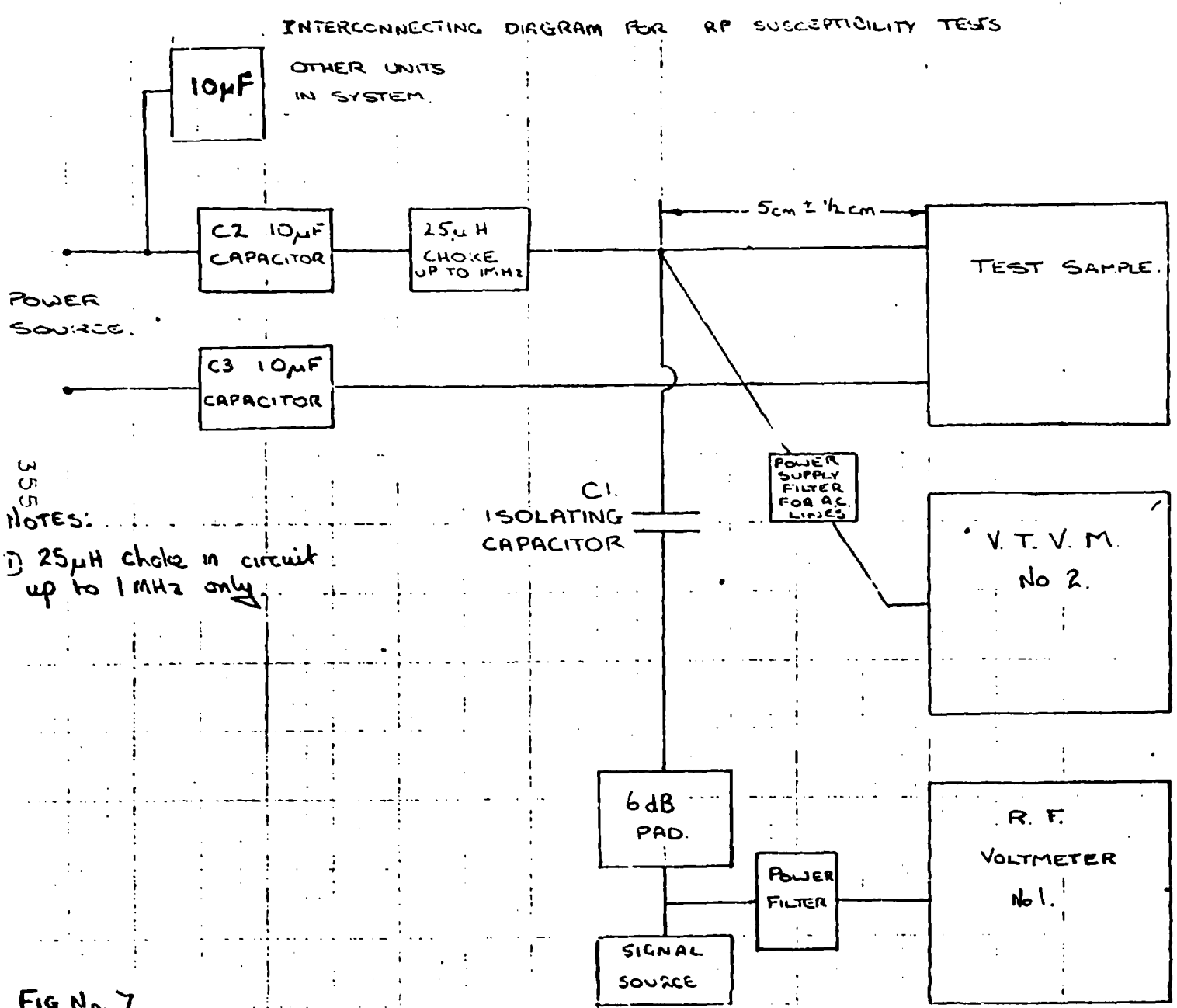


FIGURE NO 6. GRANINER FIRE DETECTION SYSTEM TEST NO CS.01.

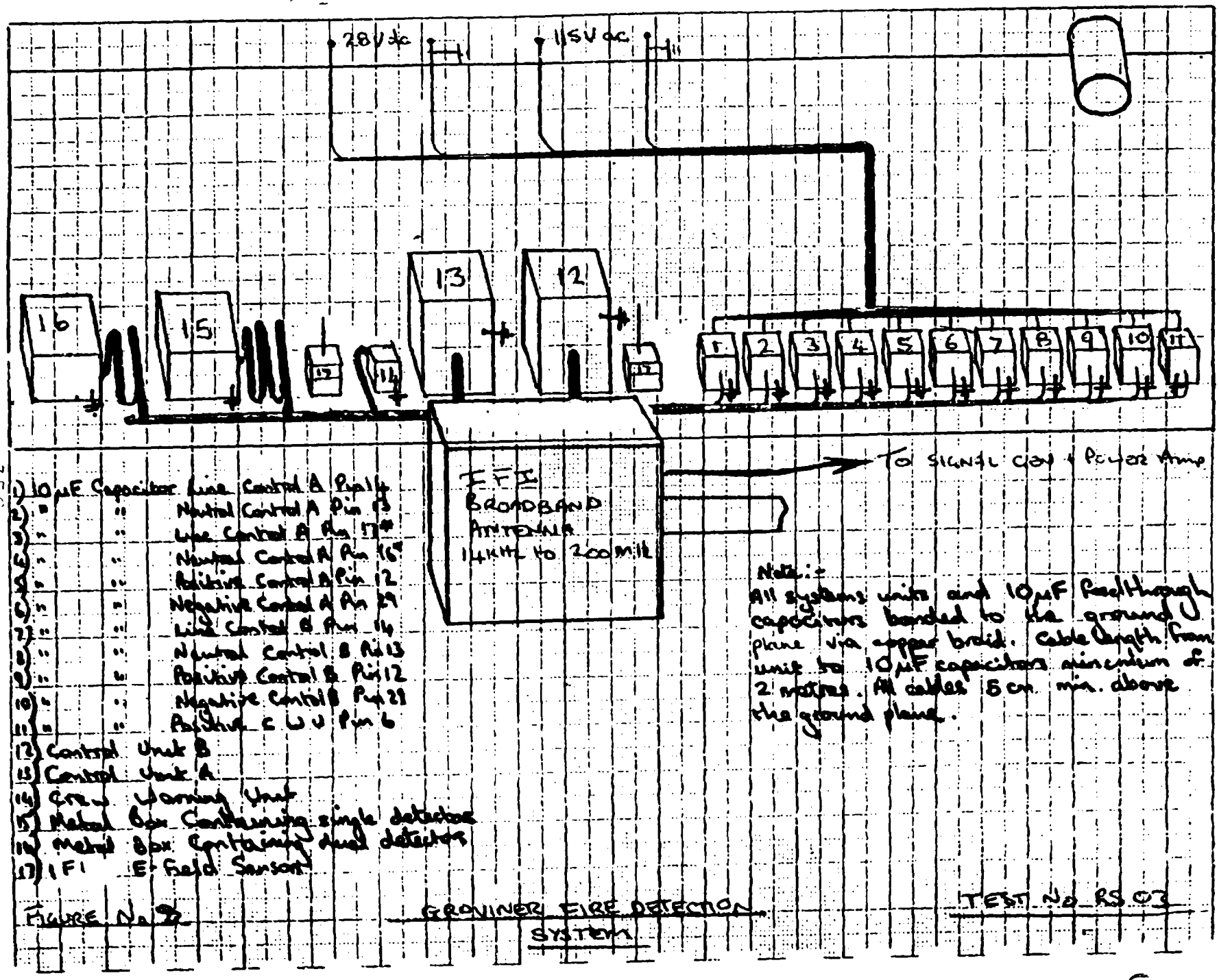


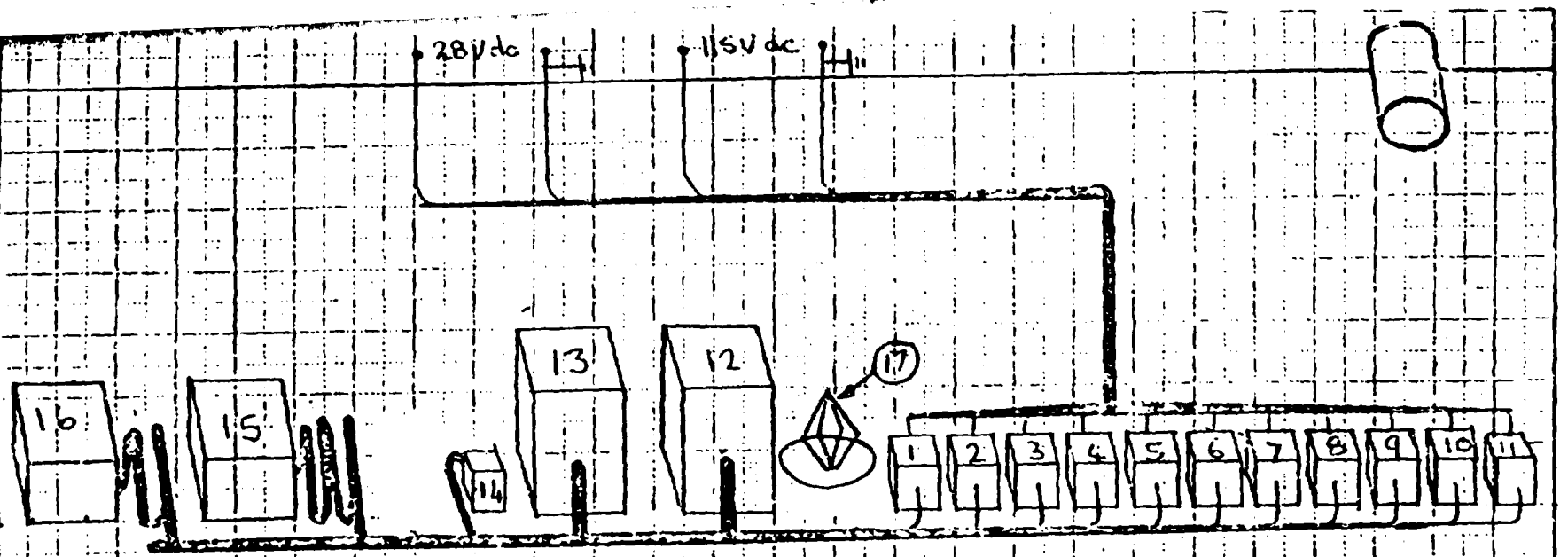
355

NOTES:

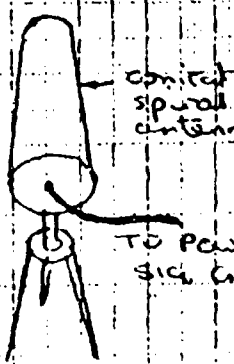
1) 25μH choke in circuit up to 1MHz only.

FIG No. 7


28V dc
115V ac
16
15
13
12
1
2
3
4
5
6
7
8
9
10
11
FIE
BROADBAND
ANTENNA
1 kHz to 200 MHz
To Signal Conditioning & Power Amp
1) 10 µF Capacitor Line Control A Pin 14
2) " " Neutral Control A Pin 13
3) " " Line Control A Pin 17*
4) " " Neutral Control A Pin 16*
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Line Control B Pin 14
8) " " Neutral Control B Pin 13
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 29
11) " " Positive c.u.v. Pin 6
12) Control Unit B
13) Control Unit A
14) Fire Warning Unit
15) Metal Box Containing single detector
16) Metal Box Containing dual detectors
17) FI E-field Sensor
Note:-
All systems units and 10µF feedthrough capacitors bonded to the ground plane via copper braid. Cable length from unit to 10µF capacitors minimum of 2 metres. All cables 5 cm min. above the ground plane.
FIGURE No 2
GROVINER FIRE DETECTION SYSTEM
TEST No RS 03



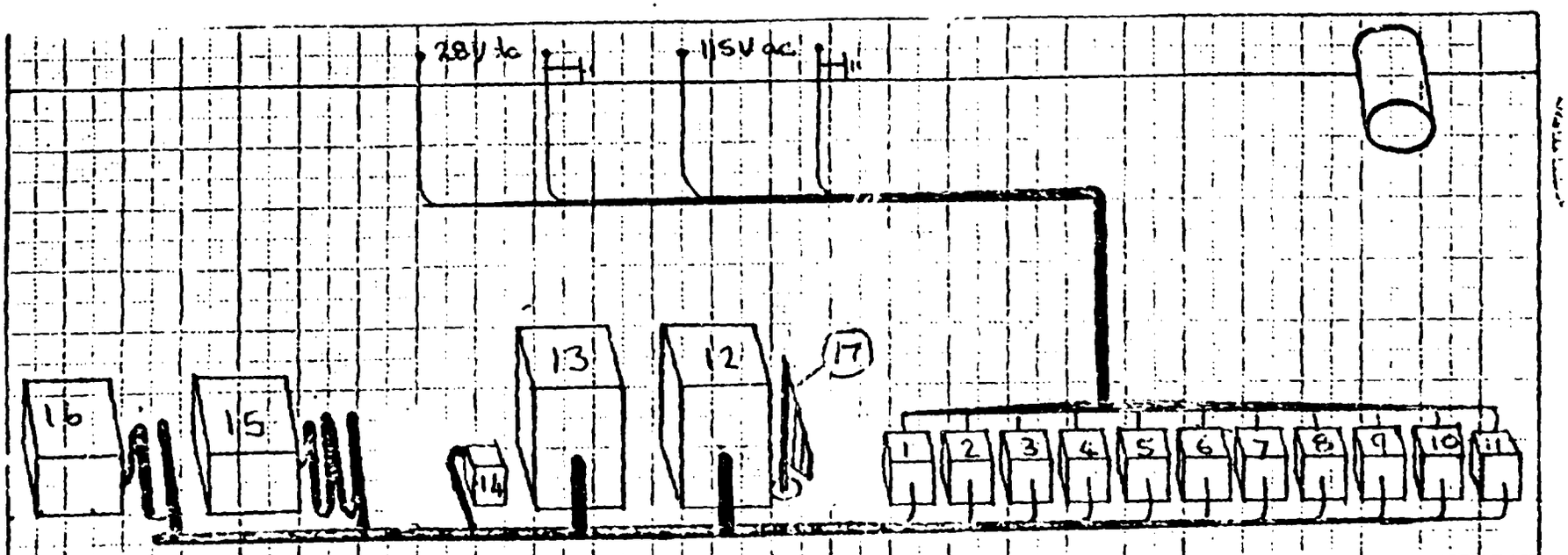
1) 10μF Capacitor Fire Control A Pin 14
2) " " Neutral Control A Pin 13
3) " " Fire Control A Pin 17
4) " " Neutral Control A Pin 16
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Fire Control B Pin 14
8) " " Neutral Control B Pin 13
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 29
11) " " Positive Fire Unit Pin 6
12) Control Unit B
13) Control Unit A
14) Crew Warning Unit
15) Metal Box Containing single detector
16) Metal Box Containing dual detector
17) Lucas mono conical monitoring antenna



Note:-
All systems units and 10μF feedthrough capacitors bonded to the ground plane via copper braid. Cable length from unit to 10μF capacitors minimum of 2 metres. All cables 5cm min. above the ground plane.
Antenna 1 metre from test sample
Lucas mono conical monitoring antenna used between 200MHz and 400MHz

357

Figure No 9 GRAVINER FIRE DETECTION SYSTEM TEST No 2502



1) 10 µF Capacitor Line Control A Pin 14
2) " " Neutral Control A Pin 15
3) " " Line Control A Pin 17*
4) " " Neutral Control A Pin 16*
5) " " Positive Control A Pin 12
6) " " Negative Control A Pin 29
7) " " Line Control B Pin 14
8) " " Neutral Control B Pin 13
9) " " Positive Control B Pin 12
10) " " Negative Control B Pin 29
11) " " Positive + 5 V Pin 6
12) Control Unit B
13) Control Unit A
14) Crew Warning Unit
15) Metal Box Containing single detector
16) Metal Box Containing dual detector
17) Log. Periodic monitoring antenna

Note:-
All systems units and 10nF Feedthrough capacitors bonded to the ground plane via copper braid. Cable length from unit to 10nF capacitors minimum of 2 metres, all cables 5cm min. above the ground plane.
Antenna 1 metre from test samples
Log Periodic monitoring antenna used between 4 dom/m and 1 GHz

358

Figure No 10 — RAYLINER FIRE DETECTION SYSTEM — TEST NO RS03

Appendix 2

Test Results

PAGE 1

Company GRAINGER LTD

Program Advanced Fire Detection System

Test No. CE.03

Test Specimen 115 V LINE CONTROL A PIN 14

Date 31-3-80

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 1, 2, 3

Section CE.03, CE.04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS-258, S.N

S.N.

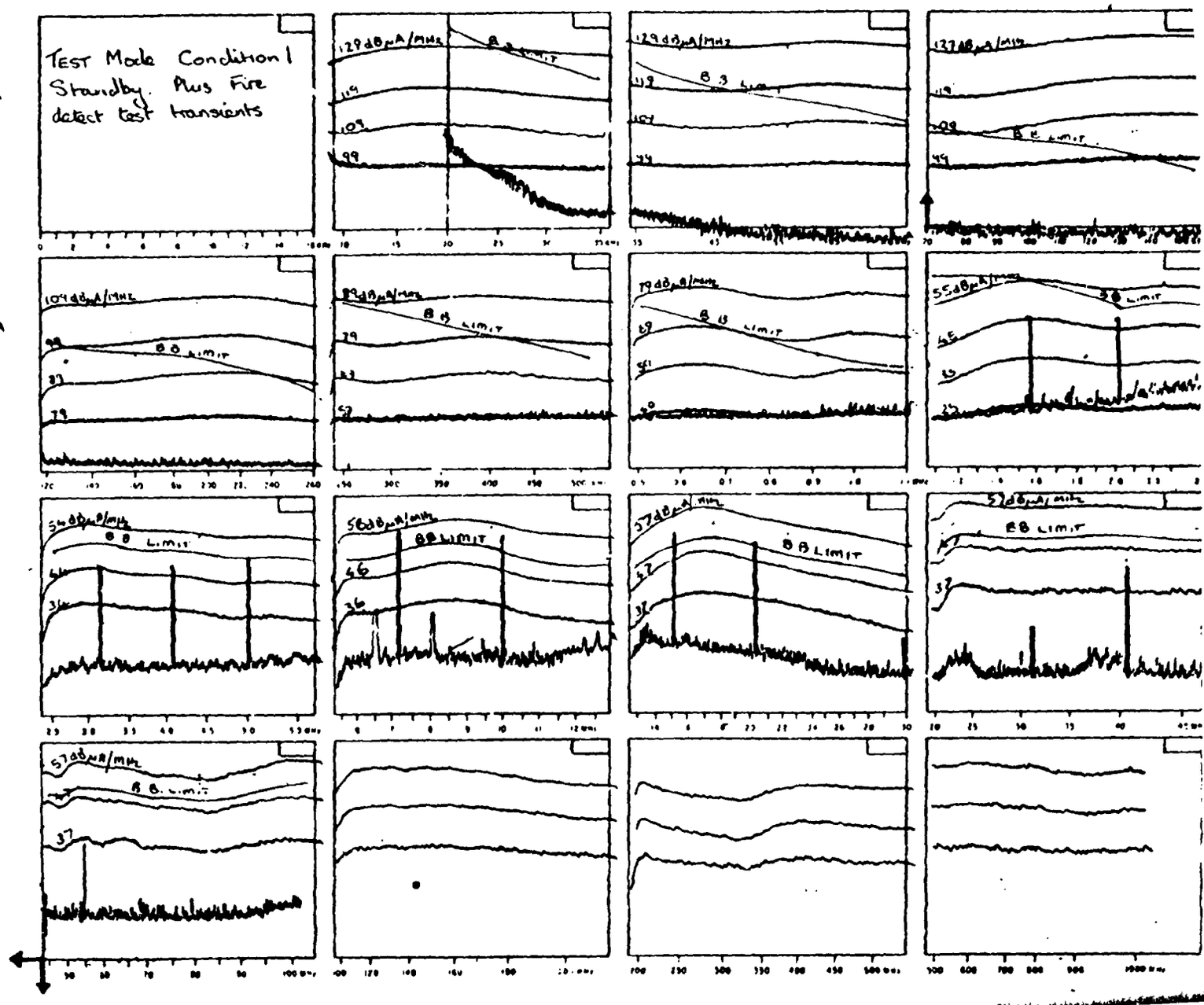
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 2

Company GORDINER LTD
Advanced Fire
Program Detection System

Test No. CE.03
115V Neutral
Test Specimen Control A
PIN 13

Date 31-3-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1, 2, & 3

Section CE 03, CE 04

Scan Speed 2 min/Band

Bandwidth WIDE

Detector PEAK

Atten Pos

TEST EQUIPMENT

FSS-250. S/N

S/N.

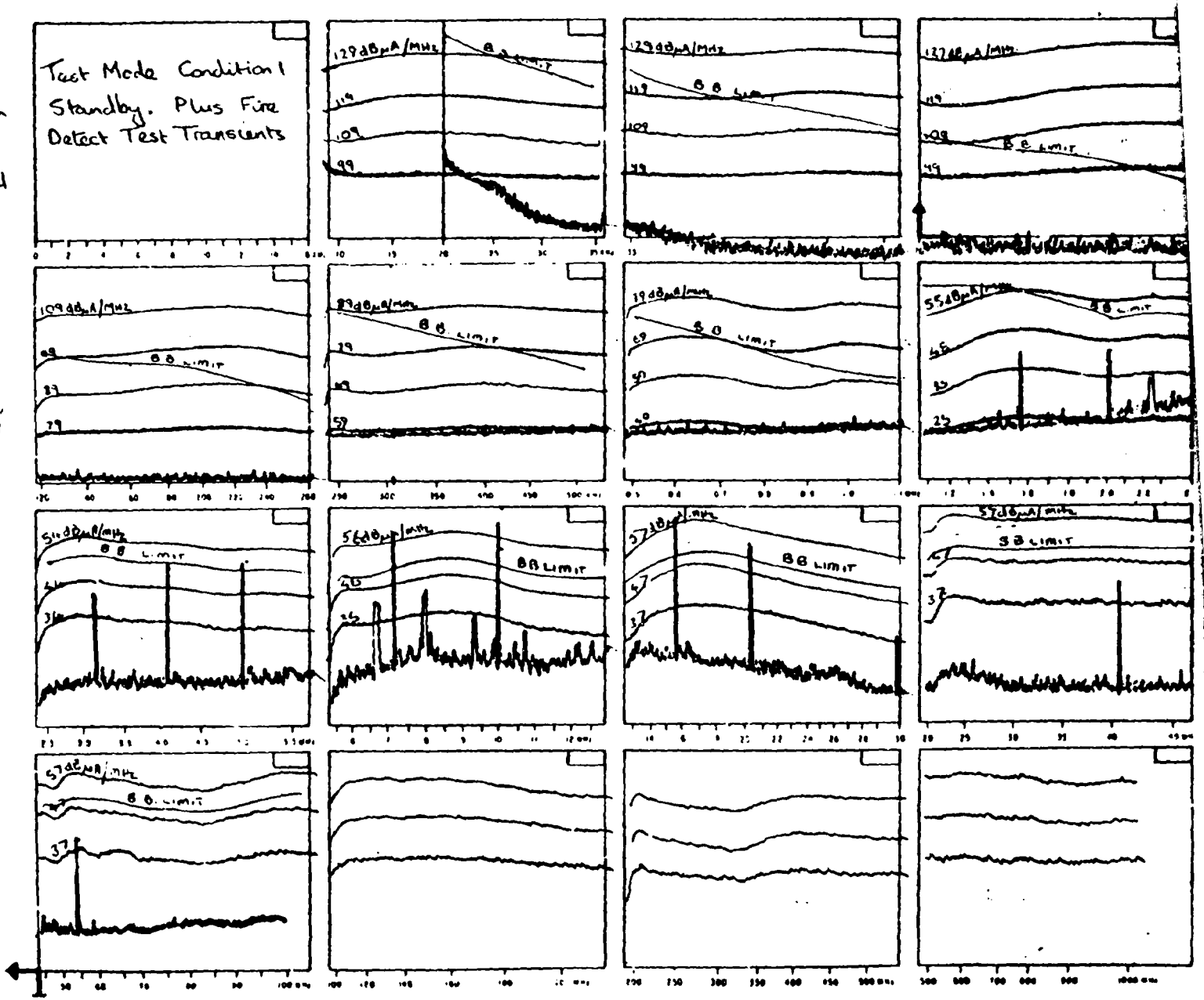
S/N.

S/N.

S/N.

S/N.

ELECTRO-METRICS



PAGE 3

Company GRAVINER LTD
Aluminal Fire
Program Detection System

Test No. CE.03

Test Specmen 22V dc Pos.
Control A
Pin 12

Date 31-3-80

Conducted By PPC

Test Spec MIL-STD-461A
NOTICE 1, 2, 3

Section CE03, CE04

Scan Speed 2mins/band

Bandwidth WIDE

Detector PEAK

Attn. Pos.

TEST EQUIPMENT

FSS-250, S.N.

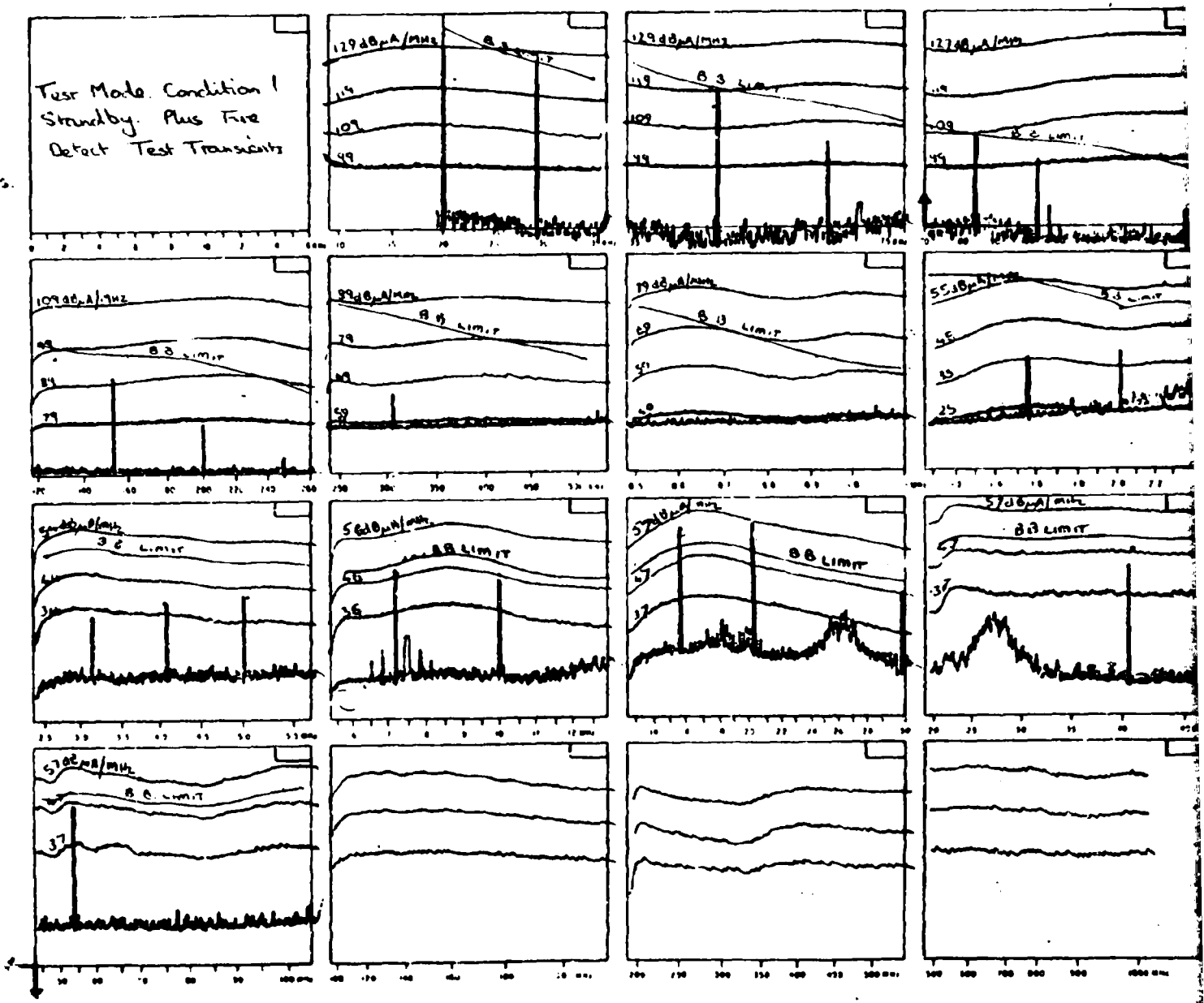
S.N.

S.N.

S.N.

S.N.

S.N.



PAGE 4

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE 03
28 Vdc Neg
Test Specimen Control A
Pin 29

Date 1-4-70

Conducted By PPC

Test Spec. MIL-STD-461A
Notice 1, 2 & 3

Section CE 03, CE 04

Scan Speed 2 mins/band

364 Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

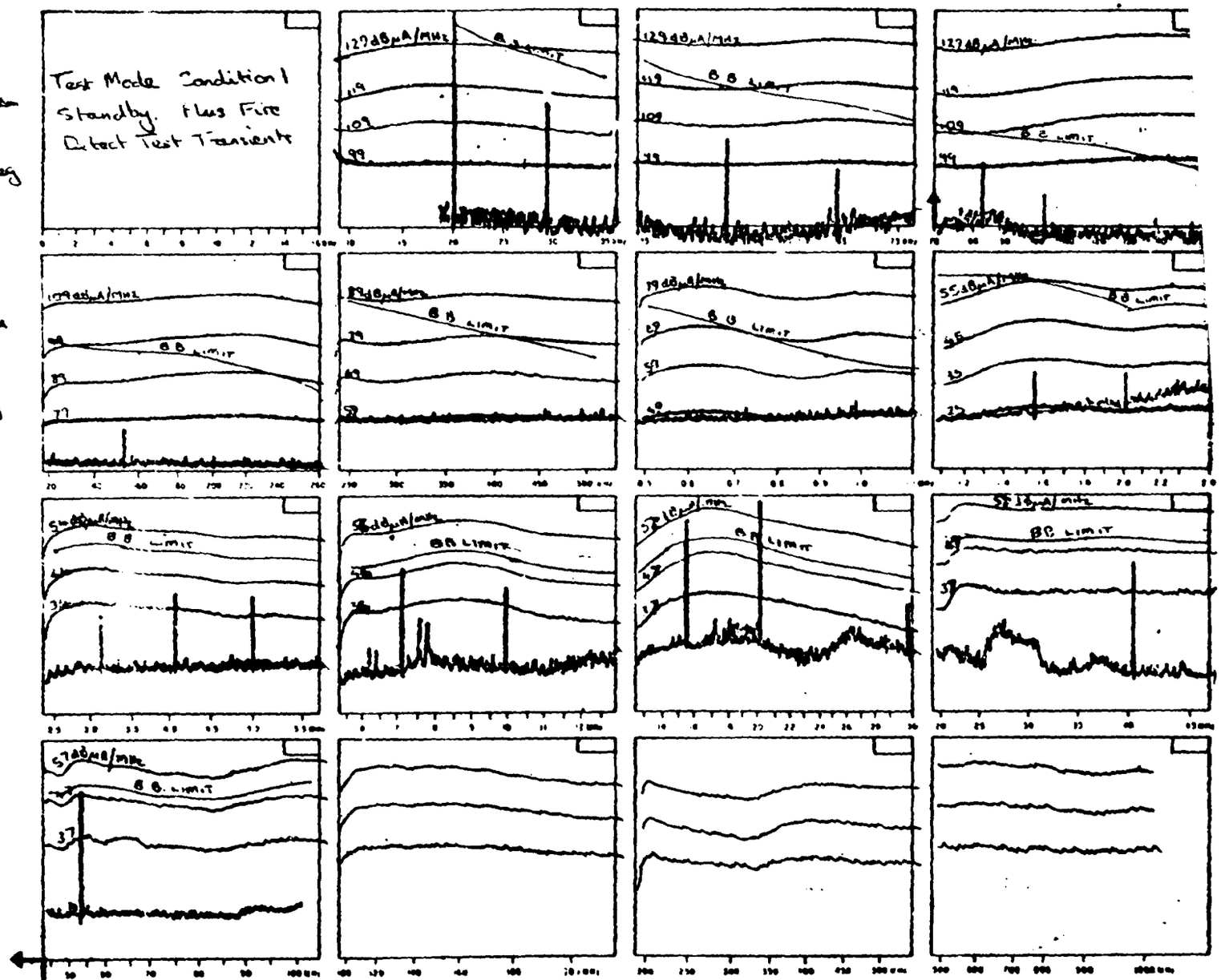
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 5

Company GRAVINER LTD
Advance Fire
Program Detection System

Test No CE-03

Test Specimen 115V Line
Control B
Pin 14

Date 1-4-30

Conducted By PPC

Test Spec MIL-STD-461A
NOTICE 1, 2, & 3

Section CE 03, CE 04

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

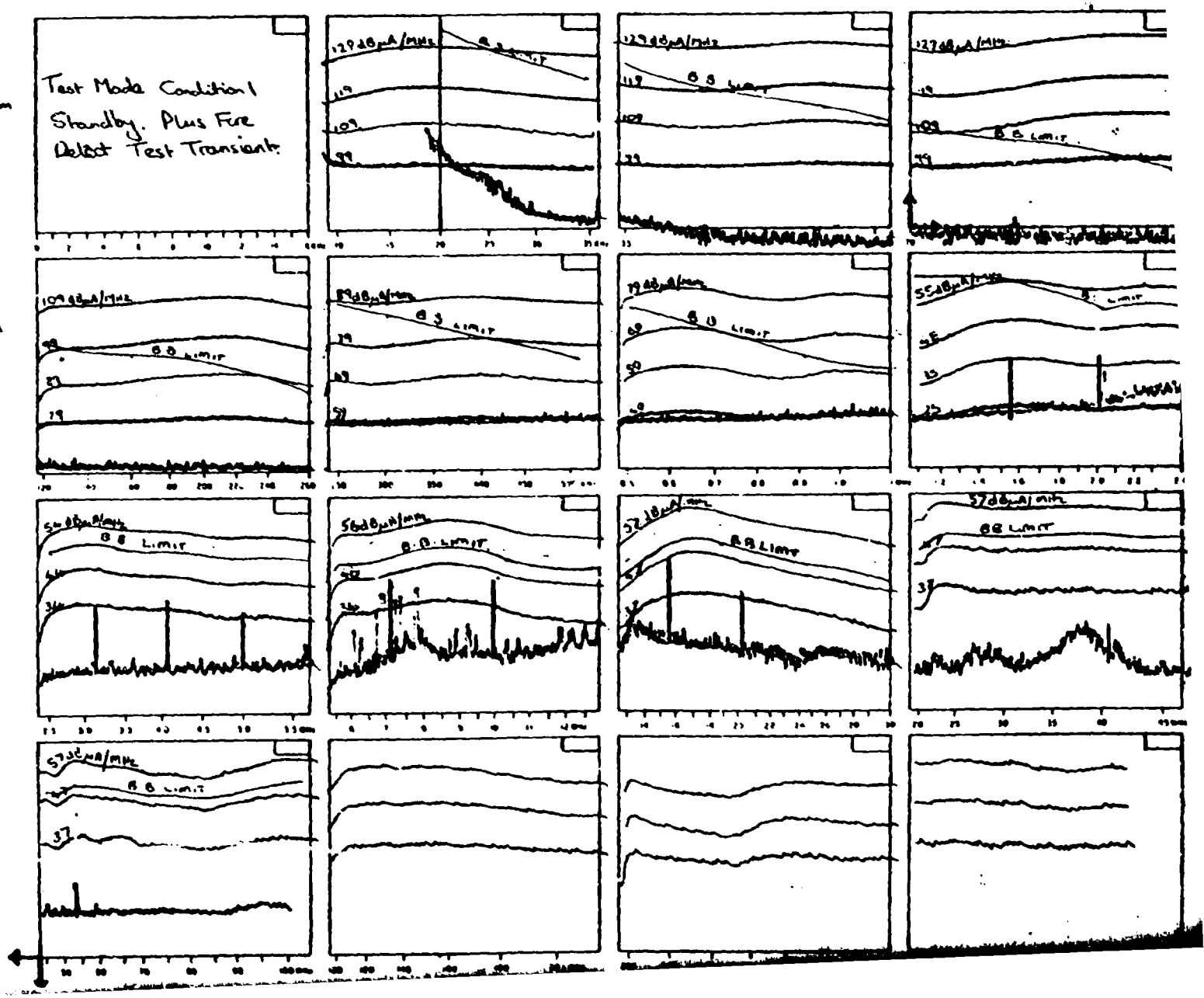
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 6

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE.03
115V Neutral
Test Specimen Control B
AN 13

Date 1-4-80

Conducted By PPC

Test Spec MIL-STD-461A
NOTICE 1, 2 & 3

Section CE 03, CE 04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

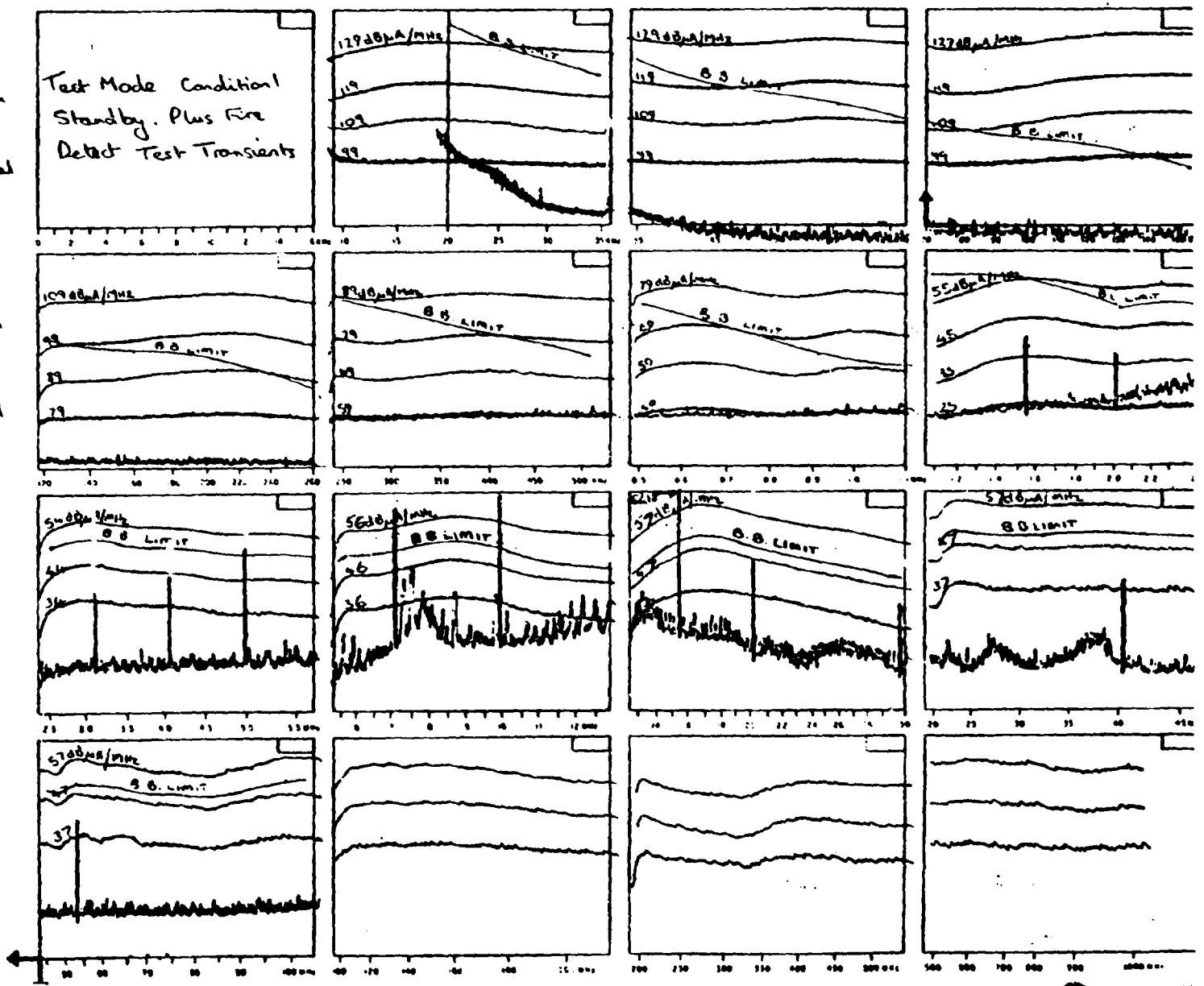
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 7

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No CE-03

Test Specimen 23V dc Pos
Control B
PIN 12

Date 1-4-80

Conducted By PPC

Test Spec MIL-STD-461A
Notice 1, 2 & 3

Section CE 03, CE 04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS 250. S.N.

S.N.

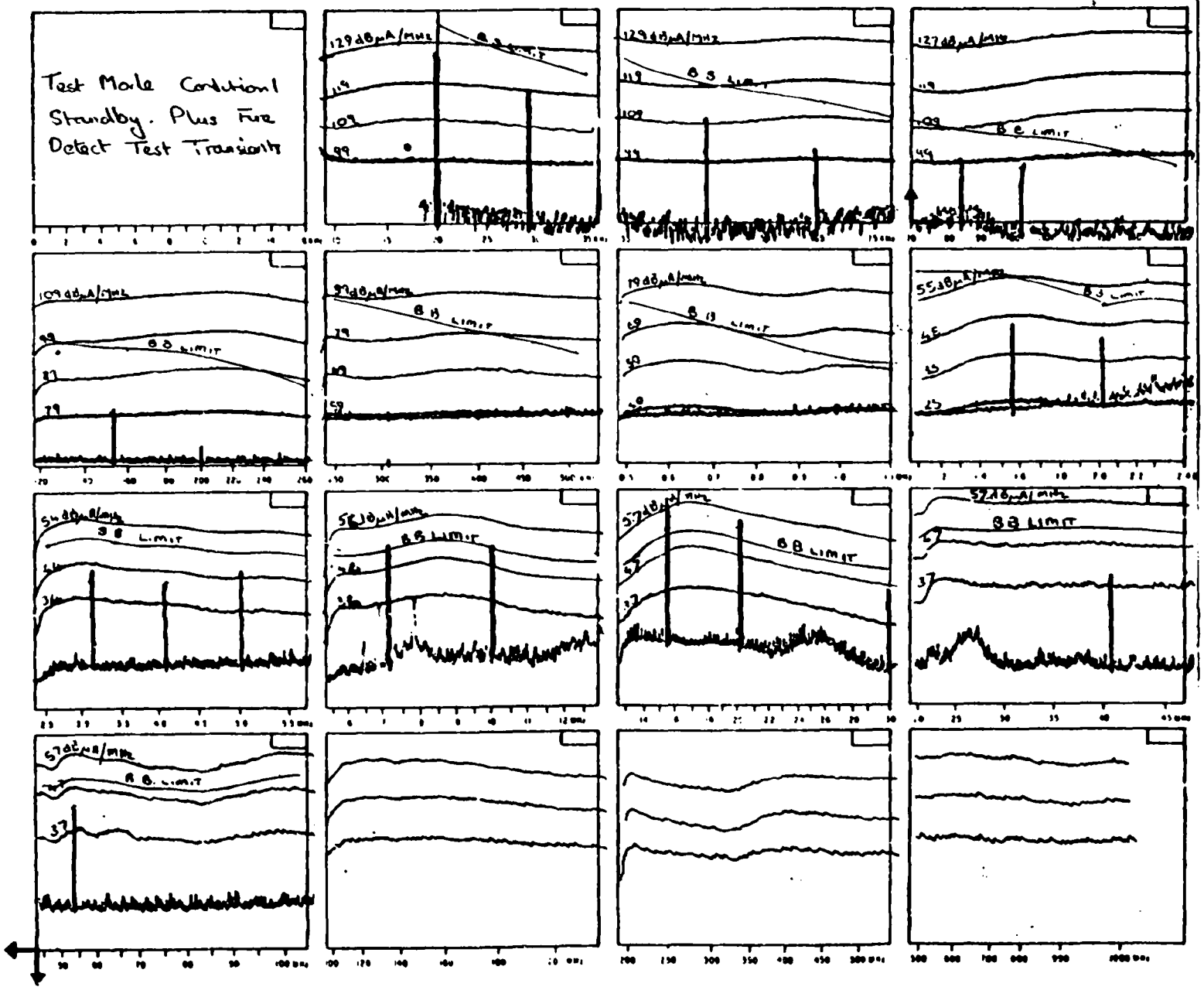
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 8

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE-03

Test Specimen Control B
28Vdc Neg
AN 29

Date 1-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1, 2, 03

Section CE03, CE04

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N. ____

____ S.N. ____

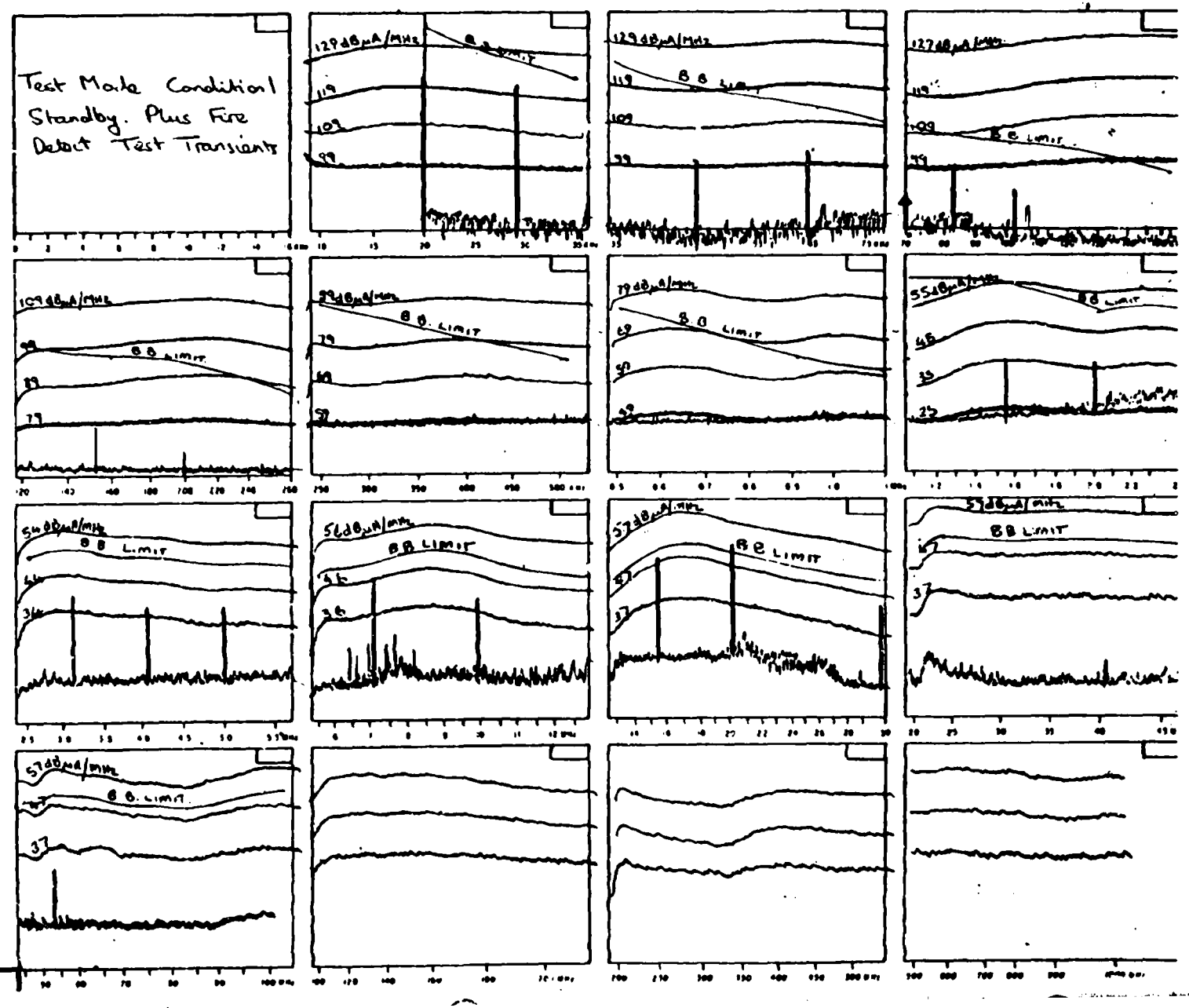
____ S.N. ____

____ S.N. ____

____ S.N. ____

____ S.N. ____

ELECTRO-METRICS



366

PAGE 9

Company GRAVINER LTD

Program Advanced Fire Detection System

Test No. CE 03

Test Specimen 28 V dc Pos Crew Warning Unit Pin 6

Date 8-4-30

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 1, 2 & 3

Section CE03, CE04

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

S.N.

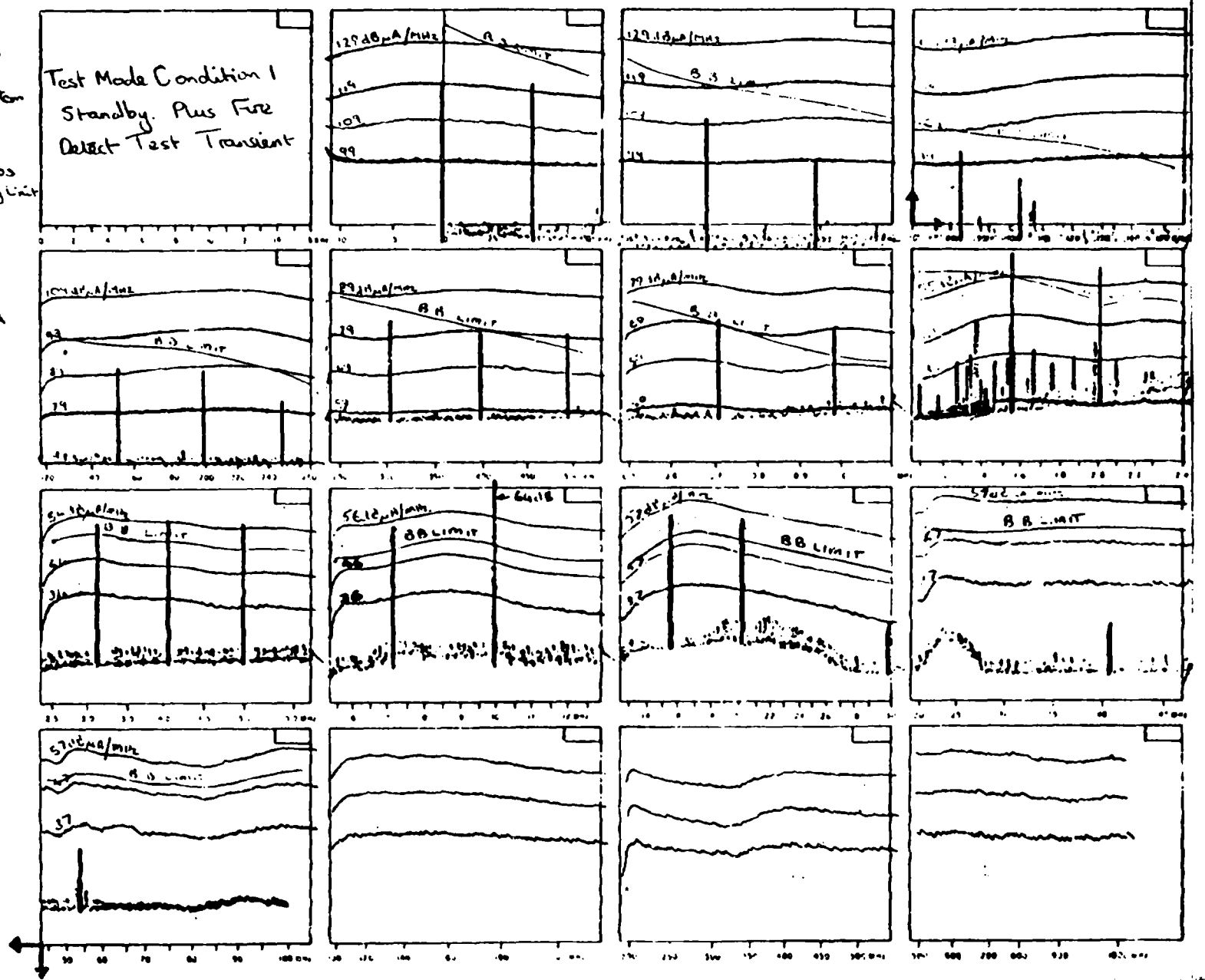
S.N.

S.N.

S.N.

ELECTRO-METRICS

Test Mode Condition 1
Standby. Plus Fire
Detect Test Transient



PAGE 10

Company GRAUNER LTD
Advanced Fire
Program Detection System

Test No CE-03

Test Specimen 115V Line
CONTROLA
P/N 14

Date 31 - 3 - 80

Conducted By _____

Test Spec. MIL-STD-461A
NOTICE 1, 2 & 3

Section CE 03 CS 04

Scan Speed 2 secs/band

Bandwidth WIDE

Detector Peak

Atten. Pos. _____

TEST EQUIPMENT

FSS-250, S.N. _____

_____ S.N. _____

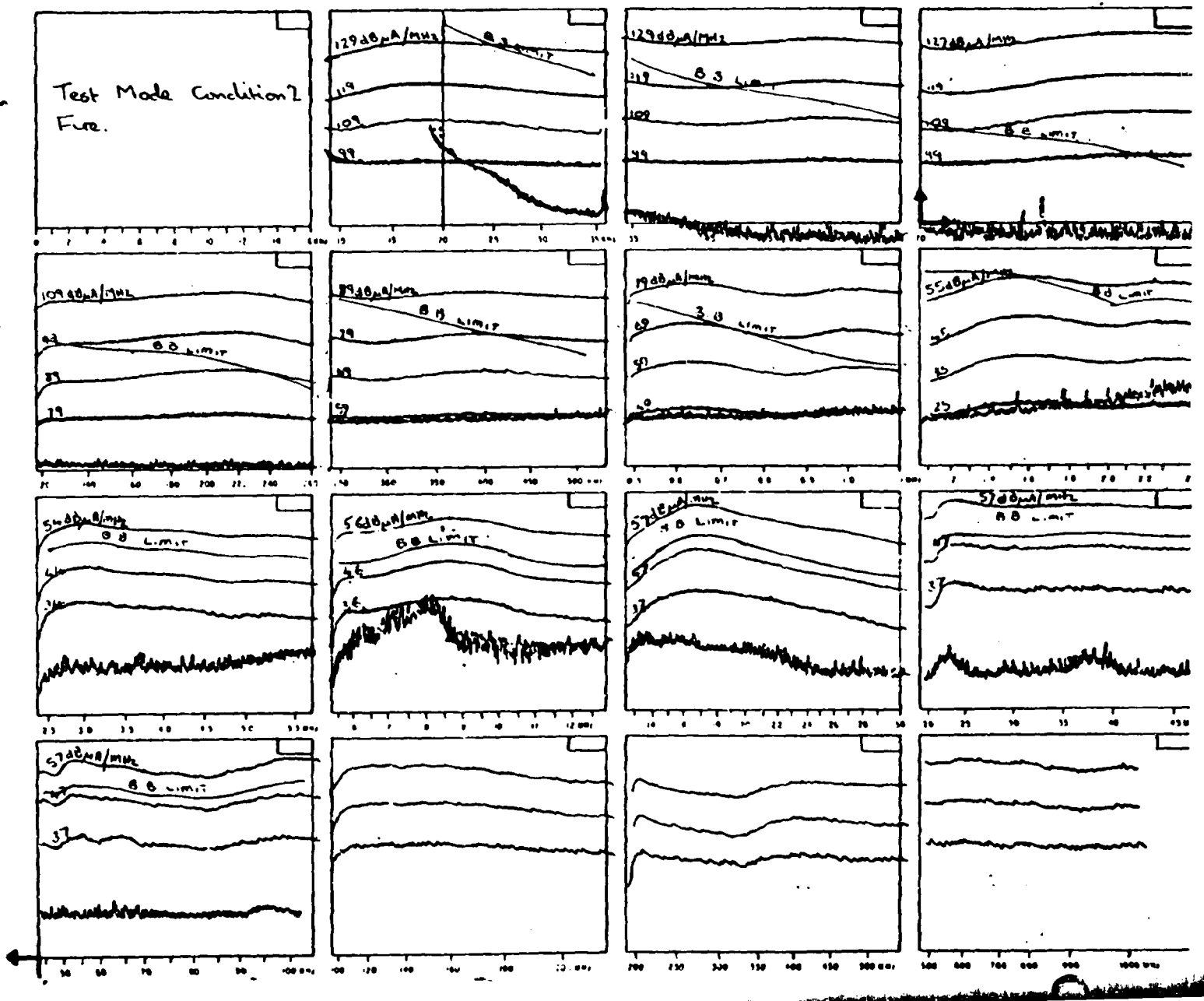
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS



270

PAGE 11

Company GRAVINER LTD

Program Advanced Fire Detect System

Test No. CE-03

Test Specimen 115V Neutral Control A Pins 13

Date 1-4-30

Conducted By PPC

Test Spec. MIL-STD-461A Notice 1, 2, & 3

Section CE 03, CE 04

Scan Speed 2mins/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

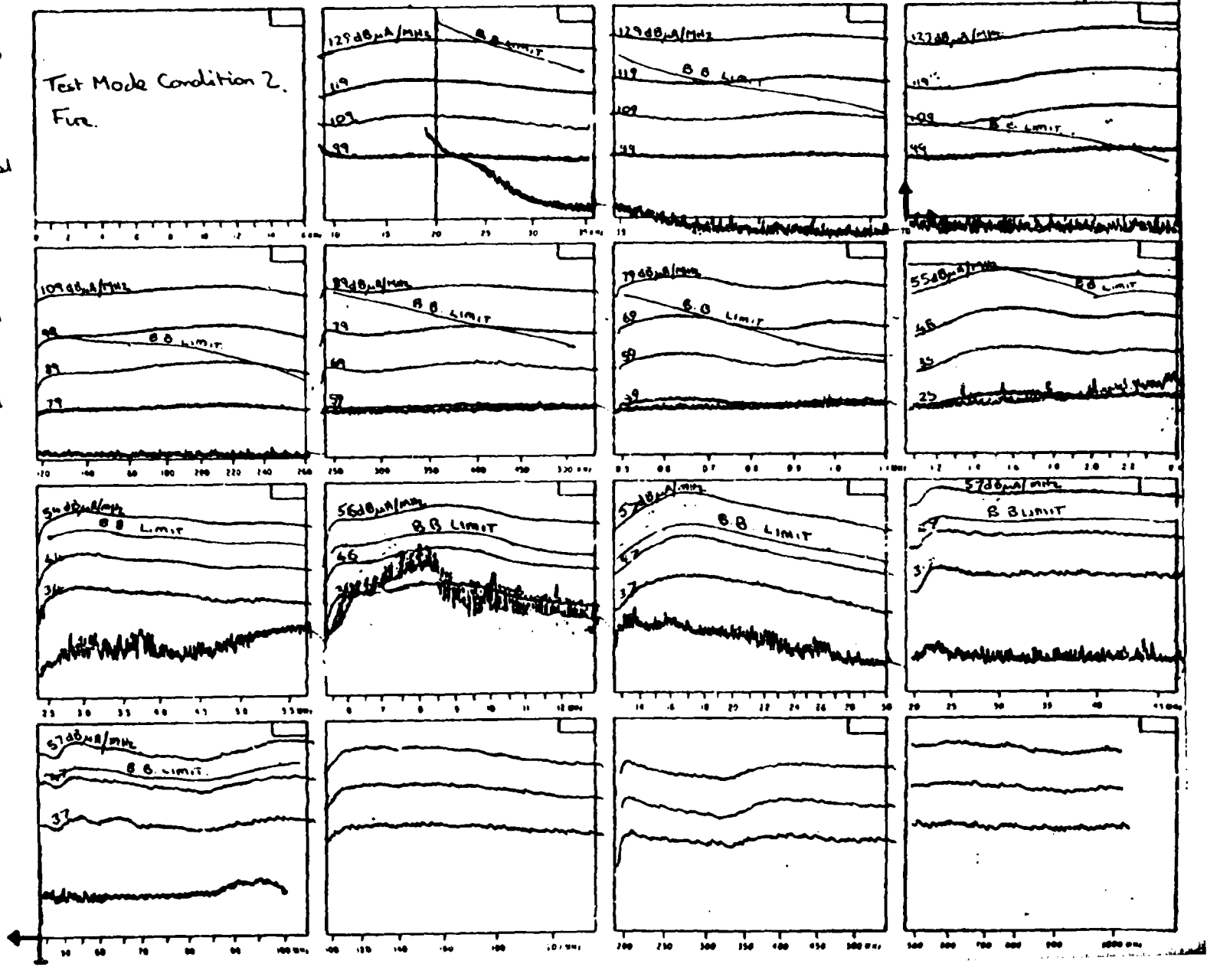
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 12

Company GRAVINER LTD
Advanced Fire
Program Detect System

Test No. CC-03
22 V dc Pos

Test Specimen Control A
P/N 12

Date 1-4-90

Conducted By PPC

Test Spec. MIL-STD-461A
Notice 1, 2, & 3

Section CE 03, CE 04

Scan Speed 2 min/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS-258. S/N

S/N

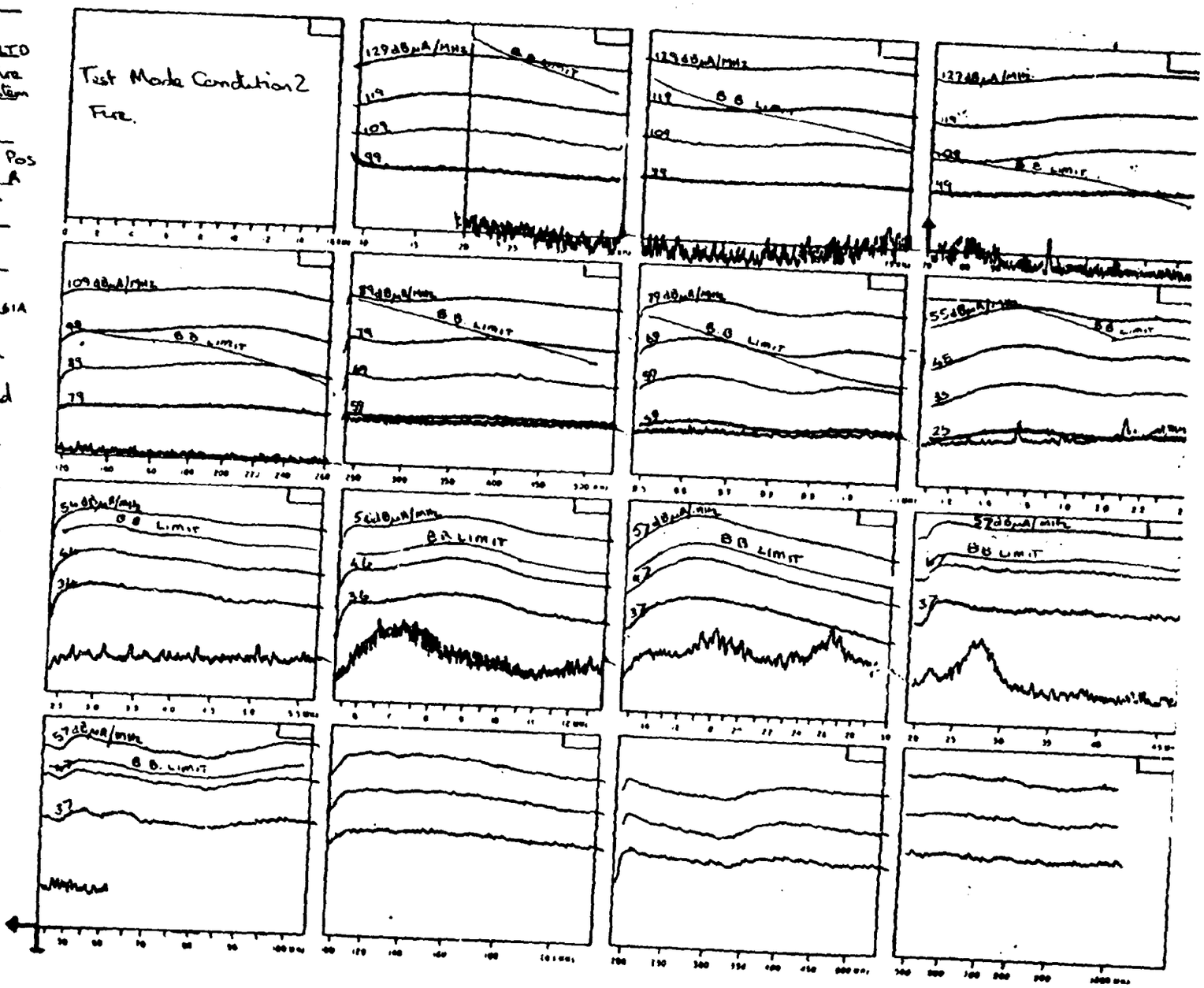
S/N

S/N

S/N

S/N

ELECTRO-METRICS



PAGE 13

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE.03

Test Specimen 28 v dc Neg
Control A
Pin 29

Date 1-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1, 2, & 3

Section CE03, CE04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector PEAK

Attea. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

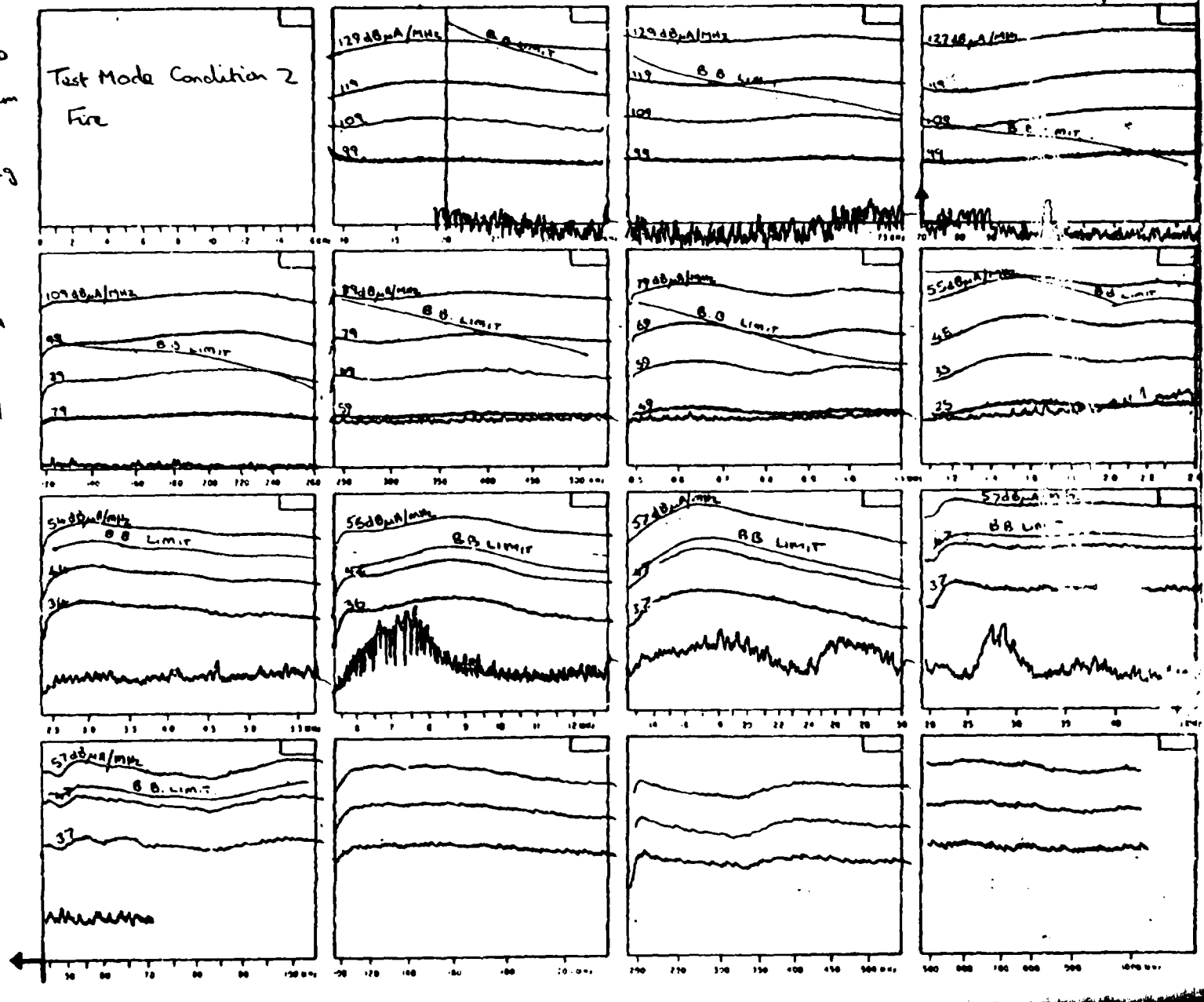
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 14

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE.03

Test Specimen 115V Line Power
Control B

Date 1-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1, 2, 03

Section CE03, CE04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector PEAK

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

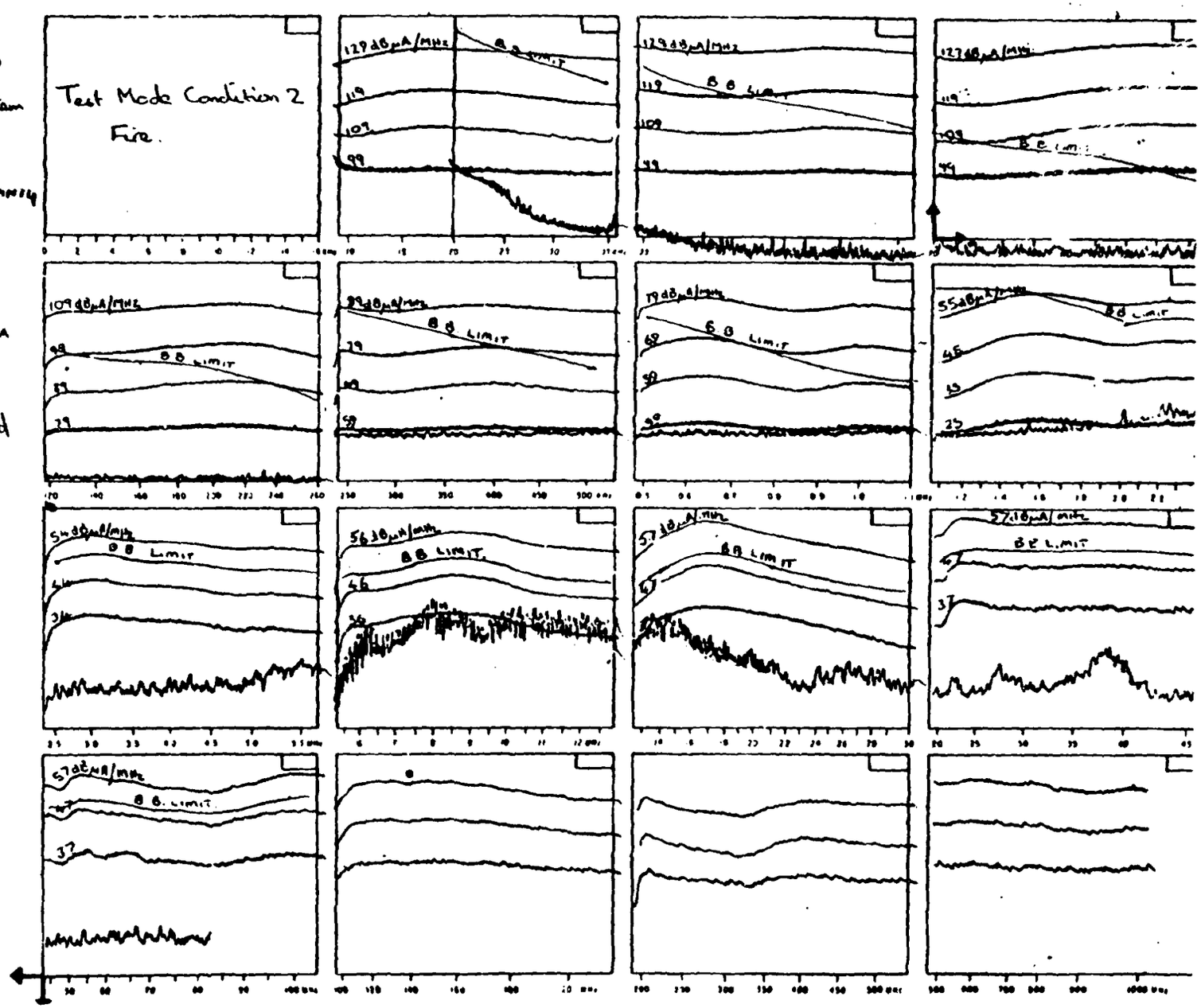
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 15

Company GRAYNER LTD
Advanced Fire
Program Detection System

Test No. CE 03

Test Specimen 115 V Neutral
Control B PIN 13

Date 1-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1, 2, & 3

Section CE 03, CE 04

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

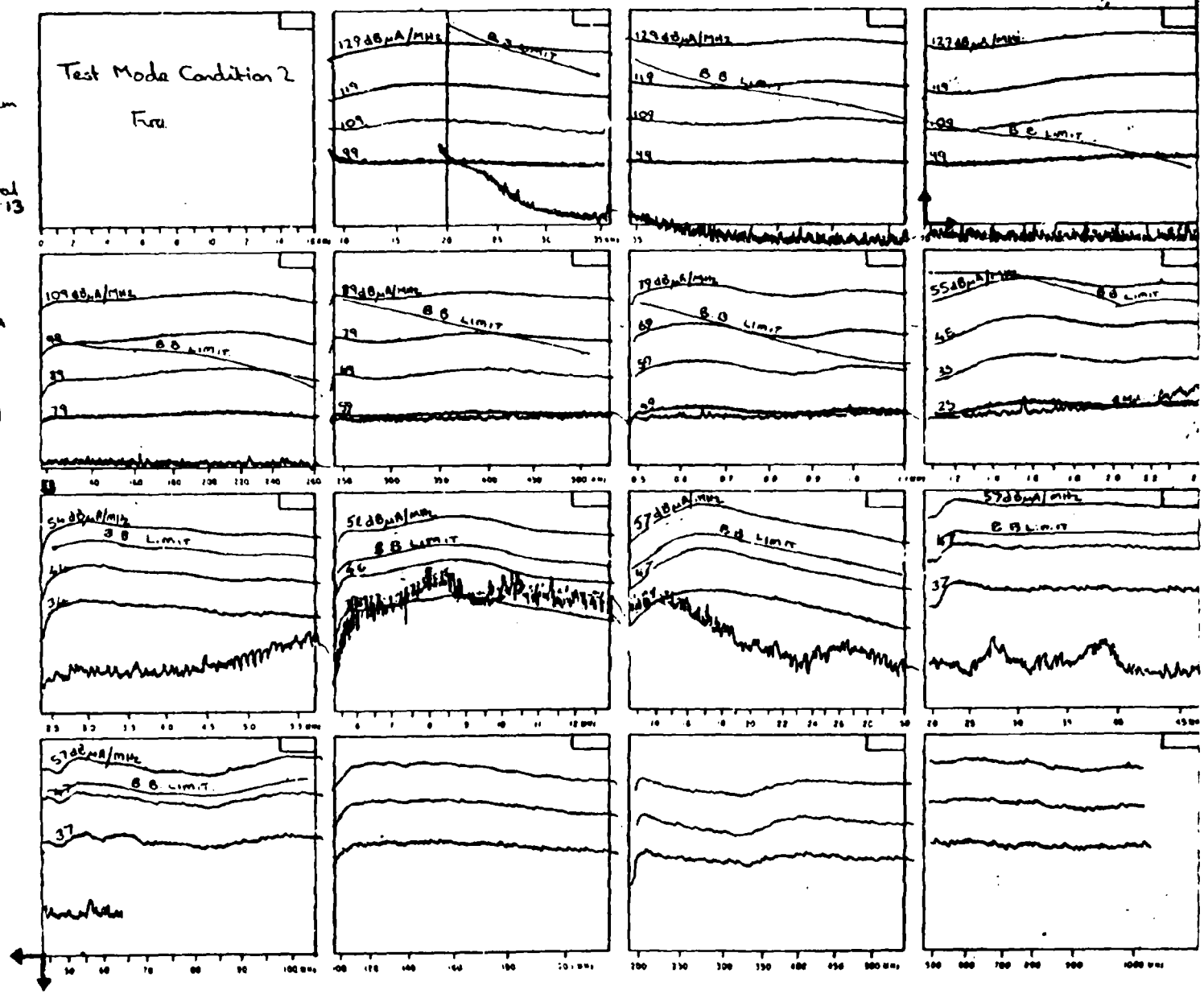
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 16

Company GRAVINER LTD

Program Advanced Fire Detection System

Test No. CE-23

Test Sample 22V dc Pos Control B Panel

Date 1-6-88

Conducted By PPC

Test Spec MIL-STD-461A NOTICE 1, 2, & 3

Section CE03, CE04

Scan Speed 2min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-256, S/N

S/N

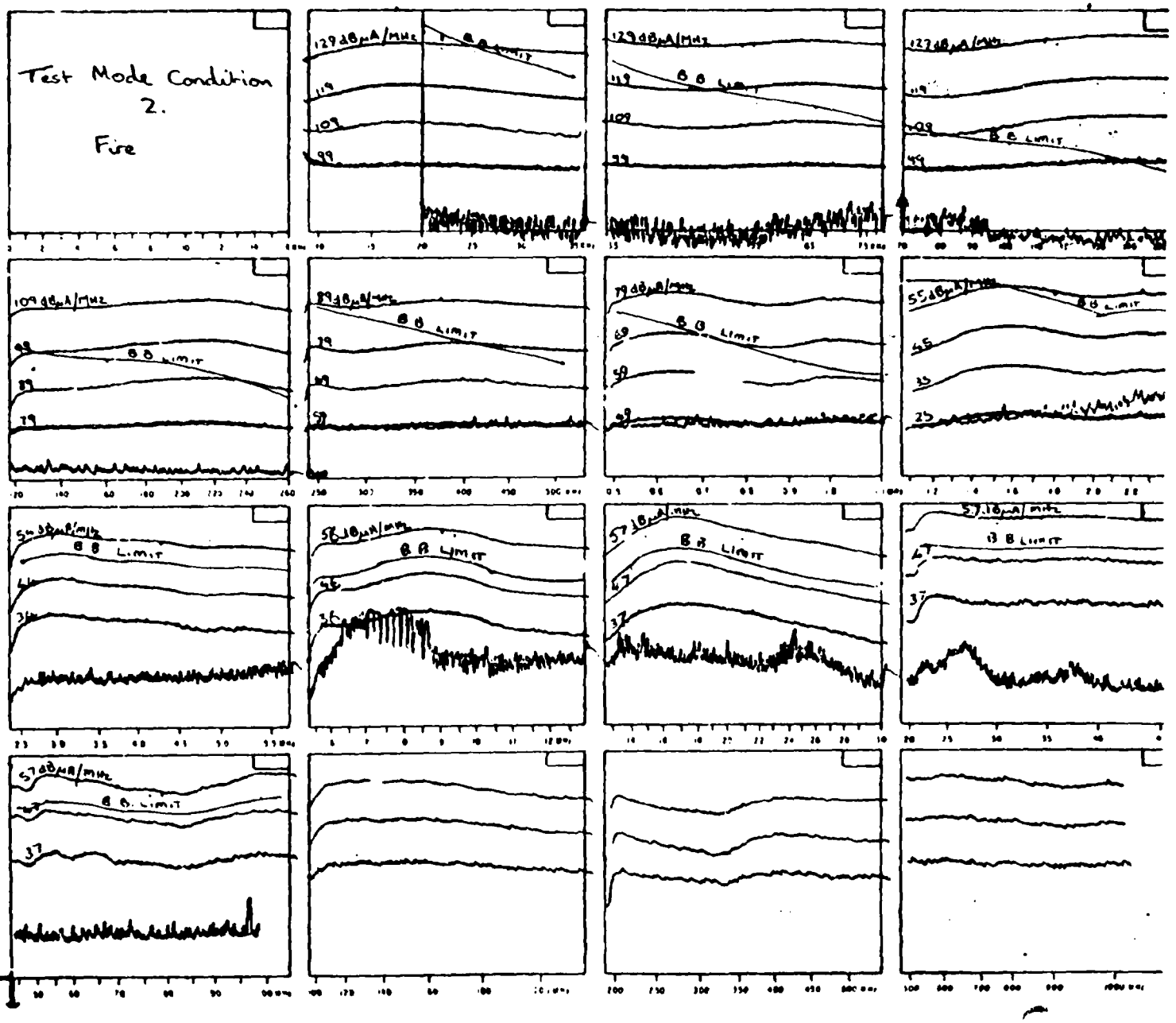
S/N

S/N

S/N

S/N

ELECTRO-METRICS



PAGE 17

Company GRAV: R LTD

Program Advanced Fire Detection System

Test No CE 03

Test Specimen 28V dc Neg. Control B. Part 2

Date 1-4-80

Conducted By PPC

Test Spec MIL-STD-461A NOTICE 1,2,3.

Section CE03 CE 04.

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

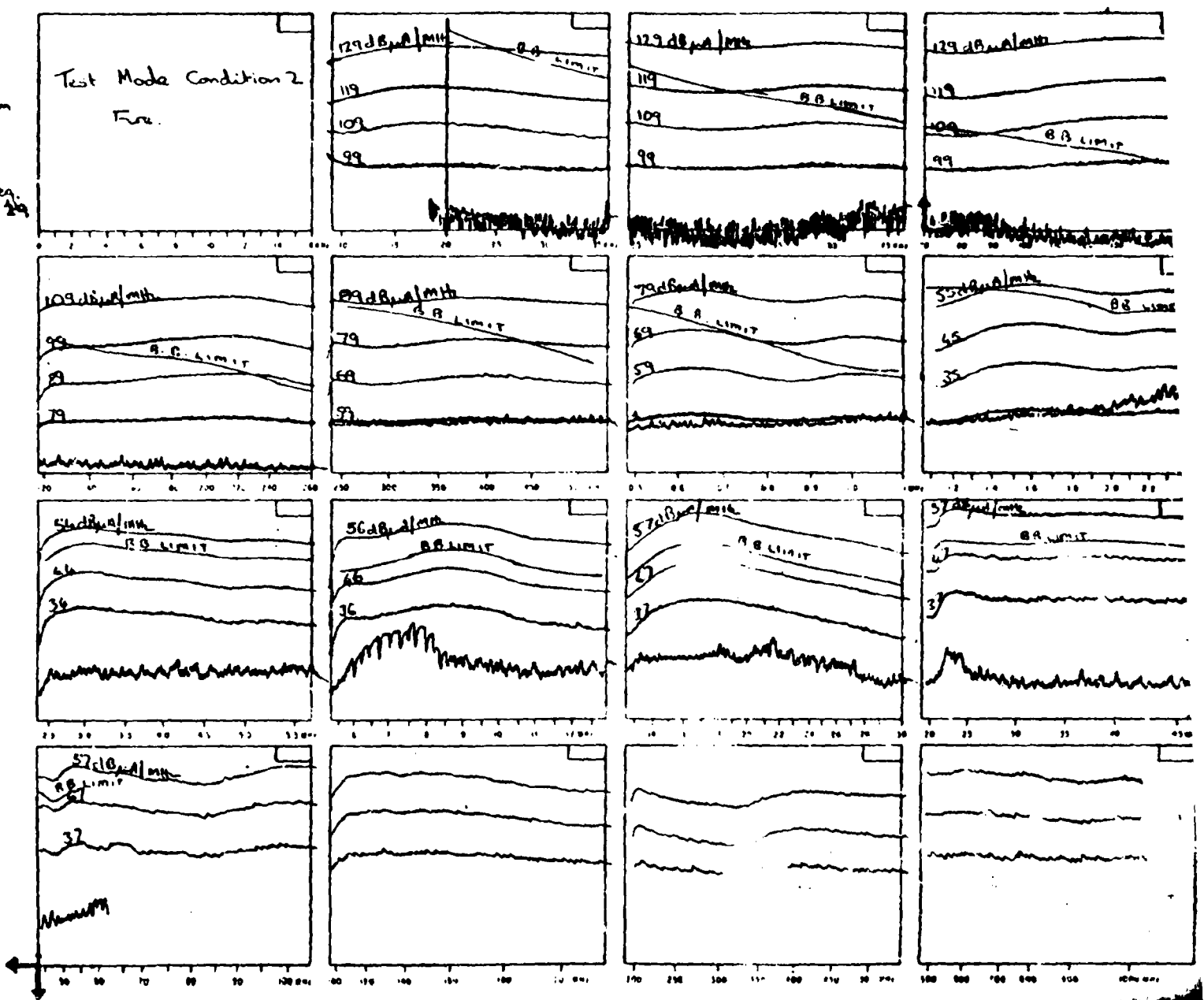
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 18

Company SCRANTON LTD

Program Advanced Fire Detection System

Test No CE 03

Test Specimen 27 V dc Pos
Fire 6

Date 8-6-90

Conducted By PPC

Test Spec MIL-STD-461A
NOTICE 3

Section CE03

Scan Speed 2 mm/second

Bandwidth NBE

Detector PEAK

Atten Pos

TEST EQUIPMENT

FSS 250. S/N

S/N

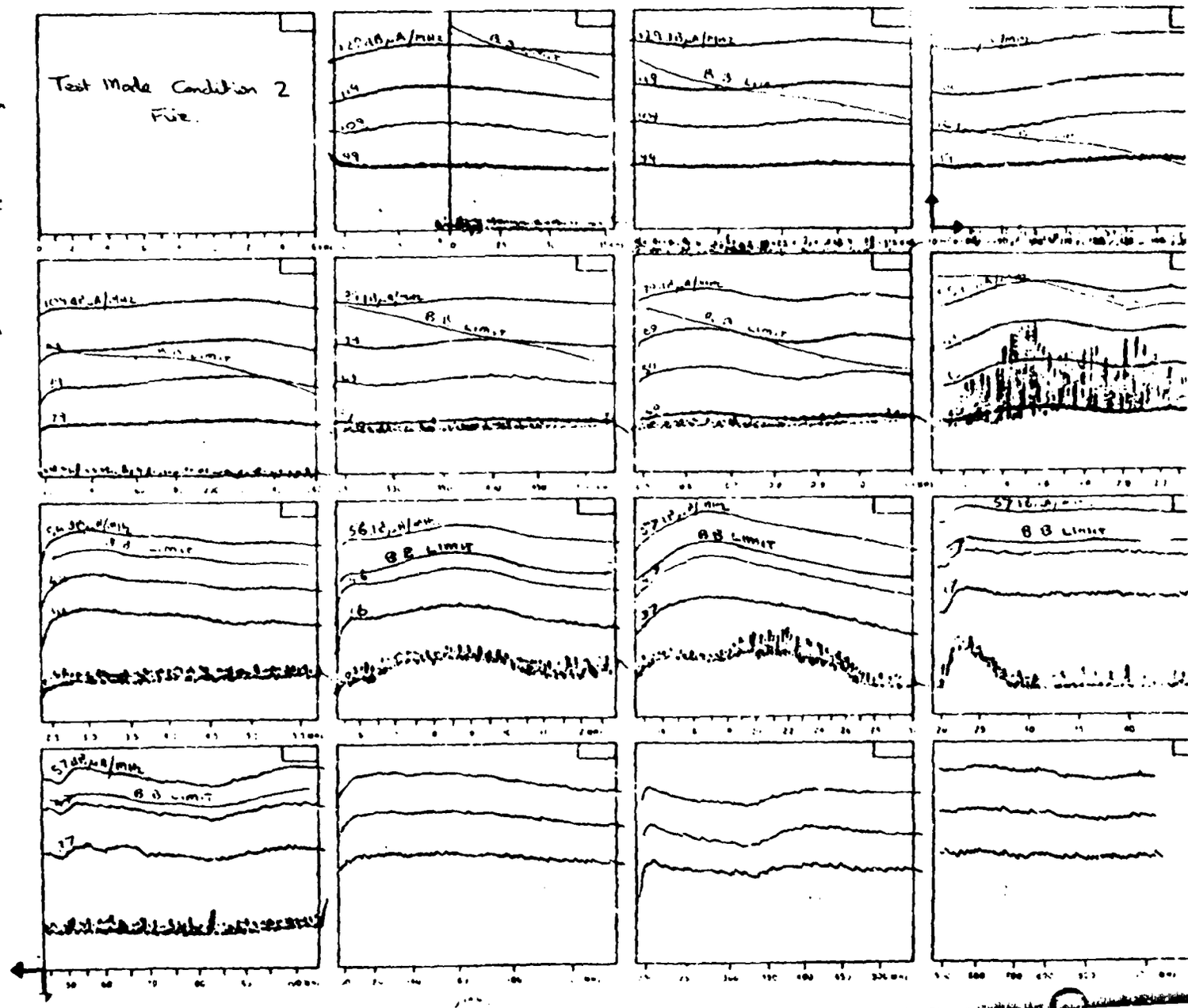
S/N

S/N

S/N

S/N

ELECTRO-METRICS



PAGE 19

Company GRAVINER LTD

Program Advanced Fire Detection System

Test No. CE04
Bunch 1

Test Specimen All leads Detectors control units and C.I.E. as supplied

Date 1-4-90

Conducted By PPC

Test Spec MIL-STD-461D NOTICE 3

Section CE03, CE04

Scan Speed 2 mins / band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250. S/N

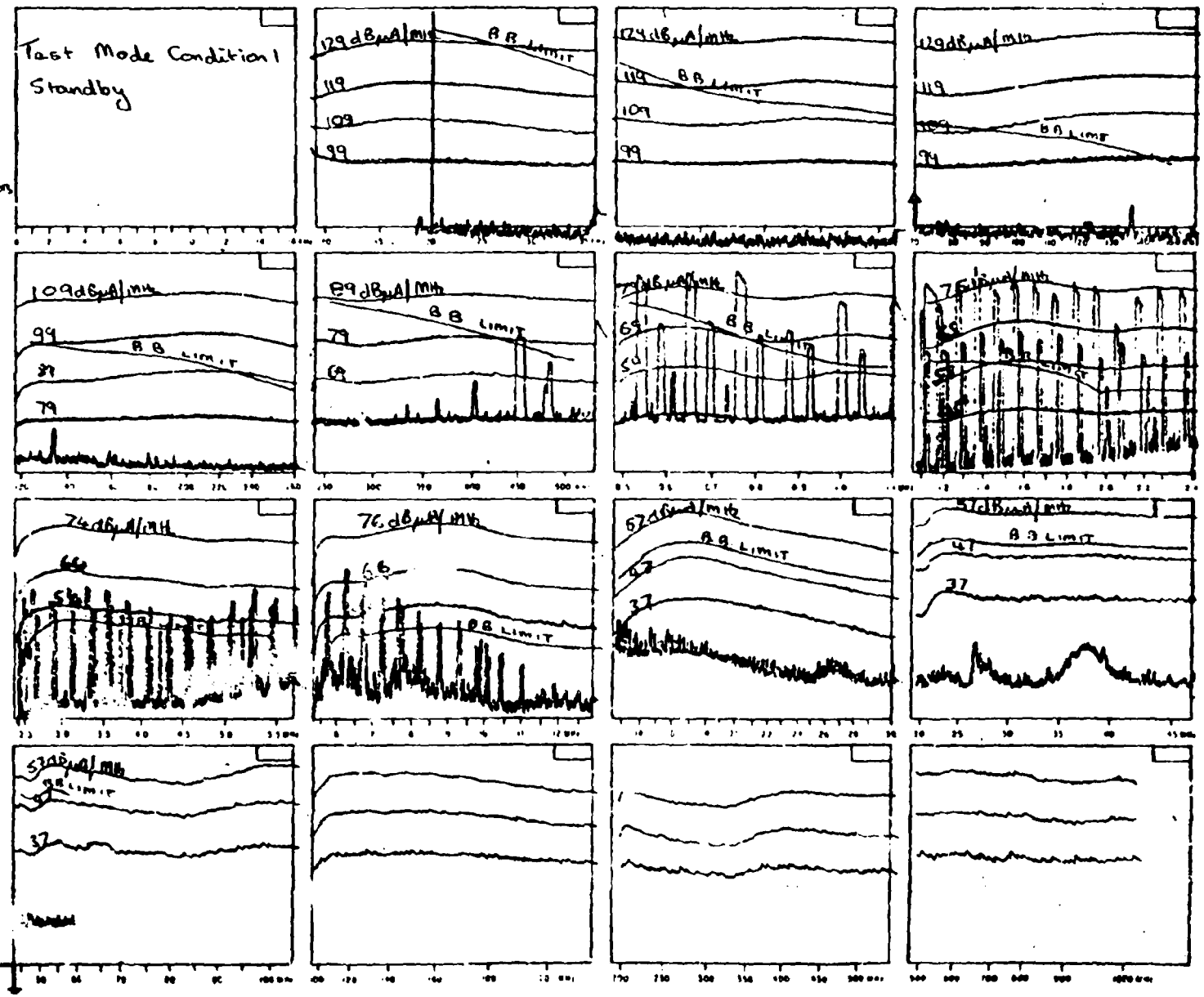
S/N

S/N

S/N

S/N

S/N



PAGE 20

Company GRAVINER LTD

Program Advanced Fire Detection System

Test No CE04 Bunch 2

Test Specimen Single Detector long cable bunch

Date 1 - 4 - 80

Conducted By PPC

Test Spec. MIL-STD-461A Notice 3.

Section CE03 CE04

Scan Speed 2 mins/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-256. S/N

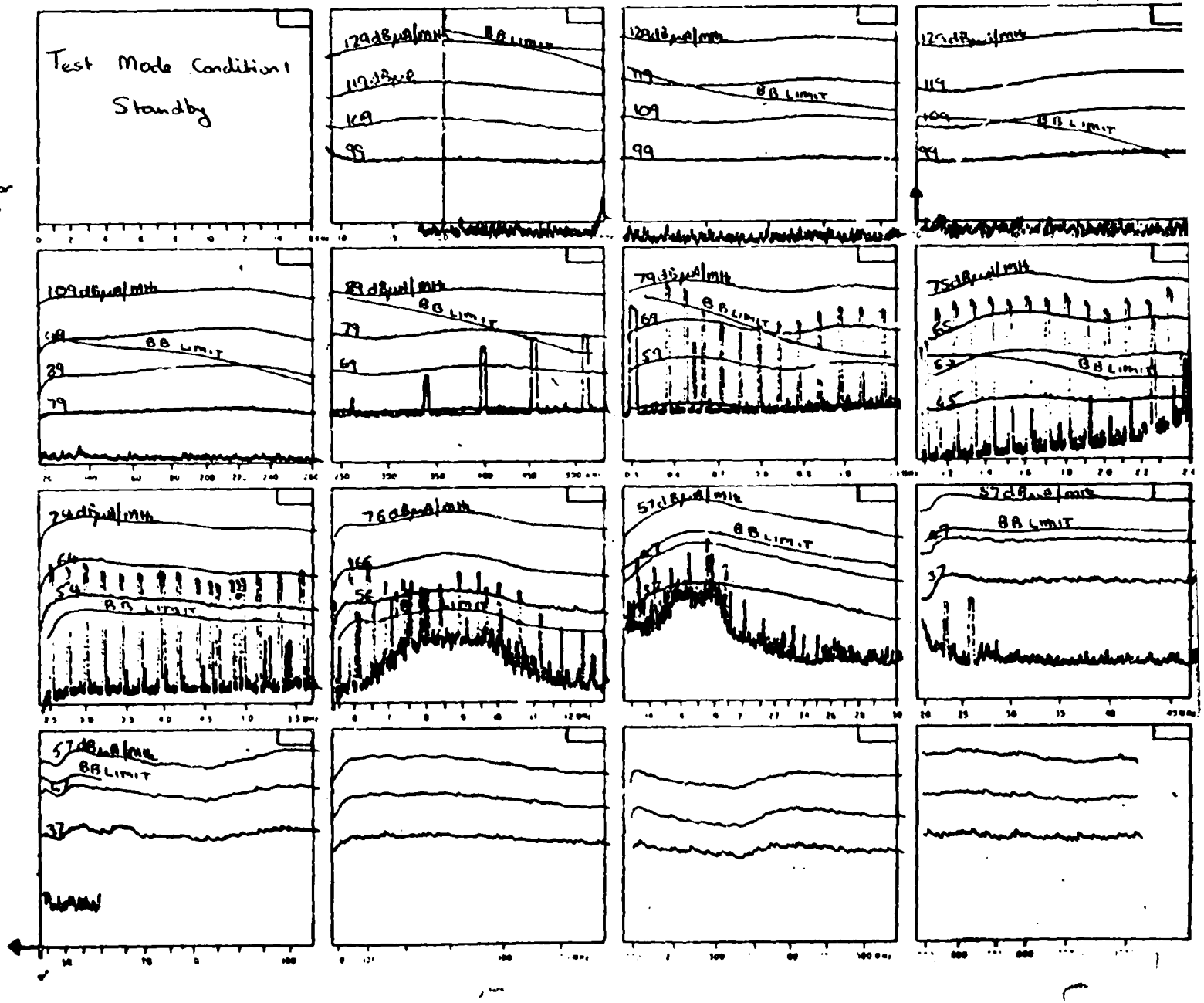
S/N

S/N

S/N

S/N

S/N



PAGE 21

Company GRAMMER LTD
Advanced Fire
Program Detection System

Test No CE 04
Bunch 3

Test Specimen Quad Detector
long cradle bunch

Date 1-4-90

Conducted By PPC

Test Spec MIL-STD-461A
Notice 3

Section CE04-CE03

Scan Speed 2min/band

Bandwidth WIDE

Detector Peak

Atten Pos

TEST EQUIPMENT

FSS-250. S.N.

S.N.

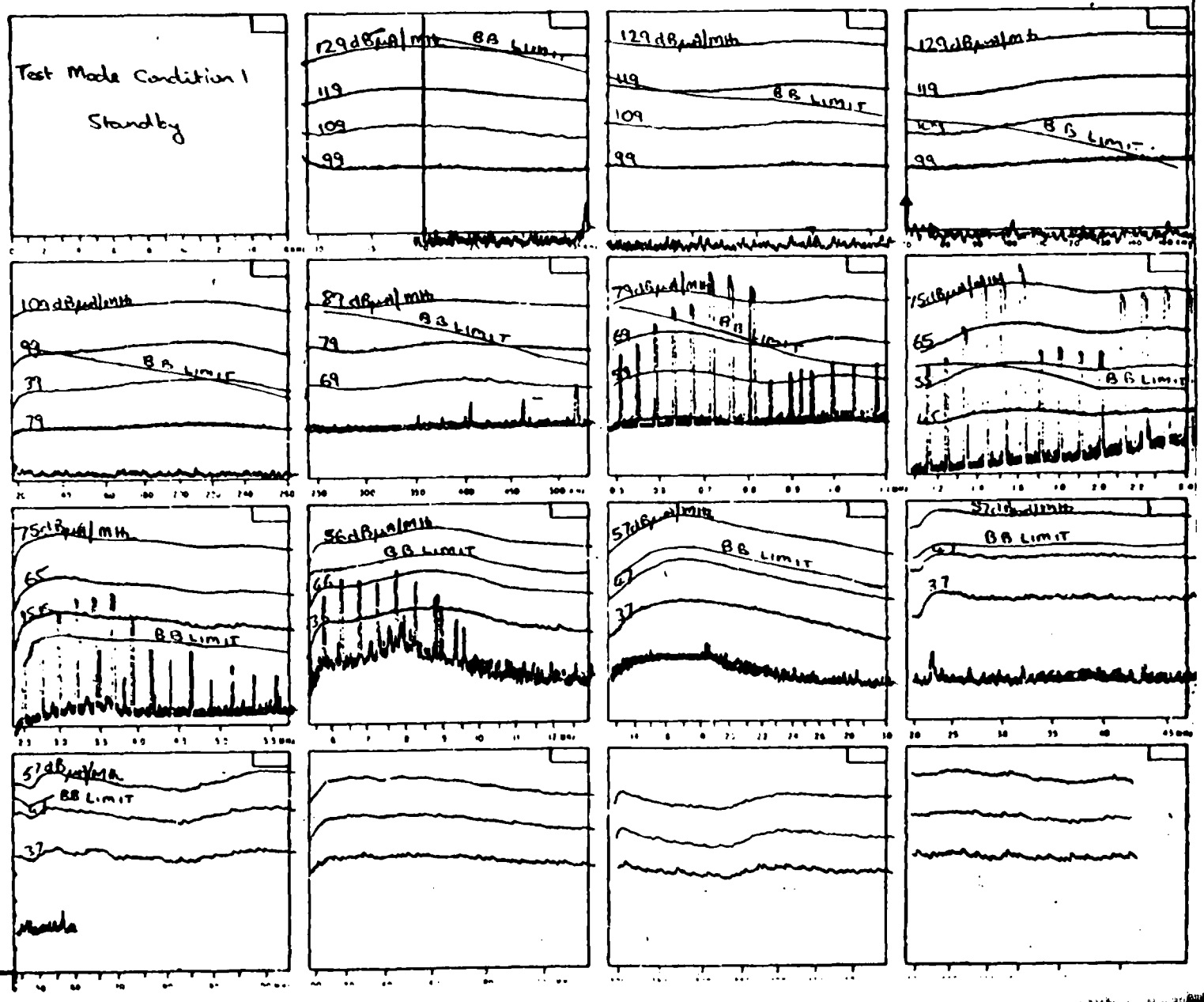
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 22

Company GRUMMAN ASD
Aircraft Fire
Program Detection System

Test No CE04
Bunch 1

Test Specimen All Inputs/Effectors
Control Units and W/U Eq.
P. Stiffler

Date 1-6-82

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section CE03 - CE04

Scan Speed 2 runs/band

Bandwidth WIDE

Detector Peak

Atten Pos

TEST EQUIPMENT

FSS-250, S.N.

S.N.

S.N.

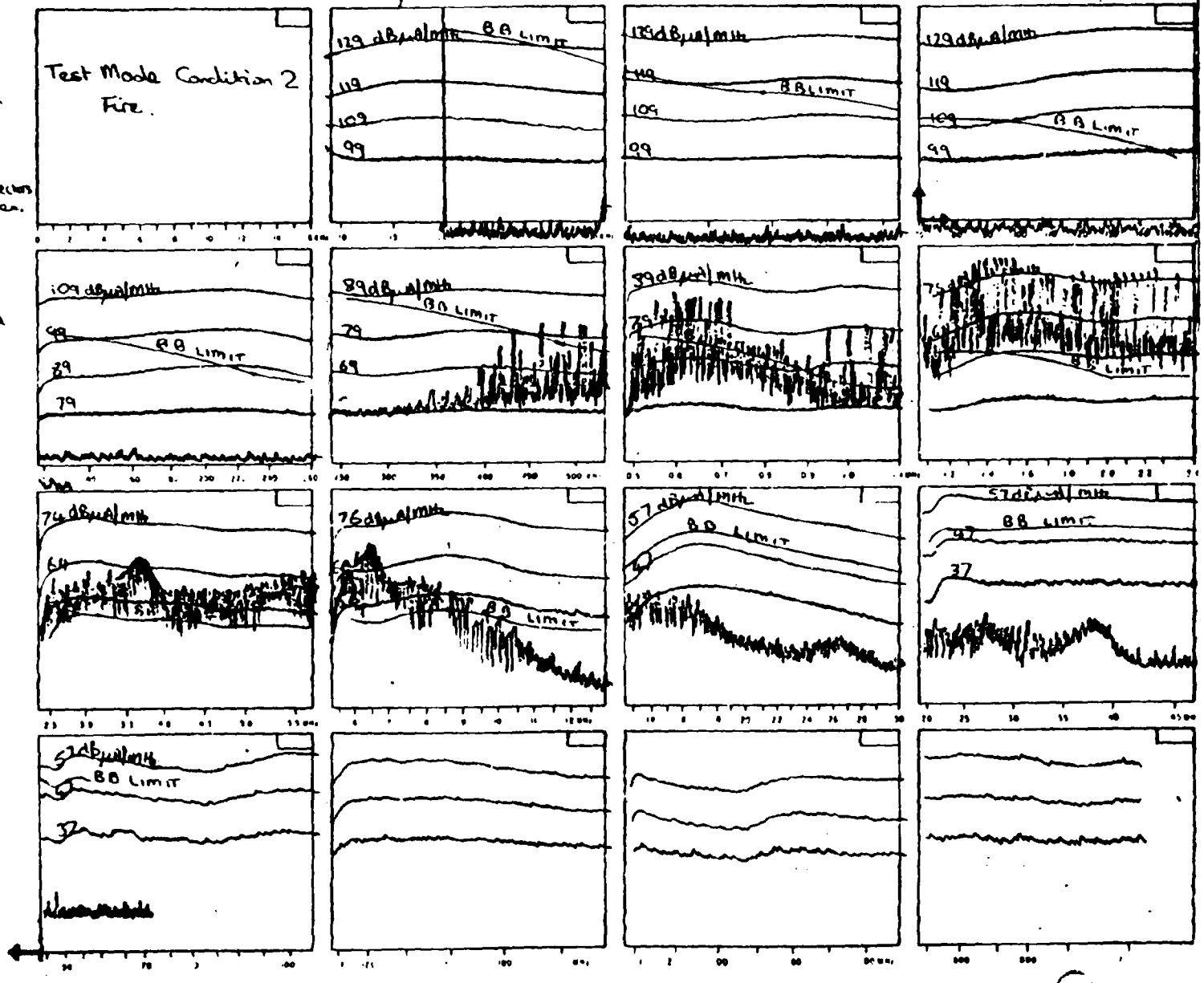
S.N.

S.N.

S.N.

ELECTRO-METRICS

3492



PAGE 23

Company GRAYLINER LTD

Program Advanced Fire Detection System

Test No CE04 Bunch 2

Test Specimen Single Detector long with bunch

Date 1-6-80

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 3

Section CE03 CE04

Scan Speed 2 min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

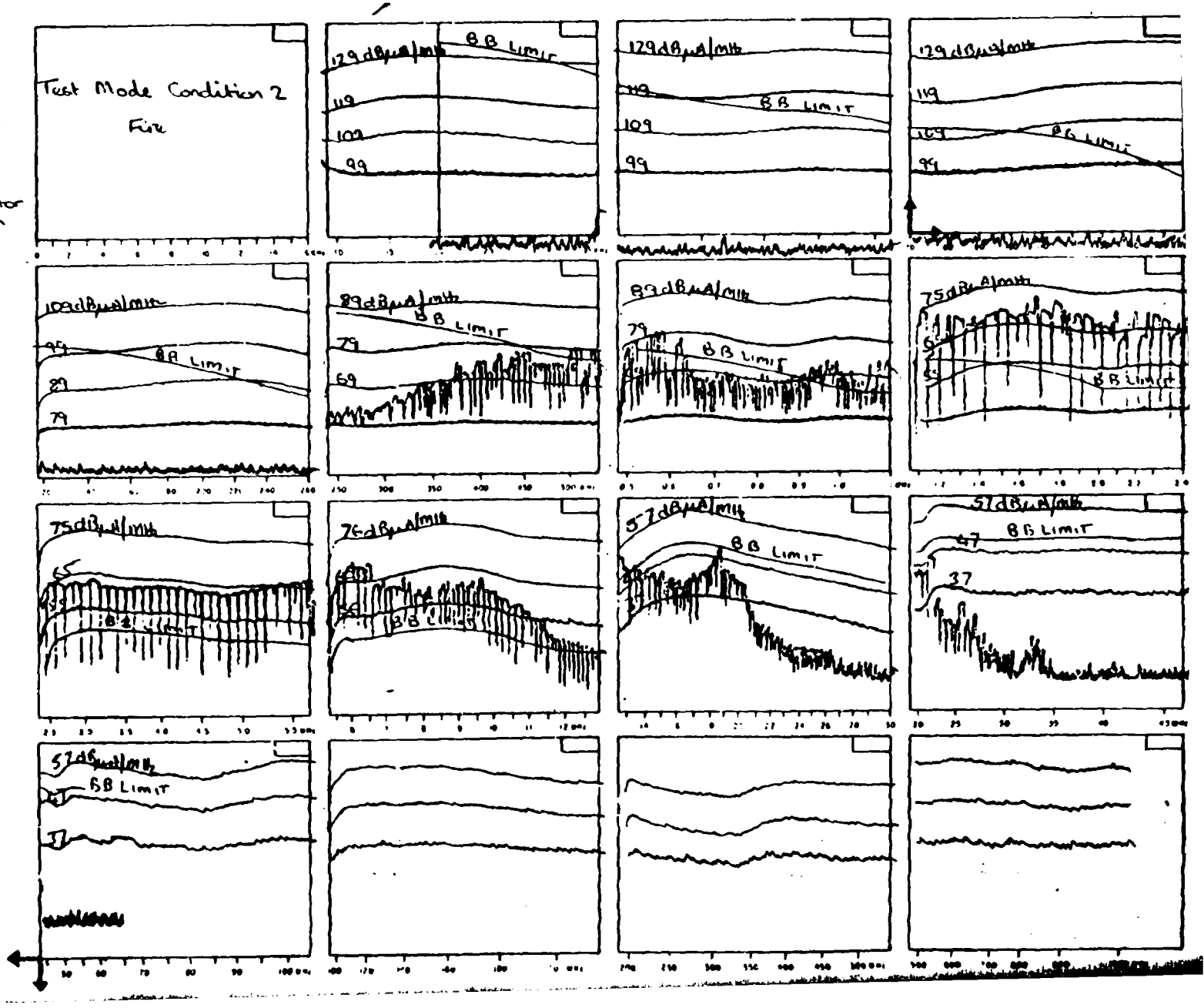
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 24

Company GRUMMAN LTD

Program Advanced Fire Detection System

Test No. CE-04 Bunch 3

Test Specimen Dual Detector long cable bunch

Date 2-4-80

Conducted By PFC

Test Spec MIL-STD-461A Notice 3.

Section CE03 - CE04

Scan Speed 2min/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

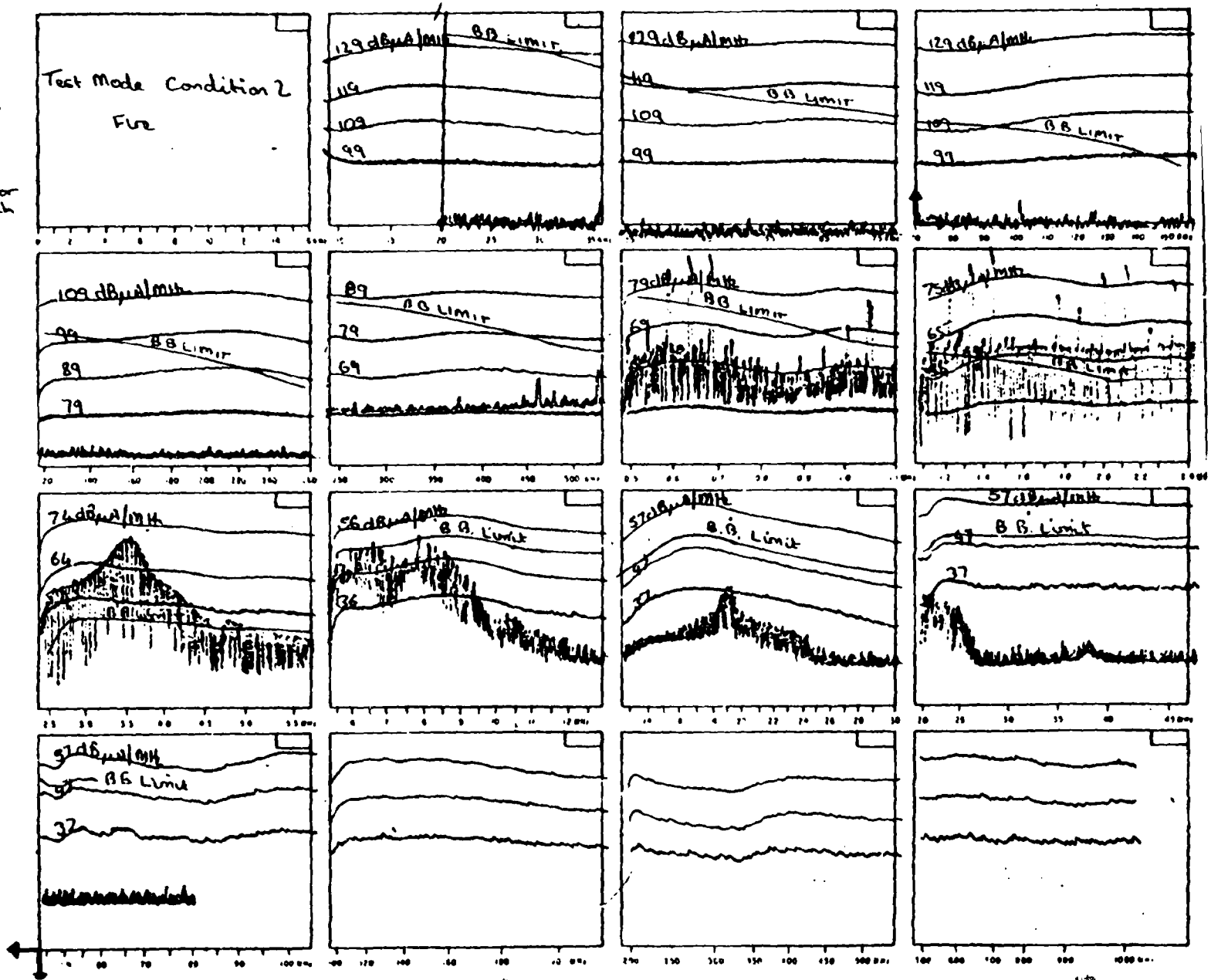
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 25

Company GRUMMAN LTD
Advanced Fire
Program Detection System

Test No. CE01
115V ac Line
Test Specimen Control A
PWB 16

Date 2-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20secs

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

400 Hz blocking filter
in measuring line.

Test Mode Condition
Standby

FSS-250, S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

385

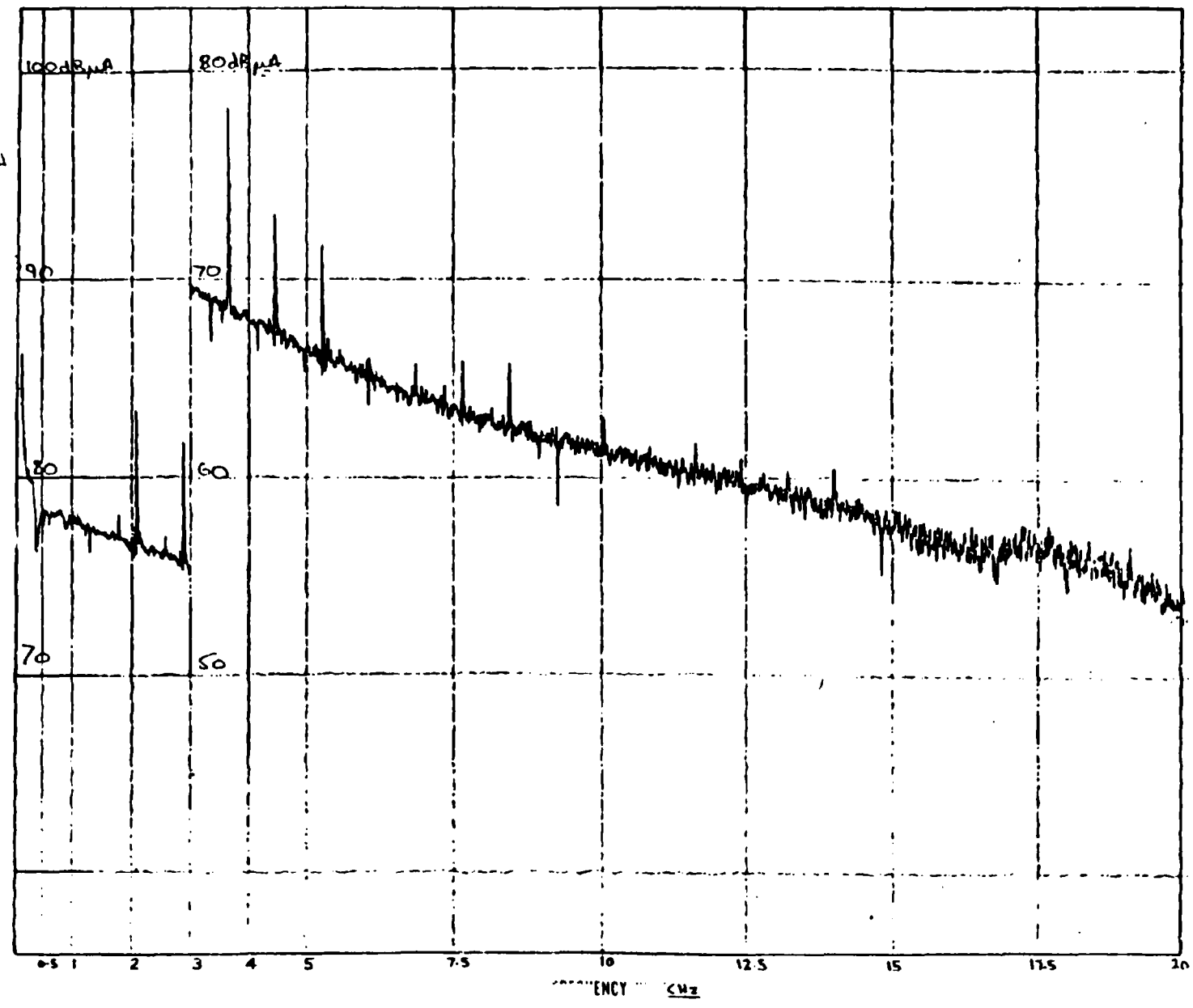
FREQUENCY IN KHz

100 dBμA
80 dBμA
90
70
60
50
70
0.5 1 2 3 4 5 7.5 10 12.5 15 17.5

PAGE 26

Company GRAINGER LTD
Advanced Fire
Program Detection System
Test No. CE 01
115V ac Neutral
Test Specimen Control A
Rev 13
Date 2-4-80
Conducted By PPC
Test Spec. MIL-STD-461A
NOTICE 3
Section —
Scan Speed 20 msec
Bandwidth 5 Hz
Detector PEAK
Atten. Pos. ____ dB
400 Hz blocking filter in measuring set
Test Mode Condition
Standby
FSS-250. S.N. ____
____ S.N. ____
____ S.N. ____
____ S.N. ____
____ S.N. ____
____ S.N. ____

ELECTRO-METRICS



PAGE 27

Company Grenville Ltd
Advanced Fire
Program Detection System

Test No. CE 01

Test Specimen 28 vdc Pos
Control A
PIN 12

Date 2-4-80

Conducted By PFC

Test Spec. MIL-STD-461B
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition
Standby

587

FSS-250. S.N. _____

_____ S.N. _____

_____ S.N. _____

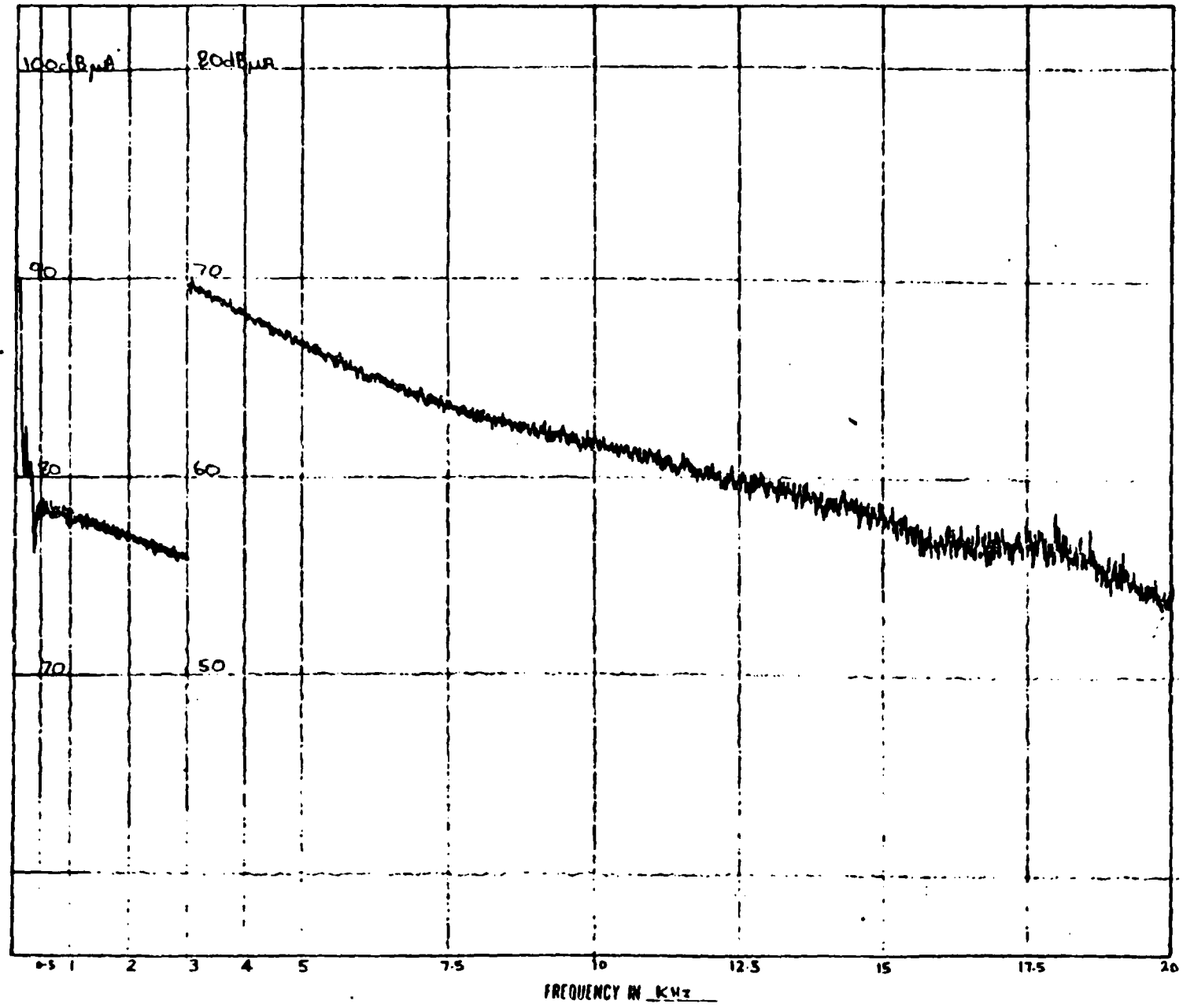
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz



FREQUENCY IN KHz

PAGE 28

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. C E 01
28V d.c. Nom.
Test Specimen Control A
Pin 29

Date 2-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz.

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition
Standby

TEST EQUIPMENT

FSS-250. S.N. _____

_____ S.N. _____

_____ S.N. _____

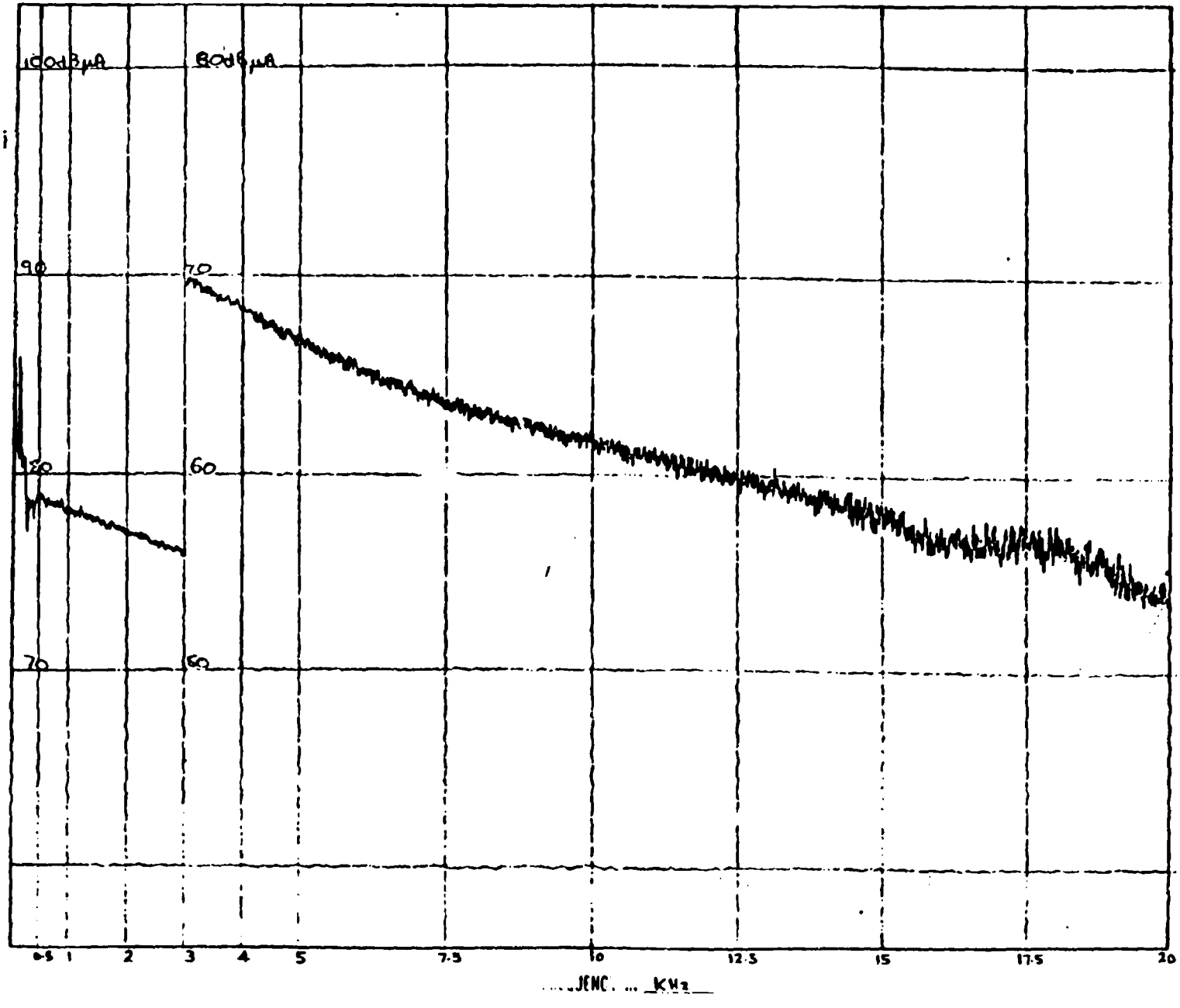
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz

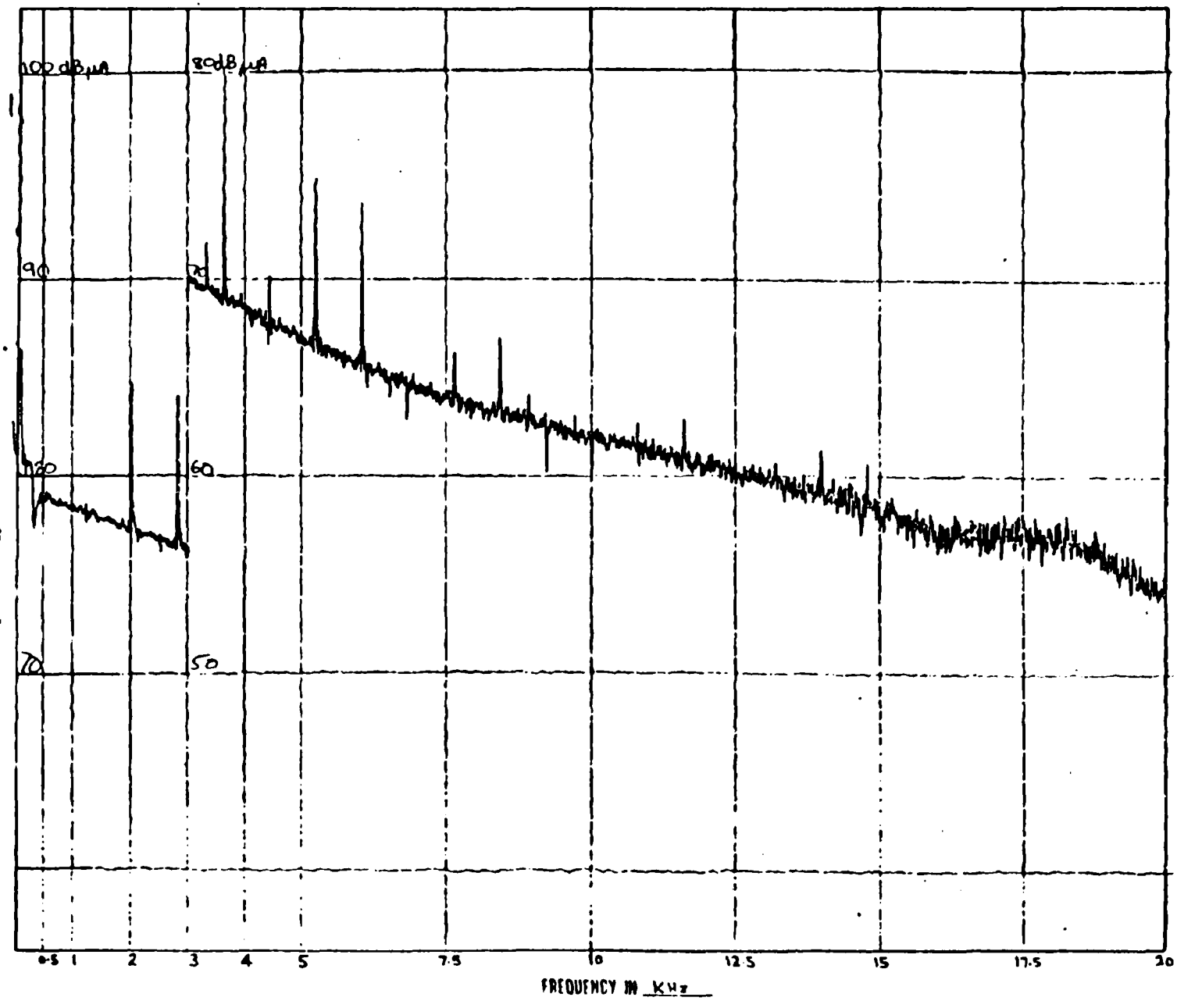


JENC. ... KHz

PAGE 29

Company GRAVINER LTD Advanced Fire
Program Detection System
Test No. CE-01
Test Specimen 115 Vac Line Control B PWB
Date 2-4-80
Conducted By PPC
Test Spec.
Section —
Scan Speed 20 mins
Bandwidth 5 Hz
Detector PEAK
Atten. Pos.
400 Hz blocking Filter in measuring Lead
Test Mode Condition 1 Standby
FSS-250. S.N.
S.N.
S.N.
S.N.
S.N.
S.N.

ELECTRO-METRICS



PAGE 30

Company GRUMMAN LTD

Program Advanced Fire Detection System

Test No. CE01
115V ac Neutral

Test Specimen Control B
P/N 13

Date 2-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 msec

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

400 Hz blocking Filter
in measuring lead

Test Mode Condition I
Standby

FSS-250. S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz

100 dBμA 80 dBμA

90 70

80 60

70 50

0.5 1 2 3 4 5 7.5 10 12.5 15 17.5 20

JENC KHz

PAGE 31

Company GRAVINER LTD

Program Advanced Fire Detection System

Test No. CE01

Test Specimen 22V dc Pos Control B PIN 12

Date 2-11-80

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition Standby

TEST EQUIPMENT

FSS-25U. S.N. _____

_____ S.N. _____

_____ S.N. _____

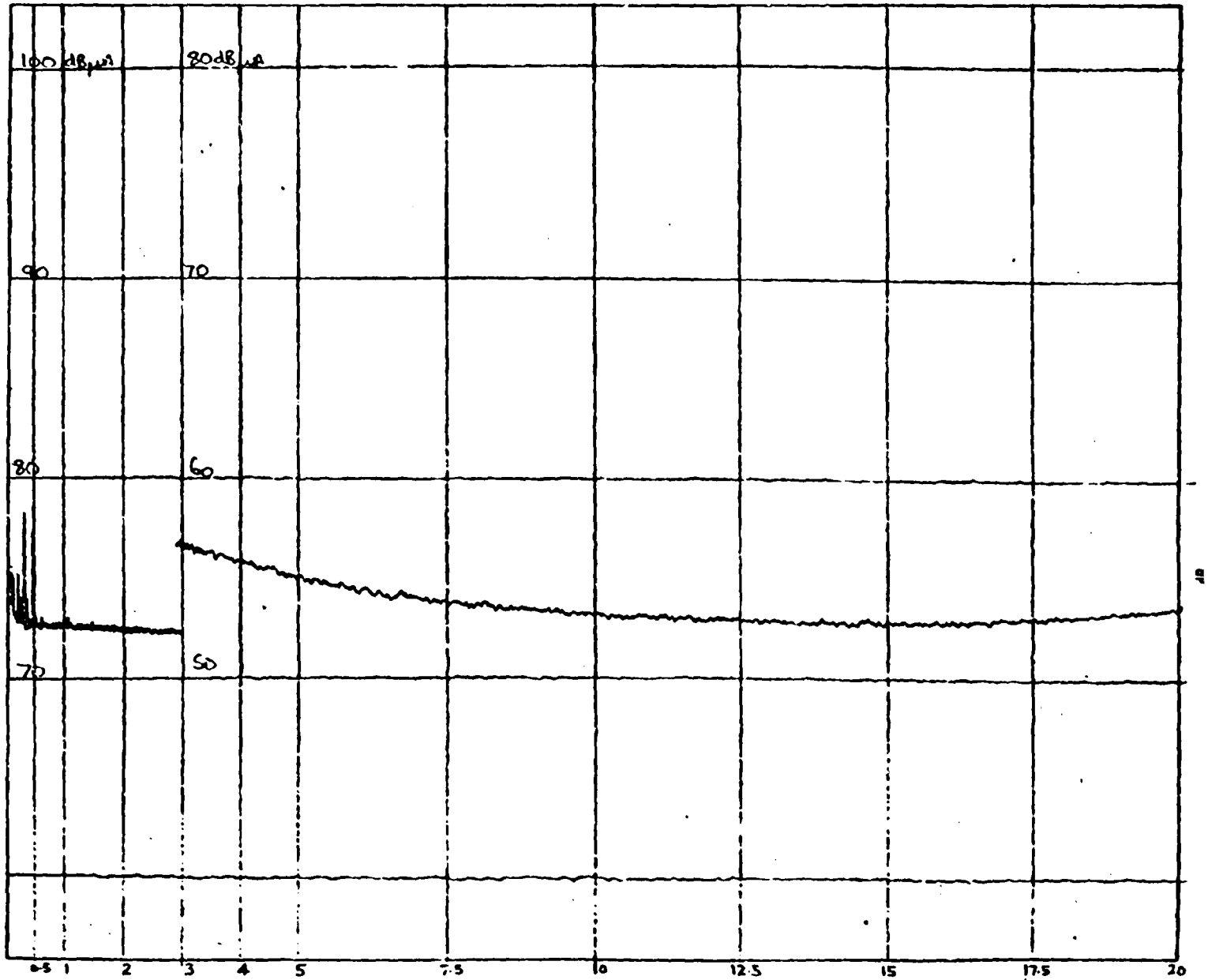
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz



FREQUENCY IN KHz

PAGE 32

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE 01
22V dc Neg.
Test Specimen Control BJ
RN 29

Date 2-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mm/s

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____

Test Mode Condition
Standby

TEST EQUIPMENT

FSS-250. S.N. _____

_____ S.N. _____

_____ S.N. _____

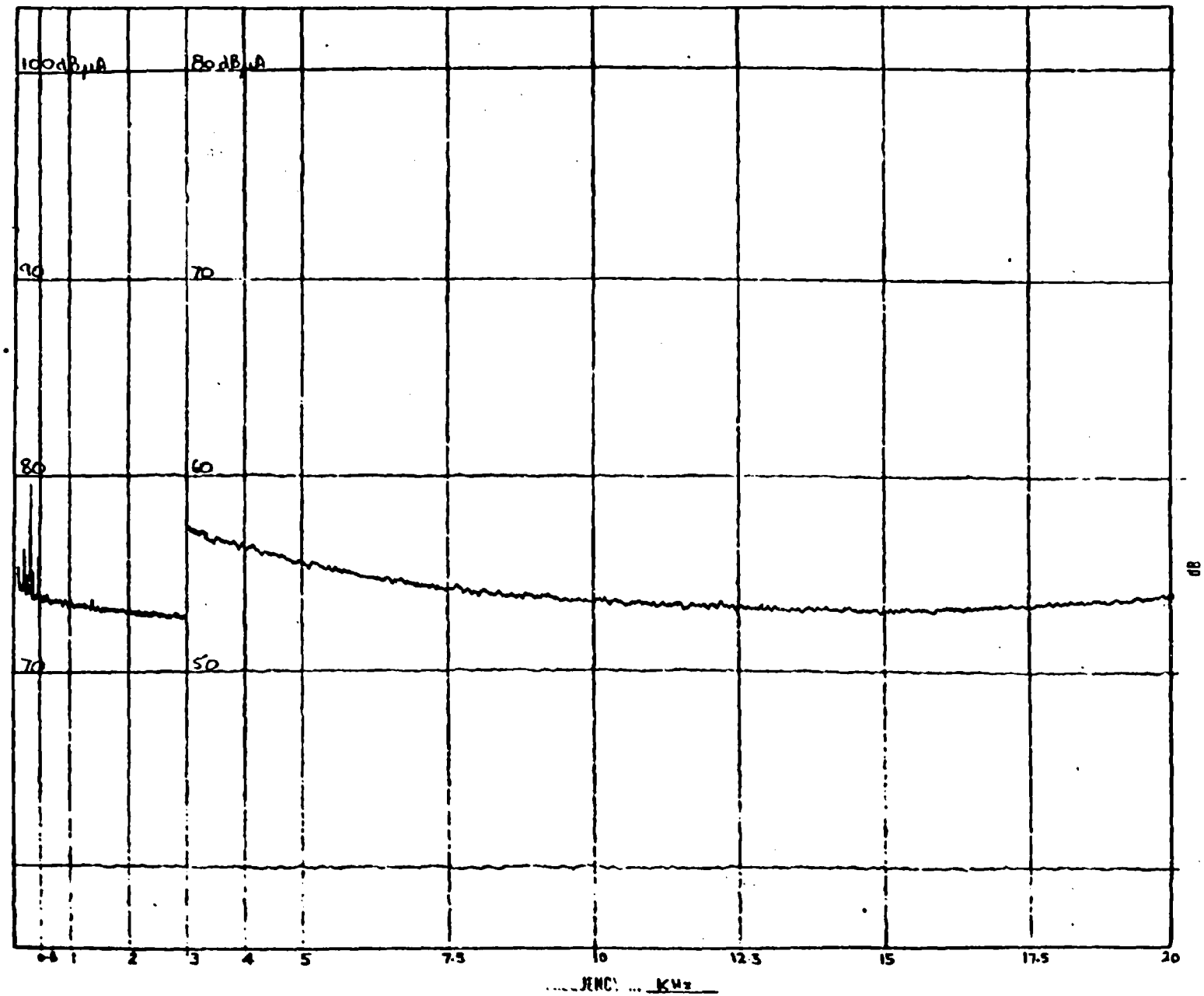
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz



PAGE 33

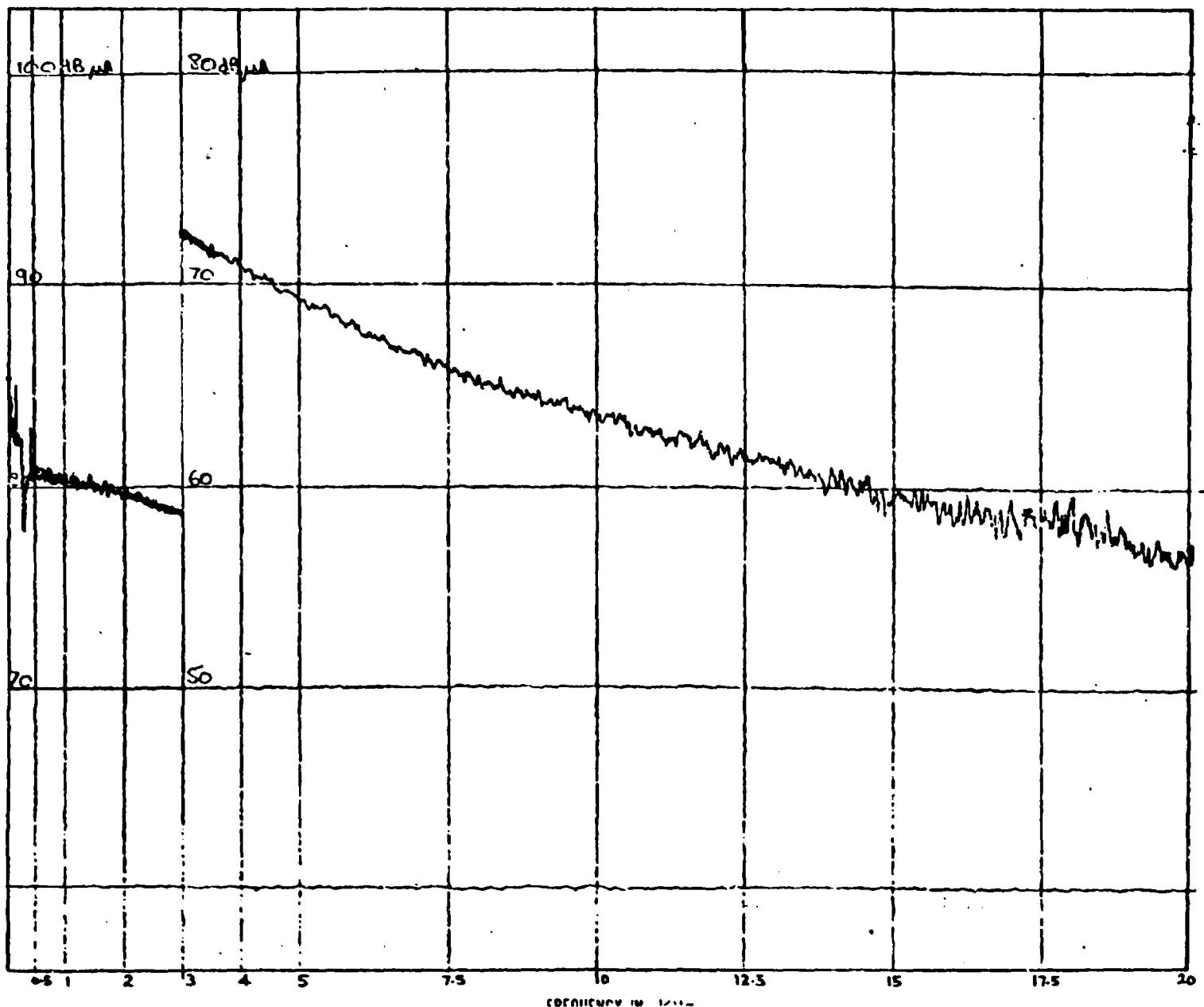
Company Canadian LTD
Program Advanced Fire Detection System
Test No. CE 01
Test Specimen 28 V dc Pos S W J P1 N 6
Date 8-4-80
Conducted By PPC
Test Spec. MIL-STD-461A NOTICE 3
Section —
Scan Speed 20 mins
Bandwidth 5 Hz
Detector PEAK
Atten. Pos.
Test Mode Condition 1 Standby

TEST EQUIPMENT

FSS-250, S.N.
S.N.
S.N.
S.N.
S.N.
S.N.

ELECTRO-METRICS

FREQUENCY IN KHz



PAGE 34

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE-01
115V ac Line

Test Specimen CONTROL
PIN 14

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos.

400 Hz blocking Filter
in measuring lead

Test Mode Condition 2
Fire

FSS-250. S.N.

S.N.

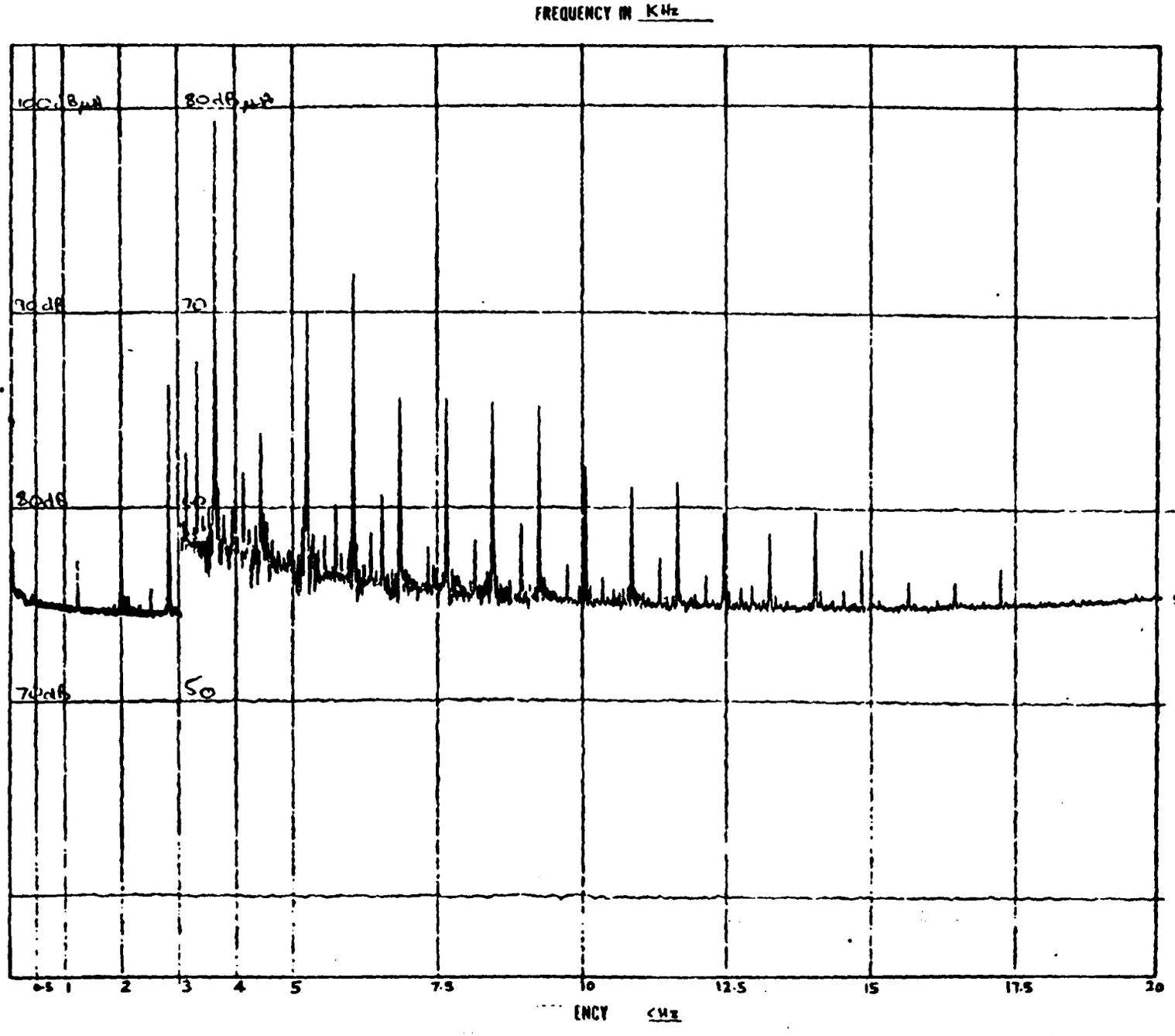
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 35

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE-01

Test Specimen 115V ac Neutral
Control A
PIN 13

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. —

40 m Hz blocking Filter
in measuring lead

Test Mode Condition 2
Fire

FSS-250. S.N. —

— S.N. —

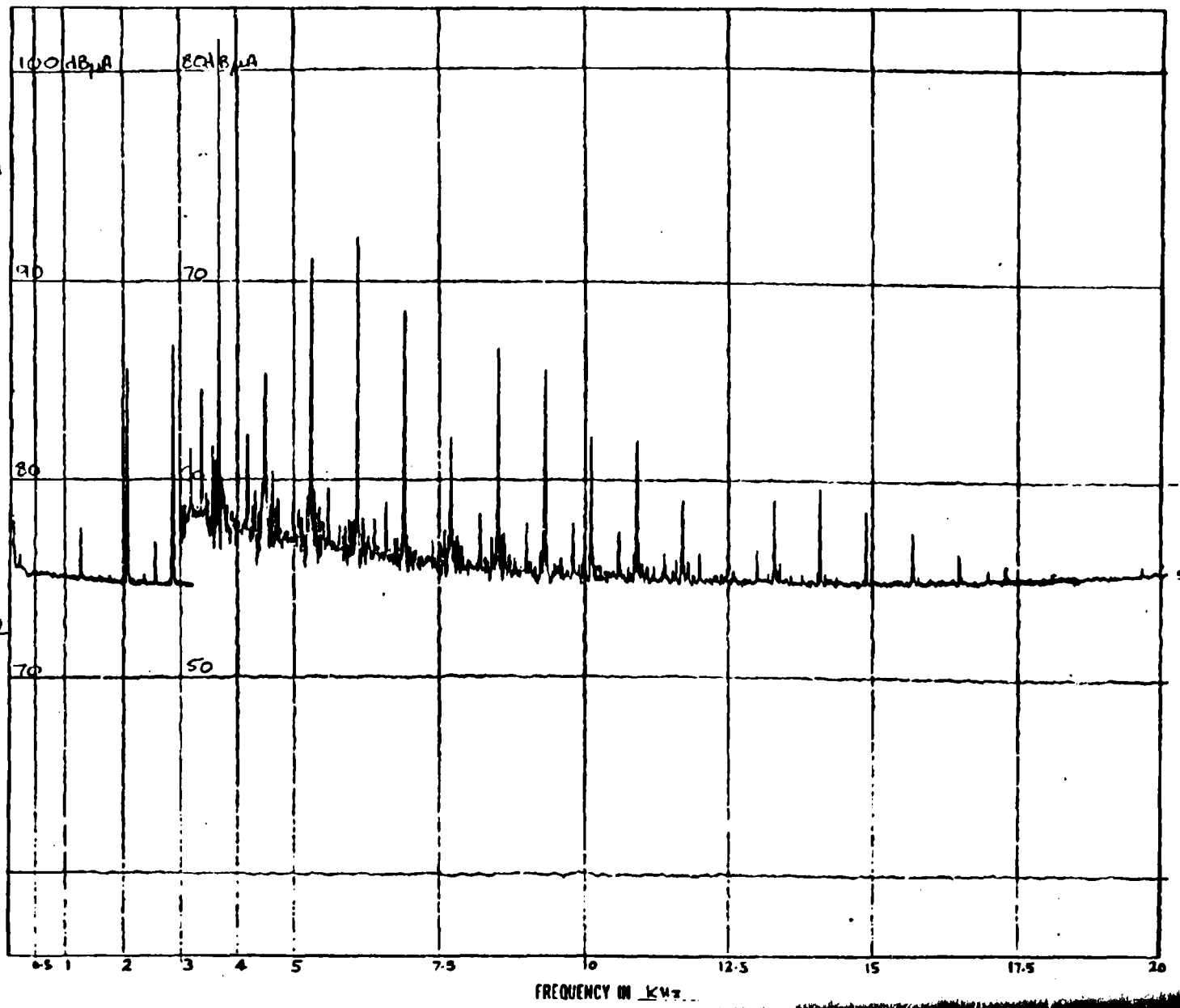
— S.N. —

— S.N. —

— S.N. —

— S.N. —

ELECTRO-METRICS



PAGE 36

Company GRAINER LTD Advanced Fire
Program Detection system

Test No. CE 01
23V dc Pos
Test Specimen Control A PN 12

Date 8-4-80

Conducted By PFC

Test Spec. MIL-STD-461A NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos.

Test Mode Condition 2 Fire

TEST EQUIPMENT

FSS-250, S.N.

S.N.

S.N.

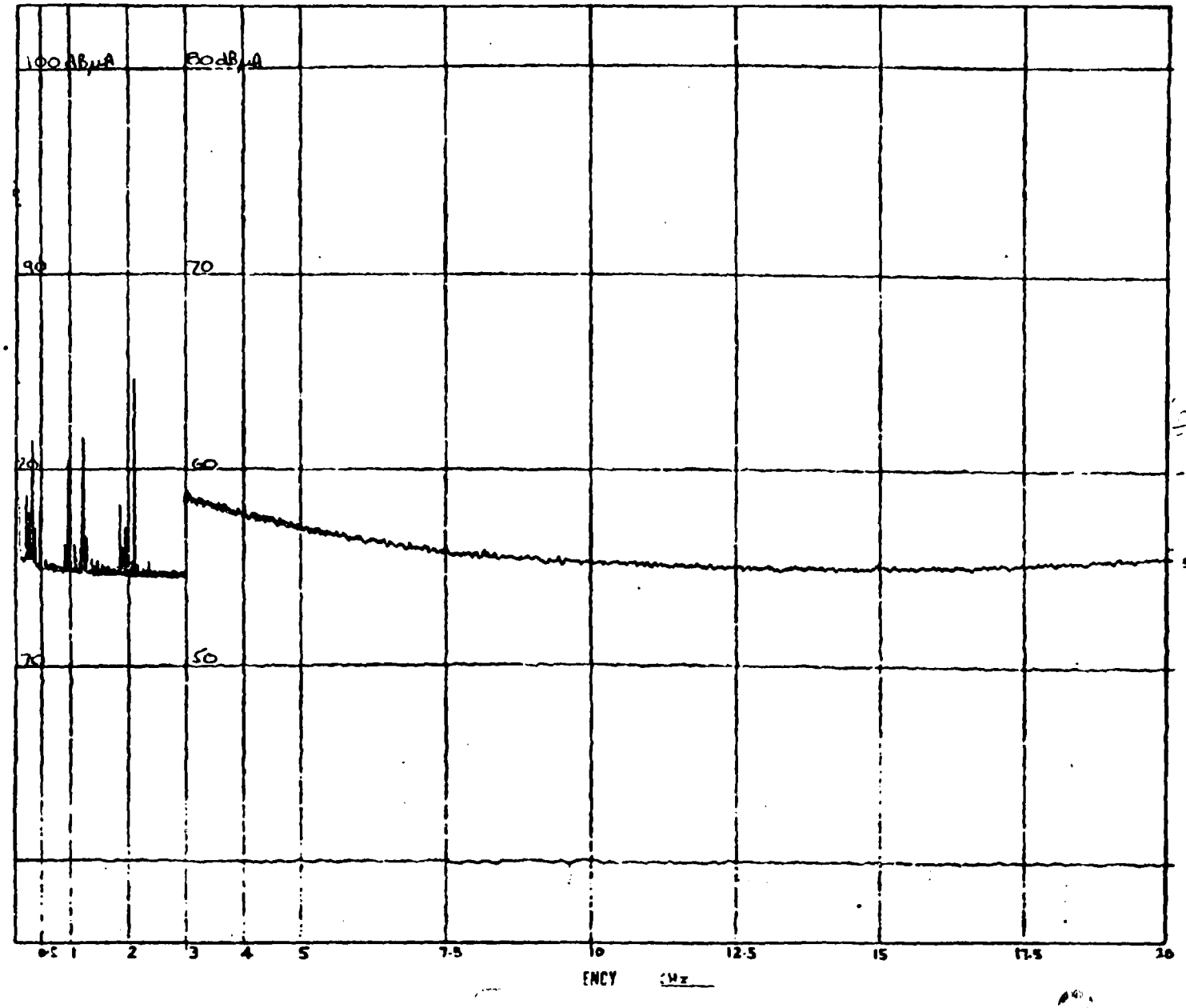
S.N.

S.N.

S.N.

ELECTRO-METRICS

FREQUENCY IN KHz



PAGE 37

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE01
28 V dc Neg

Test Specimen Control A.
PIN 29

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461B
NOTICE 3

Section —

Scan Speed 2 am/s

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition 2
Fire

TEST EQUIPMENT

FSS-250, S.N. _____

_____ S.N. _____

_____ S.N. _____

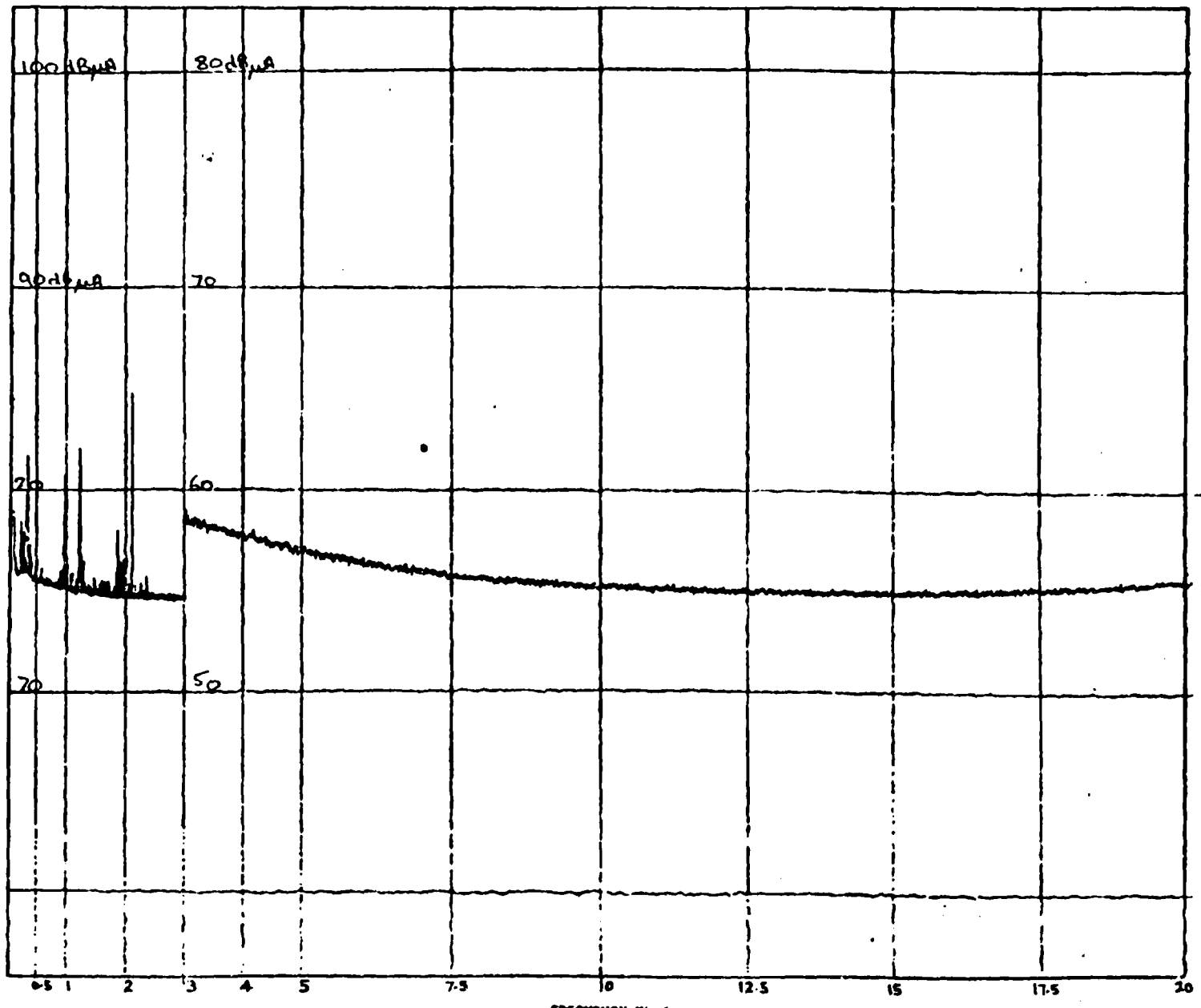
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS

FREQUENCY IN KHz



FREQUENCY IN KHz

PAGE 38

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. CE 01

Test Specimen 115V ac Line
Control B
Pin 14

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mm/s

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition 2
Fire
400 Hz blocking filter
in measuring lead

FSS-250. S.N. _____

398 S.N. _____

_____ S.N. _____

_____ S.N. _____

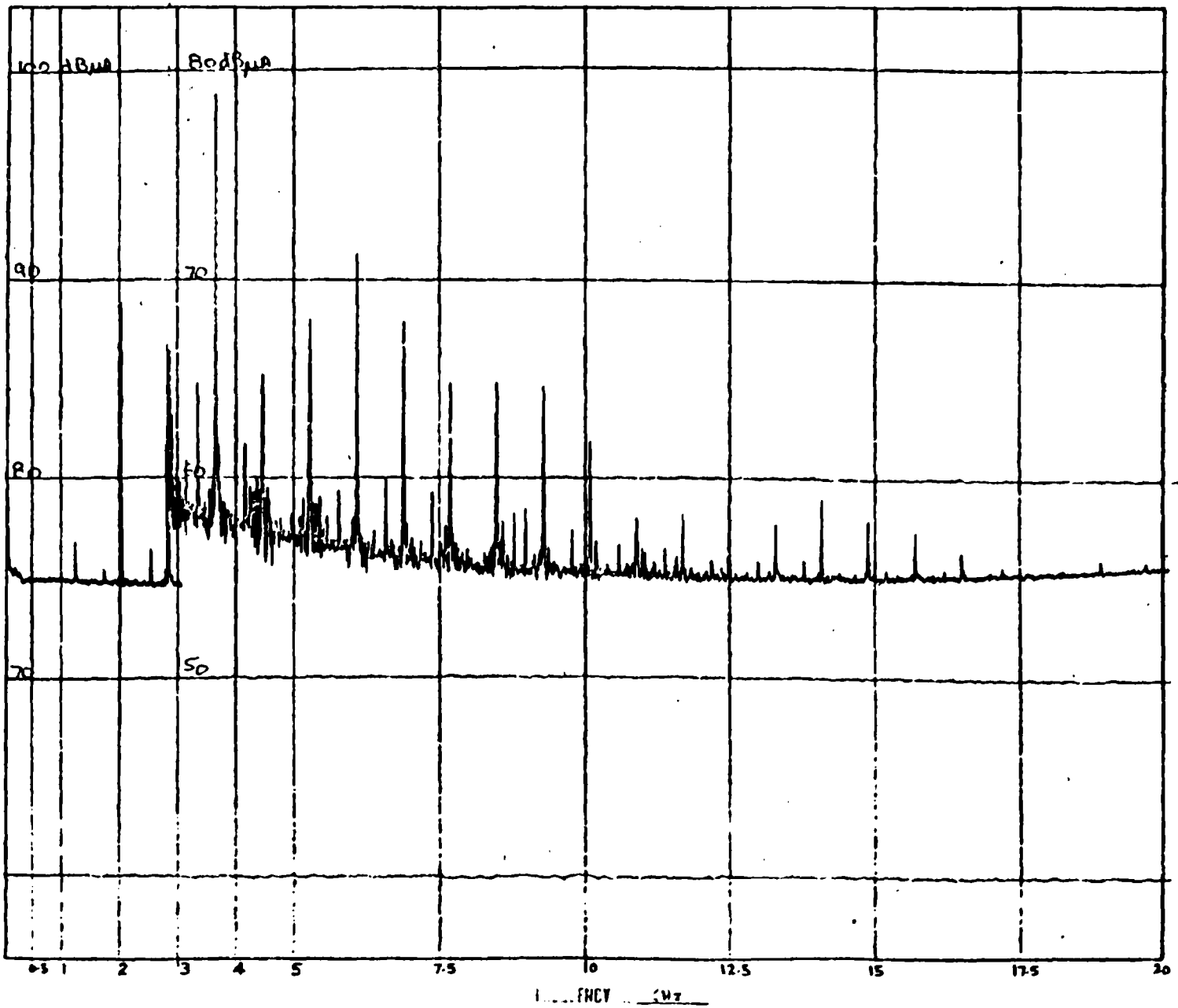
_____ S.N. _____

_____ S.N. _____

_____ S.N _____

ELECTRO-METRICS

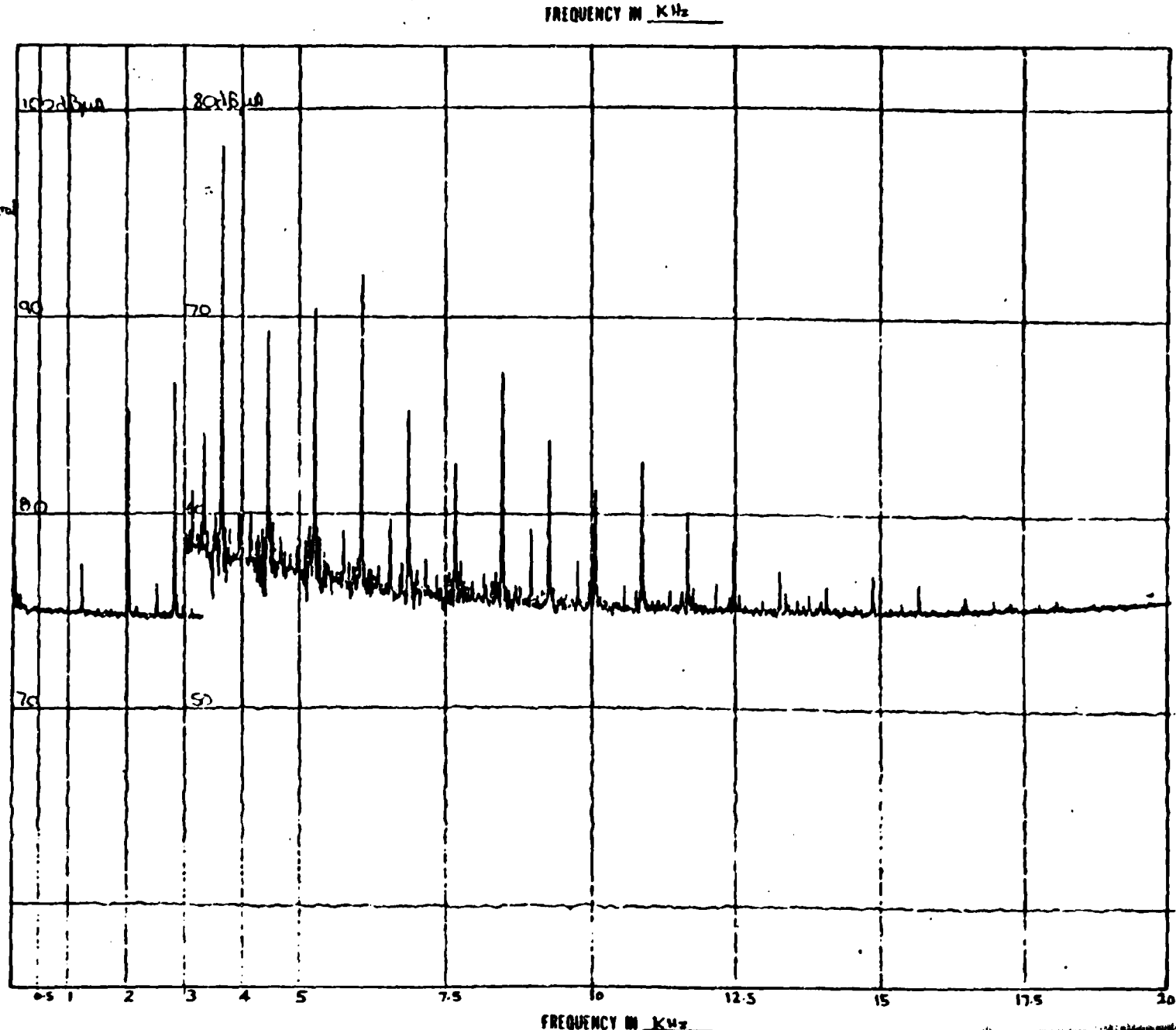
FREQUENCY IN KHz



PAGE 39

Company GRUMMAN A/C
Program Advanced Fire Detection System
Test No CE 01
Test Specimen 115 V ac Neutral Control B PIN 13
Date 8-6-80
Conducted By PPC
Test Spec. MIL-STD-461B NOTICE 5
Section —
Scan Speed 20 mins
Bandwidth 5 Hz
Detector PEAK
Atten. Pos. 60 dB
With 400 Hz blocking filter in measuring lead
Test Mode Condition: Fire
FSS-250. S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____

ELECTRO-METRICS



PAGE 40

Company GRAVINER LTD Advanced Fire
Program Detection System

Test No. CE 01

Test Specimen 22 v dc Pos Control B Pin 12

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 3

Section —

Scan Speed 2 min

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. ____ dB

Test Mode Condition 2 Fire

400

TEST EQUIPMENT

FSS-250. S.N. ____

____ S.N. ____

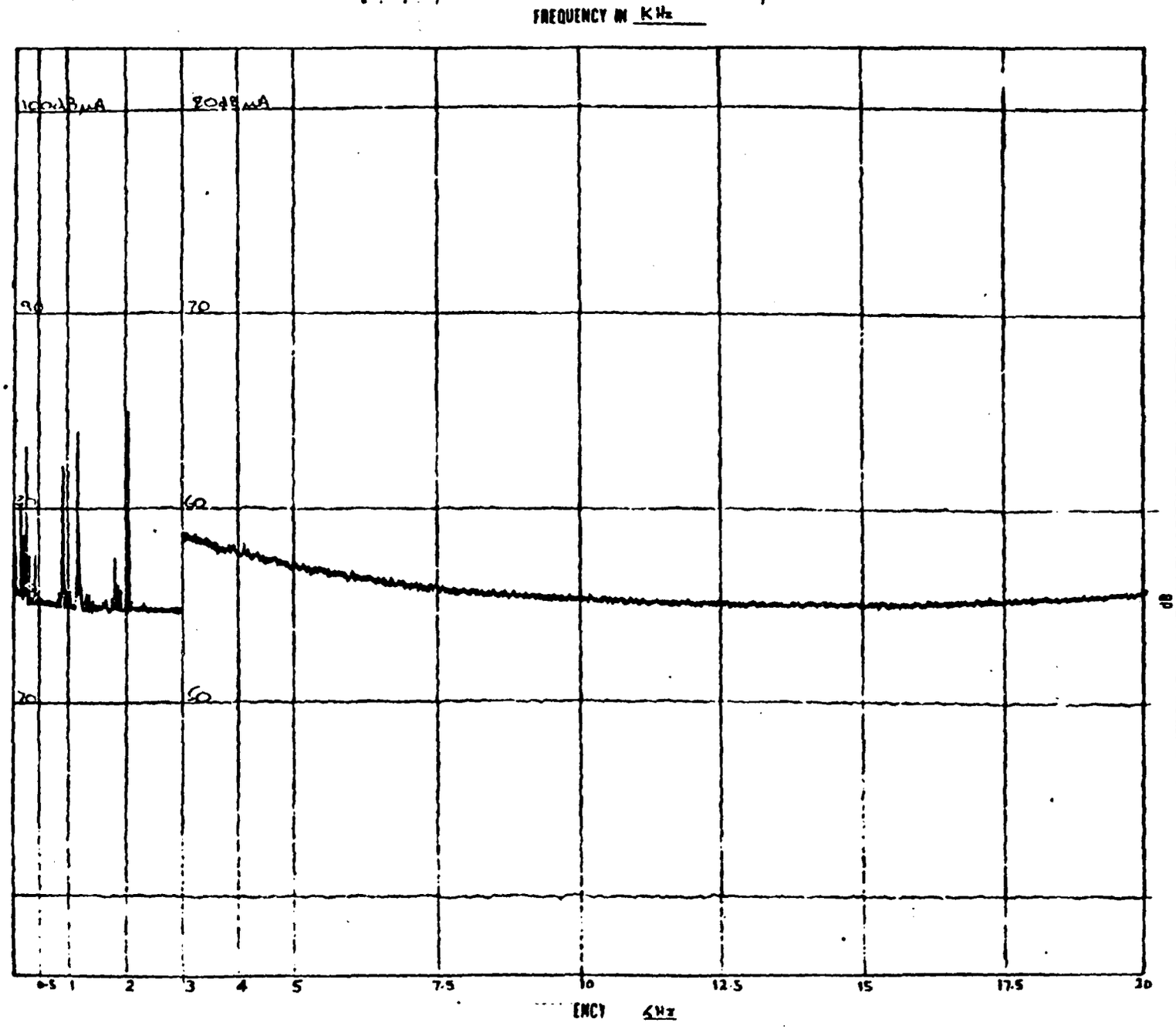
____ S.N. ____

____ S.N. ____

____ S.N. ____

____ S.N. ____

ELECTRO-METRICS



PAGE 41

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No CE 01
28V dc Neg
Test Specimen Control B
AN29

Date 8-4-80

Conducted By PPC

Test Spec MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten Pos

Test Mode Condition 2

401 Fire TEST EQUIPMENT

FSS-250. S N.

S N

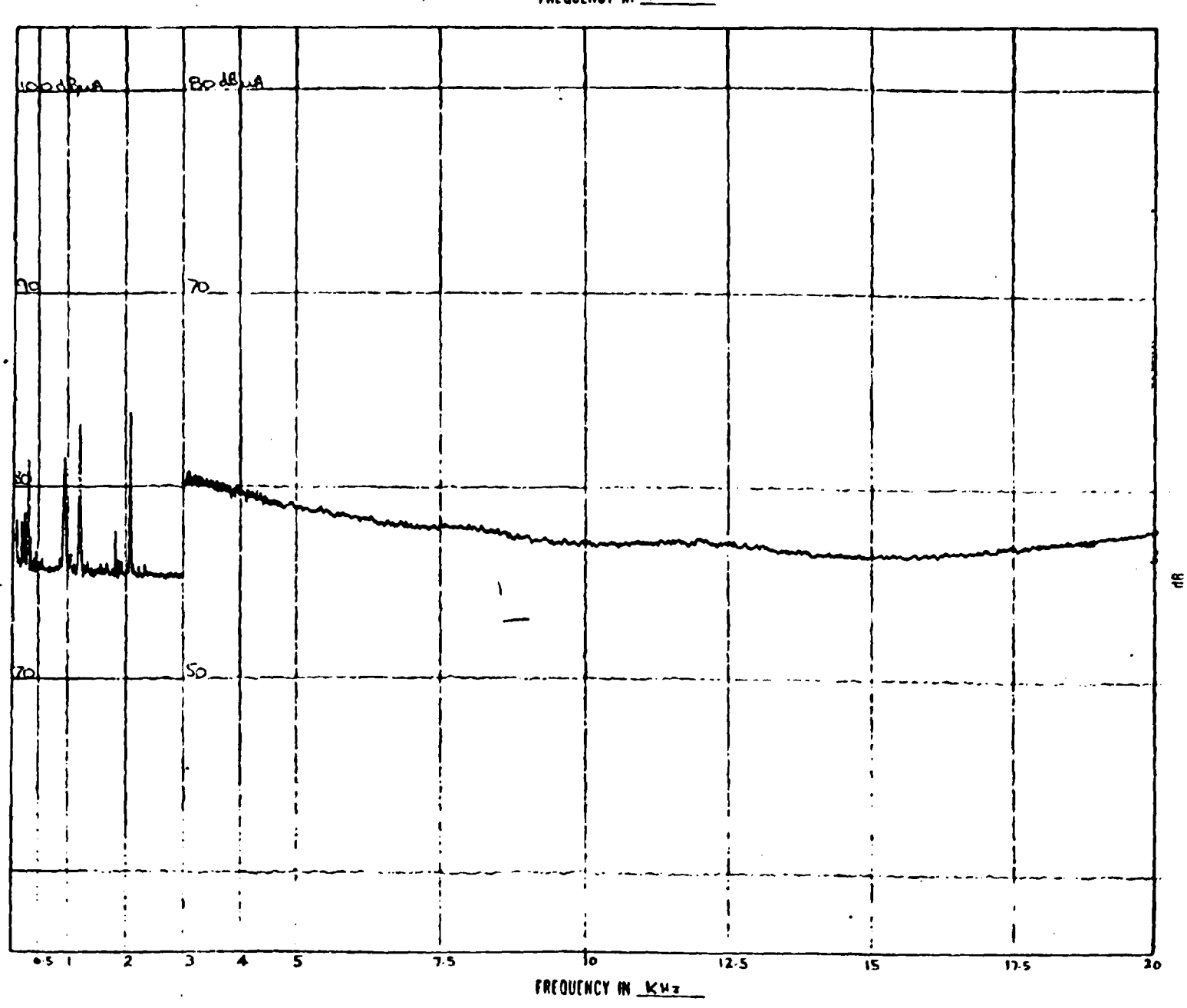
S N

S N

S N

S N

ELECTRO-METRICS



PAGE 42

Company GRENNER LTD
Advanced Fire
Program Detection System

Test No. CE 01
28V dc Pos

Test Specimen Conv
Pin 6

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 dB/s

Bandwidth 5 Hz

Detector PEAK

Atten. Pos.

Test Mode Condition 2
Fire

402 TEST EQUIPMENT

FSS-250. S.N.

S.N.

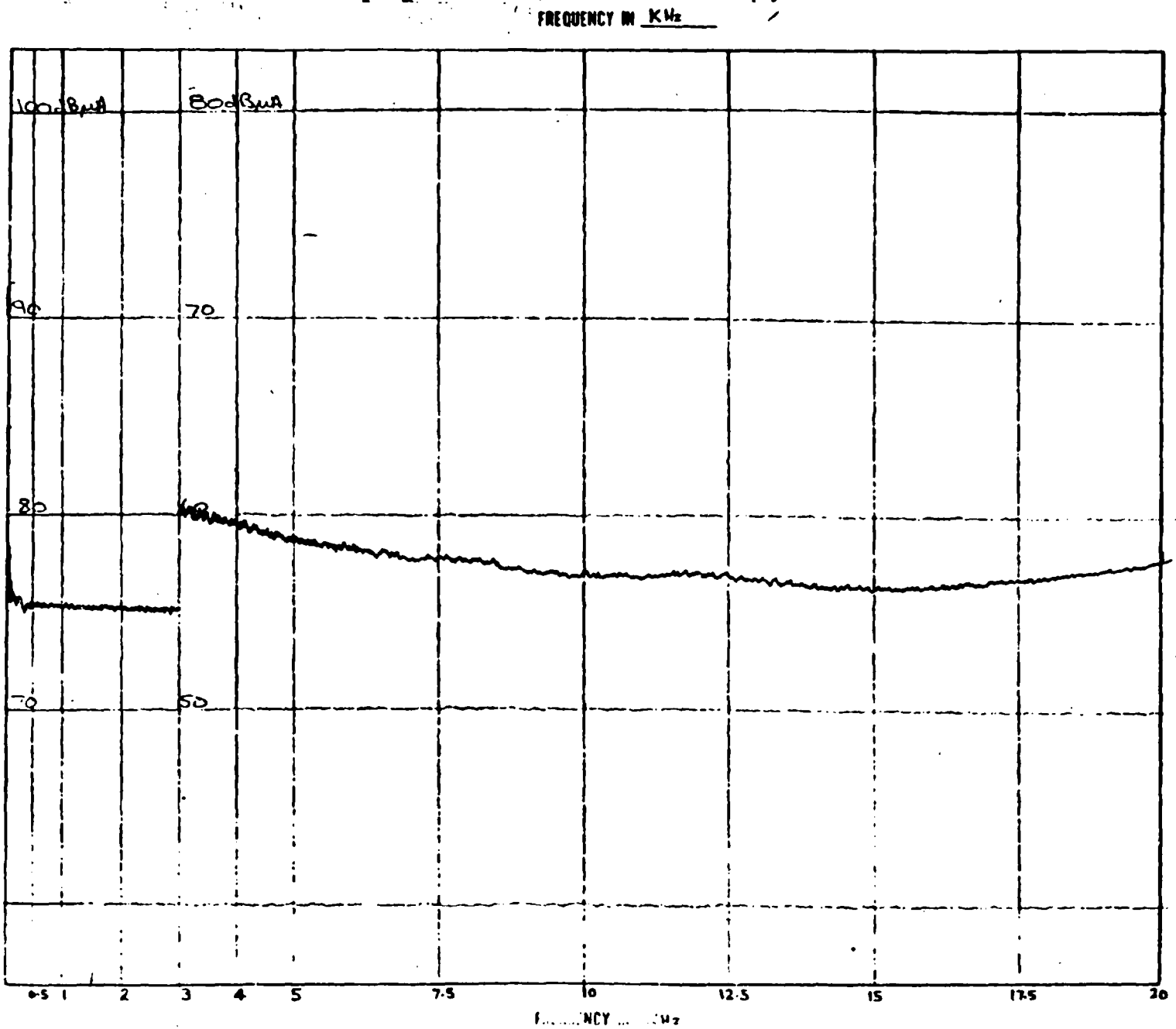
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 43

Company GRUMMAN LTD Advanced Fire

Program Detection System

Test No. CE02 Bunch 1

Test Specimen All locals, Detector Control Unit and CRU ex. Simplex

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461B Notice 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____

Test Mode Conduction Standby

403

TEST EQUIPMENT

FSS-250. S.N. _____

_____ S.N. _____

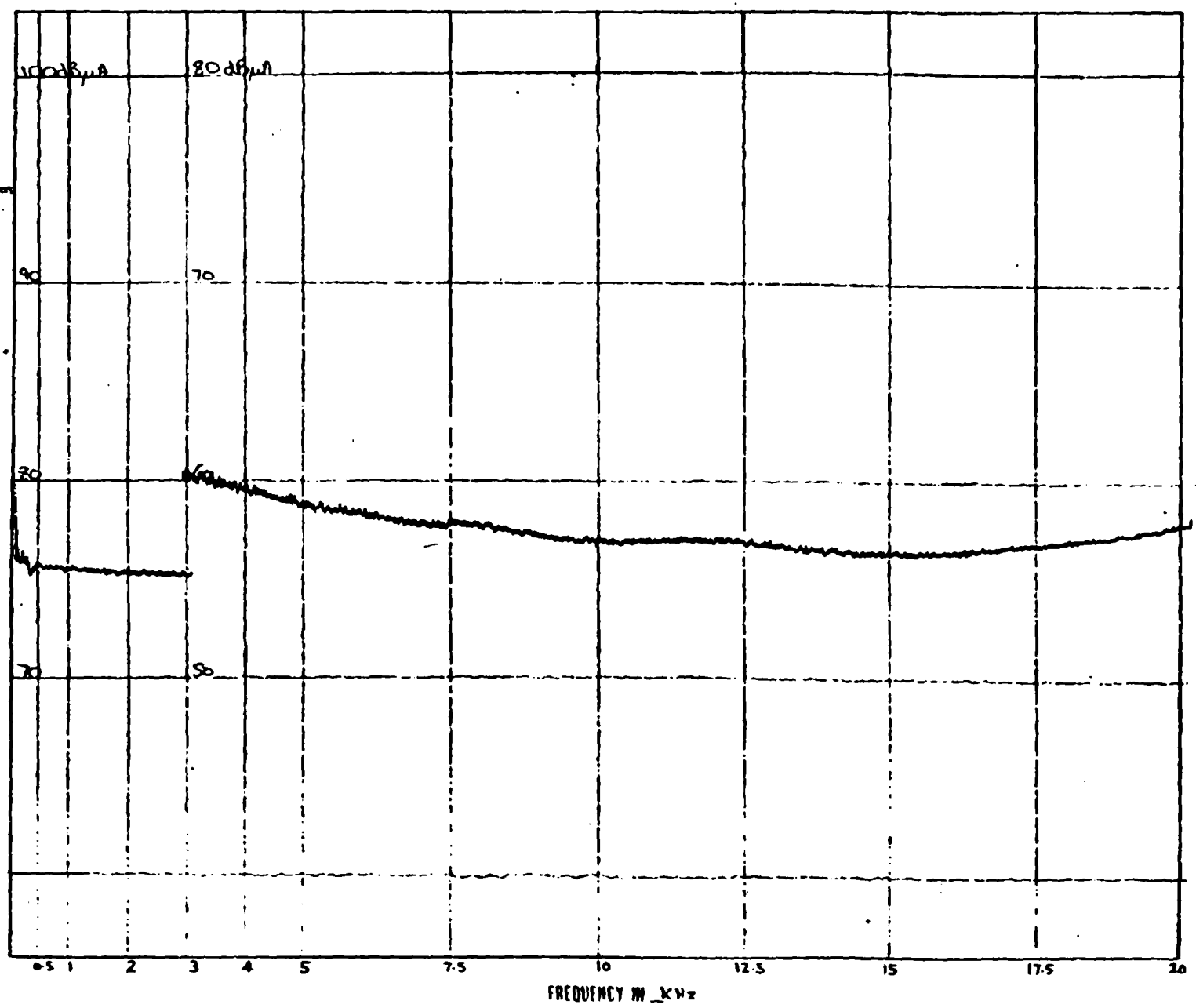
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS



PAGE 44

Company Grumman LTD
Advanced Fire
Program Detection System

Test No. CE 02
Bunch 2

Test Specimen Single Detector
long cable bunch

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos

Test Mode Condition 1
4 Standby
0 TEST EQUIPMENT
4

FSS-250. S.N.

S.N.

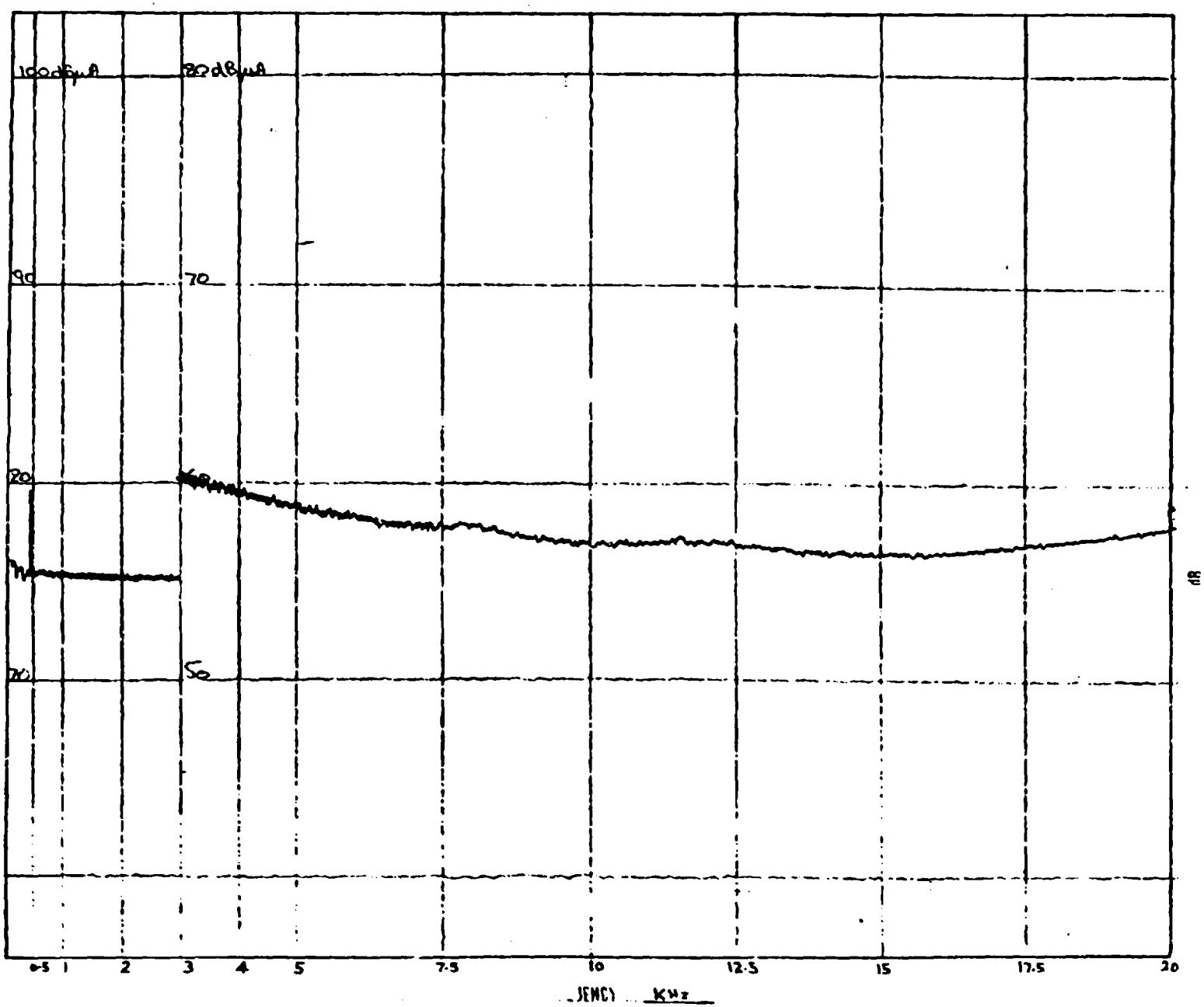
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 45

Company GRUMMAN Aerospace Advanced Fire

Program Detection System

Test No CE 02 Bunch 3

Test Specimen Dual Detector long cable bunch

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A Notice 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____

Test Mode Condition 1 Standby

TEST EQUIPMENT

FSS-250, S.N. _____

_____ S.N. _____

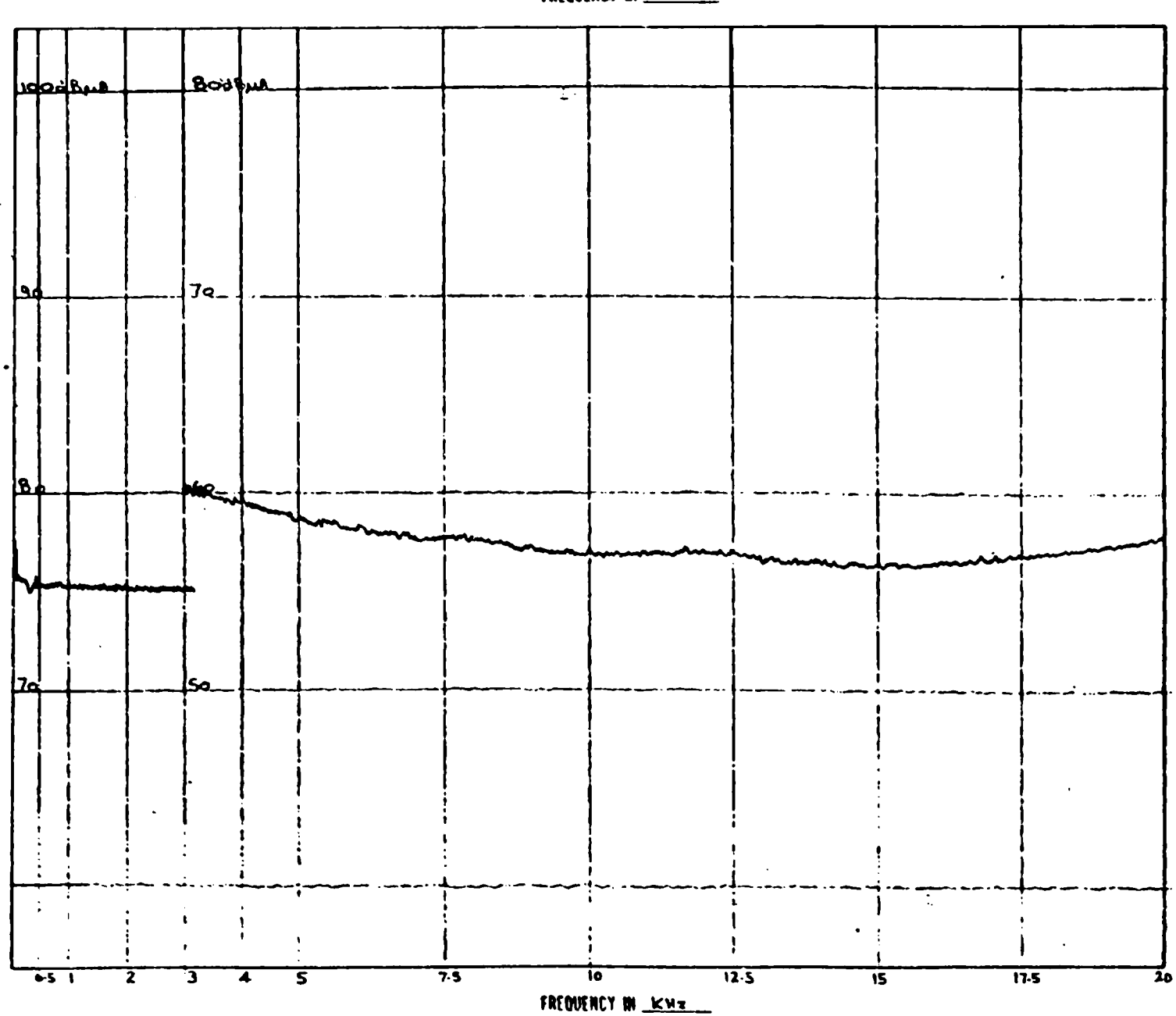
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS



PAGE 46

Company GRUMMAN LTD

Program Advanced Fire Detection System

Test No CE 02

Test Specimen Bunch 1 Loads, Detector Control Units and C.W.U. excluding P. Supplies

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A NOTICE 3

Section —

Scan Speed 20 mm

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____ dB

Test Mode Condition 2 Fire.

406

TEST EQUIPMENT

FSS-250. S.N. _____

_____ S.N. _____

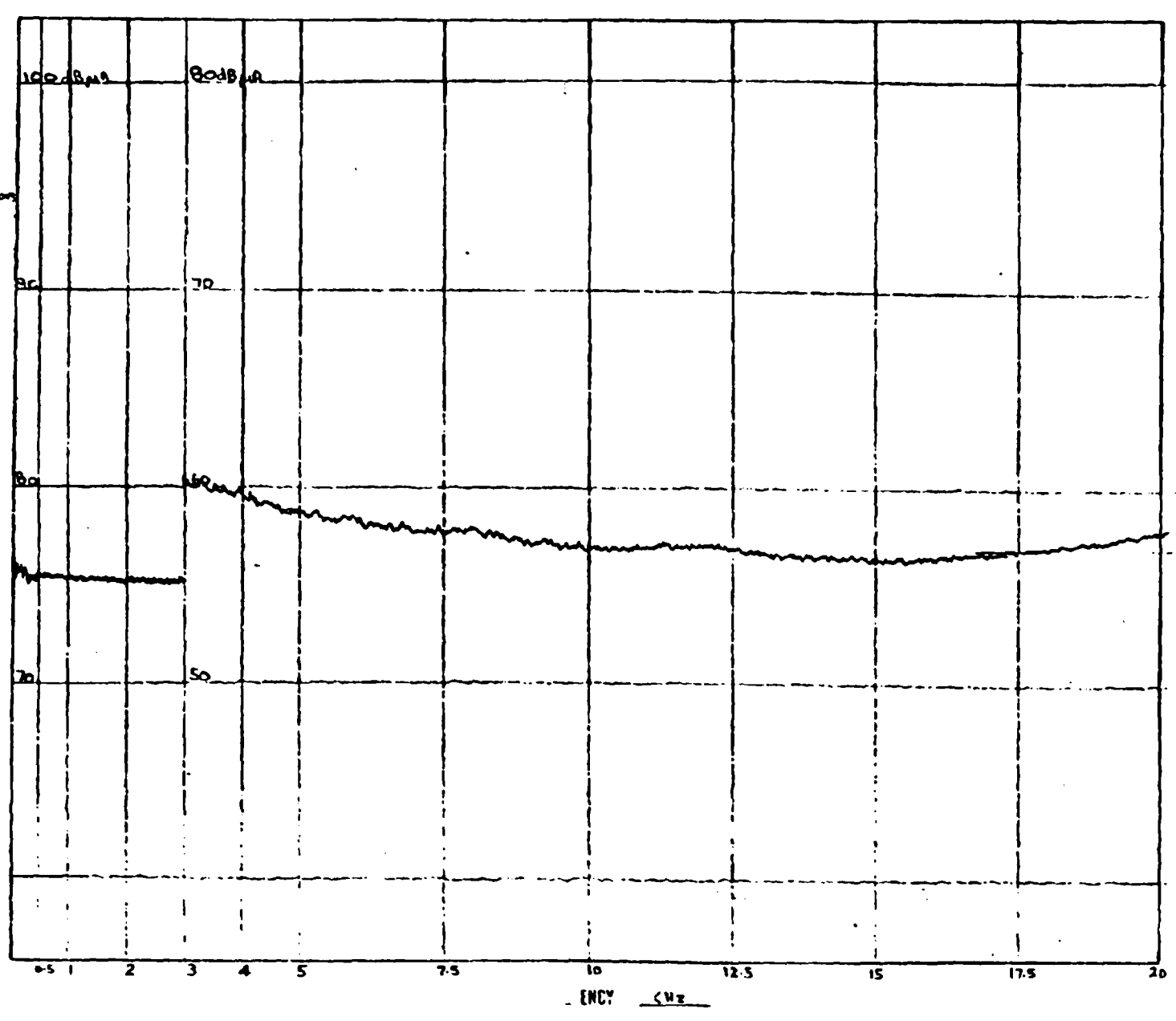
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS



PAGE 47

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No CE.02
Bunch 2
Test Specimen SINC DETECTOR
long cable bunch

Date 8-4-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

Detector PEAK

Atten. Pos. _____

Test Mode Condition 2
Fire

TEST EQUIPMENT

FSS-25U. S.N. _____

_____ S.N. _____

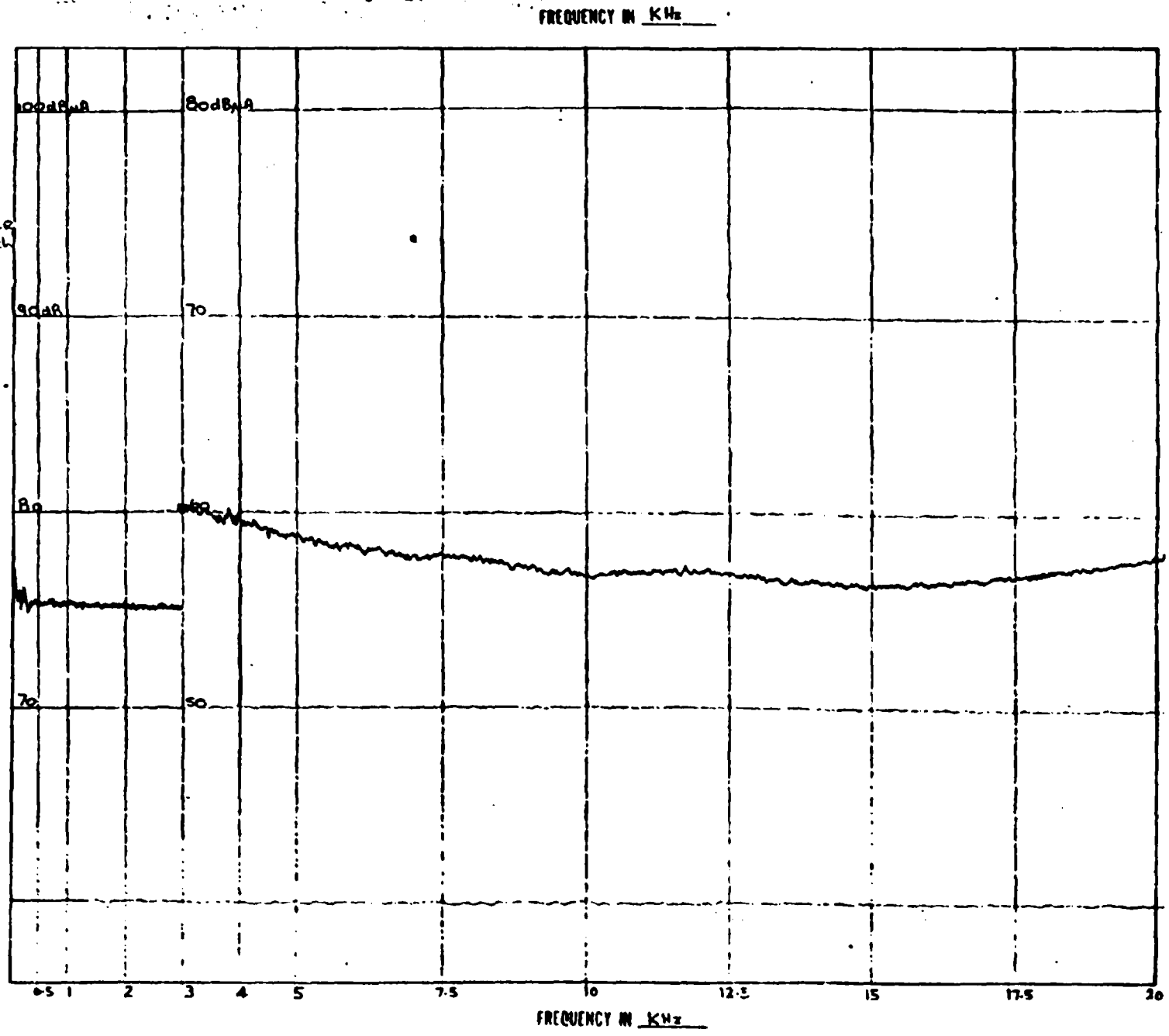
_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

_____ S.N. _____

ELECTRO-METRICS



PAGE 48

Company GRAVNER LTD
Advanced Fire
Program Detection System

Test No. CE.02
Bunch 3
Test Specimen Dual Detector
long cable bunch
Date 8-4-80

Conducted By P P C

Test Spec. MIL-STD-461A
NOTICE 3

Section —

Scan Speed 20 mins

Bandwidth 5 Hz

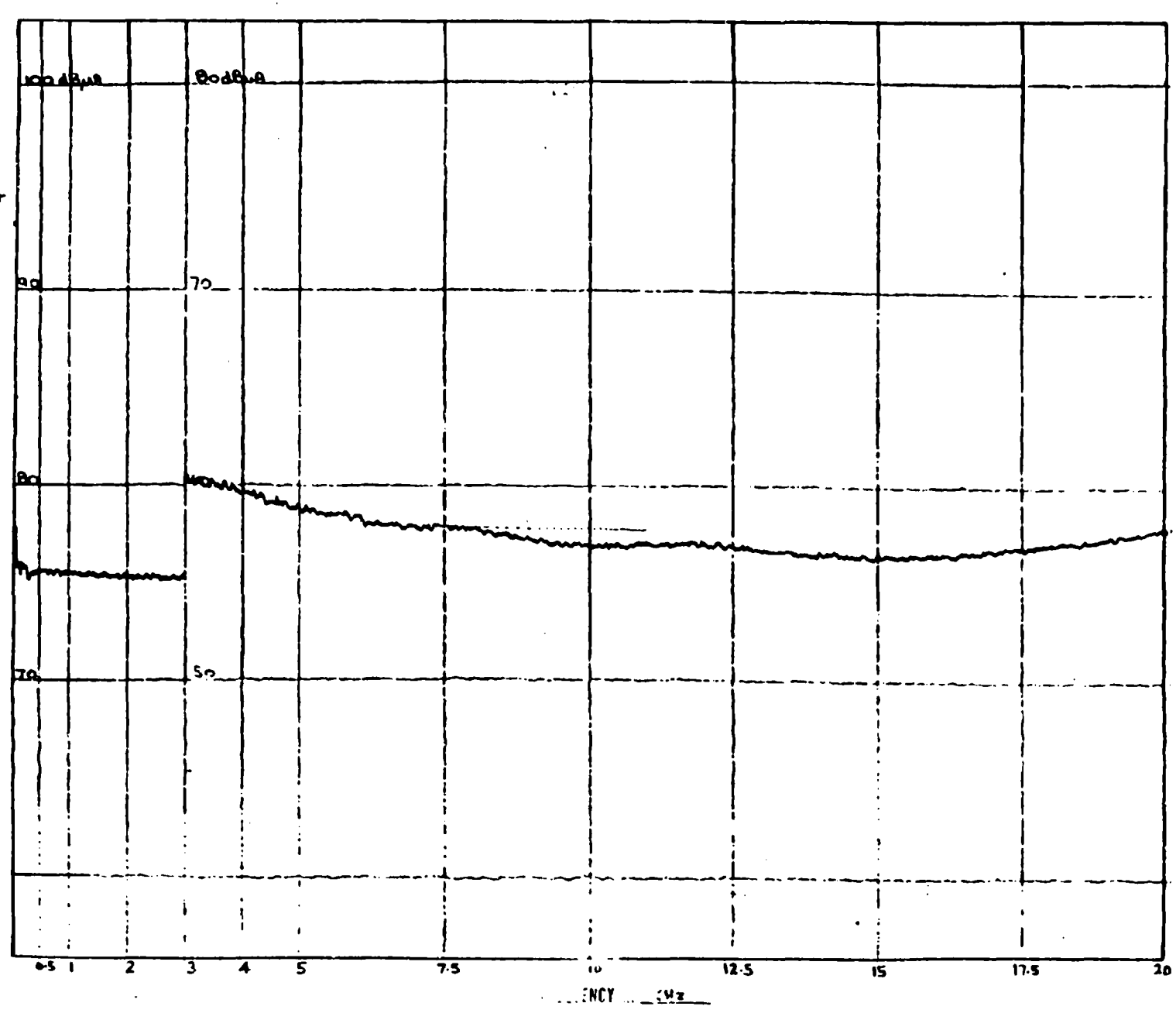
Detector PEAK

Atten. Pos. _____

Test Mode Condition 2
△ Fire
○ TEST EQUIPMENT
∞

FSS-250. S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____
_____ S.N. _____

ELECTRO-METRICS



PAGE 49

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. —

Test Specimen —

Date 7-5-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1,2 & 3

Section RE 02

Scan Speed 4 mins/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

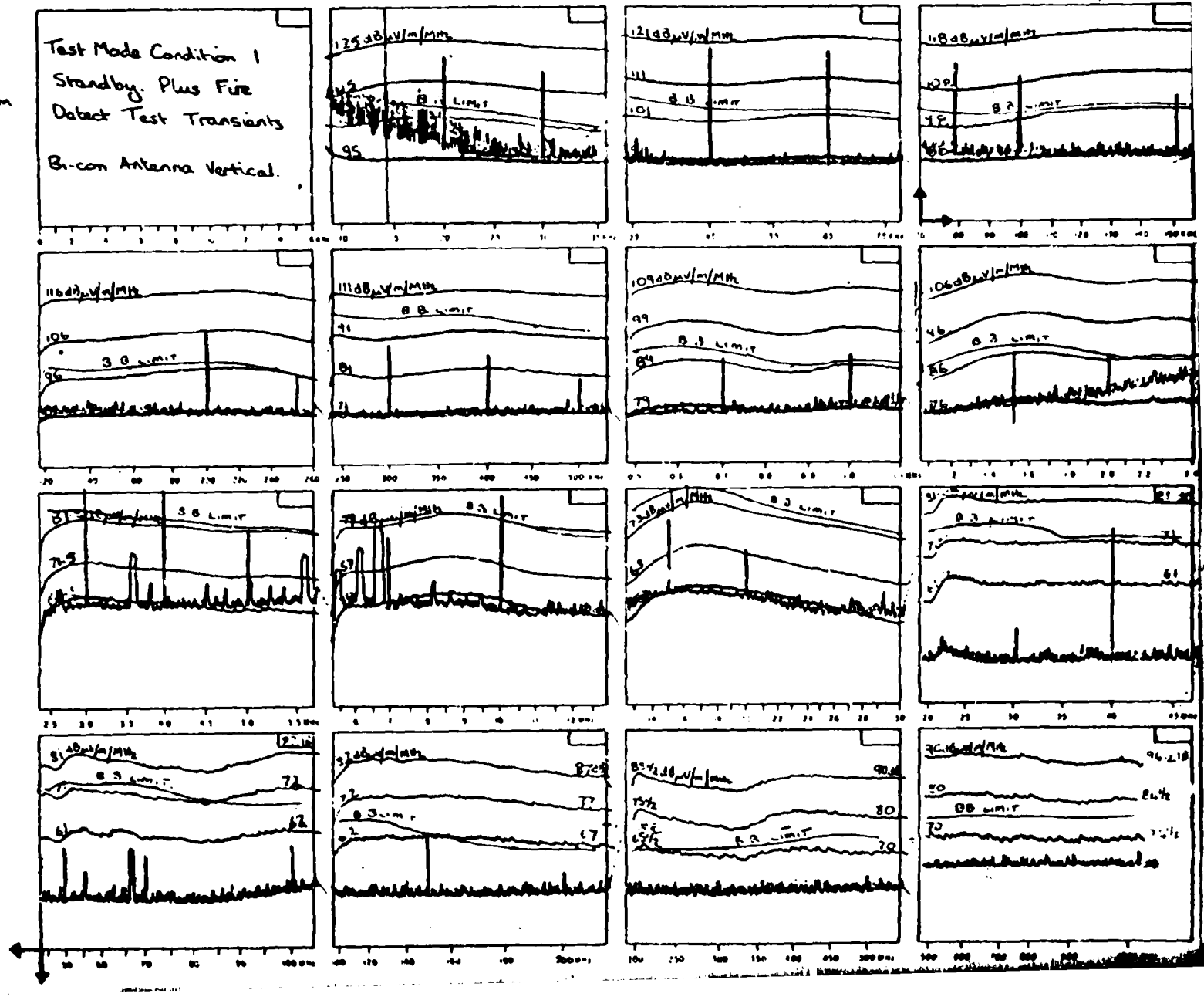
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



Company Gemaner Ltd

Program Advanced Fire Detection System

Test No. -

Test Specimen -

Date 10-6-80

Conducted By PP

Test Spec. MIL-STD-461A NOTICE 1,2&3

Section RE 02

Scan Speed 4 mins/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250. S.N.

S.N.

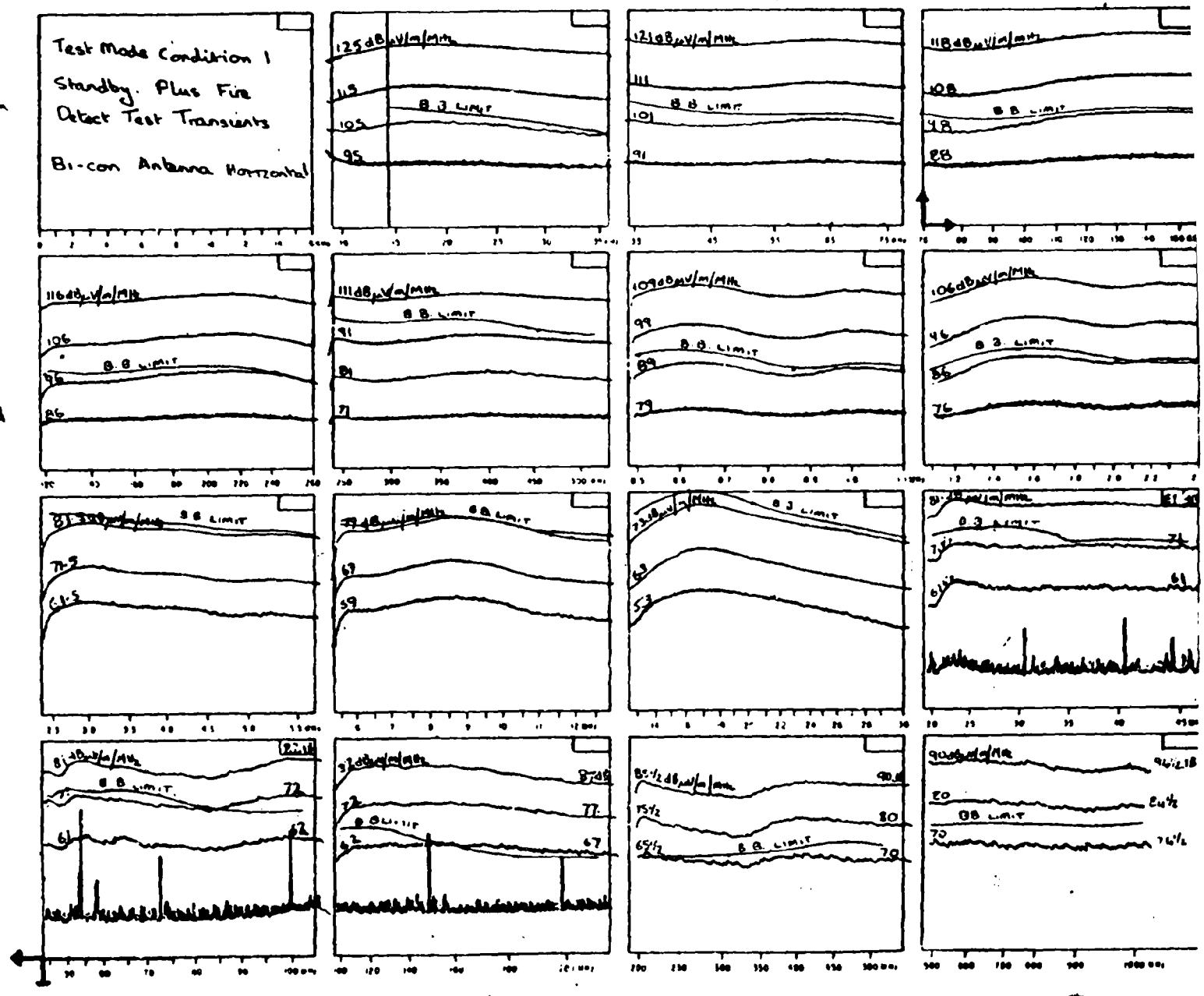
S.N.

S.N.

S.N.

S.N.

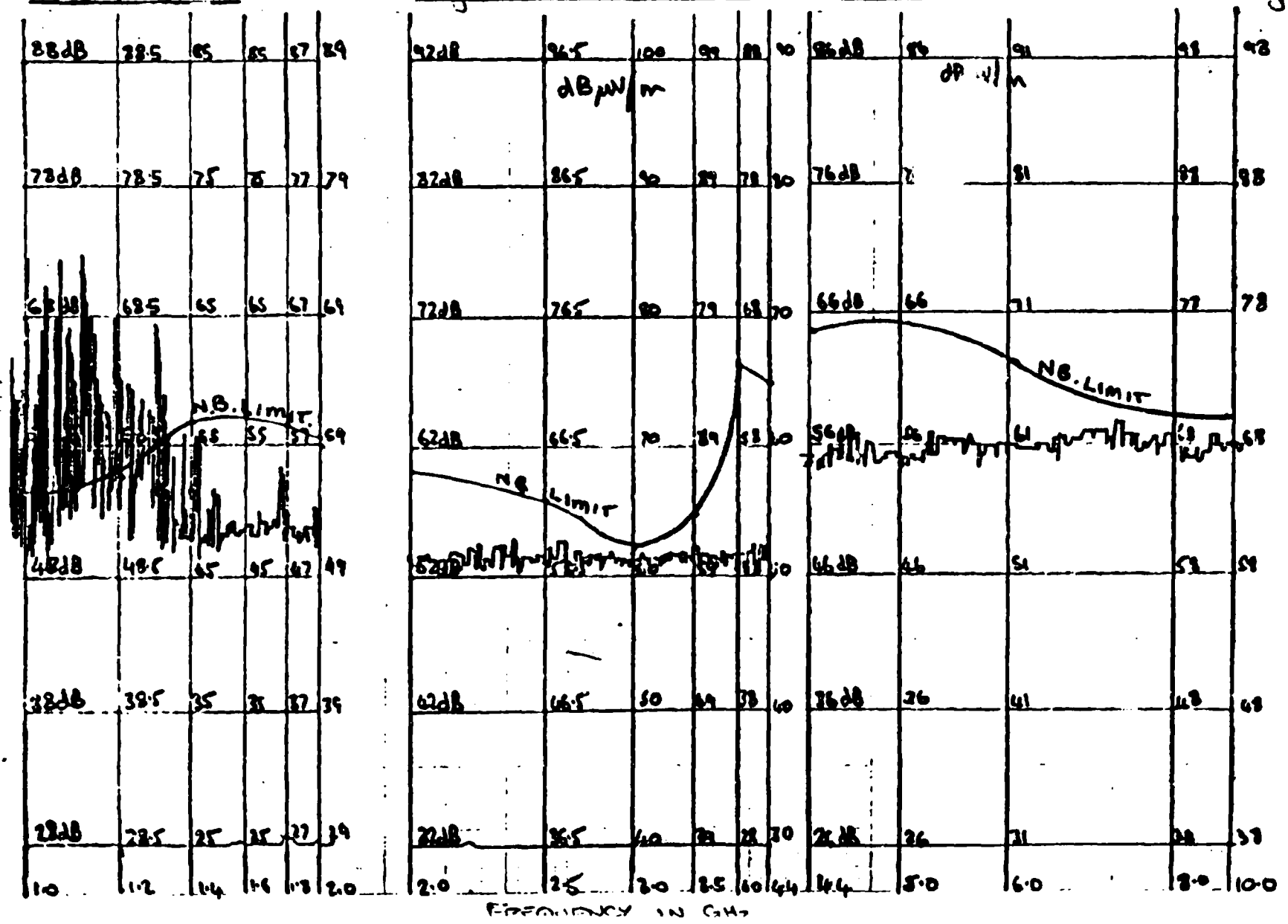
ELECTRO-METRICS

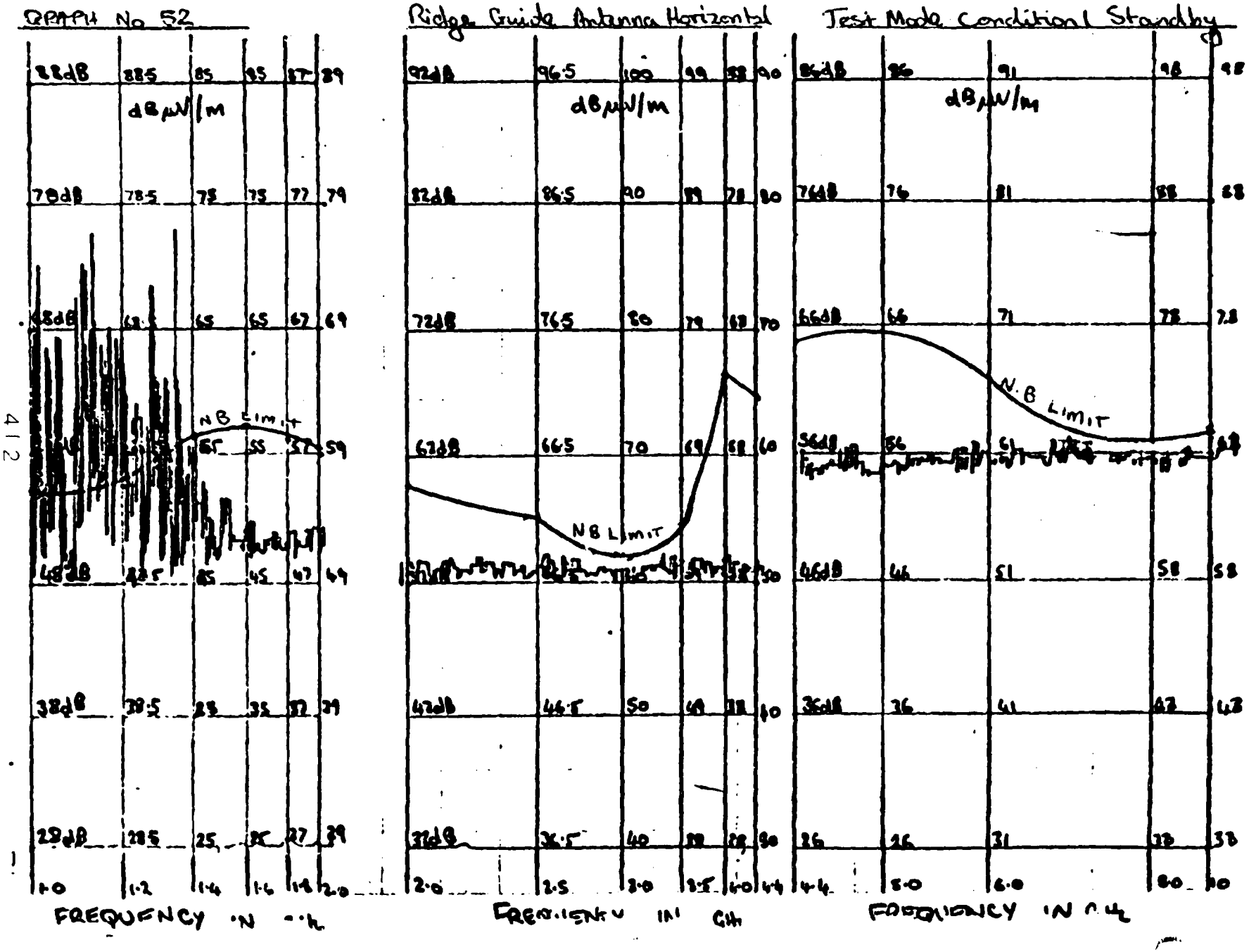


GRAPH NO 51

Ridge Guide Antenna VERTICAL

Test Mode Condition 1 Standby




QPPH No 52
dBμV/m
NB Limit
FREQUENCY IN GHz
Ridge Guide Antenna Horizontal
dBμV/m
NB Limit
FREQUENCY IN GHz
Test Mode Conditional Standby
dBμV/m
N.B Limit
FREQUENCY IN GHz

PAGE 53

Company GRAVINER LTD
Advanced Fire
Program Detection System

Test No. —

Test Specimen —

Date 7-5-80

Conducted By PPC

Test Spec. MIL-STD-461A
NOTICE 1 & 3

Section RE 02

Scan Speed 4 mins/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-258, S.N.

S.N.

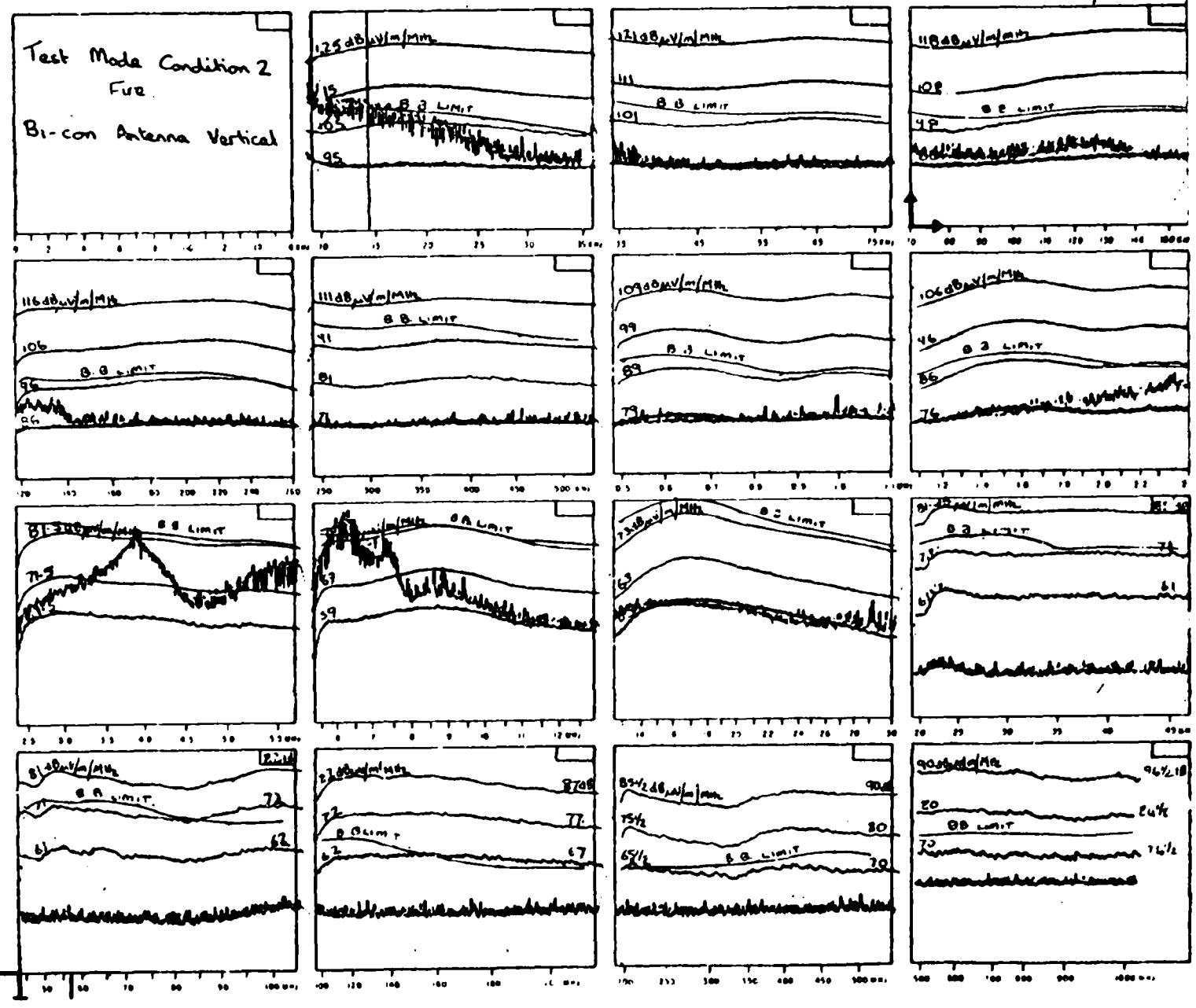
S.N.

S.N.

S.N.

S.N.

ELECTRO-METRICS



PAGE 54

Company GRAVINER LTD. Advanced Fire

Program Detection System

Test No. RE 02

Test Specimen —

Date 10-4-82

Conducted By PAC

Test Spec. MIL-STD-461A NOTICE 1,2 & 3

Section RE 02

Scan Speed 4/mins/band

Bandwidth WIDE

Detector Peak

Atten. Pos.

TEST EQUIPMENT

FSS-250, S.N.

S.N.

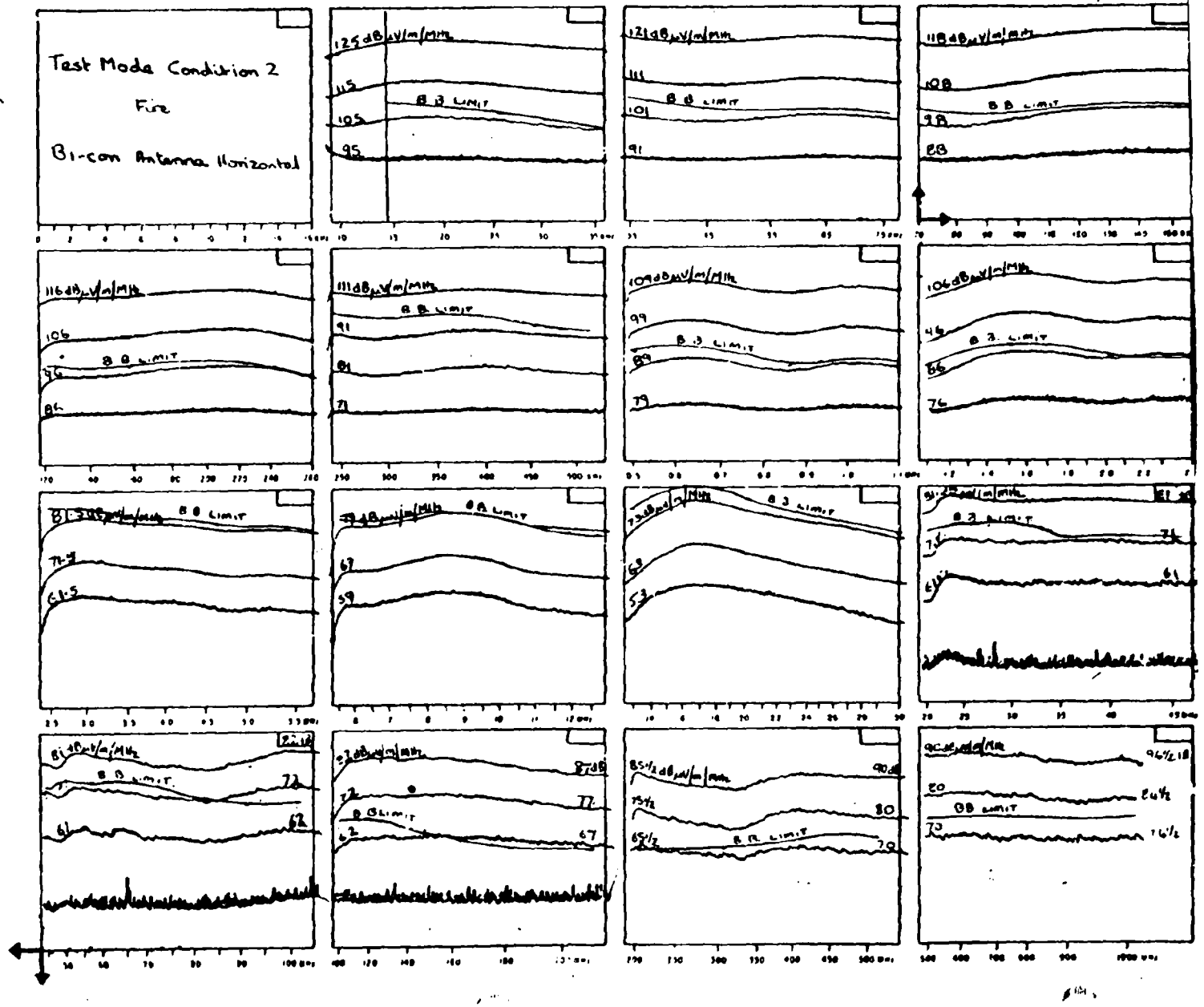
S.N.

S.N.

S.N.

S.N.

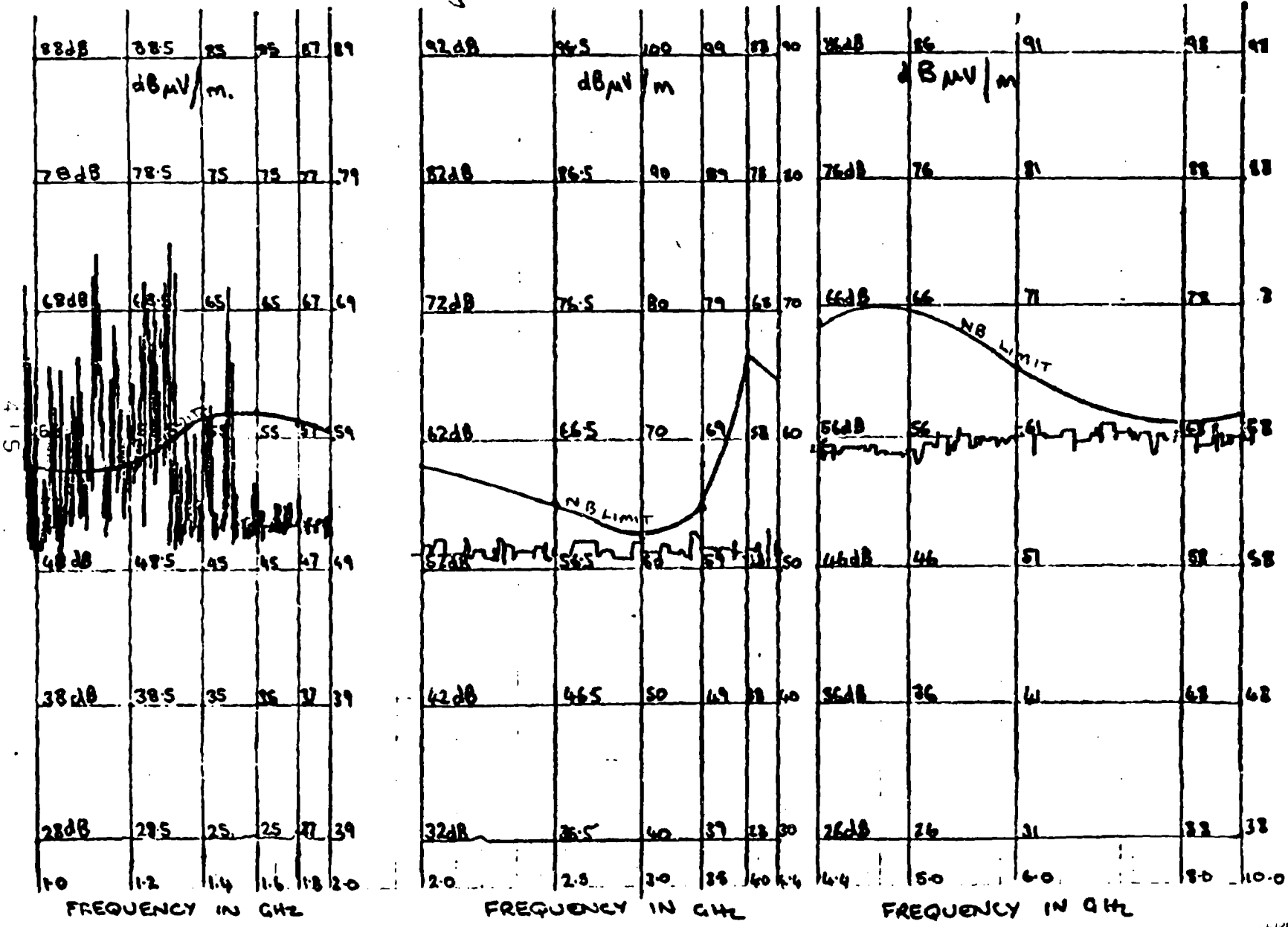
ELECTRO-METRICS



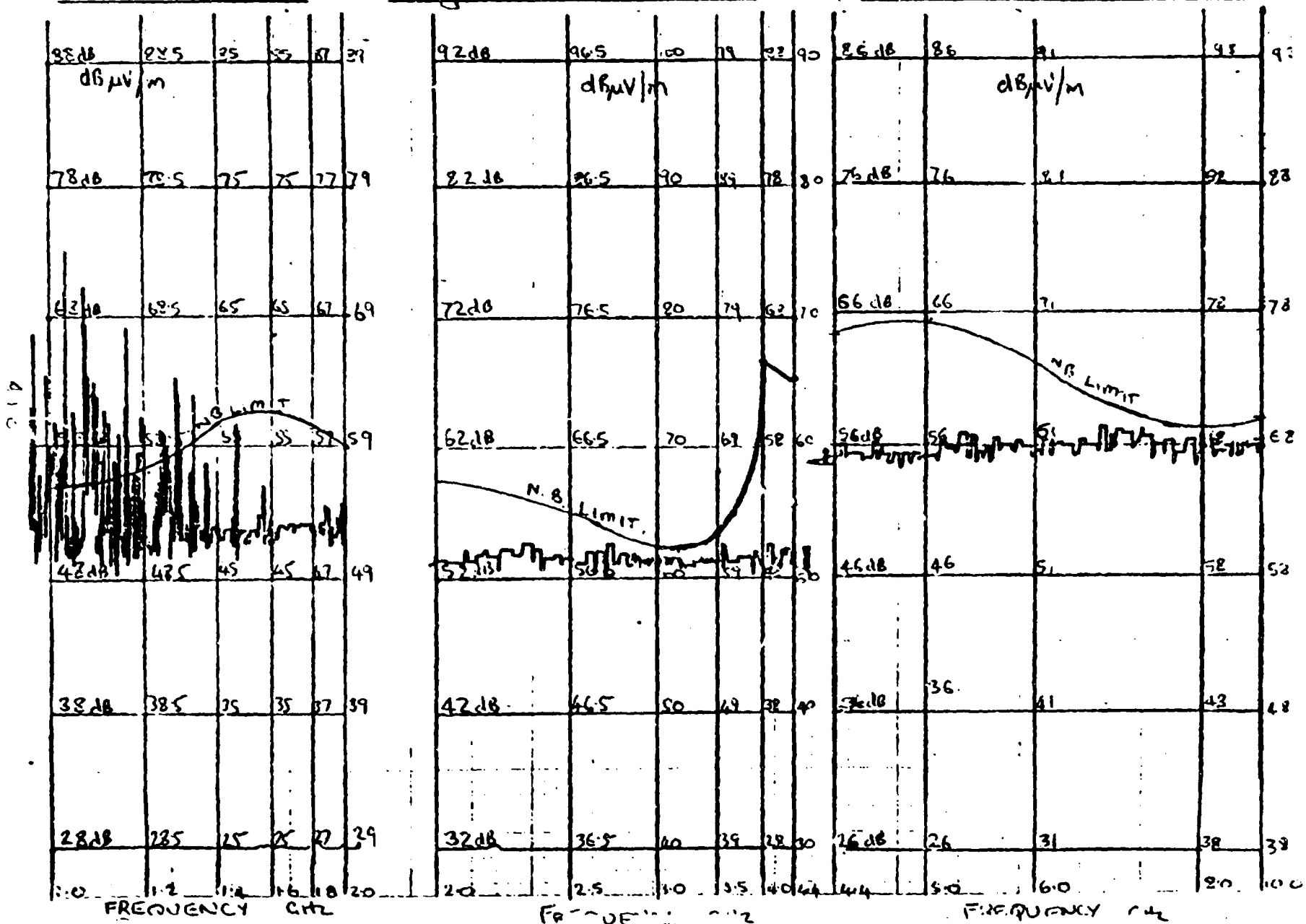
GRAPH No 55

Ridge Guide Antenna Vertical

Test Mode Condition 2



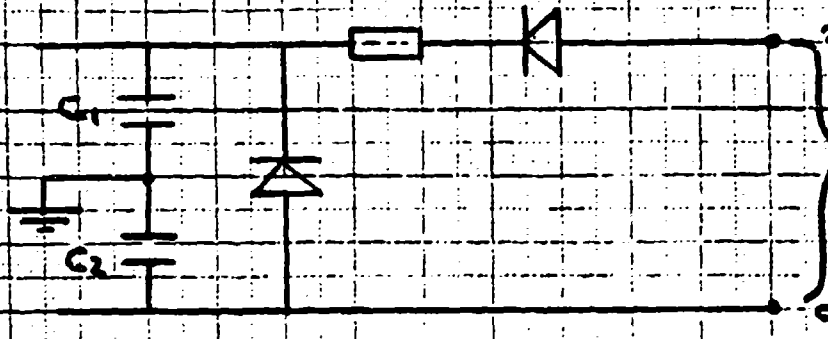
GRAPH No 56 — Ridge Guide Antenna Horizontal — Test Mode Condition 2 Fire



Appendix 3

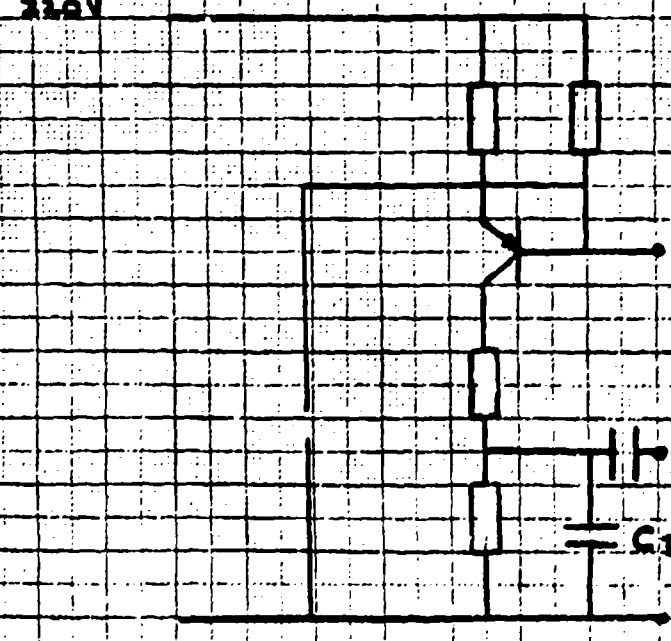
Test Sample Circuit Modifications

Modification To Common Logic P.C.B. In Both Control Units



C1 and C2 added to P.C.B as shown = 6.8μF

Modification To Drive Supply P.C.B. 2 P.C.B's in Control Unit B. One P.C.B in Control Unit A.



C3 added to P.C.B on each head drive, i.e. across resistors R25, R27, R29, R31, R49, R51, R53 and R55.

Appendix 4

Test Equipment Data

MEASUREMENT STANDARDS LABORATORY

MARCONI INSTRUMENTS LIMITED
Longacres St. Albans Herts. England

B.C.S approval no. 0006

Certificate of Calibration

Date of Issue 6th February, 1980.

Serial no 04195

Page 1 of 4 pages

A.D. Skinner.
Head of Laboratory.

Tested for :	Lucas Aerospace Ltd., Maylands Avenue, Hemel Hempstead, Herts.
Reference No. :	554315, 554317, 554318.
Order No. :	O/J/3144
Apparatus tested :	Interference Analyser. Model EMC-10. Serial No. 10471-E. with Current Probe PCA-10. Serial No. 471. Fairchild Electro-Metrics Corp.

The ambient temperature was 20 °C ±1 °C and the relative humidity was 50% ±10% RH.

Unless otherwise stated, the basis for estimating the limits of uncertainty quoted for the measurements shown, is the arithmetic summation of the relevant contributions.

The instrument was switched on for several hours before the tests were made to ensure that a stable operating temperature was reached. The tests were carried out in accordance with the procedures described in the instrument handbook supplied, the relevant paragraphs being quoted in each case.

423

continued .....

SHEET. 1.

Frequency calibration

The frequency calibration was tested as in para. 3.15.3(a) and the results are shown in Table 1.

Table 1

Digital frequency indicator	Measured frequency
50 Hz	48.3 Hz
100 Hz	95.3 Hz
500 Hz	494 Hz
1 kHz	1.006 kHz
2 kHz	2.012 kHz
5 kHz	4.998 kHz
10 kHz	10.000 kHz
20 kHz	19.974 kHz
50 kHz	49.864 kHz

The estimated limits of uncertainty of the measurement did not exceed ±1 Hz.

Amplitude calibration test

The amplitude calibration test was carried out as in para. 3.15.3(b) and the meter indication did not change by more than ±0.5 dB.

Before the next test the control settings were changed to the following :

GAIN	Amplitude calibration
WB range	1 V
Selective range	1 V
Bandwidth	50 Hz

A 20 kHz test signal was applied to the receiver and the signal level was adjusted until the meter indicated 1 V. The voltage at the input was then measured and was 1.00 volts ±0.1%.

Attenuator tests

The attenuator was tested as in para. 3.15.3(c) except that the impedance control was set to 50 Ω. The results are shown in Table 2.

continued.....

Table 2

Instrument reading	Nominal attenuation dB	Attenuation measured Wide band dB	50 Hz bandwidth dB	Estimated limits of uncertainty ±dB
10 V	ref.	ref.	ref.	-
1 V	20.0	20.0	20.0	0.1
100 mV	40.0	40.0	40.0	0.1
10 mV	60.0	60.0	60.0	0.2
1 mV	80.0	80.0	80.0	0.2
100 μV	100.0	100.0	-	0.5

Meter scale shape

The meter scale shape was tested using the procedure shown in para. 3.15.3(j). The results are shown in Table 3.

Table 3

Meter scale shape

Scale mark dB	Measured attenuation dB
0	ref.
3	3.0
6	6.0
10	9.8
15	15.2
20	19.6
25	24.6
30	29.8
35	35.6
40	39.9

The estimated limits of uncertainty for the scale shape measurements do not exceed ±0.1 dB.

Bandwidth tests

The 3 dB bandwidth of the analyser was measured on each bandwidth setting where the 3 dB changes were established against the laboratory standard attenuator. The analyser was tuned to 20 kHz. The results are shown in Table 4.

Table 4

Nominal bandwidth	Measured bandwidth
5 Hz	4.5 Hz ±0.1 Hz
50 Hz	53.6 Hz ±0.1 Hz
250 Hz	235.0 Hz ±0.1 Hz

continued.....

The tests listed below were made in accordance with the procedure in the manufacturer's handbook and were within the required specification limits.

Tangential sensitivity	para. 3.15.3(h)
Detector functions	para. 3.15.3(j)
Slideback operation	para. 3.8.6
Auto scan	para. 3.15.3(m)

Current probe

The current probe was connected to the instrument using a 62.5 cm length of coaxial cable. A test current was passed through a wire around which the current probe was clamped. The test current was adjusted to give a meter reading of 1 mV (equivalent to 1 mA). The result is shown in Table 5.

Control settings

Gain	As required for amplitude calibration
Selective range	1 mV
Impedance	10 kΩ
Filter	500 kHz
Bandwidth	50 Hz
ΔF	0
Frequency	as necessary
Detector function	CARRIER

Table 5

Test frequency	Indicated current	Measured current
1 kHz	1 mA	1.00 mA ±0.01 mA

The frequency response of the current probe was determined over the range 50 Hz to 50 kHz and the results are shown in Table 6.

Table 6

Frequency	Response relative to 1 kHz	The estimated limits of uncertainty do not exceed ±dB
50 Hz	-1.5 dB	0.2
100 Hz	-0.8 dB	0.1
200 Hz	-0.1 dB	0.1
1 kHz	0 dB	0.1
* 2 kHz	-0.1 dB	0.1
* 5 kHz	-0.25 dB	0.1
* 10 kHz	-0.75 dB	0.2
* 20 kHz	-1.1 dB	0.2
* 50 kHz	-1.8 dB	0.2

*These measurements are not within the scope of the Laboratory's prevailing approval but are reported herein for completeness.

426

Measurements made by [signature] Sheet 1.

FAIRCHILD EMC 25 MEASURING SET

TABLE 1.1. SENSITIVITY AND BANDWIDTH

BAND	FREQUENCY RANGE	BANDWIDTHS (3db) (Nominal)			*SENSITIVITY		
		.1 NB	NB	WB	.1NB	NB	IMPULSE WB db/uV/MHz
1	10.0 kHz – 35.0 kHz	50 Hz	500 Hz	4 kHz	.016	.04	+34
2	35.0 kHz – 75.0 kHz	50 Hz	500 Hz	4 kHz	.016	.04	+33
3	70.0 kHz – 150 kHz	50 Hz	500 Hz	4 kHz	.016	.05	+33
4	120 kHz – 240 kHz	50 Hz	500 Hz	4 kHz	.016	.05	+33
5	240 kHz – 500 kHz	50 Hz	500 Hz	4 kHz	.016	.06	+33
6	0.5 MHz – 1.1 MHz	50 Hz	500 Hz	5 kHz	.016	.06	+32
7	1.1 MHz – 2.4 MHz	50 Hz	500 Hz	5 kHz	.016	.06	+32
8	2.4 MHz – 5.5 MHz	500 Hz	5 kHz	50 kHz	.03	.10	+22
9	5.5 MHz – 12.5 MHz	500 Hz	5 kHz	50 kHz	.03	.10	+22
10	12.5 MHz – 30 MHz	500 Hz	5 kHz	50 kHz	.03	.10	+24
11	20 MHz – 45 MHz	5 kHz	50 kHz	500 kHz	.22	0.6	+20
12	45 MHz – 100 MHz	5 kHz	50 kHz	500 kHz	.22	0.8	+20
13	100 MHz – 200 MHz	5 kHz	50 kHz	500 kHz	.22	0.8	+20
14	200 MHz – 500 MHz	5 kHz	50 kHz	500 kHz	.35	1.0	+23
15	500 MHz – 1000 MHz	5 kHz	50 kHz	500 kHz	.50	1.6	+30

* NOTE: Tangential Sensitivity – defined as the internal noise level or as the input signal level required to raise the meter reading 3 dB above the instrument noise. Tangential Sensitivity level is at least 8 dB above minimum discernible signal (MDS). MDS is sometimes defined as being 0.5 dB above the noise level.

SHEET 5

MEASUREMENT STANDARDS LABORATORY

MARCONI INSTRUMENTS LIMITED
Longacres St. Albans Herts. England

B.C.S approval no. 0006

Certificate of Calibration

Date of Issue 13th February, 1980.

Serial no 04171

A.D. Skinner.
Head of Laboratory.

Tested for : Electro Metrics Ltd.,
84 Tile House Street,
Hitchin,
Herts.

Order No. : O/J/3144.

Reference No. : 554313.

Apparatus tested : Interference Analyser.
Model EMC - 25 mk 3 Serial No. 366
Fairchild Electrometric Corp.

The ambient temperature was 20 °C ±1 °C and the relative humidity was 50% ±10% RH.

The basis for estimating the limits of uncertainty quoted for the measurements shown, is the arithmetic summation of the relevant contributions.

The instrument was tested at the 50 ohm coaxial input using a source of signals of 50 ohms impedance and having a waveform which approximated closely to a sine curve.

The instrument was tested at each of the frequencies shown in Table 1 in accordance with the following paragraphs. The function switch was set to 'CARR'.

Test 1.

With the tuning dial and range switch set to each frequency in turn, the input signal frequency was adjusted to produce a maximum reading on the meter and the measured frequency recorded in Table 1, Col. 2.

Test 2.

The 6 dB bandwidth was measured by noting the total frequency change above and below the frequency recorded in Test 1, which resulted in a fall in a meter indication of 6 dB as established against the laboratory standard attenuator. The 6 dB bandwidth was measured on both the narrow and broad bandwidth settings. The results are recorded in Table 1, Cols. 4 and 5.

Test 3.

The 'calibration setting' was determined by applying an input voltage of 100 μV for ranges 1 to 10 and 1 mV for ranges 11 to 15 with the input attenuator set to 40 dB (BLACK) for ranges 1 to 10 and to 60 dB (RED) for ranges 11 to 15. The instrument gain control was then adjusted to give an indication on the meter of 0 dB. With the detector function switch set to 'PEAK' and the bandwidth control switched to 'wide' the 'shunt cal' button was pressed and the resulting reading on the meter noted and recorded as the calibration setting (dBμV) in Table 1, Col. 3.

Test 4.

The broadband correction factor in dBμV/MHz was determined on each range using an impulse generator type CIG 25 SN 120. The results of this test are shown in Table 1, Col. 7. The impulse generator was calibrated at the 70 dBμV/MHz and 90 dBμV/MHz settings before use. The calibration showed that the output was within ±0.5 dBμV/MHz of the setting over the required frequency range. The repetition rate was set to 100 Hz.

Test 5.

For this test the receiver was first calibrated for direct reading signal levels in dBμV (see para. 3.3.1 CW CALIBRATION in the instrument handbook).

With the attenuator control set to the fully counter-clockwise position the input signal giving unity signal/noise ratio was measured by noting the input voltage which caused the meter noise reading to increase by 3 dB. The results of this test are shown in Table II.

Test 6.

The 6 x 20 dB steps of the input attenuator were compared with the laboratory standard attenuator at 30 MHz. The results are shown in Table III. For convenience the Black scale was used for these tests.

Test 7.

The scale shape of the meter was tested at 30 MHz and the result is shown in Table IV.

continued .....

Table 1

Band	Frequency kHz	Measured frequency kHz	Calibration setting dB	6 dB Bandwidth Narrow Hz	6 dB Bandwidth Wide kHz	Broad band correction factor dBμV/MHz
1	10	10.0	+1.0			
	14	14.5	+1.0			
	18	18.3	+1.0			
	22	22.3	0	880	5.80	43
	26	25.9	-0.5			
	30	30.0	-1.0			
	34	34.0	-1.0			
2	35	35.0	-1.0			
	40	40.8	-1.0			
	45	45.7	-1.0			
	50	50.3	-1.0			
	55	55.1	-1.0	890	5.62	43
	60	59.7	-1.0			
	65	64.9	-1.5			
	70	70.0	-1.5			
	75	75.2	-2.0			
3	70	68.2	-2.5			
	80	79.9	-2.0			
	90	90.5	-2.0			
	100	99.2	-1.0			
	110	109.7	-1.0	870	7.31	43
	120	118.3	-1.0			
	130	128.3	0			
	140	139.1	+0.5			
	150	149.9	+0.5			
4	120	119.2	+0.5			
	140	141.8	+0.5			
	160	161.1	+0.5			
	180	181.6	+0.5	600	7.51	43
	200	199.1	+0.5			
	220	219.5	0			
	240	238.8	0			
	260	258.6	0			
5	250	249.4	-2.0			
	300	305.4	-2.0			
	350	354.2	-2.0			
	400	400.7	-2.0	850	5.76	43
	450	450.1	-2.0			
	500	498.8	-2.1			

continued.....

Table I continued

Band	Frequency MHz	Measured frequency MHz	Calibration setting dB	6 dB Bandwidth Narrow Hz	Wide kHz	Broad band correction factor dBμV/MHz
6	0.5	0.49	-2.5			
	0.6	0.61	-2.0			
	0.7	0.71	-2.0			
	0.8	0.81	-2.0	790	6.31	43
	0.9	0.90	-2.0			
	1.0	1.00	-2.0			
	1.1	1.10	-2.0			
7	1.2	1.19	-2.0			
	1.4	1.42	-2.0			
	1.6	1.61	-1.75			
	1.8	1.79	-1.75	900	6.10	44
	2.0	1.99	-2.0			
	2.2	2.19	-2.0			
	2.4	2.40	-2.0	kHz		
8	2.5	2.49	-2.0			
	3.0	3.01	-2.0			
	3.5	3.49	-2.0			
	4.0	3.99	-1.5	10.09	65.6	23
	4.5	4.43	-2.0			
	5.0	4.96	-1.75			
	5.5	4.94	-1.75			
9	6.0	6.01	-1.0			
	7.0	7.04	-1.0			
	8.0	7.99	-0.5			
	9.0	9.01	0	9.98	66.0	24
	10.0	9.98	0			
	11.0	10.96	-1.0			
	12.0	12.00	-1.0			
10	14	13.99	-1.0			
	16	16.02	0			
	18	17.85	0			
	20	19.77	0			
	22	21.49	0	10.02	69.4	25
	24	23.66	0			
	26	25.72	0			
	28	27.77	-0.5			
	30	29.86	0			
11	20	19.72	-2.0			
	25	25.40	-1.0			
	30	30.18	-1.0	121.1	707.7	-1
	35	35.01	0			
	40	39.75	-1.0			
	45	45.04	-1.0			

Table I continued

Band	Frequency MHz	Measured frequency MHz	Calibration setting dB	6 dB Bandwidth Narrow kHz	6 dB Bandwidth Wide kHz	Broad band correction factor dBμV/MHz
12	50	50.41	0			
	60	60.59	+1.0			
	70	70.34	+1.5			
	80	79.93	+2.0	106.6	740.2	+1
	90	89.57	+1.0			
	100	100.00	+1.0			
13	100	99.8	+2.0			
	120	120.9	+2.5			
	140	141.3	+2.0			
	160	160.7	+2.0	109.0	673.2	+2
	180	179.4	0			
	200	199.4	-1.0			
14	200	200.5	-1.0			
	250	255.7	-1.0			
	300	303.5	-2.0			
	350	352.1	-3.0	114.6	624.6	+2
	400	399.3	-2.0			
	450	448.1	-2.0			
	500	500.3	-2.0			
15	500	504.4	0			
	600	612.4	+1.0			
	700	708.1	+1.0			
	800	805.5	+1.5	132.1	753.7	+1
	900	899.1	+1.0			
	1000	997.7	+1.0			

continued.....

Table II

Ranges	Input voltages for unity signal/noise ratio
1 - 5	Less than -27 dBμV
6 & 7	Less than -27 dBμV
8 & 9	Less than -20 dBμV
10	Less than -11 dBμV
11	Less than -5 dBμV
12	Less than -4 dBμV
13	Less than +1 dBμV
14	Less than 0 dBμV
15	Less than +6 dBμV

Table III

Switch setting (Black scale) (dB)	Attenuation relative to 40 dB position Frequency 30 MHz (dB)
0	-38.2
20	-20.0
40	ref.
60	+20.0
80	+40.0
100	+60.2

Table IV

Attenuator setting (dB)	Meter reading (dB)
+20	+20.2
+18	+18.2
+16	+17
+14	+15
+12	+12.2
+10	+9.8
+8	+7.5
+6	+5
+4	+3.5
+2	+2
0	ref.
-2	-2.4
-4	-5
-6	-7.2
-8	-9
-10	-10
-12	-11
-14	-13
-16	-16
-18	-18
-20	-20
-30	-30.5
-40	-39.5

The estimated limits of uncertainty of the measurements did not exceed the following :

for frequency : ±1.0%.

for bandwidth :

	narrow	wide
ranges 1 to 7	±30 Hz	±100 Hz
ranges 8 to 10	±100 Hz	±1 kHz
ranges 11 to 15	±1 kHz	±10 kHz

for calibration settings : ±0.5 dB.

for attenuation and meter scale law : ±0.5 dB.

The insertion loss of the three coaxial cables fitted with type TNC male connectors was measured at the frequencies shown in Table V.

Table V

Cable No./length	Frequency MHz	Insertion loss dB	Estimated limits of uncertainty ±dB
CAC-25 RG223	1	0.08	0.02
7.52 metres	30	0.54	0.02
	500	2.73	0.1
	1000	3.85	0.1
CAC-25 RG223	1	0.09	0.02
	30	0.56	0.02
	500	2.70	0.1
	1000	3.89	0.1
CAC-25 RG223	1	0.10	0.02
7.95 metres	30	0.57	0.02
	500	2.87	0.1
	1000	4.17	0.1
CAC-15 RG223	1	0.09	0.02
	30	0.58	0.02
	500	2.94	0.1
	1000	4.29	0.1

Measurements made by : R. Jewell

----- END -----

Telephone [illegible]
Telex 82431 Cables Robelect Hitchin

REL Industrial Limited

CALIBRATION REPORT No. 2018

INSTRUMENT 60d8 Step Attenuator		CUSTOMER & ADDRESS
TYPE No. 90389-3	SER. No. -	Lucas Aerospace,
MANUFACTURER	Singer	Hemel Hempstead.
CAL. DATE	4.3.80	
RECOMMENDED RECALIBRATION DATE	4.9.80	

CALIBRATION

Attenuator Setting (dB)	Actual Attenuation (dB) 10Hz	1MHz	100MHz	1GHz
3	2.9	2.9	2.9	3.0
6	5.8	5.9	5.9	6.3
10	11.1	11.1	11.6	11.2
20	20.0	20.0	20.3	20.0
30	30.2	30.2	30.1	30.2
60	60.8	61.0	61.2	60.8

Cal Lab has 0524 (0526) approval cert no. 71990/ 1/01

All measurements are traceable to national standard via B.C.S.

Telex no. 151 Cables Robject Hitchin

REL Industrial Limited

CALIBRATION REPORT No. 2020

INSTRUMENT Radio Interference Analyser Receiver		CUSTOMER & ADDRESS
TYPE No. NM 65T	SER. No. 145	Lucas Aerospace,
MANUFACTURER	Singer	Hemel Hempstead.
CAL. DATE	5.3.80	
RECOMMENDED RECALIBRATION DATE	5.9.80	

CALIBRATION

Meter Scale Shape (Tracking Accuracy)

dB	Field Intensity	Direct Peak	Slideback Peak
0	0.3	2.5	2.5
10	10.0	10.1	10.1
20	20.0	20.0	20.0
30	30.5	30.1	30.1
40 ref	40.0	39.9	39.9
50	50.0	49.5	49.8
60	59.0	58.8	58.8

Attenuator Accuracy		Output Sockets
dB	Meter Reads	X O/P Single Band 1.0V to 10.36V
0 ref	40.0	X O/P Multiple Band 1 0.97V to 3.29V
+ 20	39.2	Band 2 3.88V to 6.5V
+ 40	39.2	Band 3 6.81V to 9.92V
+ 60	38.9	Y O/P 7.325V
		Video Linear 0.4V pk-pk
		Stretched Linear 1.65V pk
		Pulse Width 0.5 m'sec
		Audio ✓

CALIBRATED BY

APPROVED BY

CALIBRATION DETAILS CONTINUATION SHEET 2 CALIBRATION REPORT No. 2020

Dial	Actual	Cal.	Sensitivity		Reserve
Freq.	Freq.	Figures	NB	BB	Gain
GHz	GHz	dB	dB referred 10 uV		dB
Band 1					
1.0	1.002	41.5	0	25.5	17.0
1.5	1.502	41.0	0	22.0	20.0
2.0	2.003	41.4	0	24.0	20.0
Band 2					
2.05	2.059	43.0	3.0	32.5	15.0
2.5	2.508	43.0	0	28.0	15.5
3.0	3.007	42.5	0	28.5	15.0
3.5	3.510	42.0	0	28.0	16.2
4.0	4.001	41.5	3.5	33.0	11.0
4.4	4.403	40.5	5.5	35.0	9.5
Band 3					
4.4	4.406	40.5	9.0	38.0	13.0
5.0	5.008	39.8	9.1	38.5	13.2
5.5	5.507	40.0	12.0	41.0	11.0
6.0	6.014	38.6	14.5	44.0	10.0
6.5	6.516	38.2	8.0	37.0	15.8
7.0	7.022	38.0	9.5	38.5	15.0
7.5	7.516	38.0	11.2	41.0	13.5
8.0	8.020	38.0	7.5	37.0	16.0
8.5	8.518	37.5	6.5	38.0	17.0
9.0	9.016	35.0	6.4	35.5	18.0
9.5	9.520	34.5	5.0	34.0	19.5
10.0	10.011	34.2	6.0	35.0	13.0

CALIBRATION DETAILS CONTINUATION SHEET 3 CALIBRATION REPORT No. 2020

EQUIPMENT USED

Hewlett Packard 612A Signal Generator

Marconi 6055 Signal Source

" 6056 " "

" 6057B " "

" 6058 " "

PRD Directional Coupler P 4420 - 20

" " " L 4420 - 20

" " " C 4420 - 20

" " " S 4420 - 20

" " " X 4420A - 20

Rohde & Schwarz Power Meter NRS

Systron & Donner Counter 6016

Weinschel 10 dB Step attenuator

" 10 dB Pads

" 50 ohms load

REMARKS

I F gain control intermittant in 'Automatic' position.

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard via B.C.S.

438

CALIBRATION REPORT No. SHEET 16.

[illegible] INDUSTRIES LTD

Telex 8243i Cables Roble Harman

REL Industrial Limited

CALIBRATION REPORT No. 2019

INSTRUMENT 6' Transmission Lead		CUSTOMER & ADDRESS
TYPE No. 92194	SER. No -	Lucas Aerospace,
MANUFACTURER	Singer	Hemel Hempstead.
CAL. DATE	5.3.80	
RECOMMENDED RECALIBRATION DATE	5.9.80	

CALIBRATION

Frequency GHz	Loss dB
1	- 0.6
2	- 1.0
3	- 1.4
4	- 1.6
5	- 1.8
6	- 2.2
7	- 2.2
8	- 2.6
9	- 2.9
10	- 3.6

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard vis B.C.S.

439

SHEET 17

Telex 6243i Cables Rodlect Hemel

REL Industrial Limited

CALIBRATION REPORT No. 1996

INSTRUMENT Current Probe		CUSTOMER & ADDRESS
TYPE No. 91197-1	SER No. BC 72	Lucas Aerospace,
MANUFACTURER		Hemel Hempstead.
CAL. DATE	12.2.80	
RECOMMENDED RECALIBRATION DATE	12.3.80	

CALIBRATION

Frequency	ZT Ohms	dB Above or Below 1 ohm
30 Hz	0.006	- 44.44
100 Hz	0.03	- 30.46
200 Hz	0.06	- 24.44
500 Hz	0.14	- 17.08
1 KHz	0.24	- 12.40
2 KHz	0.32	- 9.90
5 KHz	0.38	- 8.40
10 KHz	0.38	- 8.40
20 KHz	0.38	- 8.40
50 KHz	0.36	- 8.87
100 KHz	0.37	- 8.64
200 KHz	0.38	- 8.40
500 KHz	0.38	- 8.40
1 MHz	0.36	- 8.87
2 MHz	0.35	- 9.12
5 MHz	0.30	- 10.46
8 MHz	0.19	- 14.42

Telex 8243[illegible]

REL Industrial Limited

CALIBRATION REPORT No. 1997

INSTRUMENT Current Probe.		CUSTOMER & ADDRESS
TYPE No. 91550-1	SER. No. 912-130	Lucas Aerospace,
MANUFACTURER	Stoddart	Hemel Hempstead.
CAL. DATE	12.2.80	
RECOMMENDED RECALIBRATION DATE	12.8.80	

CALIBRATION

Frequency MHz	ZT Ohms	dB Above or Below 1 Ohm
0.01	0.16	- 15.92
0.02	0.29	- 10.75
0.05	0.72	- 2.85
0.1	1.2	1.58
0.2	2.3	7.23
0.5	4.5	13.06
1.0	5.2	14.32
2.0	5.6	14.96
5.0	6.0	15.56
10.0	5.5	14.81
20.0	5.5	14.81
50.0	4.4	12.87
60.0	4.4	12.87
70.0	4.2	12.46
80.0	3.0	9.54
90.0	3.4	10.63
100.0	3.4	10.63

Telephone Hitchin (0462) 57161 (10 lines)
Telex 82431 Cables: Roblect Hitchin

REL Industrial Limited

CALIBRATION REPORT No. 1973

INSTRUMENT EFS/LMT/LDI		CUSTOMER & ADDRESS
TYPE No.	SER. No. 056/011	Lucas Aerospace,
MANUFACTURER	IFI	Hemel Hempstead.
CAL. DATE	20.12.79	
RECOMMENDED RECALIBRATION DATE	20.6.80	

CALIBRATION

Input Volts/Range—	EFS Meter Reading Volts/Metre	LDI Meter Reading Volts/Metre
3 Volt Range	3 Volt Range	3 Volt Range
1.0	1.0	1.0
1.5	1.5	1.5
2.0	2.0	2.0
2.5	2.49	2.49
3.0	3.0	3.0
10 Volt Range	10 Volt Range	10 Volt Range
3.0	3.0	3.0
4.0	4.1	4.0
5.0	5.2	5.0
6.0	6.2	6.0
7.0	7.1	7.0
8.0	8.0	8.0
9.0	9.0	9.0
10.0	10.0	10.0

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard via B.C.S.

Telephone Hitchin (0462) 51151 (10 lines)
Telex 82431 Cables Roblect Hitchin

REL

REL Industrial Limited

CALIBRATION REPORT No. 1974

INSTRUMENT EFS/LMT		CUSTOMER & ADDRESS
TYPE No.	SER. No. 055	Lucas Aerospace,
MANUFACTURER	IFI	Hemel Hempstead.
CAL. DATE	20.12.79	
RECOMMENCED RECALIBRATION DATE	20.6.80	

CALIBRATION

Input Volts/Range	EFS Meter Reading Volts/Metre
3 Volt Range	3 Volt Range
1.0	1.05
1.5	1.5
2.0	2.0
2.5	2.5
3.0	3.0
10 Volt Range	10 Volt Range
3.0	3.0
4.0	4.0
5.0	5.1
6.0	6.1
7.0	7.1
8.0	8.1
9.0	9.0
10.0	10.0

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard via B.C.S.

SHEET 21

S P Mead

Telephone Hitchin (0462) 51161 (15 lines)
Telex 82431 Cables Robject Hitchin

REL Industrial Limited

CALIBRATION REPORT No. 1976

INSTRUMENT Levelling Pre-Amp		CUSTOMER & ADDRESS
TYPE No. LPA-I	SER. No 0374942	Lucas Aerospace,
MANUFACTURER	I.F.I.	Hemel Hempstead.
CAL. DATE	4.1.80	
RECOMMENDED RECALIBRATION DATE	4.7.80	

CALIBRATION

E.F.S. Meter Reading	LPA-I Meter Reading Channel A Unit A	Channel B Unit B
Volts/Metre	Volts/Metre	Volts/Metre
3 Volt Range		
1.0	1.0	0.9
1.5	1.5	1.45
2.0	1.99	1.9
2.5	2.5	2.44
3.0	3.0	3.0
10 Volt Range		
3.0	3.0	3.0
4.0	4.0	4.0
5.0	5.0	4.9
6.0	5.9	5.9
7.0	7.0	6.9
8.0	8.0	7.8
9.0	9.0	8.8
10.0	10.0	10.0

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard via B.C.S.

marconi instruments

MARCONI INSTRUMENTS LIMITED
SERVICE DIVISION
Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds. LU2 9NS
Telephone: Luton 33866 Telex: 825248

Def Stan. 05-24/2 Registration No. 13 L M 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M.I. 90-day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No. 630490/3

Description Signal Generator TF. 144E/-4

Serial No. 53698-12
c/w. 13 Amp Plug & Lead

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

The calibration was carried out in accordance with the general requirements of Def Stan. 05-26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

Remarks Periodicity 12 Months

CALIBRATED TO :- EH035 1552

Signed C. C. Payne
for Quality Manager, Service Division

Date 19-2-80

445

SHEET 23

MARCONI INSTRUMENTS LIMITED
SERVICE DIVISION
Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds. LU2 9NS
Telephone Luton 33866 Telex 825248

Def Stan 05-24/2 Registration No 13 LM01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M I 90 day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements

Job No	614285
Description	Signal Generator TF. 801D/1
Serial No	53599/24 c/w. Mains Lead & 13 Amp Plug

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist

The calibration was carried out in accordance with the general requirements of Def Stan 05-26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist

Remarks

CALIBRATED TO MAN. SPEC.

Signed Alan Bates
for Quality Manager, Service Division

Date 22 MAR 1979

RSL Industrial Limited

CALIBRATION REPORT No. 1930

INSTRUMENT Power Signal Source		CUSTOMER & ADDRESS
TYPE No. C203	SER. No. 125	Lucas Aerospace,
MANUFACTURER	AHL	Hemel Hempstead.
CAL. DATE	26.9.79	
RECOMMENDED RECALIBRATION DATE		

CALIBRATION

7050H

Frequency	Dial	Meter 100W		Meter 50W	
		Monitor O/P	O/P Power	Monitor O/P	O/P Power
200	3160	No Coupler		No Coupler	
250	5580	+ 17 dBm	45W	+ 17 dBm	45W) •
300	7220	+ 16 "	50W	+ 16 "	50W) •
350	8230	+ 16 "	50W	+ 16 "	50W) •
400	9100	+ 15 "	50W	+ 15 "	50W) •
450	9790	+ 15"	50W	+ 15 "	50W) •

7051AH

		Meter 80W		Meter 40W	
450	-	-	-	-	-
475	3520	+ 17 dBm	40W	+ 14.4 dBm	20W
500	3790	+ 17 "	52W	+ 14.4 "	25W
525	4050	+ 17.8 dBm	54W	+ 14.5 "	26W
550	4260	+ 18.0 "	54W	+ 14.6 "	26W
575	4480	+ 18.3 "	58W	+ 15.2 "	27W
600	4660	+ 18.5 "	58W	+ 15.2 "	27W
625	4840	+ 19.0 "	60W	+ 15.6 "	28W
650	5000	+ 19.2 "	60W	+ 16.2 "	29W
675	5170	+ 19.2 "	62W	+ 16.0 "	30W
700	5320	+ 19.5 "	63W	+ 16.2 "	30W
725	5430	+ 19.2 "	60W	+ 16.2 "	28W
745	5540			+ 16.3 "	28W

CALIBRATED BY 447

7051BH

Frequency	Dial	Meter 50W Monitor O/P	O/P Power
750	7650	+ 17.6 dBm	47W
800	8130	+ 17.6 "	47W
850	8540	+ 18.0 "	49W
900	8920	+ 18.3 "	49W
950	9250	+ 18.5 "	49W
1000	9560	+ 18.6 "	48W

* Meter reads same on both high and low ranges

EQUIPMENT USED

Rohde & Schwarz Power Meter

Systron & Donner Counter type 6016

P.R.D. Directional Couplers

Weinschel Attenuator Pads

Cal Lab has 0524 (0526) approval cert no. 71990/1/01

All measurements are traceable to national standard via B.C.S.

marconi instruments

MARCONI INSTRUMENTS LIMITED
SERVICE DIVISION
Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds. LU2 9NS
Telephone: Luton 33866 Telex 825248

Def. Stan. 05-24/2 Registration No. 13 LM 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M.I. 90-day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No. 630490/8

Description Voltmeter TF. 1041B

Serial No. JA 217-484
c/w. 2 Probes & Leads & T Connector Unit

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

The calibration was carried out in accordance with the general requirements of Def. Stan. 05-26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

Remarks Periodicity 12 Months

EH. 006. 153. III

Signed ..... for Quality Manager, Service Division

450 Date .....

SHEET 28

Marconi instruments

MARCONI INSTRUMENTS LIMITED
SERVICE DIVISION
Electrical and Electronic Calibration Laboratories
The Airport, Luton, Beds. LU2 9NS
Telephone: Luton 33866 Telex: 825248

Def Stan 05-24/2 Registration No 13 L M 01

Certificate of Test

This certificate is issued in accordance with our Order Acknowledgment, and the general terms and conditions of business of Marconi Instruments Limited. The M I. 90-day Warranty, details of which are given overleaf, applies only to the repairs carried out.

The equipment described below has been calibrated and found to comply with the manufacturer's published performance specification at the measured points, due allowance having been made for the uncertainty of the measurements.

Job No. 630490/9A

Description Electronic Voltmeter TF. 2604

Serial No. 200933-037
c/w. 2 Probes & Leads TM 5031B
+ 13 Amp Plug & Lead

The calibration was carried out using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

The calibration was carried out in accordance with the general requirements of Def. Stan. 05-26/2, using working standards which are subject to regular periodic verification, and the measurements are traceable to National Standards, except where none exist.

Remarks Periodicity 12 Months

[illegible] - 15/10/1984

Signed R. C. S. Payne
for Quality Manager, Service Division

Date 2.10.84

451

SHEET 29.

Appendix 5

TRANSIENT & SPIKE REPORT
AED/ENV/480550

Lucas Aerospace

Electrical Division

LABORATORY REPORT

GRAVINER LTD.

SLOUGH.

ADVANCED AIRCRAFT FIRE DETECTION SYSTEM :-

CONTROL UNIT TYPE 53813-203 SERIAL No 100

CONTROL UNIT TYPE 53813-204 SERIAL No 100

CREW WARNING UNIT TYPE 53813-202

TESTS CS06, RS02 TO MIL-STD-461A.

TRANSIENT VOLTAGE ACCEPTANCE TO MIL-STD-704A.

Leeds Old Road Bradford
West Yorkshire BD3 8LA England

WORKING NUMBER	A5704018
CUSTOMER	Graviner Ltd, Slough.
CUSTOMER'S EQUIPMENT	Advanced Aircraft Fire Detection Syst Control Unit Type 53813-203 S/N 100. Control Unit Type 53813-204 S/N 100. Crew Warning Unit Type 53813-202.
CUSTOMER'S REQUIREMENTS	The system is to be subjected to test. CS06, RS02 to Spefication MIL-STD-461A Tests for transient voltage acceptanc to be applied to the requirements of MIL-STD-704A for category "B" Equipme
CUSTOMER'S REPRESENTATIVE	Mr A. Mackrell.
TESTED BY	G. Mitchell.
DATE OF TESTS	April 1980.
TEST LOCATION	Environmental Laboratories, Bradford.
TEST EQUIPMENT	Pulse Generator Type AE 7753 Pulse Generator Type AE 7746 Oscilloscope Type 180A Serial No M2370, calibrated on each day of test.

1. INTRODUCTION

Tests were performed on the Advance Fire Detection System in accordance with the requirements of paragraphs 1.2.7., 1.2.9. and 1.2.11. of Messrs. Graviner Ltd E.M.I. Test Plan (Issue No 4). The tests were performed in order to demonstrate the system compliance with Tests CS06, RS02 to MIL-STD-461A, Notice No 3, Class A1 and MIL-STD-704A.

2. TEST ARRANGEMENT

2.1. TEST LAYOUT

The test layout was as shown in figure No 1 of the test plan.

2.2. OPERATION OF THE SYSTEM

2.2.1. CONDITION 1 "STANDBY"

This condition was when the U.V. source was switched off and the "FIRE" and "FIRE DET FAIL" indicators were not illuminated.

2.2.2. CONDITION 2 "FIRE"

This condition was when the U.V. source was switched on and the "FIRE" indicators were illuminated on the crew warning unit.

2.3. SUSCEPTIBILITY CRITERIA

The criteria for susceptibility/non-susceptibility was as follows :-

CONDITION 1 - Illumination of any Crew Warning Unit "FIRE" and "FIRE DETECT FAIL" indicators.

CONDITION 2 - Cancellation of either "FIRE" indicators.

2.4. TEST PROCEDURE

2.4.1. TESTS FOR TRANSIENT VOLTAGE ACCEPTANCE TO MIL-STD-704A.

2.4.2. POWER LEAD CONNECTIONS FOR TRANSIENT ACCEPTANCE.

For the purposes of transient voltage acceptance the power cables were linked as follows and treated as a single cable.

(1) 115V 400Hz Line to Control Unit "A" Pin 14.)
115V 400Hz Line to Control Unit "A" Pin 17.) all linked together
115V 400Hz Line to Control Unit "B" Pin 14.)

(2) 115V 400Hz Neutral to Control Unit "A" Pin 13.)
115V 400Hz Neutral to Control Unit "A" Pin 17.) all were linked together
115V 400Hz Neutral to Control Unit "B" Pin 13.)

(3) 28V D.C. Positive to Control Unit "A" Pin 12)
28V D.C. Positive to Control Unit "B" Pin 12) all linked together
28V D.C. Positive to Crew Warning Unit Pin 6)

(4) 28V D.C. Negative to Control Unit "A" Pin 29)
28V D.C. Negative to Control Unit "B" Pin 29) linked together

2.4.3. TESTS FOR TRANSIENT ACCEPTANCE TO A.C. POWER LEADS

The following step functions were selected from figure No 3 of MIL-STD-704A for category "B" equipment.

The step functions were applied with the system operating in the "STANDBY" mode and then repeated whilst in the "FIRE" mode. The results of the tests are shown below :-

STANDBY MODE			
BASIS OF STEP FUNCTION	APPLIED VOLTAGE	TIME PERIOD	REMARKS
Limit No 1	180V	0.1SEC.	Not Susceptible
1	149	1.0	
2	160	0.04	
3	60	0.05	
3	Zero	0.05	
4	102	7.0	
4	Zero	7.0	
5	140	0.02	
6	74 458	0.02	

OPERATE MODE			
BASIS OF STEP FUNCTION	APPLIED VOLTAGE	TIME PERIOD	REMARKS
Limit No 1	180	0.1 SEC.	Not Susceptible
1	148	1.0	Not Susceptible
2	160	0.04	Not Susceptible
3	60	0.05	Both "FIRE" lights extinguish and relight on resumption of the normal 115V supply
3	Zero	0.05	
4	102	7.0	Not Susceptible
4	Zero	7.0	"FIRE" lights extinguish and fire detect fail become illuminated and extinguish after the transient and fire lights re-illuminated.
5	140	0.02	Not Susceptible
6	74	0.02	Occasional R.H. fire lamp
			extinguishes but re-illuminates.

2.4.4. TESTS FOR TRANSIENT ACCEPTANCE TO D.C. POWER LEADS.

The following step functions were selected from figure No 9 of MIL-STD-704A for category "B" equipment.

CYCLE No	APPLIED VOLTAGE	TIME PERIOD
1	80	0.06 SEC
2	49	1.0
3	70	0.02
4	60	0.015
5	11	0.03
6	8	0.05
7	Zero	7.0
8	22.5	7.0

The system was set to operate in the standby mode. Test cycle No 1 was then applied. This application caused both the "FIRE" lamps to fail.

The unit was examined by the customer's representative and it was found that R36,(150 1/2 W resistor),in both common logic boards had gone open circuit.

These components were then replaced with type W21 resistors,(150Ω 2.5W), resistors. The unit then operated satisfactorily.

The step functions were then applied with the system operating in the "STANDBY"mode and then repeated with the system operating in the "FIRE" mode.

The results of the tests are shown below :-

Cycle No	REMARKS	
	STANDBY MODE	OPERATE MODE
1 2 3 4	Not Susceptible	Fire lamps momentarily bright...
5 6 7	not susceptible	Both "FIRE" lamps extinguish then relight following the transient.
8		Both lamps dim for 7 seconds

2.5. TESTS WITH IMPORTED VOLTAGE SPIKES ON D.C. POWER LINES

Paragraph 5.2.3. and figure 17 of MIL-STD-704A calls up an imported voltage spike test for d.c. powered equipment. The spike is to be in the form of a single half sine wave of base width 10μS. The spike is to be superimposed onto the d.c. power leads. The amplitude of the test spikes is to be ± 600 volts when at open circuit. The source impedance of the spike generator is to be 50Ω.

The +600v spikes were applied at a rate of one pulse per second to the d.c. lines. The system was then operated for a five minute period in each of the two operating modes. This procedure was then repeated with the polarity of the test spikes reversed.

When on line then the amplitude of the positive going spikes was attenuated to +400 volts. The negatively imposed spikes were unattenuated.

The Fire Detection System operated normally throughout the application of these tests.

2.6. TEST CS06 - CONDUCTED SUSCEPTIBILITY - POWER LEADS

2.6.1. TEST CS06 - D.C. POWER LEADS

The spikes were parallel injected onto the d.c. power lines by means of the pulse generator type AE7746. The base width of the spikes was 10μS and the amplitude was set to twice the line voltage of 28 volts which = 56 volts. The total peak voltages in the case of positive and negative superimposed voltage spikes was +84 and -28 volts respectively with respect to the zero voltage level. The spike repetition frequency was set to ten pulses per second and the test was applied for a period of five minutes in each polarity for each operating mode.

The Fire Detection System operated normally throughout the application of the tests.

2.6.2. TEST CS06 - A.C. POWER LEADS

The spikes were parallel injected onto the a.c. power lines by means of the pulse generator type AE7746. The base width of the spikes was 10μS and the amplitude of the spikes was set to 100 volts. The spike repetition frequency was set to ten pulses per second.

The spikes were synchronised to the power line frequency and positioned at each 90° position for a period of five minutes. The spike was also positioned from 0 to 360° of the power line waveform.

Positive and negative spikes were applied for equal time periods at all the phase positions listed above. The total time that the spikes were applied was not less than 30 minutes. This test was performed in the standby mode and then repeated for the fire mode.

The fire Detection System operated normally throughout the application of the tests.

2.7. TEST RS02 - SUSCEPTIBILITY TO MAGNETICALLY INDUCED FIELDS

2.7.1. CABLE TEST

Magnetic Induction field tests were performed on all the cable bundles interconnecting the system. This bundle was wrapped with wire along the length of the bundle at a rate of two turns per metre length. The following tests were then applied :-

Test (a) A current of 20 Amps r.m.s. 400Hz was passed through the wire.

Test (b) Voltage spikes were applied to the wire at a rate of 10 pulses per second. The spikes were of a base width of 10μS and peak voltage 400 volts when measured across a 5Ω impedance in series with the wire wrappings.

Test (a) was applied for a period of 5 minutes with the Fire Detection system operating in the standby mode. This procedure was then repeated with the system operating in the fire mode.

Test (b) was then applied to the wire whilst the system was operated for a period of 5 minutes in each of the two operating modes. These tests were then repeated with the polarity of the spikes reversed. The Fire Detection System operated normally throughout the application of the tests.

2.7.2. CASE TEST

2.7.2.1 CASE TEST - CREW WARNING UNIT

The case of the Crew Warning Unit was wrapped with three turns of wire as shown in figure (a) of Appendix "A" of this report. Tests (a) and (b) as detailed in paragraph 2.7.1. of this report were then applied to the wire wrapping.

2.7.2.2. CASE TEST - CONTROL UNIT TYPE 53513-203

The case of the control unit was wrapped with wire in a similar manner as described in para. 2.7.2.1. of this report. Tests (a) and (b) were then applied.

2.7.2.3. CASE TEST - CONTROL UNIT TYPE 53813-204

The case of the control unit was wrapped with wire in a similar manner as described in para. 2.7.2.1. of this report. Tests (a) and (b) were then applied.

RESULTS

The Fire Detection System operated normally throughout the application of the tests.

3. CONCLUSIONS

The system was damaged by the application of the 80 volt transient acceptance requirement of MIL-STD-704A. This was due to the failure of R36,(1/2 W resistors).

Components R36 were replaced by type W22,(2.5 Watt resistors) and the acceptance tests were then satisfactorily completed. The system then operated normally throughout the tests and was not susceptible in any way to the test applications.

4. RECOMMENDATIONS

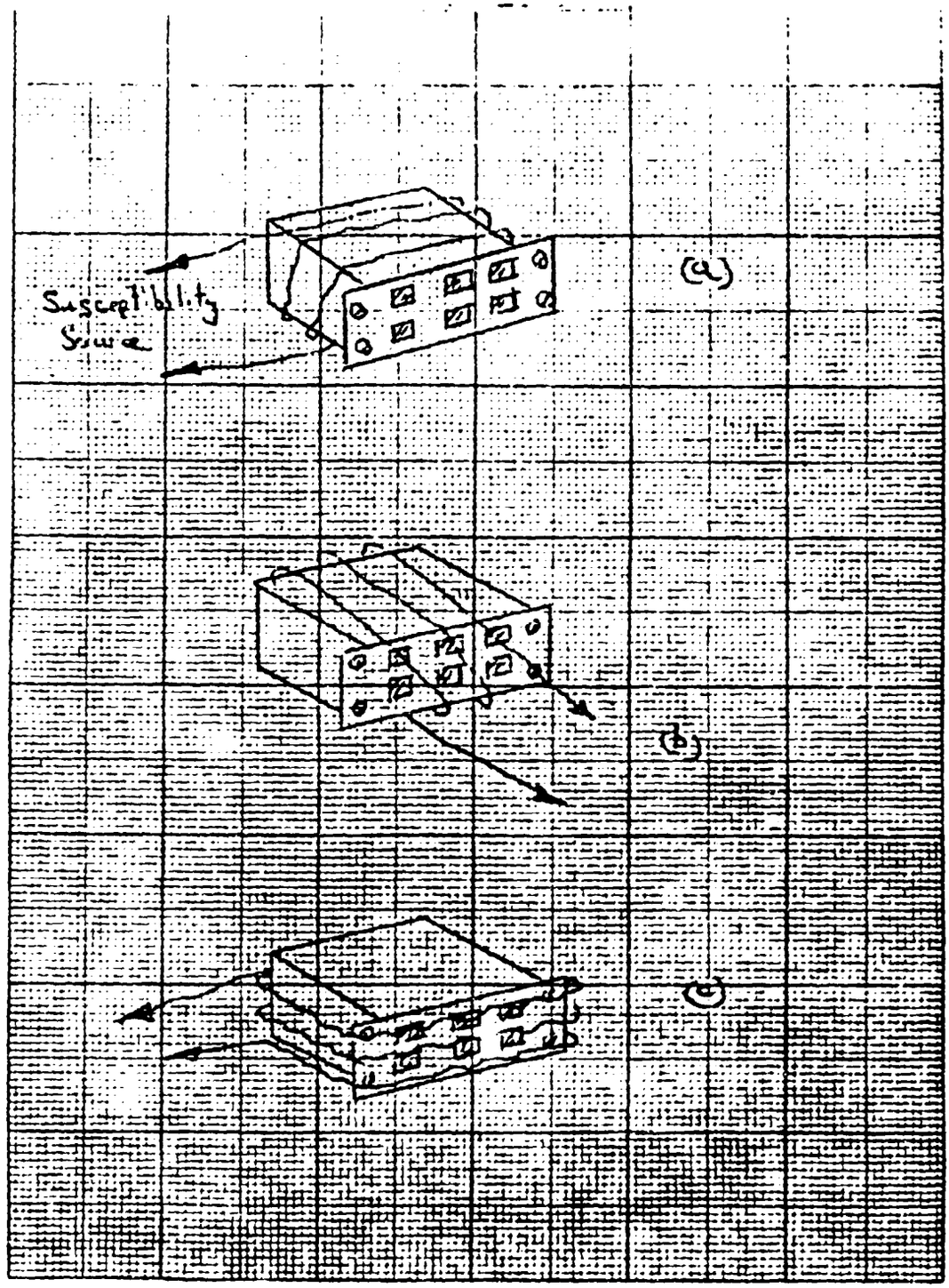
That the build standard of the units incorporates the modification to uprate R36 to a type W22 component.

Signed S. Mitchell.

(C. Mitchell)

463

Approved K Blakeman



WIRE WRAP TEST RS02

CREW WARNING UNIT

LUCAS AEROSPACE LTD. ELECTRICAL GROUP, BRADFORD ENGLAND	Date [redacted]. SHEET 9 OF 9 SHEETS Report No. AED/EMV/80550 Figure Sheet No.

GAF 18789/77

APPENDIX B-4

VIBRATION TEST RESULTS

EMI ELECTRONICS LIMITED, TEST HOUSE, FELTHAM

TEST REPORT No. ENV 2739
ETR 4605

TESTING AUTHORITY	DATE 25-6-80
E.M.I., ENVIRONMENTS DEPARTMENT D.G. of Q.A., APPROVAL NUMBER 10891	C.A.A. APPROVAL NUMBER AI/2925/49
TEST REQUESTED BY:	NAME: A.J.Littlewood Graviner Ltd., ADDRESS: Colnbrook, SLOUGH.Berks.
TEST CLASSIFICATION:	Type approval
CUSTOMER'S ORDER NUMBER:	84808
CONTRACT NUMBER:	-
PROJECT:	249
E.M.I. REFERENCE NUMBER:	31401/38800
EQUIPMENT TESTED:	NAME: Computer Control Units Crew Warning Unit and SERIAL NOS: Single and Dual Detector Heads DRAWING NOS:
TESTED TO:	SPECIFICATION: See Report LIST:
CONCESSIONS: AUTHORITY AND REFERENCE:	
PREVIOUS SUBMISSIONS:	
REPORTED BY:	P.A.Brackley
APPROVED BY: 467	
QUALITY OFFICER IN CHARGE, E.Q.D.	

SHEET 2 OF 13

Test Gear used in conjunction with Report No: ENV 2739

ITEM	TYPE	SERIAL NO.	PLANT NO.
Vibrator	Ling 805	201	1111/P
Amplifier	Ling HPA 8KW	158	111A/P
Oscillator	B & K 1025	338320	756/P
Voltmeter	B & K 2416	373223	800/P
Freq.Counter	Venner	H9866	93/P
Auto Strobe	EMI A53	-	565/P
Oscilloscope	Telequipment D43R	5299	242G/P
	Amplifier A	-	242S/P
	Amplifier A	-	242T/P
Charge Amplifier	Birchall CA-01-2CH	38	677/P
Stroboscope	EMI Type 6	-	582/P
Accelerometer	Bruel & Kjaer 4369	614776	
Accelerometer	Endevco 224C	TC80	
Digital Random Noise Control	Gen.Rad. TDV32PR	-	845/P
Teletype	Data Dynamics	-	845A/P

1. INTRODUCTION

The following units were subjected to the following tests in accordance with the following specifications:

1.1 Crew Warning Unit

Crew Warning Unit Type 53813-202 Serial No.101 was subjected to a resonance search in accordance with Specification MIL-STD-810C; method 514.2-2:Procedure 1;Curve J of Fig.514.2-2 and to random vibration in accordance with Specification MIL-STD-810C: method 514.2; Procedure 1A;Figs.514-2-11A and 514-2-2A.

1.2 Computer Control Unit

The units, Computer Control Unit Type 53813-203,Serial No.100 (System A): Type 53813-204;Serial No.100 (System B with Battery Card), were subjected to a resonance search in accordance with Specification MIL-STD-810C, Method 514.2.2; Procedure 1, curve J of Fig.514.2.2: to random vibration in accordance with Specification MIL-STD-810C, Method 515.2 Procedure 1A, Figs.515-2-11A and 514-2-2A, agd to an acceleration test in accordance with Specification MIL-STD-810C, Method 513-2 Procedure 1.

1.3 Single and Dual Detector Heads

The units, single detector head type 53521-012-and dual detector head type 53522-011, were both subjected to a resonance search in accordance with Specification MIL-STD-810C Method 514.2 Procedure 1, Curve G of Fig.514.2-2, and to random vibration in accordance with Specification MIL-STD-810C Method 514.2 Procedure 1A, Fig.514.2-11A and 514.2-2A.

2. TEST DETAILS

2.1 Crew Warning Unit

Resonance Search

The unit was subjected to a resonance search in each of the three mutually perpendicular axes at the following frequencies and levels:

5 - 14 Hz @ 0.10" peak-to-peak

14 - 23 Hz At 1g

23 - 52 Hz @ 0.036" peak-to-peak

52 - 2000 Hz @ 5g

2.1 Crew Warning Unit (cont)

Random Vibration

The unit was subjected to random vibration at the levels shown in Fig.1 for one hour's duration in each of the three mutually perpendicular axes.

2.2 Computer Control Unit

Resonance Search

The units were subjected to a resonance search in each of the three mutually perpendicular axes at the following frequencies and levels:

5 - 14 Hz @ 0.10" peak-to-peak
14 - 23 Hz @ 1g
23 - 52 Hz @ 0.036" peak-to-peak
52 - 2000 Hz @ 5g

Random Vibration

The units were subjected to random vibration at the levels shown in Fig.1 for one hour's duration in each of the three mutually perpendicular axes.

Accleration

The units, System A and System B (with Battery Card), were subjected to a constant acceleration of 25.5g for 60 seconds in each direction of each of the three mutually perpendicular axes.

2.3 Single and Dual Detector Heads

Resonance Search

The units were subjected to a resonance search in each of the three mutually perpendicular axes at the following frequencies and levels:

5 - 14 Hz @ 0.10" peak-to-peak
14 - 23 Hz at 1g
23 - 90 Hz @ 0.036" peak-to-peak
90 - 2000 Hz at 15g

Random Vibration

The units were subjected to random vibration at the levels shown in Fig.2 for one hour's duration in each of the three mutually perpendicular axes.

3. TEST RESULTS

3.1 Crew Warning Unit

Resonance Search

AXIS 1
A monitor accelerometer was mounted in positions A and B (see Fig.4)

Monitor Accelerometer position	Peak Resonance Frequency (Hz)	Input Level (g)	Output Level (g)
A	134	5	22
B	142	5	37

AXIS 2
Between 115 Hz and 150 Hz, there was a resonance in the direction of the vibration, and between 150 Hz and 196 Hz there was a resonance normal to the direction of vibration.

AXIS 3
There was a resonance between 130 Hz and 234 Hz with a peak at 198 Hz.

Random Vibration

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit functioned satisfactorily during the tests in Axes 2 and 3. After 35 minutes in Axis 1, the left-hand fire warning light failed to operate. The unit was opened by the visiting Engineer, and a broken lead was found at the soldered joint by the lamp. This was repaired and a tie rap was added to hold the cable and reduce movement. The test was then repeated and the unit found to function satisfactorily.

3.2 Computer Control Unit

Resonance Search - System A

Axis	Frequency (Hz)	Comments
1 (normal to mounting face)	180-202	End board moving at bottom.
	263	Brown loom lead. (No resonance could be seen at the main cards)
2 (normal to long side)	73-94	Cards moving slightly together.
	94-112	Outside card moving more.
	112-118	Peak (especially outside cards)
	140-162	All cards moving, not together.
	162-200	All cards moving slightly
	255	Wire moving inside loom.
3 (normal to short side)	40-50	Slight movement of end card.
	50-57	All cards moving slightly.
	85-113	All cards moving slightly.
	110	Middle card moving.
	115-140	Single card moving strongly.
	140-155	Single card moving very strongly.
	155	Peak movement of single card.
	155-174	Single card moving strongly.
	174-200	Single card moving slightly.

Random Vibration - System A

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Acceleration - System A

The unit was functionally tested after each direction and axis before commencing with the following run. After the test was completed, the unit was returned to Graviners Ltd., when full functional tests were carried out. The visiting Engineer holds these functional test results.

Resonance Search - System B (without Battery Card)

Axis	Frequency (Hz)	Comments
1 (normal to mounting face)	150-160	Outside board moving very slightly.
	160-180	Inside and outside boards moving very slightly.
	180-200	Inside boards moving very slightly.
	208-230	End board moving.
2 (normal to long side)	93-118	Boards moving slightly together.
	118-123	Outside boards moving strongly. Other boards moving less strongly.
	123	Peak movement.
	123-160	Slight movement of boards.
	160-197	Very slight movement of boards.
3 (normal to short side)	48-53	End card moving slightly.
	53-55	Middle and end cards moving slightly.
	55-60	All cards moving slightly.
	75	Single card moving slightly.

Random Vibration - System B (without Battery Card)

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Resonance Search - System B (without Battery Card)

Axis	Frequency (Hz)	Comments
1 (normal to mounting face)	150-190	Two support cards moving.
	195	Battery and its support card moving slightly.
	300 - 320	Support board moving.
	320	All long cards moving slightly.
	450-529	Front short board moving.
2 (normal to long side)	65-109	Long cards moving together in the direction of vibration.
	109	Peak movement.
	135	Peak movement of outside card.
	140-200	All cards (except Battery Card) moving.
	451	Outside card moving slightly. (No appreciable resonances could be seen of the Battery Card and its support card).
3 (normal to short side)	170-202	Short board moving.
	202-214	Peak movement of short board.
	270-340	Outside long card moving slightly.
	370-390	Short board moving slightly.

Random Vibration - System B (with Battery Card)

The unit was functionally tested by the visiting Graviner Engineer throughout the test. The unit was found to function satisfactorily in all axes.

Acceleration - System B (with Battery Card)

The unit was functionally tested after each direction and axis before commencing with the following run.

After the test was completed, the unit was returned to Graviners Ltd. where full functional tests were carried out.

The visiting Engineer holds these functional test results.

3.3 Single and Dual Detector Heads

Resonance Search

In Axis 1 (see Fig.5), there was rocking on the mountings of the dual detector head between 368 and 385 Hx. There was no detectable resonances of the single detector head in this axis.

In Axis 2, the single head was rocking on its mountings, especially between 651 and 687Hz.

In Axis 3, the dual detector head was rocking on its mounts at 597 Hz.

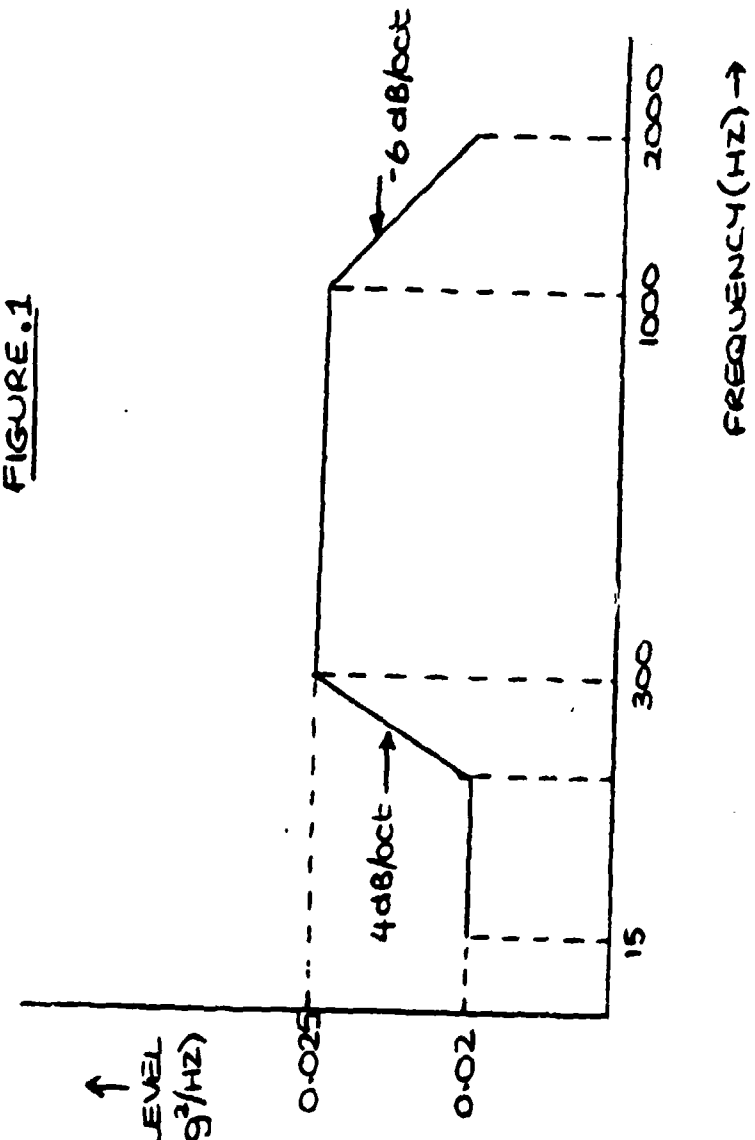
Random Vibration

The units were functionally tested by the visiting Graviner Engineer throughout the test. Both units were found to function satisfactorily in all axes.

Reported by: P.A.Brackley
Report No: ENV 2739
ETR 4605

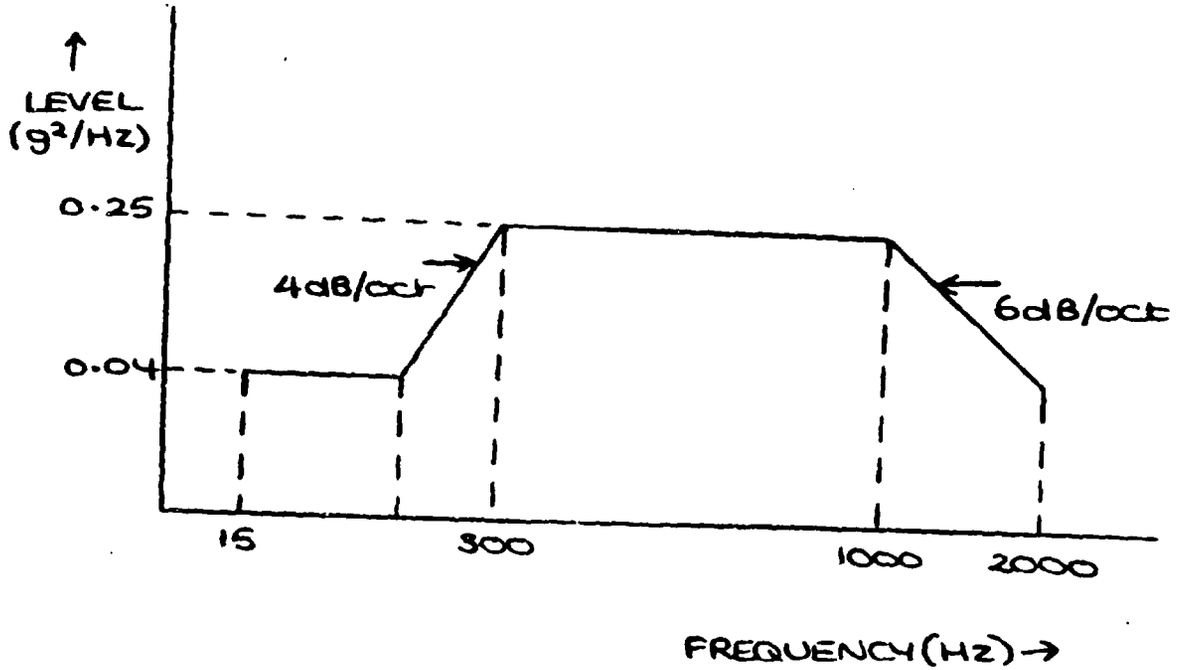
Copies to: Mr.R.Leney
Quality Service Department
Graviner Ltd.,
Colnbrook
SLOUGH.Bucks (4)

FIGURE.1



RANDOM VIBRATION LEVELS FOR CREW WARNING UNIT AND FOR COMPUTER CONTROL UNITS.

FIGURE 2

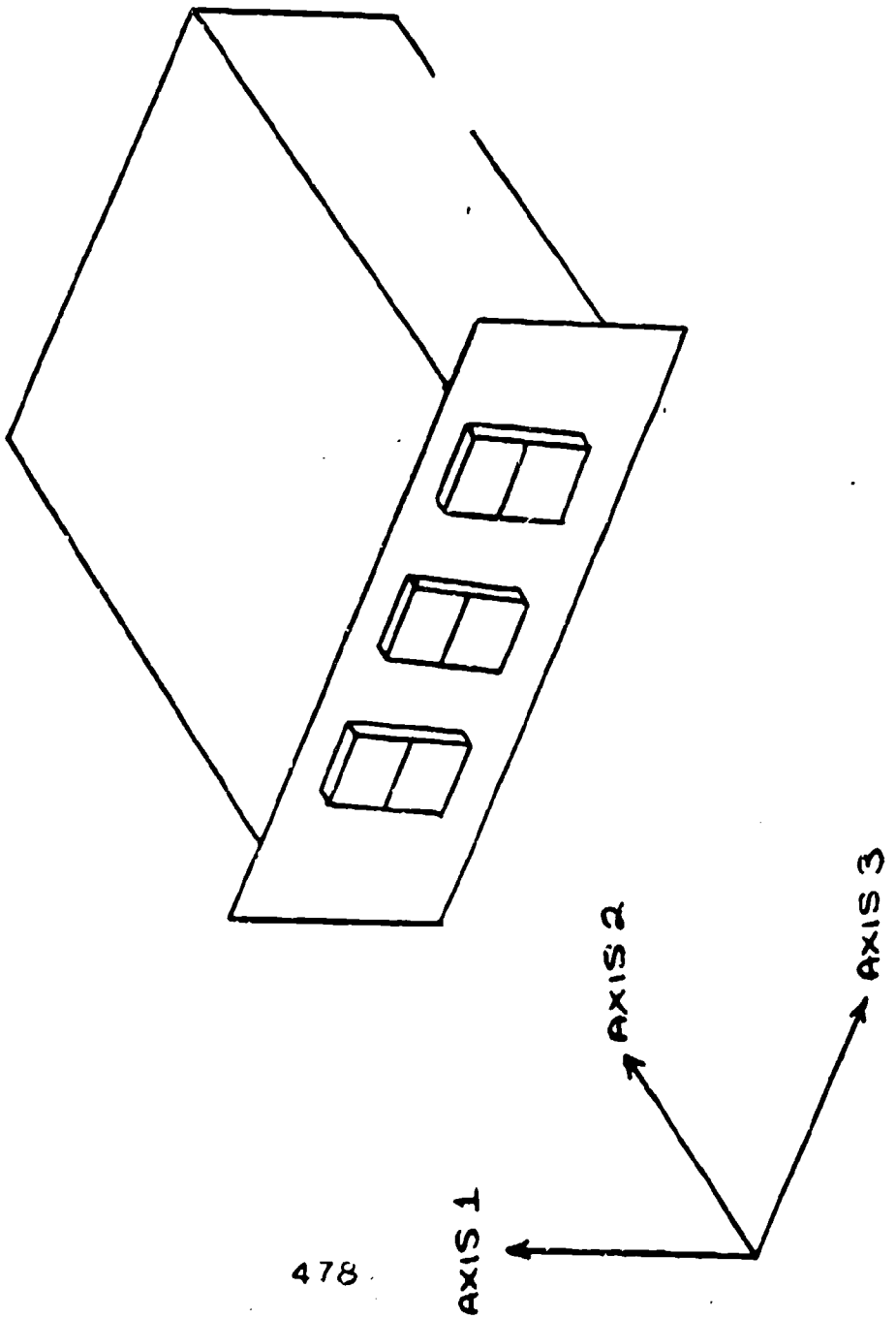


RANDOM VIBRATION LEVELS FOR

SINGLE AND DUAL DETECTOR HEADS

FIGURE 3

AXES OF CREW WARNING UNIT



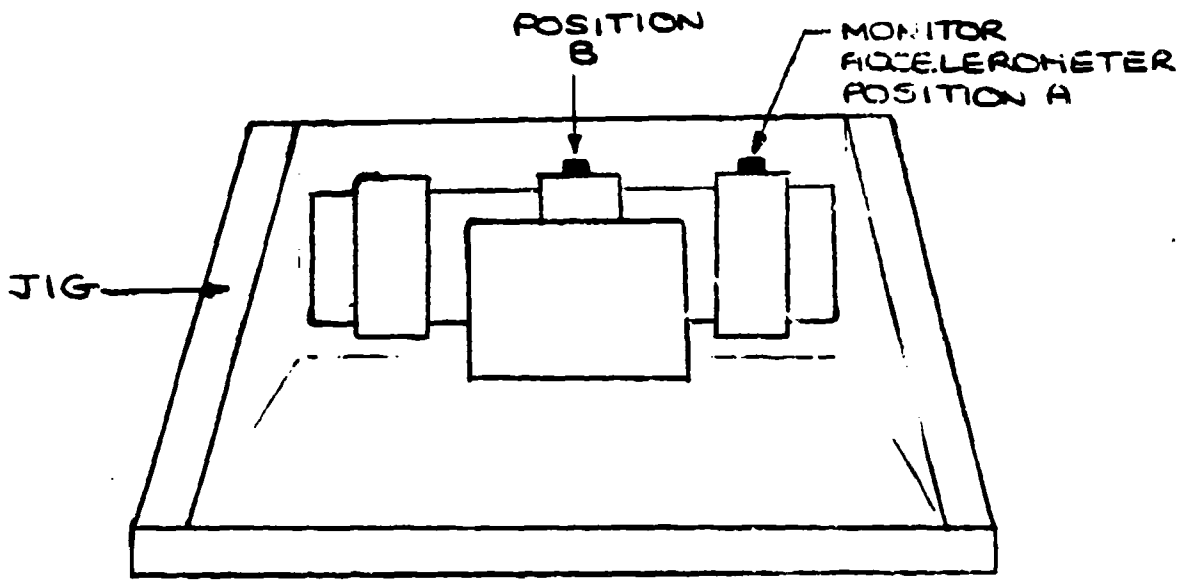


FIGURE 4 – POSITIONS OF MONITOR ACCELEROMETER DURING THE RESONANCE SEARCH FOR CREW WARNING UNIT

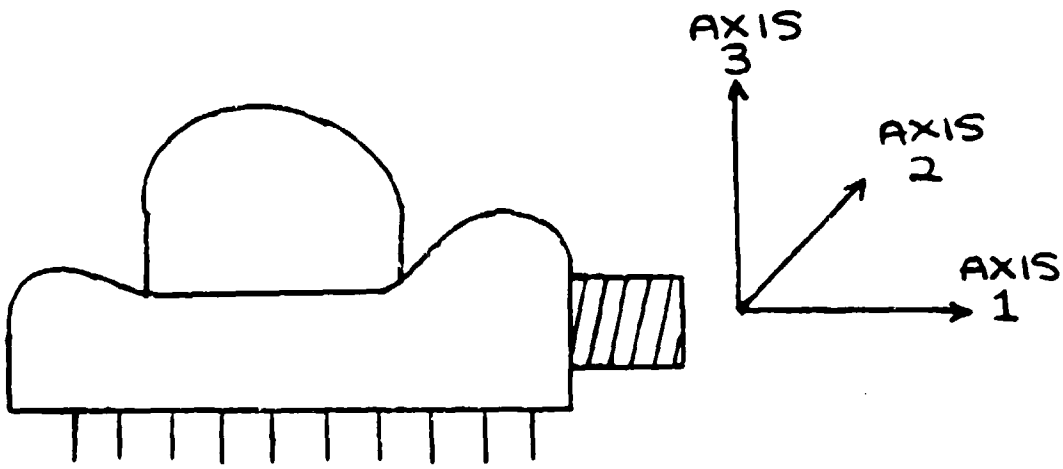


FIGURE 5 - AXES OF SINGLE AND DUAL DETECTOR HEADS

British Aerospace
DYNAMICS GROUP
HATFIELD, HERTFORDSHIRE
ENGLAND

TEST HOUSE CERTIFICATE

A W 117
Issued under Ministry of Defence Quality Assurance Board Approval No. 12718

Date 4 August 1980

To: Messrs. Graviner Ltd.
Address Poyle Road, Colnbrook, Slough, SL3 0HB

Contract No. IND 85604
Sub Contract Order No.
Works Order No. AA 0942/00000

Environmental Engineering LABORATORY

Report No. E T R 2297

Item Tested:— U-V Detector Head Type 53522-011 Serial Number XP 1 and XP7.
Type 53521-012 Serial Number XP1 and XP5

Test Specification:— MIL-STD-810, Method 515, Procedure 1, Category B.

Result Summary:— The four units were subjected to an acoustic environment to MIL-STD-810 for a duration of 30 minutes. The Overall Sound Pressure Level, measured using three Bruel & Kjaer Type 4135 microphones, was 154 dB re. 2×10^{-5} N/m^2.

Prepared by: (Sgd.) W.E. Betts
(Printed) W E Betts

Certified that the tests have been carried out to the requirements of the Director-General of Quality Assurance

Certified: (Sgd.) W B. Roberts
(Printed) W B Roberts
for and on behalf of
British Aerospace
Dynamics Group

Distribution.
Customer
Customer's Chief Inspector
N O Q D
Chief Inspector. Hatfield
Head of Test House Laboratory
Files 480

Form No. 6844

APPENDIX B-5

TEST CERTIFICATE ETR 2297

ACOUSTIC VIBRATION

British Aerospace
DYNAMICS GROUP
HATFIELD, HERTFORDSHIRE
ENGLAND

TEST HOUSE CERTIFICATE

A W 117
Issued under Ministry of Defence Quality Assurance Board Approval No. 12718

Date 4 August 1980

To: Messrs. Graviner Ltd.
Address Poyle Road, Colnbrook,
Slough, SL3 OHB

Contract No. IND 85604
Sub Contract Order No.
Works Order No. AA 0942/00000

Environmental Engineering LABORATORY

Report No. E T R 2297

Item Tested:— U-V Detector Head Type 53522-011 Serial Number XP 4 and XP7.
Type 53521-012 Serial Number XP1 and XP5

Test Specification:— MIL-STD-810, Method 515, Procedure 1, Category B.

Result Summary:— The four units were subjected to an acoustic environment to MIL-STD-810 for a duration of 30 minutes. The Overall Sound Pressure Level, measured using three Bruel & Kjaer Type 4135 microphones, was 154 dB re. 2×10^{-5} N/m^2.

Prepared by: (Sgd.) W E Betts
(Printed) W E Betts

Certified that the tests have been carried out to the requirements of the Director-General of Quality Assurance

Certified: (Sgd.) W B Roberts
(Printed) W B Roberts
for and on behalf of
British Aerospace
Dynamics Group

Distribution
Customer
Customer's Chief Inspector
N Q Q D
Chief Inspector, Hatfield
Head of Test House Laboratory
Files 483

Form No. 6844

APPENDIX B-6

TABLES FOR APPENDIX B

TABLE NO. 1

U.V.A.F.D.S. CREW. WARNING UNIT.

TYPE: 53813-202. SERIAL No. 100

TEST STAGE: At 71°C

Q.5308 PARA. No.	16·0v. D.C. INPUT. VOLTS.	16·0v. D.C. INPUT. m.A.	29·0v. D.C. INPUT. VOLTS.	29·0v. D.C. INPUT. m.A.
4.3.2.		77.3		105.0
4.3.3.		75.5		104.0
4.3.4.		57.2		81.0
4.3.5.		75.9		105.0
4.3.6.	1.7	8.5	1.4	15.0
4.3.7.	1.2	8.5	1.4	15.0
4.3.8	1.7	8.5	1.4	15.0
4.3.9.	1.7	8.5	1.4	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Meg			

TABLE NO. 2

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: at -54°C

Q.5308 PARA. No.	16.0V. D.C. INPUT.		29.0V D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		73.0		105.0
4.3.3.		70.5		100.0
4.3.4.		71.0		100.0
4.3.5.		69.5		102.0
4.3.6.	1.7	7.9	1.5	15.0
4.3.7.	1.7	7.9	1.5	15.0
4.3.8	1.7	7.9	1.5	15.0
4.3.9	1.7	7.9	1.5	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Meg.			

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'A'

TYPE: 53813-203. TEST STAGE: at -54°C

SERIAL No. 101 TABLE No. 3

PARA No.	0.5309 RESULTS							
4.1.	0.29 OHMS.							
	124v. 420Hz A.C.				102v 380Hz. 16.0v.D.C.			
	M1.	M2.	M3.	M4.	M1.	M2.	M3.	M4.
4.2.1.			111	0.95			78	0.8
4.2.2.	110	112	68	0	85	89	34	0
4.4.	95	101	56	0	75	80	30	0
4.5.	111	118	228	0	87	91	136	0
	102v. 380Hz. 16.0V.D.C.				124v 420Hz A.C.			
	SIDE 1 (VOLTS)		SIDE 2. (VOLTS)		SIDE 1 (VOLTS)		SIDE 2 (VOLTS)	
	4.7.3.	5.44	4.7.4.	5.51	4.7.3.	5.45	4.7.4.	5.52
	4.7.5.	297	4.7.6.	296	4.7.4.	312	4.7.6.	310
4.8.3.1.	t= 0.53 SECS.							
4.8.3.2.	t= 0.52 SECS.							
4.8.6.2.	SIDE 1. 0.337 SECS.		SIDE 2. 0.338 SECS.					
4.8.6.3.	SIDE 1. 0.837 SECS.		SIDE 2. 0.169 SECS.					
4.8.9.	SIDE 1. 14.82 SECS.		SIDE 2. 0.1675 SECS.					
4.8.10.	SIDE 1. 14.82 SECS.		SIDE 2. 0.1676 SECS.					
4.9.2.	5.47 VOLTS.							
4.9.3.	4.39 VOLTS.							
4.9.4.	114.9 VOLTS.							
4.9.5.	114.9 VOLTS.							
4.10.2.	27.6 VOLTS.							
4.10.3.	27.6 VOLTS.							
4.10.4.	27.8 VOLTS.							
4.10.5.	27.8 VOLTS.							
4.11.3.2.	t1= 0.38 SECS.		t2= 0.38 SECS.					
4.11.3.3.	t= 0.38 SECS.		t= 0.38 SECS.					
4.11.3.5.	t= 1.9 SECS.							
4.11.6.	M4. 0.33 mA.							
4.11.7.1.	GRUTIL V4							
4.12.10.2.	t= 1.15 SECS.							
4.12.10.3.	t= 11.8 SECS.							

TABLE NO. 4

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'B'

TYPE: 53813-204. SERIAL No. 101 WITHOUT BATTERY

TEST STAGE: at -54°C

PARA. No.	RESULTS.					
4.1.	0.04 OHMS.					
	124v 420 Hz. A.C.			102v 380 Hz. 160 v D.C.		
	M2.	M3.	M4.	M2.	M3.	M4.
4.2.1.		111	0.8		78	0.7
4.2.2.	110	53	0	90	28	0
4.4.	99	50	0	78	28	0
4.5.	116	220	0	90	135	0
	SIDE 2. VOLTS.					
	102v 380 Hz 160 D.C.			124v 420 Hz. A.C.		
4.7.3.	5.97			5.98		
4.7.4.	297			320		
4.8.3.1.	t= 0.52 SECS.					
4.8.6.2.	t= 0.335 SECS.					
4.8.6.3.	t= 0.168 SECS.					
4.8.8.	t= 14.77 SECS.					
4.8.9.	t= 0.1675 SECS.					
4.9.2.	4.77 VOLTS.					
4.9.3.	114.9 VOLTS.					
4.10.2.	27.67 VOLTS.					
4.10.3.	27.67 VOLTS.					
4.10.4.	27.82 VOLTS.					
4.10.5.	27.82 VOLTS.					
4.11.3.2.	t1= 0.38 SECS.			t2= 0.38 SECS.		
4.11.6.	M4. 0.75 mA.					
4.11.7.	GRATIL. V4.					
4.12.6.2.	t= 0.84 SECS.					
4.12.6.3.	t= 0.68 SECS.					
APPENDIX B.	4.7 VOLTS.			4.9 VOLTS.		

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'A'

Type: 53813-203. TEST STAGE: After Acceleration

SERIAL No. 100 TABLE NO. 5

PARA No.	0.5309 RESULTS							
4.1.	0.06 OHMS.							
	124 V. 420 Hz A.C.				102 V 380 Hz. 16·0 V.D.C.			
	M1.	M2.	M3.	M4.	M1.	M2.	M3.	M4.
4.2.1.			111	5.6			78	2.05
4.2.2.	106	115	68	0	73	90	34	0
4.4.	96	101	58	0	73	80	31	0
4.5.	110	120	225	0	88	94	137	0
	102 V. 380 Hz. 16·0 V.D.C.				124 V 420 Hz A.C.			
	SIDE 1 (VOLTS)		SIDE 2. (VOLTS)		SIDE 1 (VOLTS)		SIDE 2 (VOLTS)	
	4.7.3.	5.68	4.7.4.	5.62	4.7.3.	5.69	4.7.4.	5.53
	4.7.5.	294	4.7.6.	297	4.7.4.	313	4.7.6.	317
4.8.3.1.	t_0 0.55 SECS.							
4.8.3.2.	t_0 0.52 SECS.							
4.8.6.2.	SIDE 1. 0.338 SECS.		SIDE 2. 0.338 SECS.					
4.8.6.3.	SIDE 1. 0.168 SECS.		SIDE 2. 0.168 SECS.					
4.8.9.	SIDE 1. 14.85 SECS.		SIDE 2. 14.82 SECS.					
4.8.10.	SIDE 1. 0.1675 SECS.		SIDE 2. 0.1676 SECS.					
4.9.2.	5.71 VOLTS.							
4.9.3.	4.45 VOLTS.							
4.9.4.	114.9 VOLTS.							
4.9.5.	114.9 VOLTS.							
4.10.2.	27.7 VOLTS.							
4.10.3.	27.7 VOLTS.							
4.10.4.	27.8 VOLTS.							
4.10.5.	27.8 VOLTS.							
4.11.3.2.	t_1 = 0.38 SECS.		t_2 = 0.38 SECS.					
4.11.3.3.	t_0 0.38 SECS.		t_0 0.38 SECS.					
4.11.3.5.	t_2 2.3 SECS.							
4.11.6.	M4. 4.1 mA.							
4.11.7.1.	GRUTIL V4.							
4.12.10.2.	t_0 1.16 SECS.							
4.12.10.3.	t_0 [illegible] SECS.							

491

491

TABLE NO.6

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'B'

TYPE: 53813-204. SERIAL No. 100 WITHOUT BATTERY

TEST STAGE: After Acceleration

Q.5310

PARA. No.	RESULTS.					
4.1.	0.05 OHMS.					
	124v 420 Hz. A.C.			102v 380 Hz. 160 D.C.		
	M2.	M3.	M4.	M2.	M3.	M4.
4.2.1.		111	3.25		68	1.55
4.2.2.	120	60	0	91	30	0
4.4.	106	51	0	80	29	0
4.5.	121	226	0	95	136	0
	SIDE 1. VOLTS.					
	102v 380 Hz 160 D.C.			124v 420 Hz. A.C.		
4.7.3.	5.63			5.64		
4.7.4.	297			320		
4.8.3.1.	t_v 0.47 SECS.					
4.8.6.2.	t_s 0.335 SECS.					
4.8.6.3.	t_o 0.168 SECS.					
4.8.8.	t_s 14.77 SECS.					
4.8.9.	t_s 0.1675 SECS.					
4.9.2.	4.36 VOLTS.					
4.9.3.	114.8 VOLTS.					
4.10.2.	27.6 VOLTS.					
4.10.3.	27.6 VOLTS.					
4.10.4.	27.8 VOLTS.					
4.10.5.	27.8 VOLTS.					
4.11.3.2.	t_{R1} 0.38 SECS.			t_{R2} 0.38 SECS.		
4.11.6.	M4. 4.0 mA.					
4.11.7.	GRUTIL. V4.					
4.12.6.2.	t_o 0.84 SECS.					
4.12.6.3.	t_s 0.67 SECS.					
APPENDIX B.	4.7 VOLTS.			4.9 VOLTS.		

TABLE NO. 7

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: After Acceleration

Q.5308 PARA. No.	16.0v. D.C. INPUT. VOLTS.	m.A.	29.0v. D.C. INPUT. VOLTS.	m.A.
4.3.2.		72.5		100.0
4.3.3.		71.0		100.0
4.3.4.		79.5 •		110.0
4.3.5.		71.0		100.0
4.3.6.	1.7	7.95	1.5	14.5
4.3.7.	1.7	7.95	1.5	14.5
4.3.8	1.7	7.9	1.5	14.5
4.3.9.	1.7	7.95	1.5	14.5
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TABLE NO.8

Detector Type 53522-011, S/No. XP6 and Detector Type 53521-012 S/No.ENV.

After Acceleration

Calibration Count 75 p.p.s.

Detector Unit Type	53522-011		53521-012
	XP6		ENV
	A	B	
Q.5304 Para.			
5.2	76.0	77.4	97.0
5.2.1.	28.0	30.0	34.0
5.3.	0	0	0
5.4.1.	SATISFACTORY		SATISFACTORY
5.4.2.	SATISFACTORY		SATISFACTORY
5.5	>20 Megohms		>20 Megohms

TABLE NO. 9

U.V.A.F.D.S. CREW. WARNING UNIT.

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: After Resonance Search

Q5308 PARA. No.	16.0v. D.C. INPUT.		29.0v. D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		71.0		100.0
4.3.3.		70.0		100.0
4.3.4.		71.0		100.0
4.3.5.		69.5		100.0
4.3.6.	1.7	7.9	1.4	14.5
4.3.7.	1.7	7.9	1.5	14.0
4.3.8	1.7	7.9	1.5	14.0
4.3.9.	1.7	8.0	1.5	14.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TABLE NO. 10

U.V.A.F.D.S. CREW. WARNING UNIT.

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 1.

Q5308 PARA. No.	16.0V. D.C. INPUT.		29.0V. D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		71.0		100.0
4.3.3.		66.0		100.0
4.3.4.		70.0		100.0
4.3.5.		69.0		100.0
4.3.6.	1.7	8.0	1.5	15.0
4.3.7.	1.7	8.0	1.5	15.0
4.3.8	1.7	8.0	1.5	15.0
4.3.9.	1.7	8.0	1.5	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TABLE NO. 11

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 2.

Q.5308 PARA. No.	16.0v. D.C. INPUT.		29.0v. D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		70.0		100.0
4.3.3.		49.0		95.0
4.3.4.		52.0		100.0
4.3.5.		67.0		100.0
4.3.6.	1.4	8.0	1.5	15.0
4.3.7.	1.7	8.0	1.5	15.0
4.3.8	1.7	8.0	1.5	15.0
4.3.9.	1.7	8.0	1.5	15.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TABLE NO. 12

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: During Random Vibration - Plane 3.

Q.5308 PARA. No.	16.0v. D.C. INPUT.		29.0v. D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		69.0		100.0
4.3.3.		66.0		98.0
4.3.4.		69.0		100.0
4.3.5.		68.0		99.0
4.3.6.	1.7	7.9	1.5	14.5
4.3.7.	1.7	7.9	1.5	14.5
4.3.8	1.7	7.9	1.5	14.5
4.3.9.	1.7	7.9	1.5	14.5
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	> 20 Meg.			

TABLE NO. 13

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: After Vibration Testing.

Q.5308 PARA. No.	16·0v. D.C. INPUT. VOLTS.	16·0v. D.C. INPUT. m.A.	29·0v. D.C. INPUT. VOLTS.	29·0v. D.C. INPUT. m.A.
4.3.2.		73.0		100.0
4.3.3.		72.0		100.0
4.3.4.		80.0		110.0
4.3.5.		71.0		100.0
4.3.6.	1.7	8.1	1.5	14.5
4.3.7.	1.7	8.1	1.5	14.2
4.3.8	1.7	8.1	1.5	14.2
4.3.9.	1.7	8.1	1.5	14.0
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Meg.			

TABLE NO. 14

System A, C.C.U. Type 53813-203 S/No. 100

Testing during random vibration was limited to response and reset time tests.

	Response Time	Reset Time
Plane 3	1.18 seconds	0.876 second
	1.30 seconds	0.931 second
	1.15 seconds	0.902 second
Plane 2	1.30 seconds	0.936 second
	1.20 seconds	0.885 second
	1.18 seconds	0.984 second
Plane 1	1.16 seconds	0.90 second
	1.25 seconds	0.98 second
	1.26 seconds	0.93 second

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'A'

TYPE: 53813-203. TEST STAGE: After Vibration Testing

SERIAL No. 100

TABLE NO. 15

PARA No.	0.5309 RESULTS.							
4.1.	0.16 OHMS.							
	124v. 420Hz A.C.				102v 380Hz. 16·0v.D.C.			
	M1.	M2.	M3.	M4.	M1.	M2.	M3.	M4.
4.2.1.			111	5.1			76	2.1
4.2.2.	109	117	63	0	85	92	33	0
4.4.	97	102	56	0	75	80	30	0
4.5.	111	118	222	0	88	105	135	0
	102v 380Hz. 16·0 V.D.C.				124v 420Hz A.C.			
	SIDE 1 (VOLTS)		SIDE 2. (VOLTS)		SIDE 1 (VOLTS)		SIDE 2 (VOLTS)	
	4.7.3.	5.65	4.7.4.	5.49	4.7.3.	5.55	4.7.4.	5.49
	4.7.5.	295	4.7.6.	297	4.7.4.	312	4.7.6.	315
4.8.3.1.	t_0 0.55 SECS.							
4.8.3.2.	t_0 0.54 SECS.							
4.8.6.2.	SIDE 1. 0.3378 SECS. SIDE 2. 0.3378 SECS.							
4.8.6.3.	SIDE 1. 0.1683 SECS. SIDE 2. 0.1683 SECS.							
4.8.9.	SIDE 1. 14.84 SECS. SIDE 2. 14.82 SECS.							
4.8.10.	SIDE 1. 0.1676 SECS. SIDE 2. 0.1676 SECS.							
4.9.2.	5.68 VOLTS.							
4.9.3.	4.42 VOLTS.							
4.9.4.	115.0 VOLTS.							
4.9.5.	115.0 VOLTS.							
4.10.2.	27.6 VOLTS.							
4.10.3.	27.6 VOLTS.							
4.10.4.	27.7 VOLTS.							
4.10.5.	27.7 VOLTS.							
4.11.3.2.	t_1 = 0.39 SECS. t_2 = 0.39 SECS.							
4.11.3.3.	t_0 0.39 SECS. t_0 0.39 SECS.							
4.11.3.5.	t_2 2.3 SECS.							
4.11.6.	M4. 3.7 mA.							
4.11.7.1.	GRUTIL V4.							
4.12.10.2.	t_2 1.2 SECS.							
4.12.10.3.	t_0 0.3 SECS.							

TABLE NO. 16

System B, C.C.U. Type 53813-204 S/No. 100

Without Battery Card

Testing during random vibration was limited to response and reset times.

	Response Time	Reset Time
Plane 3	0.964 second	0.955 second
	1.09 seconds	0.845 second
	0.964 second	0.905 second
Plane 2	1.02 seconds	0.903 second
	0.938 second	0.957 second
	0.775 second	0.898 second
Plane 1	0.857 second	0.933 second
	0.885 second	0.839 second
	0.932 second	0.915 second

TABLE NO. 17

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'B'

TYPE: 53813-204. SERIAL No. WITHOUT BATTERY

TEST STAGE: After Vibration Testing

Q.5310

PARA. No.	RESULTS.					
4.1.	OHMS.					
	124v 420 Hz. A.C.			102v 380 Hz. 16·0 v D.C.		
	M2.	M3.	M4.	M2.	M3.	M4.
4.2.1.		88	3.3		60	1.6
4.2.2.	119	60	0	100	30	0
4.4.	108	51	0	83	28	0
4.5.	120	192	0	95	119	0
	SIDE 1. VOLTS.					
	102v 380 Hz 16·0 D.C.			124v 420 Hz. A.C.		
4.7.3.	5.6			5.		
4.7.4.	296			319		
4.8.3.1.	t = 0.49 SECS.					
4.8.6.2.	t = 0.335 SECS.					
4.8.6.3.	t = 0.168 SECS.					
4.8.8.	t = 14.77 SECS.					
4.8.9.	t = 0.1677 SECS.					
4.9.2.	4.35 VOLTS.					
4.9.3.	114.8 VOLTS.					
4.10.2.	27.7 VOLTS.					
4.10.3.	27.7 VOLTS.					
4.10.4.	27.8 VOLTS.					
4.10.5.	22.8 VOLTS.					
4.11.3.2.	t1 = 0.38 SECS.			t2 = 0.38 SECS.		
4.11.6.	M4. 1.7 mA.					
4.11.7.	GRUTIL. V4.					
4.12.6.2.	t = 0.81 SECS.					
4.12.6.3.	t = 0.68 SECS.					
APPENDIX B.	4.7 VOLTS.			4.9 VOLTS.		

TABLE NO. 18

System B. C.C.U. Type 53813-204 S/No. 100

With Battery Card

Testing during random vibration was limited to response and reset times.

	Response Time	Reset Time
Plane 3	0.940 second	0.953 second
	1.08 seconds	0.907 second
	0.996 second	0.926 second
Plane 2	1.06 seconds	0.627 second
	0.858 second	0.661 second
	0.924 second	0.889 second
Plane 1	0.952 second	0.620 second
	1.100 seconds	0.921 second
	0.911 second	0.971 second

TABLE NO. 19

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'B'

TYPE: 53813-204. SERIAL No. 100 WITHOUT BATTERY

TEST STAGE: After vibration testing

Q.5310

PARA. No.	RESULTS.					
4.1.	0.04 OHMS.					
	124v 420 Hz. A.C.			102v 380 Hz 160 V D.C.		
	M2.	M3.	M4.	M2.	M3.	M4.
4.2.1.		90	3.4		60	1.8
4.2.2.	120	58	0	102	30	0
4.4.	106	50	0	94	28	0
4.5.	121	213	0	108	130	0
	SIDE 1. VOLTS.					
	102v 380 Hz 160 D.C.			124v 420 Hz. A.C.		
4.7.3.	5.6			5.61		
4.7.4.	297.1			318.2		
4.8.3.1.	t = 0.48 SECS.					
4.8.6.2.	t = 0.316 SECS.					
4.8.6.3.	t = 0.168 SECS.					
4.8.8.	t = 14.22 SECS.					
4.8.9.	t = 0.1675 SECS.					
4.9.2.	4.35 VOLTS.					
4.9.3.	114.91 VOLTS.					
4.10.2.	27.59 VOLTS.					
4.10.3.	27.59 VOLTS.					
4.10.4.	27.59 VOLTS.					
4.10.5.	27.59 VOLTS.					
4.11.3.2.	tf = 0.38 SECS.			tR = 0.38 SECS.		
4.11.6.	M4. 3.4 mA.					
4.11.7.	GRUTIL. V4.					
4.12.6.2.	t = 0.85 SECS.					
4.12.6.3.	t = 0.67 SECS.					
APPENDIX B. 4.7	VOLTS.			4.9 VOLTS.		

TABLE NO.20

Detector Unit Type 53522-011 S/No.XP6 and Detector Type 53521-012 S/No. ENV.

Testing during random vibration was limited to response and reset times.

	53522-011 (XP6)		53521-012 (ENV)	
	Response Time	Reset Time	Response Time	Reset Time
Plane 3	0.903 second	0.942 sec.	1.06 seconds	0.895 sec.
	0.847 second	0.947 sec.	0.790 second	0.953 sec.
	1.20 seconds	0.975 sec.	1.16 seconds	0.931 sec.
Plane 2	1.19 seconds	0.963 sec.	0.929 second	0.631 sec.
	0.968 second	0.949 sec.	1.03 seconds	0.979 sec.
	1.2 seconds	1.13 sec.	0.996 second	0.931 sec.
Plane 1	1.03 seconds	0.989 sec.	1.08 seconds	0.928 sec.
	1.17 seconds	0.839 sec.	1.09 seconds	0.878 sec.
	0.770 second	0.870 sec.	0.934 second	0.870 sec.

After Vibration testing. Calibration count 64.5 p.p.s.

	53522-011(XP6)		53521-012(ENV)
	A	B	
Q.5304 Para.			
5.2.	66.74	69.79	90.51
5.2.1.	33.1	28.0	41.6
5.5.	>20 Megohms		>20 Megohms

TABLE NO.21

Detectors Type 53522-011, S/Nos. XP1 and XP7 and Detectors Type 53521-012, S/Nos. XP1 and XP5.

Before acoustic vibration. Calibration count 52 p.p.s.

Detector Type	53522-011				53521-012	
	XP1		XP7		XP1	XP5
Q.5304 Para.	A	B	A	B		
5.2.	79	65	54	73	68	58
5.2.1.	46	28	25	29	36	56
5.3.	0	0	0	0	0	0
5.4.1.	SATISFACTORY				SATISFACTORY	
5.4.2.	SATISFACTORY				SATISFACTORY	
5.5.	>20 Megohms				>20 Megohms	

After acoustic vibration. Calibration count 59 p.p.s.

Detector Type	53522-011				53521-012	
	XP1		XP7		XP1	XP5
Q.5304 Para.	A	B	A	B		
5.2.	76	63	49	70	70	55
5.2.1.	40	28	32	31	35	24
5.3.	0	0	0	0	0	0
5.4.1.	SATISFACTORY				SATISFACTORY	
5.4.2.	SATISFACTORY				SATISFACTORY	
5.5	>20 Megohms				>20 Megohms	

TABLE NO.22

U.V.A.F.D.S. CREW. WARNING UNIT

TYPE: 53813-202. SERIAL No. 101

TEST. STAGE: After Shock Testing

Q.5308 PARA. No.	16.0V. D.C. INPUT.		29.0V. D.C. INPUT.	
	VOLTS.	m.A.	VOLTS.	m.A.
4.3.2.		71.0		100.0
4.3.3.		70.5		100.0
4.3.4.		78.5		110.0
4.3.5.		69.5		100.0
4.3.6.	1.7	7.8	1.5	14.5
4.3.7.	1.7	7.8	1.5	14.5
4.3.8	1.7	7.8	1.5	14.3
4.3.9.	1.7	7.8	1.5	14.3
4.6.0			N/A	
4.6.1.			N/A	
4.6.2.			N/A	
4.6.3.			N/A	
INSUL.	>20 Meg.			

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'A'

TYPE: 53813-203. TEST STAGE: After Shock Testing

SERIAL No. 100 TABLE NO. 23

PARA No.	Q.5309 RESULTS							
4.1.	0.07 OHMS.							
	124v. 420Hz A.C.				102v 380Hz 16·0v.D.C.			
	M1.	M2.	M3.	M4.	M1.	M2.	M3.	M4.
4.2.1.			110	5.3			75	2.1
4.2.2.	110	115	68	0	85	100	35	0
4.	95	100	54	0	75	78	30	0
4.5.	110	120	220	0	86	95	136	0
	102v. 380Hz, 16·0V. D.C.				124v 420Hz A.C.			
	SIDE 1 (VOLTS)		SIDE 2. (VOLTS)		SIDE 1 (VOLTS)		SIDE 2 (VOLTS)	
	4.7.3.	5.69	4.7.4.	294	4.7.3.	5.7	4.7.4.	314
	4.7.5.	5.53	4.7.6.	297	4.7.4.	5.53	4.7.6.	317
4.8.3.1.	t= 0.56 SECS.							
4.8.3.2.	t= 0.54 SECS.							
4.8.6.2.	SIDE 1. 0.337 SECS.		SIDE 2. 0.337 SECS.					
4.8.6.3.	SIDE 1. 0.173 SECS.		SIDE 2. 0.173 SECS.					
4.8.9.	SIDE 1. 14.82 SECS.		SIDE 2. 14.86 SECS.					
4.8.10.	SIDE 1. 0.172 SECS.		SIDE 2. 0.172 SECS.					
4.9.2.	5.54 VOLTS.							
4.9.3.	4.51 VOLTS.							
4.9.4.	114.9 VOLTS.							
4.9.5.	114.9 VOLTS.							
4.10.2.	27.7 VOLTS.							
4.10.3.	27.7 VOLTS.							
4.10.4.	27.9 VOLTS.							
4.10.5.	27.9 VOLTS.							
4.11.3.2.	t1= 0.38 SECS.		t2= 0.38 SECS.					
4.11.3.3.	t= 0.38 SECS.		t= 0.38 SECS.					
4.11.3.5.	t= 2.3 SECS.							
4.11.6.	M4. 3.8 mA.							
4.11.7.1.	GRUTIL V4.							
4.12.10.2.	t= 1.15 SECS.							
4.12.10.3.	t= 0.68 SECS.							

TABLE NO. 24

U.V.A.F.D.S. COMPUTOR CONTROL UNIT SYSTEM 'B'

TYPE: 53813-204. SERIAL No. 100 WITH [redacted] BATTERY

TEST STAGE: After Shock Testing

Q.5310

PARA. No.	RESULTS.					
4.1.	0.03 OHMS.					
	124v 420 Hz. A.C.			102v 380 Hz. 16.0v D.C.		
	M2.	M3.	M4.	M2.	M3.	M4.
4.2.1.		88	5.6		60	2.0
4.2.2.	120	55	0	90	28	0
4.4.	105	48	0	80	25	0
4.5.	128	187	0	95	112	0
	SIDE 1. VOLTS.					
	102v 380 Hz 16.0 D.C.			124v 420 Hz. A.C.		
4.7.3.	5.68			5.60		
4.7.4.	296			321		
4.8.3.1.	t= 0.48 SECS.					
4.8.6.2.	t= 0.336 SECS.					
4.8.6.3.	t= 0.173 SECS.					
4.8.8.	t= 14.77 SECS.					
4.8.9.	t= 0.172 SECS.					
4.9.2.	4.4 VOLTS.					
4.9.3.	115 VOLTS.					
4.10.2.	27.7 VOLTS.					
4.10.3.	27.8 VOLTS.					
4.10.4.	27.9 VOLTS.					
4.10.5.	27.9 VOLTS.					
4.11.3.2.	t1= 0.18 SECS.			t2= 0.18 SECS.		
4.11.6.	M4. 3.8 mA.					
4.11.7.	GRUTIL. V4.					
4.12.6.2.	t= 0.81 SECS.					
4.12.6.3.	t= 0.68 SECS.					
APPENDIX B.	4.7 VOLTS.			4.9 VOLTS.		

510

TABLE NO.25

Detector Unit Type 53522-011 S/No. XP6 and Detector Unit Type 53521-012 S/No. ENV

Response and Reset times after shock testing.

53522-011(XP6)		53521-012(ENV)	
Response Time	Reset Time	Response Time	Reset Time
1.28 sec.	1.01 sec.	0.958 sec.	0.825 sec.
1.28 sec.	1.00 sec.	0.782 sec.	0.94 sec.
1.28 sec.	0.82 sec.	0.992 sec.	0.60 sec.