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DESIGN AND OPERATION OF A SIMPLE CIRCUIT USEFUL AS A MODULATOR --ETC(U)
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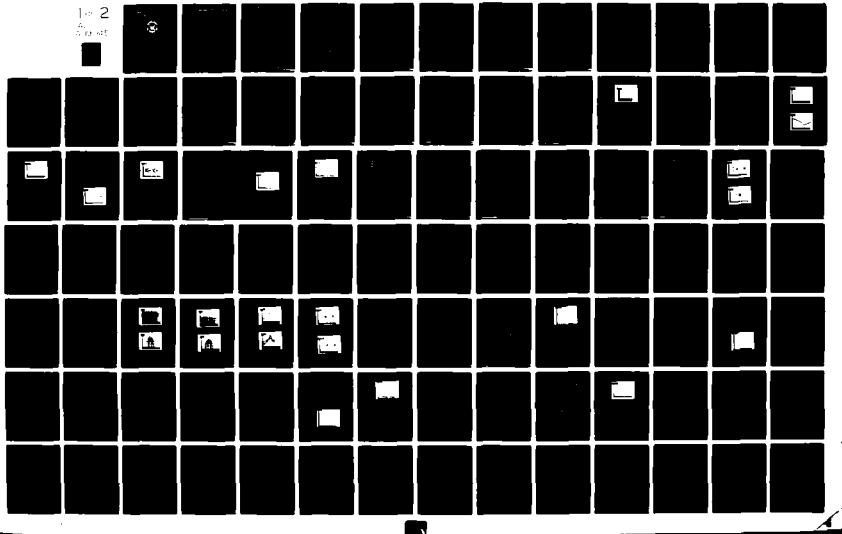

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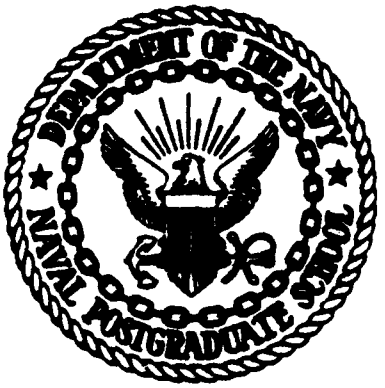

THESIS

Design and Operation of a Simple Circuit Useful as a Modulator to Generate Arbitrary Composite ASK and PSK Carriers

by

Allan M. Maughan

June 1982

Thesis Advisor: Glen A. Myers

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#20 ABSTRACT (CONTINUED)

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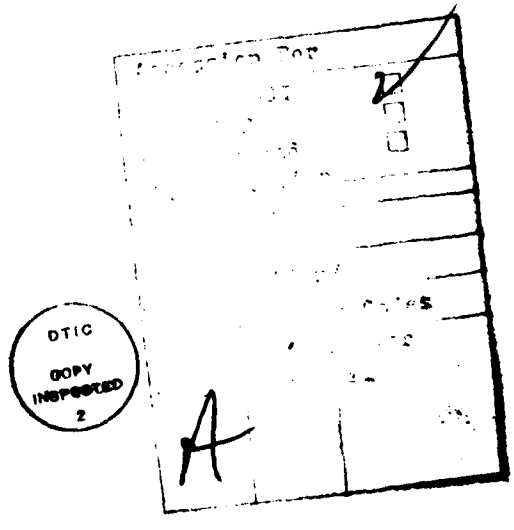
This report considers a simple circuit which can be used to generate any arbitrary composite ASK and PSK carrier. Circuit operation is described and measured performance presented. To determine the noise behavior of particular types of composite ASK and PSK, a demodulator and error counter was built and used. Results are presented as curves of probability of error as a function of demodulator input signal to noise ratio.



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Design and Operation of a Simple Circuit Useful as a Modulator to Generate Arbitrary Composite ASK and PSK Carriers

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ABSTRACT

In radio transmission of binary data, it is often desirable to conserve bandwidth at the expense of signal power. To reduce carrier bandwidth (switching rate), M bits are used to change a parameter of the carrier, so the carrier has 2^M discrete combinations of amplitude, frequency, or phase. A common form of M-ary data transmission is composite amplitude shift keying (ASK) and phase shift keying (PSK).

This report considers a simple circuit which can be used to generate any arbitrary composite ASK and PSK carrier. Circuit operation is described and measured performance presented. To determine the noise behavior of particular types of composite ASK and PSK, a demodulator and error counter was built and used. Results are presented as curves of probability of error as a function of demodulator input signal to noise ratio.

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I. INTRODUCTION

A. OBJECTIVE

The objective of this study is to investigate the operation of an analog multiplexer when used to generate composite amplitude-shift keying (ASK) and phase-shift keying (PSK) carriers, sometimes called quadrature amplitude modulated (QAM) carriers, when the message is digital data. The analog multiplexer modulator is a simple circuit which uses inexpensive components. This circuit also has the potential of improving the noise performance of digital communication systems by conveniently allowing the generation of a variety of modulation formats.

B. BACKGROUND

Digital communication systems assume increasing importance as the use of digital systems expands. As the number of installed or planned digital systems increases, the cost of individual components and the performance of the system become increasingly important.

The noise performance of a digital communication system is largely determined by the modulation scheme since the

modulation scheme determines the decision regions the receiver must resolve. The simplest modulation scheme is binary in which one of two possible signals is transmitted during each signaling interval. Higher data rates can be achieved over a channel of limited bandwidth at the expense of increased transmitter power by increasing the number of possible signals. In an M-ary scheme one of M possible signals is transmitted during each signaling interval. Each of the M possible signals represents a combination of N data bits where $M = 2^N$. Each possible signal is a symbol in the M-ary message and is uniquely identifiable by its amplitude and phase combination.

Typical M-ary modulation schemes transmit particular modulated carriers such as quadrature phase shift keying, 8-phase shift keying, and 16-level composite amplitude and phase shift keying [Ref. 1]. An example of an M-ary scheme is the composite ASK and PSK scheme in which the carrier amplitude may be A or 2A and the phase may be 0° or 180°. Four possible symbols may be transmitted each of which represents two data bits. Figure 1.1 is the block diagram of such a digital modulator. The input is a data stream; the output is a modulated sinusoid. The coding scheme is

arbitrary, but the truth table in Fig. 1.2 is used for this example. Given this coding scheme and the data stream d(t) in Fig. 1.2, the modulator generates the voltage waveform v(t) in Fig. 1.2. Figure 1.3 is the circuit diagram of a 2-phase, 2-amplitude digital modulator.

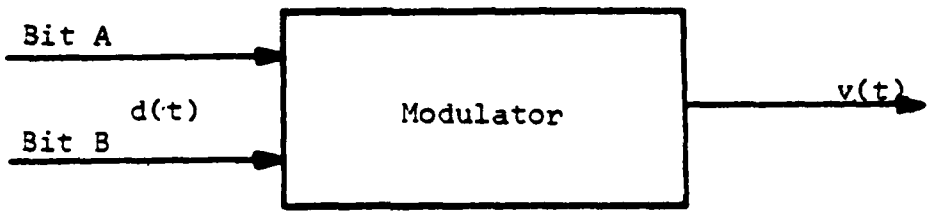
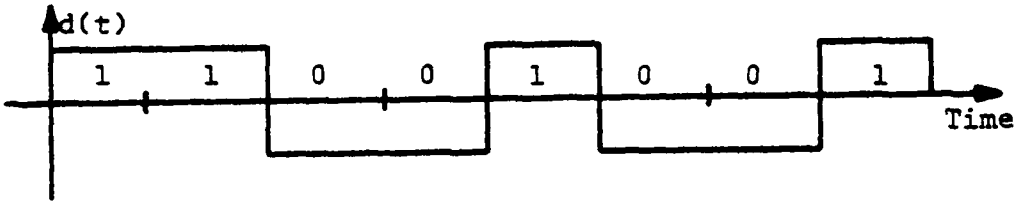


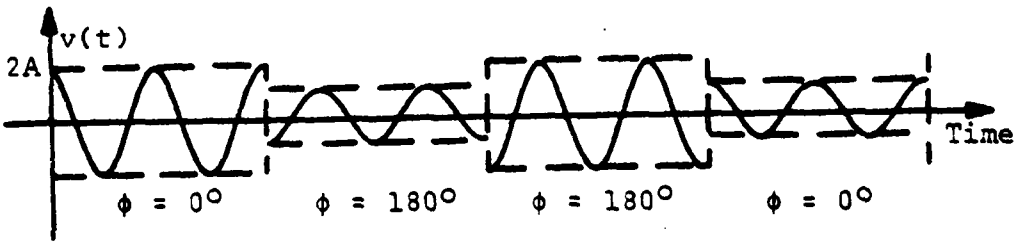
Figure 1.1. 2-Phase, 2-Amplitude Digital Modulator Block Diagram

The typical modulation schemes may not be optimum. The modulator in this study permits the transmission of a carrier having an arbitrary ASK and PSK format. Use of this modulator permits the experimental investigation of the noise performance of any type of ASK, PSK, or combined modulation. Determination of the optimum type of modulation is the subject of future studies.

Data Bit			
A	B	Amplitude	Phase
0	0	A	180°
0	1	A	0°
1	0	2A	180°
1	1	2A	0°



Data Stream



Modulated Carrier Output

Figure 1.2. 2-Phase, 2-Amplitude Modulator Truth Table and Signals

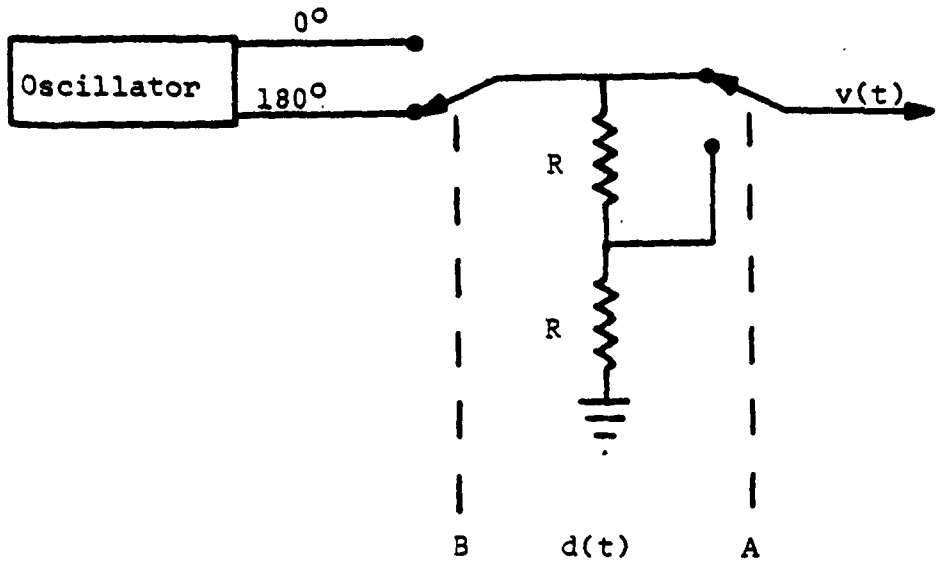


Fig. 1.3. 2-Phase, 2-Amplitude Modulator Circuit Diagram

C. SUMMARY OF RESULTS

The conclusion from this study is that the analog multiplexer is suitable for use as a modulator. These modulators allow the transmitted phasors to be placed arbitrarily. The modulators are simple circuits using inexpensive components.

The following chapters of this report deal with the multiplexer, the modulator, and the experimental method. Chapter II is an examination of the analog multiplexer. Chapter III describes modulators using analog multiplexers. It describes amplitude modulators, phase modulators, and

composite amplitude and phase modulators. The most general modulator circuit described can transmit up to 81 phasors from which 8 may be arbitrarily chosen. Chapter IV describes the system and methods used to test the modulators and gives the results of these tests. Chapter V contains the conclusions and suggests further studies.

II. THE ANALOG MULTIPLEXER

The analog multiplexer used in this investigation is the 4051. No attempt is made to compare its performance with other multiplexers. This chapter considers the suitability of the analog multiplexer as a modulator. The first section discusses required characteristics and the second section the measured performance of this specific multiplexer. The conclusion is that the 4051 is a suitable device at the carrier frequency and switching rates used in this investigation.

A. REQUIRED CHARACTERISTICS

The minimum requirements for a multiplexer to function satisfactorily as a carrier modulator are negligible amplitude distortion, negligible phase shift, negligible OFF current, uniform switch characteristics, a fast switching capability, and negligible undesirable transients.

Amplitude distortion is a function of the ON resistance of the switch. If the ON resistance varies with the applied voltage, the switch will distort an applied sinusoid. In a circuit that sums sinusoids the effects of such amplitude

distortion will appear at the output of the amplitude and phase detectors as increased noise. The ON resistance of a given switch should be constant for the range of applied voltages. Circuit adjustment will be simplified if the set of switches also has uniform ON resistance.

Negligible phase shift in the multiplexer is essential in this phase modulator circuit. Since the switches in the analog multiplexer are electronic, there is potential for phase shift through the integrated circuit. Phase shift will be negligible if it is constant regardless of the applied voltage at the frequency used. Phase shift should be uniform across the set of switches.

The OFF current must be low since any leakage will appear as a phase shift when summed with another sinusoid.

The switch must be fast enough that the sinusoidal carrier can be switched at the data rate.

Undesirable transients must be removable by filtering without affecting the information content of the signal.

B. MEASURED PERFORMANCE

The National Semiconductor Analog Integrated Circuits manual advertises the 4051 as having low ON resistance, typically about 80 ohms, with the switches matched to about

five ohms [Ref. 2]. The OFF resistance is claimed to be high with input leakage currents typically 5 pA. The switching time from control input to signal output is stated as about 400 ns and the time from INHIBIT input to signal output is typically 550 ns. The control lines are TTL compatible with binary address decoding on the chip.

Four switches of a 4051, tested in detail in the circuit of Fig. 2.1, showed the ON resistances in Fig. 2.2. The ON resistance varies less than three ohms for input voltages under 1 V. If other resistors in the circuit are much larger than this three ohm variation, amplitude distortion will be negligible.

The 4051 in the test circuit of Fig. 2.1 showed no discernable phase shift either in superimposed input/output sinusoid displays or in Lissajous patterns. Figure 2.3 is a dynamic display of a Lissajous pattern showing the output from a 4051 with seven inputs grounded and a 30 kHz signal applied to the other. The switching rate is 10 kHz. For the purposes of this modulator, the phase shift across a 4051 can be considered to be zero radians.

The OFF resistance of the 4051 is high, but a precaution must be observed. The input and output circuits must be

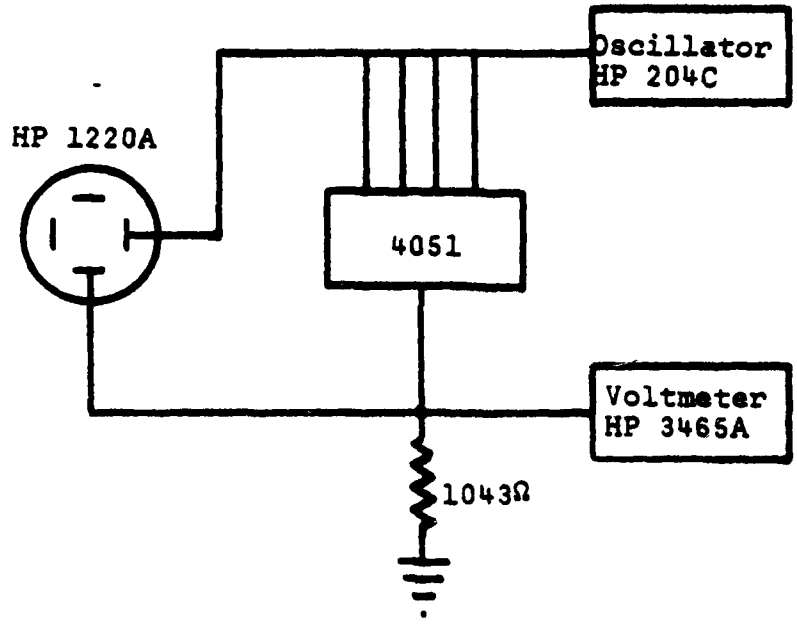


Fig. 2.1. ON Resistance Test Circuit

isolated. With a 0.713 V, 30 kHz sinusoid applied to all eight inputs and with the chip INHIBIT low, the output across a 1063 ohm resistor is 0.628 V. With the INHIBIT high the output is 0.31 mV. By carefully isolating the input and output circuits, this leakage can be reduced to less than 0.2 mV. It is important that this leakage be low for the circuits that follow.

The turn-on and turn-off times as controlled by the chip INHIBIT are 500 ns and 600 ns respectively.

Some transients were observed at the switching times. These transients were removed by the filters discussed in Chapter III.

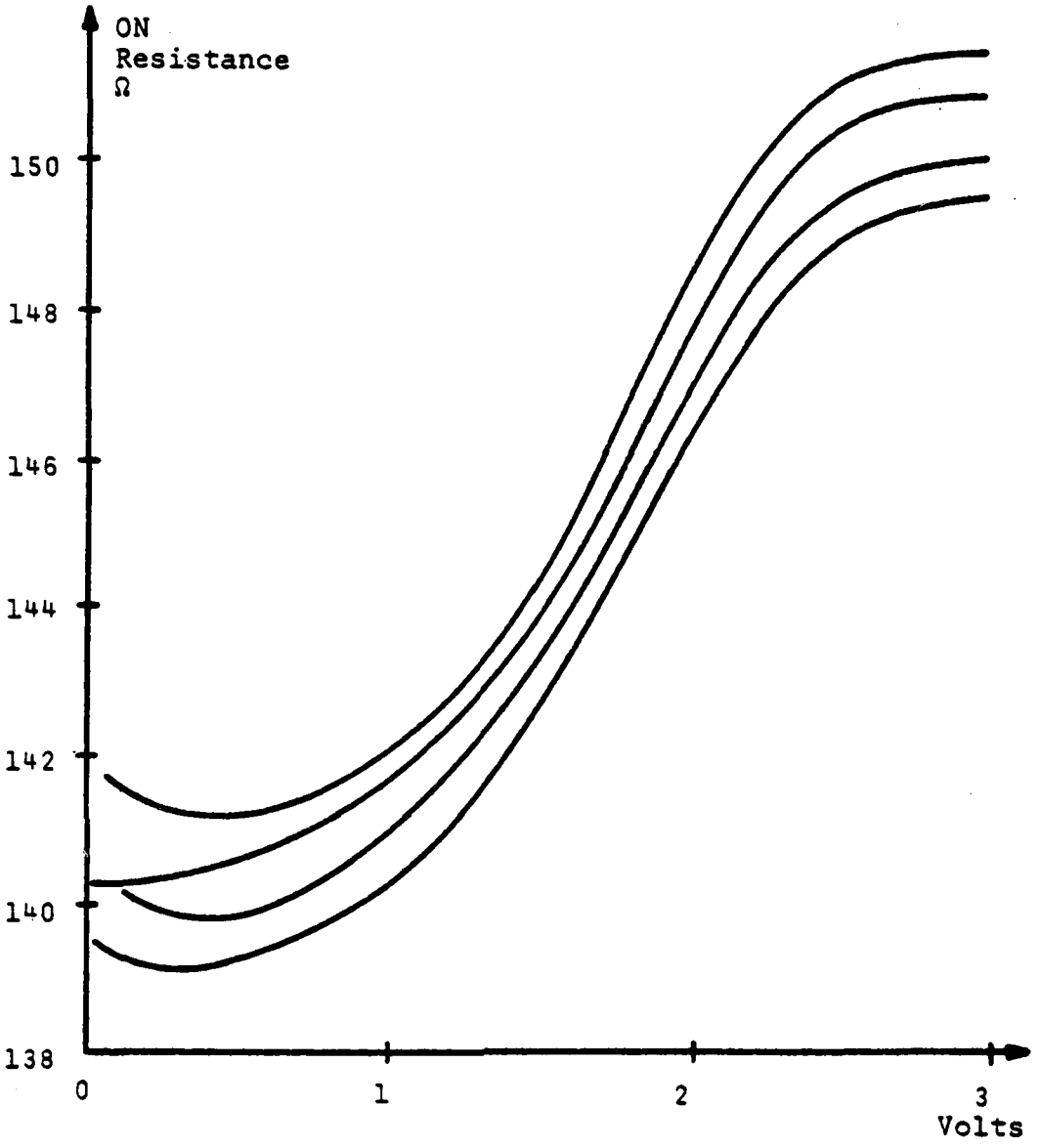


Fig. 2.2. ON Resistance of the 4051 Switches

The 4051 is suitable for use in this investigation. The carrier frequency of 30 kHz can be passed with negligible amplitude distortion and phase shift as long as the

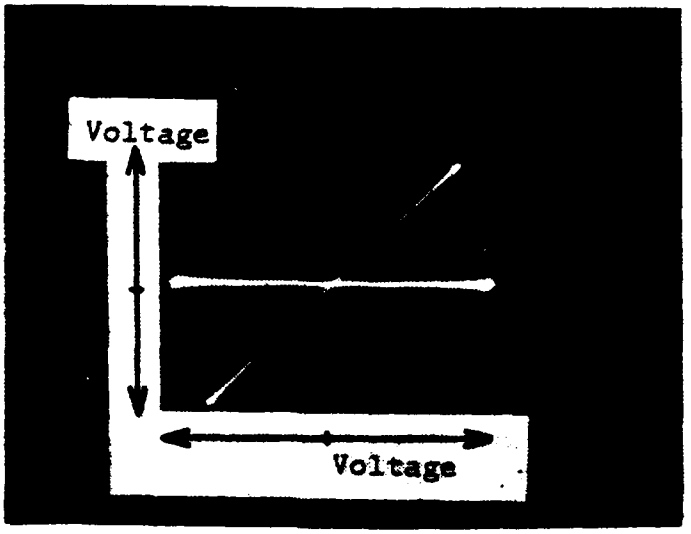


Fig. 2.3. Multiplexer Phase Shift

amplitude is not greater than 1 V. The leakage current is low if input and output circuits are isolated. The switches are quite uniform. The observed transients can be removed by filtering. A data rate of 1 kHz is well within the switching capability of the 4051.

III. ANALOG MULTIPLEXER MODULATOR

The value of an analog multiplexer as a digital modulator lies in its ability to select rapidly among pre-set signals. This chapter describes switching modulators for M-ary phase, amplitude, and composite phase-amplitude systems. The last section describes a general analog multiplexer modulator which can generate up to 81 points on the phase plane from which any eight may be selected arbitrarily using 4-bit control codes on the modulators.

A. PHASE MODULATOR

Phase modulation with an analog multiplexer involves the selection of one of a set of sinusoids with predetermined phase relationships. The diagram in Fig. 3.1 represents a modulator which may transmit any of four sinusoids as selected by the combination of data bits. The use of a single low-cost integrated circuit as a modulator is an obvious advantage over more complex circuits. The ability to pre-set and control precisely the phase shift circuits is also advantageous. A disadvantage of discrete phase switching is the phase discontinuity at switching time.

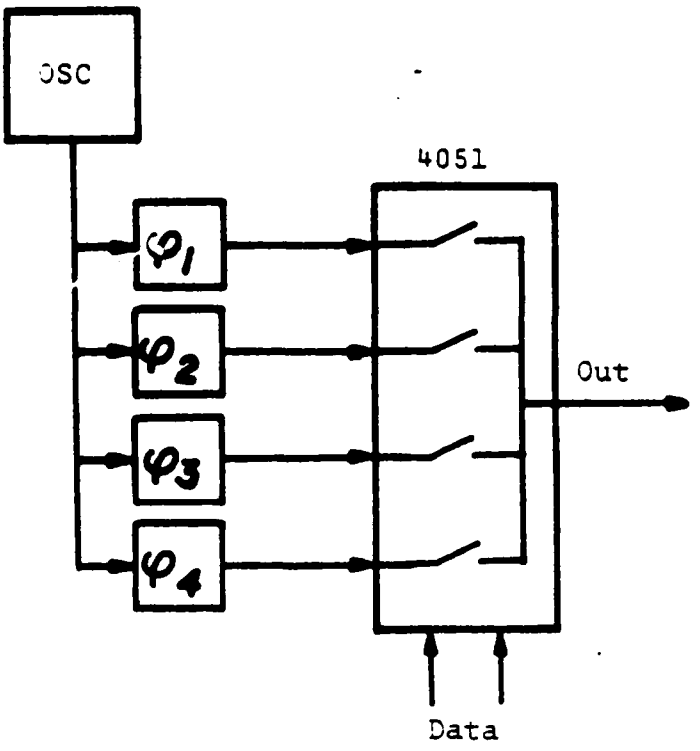


Fig. 3.1. Phase Modulator Block Diagram

The performance of a 4-phase modulator is shown in Fig. 3.2 through Fig. 3.4. Figure 3.2 is a photograph of the output of a 4-phase modulator with a 30 kHz carrier and data switching at 5705 Hz. Figure 3.3 is a photograph of the 16 times expanded display of the transient that occurred at the center of Fig. 3.2. This transient was removed by a bandpass filter. Figure 3.4 is the output of a 4-phase modulator with a 30 kHz carrier and a 10 kHz switching rate shown with the data clock superimposed. The phase transitions are rapid with negligible distortion.

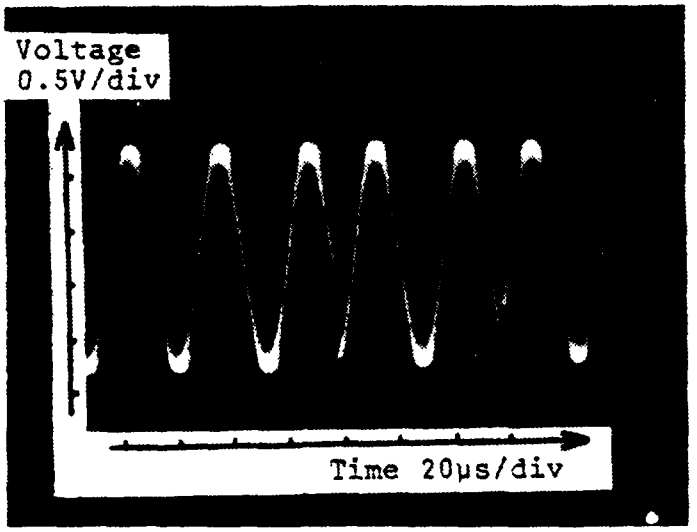


Fig. 3.2. Phase Modulator Output

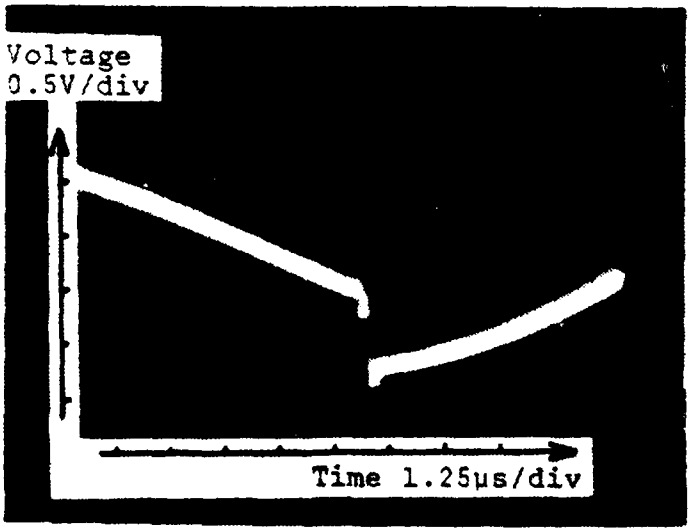


Fig. 3.3. Phase Switching Transient

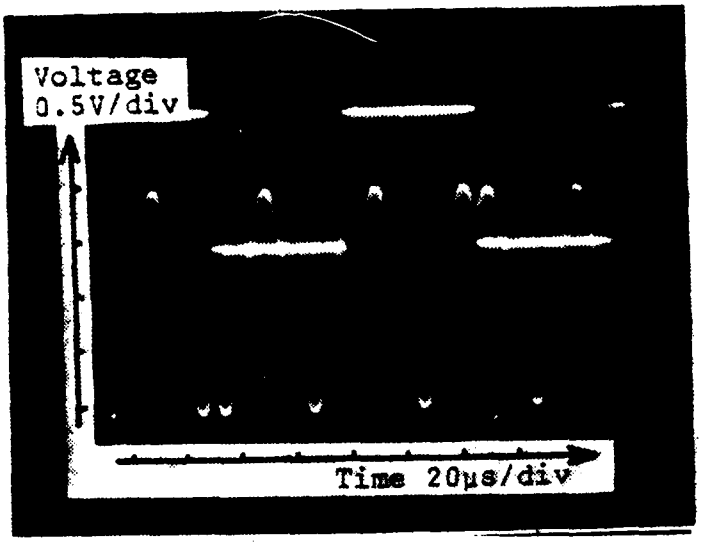


Fig. 3.4. 4-Phase Modulator Output

B. AMPLITUDE MODULATOR

Amplitude modulation may also be done simply with an analog multiplexer. In this case we select a predetermined voltage divider (Fig. 3.5). The data bits select the resistor which, with R, establishes the output amplitude.

The performance of a 4-amplitude modulator is shown in Fig. 3.6 and Fig. 3.7. At the transition point of Fig. 3.6 there is a transient similar to that seen in the phase modulator. This transient is removable by filtering. The carrier frequency is 30 kHz and the switching rate is 9 kHz in Fig. 3.6 and 1 kHz in Fig. 3.7. The amplitude transitions are rapid with negligible distortion.

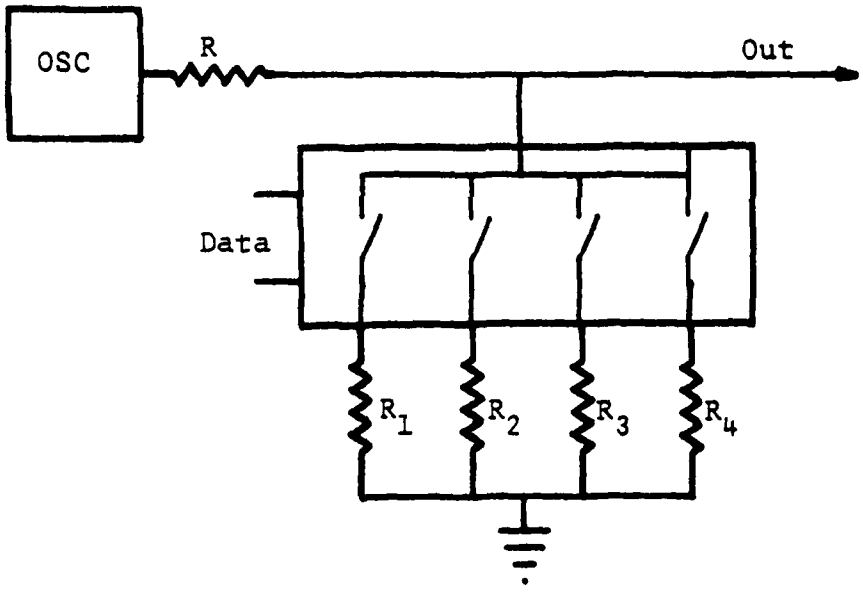


Fig. 3.5. Amplitude Modulator Block Diagram

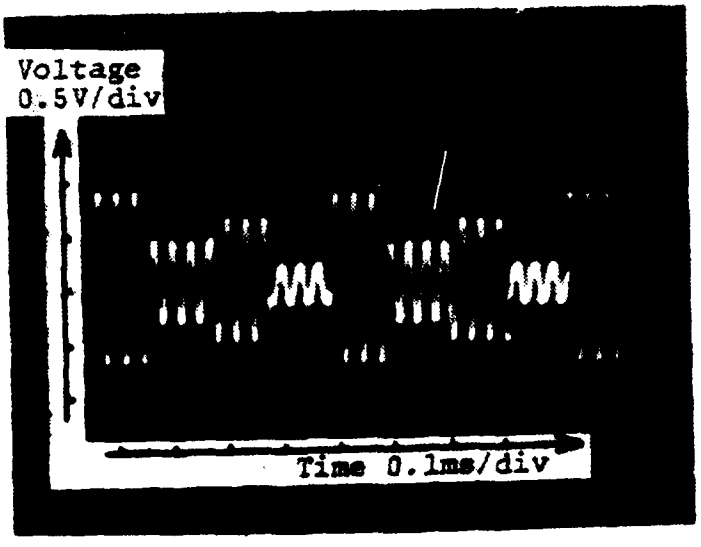


Fig. 3.6. Amplitude Modulator Output

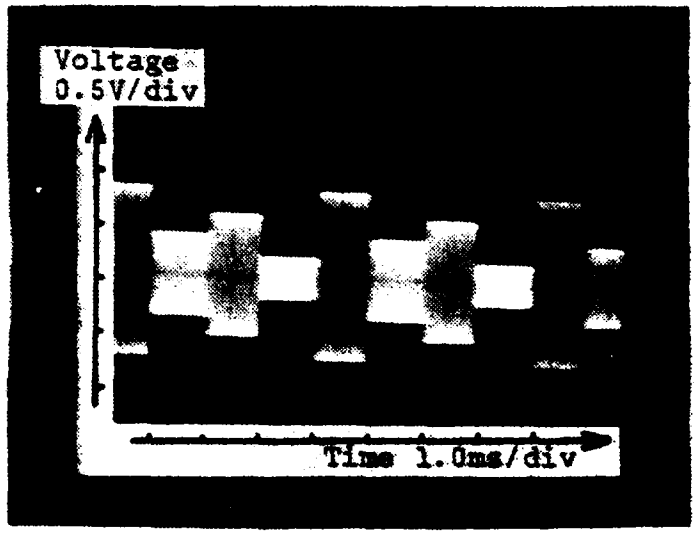


Fig. 3.7. 4-Amplitude Modulator Output

C. COMPOSITE AMPLITUDE AND PHASE MODULATORS

Composite amplitude and phase modulation with analog multiplexers can be done many ways. One way is to select among sinusoids of pre-set phase and amplitude as in the phase modulator described above. This, however, is rather restrictive. Two multiplexers in combination provide more flexibility.

1. 4-Phase, 4-Amplitude Modulator

Figure 3.8 is a block diagram of a modulator that combines the phase and amplitude functions. In this arrangement any of four amplitudes at any of four phase

angles may be selected. The output can be a 16-ary signal. The four phase angles and the four amplitudes may be pre-set to take advantage of the properties of the transmission system.

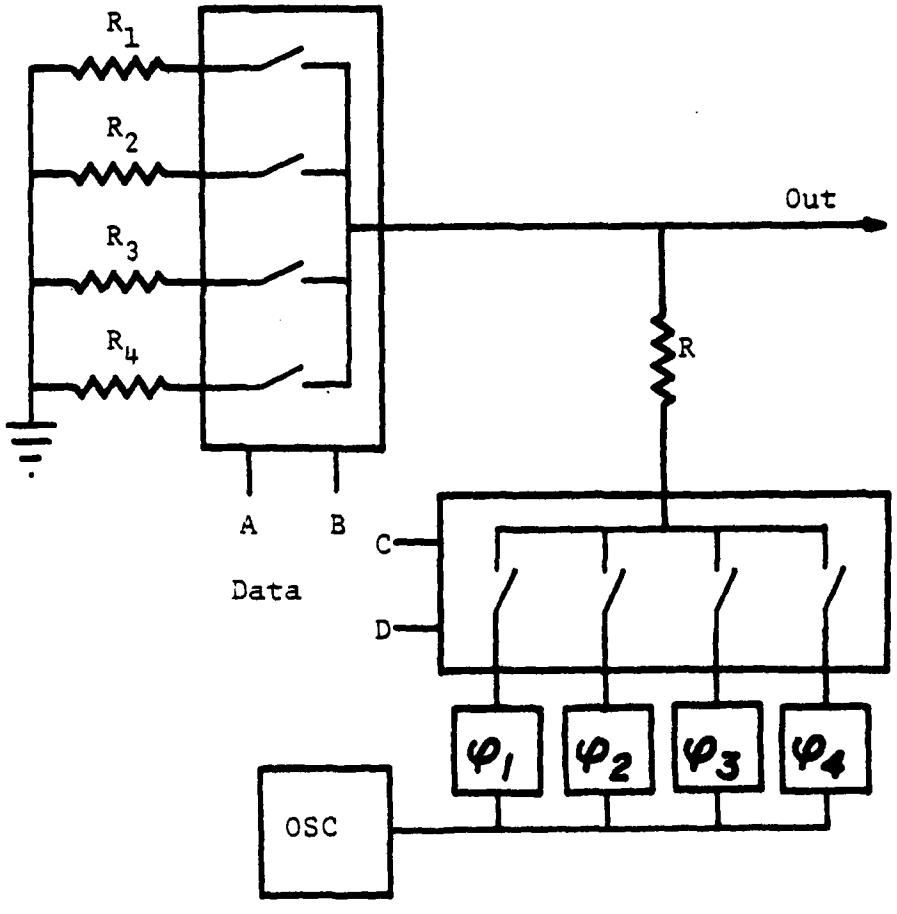


Fig. 3.8. 4-Phase, 4-Amplitude Modulator Block Diagram

The performance of a 4-phase, 4-amplitude modulator is shown in Fig. 3.9 and Fig. 3.10. Figure 3.9 is the

output with a 30 kHz carrier and a 10 kHz switching rate with periodic data switching both phase and amplitude simultaneously. Figure 3.10 is the output with a 1 kHz switching rate. Again the transitions are rapid with negligible distortion.

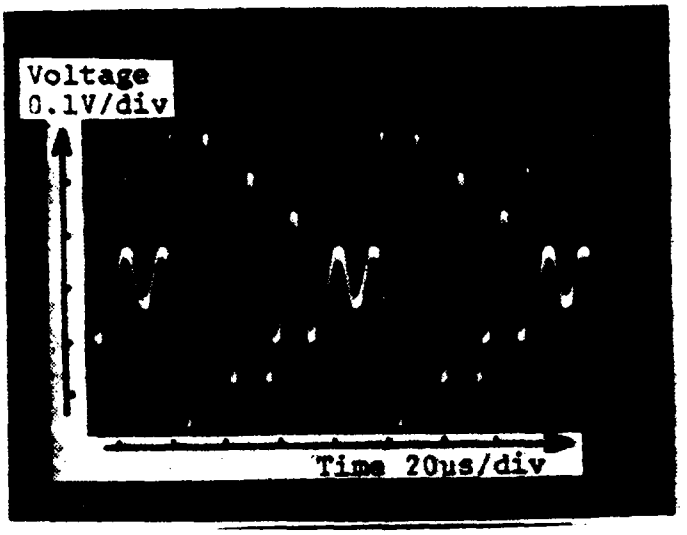


Fig. 3.9. 4-Phase, 4-Amplitude Modulator Output - 10 kHz

Some observations are in order. Any number of phase angles and amplitudes may be generated. This number is limited only by the number of inputs on the multiplexer. If there were a need to do so, additional capacity could be had by using the INHIBIT control of the multiplexer to select

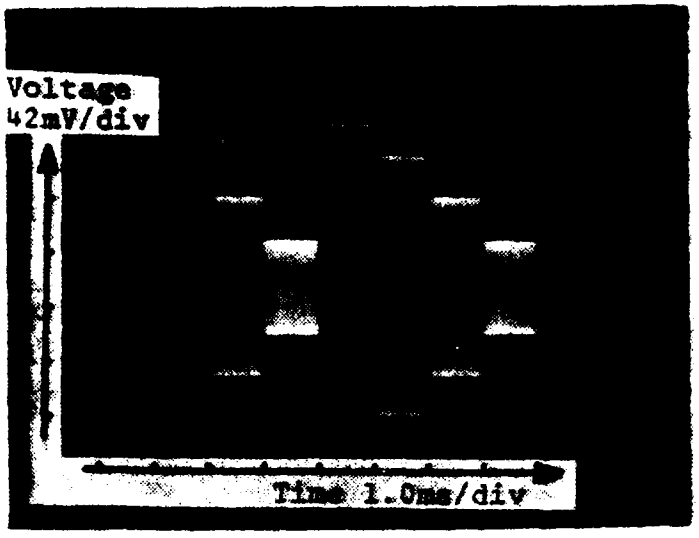


Fig. 3.10. 4-Phase, 4-Amplitude Modulator Output - 1 kHz

among chips. It is possible to carry separate data streams in the amplitude and phase of the signal, but it may not be desirable because of the significantly larger probability of error in the amplitude detector as compared with the phase detector. It would also be possible to clock the data inputs to the two multiplexers at different rates.

Figure 3.11 is the circuit diagram of a 4-phase, 4-amplitude modulator. The voltage follower in the output buffers the voltage divider. The output amplifier matches the voltage level to the channel. Details of the 4-phase source and channel are in Appendix A. Table I shows the control truth tables.

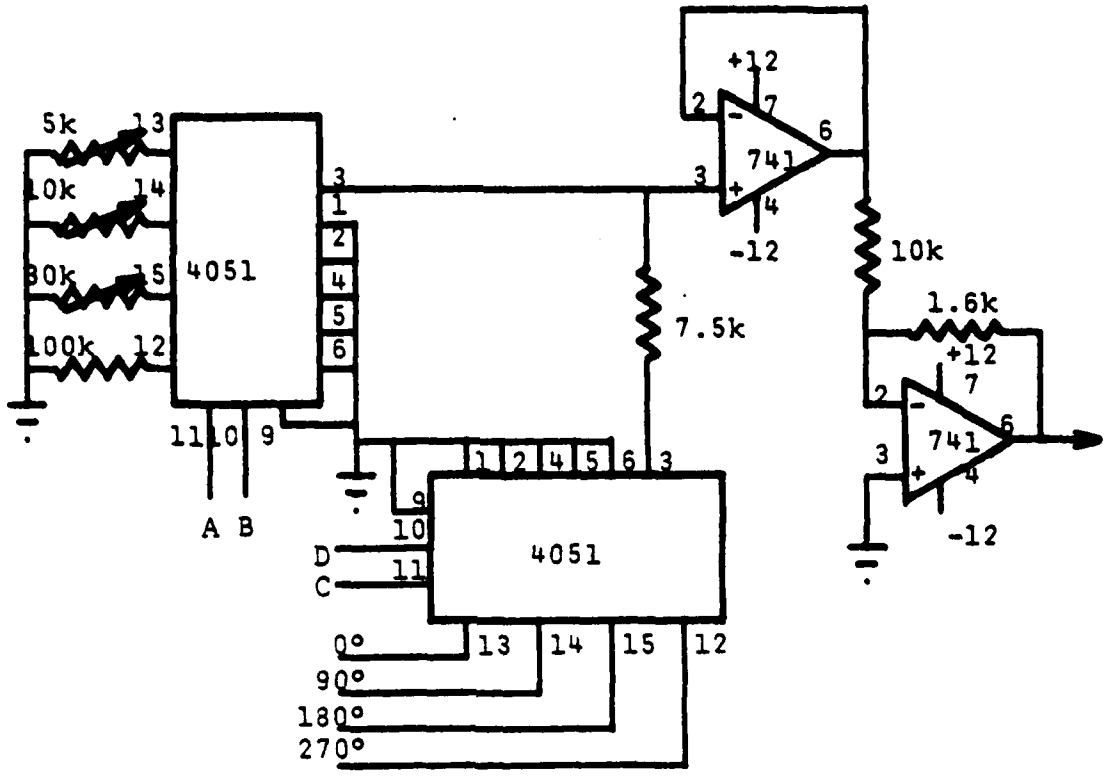


Fig. 3.11. 4-Phase, 4-Amplitude Modulator Circuit Diagram

TABLE I

4-Phase, 4-Amplitude Modulator Truth Tables

A	B	Resistor	Vout	C	D	Angle
0	0	5k	V/4	0	0	0°
0	1	10k	V/2	0	1	90°
1	0	30k	3V/4	1	0	180°
1	1	100k	V	1	1	270°

2. General Analog Multiplexer Modulator

The modulators described earlier have limited flexibility in phasor placement. There is another class of analog multiplexer modulators that gives greater flexibility. Figure 3.12 is the block diagram of this general analog multiplexer modulator.

The general analog multiplexer modulator output is the sum of two sinusoids. The data inputs are the address lines on a ROM which is programmed to select the input sinusoids necessary to sum to the desired output. Figure 3.13 is a phase plane diagram of one possible output constellation from this modulator. If, for example, we wish to transmit the phasor designated "P" in Fig. 3.13, we select the cosine input weighted "C" and the sine input weighted "E". The modulator sums these two sinusoids giving a sinusoid with the amplitude and phase indicated by phasor "p".

The flexibility of the modulator lies in its ability to sum sinusoids with any pre-set coefficients. There is no reason the input coefficients must be equally spaced as drawn. They may be any value. The use of the INHIBIT control allows one to place the phasor on an axis, even at the origin if desired.

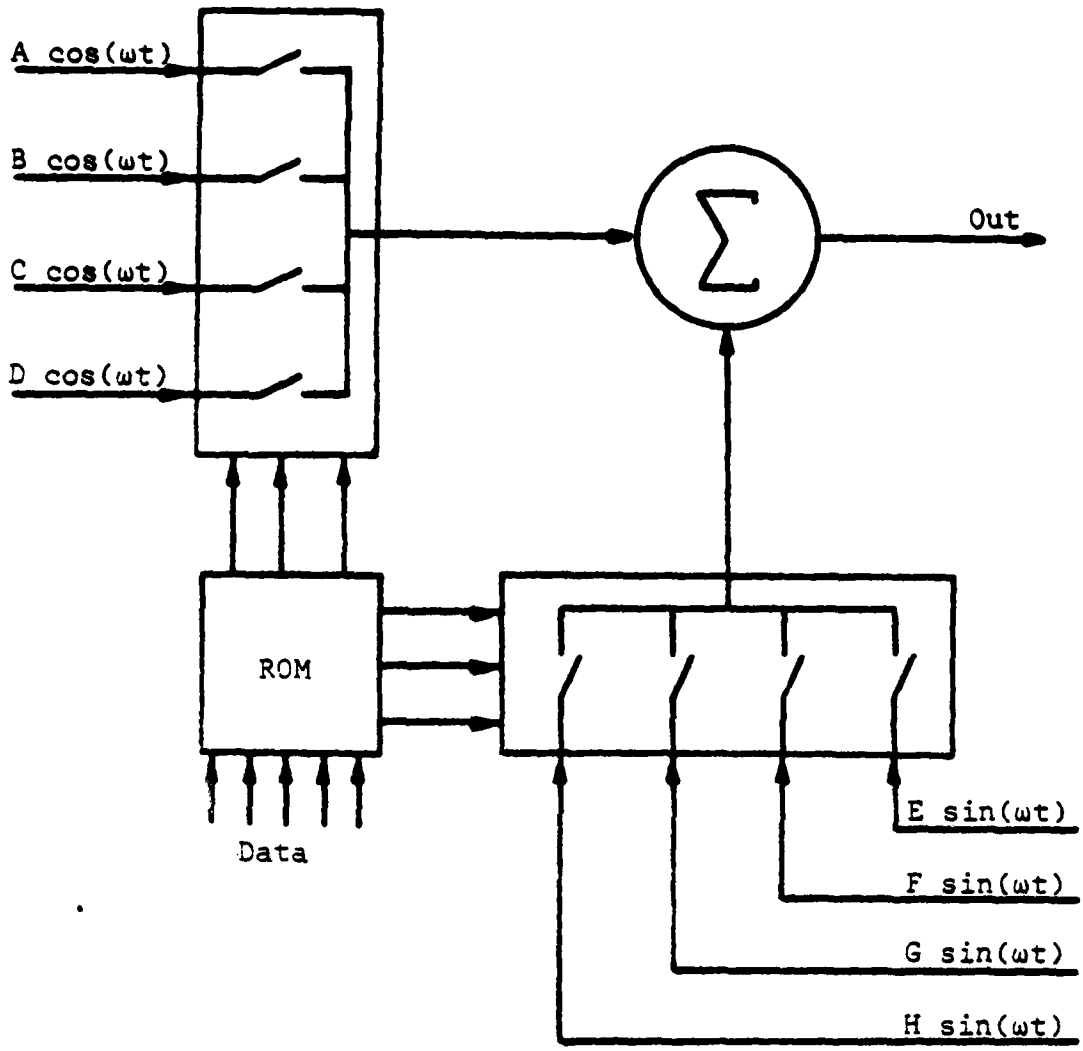


Figure 3.12. General Analog Multiplexer Modulator Block Diagram

While the modulator in Fig. 3.12 has 25 possible output phasors, only four are arbitrary. Once one coefficient is fixed, one component of five phasors is fixed.

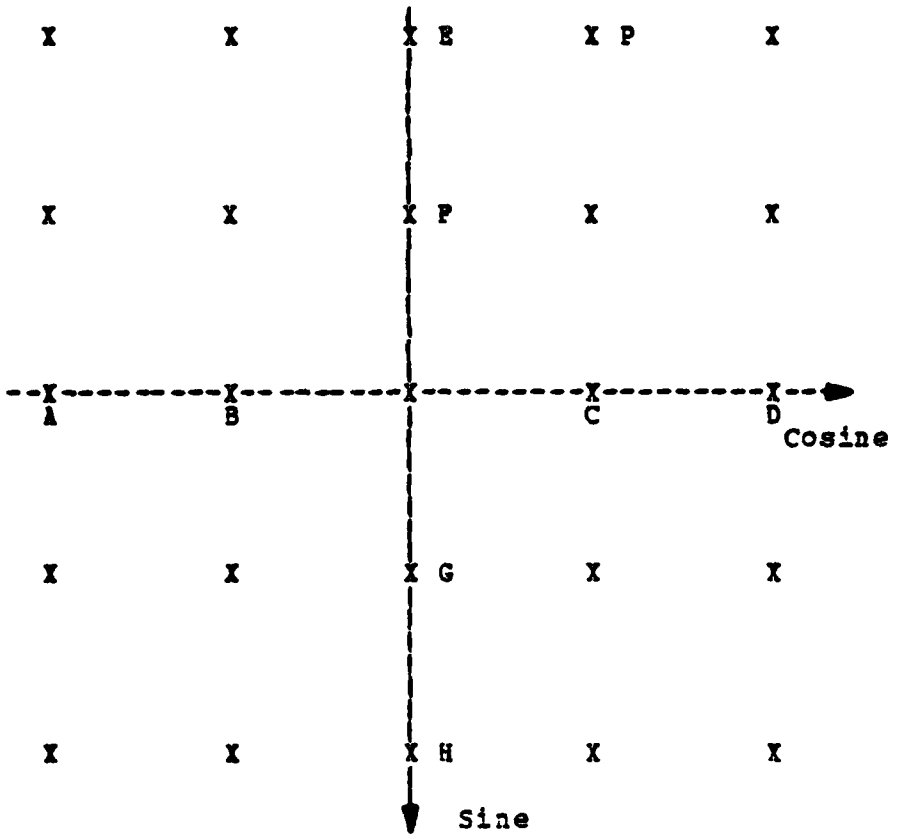


Figure 3.13. General Analog Multiplexer Modulator Phase-Plane Diagram

The 4051 analog multiplexer used in this investigation has eight inputs. This capability expands the potential illustrated in Fig. 3.13 to nine points including zero on each axis for a total of 81 possible phasors with eight arbitrary. The number of arbitrary phasors can be made as large as we please by increasing the number of multiplexers and changing the ROM to select both the required chips and the required inputs.

The circuit of one implementation of the general analog multiplexer modulator is shown in Fig. 3.14. The experimental circuit was aligned for a 4-phase, 4-amplitude output like that produced by the modulator in Section 3.C.1. The ROM was also programmed to give the same constellation rotated 45°. These patterns demonstrate the flexibility of the modulator while remaining compatible with the receiver previously constructed. Appendix A gives the details of the experimental circuits. Appendix B describes the programming of the ROM.

The voltage followers in Fig. 3.14 buffer the voltage dividers. The output amplifier sums the sinusoids and reduces the voltage to a level compatible with the channel.

The performance of the general analog multiplexer modulator with periodic data is shown in Fig. 3.15 and with random data in Fig. 3.16. The carrier is 30 kHz and the symbol rate is 1 kHz. The observable transitions are rapid with negligible distortion.

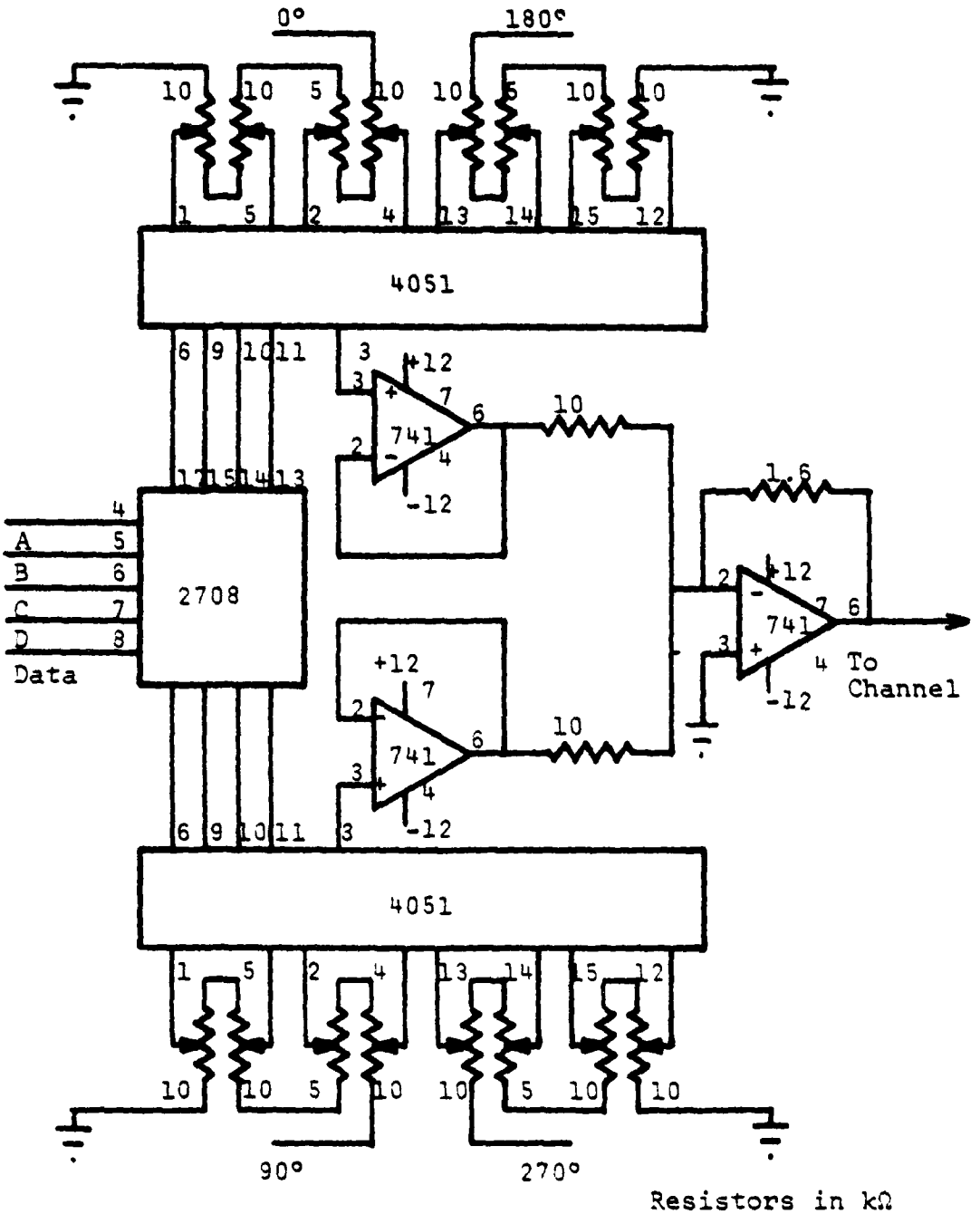


Figure 3.14. General Analog Multiplexer Modulator Circuit Diagram

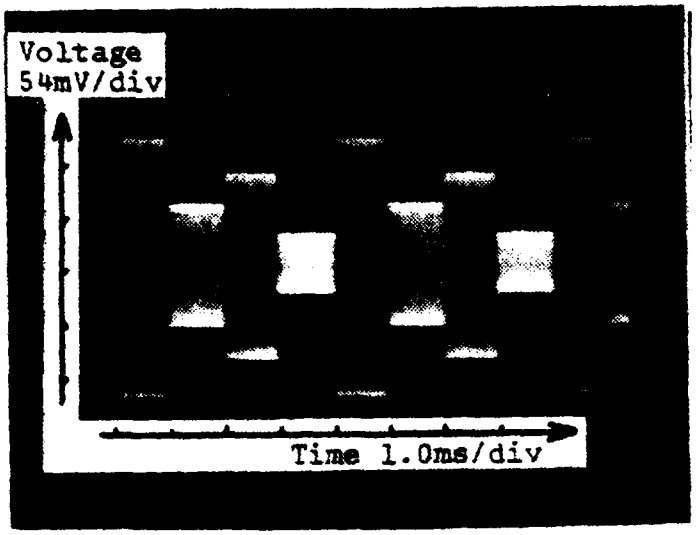


Figure 3.15. General Analog Multiplexer Modulator Output - Periodic Data

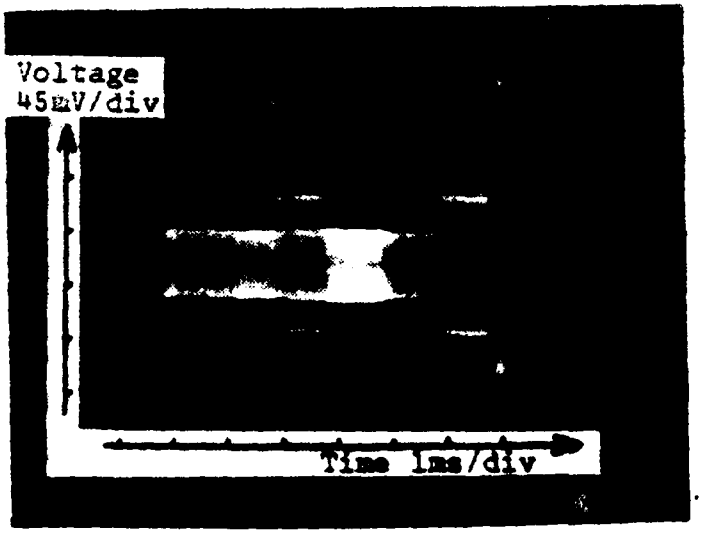


Figure 3.16. General Analog Multiplexer Modulator Output - Random Data

IV. EXPERIMENTAL METHOD

Both the 4-phase, 4-amplitude modulator and the general analog multiplexer modulator were built and tested. The 4-phase, 4-amplitude modulator transmits the phase plane constellation shown in Fig. 4.1. The general analog multiplexer modulator transmits both the constellation in Fig. 4.1 and that in Fig. 4.2. Both modulation schemes are the same since the 45° rotation is with respect to an arbitrary reference. Each of the 16 symbols represents four bits of data.

The objective of the test was to determine if the modulators, constructed as simply as Chapter III suggests, would perform well enough to warrant further investigation. The results support the basic concept. Further investigation with this flexible modulator concept is warranted.

The following sections describe the experimental system, the experimental procedure, and the experimental results.

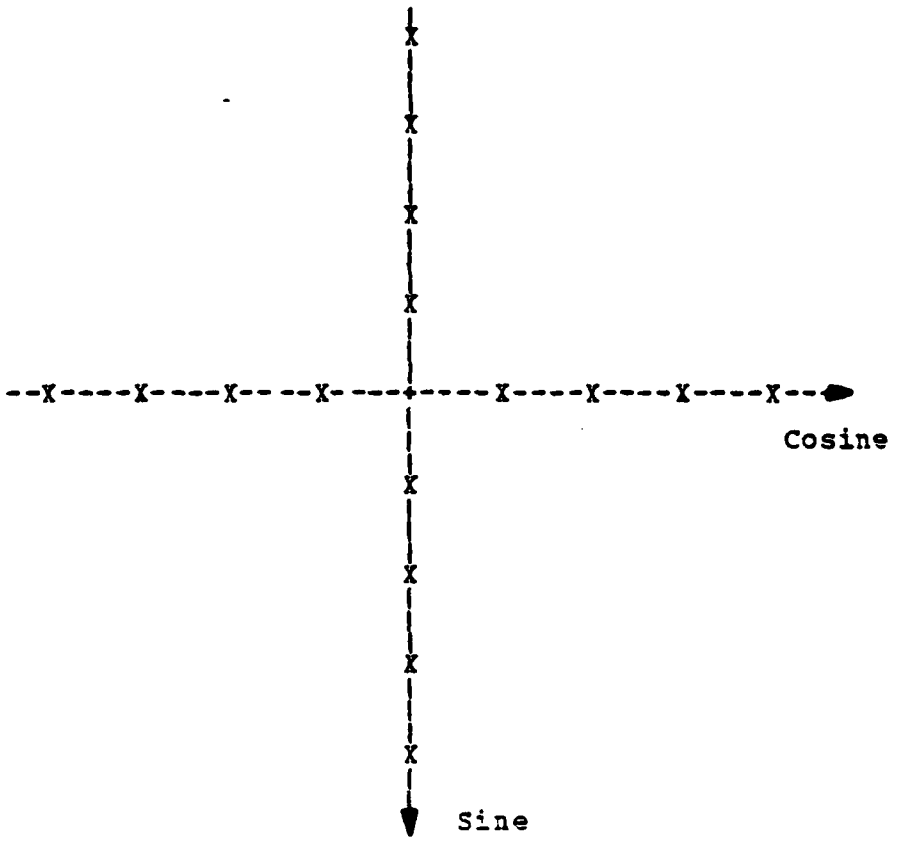


Fig. 4.1. Experimental Phase Plane Constellation

A. EXPERIMENTAL SYSTEM

Figure 4.3 shows the experimental system that tests the modulators by sending data to the modulators, adding a variable level noise to the modulated signal, extracting an estimate of the data from the signal plus noise, and counting errors in the receiver output. Appendix A describes the experimental system in detail.

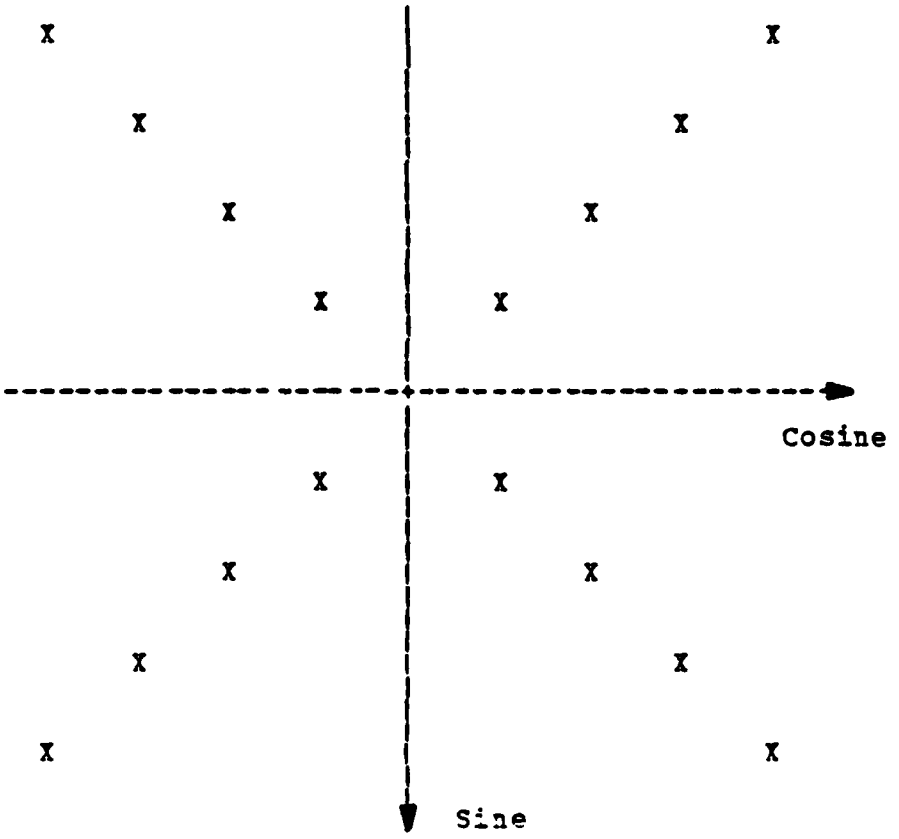


Fig. 4.2. Experimental Phase Plane Constellation

The data source is a 16-stage feedback shift register which generates a pseudo-random sequence 65535 bits long. The data rate is 4 kHz. This data, with a random starting point for each test run, is presented four bits at a time to the modulator which transmits a carrier at an amplitude and phase that represents the four-bit symbol. The symbol rate through the transmission system is 1 kHz. The carrier frequency is 30 kHz.

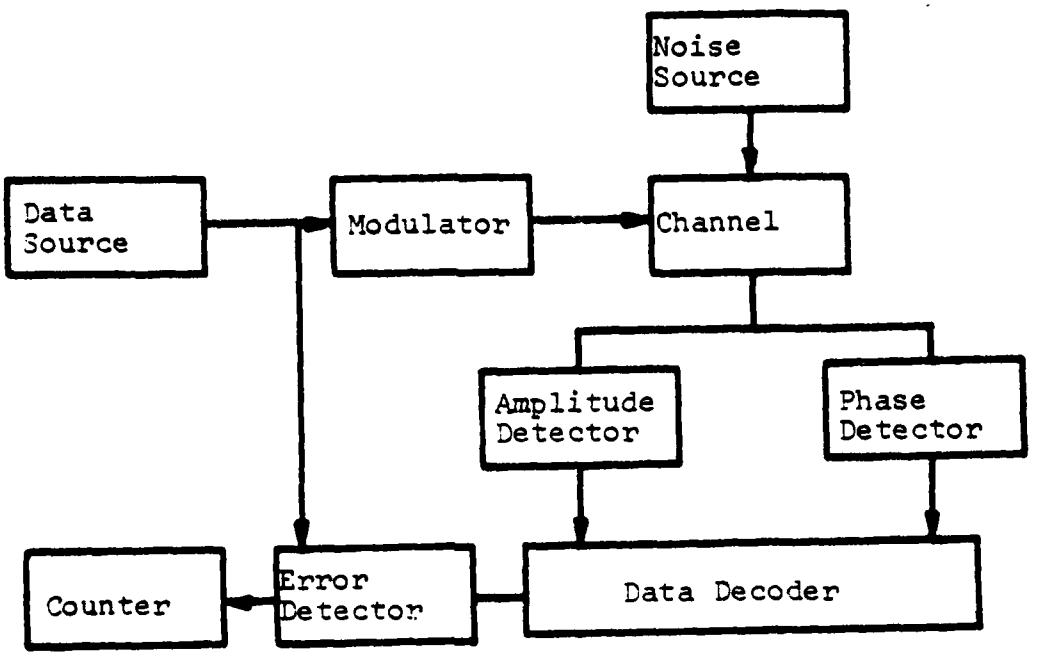


Fig. 4.3. Experimental System

The transmitted symbol passes through a channel with a variable signal to noise ratio. The output power level of the modulator is fixed at a predetermined value. The signal to noise ratio in the channel is varied by changing the input noise level. The signal to noise ratio is measured at the input to the detectors with an RMS voltmeter (HP 3400A). Signal and noise are measured separately with the other input grounded. The idle channel noise was measured with both carrier and noise inputs grounded and determined to be at least 50 dB below the signal level.

An error detector compares bit by bit the data estimate from the receiver with the transmitted data and records the differences as errors.

B. EXPERIMENTAL PROCEDURE

The objective of the experimental procedure was to produce curves of the probability of error versus signal to noise ratio over a probability of error range of about 10^{-2} to 10^{-5}. The procedure for taking data was the following:

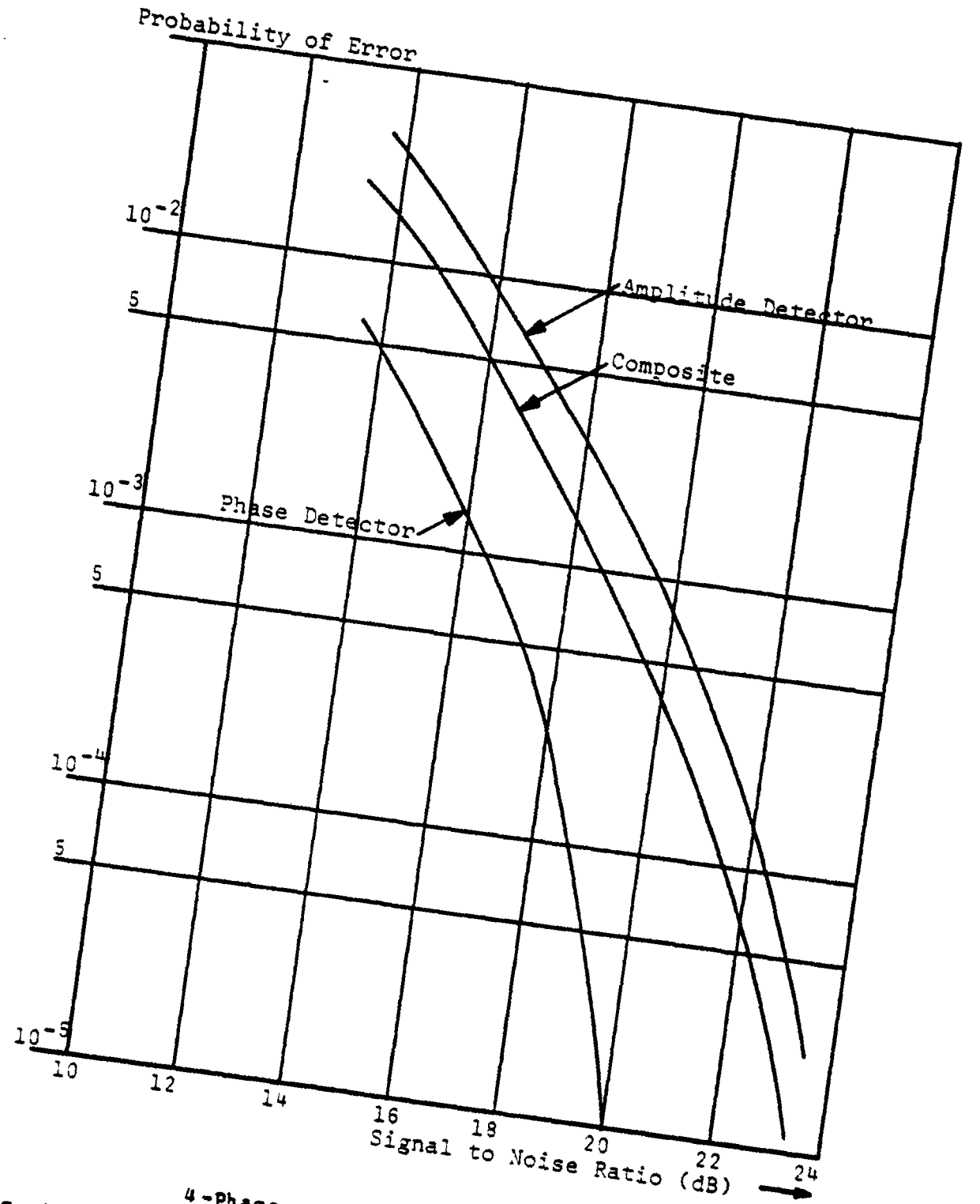
1. The carrier level at maximum amplitude was fixed at a level well within the dynamic range of system components and recorded. This level was constant for all test runs.
2. The noise level was set to a value within the range of interest and recorded.
3. Continuous random data was sent through the system.
4. The error detector counters were reset to zero and started. The counters stopped after 100,000 data bits had been examined. The number of errors in 100,000 bits was recorded.
5. Step 4 was repeated three times.
6. The errors in four runs were summed and the probability of error was computed.
7. Steps 2 through 6 were repeated for various signal to noise ratios sufficient to generate the desired performance curves.

The experimental results are given in the next section.

C. EXPERIMENTAL RESULTS

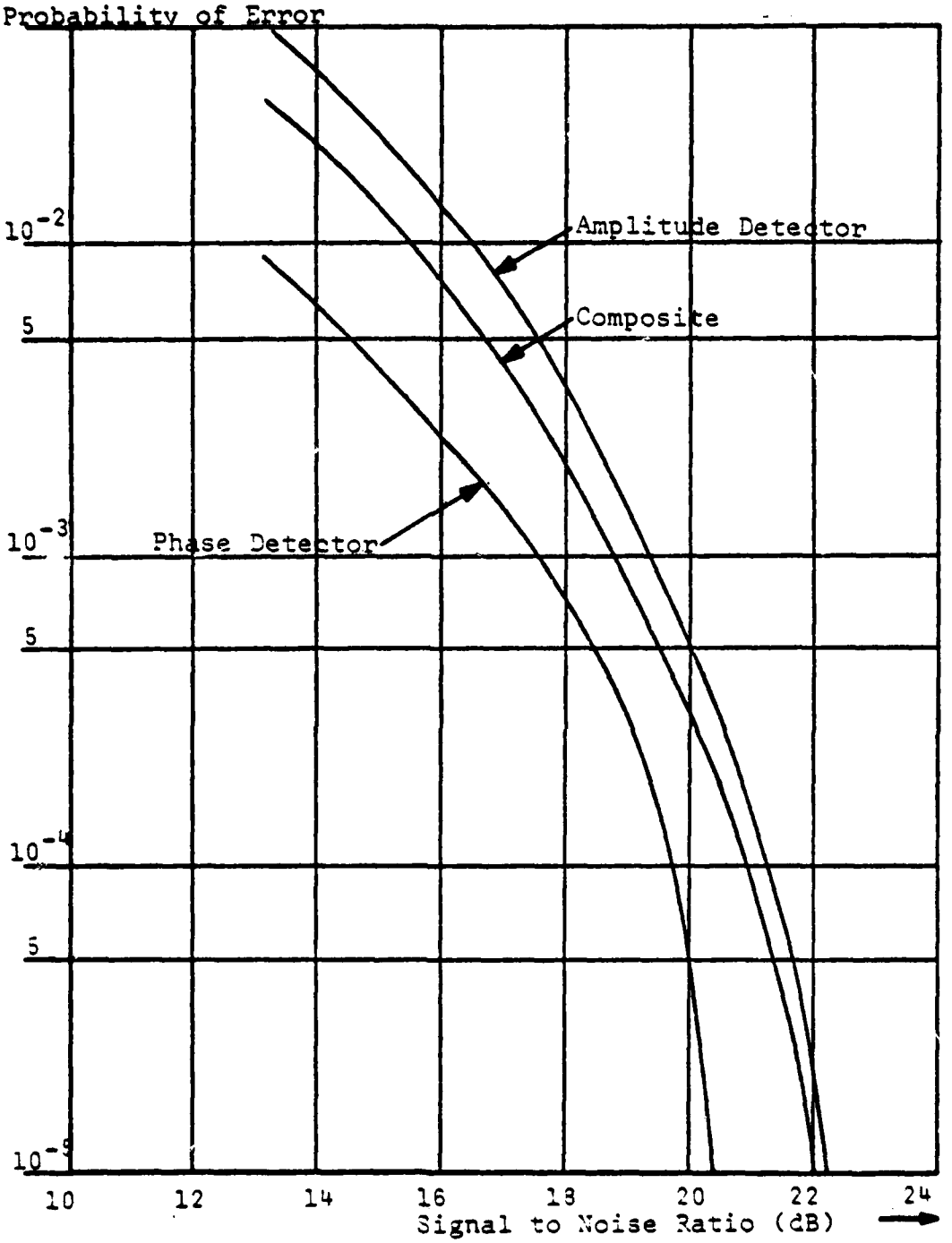
Data taken with the procedure outlined in the preceding section is summarized in the curves displayed in Fig. 4.4 through Fig. 4.6. All three figures show the measured probability of error of the composite system and the detectors separately. Figure 4.4 is the set of curves for the 4-phase, 4-amplitude modulator of Section III.C.1. Figures 4.5 and 4.6 are the sets of curves for the general analog multiplexer modulator transmitting the constellations of Fig. 4.1 and Fig. 4.2 respectively.

The curves show differences, but they also show strong similarities. The composite curves are within 2 dB at a 10^{-5} error rate. The differences are the result of alignment variations in the receiver where a few millivolts change in a threshold or offset adjustment made a significant difference in performance. The magnitudes expressed in the curves show that the receiver is not optimum. A conclusion one should draw from the curves is that the two classes of modulators are comparable. Another conclusion is that the overall performance is such as to warrant further study.



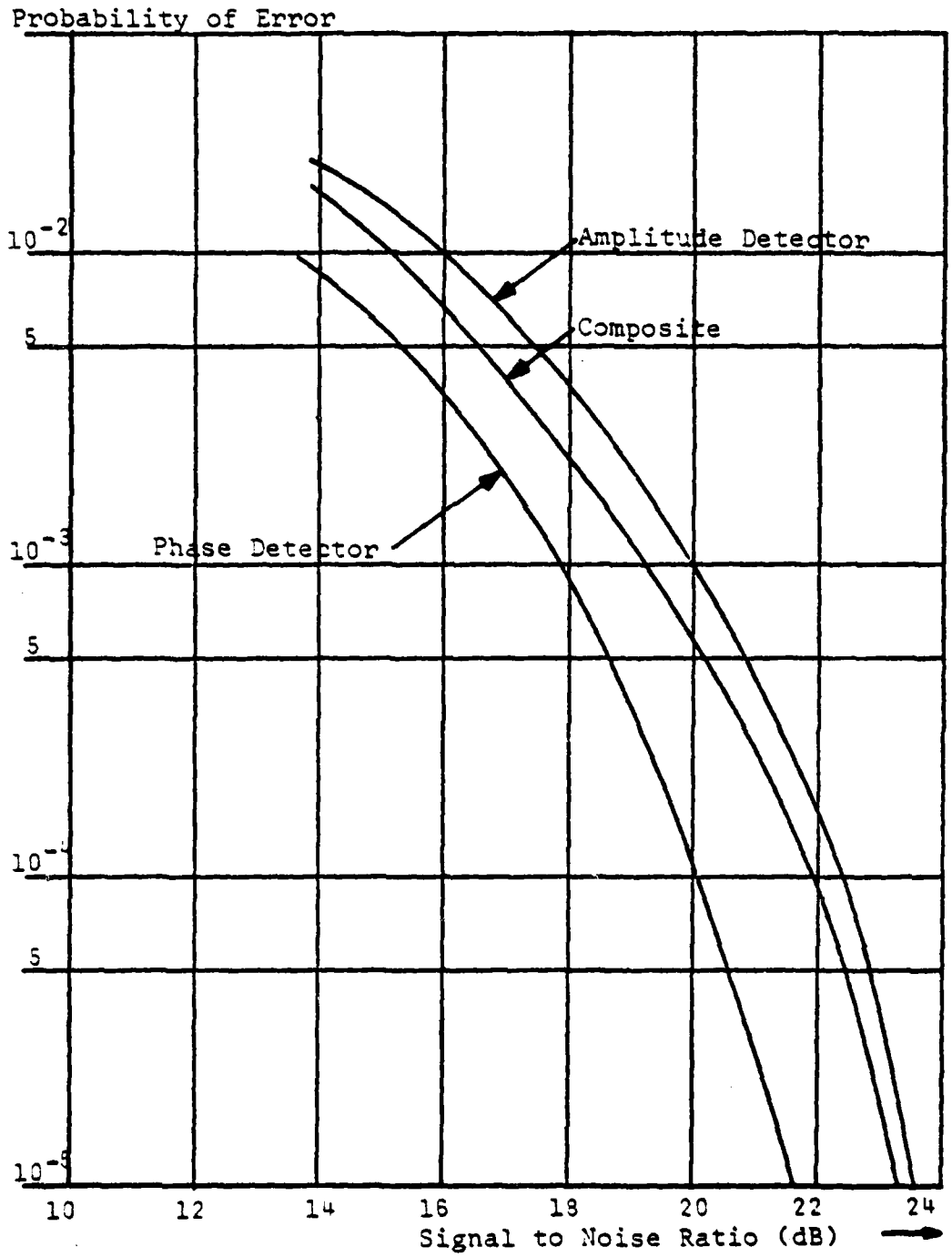
4-Phase, 4-Amplitude Modulator

Fig. 4.4. Probability of Error versus Signal to Noise Ratio



Modulation Scheme of Fig. 4.1

Fig. 4.5. Probability of Error versus Signal to Noise Ratio



Modulation Scheme of Fig. 4.2

Fig. 4.6. Probability of Error versus Signal to Noise Ratio

V. CONCLUSIONS AND RECOMMENDATIONS

The analog multiplexer is a suitable device for a digital modulator at the carrier frequency and data rate used in this research. It switches the carrier rapidly with negligible distortion and generates only removable transients.

The two classes of modulator built for this investigation perform well. The outputs of the 4-phase, 4-amplitude modulator and the general analog multiplexer modulator are comparable for a given modulation scheme. The general analog multiplexer modulator, however, allows more flexibility in the placement of phasors. There is no inherent limit to the number of arbitrary phasors one can generate. Both modulators are simple circuits using inexpensive components.

Some suggestions for further study follow:

1. Seek higher carrier frequencies and faster symbol rates.
2. Use the flexibility of the general analog multiplexer modulator to study optimum phasor placement in terms of lowest post-detection probability of error.
3. Given optimum phasor placement, determine the optimum data-to-phasor coding scheme.

4. Look at the effects of switching phase and amplitude with independent data streams on independent clocks.

5. Look at the security and receiver addressing potential of switching modulation schemes.

6. Determine if switching modulation schemes to optimize the system dynamically improves the bit error performance over a system with a fixed modulation scheme.

APPENDIX A

THE EXPERIMENTAL SYSTEM

A. OVERVIEW OF THE EXPERIMENTAL SYSTEM

The experimental system consists of a transmission system, a test system, and a timing system. The transmission system contains the modulator, channel, and receiver (Fig. A.1). The test system has a data source and an error detector. The timing system provides clocking for both the transmission system and the test system. The following sections of this appendix describe each system.

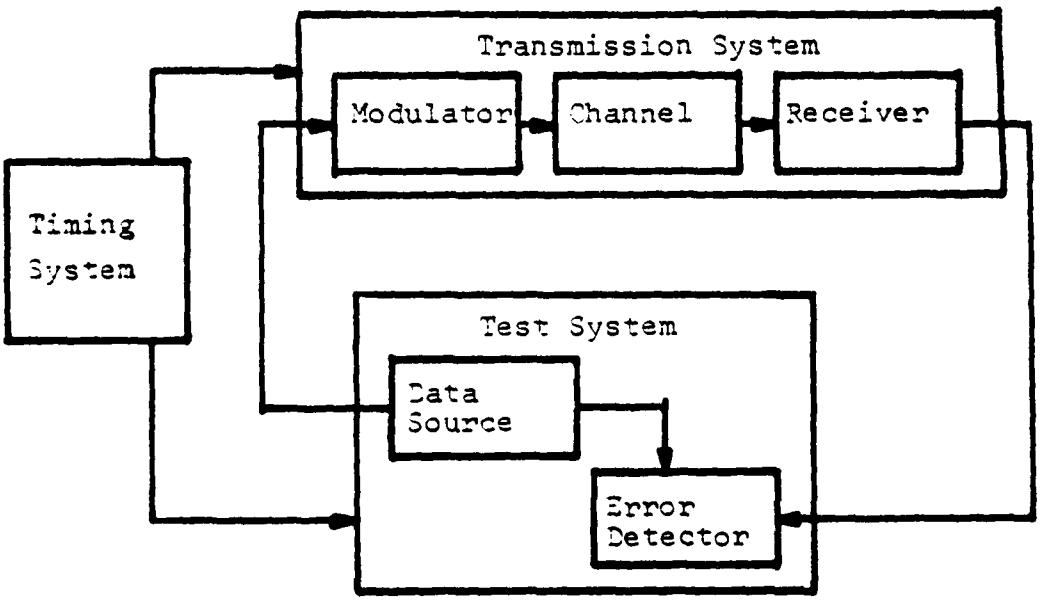


Fig. A.1. Experimental System Block Diagram

B. TRANSMISSION SYSTEM HARDWARE

A complete transmission system is used to test the operation of the modulator (Fig. A.2). The transmitter is just the modulator which is discussed in detail in Chapter III. The channel adds white Gaussian noise to the signal, bandlimits the sum, and provides level adjustment before the receiver. The receiver has both amplitude and phase detectors. Timing signals are from the common timing system. The following sections describe the channel and receiver.

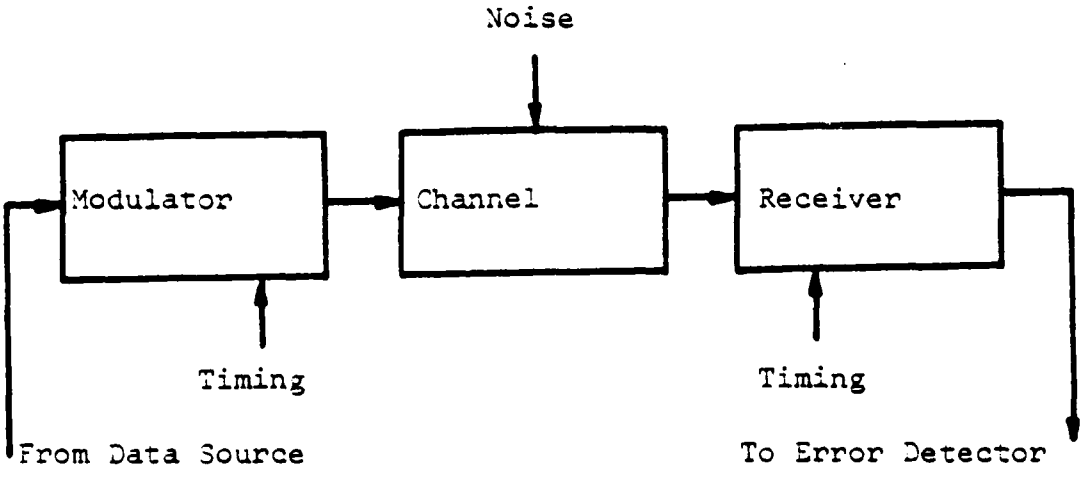


Fig. A.2. Transmission System Block Diagram

1. Channel

The transmission channel consists of a noise summer, a bandpass filter, and a predetector level adjusting amplifier (Fig. A.3).

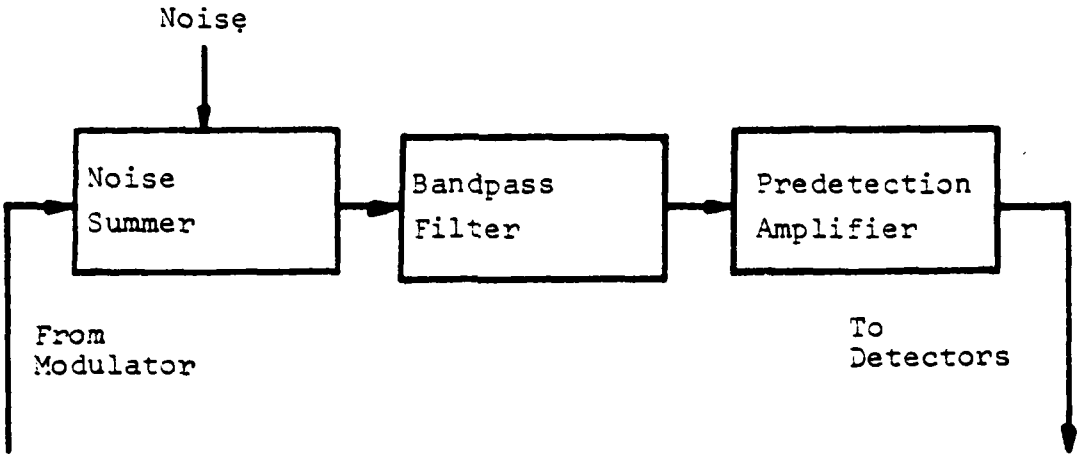


Fig. A.3. Transmission Channel Block Diagram

a. Noise Summer

The noise summer provides isolation of the modulator and the noise generator and provides the correct voltage level into the bandpass filter (Fig. A.4). The modulated signal passes through a blocking capacitor to the summer with an input gain control. The signal level out of the summer is fixed by the following procedure:

1. Ground the noise input.
2. Set the modulator data input for a fixed output carrier signal of maximum amplitude.

3. Adjust the carrier input to the modulator to 2 V(p-p).

4. Adjust the signal gain for a summer output of 300 mV(p-p).

The noise goes through an isolating voltage follower to the summer. The noise level may be set by adjusting the output level of the random noise generator.

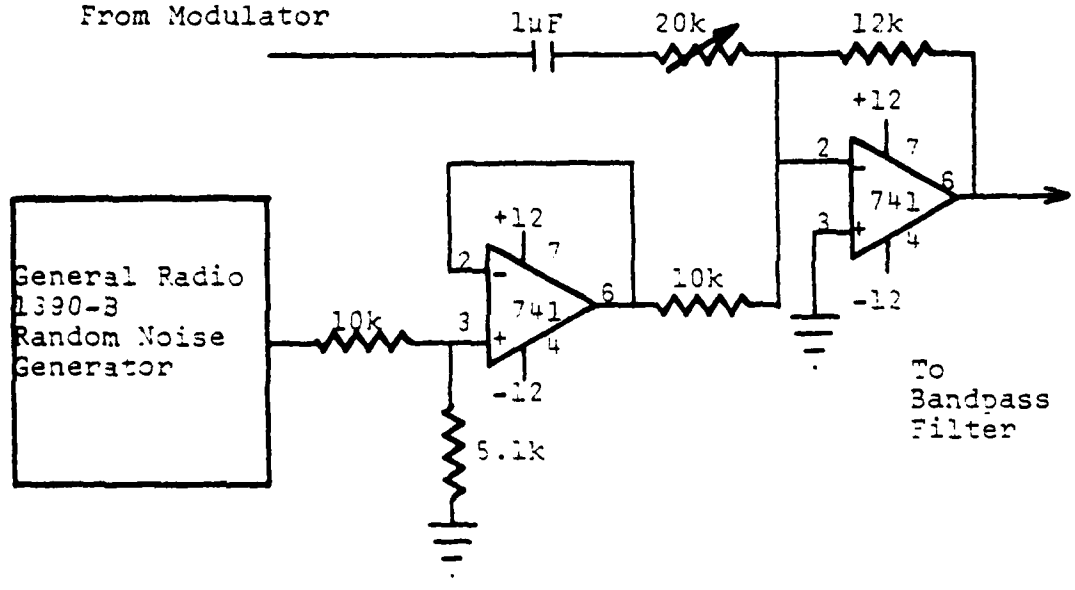


Fig. A.4. Noise Summer Circuit Diagram

b. Bandpass Filter

The ideal bandpass filter would pass all of the signal power and limit noise power to that within the signal passband. The bandwidth of the passband is a function of

the signaling rate and the modulation scheme. This system operates at a symbol rate of 1 kHz with both phase and amplitude modulation at that frequency. The carrier frequency is 30 kHz. A bandwidth of 3 kHz is a compromise between low noise and low intersymbol interference.

The bandpass filter design is based on the procedure of Helburn and Johnson [Ref. 3]. The Q of the resulting filters is higher than that indicated in the procedure. Using a gain of 2 and a Q of 6 rather than a Q of 10 as indicated by the ratio of bandwidth to center frequency resulted in the circuit in Fig. A.5. The variable resistors permit some adjustment of the center frequency. They are adjusted for a maximum output with an unmodulated 30 kHz input.

The transfer function of the filter, generated by sweeping the input frequency and recording the output on a storage display spectrum analyzer, is shown in Fig. A.6. The 3 dB points are 28.5 and 31.5 kHz.

The performance of the filter is shown in Fig. A.7 where the spectrum of the input noise is shown with the spectrum of the filter output and in Fig. A.8 where the spectrum of the amplitude and phase modulated input signal is shown with the spectrum of the filter output.

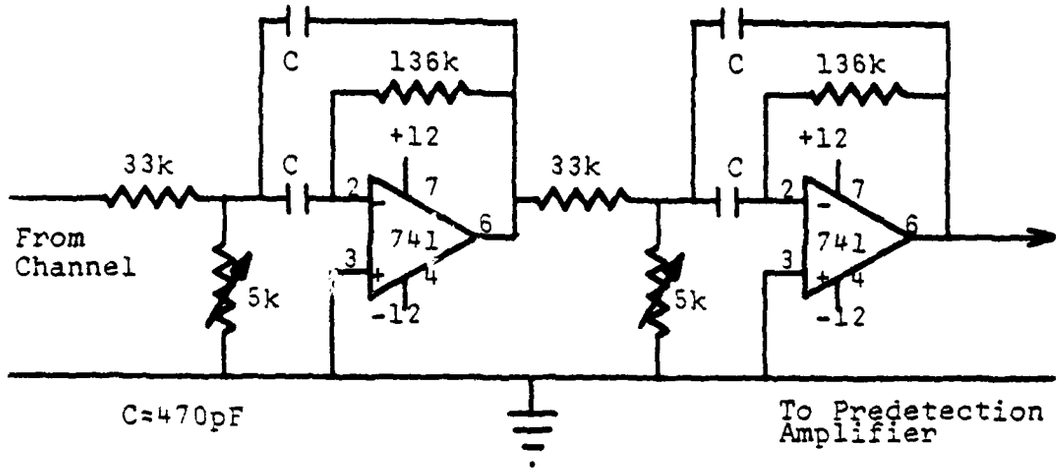


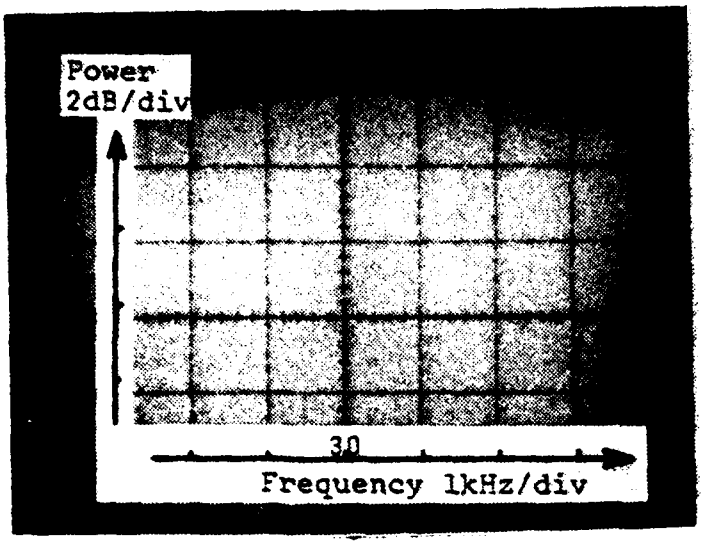
Fig. A.5. Bandpass Filter Circuit Diagram

The signal out of the bandpass filter is shown in Fig. A.10. The input signal was the general analog multiplexer modulator 4-phase, 4-amplitude signal shown in Fig. A.9 which is similar to Fig. 3.15.

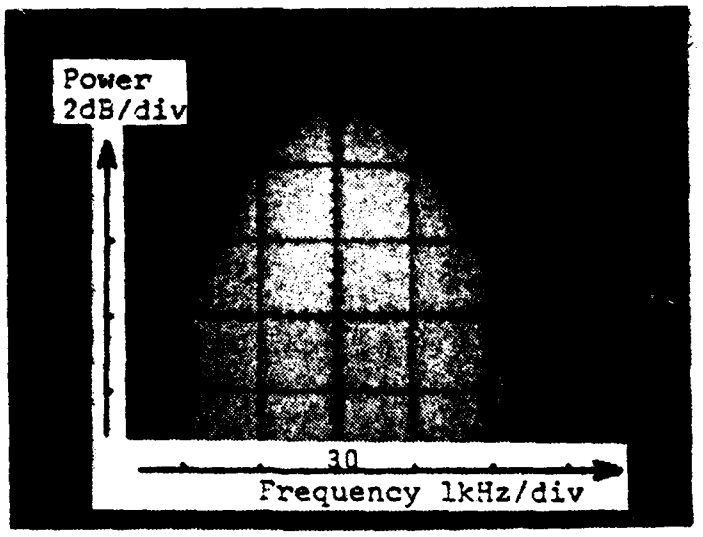
c. Predetection Amplifier

The predetection amplifier (Fig. A.11) sets the level of the signal into the detectors. There are two adjustments.

The gain of the first stage controls the level of the AC signal to the detectors. The level out of the bandpass filter is about 1.5 V(p-p). The desired level into

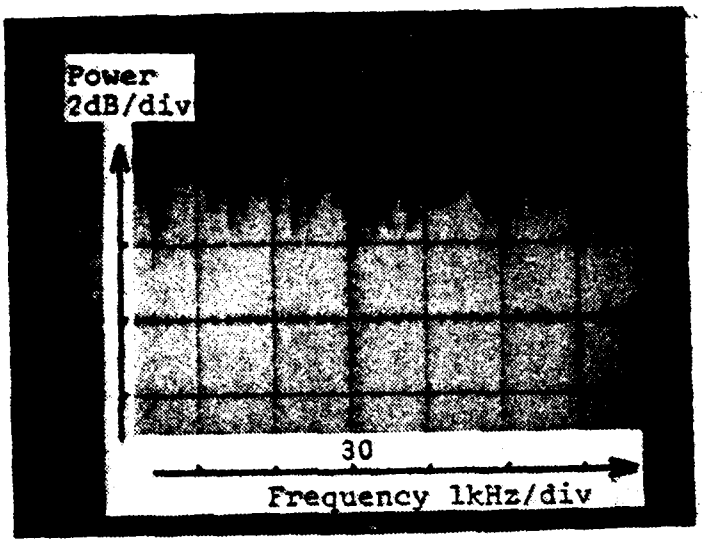


Input

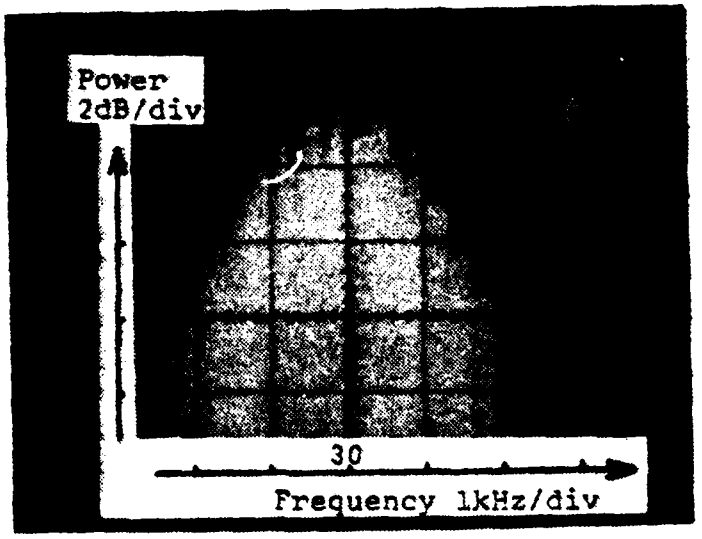


Output

Fig. A.6. Bandpass Filter Transfer Function

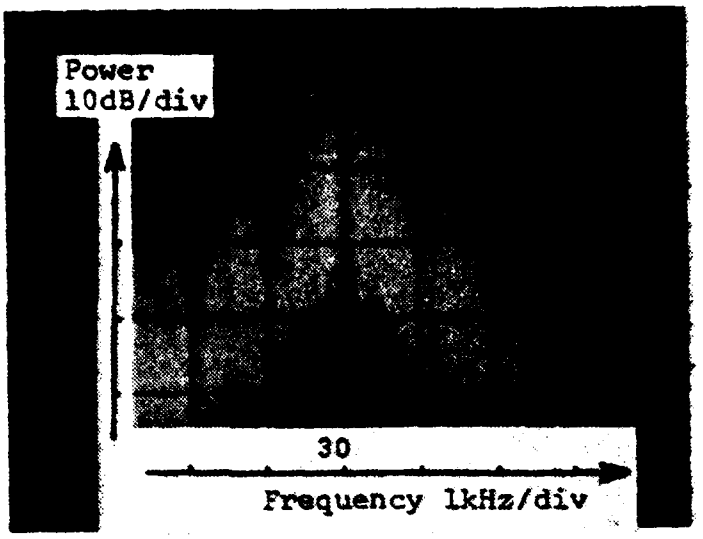


Input

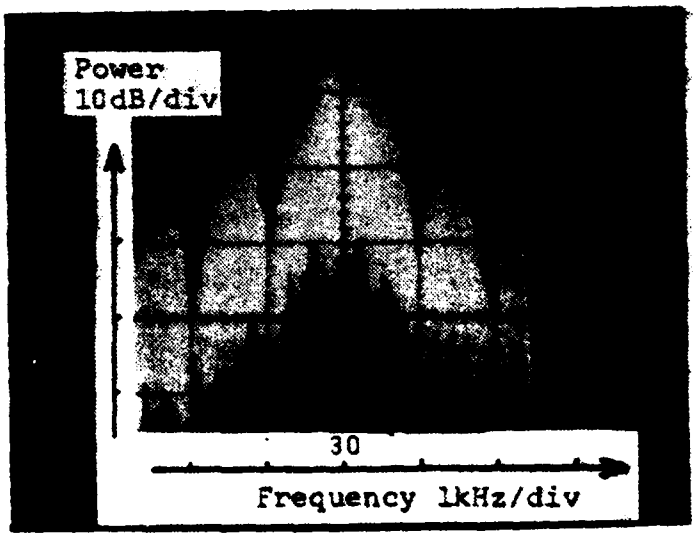


Output

Fig. A.7. Input and Output Spectra - Noise



Input



Output

Fig. A.8. Input and Output Spectra - Modulated Signal

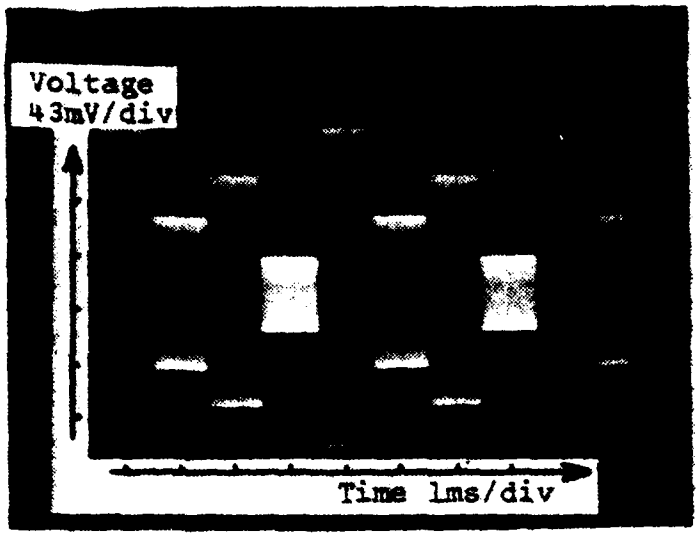


Figure A.9. General Analog Multiplexer Modulator Output - Periodic Data

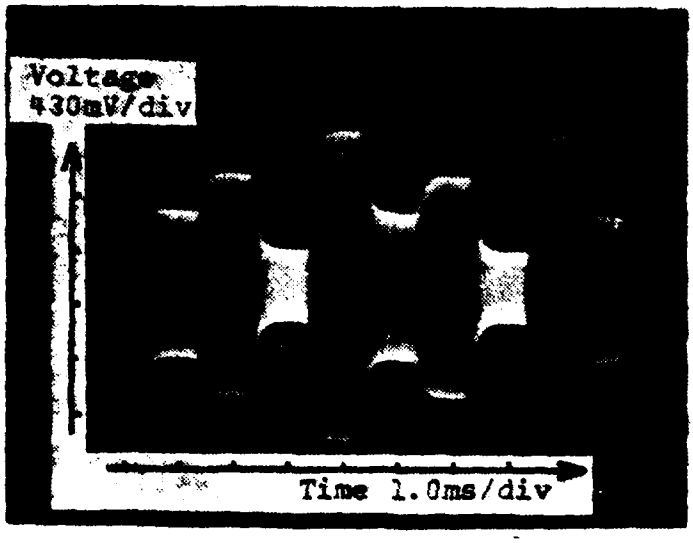


Fig. A.10. Bandpass Filter Signal Out

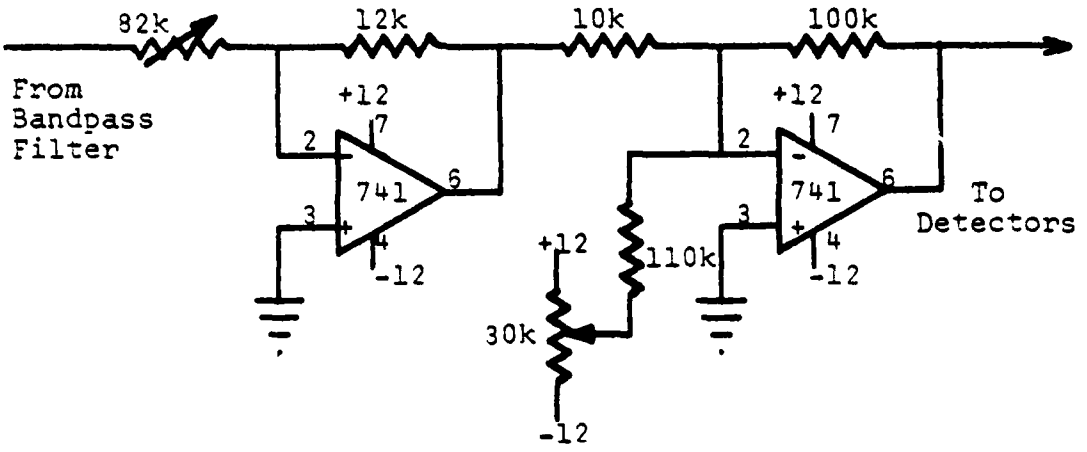


Fig. A.11. Predetection Amplifier Circuit Diagram

the envelope detector is 2.5 V(p-p). The input to the phase detector is not critical at this stage since it is further amplified.

The DC adjust on the second stage biases the signal above the diode drop of the envelope detector.

2. Receiver

The receiver has detectors to extract data from the amplitude and phase information of the input signal (Fig. A.12). The next paragraphs treat the two detectors.

a. Amplitude Detector

The amplitude detector is an envelope detector followed by a low pass filter, a decision circuit, and a decoding circuit (Fig. A.13). Each is described below.

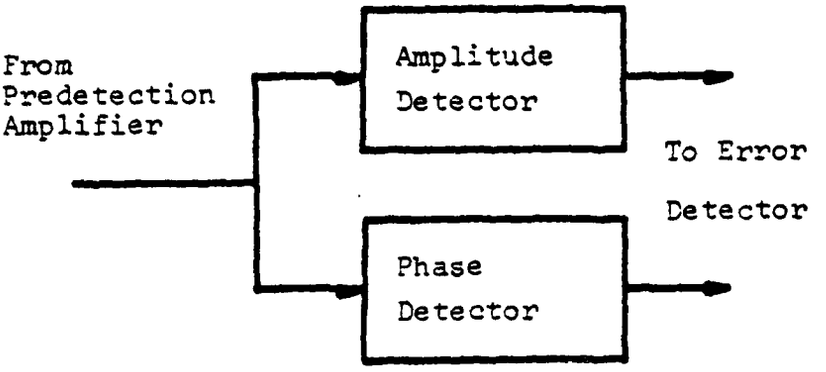


Fig. A.12. Receiver Block Diagram

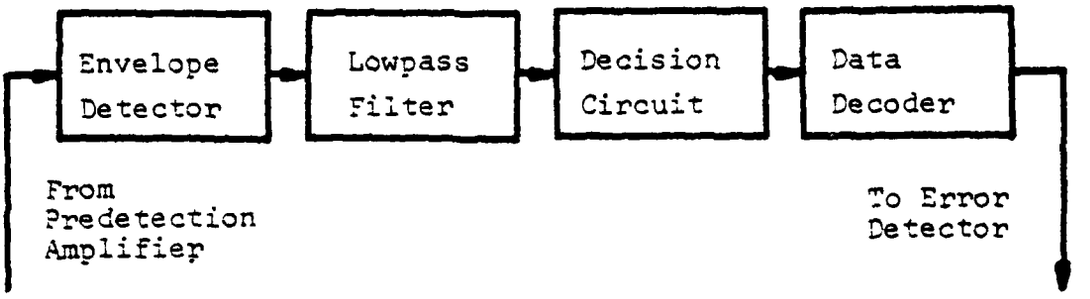


Fig. A.13. Amplitude Detector Block Diagram

An envelope detector was selected for simplicity. It is recognized that other detector circuits would reduce the probability of error for a given ratio of signal power to noise power. The demodulator is, however, not a primary concern of this research.

A voltage follower isolates the envelope detector from the input circuit and phase detector

(Fig. A.14). The diode has a voltage drop of about 0.8 V that must be overcome to get an output. If the input signal voltage is symmetric about zero, the low level envelope step will be reduced compared to the other steps (Fig. A.15). With a properly chosen threshold, this probably would not cause a problem, but for ease in setting the thresholds, the input signal is biased to be symmetric about the diode voltage (Fig. A.18). This is done at the predetection amplifier (Fig. A.11).

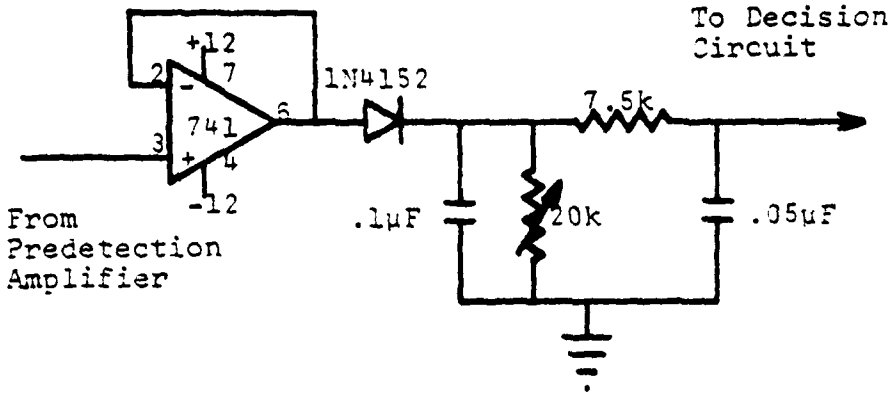


Figure A.14. Envelope Detector and Low Pass Filter Circuit Diagram

The RC time constant of the envelope detector is about 0.3 ms or three times the symbol period.

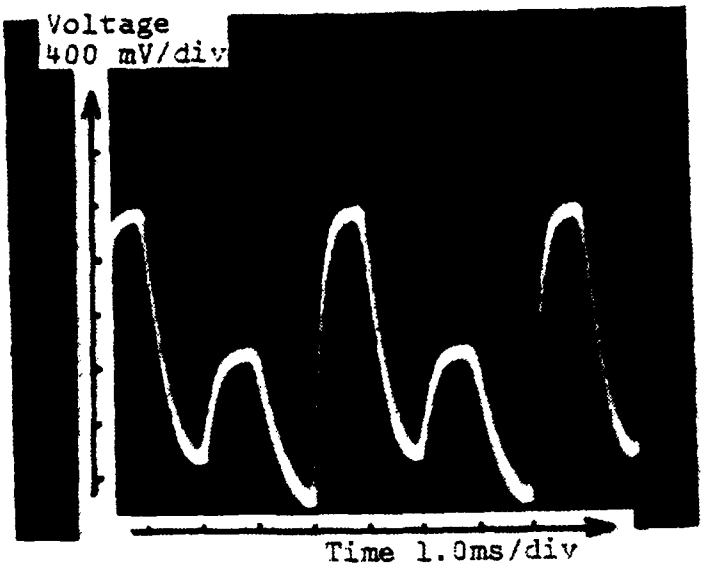


Fig. A.15. Effect of Envelope Detector Diode Drop

The breakpoint of the low pass filter transfer function is 2600 Hz.

The decision devices in the decision circuit are comparators (Fig. A.16). The signal from the low pass filter must be amplified to place it within the usable range of the comparators. Two stages of amplifiers retain a positive-going signal. The range control adjusts the signal gain of the amplifier which determines the range of levels presented to the comparators. The DC bias sets the absolute value of the levels. The comparators are connected for a TTL compatible output [Ref. 4]. This configuration requires

input levels between 0 and 4 V. The range and DC bias are set to give the voltage levels indicated on the representative waveform in Fig. A.17. Figure A.18 is a photograph of the actual waveform at the input to the comparators.

The thresholds are the midpoints between levels which one would expect assuming Gaussian noise. Measurements of bit error rates versus threshold voltage confirmed the midpoint threshold within experimental accuracy (Fig. A.19). Note the probability of error variation with only a 0.1 V change in threshold voltage. The final threshold values used in the experiment are shown in Fig. A.17.

The three comparator outputs from the decision circuit carry the estimate of two data bits encoded according to the truth table in Fig. A.20. Data bit A follows threshold 2 exactly, so only data bit B needs to be decoded. That is done using a 74151, one-of-eight data selector, with inputs 1 and 7 high and all others grounded as in Fig. A.20.

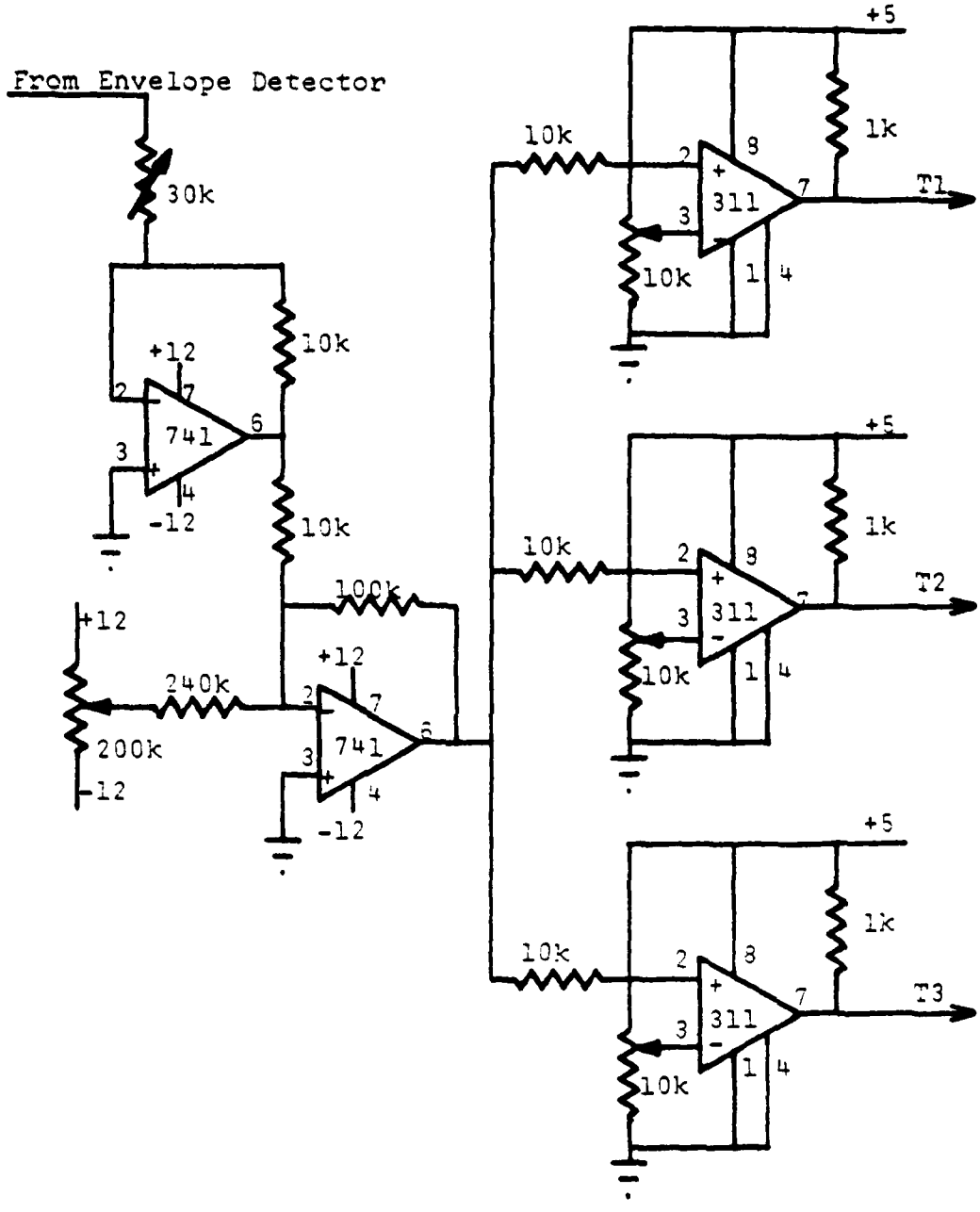


Fig. A.16. Amplitude Decision Circuit Diagram

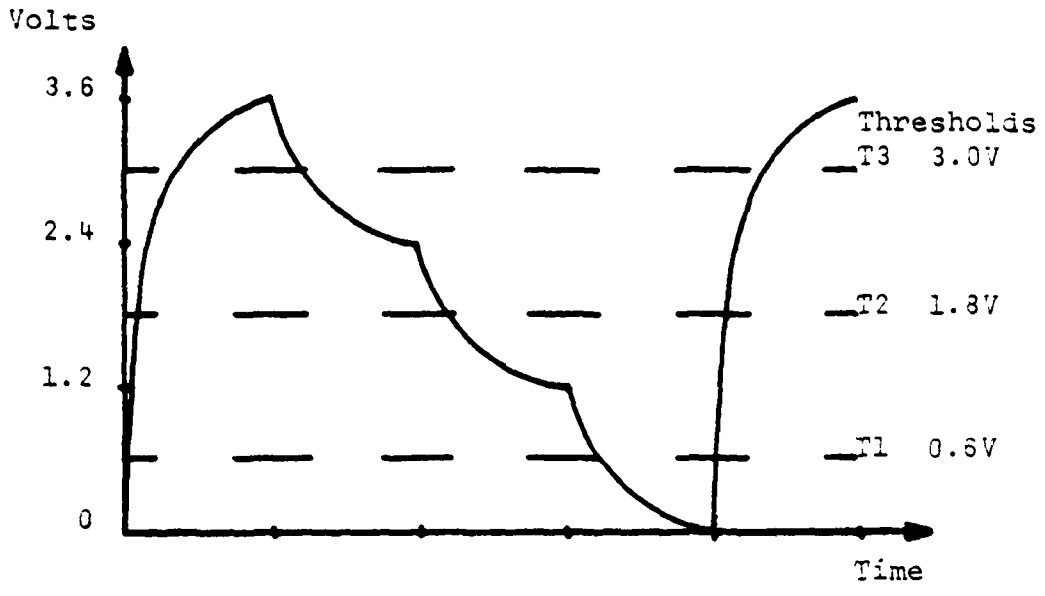


Fig. A.17. Amplitude Decision Circuit Input Levels

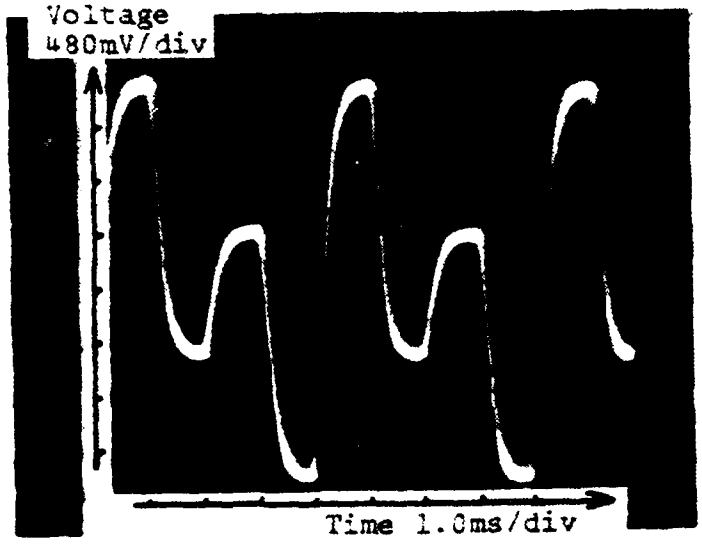


Fig. A.18. Amplitude Comparator Input Signal

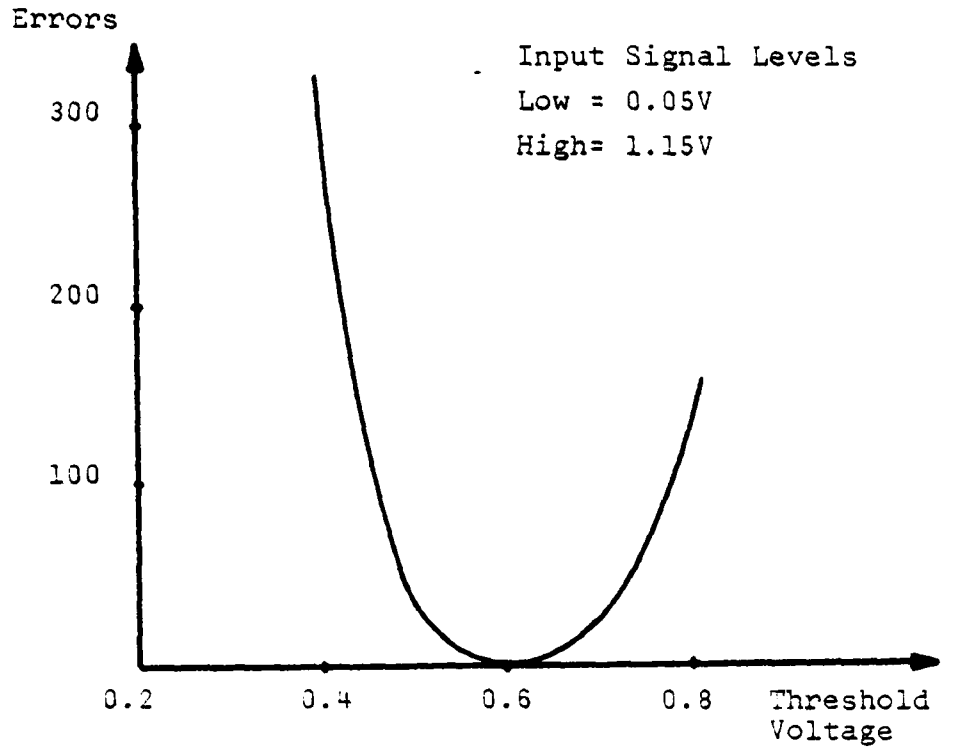
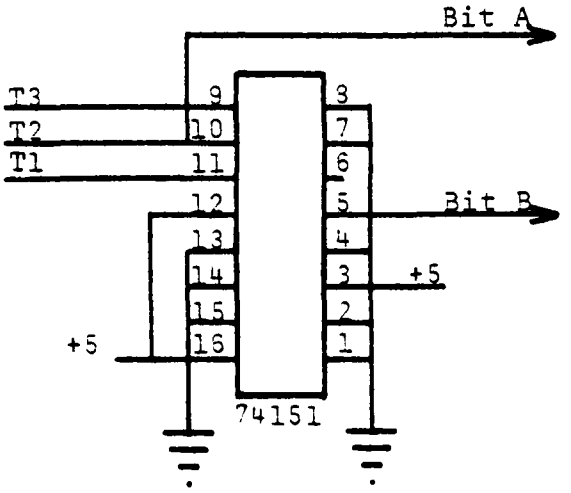


Fig. A.19. Bit Error Rate versus Threshold Voltage

b. Phase Detector

The phase detector is a two-channel coherent multiplier followed by a lowpass filter, a decision circuit, and a decoding circuit (Fig. A.21). Since the circuitry and operation of the in-phase and quadrature channels are the same except for the reference sinusoid, only the in-phase channel is described below.

A phase coherent system is assumed in this experiment. There is no attempt to recover a coherent



Possible Inputs			Data	
T3	T2	T1	A	B
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Figure A.20. Amplitude Data Decoder Truth Table and Circuit Diagram

reference from the received signal. The reference sinusoids are taken directly from the same multi-phase source that supplies the transmitter.

The signal from the predetection amplifier goes through a DC blocking capacitor and a voltage follower which isolate the phase detector from the rest of the system (Fig. A.22). A signal conditioner corrects for phase shift introduced by the transmission system and removes the

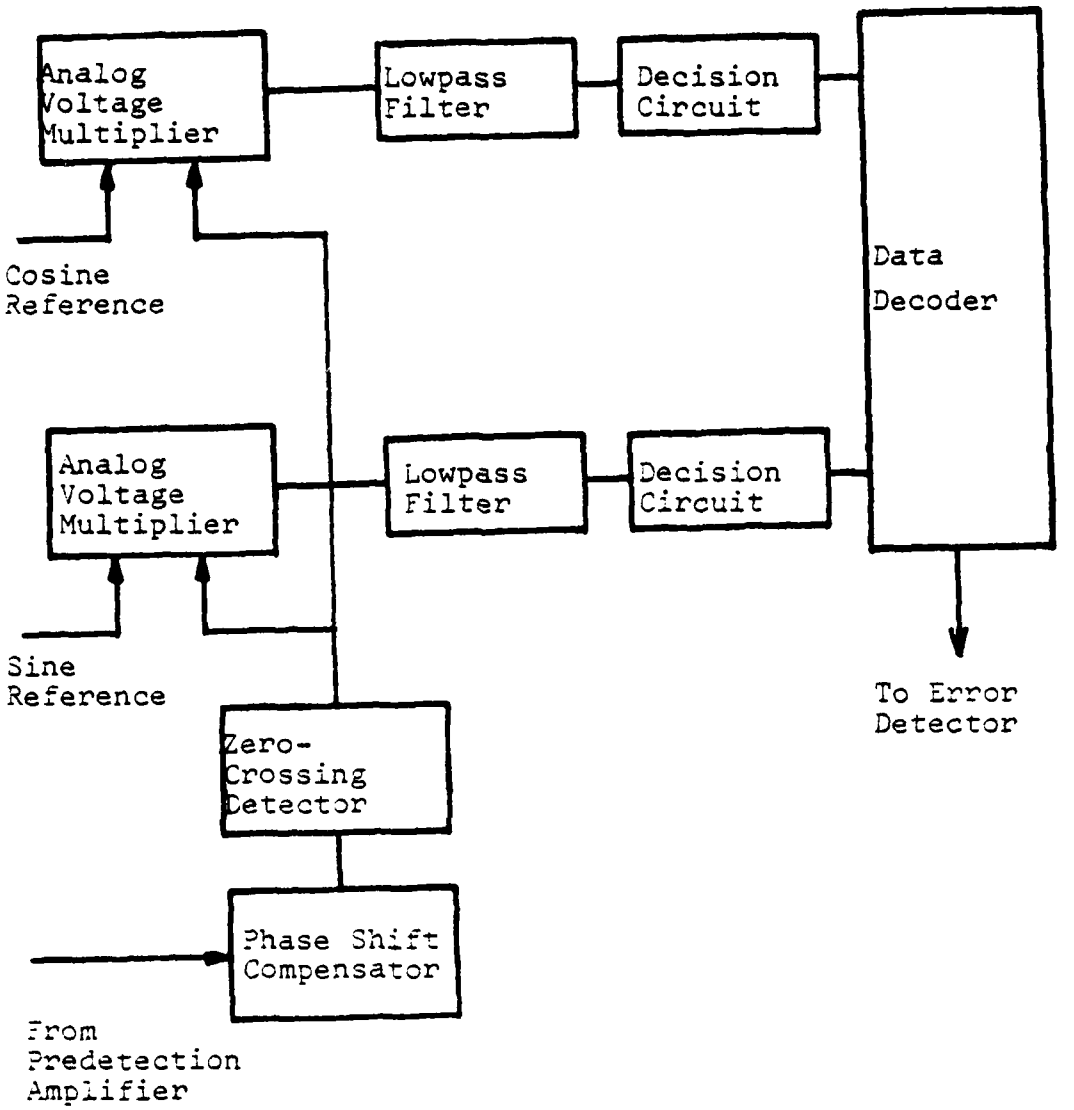


Fig. A.21. Phase Detector Block Diagram

amplitude variations. The phase shift compensator can be adjusted by the following procedure:

1. Transmit a sinusoid with phase reversal modulation.
2. Compare the inputs to the multiplier using Lissajous patterns.

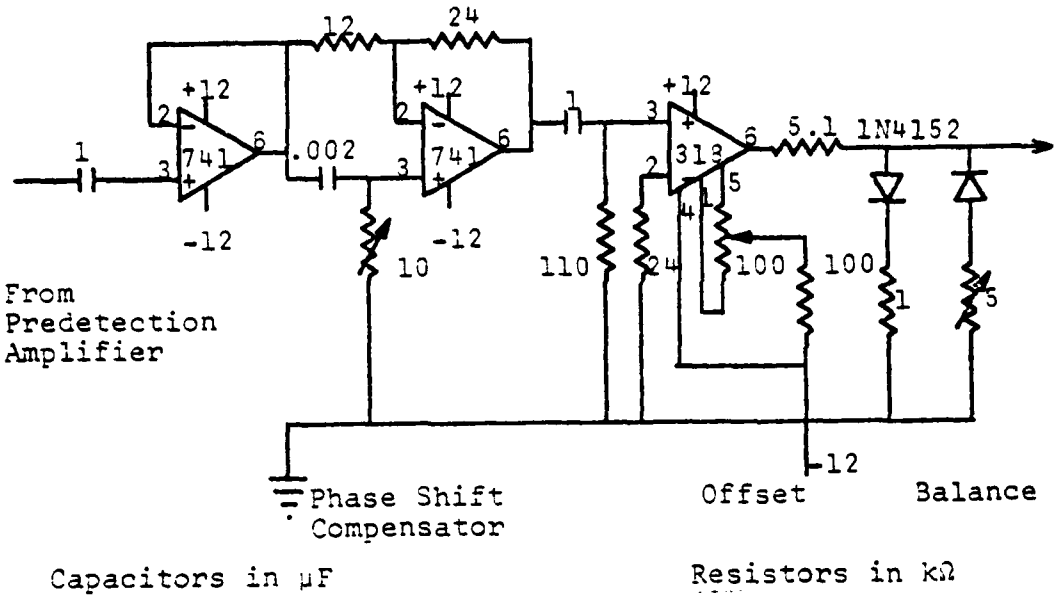


Fig. A.22. Signal Conditioner Circuit Diagram

3. Adjust the phase compensator to produce a display corresponding to phase coherence.

A zero crossing detector removes amplitude information by producing a square output clipped at about ±2.3 V for input to the multiplier. This signal retains the phase information. The offset control adjusts the relative duration of the positive and negative excursions of the resulting square wave. The balance control balances the magnitude of the positive and negative excursions.

The basic element of the phase detector is an analog voltage multiplier (Fig. A.23). The output of the analog voltage multiplier is the instantaneous product of the reference sinusoid and signal square wave. This product integrates over time to +V if the two are in phase, -V if they are out of phase, and 0 if they are in quadrature. The multiplier also includes an offset control to compensate for all offsets in this branch of the system. The nominal measured voltage at this summing input of the analog voltage multiplier is 36 mV. This must be held to ±2 mV to maintain satisfactory phase detector performance. The product from the analog voltage multiplier goes through a buffering voltage follower to an amplifier. The amplifier includes a gain control to present the correct voltage levels to the comparators. A lowpass filter removes the high frequency components.

The decision devices are comparators configured for TTL compatible outputs as are those in the amplitude decision circuit (Fig. A.24). The input signal to the phase decision circuit is a three-level voltage with +V, -V, and 0 representing respectively in-phase, out-of-phase, and quadrature input signals (Fig. A.25). The comparators will

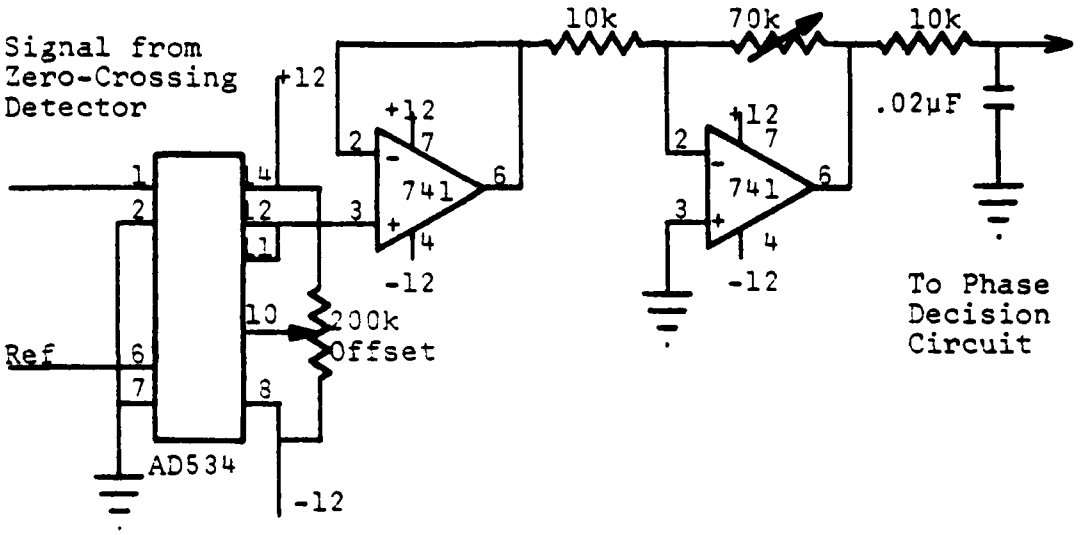


Fig. A.23. Multiplier and Lowpass Filter Circuit Diagram

respond only to inputs between 0 and 4 V. The incoming signal is applied to a diode and sent to one comparator and it is inverted, applied to a second diode, and sent to the other comparator. Both comparators then see positive input voltages. The gains of the amplifiers in the system are set to make the input voltage range at the comparators 0 to 3.6 V. The threshold is 1.8 V. The waveform at the comparator input is in Fig. A.26.

The phase data decoder has as inputs the outputs of four comparators estimating two data bits with a straight binary code according to the truth table in Fig. A.27. The

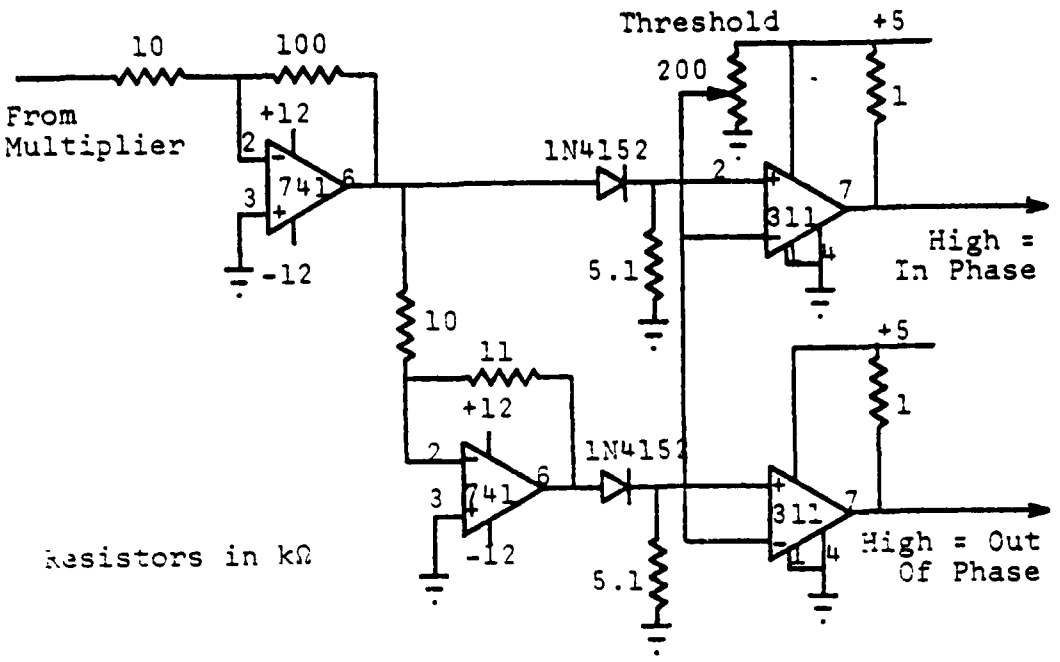


Fig. A.24. Phase Decision Circuit Diagram

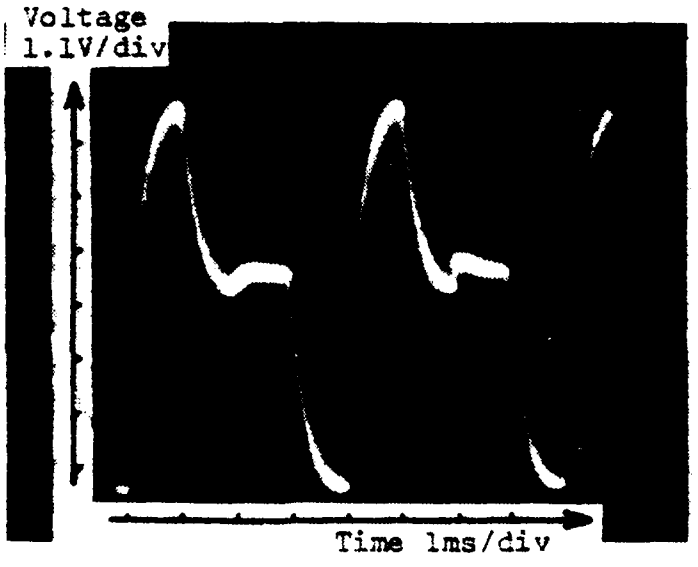


Fig. A.25. Phase Decision Circuit Input

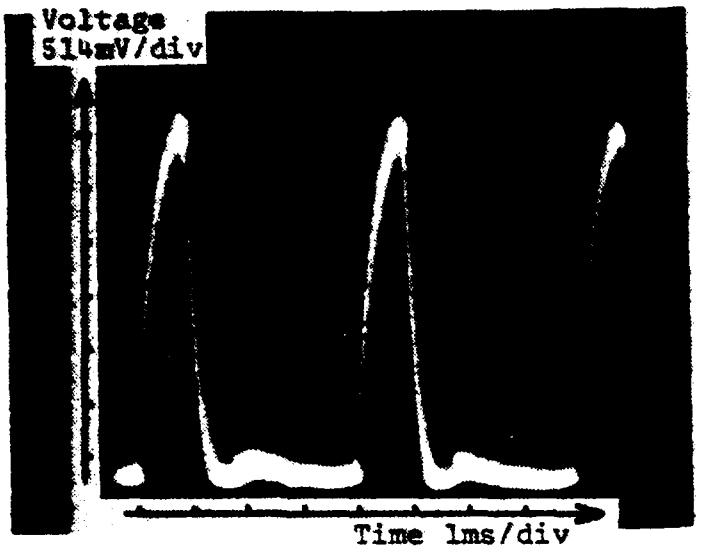
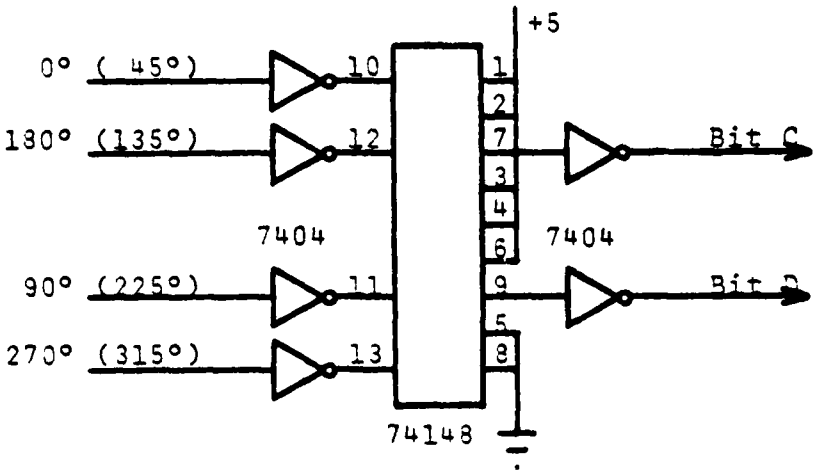


Fig. A.26. Phase Detector Comparator Input

decoding is by a 74148 priority encoder. The 74148 is a negative logic device, so all signals must be inverted.

3. Multi-Phase Source

The transmission system requires up to six sinusoids of the same frequency but different phase angles for coherent operation. The phase shift circuits of Stout and Kaufman with minor modification provide a convenient method for generating the necessary phase shifts and controlling the output amplitudes of the needed signals given a common input sinusoid (Fig. A.28) [Ref. 5].



Angle	C	D
0° (+45°)	0	0
90° (+135°)	0	1
180° (+225°)	1	0
270° (+315°)	1	1

Figure A.27. Phase Data Decoder Truth Table and Circuit Diagram

The input oscillator is a Hewlett-Packard HP 204C. The chosen operating frequency is 30 kHz.

The circuit is constructed with 747 (dual 741) operational amplifiers (Fig. A.29). These amplifiers work well at the frequency and amplitudes used. The variable feedback resistors control the gain. The variable resistors to ground adjust phase. There is some interaction between these controls, so peaking adjustments are necessary.

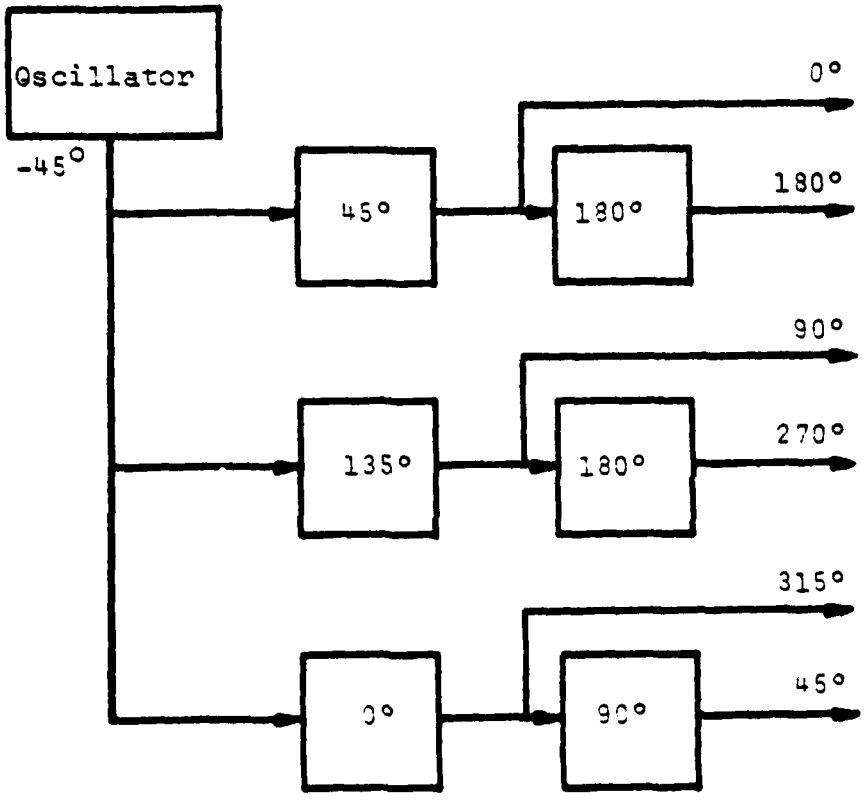


Fig. A.28. Multi-Phase Source Block Diagram

Figure A.30 shows the outputs of an 8-phase source constructed for this research with the input signal superimposed.

C. TEST SYSTEM

The test system provides test data to the transmitter, receives the estimate of the data from the receiver, and records errors (Fig. A.31).

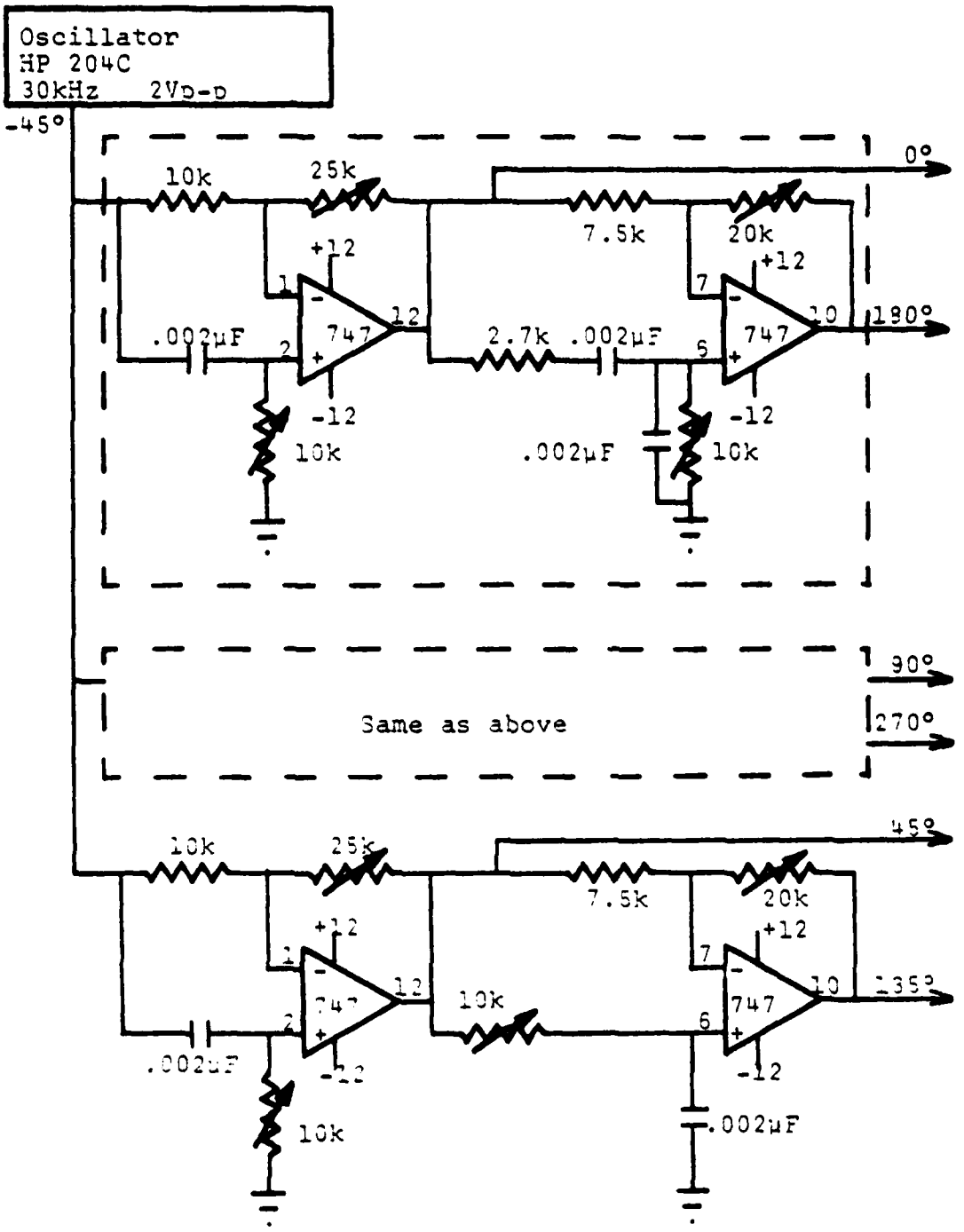


Fig. A.29. Multi-Phase Source Circuit Diagram

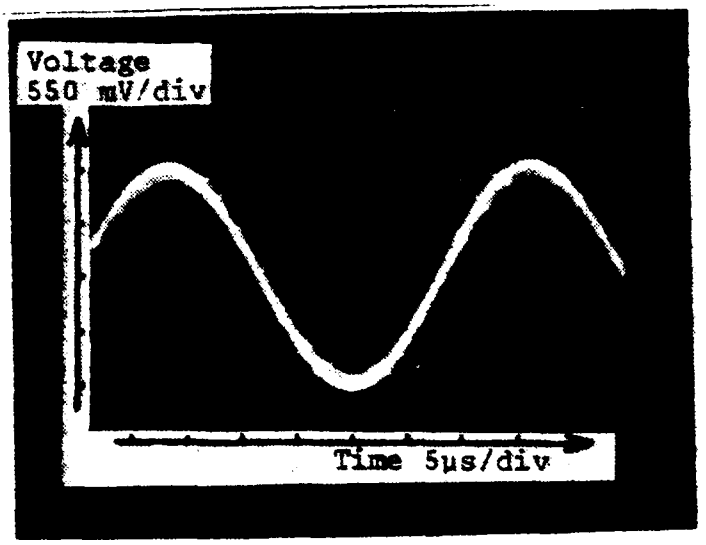


Fig. A.30. 8-Phase Source Output

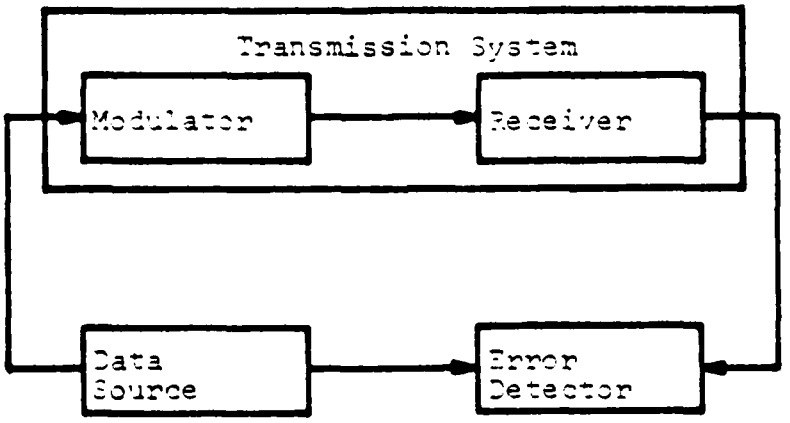


Fig. A.31. Test System Block Diagram

1. Data Source

The data source is a 16-stage pseudo-random sequence generator with feedback taps from stages 16, 15, 13, and 4 (Fig. A.32) [Ref. 6]. This connection generates a maximal length sequence of 65535 bits. The data generator has provision for getting out of the forbidden state (all 0) by taking the parallel load enable high momentarily. Rarely was this necessary and then only on start-up. The parallel load enable could have been tied to the system CLEAR, but this was not done to randomize the starting point within the data sequence on each test run.

The data source also has a serial to four-bit parallel converter since the transmission system handles four bits in parallel (Fig. A.33). The serial data stream is clocked into a four-bit shift register and latched every fourth bit. The latch output goes both to the modulator and to the test system for later comparison with the received estimate.

2. Error Detector

The error detector detects bit errors (Fig. A.34). While symbol errors may be more meaningful in an operating system, bit error identification in this evaluation system

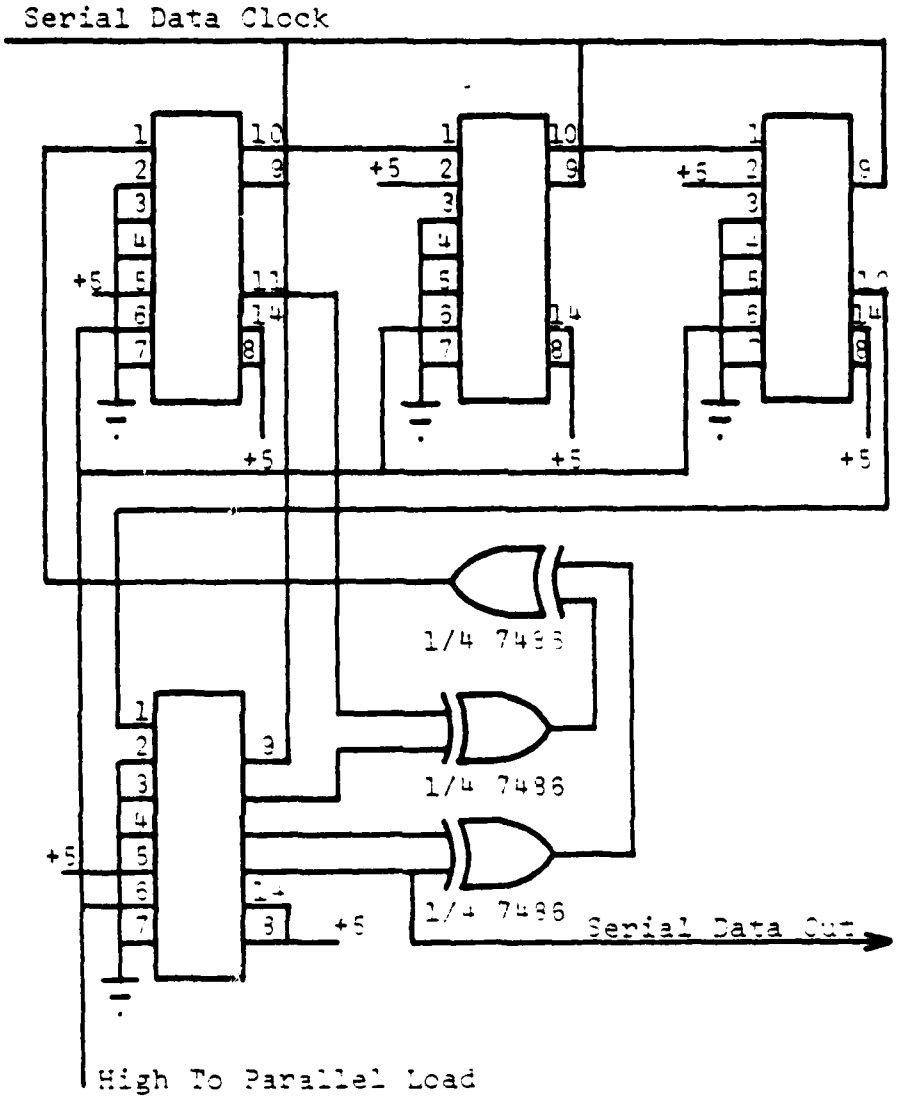


Fig. A.32. Pseudo-Random Sequence Generator Circuit Diagram

allows one to trace the source of the error. At the end of the current symbol period, the hold latch receives a copy of the parallel data which has been transmitted through the

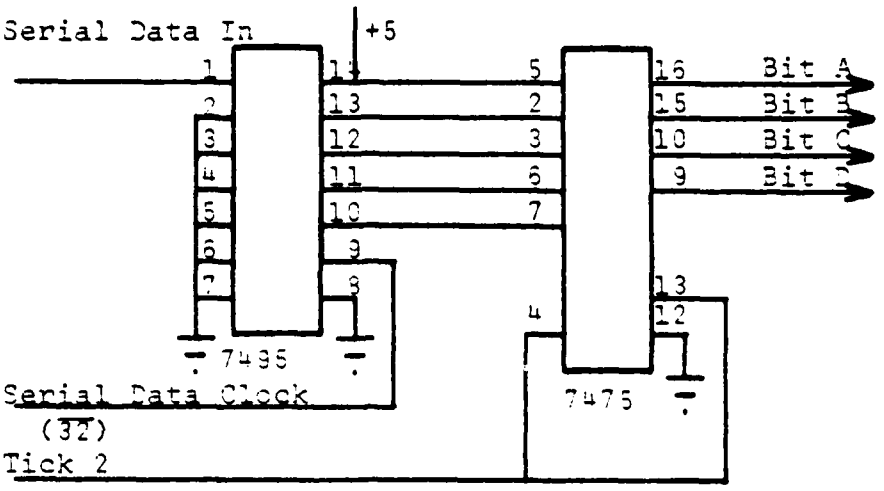


Fig. A.33. Serial to Parallel Converter Circuit Diagram

system. The output latch receives the estimate of the data from the receiver data decoders at the same time. At the beginning of the following symbol period the hold and output shift registers receive the data from the respective latches. The output serial data clock shifts the data through the shift registers at 4 kHz or 4 times the symbol rate. An exclusive-or gate compares stage 4 of the shift registers. A difference is presented as a high to an AND gate. If the data count pulse simultaneously is high, the error counter receives the pulse and counts an error.

It is possible to use the error detector circuit to look at a subset of the output data by making the

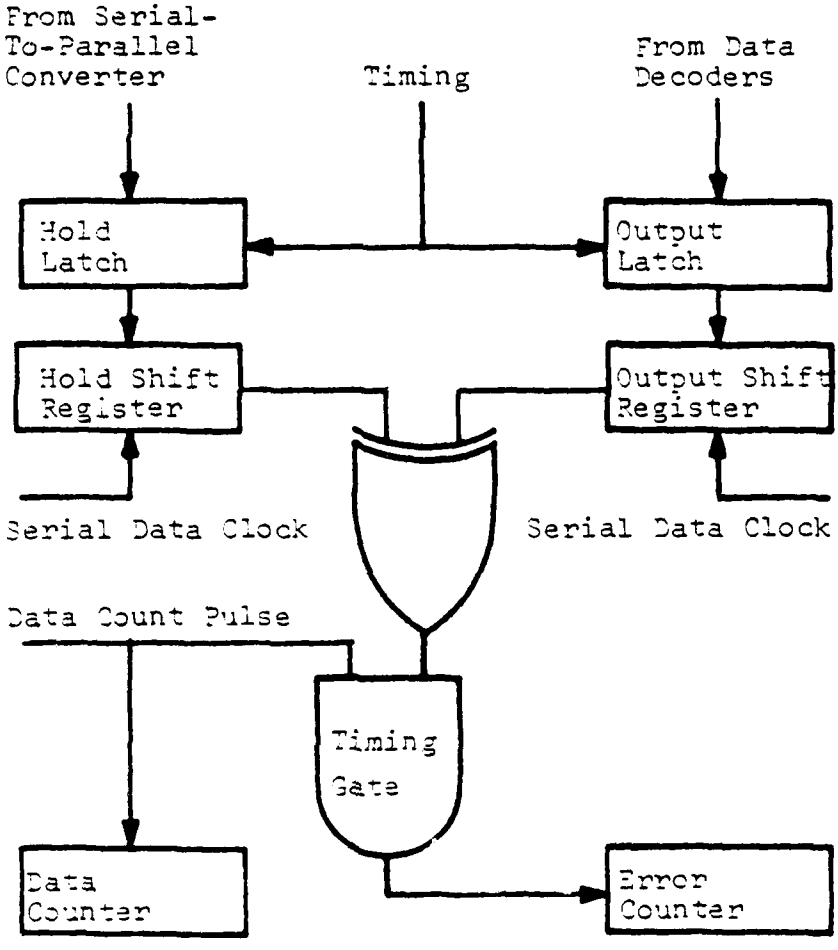


Fig. A.34. Error Detector Block Diagram

exclusive-or gate compare the proper stage of the shift registers. If, for example, the exclusive-or gate gets its input from stage two, only two bits will be compared during the symbol period. Four bits will be seen by the

exclusive-or gate, but since the serial input to the shift registers are grounded, the last two bits will always be low. Using this technique one can determine selectively the performance of the amplitude and phase modulation systems. It is necessary only to insure the bits of interest are loaded into the proper stages of the hold and output latches and consider the reduced number of bits being compared.

3. Counters

The test system has two counters, a bit counter and an error counter. The basic counter is a three decade counter and display circuit (Fig. A.36). The error counter is just a basic counter with the count input coming from the error detector. The data bit counter has a basic three decade counter preceded by a two decade divider for a 100,000 bit count capacity (Fig. A.37). The carry-out of the high order stage is the STOP COUNT pulse. This makes the system count 100,000 data bits and the errors made in those 100,000 bits and stop. The count input for the bit counter comes directly from the system data count pulse source. The system CLEAR clears both counters.

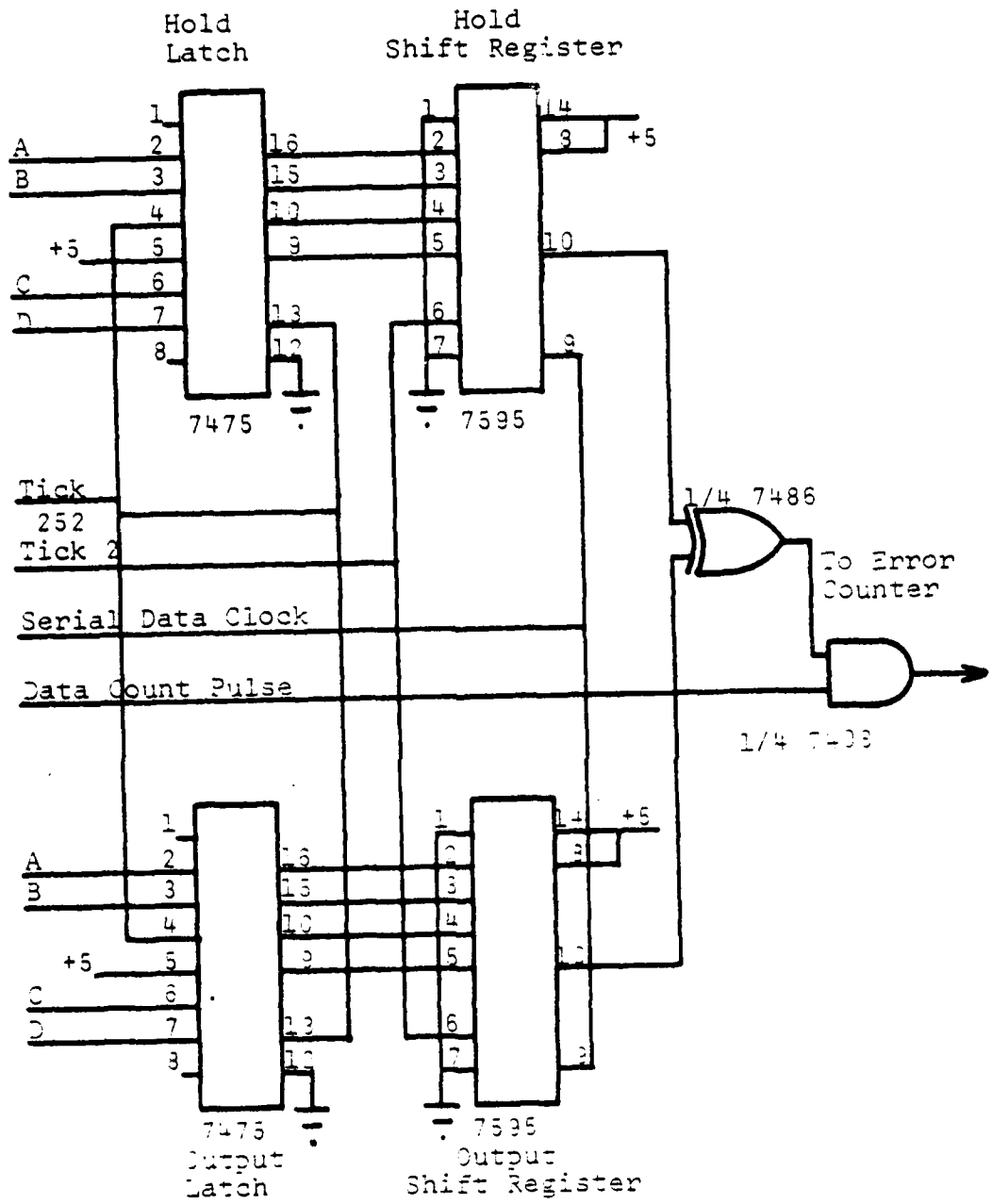


Fig. 7.35. Error Detector Circuit Diagram

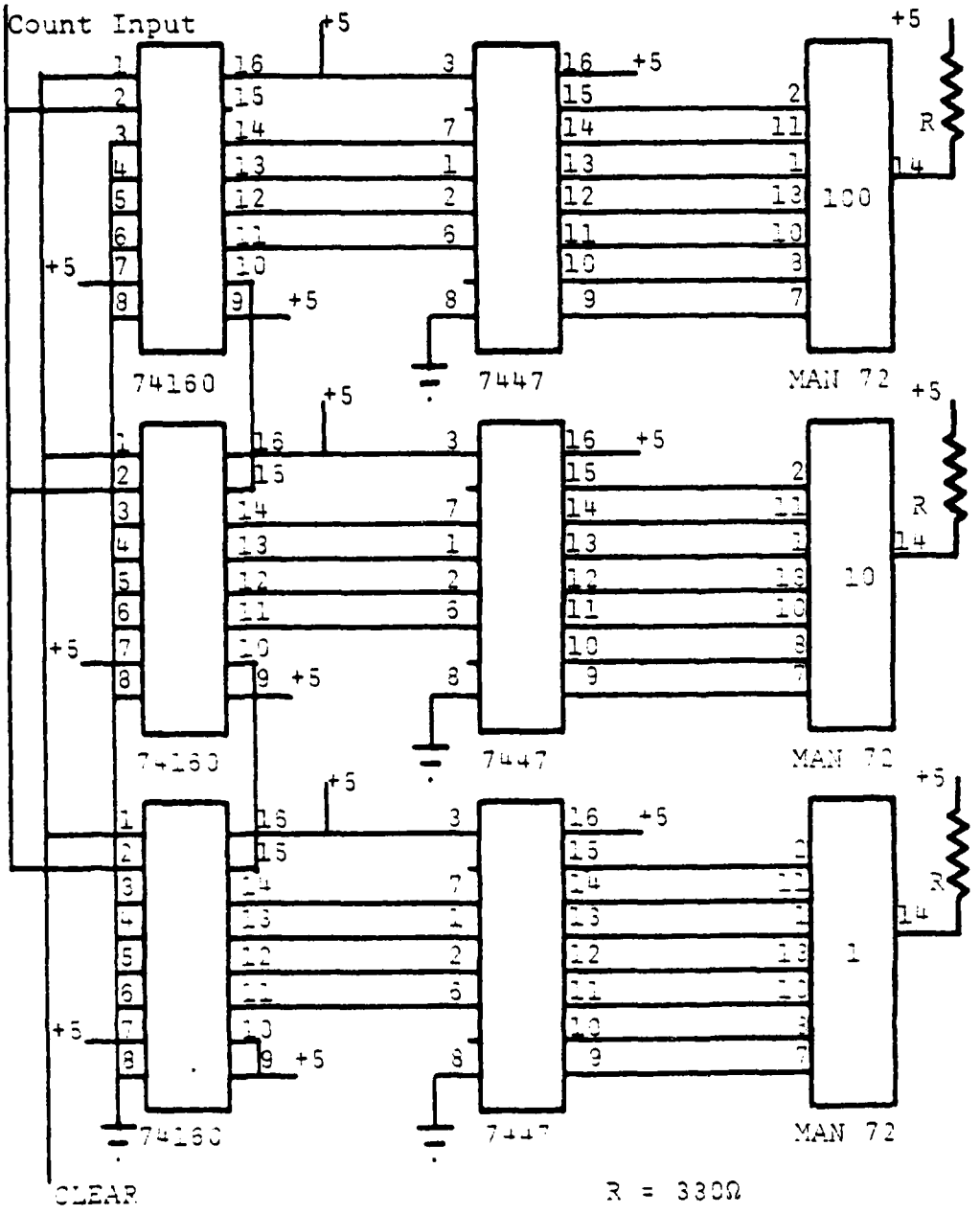


Fig. A.36. Basic Counter Circuit Diagram

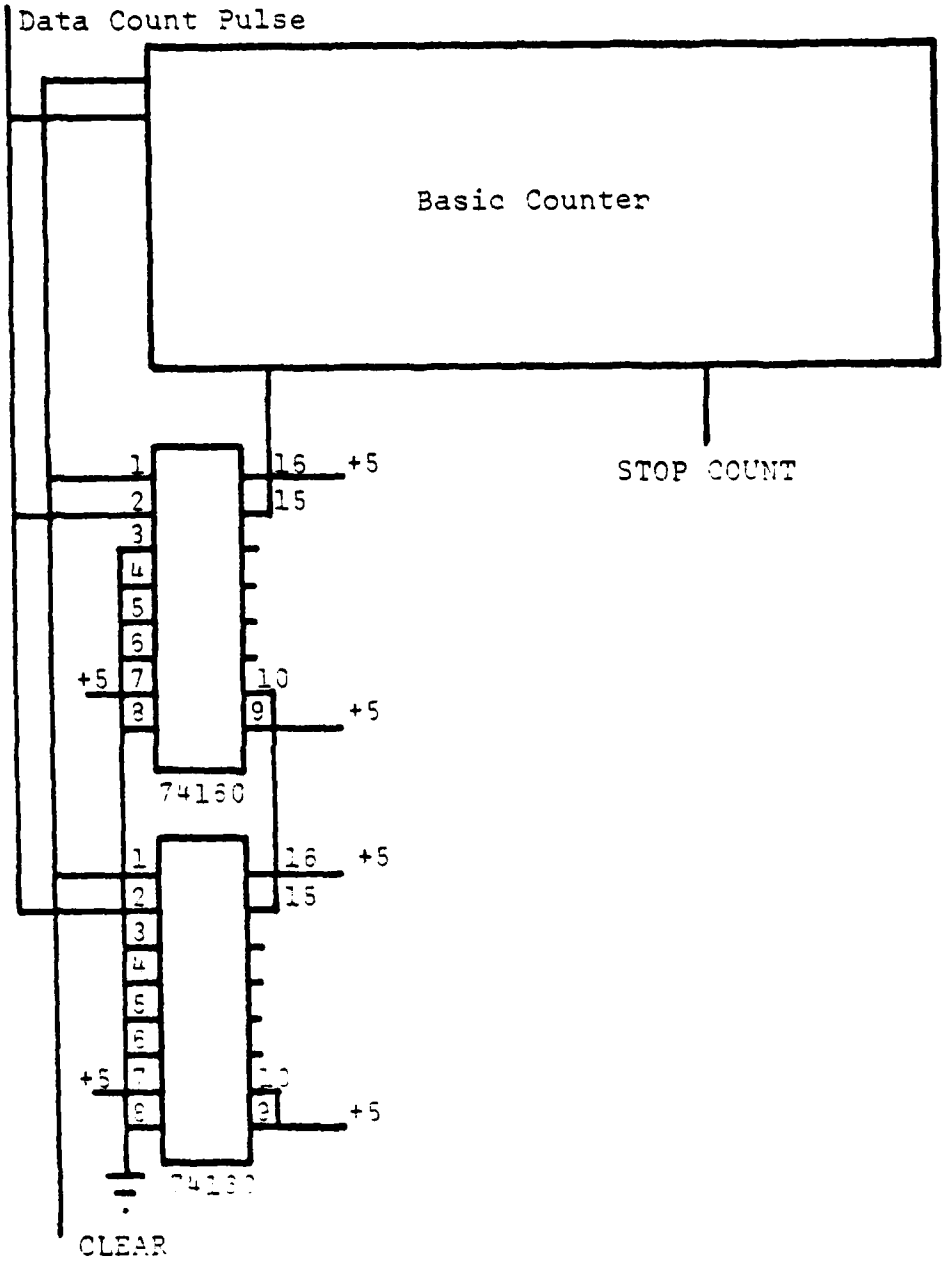


Fig. A.37. Data Bit Counter Circuit Diagram

D. TIMING SYSTEM

1. Timing Requirements

The timing system provides synchronization between the transmitter and receiver and clocks the test system. The symbol period must be clearly defined so the received symbol can be sampled near the end of the period. This symbol period defines the operating rate of the entire experimental system.

A symbol rate of 1 kHz was chosen as a reasonable, illustrative rate that avoids the complications introduced by high speed timing. This rate corresponds to a data rate of 4000 bits per second or the equivalent of 500 ASCII characters with parity per second. The highest frequency required is the master clock which has only to run at 256 kHz to give all the flexibility required.

The required timing functions include transmitter and receiver symbol timing, data source clocking, and error detector timing. The timing diagram (Fig. A.38) illustrates these relationships. References to line numbers in the following discussion refer to lines of the timing diagram. The master clock operates at 256 times the symbol period. The smallest definable interval is one tick (period) of the master clock. Ticks 0 through 255 define one symbol period.

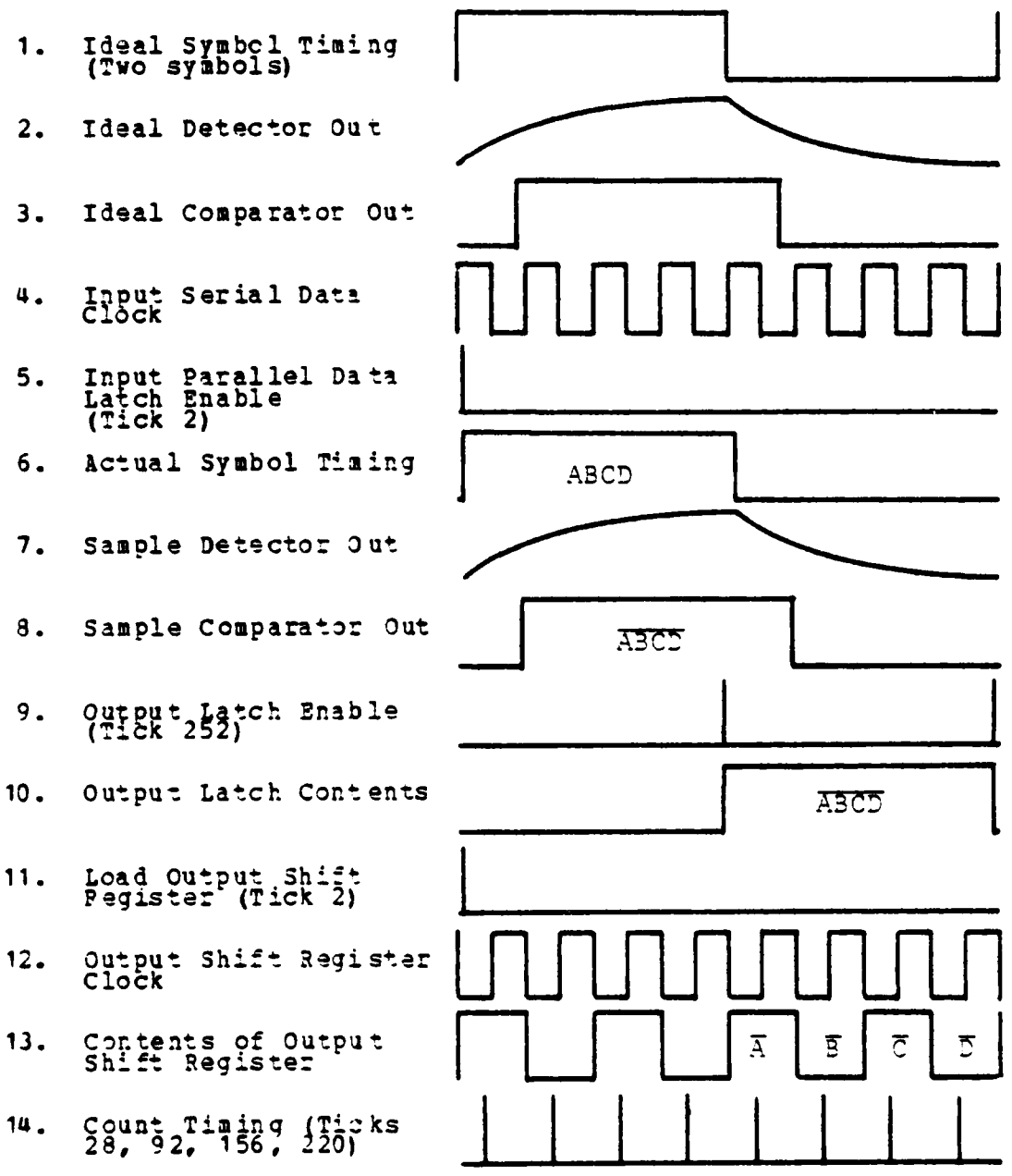


Fig. A.38. System Timing Diagram

The ideal symbol (Line 1) defines a time frame within which all other timing functions must be defined. Given the ideal symbol, the detector output would resemble Line 2 and the comparator output would resemble Line 3. All comparators will reach their final state before the end of the period and will remain high for some time into the following symbol period. The actual waveforms are shifted somewhat from the ideal to avoid the edge effects at the symbol boundries. The definitive timing standard is the master clock.

The master clock defines 256 ticks per symbol which may be divided or logically extracted to clock and time all system functions. Serial data must be clocked and latched to present a 4-bit parallel word to the modulator at the beginning of the symbol period. The data estimate from the detector decoders must be sampled at the end of the symbol period. The input and output data must be latched, loaded into shift registers, and clocked out for comparison. The individual bits must be counted and, simultaneously, the errors must be counted. All handling and counting of data must be timed to occur when the data are valid.

The inverted 4 kHz timing output (Line 4) clocks the serial data source and the input shift register. Since the shift registers shift on the negative-going edge of the clock, this signal is inverted to make the data valid at the time the data latch samples it. This input timing places a new set of valid data in the input shift register 32 ticks before the end of the symbol period and leaves it there for the first 31 ticks of the following period.

The input parallel data latch is enabled by tick 2 (Line 5). This timing marks the beginning of the actual symbol period. It is not necessary to delay the symbol to tick 2, but tick 2 is used elsewhere and is convenient here. With the symbol period defined by tick 2, the actual symbol timing is as shown on Line 7. Representative detector and comparator outputs are shown on Lines 7 and 8 respectively.

The output data must be sampled near the end of the symbol period when the comparators are most likely to be at the final value. The output latch is enabled by tick 252 (Line 9). Tick 252 also enables the input hold latch to preserve the transmitted data for comparison with the received data. The contents of the output data latch and input hold latch are valid from tick 252 of the symbol

period to tick 252 of the following period (Line 10). That provides a stable sampling of the data for the comparison shift registers to read.

The comparison shift registers load on tick 2 (Line 11) and shift at the same rate as the input serial data source (Line 12). They, however, use the uncomplemented clock which moves the bits uniformly throughout the symbol period (Line 13). This uniform timing makes counting convenient.

Both the bit counter and the error counter are enabled approximately midway during each of the four bit intervals within the symbol period. The timing pulses occur at ticks 28, 92, 156, and 220 (Line 14). Each of these four ticks is counted as a data bit. An error is recorded only if the error detector output is high during one of these ticks.

2. Timing System Hardware

The timing system has a divider and a pulse generator to provide clocking for all sections of the experimental system (Fig. A.39). The master clock is a Wavetek Model 142 HF VCG Generator with a square pulse output at 256 kHz. The divider provides eight binary

weighted outputs. The outputs from the combinational logic circuit are the timing pulses needed in both the transmission and test systems.

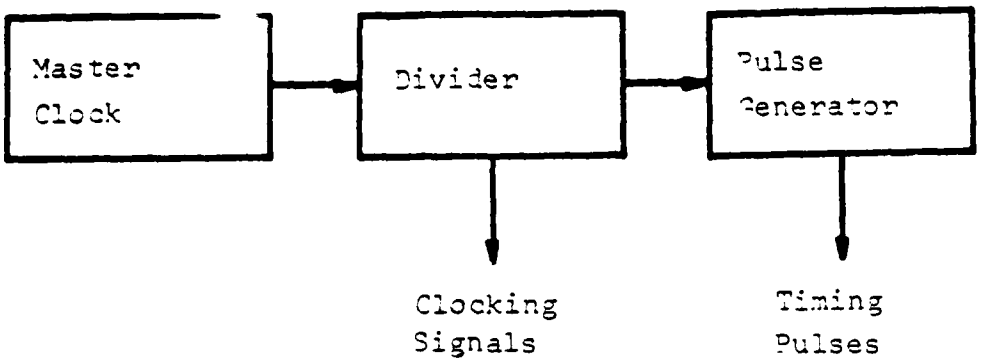


Fig. A.39. Timing System Block Diagram

a. Clock Divider

The clock divider is a pair of 74161's cascaded with outputs from all divider stages. Some of the outputs are available complemented to provide the signals required by both the combinational logic of the pulse generator and the synchronization of the experimental system. Figure A.40 is the schematic diagram of the clock divider.

b. Pulse Generator Combinational Logic

The combinational logic curcuit is built around 74151's, one-of-eight data selectors, which provide a convenient way to generate complicated logic functions with

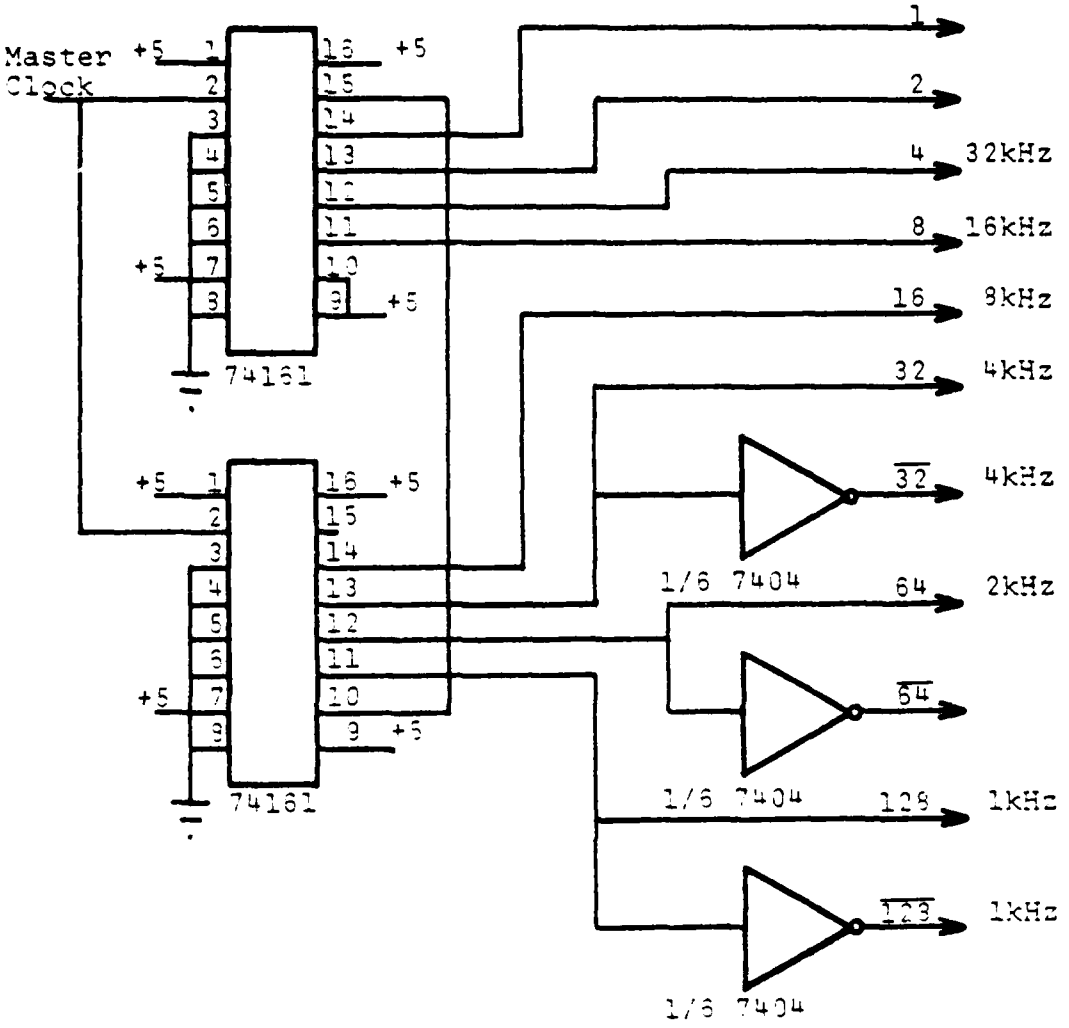


Fig. A.40. Clock Divider Circuit Diagram

a small chip count. These chips, with the use of the INHIBIT line included, can generate any four-bit logic function. The outputs of these data selectors are combined with AND gates to give the specific tick pulses required.

The truth tables for the data selectors are in Tab. II. The outputs of the selectors are sets of pulses which can be combined to give the desired output pulses.

Figure A.41 is the schematic diagram of the combinational logic that generates the timing pulses. All inputs come from the timer divider except the system CLEAR and the STOP COUNT signals. The system CLEAR is a manually activated clear signal used to reset the counters before taking data. The STOP COUNT signal is from the carry out of the last stage of the data bit counter. This arrangement counts 100,000 data bits and sets the flip flop to inhibit the data count pulse output.

TABLE II

Data Selector Truth Tables

Selector 1					Selector 2				
32	1	64	128	Out	2	4	8	16	Out
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0	1	0
0	0	1	0	1	0	0	1	0	0
0	0	1	1	0	0	0	1	1	0
0	1	0	0	1	0	1	0	0	0
0	1	0	1	0	0	1	0	1	0
0	1	1	0	1	0	1	1	0	0
0	1	1	1	0	0	1	1	1	1
1	X	X	X	0	1	X	X	X	0

Selector 3					Selector 4				
1	32	64	128	Out	16	2	4	8	Out
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	1	0	0	0	1	1	0
0	1	0	0	0	0	1	0	0	0
0	1	0	1	0	0	1	0	1	0
0	1	1	0	0	0	1	1	0	0
0	1	1	1	1	0	1	1	1	0
1	X	X	X	0	1	X	X	X	0

NOTE: Column headings are the binary weights of select inputs from the clock divider.

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DESIGN AND OPERATION OF A SIMPLE CIRCUIT USEFUL AS A MODULATOR --ETC(U)
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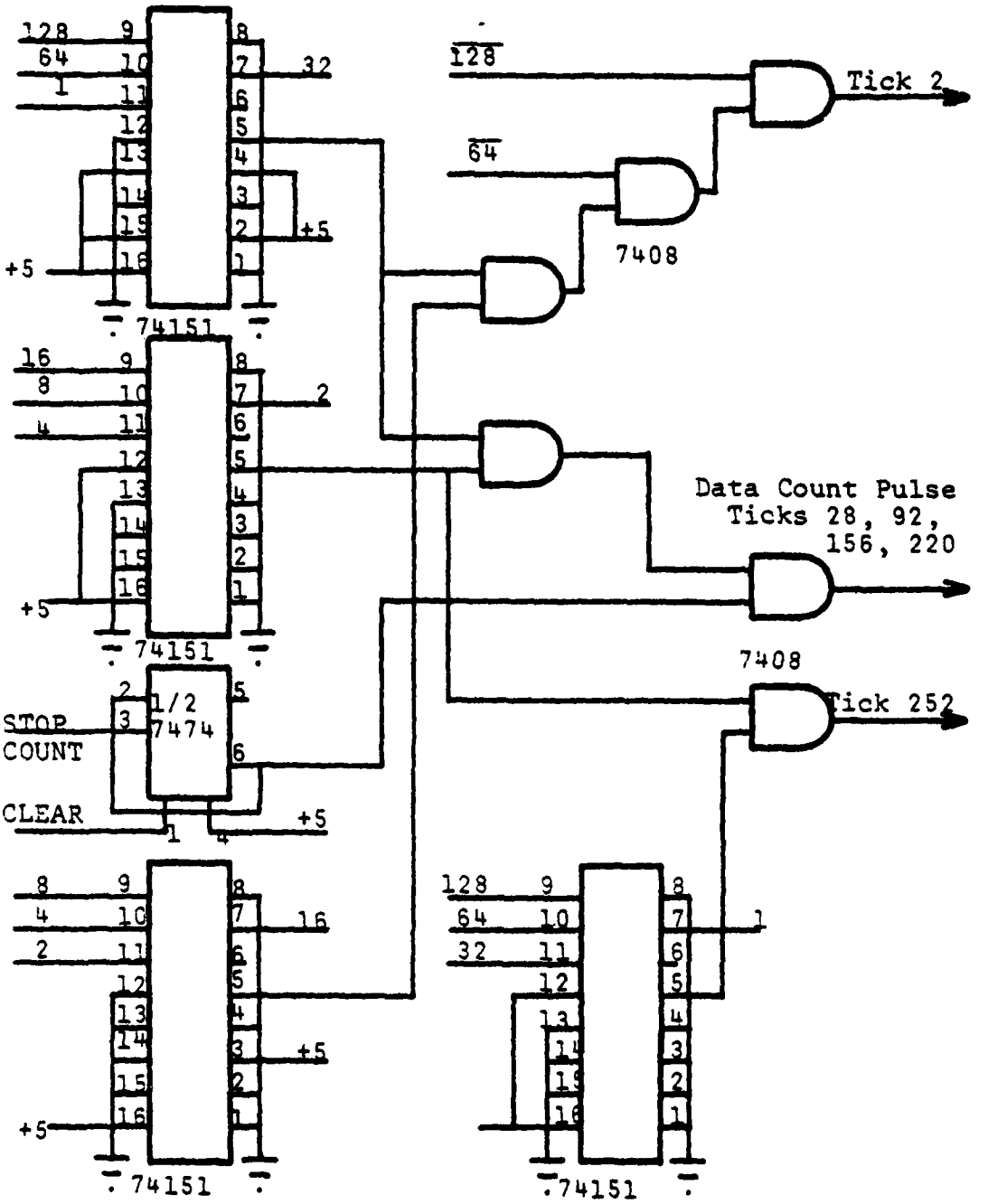

Fig. A.41. Pulse Generator Combinational Logic

APPENDIX B

EPROM PROGRAMMING

The multiplexers of the general analog multiplexer modulator require more control lines in general than the number of data bits represented by each symbol. Some logic is necessary between the data inputs and the multiplexer controls.

The modulator logic and the receiver data decoder logic are related. The choice of an encoding scheme is arbitrary, but once made, the logic at both ends is determined. While the logic can be realized other ways, a memory is convenient. The scheme chosen for this research encodes the first two bits of the input symbol in the amplitude information and the last two bits in the phase information.

The input data bits are a part of the address for a programmable read only memory (EPROM). The address for each phasor is the same as the decoded symbol each phasor represents (Fig. B.1). Each amplitude circle is binary numbered from low to high. That binary number is the first two bits. The four phase angles are binary numbered and represented in the last two bits. That completely determines the data part of the EPROM address.

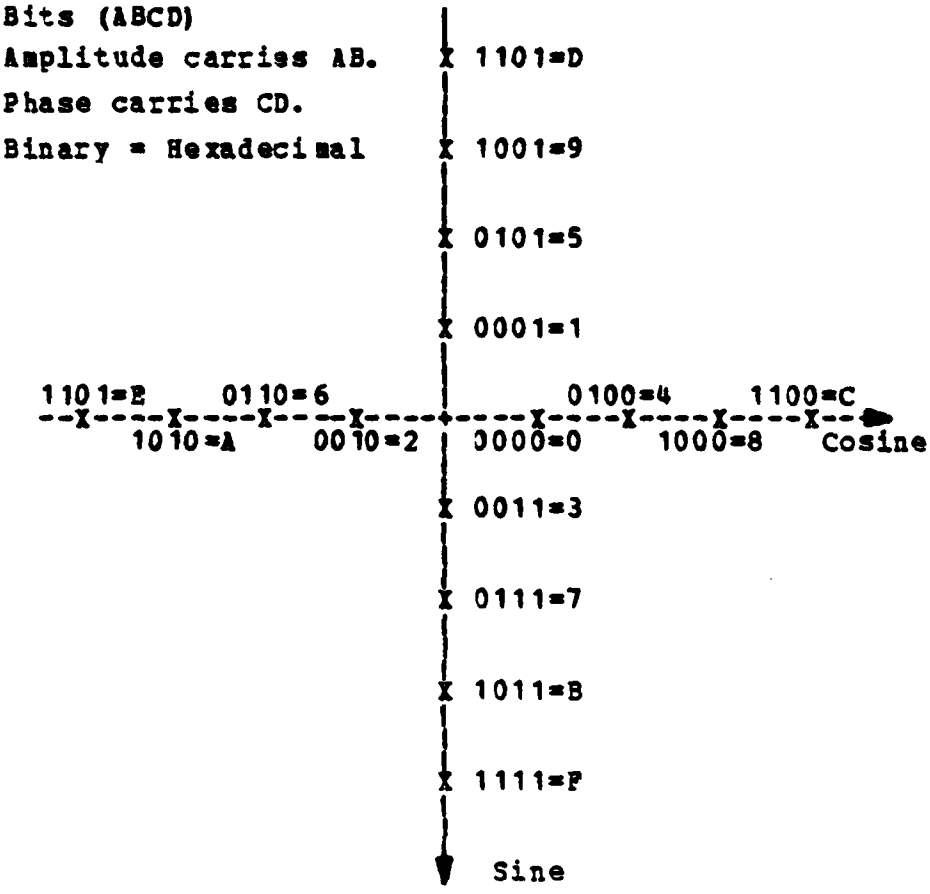

Fig. B.1. Phase Plane Address Codes

The same address pattern, rotated 45°, is used for the rotated phase plane constellation. Another bit in the EPROM address selects between the two constellations. This feature is for experimental convenience here, but it illustrates the flexibility one has with the general analog multiplexer modulator.

Given the address for each phasor, the EPROM data at each address is the control signal set needed to generate

the desired phasor. The 4051 has three switch select lines plus INHIBIT which must be controlled. For this two-multiplexer modulator, an eight-bit word is needed at each address. Arbitrarily the first four bits control the cosine multiplexer and the last four bits control the sine multiplexer. The first bit of each group is the INHIBIT signal. The other three match the binary code of the switch select lines. Figure B.2 shows the EPROM data pattern. The full data word of any possible phasor is made by concatenating the cosine and sine parts as illustrated in Fig. B.3.

The program for the realization of the general analog multiplexer modulator with the constellation on the quadrature axes is in Tab. III. The program that rotates the constellation by 45° is in Tab. IV. Figures B.4 and B.5 diagram the hexadecimal address and data codes for the two constellations.

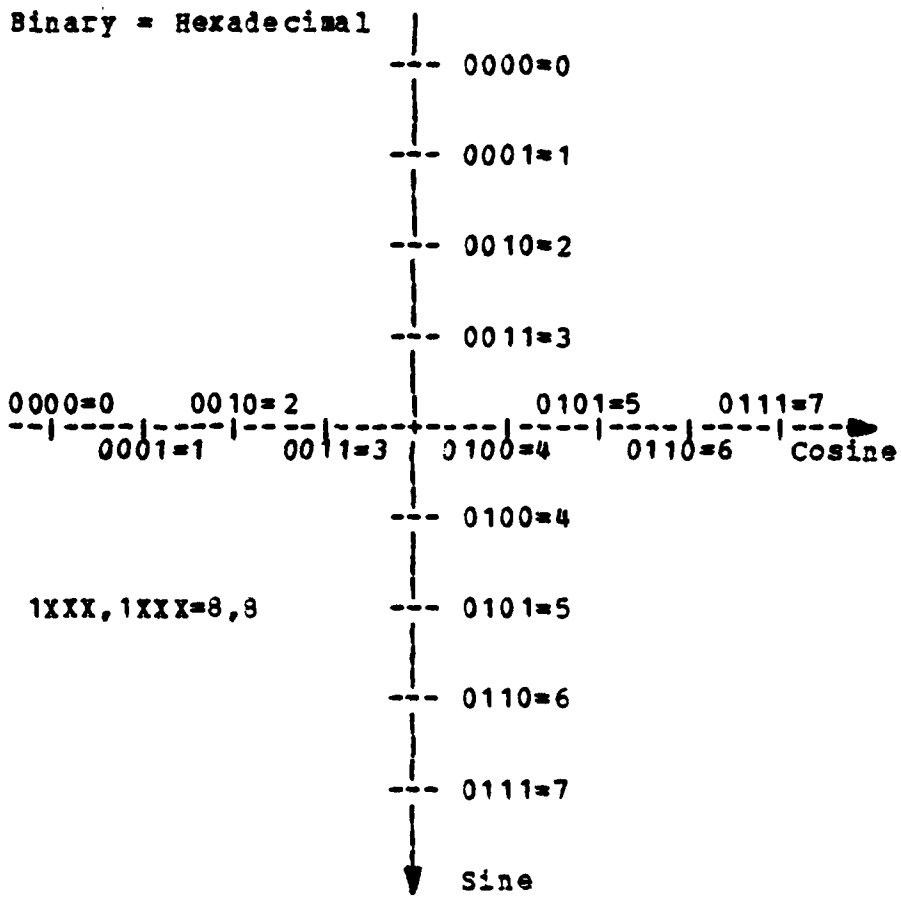

Fig. B.2. Multiplexer Control Codes

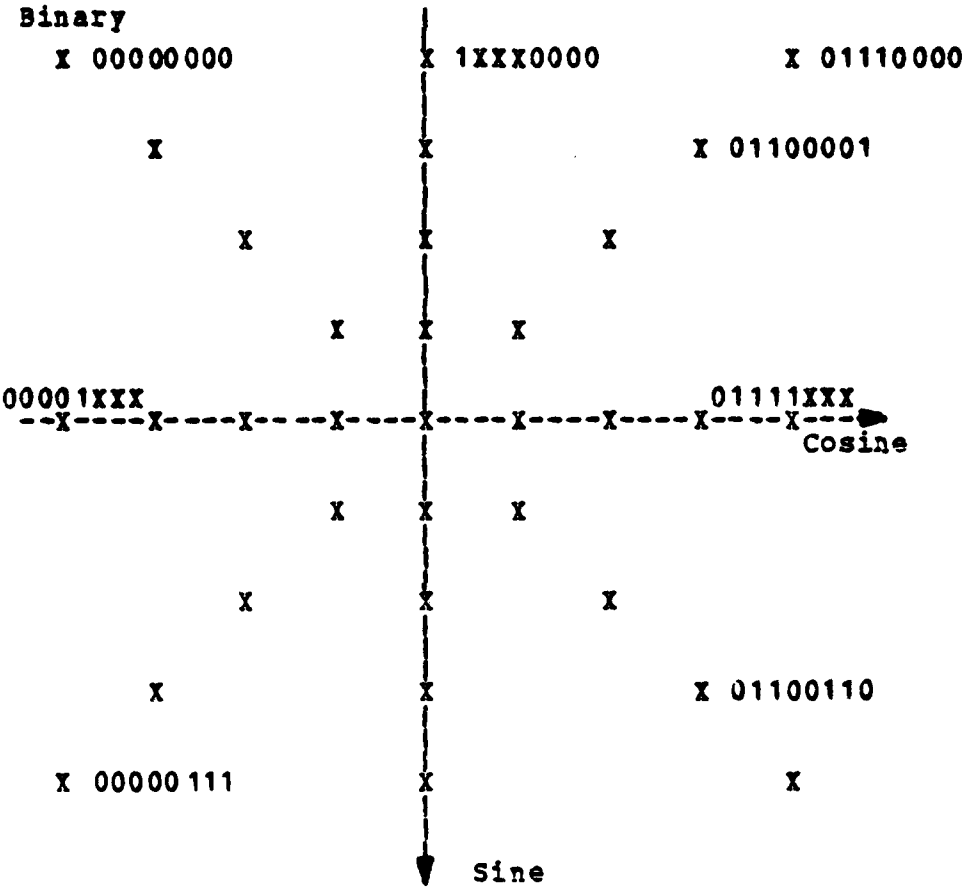

Fig. B.3. Phase Plane Data Codes

TABLE III

EPROM Program - Case 0

EPROM Address			EPROM Output Data	
Dec	Hex	Binary	Binary	Hex
0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0	4 8
0 1	0 0 1	0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 1 1	8 3
0 2	0 0 2	0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 0 0 0	3 8
0 3	0 0 3	0 0 0 0 0 0 0 0 1 1	1 0 0 0 0 1 0 0	8 4
0 4	0 0 4	0 0 0 0 0 0 0 1 0 0	0 1 0 1 1 0 0 0	5 8
0 5	0 0 5	0 0 0 0 0 0 0 1 0 1	1 0 0 0 0 0 1 0	8 2
0 6	0 0 6	0 0 0 0 0 0 0 1 1 0	0 0 1 0 1 0 0 0	2 8
0 7	0 0 7	0 0 0 0 0 0 0 1 1 1	1 0 0 0 0 1 0 1	8 5
0 8	0 0 8	0 0 0 0 0 0 1 0 0 0	0 1 1 0 1 0 0 0	6 8
0 9	0 0 9	0 0 0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1	8 1
1 0	0 0 A	0 0 0 0 0 0 1 0 1 0	0 0 0 1 1 0 0 0	1 8
1 1	0 0 B	0 0 0 0 0 0 1 0 1 1	1 0 0 0 0 1 1 0	8 6
1 2	0 0 C	0 0 0 0 0 0 1 1 0 0	0 1 1 1 1 0 0 0	7 8
1 3	0 0 D	0 0 0 0 0 0 1 1 0 1	1 0 0 0 0 0 0 0	8 0
1 4	0 0 E	0 0 0 0 0 0 1 1 1 0	0 0 0 0 1 0 0 0	0 8
1 5	0 0 F	0 0 0 0 0 0 1 1 1 1	1 0 0 0 0 1 1 1	8 7

TABLE IV

EPROM Program - Case 1

EPROM Address			EPROM Output Data	
Dec	Hex	Binary	Binary	Hex
0 0	0 0 0	0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 0 1 1	4 3
0 1	0 0 1	0 0 0 0 0 0 0 0 0 1	0 0 1 1 0 0 1 1	3 3
0 2	0 0 2	0 0 0 0 0 0 0 0 1 0	0 0 1 1 0 1 0 0	3 4
0 3	0 0 3	0 0 0 0 0 0 0 0 1 1	0 1 0 0 0 1 0 0	4 4
0 4	0 0 4	0 0 0 0 0 0 0 1 0 0	0 1 0 1 0 0 1 0	5 2
0 5	0 0 5	0 0 0 0 0 0 0 1 0 1	0 0 1 0 0 0 1 0	2 2
0 6	0 0 6	0 0 0 0 0 0 0 1 1 0	0 0 1 0 0 1 0 1	2 5
0 7	0 0 7	0 0 0 0 0 0 0 1 1 1	0 1 0 1 0 1 0 1	5 5
0 8	0 0 8	0 0 0 0 0 0 1 0 0 0	0 1 1 0 0 0 0 1	6 1
0 9	0 0 9	0 0 0 0 0 0 1 0 0 1	0 0 0 1 0 0 0 1	1 1
1 0	0 0 A	0 0 0 0 0 0 1 0 1 0	0 0 0 1 0 1 1 0	1 6
1 1	0 0 B	0 0 0 0 0 0 1 0 1 1	0 1 1 0 0 1 1 0	6 6
1 2	0 0 C	0 0 0 0 0 0 1 1 0 0	0 1 1 1 0 0 0 0	7 0
1 3	0 0 D	0 0 0 0 0 0 1 1 0 1	0 0 0 0 0 0 0 0	0 0
1 4	0 0 E	0 0 0 0 0 0 1 1 1 0	0 0 0 0 0 1 1 1	0 7
1 5	0 0 F	0 0 0 0 0 0 1 1 1 1	0 1 1 1 0 1 1 1	7 7

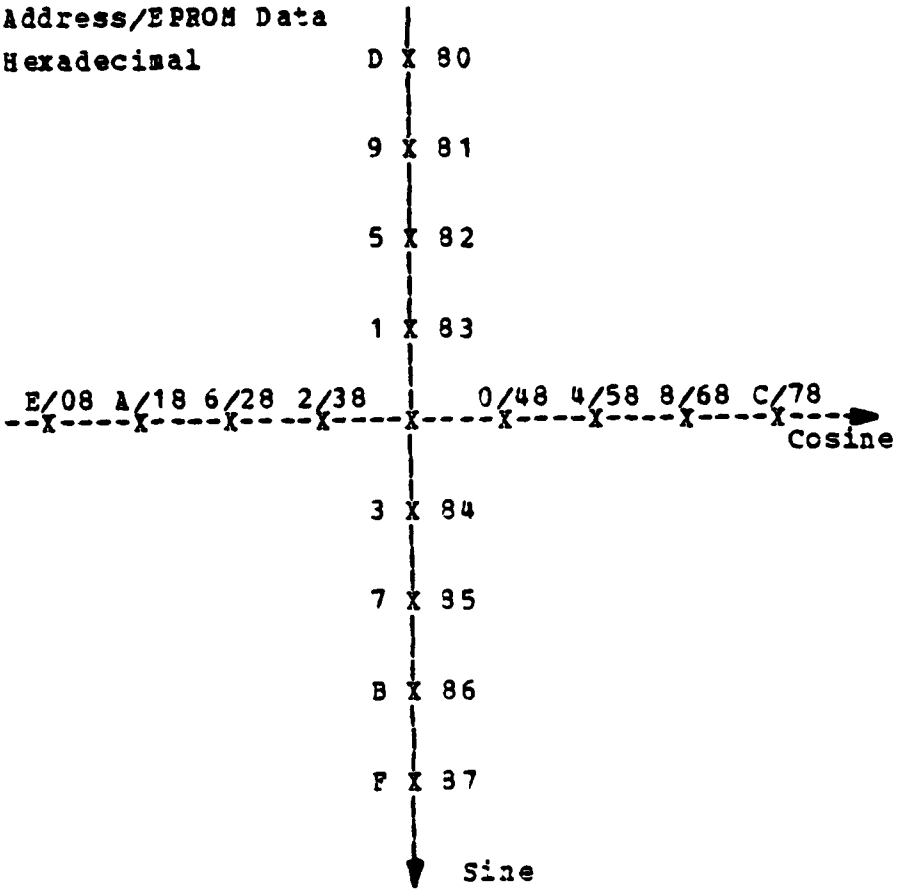

Fig. B.4. Phase Plane Codes - Case 0

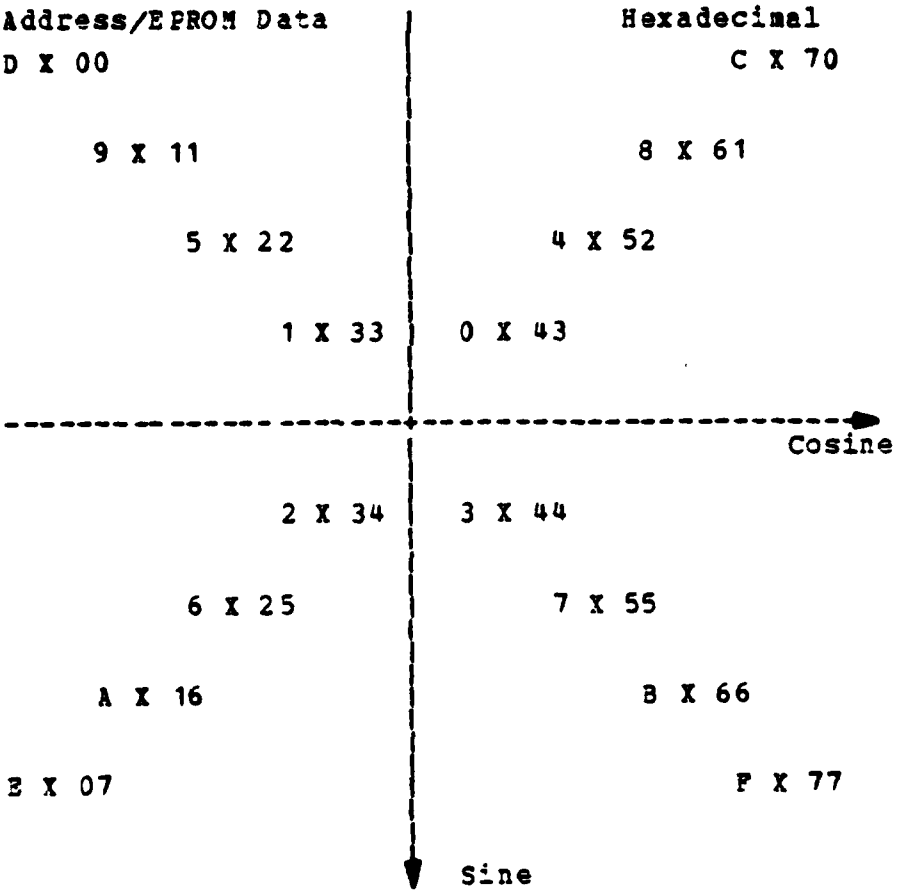

Fig. B.5. Phase Plane Codes - Case 1

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