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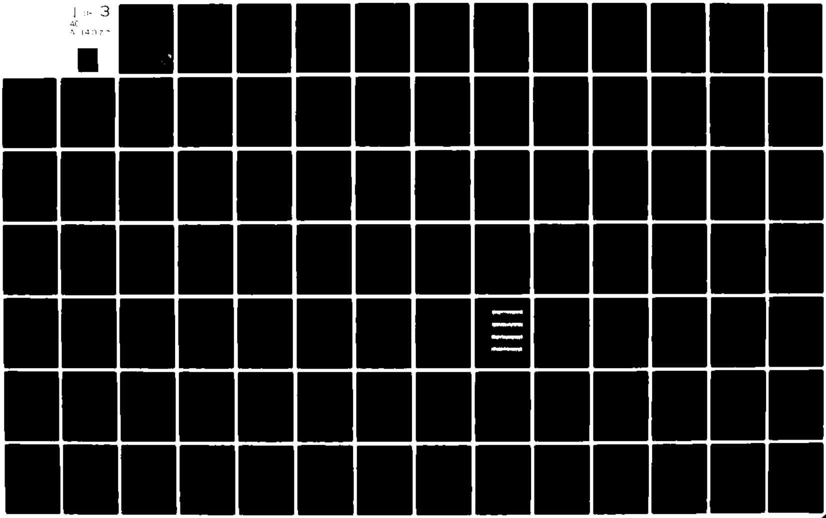

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A PRELIMINARY INVESTIGATION OF CONCATENATED CODING SCHEMES UTILIZING SOFT DECISION PROCESSING

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1 March 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Several preliminary investigations into various concatenated coding schemes were performed. All concatenated schemes passed symbol reliability information from the inner decoder to the outer decoder. All analyses were performed using computer simulation of the communication links. Explicit implementation of digital functions and detailed models of analog functions of the receiver terminal were included in the link simulations. The propagation disturbances were modeled using the multiple phase screen (MPS) propagation simulation. Several concatenated codes were analyzed and their

20. ABSTRACT (Continued)

performance was compared to standard convolutional codes using Viterbi soft decision decoding. Advantages and disadvantages of the various error correction schemes were discussed. Issues relating to quantization effects were given particular attention. An advanced concatenated coding/decoding structure with apparent promise was developed, but has not yet been studied in detail.

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SECTION 1
INTRODUCTION

Coded satellite communication links usually operate under benign channel conditions, but occasionally transionospheric propagation effects disturb the received signal significantly, causing a phenomenon called fading. Links that are jointly optimized for minimum link complexity and benign channel error correction performance are generally unsuited for fading channel conditions. To mitigate the effects of fading, diversity techniques are often added to the benign-channel-optimized receiver. In particular, temporal diversity is introduced by interleaving coded symbols. Though frequency and spatial diversity techniques may also be applicable to the channels of interest, here we shall center attention on time diversity via interleaving with error correction coding.

Coded satellite communication links utilizing interleaving are generally non-optimal for all anticipated fading channels and usually inadequate for some. The key parameters characterizing the fading channel are mean E_b/N_0, bit energy to noise-spectral-density level, and τ_0, the complex electric field decorrelation time. The cost of a satellite link capable of satisfactory operation over the expected range of signal fading conditions can be high because of received power requirements and complex interleaving and coding implementations.

The issue of this preliminary work is the feasibility of a few concatenated coding techniques utilizing temporal diversity that ameliorate fading effects. A second consideration is the digital processing and hardware requirements of these concatenated schemes. A final objective is to use the results of this work to identify new coding schemes that merit future consideration.

As with previous analyses in demodulation and coding theory done by MRC, we rely heavily on detailed computer simulation in this work. Based upon previous studies in nuclear phenomenology, we characterize a typical disturbed ionosphere and specify realistic parameters with which to generate unmodulated sampled-data realizations of baseband received signals via a multiple phase screen (MPS) simulation program. These signal realizations completely represent the propagation channel and are used directly by computer programs that simulate link receivers and post-demodulator signal processors in detail. Our approach here is to implement several coding schemes into the post-demodulator signal processors to quantify their impact on link performance.

Section 2 presents an overview of several topics related to digital communications via satellites. Section 3 documents the verification of a concatenated scheme employing soft decision interfacing (SDI) of the inner and outer codes. Section 4 covers a study of quantization effects in the context of a concatenated scheme where the inner code is channel symbol repetition. Section 5 describes an advanced concatenated scheme that promises satisfactory error correction strength and a relatively simple implementation.

SECTION 2
BACKGROUND MATERIAL

Figure 1 shows a block diagram of a one-way communication link that has a provision for correcting transmission errors. The link is viewed as an error correction encoding/decoding scheme nested about a discrete channel. Throughout this report, the discrete channel is taken as the signal path originating at the transmitter terminal modulator and terminating at the receiver demodulator. Message conditioning and message estimation functions of Figure 1 are indicative of some error correction scheme. Two basic schemes of interest here are the non-concatenated and concatenated structures shown in Figures 2 and 3, respectively. Sections 3, 4 and 5 of this report document three separate, but not disjoint, investigations of concatenated codes. To reduce repetition in these subsequent sections, the discussion of all material common to these sections is given here. Also a standard nomenclature and notation is established to further unify the report. The first part of this section will center on error correction. A discussion contrasting standard concatenation with SDI concatenation is followed by descriptions of important link components such as quantizers, encoders, soft decision decoders, interleavers and deinterleavers. Next we detail our approach to link simulation. The section ends with a discussion of the discrete channel.

The important aspects of this report are found in the three sections to follow. No one of these sections is dependent upon the whole of this section. Hence we recommend that the reader briefly glance over this

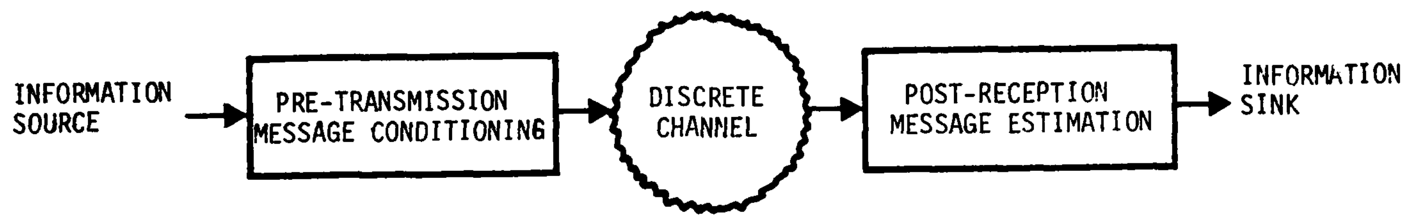


Figure 1. Abstract block diagram of one-way communication link.

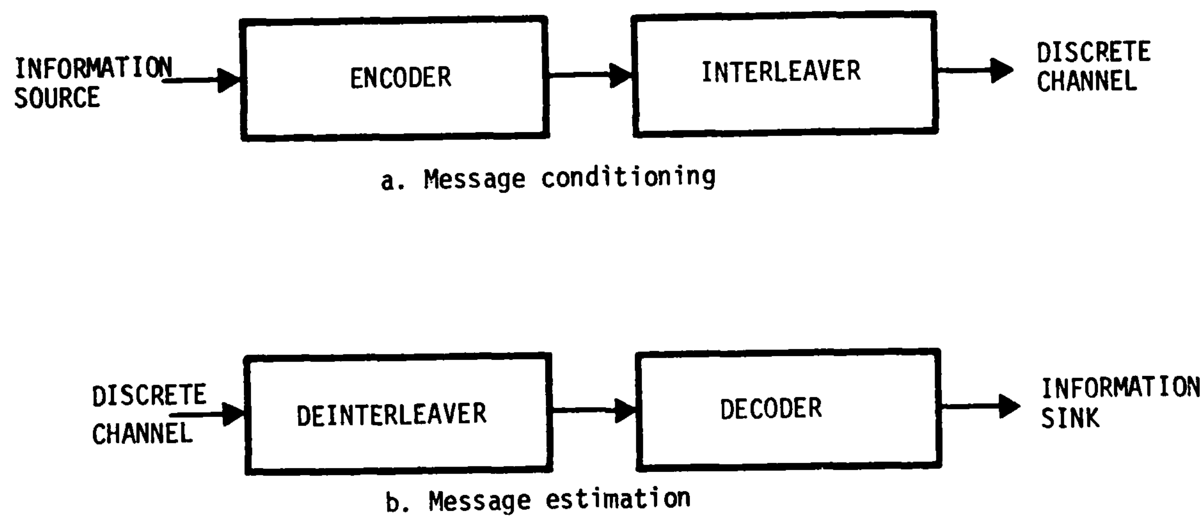


Figure 2. Non-concatenated error correction scheme.

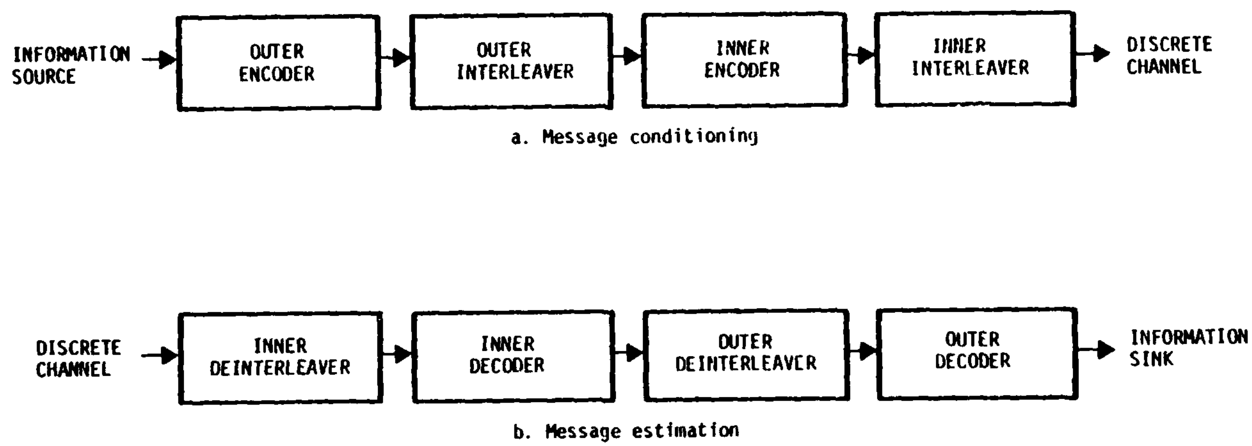


Figure 3. Concatenated error correction scheme.

section upon first encounter. One may later refer back to this section for background information as needed.

2.1 STANDARD VERSUS SOFT DECISION INTERFACE CONCATENATED CODING

Figure 3 shows a general concatenated coding scheme. Two nested error correction encoder/decoder pairs are shown, but in principle additional encoder/decoder pairs could be nested. In practice, however, two codes are usually used and either or both of the interleaver/deinterleaver pairs may be eliminated. Concatenated codes are a general solution to the coding problem. Forney (Reference 1) has shown that for the binary symmetric channel of capacity greater than R, there exists a standard concatenated code of at least rate R that can attain an arbitrarily small decoded bit error rate. Concatenated codes are often superior to non-concatenated codes in terms of implementation requirements.

In a standard concatenated scheme, the inner decoder outputs a binary (i.e., hardlimited) data stream, even though the inner decoder may use channel reliability information to generate these hardlimited outputs. The distinction between hard and soft decision processing will be discussed in Section 2.5. At this point suffice it to say that a key ramification of the hardlimited nature of the inner decoder output symbols is that the outer decoder treats all of its input symbols equally. For stationary hardlimited input symbol statistics, the outer decoder can be well characterized by an input/output error rate curve. Given some link error rate specification, the outer decoder input/output rate characteristic provides a well defined specification with which to choose or design the inner code.

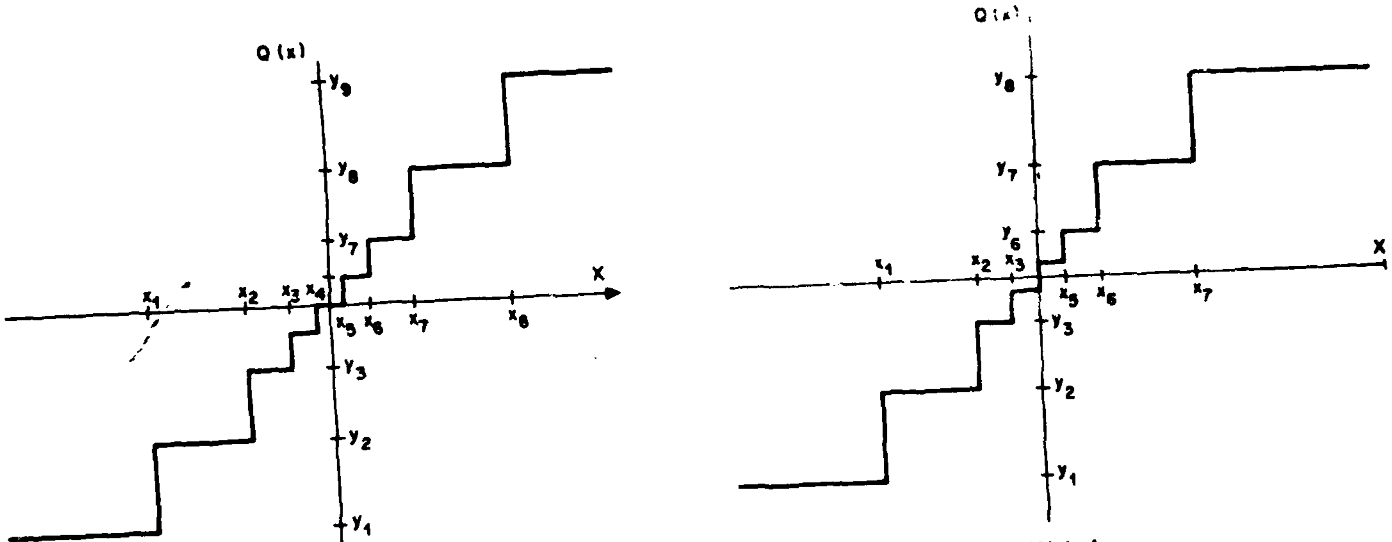
Soft decision interfacing (SDI) refers to the generation of reliability measures of the inner decoder outputs for use by the outer decoder. In effect the outer decoder deemphasizes unreliable input symbols and generally has a more favorable input/output error rate characteristic than would the outer decoder of a standard concatenated scheme. Hence the specification of the inner decoder symbol error rate can be somewhat relaxed provided the inner decoder generates high-fidelity output symbol reliabilty estimates. We will use the term "soft symbol" to indicate a multi-bit word representing not only the (binary) value of the symbol but also the reliability of that value. SDI is then the passing of soft symbols from an inner decoder to an outer one (perhaps through a deinterleaver). The potential utility of SDI results from the fact that the implementation complexity and cost of a standard concatenated coding scheme may far exceed that of a comparably performing, but algebraically weaker, SDI scheme.

2.2 QUANTIZERS

Though not explicitly shown in Figures 2 or 3, quantizers are important components of modern digital receivers. In a digital communication receiver, the received analog signal must be sampled in time and digitized in amplitude prior to digital processing. This conversion typically occurs at the I and Q (in-phase and quadrature) channels of the quadricorrelator, but may instead occur at the output of an analog demodulator. This digital conversion may or may not be the quantizer of interest here. If the signal amplitudes are digitized with several bits of resolution and with proper choice of overload point, then the quantization error will be negligible when compared to the effects of other sources of distortion or noise. In the limiting case of one-bit resolution (henceforth termed "hardlimiting"), the quantized symbols are just the received binary code symbols. If not hardlimited, the additional bits are a measure of the reliability of each symbol. For SDI concatenation, the reliability outputs of the inner decoder (which will be discussed explicitly in Section 3) can be viewed as continuous-amplitude bipolar values which must be digitized prior to deinterleaving. Hence, quantization effects of interest usually occur just prior to both deinterleavers of Figure 3.b and just before the one deinterleaver of Figure 2.b.

Figure 4 shows two typical quantizer input/output characteristics which are appropriate for input signals with probability densities exhibiting even symmetry about the origin. These quantizers are completely specified by the positive decision boundary values. If there are B strictly positive decision boundaries, a midtread quantizer (Figure 4.a) has 2B decision boundaries and 2B+1 possible output values, while a midriser quantizer (Figure 4.b) has 2B+1 decision boundaries and 2B+2 possible output values. Obviously a midriser quantizer has a zero-valued decision boundary and a midtread quantizer does not. Figure 5 shows the quantizer error as a function of input value for the midtread quantizer.

Quantizers decrease signal information content and hence are properly viewed as noise or error sources. There are two types of quantization error: "granular" error due to non-zero step sizes and "overload" error due to limited dynamic range. Unlike thermal noise, the quantization error and input signal are <u>not</u> independent. However, for small step sizes relative to signal dynamic range and at least moderately uncorrelated successive input samples, the granular quantization error is approximately uncorrelated with the input symbols and is uniformly distributed if the decision boundaries are equally spaced. Overload noise is highly correlated with the input signal and as such has a probability density function that is related to the input density.



a. Midtread

b. Midriser

Figure 4. Quantizer I/O characteristics.

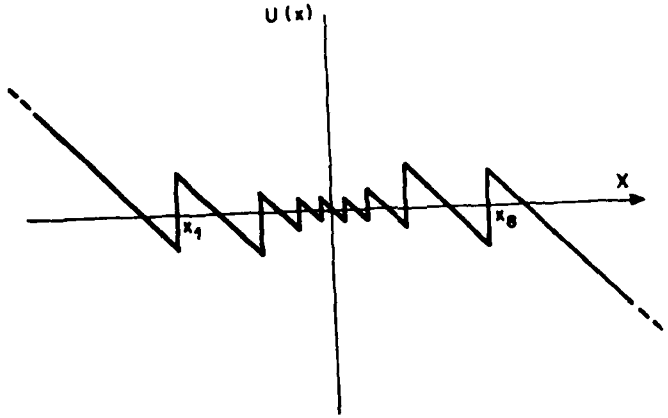


Figure 5. Quantizer error versus input sample value.

The choice for the number of quantization levels (or alternately the number of bits of resolution) is a compromize of two opposing goals. On the one hand, minimization of q, the number of bits representing each symbol, is desirable because the interleaver storage increases linearly with 2^q. On the other hand, the number of reliability levels is limited to 2^{q-1} since the polarity bit is taken as the decoded symbol. Thus a large value of q is desirable to adequately distinguish symbols with significantly different reliability measurements. With the exception of Section 5, we restrict our attention to three-bit symmetric midriser quantizers for which seven decision boundaries and eight output symbol values (henceforth called "weights") must be assigned. Even with complete knowledge of input statistics, there is no known tractable analytic procedure by which to simultaneously choose the decision boundaries and weights to minimize the quantization error for $q > 1$, and one must resort to numerical search algorithms. In this work, the input statistics are generally considered to be non-stationary and even the numerical methods will not work.

For non-stationary input statistics, either robust (i.e., companding) or adaptive quantization schemes (both discussed by Gersho in Reference 2) could be utilized. As previously stated, we are primarily interested in three-bit quantizers, and three bits do not provide sufficient dynamic range and resolution for a practical robust scheme. Adaptive schemes must be highly tailored to a particular non-stationary channel and are outside the scope of this more general study. However, these two approaches to quantization are potentially very interesting and may be pursued in future MRC coding studies. In each of the subsequent sections, quantization is considered from a different perspective. Hence, each section will contain a discussion of quantizer-related issues.

2.3 ERROR CORRECTION CODING

In the following, it shall be assumed that the reader is acquainted with error correction coding. A nomenclature for consistent use in subsequent sections of this report shall be established here. For a detailed introduction to coding theory applied to the digital communication channel, see References 3 and 4.

There are two classes of error correction codes: block codes and tree codes. We are only concerned with a small subset of each class. The block codes of interest are binary, systematic, cyclic codes or simple modifications thereof (i.e., shortened or parity bit augmented). Important binary block code parameters are:

- k - the information word length (bits)
- n - the codeword length (bits)
- R - the code rate = k/n
- 2^k - the number of codewords
- d_H - the minimum Hamming distance.

The tree codes of interest are binary, time-invariant, convolutional codes. Important characteristics of these codes are:

- k - the number of input bits per coding iteration
- n - the number of output bits per coding iteration
- R - the code rate = k/n
- K - the constraint length
- h - the number of contraint lengths of path history stored for each state
- hK - the number of bits of path history stored for each state
- $2^{k(K-1)}$ - the number of nodes (candidate values) for each state; also the number of paths stored
- d_f - the minimum free distance.

The commonality in notation is not accidental; in both block and convolutional codes k is the number of input symbols and n is the number of output symbols at each encoding iteration. Since block and convolutional codes will both be discussed in this report, when k or n is mentioned, the context should indicate whether the reference is to a block or convolutional code parameter.

Any $(n,k;d_H)$ block code can be characterized with a codeword look-up table which has an entry of n output symbols for each of the 2^k possible sequences of k binary input symbols. Cyclic codes can be much more concisely represented due to their mathematic structure. Either a generator polynomial of degree n-k or a parity check polynomial of degree k completely specifies a systematic cyclic code. Alternately, the exponents of the generator polynomial roots (usually elements of an extension field of the polynomial field) may be specified, as in Appendix D of Reference 3. The minimum Hamming distance, d_H, is a figure of merit for block codes. d_H is defined as the smallest bit-wise difference between any two non-identical codewords.

Any convolutional code can be specified by the parameters n, k and K and the n modulo-2 adder connection patterns. Unlike block codes, convolutional codes cannot be straightforwardly constructed. Good codes are usually found by extensive search procedures on a digital computer. Short binary convolutional codes that are well suited for the Viterbi decoding algorithm are tabulated in Reference 5. The most appropriate figure of merit for binary convolutional codes used in conjunction with Viterbi decoding is d_f, the minimum free distance. d_f is defined as the smallest bit-wise difference between any two non-identical, arbitrarily long encoded sequences. The linearity of convolutional codes allows an equivalent definition: the least possible number of one's in any non-zero encoded sequence. d_f can be used in a general sense to apply to any coding scheme, such as a "supercode" made up of concatenated codes. The minimum free distance of a concatenated supercode is not generally equal to the sum of the minimum free distances of the individual concatenated codes.

As a last general comment, error correction coding does not necessarily improve link operation. For high channel symbol error rates, the decoder often becomes "confused" and generates more errors than it corrects. This is a key point for concatenated codes used against fading, since the inner decoder outputs are always unreliable during a deep fade. The need for the outer decoder to distinguish between the reliable and unreliable code symbols is the basis for interest in SDI concatenation.

2.3.1 Complexity Estimation

Before discussing encoding, decoding, interleaving, and deinterleaving implementations, a few words should be said about how the complexity of the different schemes can be estimated. We will only be concerned with the digital processes of coding and interleaving. Memory and processing requirements will be considered separately.

The memory requirement will be measured in bits, without regard to word widths or other architectural features. Only the memory needed for major arrays of data will be considered; program storage will not be considered, this being too processor dependent to estimate accurately.

Processing will be estimated in operations-per-second. An operation will be defined loosely as any process that can be performed by a single chip microprocessor in one instruction. More specifically: addition, subtraction, comparison, and conditional branching (binary decision) are operations. A fetch or store will be considered an operation only when it is not associated with an operation mentioned above. An operation must involve no more than one address; multi-address processes and indirect or indexed addressing involve multiple operations. Fortunately there are no multiplications, divisions, floating-point operations or other complicated arithmetic to contend with in any of the processes considered.

The complexity estimates made using these guidelines will provide a consistent means of comparing the relative costs of implementing the different schemes to be discussed in later sections.

2.3.2 Encoding

With both block and convolutional codes of interest, encoding is very straightforward and has little impact on link complexity compared to decoding, interleaving or deinterleaving. Encoders for short block codes can be implemented with codeword tables stored in RAM or ROM, while long block codes are usually implemented with feedback shift registers, parity bit generators and other Galois field arithmetic circuits. The amount of storage required for a simple code lookup table is 2^k n-bit words. If codewords are generated with a feedback shift register instead of being stored in a code table, negligible storage is required; but the required processing is given by:

$$P_{block} = \frac{k + m}{n} R_s \quad \text{operations/second} \tag{1}$$

where m is the total number of delay line tap connections, and R_s is the output symbol rate.

Encoders of convolutional codes are usually implemented with modulo-2 adders and a tapped delay line without feedback connections. The output is the modulo-2 convolution of the binary, possibly semi-infinite, input sequence with the binary length-K sequence formed by the modulo-2 adder connection pattern of the encoders. A convolutional encoder similarly requires about

$$P_{conv.} = \frac{k + m}{n} R_s \quad \text{operations/second} \quad . \tag{2}$$

For detailed information on encoding of cyclic block codes and convolutional codes, see Reference 3.

2.3.3 Soft Decision Decoding

We shall refer to decoders that utilize channel reliability information as "soft decision" decoders. It is presumed that from the discrete channel outputs one can generate some measurement of the reliability of each channel symbol. For the i^{th} received symbol, denoted as r_i, one appropriate reliability measurement takes the form of the bit log likelihood ratio defined as

$$\phi_i = \log[\ Pr(r_i/0)\ /\ Pr(r_i/1)\ ] \tag{3}$$

where $Pr(r_i/0)$ is the a posteriori probability of receiving r_i when a "0" is transmitted and $Pr(r_i/1)$ is the same except for transmission of a "1". Soft decision decoders utilize not only the polarity of ϕ_i but also its suitably quantized magnitude. *In contrast, hard decision decoders* utilize only the polarity of ϕ_i. We shall use the convention that negative values of r_i and ϕ_i correspond to the code symbol 1 and positive values correspond to 0. Futhermore, r_i itself (i.e., the discrete channel output) will be taken as an approximation to ϕ_i. Hence the r_i contains all information needed by a soft decision decoder and further, r_i is assumed to be in the proper form for direct manipulation by the soft decision decoder. In subsequent discussions, r_i is referred to as a "soft symbol" when it is quantized with more than one bit. In the two subsections to follow, soft decision decoders for block and convolutional codes will be discussed.

2.3.3.1 A Soft Decision Decoder for Linear Binary Block Codes

An (n,k) block code has 2^k possible codewords and each codeword is a binary sequence of length n. Let C_{ji} denote the i^{th} element of the j^{th} codeword, where i and j are integers ranging from 1 to n and from 0 to 2^k-1, respectively. Let the transmission of some codeword result in a length n received code vector of discrete channel outputs, the i^{th} element of which is r_i. A brute-force soft decision decoder correlates each binary sequence with the received code vector. Define C^*_{ji} as -1 when C_{ji} is 1 and as 1 when C_{ji} is 0. Then the correlation of the j^{th} codeword with the received code vector is

$$\lambda_j = \sum_{i=1}^{n} C^*_{ji} \, \phi_i \quad . \tag{4}$$

The output of this soft decision decoder is simply the k bit value of j for which λ_j is a maximum. λ_{max} can then be used as a reliability metric for the entire block. When λ_{max} is suitably combined with the k decoded bits from the block, soft symbols are formed which can be used as inputs to the outer decoder of a nested scheme.

The following operations must be performed in soft decision block decoding:

1. Input the n soft symbols of the codeword from the demodulator.

2. Compute the 2^k different λ_j values by summing the products as indicated in Equation 4. Note that the product does not really involve a multiply operation but only a sign manipulation, since the values of C^*_{ij} are limited to -1 and +1. $n2^k$ conditional sign changing operations and $(n-1)2^k$ adds are used.

3. Compare λ_j's using 2^k-1 operations to find λ_{max}.

4. Select and output the decoded k bits associated with λ_{max}.

The equations below give the total number of operations per output bit required. Each term in Equation 5 represents one of the numbered steps above, while Equation 6 is a simplified approximation.

$$P_{Block} = \frac{n + [n2^k + (n-1)2^k] + (2^k-1) + k}{k} R_s \text{ operations/second} , \qquad (5)$$

or

$$P_{Block} \simeq \frac{n2^{k+1}}{k} R_s \text{ operations/second} , \qquad (6)$$

where R_s is the output symbol rate.

The code lookup table is the only substantial memory requirement for the block decoder scheme described above. It requires 2^k n-bit words (Equation 7) just as for the encoder; and, just as for the encoder, it can be replaced by a feedback shift register if a suitable code is used,

$$M_{Block} = n2^k \text{ bits} . \qquad (7)$$

2.3.3.2 A Soft Decision Decoder for Convolutional Codes, The Viterbi Algorithm

The Viterbi algorithm is an efficient means of soft decision decoding convolutional codes. It is assumed the reader is already familiar with the algorithm, which is well documented (References 6 and 7); only a brief description is given here to refresh the readers memory and to indicate the processing operations required.

The processing for a Viterbi decoder must encompass the following steps:

1. Shift the n received soft symbols into the decoder.

2. Compute those branch metrics which will be used in forming path metrics by correlating the soft symbol sequence with the n-bit reference sequence for each branch. The number of branch metrics computed is the smaller of 2^n or 2^{kK}, where 2^n is the number of different branch codes and 2^{kK} is the number of branches.

   The actual calculation of the branch metrics can be done by summing the soft symbols if $C_{ji}= 0$ or their negatives if $C_{ji}= 1$. nB operations are required to decide whether to negate each soft symbol and to do the negation if required, and (n-1)B operations are used to accumulate them, where

   $$B = \min(2^n, 2^{kK}) \quad . \tag{8}$$

3. Compute the 2^{kK} path metrics by adding the appropriate branch metric to each of the $2^{k(K-1)}$ surviving old path metrics.

4. Select the most likely of the 2^k paths entering each of the $2^{k(K-1)}$ nodes by comparing their metrics.

5. Finally, output the oldest decoded k bits in the path history memory from a suitable path. The path may be selected arbitrarily if sufficient path history is provided since all paths tend to converge, or equal performance may be obtained with somewhat less path history storage if the path with the largest metric is selected (Reference 8). For the present links an arbitrary path was used.

6. One final step <u>may</u> be necessary. The accumulated path metrics will increase without bound as time goes by if something does not prevent them. In some systems, messages are broken into packets, with path metrics being reinitialized every packet. With a large enough accumulator there can never be an overflow. In systems where reinitialization does not occur frequently, overflow must be prevented by periodically subtracting the same quantity from all metrics. This quantity must be smaller than the smallest metric to avoid negative metrics, yet as large as possible to avoid having to do metric reduction too often.

   In practice all metrics tend to be tightly clustered, so these objectives are easily met. The frequency of metric reduction is minimized if the largest metric is located and checked at each iteration. Then when overflow is imminent, the smallest metric is located and subtracted from all metrics. This procedure requires $3\times 2^{k(K-1)}$ operations since there are $2^{k(K-1)}$ path metrics. A simpler procedure is to check an arbitrary metric each iteration. When this metric is within $\delta+\varepsilon$ of overflow, subtract a constant which is less than $A-\delta-\varepsilon$ from all metrics, where δ is the maximum possible spread between path metrics, ε is the largest possible branch metric, and A is the largest value the path metric accumulator can store without overflow. This procedure requires only one third as many operations, since there are no searches for the largest and smallest metrics. In either case metric reduction is normally done so infrequently that its effect on average processing load is small. Step 6 will be neglected on the assumption that messages are packetized and the accumulator is large.

From the above description it is easy to obtain an algorithm for the number of operations per output bit. It is

$$P_{Viterbi} = \frac{n + [n+(n-1)]B + 2^{kK} + (2^k-1)\,2^{k(K-1)} + 1}{k} R_s \quad \text{operations/second,} \tag{9}$$

where R_s is the output symbol rate and B is defined in Equation 8. For $n \geq kK$ this can be closely approximated by

$$P_{Viterbi} \approx \frac{n}{k} 2^{1+kK} R_s \quad \text{operations/second,} \tag{10}$$

or for $n2^n \ll 2^{kK}$,

$$P_{Viterbi} \approx \frac{(2 - \frac{1}{2^k})2^{kK}}{k} R_s \quad \text{operations/second.} \tag{11}$$

The memory required for Viterbi decoding is the number of nodes per state, $2^{k(K-1)}$, times the number of states of path history, hK, times the base 2 log of the number of branches per node, $\log_2(2^k) = k$, plus the path metric storage, $2^{k(K-1)}$ words of, say, 16 bits each:

$$M_{Viterbi} = hkK2^{k(K-1)} + (16)2^{k(K-1)} \text{ bits} \quad . \tag{12}$$

2.4 INTERLEAVING AND DEINTERLEAVING

Interleaving, in conjunction with coding, is the most cost effective mitigation against slow fading, wherein τ_0 is much longer than the channel symbol period. Block or convolutional coding without interleaving is effective for moderate error rates if the errors are randomly distributed in time, i.e., the channel is memoryless. However, bursts of errors may overwhelm a decoder. Interleaving introduces time diversity whereby each link output symbol is decoded from channel symbols greatly separated in time. An input to an interleaver appears exactly once as an output. Interleavers and deinterleavers can be characterized by parameters n_1 and n_2. An interleaver reorders the data stream so that no contiguous sequence of n_2 output symbols contains two symbols separated by fewer than n_1 symbols in the input sequence. A deinterleaver unscrambles the interleaved data stream to produce the original sequence ordering. The value of n_2 is determined by the maximum expected fade duration. For a given value of τ_0, n_2 ideally should exceed $\tau_0 R_c$, where R_c is the symbol rate. (In practice n_2 can be somewhat less than $\tau_0 R_c$ without greatly affecting decoded error rates.)

The effect of using combined interleaving and coding can be seen in Figure 6, which plots E_b/N_0, the average received energy per information bit to noise spectral density ratio required to achieve some average decoded symbol error rate, versus τ_0. On the left end of the curve τ_0 is so small that received signal coherence over the minimum modulator signaling interval is lost, resulting in very high channel symbol error rates. In the central region, where τ_0 is moderate, the interleaving/coding combination is effective in correcting errors. As τ_0 becomes larger a point is reached where $\tau_0 R_c$ equals n_2. As this point is approached, the symbols are no longer independent and the value of E_b/N_0 required to achieve a given error rate increases until the slow fade limit is reached. The resulting smoothed stairstep on the right half of Figure 6 can be moved right by increasing n_2/R_c.

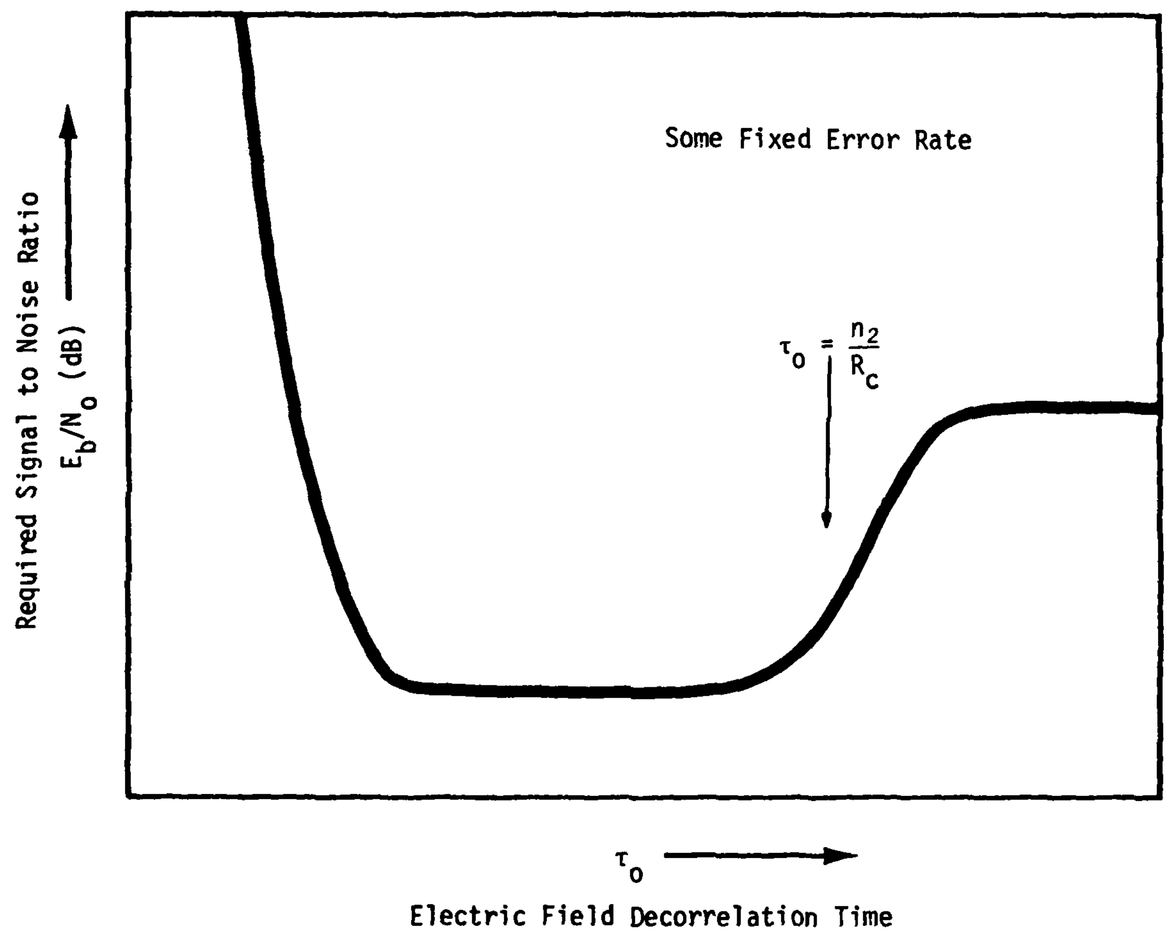


Figure 6. Typical curve of mean E_b/N_o required to attain some fixed error rate versus τ_o for a link utilizing error correction coding and interleaving.

The combination of high modulation rates and slow fading rates sometimes results in impractically large interleaver storage requirements. The latter sections of this report focus on a few alternative coding and interleaving formats that may offer attractive trades of implementation complexity (particularly interleaver storage) for performance.

The following discussion on the implementation and complexity will be restricted to synchronous interleavers and deinterleavers (those in which a symbol is read out each time a symbol is read in). When the symbol rate is constant and the interleaver and deinterleaver are both synchronous, the delay due to interleaving and deinterleaving is constant and will be at least

$$D \geq (n_1-1)\ (n_2-1) \text{ symbols} \quad . \qquad (13)$$

This sets a lower bound on the sum of the interleaver memory plus deinterleaver memory, and D/2 symbols is the minimum storage required for either the interleaver or deinterleaver alone.

Ramsey, in Reference 9, discusses four types of synchronous interleavers and deinterleavers which are used throughout this report. Type III is shown in Figure 7; the other types differ only in the rotation direction of the rotary tap-selector switch and the orientation of the rotary switch to the shift register. Each type has a different range of relative values of n_2 and n_1 over which it is optimal in the sense of using least memory (e.g., a Type III (n_2,n_1) is optimal for $2n_2 < n_1$). However, the penalty for using a nonoptimal interleaver is small - for example: $(n_1+1)(n_2-1)$ quantized symbols of storage are required for Type III versus $n_1(n_2-1)$ for Type I. There are relative values of n_1 and n_2 for

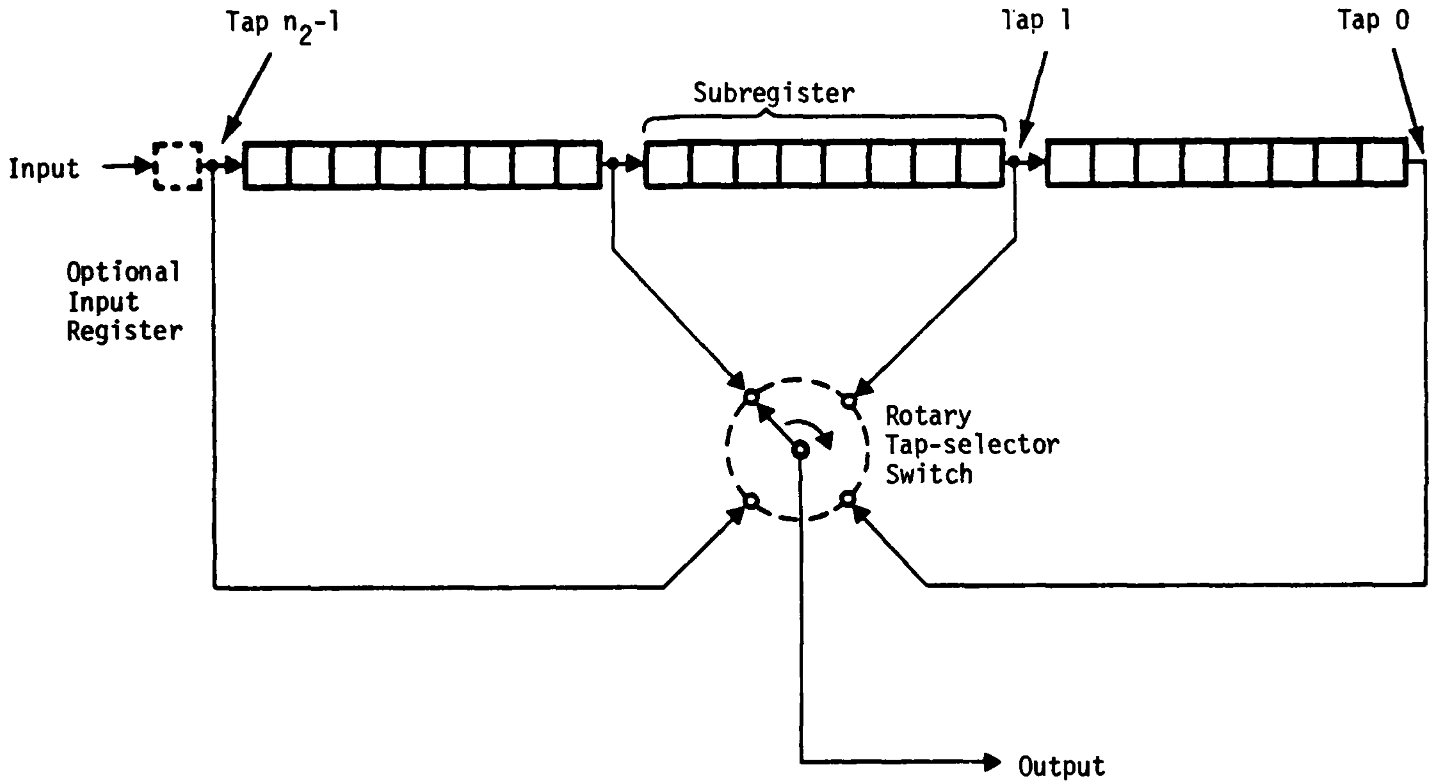


Figure 7. Type III equal subregister interleaver ($n_2 = 4$, $n_1 = 7$).

which a given type cannot be used: all types have relative primeness requirements between n_1 and n_2, and n_2 must be less than n_1 for Type I and n_1 less than n_2 for Type II. Each of the four interleavers is identical to a deinterleaver of a different type with the values of n_1 and n_2 reversed. For example, a Type III (7,4) interleaver is identical to a Type IV (4,7) deinterleaver. All these details are given in Tables 1 and 2. Interleaver and deinterleaver must match in n_1, n_2 and type for proper operation.

The equal subregister synchronous interleaver shown in Figure 7 requires one-half the memory of the classical write-rows-read-columns block interleaver, which must be configured as a ping-pong double buffer to achieve synchronous operation. It is possible to modify the synchronous interleaver of Figure 7 to reduce the memory size by an additional factor of two. In Figure 7, all subregisters are right shifted one position and the rotary switch is advanced one tap on each clock pulse. Note that after a symbol is read out, it is unnecessarily retained in memory. On the average, the symbols are stored twice as long as necessary.

Figure 8 shows an implementation of a Type III interleaver that does not retain symbols in memory longer than necessary and, hence, requires half as much memory. Only the subregisters preceding the tap currently selected are shifted on any given clock pulse, and the length of the subregisters decreases toward the right. A similar scheme is used for the interleaver types which have the rotary switch on their input, but the shorter subregisters are on the left, and only subregisters following the selected tap are shifted. This reduced storage implementation is discussed in Reference 9 and is henceforth termed the "tapered subregister" implementation. Its storage requirements very nearly satisfy the lower bound of Equation 13.

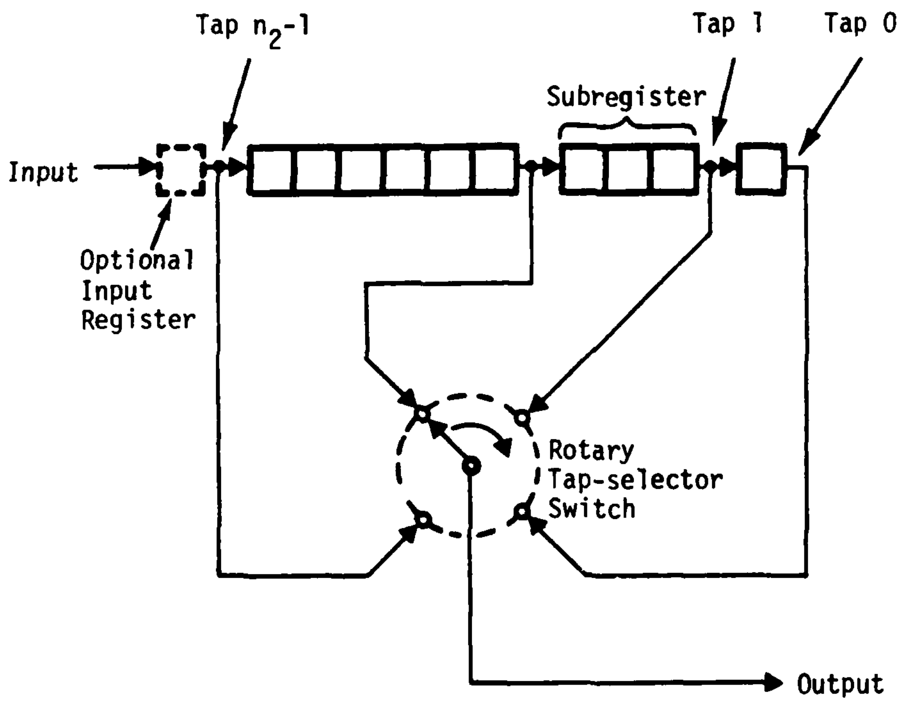


Figure 8. Type III tapered subregister interleaver ($n_2 = 4$, $n_1 = 7$).

While interleavers may be built using actual hardware shift registers, a random access memory (RAM) implementation is generally preferable because RAM's of a given size are cheaper, lighter, more compact, and use less power than shift registers. In a RAM implementation, pointers are used to access the taps. For the equal subregister scheme a single pointer can be used to access all taps, but when tapered subregisters are used, separate pointers must be maintained and independently decremented for each tap, which thereby increases the processing complexity.

The memory requirements for interleavers with equal subregisters are presented in Table 1, and the deinterleaver requirements are presented in Table 2. The four types have slightly different RAM storage requirements, but each can be approximated by

$$M_{equal} \approx n_1 n_2 w \text{ bits} \quad , \tag{14}$$

where w is the number of bits per quantized (soft) symbol. If the tapered register implementation is used, half the memory is required:

$$M_{tapered} \approx \frac{n_1 n_2 w}{2} \text{ bits} \quad . \tag{15}$$

The digital processing requirements for a Type III interleaver with equal subregisters are given in Table 3. The operations shown utilize the optional extra symbol storage shown in broken lines in Figure 7. Addresses and tap numbers advance from right to left following Ramsey (Reference 9). The processing complexity for an interleaver or deinterleaver with equal subregisters is

$$P_{eq} = 8R_s \text{ operations/second} \tag{16}$$

Table 1. Interleaver characteristics.

TYPE	I	II	III	IV
Relatively Prime Requirement	n_1, n_2+1	n_1+1, n_2	n_1, n_2	n_1, n_2
Range Requirement	$n_2+1<n_1$	$n_1+1<n_2$	none	none
Subregister Length (L) (nontapered)	n_1-1	n_2-1	n_1+1	n_2+1
Number of Subregisters (S)	n_2	n_1	n_2-1	n_1-1
Number of Taps (S+1)	n_2+1	n_1+1	n_2	n_1
Storage (nontapered)	$n_2(n_1-1)q$	$n_1(n_2-1)q$	$(n_2-1)(n_1+1)q$	$(n_1-1)(n_2+1)q$
Rotary Switch Location	output	input	output	input
Rotary Switch Rotation	CCW	CW	CW	CCW
Range of Minimum Storage	$n_2<n_1<2n_2$	$n_1<n_2<2n_1$	$2n_2<n_1$	$2n_1<n_2$
Range of Minimum Processing (tapered subregisters)	never min	never min	$n_2<n_1$	$n_1<n_2$

Notes: All deinterleaver characteristics are the same as the interleaver of the same type except for the tap selector location and direction, which are opposite.

A Type I (n_2=A, n_1=B) interleaver is identical to a Type II (n_2=B, n_1=A) deinterleaver. Similarly Types III and IV are complementary.

A Type X (n_2=A, n_1=B) deinterleaver must be used with a Type X (n_2=A, n_1=B) interleaver.

Table 2. Deinterleaver characteristics.

TYPE	I	II	III	IV
Relatively Prime Requirement	n_1, n_2+1	n_1+1, n_2	n_1, n_2	n_1, n_2
Range Requirement	$n_2+1<n_1$	$n_1+1<n_2$	none	none
Subregister Length (L) (nontapered)	n_1-1	n_2-1	n_1+1	n_2+1
Number of Subregisters (S)	n_2	n_1	n_2-1	n_1-1
Number of Taps (S+1)	n_2+1	n_1+1	n_2	n_1
Storage (*nontapered*)	$n_2(n_1-1)q$	$n_1(n_2-1)q$	$(n_2-1)(n_1+1)q$	$(n_1-1)(n_2+1)q$
Rotary Switch Location	input	output	input	output
Rotary Switch Rotation	CW	CCW	CCW	CW
Range of Minimum Storage	$n_2<n_1<2n_2$	$n_1<n_2<2n_1$	$2n_2<n_1$	$2n_1<n_2$
Range of Minimum Processing (tapered subregisters)	never min	never min	$n_2<n_1$	$n_1<n_2$

Notes: All deinterleaver characteristics are the same as the interleaver of the same type except for the tap selector location and direction, which are opposite.

A Type I (n_2=A, n_1=B) interleaver is identical to a Type II (n_2=B, n_1=A) deinterleaver. Similarly Types III and IV are complementary.

A Type X (n_2=A, n_1=B) deinterleaver must be used with a Type X (n_2=A, n_1=B) interleaver.

Table 3. Equal subregister interleaver (Type III).

	OPERATIONS	COMMENTS
1.	If TAPNO = 0	The rotary switch has reached tap zero.
2a.	Then TAPNO = NOTAPS	Start the switch again at the highest tap number and set the appropriate address for TAP.
3a.	Set TAP = INTAP	
2b	Else decrement TAPNO	Rotate the switch one step.
3b.	If TAP < REGSTART + (REGSIZE-1)	The start of the array is near.
4a.	Then TAP = TAP + (REGEND - REGSIZE + 1)	Restart near the beginning of the array.
4b.	Else TAP = TAP - (REGSIZE - 1)	Step to the next tap address.
5.	Output the symbol at location TAP	
6.	If INTAP = REGEND	The end of the array has been reached.
7a.	Then INTAP = REGSTART	Move INTAP back to the start of the array.
7b.	Else increment INTAP	Equivalent to a register shift.
8.	Write an input symbol into location INTAP and go to 1.	

where:

TAPNO	- the tap number selected by the rotary switch.
NOTAPS	- the total number of taps (minus one).
TAP	- the symbol register address pointed to by the currently selected tap.
INTAP	- the symbol register address where an input symbol is to be written.
REGSTART	- the address of the start of the symbol register.
(REGSIZE - 1)	- the size of each of the subregisters minus 1, a precomputed constant.
(REGEND - REGSIZE + 1)	- another precomputed constant.
REGEND	- the address of the (left) end of the symbol register array.

where R_S is the interleaver's input/output symbol rate processed by the interleaver in symbols/second. Note that the processing load is a function of the symbol rate only, and in particular it is not a function of n_1 or n_2 when the equal subregister implementation is used.

Such is not the case if the tapered subregister implementation is used. As previously stated, each subregister must be shifted individually, implying separate pointers for each subregister and the actual movement of the right-most symbol of one subregister into the left-most position of the next (right) subregister. Table 4 shows the operations performed. Note that there is an inner loop (operations 4 thru 12a) repeated for shifting each subregister, and an outer loop (operations 1 thru 14a) repeated once per symbol output. Operations 14b thru 16b are performed in the special case where the next symbol for output is the one that has just been input. The number of operations for outputting this symbol is only 3, but in general many more operations are required for each symbol. In the worst case, where the output tap is number zero, all of the subregisters must be shifted, and the inner loop must be executed once per subregister shifted. The number of subregisters is approximately n_1 for Types II and IV, and n_2 for Types I and III. To minimize processing, then, Type I or III should be chosen if n_1 is greater than n_2; otherwise Type II or IV should be used. Tables 1 and 2 give the relative ranges of n_1 and n_2 for which Types III and IV require least processing of any type. (Type I will always require a bit more processing than Type III, and Type II will always require a bit more than Type IV.)

The algorithm for computing the processing load for a tapered subregister interleaver or deinterleaver, based on the operations in Table 4, is

$$P_{\text{tapered (avg)}} = \frac{2 + S\left[5 + \left(8 + \frac{2}{L}\right)\left(\frac{S+1}{2}\right)\right]}{S + 1} R_s \quad \text{operations/second} \qquad (17)$$

Table 4. Tapered subregister interleaver (Type III).

OPERATIONS	COMMENTS
1. Set THIS = TAPNO. 2. Fetch TAP(THIS). 3. Output the symbol at location TAP(THIS).	Output a symbol.
4. Compute THIS + 1. 5. Fetch TAP(THIS + 1). 6. Fetch the symbol at location TAP(THIS + 1). 7. Store the symbol into location TAP(THIS).	Move the symbol from the tap of the next (left) register into the tap location of this subregister.
8. If TAP(THIS = REGEND(THIS). 9a. Then Fetch REGEND(THIS - 1) 10a. Tap(THIS) = REGEND(THIS - 1) + 1. 9b. Else increment TAP(THIS).	Shift this register
11. If THIS = (NOTAPS - 1). 12a. Then increment THIS and go to 4. 12b. Else write an input symbol into location *INTAP*.	Continue shifting subregisters *until the last subregister is reached*
13. If TAPNO = 0. 14a. *Then* decrement TAPNO and go to 1.	Continue decrementing the output tap until the last tap position is reached
14b. Else output the symbol at location INTAP. 15b. *Write an input* symbol into location INTAP. 16b. Set TAPNO = NOTAPS and go to 1.	Then output the symbol in the extra input register, restart the tap number and continue

where:

THIS	- the subregister being *manipulated*.
TAPNO	- the tap number selected by the rotary switch.
TAP(0...NOREG-1)	- an array of symbol subregister addresses pointed to by the rotary switch taps. There are NOREG elements indexed 0 through NOREG-1.
REGEND(-1...NOREG)	- an array of the ending addresses of the symbol subregisters. There are NOREG+2 elements (constants) indexed -1 through NOREG. REGEND(-1) is the address just preceding the first address of the symbol register array and REGEND(NOREG) is the address of the optional input subregister, also called INTAP for readability.
INTAP	- the address of the optional input subregister. (See REGEND(NOREG).)

or approximately

$$P_{tapered\ (avg)} \approx (5+4S)R_s \quad \text{operations/second,} \qquad (18)$$

where S is the number of subregisters, L/2 is the average length of the subregisters and R_S is the symbol rate. For real-time processing such as this, it is generally the peak processing requirement that drives the complexity of the processor and

$$P_{tapered(peak)} = (5+9S)R_s \quad \text{operations/second.} \qquad (19)$$

It is the peak processing that will be referenced in following sections. While the algorithms in Tables 3 and 4 apply to Type III interleavers (or Type IV deinterleavers), the algorithms for the other types differ only in details; the number of operations remains the same. Only those operations which must be repeated for every processed symbol are shown; initialization operations, since they are done only once, are not shown.

2.5 SIMULATION APPROACH

Figure 9 is a diagram of the structure of all link simulations used in this work. As shown, each satellite link simulation was performed in three simulation stages: (1) multiple phase screen propagation simulation; (2) receiver simulation; and (3) error correction coding simulation. Notice that two programs are used to model the discrete channel and one is used to model the error correction scheme.

Partitioning the link simulation into three distinct programs very significantly reduces the amount of computer time required to execute the simulation. For instance, with the partitioned structure, the sensitivity of link performance to a particular code parameter (i.e., the quantizer dynamic range) can be studied by executing only the error correction scheme program for several values of that parameter. To make this

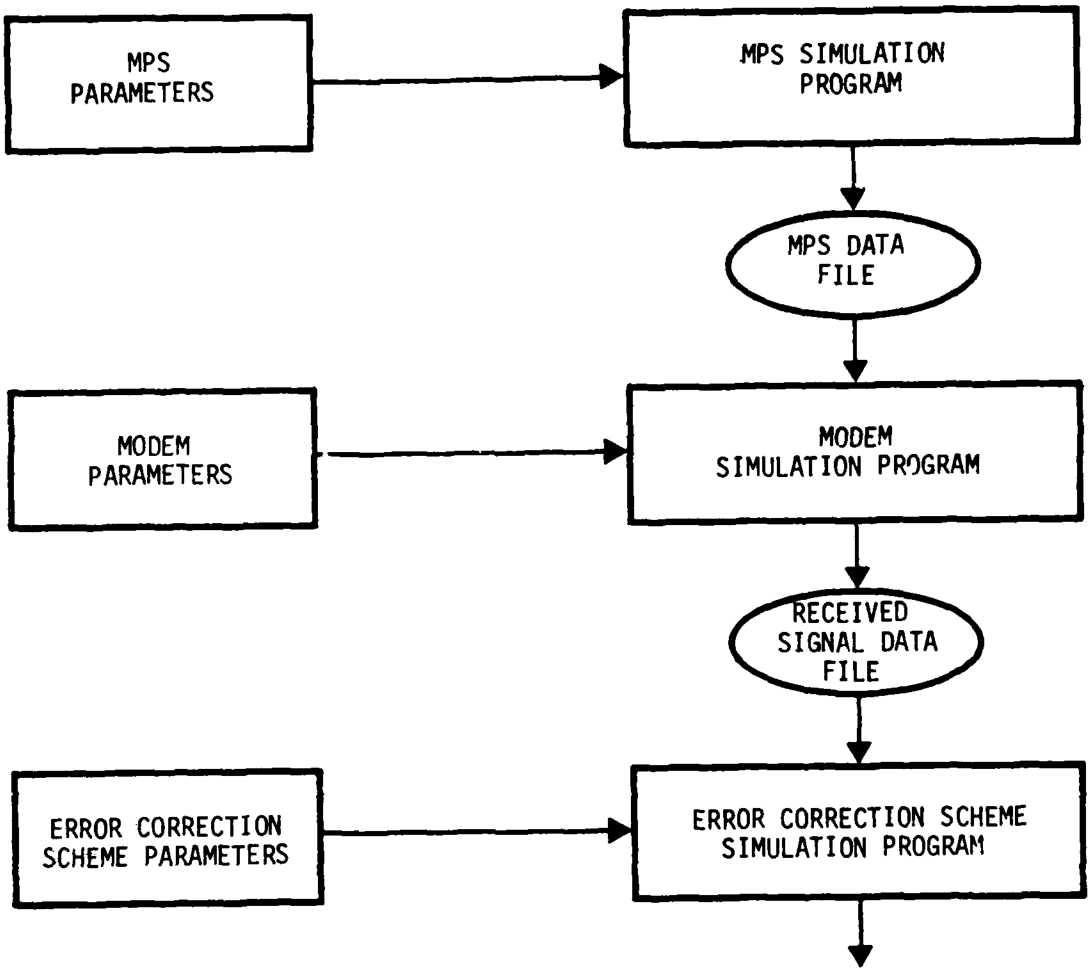


Figure 9. Block diagram of link simulation structure.

study with a non-partitioned structure would require regeneration of identical discrete channel data for each parameter value evaluated. The same reasoning motivates the partitioning of the discrete channel into two programs. Indeed, only one MPS realization was used to generate all results in this report, but several transmitter/receiver runs were made with different values of V_{eff} and E_b/N_o. Hence the MPS data was only generated once, but was used several times.

2.6 THE DISCRETE CHANNEL

The discrete channel is the signal flow path from the input of the modulator in the transmitting terminal to the output of the demodulator in the receiving terminal. The discrete channel of interest here takes discrete-time binary inputs and generates discrete-time, continuous amplitude outputs. As discussed above, the discrete channel is simulated with two distinct models, which are discussed separately below.

2.6.1 Multiple Phase-Screen Propagation Simulation

The MPS propagation model has been used extensively by MRC and others to simulate electromagnetic propagation through disturbed media (References 10 through 13). Signal energy transmitted from a satellite to a ground station in the presence of large, spatially extended regions of high-altitude, nuclear-burst-produced striations of electron density can be modeled as propagation through a thick medium composed of random index-ofrefraction fluctuations. Since no general analytical solution is available for this type of problem, it must be handled numerically. The MPS model is an analytical/numerical technique which provides a numerical solution for the propagation of a plane wave through a disturbed ionosphere. By modeling the ionosphere as a series of random phase screens with a power-law power spectral density, the MPS model simulates the propagation of electromagnetic waves through statistically chosen realizations of the random medium.

The MPS propagation model represents the disturbed region by a number of phase-screens located in the disturbed region between the satellite and the receiver. Random phase fluctuations in each screen are generated using the statistical properties of the electron-density fluctuations as determined by the electron-density power spectral density. A wave (initially plane as it enters the disturbed region) is then propagated numerically from one screen to the next by use of the Fresnel-Kirchhoff integral equation until a solution is obtained for the complex electric field in the receiver plane. This technique is equivalent to a solution of the parabolic wave equation and is thus able to account for multiple scattering. Since the phase-screens are random, the signal propagated to the receiver is random and, if desired, statistics may be obtained by averaging a number of different simulations, each based on a different sequence of random numbers.

Parameters specifying the scattering region geometry, the statistical variation of scattering region irregularities and various modeling options are taken as input by the MPS simulation. Detailed discussions of the MPS simulation parameter set can be found in References 10, 14 and 15. The values of these parameters used here were chosen to model the earth's ionosphere in a saturated electron density condition and are tabulated below:

number of phase screens	10
number of complex samples per realization	16384
analytic form of Power Spectral Density	Power Law
RMS phase fluctuation	300 radians
carrier frequency	7.5 GHz
grid length	30 km
outer scale size	3 km
inner scale size	10 m
scattering region thickness	14000 km
receiver-to-region center distance	8000 km

The MPS simulation results consist of realizations of electric field amplitude and phase as measured at the receiver input. Plots of the amplitude and phase fluctuations for the MPS realization used throughout this work are shown in Figures 10 and 11. Important measured statistics of this realization are

S4 scintillation index	1.00
skewness	2.04
excess	6.39

These parameters correspond very closely to a Rayleigh fading condition. A general discussion of the above statistical parameters and their consequence on the discrete channel can be found in References 16 and 17.

The MPS propagation simulation results consist of realizations of the electric field amplitude and phase as measured at the receiver input. The signal scintillation correlation distance, ℓ_0, is defined as the e^{-1} point on the spatial autocorrelation function of the complex *signal in* the receiver plane. A theoretical treatment of the spatial autocorrelation of the complex signal is found in Reference 18. The MPS data are co-linear, uniformly spaced samples separated by ΔX. A conversion to the time domain is made through an effective velocity, V_{eff}, which is a weighted average of the component of the relative velocity between the propagation path and striated medium in a direction normal to the path and normal to the field-aligned striation axes. Thus this effective velocity is a function of many system and environmental parameters. These include satellite and airborne terminal velocities, plasma velocities, orientation of the geomagnetic field and propagation path geometry.

The signal scintillation decorrelation time, denoted as τ_0, and the time sample spacing, denoted by ΔT, are related to ℓ_0 and ΔX by

$$\tau_o = \frac{\ell_o}{V_{eff}} \text{ seconds} \tag{20}$$

$$\Delta T = \frac{\Delta X}{V_{eff}} \text{ seconds} \tag{21}$$

A reasonable range of effective velocities to consider is from a few tens of meters per second to around 1000 m/s. When scintillation is intense, signal correlation distances at UHF range from around 100 to 200 meters down to around 1 meter. Thus the likely range of signal decorrelation times, τ_0, is from around 1 millisecond to about 10 seconds. The decorrelation distance, ℓ_0, is measured to be 6.4 m. The realization of Figures 10 and 11 was used to simulate the fading channel at two values of τ_0 by varying V_{eff}. By Equation 20, τ_0's of 0.1 and 1.0 seconds are attained with values of V_{eff} of 6.4 and 64., respectively. These values

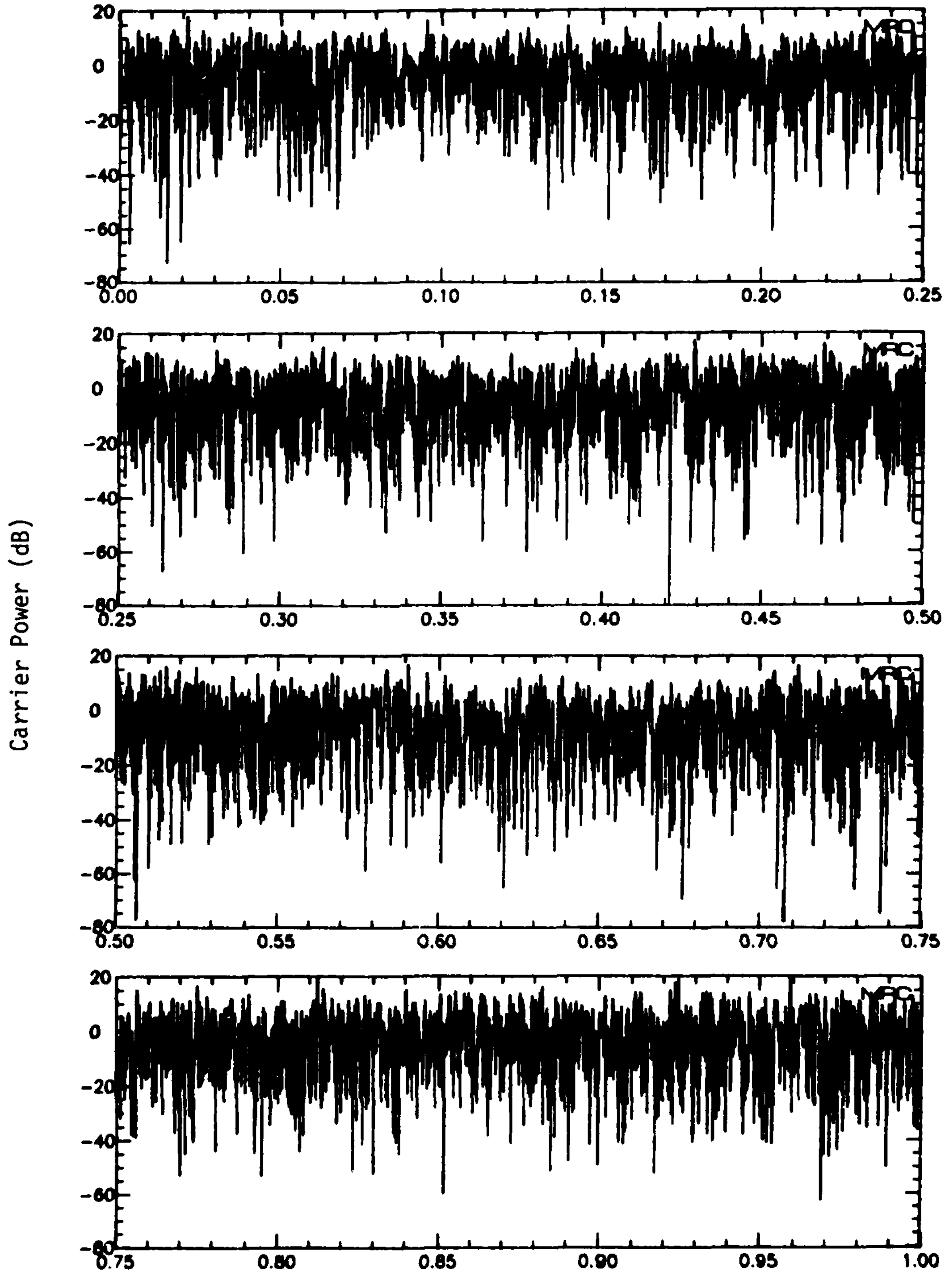


Figure 10. Carrier power fluctuations versus normalized time.

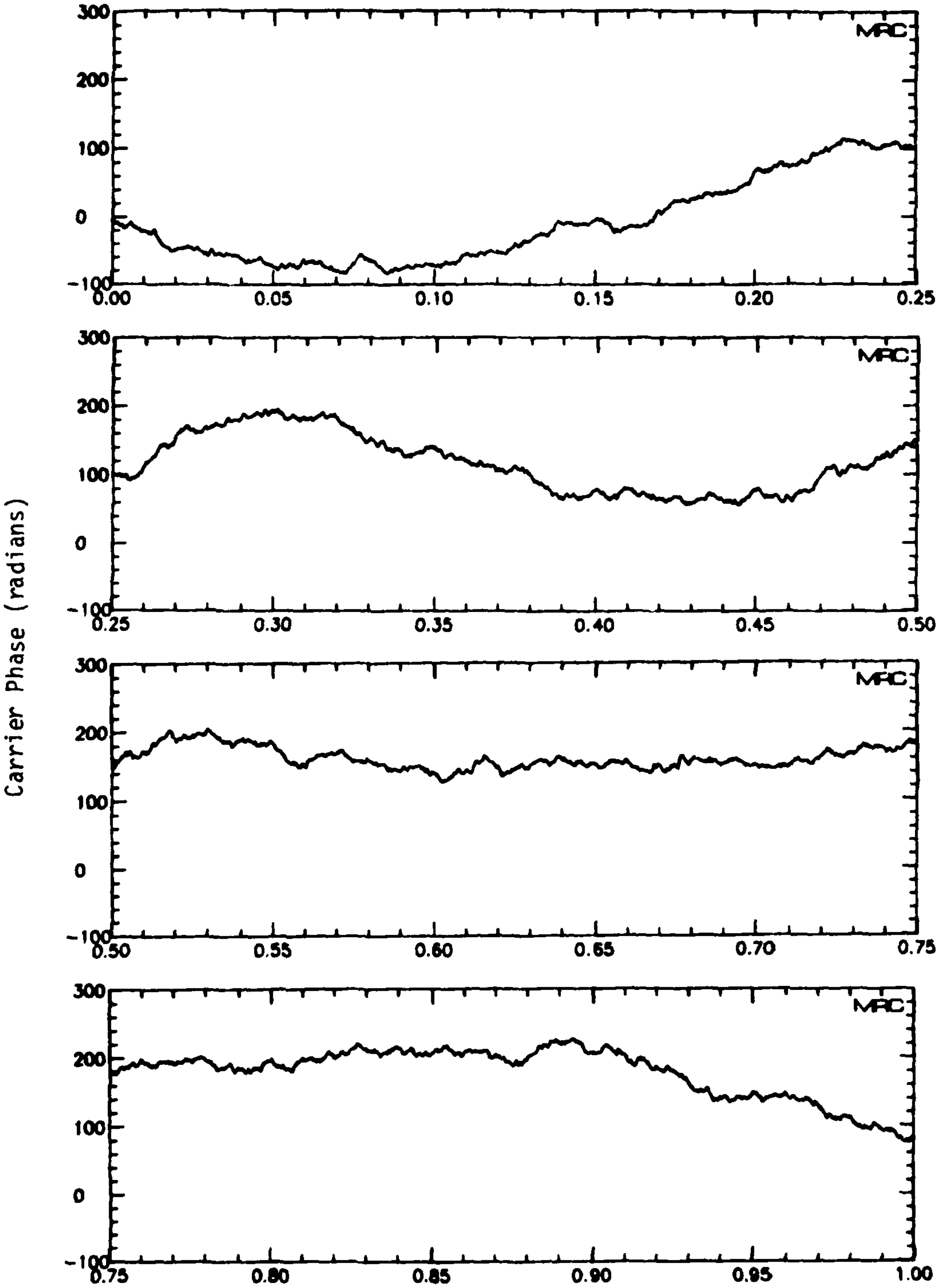


Figure 11. Carrier phase fluctuations versus normalized time.

of τ_0 were chosen to test link performance just inside and just outside the interleaver's slow fading break point.

2.6.2 Modem Simulation

The second part of the discrete channel model is performed by the Modem (Modulation/Demodulation) simulation. The Modem simulation incorporates models of direct sequence PNSS code tracking loop, binary DPSK demodulation, frequency tracking and automatic gain control. A comprehensive treatment of these models can be found in Reference 19, and only two additional comments need be added here. First, the simulated channel has no frequency selectivity, and hence no gain results from the spread spectrum function. In fact, the error in the simulated code tracking loop results in a net loss. Second, the data file created by the Modem simulation for use by the error correction scheme simulations must be free of modulation, since each scheme must superimpose its own encoded modulation onto the received signal data. However, to get realistic frequency tracking performance, random channel symbols need to be modulated onto the carrier. This dilemma is solved by performing the Modem simulation with an arbitrary encoded message and then stripping the modulation off the received signal data just prior to writing it to the received data file. This is easily done due to the simple correspondence between the phase of the modulation and the polarity of the demodulator output. The modulation is stripped from the demodulator outputs by simply negating all output values associated with the transmission of the encoded binary symbol "1." This result is equivalent to the transmission of the all zero message, but with the frequency tracking error of a random message. Pertinent receiver parameters are listed below:

Receiver Design Parameters

carrier frequency	7.5 GHz
pseudo noise code chip rate	40 Mbits/s
channel bit rate	600 Hz
A/D sampling rate	600 Hz
I.F. bandwidth	600 Hz

AGC Parameters

charging time constant	10 s
discharging time constant	10 s
maximum voltage gain	50
minimum voltage gain	0.02
loop feedback gain	40
detector type	envelope

PN Code Tracking Loop Parameters

bandwidth	0.5 Hz
damping factor	0.707
order	2
iteration rate	37.5 Hz
doppler aiding	none
configuration	tau dither

Runs of the receiver stage simulation were made at various values of E_b/N_o for both values of τ_o. Since the simulated propagation media do not exhibit frequency selective effects, the de-spreader can be viewed as a simple loss in E_b/N_o. Table 5 tabulates all utilized values of E_b/N_o before and after the code tracking loop for both values of τ_o, allowing the results to be generalized to a channel not utilizing frequency diversity.

Table 5. **Correspondence of E_b/N_0 at input and output of code tracking loop for all simulation runs**

τ_0 (s)	Before Despreader E_b/N_0 (dB)	E_s/N_0 (dB)	After Despreader E_b/N_0 (dB)	E_s/N_0 (dB)	Channel Symbol Error Rate (percent)
0.1	7.81	-1.22	6.48	-2.55	32.12
0.1	8.81	-0.22	7.65	-1.38	28.93
0.1	9.01	-0.02	7.86	-1.17	28.17
0.1	9.71	0.68	8.60	-0.43	26.29
0.1	9.80	0.77	8.73	-0.30	25.75
0.1	10.90	1.86	9.86	-0.83	22.52
1.0	12.00	2.97	10.97	1.94	19.19
1.0	14.00	4.97	13.03	4.00	13.72
1.0	16.00	6.97	15.06	6.03	9.37

We hasten to point out that the conventional DPSK modem used here is designed solely to provide binary output decision information and not the bit log-likelihood ratios ideally suited to the soft decision decoders. Our use of the conventional DPSK demodulator confuses the issue somewhat because of the "mismatch" between the demodulator and decoders. The conventional DPSK modem does have the desirable characteristic that the more reliable output symbols tend to have a larger magnitude, but it is quite possible that the performance of the error correction schemes could be significantly improved if the demodulators could provide actual bit log-likelihood ratios. More importantly, the simulation-aided interface between the demodulator and the decoders may bias the comparisons of coding schemes described and evaluated in this report, due to differing sensitivities of the various codes to the mismatch. A demodulator that does provide actual bit log-likelihood ratios has been developed for M-ary FSK modems operating under fading conditions by Barrett (Reference 20), and work on a similar DPSK modem is currently being done at MRC. We anticipate that future coding studies involving modem simulations will utilize these advanced modem designs to eliminate the demodulator-to-decoder interface issue.

SECTION 3

SDI CONCATENATION PERFORMANCE VERIFICATION STUDY

This section documents a viability study of SDI concatenation as a coding technique against scintillation effects. Estimates of the implementation complexity of coding and interleaving were given in Section 2. Those estimates indicate that SDI concatenated coding schemes that do not interleave channel symbols are often simpler to implement than nonconcatenated schemes that do interleave channel symbols. This is particularly true for channels where fade durations are orders of magnitude larger than the channel symbol modulation interval. However, the error correction strength of such SDI concatenated schemes relative to non-concatenated schemes had not been quantified. To this end, two detailed satellite-to-ground link simulations, termed the "baseline link" and the "concatenated link," were constructed. The propagation path of these two links passes though a simulated region of a highly disturbed ionosphere. The concatenated link uses SDI concatenation with interleaving between the inner and outer error correction codes. The baseline link uses convolutional encoding, interleaving and Viterbi soft-decision decoding. Detailed descriptions of the error correction schemes of the two links will be presented first, followed by a discussion of the relative implementation complexity of these functions. Next will come a discussion of the details concerning the simulation of the error correction schemes. Finally, results showing the relative performance of the two coding schemes shall be presented and interpreted.

3.1 ERROR CORRECTION SCHEMES FOR THE TWO LINKS

The baseline link uses the non-concatenated error correction coding scheme shown in Figure 12. The quantizer, labeled Q in Figure 12, operates directly on the discrete channel outputs. This channel symbol quantizer uses uniform decision boundary spacings and generates three-bit outputs. The decision boundaries, like the a priori discrete channel output probability densities, are symmetric about zero. The decision boundaries fall at 0%, 25%, 50% and 75% of the discrete channel output that would occur for noiseless operation under benign channel conditions.

The three-bit quantized channel symbols are next deinterleaved with a Type IV (99,61) synchronous deinterleaver. Then reliability weights are assigned to the deinterleaved symbols. For this scheme, the integer values of the three-bit output symbols are good choices for the reliability weights, and hence the W function shown in Figure 12 is actually very trivial. Finally, decoding is performed. The convolutional error correction code has constraint length 7, rate 1/8 and minimum free distance 40. The modulo-2 adder connection pattern is 135 135 147 163 135 135 147 163 (octal). This modulo-2 adder connection pattern is simply two replications of that of the outer code of the concatenated link. The associated soft decision Viterbi decoder retains 31 bits of path history for each state.

As the name suggests, the concatenated link uses a concatenated error correction scheme as shown in Figure 13. This is similiar to the general concatenated code shown in Figure 3 of Section 2, except the innermost interleaver/deinterleaver pair is eliminated to reduce link complexity. The discrete channel output symbols are digitized to several bits of resolution and, unlike the baseline scheme, the quantization error of the discrete channel quantizer can be neglected. These highly resolved digitized symbols are processed by the inner decoder. The inner code is a binary (16,8;5) block code formed by shortening the (17,9;5) cyclic code found in Appendix D of Reference 3. The soft decision inner decoder is

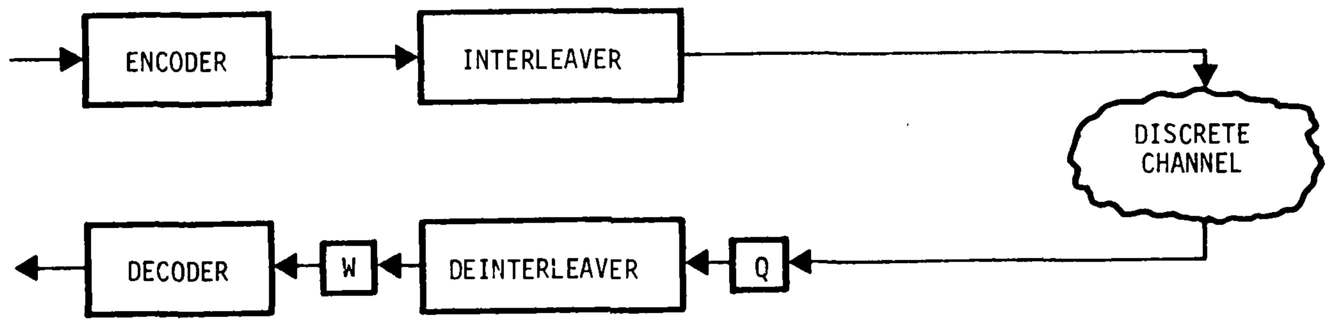


Figure 12. Error correction scheme of baseline link.

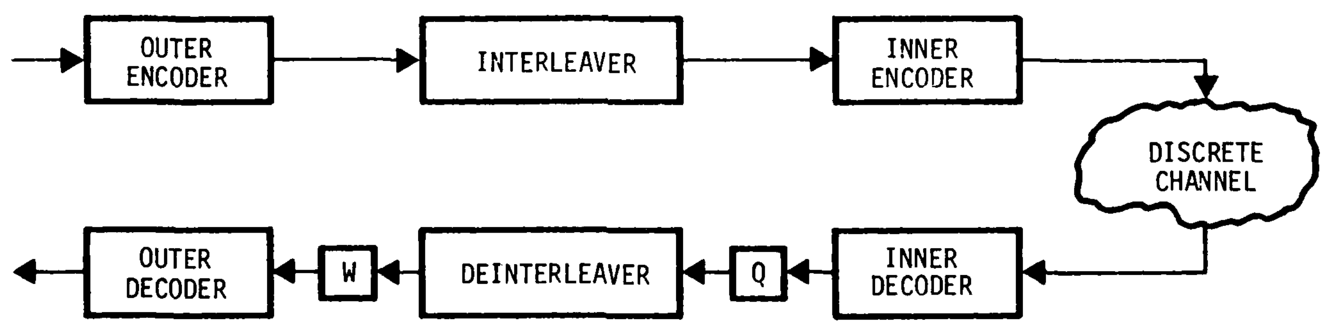


Figure 13. Error correction scheme of concatenated link.

the brute force correlative implementation described in Section 2 with the additional capability of generating a reliability measure for each of the k decoded output bits. These reliabilty measures are formed as follows: Let λ_0 be the largest correlation generated by the decoding algorithm of Section 2 and let m be the index of the codeword associated with λ_m. For $0 \leq i \leq k$, let λ_i be the largest correlation between the input discrete channel sequence and all codewords with indices that differ from m in the $i^{\underline{th}}$ bit. Then the reliability value for the $i^{\underline{th}}$ output bit is taken to be $\lambda_0 - \lambda_i$.

The reliability values are quantized to three bits prior to deinterleaving. It was discovered early in this work that the uniform quantizer decision boundary spacings used by the baseline scheme are unsuited for three-bit quantization of the inner decoder reliability values. This unanticipated difficulty was temporarily resolved by using the following ad hoc rule to choose nonuniformly spaced decision boundaries: Select the boundaries to make the occurrence of the four possible correct quantization levels of the output soft symbols equally likely. Then the proper weighting of each quantized symbol is chosen as the bit log-likelihood ratio as discussed in Section 2. This rule works well but requires knowledge of the inner decoder reliability measure probability distribution, and hence could not readily be used on an actual link because the quantizer would have to adapt to dynamic channel conditions. However, the issue at hand is if the concatenated codes are comparable in performance to non-concatenated codes, and this technique allowed us to carry on with the validation of the performance strength of the concatenated scheme. An advanced SDI concatenated scheme with less sensitivity to quantization threshold spacing will be discussed in Section 5.

Next the quantized inner decoder outputs are deinterleaved. Our intent was to use a Type IV (49,61) interleaver to get a slow fading rate break point of about 1/6 second, nearly identical to that of the baseline link. A subtle programming error, not discovered until after this task was complete, resulted in a Type III (61,49) interleaver actually being modeled. This interleaver has a slow fading break point at 1/5 second instead of the desired 1/6 second, and hence the erroneously used Type III (61,49) interleaver exhibits only slightly different output statistics than those desired. Thus the results are not seriously affected.

The deinterleaved symbols weighted by their bit log-likelihood ratios are next processed by the outer decoder. This rate 1/4 constraint length 7 convolutional outer code has a modulo-2 adder connection pattern of 135 135 147 163 (octal). Like the decoder of the baseline link, the outer soft decision Viterbi decoder of the concatenated link retains 31 bits of path history per state.

3.2 RELATIVE IMPLEMENTATION COMPLEXITY OF THE TWO LINKS

Hardware of a given complexity in the satellite segment of a link costs a great deal more than it does in the ground segment due to: high reliability requirements; extreme environmental conditions; and the cost of placing hardware in orbit. At least partly offsetting this is the fact that there may be many more ground receivers than there are satellites, and the ground units too may have to be designed for severe environmental conditions. For this reason the satellite and ground portions of the link will be considered separately for complexity (and hence cost) comparisions.

Table 6. Satellite segment complexity of the baseline and concatenated links.

	Parameters	Memory Equation	Memory Value (kbits)	Processing Equation	Processing Value (k-ops/s)
BASELINE Convolutional Encoder	k=1, m=40, n=8, R_s=600		nil	(2)	3.1
Interleaver, Equal Subreg.	n =99, n =61, R_s=600 q=1, Type IV	Table 1	6.0	(16)	4.8
Interleaver, Tapered Subreg.	n_2=99, n_1=61, R_s=600, S=60, q=1, Type IV	Table 1	3.0	(19)	327.0
BASELINE TOTALS					
Equal Subreg.			6.0		7.9
Tapered Subreg.			3.0		330.1
CONCATENATED Convolutional Encoder	k=1, m=20, n=4, R_s=300		nil	(2)	1.6
Interleaver, Equal Subreg.	n_2=49, n_1=61, R_s=300 q=1, Type IV	Table 1	3.0	(16)	4.8
Interleaver, Tapered Subreg.	n_2=49, n_1=61, R_s=300, S=60, q=1, Type IV	Table 1	1.5	(19)	163.5
Block Encoder	k=8, m=85, n=16, R_s=600		nil	(1)	3.5
CONCAT. TOTALS					
Equal Subreg.			3.0		9.9
Tapered Subreg.			1.5		168.6

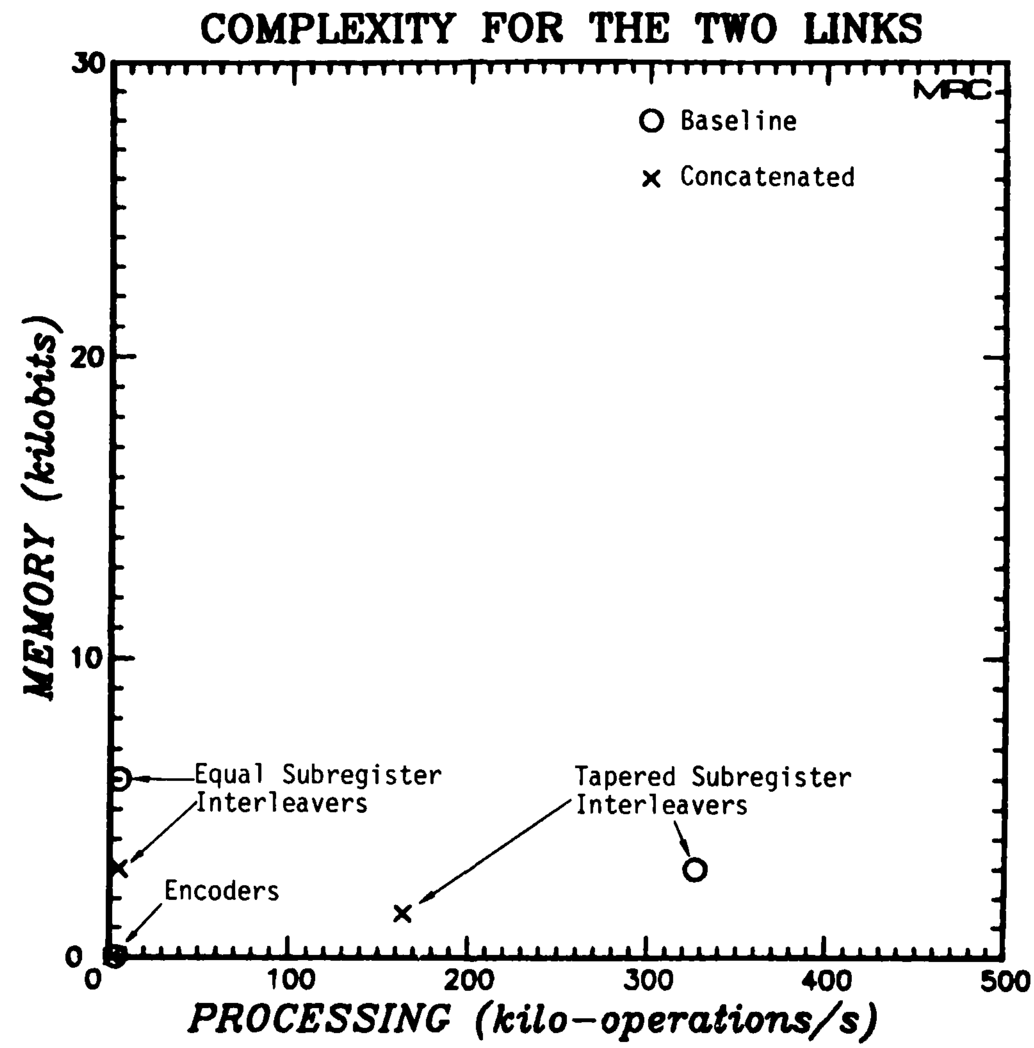


Figure 14. Complexity of satellite segment of the baseline and concatenated links.

3.2.1 Satellite Segment

The satellite segment of the baseline link consists of the convolutional encoder and the interleaver, while the satellite segment of the concatenated link consists of an outer convolutional encoder, an interleaver, and an inner block encoder. The memory and processing for each part of each link are estimated separately in Table 6 and shown graphically in Figure 14, which plots memory versus processing. The interleaver complexity has been estimated both for the equal subregister and tapered subregister implementations. It can be seen that the tapered subregister implementation cuts the memory required in half but greatly increases the processing. Totals for the satellite segment of both links are also given in Table 6 but are not plotted, being virtually the same as the interleaver alone. Clearly the interleaver dominates the cost of the satellite segment, and the concatenated scheme requires only one-half the memory and one-half the processing of the baseline scheme. The reduced complexity is a consequence of the lower symbol rate, R_S, which reduces processing and which also permits a lower value of n_2 as explained in Section 2.

3.2.2 Ground Segment

The ground segment complexity estimates are presented in Table 7 and Figure 15. While the deinterleaver processing remains the same as the corresponding interleavers, the memory is larger due to storage of 3-bit soft symbols as opposed to the single bits in the interleavers. Decoder complexity is a significant factor in overall complexity, and in fact the block decoder is the most complex single item in the concatenated scheme. This is due to the choice of a powerful (16,8;5) block inner code which requires a great deal of processing. The concatenated Viterbi decoder requires almost a factor of seven less processing than the baseline Viterbi decoder because n has been reduced from 8 to 4 (see Equation 9).

Table 7. **Ground segment complexity of the baseline and concatenated links.**

	Parameters	Memory Equation	Memory Value (kbits)	Processing Equation	Processing Value (k-ops/s)
BASELINE Deinterleaver, Equal Subreg.	n_2=99, n_1=61, R_s=600, S=60, q=3, Type IV	Table 2	18.0	(16)	4.8
Deinterleaver, Tapered Subreg.	n_2=99, n_1=61, R_s=600, S=60, q=3, Type IV	Table 2	9.0	(19)	327.0
Viterbi Decoder	k=1, K=7, n=8, R_s=75, hK=31	(12)	3.0	(9)	159.0
BASELINE TOTALS					
Equal Subreg.			20.5		163.8
Tapered Subreg.			11.5		496.0
CONCATENATED Block Decoder	n=16, k=8, R_s=300		nil	(6)	307.2
Deinterleaver, Equal Subreg.	n_2=49, n_1=61, R_s=300, S=60, q=3, Type IV	Table 2	9.0	(16)	2.4
Deinterleaver, Tapered Subreg.	n_2=49, n_1=61, R_s=300, S=60, q=3, Type IV	Table 2	4.5	(19)	163.5
Viterbi Decoder	k=1, K=7, n=4, R_s=75, hK=31	(12)	3.0	(9)	23.2
CONCAT. TOTALS					
Equal Subreg.			11.5		332.8
Tapered Subreg.			7.0		493.9

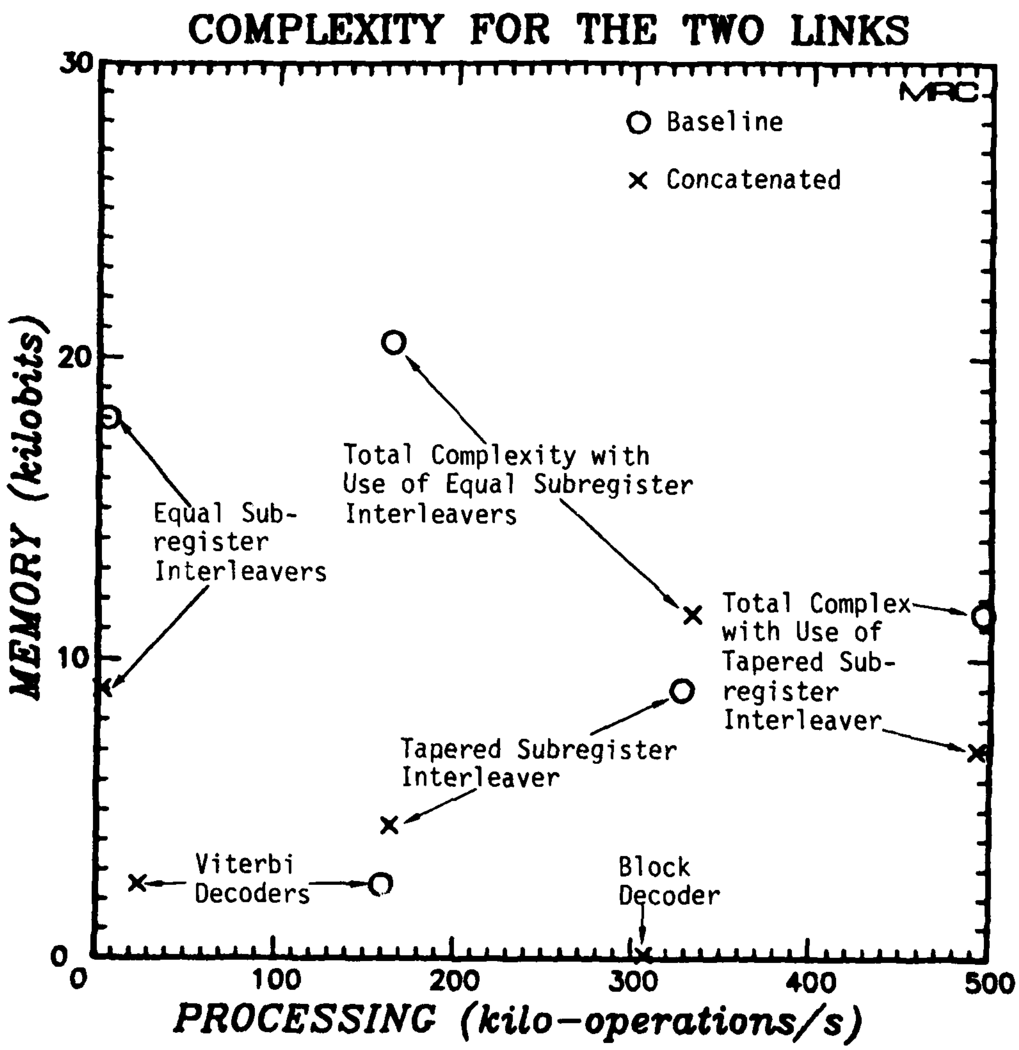


Figure 15. Complexity of ground segment of the baseline and concatenated links.

The total complexity of the ground segment of the baseline and concatenated links is comparable - the concatenated advantage gained in the deinterleaver and the Viterbi decoder was offset by the high complexity of the block decoder. The studies of Sections 4 and 5 investigate the performance of concatenated SDI schemes using less complex (but weaker) inner codes.

3.3 SIMULATION DESCRIPTION

The descriptions of the simulation in general and the simulation of the discrete channel in particular are presented in Section 2. Here we cover the simulation of the error correction coding schemes only. The error correction schemes of both links are simulated by the method shown in Figure 16. An arbitrary message is encoded and interleaved explicitly. The encoded binary message is superimposed upon the received signal data to form the simulated discrete channel output. As shown in Figure 16, *modulated discrete channel outputs* are constructed by multiplying the associated unmodulated discrete channel output from the received signal data file by -1 or +1, depending upon the transmitted binary encoded symbol being a 1 or a 0, respectively.

Since error correction schemes of modern receiving terminals are implemented with digital processors, the decoding and deinterleaving is performed in the digital computer simulation as it would be done in hardware. The channel symbol sequences are generated explicitly with the encoder and interleaver algorithms discussed in subsection 3.1. As shown in Figure 16, the decoded binary message is compared with the suitably delayed source binary message to generate an error pattern. The errors are counted to perform a Monte Carlo estimate of the link error rate.

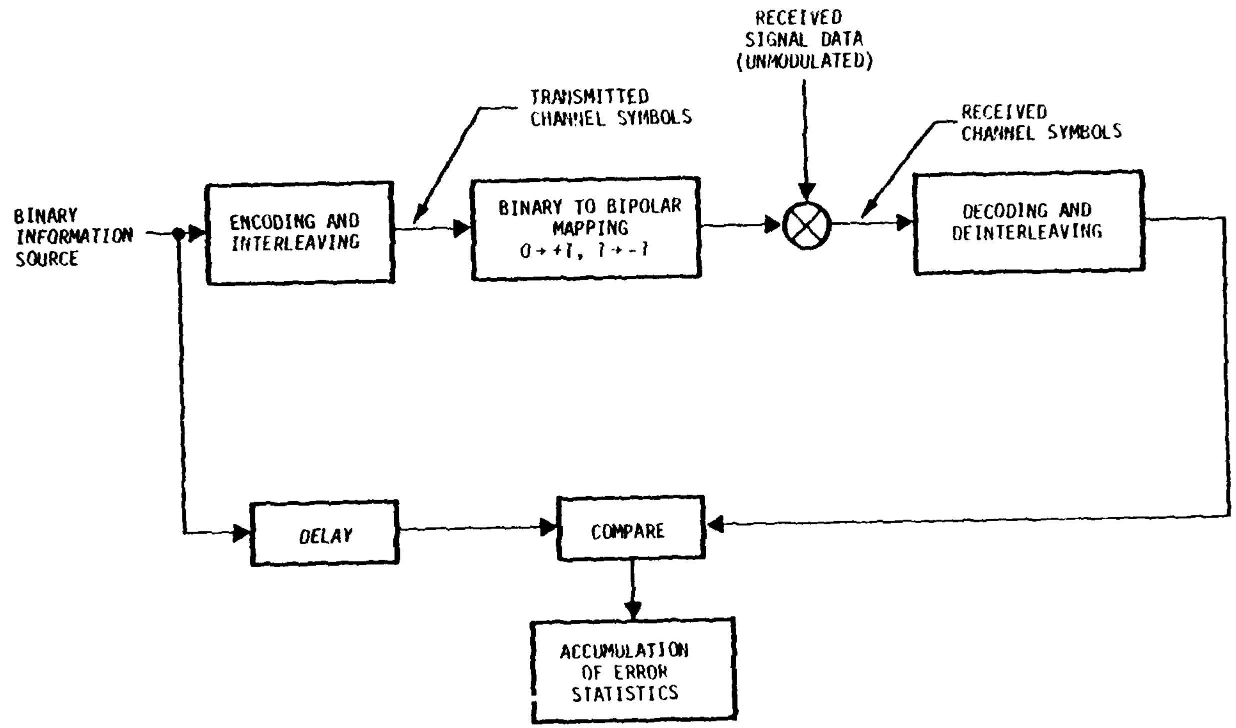


Figure 16. Error correction simulation for both the baseline and concatenated links.

The simulation could have been simplified by not encoding an arbitrary message, but rather assuming transmission of the all-zero message. Since all codes used in the two links are linear, the all-zero message is encoded into the all zero channel symbol stream, and hence the link output itself could be taken as the error pattern. However, it was feared that use of this simplification might bias the error rate estimate due to the manner in which the decoders resolve ties in the maximum codeword likelihood decision (for correlative decoders of block codes) and maximum branch metric decision (for Viterbi decoders of convolutional codes). After comparing results using the all-zero message, the all-one message and several random messages, we have observed that the error correction strengths of both code types are insensitive to the particular message transmitted.

3.4 RESULTS

The primary results of this study are in the form of a plot of information bit error rate versus E_b/N_o for the two values of τ_o. These plots are shown in Figure 17.

The error rates of the two links are plotted versus the mean E_b/N_o level seen at the output of the PNSS code tracking loop. This generalizes the results to links not using this type of spread spectrum diversity. However, for the links of interest, E_b/N_o is not precisely proportional to transmitter power because the code tracking loop loss is signal-strength dependent. To interpret the plots in terms of mean E_b/N_o seen at the code tracker input, skew the abscissa of Figure 17 according to Table 5 of Section 2.

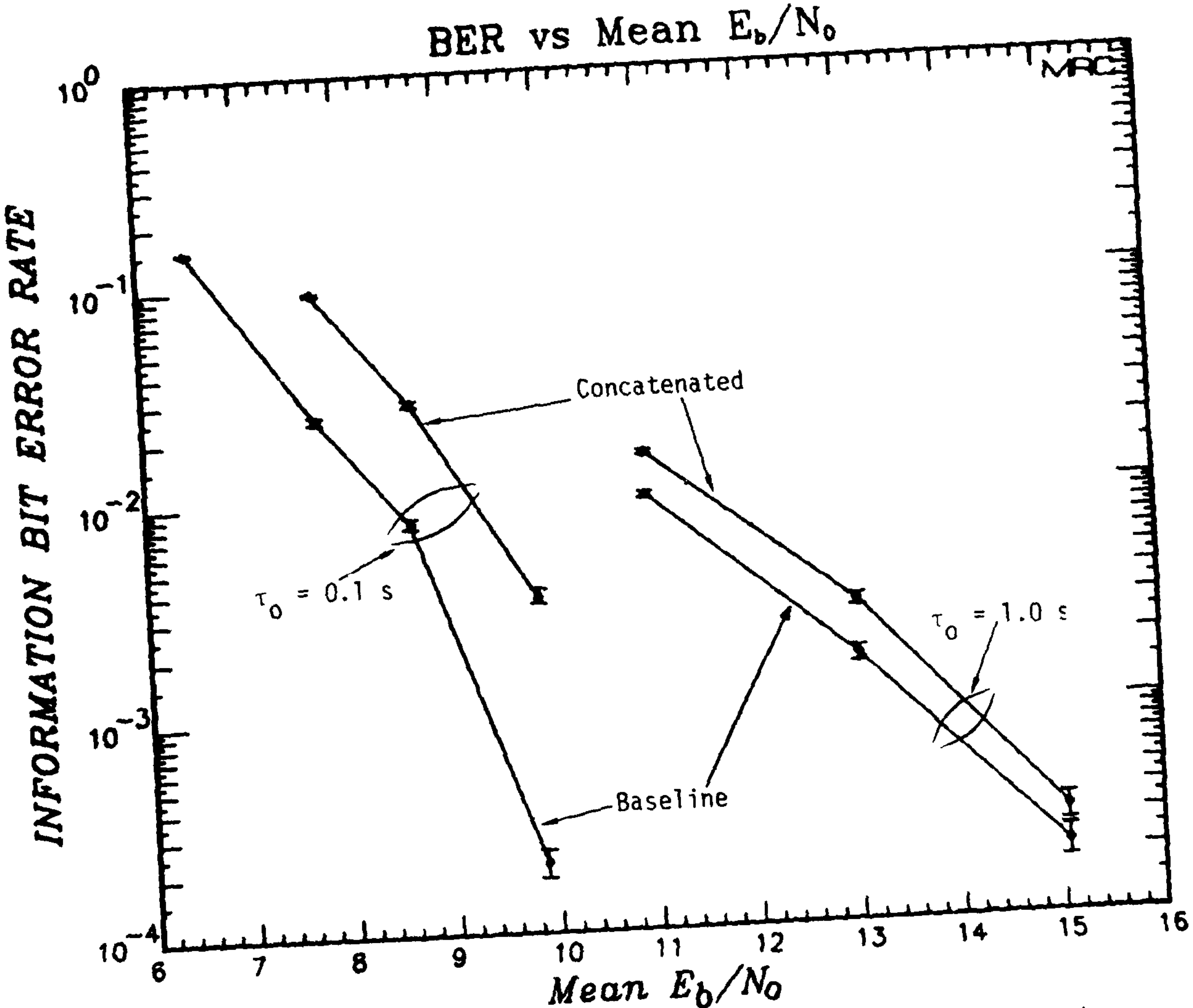


Figure 17. Information bit error rate for the two links of interest under fading channel conditions versus mean E_b/N_o.

The key point to be seen from Figure 17 is that the two schemes are within a dB of each other. Results were not obtained at lower error rates due to the excessively large sample sizes required to make statistically significant measurements. Since the simple SDI concatenated scheme used here is not a candidate for implementation, simulation runs were not made for the full range of anticipated values of τ_0. These results are only intended to be representative of link performance to establish that there is not a great difference between the performance of the coding schemes, and they are not a comprehensive evaluation of the communication links.

The error bars in Figure 17 are intended to indicate the one-sigma confidence intervals of the data. The formula used to calculate the one-sigma error bars was derived under the assumption of independent link errors. However, all error correction schemes used in this study are known to produce bursts of errors, and hence the independence assumption is invalid. As can be seen in Figure 17, the confidence intervals are optimistically narrow. In spite of this, the error bars are indicative of the relative reliability of the data in that the variance of the bit error rate estimates decreases monotonically with the separation of the upper and lower error bars.

3.5 CONCLUSION

The primary conclusion of this study is that the error correction strength of SDI concatenated codes is comparable to that of non-concatenated codes of equal rate in a disturbed channel. The particular SDI concatenated scheme used here is not recommended because of the need for an adaptive quantization function. An SDI concatenated coding scheme without this drawback shall be presented in Section 5. This brief preliminary study gives promise to the error correction encoding/decoding scheme of Section 5 as a technique to substantially reduce implementation complexity without a correspondingly great reduction in performance.

The second finding of this work, previously discussed in subsection 3.1, is that quantization effects are significantly more inportant in the SDI concatenated link than they are in the baseline link. This is due to the fact that the rate reduction of the inner code necessitates that more reliability information be contained in each deinterleaved symbol. Having identified quantization as a key issue, it will be given greater attention in our forthcoming studies.

The results of the next section were obtained after the work documented here was completed. One finding of Section 4 pertains significantly to this study and it is appropriate to mention it now. During the course of that study, the error correction strength of the rate 1/8, constraint length 7, convolutional code used in the baseline scheme became suspect. Even though the minimum free distance of this code is the largest known of any code with its rate and constraint length, we found another code with the same minimum free distance, rate and constraint length that exhibited superior error correction strength. The difference amounts to about 1 dB in a fading channel and less than half a dB in a benign channel. We hasten to point out that this finding widens the performance gap between the baseline and SDI concatenated schemes.

The findings of this preliminary investigation of SDI concatenated codes are somewhat blurred by the use of the suboptimal baseline code, and by the sensitivity of the concatenated scheme to quantizer parameters. We have verified that SDI concatenation does not pay a great performance penalty for its reduction in implementation complexity, but as yet we have not accurately quantified the performance difference between the baseline code and a concatenated code which can be implemented.

SECTION 4

SDI CONCATENATION OF CONVOLUTIONAL CODES WITH CHIP REPEATING

This study addresses several aspects of concatenated schemes employing simple chip repetition and accumulation as the inner code. The use of chip repeating to reduce link complexity was suggested by Bucher (Reference 21). This scheme has the advantage of requiring only one relatively simple algorithm to perform both the inner decoding (chip combining) and deinterleaving operations and, unlike the simple concatenated scheme of Section 3, allows the interleaver function to scramble the discrete channel symbols.

This scheme appears to be attractive for rate 1/8 codes on the basis of the effective d_f of an overall rate 1/8 convolutional code. Here we shall quantify the relative performance of four overall rate 1/8 coded links using different combinations of chip repeating and convolutional coding with detailed computer simulation-aided analysis.

As with all schemes addressed in this report, we are principally concerned with implementation complexity and error correction strength. In the context of this study, the occasion arose to specifically address the sensitivity of error correction strength to the decision boundary spacing of the memoryless, uniform quantizer used to digitize the discrete channel outputs. Also in the context of this work, the relative strength of two rate 1/8, constraint length 7 convolutional codes became an issue, and this also is discussed.

First a description of the four coding techniques will be presented. Then their relative implementation complexities will be discussed. This will be followed by a discussion of the computer simulation used to analyze the coded links of interest. Lastly the simulation-generated results will be presented and interpreted.

4.1 DESCRIPTIONS OF THE FOUR LINKS

The error correction scheme used in all four links is shown in Figure 18. The 75 bit per second information bit stream is encoded with a constraint length 7 convolutional code of rate 1/8, 1/4, 1/2 or 1 for Links 1, 2, 3 and 4, respectively. The encoded bits are immediately repeated with redundancy 1, 2, 4 or 8 to yield an overall code rate of 1/8 and a channel symbol rate of 600 chips per second for each link. The channel symbols are interleaved and transmitted over a binary symmetric discrete channel comprised of DPSK modulator/demodulator, direct sequence pseudonoise spreader/despreader and propagation medium. The discrete channel outputs are quantized to three bits (eight levels) by a midriser uniform quantizer and then simultaneously deinterleavered and combined "on the fly." The combined symbols are decoded with the Viterbi algorithm, which retains 31 bits of path history per state.

Table 8 summarizes the error correction coding parameters of each link. The last column gives the modulo-2 adder connection patterns for each convolutional code. The patterns for Links 2 and 3 were found by Larson (Reference 5), using an exhaustive search by computer. Such a search is infeasible for the rate 1/8 code of Link 4 because required computation time is proportional to 2^{nkK}. The code used for Link 4 was found by starting with the four modulo-2 adder connections of Link 3 and using a computer search to find the best connection pattern for the other four modulo-2 adders. While this is known to be a very good code, it has not been proven to be the best possible.

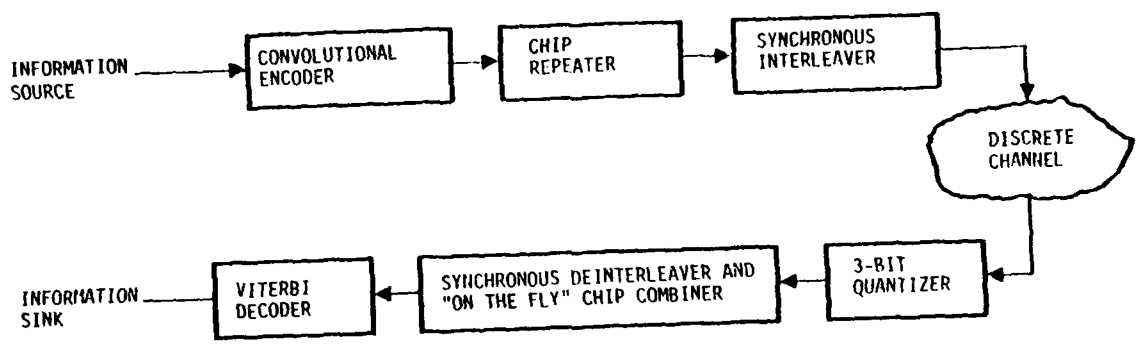


Figure 18. Block diagram for the four links of interest. (Error Correction Schemes)

Table 8. Link characteristics

Link Number	Chips Per Bit (C)	Convolutional Code Rate $R_c = (\frac{k}{n})$	Convolution Code Connection Pattern (octal)
1	8	1 (n=1)	none
2	4	1/2 (n=2)	133,171
3	2	1/4 (n=4)	135,135,147,163
4	1	1/8 (n=8)	135,135,147,163, 125,177,133,171

For all links:

Information Rate = 75 bits/s

Overall Code Rate= 1/8

Chip Rate = 600 chips/s

Convolutional Code with Viterbi Decoding K = 7, n = 1, hK = 31

Direct Sequence PNSS

DPSK Modulation

Demodulator Quantization = 3 bits, uniform

When a chip combiner is used as an inner code, the free distance of the overall code (supercode) is simply the free distance of the outer code times the number of chips combined. The minimum free distances of the convolutional outer code of Links 2, 3, and 4 are 10, 20, and 40 respectively; so the overall minimum free distance of the supercode is 40 in each case.

4.2 IMPLEMENTATION COMPLEXITY OF THE FOUR LINKS

Again the memory and processing requirements for the deinterleavers and decoders for each link will be discussed.

The chips can be combined "on the fly" as they are written into the deinterleaver memory. The equal subregister synchronous deinterleaver algorithms of Type I and III can be readily modified to perform "on the fly" chip combining. This is done by mapping the addresses for the C chips to be combined into a single address and accumulating all C chips into that one address. The number of bits for soft symbol resolution, q, increases by $\log_2 C$ in the process. This implementation gives the functional time diversity advantage of interleaved chips with the complexity advantage of reducing storage by almost 1/C in the deinterleaver.

The complexity estimates of the four links are presented in Table 9 and Figure 19. The link is broken down into its deinterleaver/chip combiner and Viterbi decoder functions in the table, while the figure shows only totals for the four links. The equations for computing deinterleaver/chip combiner complexity differ slightly from those of Table 2 and Equation 14 due to the chip combining operation:

$$M_{eq} = \frac{(n_2-1)(n_1+1)}{C} q \text{ bits} \quad , \qquad (22)$$

Table 9. Ground segment complexity of the four links.

	Parameters	Memory Equation	Memory Value (kbits)	Processing Equation	Processing Value (k-ops/s)
LINK #1 Deinterleaver/ Chip Combiner	n_2=100, n_1=9, R_{out}=75, R_{in}=600, q=6, Type III	(22)	0.7	(23)	5.5
Viterbi Decoder	None		--		--
LINK #1 TOTALS			0.7		5.5
LINK #2 Deinterleaver/ Chip Combiner	n_2=100, n_1=61, R_{out}=150, R_{in}=600, q=5, Type III	(22)	7.7	(23)	5.7
Viterbi Decoder	k=1, K=7, n=2, R_s=75, hK=31	(12)	3.0	(9)	15.5
LINK #2 TOTALS			10.7		21.2
LINK #3 Deinterleaver/ Chip Combiner	n_2=100, n_1=61, R_{out}=300, R_{in}=600, q=4, Type III	(22)	12.3	(23)	6.0
Viterbi Decoder	k=1, K=7, n=4, R_s=75, hK=31	(12)	3.0	(9)	23.2
LINK #3 TOTALS			15.3		29.2
LINK #4 Deinterleaver/ Chip Combiner	n_2=100, n_1=61, R_s=600, q=3, Type III	(22)	18.4	(16)	4.8
Viterbi Decoder	k=1, K=7, n=8, R_s=75, hK=31	(12)	3.0	(9)	159.0
LINK #4 TOTALS			21.4		163.8

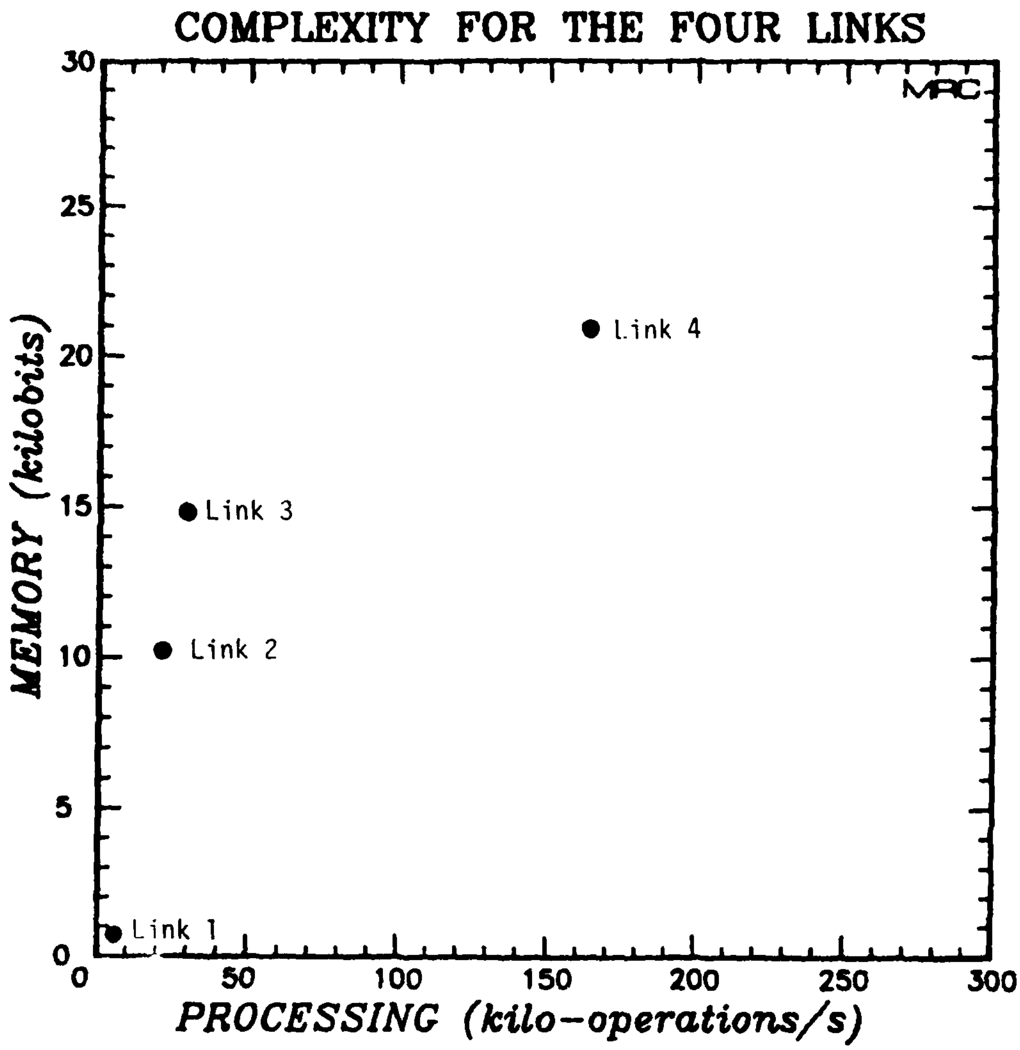


Figure 19. Total complexity of the four links of interest.

$$P_{eq} = 9R_{in} + 2R_{out} \quad \text{operations/second,} \tag{23}$$

where R_{in} is the deinterleaver input symbol rate and R_{out} is the output symbol rate ($R_{in} = CR_{out}$). As expected, both processing and memory complexity increase with link number.

4.3 SIMULATION DESCRIPTION

Our link simulations in general and the simulation of the discrete channel in particular are discussed in Section 2. Here only the simulation of the error correction coding schemes is covered. The error correction of all four links is simulated by the method shown in Figure 20. An arbitrary message is encoded and interleaved explicitly. The encoded binary message is superimposed upon the received signal data to form the simulated discrete channel outputs. As shown in Figure 20, this is accomplished by multiplying the associated unmodulated discrete channel output from the received signal data file by -1 or 1, depending upon the transmitted binary encoded symbol being a 1 or a 0, respectively.

Since the error correction schemes of modern receiving terminals are implemented with digital processors, the decoding and deinterleaving is performed in the digital computer simulation as it would be done in hardware. The details pertaining to these functions were discussed in Subsection 4.1, and need not be repeated here. As shown in Figure 20, the received binary message is compared with the suitably delayed input binary message to generate an error pattern. The errors are counted to perform a Monte Carlo estimate of the link error rate.

The discrete channel simulation described in Section 2 models a disturbed propagation medium with high fidelity by using the MPS data shown in Figures 11 and 12 of Section 2 to synthesize the received carrier

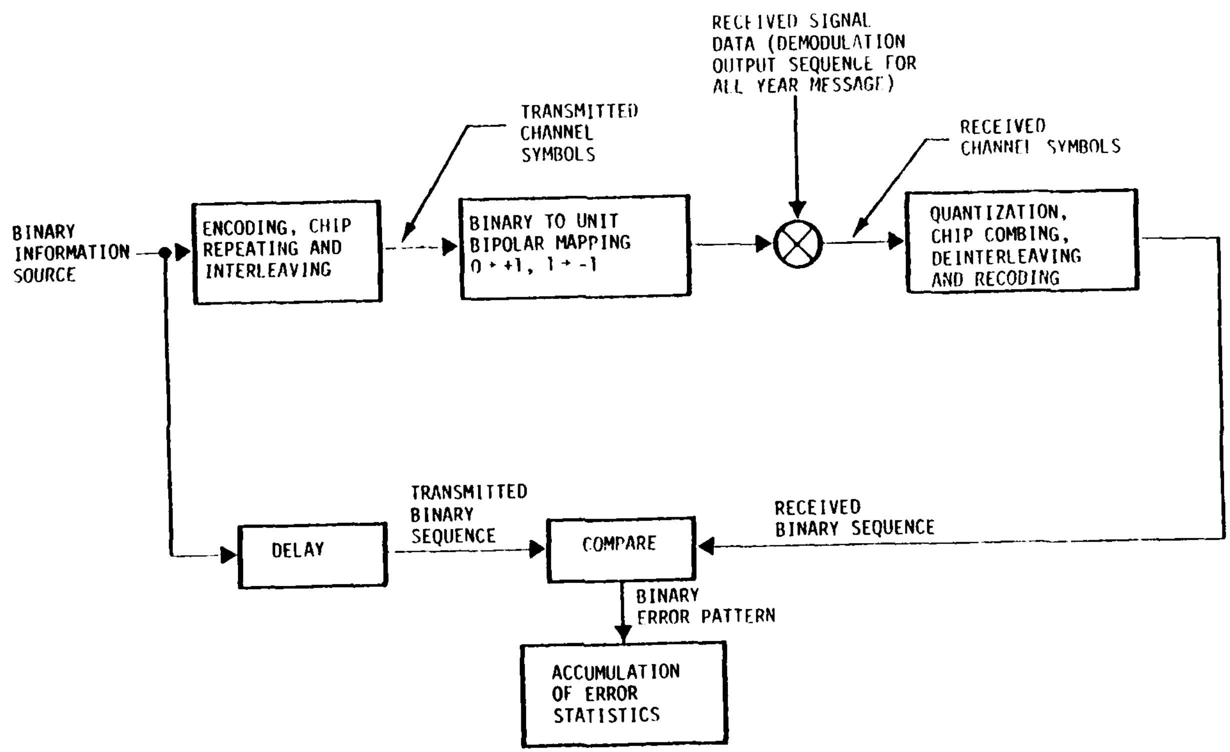


Figure 20. Error correction simulation for all four links.

complex envelope. In this study the link performance in benign channel conditions is also analyzed. This is accomplished in the Modem Simulation Program by simply making the simulated received carrier complex envelope amplitude and phase constant instead of using the MPS data.

A key parameter affecting the coding performance is the decision boundary spacing of the midriser uniform quantizer that digitizes the demodulator outputs to three bits. Each simulation run was repeated for five values of the quantizer decision boundary spacing to determine the sensitivity of this parameter in each simulated channel condition. Since the three-bit quantizer has a fixed output symbol alphabet size of eight, the choice of decision boundary spacing determines the quantizer's dynamic range. This is illustrated in the quantizer input/output characteristic of Figure 21. The inputs can be thought to fall into eight "bins" defined by $\pm x_1$, $\pm x_2$ and $\pm x_3$. As shown in the figure, the saturation points of the uniform quantizer are defined to be the outer edges of imaginary bins of width x_1 that extend past $+x_3$ and $-x_3$ away from the origin. The quantizer dynamic range (QDR) is defined as the separation between the two saturation points. Table 10 shows the values of QDR, saturation points and decision boundaries for the five sets of quantizer parameters considered in this study.

Table 10. Quantizer dynamic range, saturation point and decision boundaries for midriser uniform quantizers.

QDR	Saturation Points	Decision Boundaries x_1	x_2	x_3
1.5	±0.75	0.1875	0.3750	0.5625
2.0	±1.00	0.2500	0.5000	0.7500
3.0	±1.50	0.3750	0.7500	1.1250
4.C	±2.00	0.5000	1.0000	1.5000
5.0	±2.5	0.6500	1.2500	1.8750

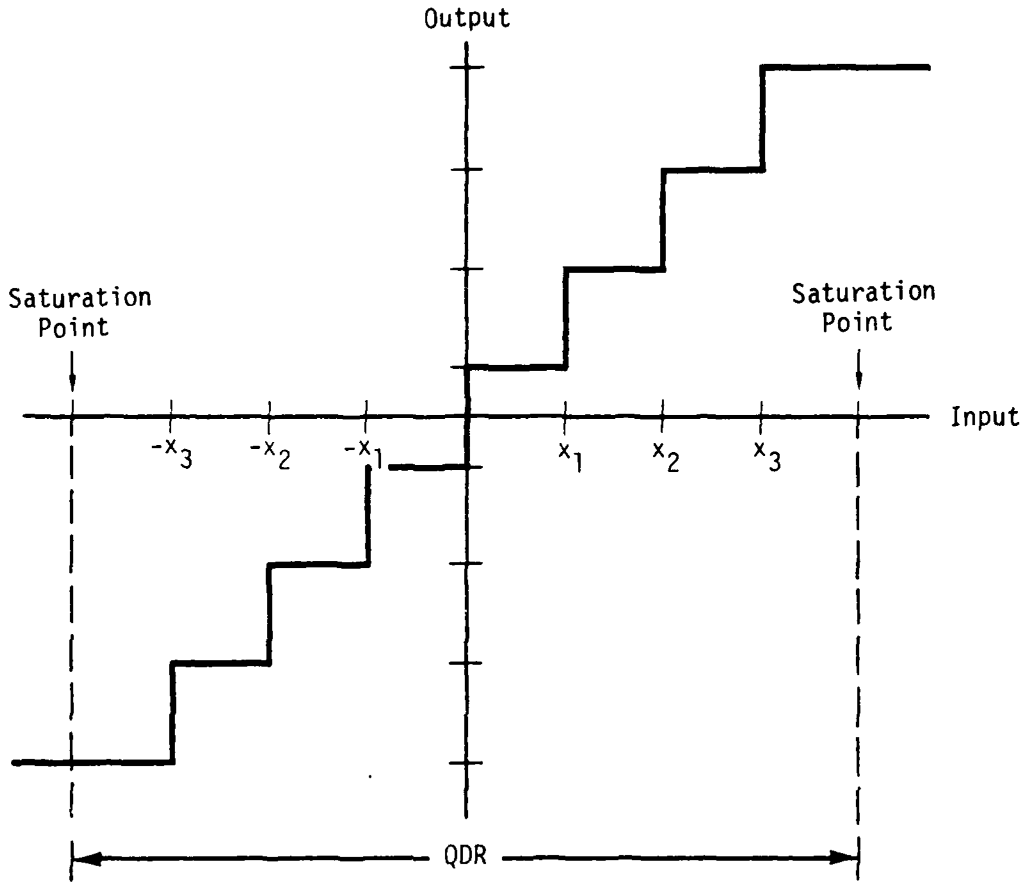


Figure 21. I/O characteristic of eight level (3 bit) midriser uniform quantizer.

Under noiseless benign channel conditions, the simulated discrete channel outputs would be either a +1 or a -1. Because the input to the quantizer has a nominal unit magnitude, QDR will often be referred to as "normalized" QDR.

4.4 RESULTS

Figure 22 illustrates the mix of computer runs that generated the results of this section. The figure has two tree structures of depth three. The top tree structure corresponds to the generation of the benign channel results and the bottom corresponds to the fading channel results. It is instructive to compare each tree with the simulation block diagram of Figure 9 in Section 2. Each tree originates with the channel description associated with the MPS Simulation Program and an MPS data file. Each channel condition branches into three noise levels associated with the Modem Simulation Program and three received signal data files. Each modem branches into the four links associated with the Error Correction Scheme Simulation Program. In addition, results for the four link types were accumulated for each of the five quantizers of Table 10. The major results generated by the simulations are plotted in three forms: histograms of demodulator output levels; measured probability distributions of quantizer output symbols; and curves of link error rate versus quantizer decision boundary spacing and E_b/N_o.

An abundance of quantized symbol and sum probability distribution plots will be presented to serve three purposes. These will characterize the manner in which, and the degree to which, the first-order statistics of the demodulator outputs are changed by quantization. Secondly, these provide sufficient information to much more efficiently model communication links utilizing an interleaver that decorrelates the channel

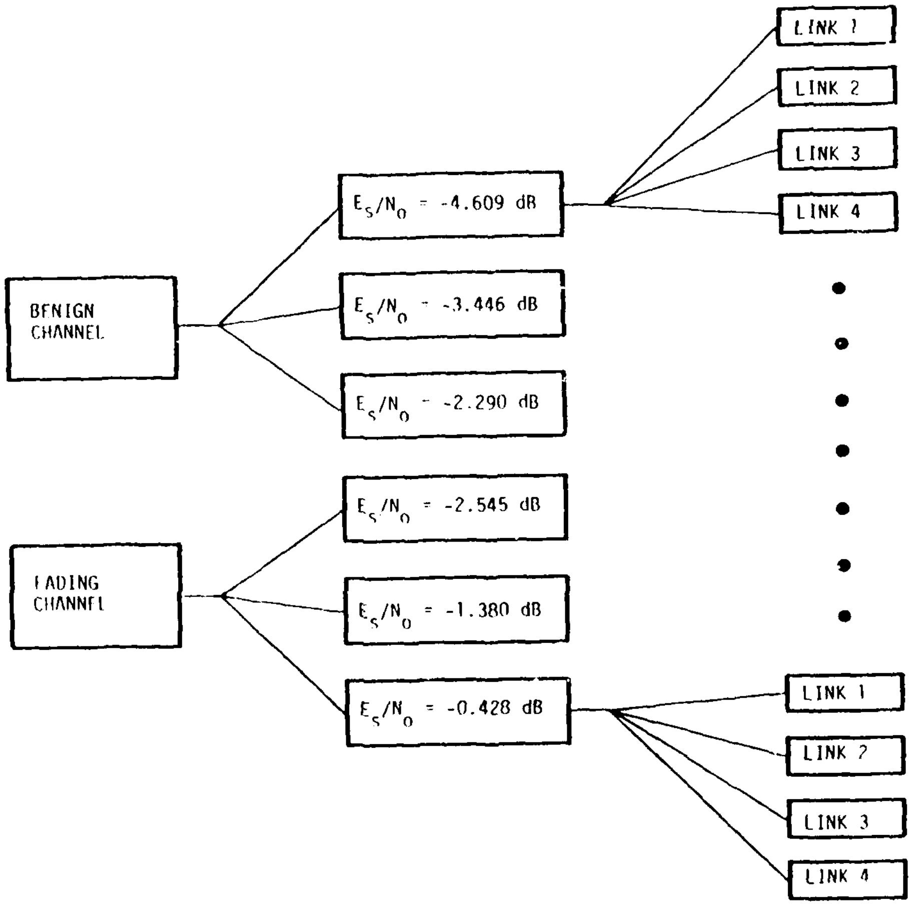


Figure 22. Tree diagram of simulation runs.

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A PRELIMINARY INVESTIGATION OF CONCATENATED CODING SCHEMES UTIL--ETC(U)
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symbols over the duration of the decoder memory. The deinterleaver output data stream can be directly generated by sampling the probability distribution associated with a particular channel condition instead of explicitly modeling the propagation medium, modem, quantizer and deinterleaver. Lastly, these data might be used to analytically bound the soft decision decoded bit error rates in a manner similar to that done for hard decision decoding in Reference 4. These bounds were not derived in this study, but such analyses may be pursued in the future.

The error bars on all plots of information bit error rate are intended to indicate the one-sigma confidence intervals of the data. The formula used to calculate the one-sigma error bars was derived under the assumption of independent link errors. However, all error correction schemes used in this study are known to produce bursts of errors, and hence the independence assumption is invalid. As will be seen in subsequent figures, the confidence intervals are optimistically narrow. In spite of this, the error bars are indicative of the relative reliability of the data in that the variance of the bit error rate estimates increases monotonically with the separation of the upper and lower error bars.

4.4.1 Additive White Gaussian Noise (AWGN) Channel Results

Simulation runs were made at three SNR levels. The discrete channel noise parameters and channel symbol error rates for the three channel conditions are summarized in Table 11.

Table 11. E_b/N_o and E_s/N_o before and after the despreader and the channel symbol error rates for each of the three noise levels in benign channel conditions.

Before Despreader E_b/N_o (dB)	Before Despreader E_s/N_o (dB)	After Despreader E_b/N_o (dB)	After Despreader E_s/N_o (dB)	Channel Symbol Error Rate
6.000	-3.031	4.420	-4.609	0.375
7.000	-2.031	5.585	-3.446	0.155
8.000	-1.031	6.740	-2.290	0.013

The histograms of the demodulator outputs and the measured distributions of the quantizer outputs for the five values of QDR are shown in Figures 23 through 85. These data were accumulated for the unmodulated discrete channel outputs and should be interpreted as being conditioned on transmission of a binary zero. The histograms and probability distribution functions (PDF) conditioned on transmission of a binary one would be just the reflection about the vertical axis of those shown in the figures. The histograms and PDF's for random equally likely channel symbols would be the average of those histograms conditioned on transmission of a zero and those conditioned on transmission of a one. Notice that the demodulator output histograms of Figures 23 and 44 and 65 are roughly centered about zero. Careful examination of these three curves reveals that the mode is closer to zero for histograms associated with smaller values of E_S/N_O. In the limiting case of infinite E_S/N_O, each histogram would have the form of an impulse at unity.

Each quantized channel symbol is represented with three bits. These bits are interpreted as being in standard binary form so that the outputs range in value from 0 to 7. In the figures, the distributions of quantized outputs are not plotted with respect to index, but rather with respect to the center of the associated "bins" partitioned by the quantizer decision boundaries. This facilitates the comparison of the quantized symbol PDF's with the demodulator output histograms. However, the chip combining is performed on the three-bit indices. Hence the indices of the 2 chip sums range from 0 to 14. Similarly the indices of the 4 and 8 chip sums range from 0 to 28 and 0 to 56. In all the PDF's of this section, the 0 index is associated with the leftmost discrete point, and the indices of the other points increase sequentially to the right in integer steps. Like the histograms, the PDF's are skewed to the right because of the conditioning of the measurements upon the transmission of the all-zero message. The quantizer output indices 3, 2, 1 and 0 correspond to reception of a binary 1, and are listed in order of increasing reliability. Similarly, the indices 4, 5, 6 and 7 correspond to reception of a 0, and again are listed in order of increasing reliability.

Figures 24 through 28 show the PDF of the quantized channel symbols for the five values of QDR with $E_S/N_0 = -4.609$ dB. For a small value of QDR of 1 (Figure 24), the quantizer extremal symbols, 0 and 7, have relatively large probabilities. Hence the quantizer output statistics are nearly equivalent to those of a hardlimiter, and most of the performance gain of soft decision processing is lost.

Figures 29 through 33, 34 through 38, and 39 through 43 show the chip combined symbol PDF's for Links 1, 2, 3 and 4, respectively. Due to the nature of DPSK modulation, channel errors usually occur in pairs. The deinterleaver randomizes error pairs, so we expect that the PDF of the combined symbols are related to the PDF of the quantized channel symbols. Specifically, the C chip sum PDF is the quantized channel symbol PDF convolved with itself C times. However, the fading decorrelation time break point of the interleavers is one-sixth second and the channel fading decorrelation time is one tenth second. Hence, an occasional fade will be sufficiently long to effect some correlation between summands of common combined symbols, and the convolutional relationships between the various PDF's are then only approximate. For example, the measured PDF of the 2 chip sums for QDR = 1.5 shown in Figure 29 is seen to be the convolution of the associated channel symbol PDF (Figure 24) with itself. Initially, the probability associated with the combined symbol of index 7 in Figure 29 may appear anomalous. However, it is predicted by the convolution relationship because of the large extremal symbol probabilities of Figure 24. The PDF's of the 4 and 8 chip sums of QDR = 1.5 (Figures 34 and 39) are progressively smoother and more Gaussian in appearance, as required by the Central Limit Theorem for truly independent summands.

Figure 28 shows the quantized channel symbol distribution for QDR equal to 5.0. Here the extremal symbol probabilities are small and the minimal symbols (indices 3 and 4) are starting to dominate. For somewhat larger values of QDR, the nonminimal quantized symbols would have very small probabilities and, as for very small QDR, most of the performance of soft decision processing again would be lost.

Figure 26 shows the quantized channel symbol distribution at the same value of E_S/N_O for a median value of QDR of 3.0. Here the extremal quantizer values are not as dominate as before. Hence the corresponding combined chip PDF's of Figures 31, 36 and 41 do not have spurious looking points for smaller QDR. Again these distributions become progressively more Gaussian as the order of the chip combining increases.

Figures 44 through 64 and 65 through 85 show the demodulator output histogram and the various channel symbol and combined symbol PDF's for E_S/N_O = -3.446 dB and E_S/N_O = -2.290 dB, respectively. All the above remarks pertaining to the data associated with E_S/N_0 = -4.609 apply to these values as well. One further observation is that a comparison of Figures 23, 44 and 65 indicates that the AGC does a good job of maintaining the first-order statistics of the demodulator outputs over the three noise levels.

Figures 86 through 89 show the decoded bit error rate versus QDR for the three values of E_S/N_0 for Links 1, 2, 3 and 4. All four links are insensitive to QDR for signal-to-noise ratio values associated with very high error rates, but the sensitivity to QDR increases with signal-to-noise ratio for Links 2, 3 and 4. It appears that a good choice of QDR is 3.0.

To confirm the proper operation of the error correction simulation program, the Link 4 simulation runs were repeated with a different convolutional code that mimics the Link 3 coding scheme. As presented in Table 7, the connection pattern of the modulo-2 adders for the Link 3 rate 1/4 code is

135 135 147 163 (octal),

and the connection pattern for the normal Link 4, rate 1/8 code is

135 135 147 163 125 177 133 171 (octal).

The modified connection pattern for the rate 1/8 code is a replication of that of the Link 3 code:

135 135 147 163 135 135 147 163 (octal).

The error correction capabilities of the two Link 4 codes are compared in Figure 90. As expected, the modified code is weaker than the original Link 4 code by about 1/4 dB. Hence these new simulation results are consistent with those discussed above. A very careful comparison of Figures 88 and 90 reveals that the modified Link 4 code slightly outperforms the Link 3 coding scheme. The small difference can be attributed to the fact that additions of an even number of 3 bit indices occasionally result in ties, and the two-chip combining operation must arbitrarily resolve these ties earlier in the Link 3 decoding process than is necessary in the Link 4 Viterbi decoder.

The next four figures repeat the data of Figures 86 through 89 in different formats. Figure 91 is the decoded bit error rate plotted against E_S/N_0 for QDR equal to 3.0, the apparent optimal value of that parameter. It can be seen that the error correction capabilities of Links 2, 3 and 4 do not differ drastically. The difference in terms of equivalent signal-to-noise ratio (SNR) is about 0.25 dB between Links 2 and 3 and the same between Links 3 and 4. Figures 92, 93 and 94 show curves of decoded bit error rate versus QDR for the four links at E_S/N_0 equal to -4.609 dB, -3.446 dB and -2.290 dB, respectively. This presentation of the data seems to indicate that the differences in link performance tend to widen as the SNR is increased.

4.4.2 Fading Channel Results

The fading channel results were accumulated using received signal data files generated in the task associated with Section 3. The associated SNR parameters and channel symbol error rates are listed in Table 5 of Section 2. Data for this section was collected for the channel conditions corresponding to only the first, second and fourth entries of the table. For these channel conditions, τ_0 is 0.1 second and the values of E_S/N_0 are -2.55 dB, -1.38 dB and -0.428 dB measured at the output of the despreader (or code tracking loop).

As shown in Figure 22, the matrix of computer runs that generated the fading channel results is very similar to that for the benign channel. Figures 95 through 157 show the demodulator output histograms and the various combined sum measured PDF's for all three channel conditions. These have the same form and are in the same order as the corresponding results of the benign channel. Hence the discussions of Figures 29 through 85 apply to Figures 95 through 157 as well.

Figures 158 through 161 show decoded bit error rate versus QDR at each E_S/N_0 for Links 1, 2, 3 and 4 respectively. As with the benign channel results, the sensitivity to QDR increases with decreasing bit error rate and again 3.0 appears to be a good value of QDR. The Link 4 results (Figure 161) indicating a sharp drop in bit error rate at QDR equal to 5.0 at the two higher values of E_S/N_0 are probably spurious. As indicated previously, the one-sigma confidence intervals are actually larger than the error bars shown in the figure.

The modified Link 4 convolutional code that mimics the operation of Link 3 was exercised for the fading channel. A comparison of the modified and normal Link 4 code strengths is shown in Figure 162. The difference between the codes is about the same 1 dB that separates the performance of Links 3 and 4 above. The modified rate 1/8 code was used in the baseline decoder of Section 3. The superior code was discovered after that work was performed. The existence of the superior rate 1/8 code impacts the findings of Section 3, and is discussed in Subsection 3.5.

Figure 163 shows the decoded bit error rate plotted against E_S/N_O for QDR equal to 3.0. The bit error rate does not decrease rapidly as E_S/N_O increases, because occasionally fade durations are too long to be randomized by the deinterleaver. These long fades cause error bursts that cannot be eliminated with only marginal increases in SNR. The error correction capabilities of Links 2, 3 and 4 differ significantly from what was found for benign channel conditions. Here the equivalent SNR difference between Links 2 and 3 is about 0.75 dB and it is about 1.0 dB between Link 3 and 4.

Figures 164 through 168 present the data of Figures 158 through 161 in a format that facilitates direct comparison between the four links.

4.5 CONCLUSIONS

The major conclusions of this study pertain to the relative merits of the "combine on the fly" interleaving/deinterleaving technique compared with normal interleaving and deinterleaving. Here Link 4 is considered the baseline coding scheme with which Links 2 and 3 are to be judged. Link 1 is too weak to be of interest and was included in this study only to exhaust the range of inner and outer code rates that produce an overall rate of 1/8.

Relative to Link 4, Links 2 and 3 do provide a significant reduction in digital processing load, but provide only modest savings in storage. The estimates of link complexity were previously given by Equations 9, 12, 16, 22 and 23 in general and Table 9 and Figure 19 for the links studied here. The reductions in complexity have associated penalties in performance. For fading conditions, the performance of Links 2 and 3 were found to be about 1.75 dB and 1.0 dB lower than that of Link 4 in terms of equivalent SNR. Under benign conditions, Links 2 and 3 suffered only about 0.5 dB and 0.25 dB of degradation, respectively.

The applicability of the schemes studied here to a particular communication link can be evaluated in terms of the marginal costs of digital processing, memory and SNR (i.e., transmittter power, antenna size, receiver sensitivity, etc.). The use of chip combining to simplify the coding and interleaving functions is considered attractive if the associated savings in complexity exceed the cost of the required increase in SNR. Since limitations on space-based transmitter power levels and antenna size are usually severe, it is expected that the chip combining approach to SDI concatenation will generally be unattractive for satellite links which must operate under fading conditions. However, for links that are not required to maintain good performance when the propagation medium is disturbed, this approach may be viable.

The effects of quantization of the demodulator outputs were given particular attention in the investigation. It was found that 3.0 is a good choice for normalized quantizer dynamic range for both fading and benign conditions when the quantizer decision boundaries are uniformly spaced. However, the demodulator output histograms peak in the region of minimum symbol reliability, which suggests that significant performance gain may be attained by using nonuniformly spaced decision boundaries. We found the histograms to be somewhat invariant over the range of channel conditions that was studied, and hence an adaptation algorithm to match the decision boundaries to dynamic channel statistics does not appear necessary.

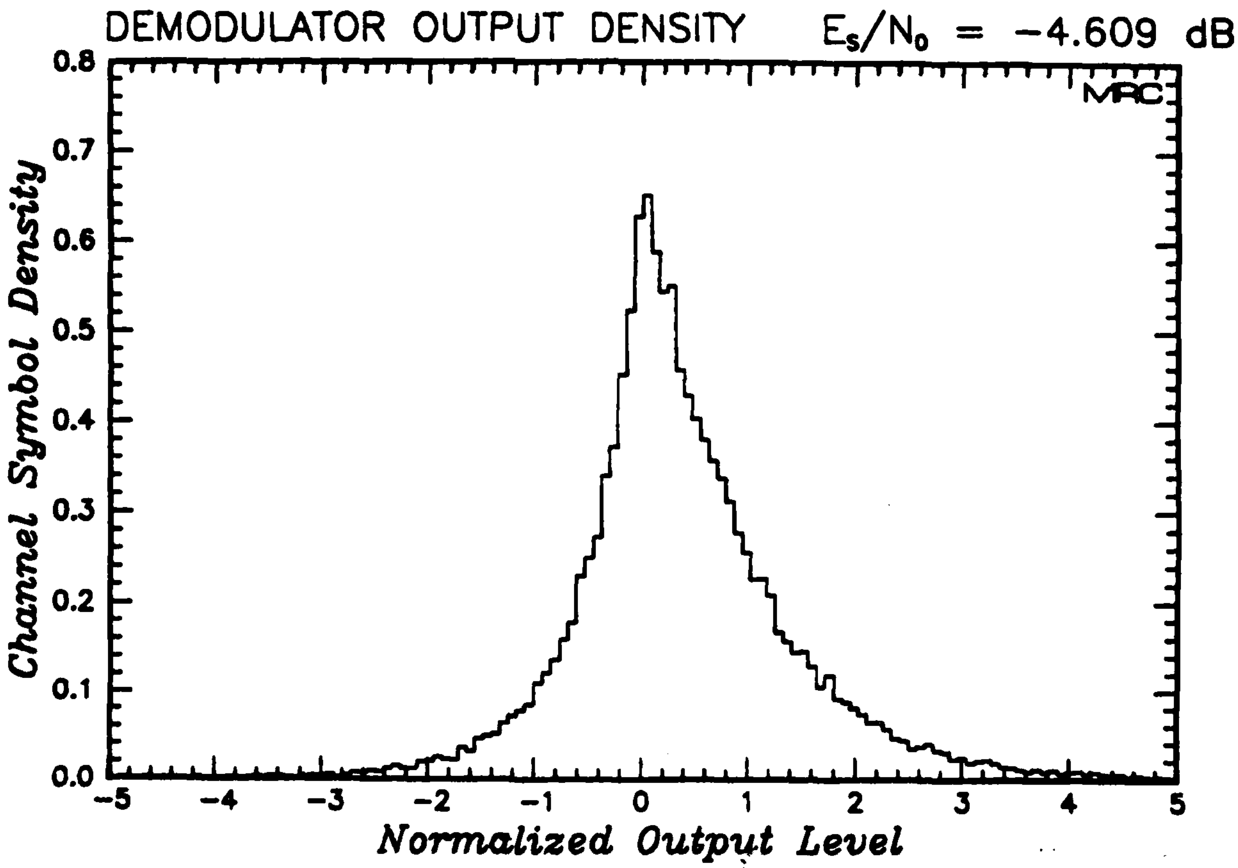


Figure 23. Histogram of demodulator outputs under benign channel conditions for E_S/N_O = -4.609 dB.

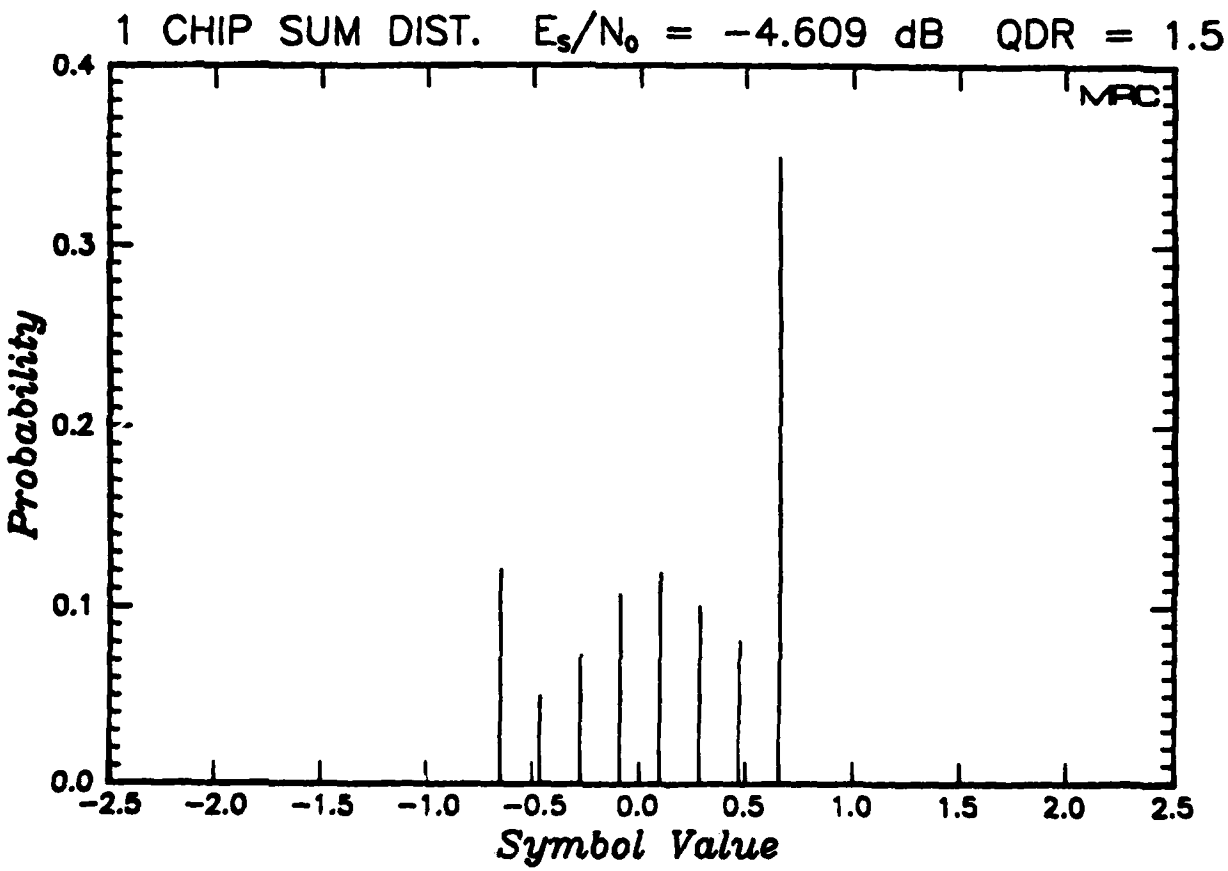


Figure 24. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_0 = -4.609 and normalized QDR of 1.5. (Applicable to Link 4)

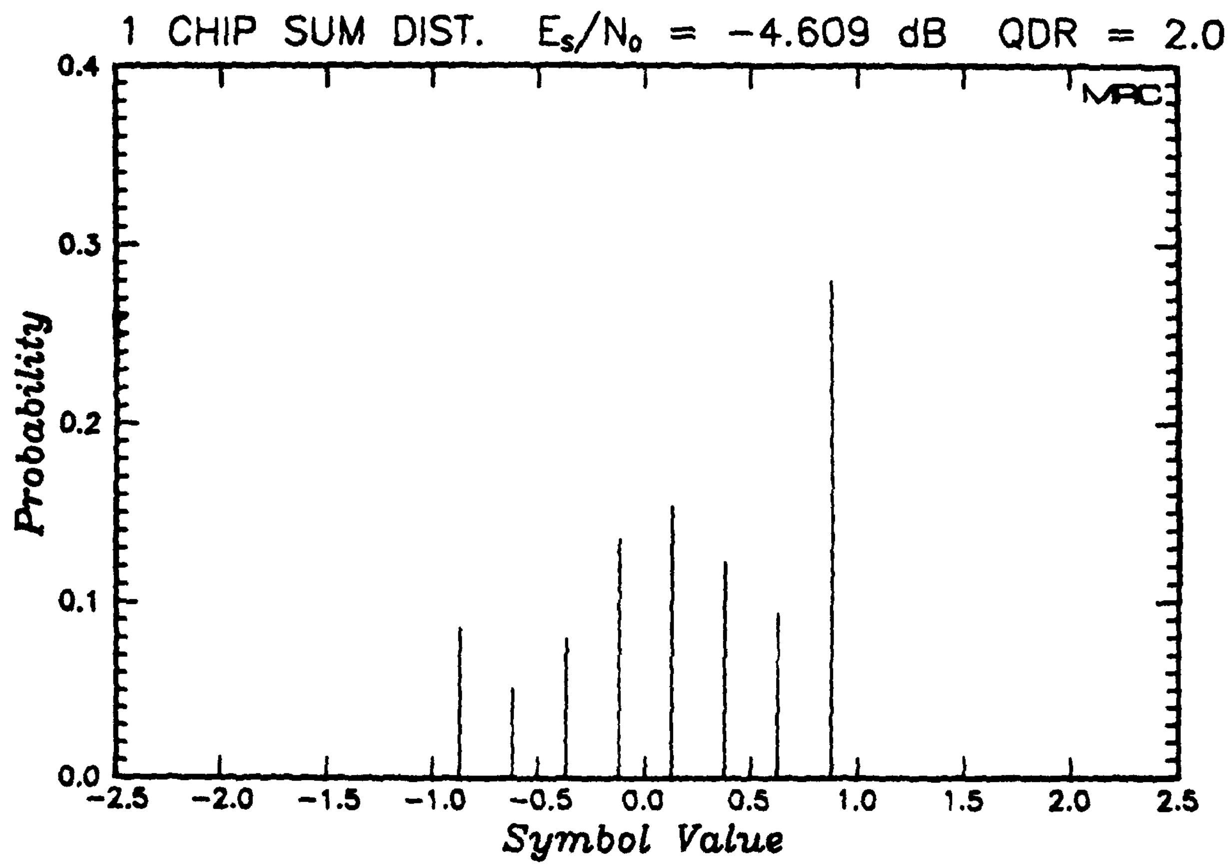


Figure 25. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -4.609 and normalized QDR of 2.0. (Applicable to Link 4)

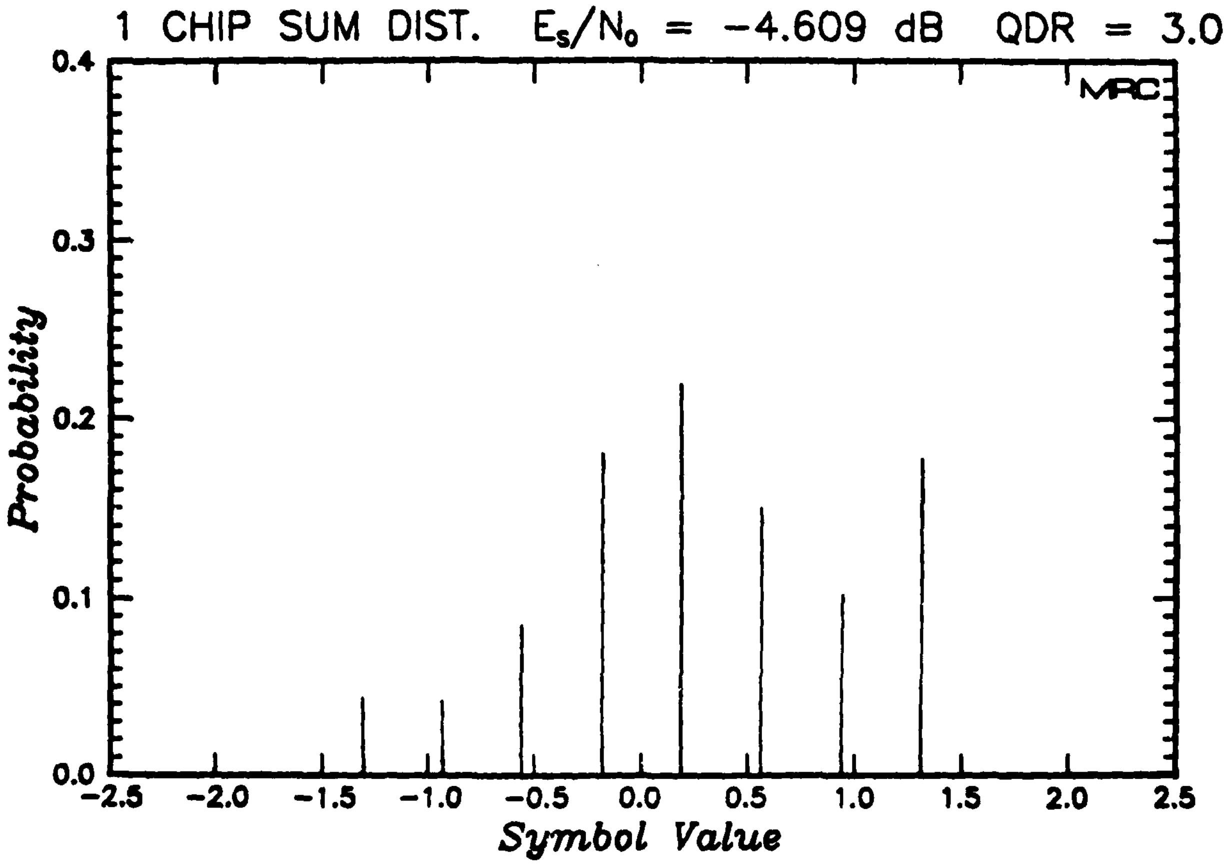


Figure 26. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 3.0. (Applicable to Link 4)

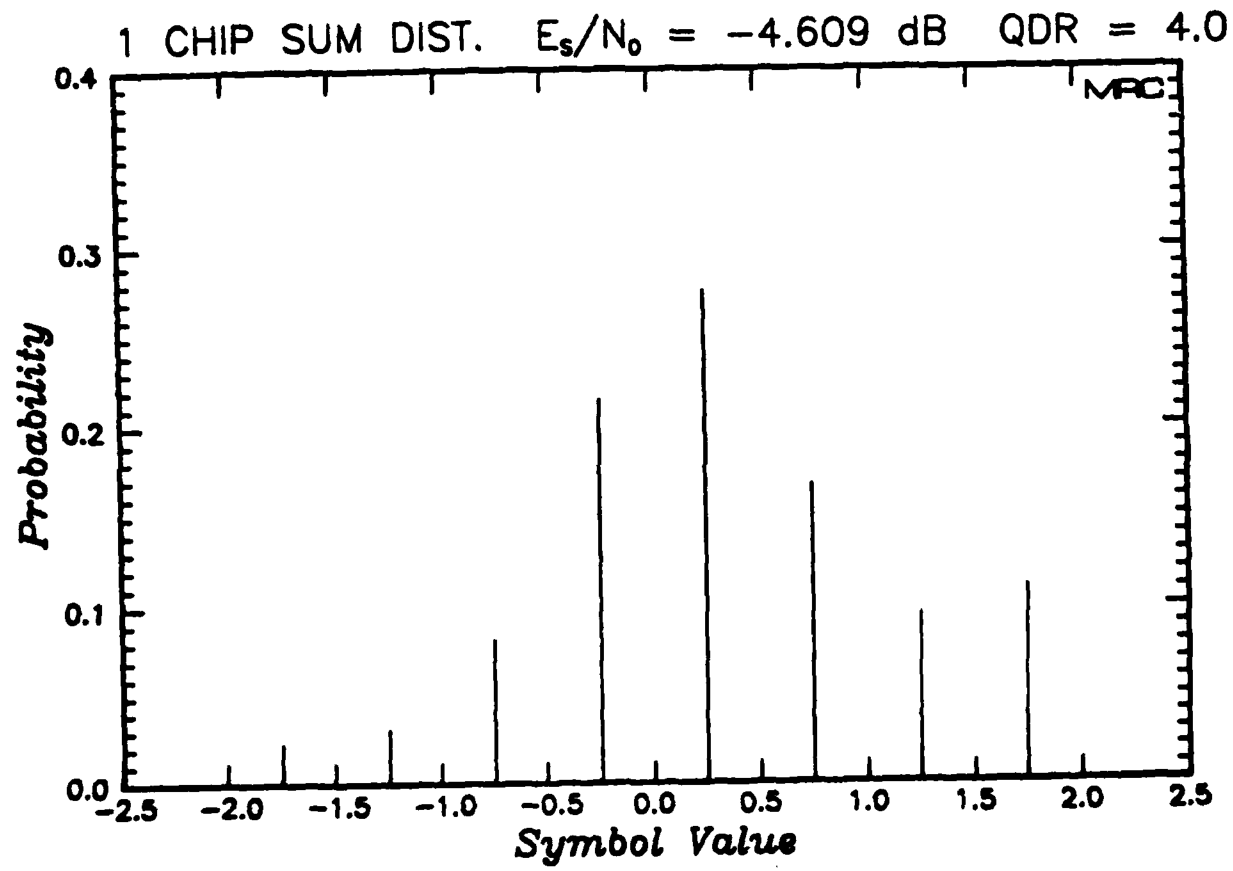


Figure 27. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -4.609 and normalized QDR of 4.0. (Applicable to Link 4)

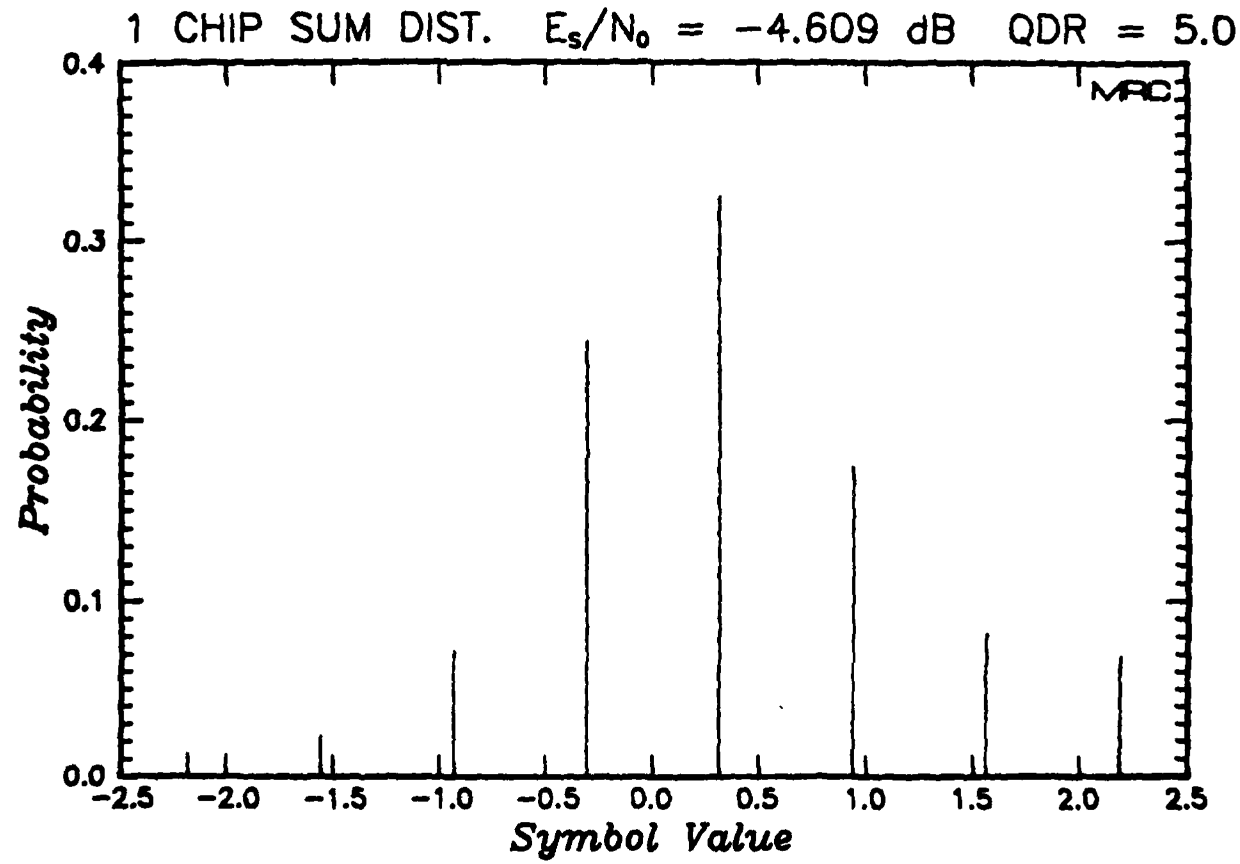


Figure 28. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -4.609 and normalized QDR of 5.0. (Applicable to Link 4)

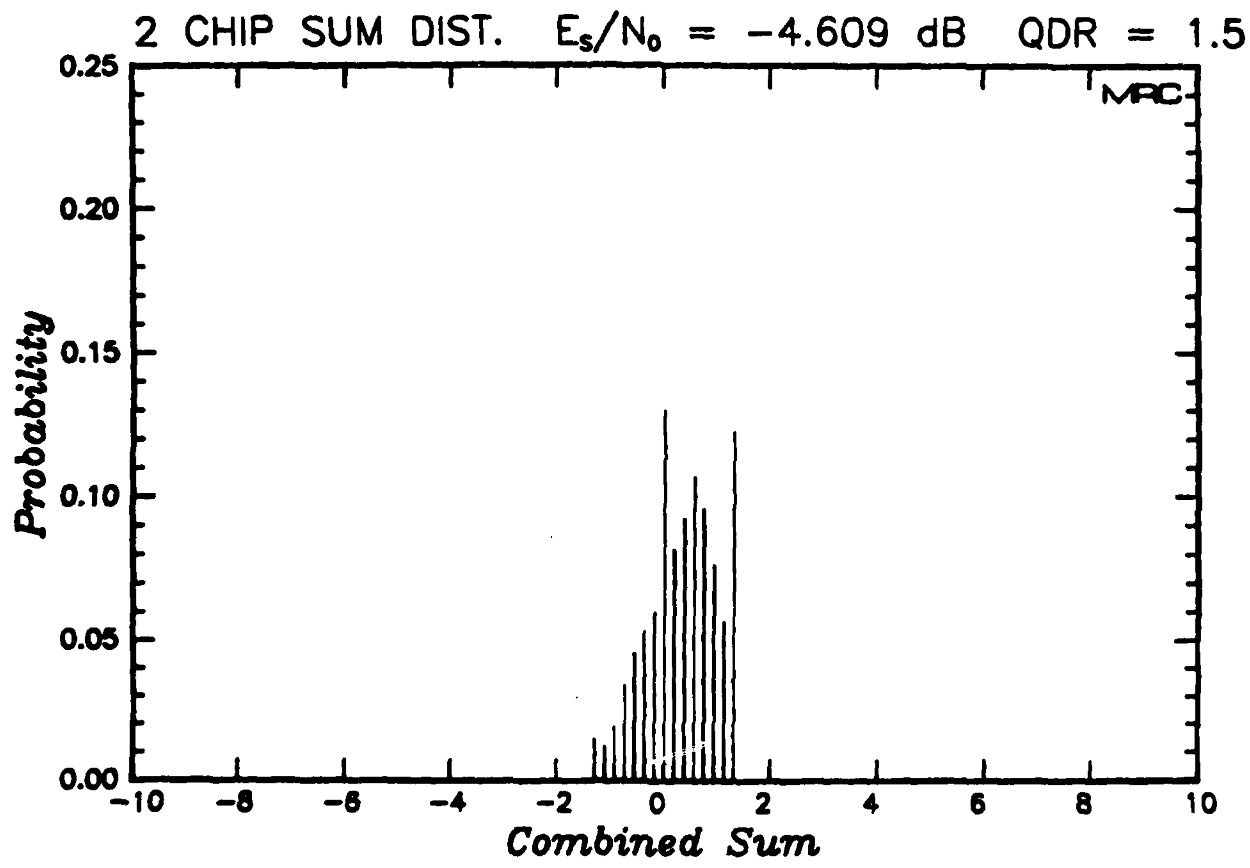


Figure 29. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 1.5. (Applicable to Link 3)

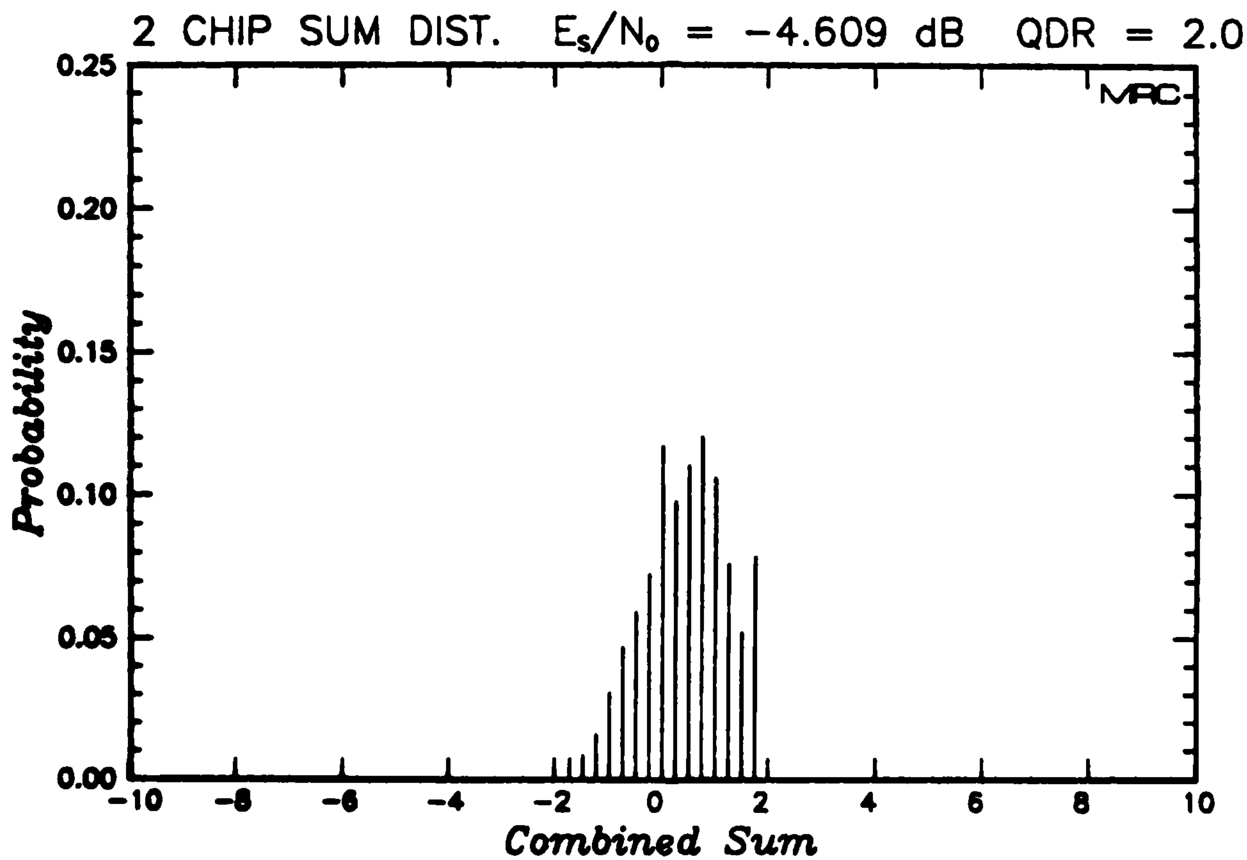


Figure 30. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 2.0. (Applicable to Link 3)

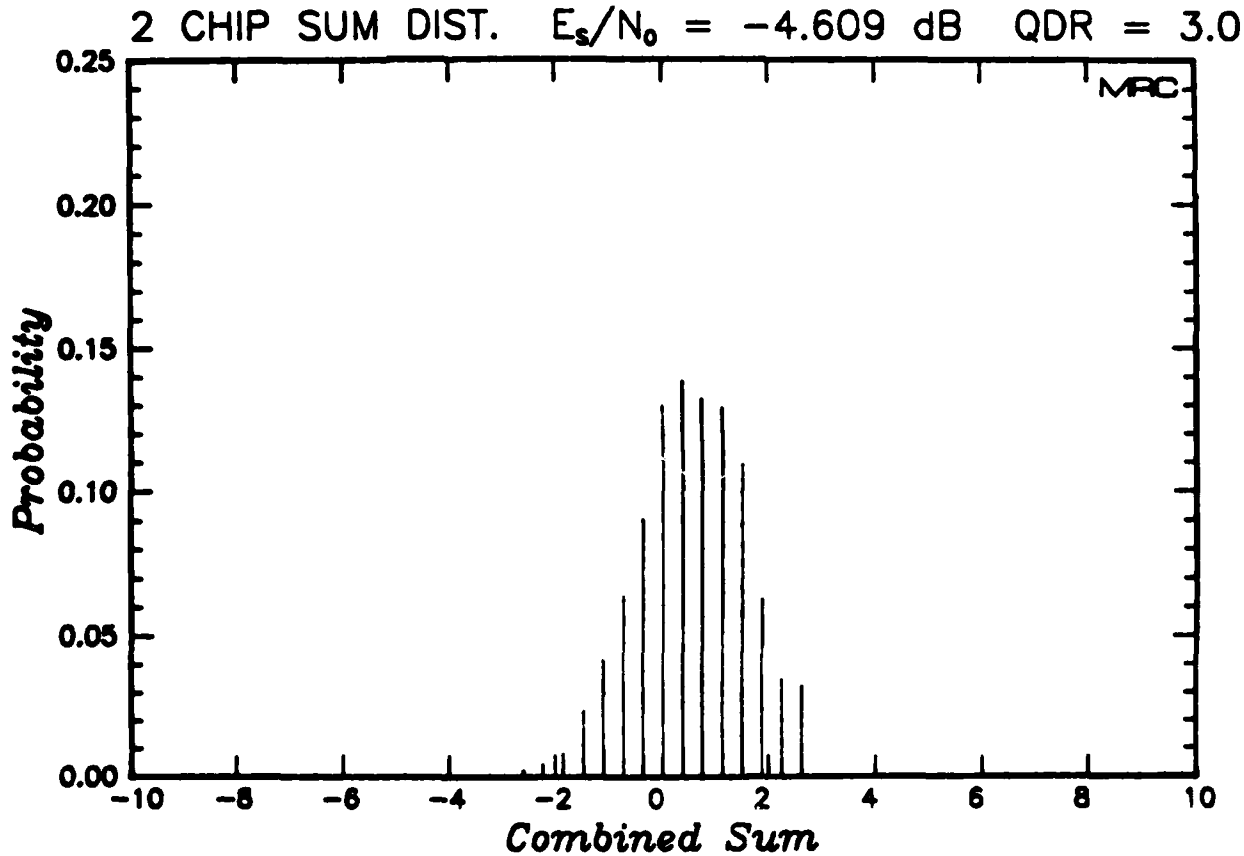


Figure 31. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 3.0. (Applicable to Link 3)

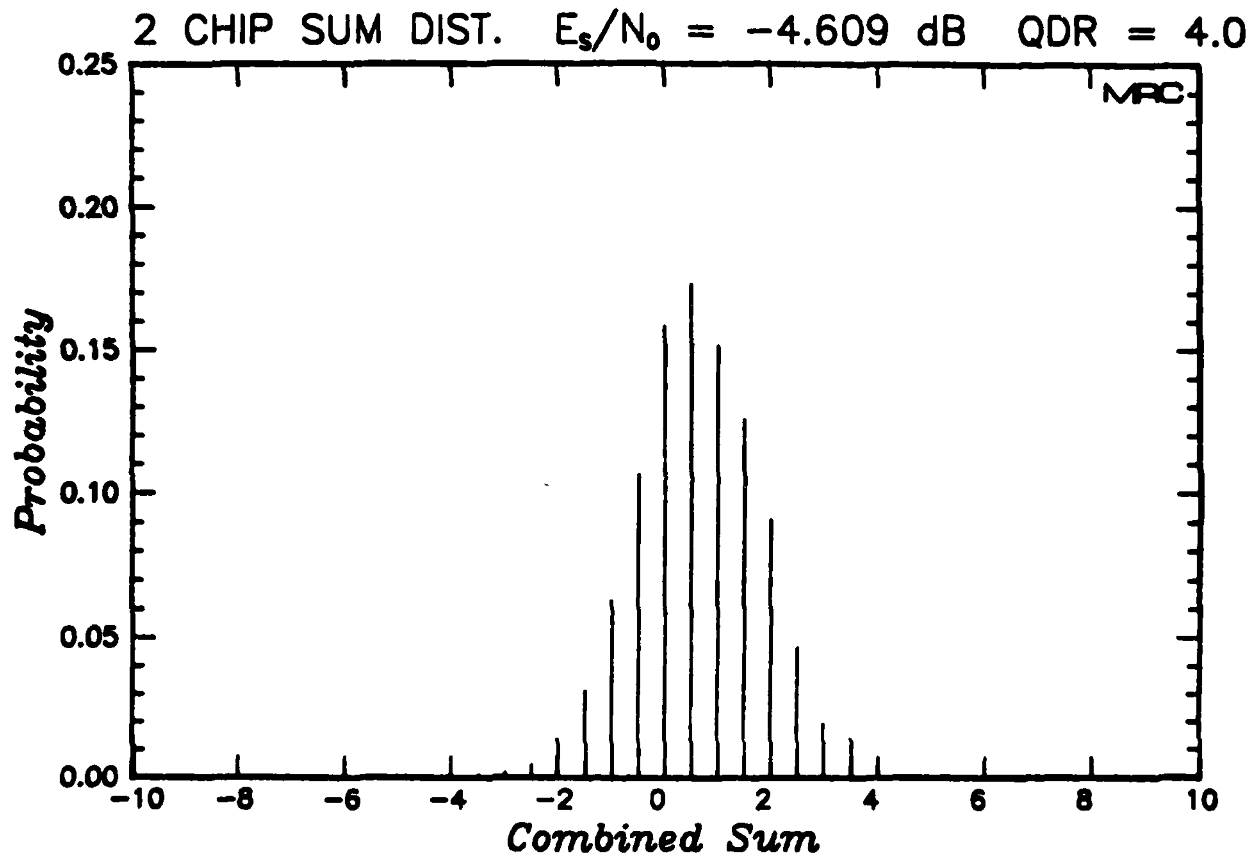


Figure 32. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_s/N_o = -4.609 and normalized QDR of 4.0. (Applicable to Link 3)

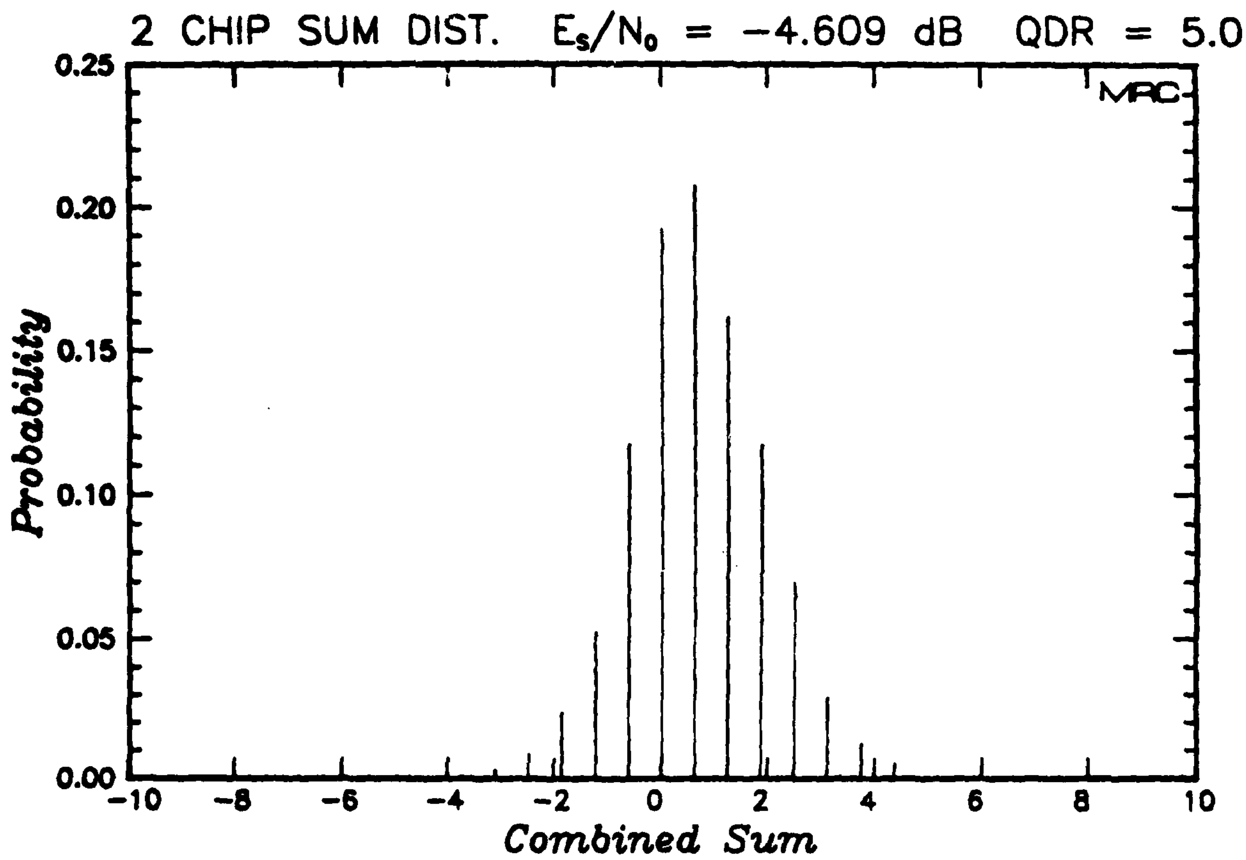


Figure 33. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 5.0. (Applicable to Link 3)

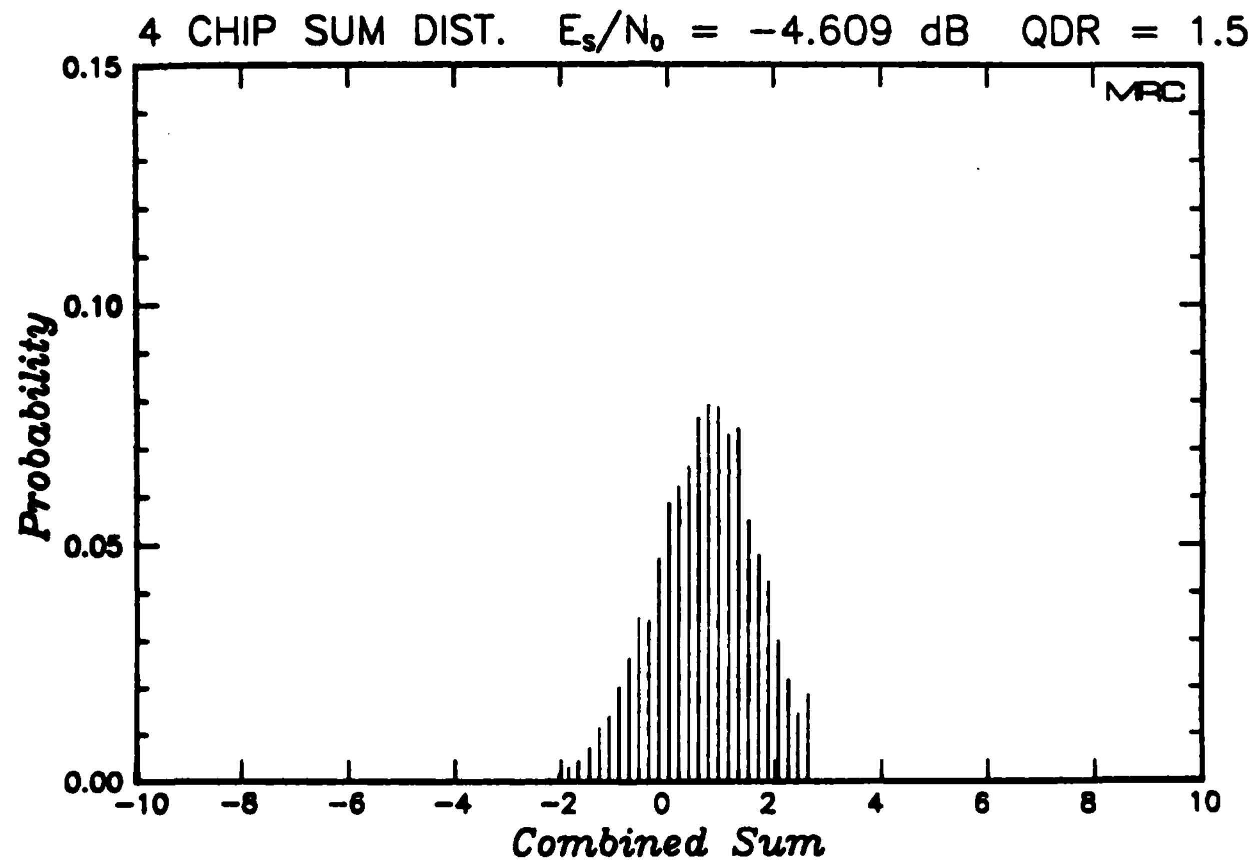


Figure 34. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 1.5. (Applicable to Link 2)

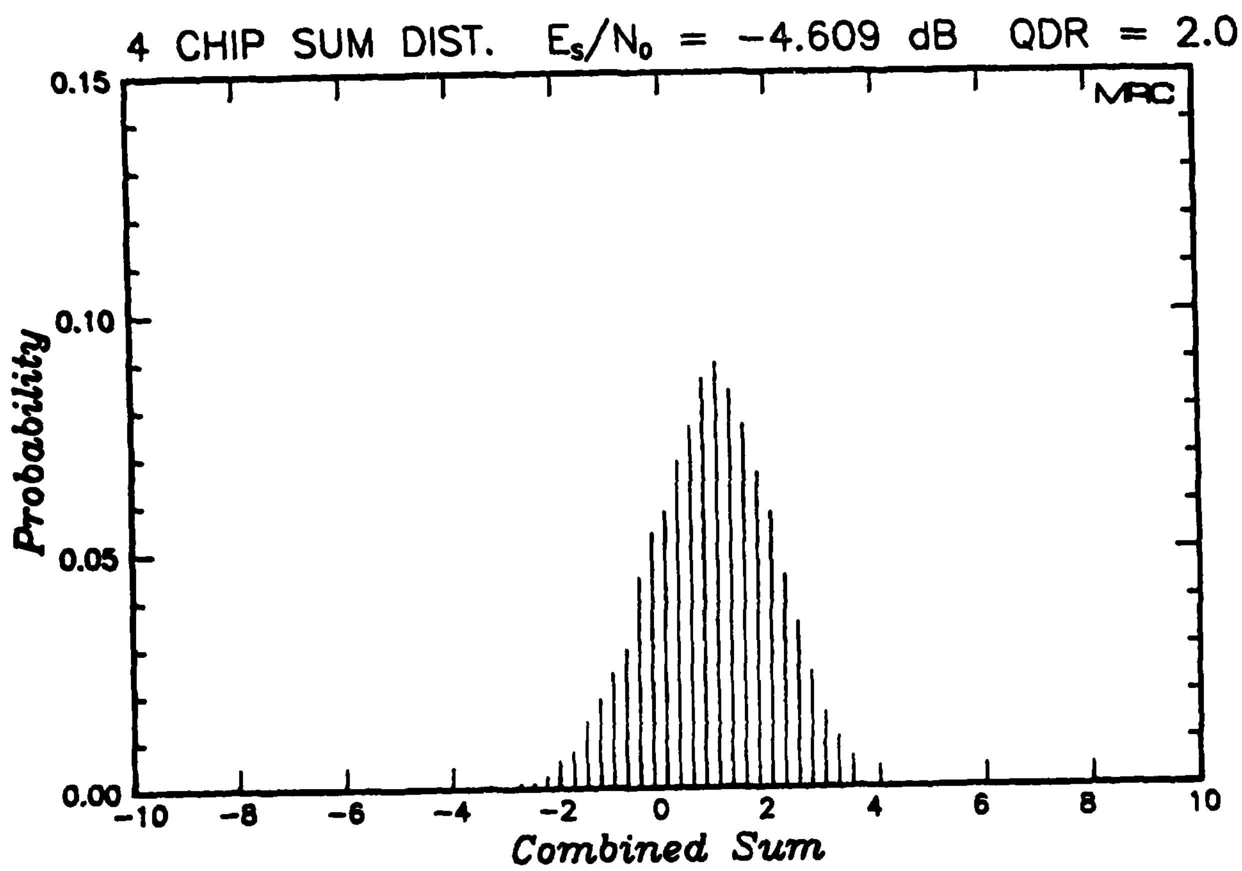


Figure 35. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 2.0. (Applicable to Link 2)

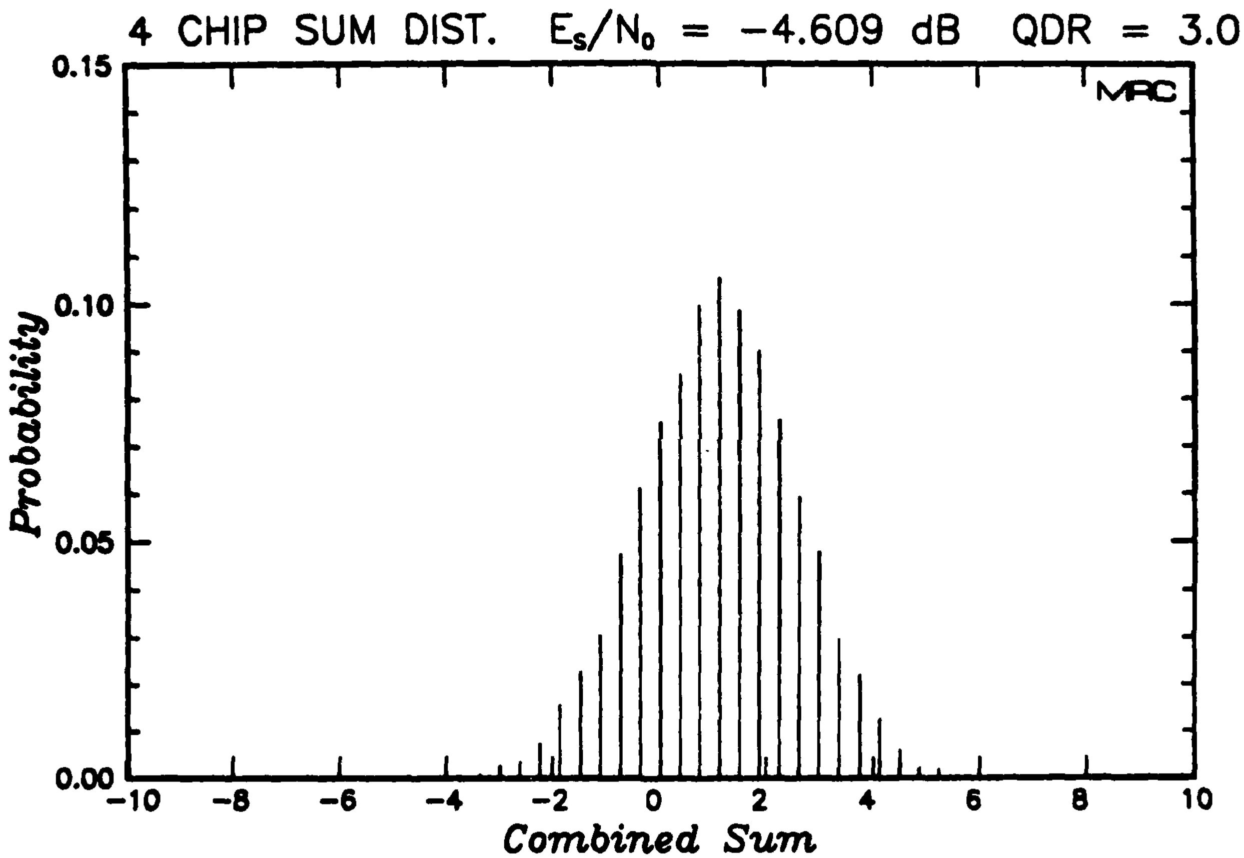


Figure 36. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 3.0. (Applicable to Link 2)

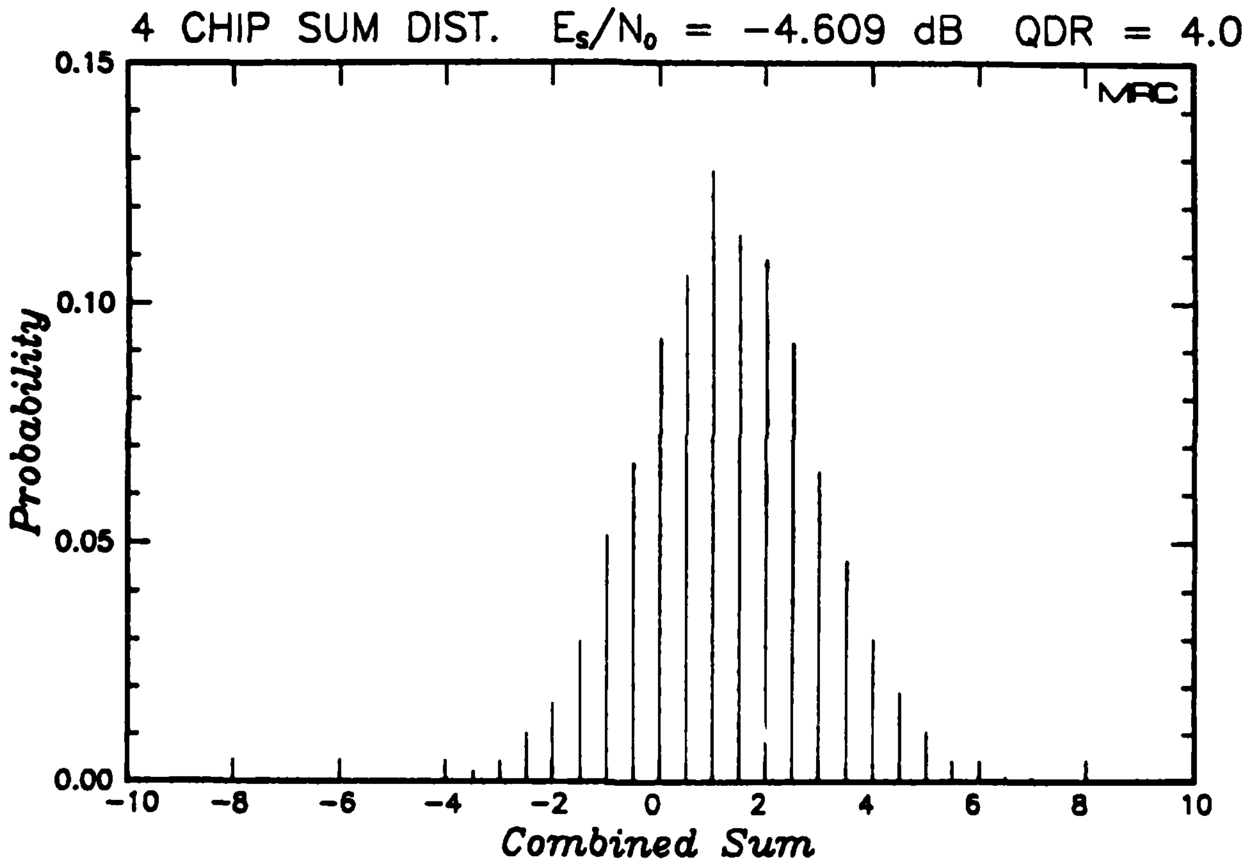


Figure 37. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 4.0. (Applicable to Link 2)

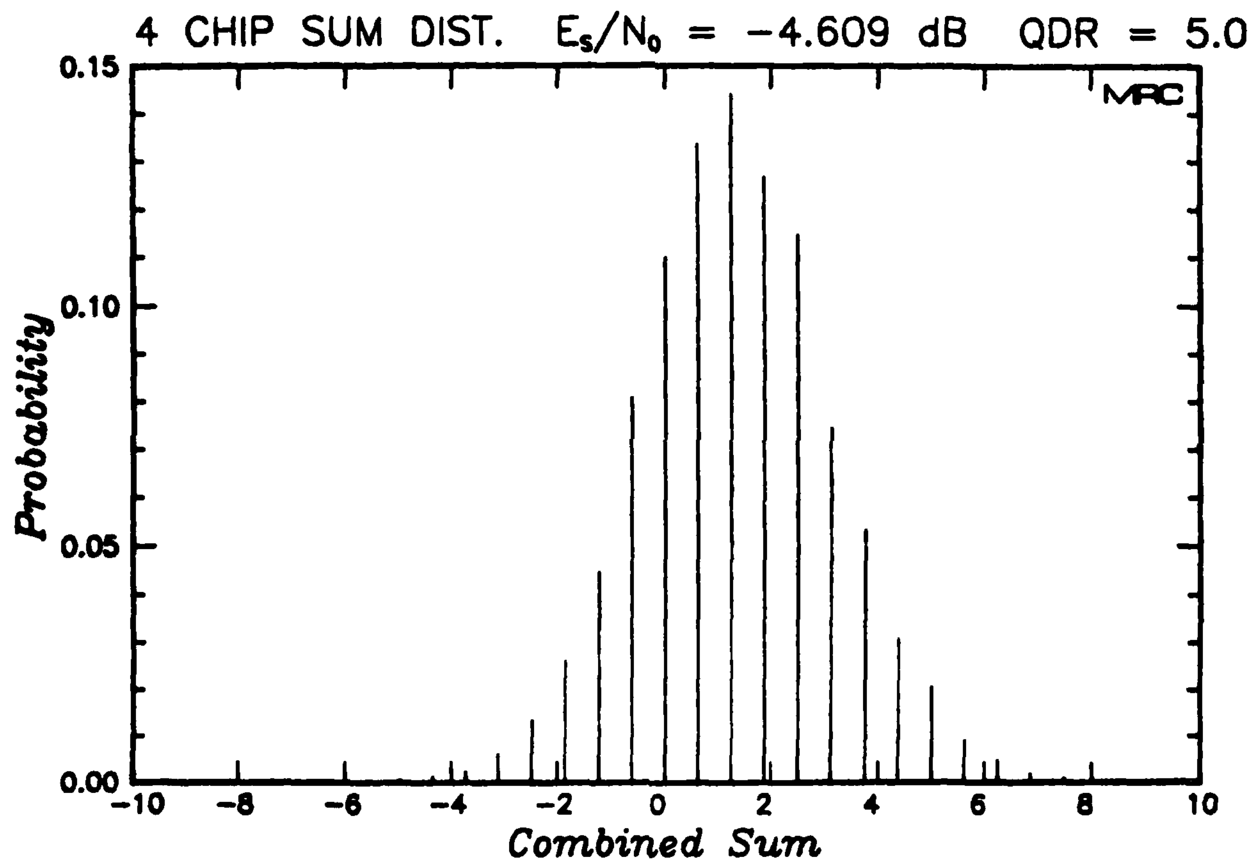


Figure 38. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 5.0. (Applicable to Link 2)

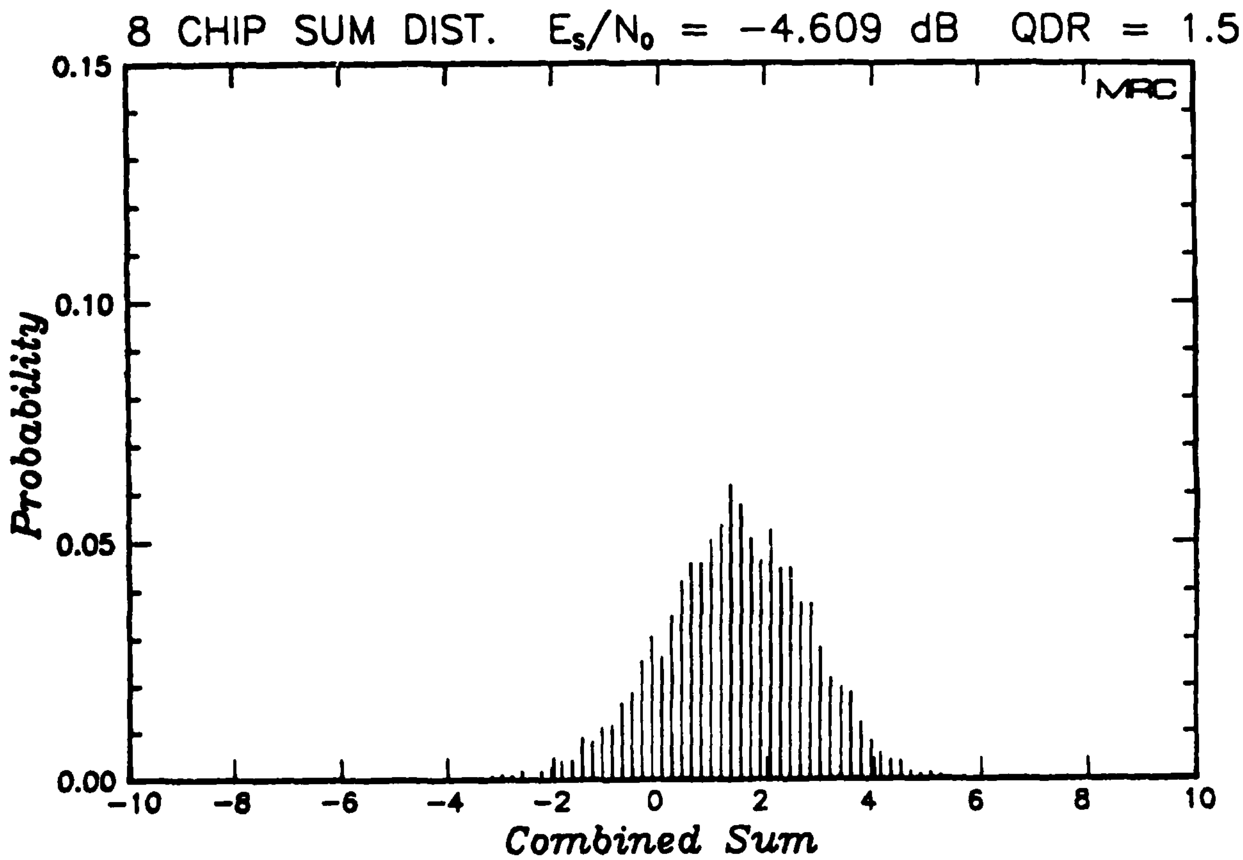


Figure 39. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 1.5. (Applicable to Link 1)

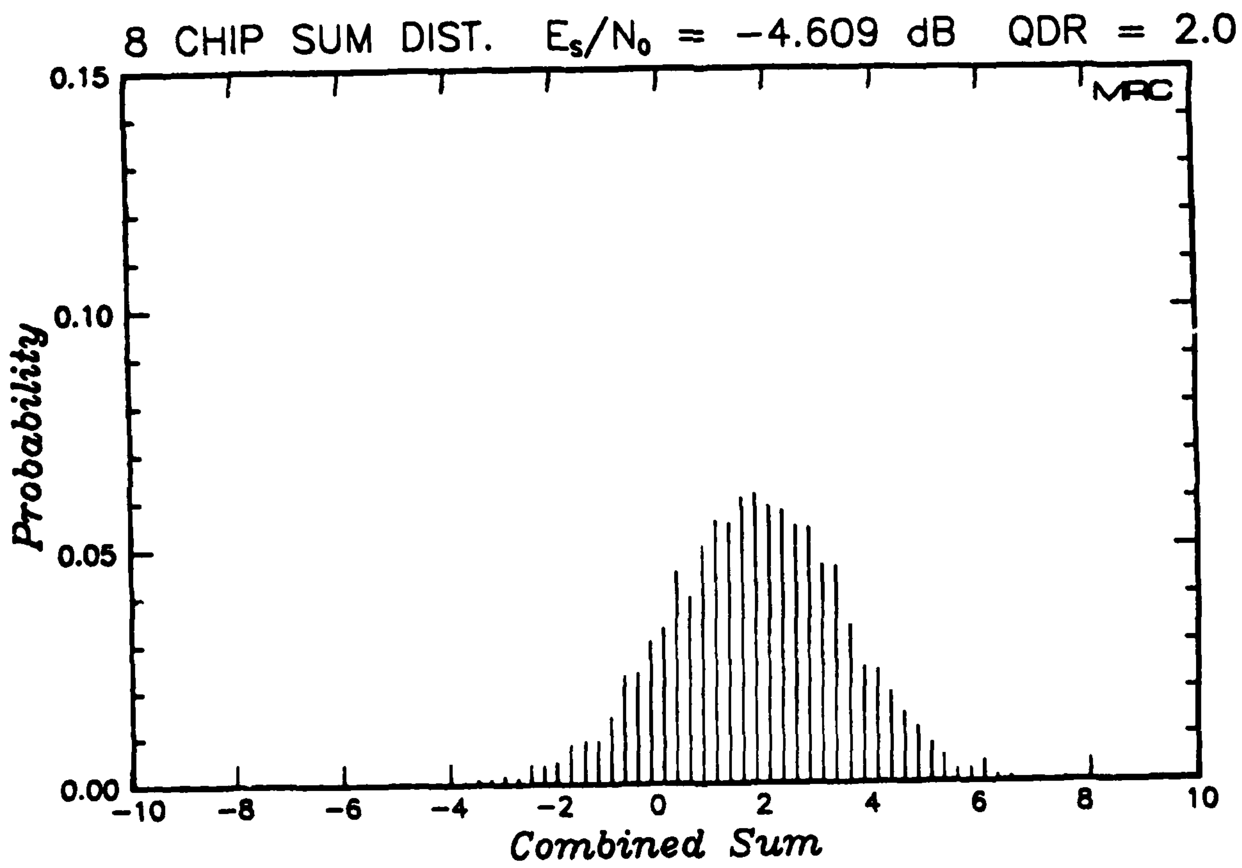


Figure 40. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -4.609 and normalized QDR of 2.0. (Applicable to Link 1)

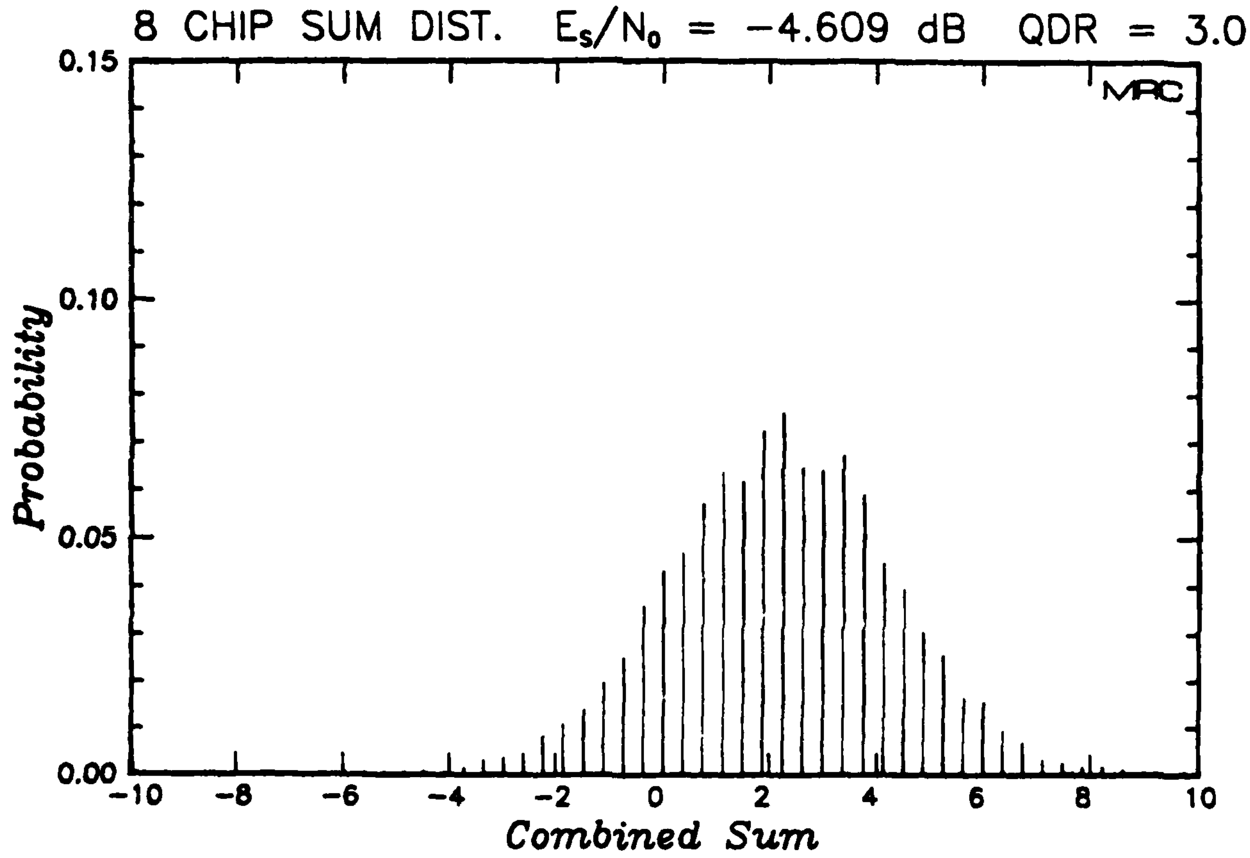


Figure 41. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -4.609 and normalized QDR of 3.0. (Applicable to Link 1)

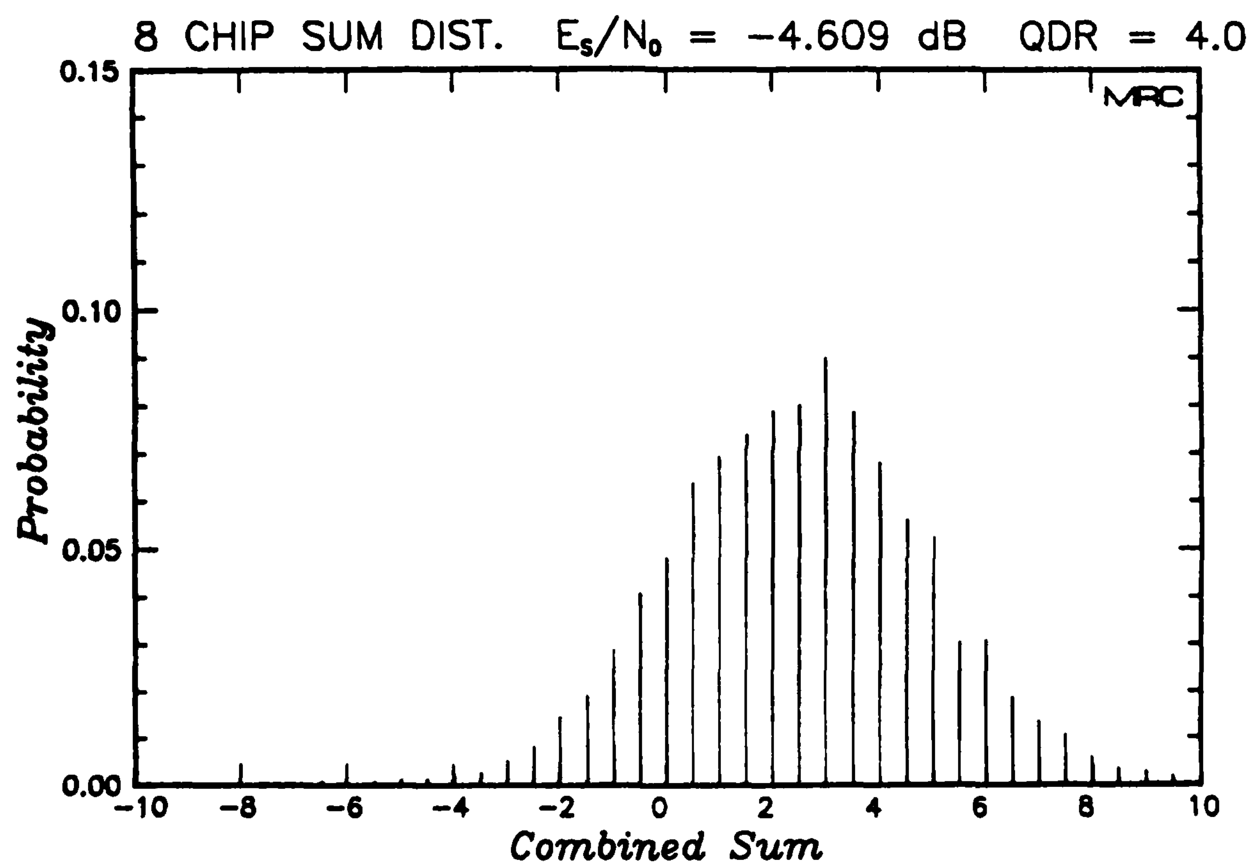


Figure 42. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -4.609 and normalized QDR of 4.0. (Applicable to Link 1)

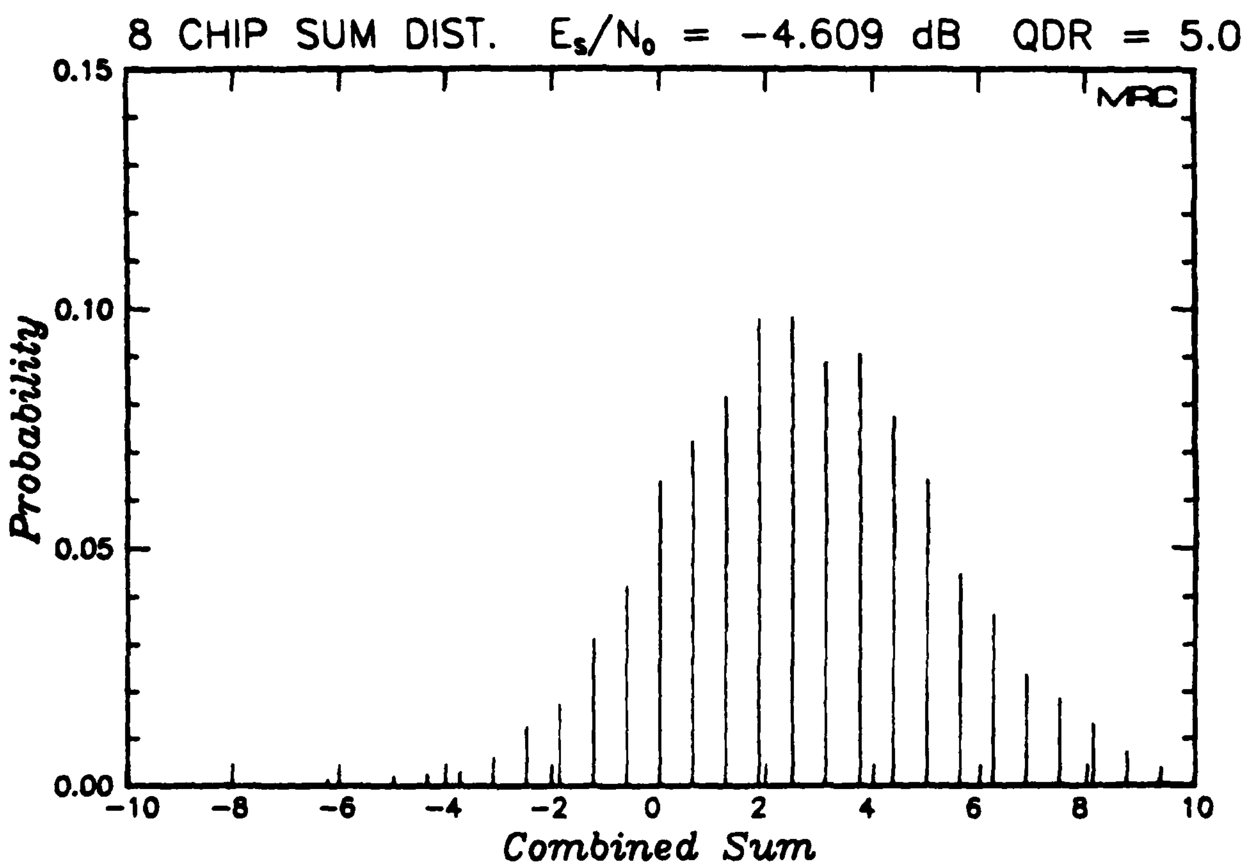


Figure 43. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -4.609 and normalized QDR of 5.0. (Applicable to Link 1)

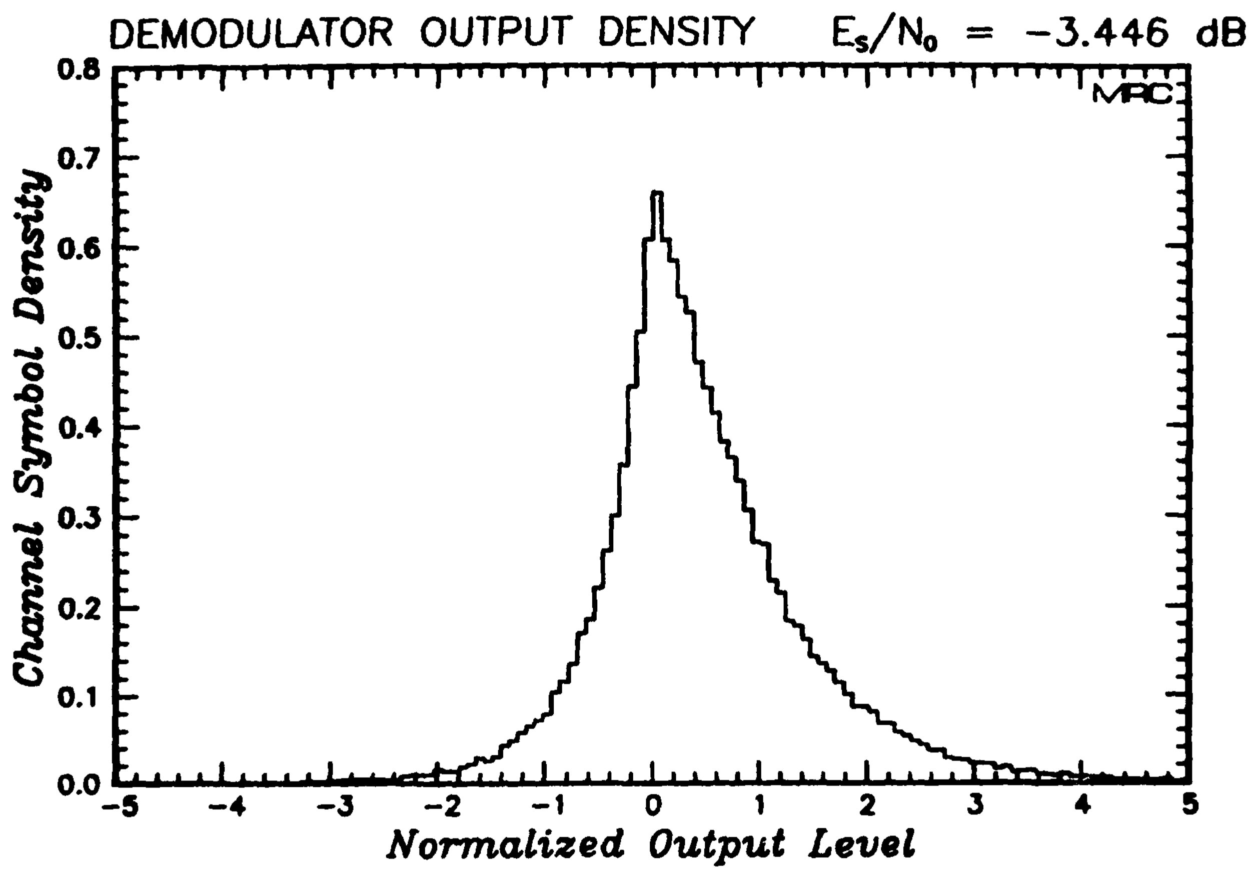


Figure 44. Histogram of demodulator outputs under benign channel conditions for E_s/N_0 = -3.446 dB.

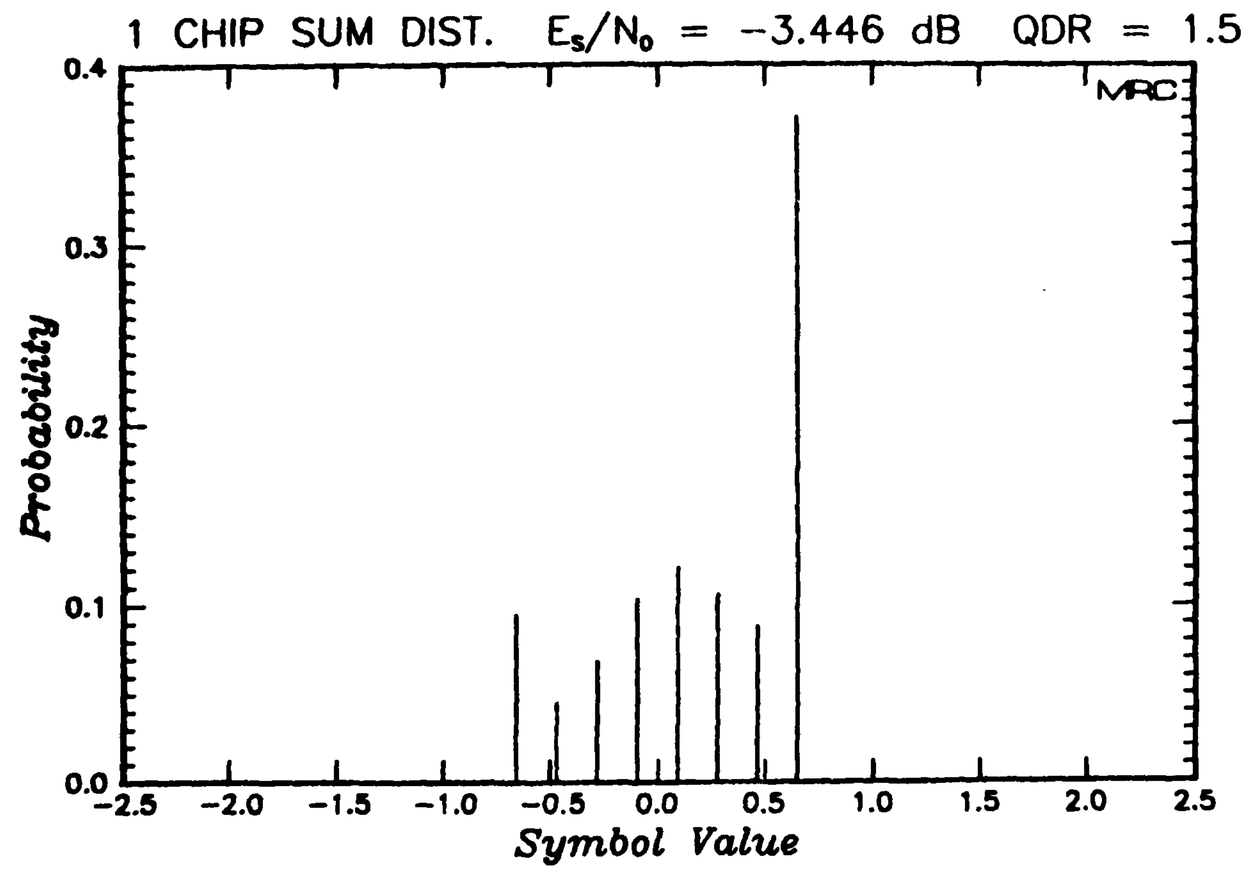


Figure 45. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 1.5. (Applicable to Link 4)

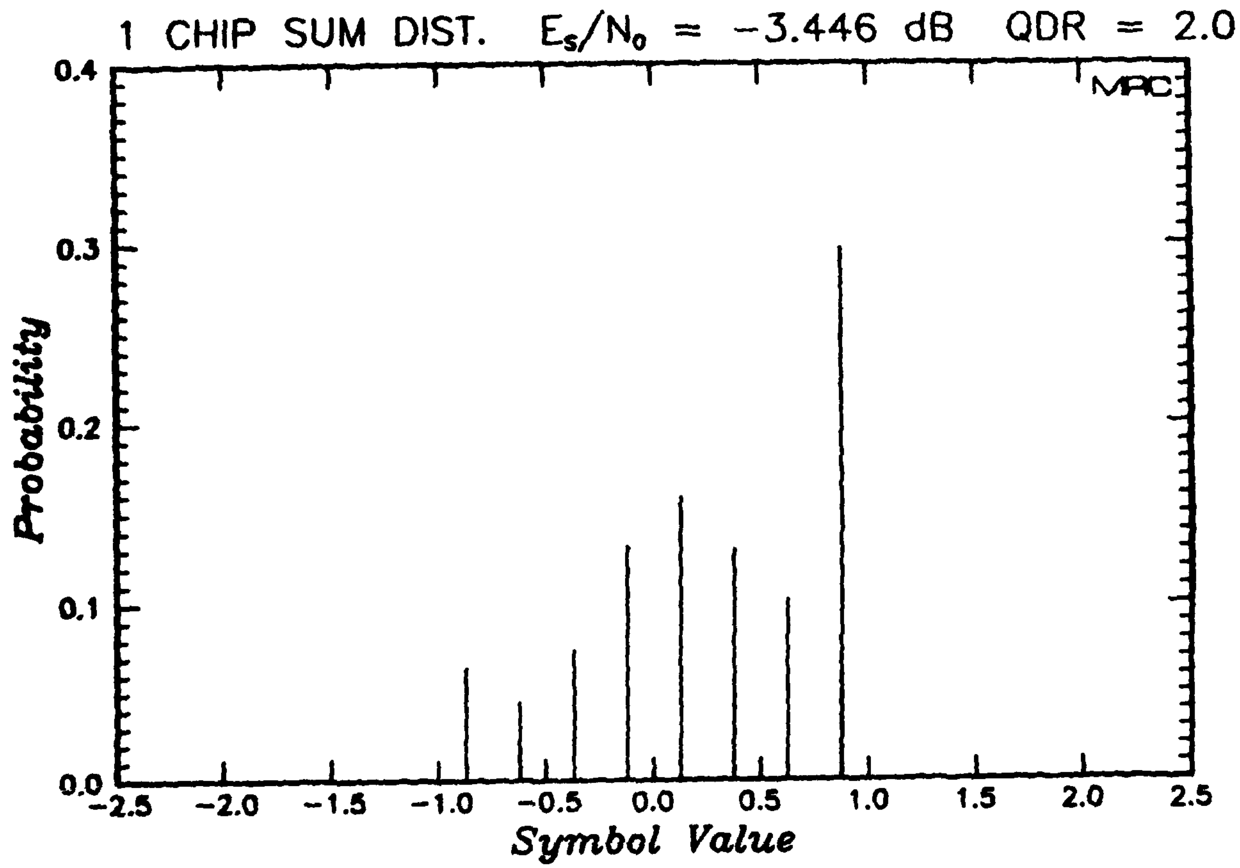


Figure 46. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 2.0. (Applicable to Link 4)

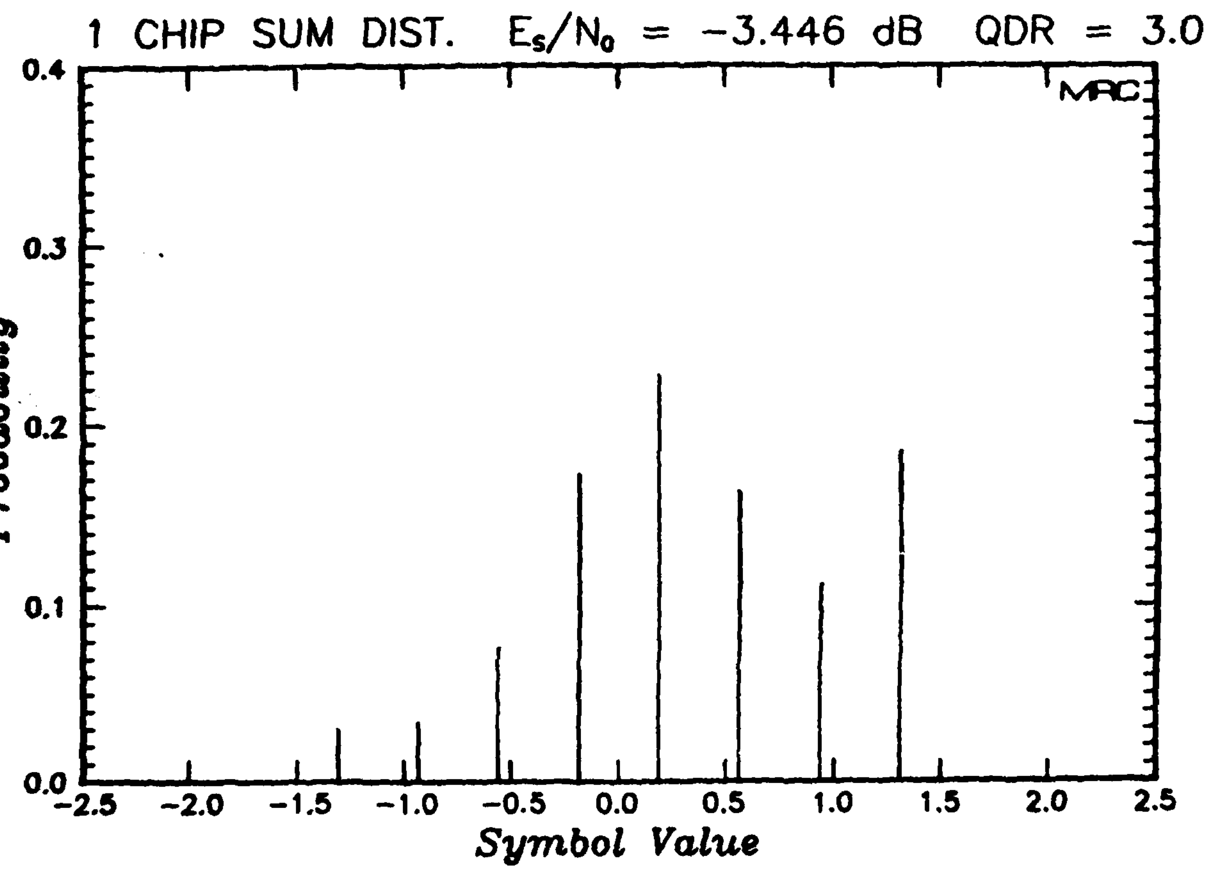


Figure 47. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 3.0. (Applicable to Link 4)

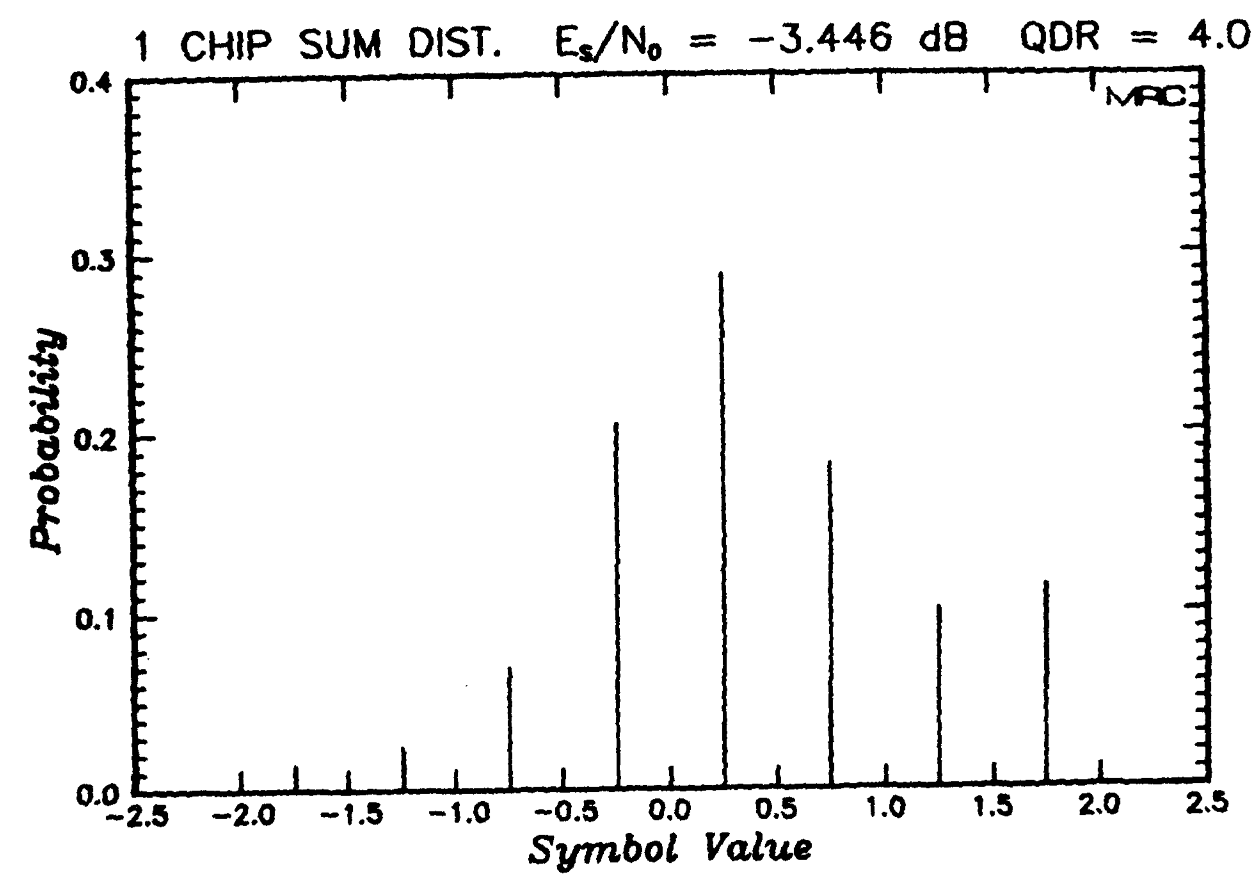


Figure 48. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 4.0. (Applicable to Link 4)

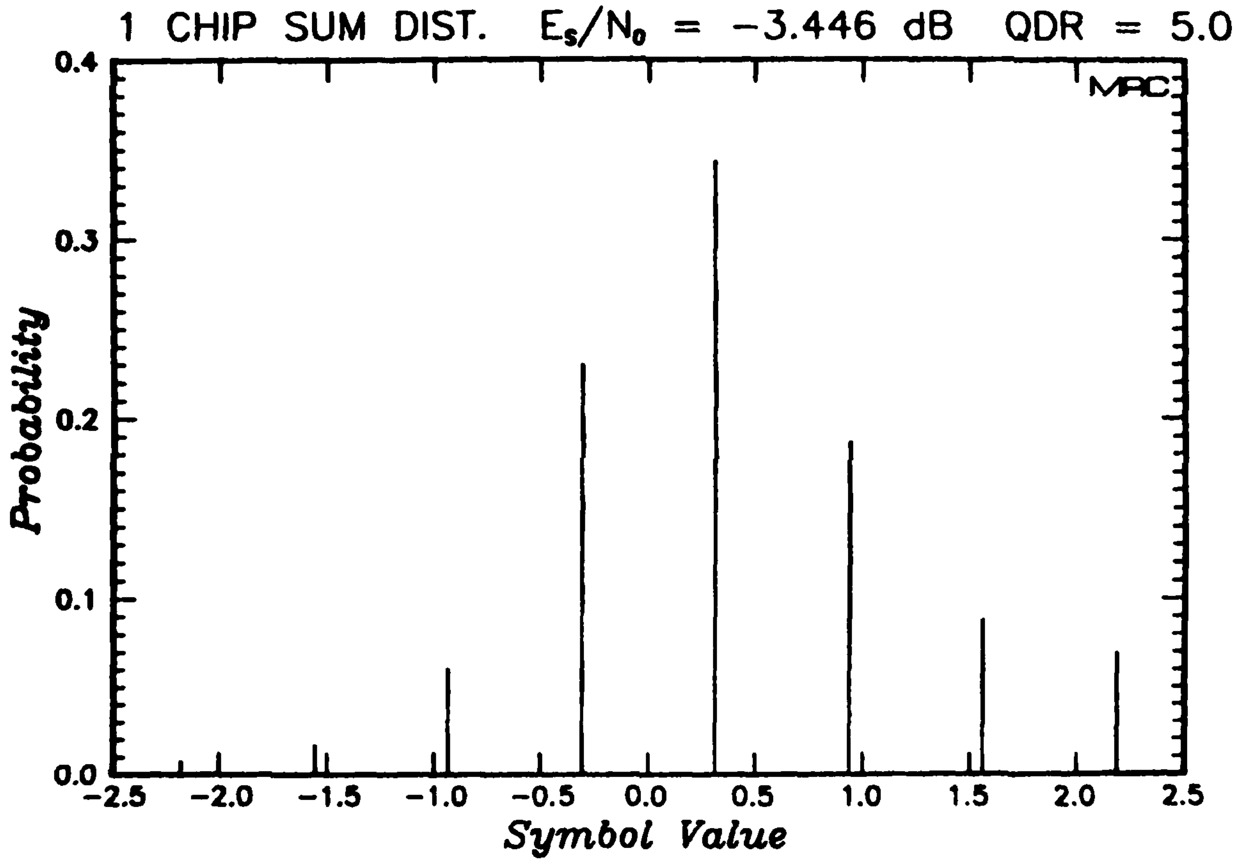


Figure 49. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 5.0. (Applicable to Link 4)

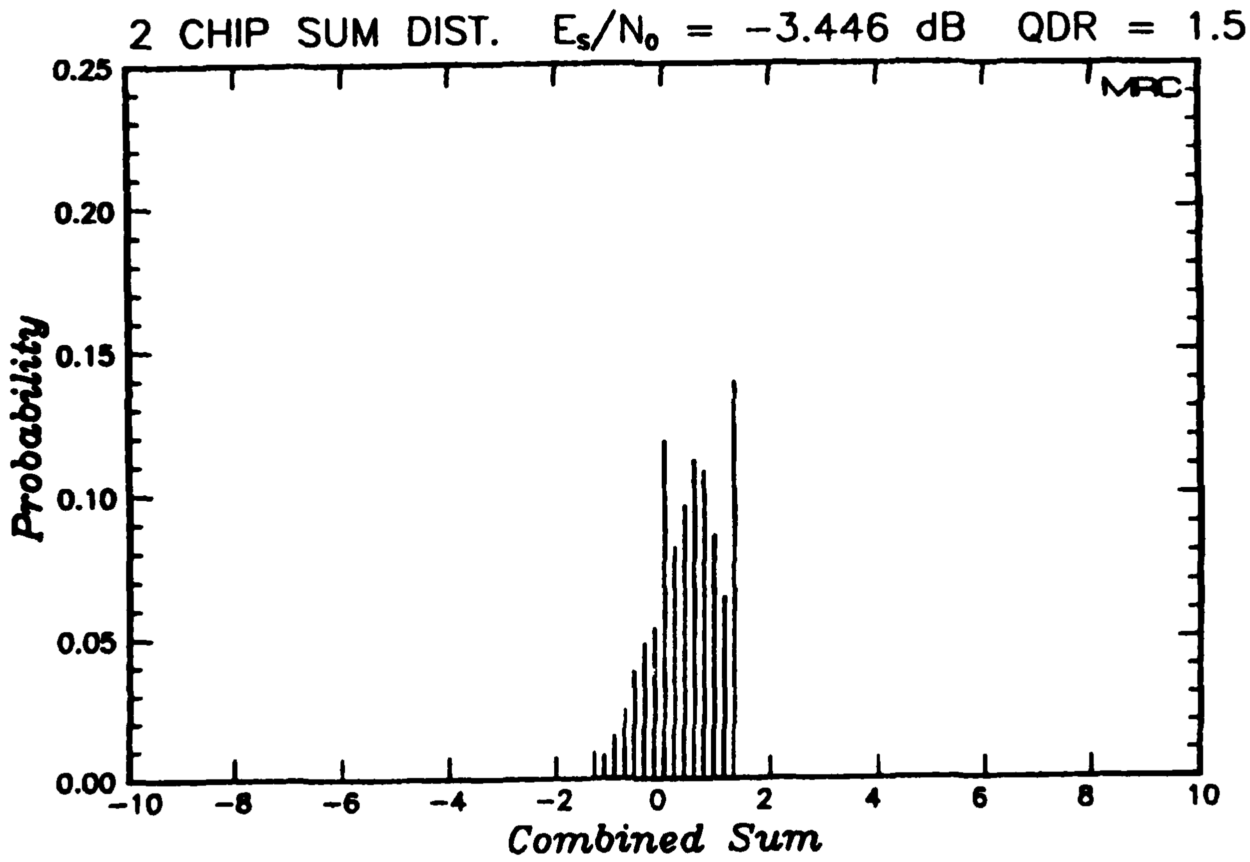


Figure 50. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_s/N_o = -3.446 and normalized QDR of 1.5. (Applicable to Link 3)

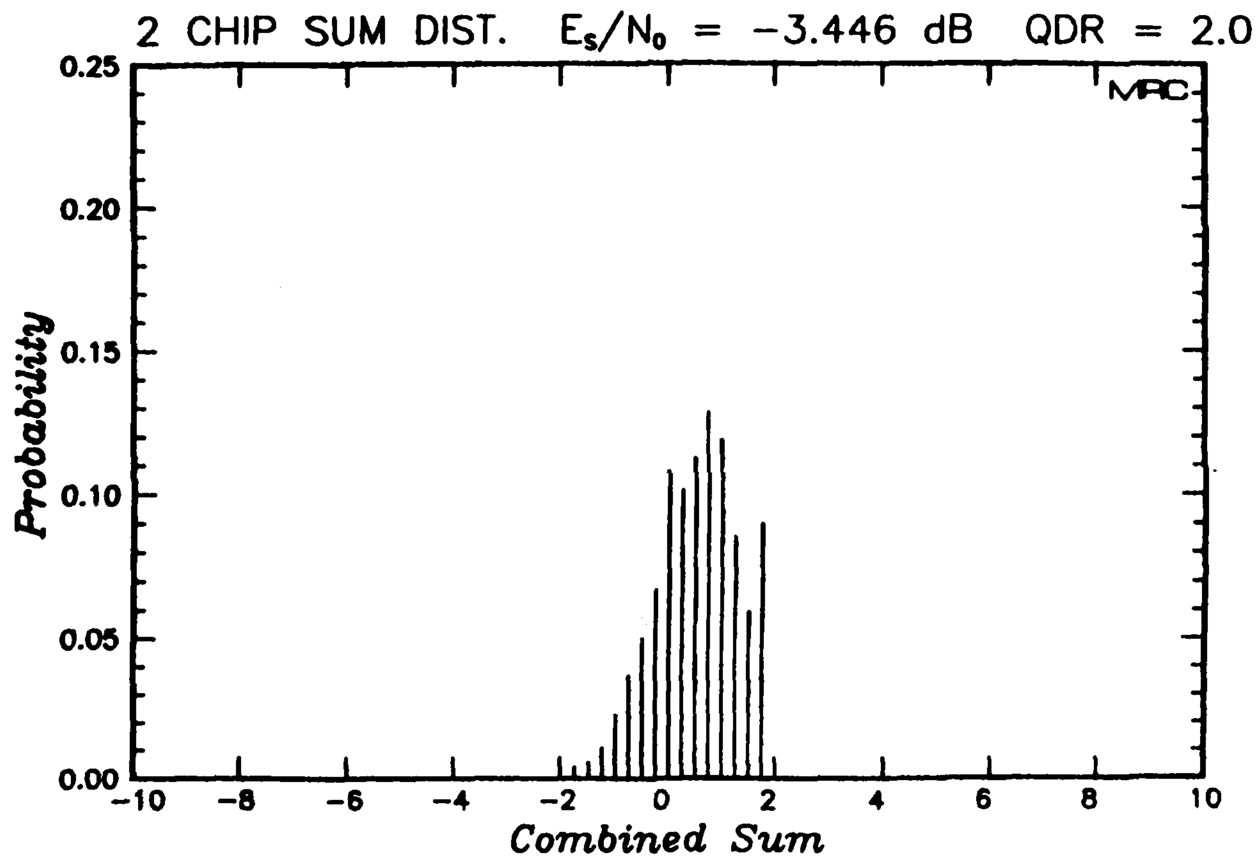


Figure 51. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 2.0. (Applicable to Link 3)

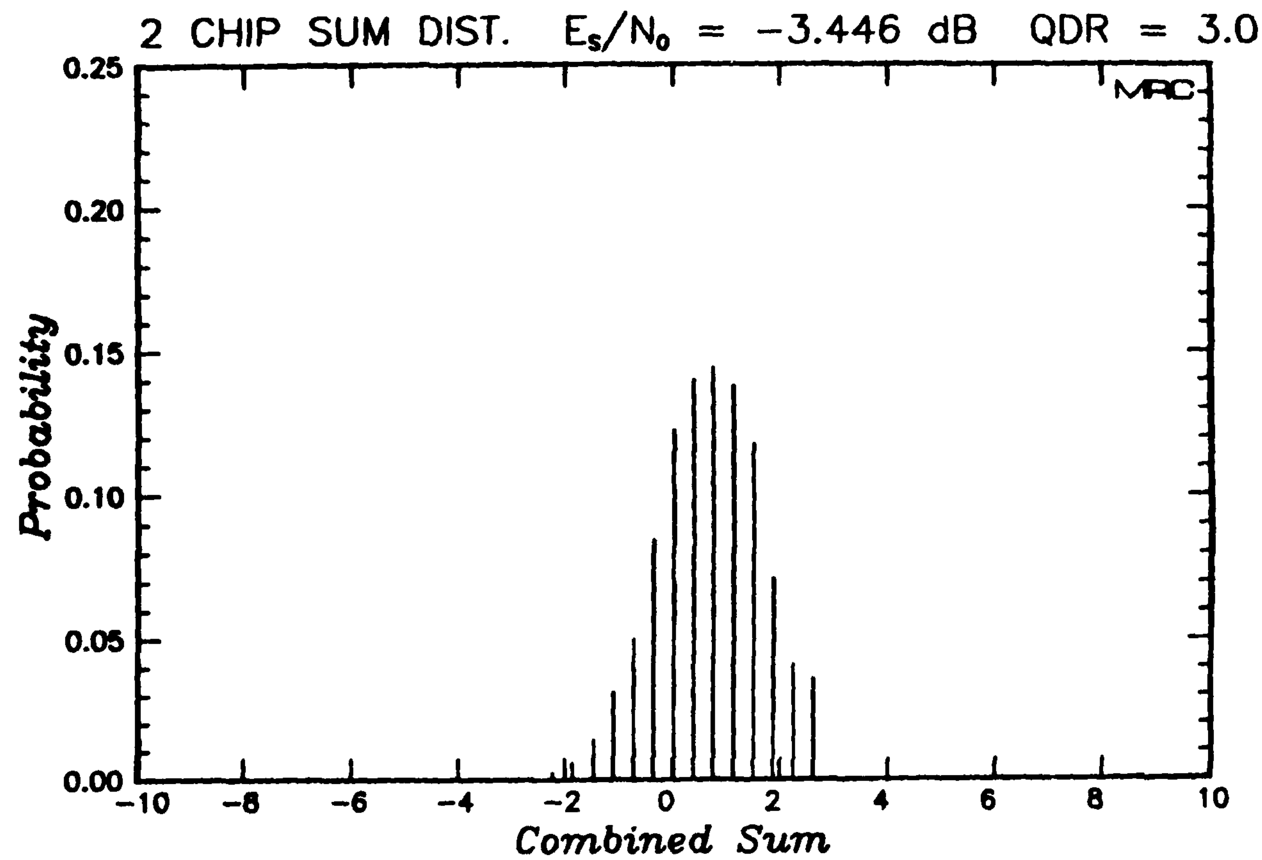


Figure 52. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 3.0. (Applicable to Link 3)

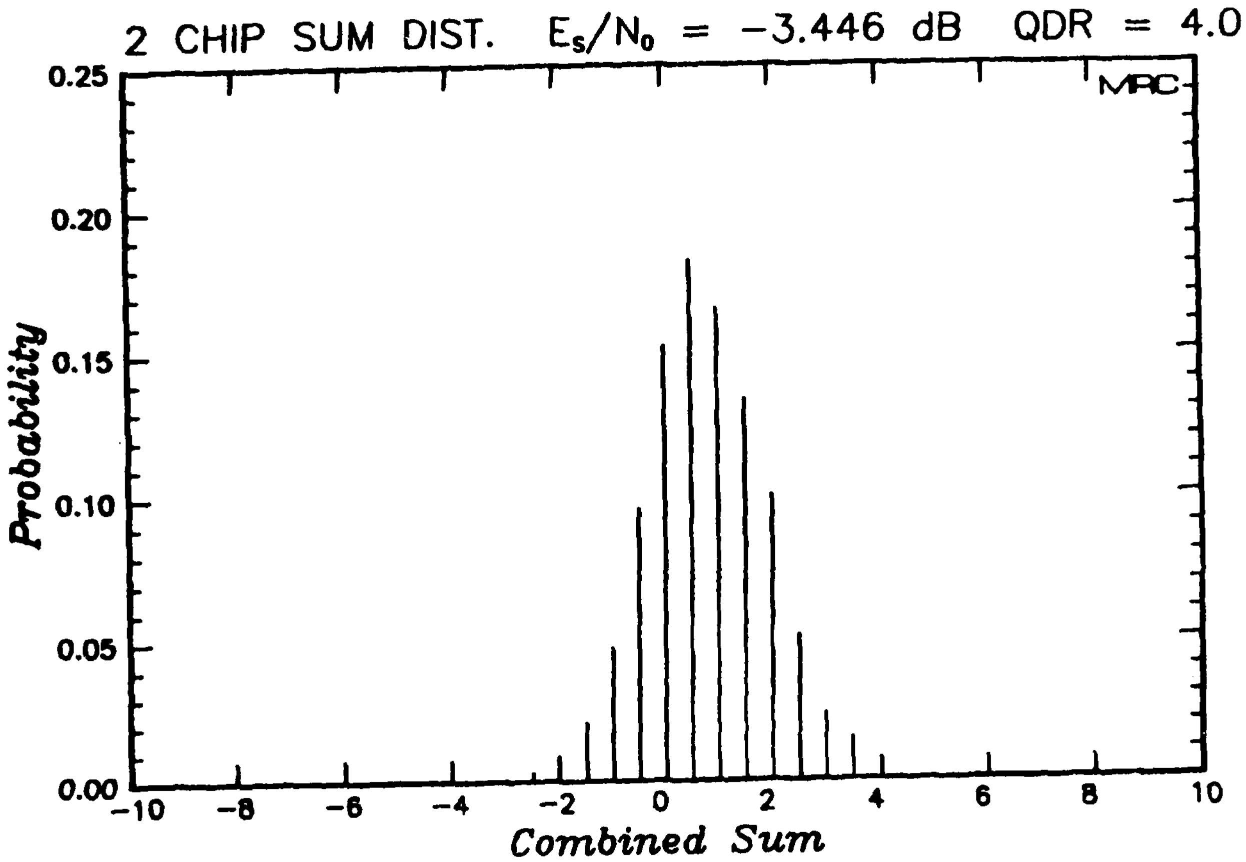


Figure 53. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -3.446 and normalized QDR of 4.0. (Applicable to Link 3)

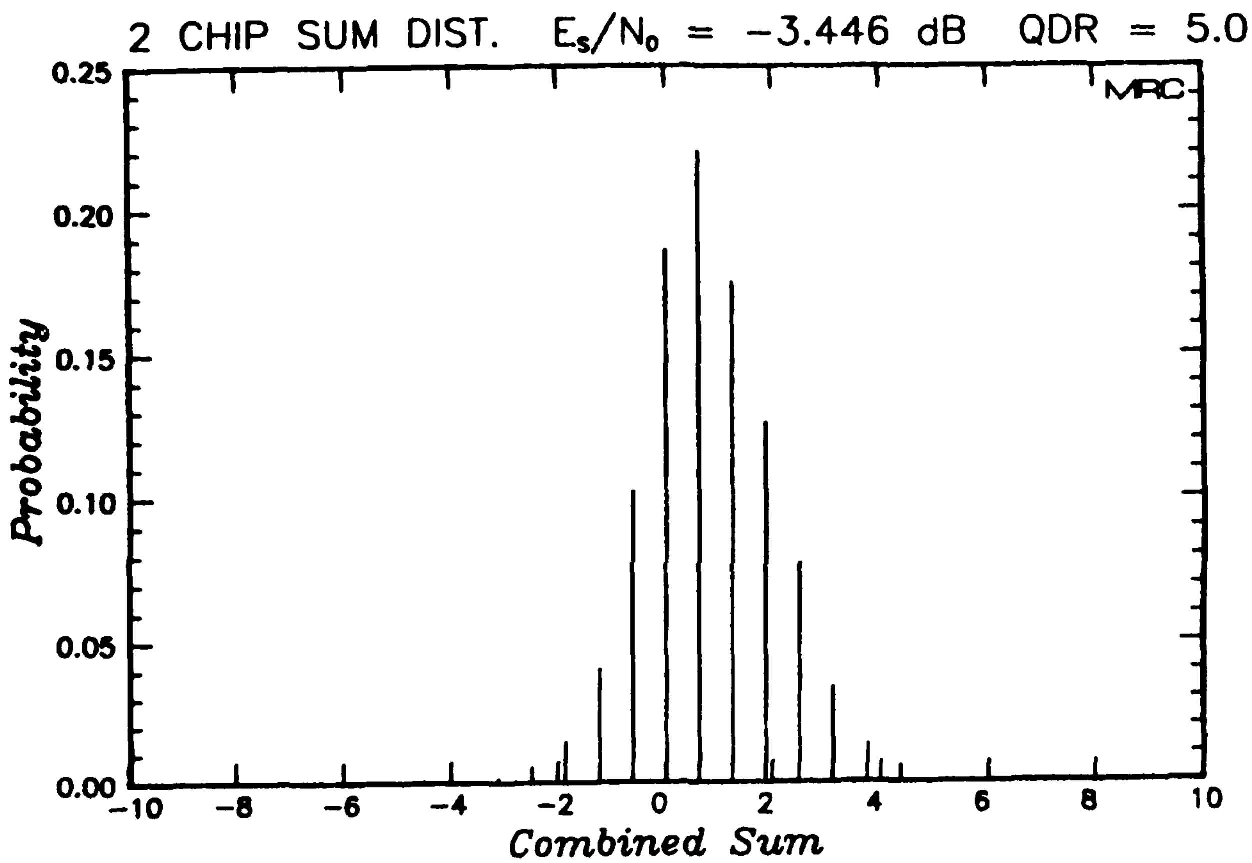


Figure 54. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 5.0. (Applicable to Link 3)

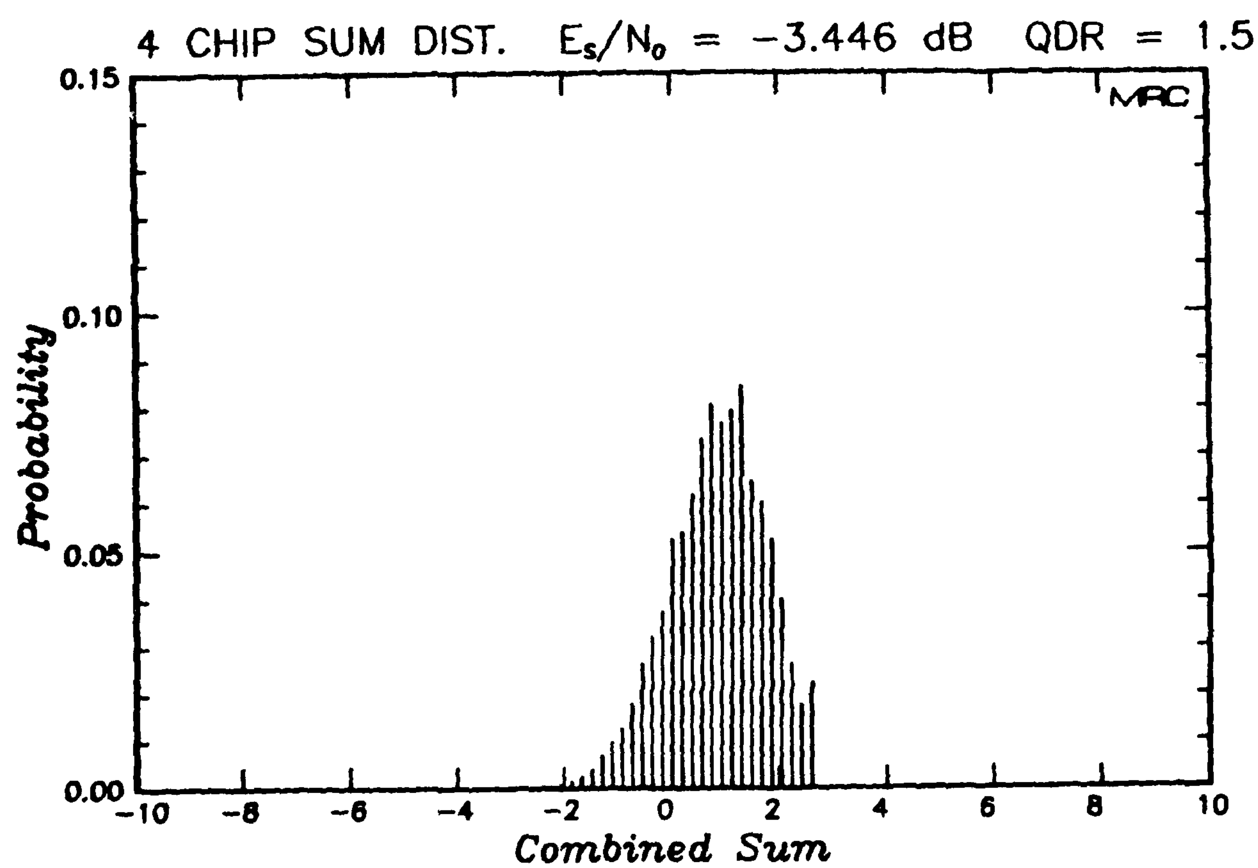


Figure 55. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_s/N_o = -3.446 and normalized QDR of 1.5. (Applicable to Link 2)

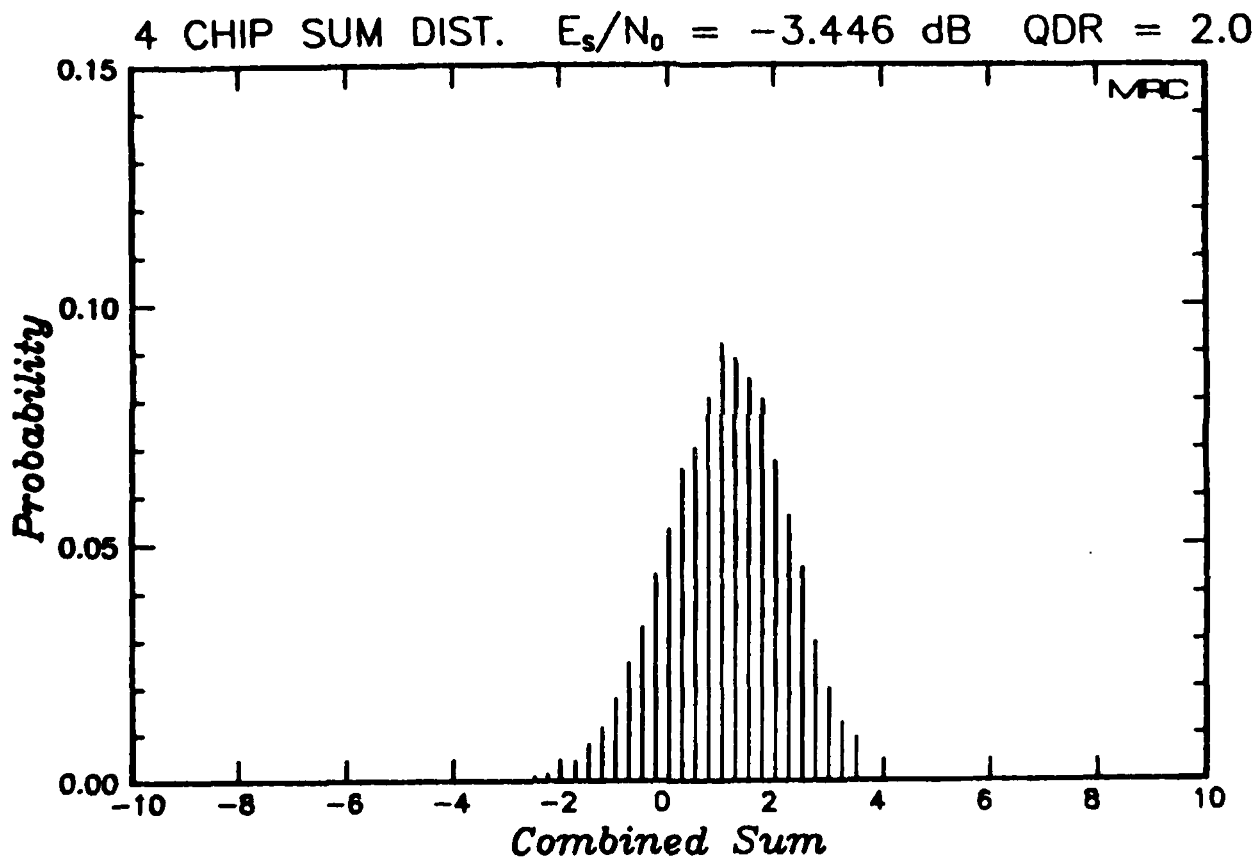


Figure 56. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 2.0. (Applicable to Link 2)

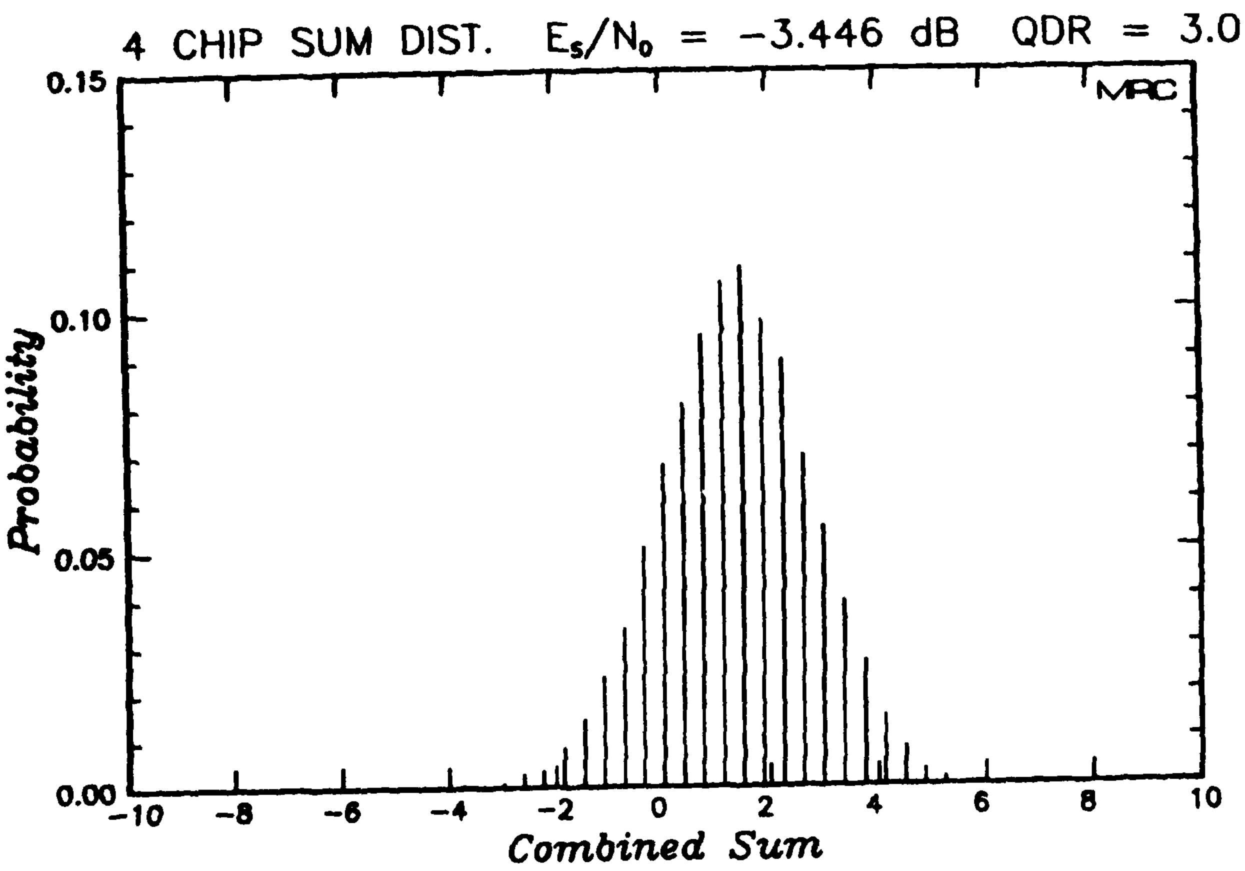


Figure 57. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 3.0. (Applicable to Link 2)

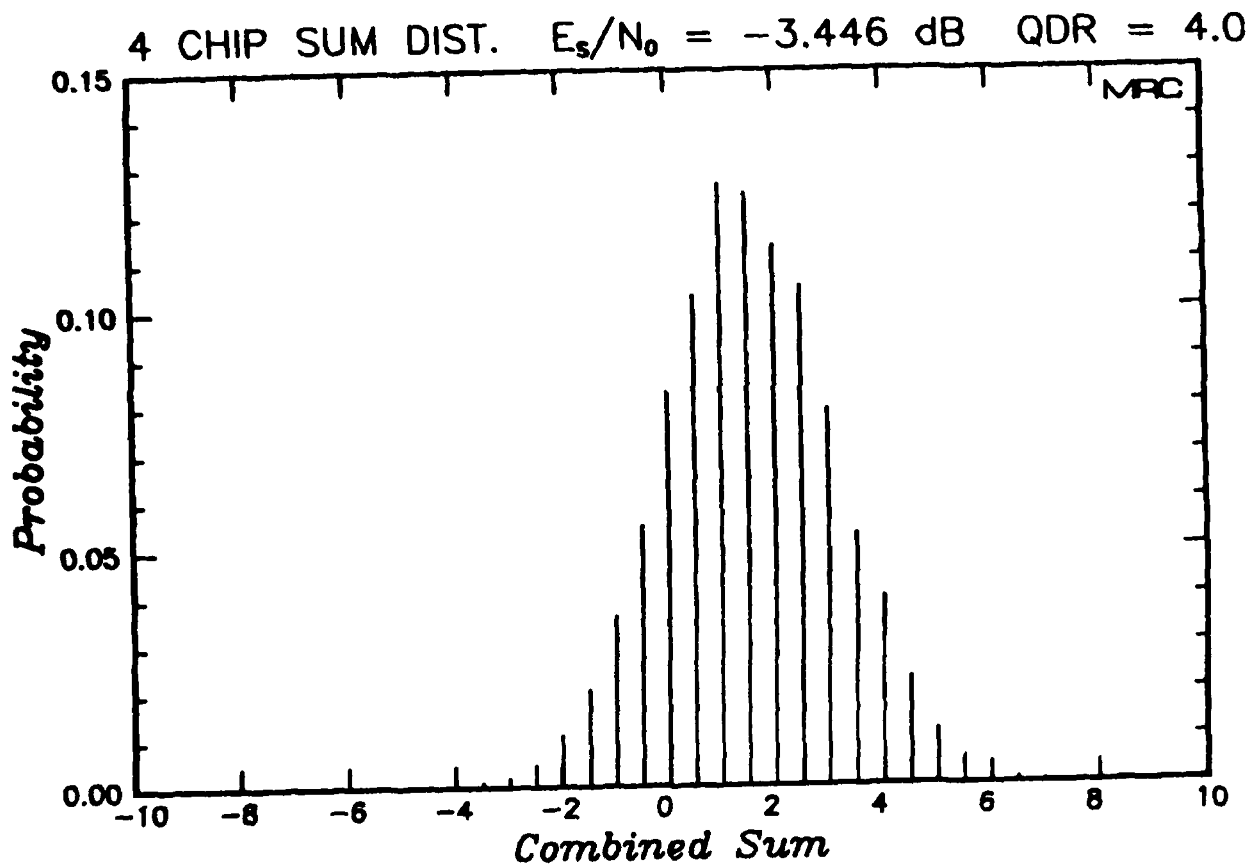


Figure 58. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 4.0. (Applicable to Link 2)

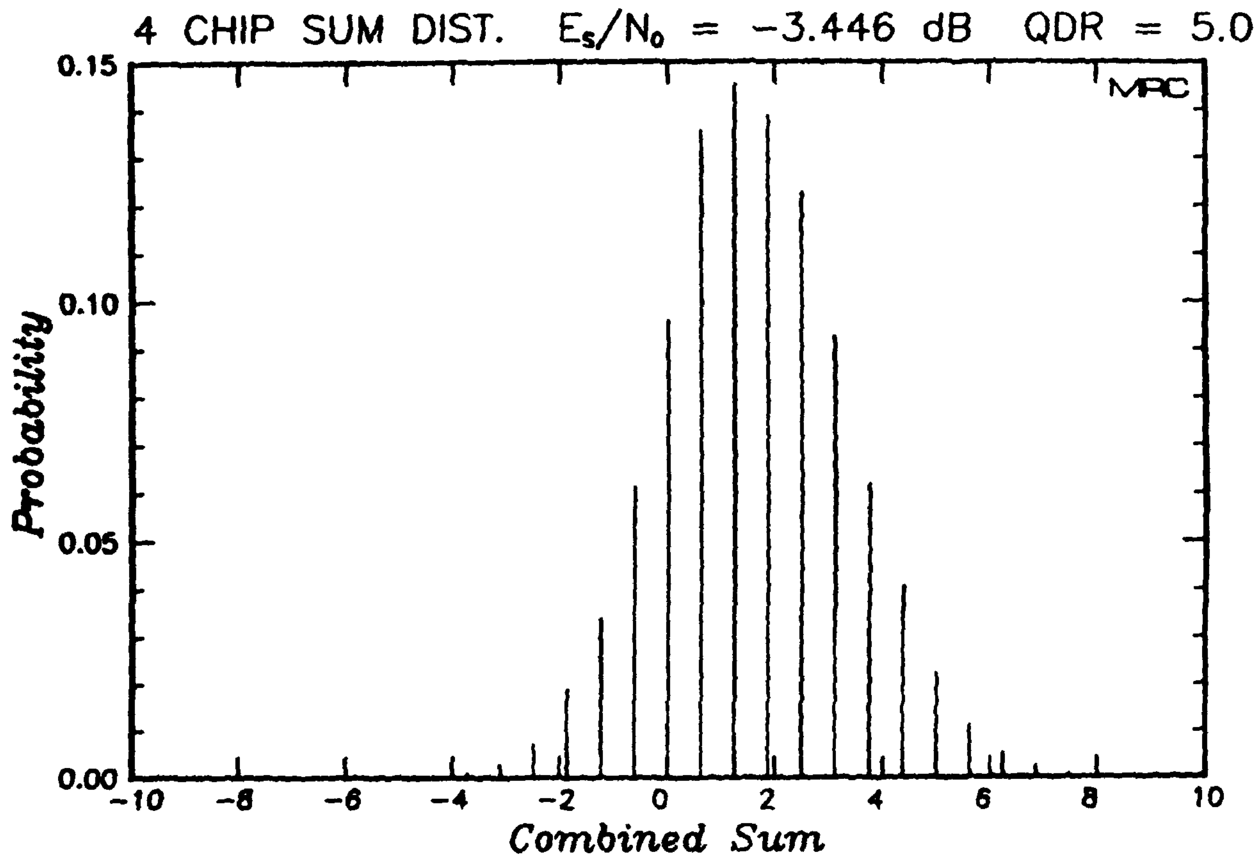


Figure 59. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 5.0. (Applicable to Link 2)

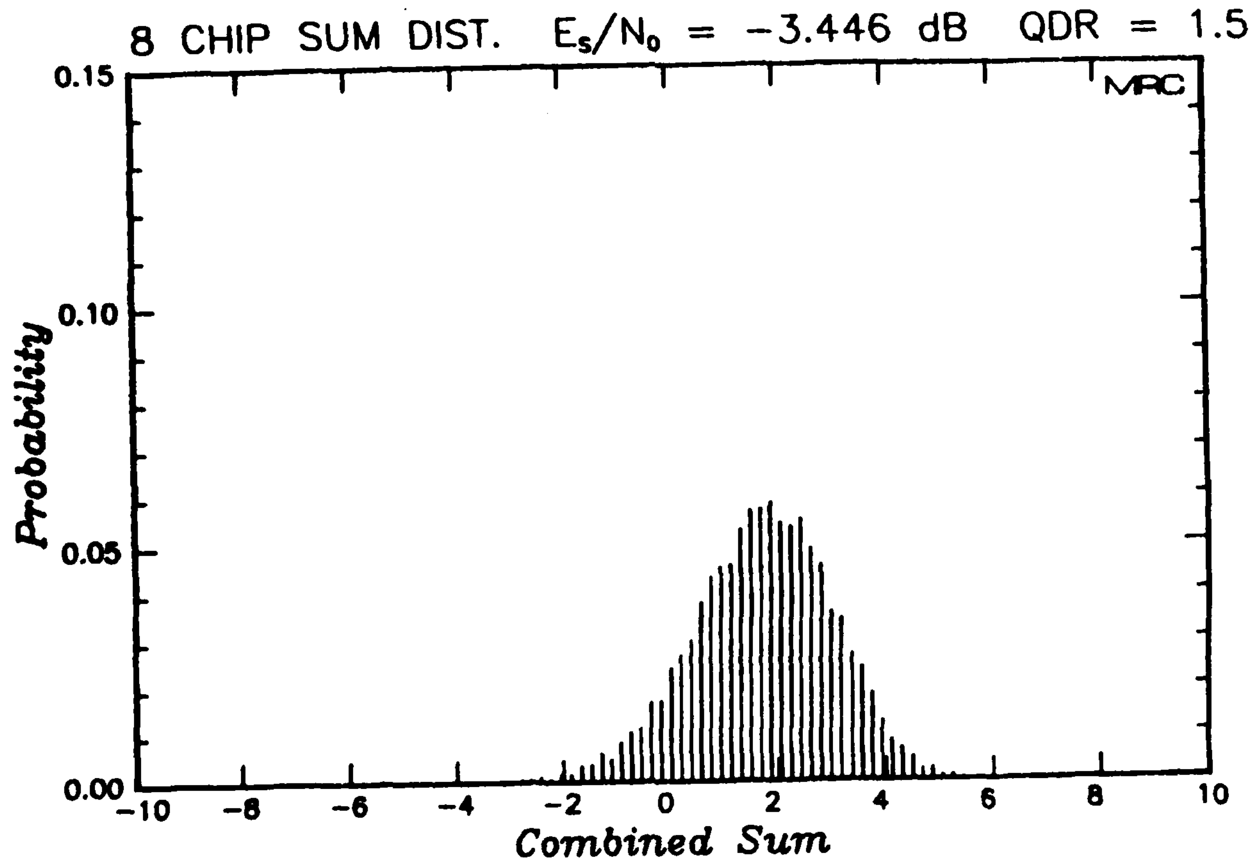


Figure 60. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_o = -3.446 and normalized QDR of 1.5. (Applicable to Link 1)

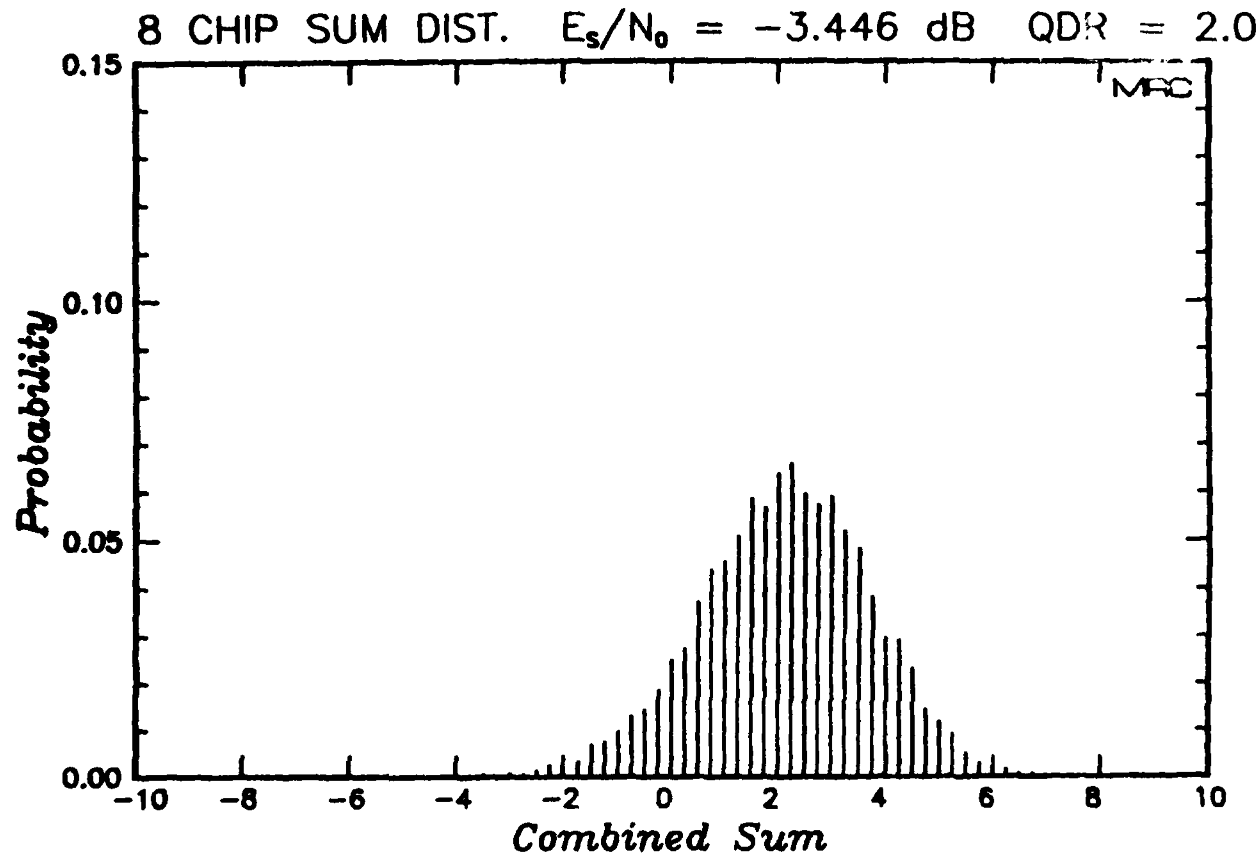


Figure 61. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -3.446 and normalized QDR of 2.0. (Applicable to Link 1)

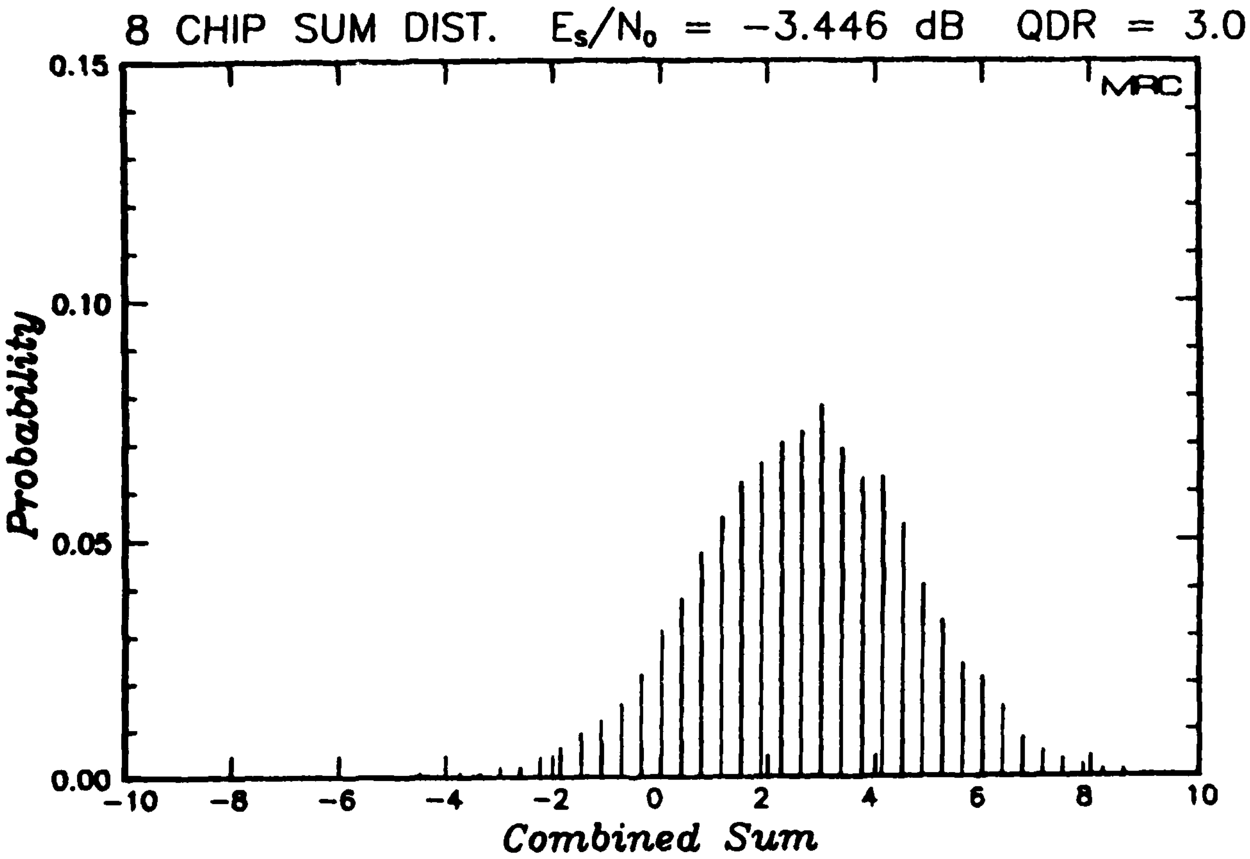


Figure 62. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -3.446 and normalized QDR of 3.0. (Applicable to Link 1)

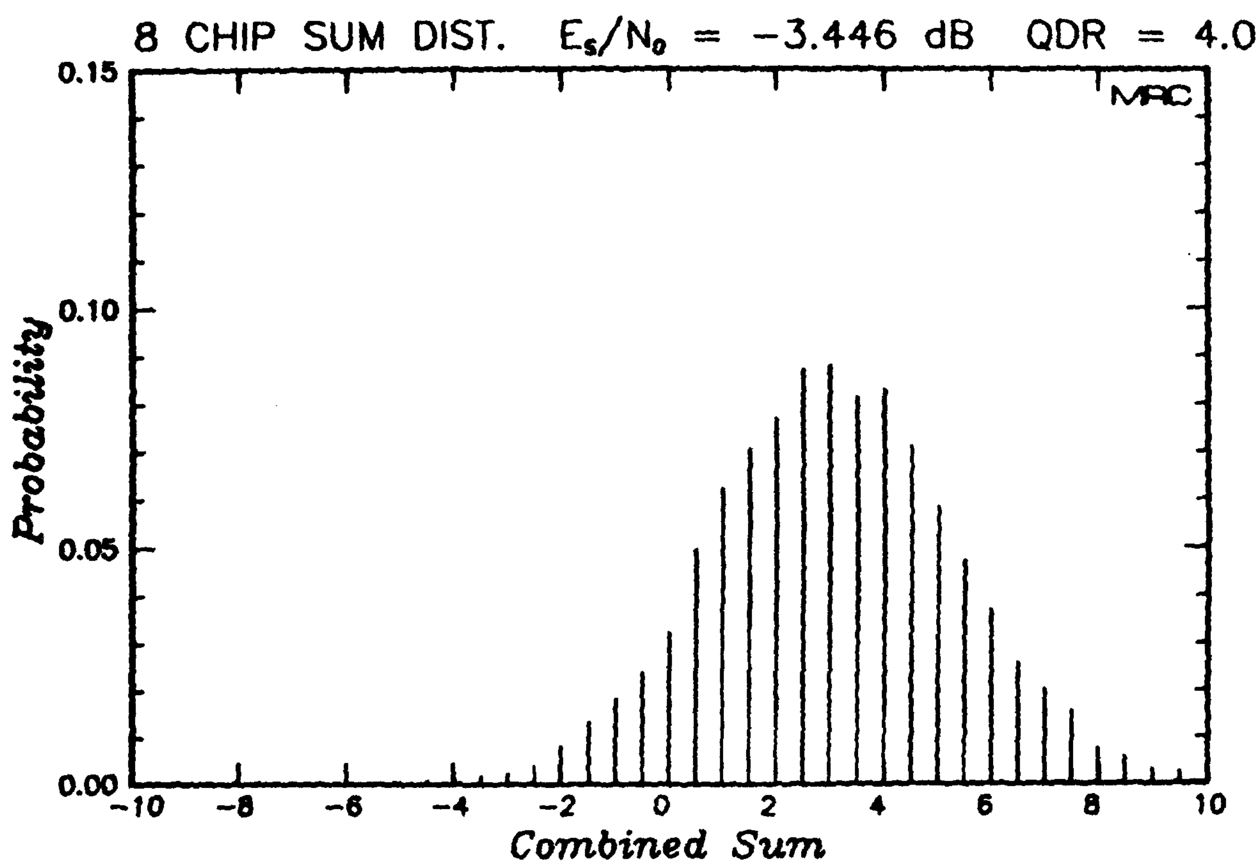


Figure 63. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 4.0. (Applicable to Link 1)

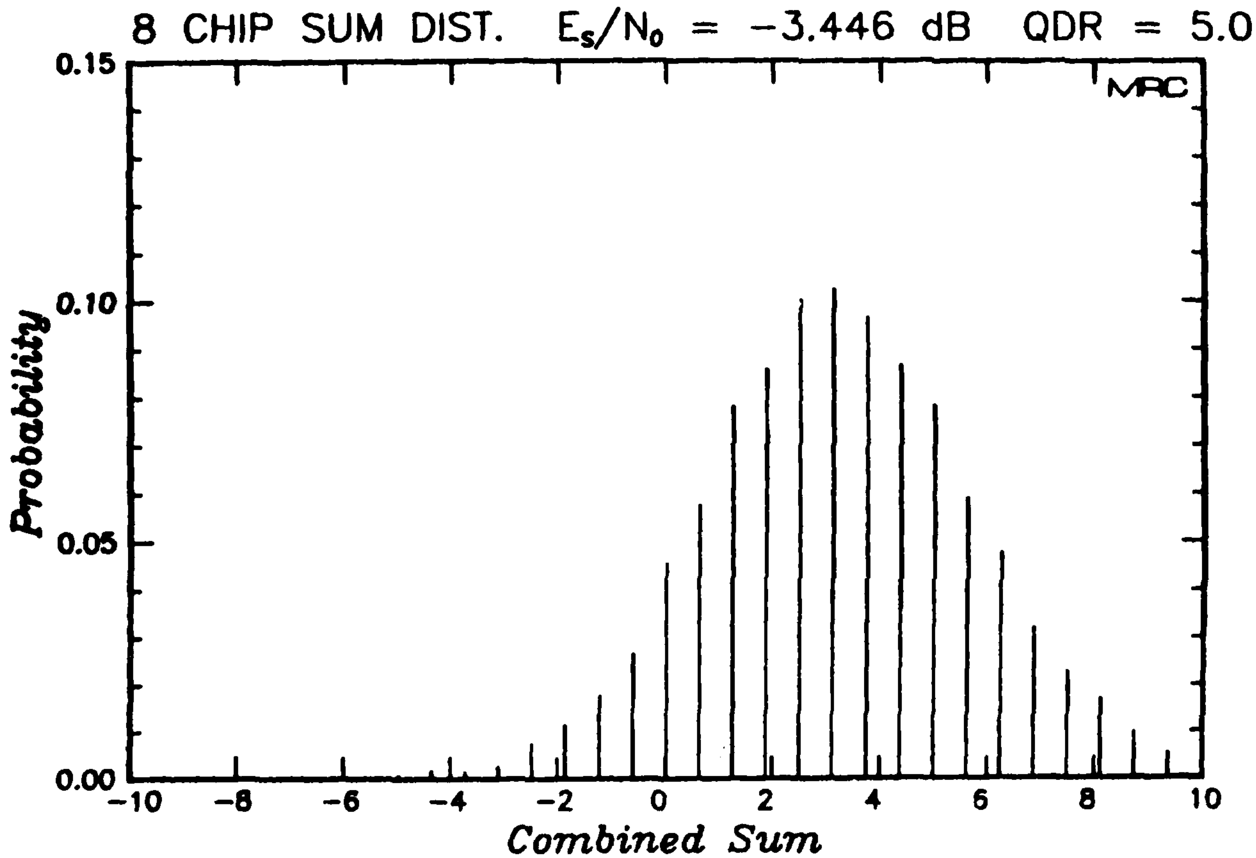


Figure 64. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -3.446 and normalized QDR of 5.0. (Applicable to Link 1)

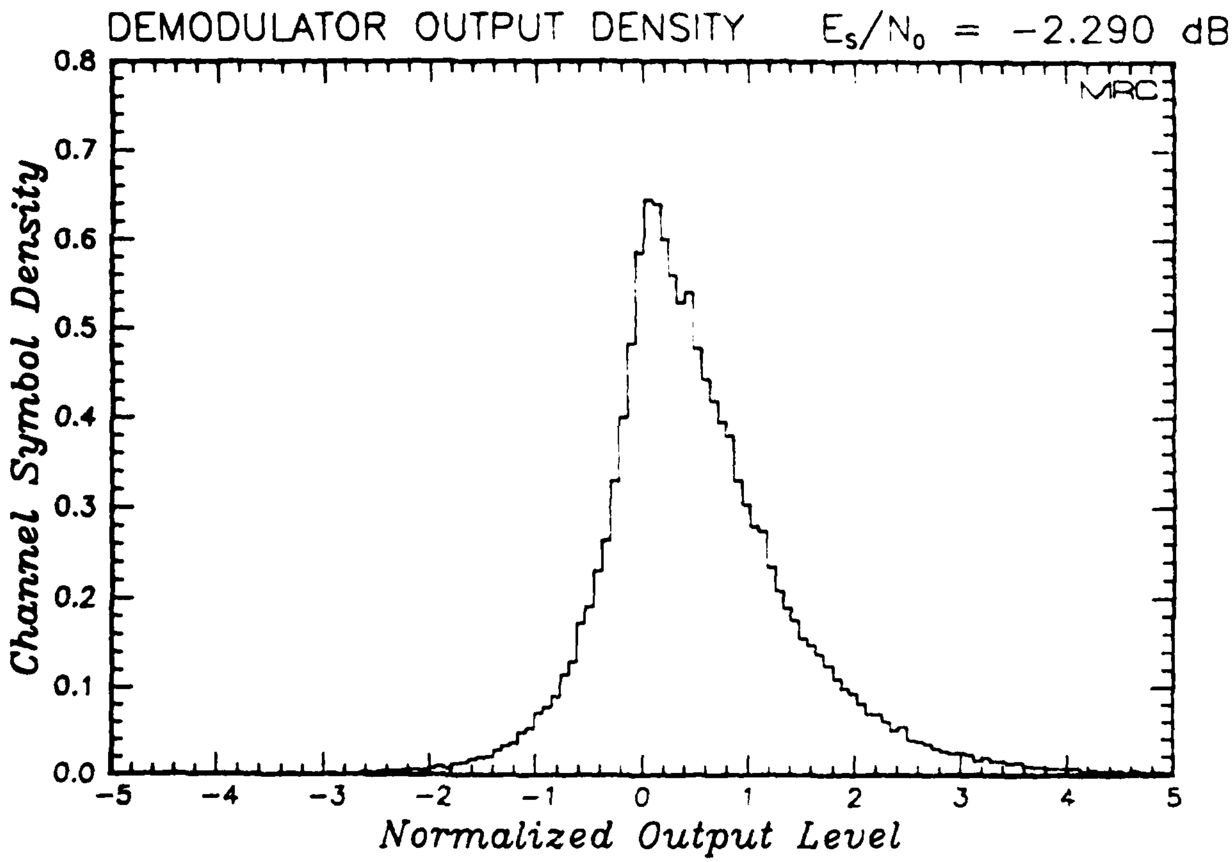


Figure 65. Histogram of demodulator outputs under benign channel conditions for E_S/N_0 = -2.290 dB.

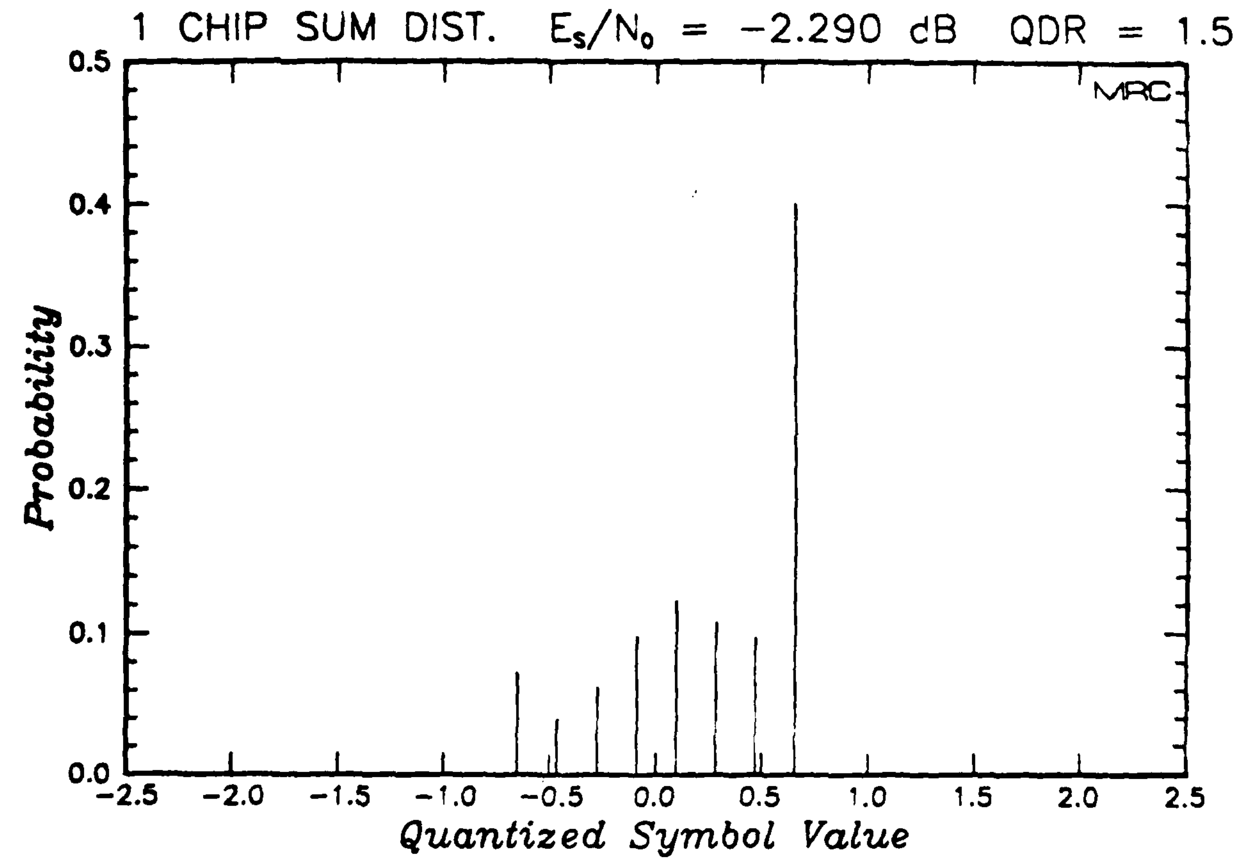


Figure 66. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_o = -2.290 and normalized QDR of 1.5. (Applicable to Link 4)

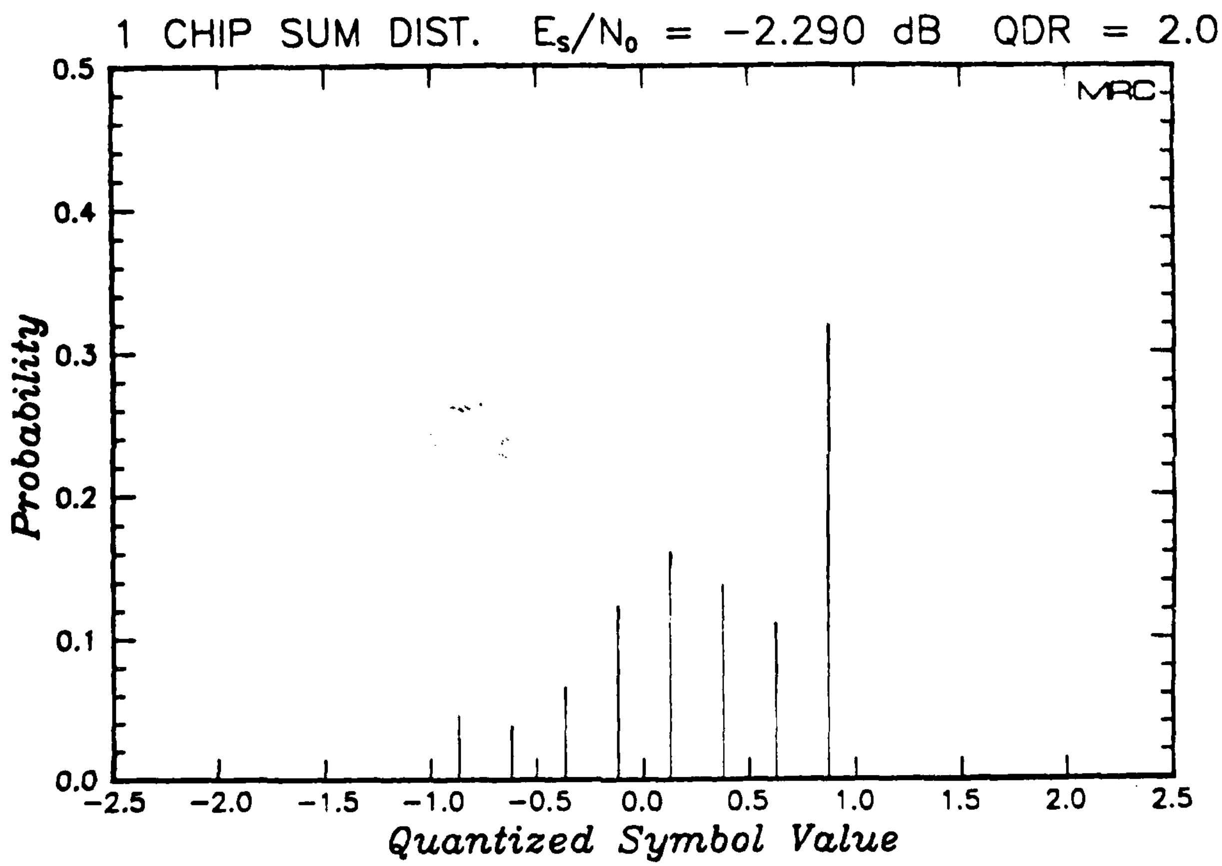


Figure 67. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 2.0. (Applicable to Link 4)

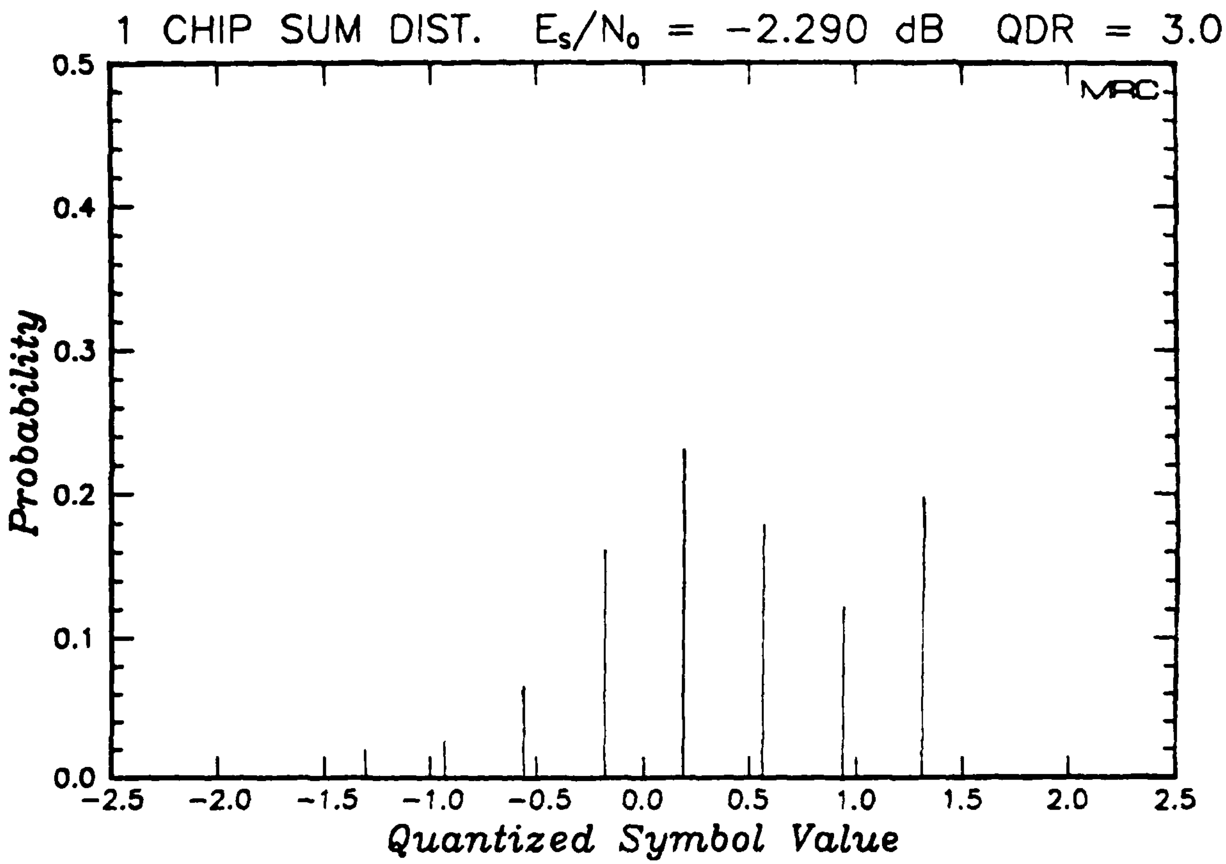


Figure 68. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 3.0. (Applicable to Link 4)

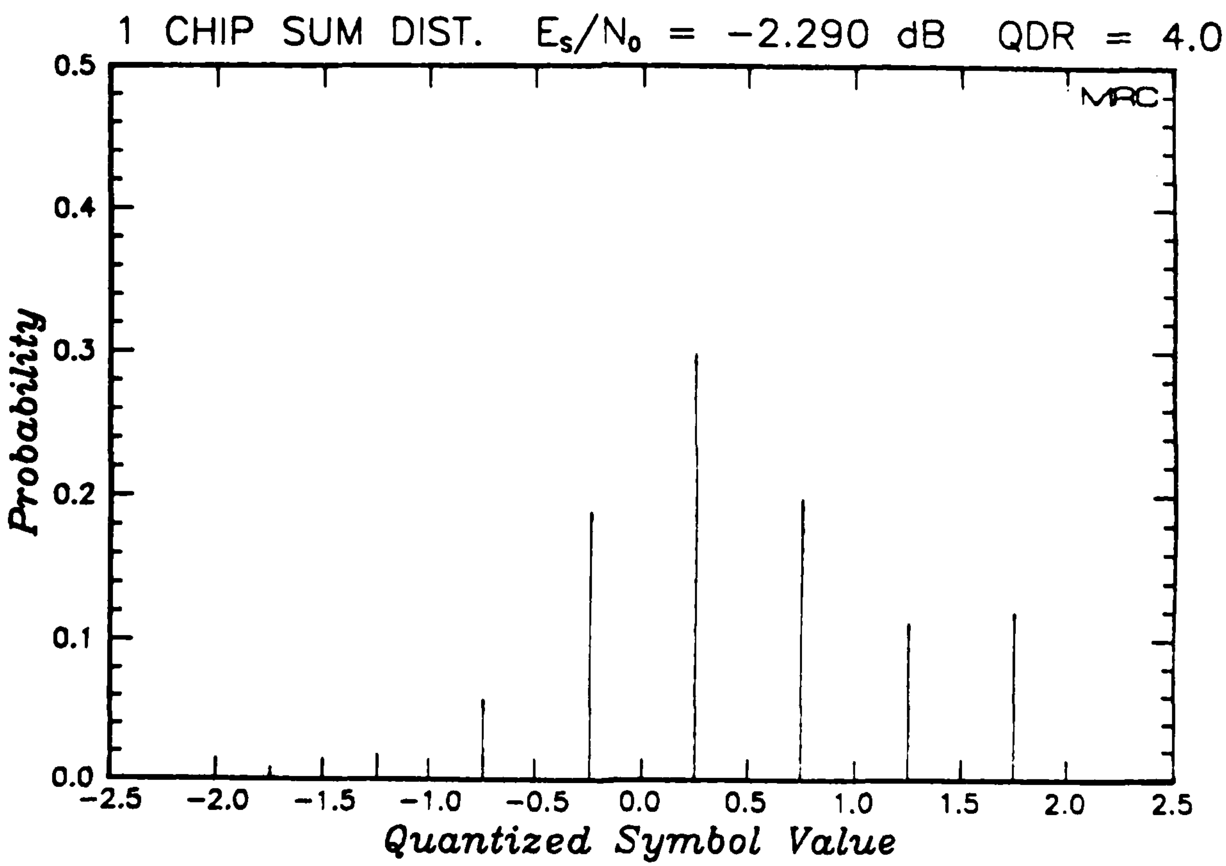


Figure 69. Measured probability distribution of quantized symbols under benign channel conditions for E_s/N_0 = -2.290 and normalized QDR of 4.0. (Applicable to Link 4)

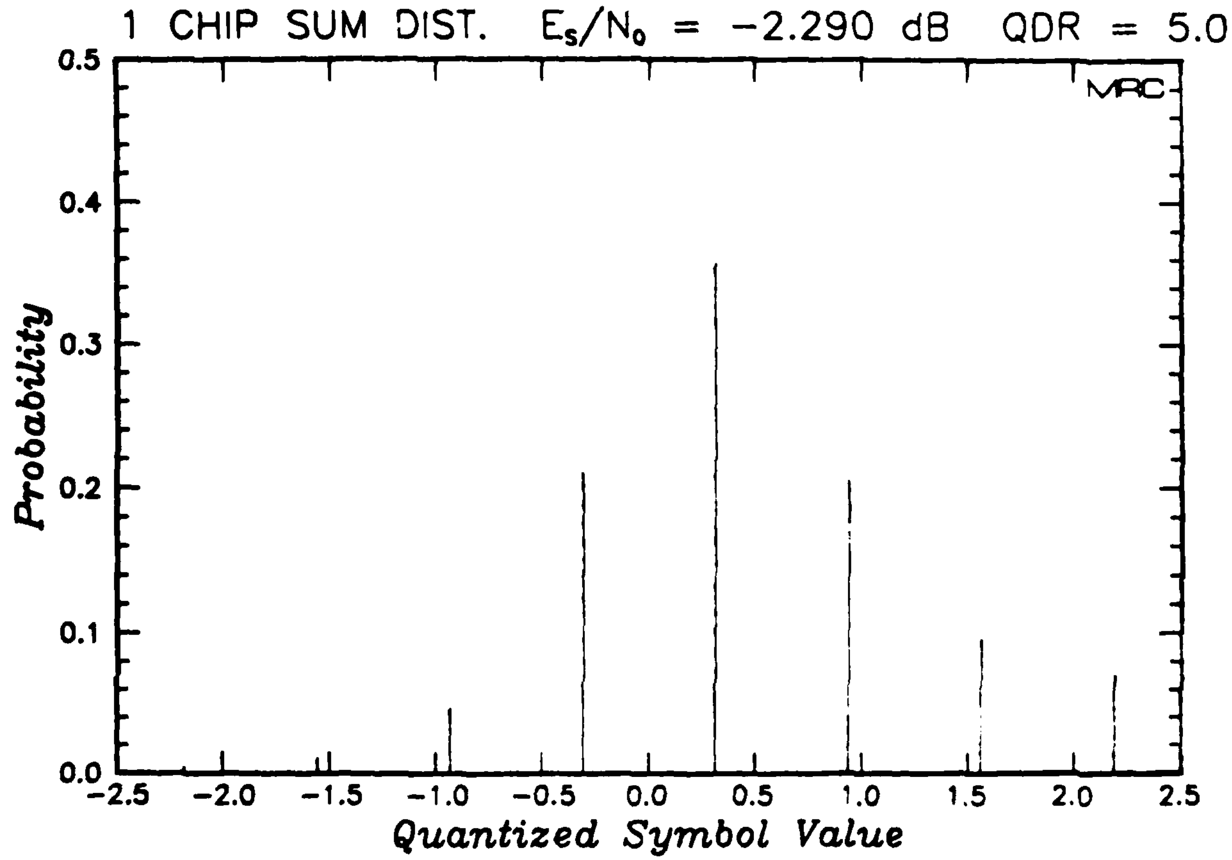


Figure 70. Measured probability distribution of quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 5.0. (Applicable to Link 4)

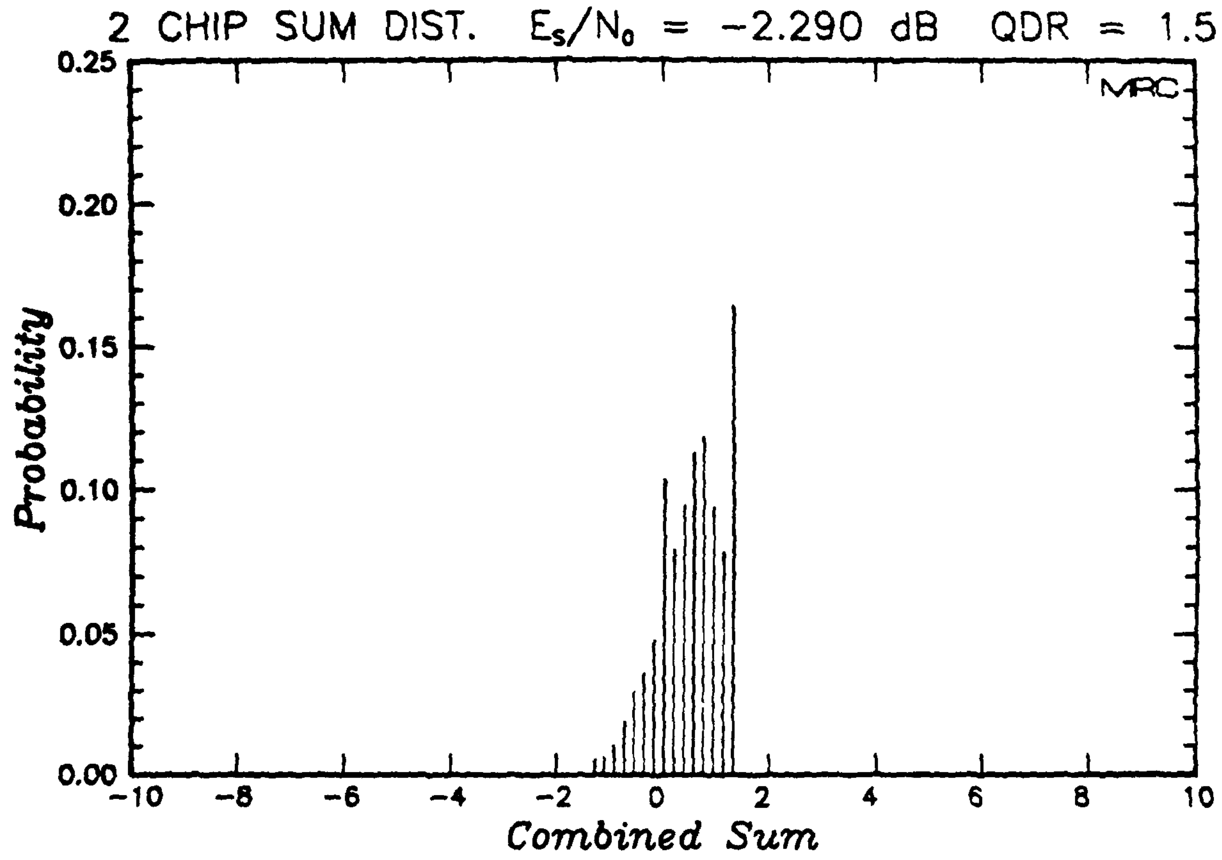


Figure 71. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 1.5. (Applicable to Link 3)

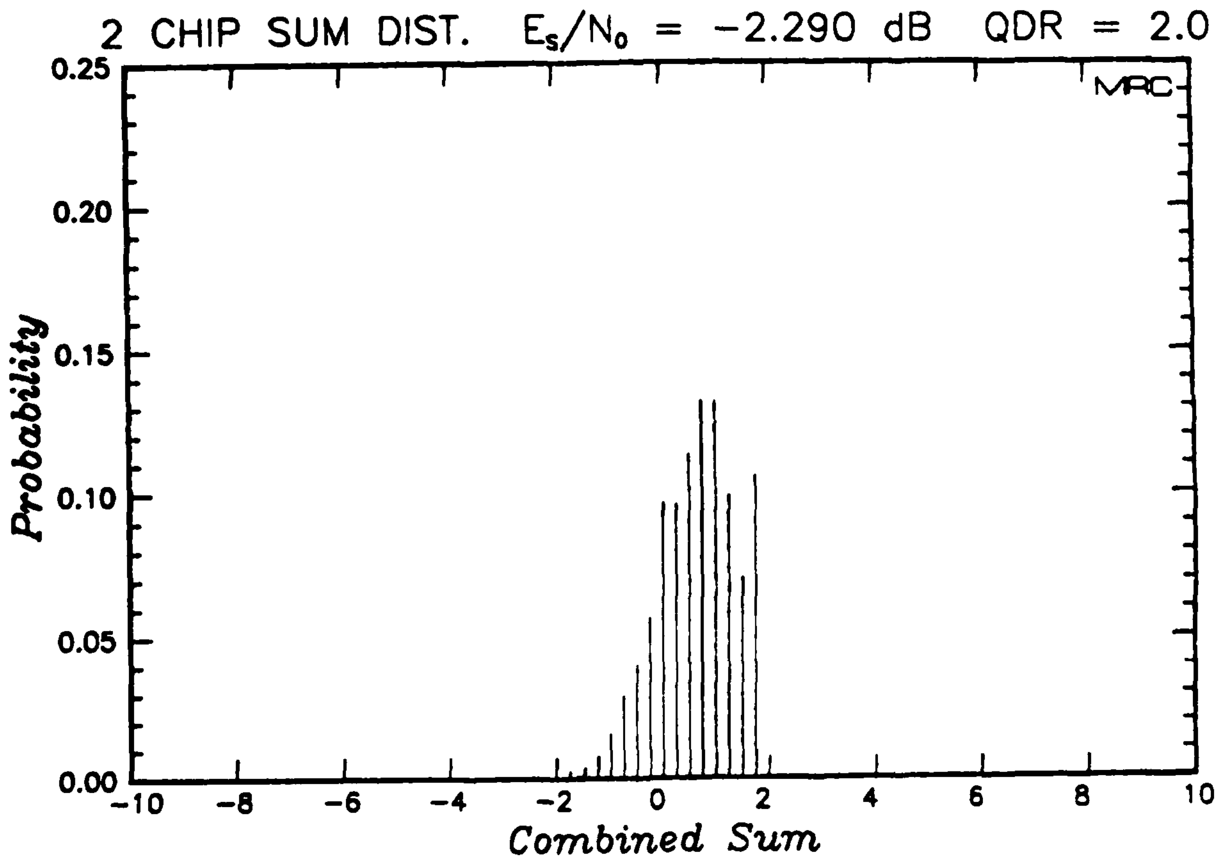


Figure 72. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 2.0. (Applicable to Link 3)

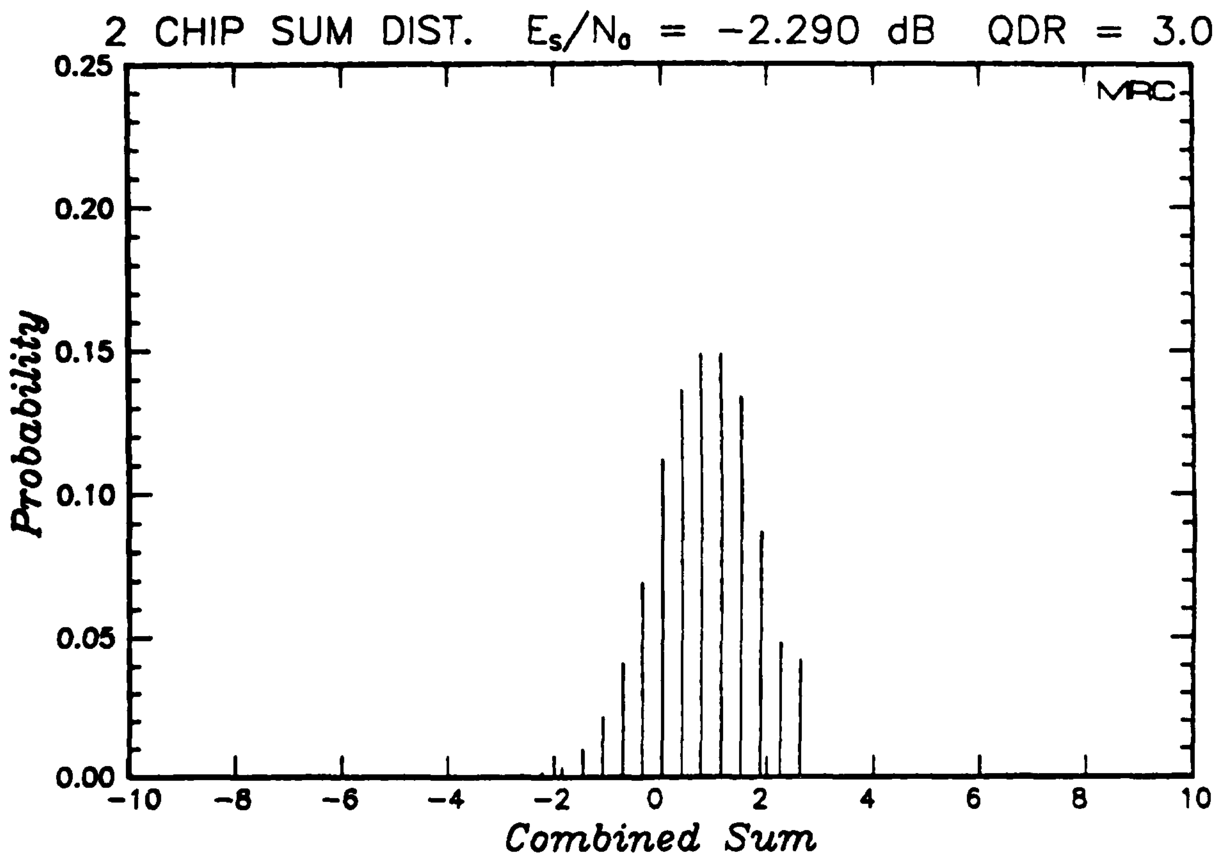


Figure 73. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 3.0. (Applicable to Link 3)

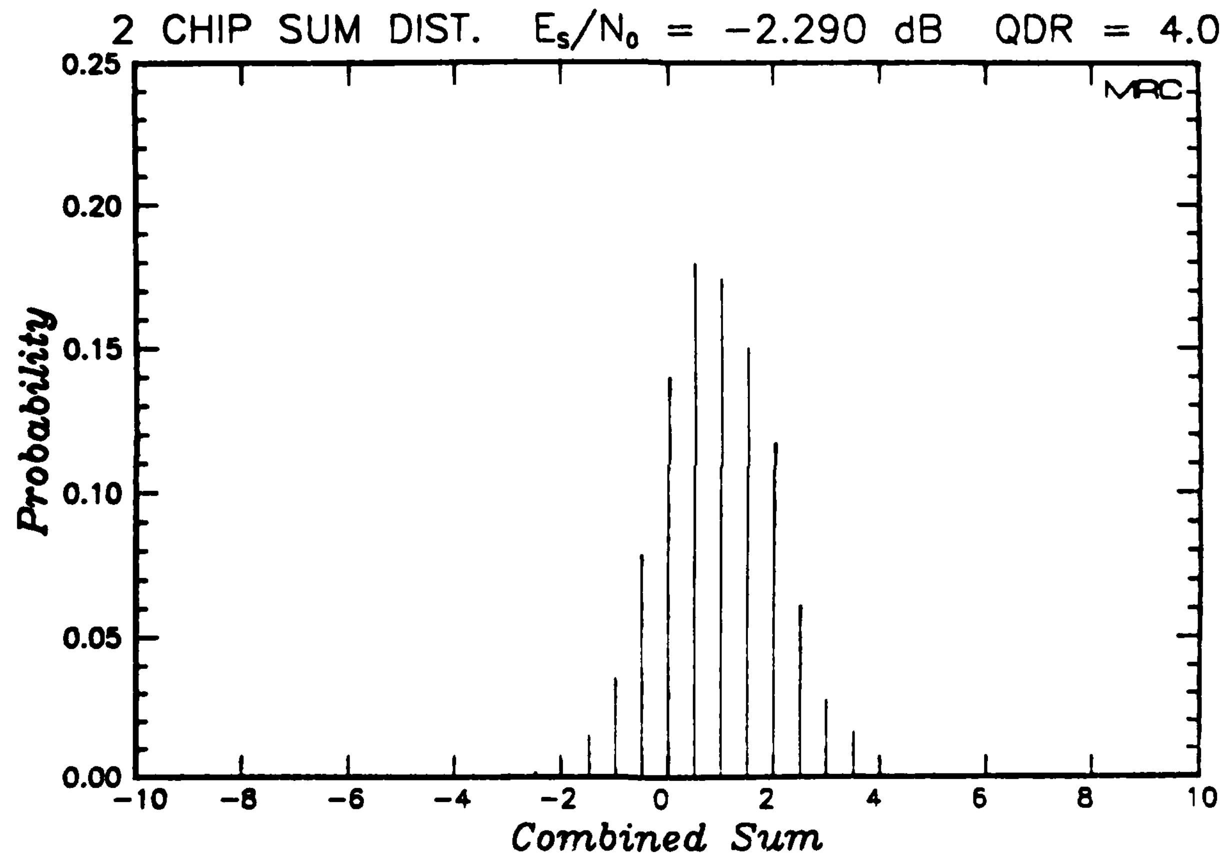


Figure 74. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -2.290 and normalized QDR of 4.0. (Applicable to Link 3)

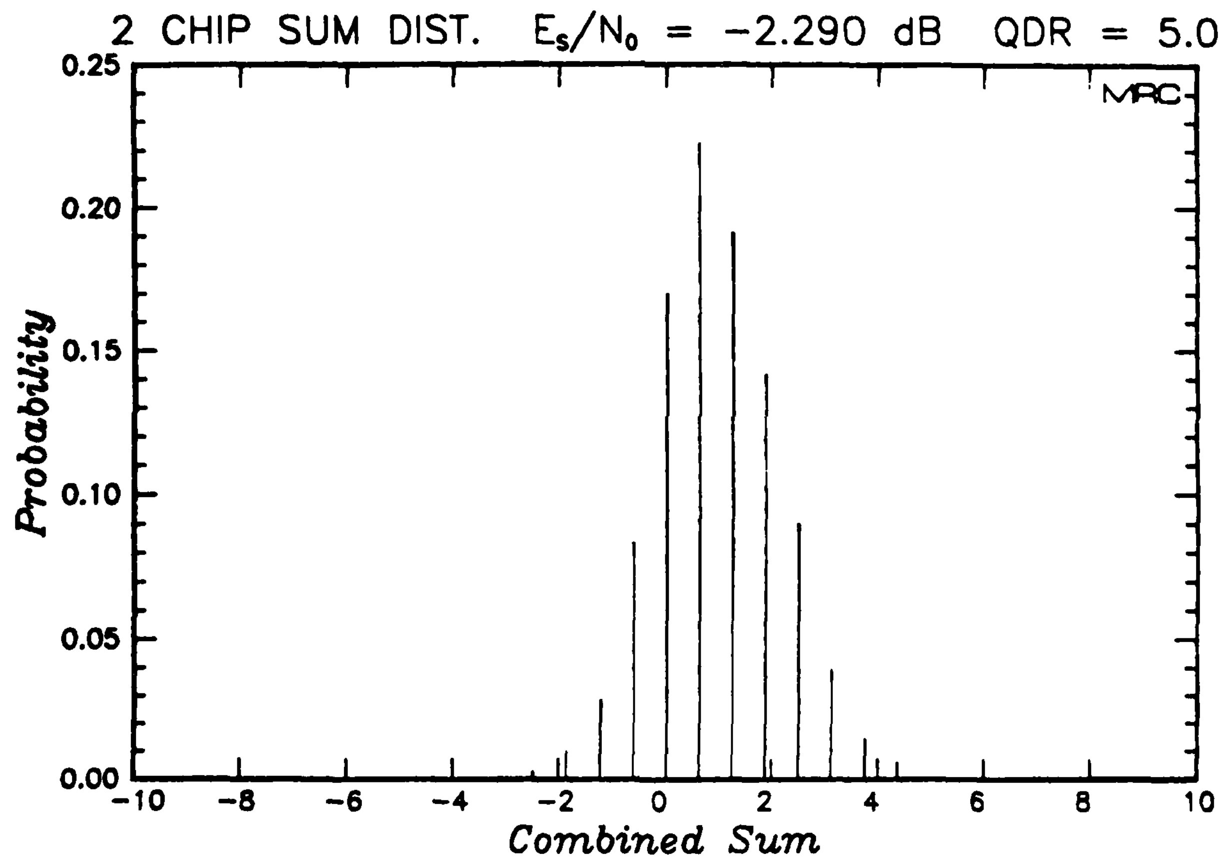


Figure 75. Measured probability distribution of the two-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 5.0. (Applicable to Link 3)

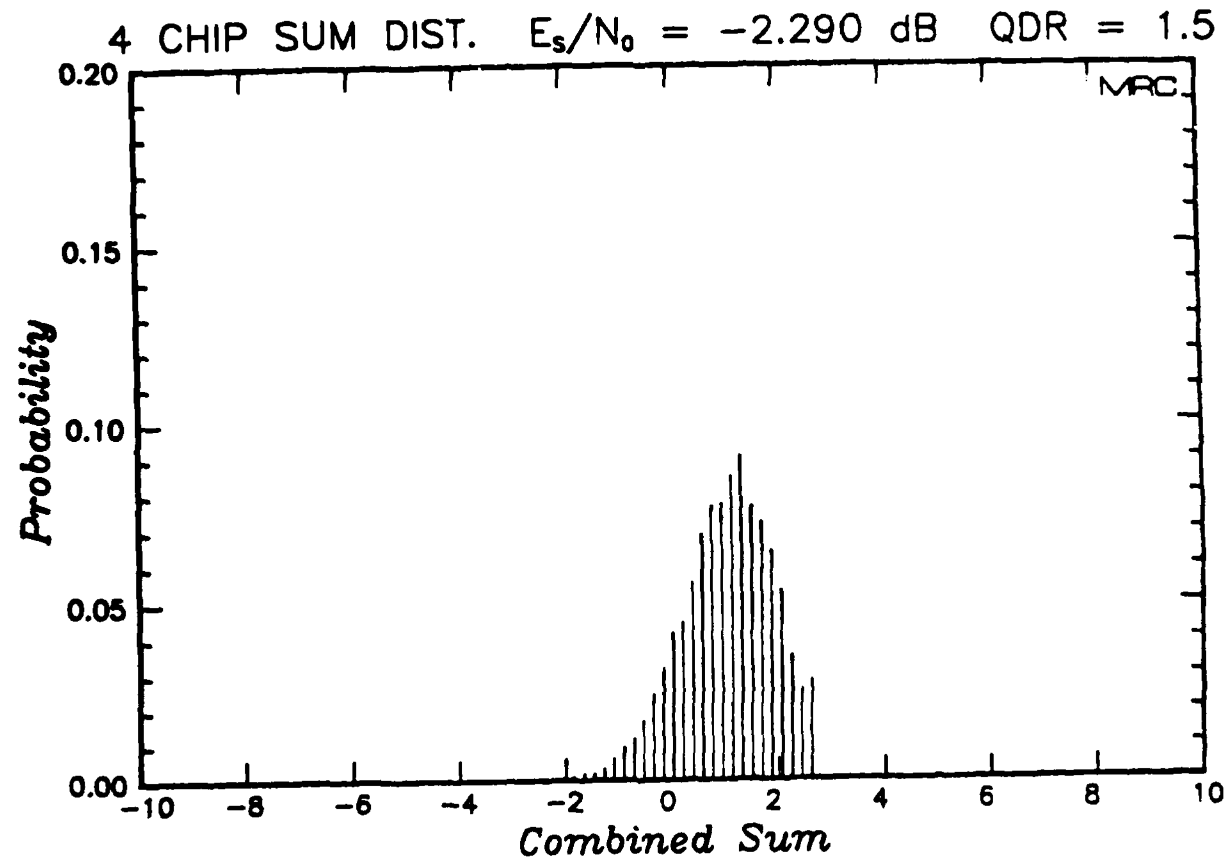


Figure 76. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -2.290 and normalized QDR of 1.5. (Applicable to Link 2)

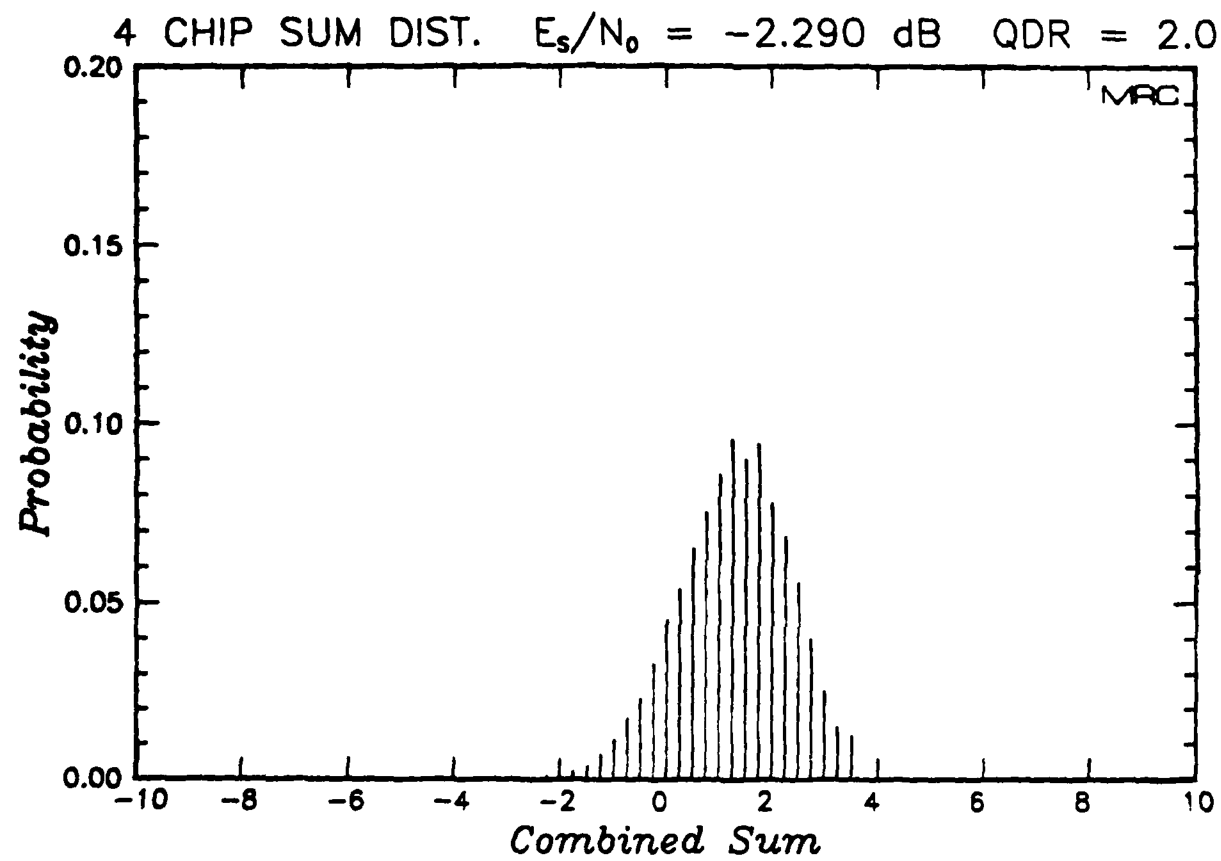


Figure 77. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -2.290 and normalized QDR of 2.0. (Applicable to Link 2)

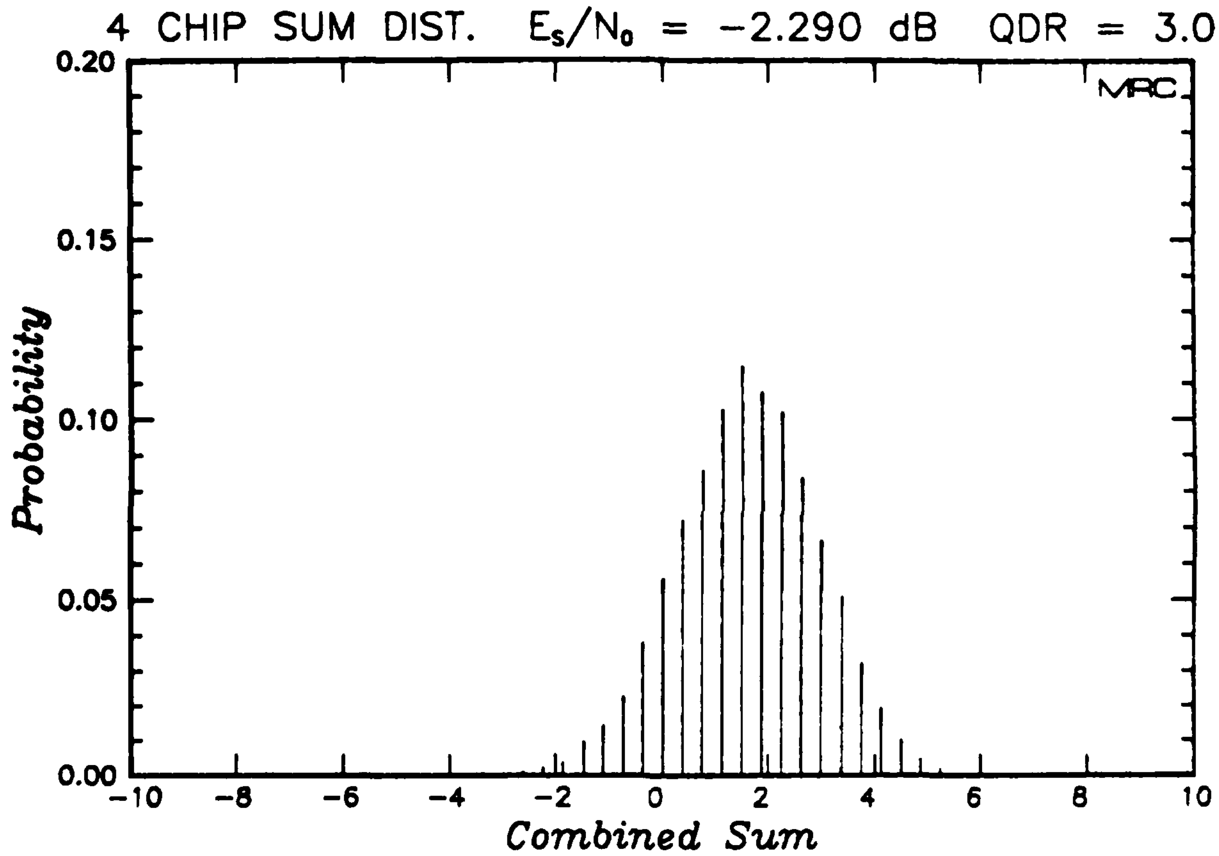


Figure 78. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 3.0. (Applicable to Link 2)

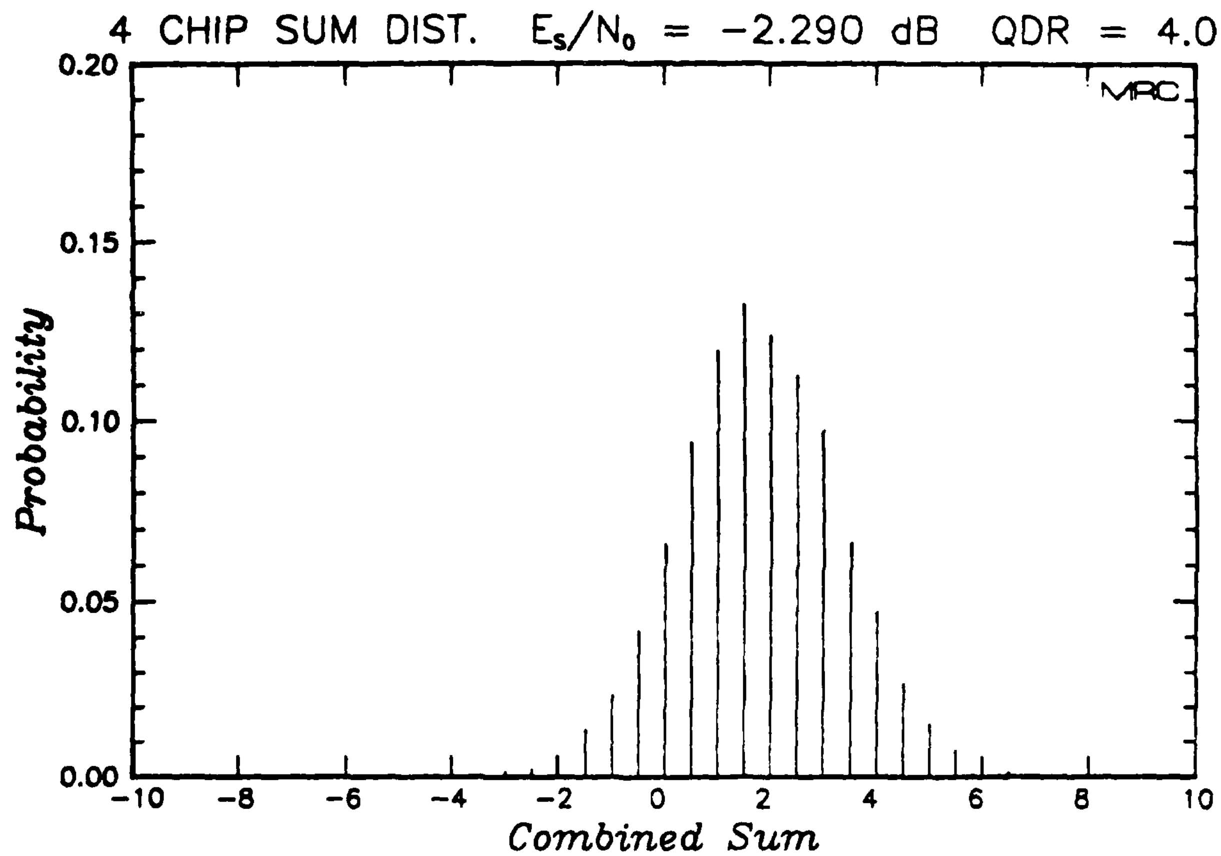


Figure 79. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -2.290 and normalized QDR of 4.0. (Applicable to Link 2)

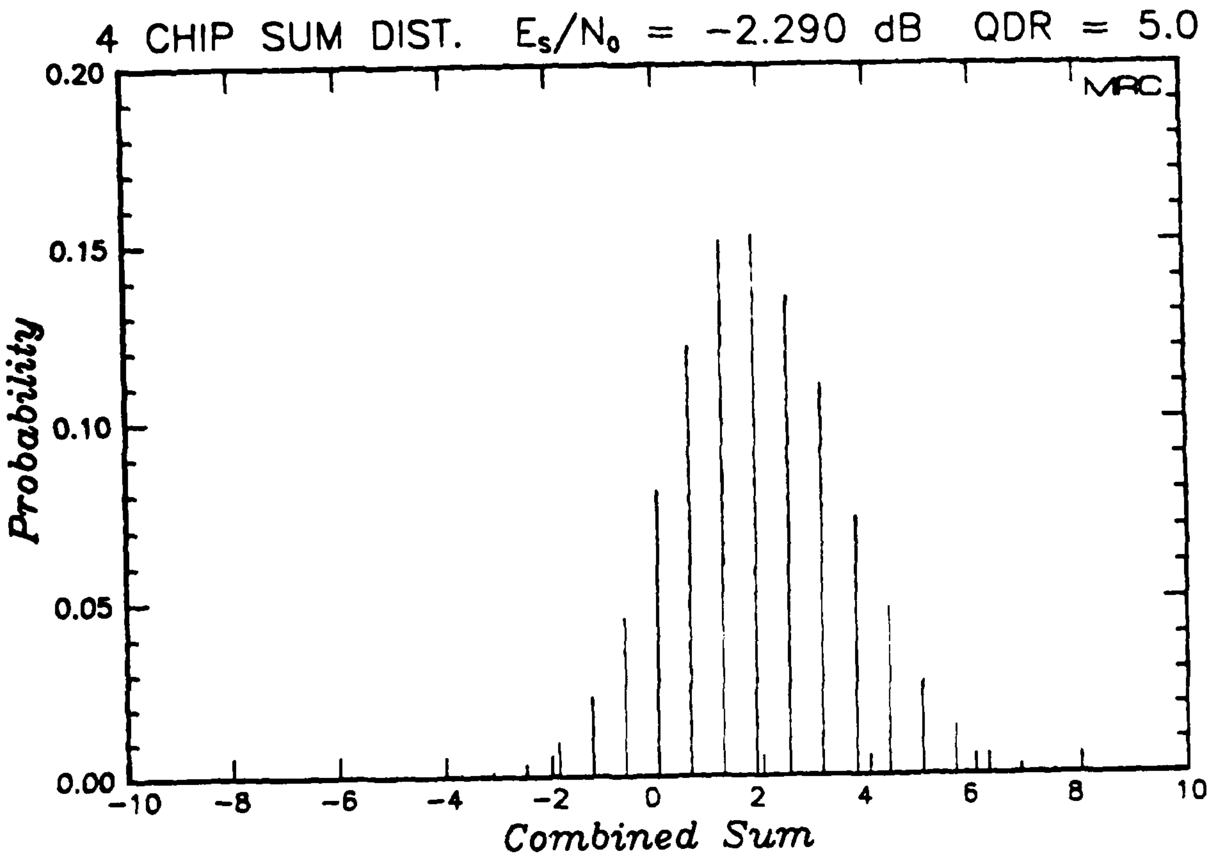


Figure 80. Measured probability distribution of the four-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 5.0. (Applicable to Link 2)

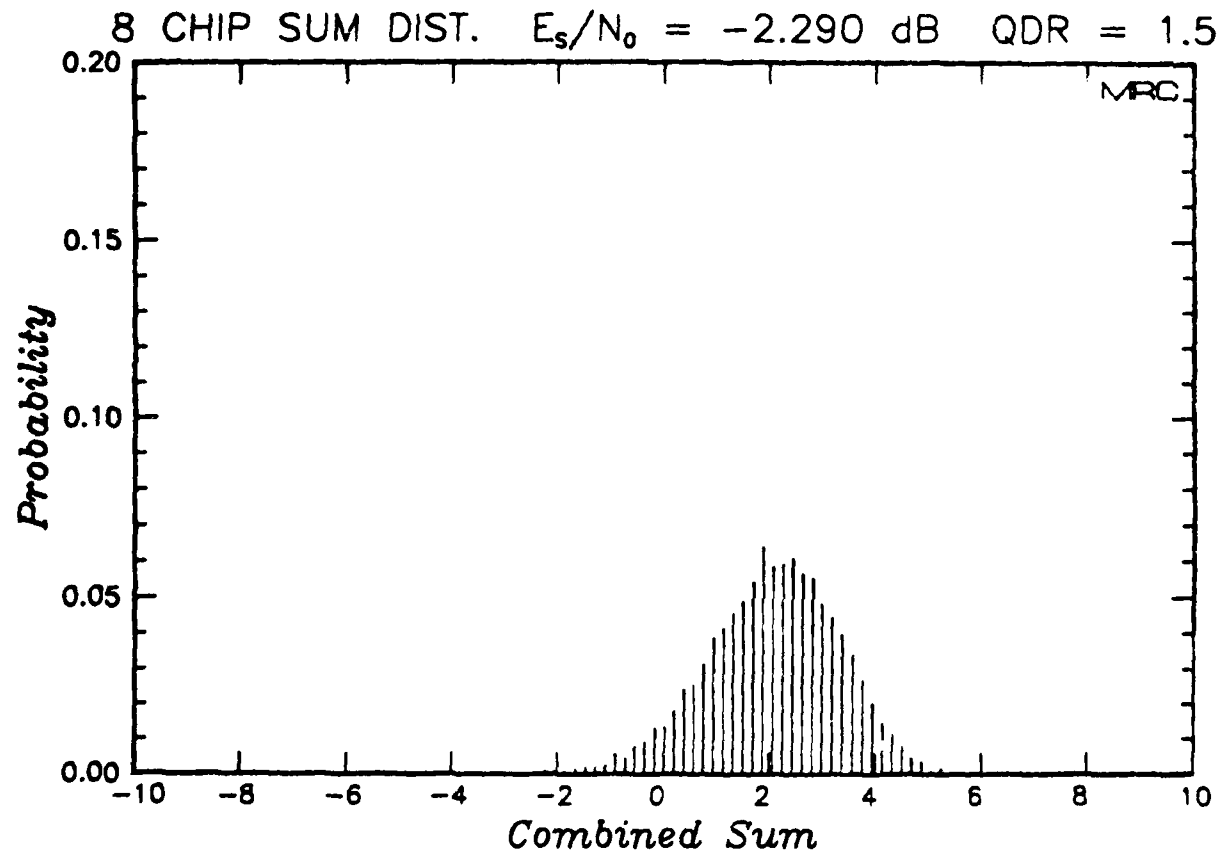


Figure 81. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 1.5. (Applicable to Link 1)

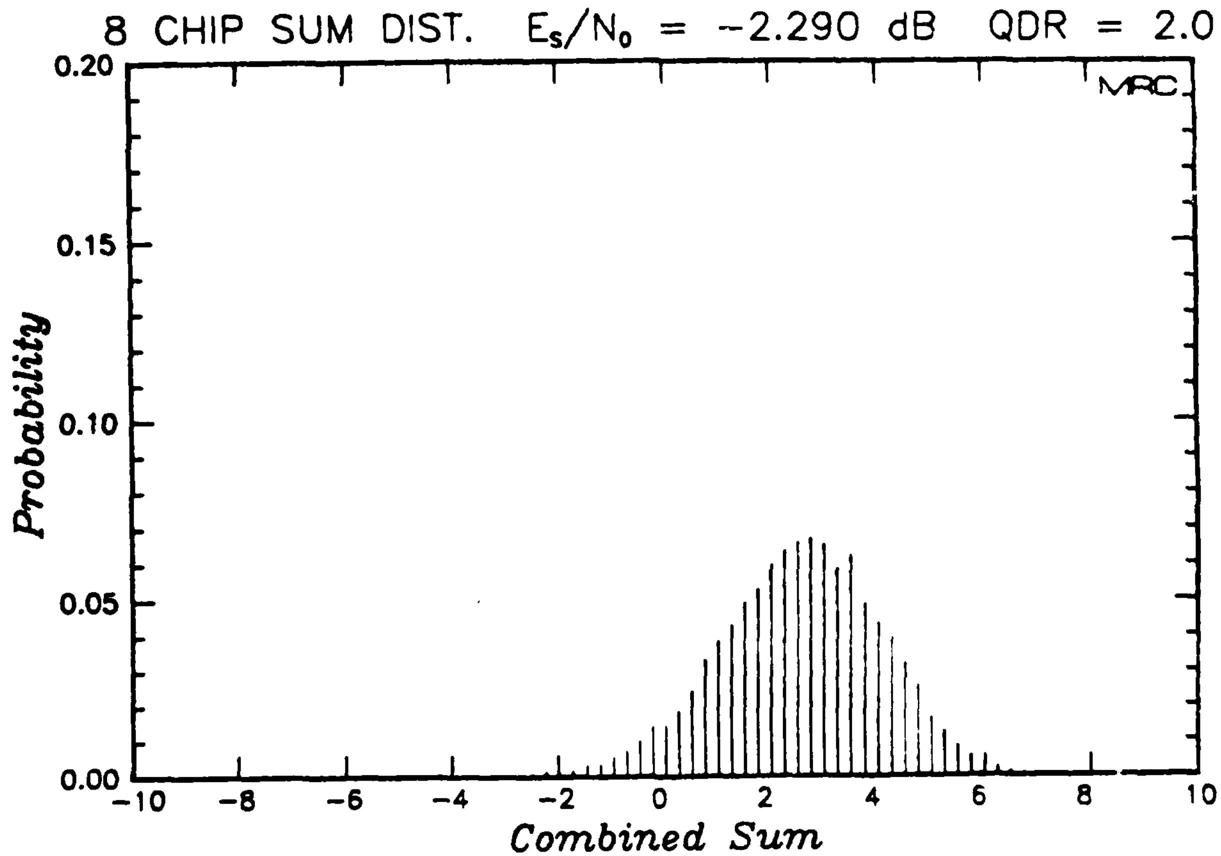


Figure 82. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_s/N_0 = -2.290 and normalized QDR of 2.0. (Applicable to Link 1)

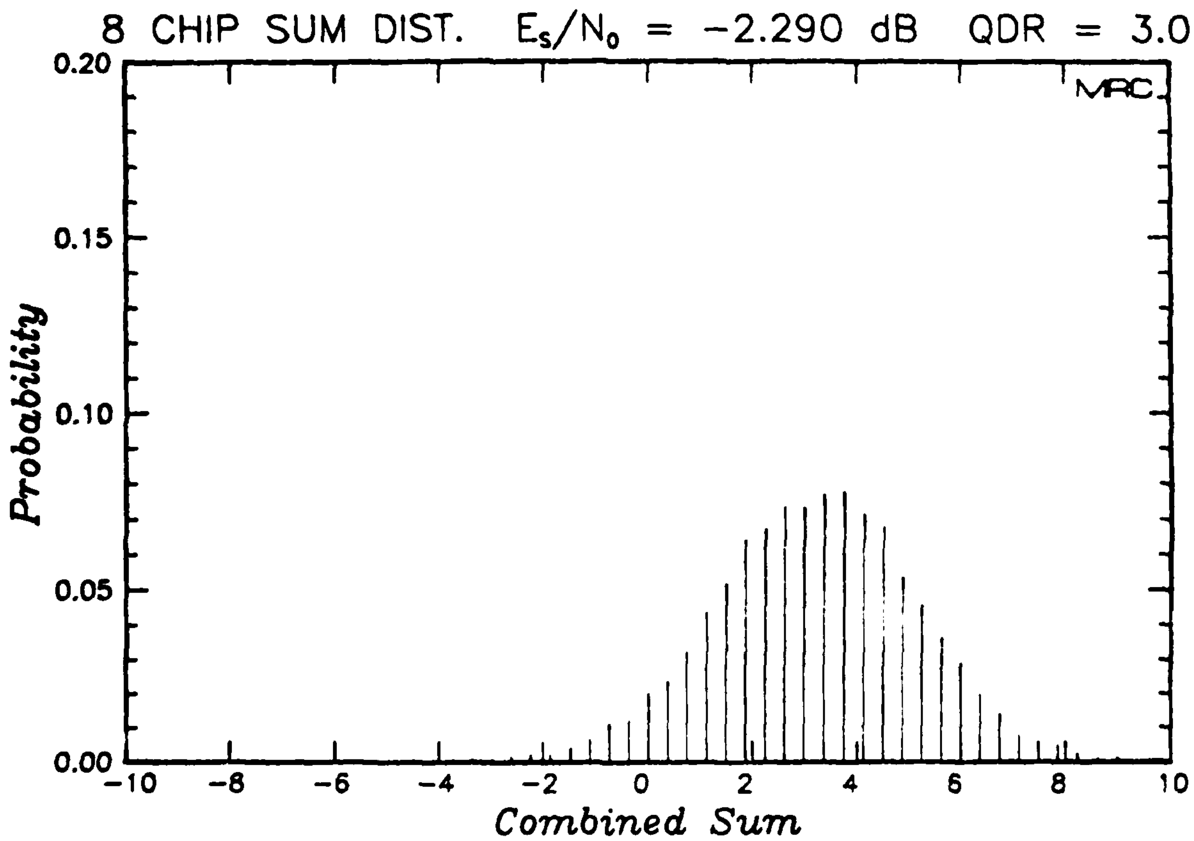


Figure 83. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 3.0. (Applicable to Link 1)

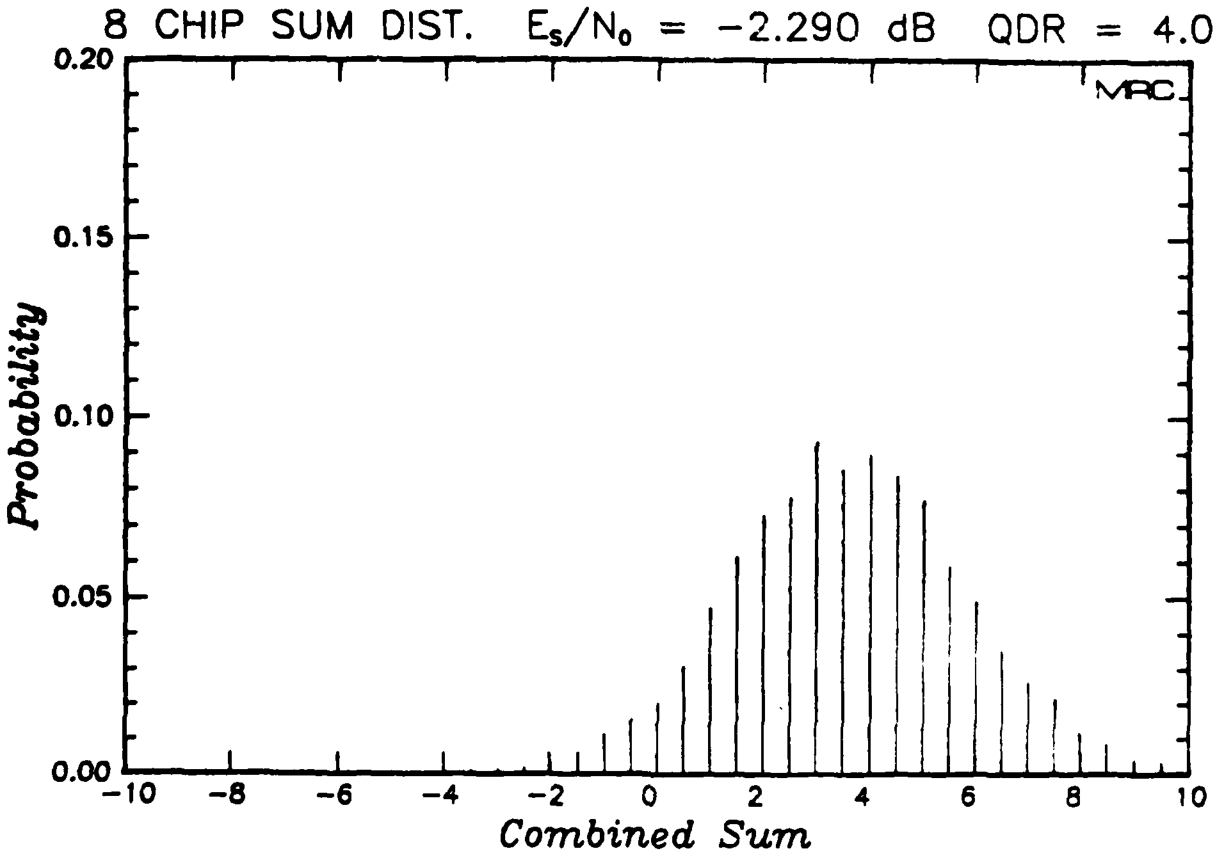


Figure 84. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_O = -2.290 and normalized QDR of 4.0. (Applicable to Link 1)

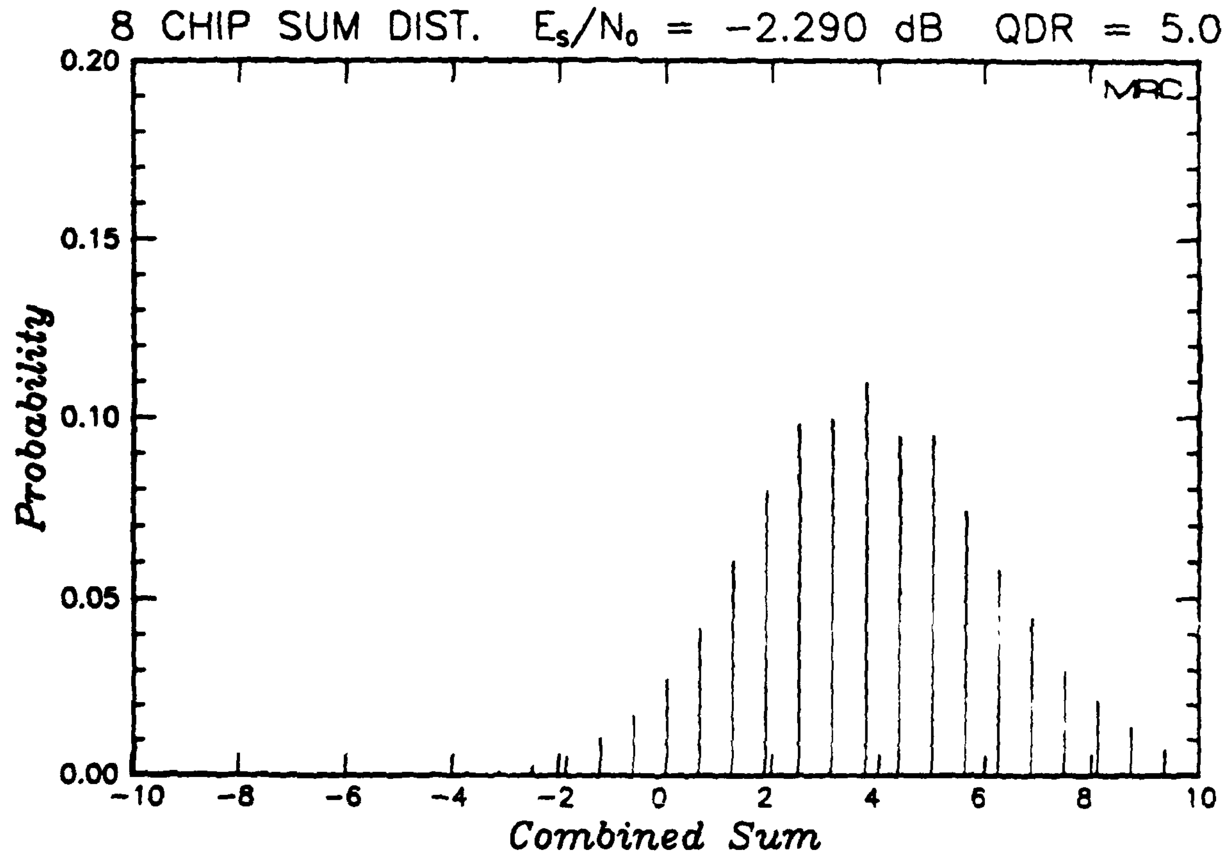


Figure 85. Measured probability distribution of the eight-chip combined quantized symbols under benign channel conditions for E_S/N_0 = -2.290 and normalized QDR of 5.0. (Applicable to Link 1)

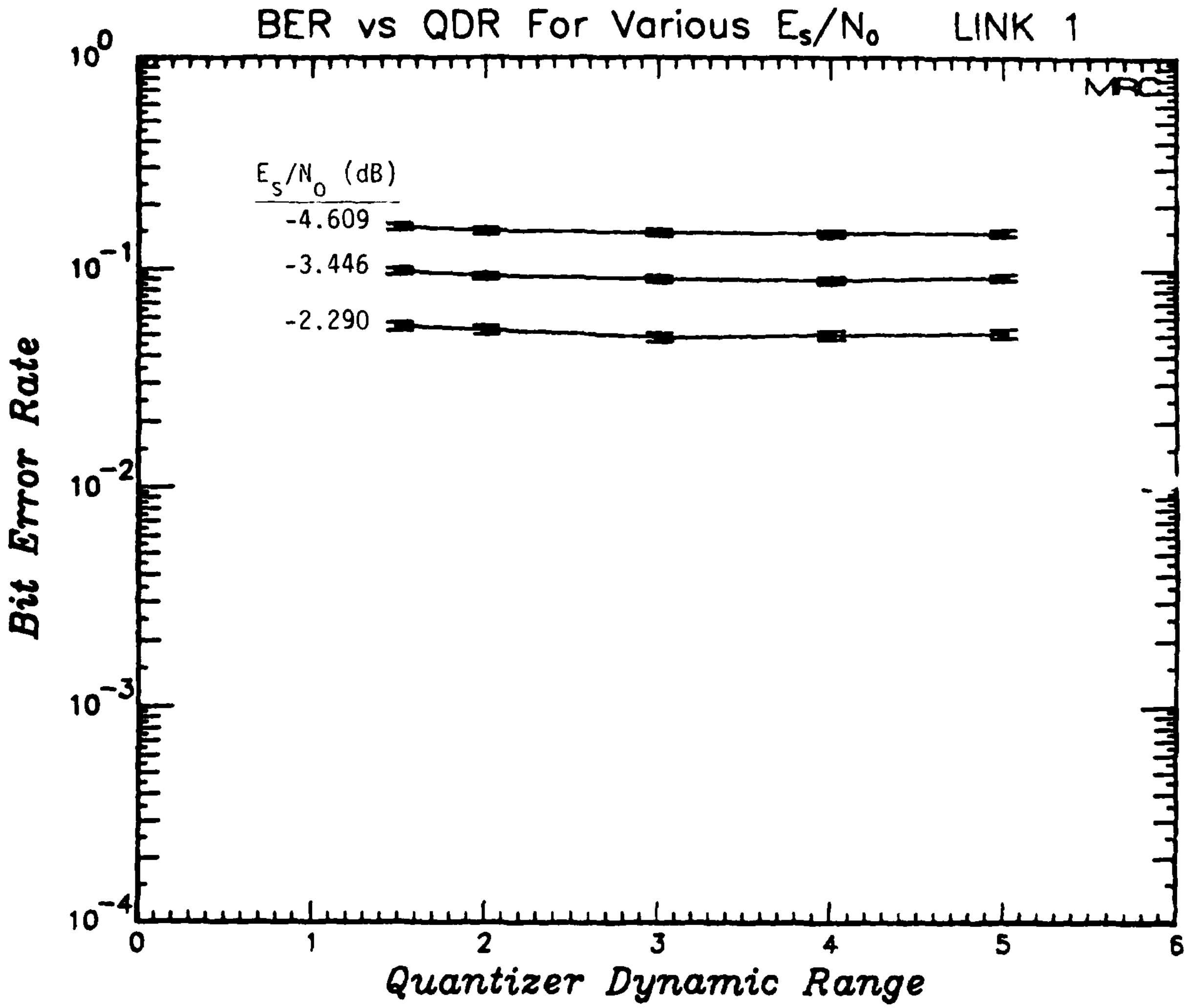


Figure 86. Information bit error rate for Link 1 under benign channel conditions versus normalized QDR for the values of E_S/N_O.

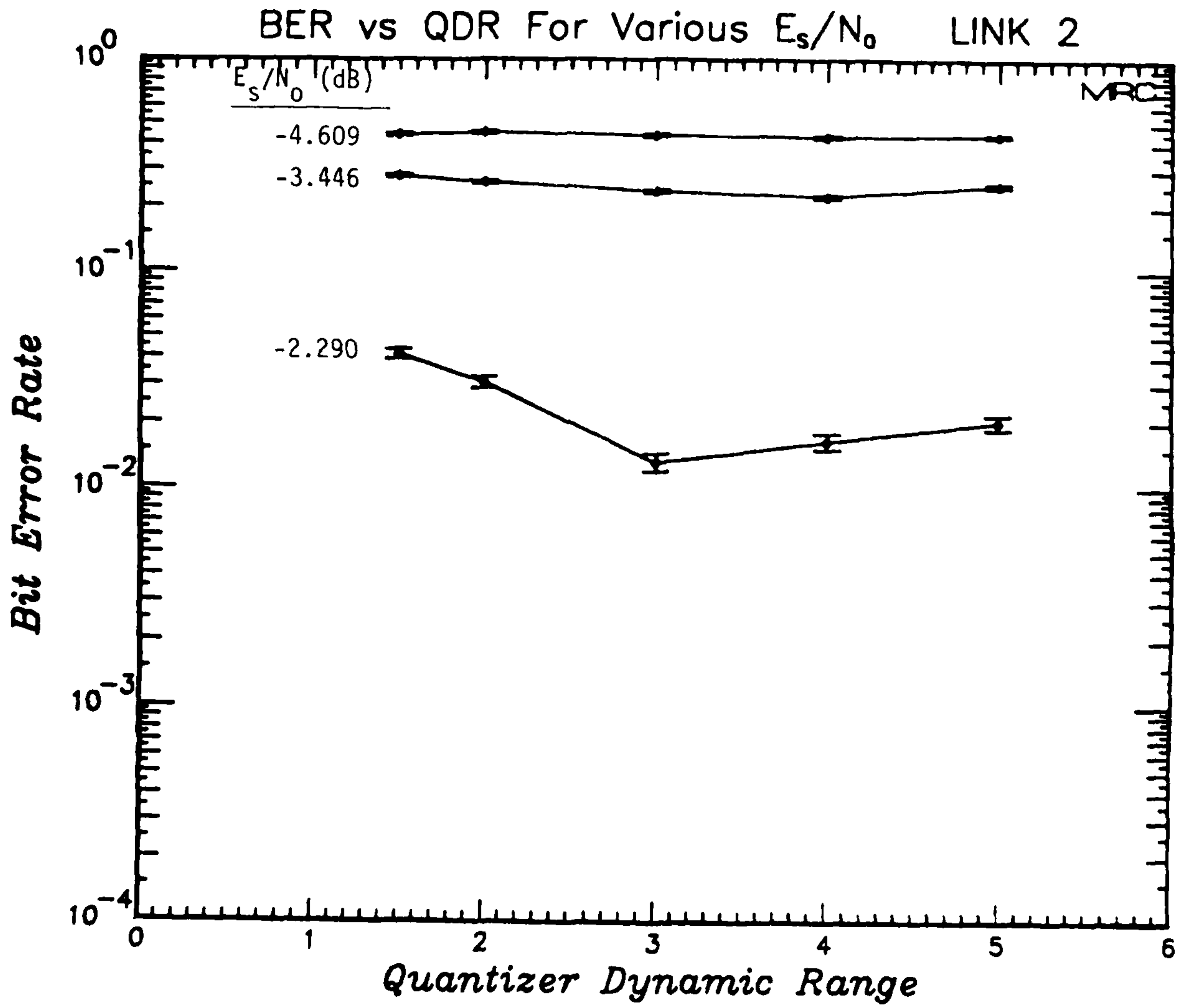


Figure 87. Information bit error rate for Link 2 under benign channel conditions versus normalized QDR for the values of E_s/N_o.

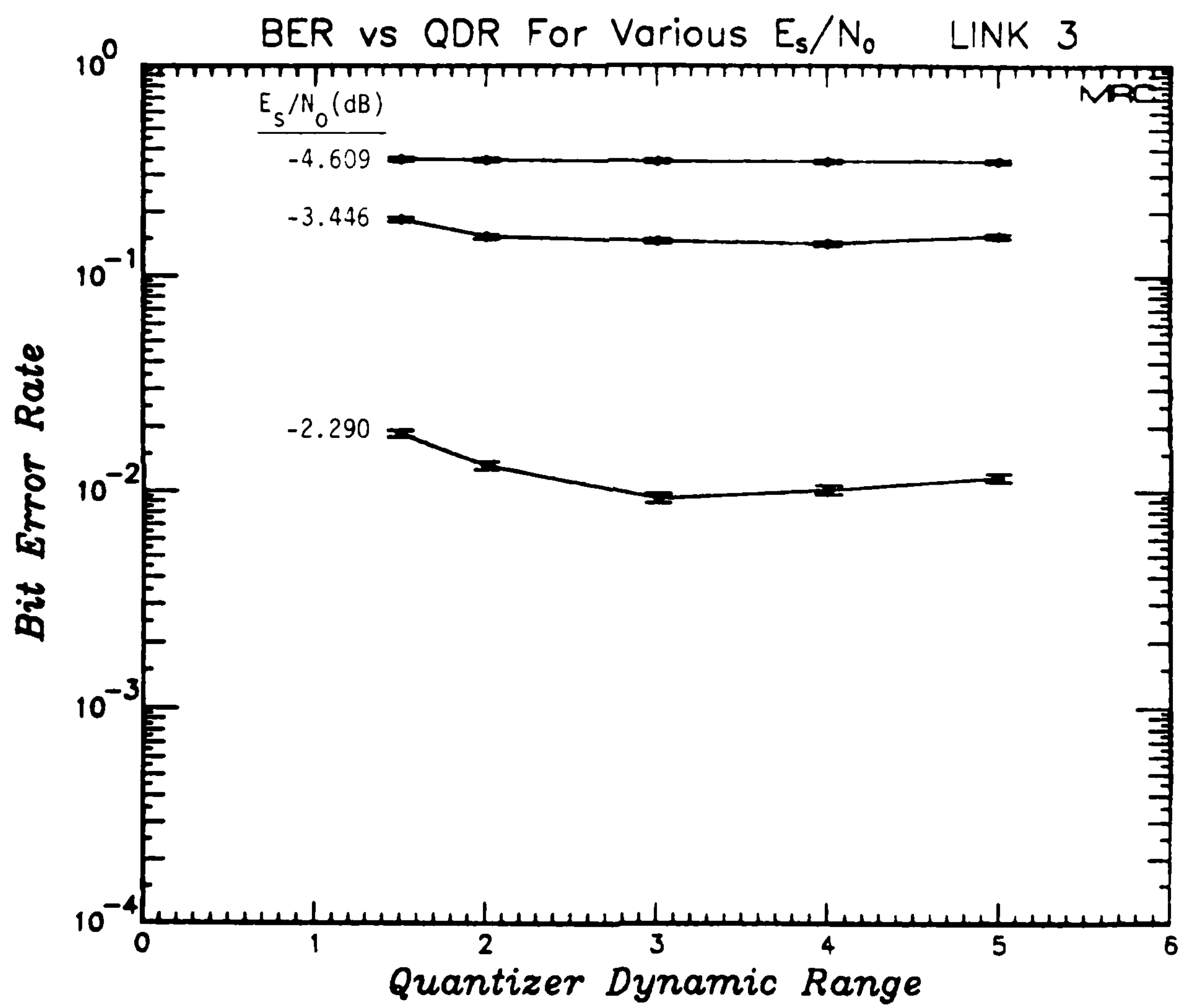


Figure 88. Information bit error rate for Link 3 under benign channel conditions versus normalized QDR for the values of E_s/N_0.

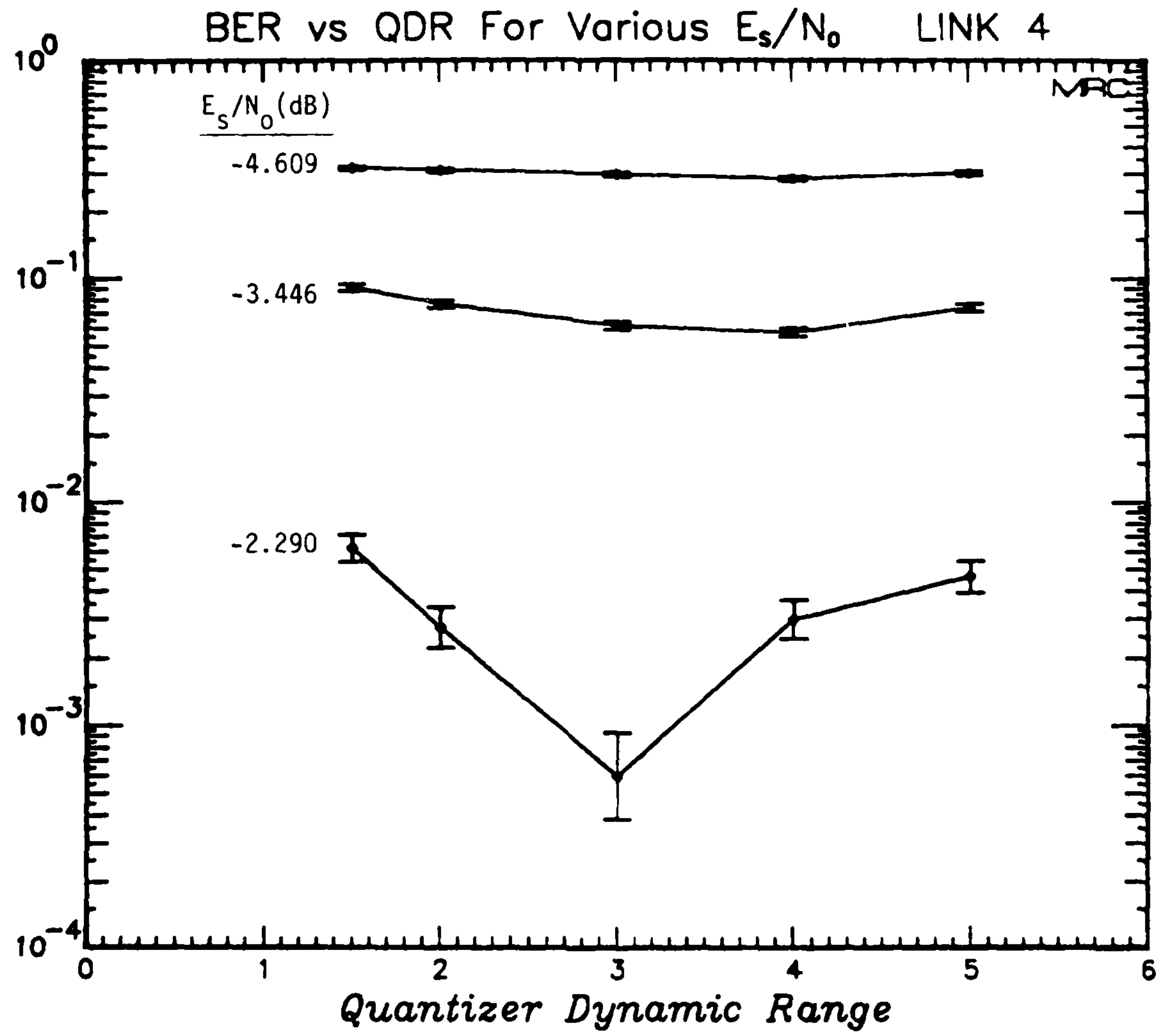


Figure 89. Information bit error rate for Link 4 under benign channel conditions versus normalized QDR for the values of E_S/N_O.

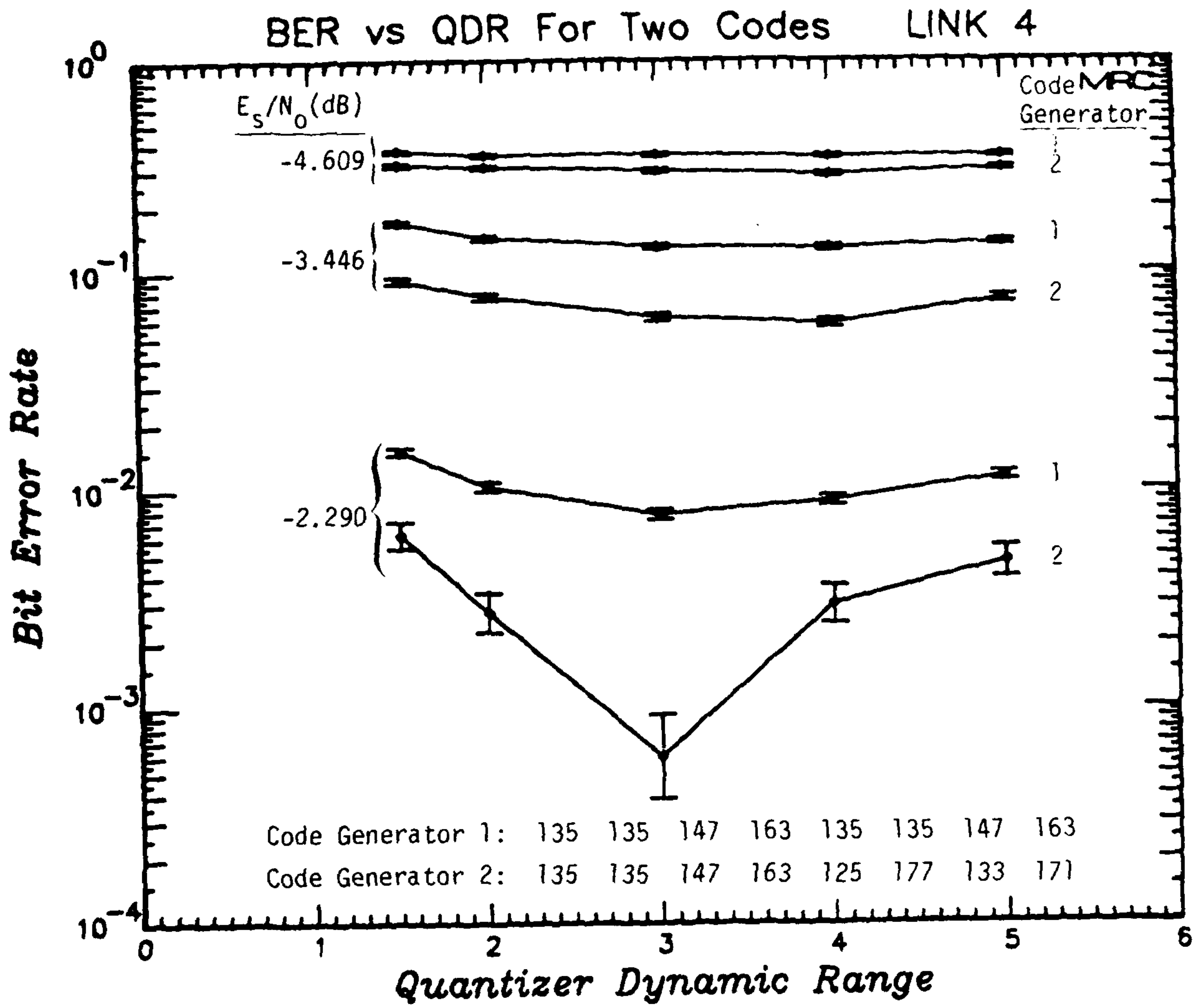


Figure 90. Performance comparison of two rate 1/8, constraint length 7 convolutional codes with df of 40 utilized in Link 4 under benign channel conditions versus normalized QDR for the values of E_S/N_O.

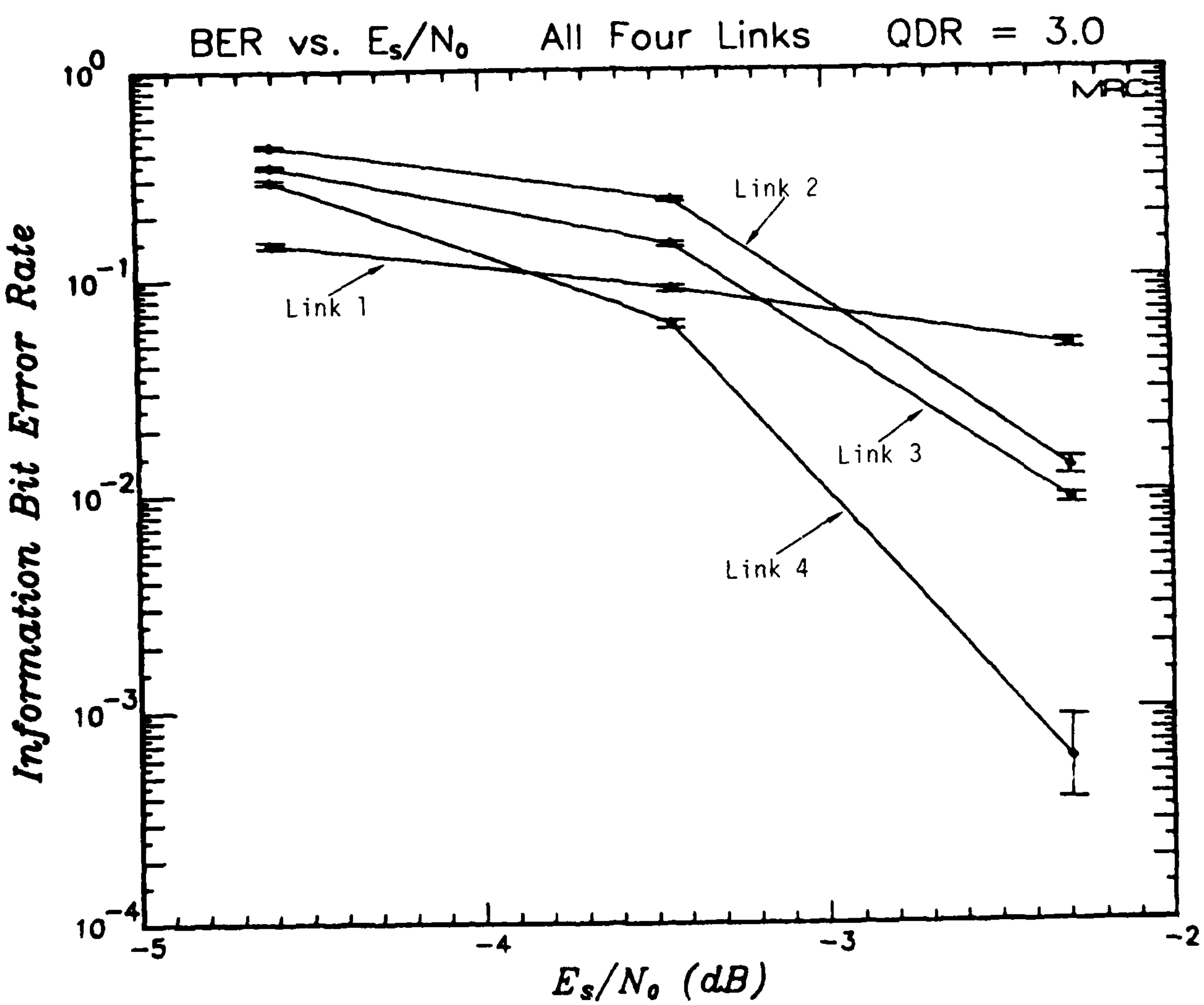


Figure 91. Information bit error rate for all links under benign channel conditions versus E_s/N_0 for QDR = 3.0.

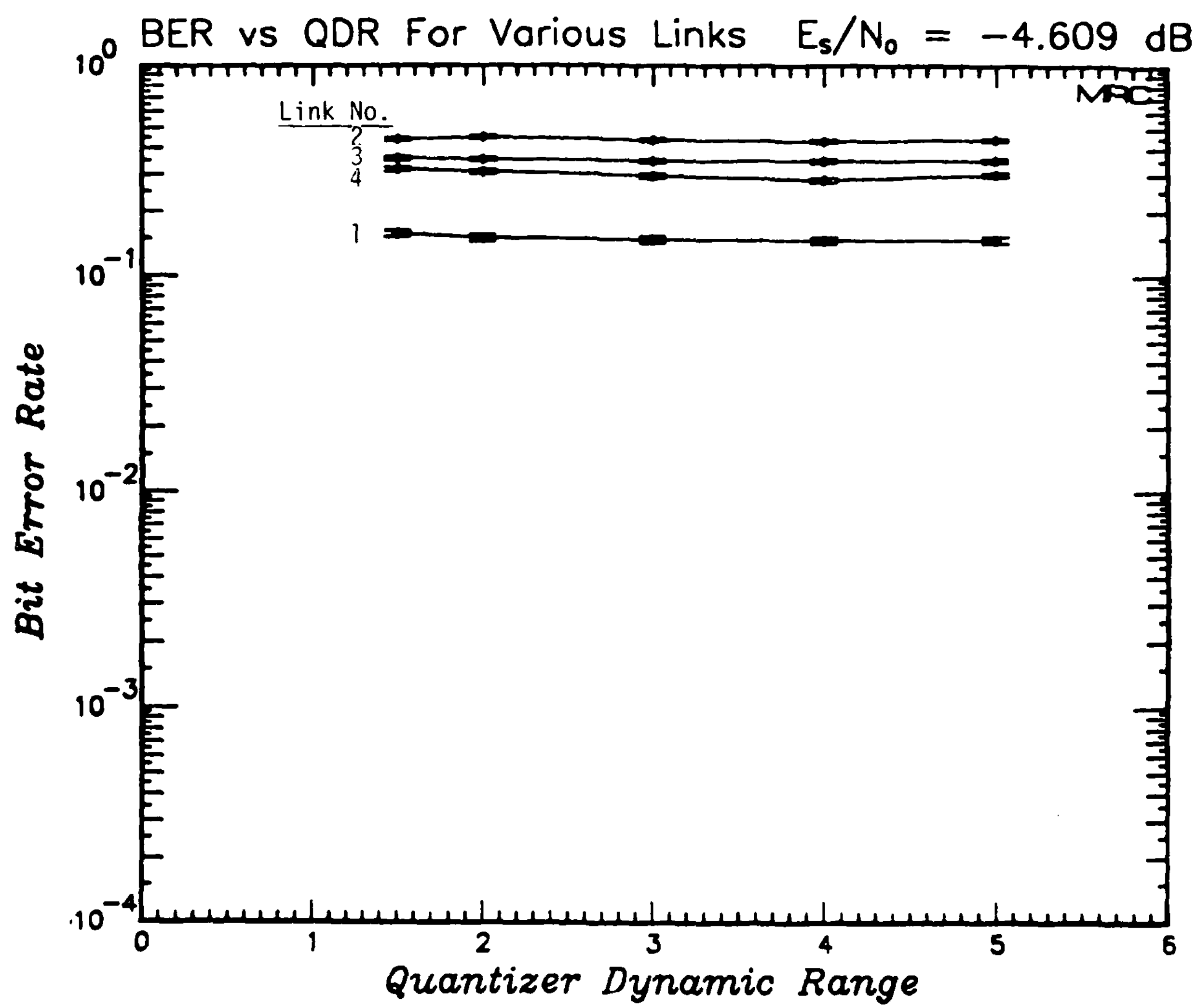


Figure 92. Information bit error rate for all links under benign channel conditions versus normalized QDR for E_S/N_O = -4.609.

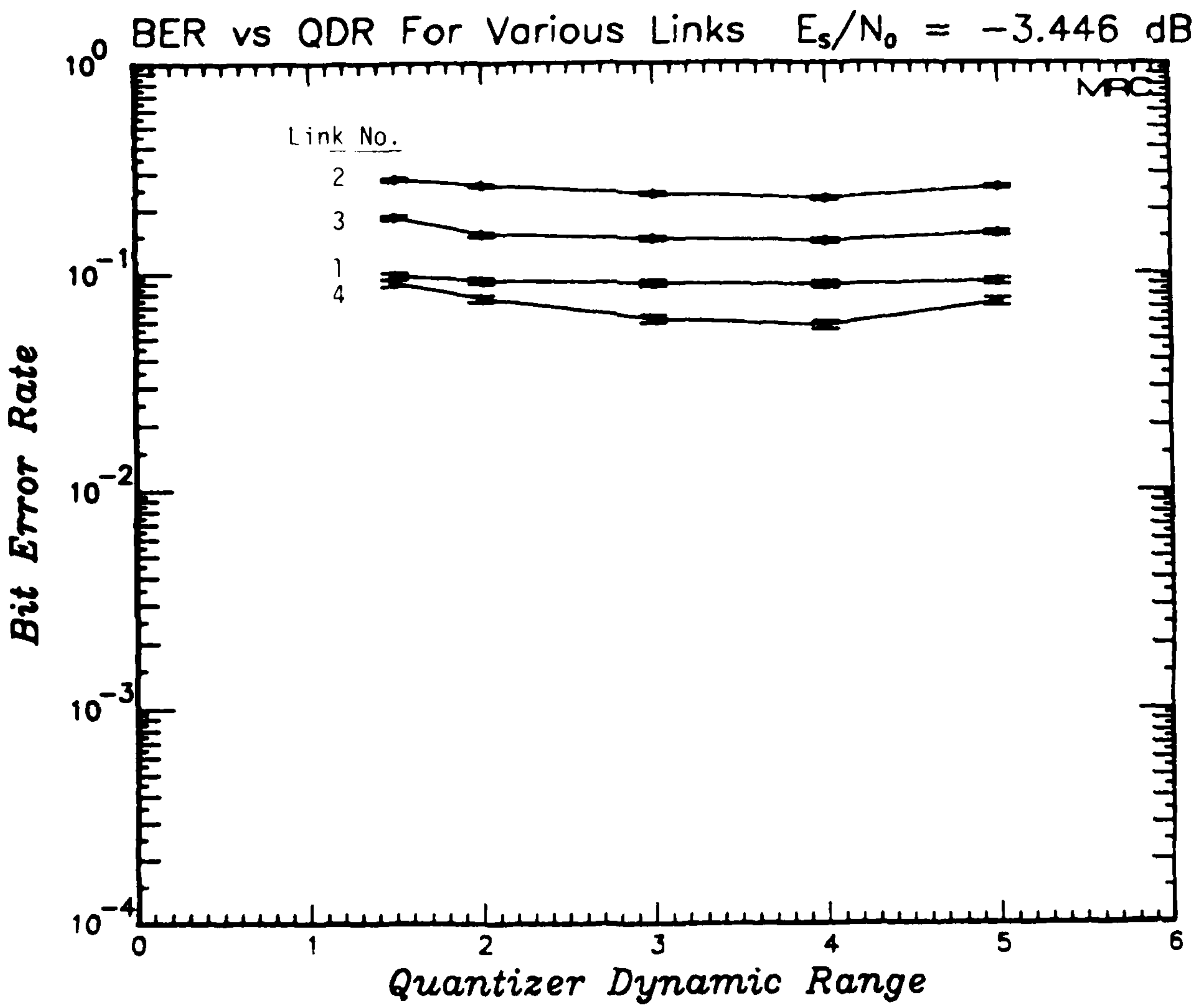


Figure 93. Information bit error rate for all links under benign channel conditions versus normalized QDR for E_S/N_O = -3.446.

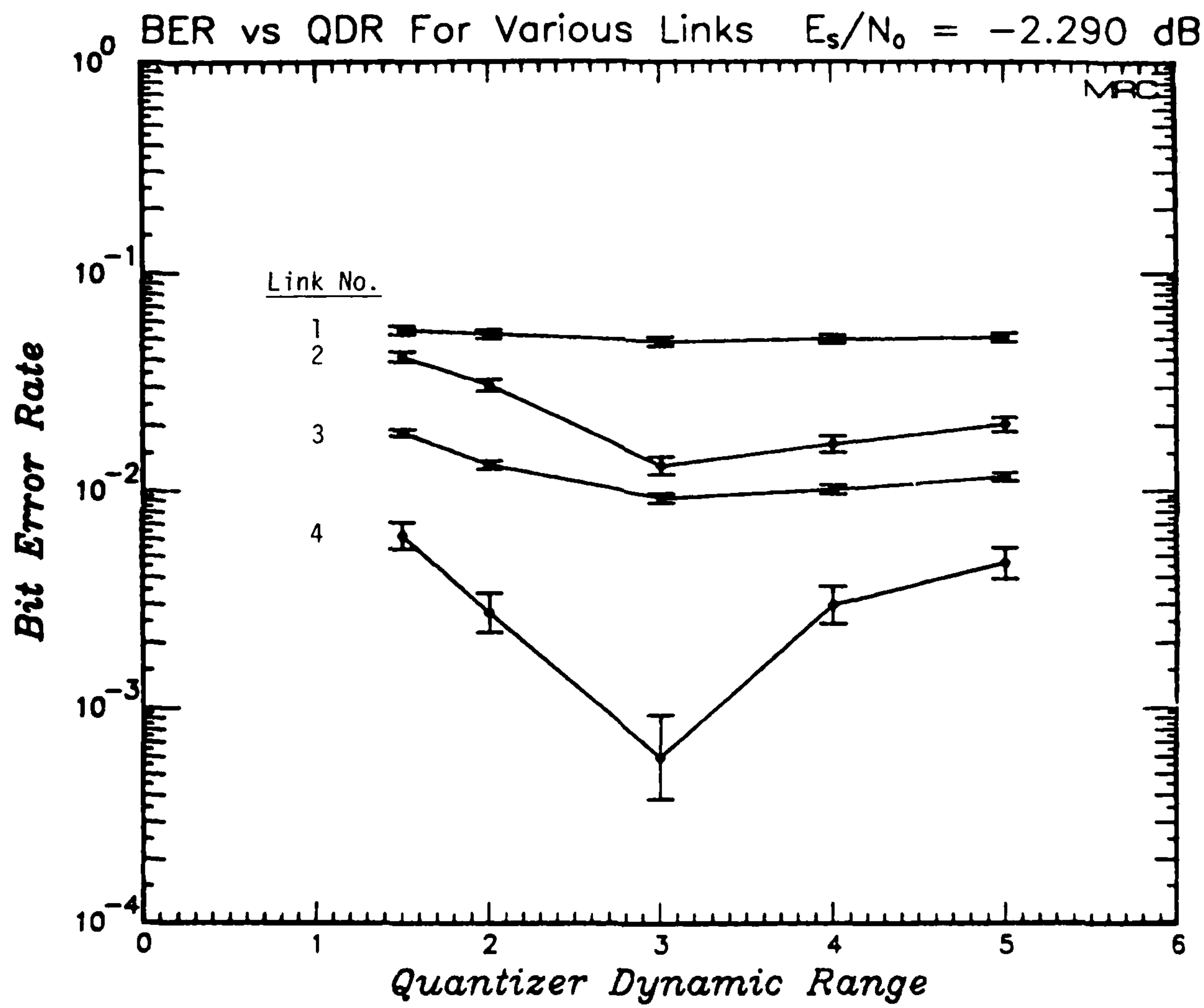


Figure 94. Information bit error rate for all links under benign channel conditions versus normalized QDR for E_S/N_O = -2.290.

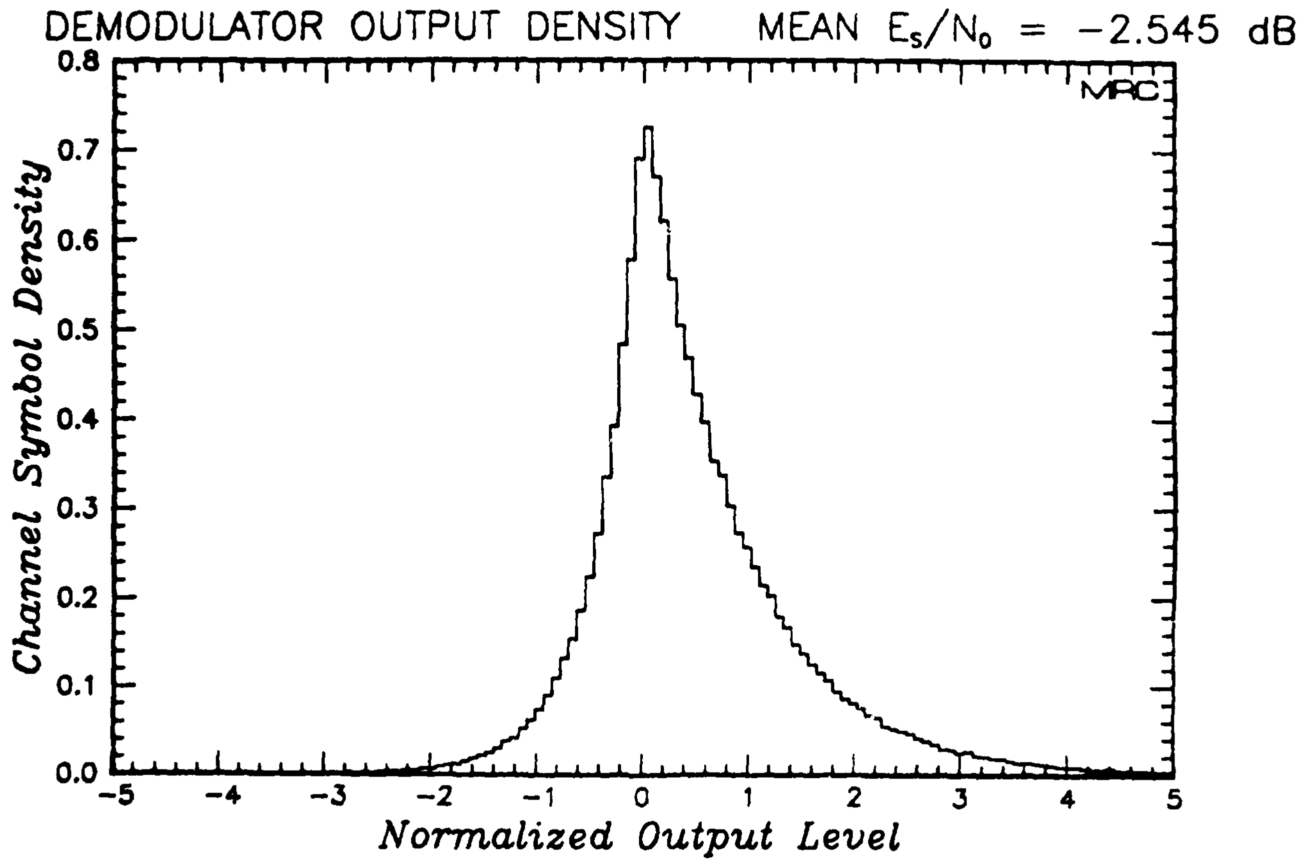


Figure 95. Histogram of demodulator outputs under fading channel concitions for τ_0 = 0.1 second and E_s/N_0 = -2.545 dB.

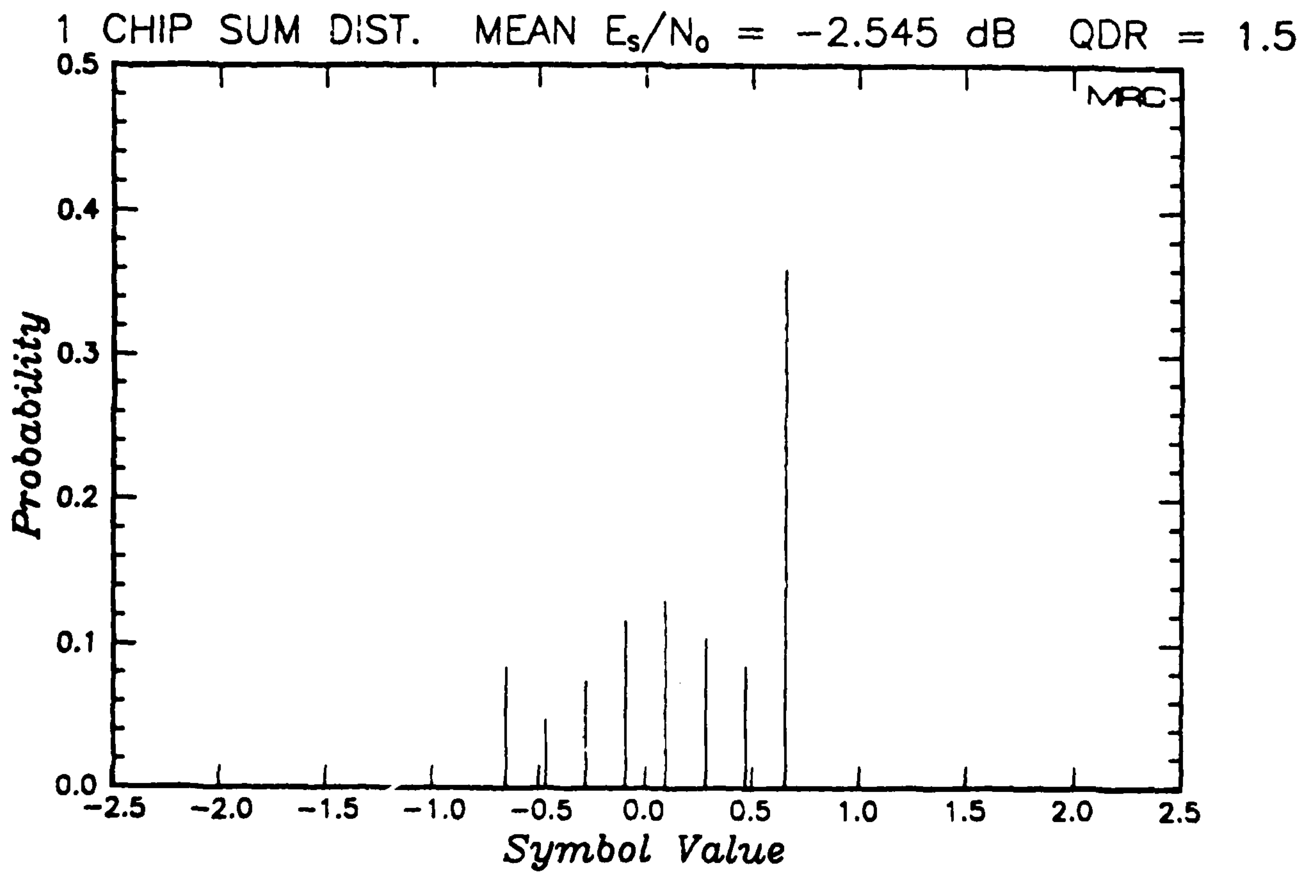


Figure 96. Measured probability distribution of quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -2.545 and normalized QDR of 1.5. (Applicable to Link 4)

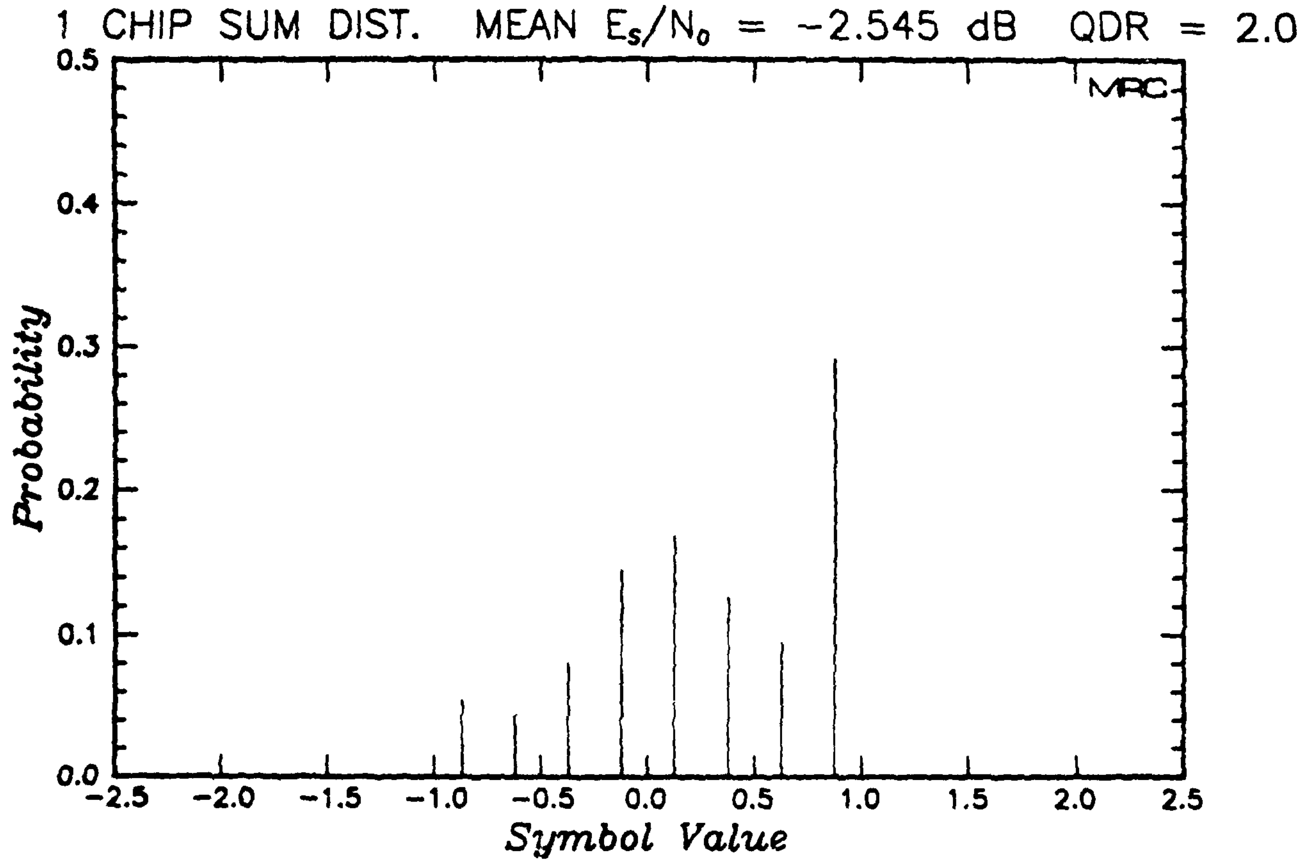


Figure 97. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -2.545 and normalized QDR of 2.0. (Applicable to Link 4)

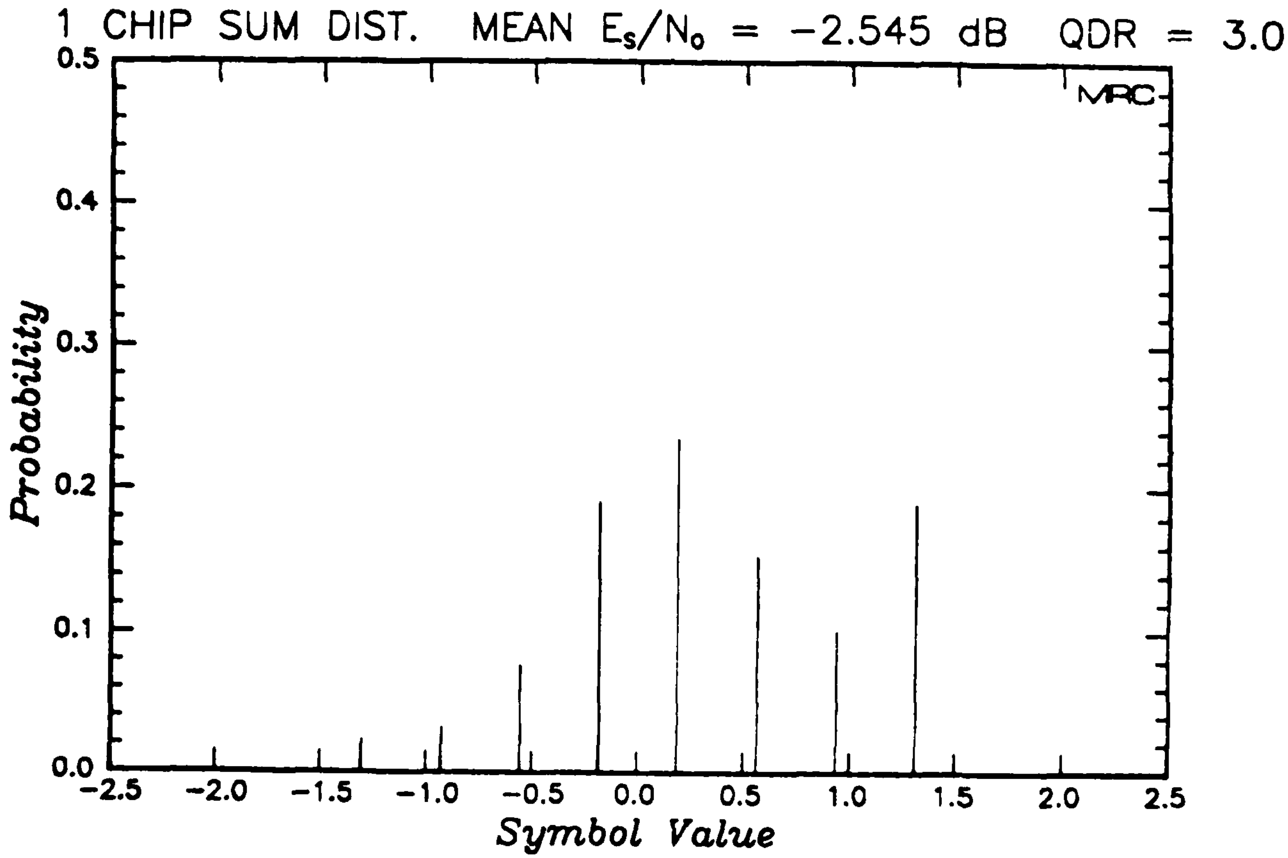


Figure 98. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 3.0. (Applicable to Link 4)

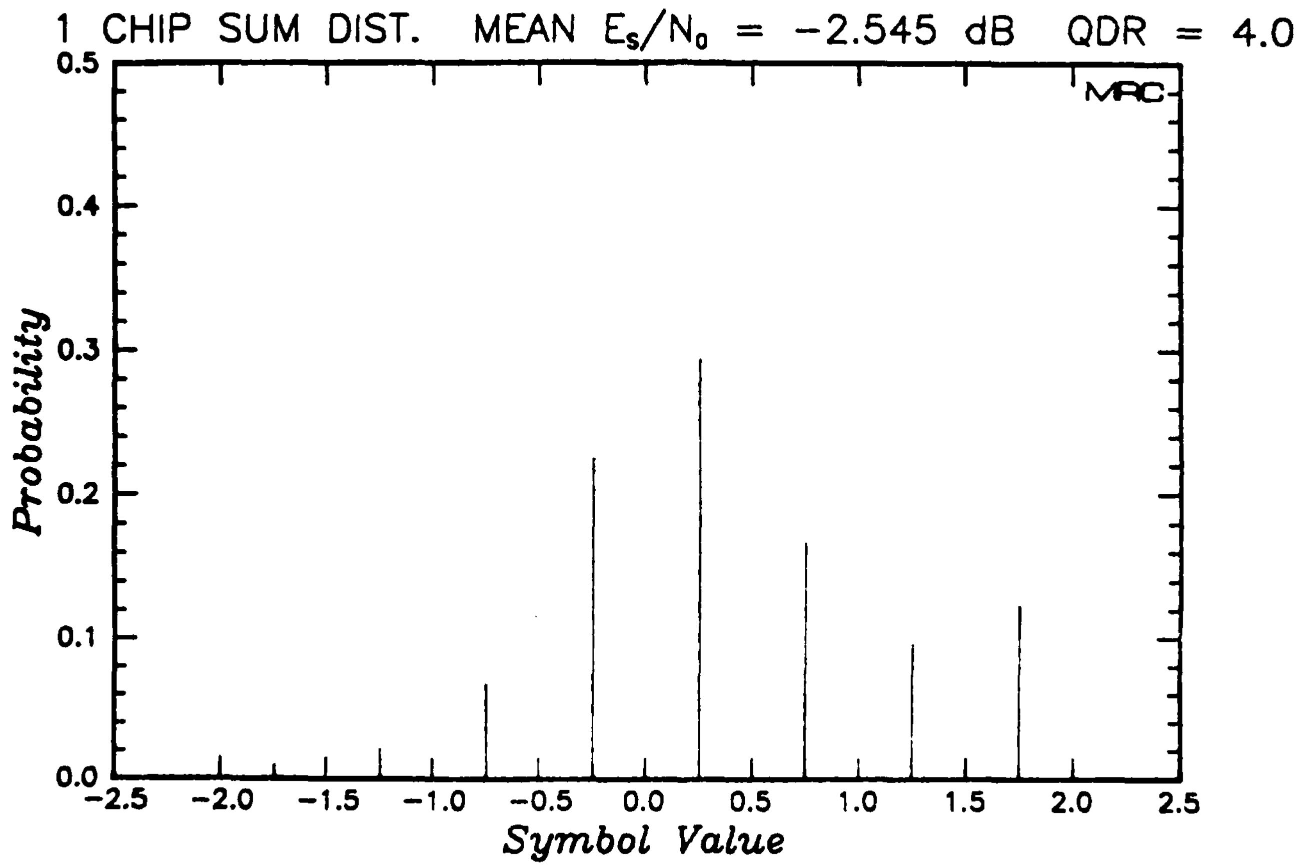


Figure 99. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -2.545 and normalized QDR of 4.0. (Applicable to Link 4)

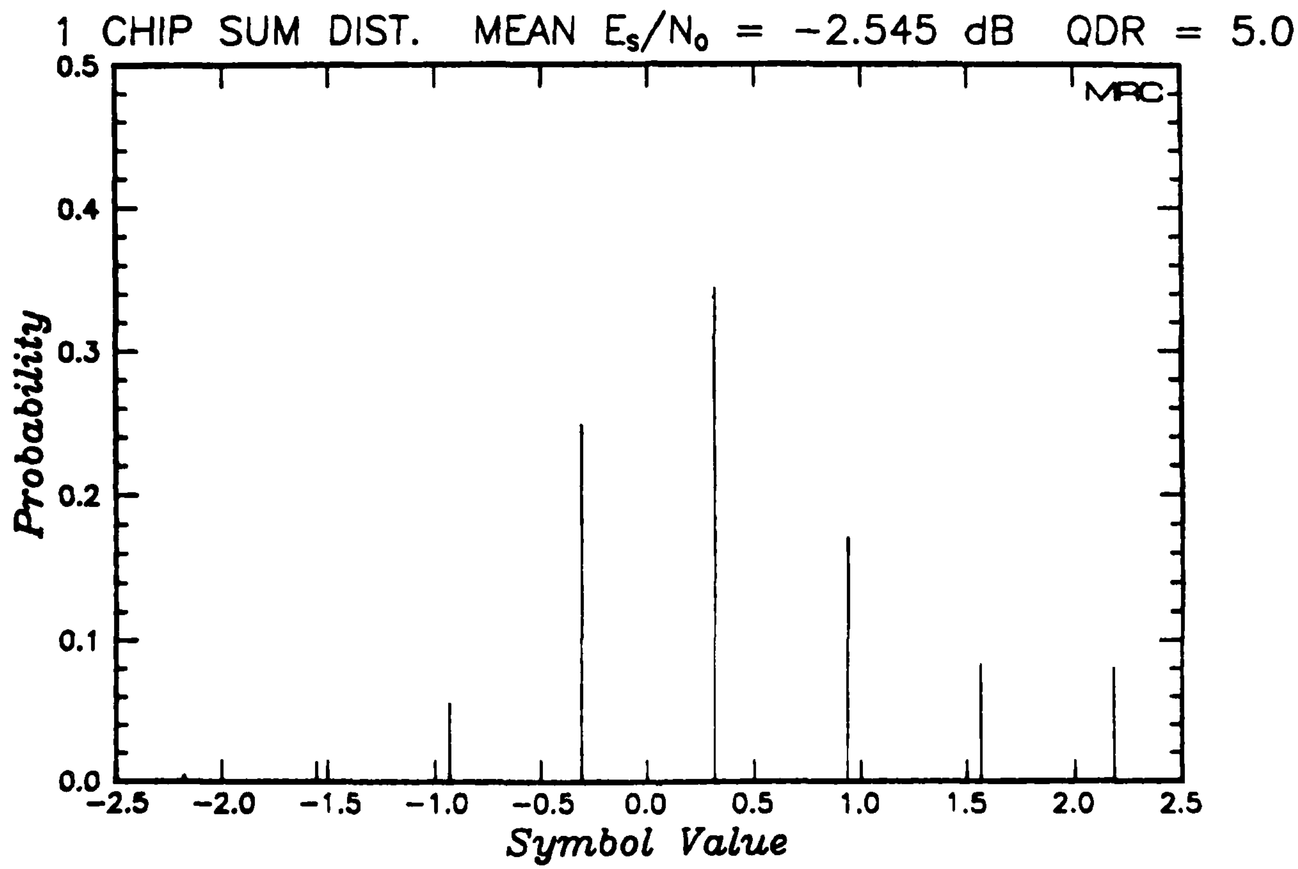


Figure 100. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 5.0. (Applicable to Link 4)

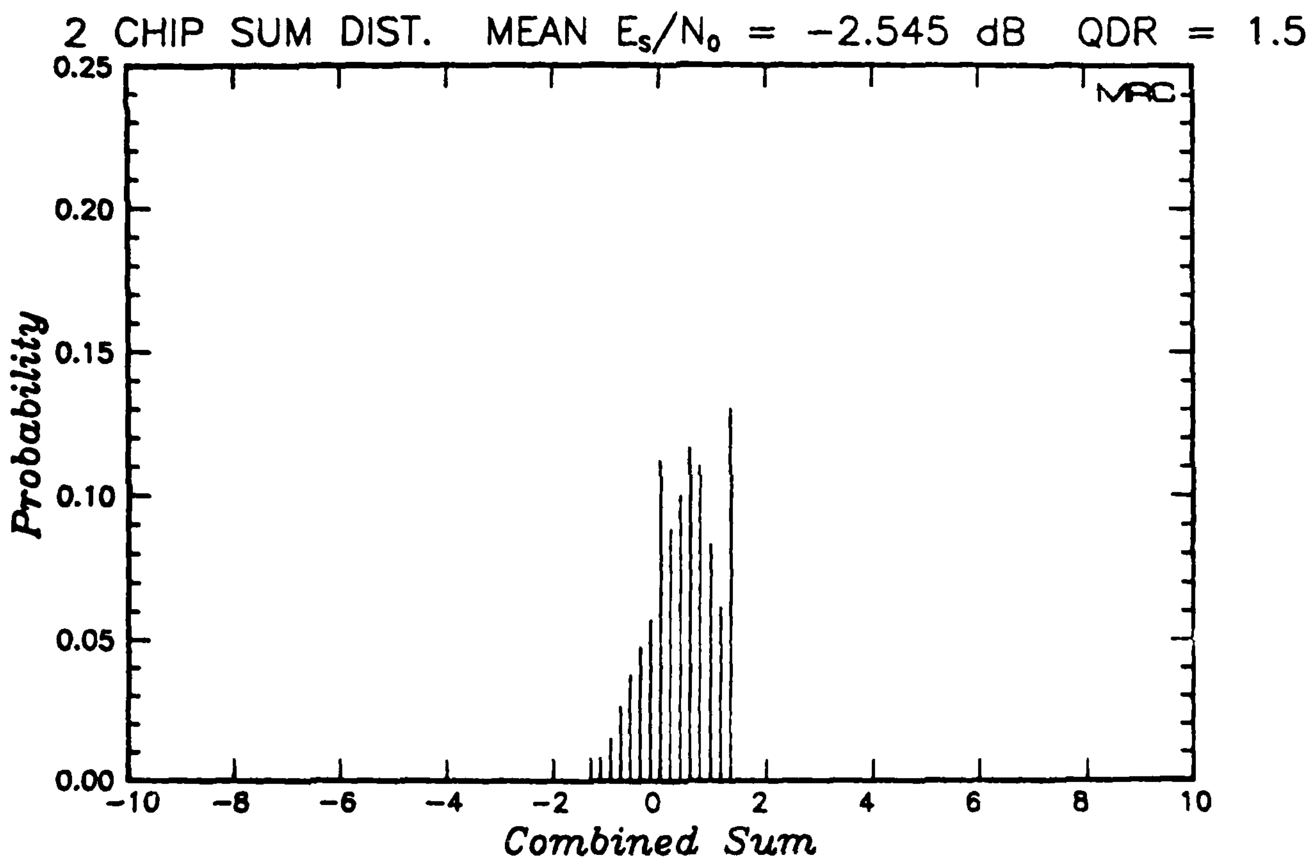


Figure 101. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_o = -2.545 and normalized QDR of 1.5. (Applicable to Link 3)

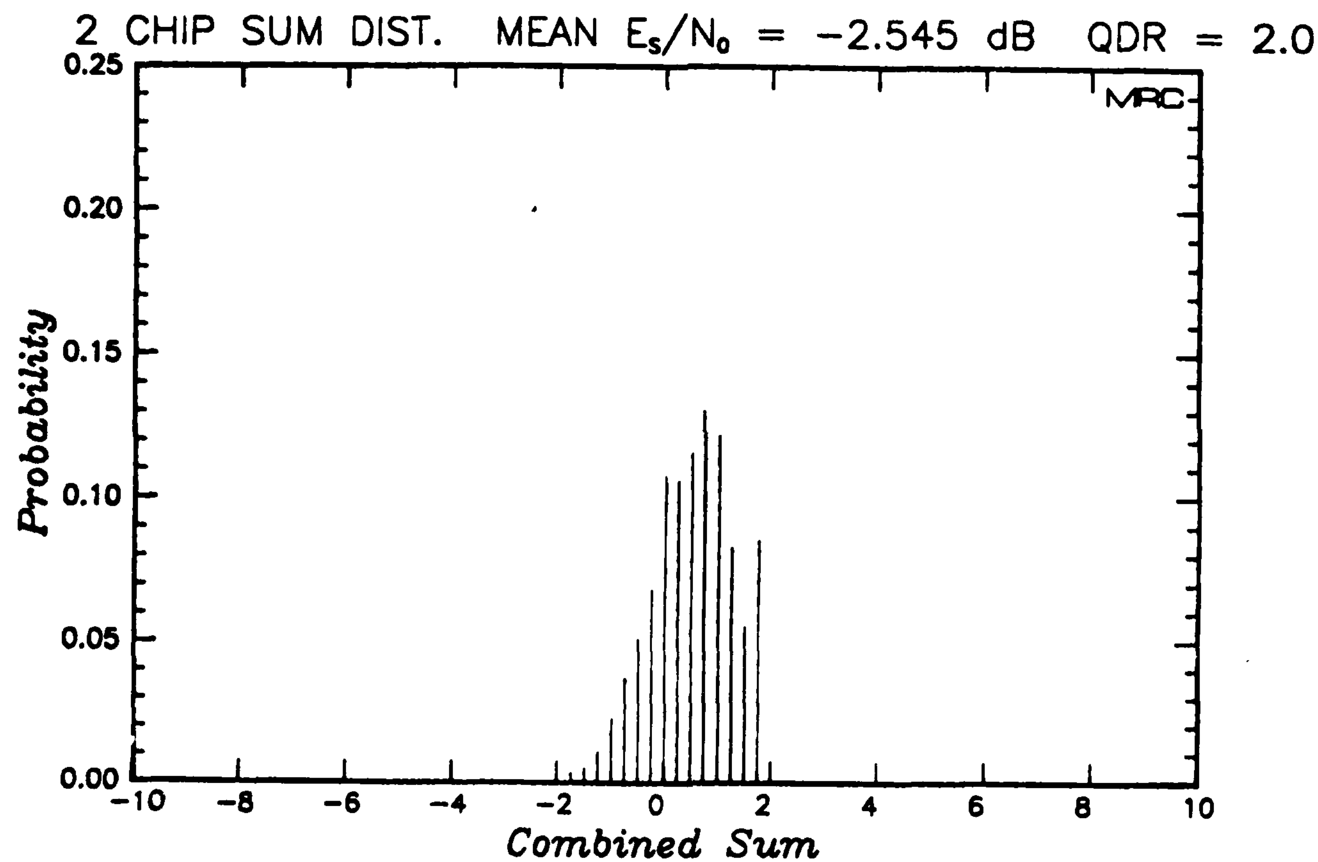


Figure 102. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 2.0. (Applicable to Link 3)

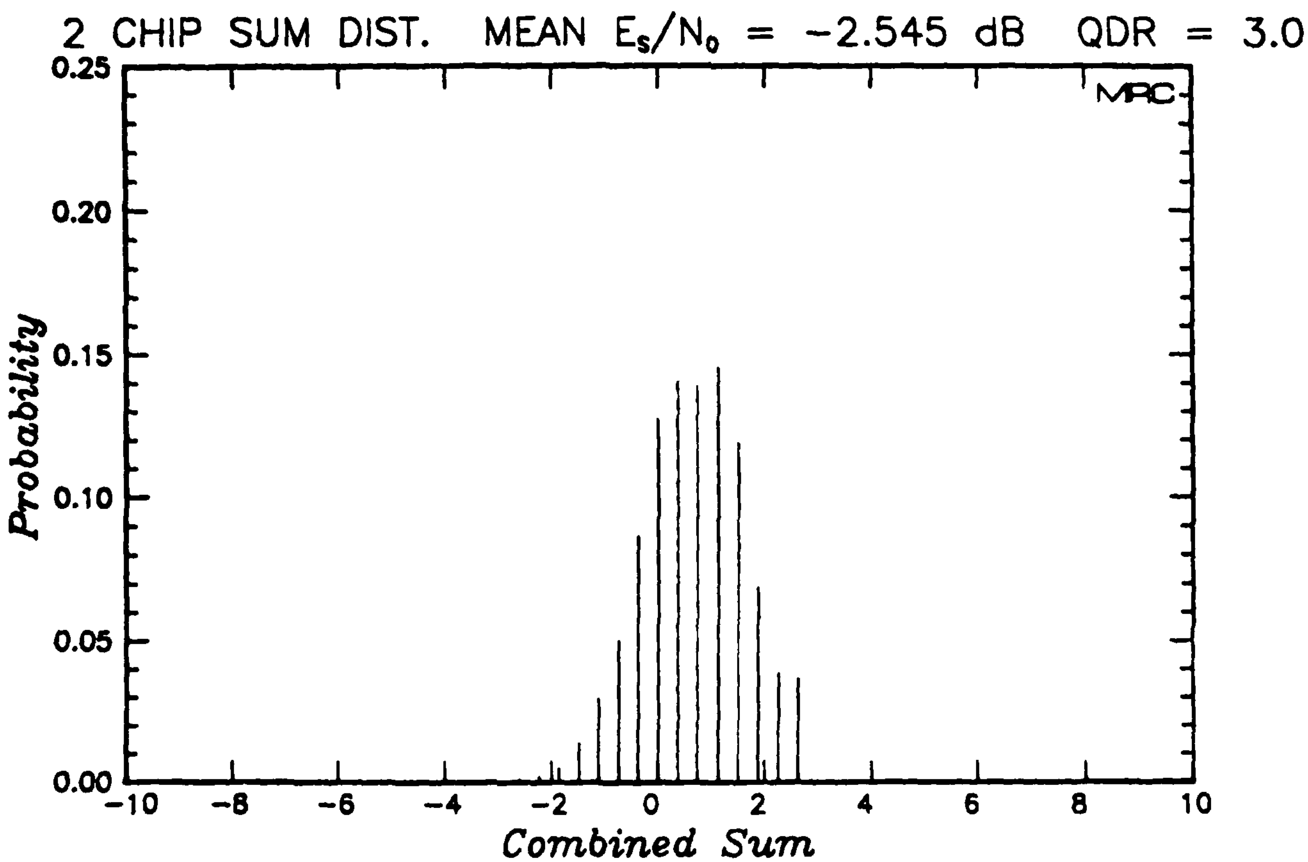


Figure 103. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 3.0. (Applicable to Link 3)

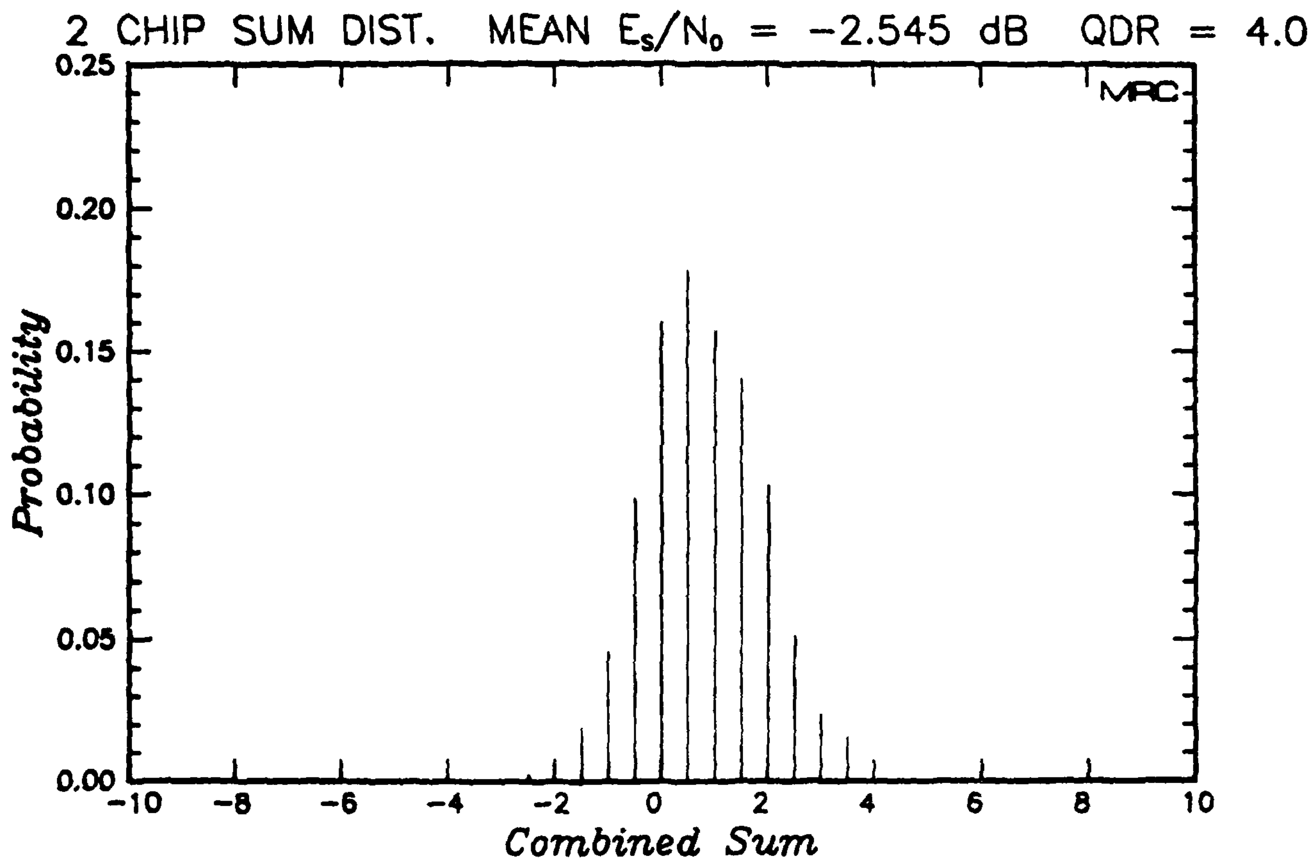


Figure 104. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 4.0. (Applicable to Link 3)

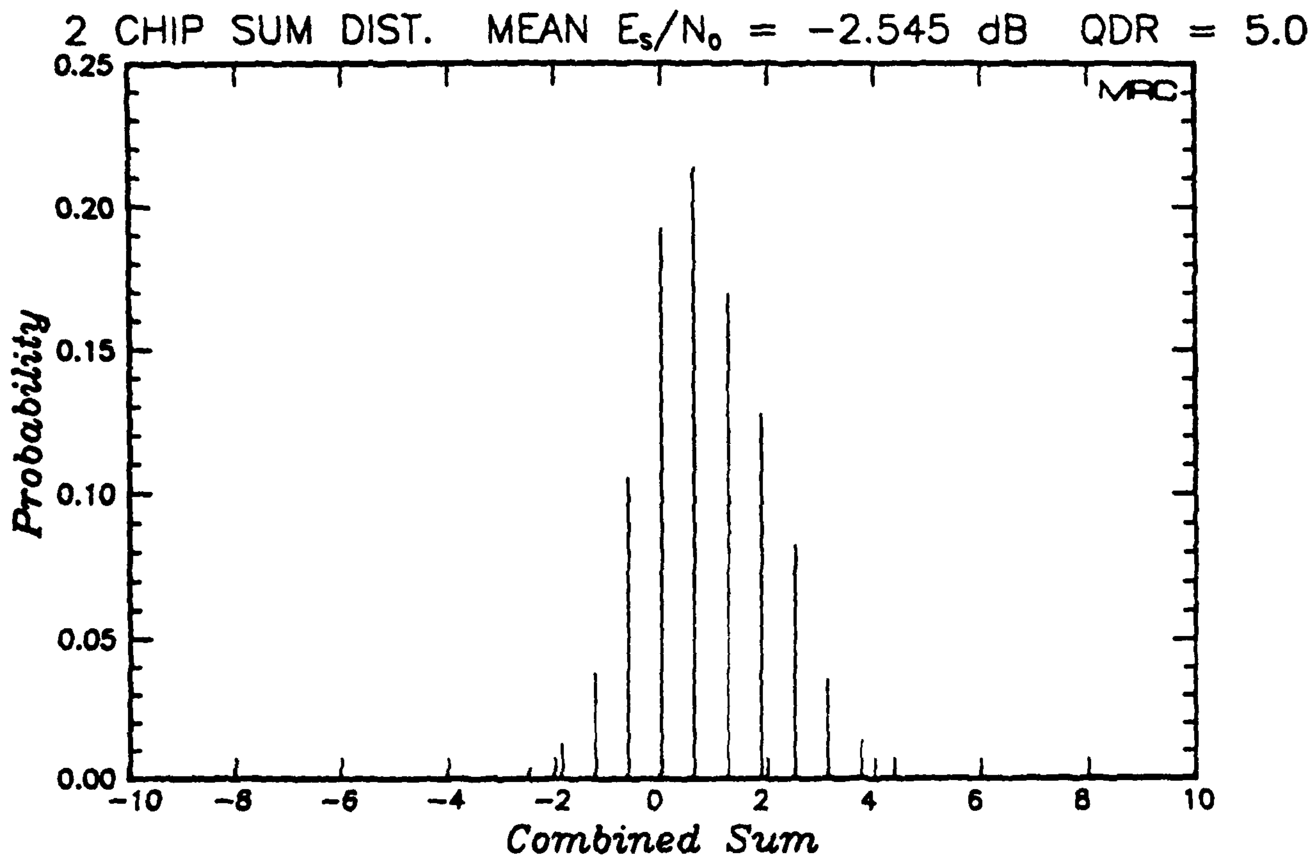


Figure 105. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_o = -2.545 and normalized QDR of 5.0. (Applicable to Link 3)

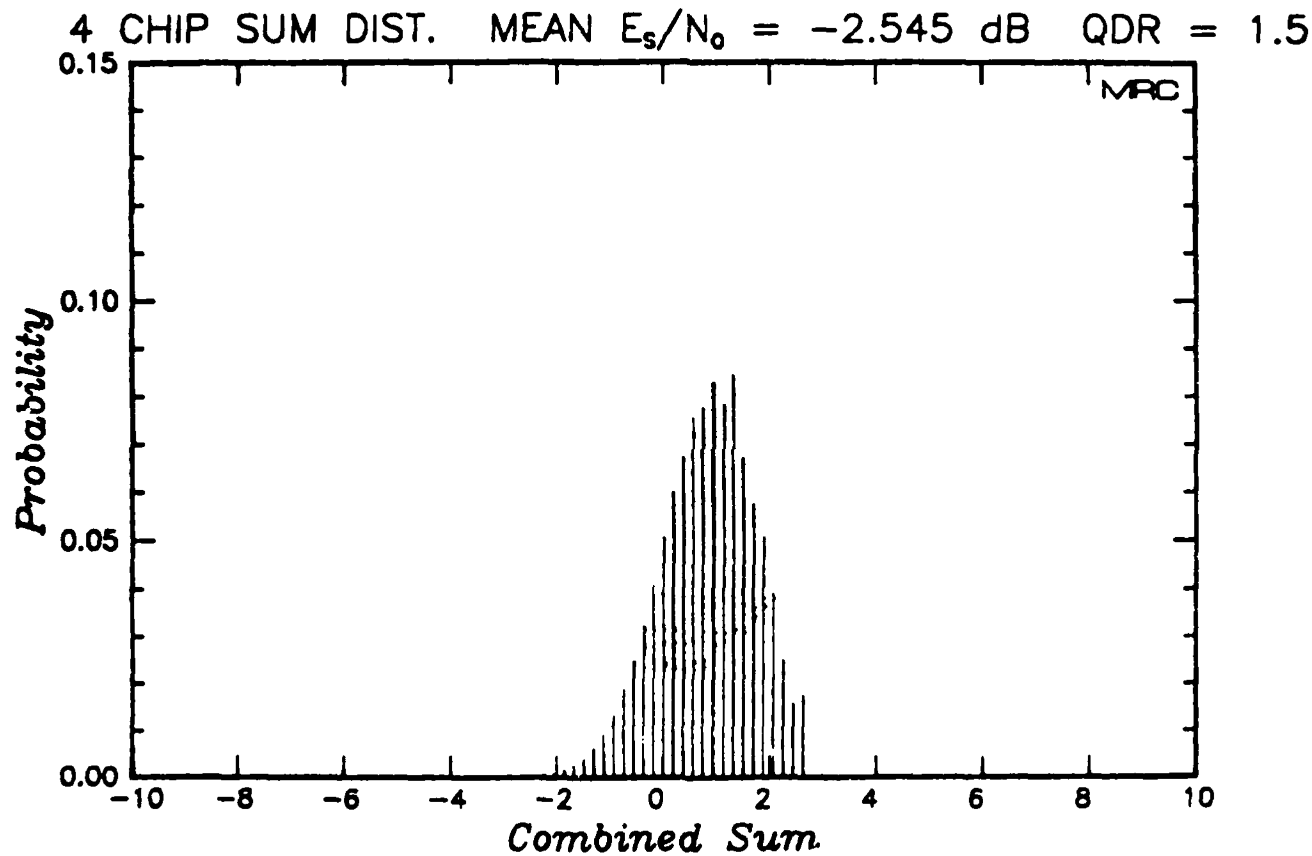


Figure 106. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 1.5. (Applicable to Link 2)

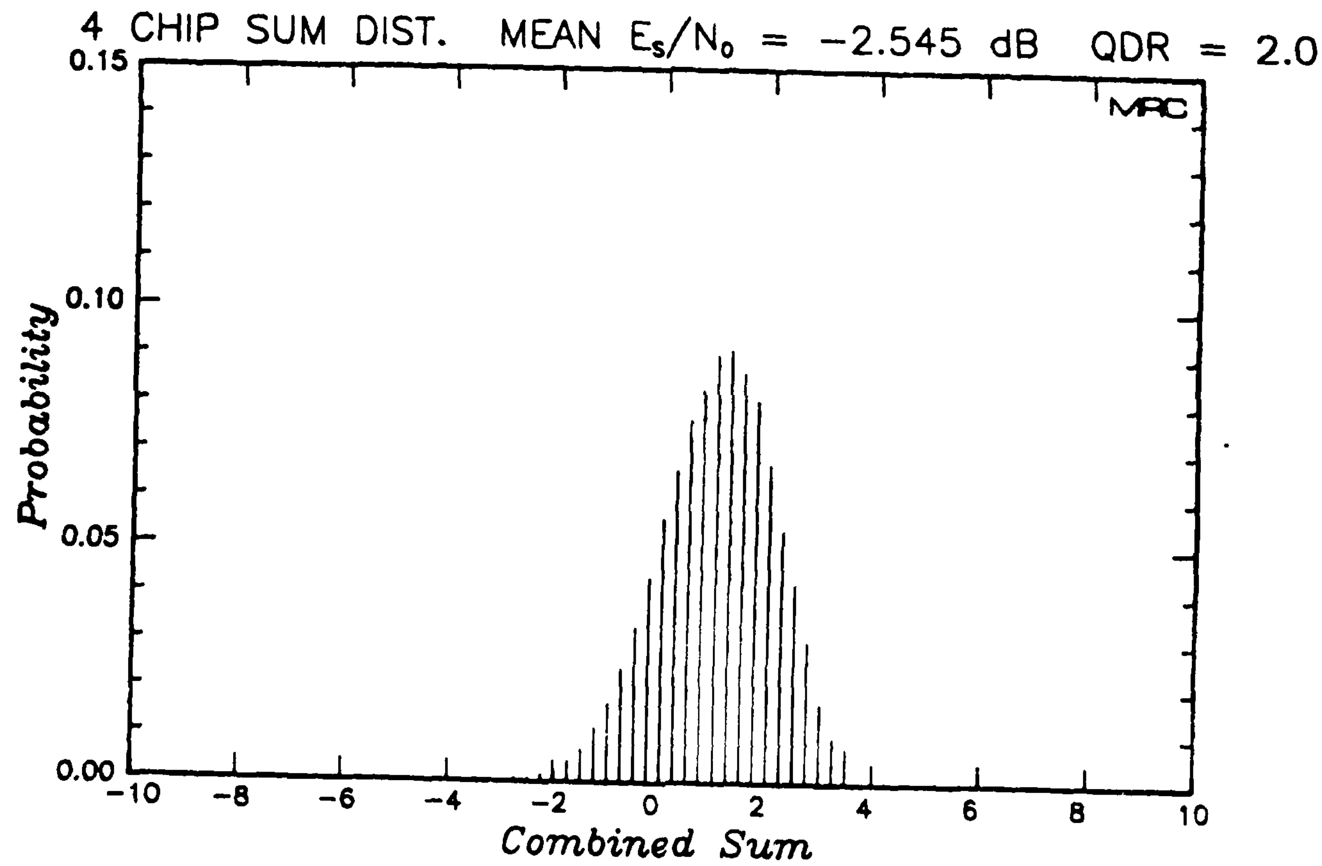


Figure 107. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 2.0. (Applicable to Link 2)

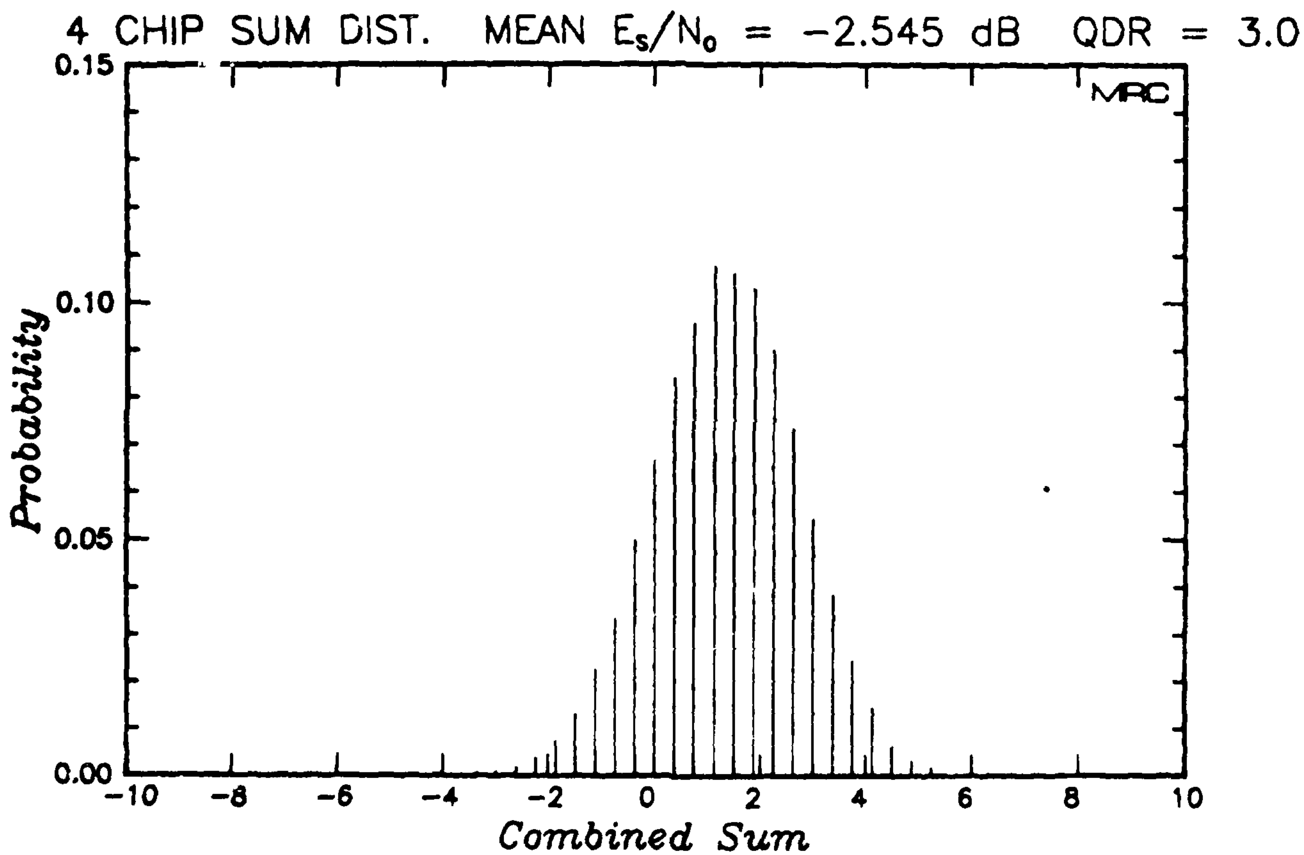
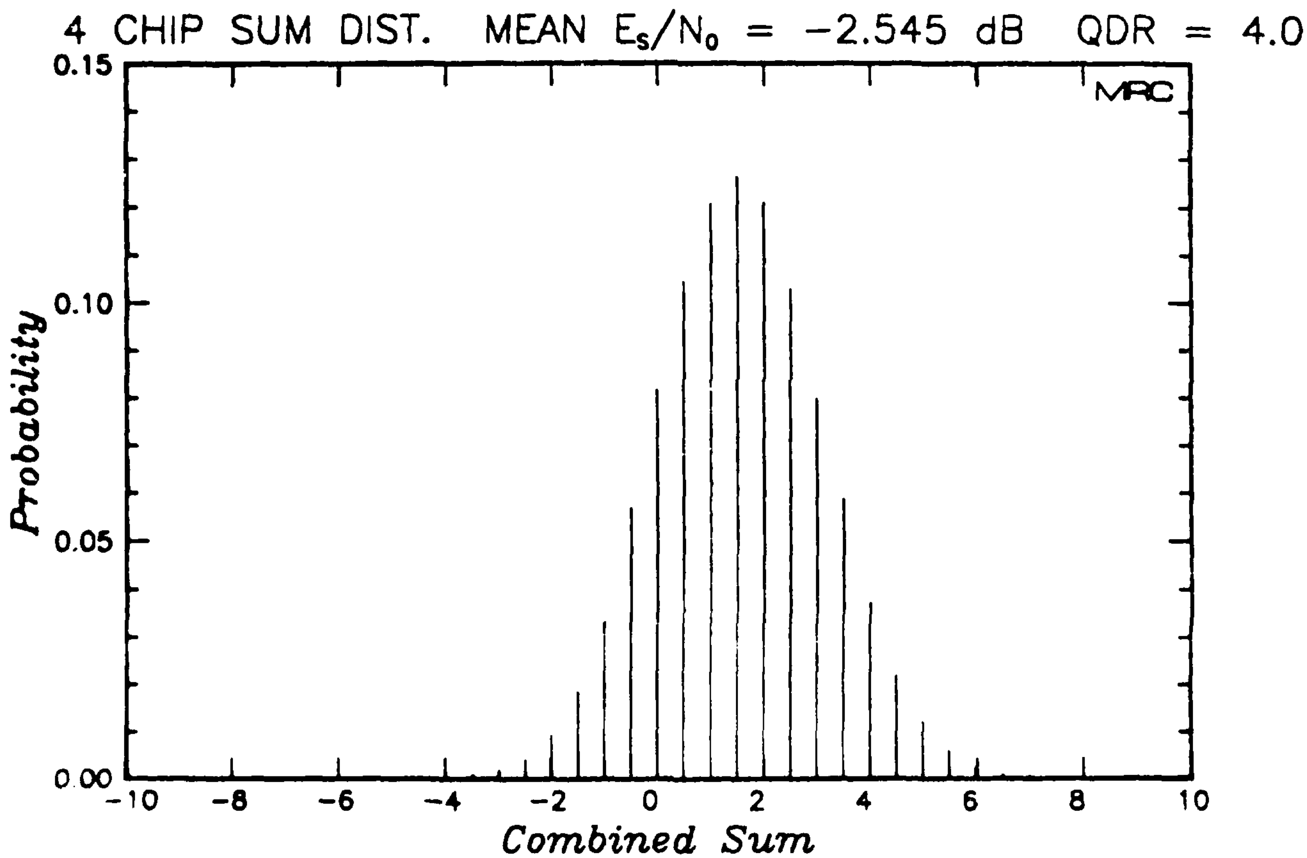


Figure 108. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 3.0. (Applicable to Link 2)



Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = [illegible] second and E_s/N_0 = -2.545 and normalized QDR of 4.0. (Applicable to Link 2)

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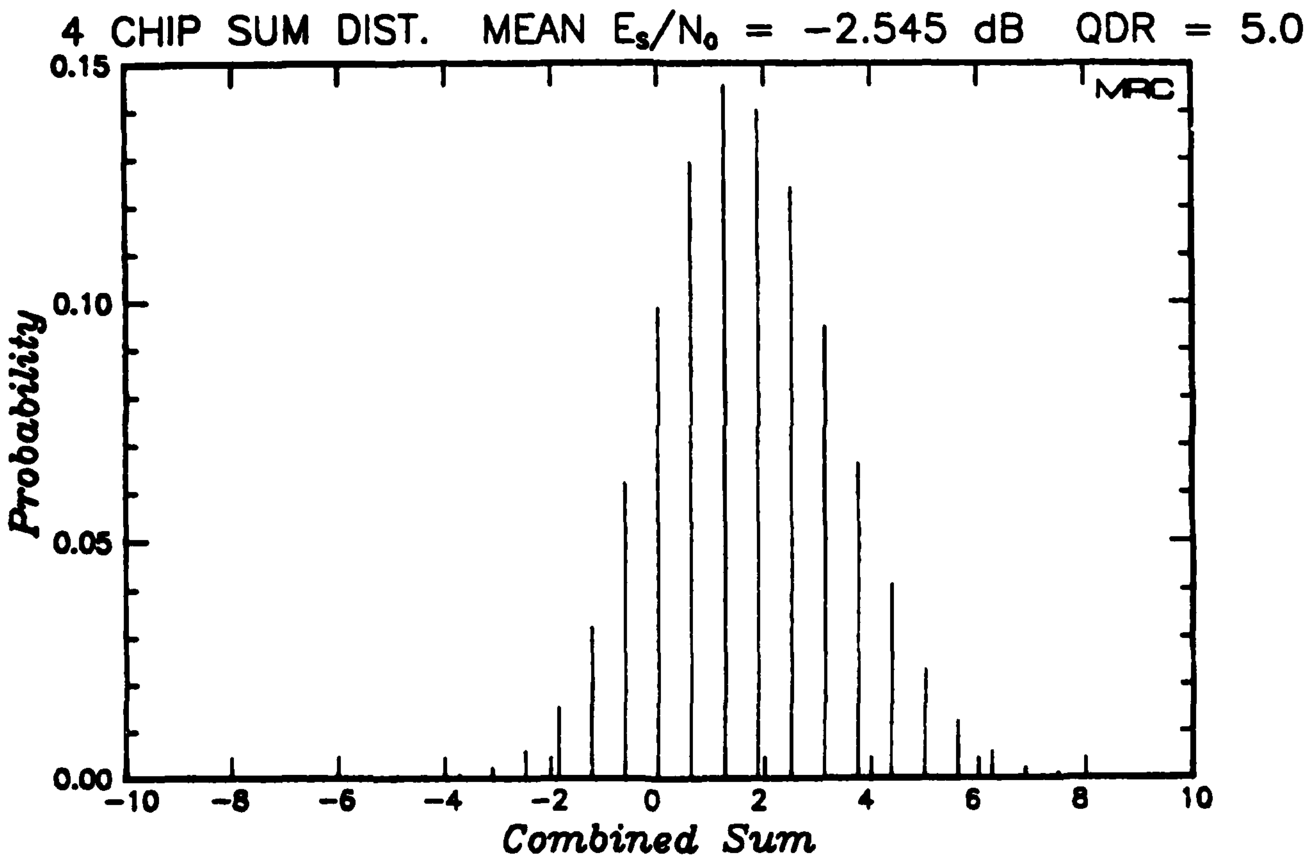

Figure 110. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 5.0. (Applicable to Link 2)

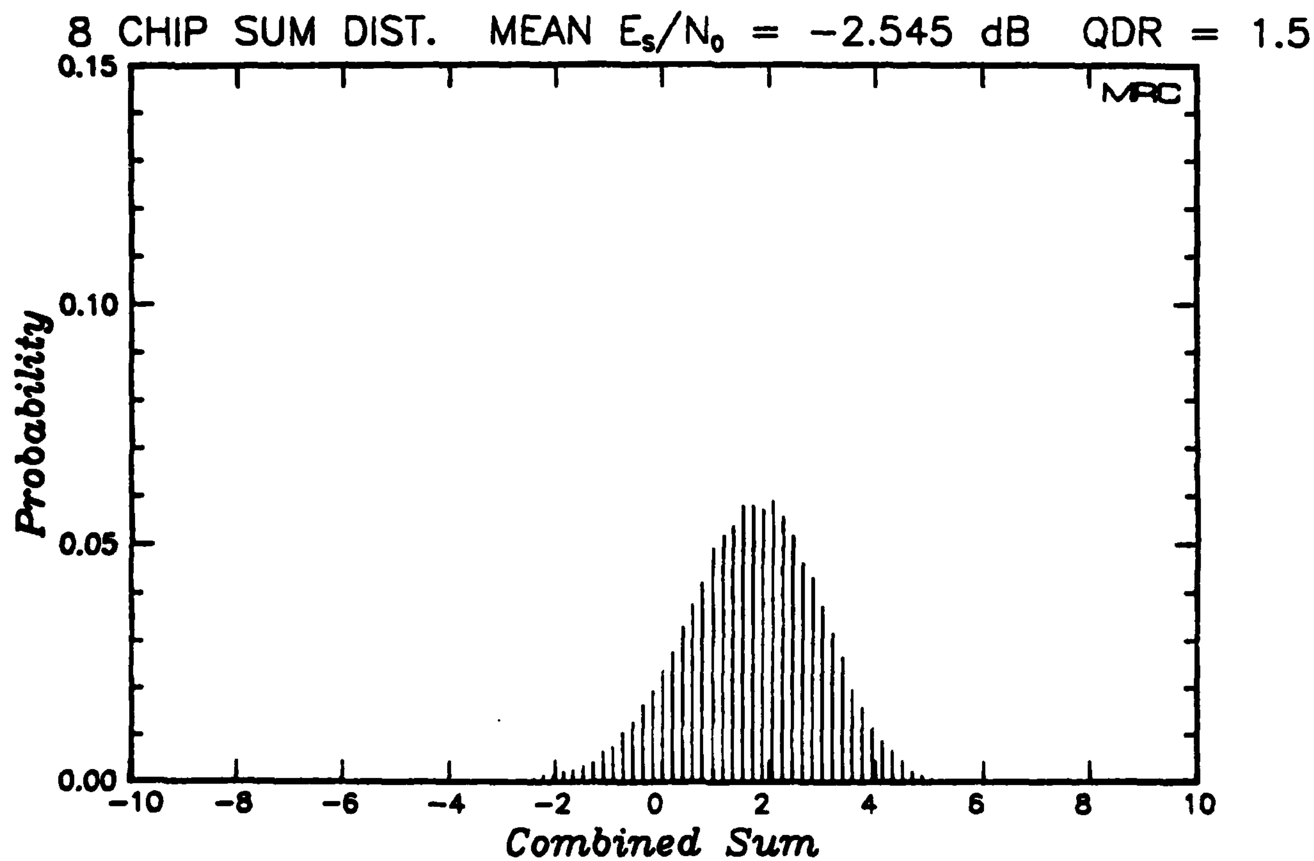

Figure 111. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 1.5. (Applicable to Link 1)

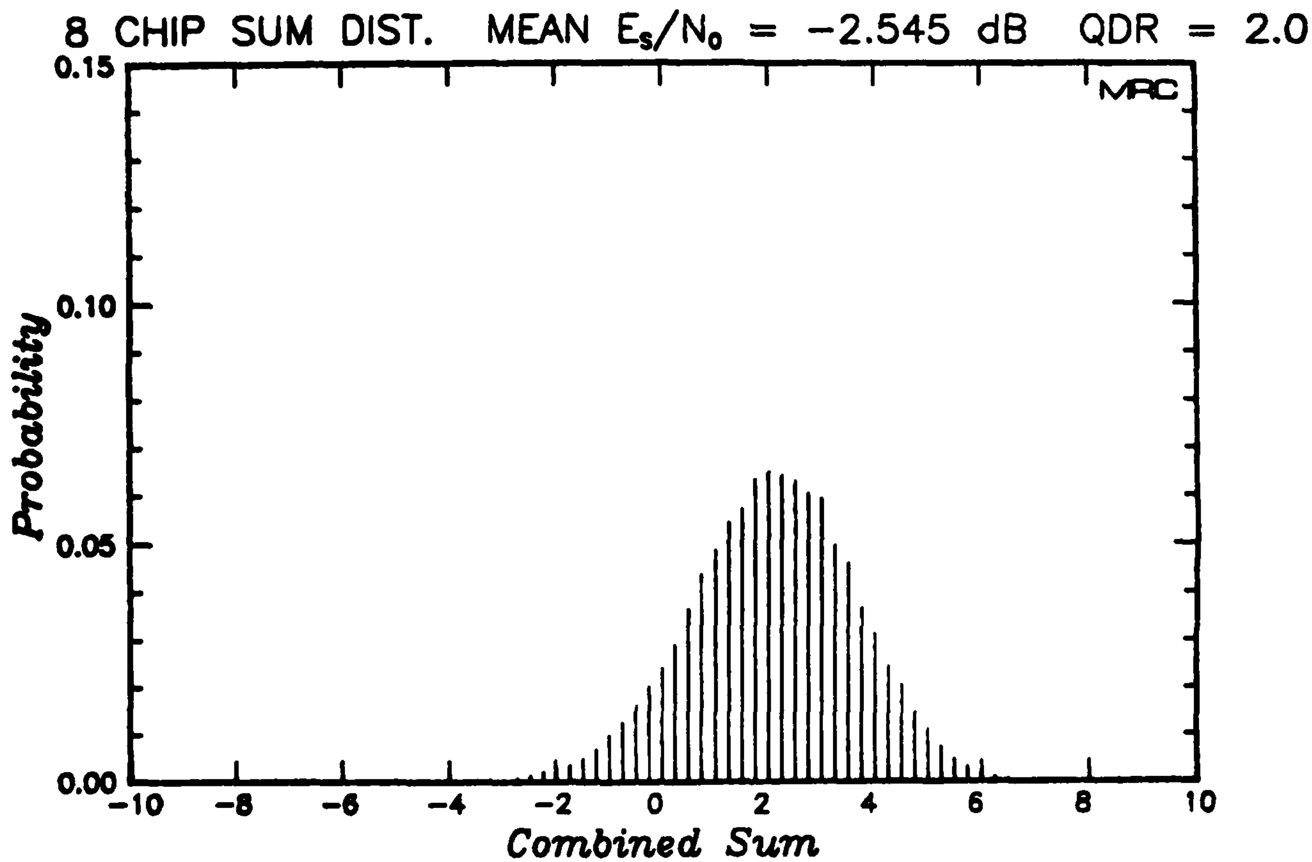

Figure 112. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -2.545 and normalized QDR of 2.0. (Applicable to Link 1)

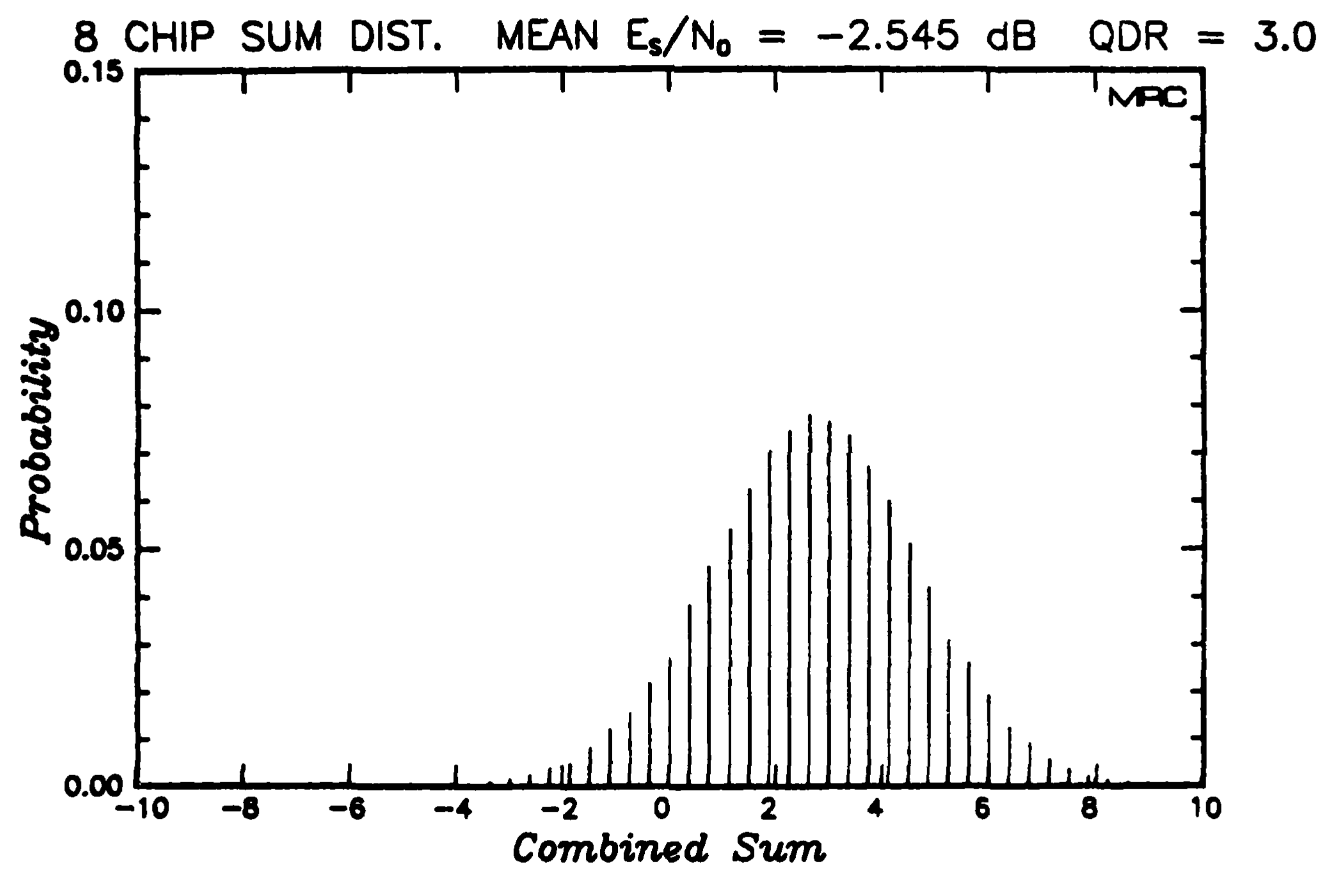

Figure 113. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 3.0. (Applicable to Link 1)

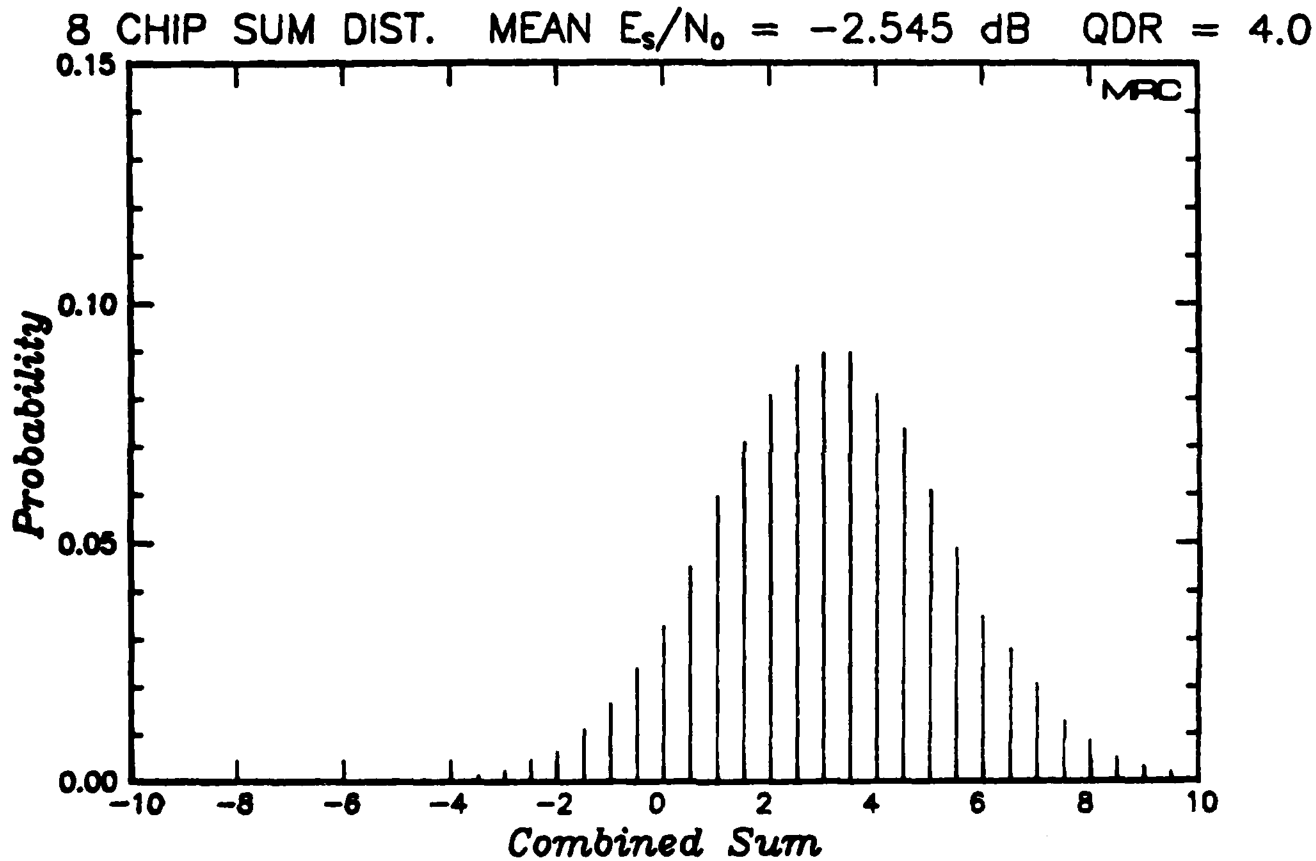

Figure 114. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 4.0. (Applicable to Link 1)

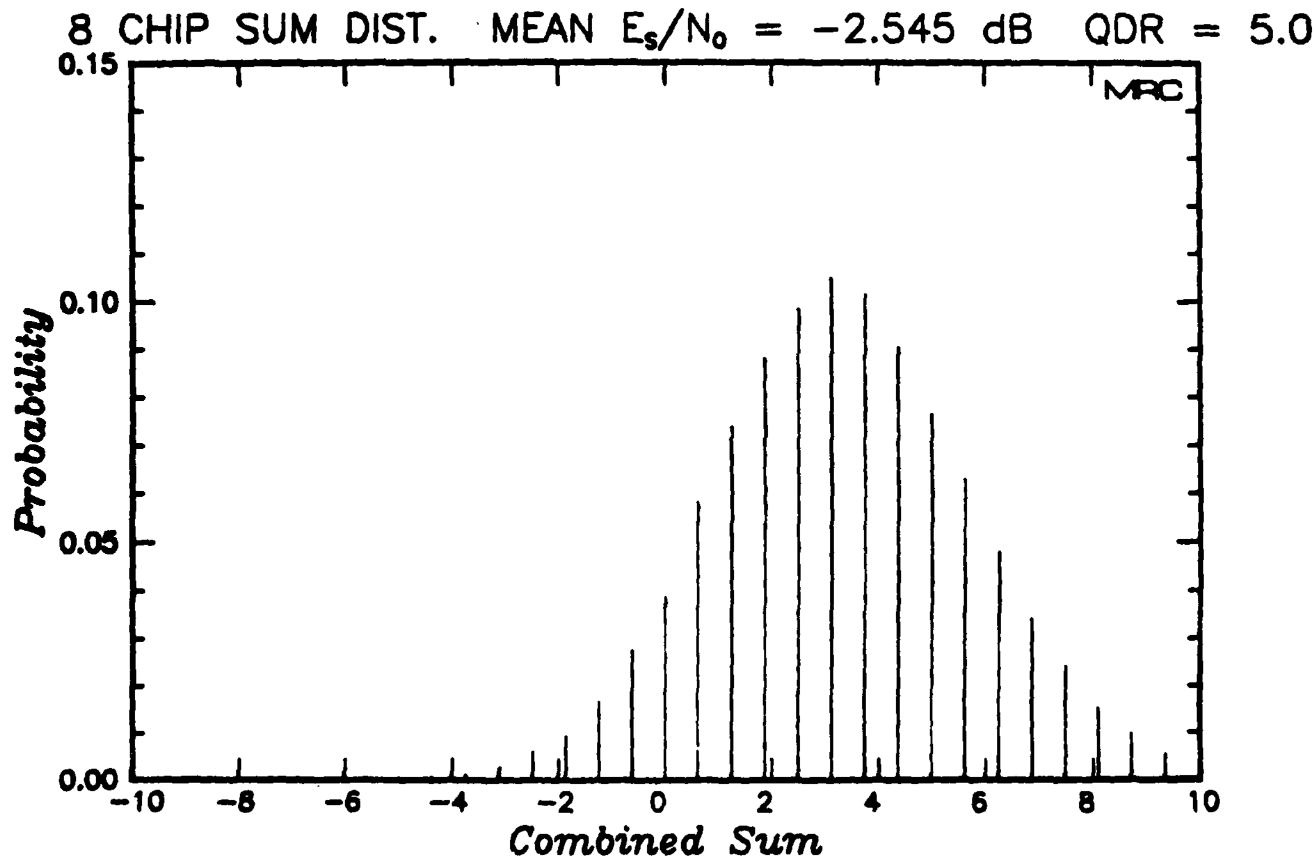

Figure 115. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -2.545 and normalized QDR of 5.0. (Applicable to Link 1)

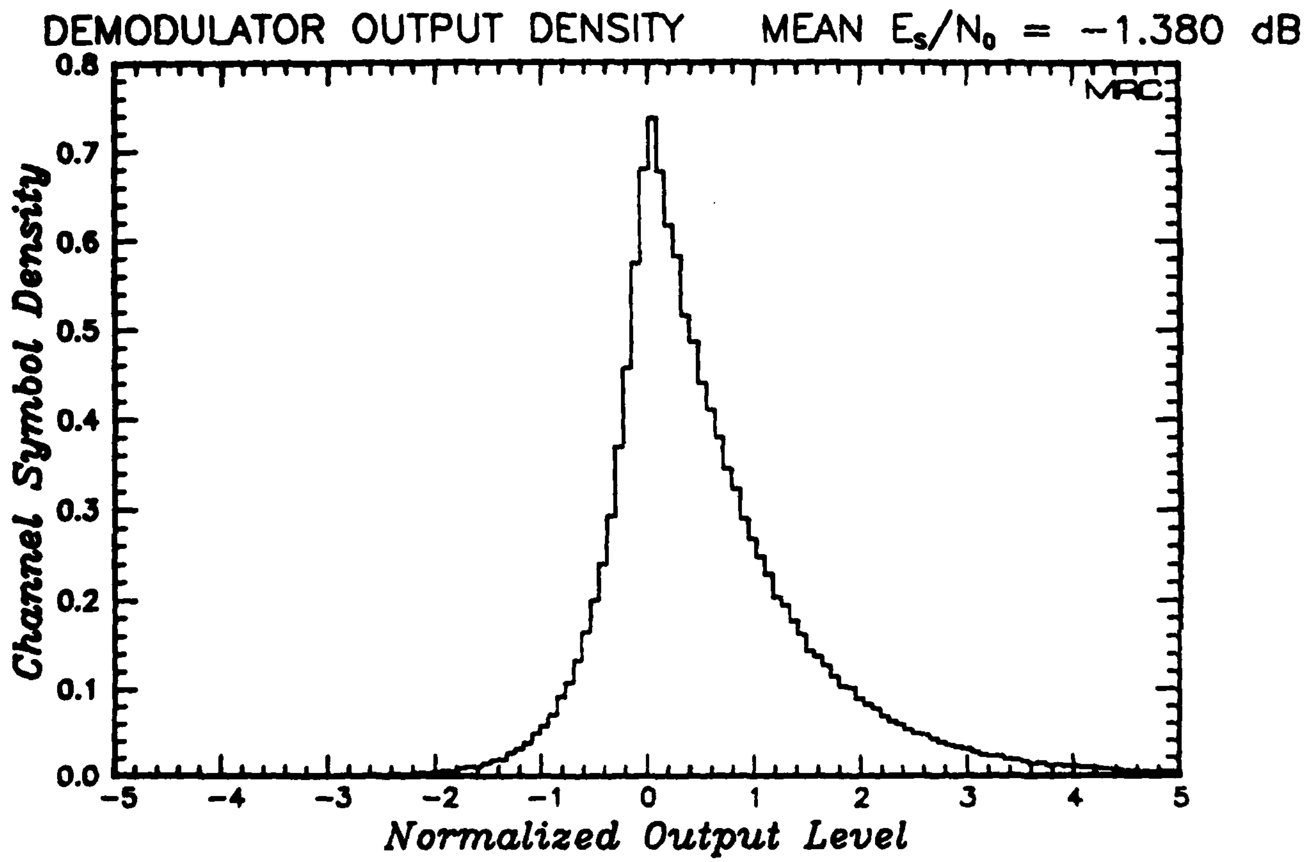

Figure 116. Histogram of demodulator outputs under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -1.380 dB.

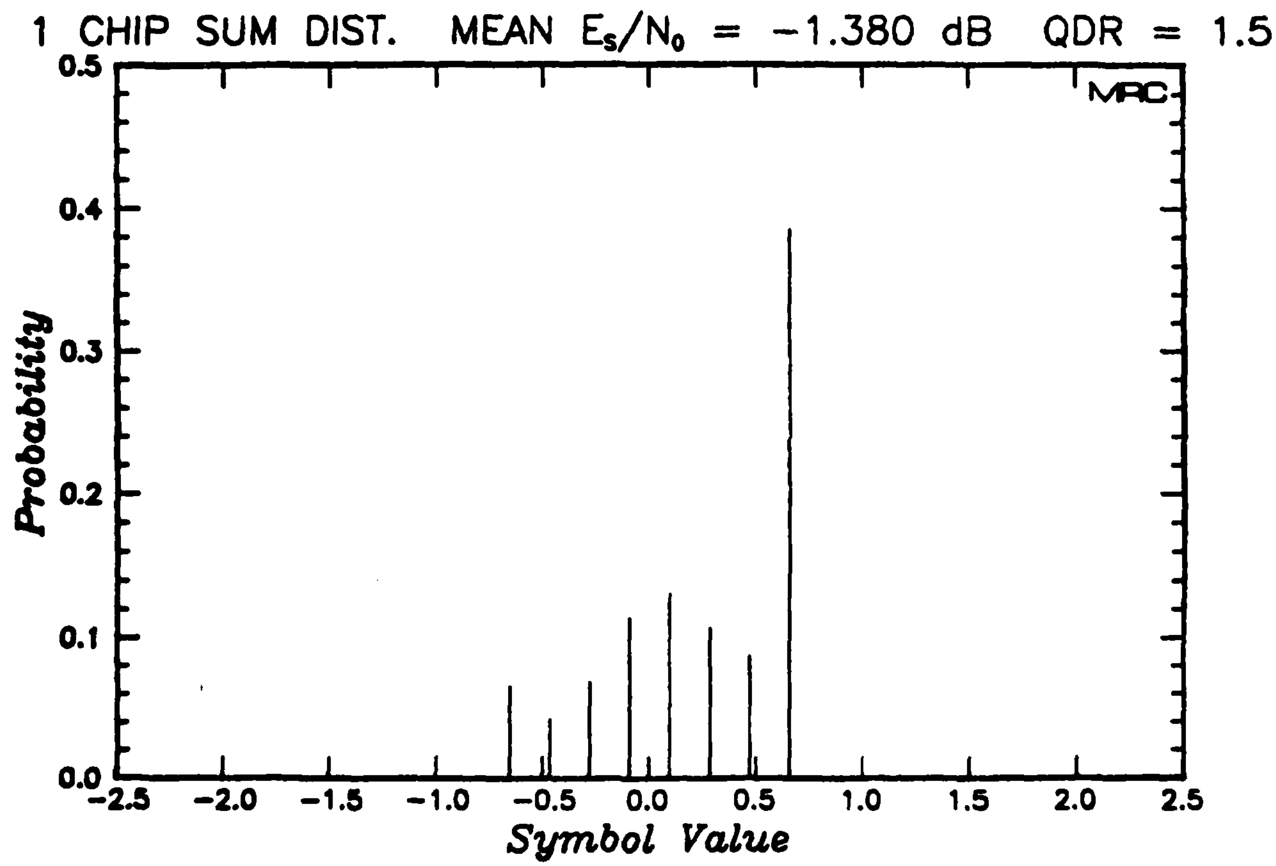

Figure 117. Measured probability distribution of quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -1.380 and normalized QDR of 1.5. (Applicable to Link 4)

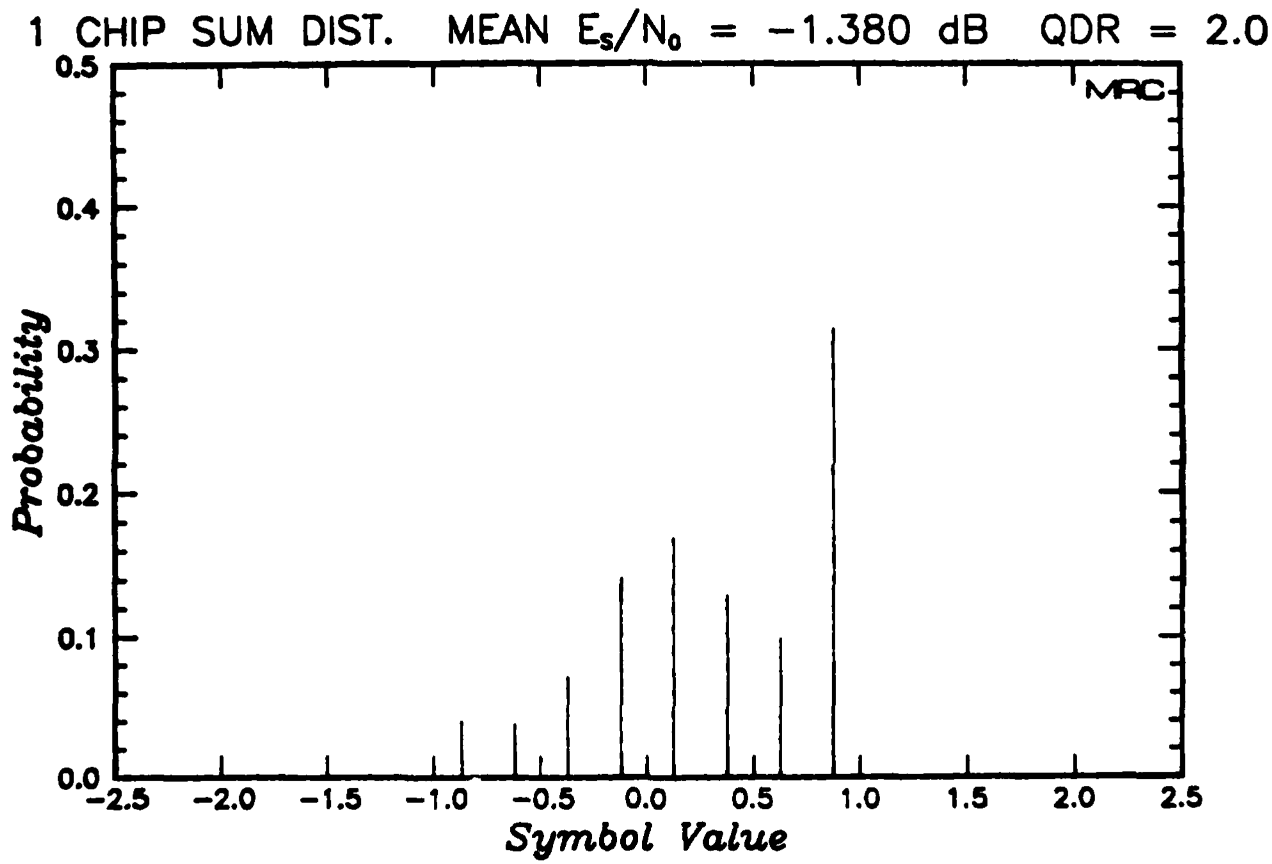

Figure 118. Measured probability distribution of quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -1.380 and normalized QDR of 2.0. (Applicable to Link 4)

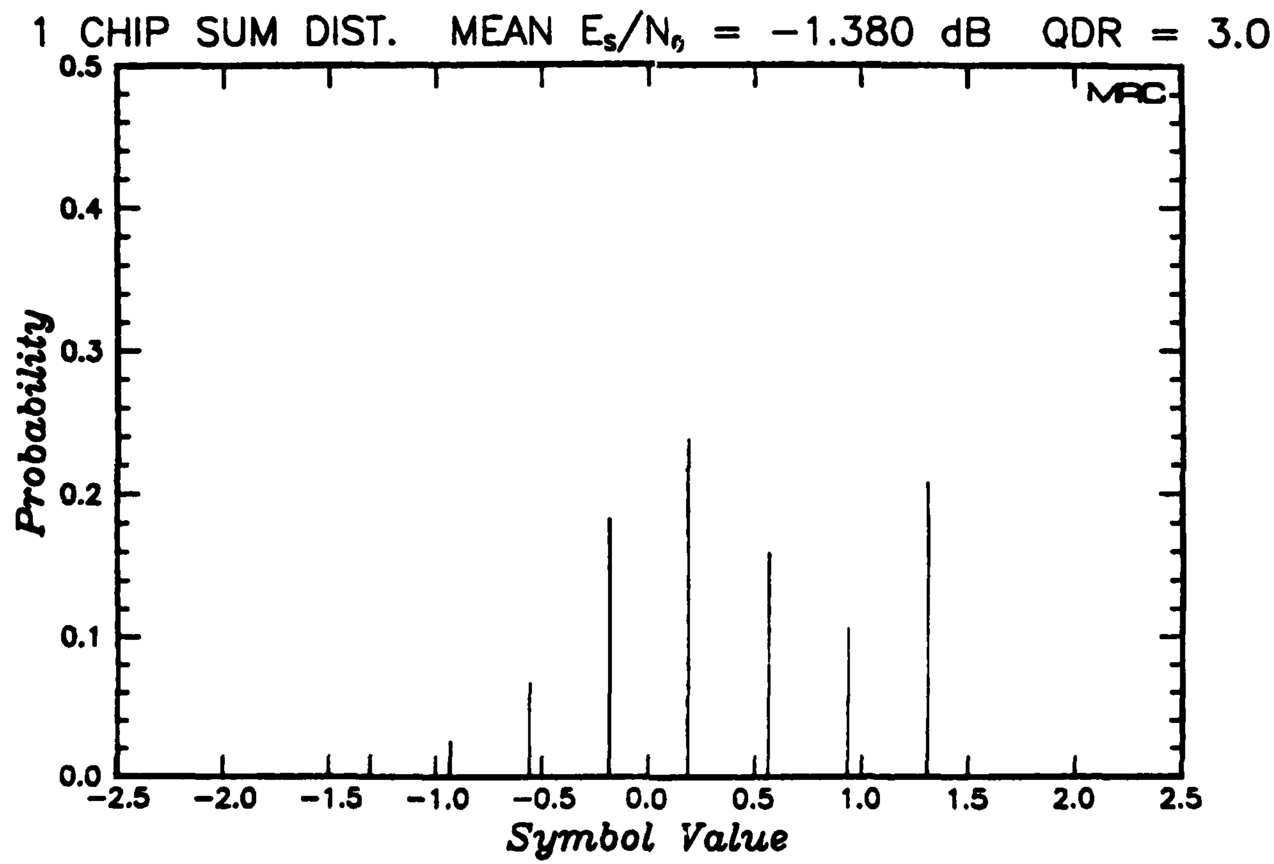

Figure 119. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_O = -1.380 and normalized QDR of 3.0. (Applicable to Link 4).

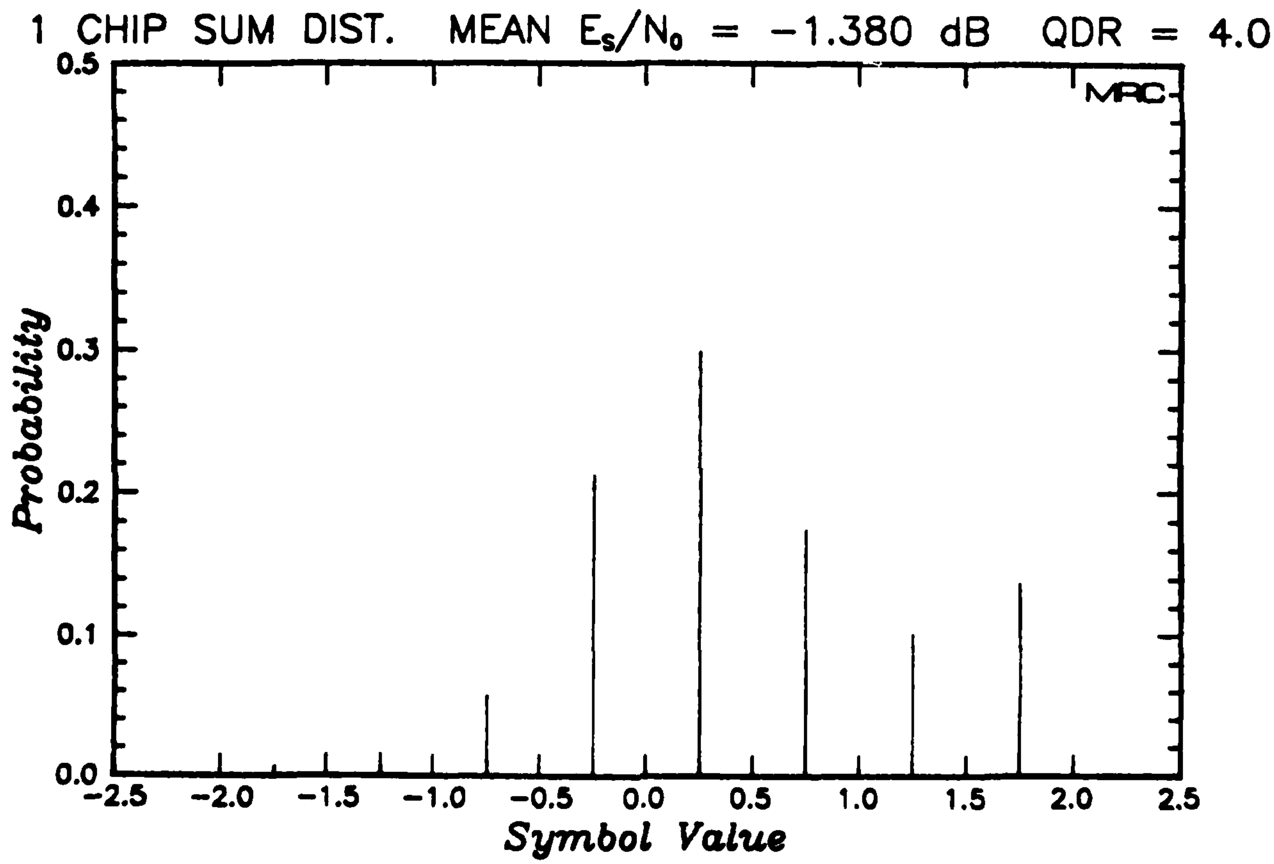

Figure 120. Measured probability distribution of quantized symbols under fading channel conditions for τ_c = 0.1 second and E_S/N_0 = -1.380 and normalized QDR of 4.0. (Applicable to Link 4)

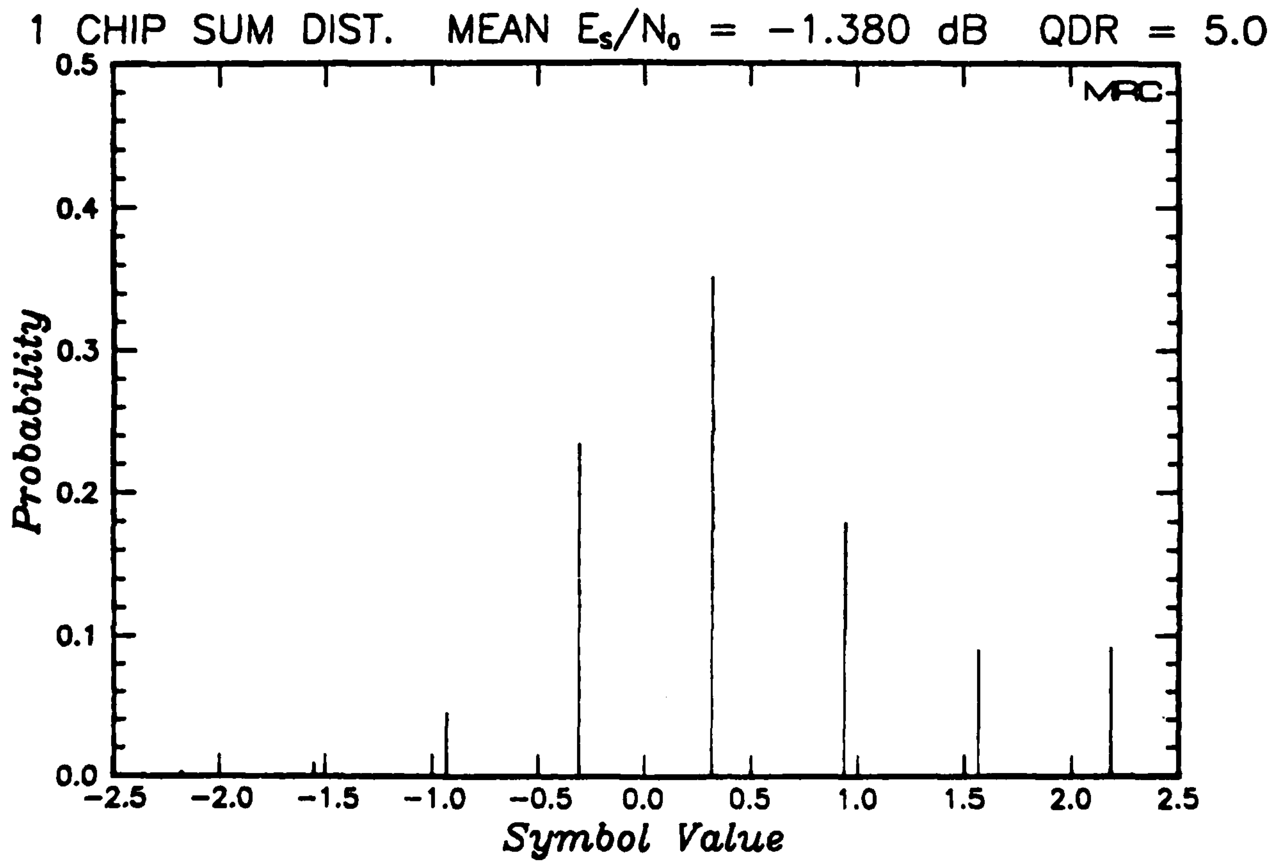

Figure 121. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -1.380 and normalized QDR of 5.0. (Applicable to Link 4)

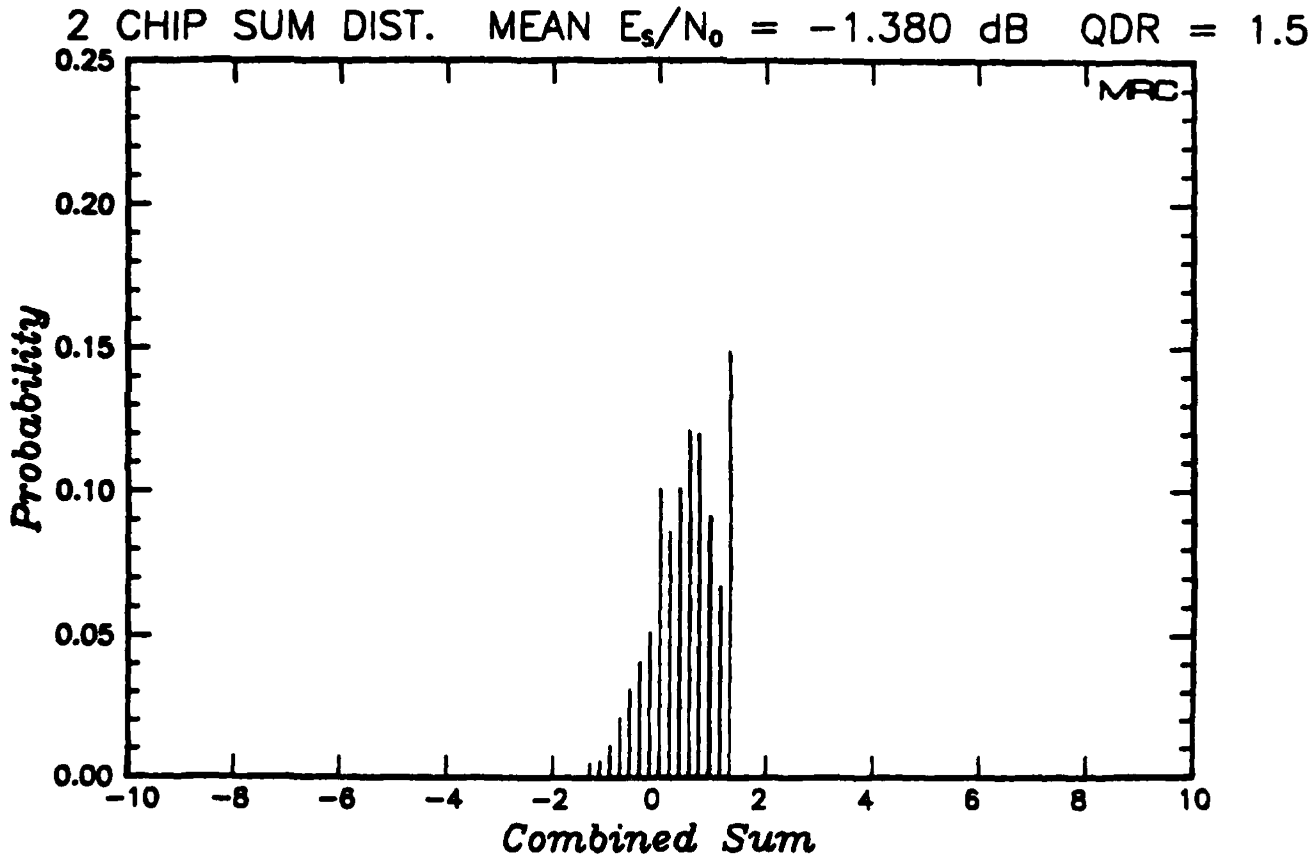

Figure 122. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 1.5. (Applicable to Link 3)

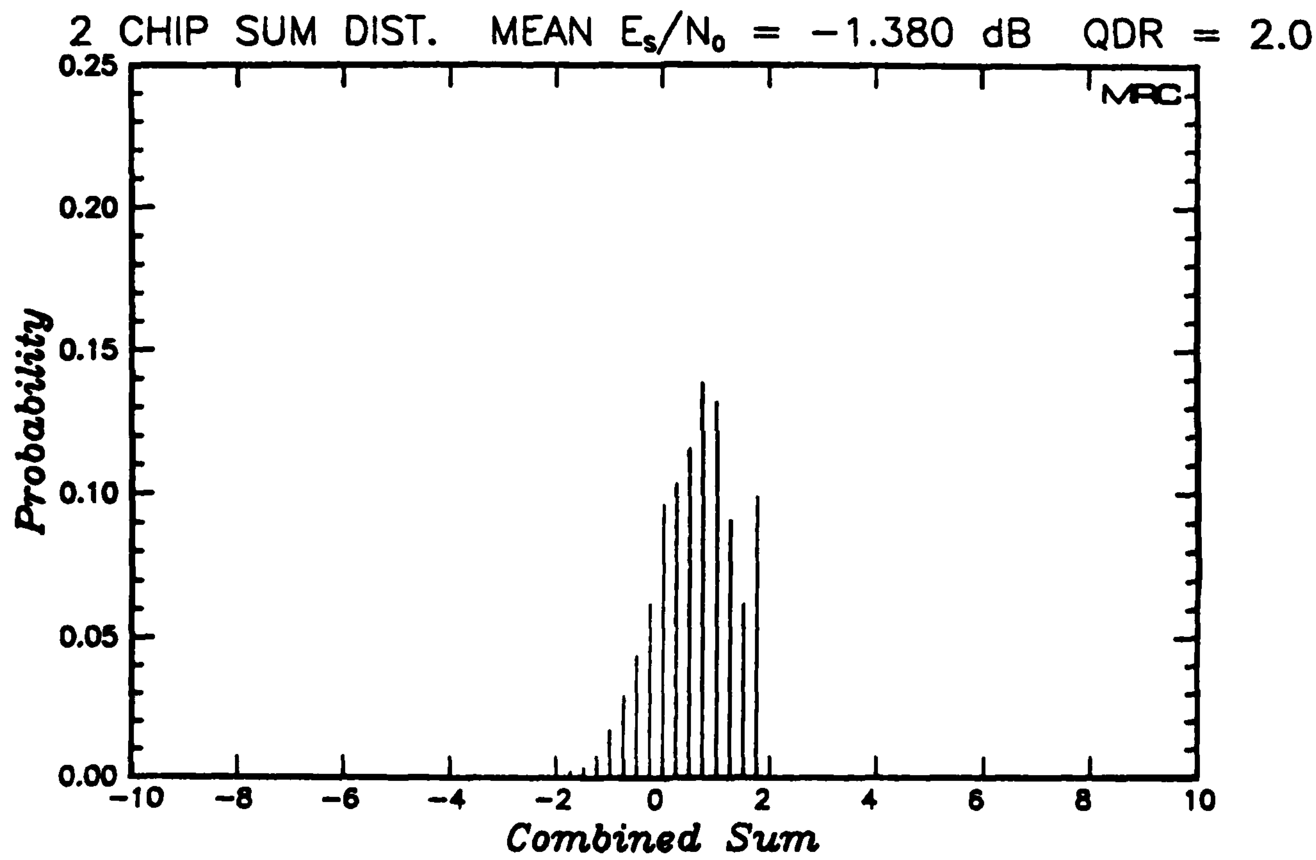

Figure 123. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 2.0. (Applicable to Link 3)

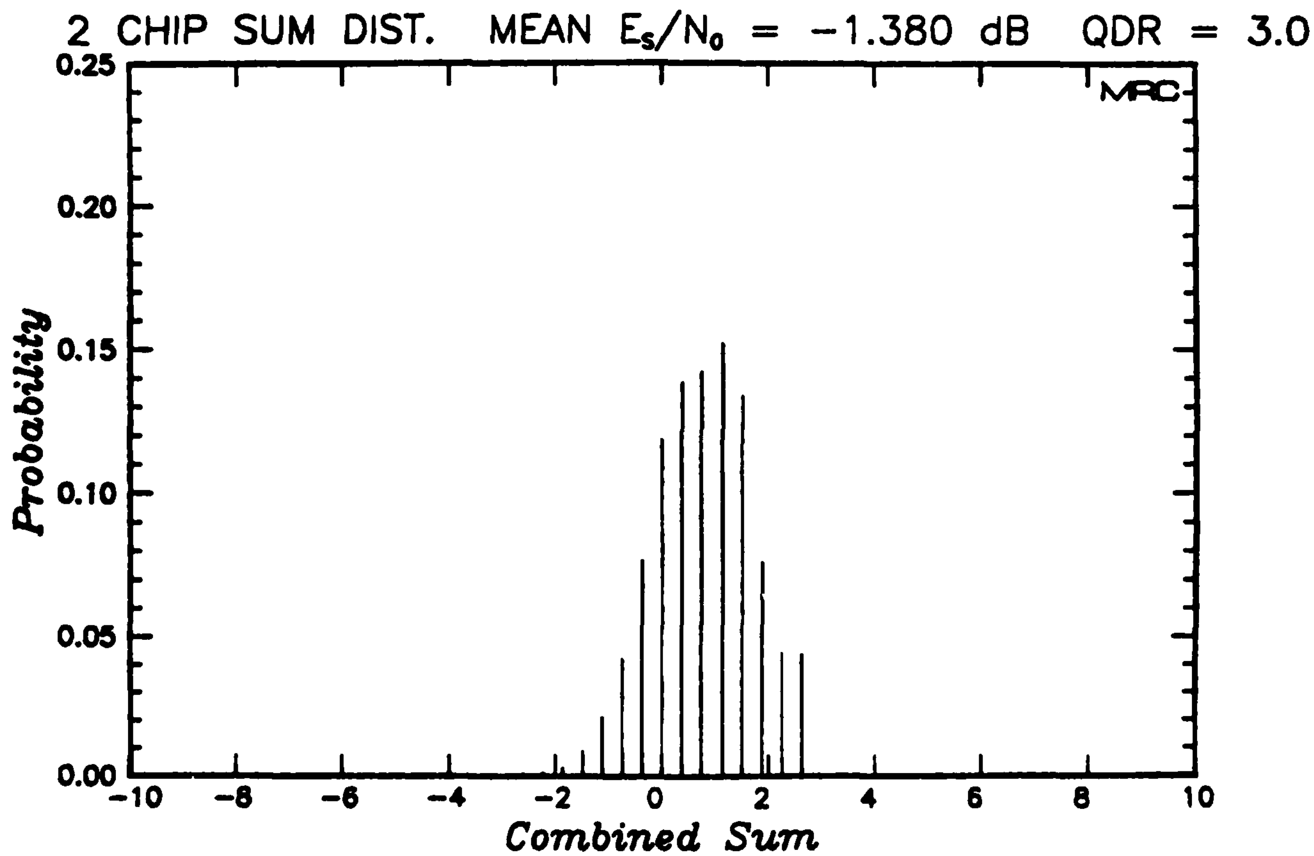

Figure 124. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 3.0. (Applicable to Link 3)

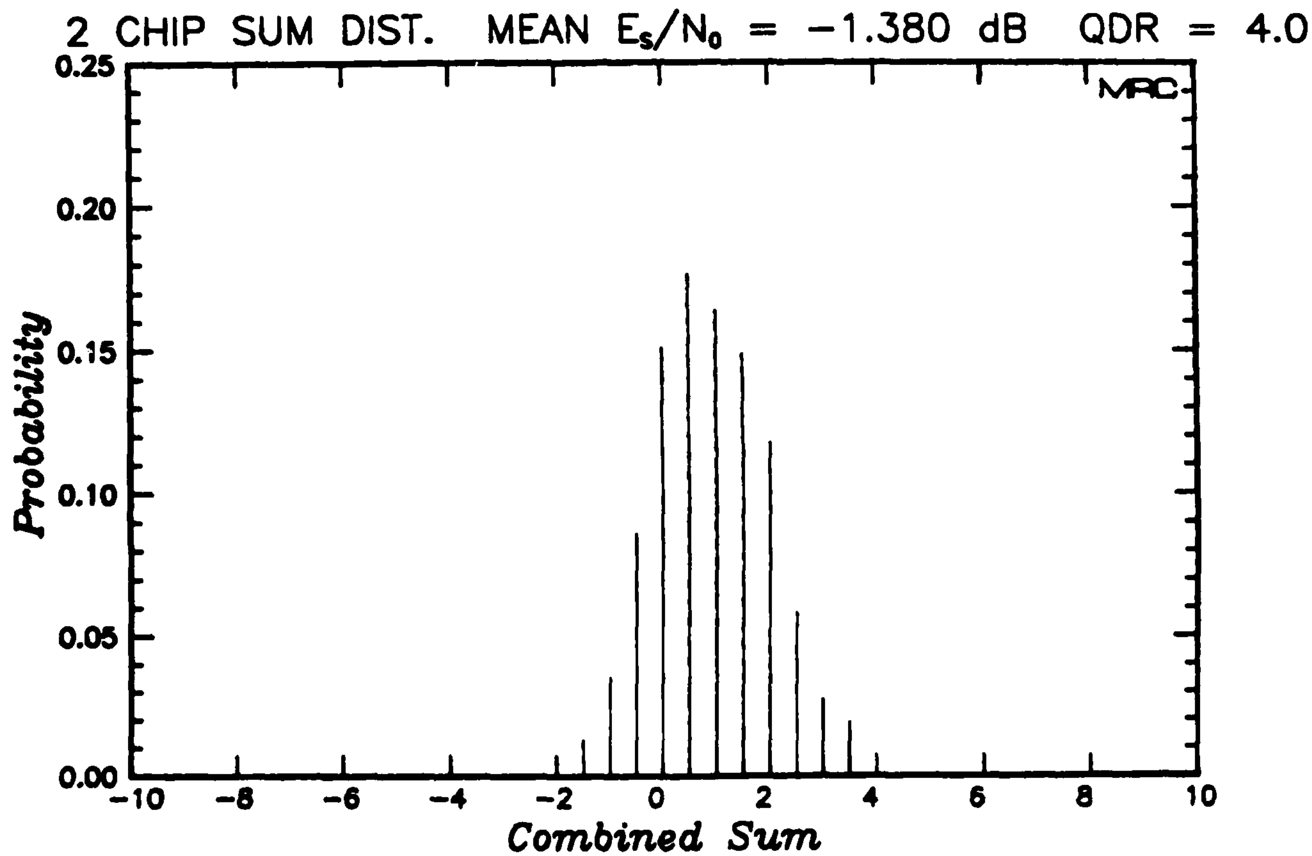

Figure 125. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 4.0. (Applicable to Link 3)

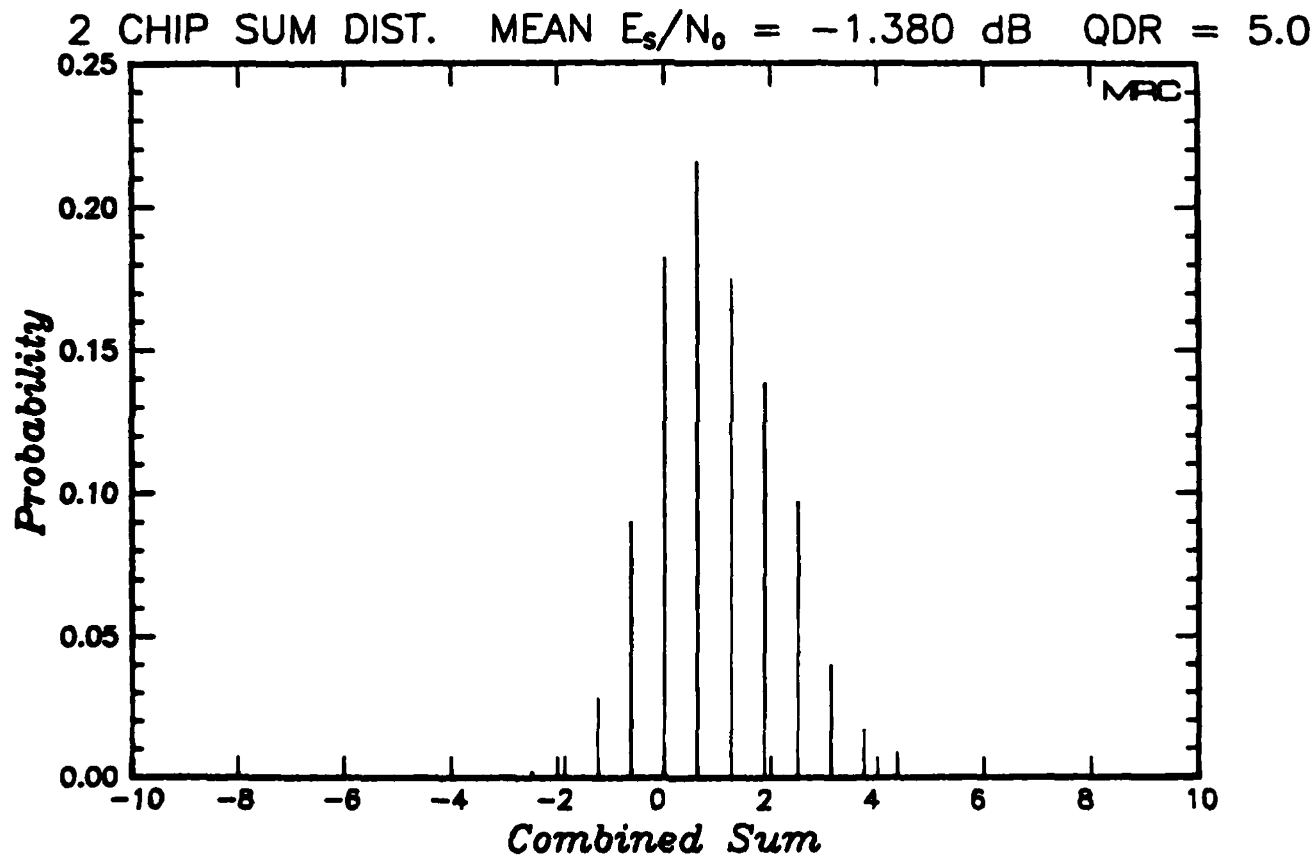

Figure 126. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -1.380 and normalized QDR of 5.0. (Applicable to Link 3)

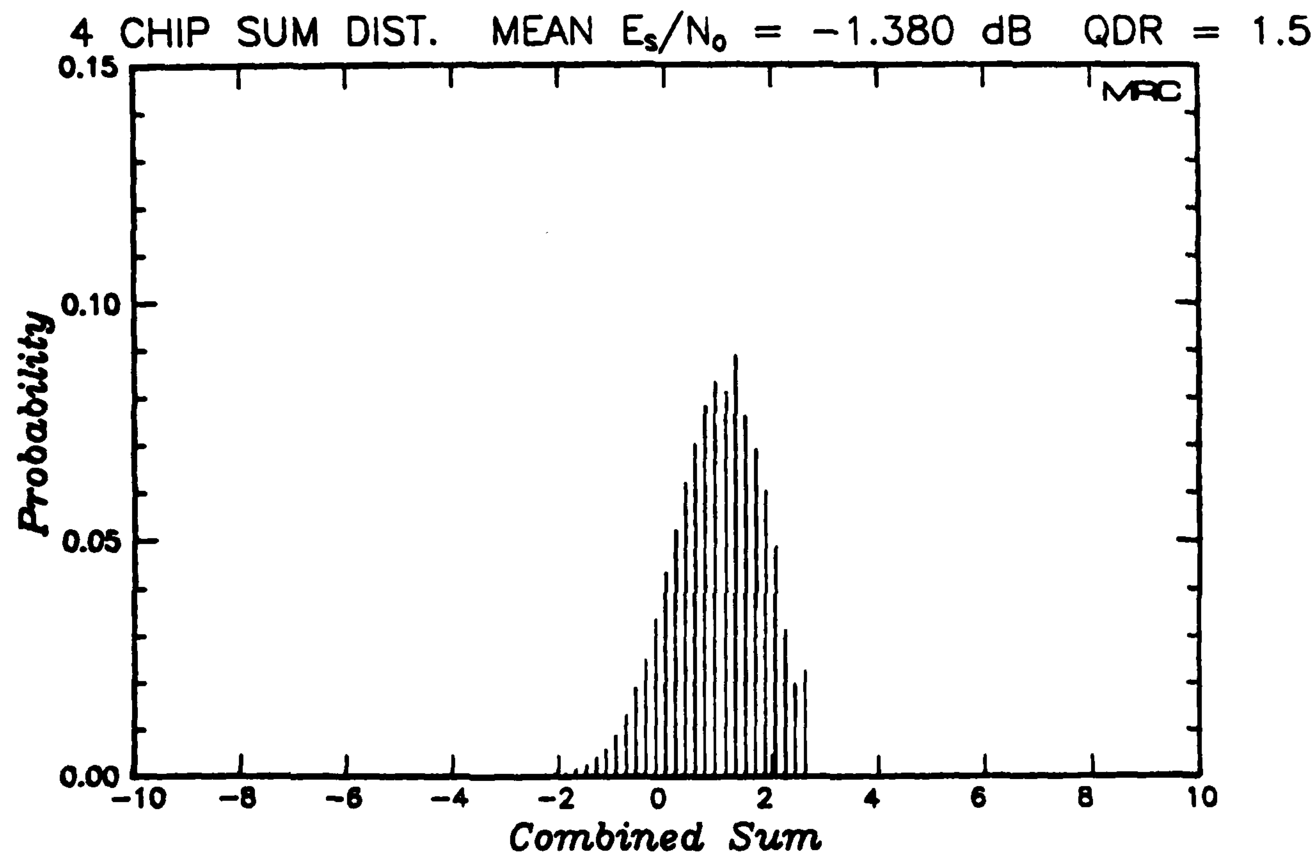

Figure 127. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -1.380 and normalized QDR of 1.5. (Applicable to Link 2)

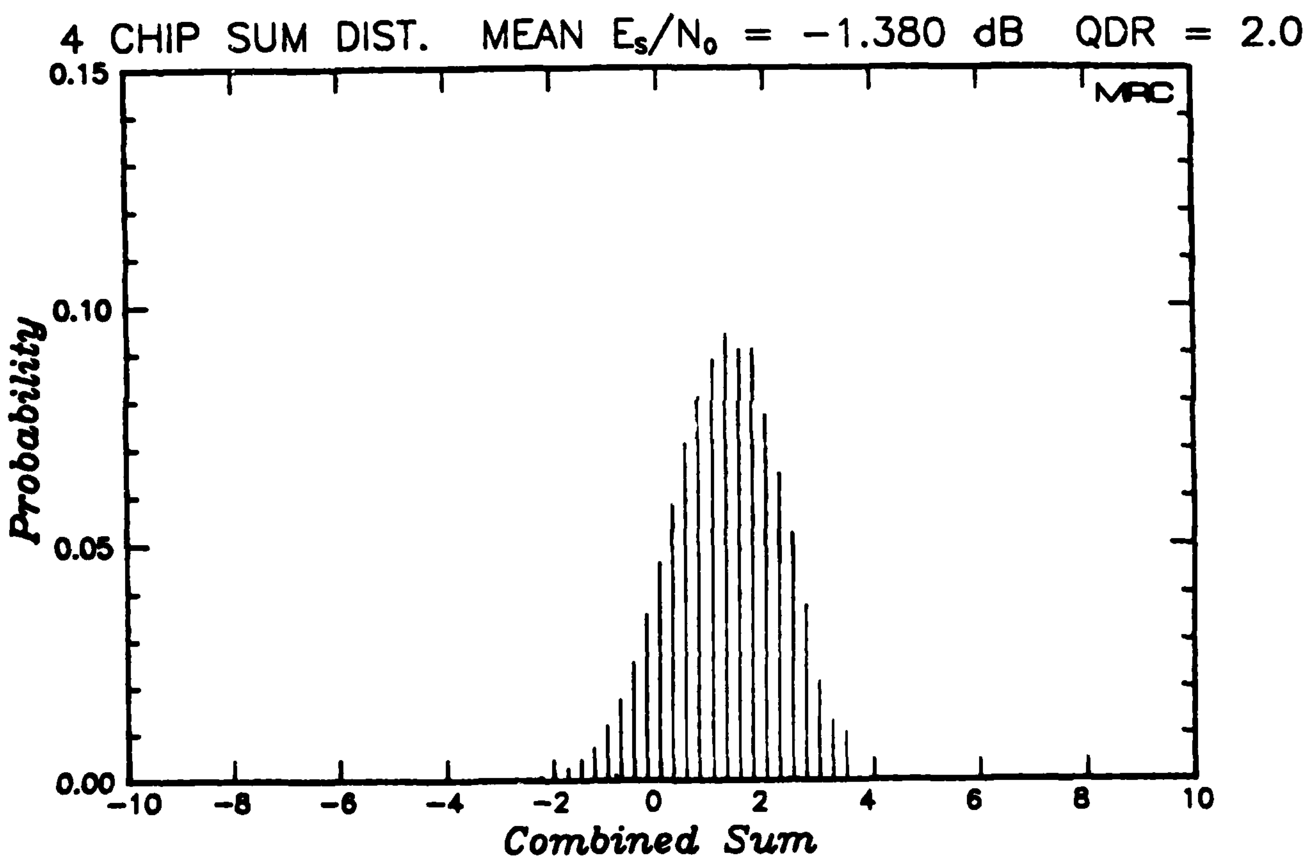

Figure 128. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -1.380 and normalized QDR of 2.0. (Applicable to Link 2)

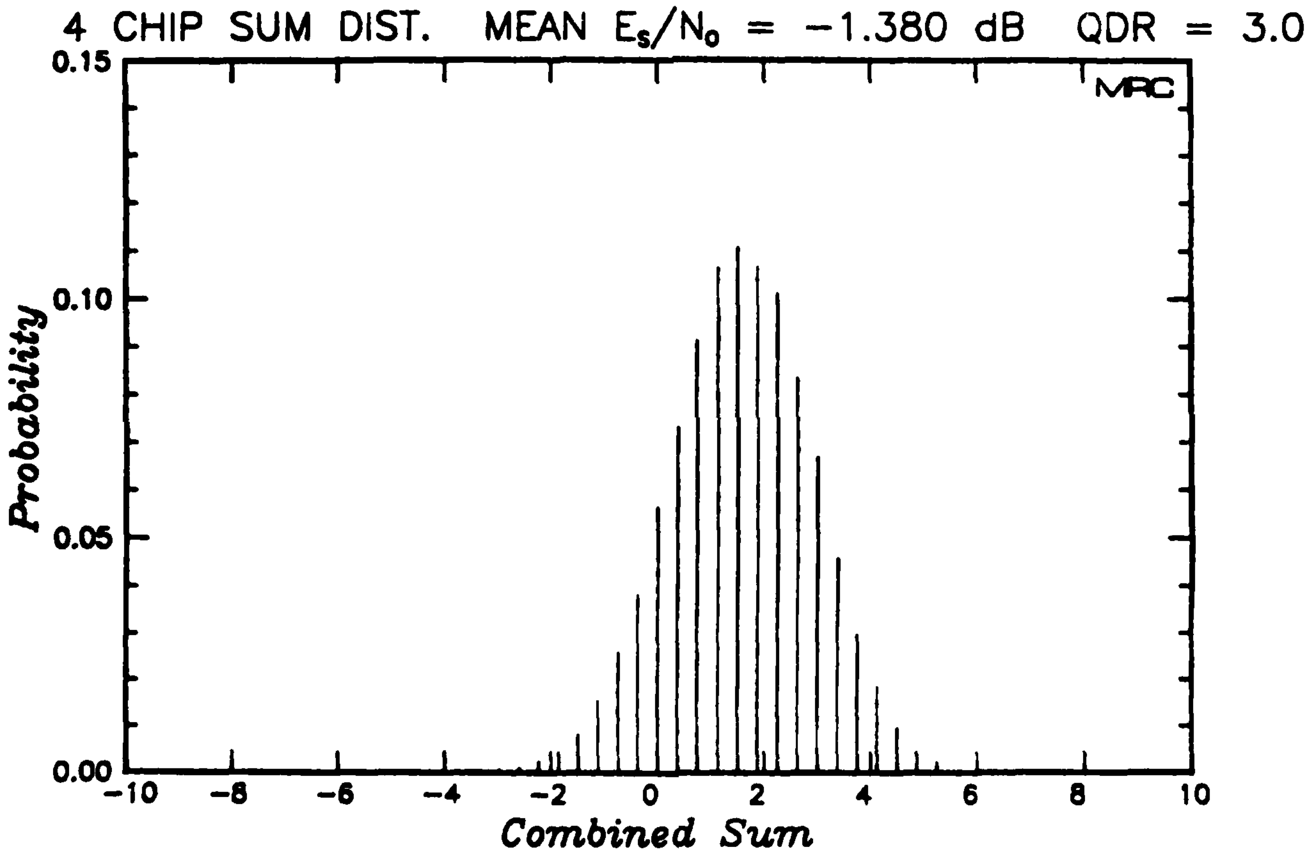

Figure 129. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_O = -1.380 and normalized QDR of 3.0. (Applicable to Link 2)

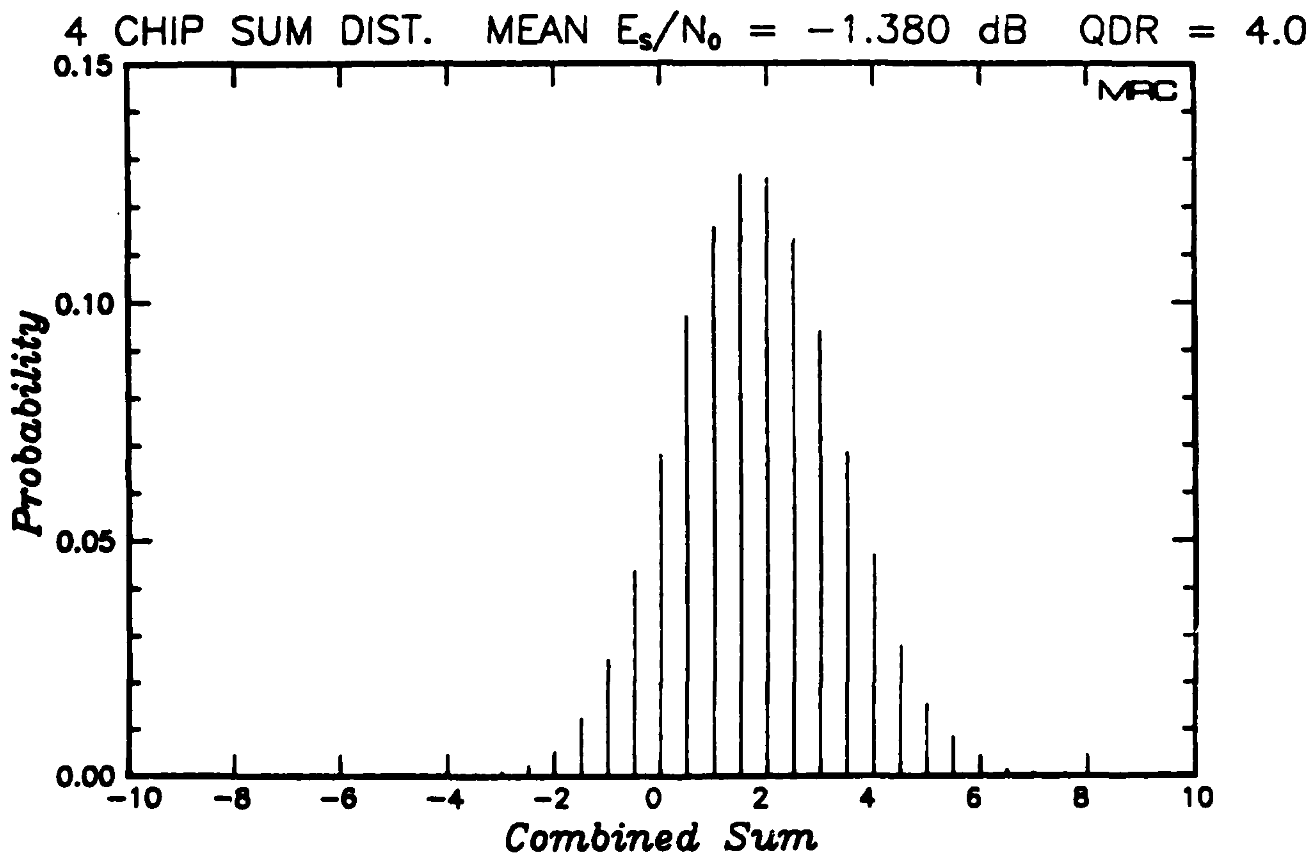

Figure 130. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 4.0. (Applicable to Link 2)

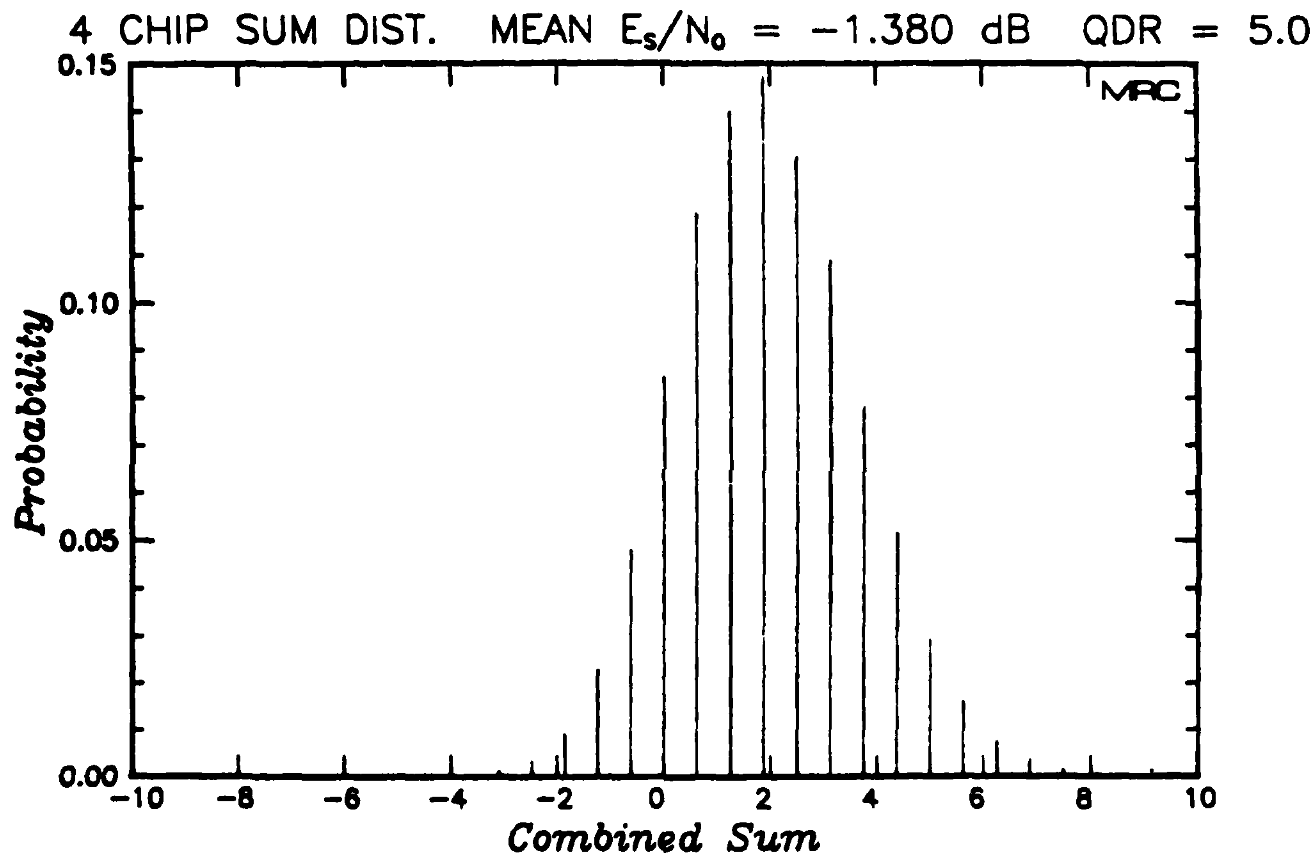

Figure 131. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 5.0. (Applicable to Link 2)

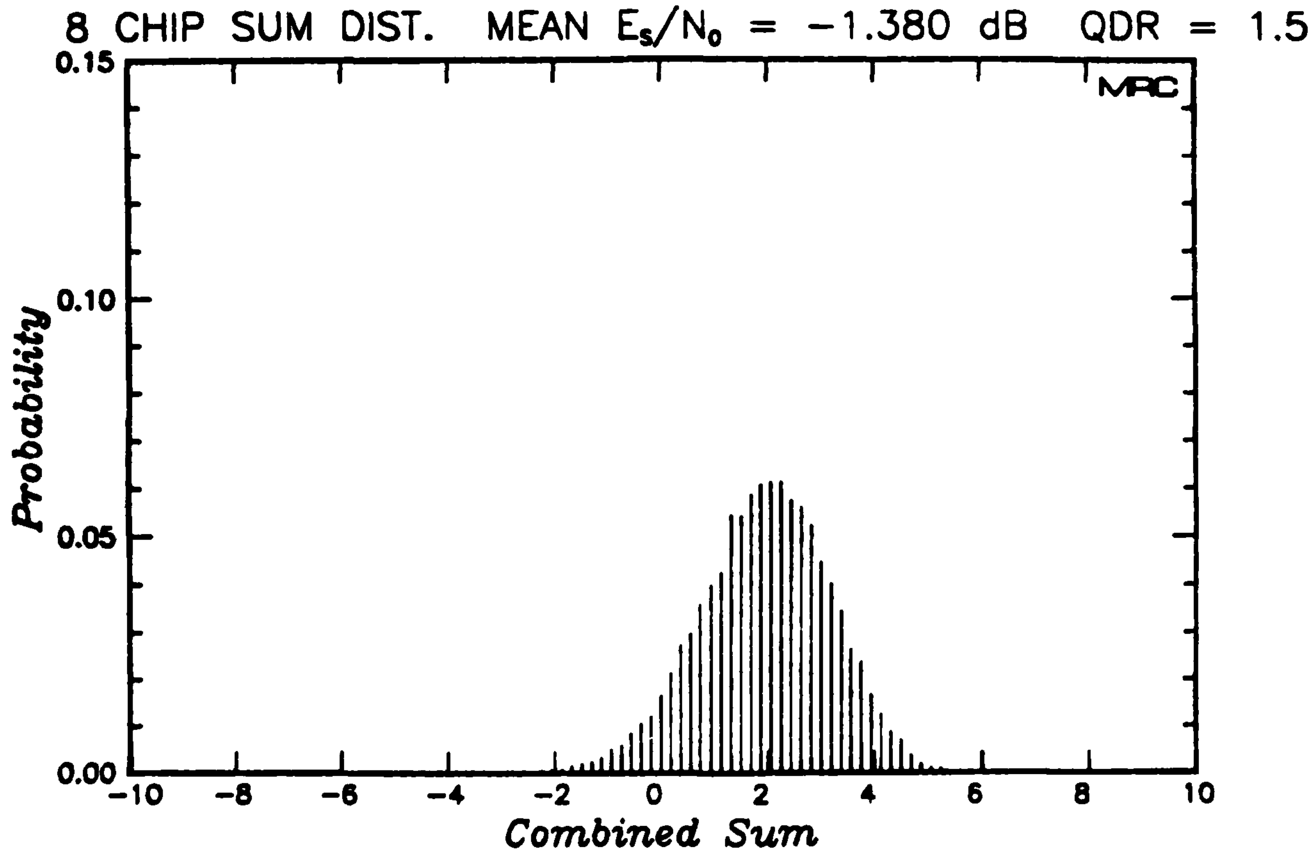

Figure 132. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -1.380 and normalized QDR of 1.5. (Applicable to Link 1)

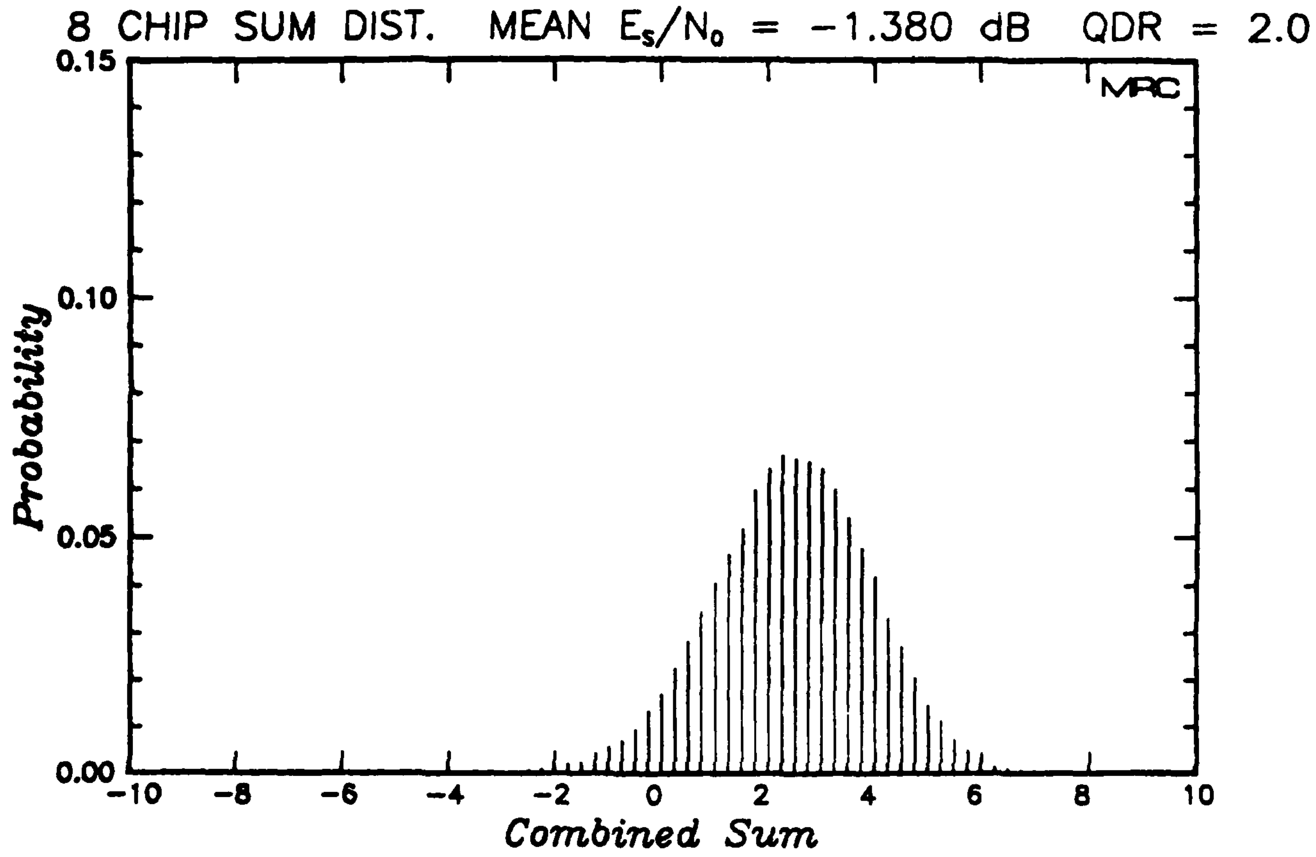

Figure 133. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 2.0. (Applicable to Link 1)

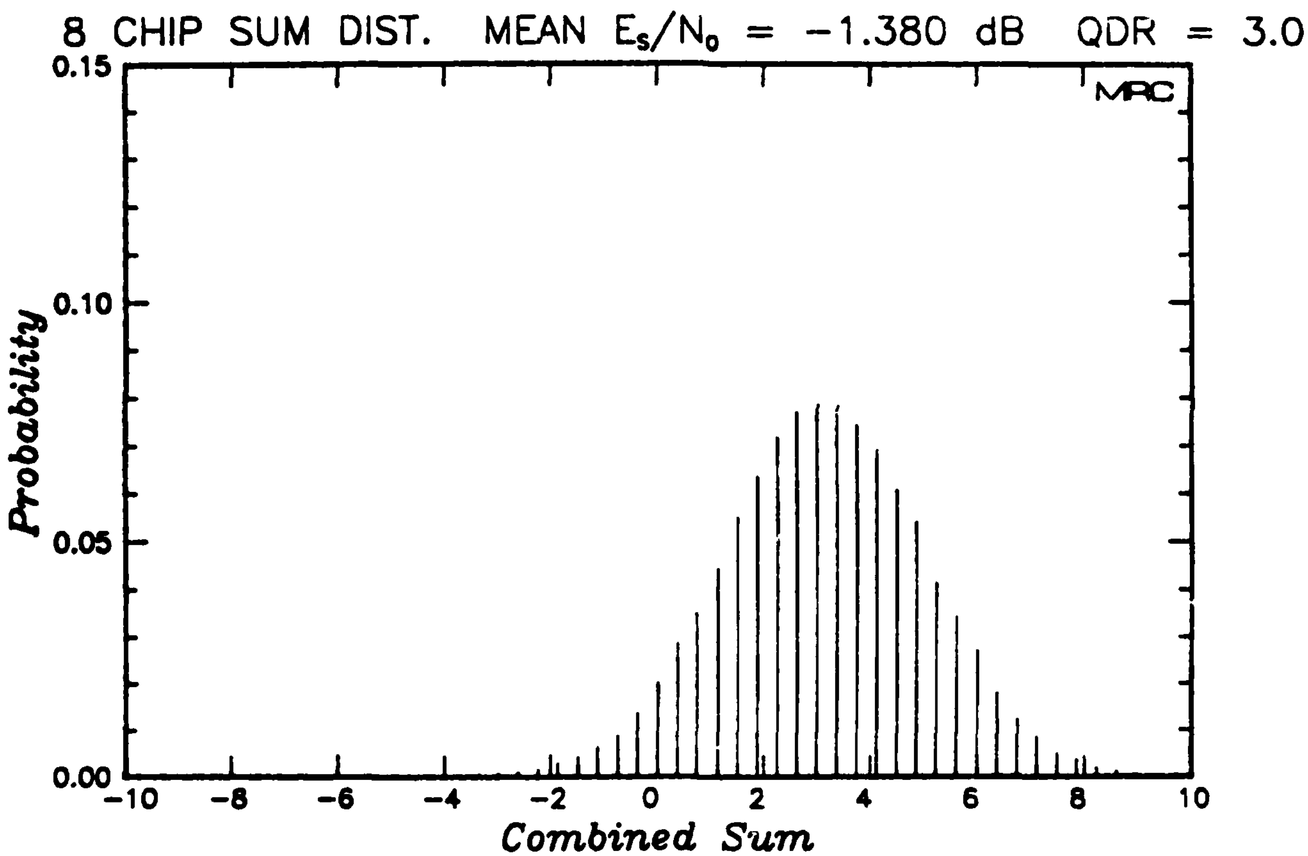

Figure 134. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 3.0. (Applicable to Link 1)

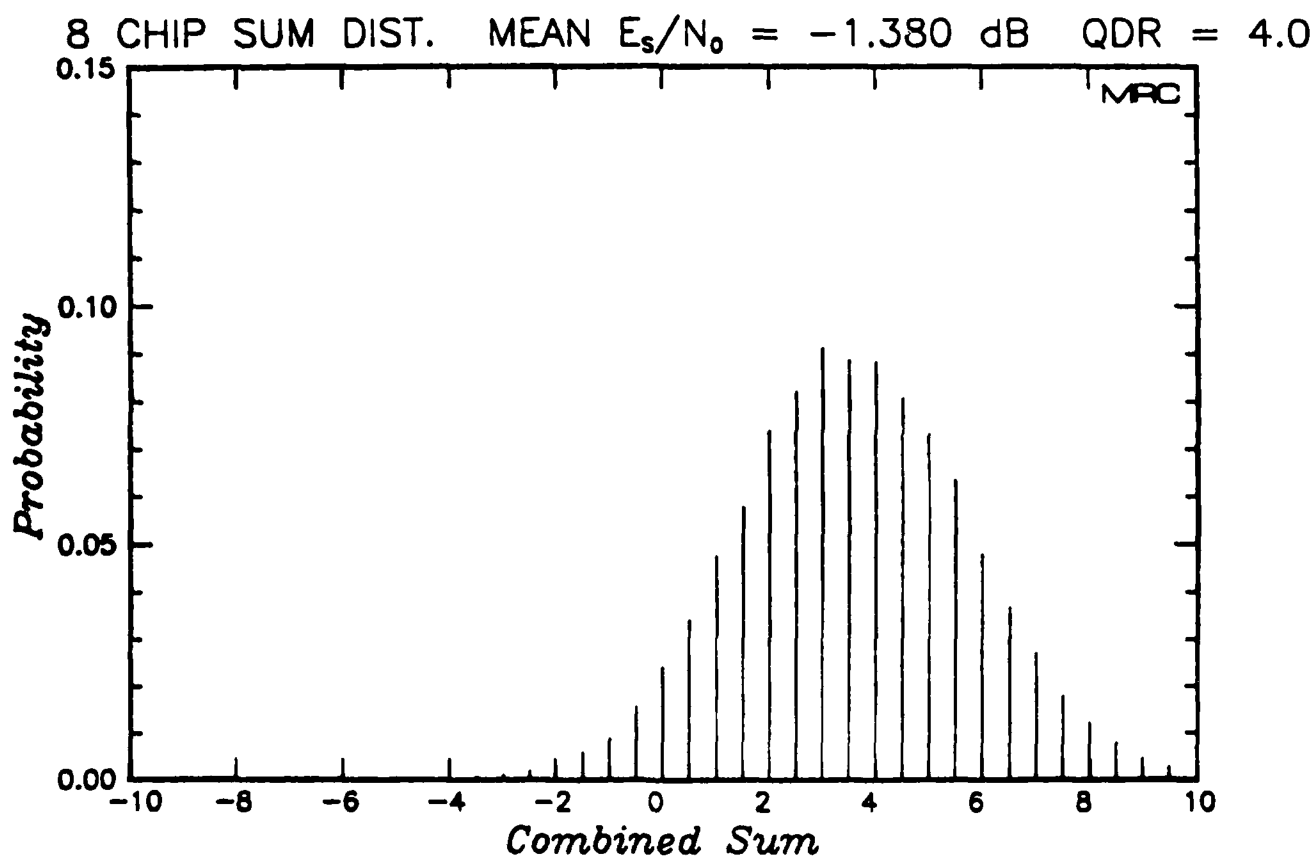

Figure 135. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 4.0. (Applicable to Link 1)

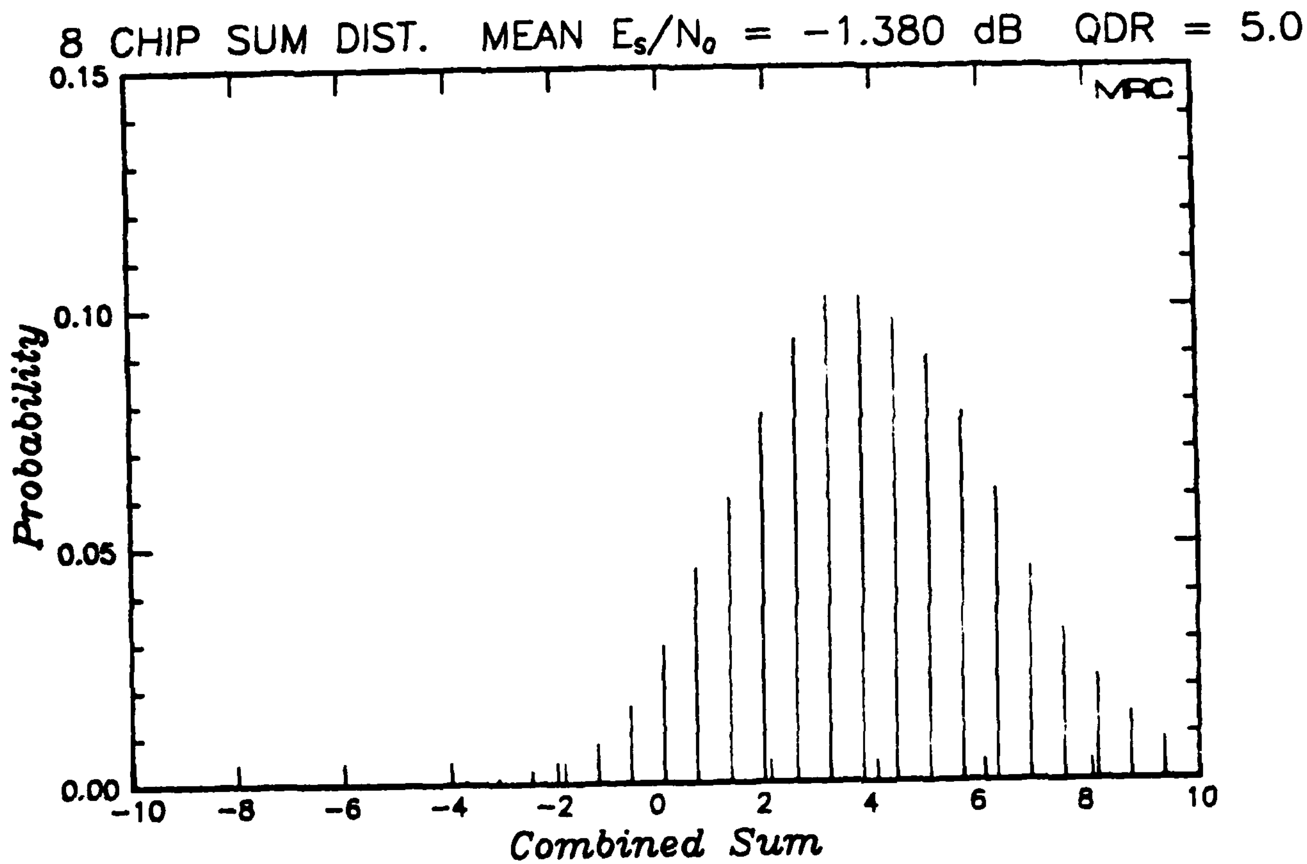

Figure 136. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -1.380 and normalized QDR of 5.0. (Applicable to Link 1)

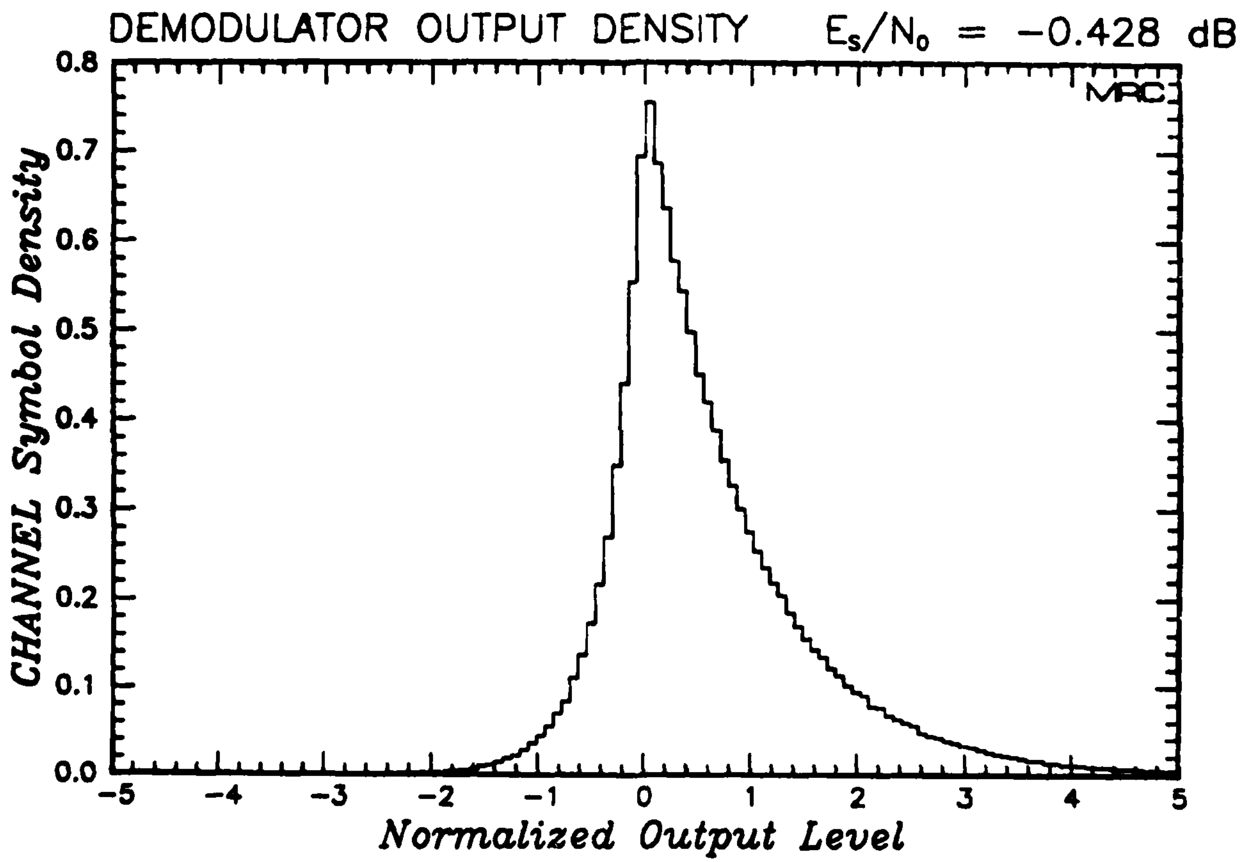

Figure 137. Histogram of demodulator outputs under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 dB.

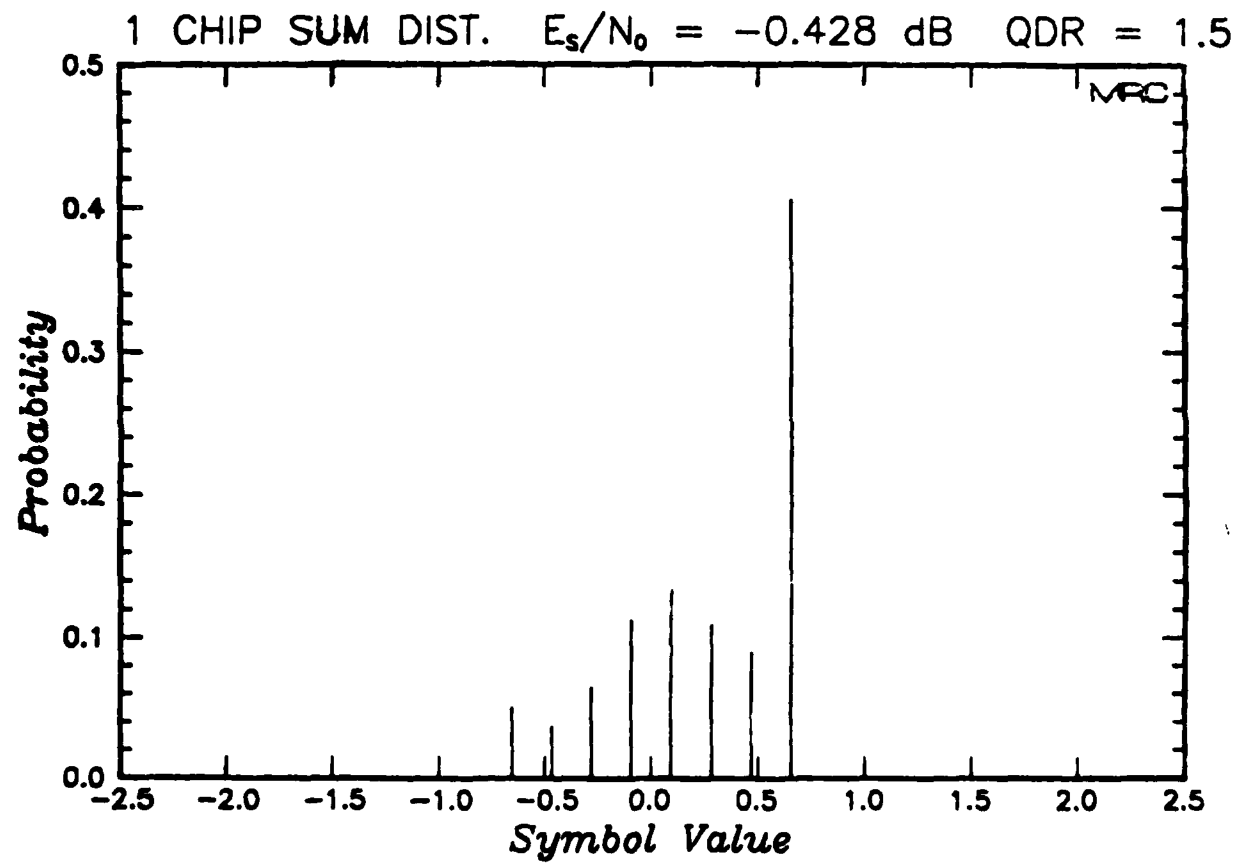

Figure 138. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -0.428 and normalized QDR of 1.5. (Applicable to Link 4)

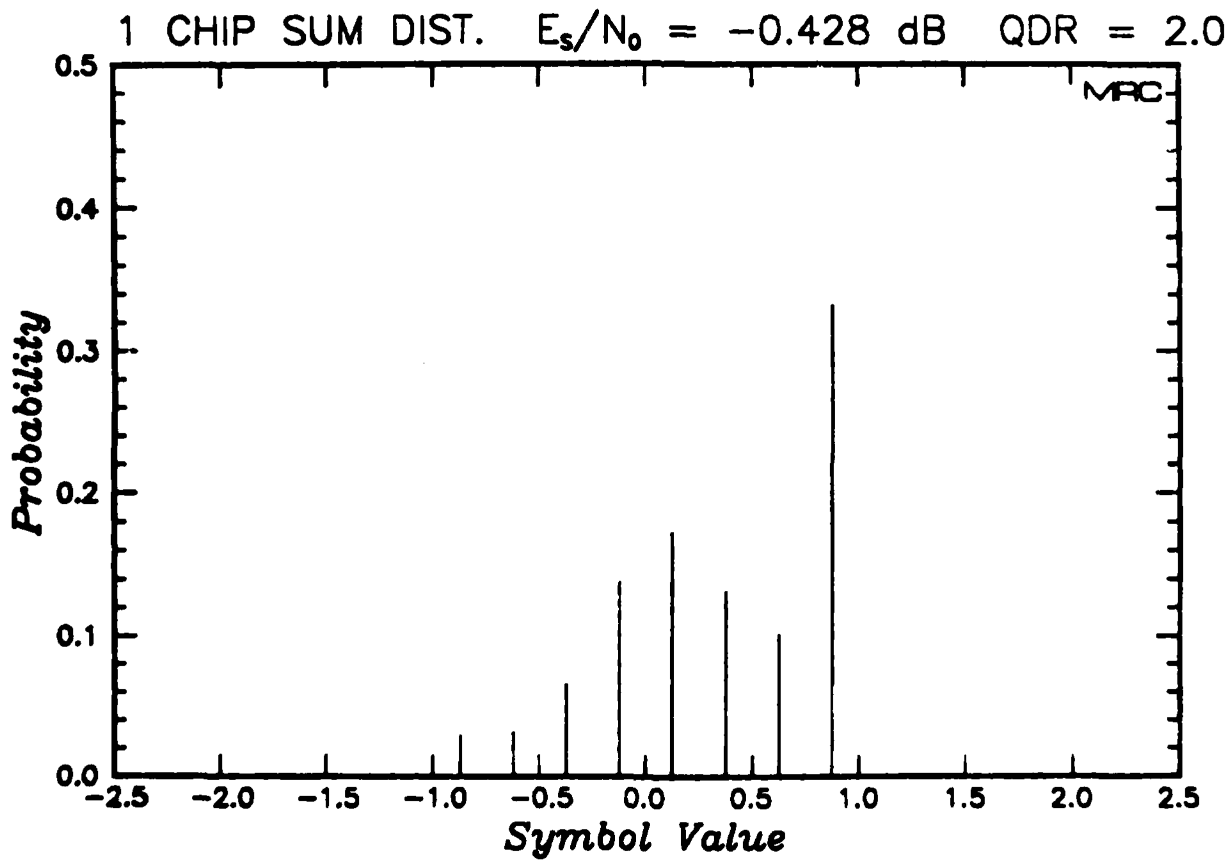

Figure 139. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -0.428 and normalized QDR of 2.0. (Applicable to Link 4)

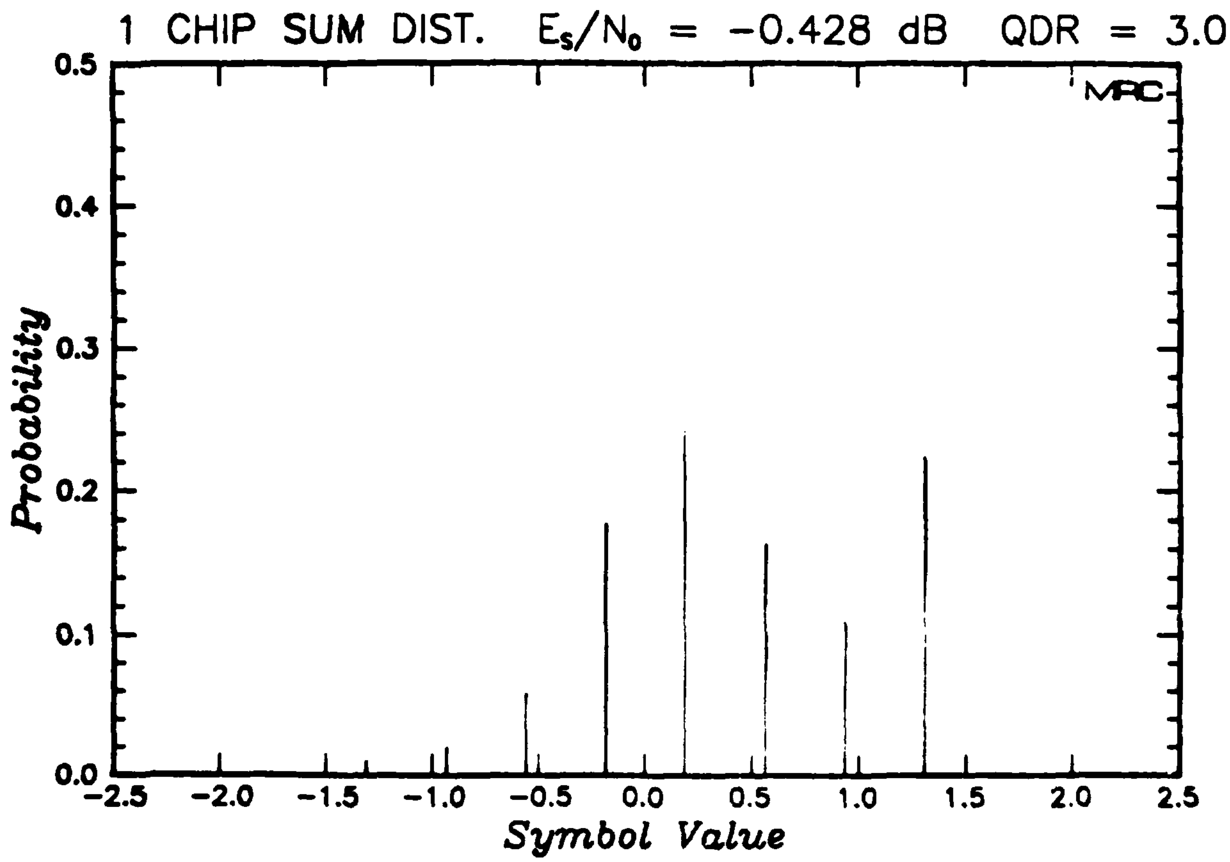

Figure 140. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_O = -0.428 and normalized QDR of 3.0. (Applicable to Link 4).

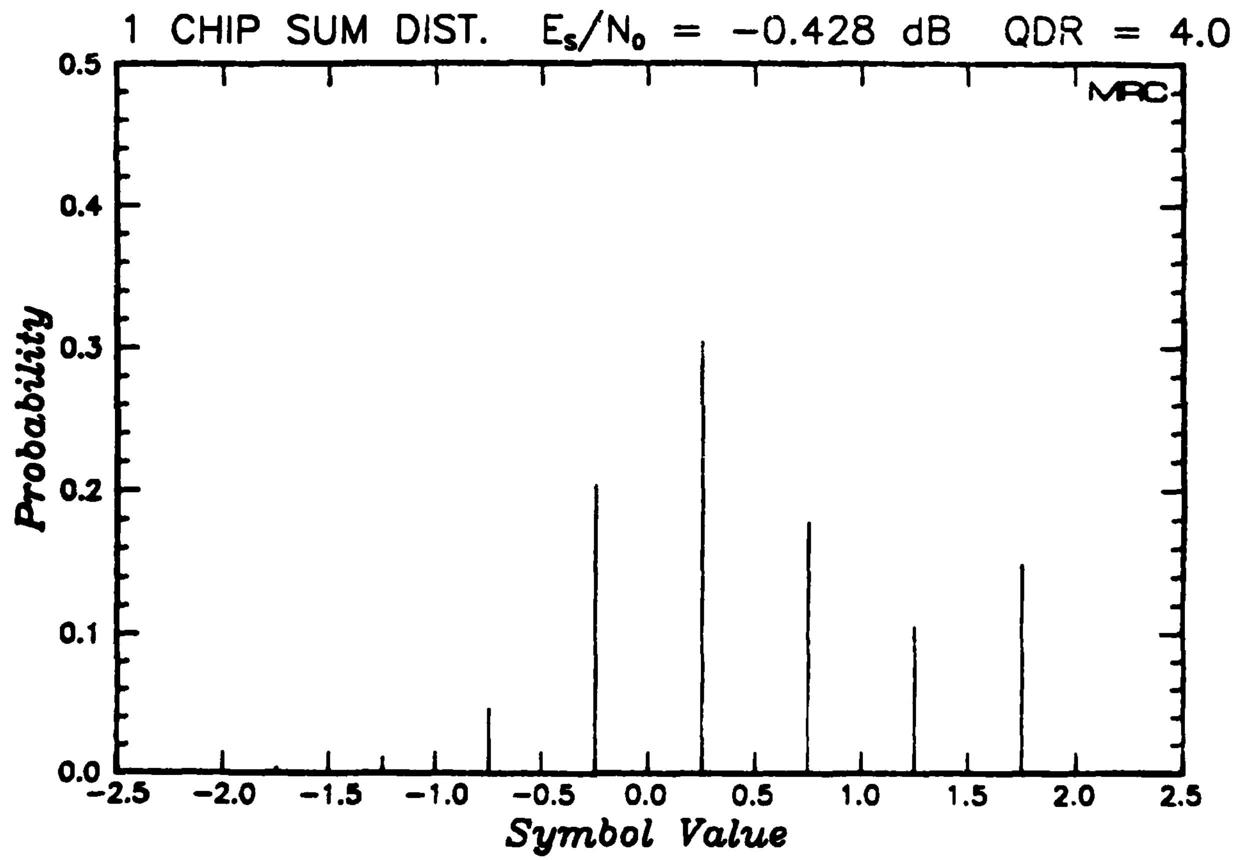

Figure 141. Measured probability distribution of quantized symbols under fading channel conditions for τ_o = 0.1 second and E_s/N_o = -0.428 and normalized QDR of 4.0. (Applicable to Link 4)

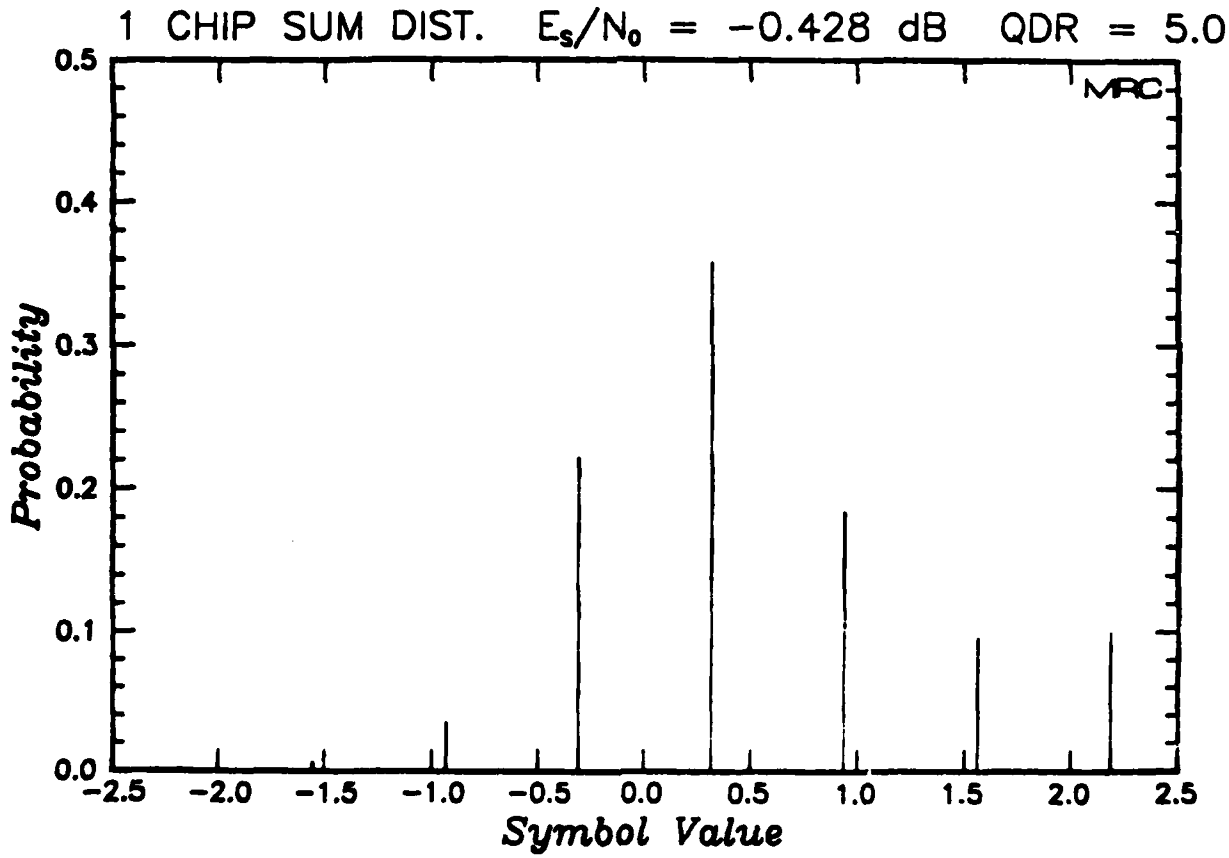

Figure 142. Measured probability distribution of quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_C = -0.428 and normalized QDR of 5.0. (Applicable to Link 4)

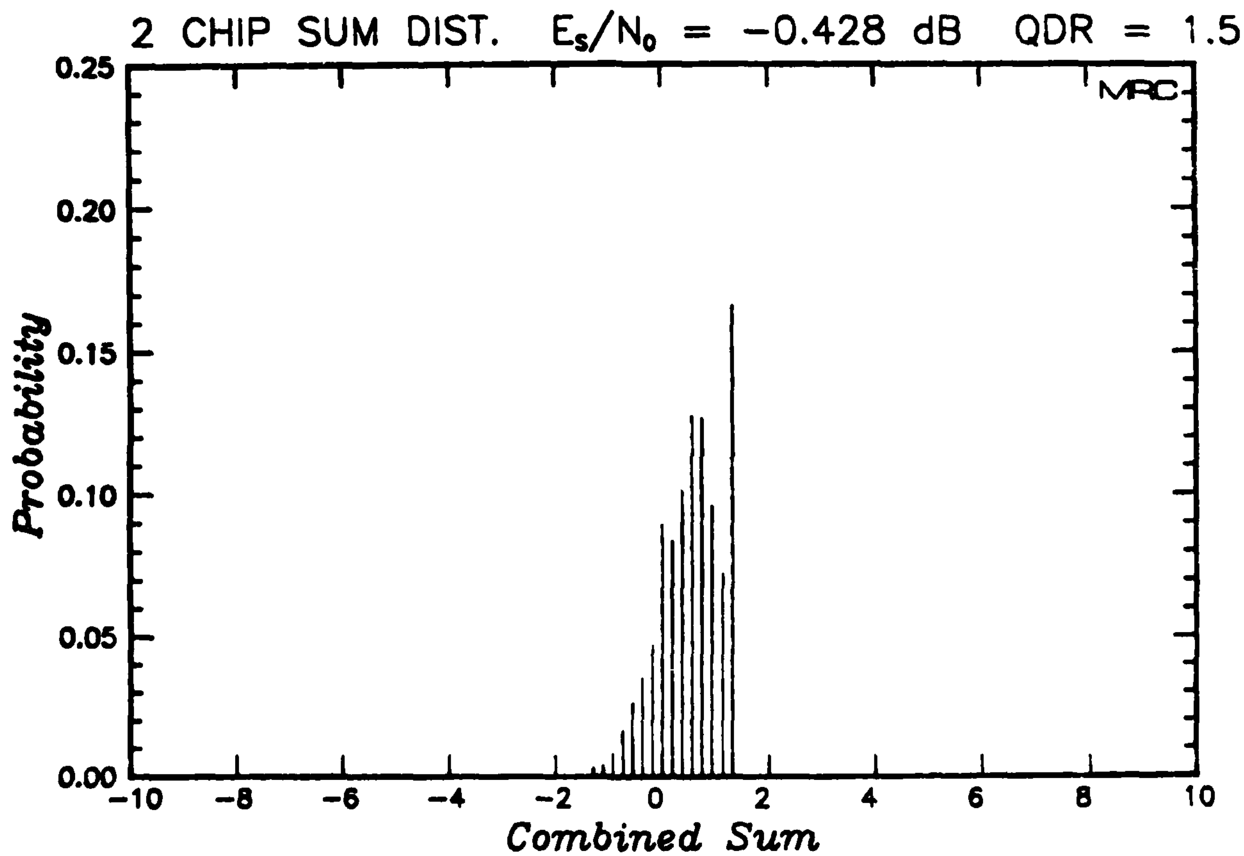

Figure 143. Measured probability distribution of tne two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 1.5. (Applicable to Link 3)

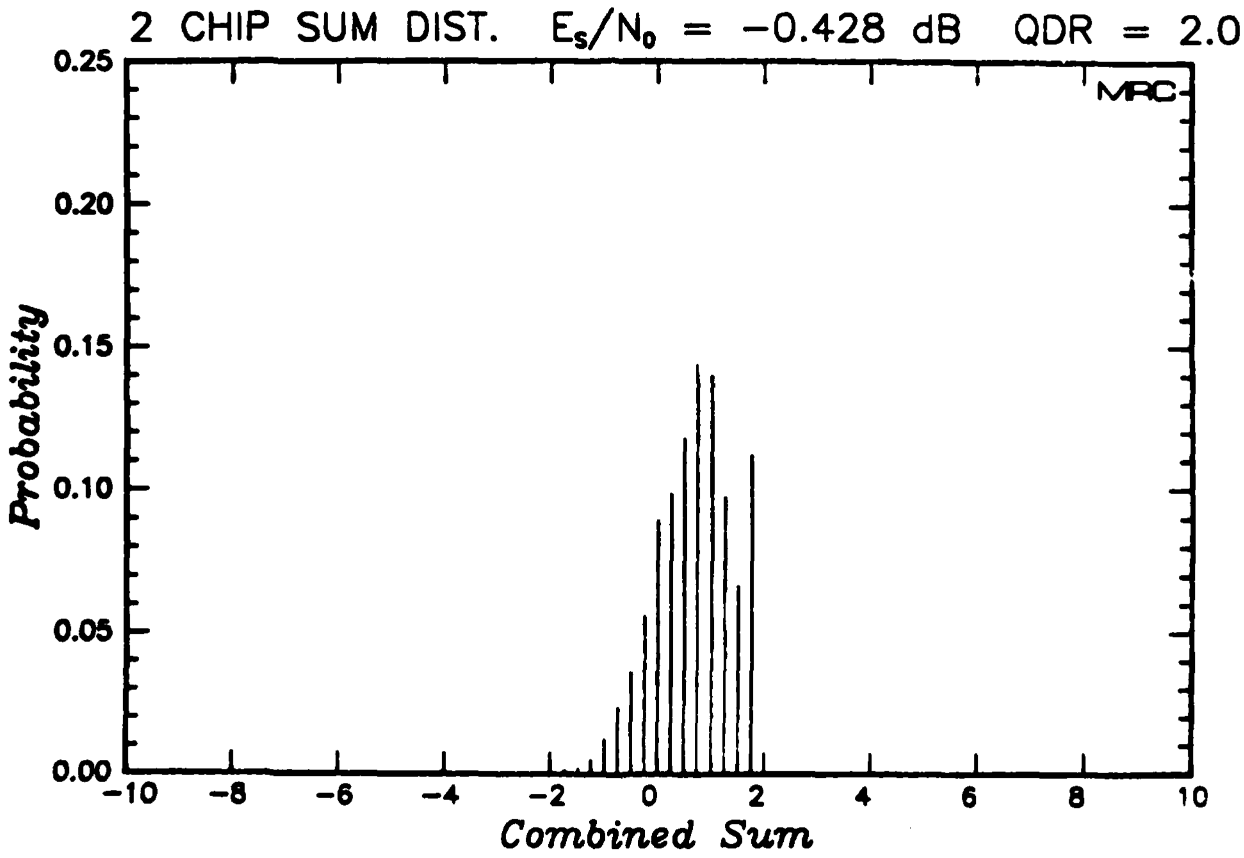

Figure 144. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 2.0. (Applicable to Link 3)

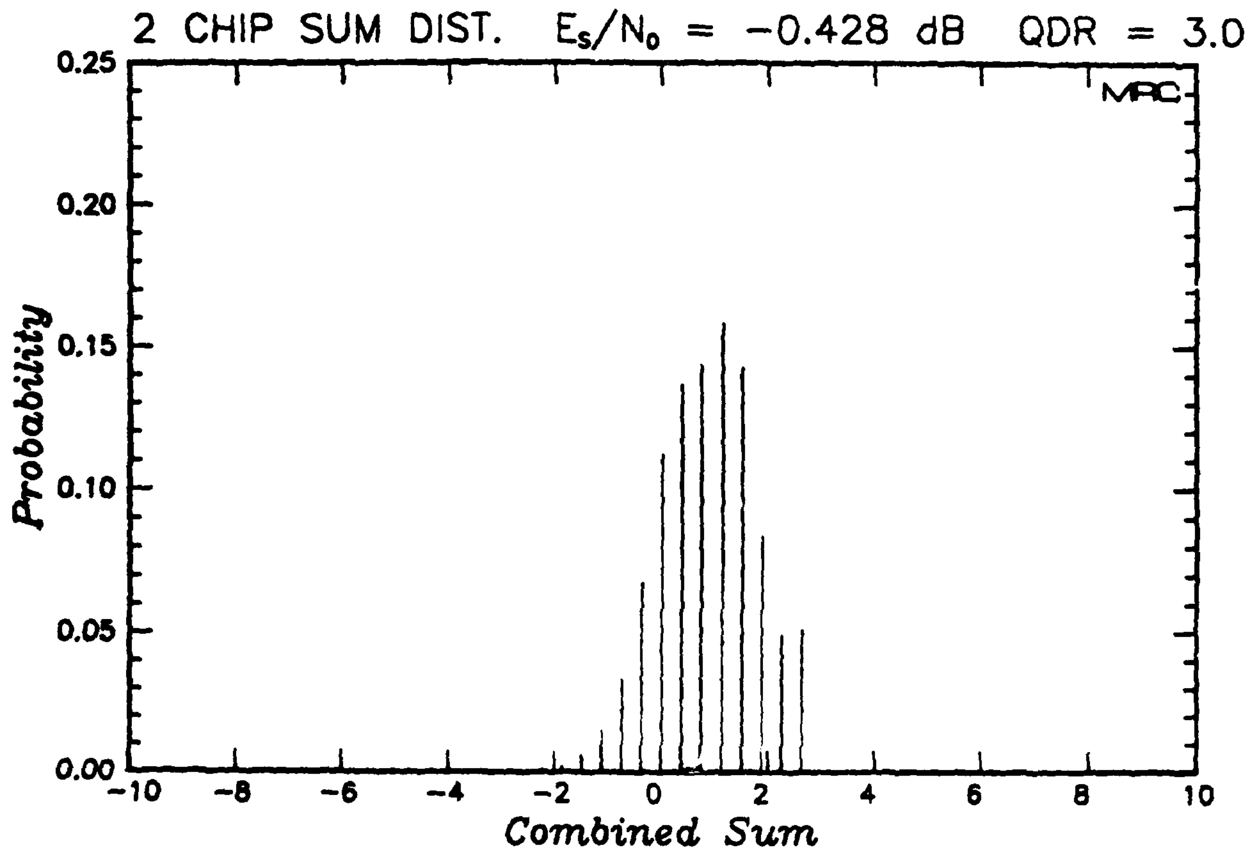

Figure 145. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 3.0. (Applicable to Link 3)

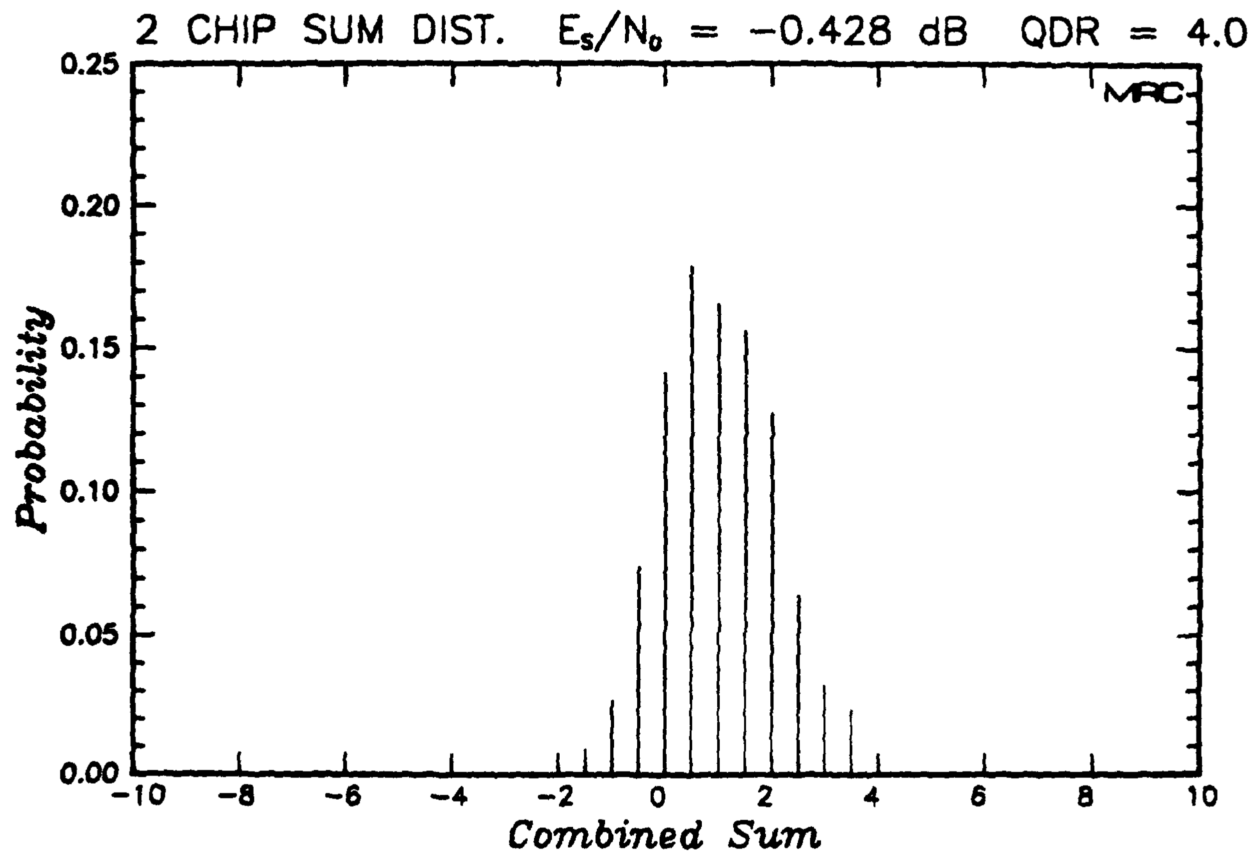

Figure 146. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_o = -0.428 and normalized QDR of 4.0. (Applicable to Link 3)

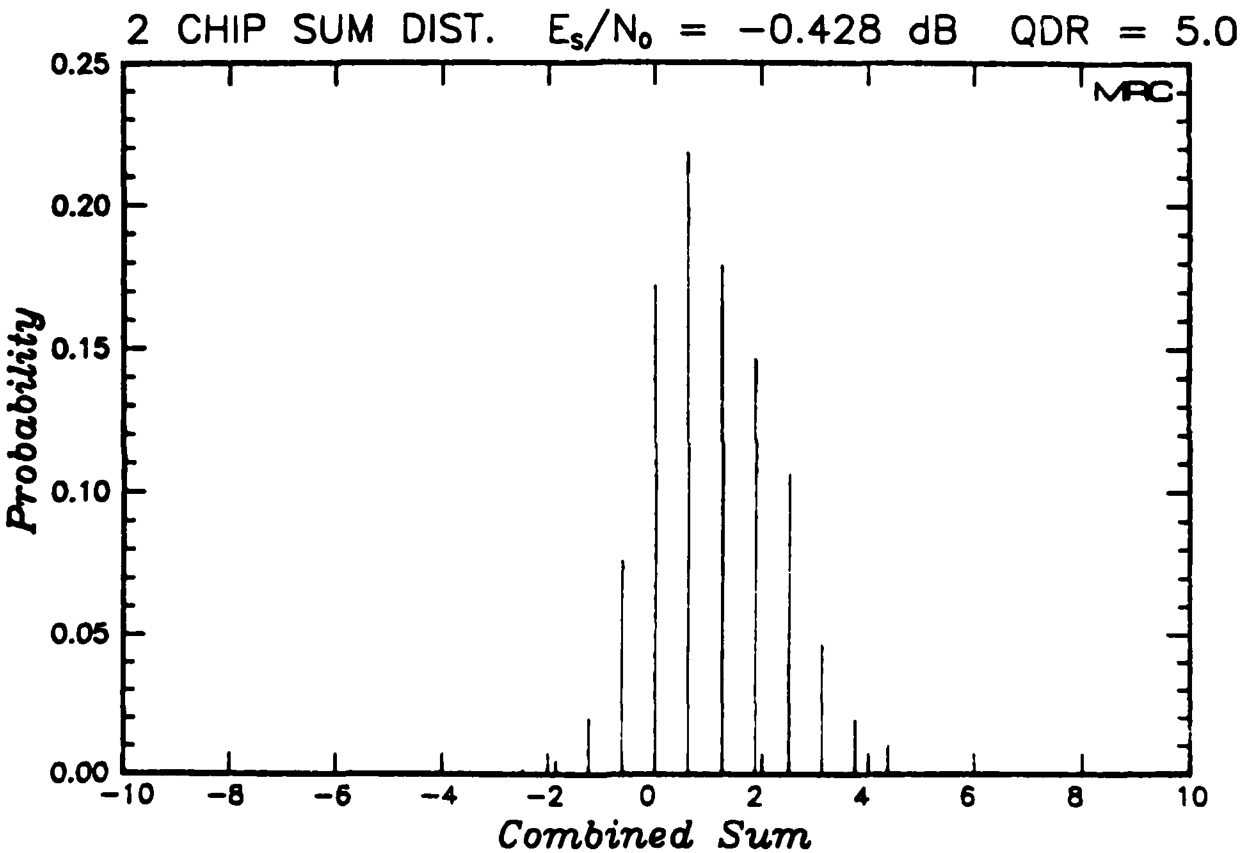

Figure 147. Measured probability distribution of the two-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 5.0. (Applicable to Link 3)

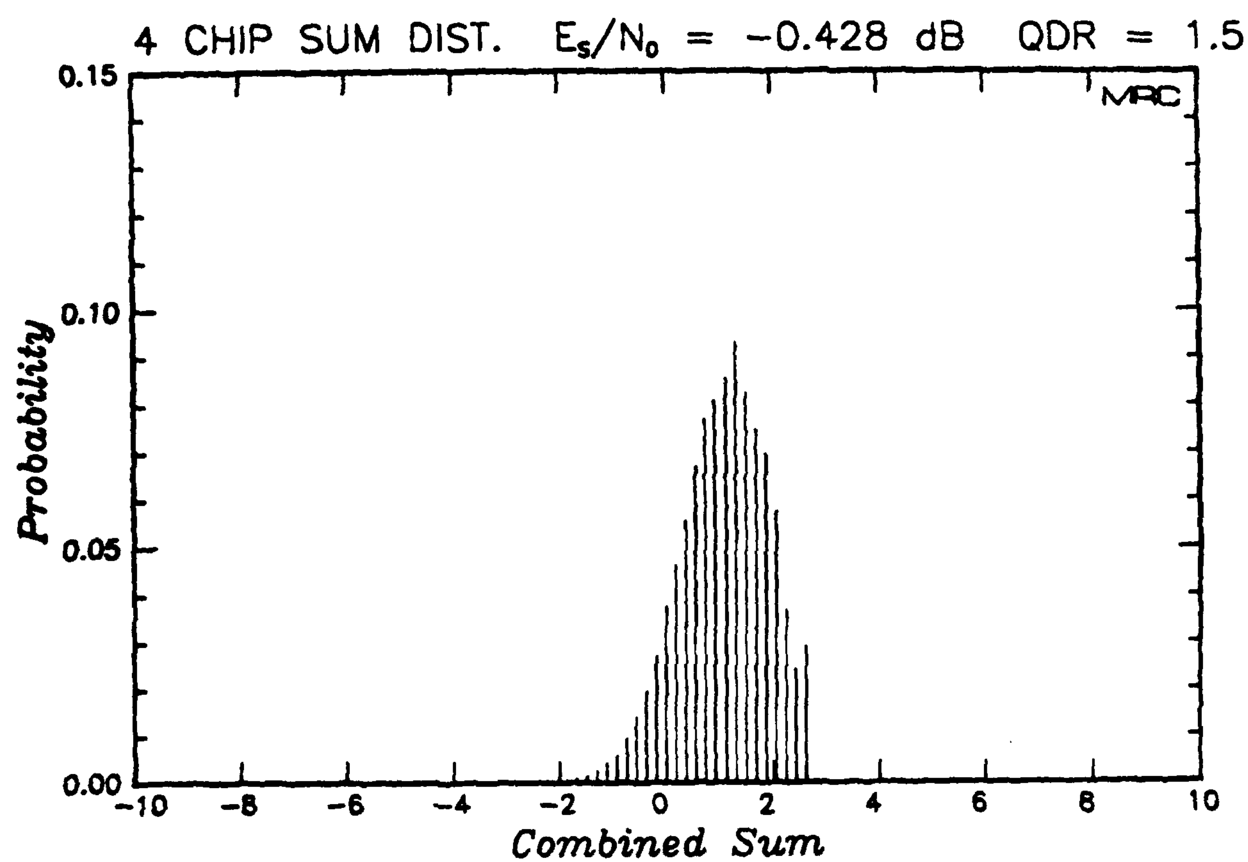

Figure 148. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_o = -0.428 and normalized QDR of 1.5. (Applicable to Link 2)

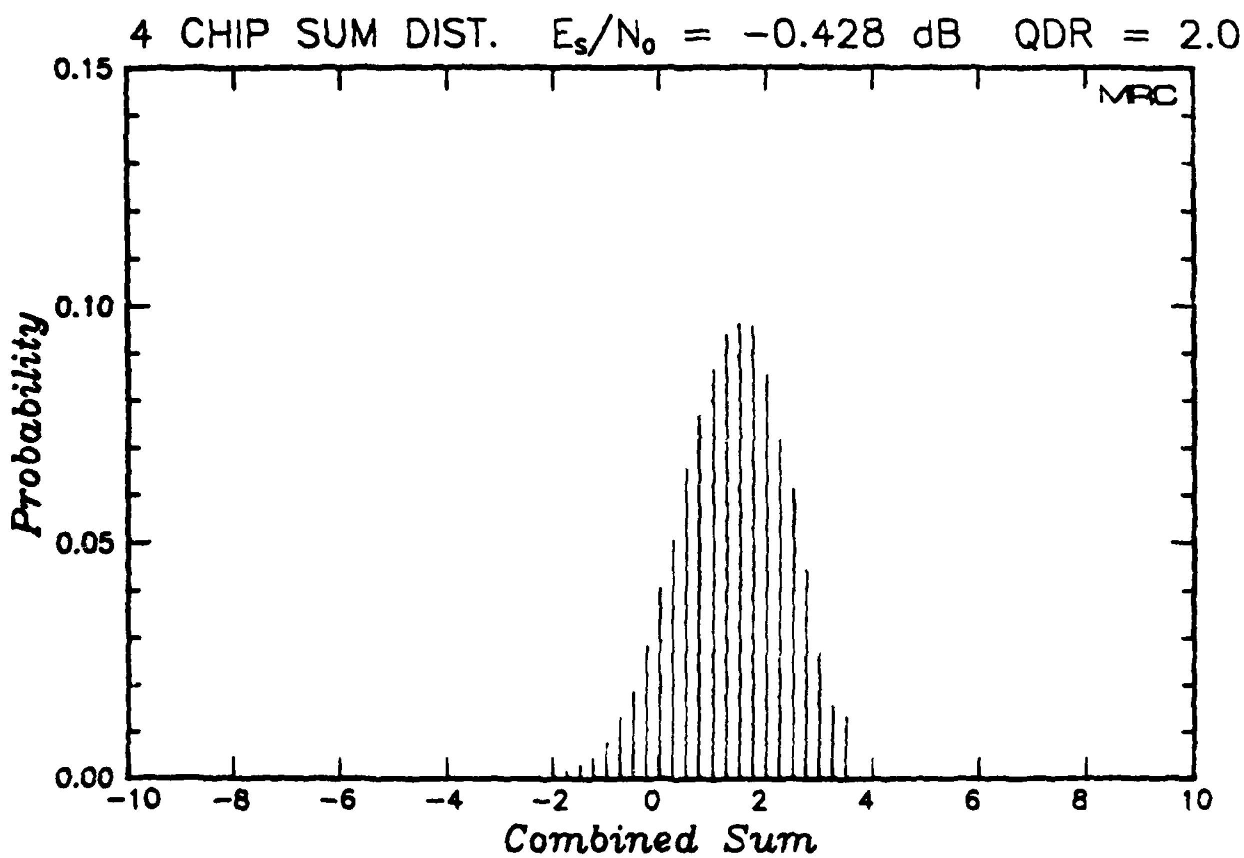

Figure 149. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 2.0. (Applicable to Link 2)

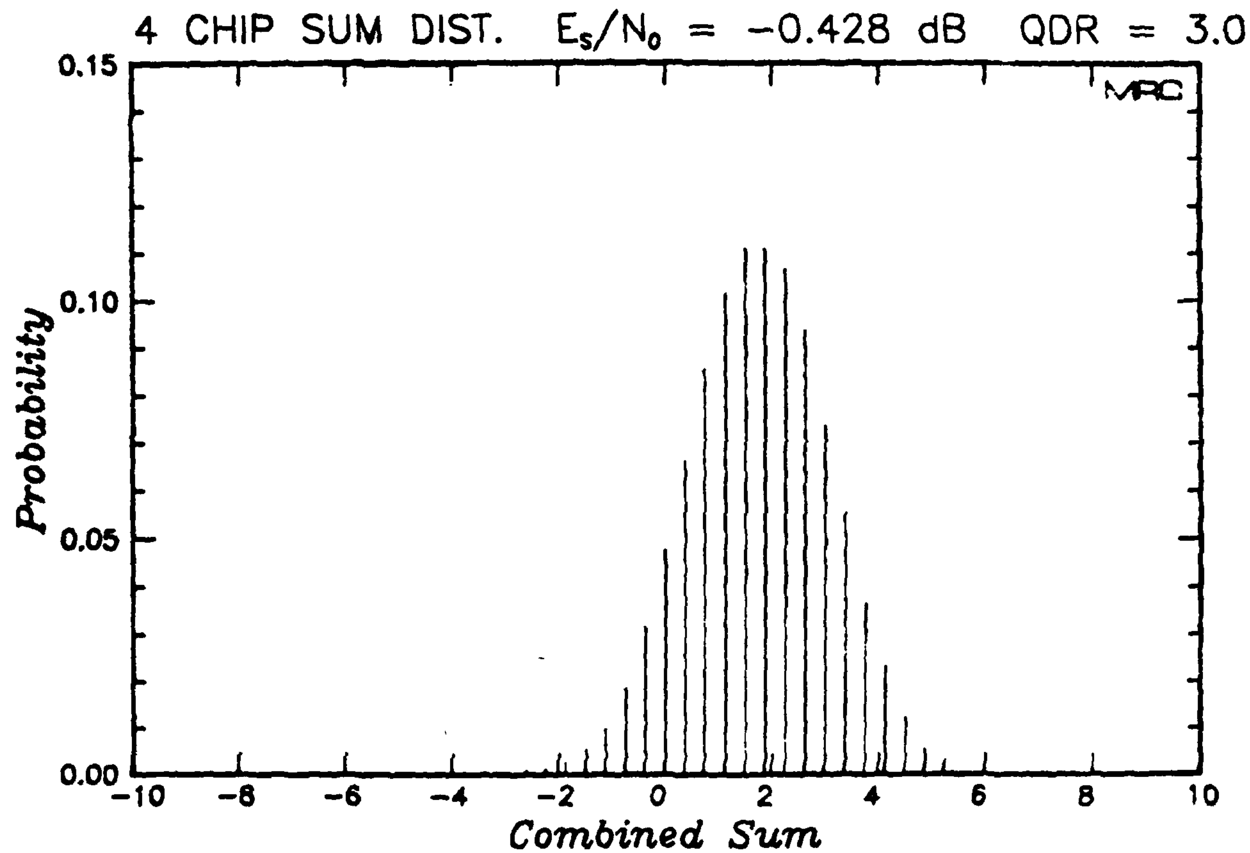

Figure 150. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 3.0. (Applicable to Link 2)

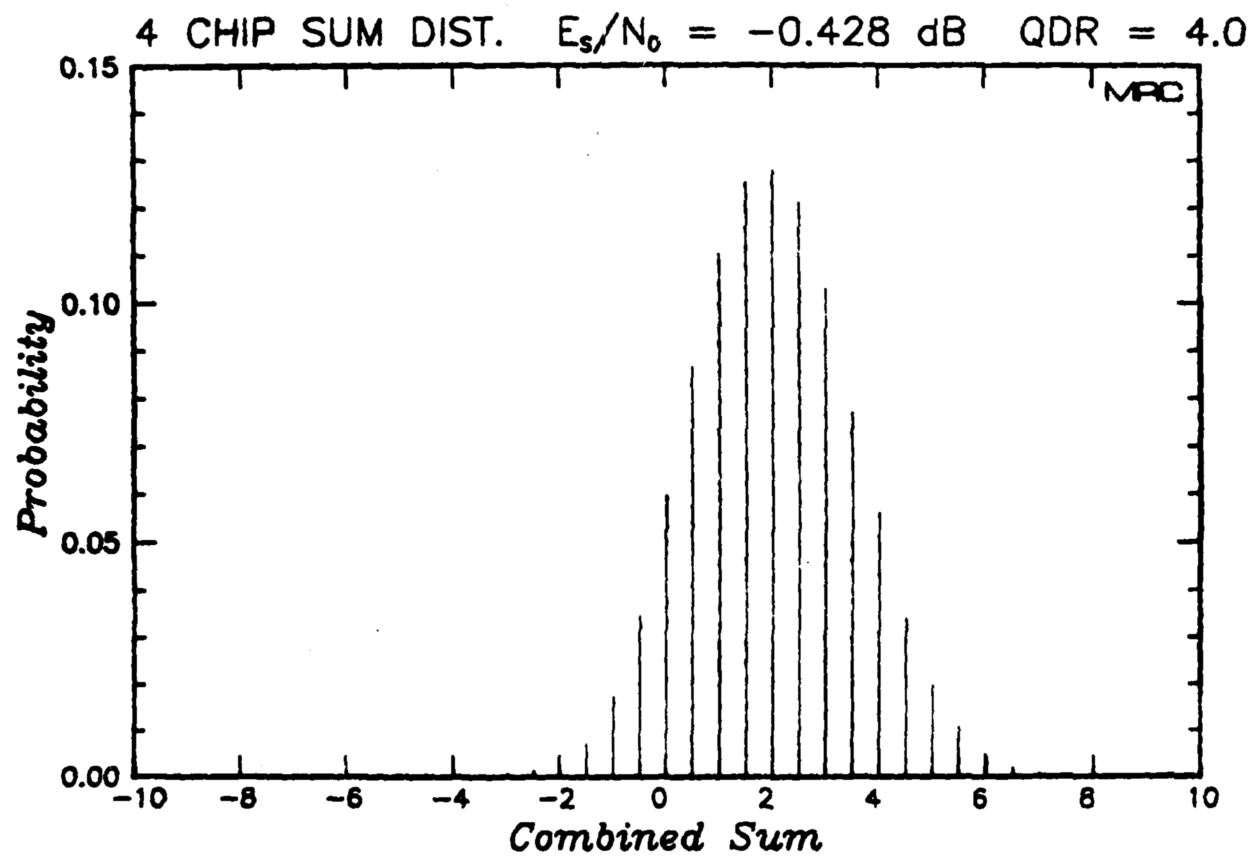

Figure 151. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 4.0. (Applicable to Link 2)

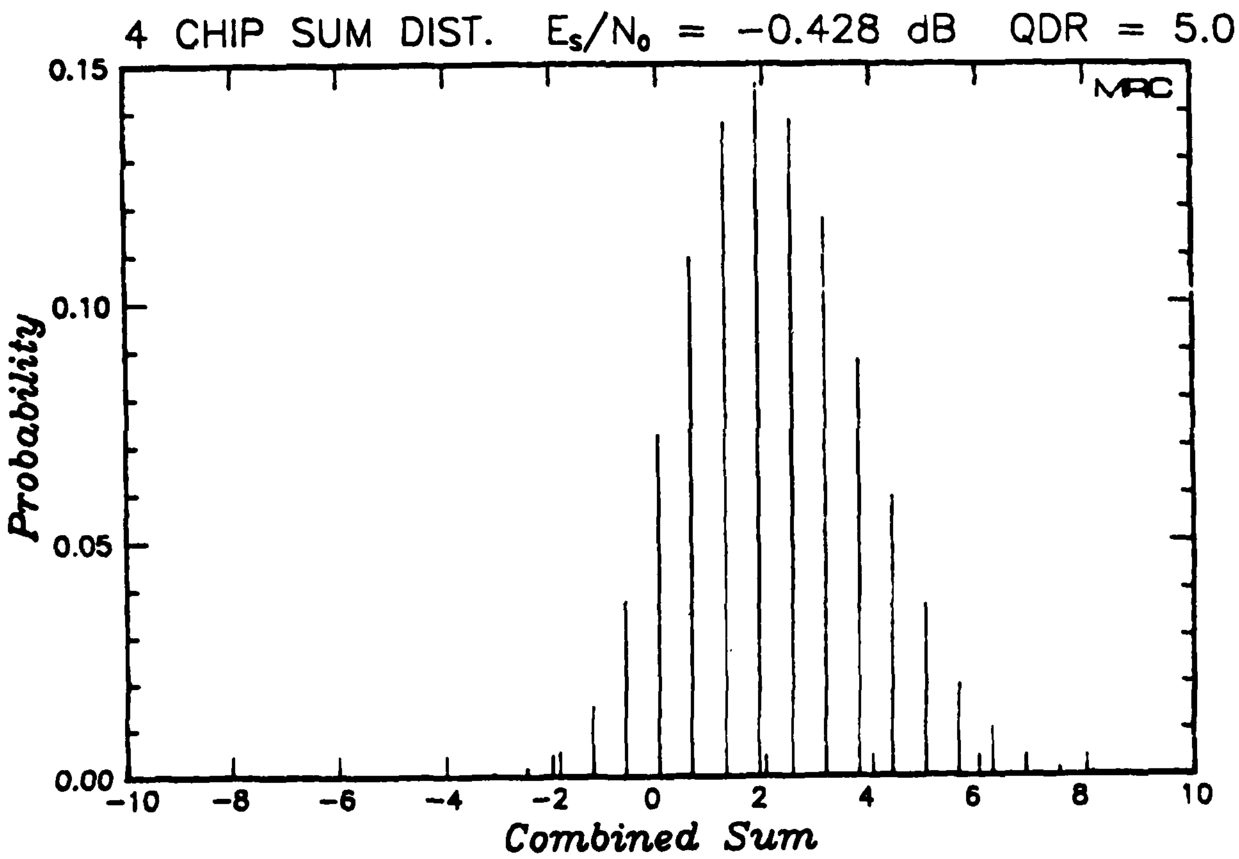

Figure 152. Measured probability distribution of the four-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 5.0. (Applicable to Link 2)

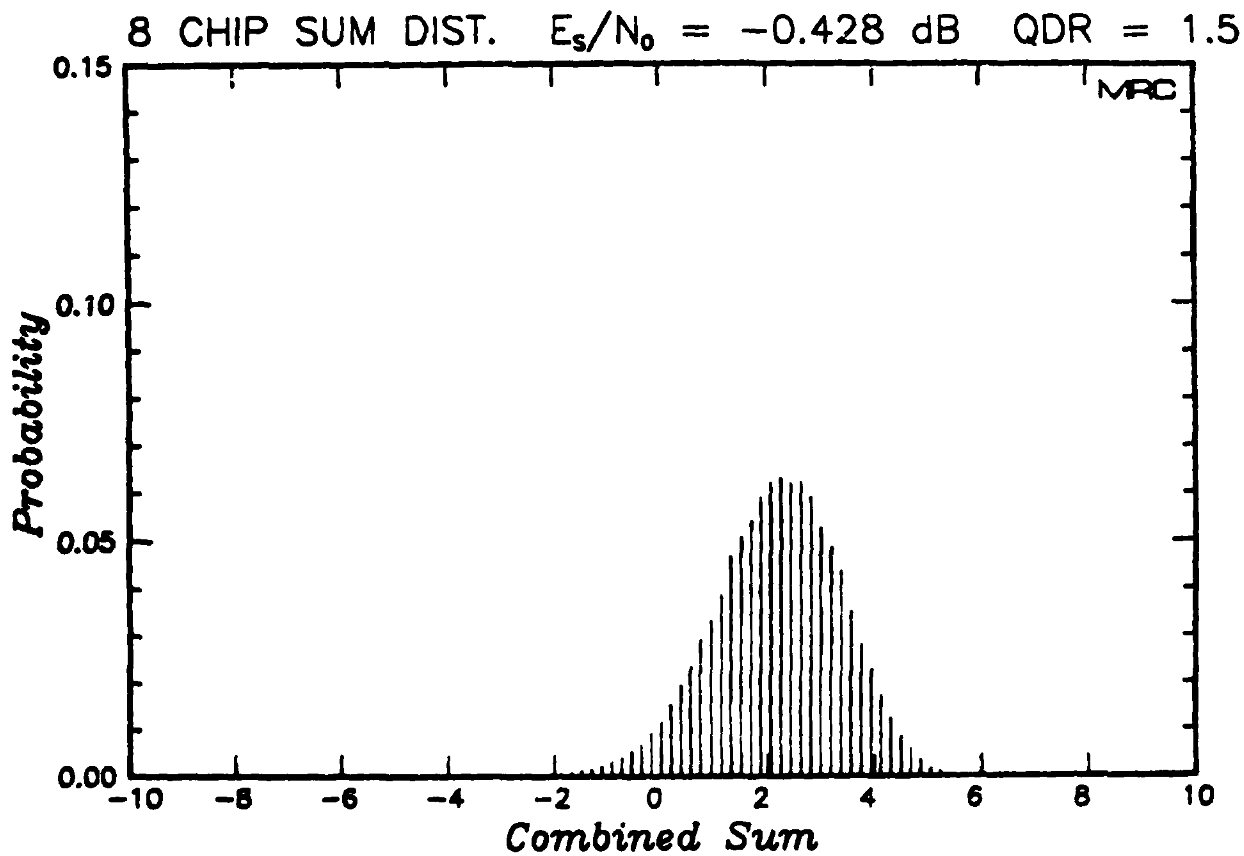

Figure 153. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 1.5. (Applicable to Link 1)

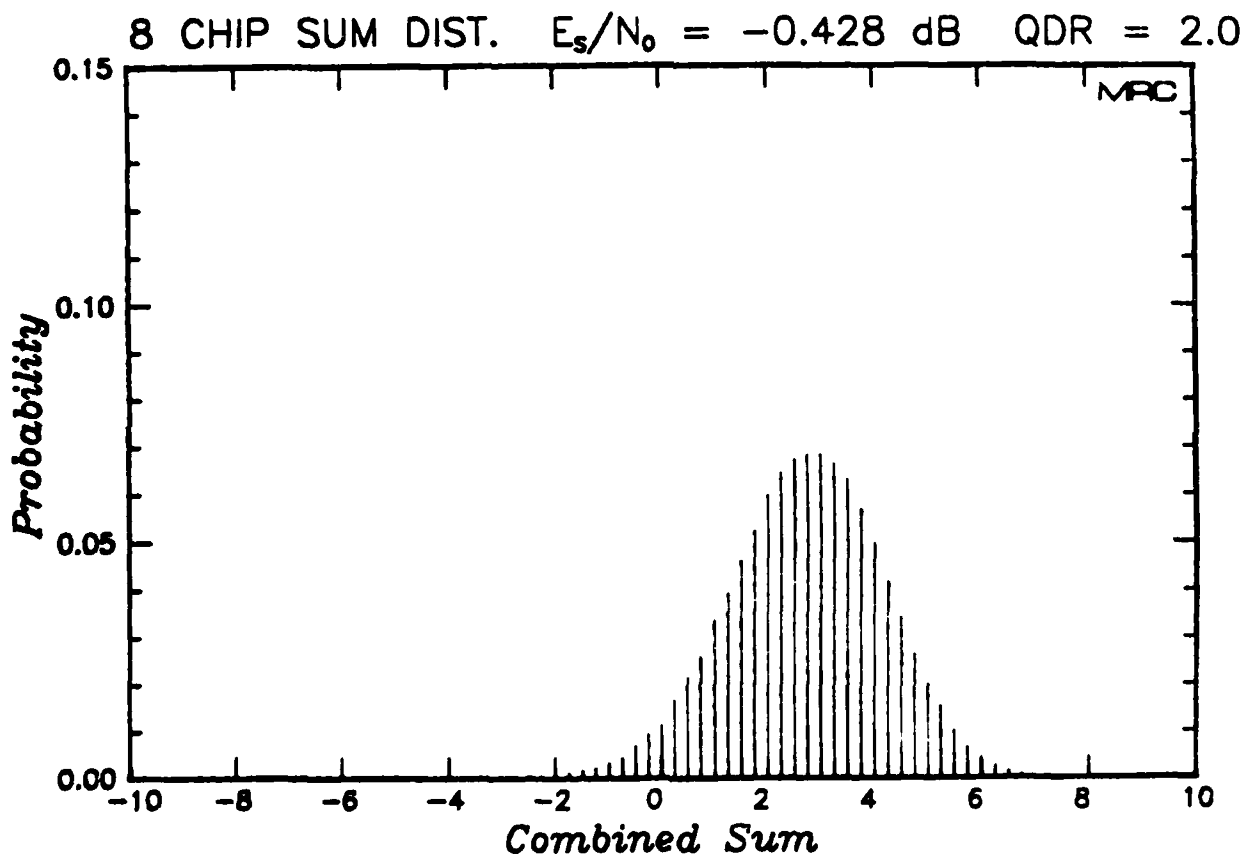

Figure 154. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -0.428 and normalized QDR of 2.0. (Applicable to Link 1)

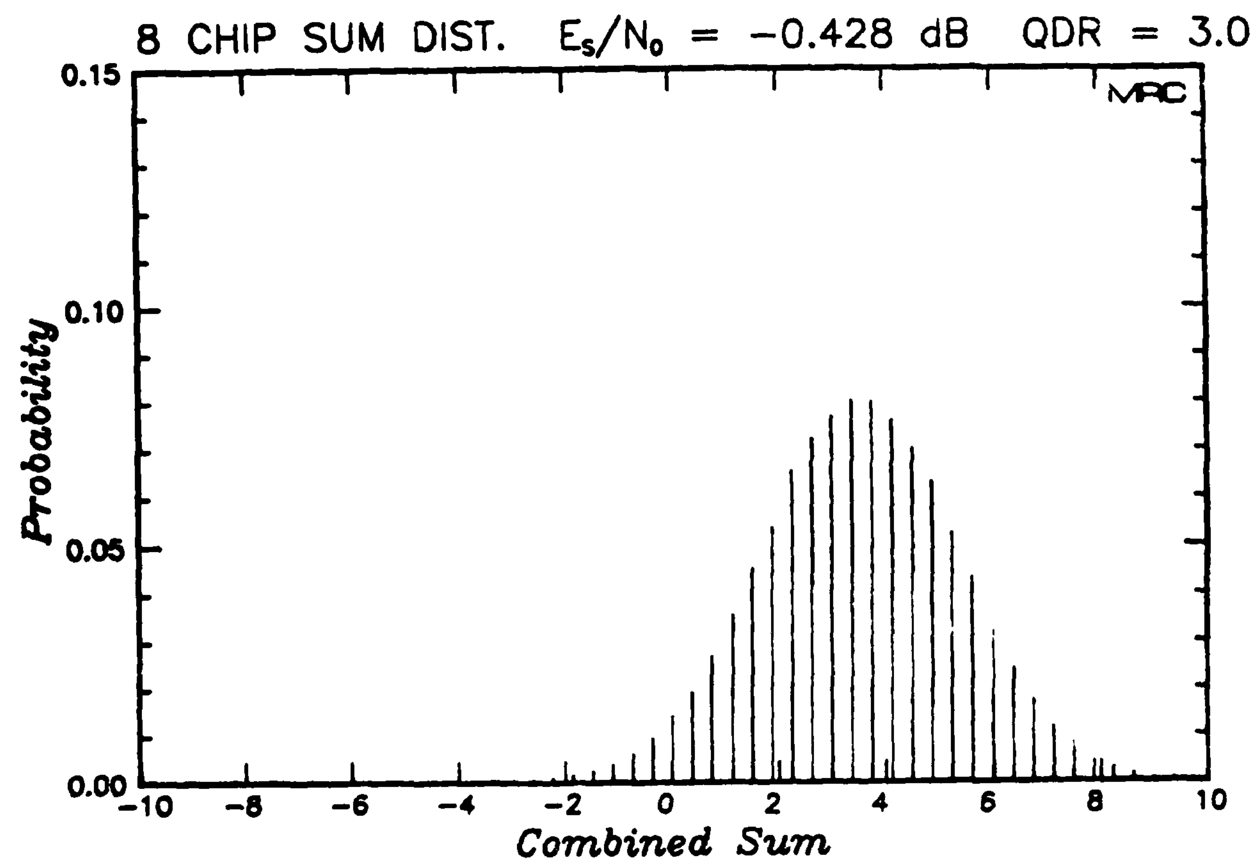

Figure 155. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 3.0. (Applicable to Link 1)

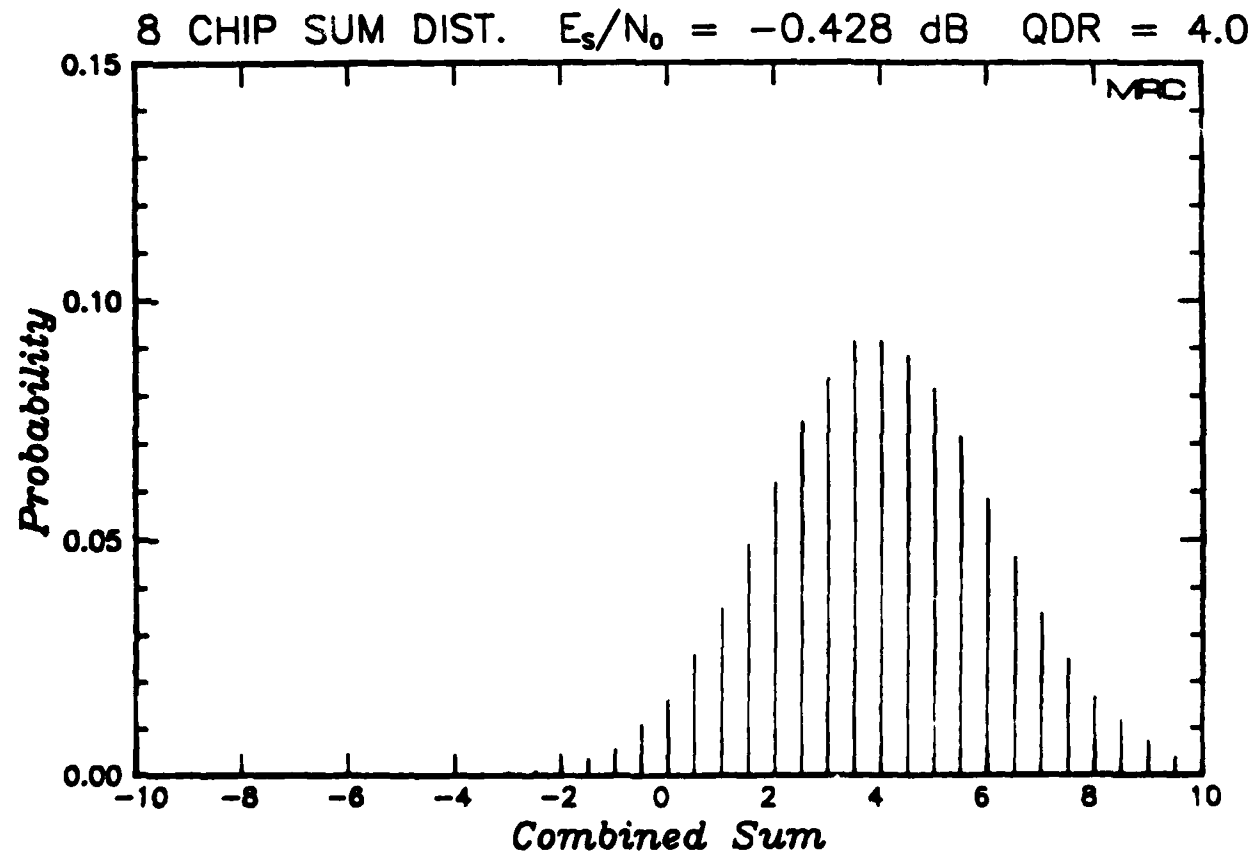

Figure 156. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_S/N_0 = -0.428 and normalized QDR of 4.0. (Applicable to Link 1)

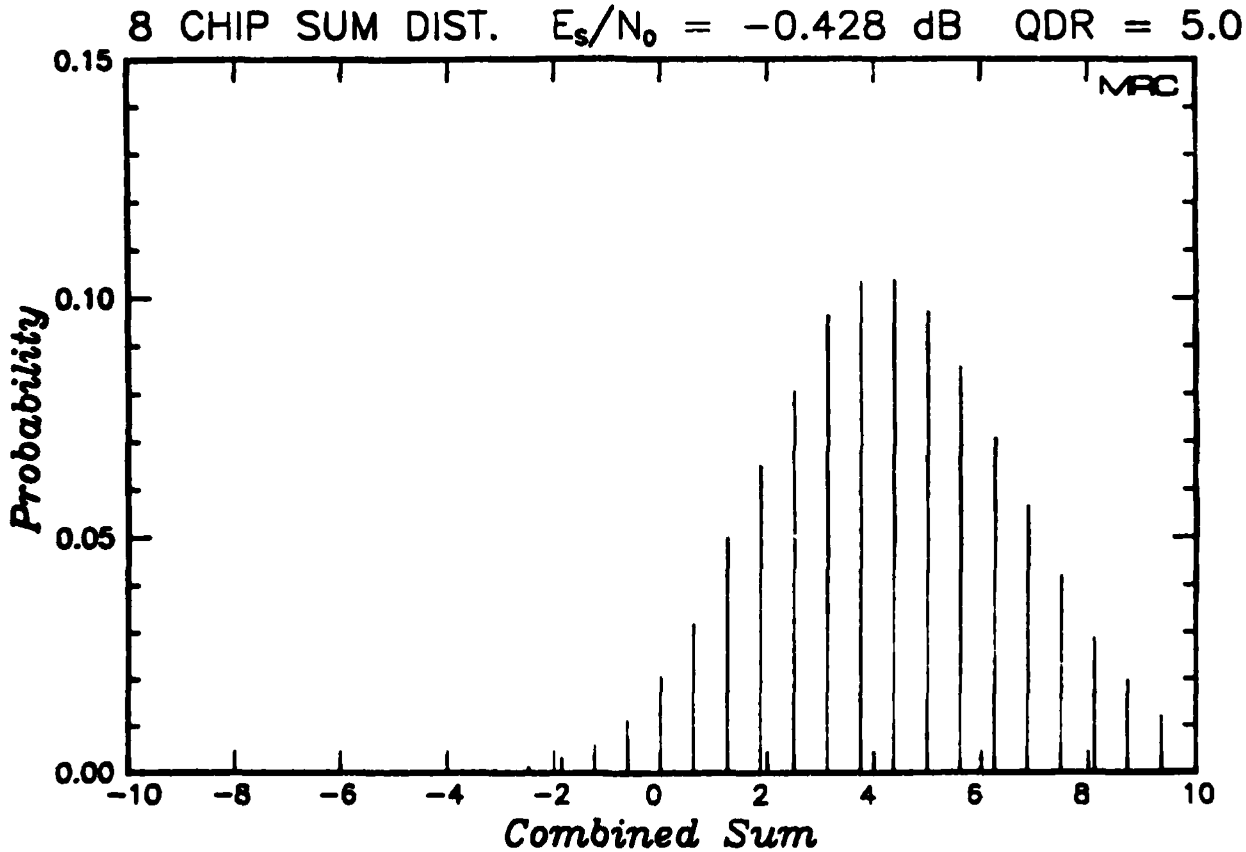

Figure 157. Measured probability distribution of the eight-chip combined quantized symbols under fading channel conditions for τ_0 = 0.1 second and E_s/N_0 = -0.428 and normalized QDR of 5.0. (Applicable to Link 1)

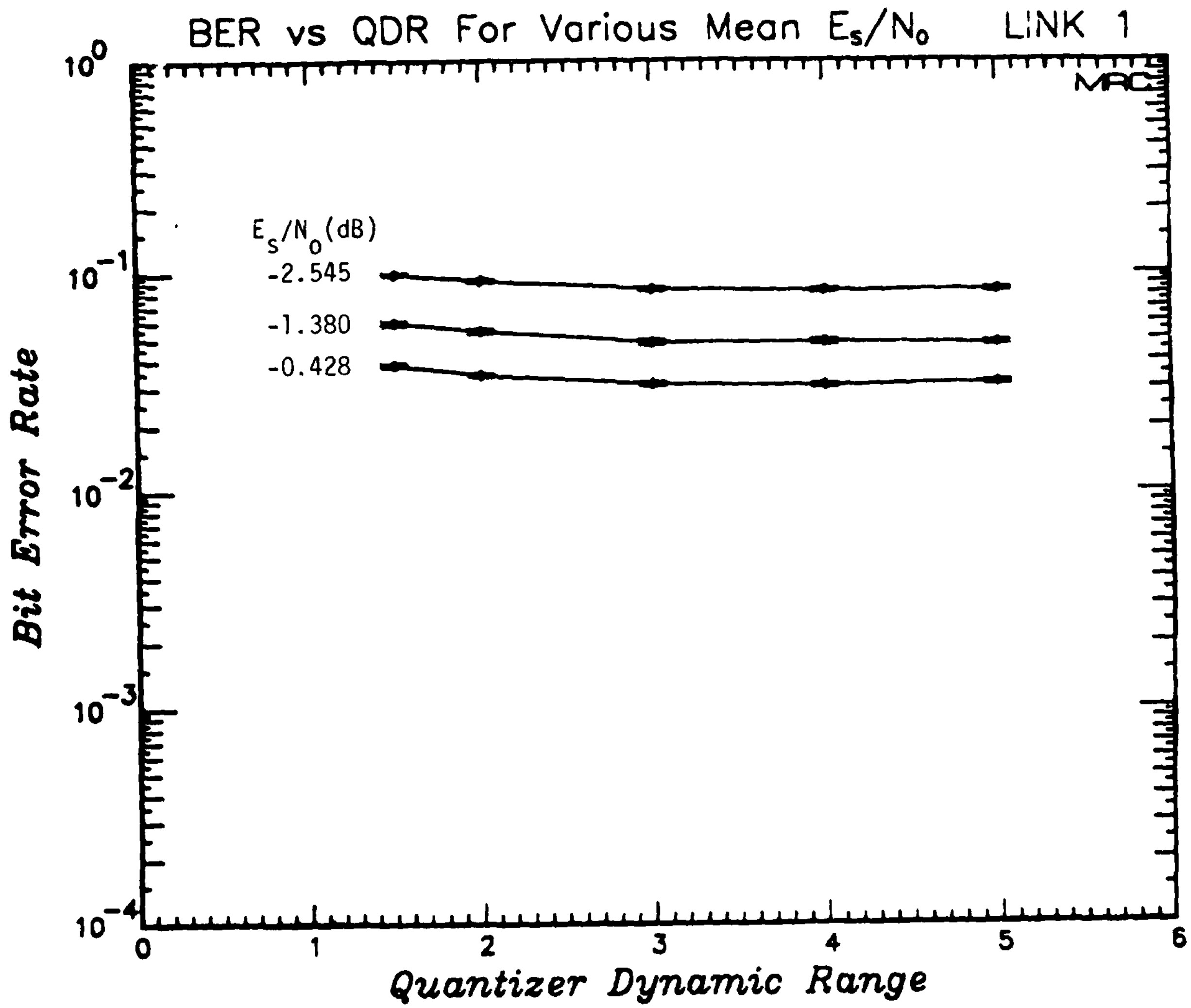

Figure 158. Information bit error rate for Link 1 under fading channel conditions versus normalized QDR for the values of E_s/N_0.

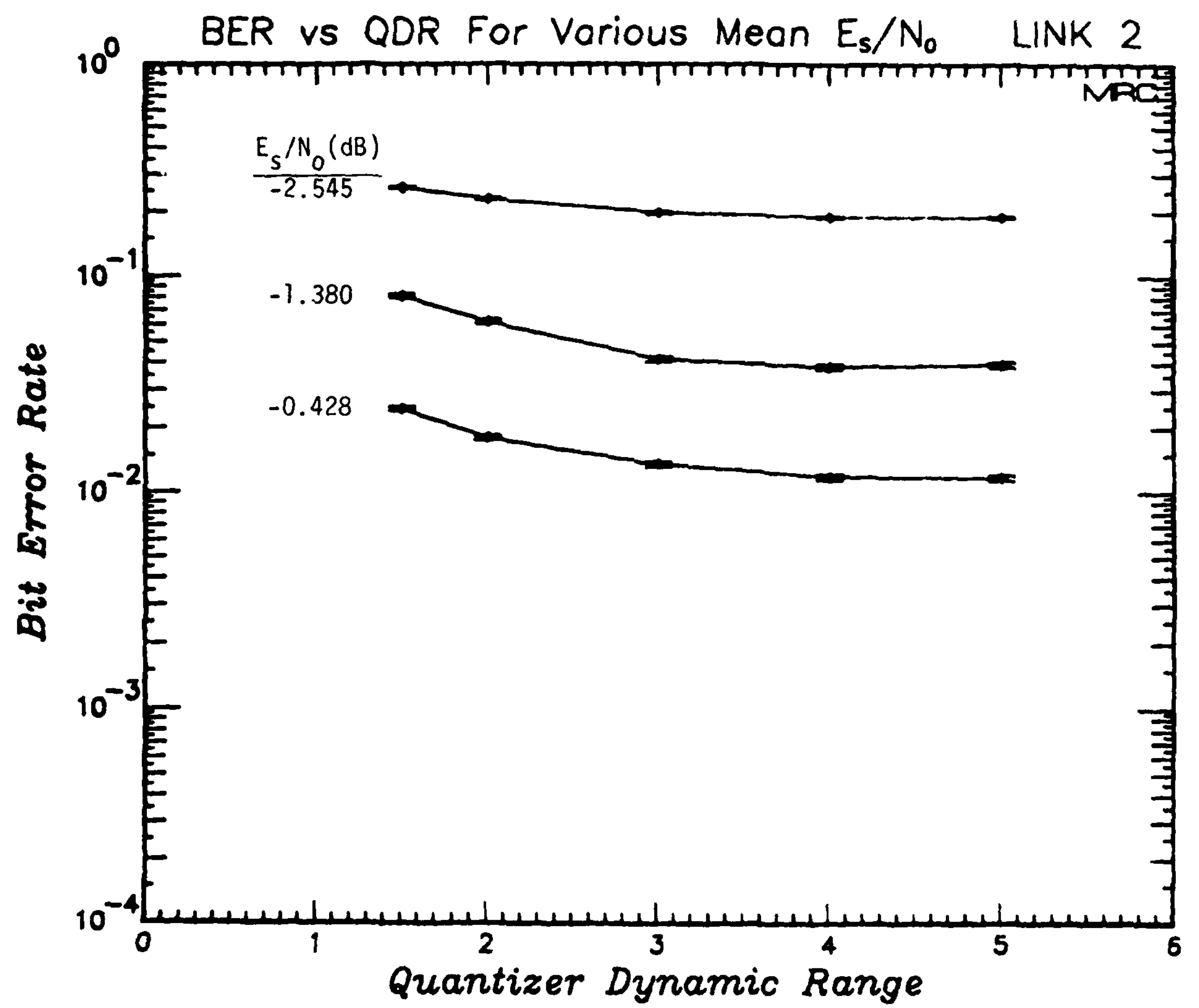

Figure 159. Information bit error rate for Link 2 under fading channel conditions versus normalized QDR for the values of E_s/N_O.

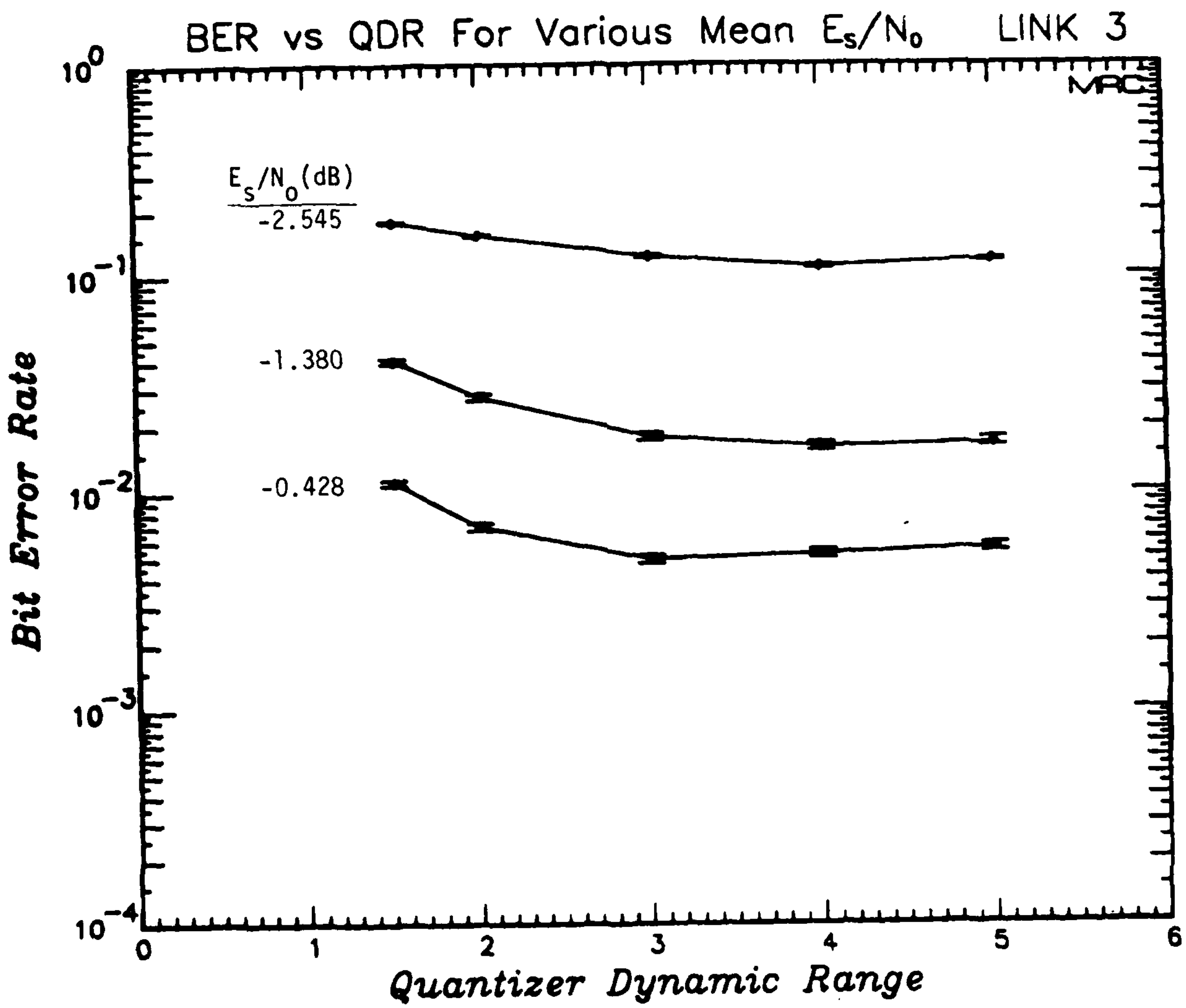

Figure 160. Information bit error rate for Link 3 under fading channel conditions versus normalized QDR for the values of E_S/N_O.

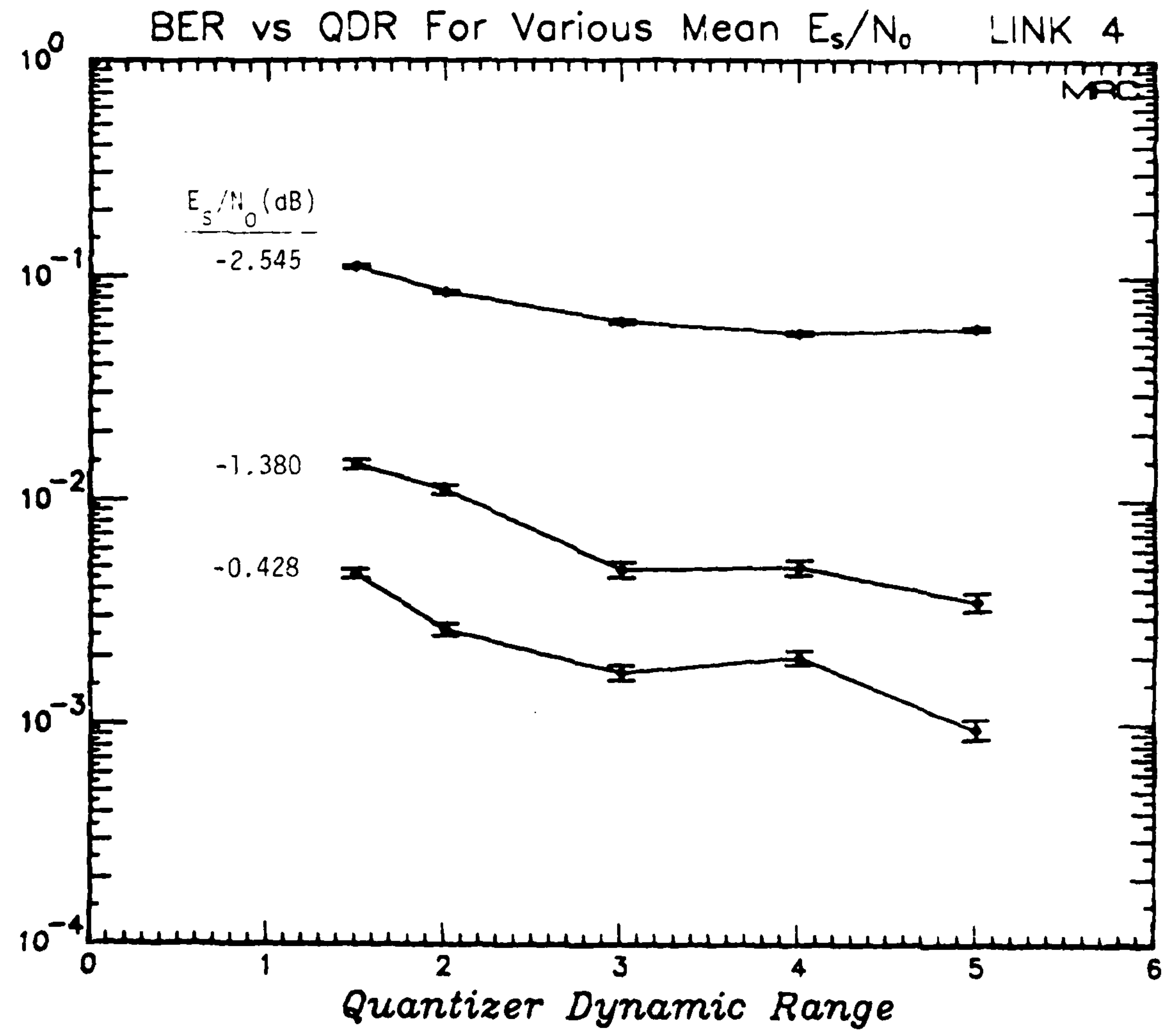

Figure 161. Information bit error rate for Link 4 under fading channel conditions versus normalized QDR for the values of E_s/N_0.

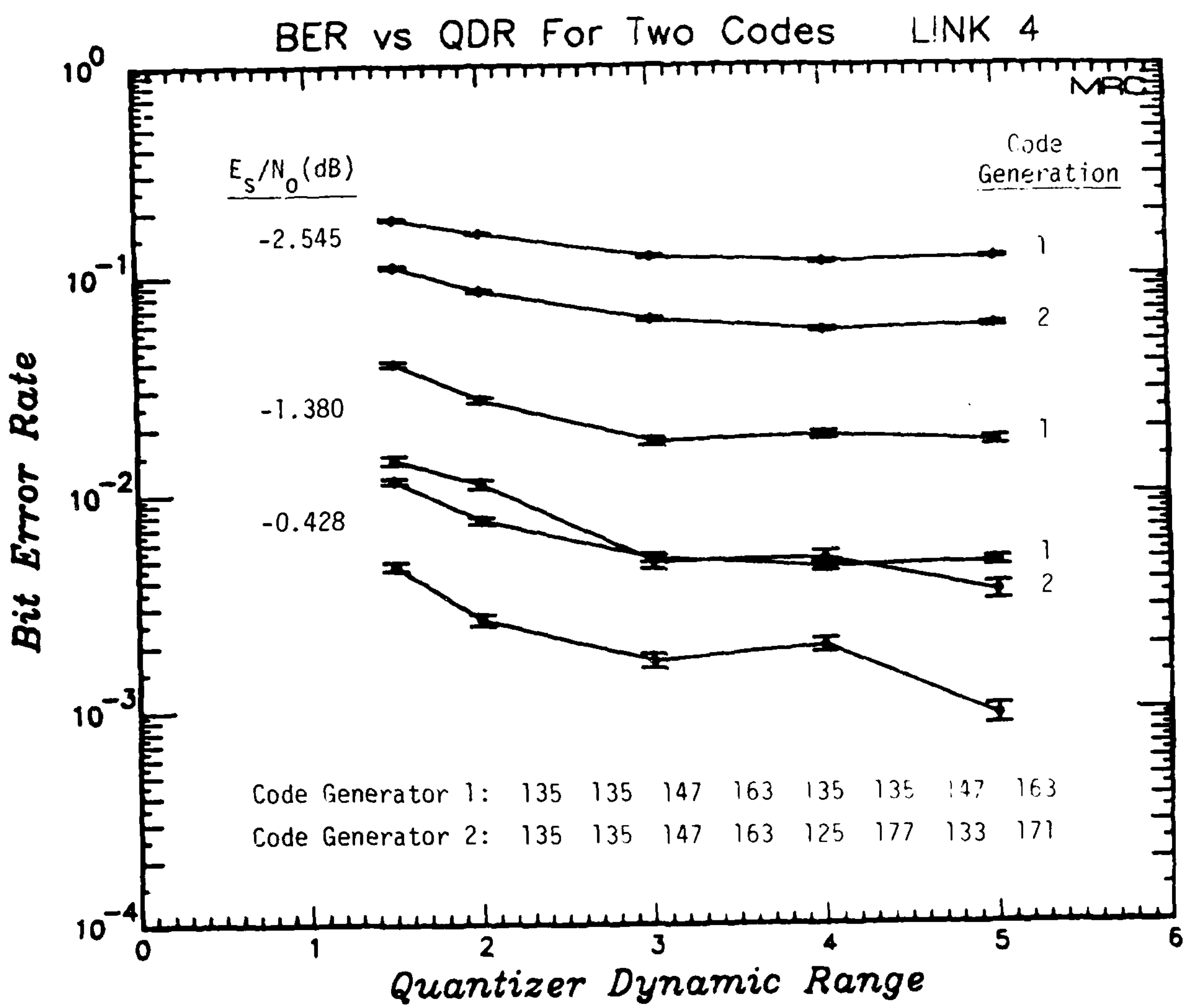

Figure 162. Performance comparison of two rate 1/8, constraint length 7 convolutional codes with df of 40 utilized in Link 4 under fading channel conditions versus normalized QDR for t values of E_S/N_O.

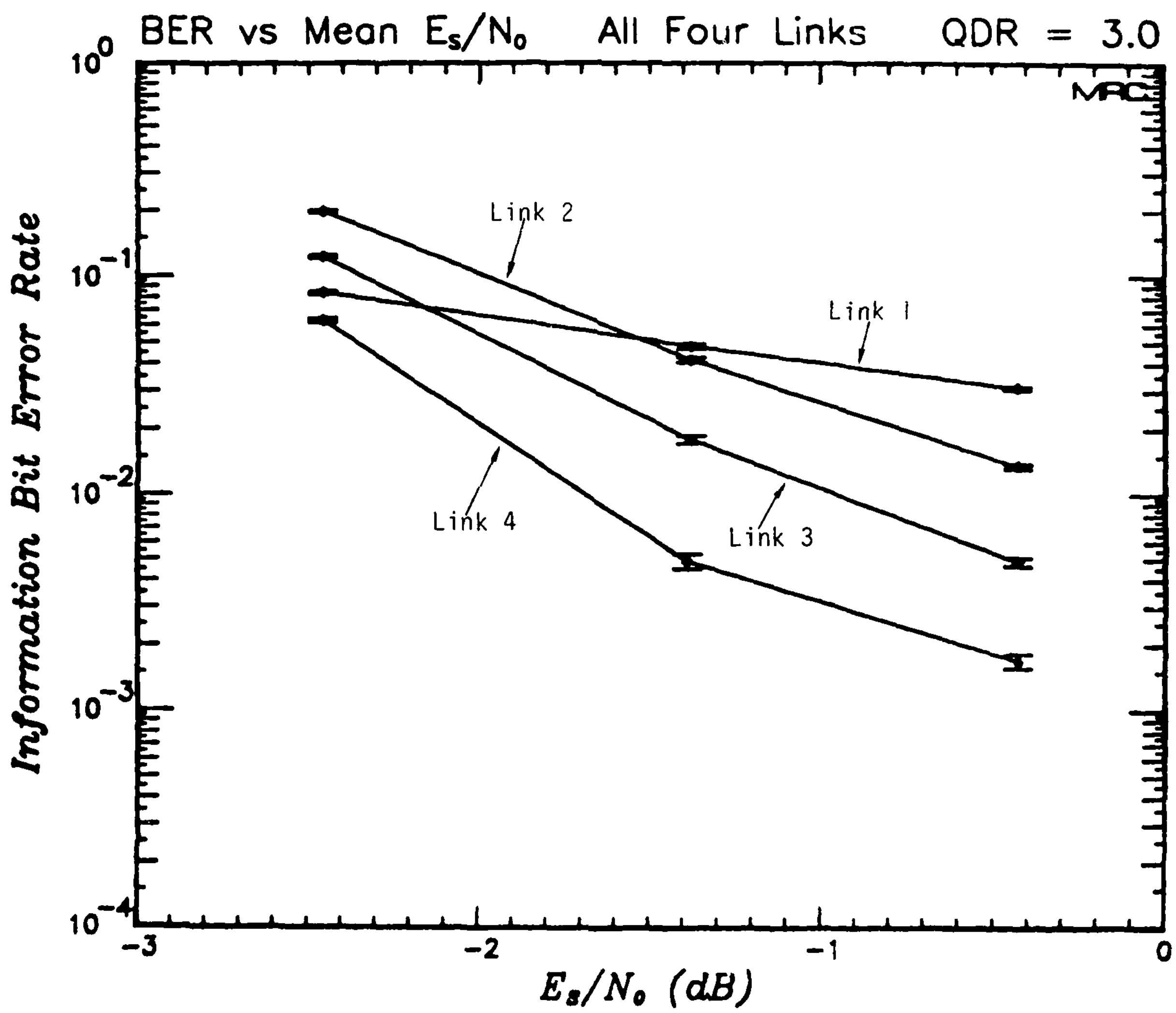

Figure 163. Information bit error rate for all links under fading channel conditions versus E_S/N_O for QDR = 3.0.

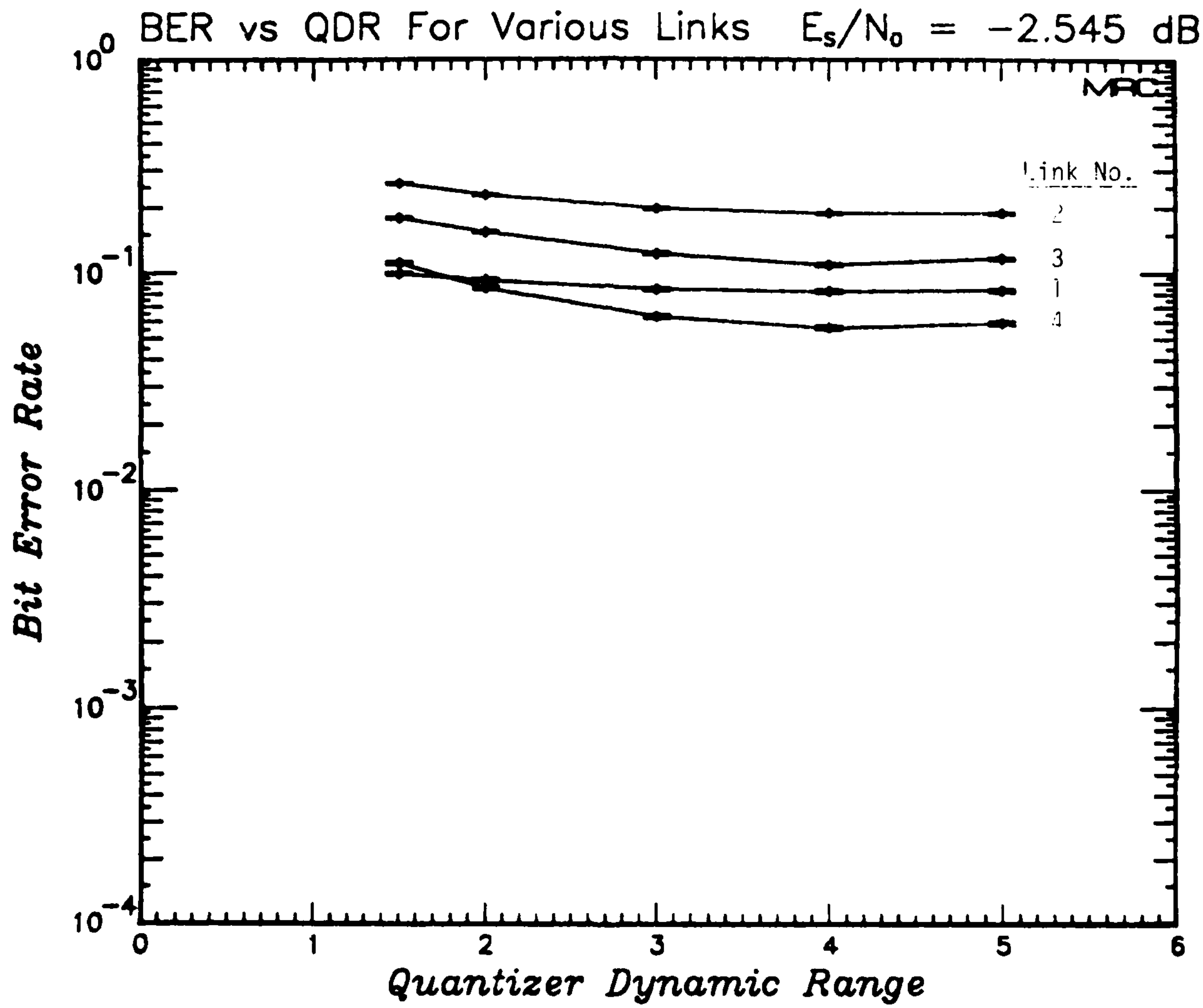

Figure 164. Information bit error rate for all links under fading channel conditions versus normalized QDR for τ_0 = 0.1 second and E_s/N_0 = -2.545.

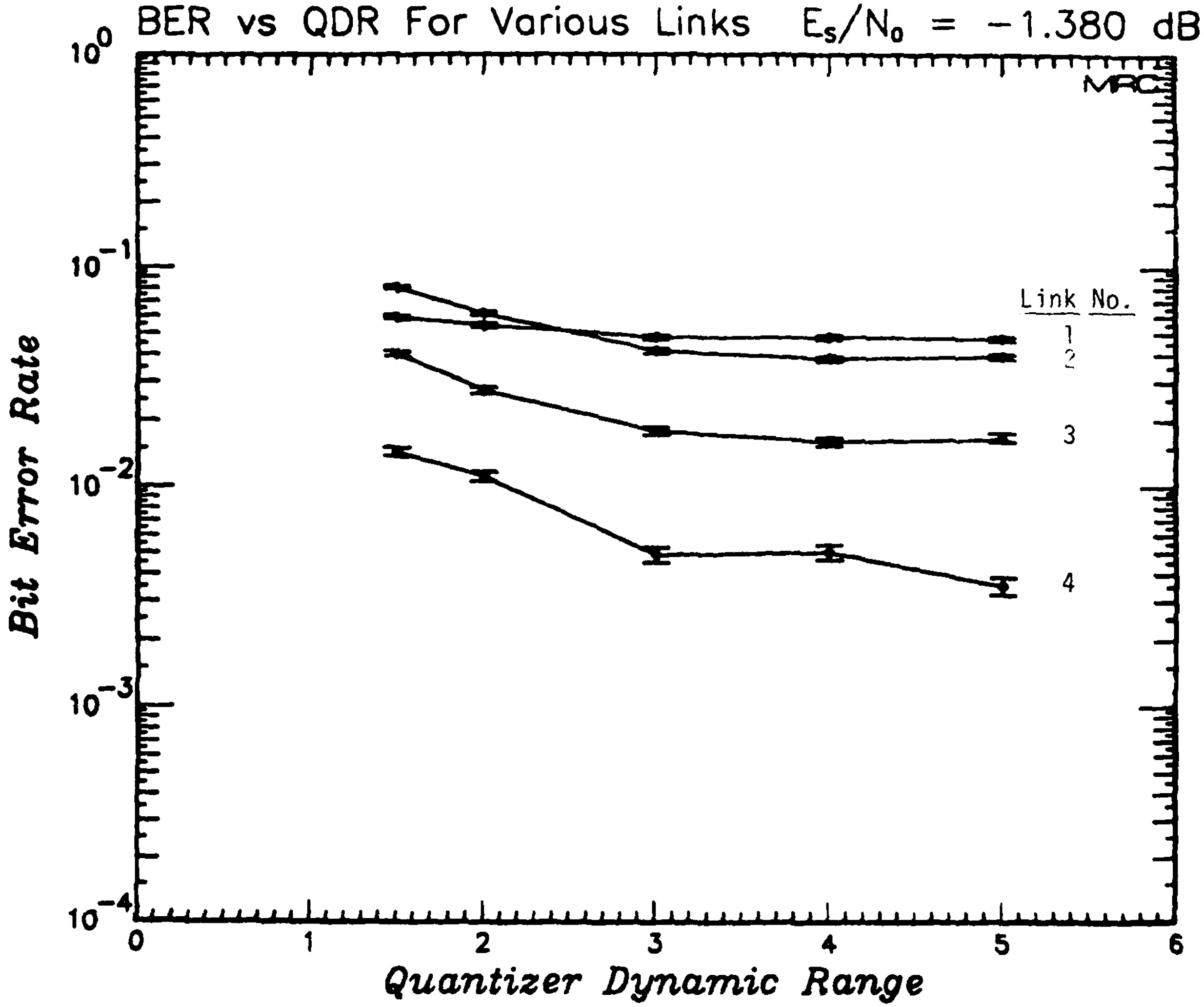

Figure 165. Information bit error rate for all links under fading channel conditions versus normalized QDR for τ_0 = 0.1 second and E_s/N_0 = -1.380.

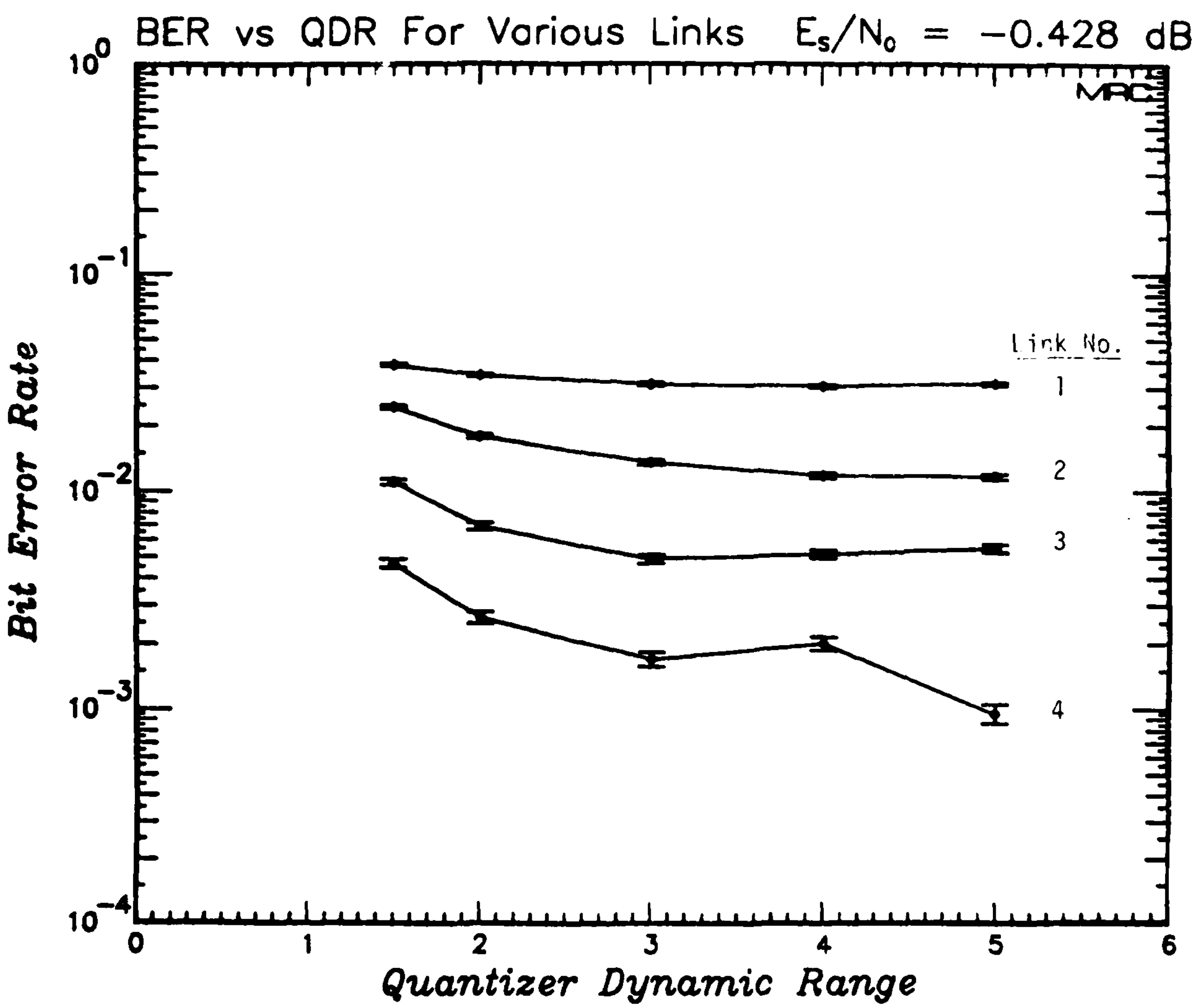

Figure 166. Information bit error rate for all links under fading channel conditions versus normalized QDR for τ_0 = 0.1 second and E_s/N_0 = -0.428.

SECTION 5
AN ADVANCED SDI CONCATENATED CODING SCHEME

Sections 3 and 4 document the study of two types of SDI concatenated coding schemes. From the results of these studies one can gain insight into the performance and implementation complexity of SDI concatenated coding schemes for digital communication links that must operate in fading channel conditions. However, neither scheme appears to be an outstanding candidate for implementation. The simple SDI concatenated scheme of Section 3 requires an adaptive quantizer on the output data stream of the inner decoder to achieve good performance with only three bits of resolution. The chip repeat and combine "on the fly" scheme of Section 4 does provide a nice reduction in the digital processing load, but does not dramatically reduce interleaver storage requirements and has somewhat disappointing fading channel performance. Here we propose an advanced SDI concatenated coding scheme that promises good performance and a substantial reduction in both storage and processing.

5.1 THE ADVANCED SDI CONCATENATED CODING SCHEME

The new coding scheme is illustrated in Figure 167. Only the decoding/deinterleaving segment is shown because that is the only part of the scheme that differs from the simpler SDI concatenated scheme shown in Figure 13 and studied in Section 3. The inner block decoder generates two data streams: one is the sequence of decoded bits and the other is the sequence of codeword reliability symbols. For each received codeword of an (n,k) block code, the inner decoder injects k decoded bits into one data path and one q_2-bit codeword reliability symbol into the other data path. The important innovation is the use of different algorithms to

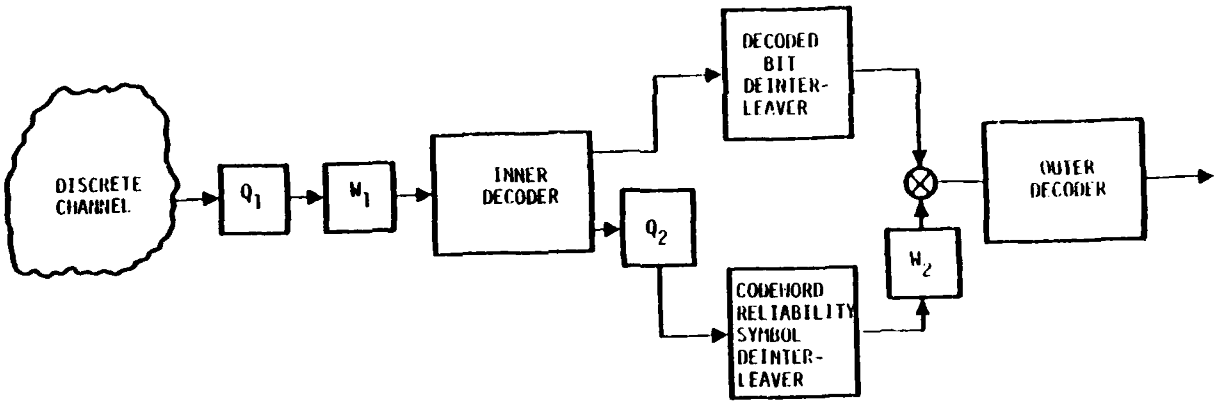

Figure 167. Block diagram of deinterleaver and decoder of advanced SDI concatenated coding scheme.

deinterleave the two data streams. The decoded bit deinterleaver can be of either the block or synchronous type. For every received codeword, this deinterleaver accepts k bits as input and generates k bits as output. The reliability symbol deinterleaver is a modification of the deinterleaver used in the decoded bit stream. For every received codeword, only one q_2-bit symbol is accepted as input and k identical symbols are generated as output in synchronization with the decoded bit deinterleaver. It is interesting to note that the reliability deinterleaver has an implicit "output symbol repeat" characteristic which is the dual of the "combine on the fly" nature of the deinterleavers studied in Section 4.

The use of the two deinterleavers in parallel can result in substantial interleaver storage savings, while allowing the reliability values to be represented with sufficient dynamic range and resolution to eliminate the need for an adaptive quantizer for the output stream of the inner decoder.

5.2 RELATIVE IMPLEMENTATION COMPLEXITY OF THE ADVANCED LINK

Two variations on the Advanced SDI Link termed "High Performance" and "Low Complexity" will be appraised for complexity and compared to the Baseline Link. The Baseline Link discussed here differs from that of Section 3 in that it uses a larger deinterleaver to cope with the long fading decorrelation times which are likely in the channels of interest. Specifically, the parameter n_2 has been increased from 99 to 1000.

The High Performance version of the Advanced SDI Link uses a rate 1/2 (n=16, k=8) block inner code and a rate 1/4 convolutional outer code, while the Low Complexity version has a rate 1/4 (n=16, k=4) block inner code and a rate 1/2 convolutional outer code. Both variations have interleaving parameters commensurate with those of the Baseline. All deinterleaving and decoding parameters of interest can be found in Table 12. The number of bits per reliability symbol in the deinterleaver has been increased to $q = 4$ for both Advanced alternatives, obviating the need for an adaptive quantizer. (This is effectively 2 bits more than the baseline value of $q = 3$ since the decoded data bit is carried in a separate deinterleaver in the Advanced Link, while one of the 3 bits in the Baseline is used to carry decoded data.)

There are a few items concerning the complexity values given in Table 12 that are noteworthy. The reduced processing requirement of the Low Compexity link with respect to the High Performance link is due to the lower inner code rate and high outer rate: lowering k from 8 to 4 in the block decoder dramatically reduces processing there, the reduced symbol rate at the deinterleaver cuts deinterleaver processsing by one-half, and the lower value of n in the convolutional code reduces Viterbi decoder processing. The only significant memory difference between the two Advanced variants is in the decoded bit deinterleaver, where the reduced bit rate makes possible a proportionally reduced value of n_2.

Figure 168 illustrates the total complexity of the links. (Note the scale change relative to previous such figures.) The Low Complexity link requires much less memory than the Baseline and much less processing than either the Baseline or the High Performance link. Further simulation work will show how its performance compares.

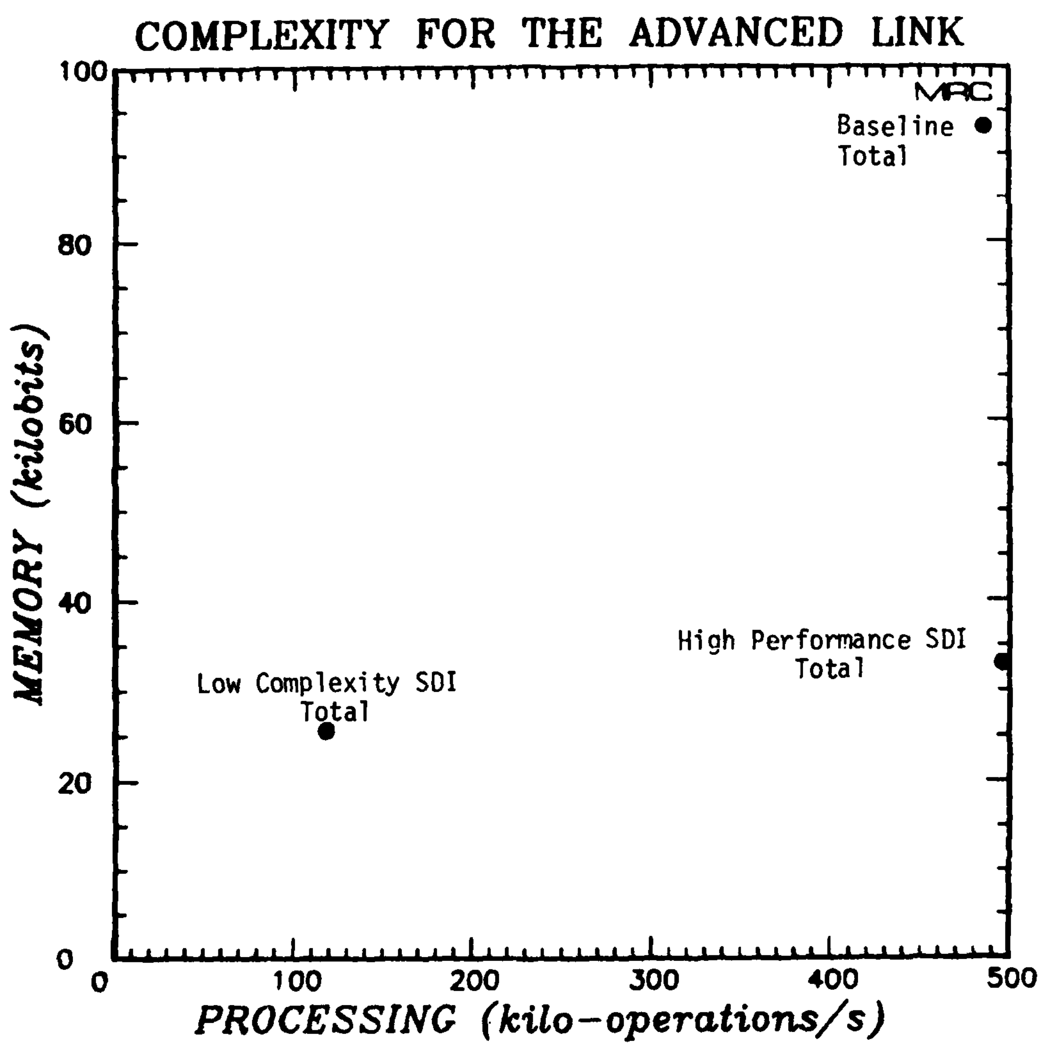

Figure 168. Ground segment complexity for the advanced links.

Table 12. Advanced SDI link complexity (ground segment).

	Parameters	Memory Equation	Memory Value (kbits)	Processing Equation	Processing Value (k-ops/s)
BASELINE Deinterleaver/ Tapered Subreg	n_2=1000, n_1=61, R_s=600, S=60, q=3, Type IV	Table 2	90.1	(19)	327.0
Viterbi Decoder	k=1, K=7, n=8, R_s=75, hK=31	(12)	3.0	(9)	159.0
BASELINE TOTALS			93.1		486.0
HIGH PERFORM SDI Block Decoder	n=16, k=8, R_s=300		Nil	(6)	307.2
Bit Deinterlv., Tapered Subreg	n_2=500, n_1=61, R_s=300 S=60, q=1, Type IV	Table 2	15.0	(19)	163.5
Reliability De-interleaver, 8:1 Mapped	n_2=500, n_1=61, R_s=300 S=60, q=4, Type IV	Table 2	15.0	(16)	2.4
Viterbi Decoder	k=1, K=7, n=4, R_s=75, hK=31	(12)	3.0	(9)	23.2
HIGH PERF TOTALS			33.0		496.3
LOW COMPLEX SDI Block Decoder	n=16, k=4, R_s=150		Nil	(6)	19.2
Bit Deinterlv., Tapered Subreg	n_2=250, n_1=61, R_s=150, S=60, q=1, Type IV	Table 2	7.5	(19)	81.8
Reliability De-interleaver, 4:1 Mapped	n_2=250, n_1=61, R_s=150, S=60, q=4, Type IV	Table 2	15.1	(16)	1.2
Viterbi Decoder	k=1, K-7, n=2, R_s=75, hK=31	(12)	3.0	(9)	15.5
LOW COMP TOTALS			25.6		117.7

REFERENCES

1. Forney, G. David, Jr., Concatenated Codes, Research Monograph No. 37, MIT Press, Cambridge, MA., 1966.

2. Gersho, Allen, "Quantization," IEEE Communications Society Magazine, pp. 16-29, September 1977.

3. Peterson, W. W., and E. J. Weldon Jr., Error Correcting Codes, Second Edition, MIT Press, Cambridge, MA., 1972.

4. Viterbi, A. J., and J. K. Omura, Principles of Digital Communications and Coding, McGraw-Hill, 1979.

5. Larsen, K. L., "Short Convolutional Codes With Maximal Free Distance," IEEE Transactions on Information Theory, IT-19, pp. 371-372, May 1973.

6. Viterbi, A. J., "Convolutional Codes and Their Performance in Communication Systems," IEEE Trans. Commun. Technol., Vol. COM-19 No. 5, October 1971.

7. Heller, J. A., "Viterbi Decoding for Satellite and Space Communication," IEEE Trans. Commun. Technol.,Vol. COM-19, No. 5, October 1971.

8. Clark, G. C., Jr., "Implementation of Maximum Likelihood Decoders for Convolutional Codes," Proceedings of the International Telemetering Conference, Washington, D. C. 1971.

9. Ramsey, John L., "Realization of Optimum Interleavers," IEEE Transactions on Information Theory, Vol. IT-16, No. 3, May 1970.

10. Knepp, D. L., Multiple Phase-Screen Propagation Analysis of Defense Satellite Communications Systems, DNA-4424T, MRC-R-332, Mission Research Corporation, September 1977.

11. Rino, C. L.,Analysis of Scintillation Effects on Communication Systems, Unpublished.

12. Wittwer, L. A., The Propagation of Satellite Signals Through Turbulent Media, AFWL-TR-77-183, Air Force Weapons Laboratory, Kirtland AFB, New Mexico, January 1978.

13. Price, G. H., W. G. Chesnut, and A. Burns, Monopulse Radar Propagation Through Thick, Structured Ionization, Stanford Research Institute, DNA-2907T, April 1972.

14. Bogusch, R. L., F. W. Guigliano, D. L. Knepp, and A. H. Michelet, "Frequency Selective Effects on Spread Spectrum Receiver Tracking," to be published in the Proceedings of the IEEE, July 1981.

15. Knepp, D. L., "Multiple Phase Screen Calculation of Frequency Selective Effects," Symposium on Satellite Communication System Performance in a Nuclear Propagation Environment, May 1980.

16 Valley, G. C., and D. L. Knepp, "Application of Joint Gaussian Statistics to Interplanetary Scintillation," Journal of Geophysical Research, Vol. 81, No. 25, pp. 4723-4729, September 1, 1976.

17. Knepp, D. L., and G. C. Valley, "Properties of Joint Gaussian Statistics," Radio Science, Vol. 13, No. 1, pp. 59-68, January-February 1978.

18. Ratcliffe, J. A., "Some Aspects of Diffraction Theory and Their Applications to the Ionosphere," in Reports on Progress in Physics, Volume 19, The Physical Society: London, England, pp. 188-267, 1956.

19. Bogusch, R. L., M. J. Barrett, B. E. Sawyer, and D. L. Knepp, Signal Propagation Effects on Selected Satellite Systems, unpublished.

20. Barrett, M. J., Optimal/Adaptive Demodulation for M-ary FSK in Fast Fading, AFWL-TR-80-69, MRC-R-453, Mission Research Corporation, November 1979.

21. Bucher, Ed, Informal discussion at the Symposium on Satellite Communication System Performance in a Nuclear Propagation Environment, RDA, April 30, 1980.

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