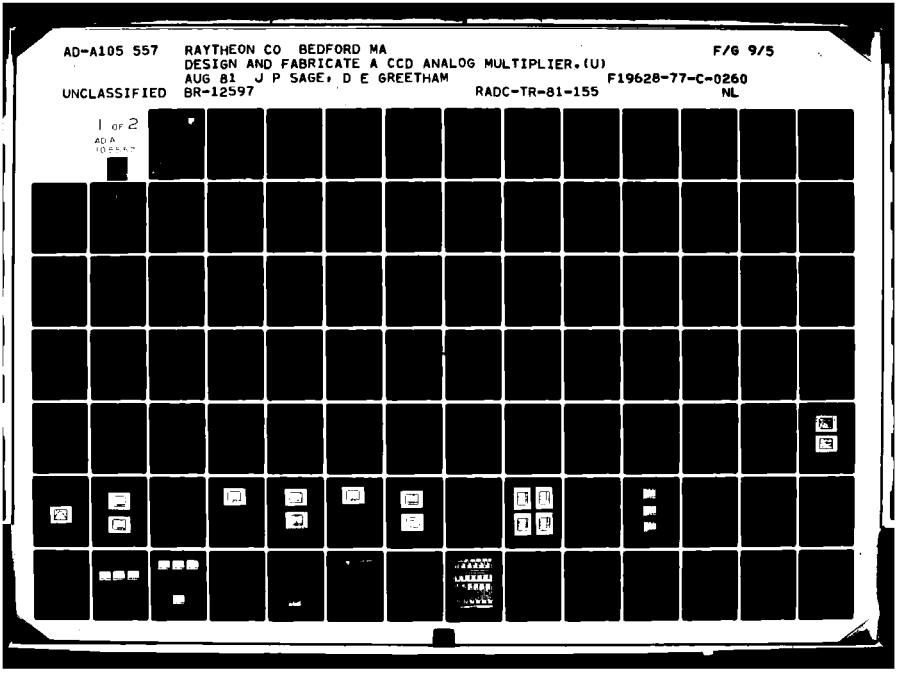
AD-A105 557 RAYTHEON CO BEDFORD MA F/G 9/5
DESIGN AND FABRICATE A CCD ANALOG MULTIPLIER.(U)
AUG 81 J P SAGE, D E GREETHAM F19628-77-C-0260
UNCLASSIFIED BR-12597 RADC-TR-81-155 NL



(12)

RADC-TR-81-155
Final Technical Report
August 1981

DESIGN AND FABRICATE A CCD ANALOG MULTIPLIER

Raytheon Company

Jay P. Sage
Douglas E. Greetham

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-81-155 has been reviewed and is approved for publication.

APPROVED: Jerry Silverman
JERRY SILVERMAN
Project Engineer

APPROVED: Freeman D. Shepherd
FREEMAN D. SHEPHERD, Jr.
Acting Director
Solid State Sciences Division

FOR THE COMMANDER: John P. Huss
JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (ESE) Hanscom AFB MA 01731. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document requires that it be returned.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
RADC-TR-81-155	AD-A105 557	

4. TITLE (and Subtitle)

DESIGN AND FABRICATE A CCD ANALOG MULTIPLIER.

5. TYPE OF REPORT & PERIOD COVERED

Final Technical Report, 30 Sep 77 — 31 Oct 80

6. PERFORMING ORG. REPORT NUMBER

BR-12597

7. AUTHOR(s)

Jay P. Sage
Douglas E. Greetham

8. CONTRACT OR GRANT NUMBER(s)

F19628-77-C-0260

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Raytheon Company
Hartwell Road
Bedford MA 01730

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

61102F
23057131

11. CONTROLLING OFFICE NAME AND ADDRESS

Deputy for Electronic Technology (RADC/ESE)
Hanscom AFB MA 01731

12. REPORT DATE

August 1981

13. NUMBER OF PAGES

122

14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)

Same

15. SECURITY CLASS. (of this report)

UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Jerry Silverman (ESE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Charge Coupled Devices	4-Transistor Bridge Multiplier
Correlator/Convolver	Silicon Integrated Circuits
Analog Multipliers	256 Stages

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A CCD based correlator/convolver having 256 stages of which serve analog signals are multiplied and summed has been designed, fabricated and tested. The design employs two dual-channel (surface channel) CCDs, source-follower buffered switched floating gate taps at each stage, block-in-section input, and as the key "breakthrough" element in the design, the analog multipliers are configured as four-transistor MOSFET transmission bridges. Various elements in the design were chosen and tested on special test arrays —

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

21400

combination both by means of computer simulations, and by a series of test pattern mask measurements in three wafer fabrication phases. Despite the size and complexity of the chip (8.7 Mn x 3.25 Mn, 4128 CCD cells and 4132 transistors), a good yield of 256 stage devices that functioned satisfactorily as correlators was obtained. On the basis of limited testing, the level of performance, however, fell short of that expected from previous component tests notably in the area of linearity of correlation ($\pm$ 5% rather than $\pm$ 1%) and in speed ($\leq$ 1 MHz rather than 10 MHz). Suggestions for further tests and experiments are given.

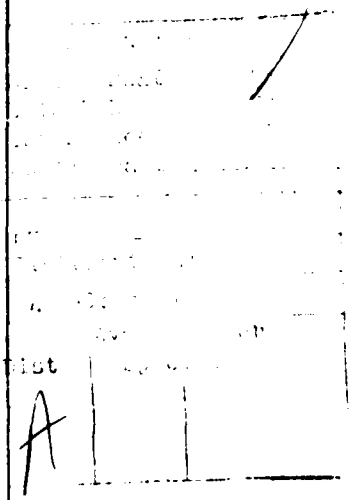


TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont)

LIST OF TABLES

1. INTRODUCTION

The purpose of this program was the development of a charge-coupled device (CCD) based correlator/convolver suitable for use in advanced USAF military electronic systems.

The specific objective of this program was to fabricate and deliver 20 best-effort samples of CCD-based correlator/convolver devices aimed at the design goals listed below in Table 1-1.

TABLE 1-1
OVERALL PERFORMANCE GOALS

CCD dynamic range	60 dB 70 dB after input normalization
CCD clock rate	32 kHz to 10 MHz at 25°C 500 kHz to 10 MHz at +85°C
CCD size	256 Stages
Relative correlation error (percent of theoretical for pulse waveforms with 25 percent duty cycle)	1 Percent
Power dissipation	$\leq$300 mW

These performance goals were selected to meet or exceed contract requirements.

The resulting device is shown in **Figure 1-1.** The chip is very large (8.7 millimeters (mm) by 3.25 mm = 340 mils x 130 mils) and very complex (more than 4000 CCD gates and more than 4000 MOS transistors). Although direct current (dc) testing for diode and gate integrity showed a yield of no more than a few percent, the yield of functional devices has been quite high (nearly 40 percent for one wafer). Undoubtedly, this is partly a result of the very high processing gain of a correlator which makes it tolerate some subunits

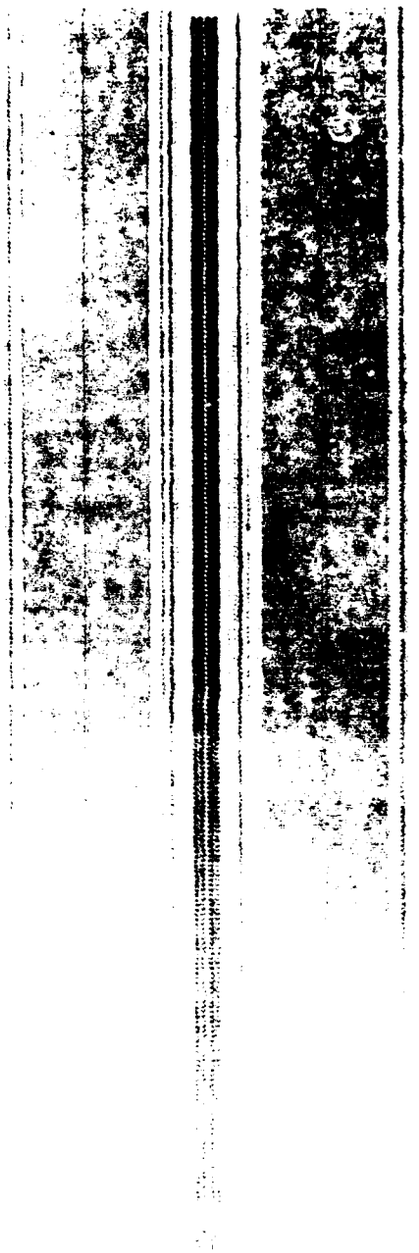


Figure 1-1 - CCD-Based Correlator/Convolver Device

which are faulty. No device has yet been seen with performance as good as what we had hoped to see. With signals that should have sidelobes of about $\pm$ 1 percent, we observe sidelobes of approximately $\pm$ 5 percent. The exact cause for the reduction in performance has not been identified, but all working correlators show about the same performance. Details are presented in Section 7.

This program began with an evaluation phase in which a range of possible designs were examined. Section 2 of this report describes that study and its conclusions. It begins with some definitions and theoretical results, gives a general analysis of critical factors in the design of a correlator/convolver, describes various options, and gives the options chosen. Finally, the detailed design parameters are determined.

The next phase of the program was the design and fabrication of a test chip containing the individual elements, such as transistors, CCDs with floating gate (FG) taps and buffer amplifiers and multiplier cells, so that their performance could be checked before assembling them into a complete correlator/convolver. Section 3 reports on the study of transistor threshold voltage uniformity; Section 4 describes the design, operation, and performance of the nondestructive readout (NDRO) FG output taps and source-follower buffer ampliers; Section 5 covers the new multiplier design and its performance.

The final phase of the program was the production of the complete 256-stage correlator/convolver. Section 6 describes the mask and process design for both the test chips and the complete chip. Finally, Section 7 presents test results for the correlator/convolver.

2. DESIGN ANALYSIS

This section presents general background information and the results of the analytical phase of the program. It contains four subsections.

Subsection 2.1 gives a brief statement of the problem including definitions of correlation and convolution and their implementation in block diagram form. This block diagram corresponds directly to a design using charge-coupled shift registers and MOS analog multipliers. A discussion of the principal problem areas in each circuit element is provided.

Subsection 2.2 presents a range of alternative designs that were considered for each part of the CCD device, the nondestructive parallel readouts and the multipliers. Included is a qualitative discussion of the relative merits and difficulties of each approach. Particular attention is paid to a number of possible analog multiplier cells.

Subsection 2.3 presents the overall configuration that was selected for use. Table 2-1 summarizes the features of the device.

Finally, Subsection 2.4 reports on the detailed circuit designs and optimization based largely on computer-aided circuit simulation techniques. Quantitative analytical verification of the qualitative features of the different possible multiplier cells is presented. Several significant interactions between the source-follower buffer amplifiers that are part of the nondestructive CCD outputs and the analog multiplier cells are analyzed in detail. The computer simulations included a parameter variation sensitivity analysis.

2.1 General Statement of the Problem

The mathematical definition of the correlation C of two real functions f and g, defined over the interval $-\infty$ to $+\infty$, is given by Equation (1) below:

$$C(y) = \int_{-\infty}^{\infty} dx\ f\ (x)\ g\ (x + y) \tag{1}$$

One can envision this operation as indicated pictorially in Figure 2-1. The two functions, f and g, are aligned next to each other with their axes running in the same direction with

TABLE 2-1

CCD-BASED CORRELATOR/CONVOLVER DESIGN FEATURES

		CCD
Surface Type	-	For low distortion, low dark current and maximum tap output levels
4-Phase Clock	-	For minimum process complexity, maximum signal charge and ability to reverse direction of either CCD electronically for convolver operation.
Differential Operation	-	Permits use of superior multiplier designs, improved dark current and harmonic rejection
Resettable Floating Gate Taps	-	For nondestructive readout
Potential Equilibration	-	For lowest input noise.
		Multiplier
4 MOSFET with source follower buffer inputs	-	For maximum accuracy and minimum errors generated by nonlinearities, offset variations and CCD dark currents

the origin of g shifted a distance y. The two displaced functions are multiplied at their adjacent points and the products are summed. The function C(y) unfolds with increasing y as g moves by f.

The discrete version of Equation (1) for functions defined at equally spaced points is given by Equation (2).

$$C_j = \sum_{i=-\infty}^{\infty} F_i \, G_{i+j} \qquad (2)$$

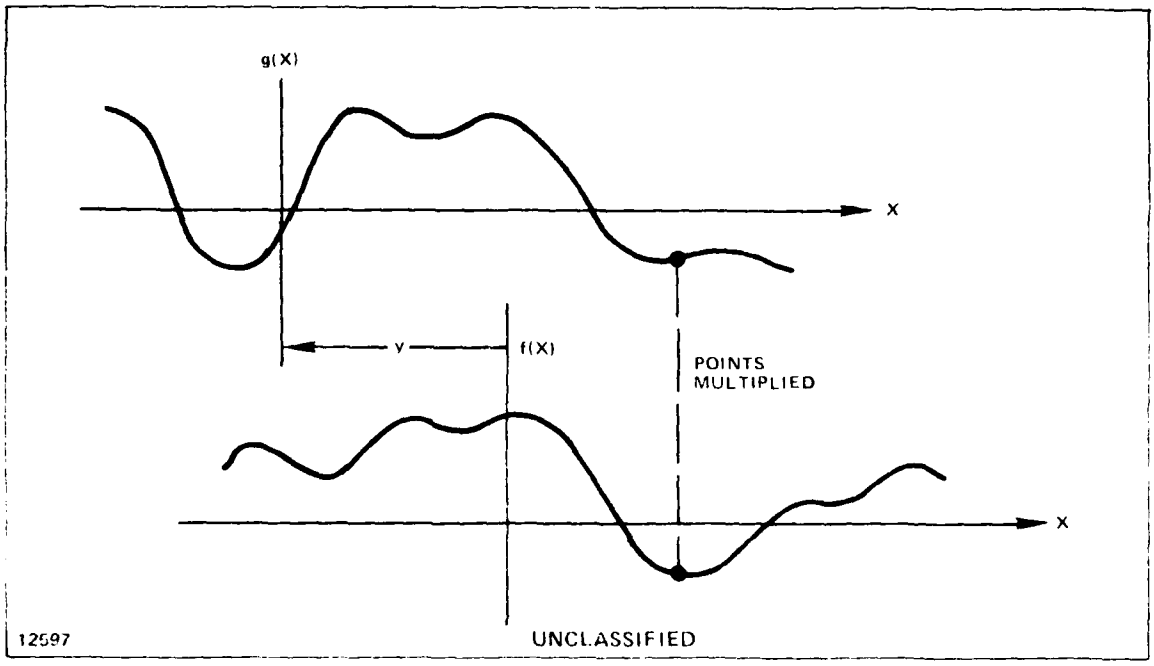


Figure 2-1 - Pictorial Representation of the Correlation Operation

This may reduce further to a finite version if one of the signals, for example F, is of finite length. The equation then becomes:

$$C_j = \sum_{i=1}^{N} F_i \, G_{i+j} \tag{3}$$

The convolution function C' of two functions f and g is defined by Equation (4)

$$C'(y) = \int_{-\infty}^{\infty} dx \; f(x) \; g \; (y-x) \tag{4}$$

$$= \int_{-\infty}^{\infty} dx \; f(-x) \; g \; (x + y)$$

The convolution can be envisioned pictorially as shown in **Figure 2-2.** The difference is that one of the functions has the direction of its x-axis reversed. The function g moves by a backward f while the sum of products is being completed.

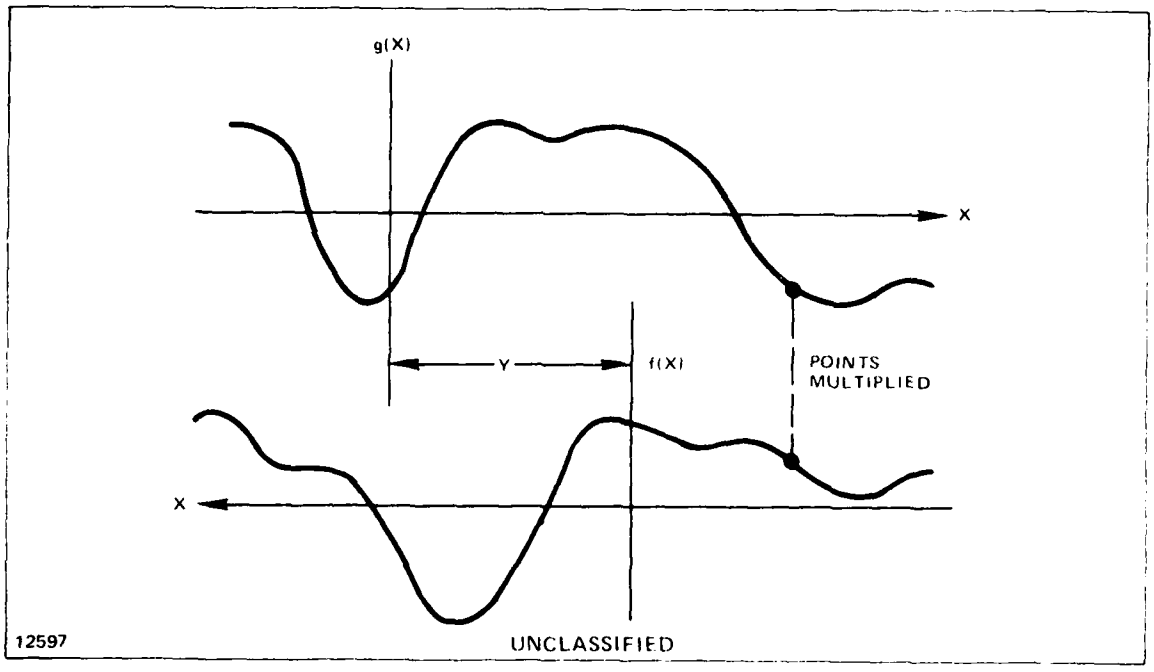


Figure 2-2 - Pictorial Representation of the Convolution Operation

The discrete and finite versions of the convolution are given by Equations (5) and (6).

$$C'_j = \sum_{i=-\infty}^{\infty} F_{-i}\, G_{i+j} \tag{5}$$

$$C'_j = \sum_{i=1}^{N} F_{-i}\, G_{i+j} \tag{6}$$

Figure 2-3 shows a block diagram of the realization of the finite discrete versions of the correlation and convolution.

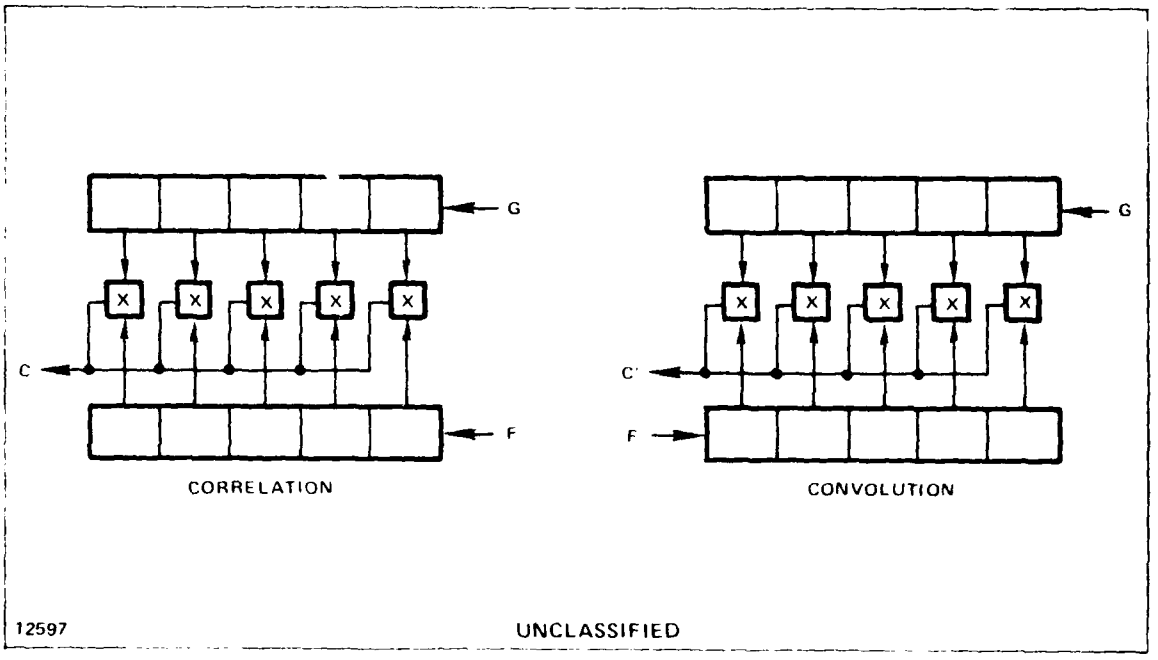


Figure 2-3 - Block Diagram of a Physical Realization of Correlation and Convolution

The upper and lower registers represent analog shift registers carrying sampled analog data. These could be charge- upled shift registers with nondestructive parallel readouts. The adjacent signal samples are multiplied by an array of analog multipliers, the outputs of which are summed, for example, on a current bus for multipliers with a current output. The correlation and convolution functions are generated by shifting the samples of G through the upper shift register and carrying out the sum-of-products operation after each shift.

Note that the convolver differs from the correlator only in the direction in which signal F is shifted into the lower shift register. If a single device is desired which is capable of performing both functions, one can readily design a CCD with symmetrical input and sink structures which, with appropriate clocking, could be made to operate in either direction. This cannot be achieved, however, using two-phase CCDs in which the directionality is determined physically and not electrically. This point will be discussed in greater detail in Subsection 2.2.1.

2.1.1 Critical Implementation Factors

In constructing an integrated circuit correlator/convolver from CCDs and analog multipliers, each element has critical factors which must be controlled in order to achieve satisfactory performance levels from the complete device. All parts must achieve sufficiently low levels of random noise, have adequate temperature insensitivity and consume minimum power.

The special considerations that apply to the various elements are set forth below.

2.1.1.1 Charge-Coupled Shift Register

2.1.1.1.1 Linearity

The CCD, considered here to include the nondestructive parallel outputs, must achieve an adequate level of input-to-output linearity. The individual conversions between voltage and charge at the input and outputs need not be linear. Indeed, as discussed in more detail later, FG outputs are inherently nonlinear and generally must be used with CCD input techniques with a corresponding nonlinearity.

2.1.1.1.2 Variations

Since the CCD has a single input structure, one source of variation from cell-to-cell is eliminated. Variation of output tap sensitivity is a factor to be considered.

2.1.1.1.3 Fixed Pattern Noise

In addition to contributing to the random noise level, thermal carrier generation (dark current) introduces nonrandom variations into the signal charge. For example, if signal F in Figure 2-3 is loaded into the lower CCD shift register and then held there as signal G is swept by it, dark current will steadily accumulate. This will cause signal F to acquire a dc offset and, to the extent that dark current is nonuniform, an alternating current (ac) variation from cell-to-cell. Similarly, a signal G clocked through the CCD at a slow steady rate will acquire an approximately linear ramp offset due to the greater accumulation of dark current in cells containing signal which has been in the CCD longer. Dark current and its uniformity are, therefore, important considerations in the CCD.

2.1.1.1.4 Transfer Efficiency

As signals are shifted through a CCD, a small fraction of each signal packet is left behind and becomes a part of the next signal packet. This gives rise to a bandwidth change and phase shift in the signal.

2.1.1.2 Analog Multipliers

2.1.1.2.1 Linearity/Accuracy

The linearity and accuracy of the multiplier are critical characteristics. Depending on the types of functions being correlated, certain error terms are far more critical than others. In a computer simulation of the matched filtering of a frequency modulation (FM) chirp waveform, a 10 percent term of the form fg^2 plus gf^2 raised the sidelobes only to minus 32 decibels (dB). A mere 1 percent term of the form f^2 plus g^2 caused a slightly greater degradation in sidelobe level.

2.1.1.2.2 Variation

Even if each individual multiplier in the integrated circuit (IC) had perfect linearity, variation in gain could be a source of trouble.

2.2 Options

This section presents a catalog of the major options available for the elements of the IC correlator/convolver.

2.2.1 CCD Design

2.2.1.1 Channel Type

The CCD may be of either the surface channel or the buried channel type. The buried-channel CCD (BCCD) offers superior charge transfer efficiency and maximum operating speed. In theory, it offers a superior signal-to-noise ratio but in practice this is

offset by the low output signal levels, especially from a FG detector. The surface channel CCD (SCCD) is somewhat simpler to fabricate, exhibits lower dark current, carries more charge and is intrinsically more linear.

2.2.1.2 Clocking Technique

CCDs are commonly made with 2, 3, or 4-phase clocking structures. All can be operated with one electrode held at a dc level instead of being clocked. These modes of operation are named 1-1/2-phase, 2-1/2-phase, and so on. The 3-phase structure provides the minimum cell pitch. Its fabrication, however, requires either three gate layers or the cross-connection of gates fabricated in two layers. The addition of a fourth gate per cell permits the gates to be made in two interdigitated layers with no cross-connections. This 4-phase structure, if operated with overlapping clocks, can store charge under at least two gates at all times. This gives the 4-phase CCD the greatest charge handling capacity. The 2-phase structure can be considered a degenerate form of the 4-phase structure with neighboring gates connected in pairs and directionality of transfer built in physically, for example, by changing the oxide thickness or by changing the substrate doping density by ion implantation. The 2-phase structure has the advantage of requiring the fewest number of clock signals and clock distribution buses. The half-phase versions all offer a reduction in clock number compared to the corresponding whole-phase design but a significant penalty in dynamic range results unless the voltage swing of the remaining clocks is increased.

Finally one should note that all of the clock schemes except 2-phase and 1-1/2-phase are capable of shifting charge in either direction. For example, exchanging the signals on clock phases 2 and 3 of a 3-phase device or 2 and 4 of a 4-phase device will reverse the direction of transfer. A 2-phase device in which all four clock lines are accessible can have its gates connected for bidirectional operation. This involves the structural complexity of a 4-phase device but the clock requirements of a 2-phase device. This is illustrated schematically in **Figure 2-4.** The switch can be implemented by discretionary bonding or with field-effect transistor (FET) switches.

2.2.1.3 Input Structure

Two generally used input techniques for CCDs are called potential charge equilibration and gated diode. In the former, as shown in **Figure 2-5**, a metering input

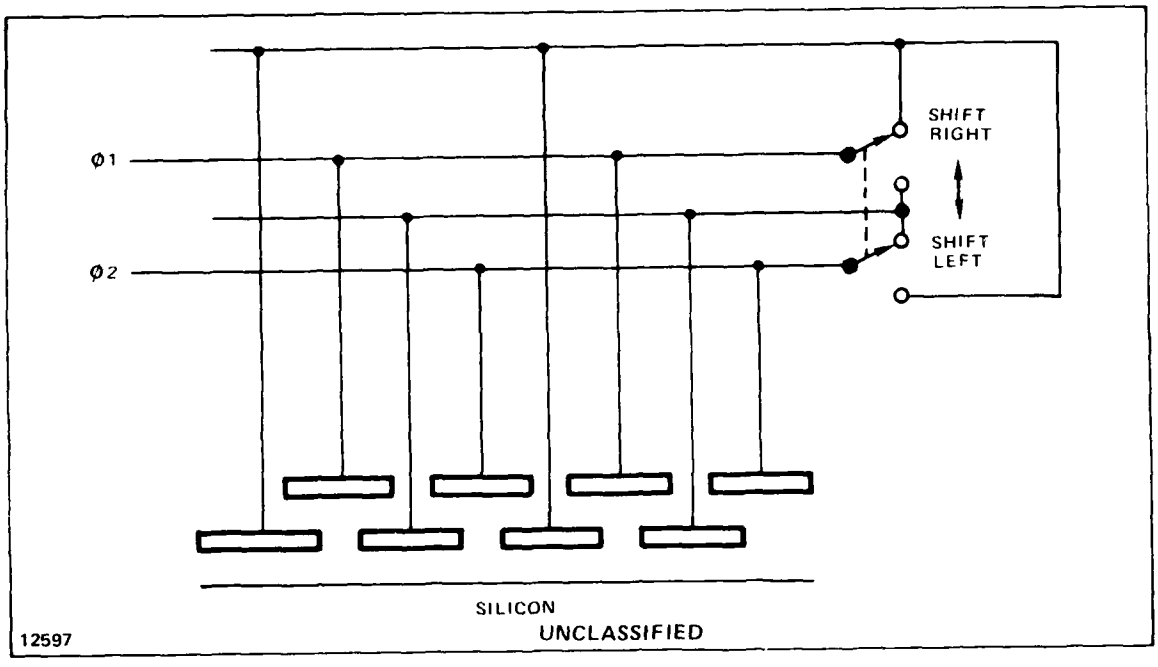


Figure 2-4 - Method for Making 2-Phase Devices Bidirectional

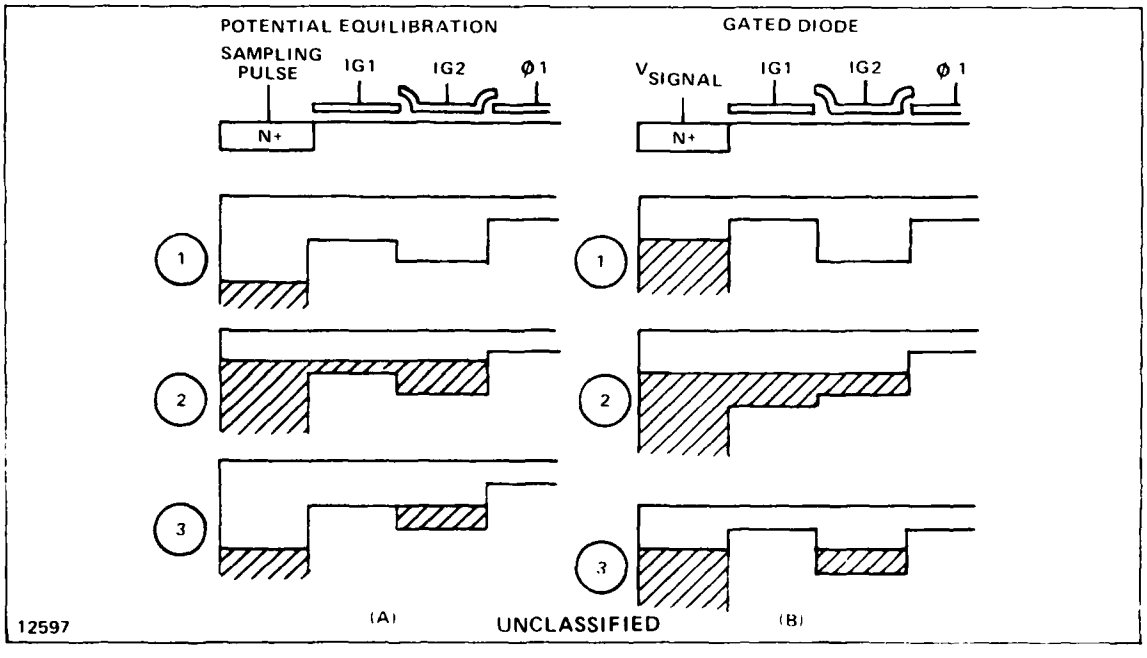


Figure 2-5 - Potential Equilibration and Gated Diode CCD Input Techniques

well is formed as a result of the difference between the voltages on input gate (IG)1 and IG2. A pulse applied to the input diffusion overfills the input region. The excess charge then flows back to the diffusion until equilibrium is established. This input technique results in a very linear conversion of the input voltages on IG1 and/or IG2 to charge (less than 0.1 percent error is possible), normal and inverting inputs are available and the noise level is very low. For most purposes this is the preferred input technique.

The gated diode input is illustrated in **Figure 2-5.** Here the signal is connected to the input diffusion. When IG1 is pulsed on, the input well under IG2 is filled to a channel potential equal to the input signal level. The conversion of voltage to charge is not linear because of the variable depletion capacitance but FG detectors, as discussed below, sense not the signal charge but the surface potential. The gated diode input thus tends to match the FG output for an overall linear transfer function.

2.2.1.4 Nondestructive Parallel Readout

The correlator design requires CCDs with outputs at every tap and the output sensing must be performed in a nondestructive way with a minimum of degradation. Two general types of NDRO are available. One is called the floating diffusion technique. Here the charge is made to flow onto a diffusion which may be under one of the gates of the CCD. The diffusion acts as a conductor which comes to the potential of the channel and can be connected to a MOSFET gate for sensing. Since the diffusion is floating (not connected to any charge source outside the CCD), total charge is conserved and the signal in the CCD passes on unchanged as the clocks cycle. The diffusion is loaded down, however, by the sensing circuitry and there can be a problem of uneven charge redistribution under the gate. More serious yet is a substantial degradation of charge transfer efficiency due to the formation of a structure that is acting essentially as a bucket brigade device. This problem has been encountered in CCD shift register designs with diffused corners. The problem is acceptable in some cases because of the small number of corners; however, a floating diffusion sensor at each stage of the CCD would probably not be acceptable in most cases. The transfer problem is substantially reduced when half-phase clocking is used with dc on the gate over the floating diffusion.

The floating diffusion does have the advantage of tending to sense charge in the channel, especially when the circuit loading on the diffusion becomes large. In that case, the diffusion voltage does not change very much and thus the depletion capacitance remains nearly constant.

The other NDRO technique is the FG. Numerous realizations are possible, but they generally fall into two classes, depending on how the FG is made to reach the necessary dc bias level. In one case, the FG is simply connected through a FET switch to the appropriate clock line. Just before the signal charge arrives under the FG, this switch is opened allowing the gate to float.

This technique sometimes requires a change from the normal clocking technique. For example, with normal 4-phase overlapping clocks, the signal charge enters the region under any gate as soon as the gate goes ON. This cannot be permitted to occur with the switched FG. The clocking must be modified, as shown in **Figure 2-6**, so that the two gates adjacent to the FG are OFF until after the float switch opens. The maximum charge handling capacity is reduced to one half.

The 3-phase structure cannot be operated in this mode because the FG must be isolated by OFF gates on both sides while another gate holds the signal charge. Thus, four gates are required. The 2-phase structure with push clocks is a natural for this FG technique because the charge transfers when the clocks make their OFF transistions. The corresponding timing and charge motion diagrams are shown in **Figure 2-7.**

The advantages of switched FG sensors are as follows:

- With this FG technique, all of the signal charge is under the FG and uneven distribution problems do not arise.
- The FG is physically just a regular CCD gate, differing only in the way it is connected. This simplifies fabrication and tends to insure undegraded CCD performance.
- The parasitic loading on the FG can be kept low, increasing its sensitivity.

The second type of FG is the capacitively coupled FG. As with the switched FG, this gate is usually connected to one end of an FET switch. The other end, however, is connected to a bias line. At infrequent intervals, the switch is closed to establish the correct total charge on the gate. Since this need not be carried out rapidly, a minimum geometry FET is sufficent. The clock swing is induced on the FG by means of coupling capacitance between a clock line and the FG. There are conflicting considerations concerning this capacitance. If it is very large, the clock signal is coupled in very

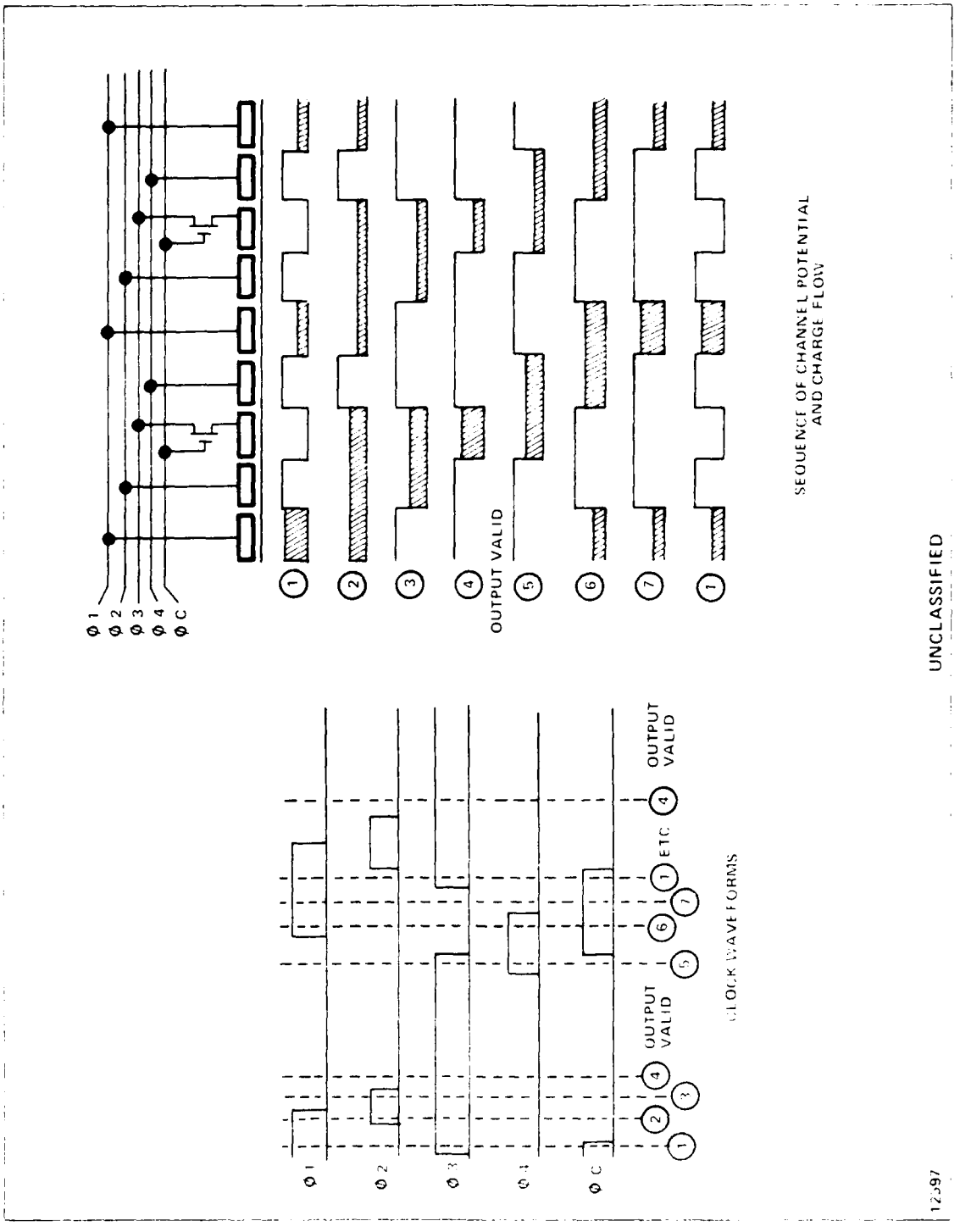


Figure 2-6 - Modification of 4-Phase Clocking Required with Switched Floating Gate Sensors

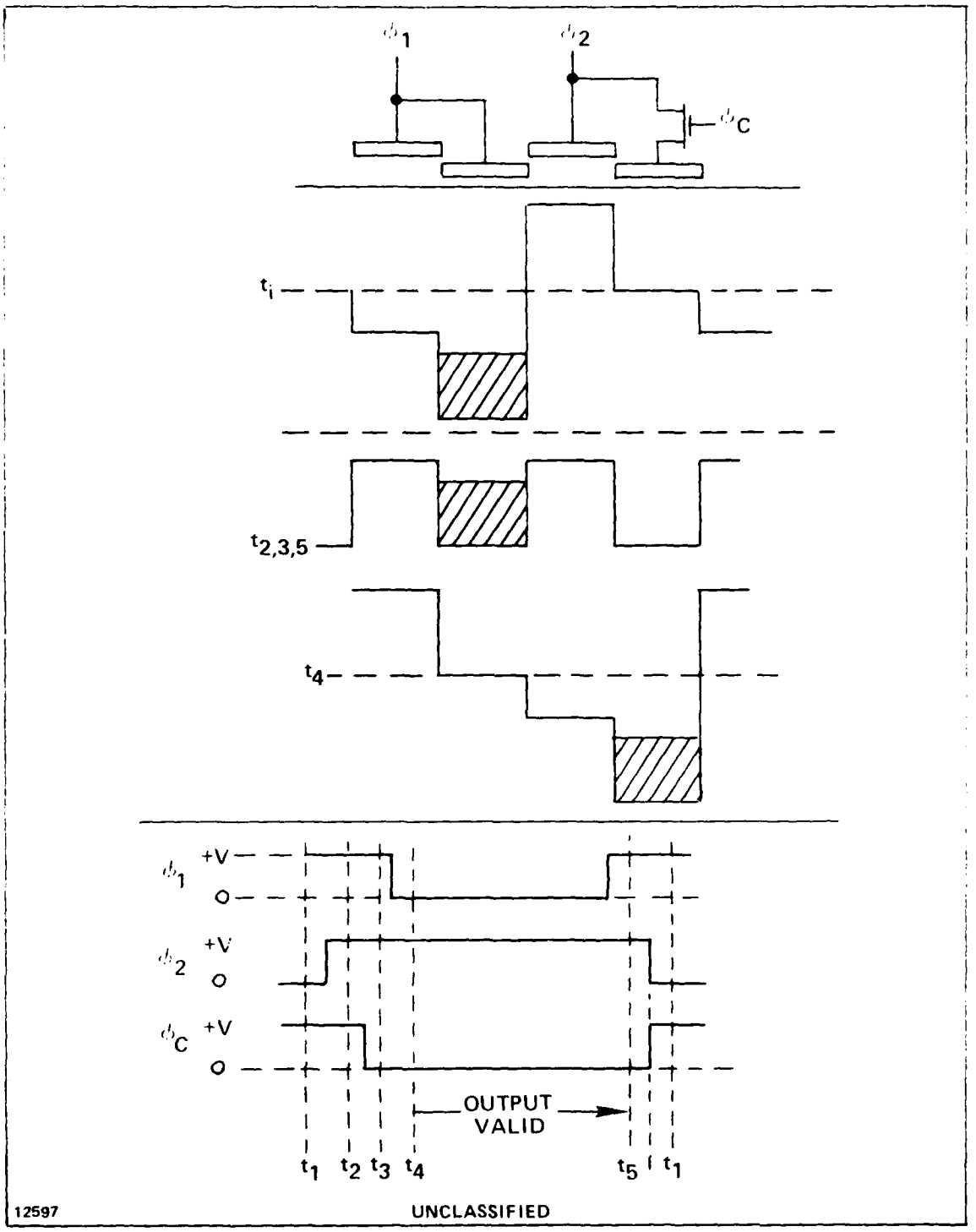


Figure 2-7 - Clock Waveforms and Charge Flow for 2-Phase Clock Operation with Switched Floating Gate Top

efficiently, but the FG is heavily loaded down and becomes less sensitive. On the other hand, if the coupling capacitance is small, a much higher amplitude clock is needed. These problems are eliminated when a half-phase clocking scheme is used with the FG serving as the dc gate.

The capacitively coupled FG has the advantage of being able to work with any clocking technique. It suffers from several disadvantages, however. It can be expected to exhibit greater loading and lower sensitivity; it requires a more elaborate CCD structure with both capacitive and FET connections; and in some implementations it suffers from linearity problems from uneven signal charge distribution under the gates.

2.2.2 Multiplier Designs

Although much work has been done on multipliers in the past, most of it is not applicable to this program since it has emphasized bipolar technology and has been aimed primarily at the analog computer market. The operating principles used in such multipliers have included the following categories:

- Bipolar transconductance multipliers
- Bipolar carrier domain multipliers
- Log-analog multipliers
- Pulse modulation multipliers
- Servomechanism multipliers

Although the previous categories can be used to make very accurate and satisfactory multipliers, the emergence of MOSFET multipliers has rendered them obsolete as far as this program is concerned. Thus, this section will be limited to a discussion of MOS structures only.

2.2.2.1 Basic MOS Operation

The gate-voltage-controlled drain-to-source conductance of a MOSFET operating in the linear region provides an excellent basis on which to build an analog multiplier. The theoretical relation between the current flowing from drain to source (I_{DS}) and the voltages on the drain and gate relative to the source (V_{DS}, V_{GS}) is given by Equation (7) to terms quadratic in the voltages:

$$I_{DS} = g\, V_{DS}\, (V_{GS} - V_T - \tfrac{1}{2} V_{DS}) \qquad (7)$$

If the source is not connected to the substrate, the threshold voltage, V_T, will depend on the source-to-substrate voltage, V_S, an effect sometimes called the back-gate-bias effect. The V_{DS} term inside the parentheses represents an effective shift in threshold due to the back-gate bias effect resulting from the change in average channel potential from drain to source of 1/2 V_{DS}. For the sake of accuracy, it should be noted that theoretically this factor is actually slightly greater than 1/2 because the back-gate bias coefficient dV_T/dV_S is greater than unity.

It is assumed that a multiplier will be constructed based on Equation (7) by holding a current bus connected to the source at a fixed potential and measuring the current. Since V_{GS} must be greater than V_T to get any current to flow, the multiplier will only work for one sign of V_{GS}. Since V_{DS} can be either positive or negative, a two quadrant multiplier results.

There are several major problems that must be overcome before the MOSFET can be used as an analog multiplier in an IC correlator. First, since V_D, the drain voltage is to be supplied from a buffered FG or floating diffusion sensor, it will consist of a bipolar signal riding on a substantial offset. This will induce an undesirable linear term in the current proportional to V_{GS}. This term can be eliminated by biasing the source to the offset level of the drain voltage. Second, if V_G also comes from a floating diffusion or FG sensor, it also will consist of a bipolar signal riding on a dc offset. This will induce an undesirable linear term in the current proportional to V_{DS}. This term could be eliminated by using a differential current bus and bleeding a current proportional to V_{DS} through a resistor corresponding to the FET conductivity with V_{GS} at its dc offset level. The third problem is the large quadratic term in V_{DS}^2. This represents a significant error term in the multiplication.

Solutions to all of these drawbacks of the simple MOSFET multiplier can be better achieved by arranging MOSFETs symmetrically in various ways. Four such arrangements are worthy of serious consideration.

2.2.2.1.1 Dual MOSFET Gate-Reference-Balanced Multiplier

In this multiplier, two MOSFETs are connected as shown in **Figure 2-8.** The two signals from buffered outputs of the two CCDs are represented by V_D and V_G. A reference voltage, $V_G^{(0)}$, equal to the value of V_G when the CCD contains a zero signal is applied to the balancing MOFSET. The sources of the two transistors are connected to two current buses which must be held as virtual voltage nodes. The output signal is represented by the difference between the currents in the two buses. These buses must be held not as virtual grounds but rather, as remarked above, at a voltage equal to $V_D^{(0)}$, the value of V_D when CCD contains a zero signal.

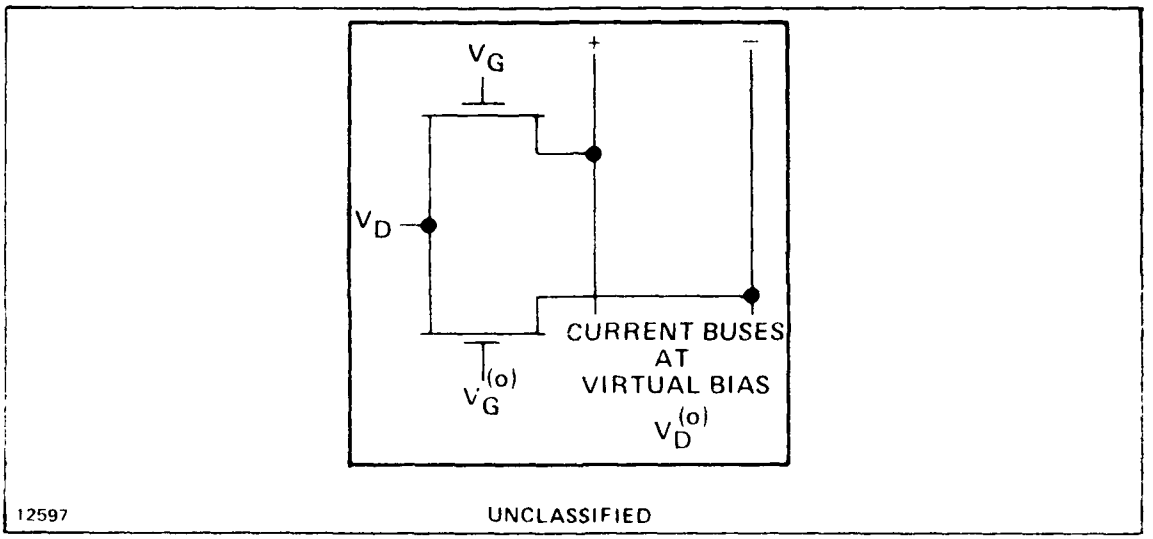


Figure 2-8 - Dual MOSFET Multiplier Structure

The advantage of this circuit is that it removes all three flaws of the single MOSFET, including the large quadratic term in V_{DS}^2. That term results in equal currents on the two buses and cancels out when the currents are subtracted.

Major deficiencies remain nevertheless. Variations in the values of $V_D^{(0)}$ and $V_G^{(0)}$ due to variations in component parameters, CCD bias charge levels and dark current accumulation will upset the balance in the circuit.

2.2.2.1.2 Dual MOSFET Differential-Gate Multiplier

This multiplier is a simple extension of the previous concept and uses the same circuit arrangement. The difference is that the CCD providing the output voltage, V_G, is configured as a split-channel differential CCD with outputs of:

$$V_G^{(1)} = V_G^{(0)} + V_G^{(S)} \text{ and } V_G^{(2)} = V_G^{(0)} - V_G^{(S)} \tag{8}$$

where $V_G^{(S)}$ represents the signal. $V_G^{(1)}$ is applied as V_G in **Figure 2-8**; $V_G^{(2)}$ replaces $V_G^{(0)}$ on the other gate. The sensitivity of the multiplier to $V_G^{(0)}$ is eliminated. Moreover, even order nonlinearities in the CCD output signal applied to the gates are also cancelled by the differential arrangement.

2.2.2.1.3 Quad MOSFET Dual Reference-Balanced Multiplier

Another improvement over the circuit in **Figure 2-8** is shown in **Figure 2-9**. Here the signal applied to the drain is also balanced against a reference. The primary advantage of this circuit is that it relieves the requirement that the current buses be held at $V_D^{(0)}$. It is conceivable that individual $V_D^{(0)}$ references for each cell could be derived in a way that would compensate for cell-to-cell variations.

2.2.2.1.4 Quad-MOSFET Dual Differential (Bridge) Multiplier

This multiplier follows from that in **Figure 2-9** in the same way that the differential-gate multiplier followed from **Figure 2-8**. Now both CCD channels are configured as differential CCDs. **Figure 2-10** shows this multiplier redrawn in the form of a bridge to show its complete symmetry. The difference between the currents on the two summing buses plus Σ and minus Σ now depends only on the product of the difference between plus D and minus D and the difference between plus G and minus G. The result does not depend on any reference value applied externally. A correlator/convolver based on any of the three previously described multipliers requires good tracking of transistor parameters across the entire device. With the bridge multiplier, each stage of the correlator/

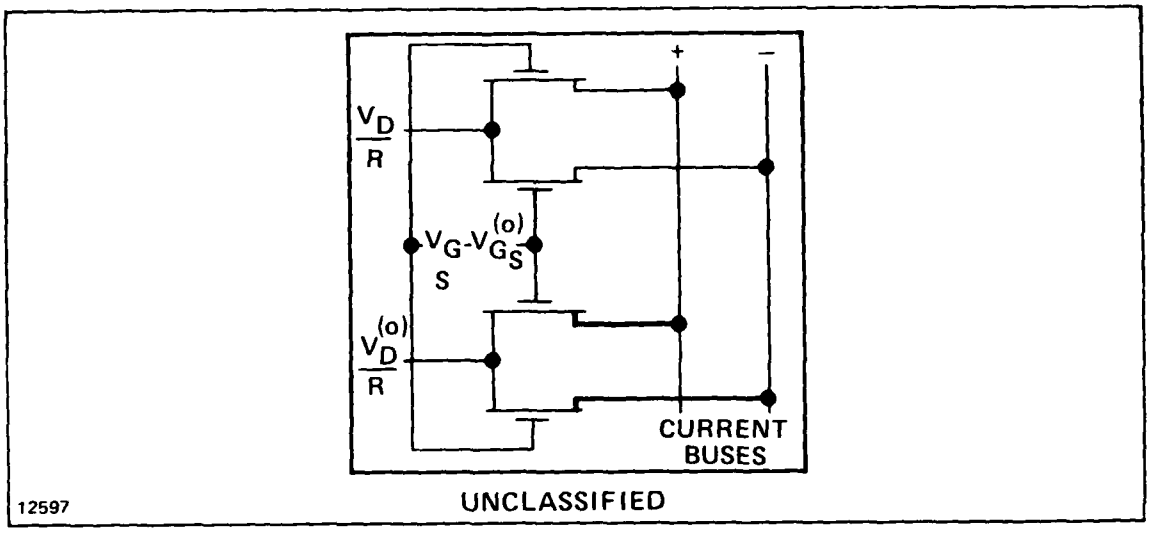


Figure 2-9 - Quad MOSFET Multiplier Structure

convolver stands alone. The plus G and minus G signals for the cell must track; the plus D and minus D signals for the cell must track; and the four multiplier MOSFETs in one cell must track. Close parameter tracking from cell to cell is not required for high accuracy performance.

This circuit configuration is a fundamental multiplier as a result of its symmetry and tends to act as a linear multiplier when virtually any three-terminal devices are used. The fact that a single MOSFET is a fairly good multiplier to begin with makes the performance that much better. Table 2-2 shows the terms, voltages, the origin and relative magnitude of the major terms and which terms are present for the four multiplier designs discussed above.

In the full correlator design, the signals represented by charge in the CCDs appear at the outputs riding on a dc bias. For example, the drain voltage is:

$$V_D = V_D^{(0)} + V_D^{(S)} \tag{9}$$

Consequently, a term of the form V_D^2 in Table 2-2 contributes a constant term, a linear term and a quadratic term in the signal voltages. Because the dc levels are large, these terms are all first order. A quadratic distortion in the CCD output adds further lower order terms. Table 2-3 shows the terms that result from the dc offsets and quadratic CCD distortions. The crosses represent first order terms and the dots second order terms.

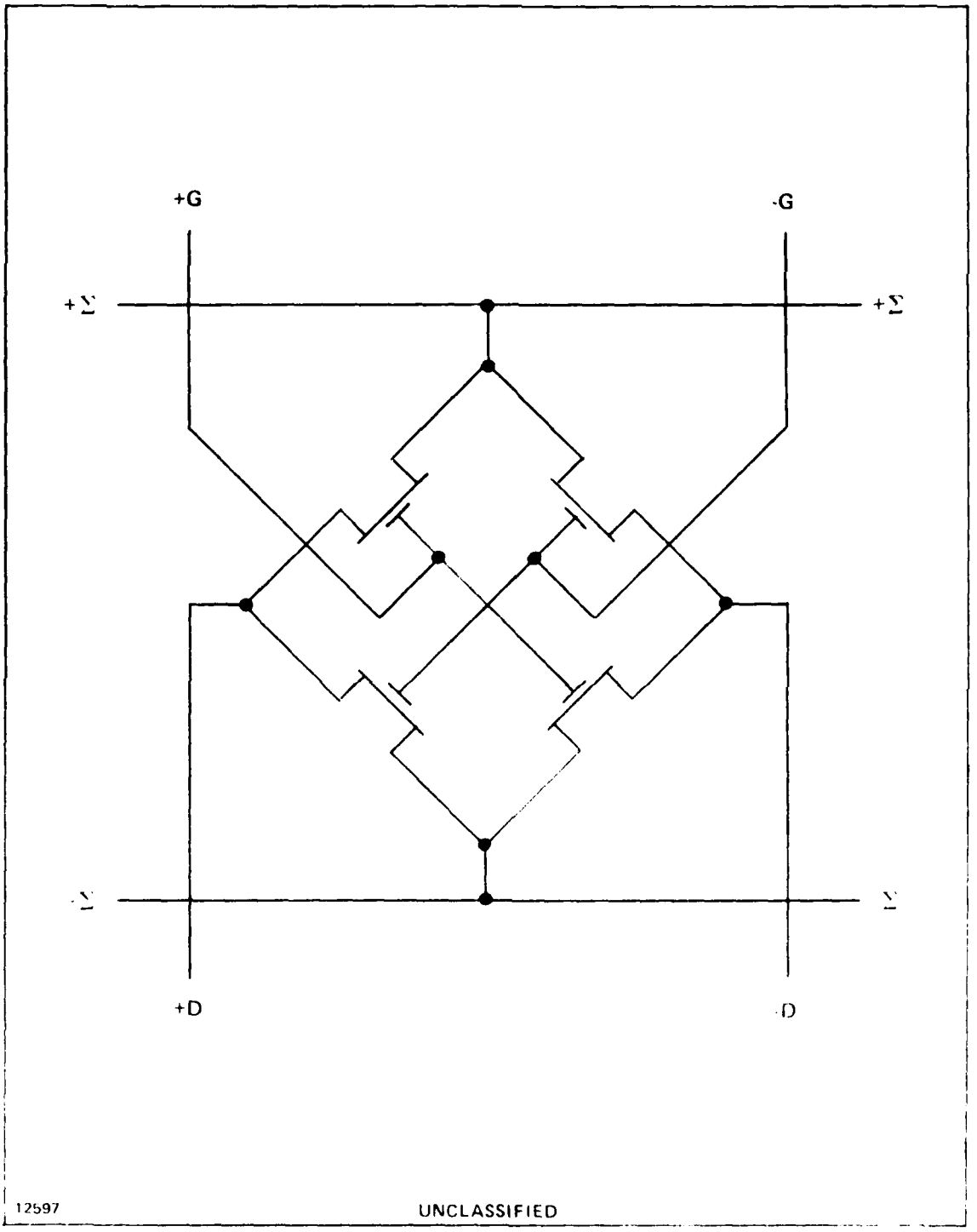


Figure 2-10 - Bridge Multiplier

TABLE 2-2
CHART OF TERMS PRESENT IN FOUR POSSIBLE MULTIPLIER DESIGNS

Form of Term	Source of Term	Relative Magnitude	Dual MOSFET		Quad MOSFET	
			Ref. Balanced	Differential	Ref. Balanced	Dual Differential
1	Threshold Voltage	Large	-	-	-	-
V_G	Gate Leakage	Very Small	X	X	-	-
V_D	Source drain Leakage	Small	-	-	-	-
V_G^2			X	-	-	-
V_GV_D	Transconductance DESIRED TERM	Large	X	X	X	X
V_D^2	Drain-voltage induced V_T shift	Large	-	-	-	-
V_G^3			X	X	-	-
$V_G^2V_D$	Mobility decrease at high surface charge	Moderate	X	-	X	-
$V_GV_D^2$	Mobility decrease at surface charge	Moderate	X	X	X	-
V_D^3						
V_G^4			X	-	-	-
$V_G^3V_D$			X	X	X	X
$V_G^2V_D^2$			X	-	X	-
$V_GV_D^3$			X	X	X	X
V_D^4			X	X	X	X

TABLE 2-3
FIRST AND SECOND ORDER ERROR TERMS RESULTING
FROM DC OFFSETS AND QUADRATIC CCD DISTORTION

	Resulting Term									
Source Term	1	V_G	V_D	V_G^2	V_GV_D	V_D^2	V_G^3	$V_G^2V_D$	$V_GV_D^2$	V_D^3
First Order V_GV_D	X	X	X	•	X	•	–	•	•	–
V_D^2	X	–	X	–	–	X	–	–	–	•
Second Order $V_G^2V_D$	•	•	•	•	•	–	–	•	–	–
$V_GV_D^2$	•	•	•	–	•	•	–	–	•	–
Net Term	X	X	X	–	•	X	–	•	•	•

If the source voltage is balanced to the drain inputs for the multiplier of type 1, it has the characteristics of the dual-reference balanced design No. 3. Only the dual-differential design No. 4 cancels all undesired MOSFET multiplier and CCD output amplifier terms to first and second order.

2.3 Selected Design

2.3.1 General

The design selected for the correlator/convolver employs two dual-channel differential CCDs with surface channels, source-follower, buffered, switches, FG taps switched at each stage and four-transistor MOSFET bridge multipliers. Although this approach requires the greatest chip area, the potential accuracy for improvement from the use of four-transistor multipliers in the presence of expected parameter variations (ΔV_T, Δg_m $\Delta R_{interconnect}$) was found to be well worth the cost in chip area.

Surface channel CCDs were selected because the linearity and dark current characteristics have been superior to those obtainable from buried channel devices. The charge transfer efficiency of surface channel CCDs, especially with the wide channels used here, has been shown to be adequate. This choice is not irrevocable, since the same mask set can be used to make a buried channel version.

Two input control gates were provided to each CCD channel so that they can be operated in either the gated diode or potential equilibration mode.

Switched FG taps were chosen to ensure that no loss of transfer efficiency would result from the presence of the taps on the delay line.

Source-followers were provided to isolate the FG taps from the multipliers and the interconnect lines. This improves the sensitivity of the taps, maintains equality of sensitivity for the four CCD channels, eliminates spurious cross-coupling of clock signals due to interconnect capacitance (except for switching transients) and provides the needed current source/sink capability for the taps driving the MOSFET drain inputs to the multipliers.

A four-phase CCD was chosen because it offered simpler processing and greater charge handling capacity. As with the choice of a surface channel, this choice is not irrevocable. The same mask, set with one additional implant, would provide a two-phase device.

Details of the design analysis of the multiplier cell and the source-follower buffer amplifiers are given in the next subsection.

2.4 Circuit Design and Optimization

2.4.1 Multipliers

Four types of multipliers are possible using MOS transistors. Two of them use a two-transistor cell and two of them use a four-transistor cell. Several general conclusions applicable to all of the designs emerged from a computer analysis performed early in the program.

First, with large transistor geometries, perfectly matched threshold voltages and transconductances and with proper and exact input voltages and biases, all four designs perform essentially perfectly. Second, when the channel lengths are reduced to 0.8 mil, small-channel effects result in a small nonlinearity (less than 0.5 percent). The two-transistor differential multiplier has twice the output signal but the same percentage nonlinearity. The four-transistor dual-differential bridge multiplier has a four times larger output signal, but again the percentage nonlinearity is the same.

The third general conclusion, applicable to all of the multipliers, is that a considerable voltage offset is required between the input signals applied to the drains of the multiplier transistors and those applied to the gates of the transistors. The voltages on the gates must be large enough to ensure that the transistors are always in the linear region of operation. Table 2-4 lists input signal conditions that are adequate. A worst case (maximum voltage on drain/minimum voltage on gate) offset of 2 volts (V) is provided. As discussed in the section on source-follower design that follows, separate bias rails have been used to permit the source-follower offsets to be adjusted externally for satisfactory operation.

2.4.1.1 Two-Transistor Reference-Balanced Multiplier

Computer analysis clearly showed two major weaknesses of this multiplier cell. The first is a severe dependence on the current summing bus bias levels compared to the zero-reference input signal level applied to the drain inputs. When the summing bus bias was reduced by a slight 0.1 V from 8.0 V to 7.9 V, the peak multiplier error increased

TABLE 2-4
INPUT SIGNALS USED IN EVALUATIONS OF MULTIPLIER CELLS

	Signals Applied To Gate Inputs (V)	Signals Applied To Drain Inputs (V)
Zero reference	12	8
Peak amplitude	1	1
Signal range	11-13	7 to 9

from less than one half percent to more than 10 percent. The problem arises from the fact that the output of this circuit is the product of the gate input signal relative to its zero-reference value and the drain input signal relative not to its zero-reference but to the summing bus bias. If there were only one multiplier in the device, the bias on the summing bus could be adjusted. However, processing variations across a device can be expected to cause small differences in source-follower characteristics (and hence zero-reference drain signal levels) from one end of the device to the other. It would then be impossible to get acceptable performance from all of the multipliers simultaneously.

The second major problem encountered was the output voltage distortion at the source-follower outputs due to variations in the drain currents furnished to the multiplier. This effect will be referred to as pulling in the discussions which follow. For example, when the two-transistor multiplier cell was driven with the source-follower, described in Table 2-6, to be seen later, and using the input signal condition listed in Table 2-5, the maximum multiplier error was 0.2 percent if the multiplier transistors has an impractical width-length (W/L) ratio of 0.001. For a more practical value of W/L of 0.25 (W = 0.2 mil, L = 0.8 mil), source-follower pulling caused the peak error to soar to 13 percent.

Two kinds of pulling are involved. For a fixed input level to the drain signal source-follower, changes in gate input signal cause the current drawn by the multiplier to vary. For a multiplier cell with W/L = 0.25, the current drawn ranges overall from 25 μA of current sink to 21 μA of current source. For a fixed drain input signal, the current variation with gate input signal is as much as 5 μA. At a 12 KΩ output impedance, the source-follower swings about 0.06 V or 10 percent of full scale.

TABLE 2-5
INPUT SIGNALS TO SOURCE-FOLLOWERS USED
IN ANALYSIS OF COMPLETE MULTIPLIER CIRCUITS

	Signals Applied To Followers Driving Gates	Signals Applied To Followers Driving Drain
Zero Reference (V)	14	9.5
Peak Amplitude (V)	1	1
Signal Range (V)	13-15	8.5-10.5
Approx. Follower Output Zero Reference Level (V)	11-1/2	7-1/2
Approx. Peak Amplitude of Follower Output	0.9	0.6

A second kind of pulling results from changes in current as the drain signal varies, even with the gate signal held constant. To a first order of approximation, this simply reduces the gain of the source-follower. However, it also introduces a nonlinearity in the source-follower. Analysis of the computer data showed a 4.2 percent maximum deviation when the gate input signal was held at its zero-reference value.

Because of these pulling effects, this multiplier could be used only if the current drawn could be substantially reduced and/or the source-follower output impedance substantially reduced. Both changes would require transistors of much greater size (length in the case of the multiplier MOSFETs and width in the case of source-follower driver FETs). This would be hard to achieve within the constraints of CCD pitch and chip size.

2.4.1.2 Two-Transistor Differential-Gate Multiplier

This cell was not examined in detail. It does nothing to alleviate the severe sensitivity of the reference-balanced cell to variations in offset between drain input level and summing bus bias. It does solve the problem of cross-pulling of the source-follower by changes in the gate input signal. As the gate signal changes, the increase in current in

one of the transistors is quite precisely balanced by a decrease in current in the other transistor with the inverted gate signal. In this respect, this multiplier cell is just one half of the dual-differential cell and a complete discussion of the current balancing can be found under that heading. The self-pulling non-linearity problem with the source-follower is still present. For the added complexity of one differential-channel CCD, the circuit offers little improvement. The benefits of going to dual differential-channel CCDs are much greater.

2.4.1.3 Four-Transistor Reference-Balanced Multiplier

This cell also was not examined in detail. It overcomes the sensitivity to summing bus bias errors, but it suffers just as much as the two-transistor reference-balanced multiplier from self-pulling and cross pulling in the drain signal source-follower. The simplicity of normal, nondifferential CCD channels could make additional real estate available for the larger transistors needed to solve the pulling problem. However, the area savings we found to be insufficient to justify the inclusion of this approach in the correlator/convolver test pattern design.

2.4.1.4 Four-Transistor Dual-Differential Bridge Multipliers

This multiplier cell performed exceptionally well in the computer simulations, overcoming all of the problems uncovered in the other designs.

a) **Summing Bus Bias** - When the bias levels on the summing buses are shifted relative to the zero-reference level of the drain inputs, the main effect is to add a common-mode current to the two current buses. A secondary effect is a small change in the overall gain of the multiplier. For the input signal conditions described in Table 2-5 and with the current bus bias reduced to 7.5 V (an offset of 0.5 V, five times greater than that applied to the two-transistor multiplier), the maximum deviations increased from 0.46 percent to 0.9 percent. Most of this was due to a gain increase of about 0.8 percent. Based on a new gain value, the maximum error of the multiplier was only 0.24 percent. Thus, the accuracy of the multiplier is actually improved when it is operated with the summing buses offset to a

slightly lower voltage. This has the drawback of introducing common-mode current which would require better common-mode rejection in the differential current amplifier and might degrade signal-to-noise performance.

b) **Source-Follower Pulling** - Under the signal conditions of Table 2-5 and with the drain-driving source-follower load current at about 40 μA, maximum pulling of the source-follower output by gate-input changes was 0.00008 V (about 0.02 percent of full scale). The changes in the currents in the paths with the normal and the inverted gate signals balanced each other to within 0.007 μA. Perturbations in device geometries will result in less perfect cancelling in a real device, but errors larger by close to two orders of magnitude would still be acceptable.

The self-pulling of the source-follower still results in a significant nonlinearity (4.6 percent) in its output. Nevertheless, the maximum error in the multiplier is only 0.15 percent. This is a dramatic indication of the extent to which the structural symmetry of the entire circuit nullifies nonlinearities in the individual circuit elements.

This is made even more dramatic when the load current in the source-follower for the drain signal is cut in half to about 20 μA. Under these conditions, the multiplier current load is between 19 μA of sink and 17 μA of source. The current through the driver transistor varies from 3 μA to 40 μA. The nonlinearity in the source-follower output is nearly 10 percent and yet the overall multiplier accuracy is better than 0.8 percent.

When an offset of -0.55 V is added to the summing bus biases, the current through the driver transistor varies from 13 μA to 56 μA; the source-follower linearity improves to 5 percent and the overall multiplier error is less than 0.3 percent.

This circuit was further analyzed with the input voltage swings increased from 2 to 3 V peak-to-peak. The drain signal zero-reference was raised to 10 V, and the V_{DD} bias of the drain-signal source-follower was increased from 10 V, to 10.5 V. Source-follower nonlinearity with 40 μA load current was 7.4 percent; overall multiplier error was a maximum of 0.4 percent.

2.4.2 Source-Followers

Source-followers are needed to buffer the outputs from the FG taps on the CCDs to the inputs of the multiplier circuit in order to prevent reverse coupling and to provide adequate drive capability. This is particularly true of the outputs that drive the drain inputs to the multipliers, since a steady current is required. The configuration of a source-follower is shown in **Figure 2-11.**

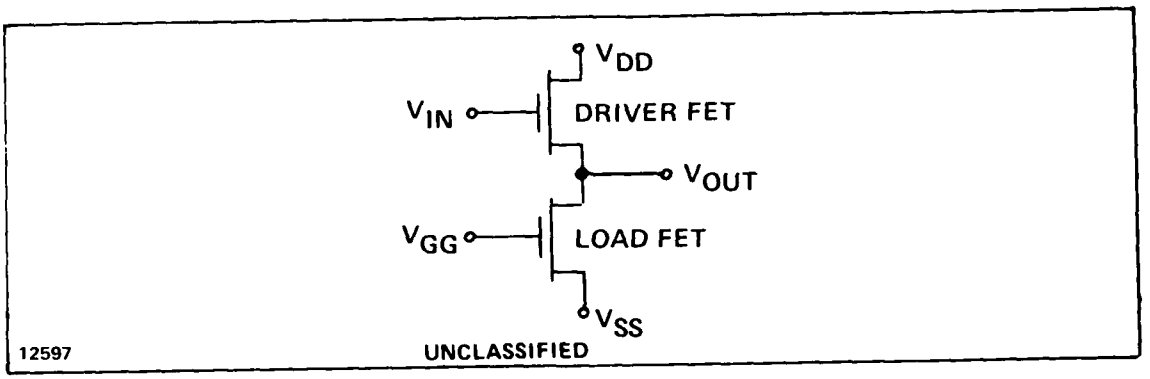


Figure 2-11- Schematic of Source-Follower

The main design considerations are: linearity, drive capacity and power consumption. The source-follower was analyzed first without any load. Nearly perfect linearity can be achieved provided the load and driver transistors are both maintained in the saturated region of operation. As a rough rule of thumb, this means that V_{GG} is below the minimum value of V_{out}, and V_{DD} is above the maximum value of V_{IN}. Power is minimized when V_{GG} and V_{SS} are as close as possible, but a reasonable margin is required between V_{GG} and V_{SS} to prevent small variations in threshold voltage from seriously affecting the load current level.

As mentioned earlier, the analysis of the performance of the multiplier cells showed that a considerable offset is required between the voltage levels applied to the gates and those applied to the drains. Obtaining the lower voltages from the drain-driving source-followers by using a small W/L ratio for the driver and pulling a large current through it was considered. This, however, results in high power consumption

and cannot give an adequate offset. It was decided instead to offset the clock voltages at which the FGs of the two CCDs are driven. This does not affect CCD performance, achieves a larger offset and is adjustable externally (without mask changes).

The source-follower parameters listed in Table 2-6 were chosen for the subsequent analysis. They are consistent with the requirements of the layout and design rules and adjustments in the bias and supply voltages permit satisfactory operation over a wide range of conditions.

TABLE 2-6
SOURCE-FOLLOWER PARAMETERS CHOSEN
AS A RESULT OF COMPUTER ANALYSIS

Parameters	Source-Followers Driving Gates	Source-Followers Driving Drains
Driver FET Width	0.5 mil	0.5 mil
Driver FET Length	0.2 mil	0.2 mil
Load FET Width	0.4 mil	0.4 mil
Load FET Length	0.8 mil	0.4 mil
VDD	14 V	10 V
VBB	11.5 V	7.5 V
VSS	8.4 V	4.8 V
Approx. Load Current	20 μA	40 μA
Power Dissipation (No External Load)	110 μW	210 μW
Output Impedance (No External Load	18 KΩ	12 KΩ
Input Signal Range	12.5 - 15.5	8 - 11 V

2.4.3 Parameter Variation Sensitivity Analysis

The sensitivity of the correlator/convolver performance to parameter variations was also investigated using computer models. The most critical parameters are expected to be the 0.2 mil channel widths in the multiplier transistors and the 0.2 mil channel lengths in the source-follower drivers. The effects of variations in these values were studied by calculating the effect of exaggerated errors.

2.4.3.1 Drain-Driving Source-Follower

When the channel length of the driver transistor in one of the two source-followers whose outputs feed drains of the multiplier transistors were increased by 1 μm (20 percent), the overall multiplication accuracy was degraded to 6.4 percent, an error that appears almost entirely as a feedthrough of the signal applied to the multiplier gates. The change in transconductance in the source-follower has two effects. One is a change in gain of about 6 percent and the other is a change in the zero-reference output level of about 75 millivolts (mV) or 12 percent of the signal amplitude. Analysis of the four transistor multiplier alone shows that the gain error contributes no measurable degradation in accuracy; the error arises entirely from the offset error, half of which appears as common mode and is rejected and half of which appears as normal mode where it acts as a dc drain signal. In the two transistor multiplier, which lacks common-mode rejection, the error under the same conditions is nearly twice as large.

One can expect a reduction in error if the minimum geometries are increased. For example, the channel length in the driver transistor can be increased to 0.4 mil provided some dc bias conditions are adjusted. A 1 μm increase in channel length is now only a 10 percent error. The multiplier error decreases by about one quarter to 4.7 percent. The reduction is less than one half because the impedance level increases. One pays a power penalty because the V_{DD} to V_{SS} voltage drop is larger and, if the transistor geometry becomes too large, one encounters problems in routing conductors around the transistors. However, should we encounter difficulties with our present dimensions, some room for reducing error sensitivity is available.

2.4.3.2 Gate-Driving Source-Followers

If the same variation is applied to the transistors in the source-followers driving the gates of the multiplier transistors, the effect and its cause are the same except that the error now consists of feedthrough of the drain signal.

2.4.3.3 Multiplier Transistors

When the 0.2 mil width of one of the multiplier transistors is increased by 1 μm (20 percent), a much larger error appears in the simulation, about 17 percent. This error consists of feedthrough of the drain signal. When this feedthrough signal is removed, the residual error is less than 1 percent. The current in the modified transistor is, to first order,

$$I = (g_m + \Delta g_m) \quad (V_G^{SIG} + V_G^{(0)} - V_{TH})\, V_D - \tfrac{1}{2} V_D^2 \tag{10}$$

The change in current due to the change in g_m is:

$$\begin{aligned} \Delta I = {} & \Delta g_m\, V_G^{SIG}\, V_D \\ & + \Delta g_m\, (V_G^{(0)} - V_{TH})\, V_D \\ & - \tfrac{1}{2} \Delta g_m\, V_D^2 \end{aligned} \tag{11}$$

The usual total output current from the four transistors together is

$$4 g_m\, V_G^{SIG}\, V_D^{SIG} \tag{12}$$

The first term represents a modest fractional gain change of

$$\tfrac{1}{4} \frac{\Delta g_m}{g_m} \tag{13}$$

The second term is the source of the large feedthrough of the drain signal. It represents a peak error to peak signal ratio of:

$$\frac{1}{4}\frac{\Delta g_m}{g_m}\frac{V_G^{(0)} - V_{TH}}{AMP} \tag{14}$$

where AMP is the amplitude of the input signals. Since $V_G^{(0)}$ must be offset from V_{Th} by at least twice, and typically three to four times AMP, this term becomes very large. Clearly, its effect is minimized by operating with as little gate signal offset as possible.

The final term is the small residual quadratic distortion. The results of the computer simulation show less of this distortion than the above equation predicts.

2.4.3.4 Conclusions

Geometrical variations in the source-follower transistors introduce inaccuracies into the multiplier output only as a result of offsets in the zero-reference level outputs. To achieve 1 percent accuracy, these offsets must be held to the order of 10 mV. Transconductances among the source-follower transistors associated with each differential CCD must be held within about 3 percent, a figure that probably can be achieved. If not, the minimum device dimensions can be increased somewhat. It should also be mentioned that feedthrough errors are among the least critical for most applications because the error signals will add incoherently along with 256 stages of the correlator, and an effective processing reduction on the order of $256^{-1/2} = 1/16$ can be expected.

The sensitivity of the selected multiplier to offset errors in the signals applied to its inputs points up another problem which is in all likelihood more serious than that of balancing the two source-followers. This is the inevitable dc imbalances between the two halves of each differential CCD. Large clock feedthrough signals occur because of capacitive coupling between pairs of lines. It is, therefore, imperative that independent biasing controls be maintained over the two halves of the CCDs. Consequently, we have brought out most clock and bias lines independently on the chip.

The selected multiplier is especially sensitive to variations in transconductance because of the $V_G^{(0)} - V_{TH}$ amplification factor. However, the four transistors in the multiplier cell are in very close proximity and oriented in such a way that parametric variation between them will be minimized.

All of the effects described herein are no greater in the four transistor multiplier than they would be in a two transistor multiplier, with minimum geometrical features that are twice as large. Thus there is no sacrifice in performance in going to the four-transistor cell, the fine geometrical features notwithstanding.

3. TRANSISTOR THRESHOLD VOLTAGE UNIFORMITY

As described in the previous chapter, close tracking of threshold voltages and transconductances of the transistors within parts of each stage of the correlator/convolver are critical to the accuracy of the device.

The analysis showed that, by virtue of symmetry and close location, the multiplier transistors will not be the major source of such errors. The major source is expected to be the lack of perfect matching of the offset voltages associated with each pair of source-followers driving the multipliers. If, for example, we assume that a 2 V peak-to-peak input is achieved at the multiplier input nodes, each pair of source-followers delivering the inputs must have a match of its two quiescent output levels to within 20 mV. This maximum mismatch of 20 mV includes all errors and must be maintained in spite of the relatively large spacing between the two source-followers (approximately 40 mils). The offset error will have first order contributions from variations in threshold and transconductance of the source-follower drivers, FG reset clock feedthrough capacitance and interconnect infrared (IR) drops. Variations of transconductance and threshold of the source-follower load devices are expected to have only second order effects.

With these requirements in mind, a test chip was designed with various subunits of the complete chip. Details of the test chip are given in Subsection 6.4. For the present discussion, we note that the test chip contains clusters of individual transistors, clusters of bridge multipliers, and short differential CCDs with FG output taps and source-follower buffer amplifiers. Manual measurements were performed on source-followers as described in Section 1. In addition, four software programs were written, debugged and used to investigate parameter variations on several wafers of correlator/convolver test patterns using the MITE and Sentry 7 automatic test systems, as shown in Table 3-1. These results are presented in Section 2.

Together, the results indicate that short-range random variations in parameters such as threshold voltage and transconductance are small enough to meet contract requirements. In a 256-stage correlator/convolver, there will, in all likelihood, be some stages whose inaccuracies exceed the 1 percent goal and others whose accuracy greatly exceeds the requirement. On the whole, short-range random parameter variations are consistent with the overall performance desired for the correlator/convolver.

TABLE 3-1

CORRELATOR/CONVOLVER TEST PATTERN AUTOMATED TEST PROGRAMS

Tester	Program
Sentry 7	Threshold and transconductance variations of the transistor test patterns (five different geometries in clusters of five devices).
MITE	Same as above.
MITE	Output voltage level variations for the floating gate tap source followers in the differential CCD test patterns.
MITE	Transconductance and threshold variations of the CISO (Common Input Separate Output) multiplier test pattern transistors.

Long-range random or systematic variations are not a problem by virtue of the characteristics of the bridge multiplier. Medium-range random variations, however, can be a problem and, in the test patterns, are somewhat larger than desired. The final 256-stage correlator/convolvers were processed using three in. wafers and projection photolithography.

In addition, the maskmaking software was rearranged somewhat. Usually, the pattern generator makes exposures cell-by-cell, resetting the aperture many times between the exposures of identical areas. This was changed so that for critical patterns in the field oxide and first poly masks the pattern generator would expose all patterns with a given aperture before resetting to the next aperture. This eliminates variations in channel length and width that could occur as a result of variations in the pattern generator aperture setting.

3.1 Manual Source Follower Measurements

The dc offset characteristics of the source followers on the CCD test pattern were investigated by turning the floating-control gates ϕ_C on with a 15 V bias and using ϕ_3 to set the FGs to a fixed dc level. This test configuration is shown in Figure 3-1. The output voltages, V_{out}, were measured for the four outer and four inner taps on numerous test patterns. Some typical results are shown in Table 3-2.

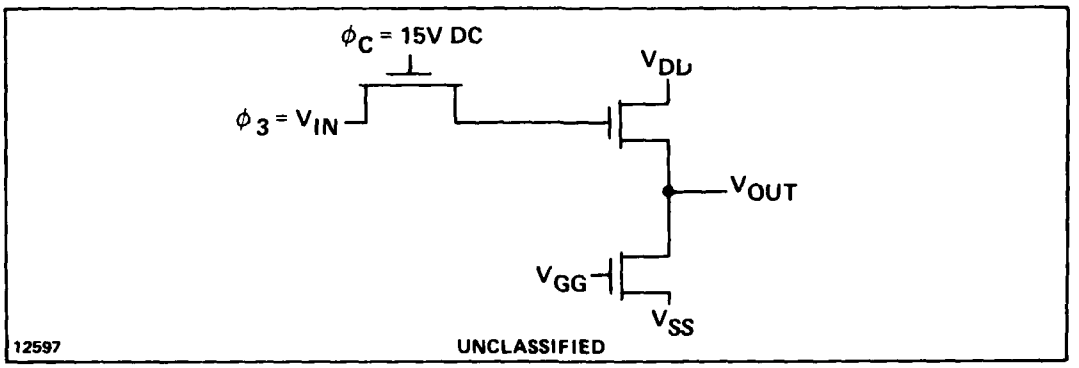


Figure 3-1 - Source-Follower Circuit

TABLE 3-2
SOURCE FOLLOWER DC CHARACTERISTICS

		Pattern 1	Pattern 2	Pattern 3
Outer Outputs	1	3.219	3.219	3.417
	2	3.208	3.237	3.398
	3	3.219	3.225	3.394
	4	3.220	3.272	3.406
Mean		3.217	3.238	3.404
Standard deviation		0.006	0.024	0.010
Inner Outputs	1	3.102	3.151	3.232
	2	3.141	3.156	3.239
	3	3.164	3.173	3.253
	4	3.136	3.157	3.245
Mean		3.136	3.159	3.242
Standard deviation		0.026	0.010	0.009

There are a number of useful statistics to be examined for the entire set of test data. For example, one can look at how uniform the outputs are for a set of four contiguous source-followers. The smallest standard deviation was 5 mV; the largest, 29 mV; and the mean standard deviation, 15 mV.

Next, one can look at the mean output voltage from one test pattern to the next. Comparing outer sets of source-followers only, we find a mean of 3.254 V with a standard deviation of 70 mV. Similarily, comparing inner sets of followers, we find a mean of 3.192 V with a standard deviation of 50 mV. The systematic difference between outer and inner followers that is apparent in the data in Table 3-2 is borne out by the full set of data, where there is a 60 mV average difference between outputs. Since the source-followers on the two sides of the CCDs are separately biased, this systematic difference can be partially compensated for.

3.2 Automatic Test Data

All test data was taken at microamp current levels comparable to the final operating conditions. Unfortunately, the measurement capability of both systems proved to be marginal for the tasks to be performed. In addition, Sentry 7 could only provide parameter distributions for the entire wafer. It could not compile distributions of matches of parameters within a chip without extensive new software.

Table 3-3 lists the performance specifications of both testers in the measurement ranges used for the measurement of the correlator/convolver test patterns.

TABLE 3-3
SPECIFICATIONS OF SENTRY 7 AND MITE TEST SYSTEMS
FOR g_m AND V_t MEASUREMENT AT LOW LEVELS

	Gate Voltage			Drain Current		
	Range (V)	Resolution (mV/step)	Accuracy (mV)	Range (μA)	Resolution (nA/step)	Accuracy (nA)
Sentry 7	0-2	2	0.1% ± 2	0-1	1	± 0.5% ± 10
MITE	0-1	1	1% ± 2	0-10	10	± 1% ± 100

The preceding table lists percent accuracies in percent of programmed value. Although the current range, resolution and accuracy are entirely adequate for devices operating at 10 μA to 20 μA drain currents, the gate voltage resolution and accuracy is marginal for the correlator/convolver since these are within an order of magnitude of the desired match of threshold voltage between nearby devices.

The software of Table 3-1 was developed in full recognition of this problem, assuming that measurements made within a short time of each other would probably reflect a better-than-specified accuracy.

The data from both automated testers was found to have less accuracy than expected because of quantization error. A considerable amount of data was collected and in spite of the marginal accuracy of some of the measurements, some useful information was obtained. Figures 3-2 through 3-6 show sections of several wafer maps prepared from data taken using the Sentry 7 and MITE systems to determine the distributions of threshold variations within five-transistor clusters across wafer 16. Five different transistor types were measured. Each wafer map shows the mean and standard deviation of V_{th} at six test pattern locations using a source-drain voltage of 10 V and drain currents of 1 μA and 10 μA.

The standard deviations of Figures 3-2 throught 3-6 are plotted in Figure 3-7 in a channel length (L) by channel width (W) format. In view of the way the standard deviations vary with drain current, one cannot conclude that there is any clearly statistically significant difference between the values. Halving the channel W from 0.4 to 0.2 mils does not appear to cause a large increase in threshold voltage variation. The use of a very short channel L (0.35 mils) may result in some increase in parameter variation.

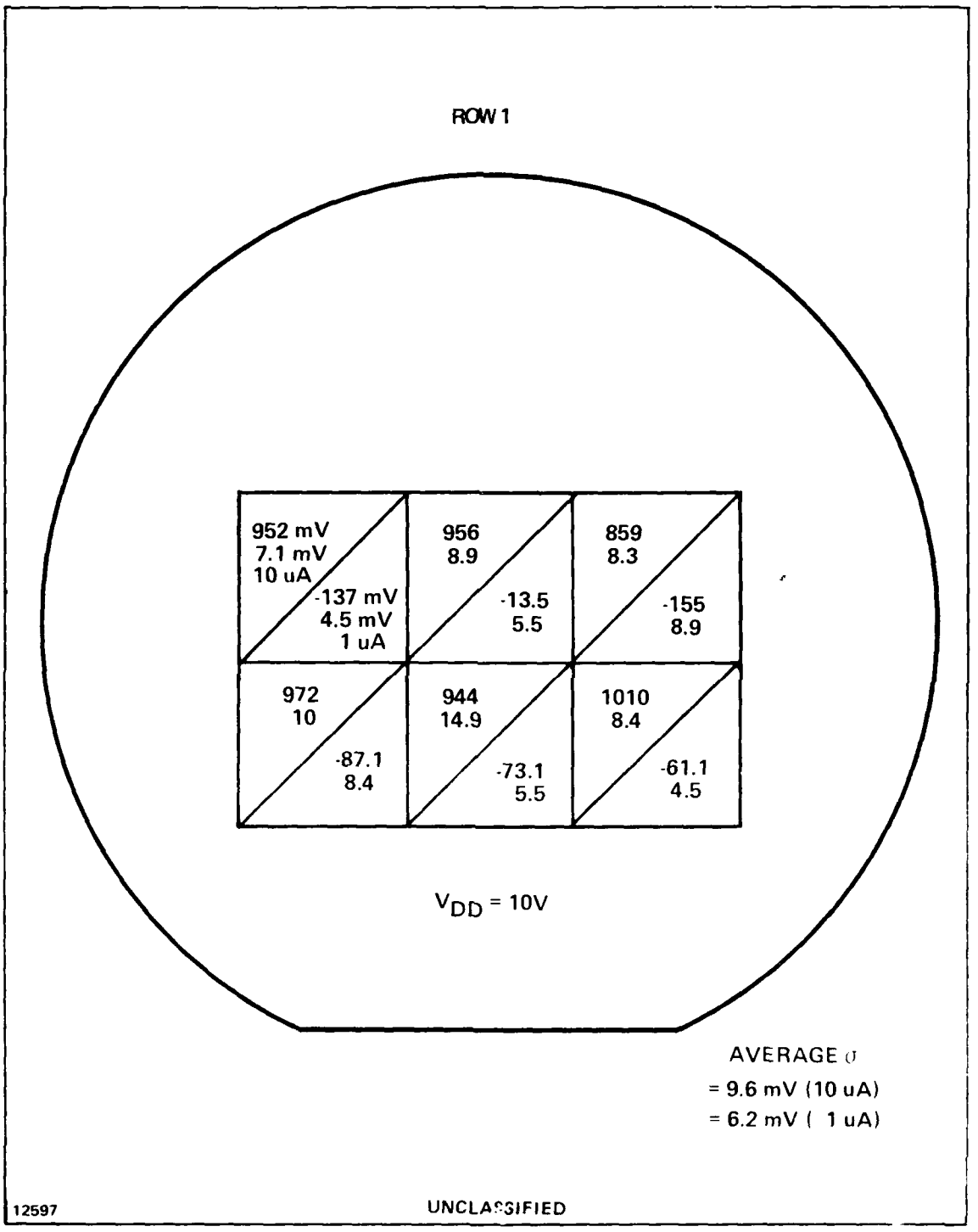


Figure 3-2 - Threshold Means and Standard Deviations of Five 0.2 x 0.8 MIL (Channel W & L) Multiplier Transistors (Wafer 16)

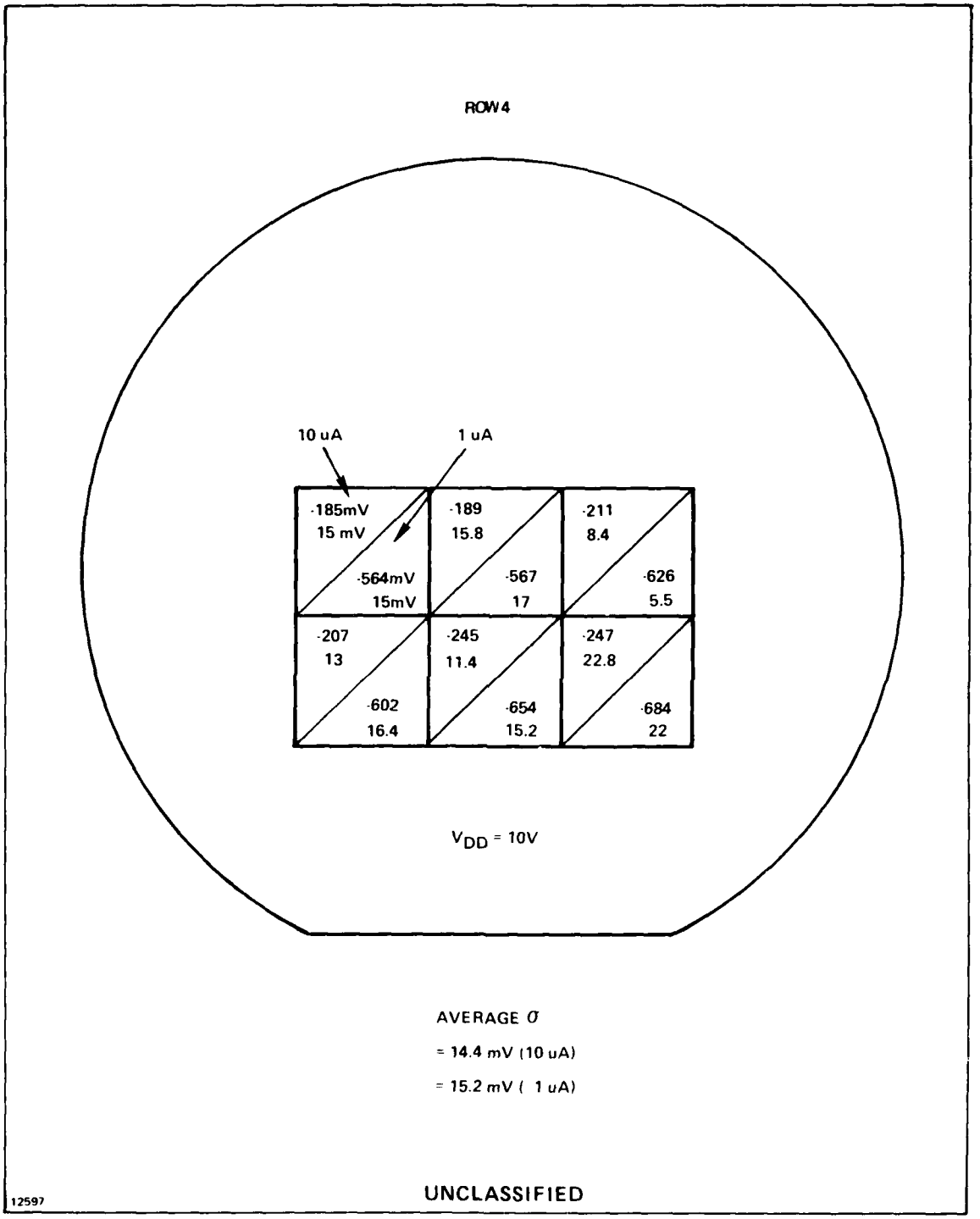


Figure 3-3 - Threshold Means and Standard Deviations of Five 0.4 x 0.5 MIL (Channel W & L) Source-Follower Driver Transistors (Wafer 16)

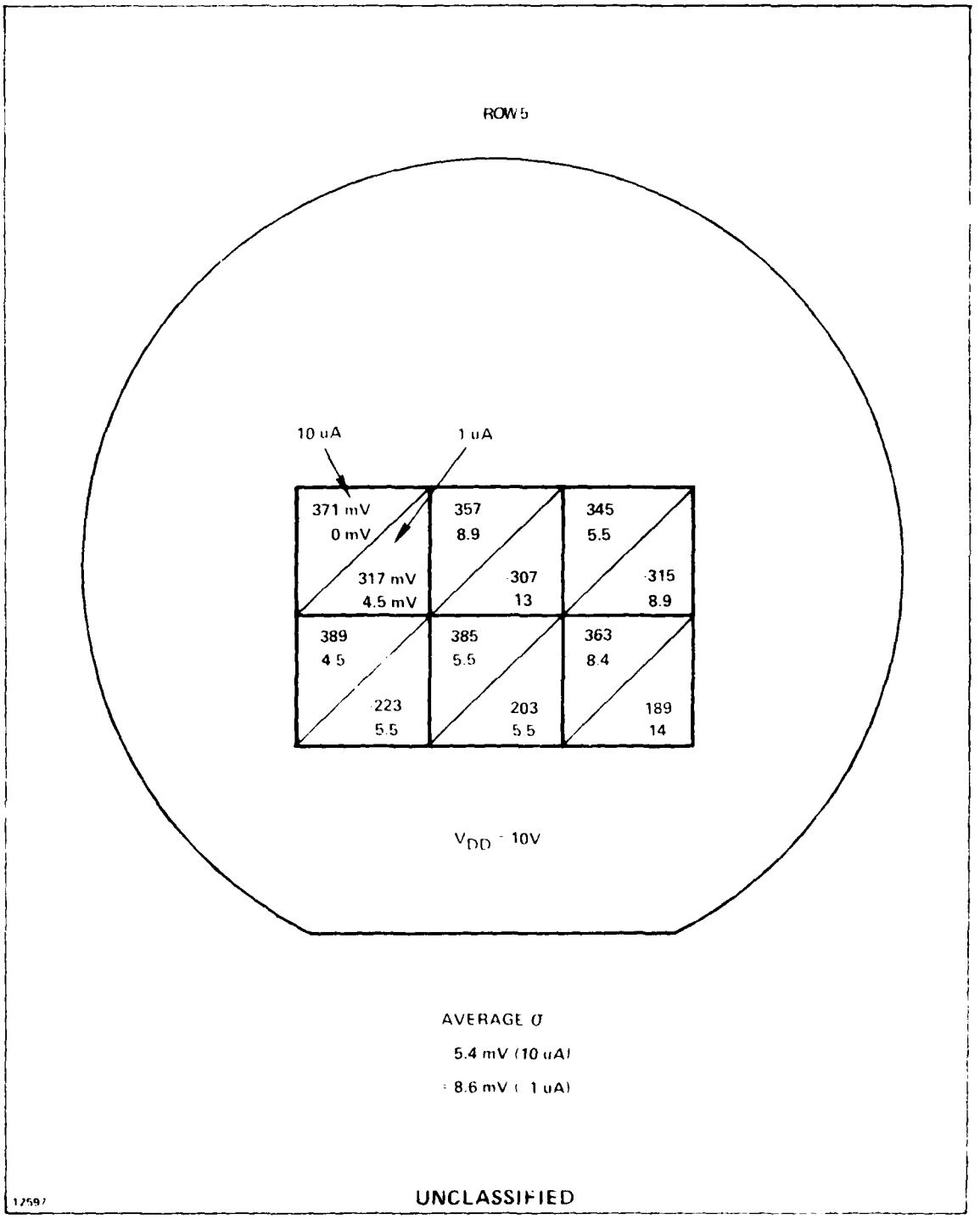


Figure 3-4 - Threshold Means and Standard Deviations Of Five 0.4 x 0.675 MIL (Channel W & L) Source-Follower Drain Driver Load Transistors (Wafer 16)

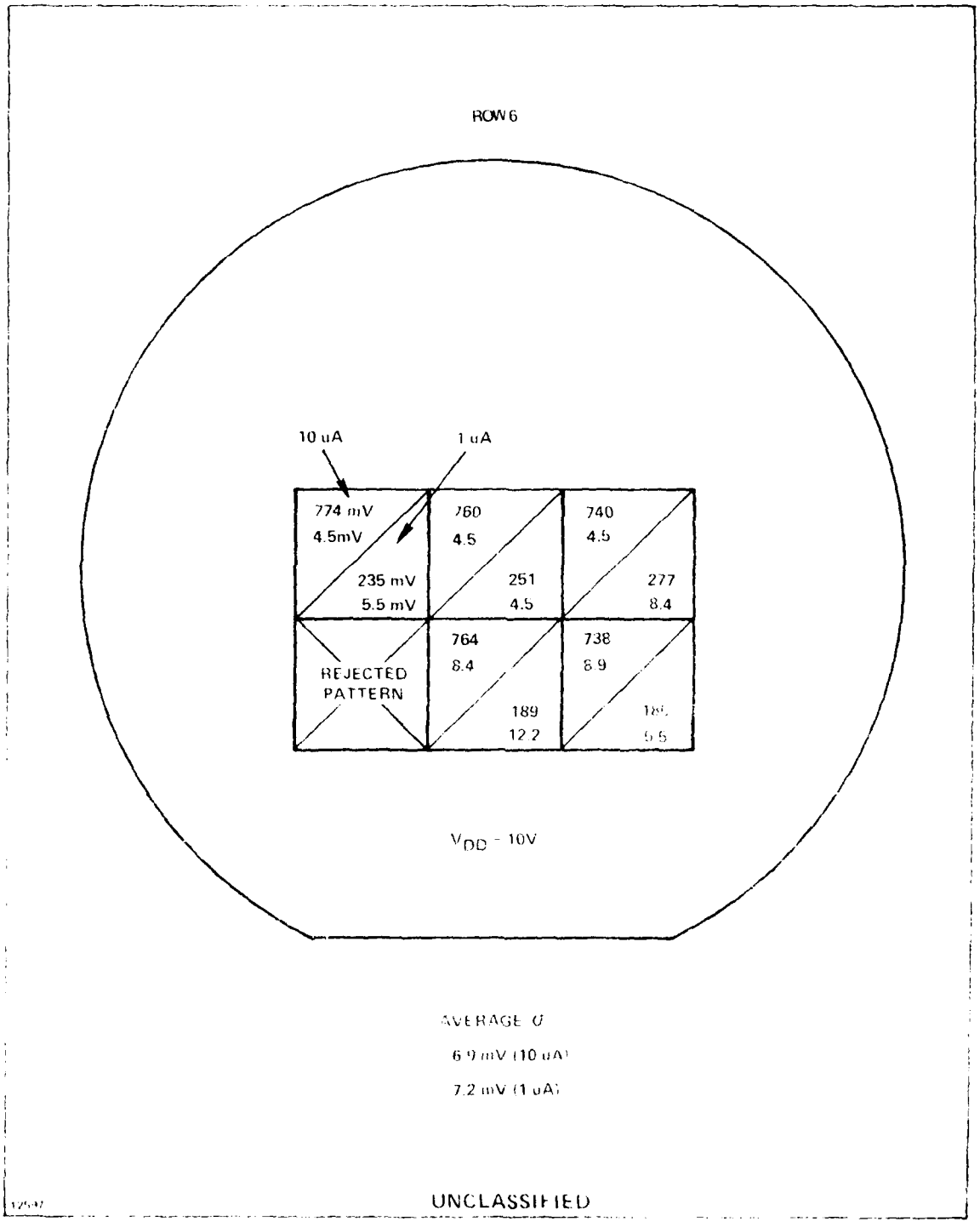


Figure 3-5 - Threshold Means and Standard Deviations of Five 0.4 x 1.15 MIL (Channel W & L) Gate Driver S.F. Load Transistors (Wafer 16)

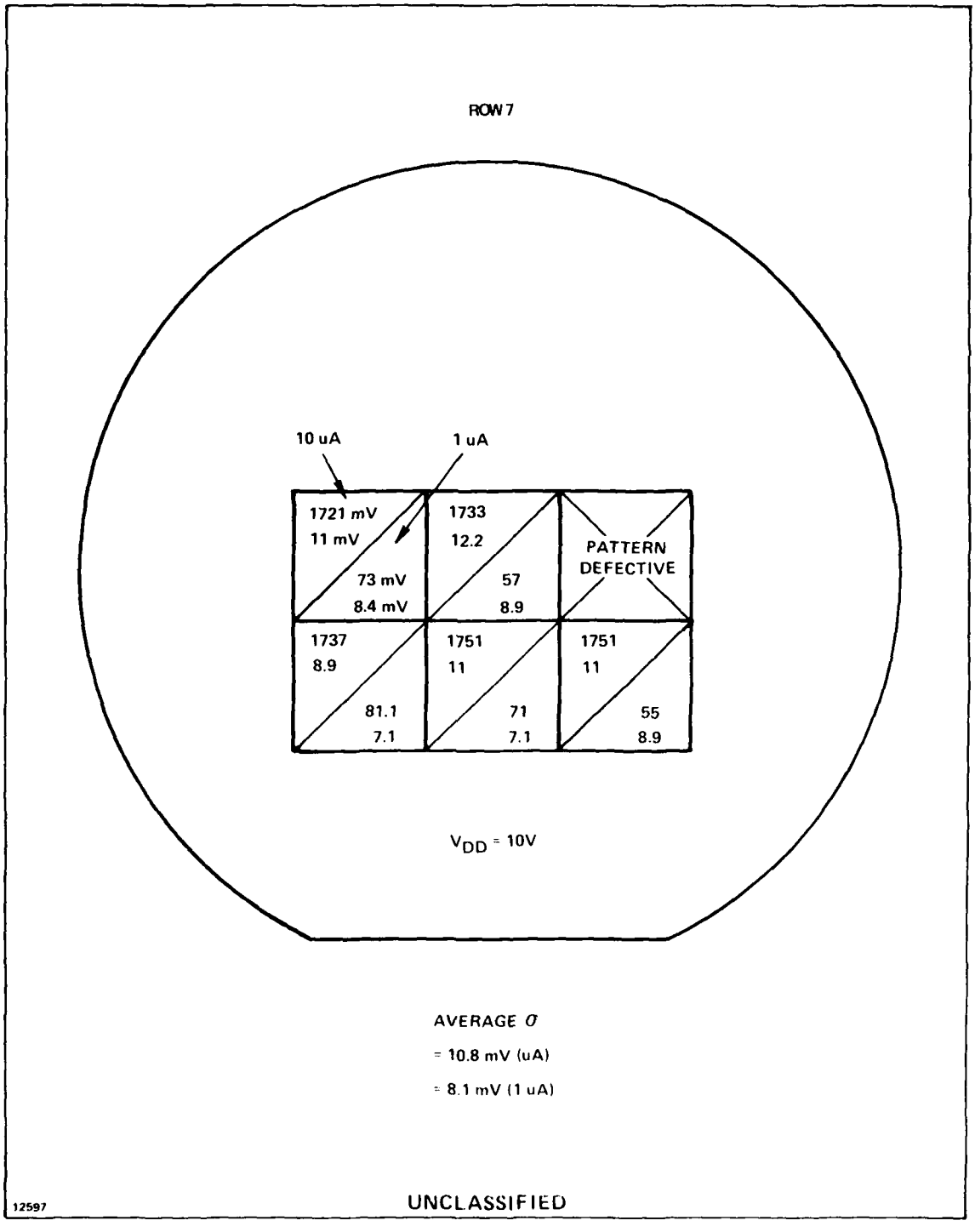


Figure 3-6 - Threshsold Measurement and Standard Deviation of Five 0.2 x 1.6 MIL (Channel W & L) Possible Multiplier (Not Used) Transistors (Wafer 16)

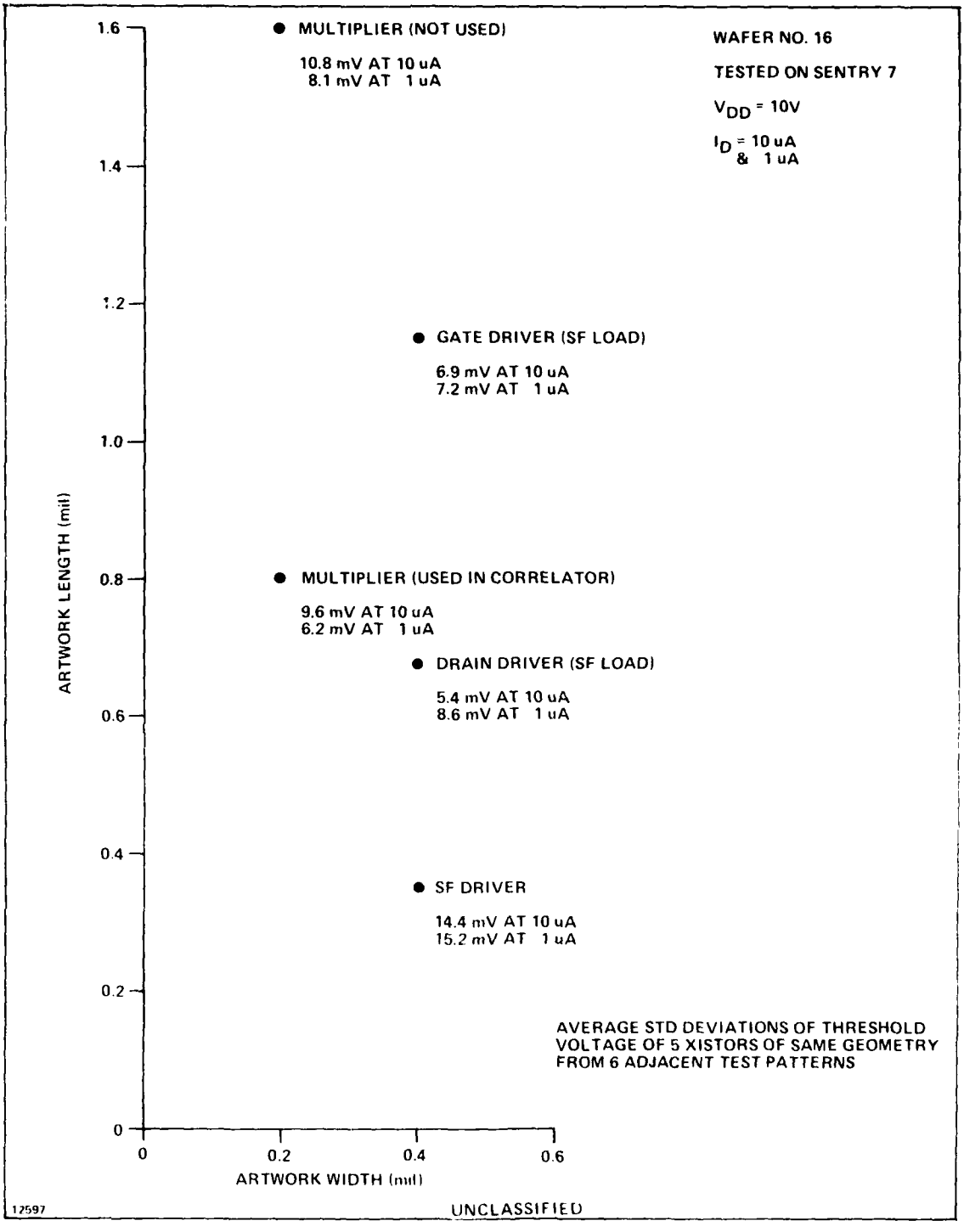


Figure 3-7 - Average Standard Deviations of Threshold Voltage of Five Transistors Of Same Geometry From G Adjacent Test Patterns

4. FLOATING GATES STUDIES

The individual CCDs with FG output taps on the test chip were studied to determine optimum operating conditions, linearity, maximum signal amplitude and noise level. We found that we could net a one percent nonlinearity requirement for signals of up to 4 V peak-to-peak. By using the potential equilibration input technique, we obtained a signal-to-noise ratio of approximately 80 dB.

4.1 Chip Schematic and Input Techniques

A partial schematic diagram of the FG CCD test pattern chip is shown in **Figure 4-1**. The CCD has a total of six stages, the second through fifth of which have FG output taps as shown. In addition, the CCD has a dual channel, so that the circuit of **Figure 4-1** really occurs twice in parallel. For the experiments performed here, the diffusions source and drain (CCD-S and CCD-D), IG1 and IG2, clock phases ($\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$ and ϕc) and the source-follower bias lines (V_{DD}, V_{GG} and V_{SS}) were connected in parallel.

The three elements of the input structure - CCD-S, IG1 and IG2 - were used in four different ways to control the conversion of input voltage to CCD charge. Two of them are shown in **Figure 4-2**. Both use equilibration of the channel potentials under IG1 and IG2 to meter the charge. The negative-going sampling pulse signal processor (SP) on the CCD-S diffusion initially overfills the input well under IG2. The charge injected into the CCD is given by Equation (15) provided $V_{IG2} \geq V_{IG1}$. If $V_{IG2} < V_{IG1}$, $Q = 0$. Also, as V_{IG2} approaches the high level of the clocks, the value of Q saturates. The coefficient C_{oxide} is the oxide capacitance of the IG2 electrode. The charge consists of electrons; hense Q is negative.

$$Q = -C_{oxide} \cdot (V_{IG2} - V_{IG1}) \qquad (15)$$

Since the constant oxide capacitance appears in this expression, the conversion of input voltage to charge is expected to be highly linear. This does not necessarily mean that the best overall device linearity will result, since the FG sensing may not be linear.

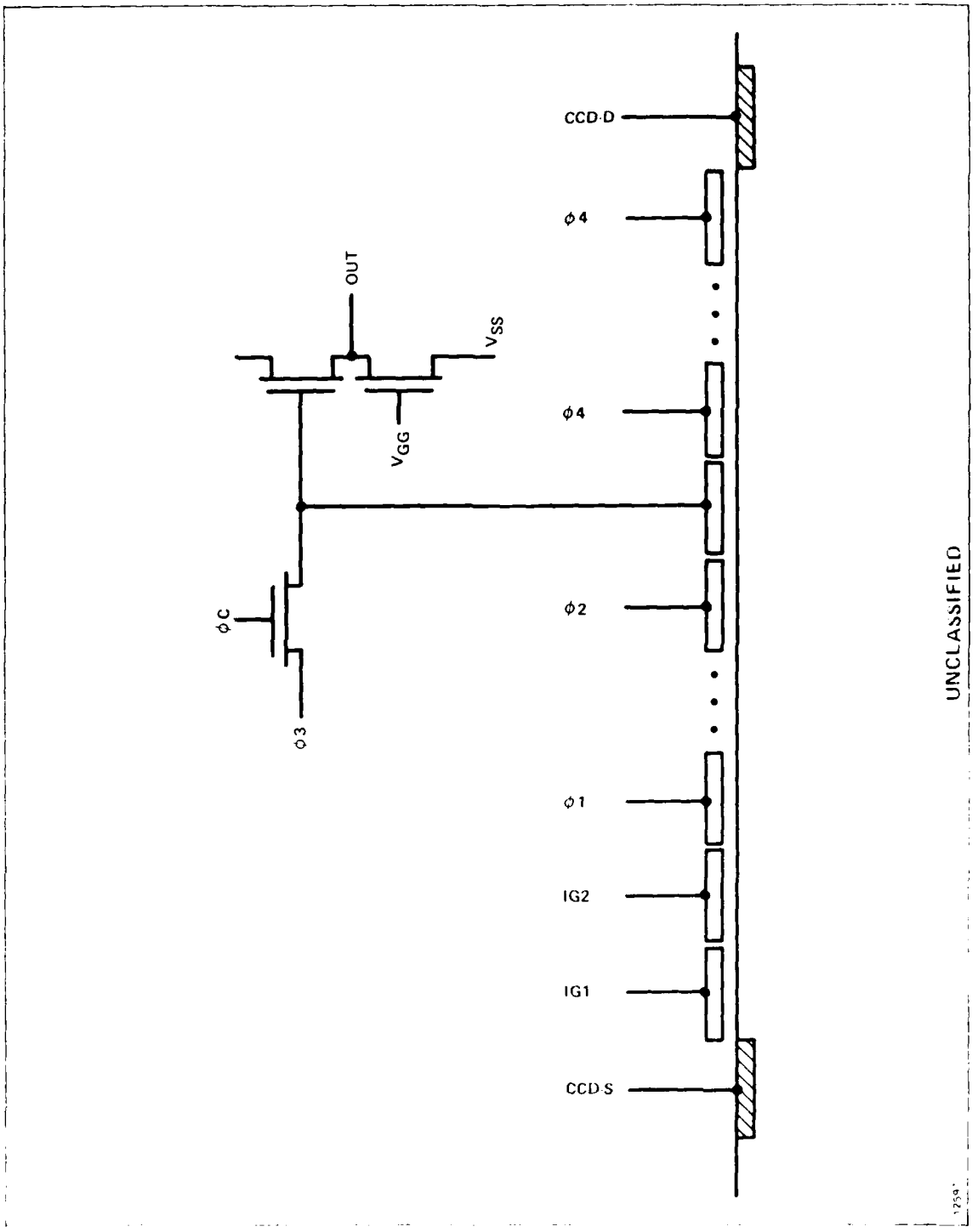
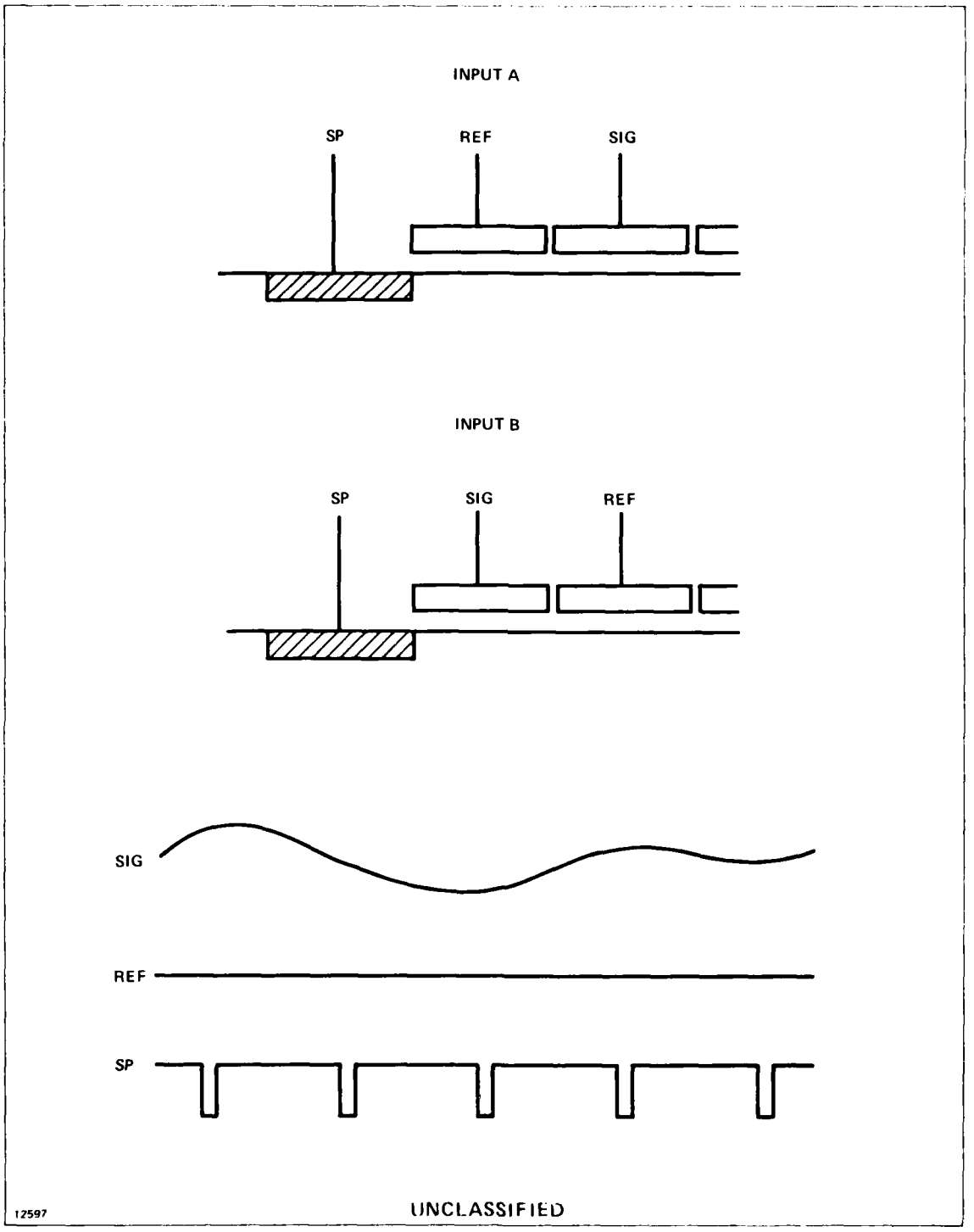


Figure 4-1 - Partial Schematic Diagram of the FG CCD Test Chip



The two charge equilibration type input techniques. Input A uses a higher value of dc reference (REF) that input B. The optimum dc bias in the signal (SIG) may also differ for the two inputs.

Figure 4-2 - Conversion of Input Voltage to CCD Charge

The two gated diode type inputs are shown in Figure 4-3. Input D should obey Equation (15) with V_{IG1} replaced by the value of IG1 voltage that would produce a channel potential equal to the reference voltage applied to the CCD-S. Input C obeys an equation of the form given in Equation (16).

$$\frac{dQ}{dV_{SIG}} = C_{oxide} + C_{DEPL}(V) \tag{16}$$

The capacitance that controls the ratio of incremental charge to incremental signal voltage includes the depletion capacitance C_{DEPL} under IG2. Since this capacitance depends on the signal voltage, a nonlinear relationship between charge and voltage is expected.

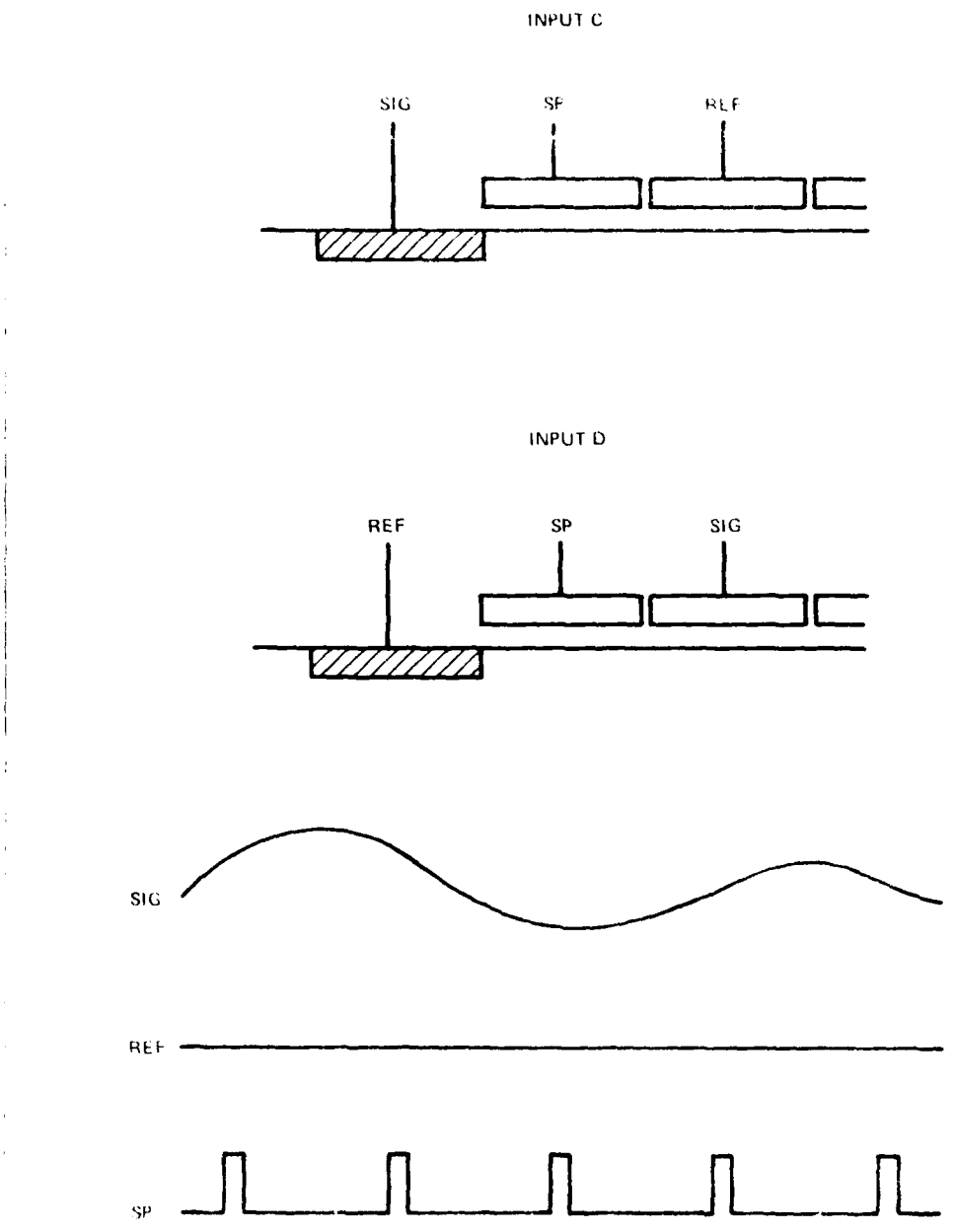
4.2 Test Fixture

The experiments reported on here were performed on a complete undiced wafer using a wafer probe station with a probe card. Poor matching conditions and high capacitance between probes limits the frequency at which measurements can be made. Laboratory pulse generators with 50 ohm back-matched outputs provided the clocking waveforms. Digitally-set power supplies with bypass capacitors on the probe card connector furnished low-noise dc levels.

The major speed limitation is determined by the drive capability of the output source-followers. The load capacitance of the scope probe and probe card was estimated to be about 20 picofarad (pF). With the source-follower load current set to 20 μA, the downward slewing rate is only 1 V per microsecond (μsec). The on-chip load in the correlator will be at least 20 times smaller.

4.3 Absolute Calibration

Measurement of the outputs from the FG taps gives no information about the absolute size of the charge packets in the CCD. To provide such information, the CCD was set up with conventional four-phase overlapping clocks operating at 0.1 megahertz (MHz). The control phase ϕ_c was held at a high dc bias so that the phase 3 gates were never floating. By measuring the average current flowing from the CCD-D at the known



UNCLASSIFIED

The two gated diode type input techniques. Reference levels, signal dc levels, and signal amplitudes will vary for the two inputs.

Figure 4-3 - Two Gated Diode Type Inputs

clock frequency, we could calculate the size of the charge packets. Data obtained using the potential equilibration input technique are shown in **Figure 4-4.** The slope of the curves gives a value of 1.1 pF for the oxide capacitance under IG2. The value actually varies by two to three percent depending on the bias on IG1.

As found from the results described in Subsection 4.5, the peak input swing on IG2 for linearity within one percent is about 3 V. This corresponds to a maximum signal charge packet of 3.3 picocoulombs (pC) or 20 million electrons. Shot noise for such a charge packet would be about 4500 electrons, 73 dB below the signal. The KTC noise on the input capacitor would be about 400 electrons, 94 dB below the signal.

4.4 Clock and Output Waveforms

Clock and output waveform timing for four-phase operation is shown in **Figure 4-5.** The polarity of SP depends on the input technique in use. Two versions of the actual output are shown in **Figure 4-6.** In both cases, $\phi 1$, $\phi 2$ and $\phi 4$ went from 2 V to 10 V. For **Figure 4-6**, $\phi 3$ went from 2 V to 12 V and ϕc from 6 V to 13 V. The source-follower biases were V_{SS} = 4.5 V, V_{GG} = 7.0 V and V_{DD} = 10 V and the drain current was 20 μA per source-follower. The bottom line in the photo is +4 V. *In* **Figure 4-6,** $\phi 3$, ϕc, V_{SS} and V_{DD} were adjusted to give the maximum possible signal swing of just under 6 V. The high level of $\phi 3$ was increased to 14.5 V and ϕc went from 7.5 V to 15 V. The source-follower load current was reduced to emphasize the slewing rate limit on negative-going output transitions. An 8.5 V difference between V_{DD} and V_{SS} was required for the 6 V signal swing; a difference of 5.5 to 6 V was adequate for a 4 V signal swing.

The various parts of the output waveform are explained herein. From time 1 to 4, the output gates are not floating but rather are driven by $\phi 3$. When $\phi 3$ is low during the time interval from 1 to 3, the output is saturated at V_{SS}. During the time interval from 4 to 5, the gate is floating but no charge has entered the gate region since $\phi 2$ is still low. The slight negative step at time 4 is presumably due to capacitive feedthrough of the negative ϕc transition. When $\phi 2$ goes high at time 5, capacitive coupling due to clock electrode overlap drives the FG more positive and allows the signal charge to spread under the $\phi 1$, $\phi 2$ and $\phi 3$ (FG) gates. At time 6, $\phi 1$ goes low, forcing the signal charge into the $\phi 2$ $\phi 3$ region. Finally at time 7, when $\phi 2$ returns low, all of the signal charge is forced under the FG $\phi 3$ and the full signal appears on the output. At time 0, phases 4 and 1 turn on, again allowing the signal charge to spread under three gates ($\phi 3$, $\phi 4$, $\phi 1$).

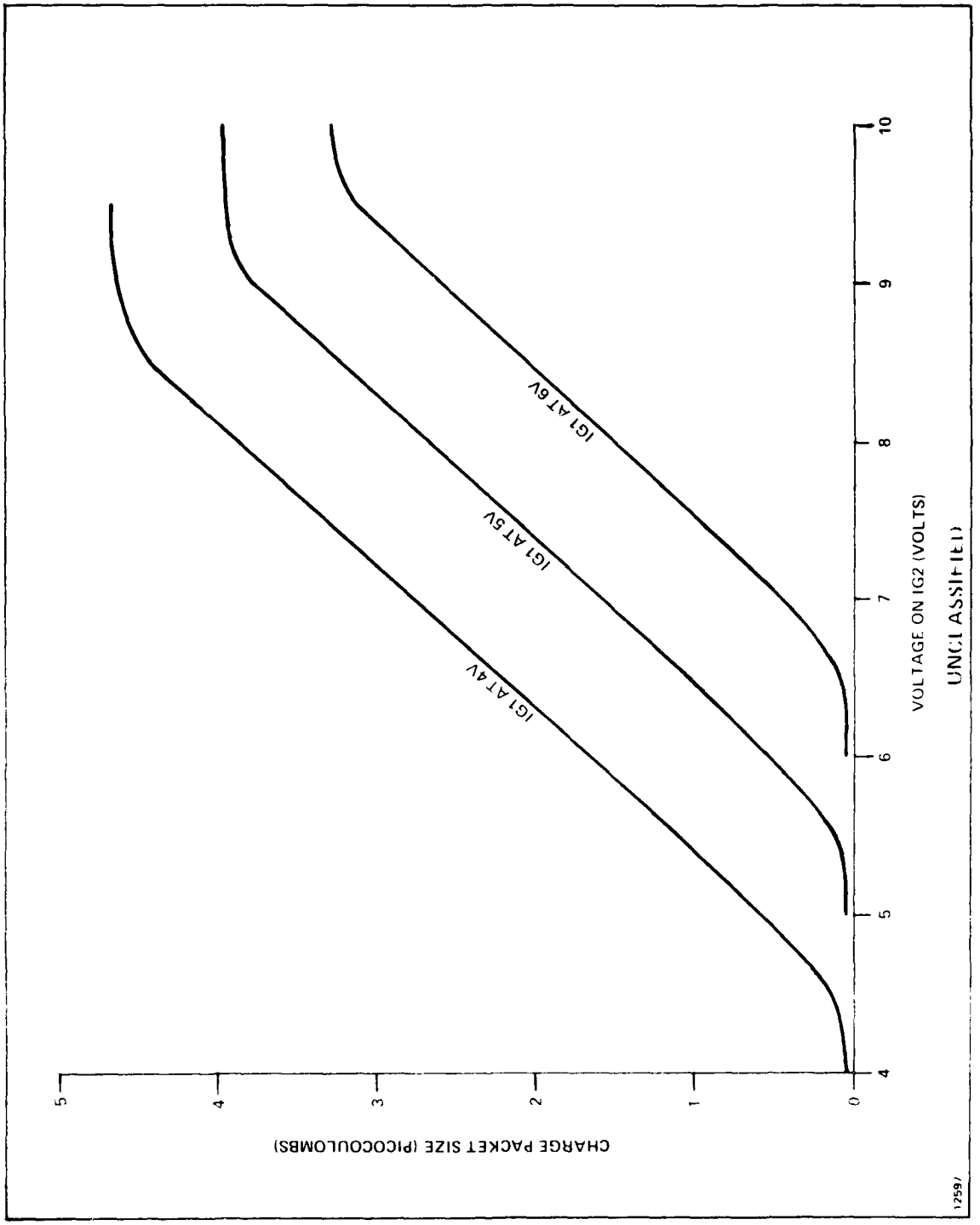


Figure 4-4 - Charge Packet Size for Potential Equilibration Input

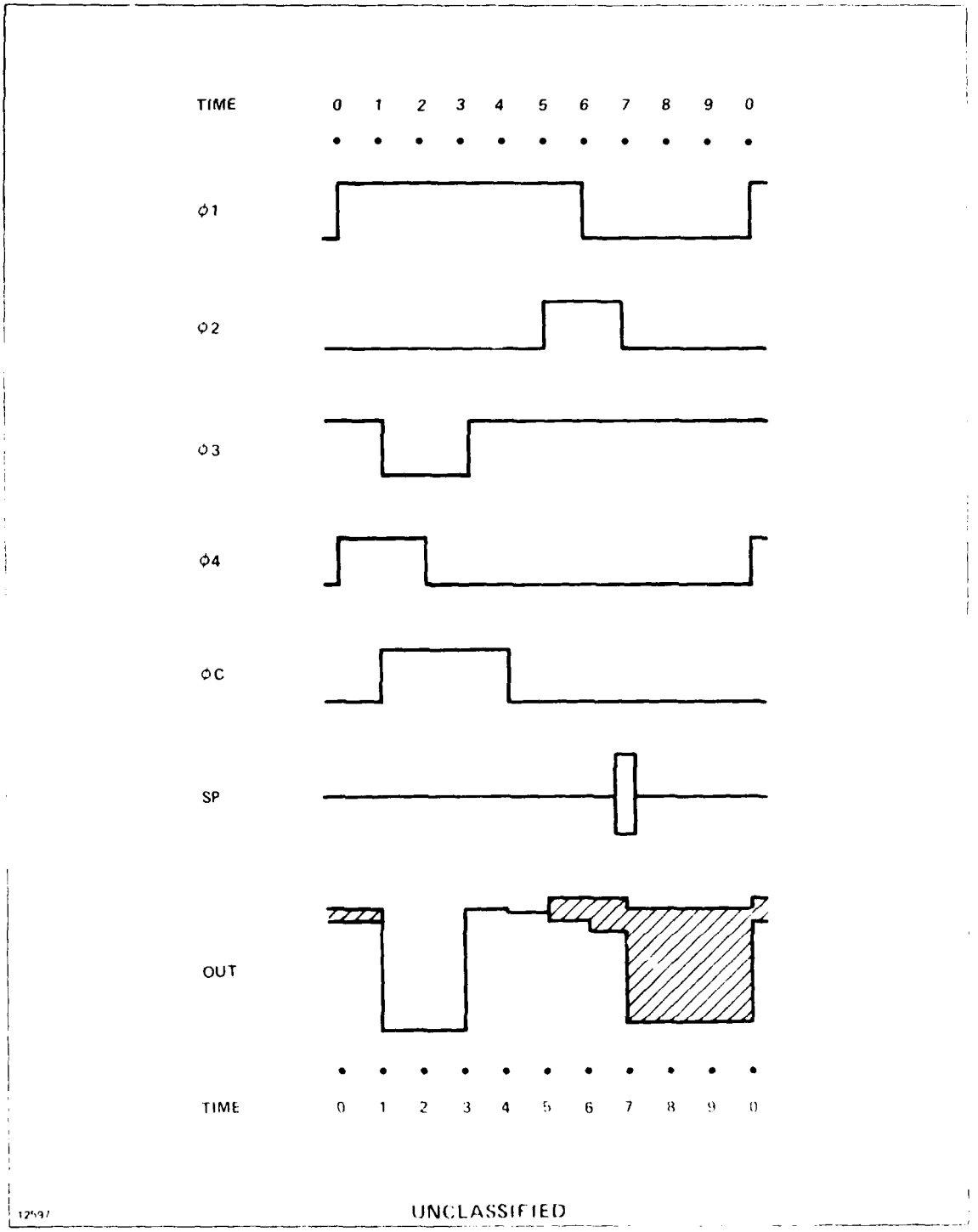
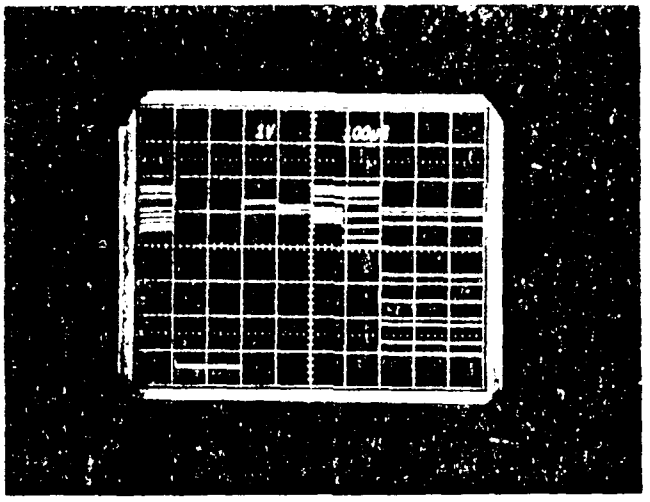
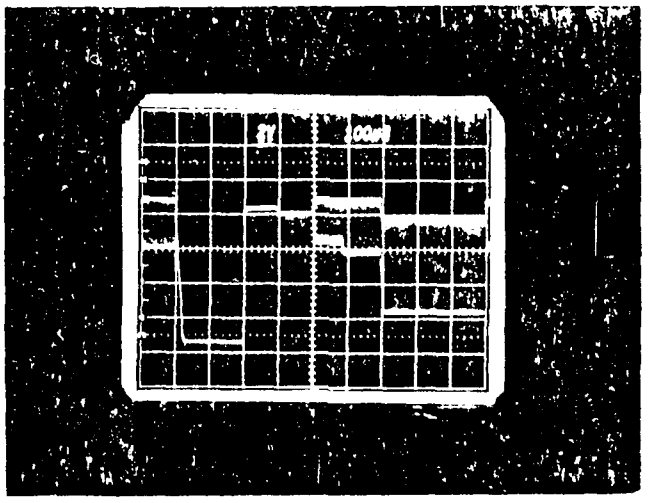


Figure 4-5 - Diagram Showing Clock and Output Timing





4.4 Linearity

For studies of the linearity and noise levels, the time unit was reduced from 100 μsec to 0.5 μsec for the interval from 0 to 7 in **Figure 4-5.** The overall clock period was reduced only 20 times to 50 μsec (f_c = 20 kilohertz (kHz)). In this way, the interval during which a valid output occurs was increased from 30 percent to 95 percent of the clock cycle. The seven percent of the time that contains an invalid signal is not visible on an oscilloscope trace.

Figure 4-7 shows the input and output waveforms for a slow, linear, triangle wave input signal. The output is displayed at 1 V per division and is inverted; the scale factor and dc level of the input signal were adjusted to bring the traces into close proximity for sensitive visual comparison. One can just barely determine that the traces track within one percent over an output signal swing of 4 V.

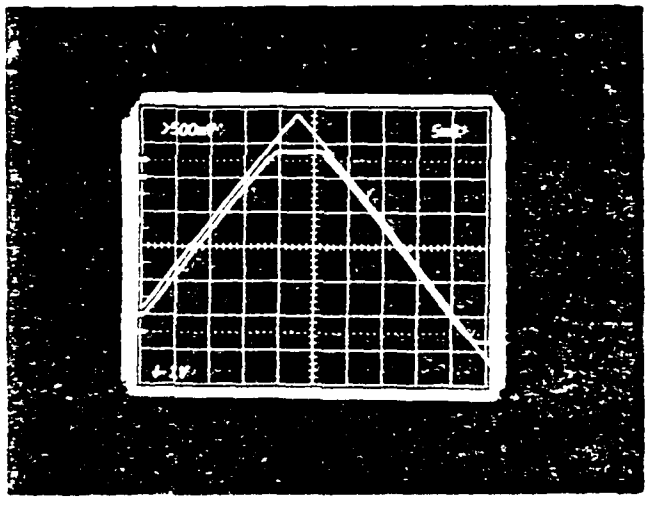
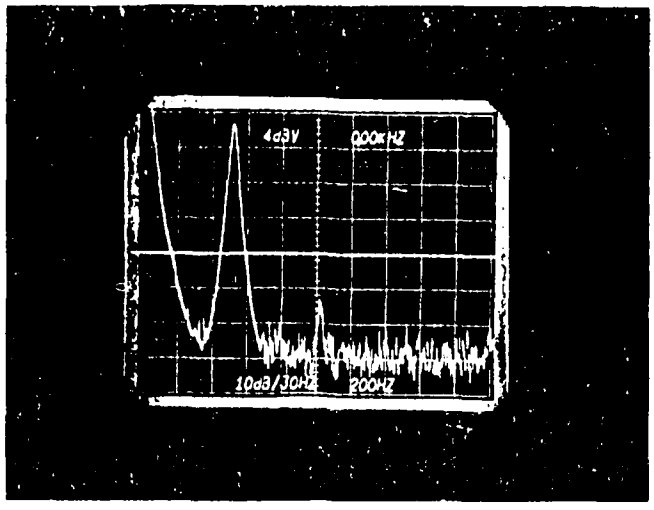


Figure 4-7. Comparison of input and output for a linear triangle wave

A vector up [illegible] spectrum analyzer with [illegible] Figure 4-8 [illegible] operating with input [illegible] Figure 4-[illegible]



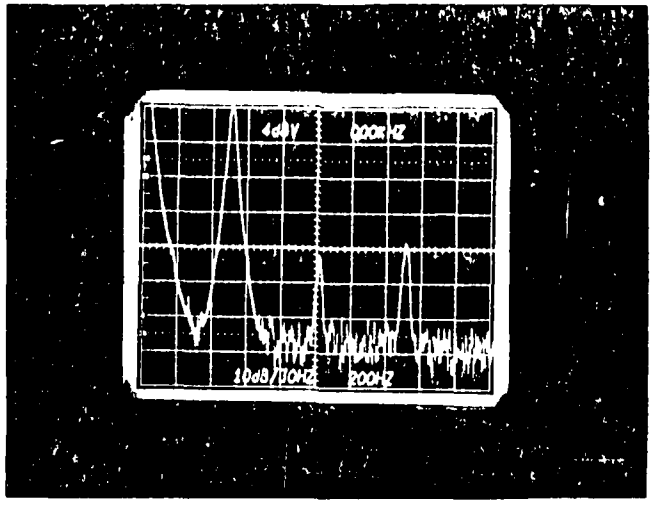


Figure 4-8 - Spectral Analysis Using Input Technique A

content of the 3 V peak-to-peak input signal (5 V to 8 V absolute) applied to IG2. The third harmonic is 50 dB down. The photo on the bottom shows the 4.5 V peak-to-peak output. The critical third harmonic is at -39 dB to -40 dB.

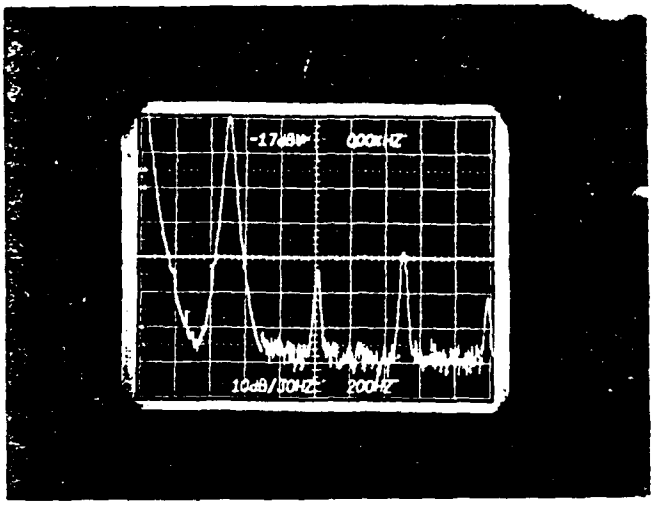
The 40 dB level is the minimum sensitivity of the experiment as performed here. Reducing the amplitude of the input signal did not dramatically decrease the harmonic distortion relative to the signal peak as would be expected ordinarily. This is due to the fact that the signal is valid over only 93 percent of the output time interval (actually a little less because of the time required for the output to slew to its final value). Of the seven percent of the time when there is an invalid output, dc levels occur over four percent and spurious signal-related output over three percent. A back-of-the-envelope estimate of the third harmonic content introduced gives a value in the range -40 dB to -50 dB, consistent with what is observed experimentally. The experiment could be improved by using an external sample-and-hold circuit, though the accuracy is quite sufficient for the present purposes. If we want to extend the measurements to higher clock frequencies, the sample-and-hold will have to be used.

The harmonic response of input type B is shown in **Figure 4-9.** Gate IG2 was held at a bias of 7.3 V while the signal on IG2 ranged from 3.3 V to 6.2 V (2.9 V peak-to-peak). The output signal ranged from 5.7 V to 10.3 V (4.6 V peak-to-peak). Again the third harmonic is 39 to 40 dB down.

Signals using input type C are shown in **Figure 4-10.** The left photo shows the input and output waveforms, both at 2 V per division. The input on CCD-S goes from 3.35 V to 6.25 V (2.9 V peak-to-peak) and the output swing is from 5.6 V to 10.6 V (5.0 V peak-to-peak). The 250 μsec (5 x 50 μsec) delay from input to output due to five stages of CCD delay can be seen. The photo on the right shows the third harmonic at about -38 dB for this very large output signal amplitude.

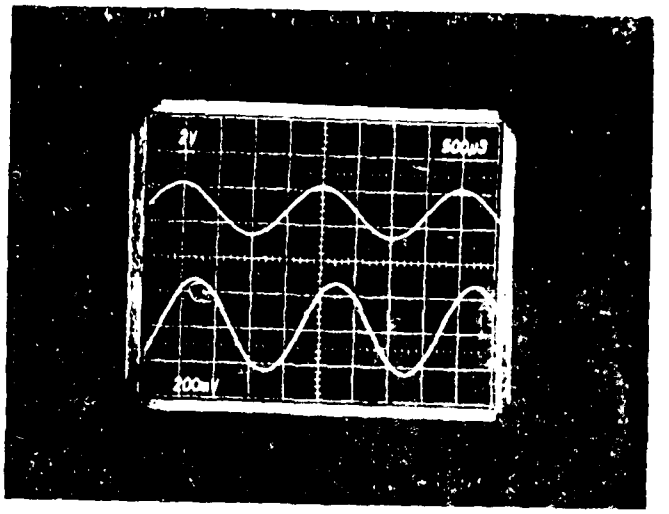
Figure 4-11 shows the spectral response for input type D. The CCD source was biased to 3.1 V dc, the input signal on IG2 swung from 3.8 V to 7.1 V (3.3 V peak-to-peak) and the output range was 5.6 V to 10.7 V (5.1 V peak-to-peak). Again the third harmonic is 38 dB down.

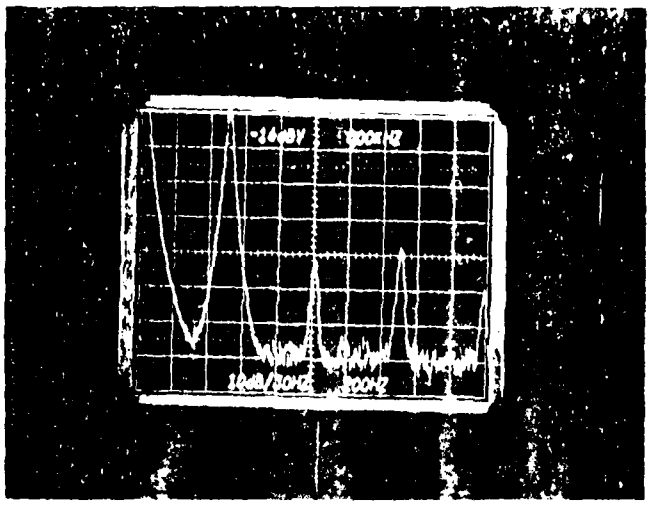
The general conclusion from these results is that any of the four input techniques can be used to produce adequately linear input voltage to output voltage transfer curves for output swings up to about 4 V peak-to-peak.



The actual signal level is 20 dB larger than indicated because of a 10X probe that was in use.

Figure 4-9 - Spectral Response/Input Type B


2V
500uS
200mV


-14dBV
10dB/DIV
100Hz

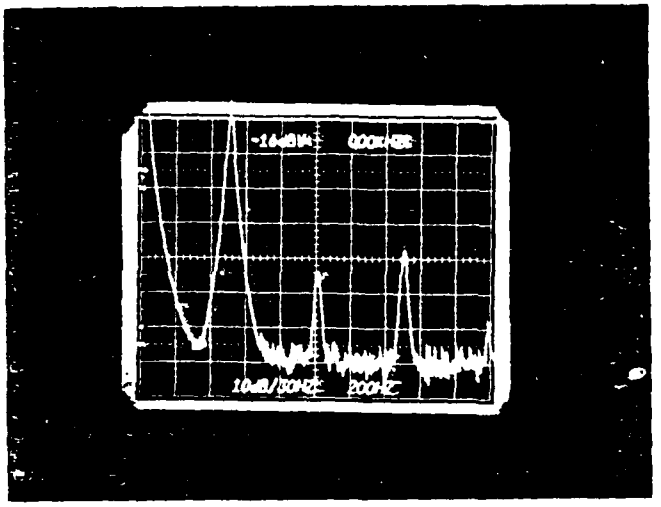
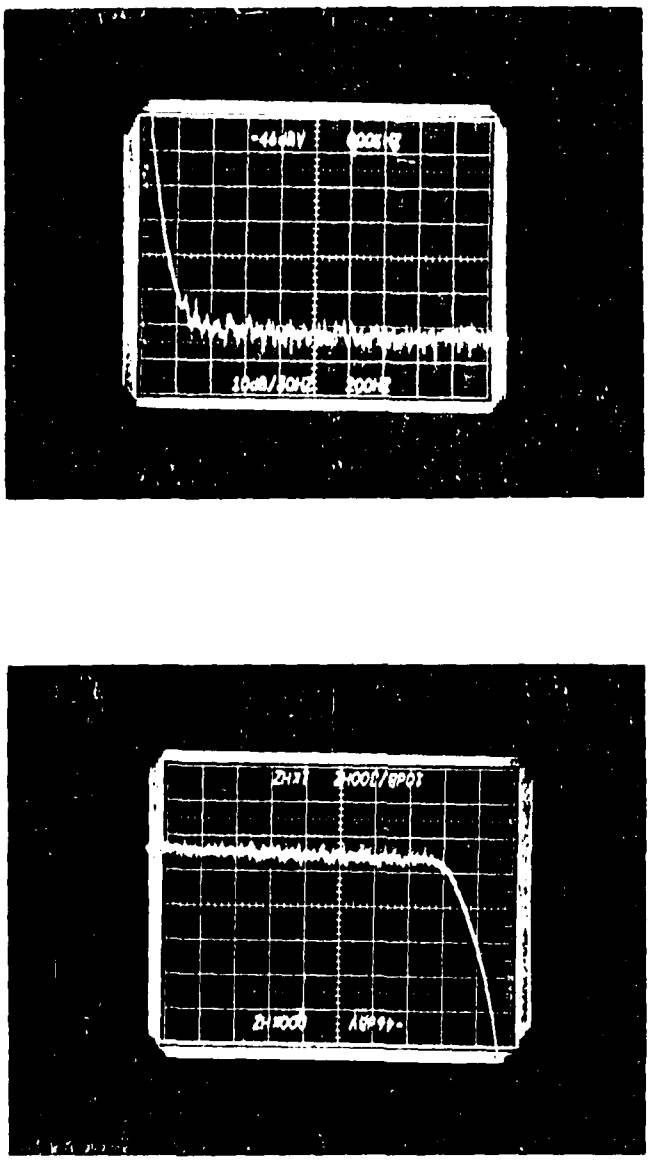


Figure 4-11 - Spectral Response for Input Type D

4.6 Noise

The noise was measured for the two general types of input techniques. Figure 4-12 shows the noise spectrum out to the Nyquist frequency of 10 kHz in two bands for input type D. Integration of the noise power over the Nyquist band yields a signal-to-noise ratio (including the 2.5 dB correction factor for the averaging characteristics of the spectrum analyzer) of 65 dB. With the probe tip grounded, the noise level was 7 dB lower than that shown in Figure 4-12. Also, when the bias IG2 was reduced to 1 V so that the input was cut off, the observed noise dropped to the analyzer noise floor level.

When a times-one probe was used to achieve greater sensitivity, the signal-to-noise ratios were found to be approximately 79 dB with the input cut off, 65 dB with IG2 at 4 V (small signal packet) and 68 dB with IG2 at 7 V (large signal packet). The dc biases on CCD-S and IG2 had noise levels at least 5 dB below the noise curve with the input cut off. The gated diode input operation was clearly responsible for the noise. The sampling pulse for the above experiments was 0.5 μsec long with 0.1 μsec rise and fall times. When the cutoff transition was lengthened to 2 μsec over the 4.5 V transition, the following improved signal-to-noise ratios were obtained: 76 dB with IG2 at 4 V, 73 dB with IG2 at 5 V and 70 dB with IG2 at 7 V. Further lengthening of the SP transition had little if any effect.



Noise spectrum for gated diode input with nearly full charge packets.

Figure 4-12 - Noise Spectrum for Gated Diode Input

Figure 4-13 shows the noise spectrum using potential equilibration input type A with a small signal present. In the upper left photo, the signal has an amplitude of 2 V peak-to-peak. In the upper right photo, the signal amplitude has been reduced 20 dB and the analyzer sensitivity increased by 20 dB. A nonrandom noise peak is clearly visible at about 2.5 kHz. It was caused by transients riding on the dc power supply lines. The signal amplitude and analyzer sensitivity were changed by another 20 dB to get the lower left photo. Finally, the lower right photo shows the full Nyquist band (the signal frequency was doubled also). Integration of the noise power over the 10 kHz Nyquist band, but excluding the coherent noise, gave a signal-to-noise ratio of 81 dB.

We do not fully understand why the gated diode input is so noisy. Conventional thinking is that partitioning of the charge stored in the channel under IG1 contributes additional noise. This is undoubtedly true. However, that noise contribution could not exceed the shot noise for a full charge packet, which we calculated to be -73 dB in Subsection 4.3. Another source of noise relates to the input sampling bandwidth. The gated diode input provides a very narrow aperture that is capable of sampling a very high bandwidth signal. Consequently it is sensitive to the noise over a bandwidth beyond the Nyquist limit. It is the classic problem of providing more input bandwidth than the remainder of the device can use; the result is degraded signal-to-noise ratio. With a sampling pulse fall time of 0.1 μsec, one can expect noise on the input control structures over a bandwidth of 10 MHz to contribute to charge fluctuations in the packet. The 1000:1 ratio (30 dB) of noise bandwidth to Nyquist frequency can result in significant noise contributions from signals whose spectral power density is very low.

The potential equilibration input technique, on the other hand, does not provide a precision sampling aperture. Input A tends to sample the minimum signal value and input B the maximum signal value in the interval between the end of the sampling pulse and when the charge enters the CCD shift register. As the equilibration progresses, the resistance of the channel under IG1 increases, increasing the RC time constant of the input. This limits the input bandwidth automatically.

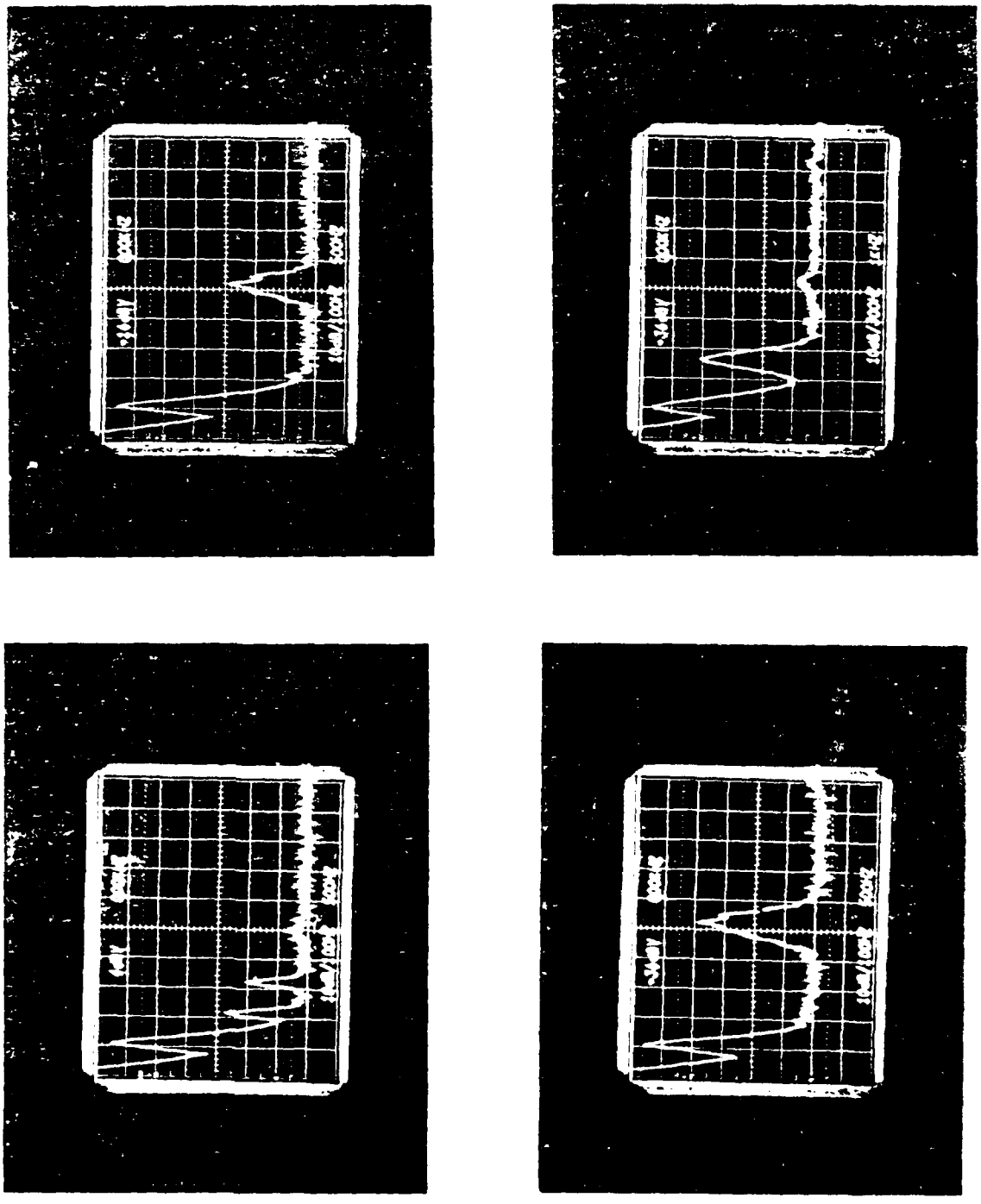
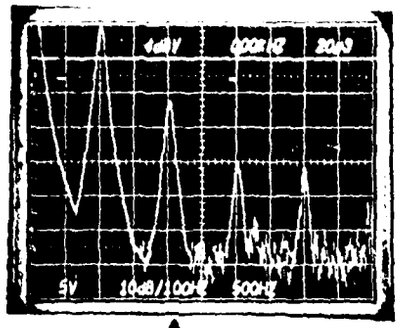
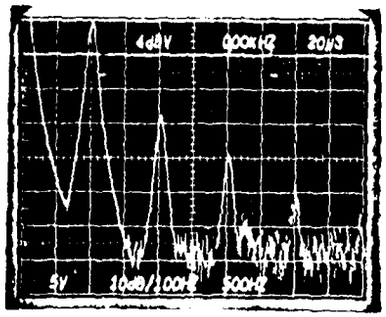


Figure 4-13 - Noise Spectra Using Potential Equilibration Input Type A

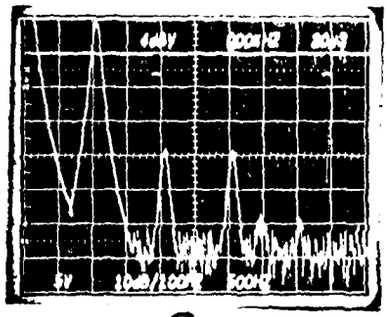
While the slow sampling characteristic of the potential equilibration input improves its noise level, it can also result in inaccuracies, as shown by the photos in **Figure 4-14.** The CCD was operating at a clock frequency of 10 kHz with an input signal at 1 kHz, 20 percent of the Nyquist limit. The upper trace in the photos shows the position of the sampling pulse relative to the $\phi 1$ ON transition. In the left photo, 80 μsec are allowed for equilibration, during which time the input signal can change by as much as 25 percent of its peak-to-peak swing. The second harmonic is only 22 dB down. In the middle photo, the equilibration time has been reduced to 50 μsec, reducing the maximum possible signal change to 15 percent. The second harmonic has dropped 5 dB. In the final photo, only 20 μsec is allowed for equilibration and the signal cannot change by more than six percent during that time. The second harmonic is now at -38 dB.



A



B



C

Figure 4-14 - Sampling Error for Long Equilibration Times with Potential Equilibration Inputs

5. MULTIPLIERS

The analog multiplier cell is the unique structure that makes an analog-analog correlator/convolver chip possible. This chapter reports the results of experiments performed using the multiplier arrays on the test chip. The theoretical advantages shown in the computer simulations were all borne out in the experiments and the multiplier is capable of meeting the 99 percent accuracy requirement of the contract.

5.1 General

The four-transistor multiplier cell can be drawn schematically as a bridge as shown in **Figure 5-1**. Three types of test patterns consisting of this multiplier cell were included on the test chip. One is a single stage multiplier with very large transistors (W = 2 mil, L = 2 mil). The purpose of this structure was to verify the basic theoretical advantages claimed for the four-transistor multiplier compared to the two-transistor multipliers used in previous attempts at making analog-analog correlators and to show the performance of such a multiplier when manufactured with relatively small geometrical errors.

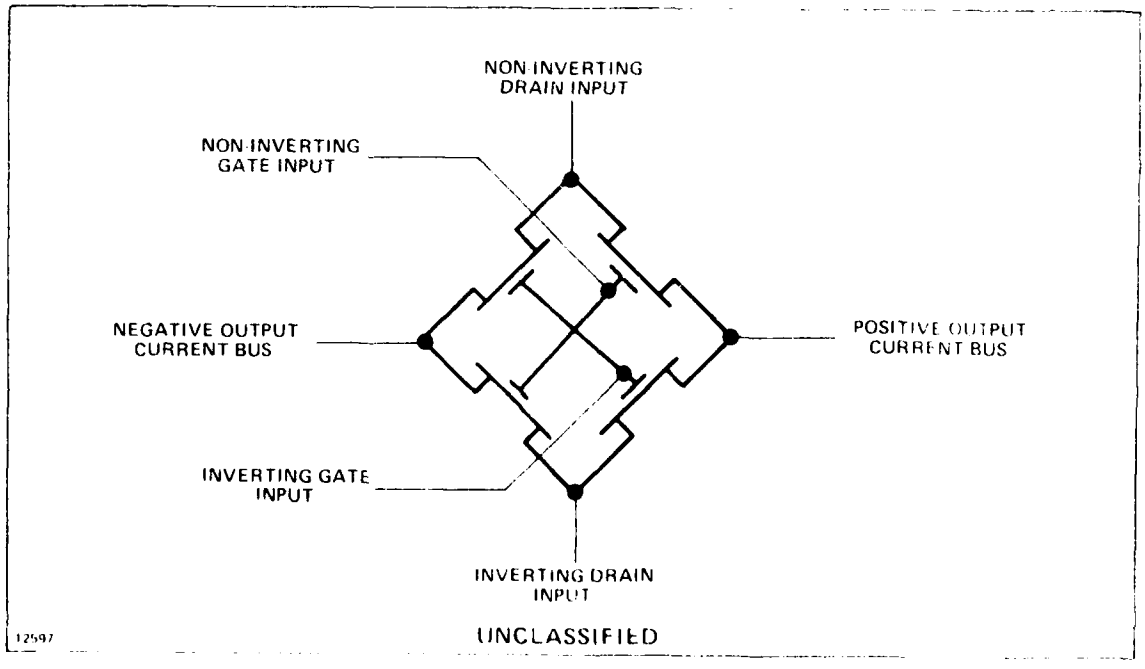


Figure 5-1 - Schematic of the Four-Transistor Bridge Multiplier Cell

The other two patterns used the fine geometry that would be used in a complete correlator and were designed to give information about inter- and intra-cell variations. One of these test patterns consists of an array of six multiplier cells as they would appear in the actual correlator, that is with common output and individual inputs. The other pattern contains an array of ten multiplier cells with common inputs and separate outputs.

The multiplier cells are tested by applying two pairs of sinusoidal input signals. Each pair has a common dc component and opposite phase ac components. The pair applied to the gate inputs is at one frequency, f_G, while the pair applied to the drain inputs is at a different frequency, f_D. The two output current buses are held at a common dc bias and the differential current is detected and displayed on a spectrum analyzer. The desired product output appears as two equal-strength sidebands at the sum and difference frequencies $|f_G + f_D|$ and $|f_G - F_D|$.

Spurious components at frequencies given by $|mf_G \pm nf_D|$, with integers m and n both not equal to one, will be generated both by the distortions inherent in the ideal field-effect transistor and by deviations from ideal behavior due to such factors as parameter variations and contact and interconnect impedances.

The performance of the four-transistor multiplier cell can be compared directly with that of the two-transistor cell simply by disconnecting one of the drain input signals. With that node floating, no current flows in that half of the bridge (the output buses are always at the same potential). Either half of the bridge can thus serve as a two-transistor multiplier. The gates can continue to be driven differentially or one can be held at a dc level as would be the case when single-channel (nondifferential) CCDs are used.

5.1.1 Results for Large-Geometry Multiplier

Table 5-1 lists the results of a test with one of the large-geometry multipliers on wafer 12, a wafer from the second phase of fabrication runs. With the exception of the entries for the desired product terms at the bottom of the table, which are expressed as decibel volts (dBV), all levels are expressed in dB relative to the product terms for the particular mode of operation. The relative noise level is the spectrum analyzer noise floor at the bandwidth selected for the measurement; it is not an indication of the

TABLE 5-1

LARGE GEOMETRY MULTIPLIER CHARACTERISTICS

Frequency kHz	Term	Relative Amplitudes (dB) Two-FET Cell with Single-ended Input	Two-FET Cell with Differential Inputs	Four-FET Cell with Dual Differential Inputs
0.75	f_D	-10 dB*	-35 dB*	-41 dB*
1.50	$2f_D$	-22	-41	-52
2.25	$3f_D$	-25	-45	-54
2.75	f_G-3f_D			
3.00	$4f_D$	-30		-41
3.50	f_G-2f_D	-12	-12	-42
5.00	f_G	- 5	- 6	-37
6.50	f_G+2f_D	-12	-12	-42
7.25	f_G+3f_D			-41
7.75	$2f_G-3f_D$	-30		
8.50	$2f_G-2f_D$	-29		
9.25	$2f_G-f_D$	-15	-37	-49
10.00	$2f_G$	-21	-41	
Noise floor		-44	-50	-56
Product output level		-30 dBV	-24 dBV	-18 dBV

* Relative to product level

multiplier's dynamic range. Blank entries in the table indicate that the particular frequency component was not visible above the noise floor. The input signals in this test were each at -3 dBV (2 V peak-to-peak). The gate signals were at 5 kHz and drain signals were at 0.75 kHz.

The amplitude of MOS multiplier outputs should be proportional to the product of the input levels with a proportionality factor as shown in equation (17):

$$G = N\left(\frac{W}{L}\right) \mu RC \tag{17}$$

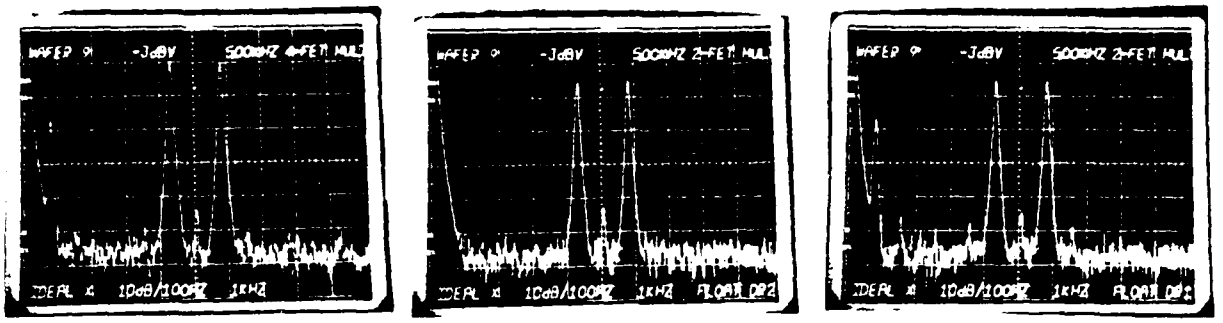
where W and L are the FET channel width and length; μ is the field effect mobility; R is the sensing resistance in the current detector (18 KΩ in our apparatus); C is the oxide capacitance per unit area. The coefficient N is the number of transistors actively contributing to the generation of the product term. This is four for the bridge multiplier and two for the two-FET multiplier with differential gate inputs. When there is only a single gate signal input, the second transistor acts as a dummy transistor to cancel nonproduct terms from the active transistor; consequently N = 1. The change in the value of N accounts for the 6 dB jumps in output level in Table 5-1. In some cases, the absolute levels of spurious components were nearly the same in the different multiplier configurations. The relative level drops significantly in the bridge multiplier because of the greater amplitude of the desired output term.

For N = 4, (W/L) = 1, μ = 500 cm^2/V sec, R = 18 kΩ and an oxide thickness of 1300 A, we find that G has the value unity. For two input signals of -3 dBV, the output should be -6 dBV, but since the power in each sideband is half, the spectrum analyzer would show -9 dBV.

The actual output was significantly lower. The discrepancy was traced to a problem with the contacts to the sources and drains. These contacts appeared to have in series a parallel combination of reversed diodes; that is, there was significant series impedance at low source-drain voltages, the precise conditions under which the transistors are operated in a multiplier. Consequently, each transistor acted as a very poor multiplier, as confirmed by the first column in the table. When four such poor multipliers were assembled into a bridge multiplier, however, the resulting circuit acted as a very good multiplier. This substantiated the theoretical observation that the bridge multiplier is a good multiplier by virtue of its symmetry alone, even when the four individual multiplying elements have high distortion.

Because the individual transistors on wafer 12 were poor, the range of dc bias conditions over which the multiplier would perform well was limited. However, 200 mV variations in gate and drain levels had virtually no effect.

Wafer 9 was not as good as wafer 12 from the standpoint of gate and junction breakdown, but its contacts were far superior. Correspondingly, the multiplier showed excellent response as illustrated by the series of photos in Figure 5-2.

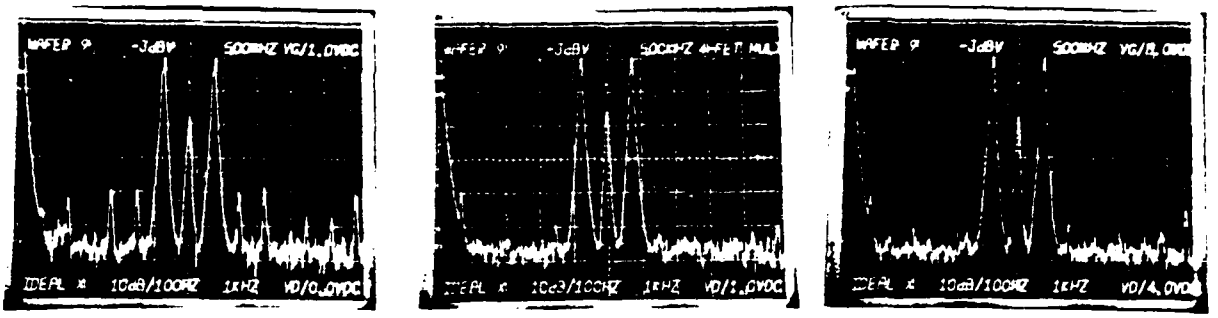


(a) (b) (c)

Figure 5-2 - Spectral Response of the Bridge Multiplier with Differential Gate Inputs

The product output level in Figure 5-2 (a) is -13 dBV, only 4 dB less than the calculated value. All spurious signals are down by at least 50 dB except for feedthrough of the drain signal at a relative level of -18 dB. The two-transistor configuration of Figure 5-2 (b) shows that excellent performance can be obtained with a two-FET multiplier under favorable conditions. Figure 5-2 (c) indicates that the large drain signal feedthrough is associated with one side of the bridge only and is due to a defect in one transistor.

Despite such defects, the results with wafer 9 showed spectacularly the ability of the bridge multiplier to perform well even with enormous bias variations. The series of photos in Figure 5-3 show the spectral response of the bridge multiplier over a range of bias conditions. In all cases, the substrate was at -4 V and the current detection buses were held at ground. The substrate bias could be varied over a very wide range with no effect. It should be noted that the gate and drain signal frequencies had been interchanged so that the drain signal leakage due to the defective transistor was at 4 kHz.



(a) (b) (c)

Figure 5-3 - Spectral Response of the Four-Transistor Multiplier
Over a Range of dc Levels for the Gate and Drain Signals

Figure 5-3 (a) was taken with the gate bias reduced to just above threshold (clipping of the negative signal excursions is occurring). Figure 5-3 (b) shows the result with a drain bias offset of 1 V (the gate bias was about 4 V and Figure 5-3 (c) shows the extreme case of a 4 V drain offset at an 8 V gate bias. Figure 5-4 shows how the two-transistor multiplier responded under the conditions of Figure 5-3 (b). The drain offset caused a spurious feedthrough of the gate signal that was 6 dB larger than the product output. Drain offsets of only tens of mV resulted in significant multiplier error.

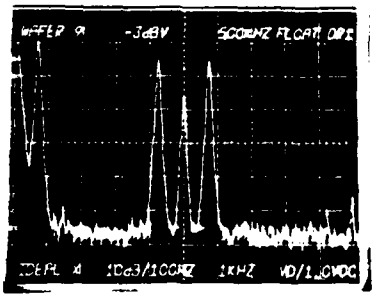


Figure 5-4 - Spectral Response of the Two-Transistor Multiplier
1 V Offset in the Drain Signals

6. MASK DESIGN

6.1 General

Figure 6-1 shows a block diagram of the chip organization of a correlator/convolver. The central portion of the chip contains an array of bridge multipliers with a pair of gate inputs and a pair of drain inputs. Figure 6-2 shows the mask layout detail of the multiplier cell used in the test pattern chip. The overall plan of the correlator places the multipliers in the center and the two tapped differential CCDs on each side of the row of multipliers. One of the differential CCDs drives the multiplier drain inputs and the other drives the multiplier gate inputs.

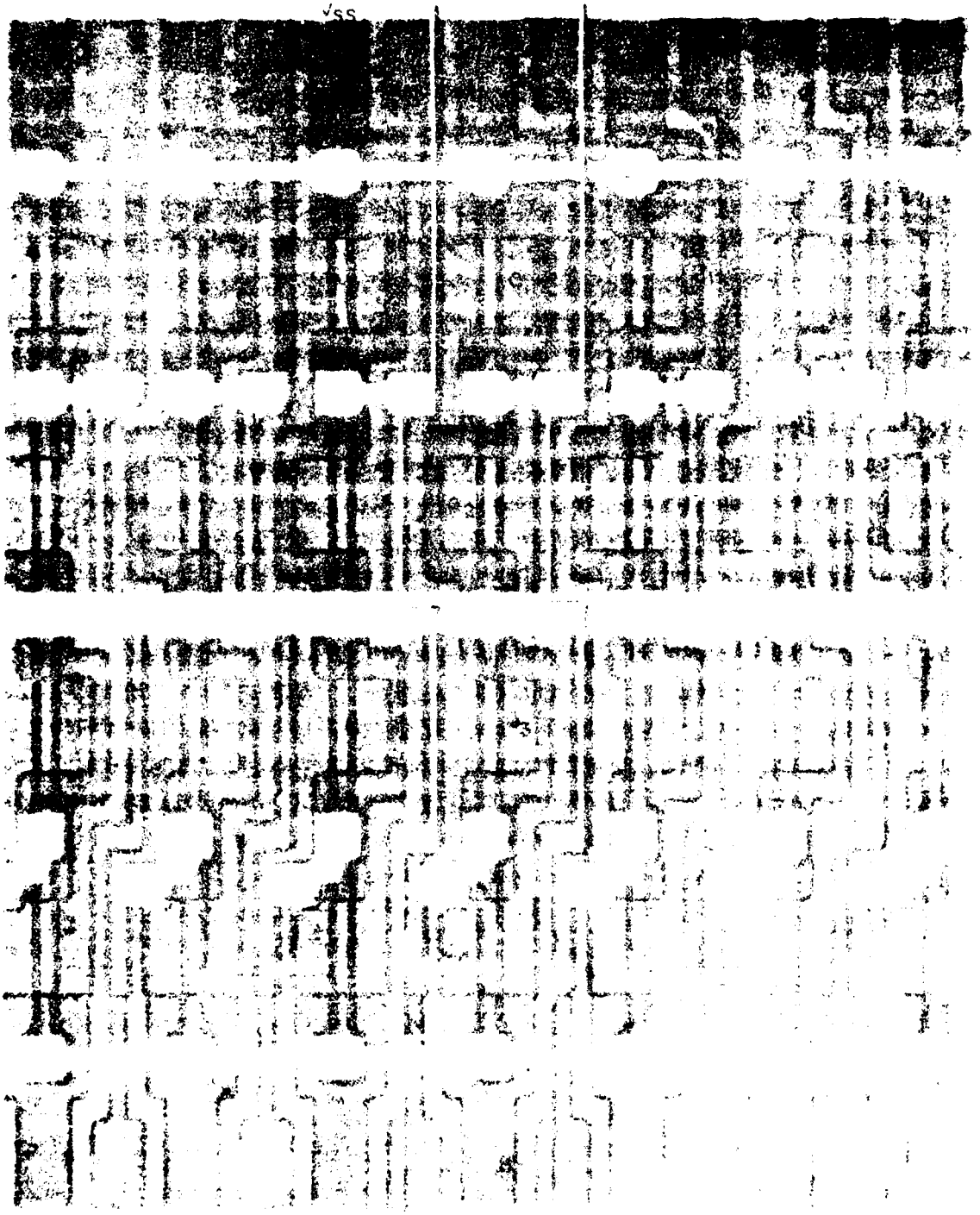
The CCD correlator/convolver was designed using depletion devices exclusively for simplicity. Major attention in both circuit design and mask design was given to minimizing the effects of parameter (threshold voltage and g_m) variations upon the accuracy of the correlator/convolver.

All transistors have gates formed from the first level of polysilicon so that process and operating temperature variations will not affect device tracking. Although the circuit configurations and mask design approach used can help greatly to reduce errors due to such systematic effects, random variations are more difficult to compensate for in this manner.

6.2 Multiplier

Figure 6-2 shows the multiplier mask design for the correlator/convolver. The four transistors in a given multiplier have been arranged with the same orientation and along a straight line. Mask alignment errors in either direction will, therefore, affect all transistors identically and will have no affect on multiplier accuracy. Furthermore, the circuit connections to the four transistors have been made in a way that compensates for constant gradients in transconductance and threshold voltage. Figure 6-4 shows schematically the circuit layout with the four transistors spaced at equal distances, d. The analysis for transconductance variations proceeds as follows.

Figure 6-1 - Chip Organization of Correlator/Convolver



If the center of the string is selected as the origin and the transistors are assumed to vary their transconductance linearly with distance, the currents in the devices are approximately (assuming identical threshold voltages):

$$I_1 = KA\,(-B)\,(1+3/2d\,\Delta)$$
$$I_2 = K\,(-A)\,(-B)\,(1+d\,\Delta/2)$$
$$I_3 = KAB\,(1-d\,\Delta/2)$$
$$I_4 = K(-A)\,B\,(1-3d\,\Delta/2)$$

where

K	=	Device transconductance
A and B	=	Input voltages
d	=	Distance between gates
Δ	=	Relative change of K with position

When these currents are summed to form the output $I_{OUT} = -I_1 + I_2 + I_3 - I_4$, all Δ terms cancel and the net current is $I \approx KAB\,(4)$.

6.3 Tapped Differential CCD

Figure 6-3 shows the mask layout of the differential CCD portion of the correlator/convolver as provided for the gate driving inputs to the multiplier. The drain driving differential CCDs are located on the opposite side of the row of multipliers and, except for the increased transconductance of the source-follower load devices, is the mirror image of Figure 6-3. The source-follower outputs from the outer FG taps must be passed undisturbed over both CCDs to the multipliers on the centerline of the chip. This is done by using aluminum interconnect over the phase 4 clock phase which, when four-phase clocking is used, remains static during the charge transfer to the FGs and the read-out time which follows. With two-phase clocking, both clocks are static during the read-out time.

The W of the CCD channels are not shown in Figure 6-3. They are relatively wide (15.5 mils) so that the capacitive loading of the interconnection to the source-followers will be relatively small. Since the source-follower outputs from the outer CCD channels must cross the input circuitry of the inner source-followers, it is impossible to have exactly symmetrical layouts for the outer and inner amplifiers. The parasitic capacitors involve six different oxides. The tracking of each contribution to the FG parasitic

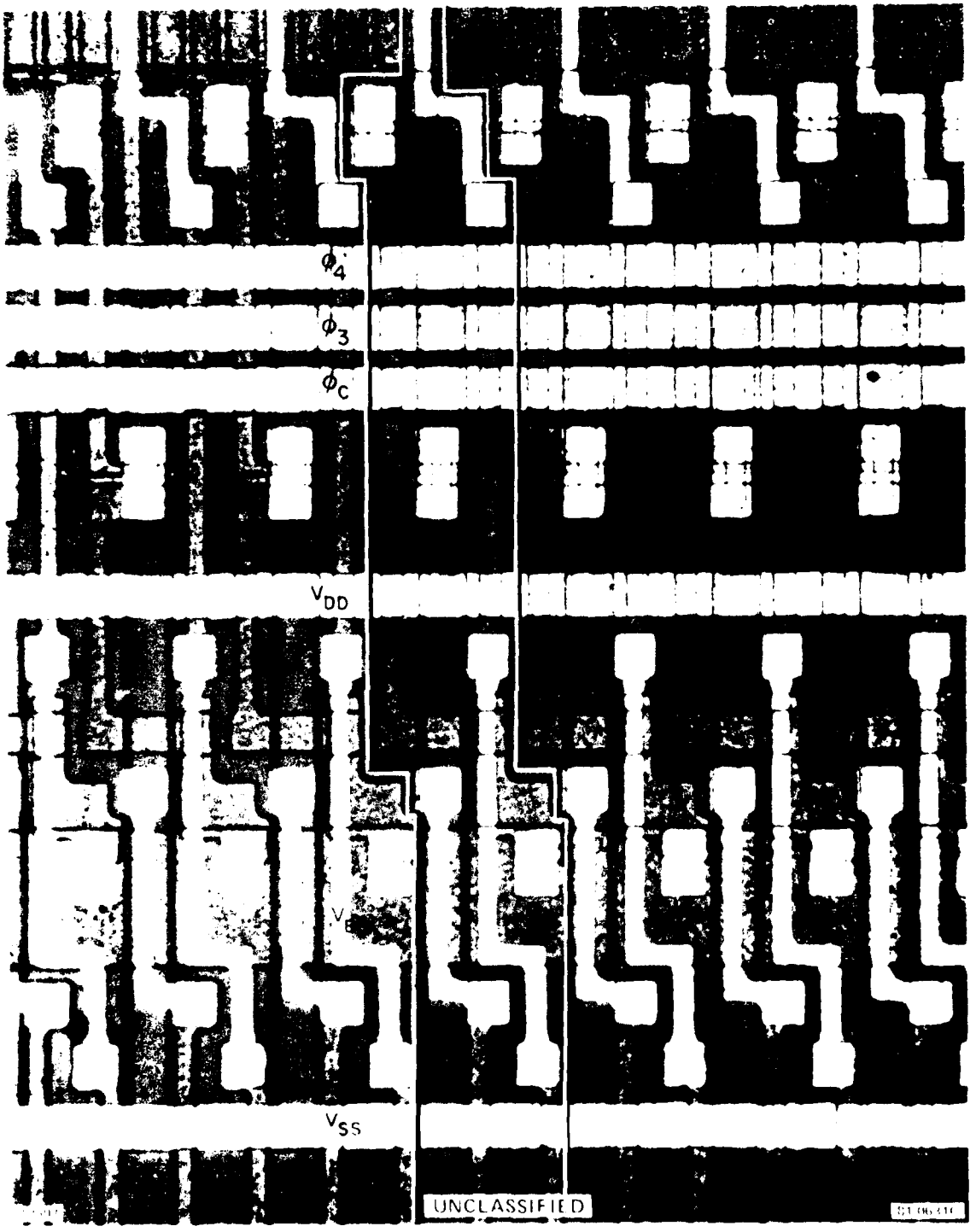


Figure 6-3 - Differential CCD/W S.F.-Buffered Floating Gate Taps

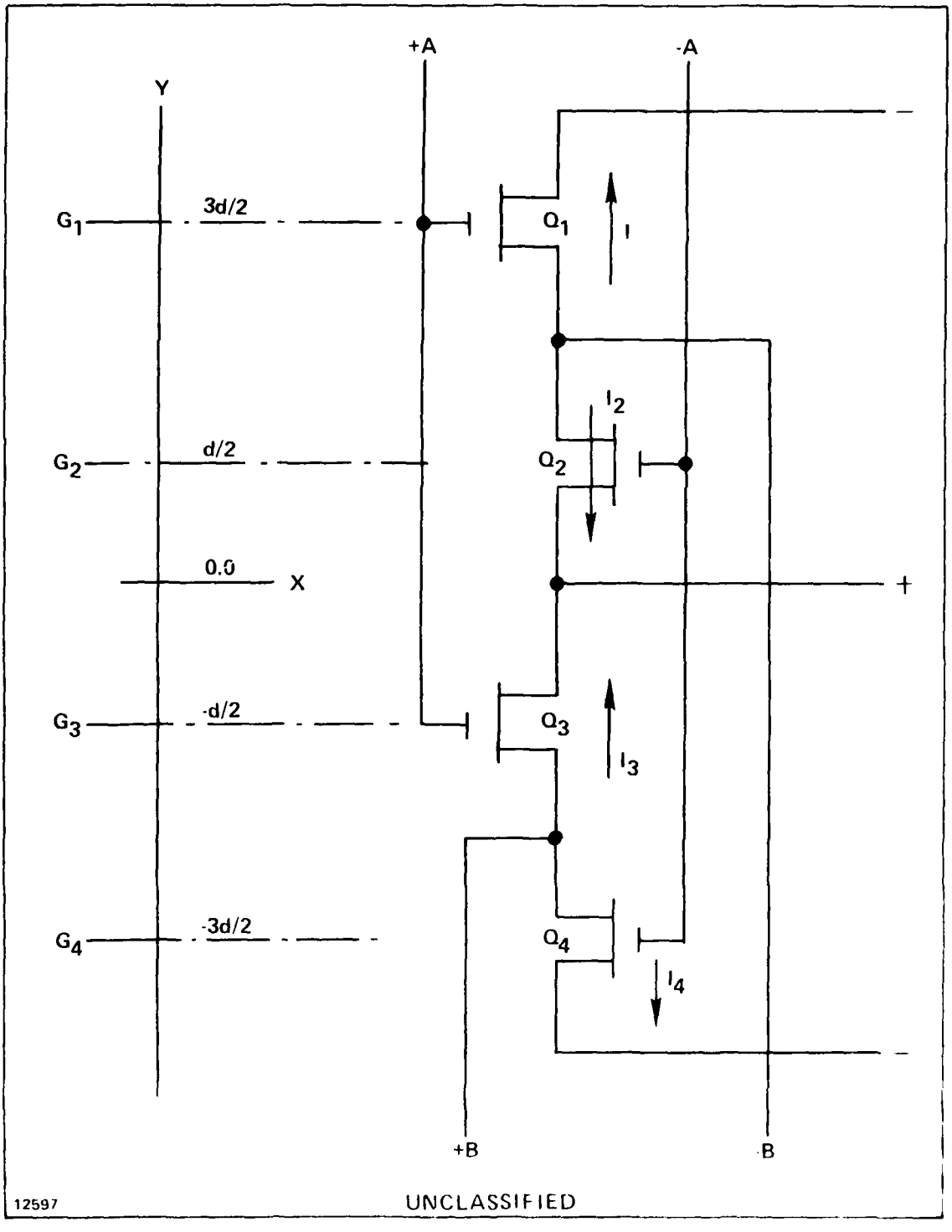


Figure 6-4 - Four Transistor Multiplier Schematic

capacitance had to be considered carefully. To achieve uniformity between the taps on different CCDs, the design must rely partially on making the unmatched parasitic capacitance a small part of the total FG capacitance.

Unfortunately, the mask design of the differential CCDs could not provide compensation for nonrandom offset voltage variations between the four source-follower outputs in the manner shown earlier for the four transistor multipliers. The use of independent biasing for the source-follower loads will permit the effects of such variations to be minimized by adjusting outside bias supply levels separately.

6.4 Test Mask Layout

The test pattern layout is largely made up of 68 mil square patterns. This was done to use the standard 28 pin probe card currently in use at the Raytheon Missile Systems and Research Divisions for CCD, MOSFET and MESFET process test patterns. The test mask has eight individual patterns in it, as itemized in Table 6-1. All eight patterns in the test mask are described in detail in the sections which follow along with the rationale for their design.

The placement and composition of the cells used in the test mask patterns were arrived at, keeping in mind the potential sources of parameter variations in finished correlator/convolver chips. The chief parameter variations to be considered included threshold and transconductance variations in the MOS transistors and the storage well and parasitic capacitance variations associated with the FG taps. In addition, the IR drop of the polysilicon interconnects had to be considered. The reason for the composition and placement of the cells in each test pattern will be considered in turn in the subsections following.

6.4.1 Pattern No. 1

This test pattern is the TC1 standard pattern used with the Raytheon poly/polv (CCD wafer fabrication process. it is described in sufficient detail in Table 6-1 and is located at one corner of the test mask plan shown in Figure 6-5. Since no attempt will be made to measure minute parameter variations between TC1 and the correlator/convolver test patterns, its location was noncritical. This pattern is 68 mils square and has 34 contact pads, 28 of which are located on the chip edges for automated process monitor testing.

TABLE 6-1

TEST MASK

Test Pattern No.	No. Pads	Description
1	34	TC1 Standard Raytheon Test Pattern for poly/poly surface/buried channel CCD. Includes patterns to evaluate capacitors, contact chains, G.B. to S/D breakdown, interconnection continuity over steps.
2	34	Sixteen stage tapped differential CCD with + and - tap outputs for stages 6, 7, 8 and 9 (drain driving version).
3	50	TC2 Standard Raytheon test pattern for poly/poly surface/BC CCD. Includes patterns to evaluate capacitors, contact chains, gated diodes, resistors, interconnection continuity over steps and transistors with implant and geometry variations.
4	34	Ten 4-transistor MOS multipliers with inputs in common and separate outputs on 1.2 mil centers.
5	34	Same as 4.
6	28	Six 4-transistor MOS multipliers with outputs in common and separate inputs on 1.2 mil centers.
7	44	Thirty-two stage correlator with independent bias and clock lines for all functions (except first CCD gates are paired for reference and signal CCD).
8	56	Six test transistors, each of 7 types on 1.2 mil centers.

<table>
<tr><td colspan="2">Test Pattern #6</td><td>Test Pattern #7</td></tr>
<tr><td>Test Pattern #4</td><td>Test Pattern #1</td><td>Test Pattern #5</td></tr>
<tr><td>Test Pattern #8</td><td>Test Pattern #3</td><td>Test Pattern #2</td></tr>
</table>

Figure 6-5 - CCD Correlator/Convolver Test Mask Plan

6.4.2 Pattern No. 2

[redacted]

6.4.3 Pattern No. 3

[redacted]

6.5.4 Pattern No. 4

This test pattern consists of ten 4-transistor multipliers [redacted] common inputs and isolated output nodes. It will enable the accuracy of each multiplier to be evaluated separately. Unfortunately, some polysilicon interconnect [redacted] changes had to be made to achieve separate outputs and this led to generation of test pattern No. 6.

This test pattern also includes an ideal 4-transistor multiplier with very large (2 mil x 2 mil) dimensions. Also included are contact chains of first poly, second poly and N+ with the 0.2 x 0.2 mil openings and 0.1 mil overlaps similar to those used in all the correlator/convolver cells. These have been included since the existing contact chains in the TC 1 and TC 2 test patterns were designed using more conservative mask layout rules.

6.4.5 Pattern No. 5

This test pattern is identical to Pattern No. 4 and is provided so that variations in device geometries due to the location in the optical field of the chip can be detected and evaluated.

6.4.6 Pattern No. 6

This test pattern consists of six multipliers with common outputs and separate inputs exactly as they would appear in a finished correlator/convolver to permit assessment of any variations in multiplier accuracy due to the rearrangement of interconnects in the other multiplier test patterns.

This test pattern is 68 mils square and has 28 pads on the edge of the chip of automated characterization testing.

6.4.7 Pattern No. 7

This test pattern consists of an entire 32 stage correlator with separate clock and power supply connections brought out for each portion of the device layout. It will allow an early assessment of problems that may occur due to interconnecting the correlator/convolver elements and permit a study of the interaction of power supply and clock waveform variations on correlator performance.

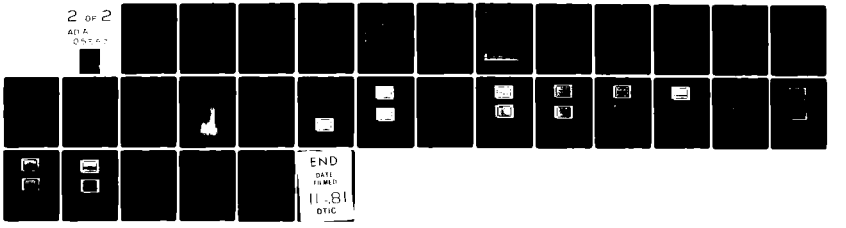
The pattern is 68 mils by 136 mils in size and has 44 pads located on its outside edges for characterization tests.

6.4.8 Pattern No. 8

This pattern is a test transistor array consisting of seven different transistor types located in rows of 6 on 1.2 mil centers. The devices in the array consist of the following types:

1) Four geometries of multiplier transistors so that the variations in multiplier transistor characteristics can be compared as a function of geometry. The following transistor geometries are included:

AD-A105 557 RAYTHEON CO BEDFORD MA F/G 9/5
DESIGN AND FABRICATE A CCD ANALOG MULTIPLIER,(U)
AUG 81 J P SAGE, D E GREETHAM F19628-77-C-0260
UNCLASSIFIED BR-12597 RADC-TR-81-155 NL



W (Mil)	L (Mil)	
0.2	0.8	(as used in multiplier currently)
0.2	1.6	
0.4	0.8	
0.4	1.6	

2) In addition, this test pattern includes clusters of six transistors on 1.2 mil centers identical to those used for the source-follower drivers, drain-driving source-follower loads and gate-driving loads in the FG output circuits of the differential CCDs.

This test pattern is 68 mils square and has 56 pads for automated characterization testing.

6.5 Process Design

6.5.1 General

The wafer fabrication of the correlator/convolver was originally expected to be performed using the existing standard Raytheon CCD process. When the cells for the correlator/convolver were designed, however, it was discovered that a considerable performance penalty would result (as well as large chip area) if the device were to be built using the existing layout rules (7.5 μm poly and aluminum line widths and spaces) compared to what could be achieved using a more advanced process.

As a result, the layout rules were revised to permit 5 μm poly and aluminum lines with 2.5 μm spacings. The revised rules were then incorporated into the design of the correlator/convolver test pattern.

Although resolution pattern data indicated that the new denser layout rules could be achieved with a conventional guardbanded thick oxide process using the new projection aligner, it was expected that superior results would be achieved using a coplanar process. The coplanar process would provide lower steps for the polysilicon and aluminum to cover and also improve the ability of photolithography to define them.

It was therefore decided to make some experimental correlator/convolver test patterns using the coplanar isolation technique as well as some using the conventional thick oxide guardbanded process.

The new coplanar process, which will be described in detail later, would use a relatively low concentration P-type implant which would come up right to the edge of the device areas and be adjacent to source, drain and channel areas. The existing thick oxide etch mask would be used to define nitride covered device islands, surrounded by etched back silicon and then a boron implant would be used to create a lightly doped guardband area everywhere but in the device regions. This would be followed by growth of the coplanar field oxide such that the field oxide would have a lightly doped P-layer under it for guardband purposes.

The following subsections will describe the characteristics of the original Raytheon CCD process and how it was modified for use in this program for both conventional guardbanded and coplanar wafer fabrication.

6.5.2 Process Development

The fabrication of the correlator/convolver test structures was based mainly on our standard CCD process which had yielded excellent results in the past in terms of device performance and die yield. In conjunction with an implanted BC, this process has enabled us to make 64 stage 60 MHz, two phase CCD structures with die yields of 40 - 50 percent. The special features of the process are:

1) **Three Levels of Conductors** - With the first and second consisting of 5000 A thick phosphorus-doped, oxidized polysilicon and the third one consisting of a composite of 2000 A of phosphorus doped polysilicon with approximately 5000 A of aluminum on top. This composite third conductor is formed by using a single photoresist masking step.
   The polysilicon portion of the third conductor layer protects shallow doped regions such as sources and drains against alloy formation with the aluminum and since it is chemically vapor deposited, it greatly improves step coverage.

2) **Self-Registered Polysilicon Gates with Source and Drain Regions Formed by Implanting Phosphorus Through Gate Oxide** - This technique is superior to implanting into source and drain regions with the gate oxide removed from them, because no oxide undercutting under the gate occurs and less damage is produced by the ion implant.

3) **Phosphorus Diffused Polysilicon** - This has a lower sheet resistance (typically 25 ohm/square for a 5000 A thick layer) than can be achieved with implanted phosphorus, even at high implant doses ($\geq 2 \times 10^{15}/cm^2$).

4) **Shallow Source and Drain Contact Regions** - These reduce space requirements and parasitic capacitances and are made possible by the use of the composite third conductor layer.

5) **Optional Diffused Guardband or Coplanar Oxide Isolation** - Either can be easily implemented in the processing without the need for additional masks.

6) **Gettering by Implanting BF_2 into the Back of the Wafer** - This implant also ensures a good electrical contact to the wafer.

High temperature processing was done in polysilicon furnace tubes periodically cleaned with HC 1 gas. The field oxide used in the coplanar process was formed in an environment produced by reacting hydrogen with oxygen. All other oxides were formed in an ultra dry oxygen atmosphere derived from a liquid oxygen supply. Supply lines were carefully leak checked and the gases were passed through submicron filters. Hydrogen chloride was added to the atmosphere for wet oxidation and trichlorethane (C33) to the atmosphere for dry oxidation to ensure the highest possible cleanliness of the oxides. Extensive use was made of a plasma etcher (barrel-type with aluminum cage) to etch the polysilicon and the silicon nitride layers and to remove photoresist after etching and residues after development.

Conventional contact printing was used for the photolithography with a registration accuracy close to 1.5 μm. The chemical processing was performed with electronic grade chemicals and with 18 MΩ water prepared by reverse osmosis and passed through a 0.2 μm filter. The resistivity of the effluent rinsing water was monitored and allowed to reach 16 MΩ before the wafers were taken from the rinsing bath. For this work, we used boron doped silicon wafers from two different vendors: Dow Corning (8-51 ohm-cm) and Monsanto (10-40 ohm-cm).

6.5.3 Mask Steps

The following masking steps were used:

Mask No. 1: Guardbands (not used in coplanar process)
Mask No. 2: Field oxide (defines guardband in coplanar process)
Mask No. 3: MOSFET gates and CCD $\phi 1$ and $\phi 3$
Mask No. 4: Interconnects and CCD $\phi 2$ and $\phi 4$
Mask No. 5: Via holes
Mask No. 6: Final interconnects

6.6 Results

6.6.1 General

The results which follow are based upon a number of wafer fabrication runs in three wafer fabrication phases.

The first phase was performed early in the program to evaluate the coplanar oxide isolation technique and to verify the design rules chosen for its implementation.

The second phase used the initial version of the correlator/convolver test pattern mask series. This cycle produced working multipliers, but mask and processing problems precluded quantitative evaluations of the remaining patterns.

The third processing phase incorporated corrected masks and process improvements. Working versions of all patterns have been seen including CCDs and full correlators. Specific data will be presented in the sections that follow.

Figures 6-6 through 6-8 are photomicrographs of the overall pattern, the 32 stage correlator and the bridge multiplier section of the 32 stage correlator taken from completed wafers.

6.6.2 Coplanar Isolation

Since the coplanar structure was expected to make fabrication of the 5 x 5 μm contacts and polysilicon and aluminum interconnects on 7.5 μm centers much easier, preliminary investigations of the new wafer fabrication steps needed were carried out early in the program. The coplanar process uses a silicon nitride oxidation barrier over

Figure 6-6 - Correlator/Convolver Test Pattern Photomicrograph
(Approximately 34x)

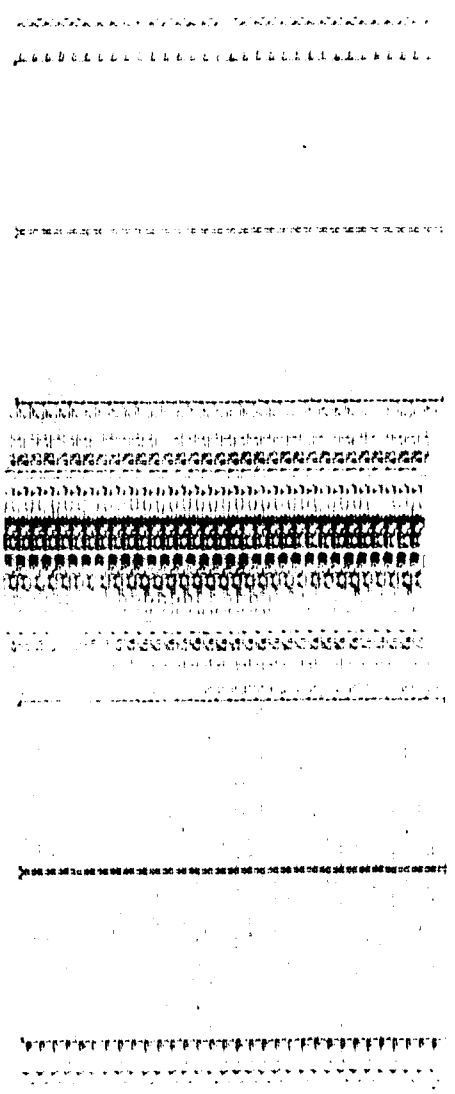


Figure 6-7 - Thirty-Two Stage Correlator Photomicrograph
(Approximately 46x)

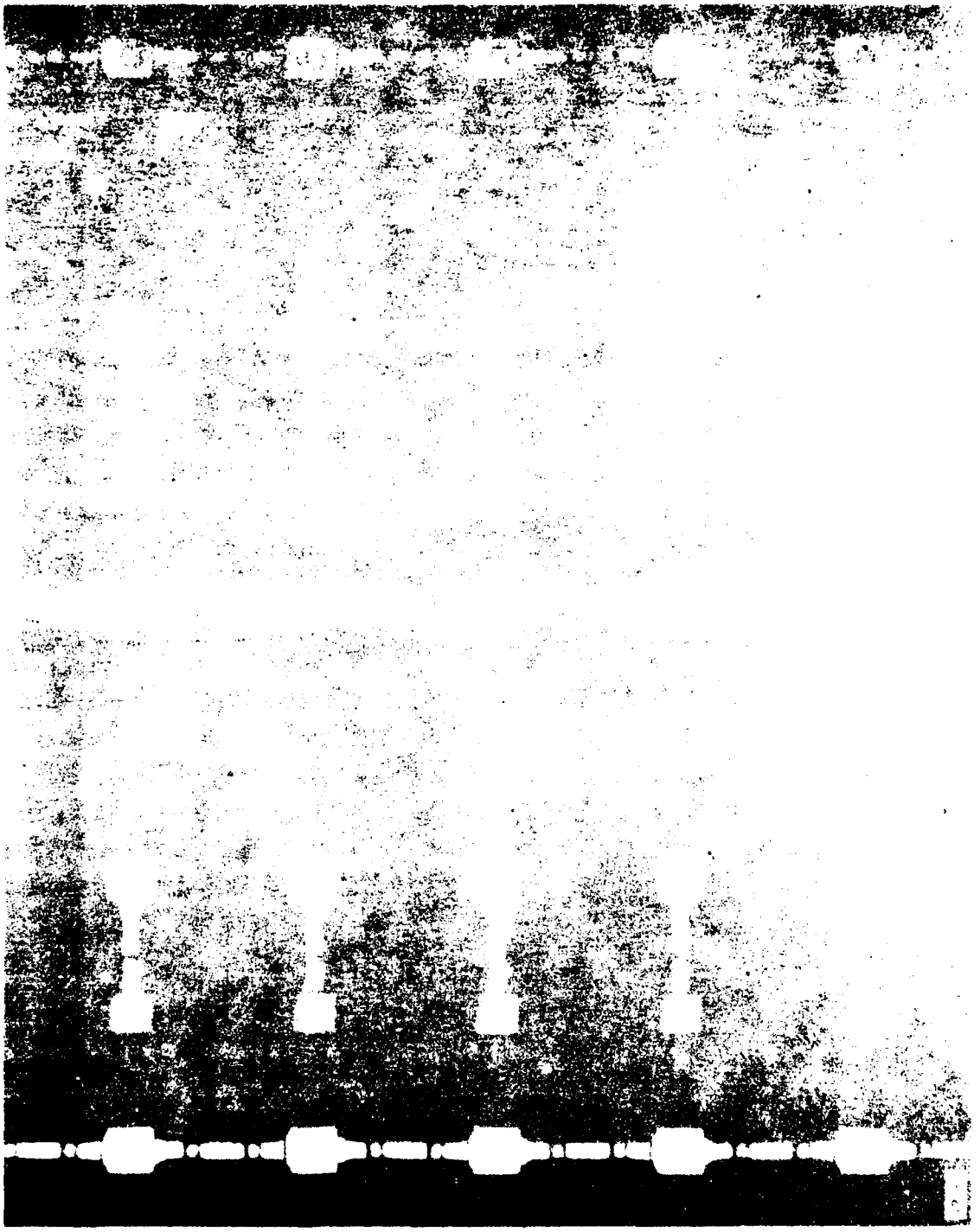


Figure 6-8 - Bridge Multiplier Photomicrograph
(Approximately 1200x)

the areas which will become active devices. The isolation areas are etched down by about one half the final field oxide thickness. Boron is lightly implanted into the isolation regions before the oxide is grown. Because of the lighter boron concentration, it is permissible to have the guardband form a junction around the transistor sources and drains without encountering an unacceptable reduction in isolation breakdown voltage. With conventional highly-doped diffused guardbands, a buffer of high-resistivity material must surround the source and drain regions.

Experiments with the coplanar process using both isotropic and anisotropic etching, etching depths from 0.3 to 0.45 μm, and boron doses from 3×10^{13} to 1.5×10^{15} per cm^2. In all cases, the final field oxide thickness was approximately twice the initial etch depth. The results of this work were used to create the curve shown in **Figure 6-9** of isolation breakdown voltage versus boron dose. In view of these results, we adapted a 0.5 μm etch depth and 10^{14} cm^{-2} implant dose for the coplanar oxide isolation version of the correlator/convolver.

6.7 Final Process

The process finally developed for the 256 stage convolver is detailed herein.

The correlator/convolver is produced using a double poly gate surface, N channel depletion mode, MOSFET transistor utilizing coplanar field oxide isolation. The process flow chart is shown in Table 6-2. A detailed description of this process follows.

Starting material for this technology is silicon and the substrates are 3 in diameter, P-type and 10-40 ohm-centimeter (cm). Wafers are rigorously cleaned using ultra pure chemicals and rinsed in 18 megohm (MΩ) D I water prior to initial processing. Upon completion of this cleaning cycle, the first set of fabrication procedures will improve minority carrier lifetime in the silicon crystal, thus improving transfer efficiency in the final CCD device. Lifetime improvement starts with the deposition of chemically vapor deposited (CVD) silicon oxide (SiO_2) on the front side only, of the wafers. This oxide will act as a barrier between the silicon substrate and layer of polysilicon which is now deposited, also, by CVD techniques. The polysilicon coats both front and back surfaces of the wafers. It is, however, only required on the back of the wafers where it will act as a lifetime improver through the introduction of stress dislocation at the poly interface, which in turn became favored migration sites for lifetime killing metallic ions. The poly is also ion implanted with boron since an electrically ohmic contact will be required at assembly. **Figure 6-10** depicts the wafer at this point in the process.

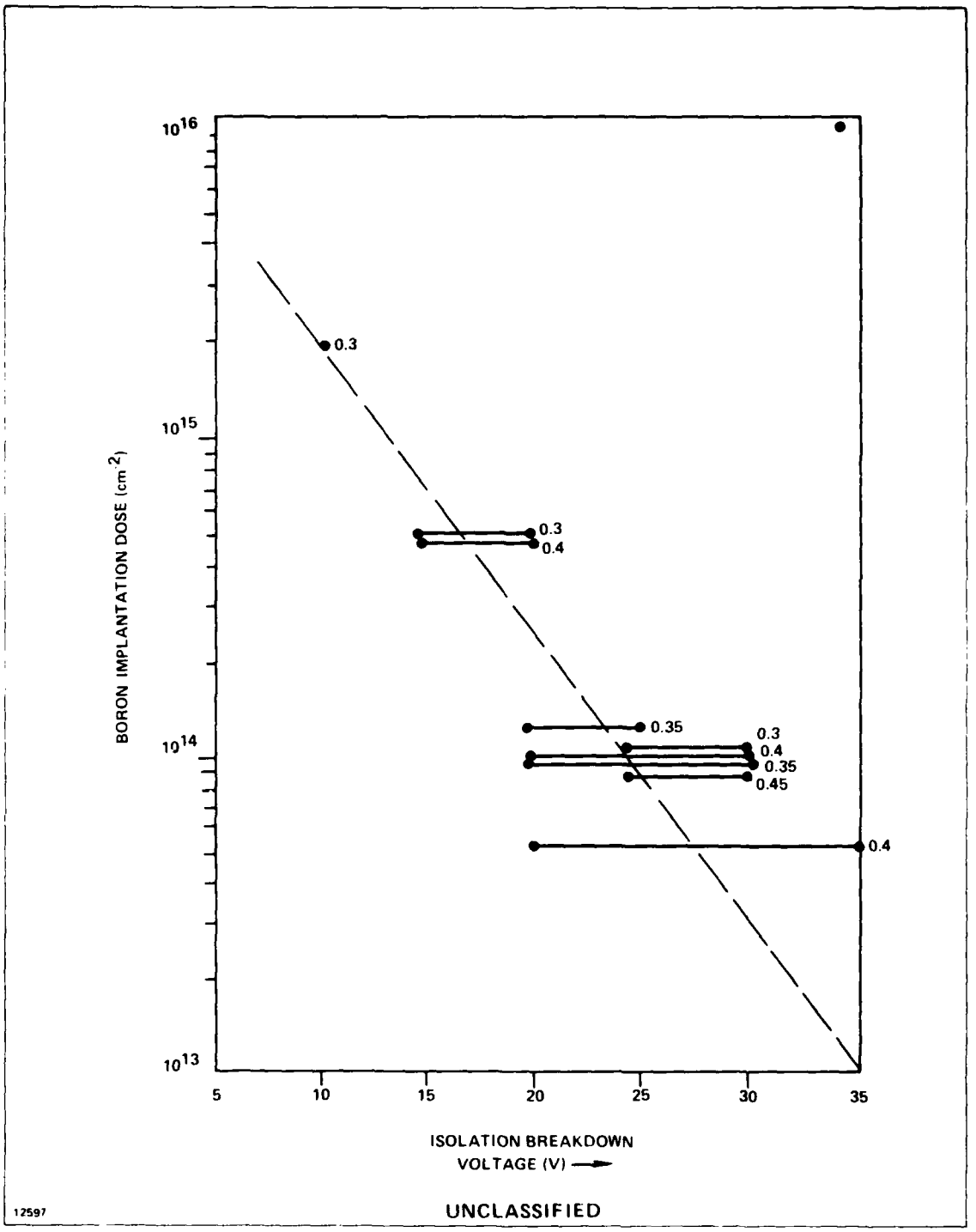


Figure 6-9 - Isolation Breakdown Voltage versus Boron Implant Dose for Coplanar Isolation Experiments (Numbers Adjacent to Data Indicate Silicon Island Etch Depth in μm)

TABLE 6-2

CCD FLOW CHART

1.	Starting Wafers	3" diameter "P" type 10-40 Ωcm.
2.	Lifetime Improvement	Deposit and implant back surface polysilicon.
3.	Isolation Mask	Define pattern, etch silicon moat, coplanar oxidation.
4.	Poly I	Deposit polysilicon and dope.
5.	Define Gates	Mask and etch first set of electrodes.
6.	Poly II	Deposit polysilicon and dope.
7.	Define Gates	Mask and etch second set of electrodes.
8.	Source/Drains	Implant S/D and anneal.
9.	Contacts	Mask and etch.
10.	Interconnects	Deposit composite poly/aluminum, interconnects, mask, etch.
11.	Backside Processing	Remove protective nitride over backside polysilicon.
12.	Backside Metallization	Deposit aluminum and alloy.
13.	Test	
14.	Scribe	
15.	Assemble	

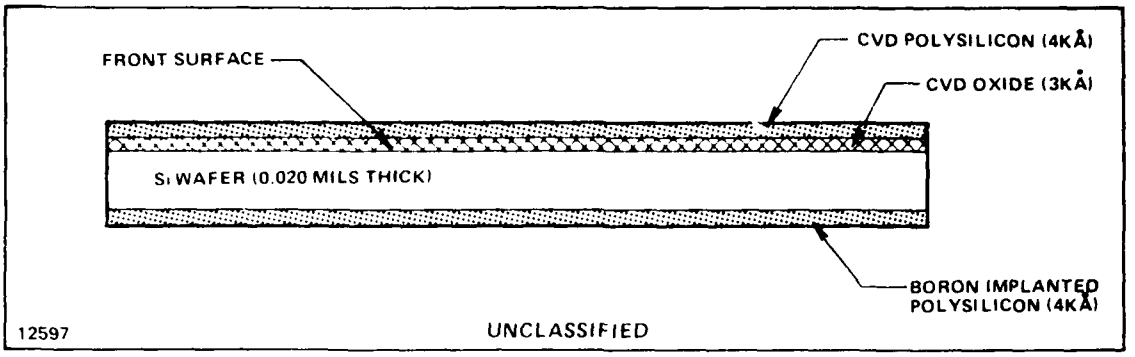


Figure 6-10 - Backside Implanted CCD Wafer

Polysilicon on the front of the wafer is not required at this point and is chemically etched away after first protecting the backside poly with a coating of photoresist as shown in Figure 6-11. CVD oxide under the poly prevents the substrate surface from being etched. It is now removed by chemical etch as well as the protective backside coating of photoresist. Wafers are now ready for frontside processing.

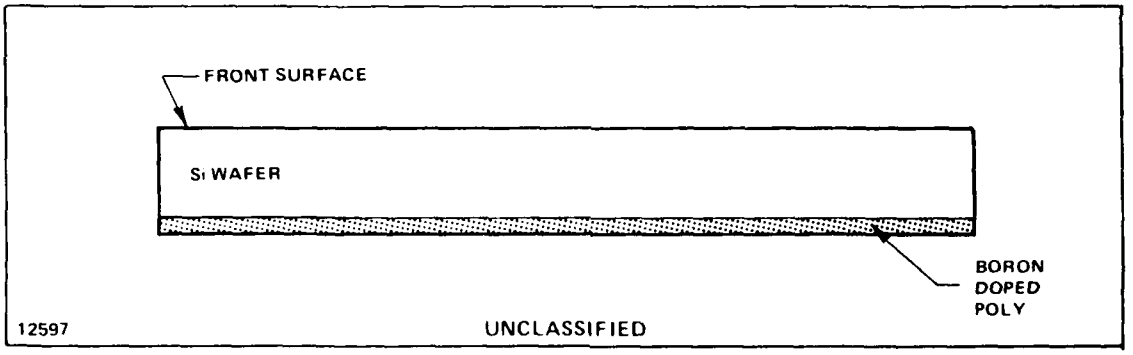


Figure 6-11 - Wafer Ready For Frontside Processing

After additional cleaning, the wafers are then put into a high temperature furnace where a high purity "gate" quality oxide is grown (700k) thermally. The polysilicon on the back of the wafers is also oxidized. Special nandling from here to the end of the process will preserve this oxide, thus protecting the backside polysilicon from being etched away at several steps in the remaining processes. Gate oxidation is then

followed by CVD deposition of silicon nitride (Si_3N_4). The wafers are now ready for the delineation of the isolation pattern surrounding the CCD transistors and all other components. Oxide isolation (OI) will be used and requires that a groove be etched into the front of the silicon wafer and then oxidized "up" to provide a co-planar surface of silicon and oxide isolation. This "groove" pattern is delineated onto the Si_3N_4 surface using standard photolithography. The Si_3N_4 is then plamsa etched down to the SiO_2 which in turn is chemically removed. The isolation groove is etched into the silicon to a depth of 4.5 kiloampere (kA) using an anisotropic chemical etchant. The wafer now appears as shown in Figure 6-12.

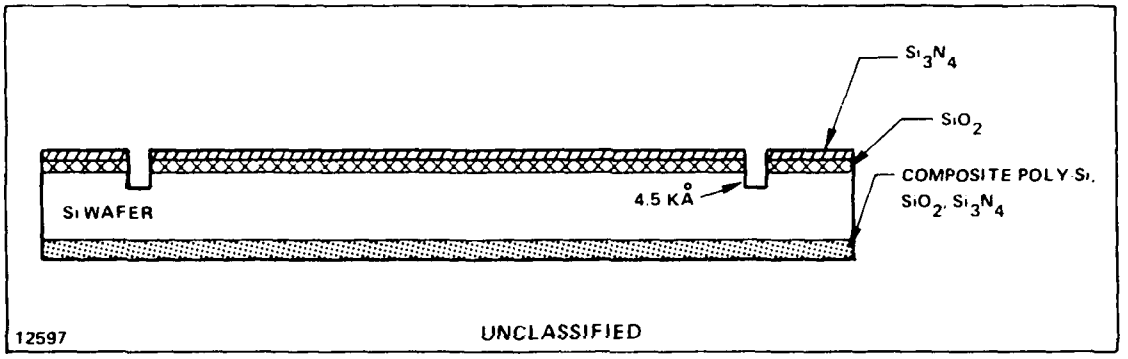


Figure 6-12 - Isolation Pattern Delineated

Prior to "planarizing" the wafers, a P-type implant is directed into the isolation groove. This implant will diffuse ahead of the oxidation front during planarization and prevents conductivity inversion in the high resistivity P silicon surrounding the isolation oxide. The wafers are implant annealed and oxidized for an amount of time sufficient to convert silicon in the groove to SiO_2. Silicon nitride used as a protective mask against oxidation in the device area is then removed as well as the underlying oxide. The wafers are now as shown in Figure 6-13.

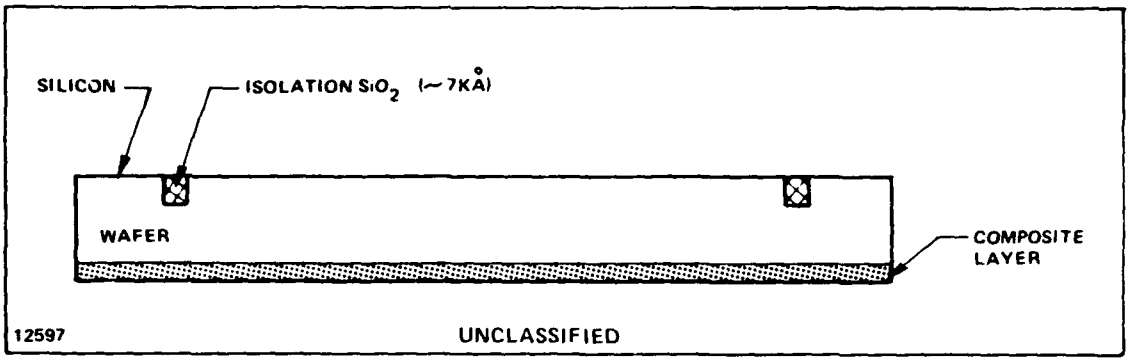


Figure 6-13 - Wafer With Co-Planar Isolation Completed

Fabrication of the split electrode, 2-phase, N-channel CCD device and associated circuitry is now ready to begin. A 1200 A gate oxide is grown on the wafers. This is followed by the deposition of CVD polysilicon 5 kA thick for delineation of first layer gate electrodes. The poly is dopen N-type with phosphorus for improved condictivity and is photolithographically patterened to delineate the first set of gate electrodes across the CCD field as shown in Figure 6-14.

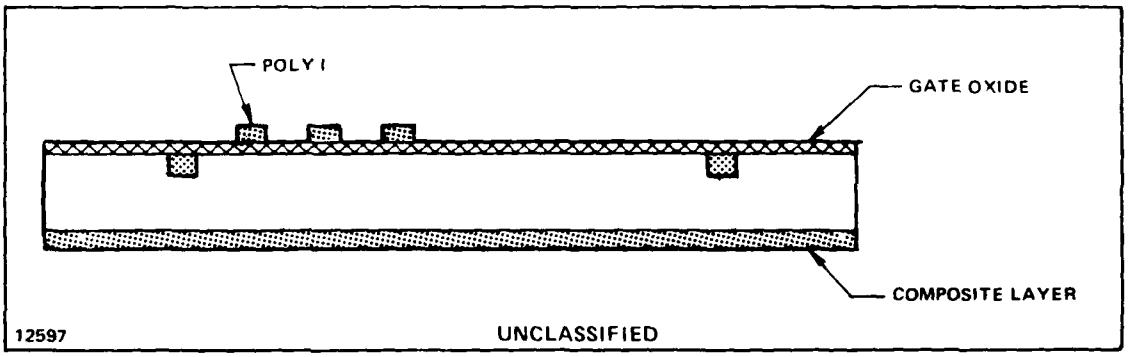


Figure 6-14 - Poly I Gates Defined

The wafers are then reoxidized. This process (a) grows a protective dielectric oxide over the poly gates and (b) increases the gate oxide thickness between the first level poly electrodes in preparation for a second layer of poly which will then be delineated and have new threshold voltage characteristics, as shown in Figure 6-15. This

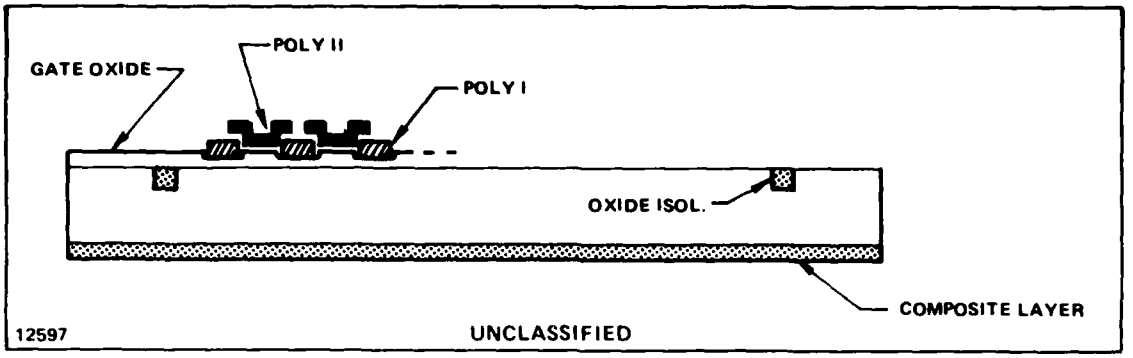


Figure 6-15 - Poly II Gates Defined

second layer of poly is also doped with phosphorus for improved conductivity prior to photomasking. Critical alignment of the second set of gates provides a small amount of overlap of Poly II to Poly I, thus preventing the occurrence of any field-free regions in the CCD array.

Using the CCD array poly gate electrodes as an implant mask, the wafers are now ion implanted with a high concentration of phosphorus to produce the source/drains of all the transistors. Thermal anneal of this implant is followed by an oxidation cycle which will passivate the Poly II gates and prepares the wafers for interconnect metallization. Contact via masking completes the preparation necessary for metallization.

Interconnect metallization consists of a laminate layer of doped polysilicon (Poly III 2.5 kA) and aluminum (5 kA). This combination has demonstrated excellent step coverage characteristics over the gate electrode topography and good definition when photomasked and etched. The wafers are complete except for the removal of the protective layers of nitride and oxide on the back surface. They have preserved the polysilicon originally deposited there for lifetime improvement purposes and are not required anymore. A final layer of aluminum is deposited onto the wafer backs and then alloyed to provide good ohmic contacts for epoxy mounting in final packaging. The completed wafers are electrically tested, scribed, and assembled.

7. 256-STAGE CORRELATOR CONVOLVER

Despite the size and complexity of the chip, a good yield of devices that functioned as correlators, was obtained. The level of performance hoped for, based on the performance seen previously for the individual elements, was however not obtained. Limitations of time and funds prevented an exhaustive and systematic characterization of the devices and a determination of the factors that limit the performance.

This section will contain a brief description of the experimental procedure and apparatus used for the tests. It will be followed by a discussion of the performance of the CCDs. Finally, a variety of correlation results will be shown. First, for reference, we show the device pinouts in **Figure 7-1.**

7.1 Experimental Procedure and Apparatus

The correlator/convolver chip is very complex with many independent operating sections. The total pin count is 44, not including the substrate connection. Each dual-channel CCD has six clock connections ($\phi 1$, $\phi 2$, $\phi 4$ and ϕC for both channels, and separate $\phi 3$ inputs for the two channels). In addition, an input diffusion is clocked with a sampling pulse. That makes a total of 14 clock inputs for the chip. Each clock signal could have separate high and low levels, requiring 28 power supplies. Each CCD also needs a bias on IG1, and the output and requires bias for OG1, plus OG2, minus OG2 and D. Each set of buffer of amplifier requires three supplies = VDD, VGG, VSS. It is easy to see that exercising all the degrees of freedom available is not practical; some simplifications must be made.

It was decided to operate the gate-driving CCDs (CCD-GD) and the drain-driving CCDs (CCD-DD) nearly identically. The input gates IG1 were wired together, and all eight output structures OG1, IOG2, and D were given the same bias. The clocks for the two CCDs must operate independently, of course, but common clock levels were used for them, except for plus $\phi 3$ and ϕC. Moreover, the same low and high levels were used for $\phi 1$, $\phi 2$ and $\phi 4$. The FG, controlled by plus $\phi 3$ and ϕC, must have different levels to provide the required dc of offset between the outputs of CCD-GD and CCD-DD.

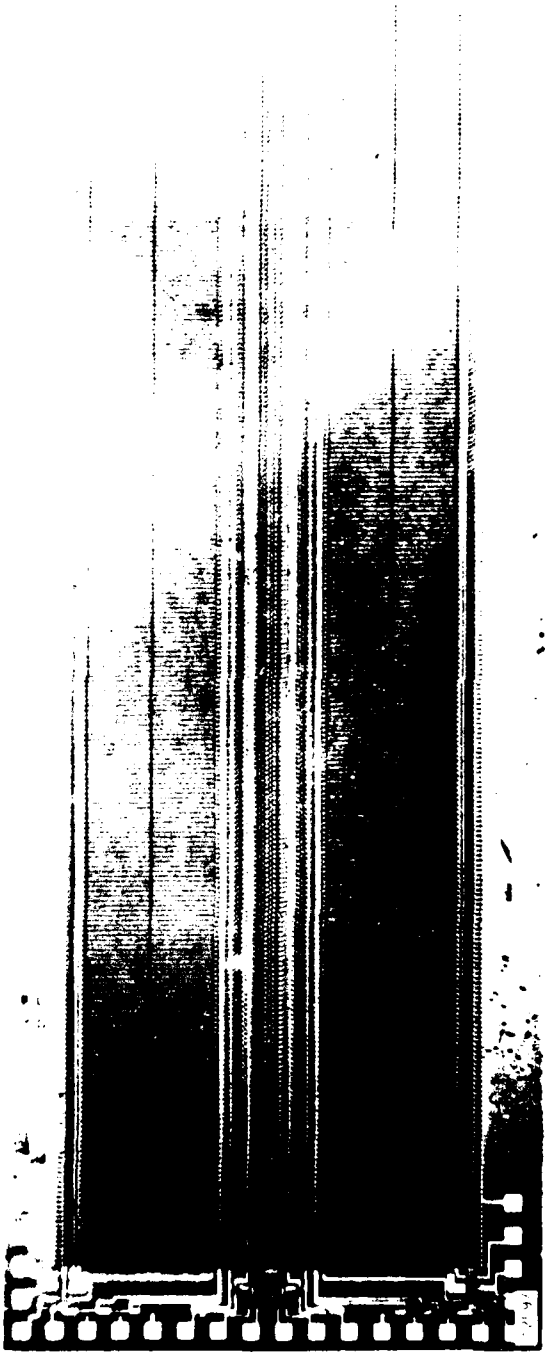


Figure 7-1 - Device Pinout of Type 457 Correlator/Convolver

To accomplish this the high level for ϕC and the high level for plus $\phi 3$ and minus $\phi 3$ (wired together) were allowed to be set individually. They shared their low level with the other clock phases.

Timing to control the periodic refreshing of the reference channel and the coherent generation of both the reference and signal waveforms is also complex. A control system was therefore built using digital logic (mostly transistor-transistor logic (TTL)). A counter driving eraseable programmable read-only memory (EPROM) address lines was used to generate the clock logical waveforms. This provided much greater flexibility and ease in changing clocking waveforms. Additional counters kept track of the number of clock cycles. The analog signal and reference waveforms were also derived from data stored in EPROMs using digital-to-analog converters. Again this provided much greater ease and flexibility in providing waveforms than would have been possible with signal generators. No further details about the test apparatus will be presented here.

7.2 Operation of CCD Channels

The CCD channels are actually 258 stages long. In addition to the 256 stages in the center that are used for correlation, one extra stage is provided at each end. These extra taps have an additional source-follower driver transistor and are brought to eight pins on the chip. In this way the signals entering and leaving each of the four CCD channels can be observed and appropriate adjustments made in clock and bias levels.

Even after all of the operating simplification described in Subsection 7.1, many variables remain. The CCDs are able to operate with an unlimited number of combination of clock levels and bias conditions. It is, therefore, impossible to provide a meaningful set of operating specifications for the devices. The values in Table 7-1 represent the conditions observed in one experiment. They can be used for the initial set up in an experiment. Results shown in this report were obtained using a variety of operating conditions.

Figure 7-2 shows the CCD outputs at the beginning and end of one of the reference channels. The effects of charge transfer loss are visible in the lower trace. The transfer efficiency per transfer is approximately 0.999, a fairly good value. Unfortunately it was not typical of the performance observed on the wafers with functional devices. **Figures 7-3A and 7-3B** shows the more commonly observed output.

TABLE 7-1
CCD OPERATING SPECIFICATION

PIN FUNCTION	DRAIN-DRIVING SECTION VOLTS	GATE-DRIVING SECTION VOLTS
SP	3-5 1/2	3-5 1/2
$\phi 1, \phi 2, \phi 4$	2-12	2-12
$\phi 3$	2-9	2-16
ϕC	4-9	6-14
$\pm OG_2, OG_1, D$	14	14
V_{DD}	9	11 1/2
V_{GG}	4 1/2	7
V_{SS}	3	5 1/2
IG_1	3 1/2	3 1/2
$\pm IG_2$	2-4	2-4
$\pm\Sigma$	6	

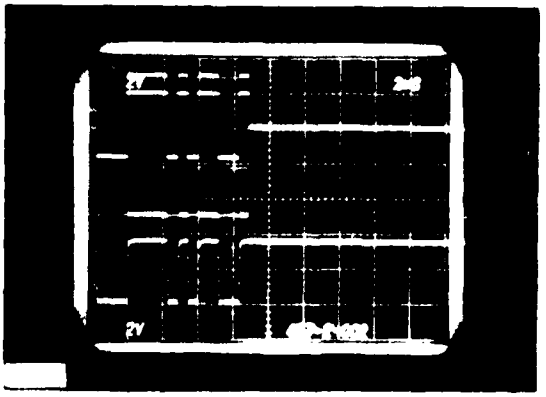


Figure 7-2 - Reference Channel CCD Output

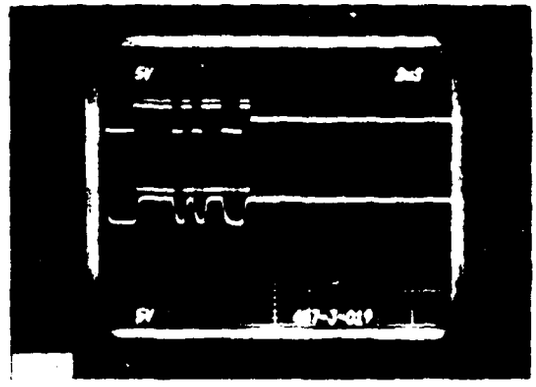


Figure 7-3A - Typical Charge Transfer Losses in CCD Outputs from Reference Channel (A) and Signal Channel (B)

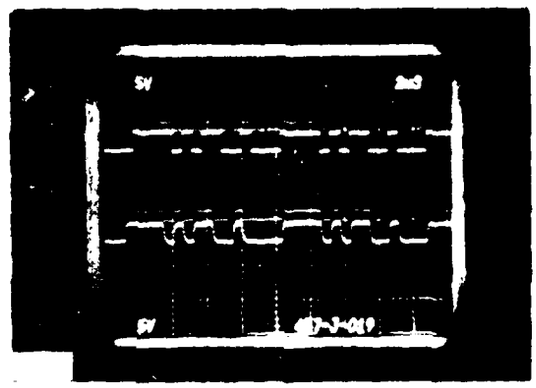


Figure 7-3B - Typical Charge Transfer Losses in CCD Outputs from Reference Channel (A) and Signal Channel (B)

The thermal leakage of most of the devices was such that signals could be stored for times in the order of 100 to 200 millisecond (msec) at room temperature. Occasional devices suffered from very poor leakage, as **Figure 7-4** shows. In **Figure 7-4A** isolated cells are seen with high leakage, whereas **Figure 7-4B** shows broad areas of excess leakage, including the last stage of the CCD. The leakage here is not all channel leakage, however, as shown by the decay of the trace after the clocks stopped. Channel leakage of that magnitude would have saturated all the wells in a small fraction of the refresh interval.

7.3 Correlation Performance

Figure 7-5 shows the correlation output (lowest trace) with a square wave reference (upper trace) and signal (middle trace). The linearity of the expected triangle wave is excellent. **Figure 7-6** shows a blow up of a section of such an output on another device. It is difficult to determine the linearity accurately from the photo, but the one percent goal seems to be met.

It was desired to examine the pulse compression capability of the device. **Figure 7-7** shows results with the 13-bit Barker code. Since each of the 13 bits is repeated eight times, each point in the theoretical output is modulated by a triangle. The peak triangle has an amplitude 13 times higher than the sidelobes.

We then looked for a signal with lower sidelobes. The ideal choice would have been the 255-point cycle PN sequence, the autocorrelation function of which has only two values, 255 and minus 1. Unfortunately, the test apparatus could only use signals with 256 cycle repetition periods. An exhaustive computer search showed that there was no place in the 255-point sequence in which a single zero could be inserted without producing huge sidelobes. A useful test waveform was however discovered. The 15-point PN sequence was employed using each point 17 times. This 255-point sequence gives an autocorrelation function which has a perfectly flat sidelobe baseline at minus 17 and a triangular peak rising from minus 17 to plus 255 in 16 steps of height 17 and falling again. Appending a single zero to this sequence gives a 256-point sequence with ripples of only one percent.

The experimental autocorrelation outputs are shown in several photos below. The input waveforms were seen already in the earlier figures (e.g., **Figure 7-2**). **Figures 7-8A and 7-8B** shows the correlation outputs for the two devices whose CCD output were shown previously in **Figures 7-2** and **7-3**. Despite their large difference in charge transfer

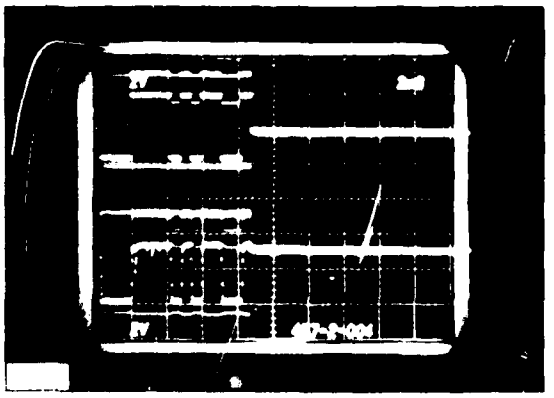


Figure 7-4A - Two Examples of Excess Thermal Carrier Generation

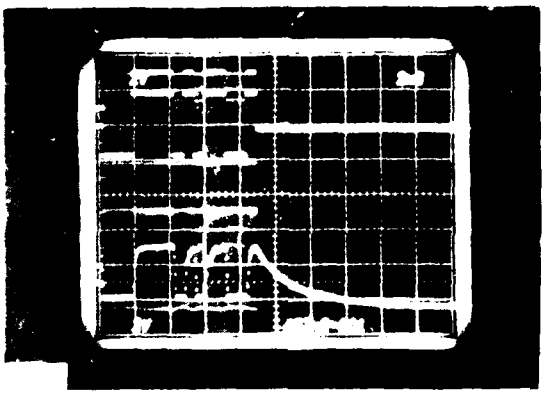


Figure 7-4B - Two Examples of Excess Thermal Carrier Generation

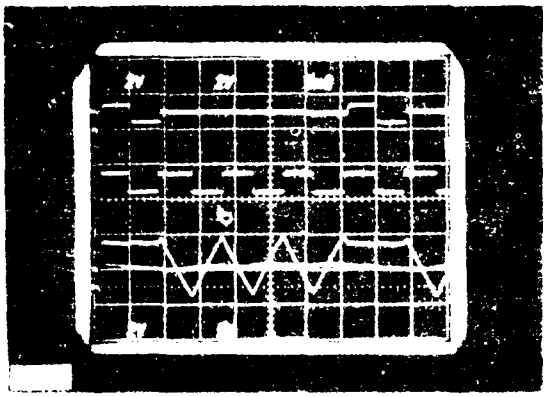


Figure 7-5 - Highly Linear Triangle Wave Correlation Output for Square Wave Outputs

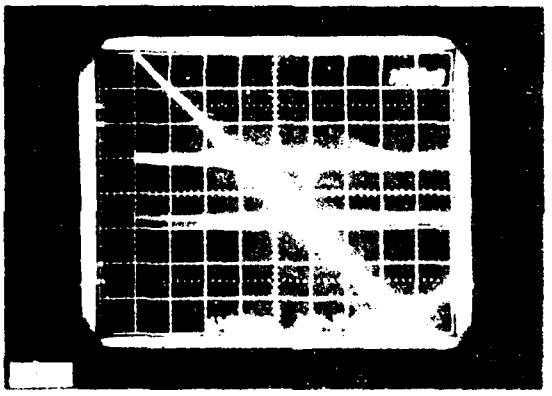


Figure 7-6 - Expanded View of Part of Triangle

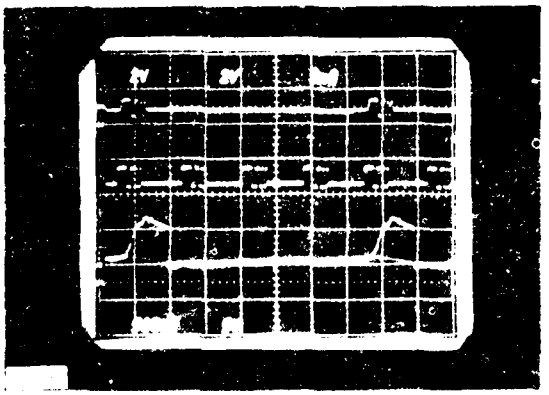


Figure 7-7 - Correlation Using a 13-bit Barker Code

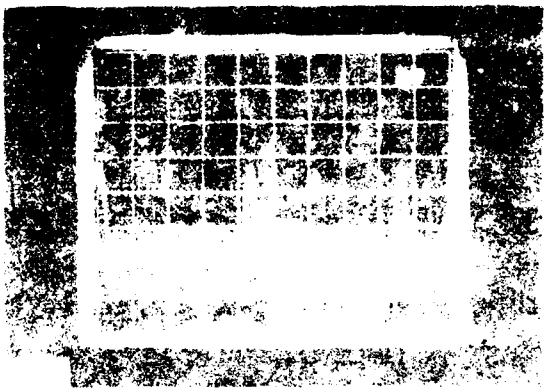


Figure 7-8 - PN-sequence Correlation

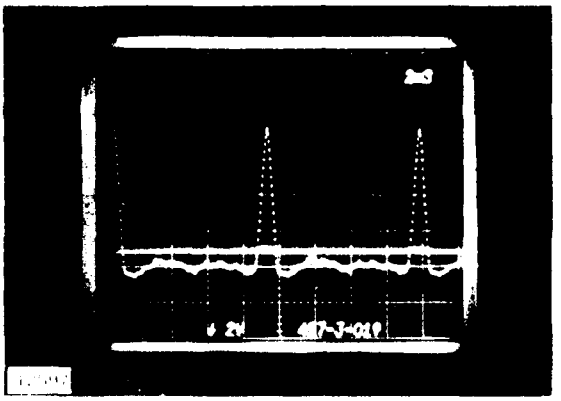


Figure 7-8B - PN-Sequence Correlation

efficiency, the two devices give equally good correlation outputs. Neither, however, exhibits the very flat sidelobes expected theoretically. The flattest sidelobes observed were about plus five percent of the peak amplitude as shown in **Figures 7-9A** and **7-9B**. A blow-up of the correlation peak is shown in **Figure 7-10**.

An interesting series of experiments, is shown in **Figures 7-11** and **7-12**. **Figure 7-11A** shows the usual correlation. It is very strong and has sidelobe fluctuations of about plus or minus five percent. **Figure 7-11B** shows the result of replacing the normal-mode signal inputs with common-mode inputs (i.e., the two halves of the signal channel CCD carry identical signals instead of a signal and its inverse). **Figure 7-11C** shows the result of using a common-mode reference waveform. In both cases fluctuations are seen of about the same magnitude as in the usual correlation. The surprise comes in **Figure 12A**, which shows the result of using both a common-mode reference and a common-mode signal. There is a clear correlation peak with very flat sidebands. The peak is only about five percent as large as the usual peak, but the ripple is corresponding small, as shown in **Figure 7-12B**, a double exposure with both correlations adjusted to have the same peak height. This phenomenon is an important clue toward understanding the defects in the chip, but as yet its meaning has not been deciphered.

The above experiments, with the essentially digital waveforms, do not really exercise the linearity of the individual multipliers; they use only the four corner products plus 1 times plus 1. Experiments were therefore performed using sinusoidal inputs. Two identical sinusoids correlated against each other gave sinusoidal outputs at the same frequency with very high purity (harmonic products at least 50 dB down). Orthogonal sinewaves,

Figure 7-9A - Correlation Peaks in Other Devices Showing Sidelobe Ripple of plus Five Percent

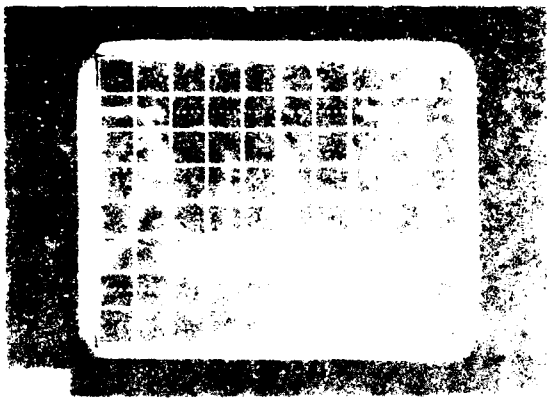


Figure 7-9B - Correlation Peaks in Other Devices Showing Sidelobe Ripple of plus Five Percent

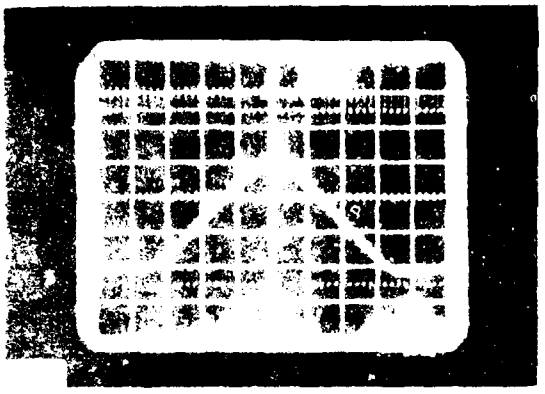


Figure 7-10 - Expanded View of the Triangular Correlation Peak

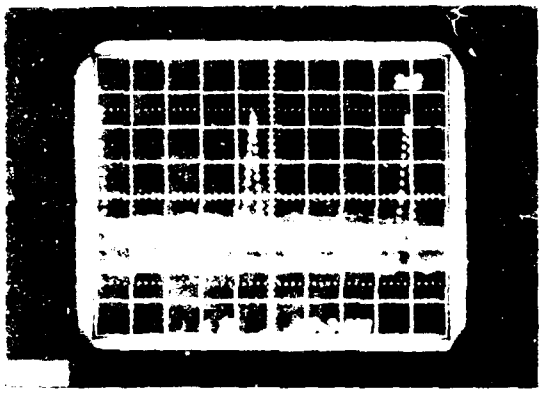


Figure 7-11A - Correlation Peak with Normal-Mode Signal and Reference

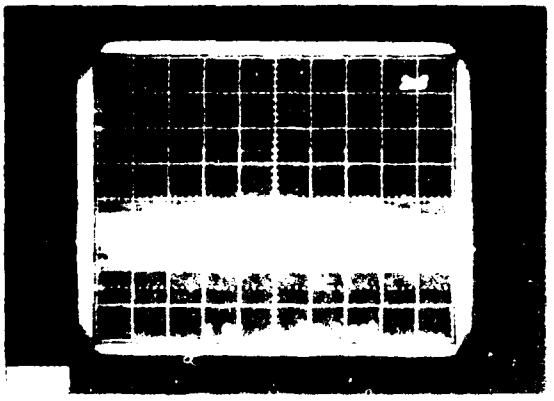


Figure 7-11B - Correlation with Common-Mode Signal Output

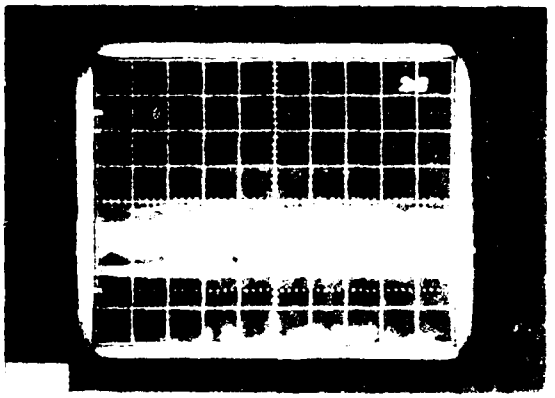


Figure 7-11C - Correlation with Common-Mode Reference Input

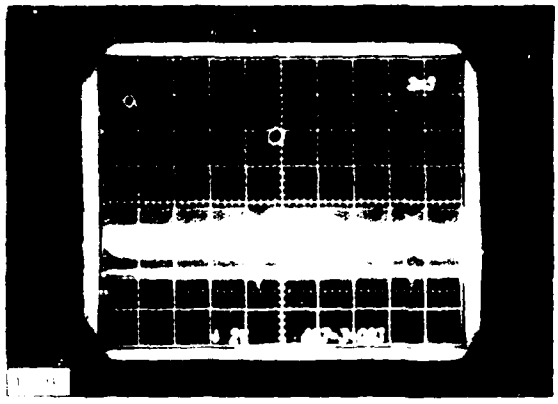


Figure 7-12A - Correlation with Common-Mode Signal and Reference Inputs

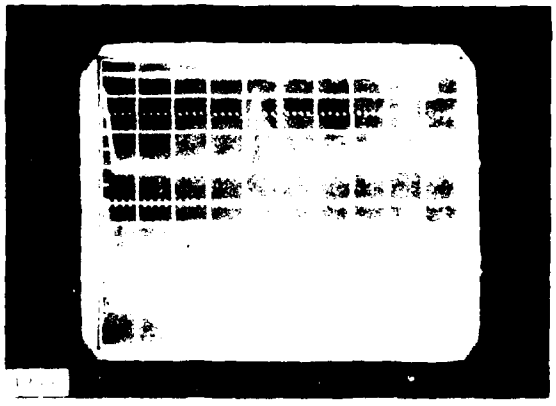


Figure 7-12B - Double Exposure Showing Common-Mode Correlation on Same Scale as Normal-Mode Correlation from Figure 7-10A

however, did not give zero output as expected theoretically. Typically, a spurious output with the general appearance of the input waveform in one of the channels was observed. The same was true for correlations of a square wave with sinewaves. With sinewaves at frequencies f, 3f, 5f, etc. (f = square wave frequency), the outputs were sinewaves at the corresponding frequencies with relative amplitudes of 1, 1/3, 1/5 etc. Correlation with a sinewave at 2f, however, gave a spurious output. In one case it was a low amplitude sinewave at frequency 2f. If the signal and reference channels were reversed, the output became a low amplitude square wave. A consistent output error in the range plus five percent was found in all experiments. The cause was not determined.

7.4 Suggestions for Further Experiments

7.4.1 Operating Frequency

The test apparatus using EPROM data to generate the clock waveforms is limited to clock cycle frequencies well below 1 MHz. Consequently, any study of the operating frequency limits would have required a different experimental set-up. A suggestion for future work is to use the EPROM-based apparatus to carry out the reference channel refresh operation but to use laboratory pulse generators (6) and a signal generator for the signal channel. Some provision for sampling and holding the correlator output would probably be needed. For the experiments reported, this requirement was circumvented using skewed clock timing as described in Section 4. The part of the clock cycle during which a valid output is available is increased in duration so that the signal is clearly visible on an oscilloscope.

Based on the skewing rate observed for the floating gate output buffer amplifiers, the ultimate operating frequency would be significantly below 10 MHz. Operation at 10 MHz would require some tricks to speed up the amplifiers without increasing power dissipation in the more than one thousand buffer amplifiers.

7.4.2 Dynamic Range

The dynamic range of the correlation output was not measured. The photos in Figure 12 show a total noise level about 62 dB below the peak. The noise observed on the oscilloscope trace however, includes noise from all sources (including the scope, clock pick-up, etc) and over a huge bandwidth. It only establishes an upper bound on the correlator's signal-to-noise ratio.

No detailed experiments were performed in which the signal amplitude (or reference amplitude) was reduced. Qualitatively, the ripples in the sidelobes tended to decrease proportionately. This can be seen to some extent in the collection of photos in this section, where different correlation peak height corresponding to different signal amplitudes are shown.

7.4.3 Convolution

Although the chip functions with equal ease as a convolver, it was only operated as a correlator. There is a defect in the design of the chip that makes it impossible to operate the chip as both a correlator and convolver with the same clock waveforms. The CCDs or the chip begin with $\phi 1$ and end with $\phi 4$. Consequently, when the CCDs carry charge forward, as in a correlator, there are two clock phases ($\phi 1$ and $\phi 2$) before the first FG ($\phi 3$). However, when they operate in reverse (using D, OG1, and plus OG2 in place of S, IG1, and plus IG2), there is only a single clock phase ($\phi 4$) before the first FG. This asymmetry necessitates different clock timing for convolution. Had the CCDs begun and ended with $\phi 1$, merely interchanging the connections to $\phi 2$ and $\phi 4$ would have reversed the direction of operation of the CCD. The correlator test apparatus could then be used equally well for convolution. At present, special clock patterns would be needed to study convolution, or laboratory pulse generators could be used for the signal channel as described in Subsection 7.4.1.

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

Printed by
United States Air Force
Hanscom AFB, Mass. 01731