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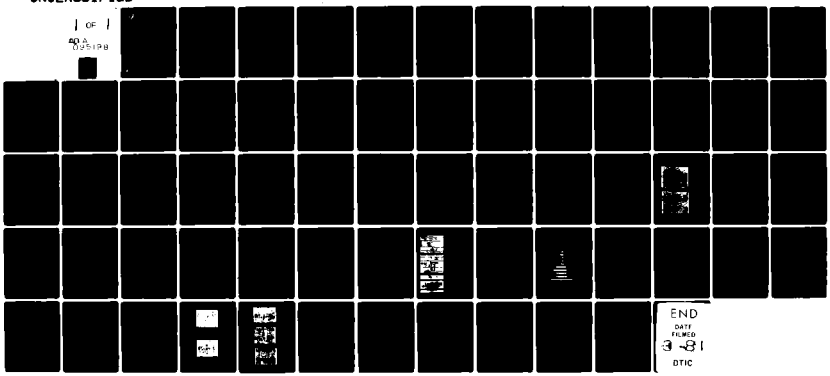

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TACTICAL VIDEO DISPLAY

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Hycom has completed the first phase of a development program to design and fabricate a 512 x 640 line electroluminescent display. The program entails two major areas of efforts: the first is to improve the display panel and the second is to improve the drive electronics. The display panel in this program is larger and is of higher resolution than any previous TFEL panel. The panel also incorporates a black layer to absorb refracted light and to enhance the contrast. The drive circuitry effort is to develop circuitry which will provide video → cont.

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modulation with low power dissipation. The objective is to design a driver that can overcome the capacitive and resistive parameters of the panel while still being implementable in a compact and inexpensive form.

PREFACE

The fabrication of the TVD panels is supported in part by the Sharp Corporation of Japan. The initial black layer development effort, prior to this contract, and continuing support has been funded by the Sharp Corporation.

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I. INTRODUCTION TO TACTICAL VIDEO PROGRAM

The Tactical Video Display Program is a two-year development effort designed to extend the state-of-the-art in the area of thin film electroluminescent display systems. The program entails two major areas of efforts: the first is to improve the display panel and the second is to improve the drive electronics. The display panel in this program is larger and is of higher resolution than any previous TFEL panel. The panel also incorporates a black layer to absorb incident light and to enhance the contrast. The drive circuitry development effort is to develop circuitry which will provide video modulation with low power dissipation. The objective is to design a driver that can overcome the capacitive and resistive parameters of the panel while still being implementable in a compact and inexpensive form.

During the second six months of this program we have continued the development efforts on both the black layer and the drive circuitry. The black layer effort continues to be limited to about one-quarter of the total active area of the TFEL panel, but this is not a problem relative to development of the desired black layer film properties.

The drive circuitry effort has produced further refinements on the specifications of the monolithic driver chips and the letting of the subcontract for their fabrication. The subcontractor, Supertex, Inc., has done extensive computer simulation of the design with the device parameters that will be achievable in the final integrated circuit. A breadboard of the total drive scheme using the closest available MOS FET's (Metal-Oxide-Semiconductor Field-Effect Transistors) has been completed and evaluated. Some potential problem areas were discovered with the breadboard, but they have all been resolved with the computer simulations. The closest transitors we could get (although made by Supertex) are not really suitable for this application so the performance shows more promise than fulfillment.

II. BLACK BACKGROUND

During the period of the TVD Phase I Contract, our efforts were concentrated on the optimization of the electro-optical characteristics of the black layer in conjunction with the TFEL structure. The merit of success of the black layer application was based upon several interdependent variables. Diffuse Reflectance (D_R), the Surface Resistance (ρ_S) of the film and the back electrode (Al) definition became very important parameters. The following disucssion is concentrated on our approach to optimize the process parameters of this black layer.

The position of the black layer within the panel is one of the problems that needed to be solved. The use of a black layer behind the phosphor layer can cause phosphor contamination, reduction of light output, shortened life and low voltage breakdowns. The black layer is more stable and durable (physically and chemically) if applied behind the second dielectric layer.

With an ideal black layer behind the second dielectric layer the internal reflection of the TFEL layers amounts to 1.9% reflectivity, while the air/glass interface (external reflection) accounts for an additional 4.0% reflectivity. The total reflection of the normal incident light through the structure of the TFEL panel is ∿5.9%, as shown in Figure 1. Part of the incident light is either absorbed or transmitted, but most of the light is trapped and reflected by many internal scatterings (halation). This phenomenon is heavily dependent upon the grain boundary structure of ZnS:Mn phosphor and the interfaces of different layers. Three different cases of the internal light scattering patterns are exhibited in Figure 2. In Figure 2A, powder ZnS is the most severe case where the scattered light intensity in an unexcited area adjacent to an energized area is very large and damaging for contrast ratio. The very small granular-structured surface is the most ideal to virtually eliminate any internal scattering; unfortunately, ZnS of that nature tends to be inefficient and poor in light emission. For an efficient ZnS:Mn phosphor it is significant and essential to grow the ZnS grain structure to an optimum size, which is greater than 0.3 μm. The scattering surface appears on the upper surface and causes a varying degree of internal scattering, but much lower than the powder structure. The scattering problem suffers further due to the Al electrode deposited on this rough surface because it has a high reflectivity of 90%.

The reflectance at the interface of air/glass must be reduced to a minimum with the application of an antireflection coating. The combined effect of an antireflection coating at the glass surface and a black layer behind the second dielectric can theoretically reduce the total reflection to less than 2% in a high intensity ambient light.

A. Theory

Basically, there are two different theoretical processes available to develop an ambient light-absorbing thin layer; they are:

1. Optical absorption effect, and
2. Dendrite structure (interference effect).

1. Optical Absorption

For a semiconductor to absorb light in the visible spectrum, it is essential to generate excess electrons in the valence band upon impinging light. The valence band contains many electrons and the conduction band has many empty states into which electrons can be excited. Excited electrons lose energy to the lattice in scattering events until their velocity reaches the thermal equilibrium velocity of other conduction band electrons already in existence there. Electrons and holes are created by this absorption process and they are out of balance and thus must recombine at some energy level in the band gap.

A photon with energy, $h\nu$, less than band gap, E_g, is unable to excite an electron from the valence to the conduction band. These photons are transmitted and appear transparent in certain wave length ranges. If a photon with $h\nu > E_g$ falls on a semiconductor, some predictable amount of light is absorbed, as given by the following equation:

$$I_t = I_o e^{-\alpha d}$$

where

- α absorption constant
- d thickness of the sample
- I_t transmitted light intensity
- I_o incident light

The light energy transfer mechanism to the crystal via electron-hole pair recombination can be categorized with respect to the intrinsic and extrinsic properties of the absorbing materials.

a. Metallic: Plenty of free carriers available in the band gap region, E_g. Light absorption with energy $h\nu < E_g$ is absorbed by these free carriers.

b. Composite metal/insulator films of small metal particles embedded in a dielectric have the optical property of a good selective absorber. They absorb strongly in the visible due to interband transitions in the metal and the small particle resonance while they are transparent in the infrared region. The Maxwell-Garnett equation satisfies the system

$$\frac{\bar{\varepsilon} - \varepsilon_o}{\bar{\varepsilon} + 2\varepsilon_o} = F \frac{\varepsilon_m - \varepsilon_o}{\varepsilon_m + 2\varepsilon_o}$$

where

$\bar{\varepsilon}$ extinction factor

ε_m metal/insulator

ε_o insulator

F volume fraction of metal

Fe, V, Ni, Zn, Al with Al_2O_3, MgO, SiO_2 and SiO have been occasionally used.

c. Semiconductors: II-VI compounds have the flexibility of self-compensation of net charge in the crystals. Composition of different compounds with different band gaps with availability of excess electrons in their interaction causes formation of new band gaps with intermediate energy level and thus absorption of photons of energy greater than or equal to the band gap.

Phenomena a, b, and c are exhibited in Figure 3.

2. Dendrite Structure (Interference Effect)

A dendrite structure is also applied to many solar absorbing devices. Incident light is trapped, scattered, and finally absorbed in a conical growth of material like WO_2, InN and Si_3N_4. Usually these types of films have been obtained using vacuum electrochemical reaction (anodic reaction) and chemically etched surfaces. For maximum visible light absorption, cones (Hillock) must have a total included apex angle of 120° or larger to minimize the dependence on the angle of incident light.

B. Hycom's Black Layer

The formation of this black layer is a result of multi-reactions of sulfur hexaflouride (SF_6) gas with the ZnS target. The exact chemical process of the formation at the target surface is least known, but the final physiochemical characteristics are similar to both metal/insulator and dendrite type structure.

In sputtering processes, the inclusion of the residual gases in thin film is very likely and dependent upon the concentrations of the gases and the reactive nature of the species. Dissocation of SF_6 is easily performed, either by heating at temperatures higher than 132°C or by simply ionization in the plasma. Fluorine, F, with electronegativity 4.0 (the highest in the periodic table), readily reacts with ZnS molecules and is believed to form ZnF_2 which itself is unstable at high temperatures and plasma and is dissociated during the formation on the substrate, leaving a Zn-rich film.

$SF_6 \rightarrow SF_5^+ + F^-$	(1)	Ionized	These reactions are only expected at the surface of the substrate.
$Zn^{++}S^{--} + 2F^- \rightarrow ZnF_2 + S_{2-8}$	(2)		
$ZnF_2 \rightarrow Zn + F_2$	(3)	Dissociation	

In reactive sputtering, chemical reaction at the surface of the substrate is a dominant one. The target material arriving at the surface of the substrate is heavily ionized and elemental. Evidently, reactions numbers 2 and 3 take place at the substrate.

X-ray and SEM analyses were performed on several black layer samples, either with the TFEL structure or on glass substrates. Fluoride F^- could not be detected by the x-ray analysis. Elemental Zn and S were easily detected. X-ray analysis of a typical black layer sample exhibited ratio of Zn^{++}/S^{--} (not atomic but proportional) in the order of 10, which clearly indicated extremely high level of Zn concentration. (Conductivity of these films is dependent upon the concentration of free Zn and the linking formation of free Zn as a layer within the ZnS layer.) A decisive conclusion was not reached due to the lack of some absolute reference.

Grain size of the black background film was amplified due to the surface structure of phosphor ZnS. Of course, a 2000A° thick Si_3N_4 film cannot cover a grain size of 2000-3000A° ZnS phosphor film uniformly. The average black layer grain size on a glass surface varies from 1000-2000A°; when applied on the TFEL structure it increased to 2000-3500A°, hence amplifying a dendrite effect. See Figures 4 and 5.

The grain structure of the black layer is rather prominent and well defined. A dendrite type of structure with a round surface also contributes to trap incident light besides the absorption via the band gap process. Preliminary thermal response (post-anneal) of the black layer, in vacuum and air, reveals the

existence of free Zn on the granular surface. At higher temperatures ($\sim 420^{o}C$), the film starts to become transparent--a surface diffusion phenomenon. Absorption of trapped light is maximized at these granular surfaces as these two phenomena are combined in one layer.

Fabrication of the black layer is very sensitive to deposition parameters such as substrate temperature, gas pressure, input power density and target voltages. A slight change of substrate temperature and input power would completely change the electro-optical characteristics of the black layer.

C. Deposition Parameters

The basic source material of the Hycom black layer is ZnS. With any increment of substrate temperature, the sticking coefficient drops drastically at, or more than, $175^{o}C$. Poor adhesion results if the substrate temperature is lower than $150^{o}C$. The substrate temperature must be maintained constant to achieve an acceptable adhesion. Hycom is currently limited with the system sputtering geometry. All the substrates are heated under a heater and then brought under the target for material deposition in the absence of any further external heat source. The substrate temperature rate of cooling is different for different deposition rates, depending upon the energy of the ad-atoms or molecules which are controlled by the input power and voltage. Eventually the substrate temperature reaches a steady state. A substrate temperatue during the deposition of the ZnS phosphor of about $220-240^{o}C$ seems very compatible to maximize all the physio-chemical qualities of the black layer, but the high substrate temperature is not suitable once the second insulator is deposited, due to the mechanical stress exerted on the phosphor film. When the black layer is deposited at a higher substrate temperature ($\geq 250^{o}C$), it tends to create crystal dislocations and hence results in severe burnouts when the EL films are electrically excited.

The concentration of free Zn in the ZnS film is sensitive and selectively dependent upon the concentration of SF_6, input power, voltage and substrate temperature.

In a reactive plasma, the following relationship determines the behavior of the phoenomenon:

$$Q = \frac{KVi_+}{dP}$$

Q	quantity of deposit
V	target voltage
i_+	positive column current
d	substrate-target spacing
P	gas pressure
K	constant

At a constant distance and pressure, the quantity (Q) is dependent upon the voltage of the target which is directly proportional to the input power applied. Hence, the dissociation reaction taking place at the surface of the target is totally dependent upon the input power, SF_6 gas concentration, and the sticking coefficient of ZnS at different substrate temperatures.

Examining Figure 6, it becomes clear that input power (350-600 watts) reduces the resistivity, and lower power increases the resistivity. In the region of 300-400 watts, conductivity changes drastically. A similar effect has also been observed with different SF_6 gas concentrations. The number of free Zn particles in the ZnS film depends upon the number of dissociations which, of course, relates directly to the available SF_6 molecules in the chamber during the deposition. See Figure 7. The black layer also usually becomes shiny in appearance when it is Zn-rich with high conductivity. Films with higher resistance usually appear opaque.

D. Optical Measurements

Under high ambient light conditions, the measurement of TFEL should be broken down into two different parts: first, the emission produced by the energized segment; secondly, reflection of the ambient light from the display surface. It is helpful to consider these two components separately, while at the same time realizing that they should be, and are, additive. Then we arrive at a generally acceptable equation of contrast which is defined as

$$CR = \frac{B_2}{B_1}$$

where

B_1 brightness of unenergized segment (due to internal scattered light and reflected ambient light)

B_2 brightness of energized segment (due to emission and reflected ambient light)

We can also break down this equation into other influencing parameters and then define as

$$CR = \frac{B + A\lambda}{A\lambda}$$

where

B segment brightness without ambient light

A ambient light

λ reflectivity

In a laboratory environment, in order to measure incident light (in foot-candles) upon some point of reference, it is generally agreed that a Lambertian surface with close to 100% reflectance can be used in conjunction with a photometer which measures in foot-Lambert.

Probably the most acceptable material, with a Lambertian surface and characteristics, is $BaSO_4$ which reflects 99 to 100%. Hence, the foot-Lambert reading at the $BaSO_4$ surface can be taken as foot-candles.

The arrangement of the experiment set-up is shown in Figure 10. In this type of experiment, readings are very sensitive to the distance between the photomultiplier and the desired surface, fluctuation of the surface of the display and the angle of incident light. To date, placing the light source at an angle of 45° to the test surface appears most feasible. Another technique, widely used to standardize and obtain absolute values from one laboratory to the other, is an integrating sphere. See Figure 11. In this set-up, impinging light on the display surface is more uniform, rather than unidirectional. The resulting values for contrast will likewise be more uniform. However, this technique would appear unrealistic as the contrast results from direct sunlight falling upon the display which is itself a directional situation.

Table 1 represents the data obtained on new black-layer-coated panels under standardized method using a Pritchard photometer.

In our standardized method, a $BaSO_4$ plaque ($\sim$ 100% D_R) is illuminated with two sun guns located about 2.5 feet an an angle of 45° from the normal surface of the object. The measured, illuminated light is 2500-2600 foot-candles. One-half side of these panels were coated with the black layer and the other half had only the Al metallization. D_R and T_R of the black layer dropped consistently with lower input power at the target and thickness of the film. It has been shown that the black films deposited at the lower input power, $\leq$ 350 watts, possess $\lambda/4$ interference effect due to the dendrite growth. Minima of D_R appear successively at the integral multiples of film thickness. See Figure 10.

$$d = \frac{m\lambda}{2n}$$

d = distance between dendrites
m = 0, 1, 2, 3 ...
n = refractive index 2.3-2.4
λ = 5500° ambient light

As the thickness increases, D_R minima decreases asymptotically further which is attributed to the number of absorbing centers available, which statistically is given by

$$F(x) = \frac{1}{2}\left\{1 \pm \mathrm{erf}\left(\frac{x}{\sigma\sqrt{2}}\right)\right\}$$

x = distance from random point
$\bar{x}$ = 0
σ = standard deviation

The worst case of sunlight readibility is when scattered light impinges upon the display surface from all possible directions. Figure 13 represents typical diffuse reflectance data of different black layers measured with an integrating sphere. Hycom's black layer ZnS:Zn exhibits superior but a dominant interference effect. A black layer must be a good absorbant as well as low reflector. Extremely shiny surfaces usually depict low D_R but high T_R. Erroneous results can be obtained if the T_R of the black layer is ignored, as we noted some panels possessing high T_R but low D_R.

As noted before, the necessity of taking the reflectance measurements on both sides of the panel arises due to the fact of varying grain size and structure of phosphor ZnS:Mn from panel to panel. Panels containing smaller grain sizes at the phosphor layer are inclined toward higher total reflection but lower in D_R. The influence of the rough surface of the ZnS:Mn phosphor must be recognized to determine the effectiveness of the black layer as an absorbant by itself.

E. Electrical Characteristics

Log B vs V: The Hycom black layer can be applied as a good conductor or as a poor dielectric. Application of either type behind the TFEL structure has shown an interesting phenomenon of threshold voltage. We have defined the effectiveness of the black layer absorption at two different stages of the brightness of the active area which is as follows:

1. At threshold:

A. Conductive Black Layer

The threshold voltage (V_{TH}) (Hycom uses the definition of 0.1 ft-L in a dark room) of panels with a conductive

black layer or without a black layer appears at the same voltage. The voltage drop at the junction of the conductive black layer and Al electrode is almost negligible, as no significant potential barrier is formed. The internal scattering at this low level of brightness (0.1 ft-L) is insignificant.

B. Non-conductive Black Layer

At low level emission, no significant absorption is realized but the threshold voltage is higher by 15-25 volts, depending upon the resistivity of the black layer.

2. From knee to saturation region:

The effectiveness of Hycom's black layer becomes apparent in the region of higher light emission. The higher the light emission, the higher the internal light scattering (halation). Figures 12 and 13 show curves of panels with the various process parameters used to achieve a high light absorbant background. Each of these sample panels was made by depositing the black material over half of the panel, thereby allowing a direct comparison of black background to aluminum background.

The absorption characteristics of the black layer being electrically conductive or non-conductive becomes apparent both at threshold and in the saturation region. In Figure 12 for panel 2-8, the threshold voltage for aluminum electrodes and conductive black layer is about the same, but as the light emission of the active area increases at higher voltages, the absorption characteristic starts dominating and the brightness drops rapidly. Similar behavior is exhibited by non-conductive black layer in the saturation region. See Figure 13 for panel 3-2.

F. Chemical Characteristics of the Black Layer

Previously, we have briefly discussed the nature of the black layer applied to the TVD panels. X-ray analysis exhibited a Zn^{++}/S^{--} ratio in the order of 10. IMA analysis performed by Sharp also confirmed the quantitative ratio. See Table 2. High concentration of Zn usually located at the surface of the granular film. The location of Zn sites is very sensitive and susceptible to the reaction with O_2 under high temperature conditions, $\geq 420^{o}C$. The absorption characteristic changes to become an optically transparent film.

The enhancement of the dendrite structure is evolved both due to the excess Zn sites and the rough structure of the previously deposited polycrystalline ZnS:Mn phosphor as shown in Figure 5.

Excess Zn and extremely rough surface of the black layer create a severe problem for the etching characteristics of the back electrode (Al). Zn and Al can both be etched by alkaline and acidic solution. Few selective etchants are developed by Sharp to define Al lines. These solutions have been partially successful as the undercutting of the black layer ranges 15-20% of the width of the Al electrode. As a result, the aluminum edges remain unattacked, while the black layer is etched away under the electrodes. The effectiveness of the black layer absorption characteristic is severely paralyzed. Following are the etchant solutions used for the TVD panels:

1. KOH 5%/KIO_3 40°C (KIO_3 acting as stabilizer)
2. NaOH 5%/KIO_3 40°C

While at Hycom, we concentrated our efforts on a lift-off process; this process flowchart is shown in Figure 14.

The severe undercut of the (Al) electrodes of the TVD panels using etchants is exhibited in Figures 15 and 16. The (Al) electrode spacing is 6 mils. The shiny edges of Al remain slightly etched but electrically conductive. When the panel is electrically excited, these edges deteriorate the contrast ratio, while, on the other hand, the lift-off process has been successfully utilized on 3 mils spacing with extremely high quality of Al electrode resolution. See Figure 17.

G. Life Test

Most of the panels fabricated with the black layer have been subjected to life test under various conditions. The time to half-brightness, measured after a 72 hour burn-in period, varied from 200 hours to more than 500 hours, depending upon the region of operation in the B vs V curve.

After the initial B vs V measurements of a panel, the same panel was burned-in at 50 volts above the threshold with 1280 Hz and 40 μs pulse width. After 72 hours, we call this measurement t = 0 for life test. Most of the brightness degradation appeared during the burn-in period. During the life test period, we maintained similar conditions as of burn-in period. The B vs V characteristics of panels 4-4 and 4-5 are given in Figure 18.

The decrease in the brightness of the saturation region was less than 30% after 700 hours of accelerated operation.

It must be remembered that the life test of these panels was carried out in a dry box filled with $CaSO_4$ pellets to absorb moisture, which is partially effective for a period of less than 400 hours. These pellets do not have the capability of removing and absorbing moisture from the TFEL structure when electrically excited. Most of the failures of the active layer have been due to the moisture, therefore we regard this life test as a more severe life test as compared to one with an encapsulated panel.

H. Further Investigation

The Hycom black layer ZnS:Mn, which is formed in the plasma by reacting ZnS with small quantities of SF_6, is sensitively dependent upon gas concentration, gas pressure, substrate temperature and input power. The reproducibility of this high quality, light-absorbing layer tends to depend upon the gas concentration and the input power. Optical and electrical properties are both dictated by these two parameters. Lower concentration of SF_6, 3.5%, and lower input power, $\leq$ 350 watts, produce extremely absorbant D_R, $\approx$ .75%, but fairly resistive films, $\approx$ 1-10Ω-cm. To avoid any electrical cross talk in the matrix panel, resistivity must be increased to 100-1000Ω-cm. A very fine region of processing parameters exists to produce a high quality, light-absorbing and non-conductive layer.

Recent work showed better control of the deposition parameters and modification of the system has produced high quality, light-absorbing and reproducible films.

Some exploratory work was also performed on the feasibility of applying a ZnTe/Te system black layer with TFEL structure. Preliminary qualitative results indicated overall better performance than the existing system. The tellurium (Te) compound system has been found very attractive for selettive solar absorbants.

Figure 19 exhibits the transmission data of several different materials. In our view, some other possibly good candidates for selective solar absorbant of visible light spectrum are:

1. ZnTe:Te
2. CdTe:Te
3. Si:Al,Ni Amorphous
4. Al_2O_3:Ni
5. ZnTe:CdTe

I. Performance Evaluation of Black Layer

The investigation of Hycom's black layer has been very encouraging and we are optimistic about the reliability and durability of its electro-optical characteristics. Most of the basic qualities of this film have been developed for the use in conjunction with the TFEL structure. Some areas still remain to be investigated to maximize its qualities. We have drawn the following conclusions from our investigations:

1. Hycom's black layer is reproducible with less than 5% of variation (for 3" x 3" area) in regard to thickness, diffuse reflectance and conductivity.

2. The average diffuse reflectance of the TFEL films with Hycom's black layer at 2500 ft-C is about 1-2.5%. Minimum D_R has been reported at 0.75% (without any AR coating at air/glass interface).

3. Hycom's black layer can be produced as a good conductor or a poor dielectric. To be used as a good conductor it must be coated with Al and a suitable selective etchant must be developed to avoid any undercutting. For a poor dielectric, more investigative work is needed to increase the bulk resistivity from 50Ω-cm to $\geq 10^3$Ω-cm to be applied effectively in the TFEL structure.

III. CIRCUITRY

This report describes and analyzes the design of EDM-32, a breadboard, which was built to test the feasibility of the new drive and scanning scheme for the Tactical Video Display Contract, Phase I.

This report is organized as follows: first, the uses of EDM-32 are summarized; next, the breadboard is described physically and operationally; the final section presents the evaluation studies performed so far.

EDM-32 became operational July 16, 1980. Since it was designed to be primarily an evaluation tool, studies will continue which contribute toward the completion of Phase II of the TVD Contract.

A. Purpose of EDM-32

1. Match panel characteristics and drive parameters for optimum performance.

2. Evaluate design approach for drive and scanning circuitry.

3. Re-evaluate TVD design goals; tailor to best represent the needs of the program.

4. Test integrated chips (from Supertex) in a "real" environment and allow chip performance comparisons with discrete version.

B. Physical Description

EDM-32 comes in two parts: the panel, and the drive/scanning electronics. This report describes the drive/scanning electronics; the panel is discussed elsewhere. The electronics assembly consists of six (6) power supplies and ten (10) circuit card assemblies. The only input required for EDM-32 is 110 volt AC. Several switches are included on a front panel to enable the user to select various shades and patterns for test and demonstration purposes. The system's basic clock rate and number of lines per frame is also selectable, but only by removing circuit cards from the EDM-32 assembly and changing DIP switches.

From the EDM-32 electronics assembly, four cables supply the necessary signals to light the panel. These four connectors are designated as Even Column, Odd Column, Even Row and Odd Row. Each connector has 16 pins connected for a total of 32 rows and 32 columns. Since the panel consists of 512 rows x 640 columns, an adapter, which connects each row output to 16 other rows and each column output to 20 other columns, was utilized during the evaluation studies.

C. Circuit Details

As shown in Figure 20, the EDM-32 electronics assembly is subdivided into eight (8) functional blocks. Each of these 8 functional blocks will now be briefly discussed. The Power Supply Block has as its input 110 volt, AC and outputs +48 (adjustable to +60 volt), +200 volt, -200 volt, -15 volt and +5 volt. The ramp and clock generator board outputs the data clock and count clock whose periods are independently selectable from 10 ns to 26 μs. Also, this board outputs a ramp waveform which is slaved to the count clock rate and stepped in accordance with an EPROM program. There is room for 64 programs in the EPROM; different programs can be selected by a DIP switch. The controller board utilizes the data clock from the ramp and clock generator to output control pulses for all the other functional blocks. On the controller is a DIP switch to allow selection of the number of lines per frame from 64 to 4,096. The pattern generator receives its inputs from the switches on the front panel and generates the column counts (0-15) which are loaded into the column shift registers for each line. The ramp driver uses the 0 to 50 volt ramp output from the ramp and clock generator and outputs a 0 to 50 (approx.) volt ramp waveform to load the 32-column driver sample and hold circuits. The column driver requires four circuit boards on EDM-32. The two digital boards control the pulse width of the sampling waveform as determined by the pattern generator outputs. The two analog boards contain sample and hold circuits. The outputs of the column drivers go directly to the electroluminescent panel. The substrate driver puts out 32, -200 volt negative going pulses and 1, +200 volt positive going pulse per each frame. The timing of these pulses is controlled by signals from the controller board. The substrate driver also contains a +5 volt floating supply to power the digital row control logic. Finally, the row driver board contains digital and analog circuitry to select when each row sees the +200 volt and -200 volt pulse outputs from the substrate driver.

In order to cause the panel to luminesce, the drive scanning circuitry must produce only two types of outputs--the column drive and the row drive. It is the instantaneous differential voltage between the row/column intersection (pixel) which causes the luminescence. The following discussion used in

conjunction with Figure 23 elucidates how this is done. The column driver utilizes the output of the ramp driver, and the row driver uses the output of the substrate driver, so each of these circuits are discussed in separate sections.

Ramp Generation and Drive

The ramp waveform is generated by using 32 8-bit values programmed in an EPROM to control the output of an 8-bit digital-to-analog converter (DAC). This allows the flexibility of tailoring the shade of the ramp to produce linear increments of brightness for the 16 shades. The output of the DAC only extends from 0 to -5 volts, so it is amplified and inverted by the ramp driver circuit to a 0 volt to 40 volt signal. Improvements are needed in the ramp driver circuit to extend its maximum closer to +60 volts.

Column Driver

Every line time, the 32-column shift registers (see Figure 22) are loaded by the 32 shift clocks using the data from the pattern generator. At the beginning of the next line, the function, Column Load Bar/Shift, strobes the data from the loaded column shift registers into the column counters (see Figure 22). Utilizing the count clock, the column counter outputs a pulse whose width is determined by the value loaded from the pattern generator. This variable pulse width signal, called Column State in Figure 21, opens up a window in the analog column sample and hold type circuit shown in Figure 22. The sample and hold circuit samples a ramp waveform from the ramp driver as shown in Figure 21 and the result is a ramp whose height is controlled by the pulse width of the column state signal. This output ramp (actually there are 32 of them) goes to the column driver input of the panel.

Substrate Driver

A schematic for the substrate driver is shown in Figure 23. The 4 MOS FET transistors in this circuit act as 4 switches to pull the substrate output to either +200 volt, -200 volt, or ground. The timing of the substrate drive

waveform is determined by 4 pulses from the controller board. The sequence is as follows: first, Scan Pulse (see Figure 19) turns Q1 on pulling the output to -200 volts. Then Scan Reset turns Q2 on and pulls the output back to ground. This repeats 32 times (32 scan lines). At the end of the scan time, Refresh Pulse causes Q3 to pull the substrate output to +200 volts. Finally, Refresh Reset turns Q4 on to return the output to ground. The resultant substrate drive waveform is shown in Figure 21.

The following are a few miscellaneous observations concerning the other components of the schematic. The digital signals which control these transistors are coupled via a pulse transformer to isolate them from the +200 volt swing on the transistors outputs. The diodes on Q2 and Q4 prevent these transistors from being damaged by the reverse voltages they would otherwise see. The local capacitor storage at Q1 and Q3 are to provide the instantaneous current that is needed to drive the load to +200 volts or -200 volts. The series resistors, R1, R2, R3 and R4 in combination with the slow-down capacitor C3 were necessary to slow the rise-fall time of the output. The reason for this will be discussed later.

Row Driver

Figure 24 shows the configuration of the row driver circuit. The ground for both the analog and digital portions are attached to the substrate driver output. The +5 volt required for the digital portion is supplied by the +5 volt floating power supply.

At the beginning of each frame, a logic 1 is loaded into the left and right scan shift registers. The enable (right) pulse permits this logic 1 to turn on 1 row driver transistor and pull that 1 row drive output to -200 volts. After that output is returned to ground, the left enable pulse turns its corresponding row driver output to -200 volts. Next, the scan shift register is clocked once and the same process repeats for the next row drive output. At the end of the scan period, all the row drive outputs are pulled up to +200 volts simultaneously and then returned to ground by the refresh signal.

D. Design Evaluation of Drive Circuitry

The TVD Technical Guidelines outlined 6 goals relevant to the drive/scanning circuitry for Phase I.

1.	Legibility Conditions	1.5:1 with 10,000 fL ambient light
2.	Shades of Gray	4
3.	Luminance Uniformity	Unspecified
4.	Dimmability	10^{-3} fL
5.	Power Consumption	15 watts
6.	Lifetime	>3,000 hours

In the following discussion, each of these goals will be separately discussed. Of course, as always is true, these goals are interrelated and so conclusions in one area are influenced by the results in another. Also, it must be kept in mind that several important conceptual changes have been made to the Phase I design approach (replacing hybrids with integrated chips) and thus, EDM-32 is radically different from what it was originally intended to be.

1. Legibility

What has been achieved so far is a maximum brightness of 22.3 fL and a maximum contrast ratio (shade 15 divided by shade 0) of 19.2:1 in a darkened room ($\sim$ .1 fL of reflected light). The following discussion will detail what has been done to optimize this goal so far.

Optimizing Scan/Refresh Voltage

The first effort required to optimize the legibility was to determine the best combination of scan (v_s) and refresh (v_r) voltage supplies. Figure 27 shows the brightness level for two different refresh supply voltages (+ 150 volts and +180 volts). Several observations are relevant. First, notice the brightness is related to the sum of the refresh pulse voltage and the scan pulse voltage. Thus, the brightness is the same for v_r = 180 volts, v_s = 150 volts, and v_s = 180 volts, v_r = 150 volts. This condition was consistent for other values of v_r and v_s measured. It should be noted, however, that when v_r or v_s became too large, v_r > 180 volts or $|v_s|$ > 200 volts, lines started burning out on the panel.

In general, it seemed best to make $|v_s| > v_r$ by a small (10 volt or 20 volt) margin. The best combination for v_r and v_s will also be a function of which combination gives the longest lifetime.

Next, note the saturation condition at the higher brightness levels. That is to say, the contrast ratio (shade 15 brightness divided by shade 0 brightness) decreases at the higher brightness levels, or, another way of looking at it is that the curves flatten out.

Modulation Voltage

The present column driver modulation scheme has two problems. First, it only has a range of 30-34 volts; secondly, the modulation (ramp) driver does not respond fast enough for the 20 μs line times required for TVD Phase II.

Figure 26 shows the voltage range of a typical column driver. The voltage range is only about 35 volts. This is a function of three phenomena. First, as shown in Picture 1, the V_R-V_D is the signal from the ramp driver board to the analog column driver board which changes the capacitor in the column driver. Thus, even with no voltage drop internal to the column driver, this is the best column drive voltage possible. Note that V_R-V_D will not be needed on the integrated chip version of TVD (Phase II); V_R can be used instead. Second, the minimum measured voltage is 2-5 volts. This is because the drive transistors on the column drivers do not completely turn off. This is also not expected to be a problem in the integrated chip version where the drive transistors (MOSFETS) will be designed for our application. Finally, the third factor contributing to the loss of voltage range of the column driver is due to timing. Because the response time of the ramp generator is so slow, the column state pulse (reference Figure 23) which controls the sample window of the ramp wave form is not properly located with respect to the ramp. Note from Figure 29B that for shade 1 the column state pulse is located where the previous lines V_R-V_D wave form is still decreasing! This situation could be improved by delaying the column state pulse, but the better solution is to speed up the V_R-V_D waveform Improving the response time of the V_R-V_D waveform will take care of one other problem. The V_R-V_D waveform never returns to 0 volts even though the EDM-32 is presently adjusted for a line time of 53 μs (remember that for Phase II this line time must be 20 μs). Improvements on the ramp driver are necessary for these reasons.

Dimming Anomaly

An unexpected anomaly was observed with regard to total panel brightness. When all row connectors were connected the brightness of the panel decreased considerably. Even though this is a somewhat unrealistic condition (when all row connectors are installed, each row driver is connected to 16 panel rows), it was deemed important to understand this anomaly.

The first correlation which was observed was that the dim panel condition corresponded with a narrower scan pulse (see Figure 28A and B). The top trace of Figure 28A shows the current waveform. Ideally the current waveform on the falling edge would be exponential like that on the rising edge. Apparently, something was limiting the current to about 150 ma.

Several circuit modifications were tried to develop an understanding of this problem. During the course of the investigation it was determined that the current limit was not because the power supply bypass capacitors did not hold adequate energy. This problem is still not fully resolved, but at this point it seems that the slow rise time can be attributed to two causes: one, the drive to the row transistors is not adequate to turn them on fast enough. This was corrected by adding pull-up resistors to the gate of the row driver transistors. Figure 28 shows the row waveform after the pull-up resistors were added. Secondly, the output of the substrate driver has a 200Ω series resistor to slow down the substrate's rise time (necessary because the substrate drive transistors were overheating). This resistor limits the current.

The reason this 200Ω resistor was added will now be explained. The substrate driver is very simple and elegant in concept. As shown in Figure 23, there are 4 transistors. Refer to the operational description for how this circuit works. The resistors R1-R4 and slow-down capacitor C3 were added to slow down the rise/fall times of the substrate waveform because capacitive coupling was causing the transistors to fight each other during transition times. Since the coupled current, $i = C(dv/dt)$, is a function of the transition time, decreasing this time was necessary.

One solution, not yet tried, is simply to increase the capacitance of C3 by, say, x5 and decrease the series resistors by the same factor.

2. Shades of Gray

Sixteen shades have been demonstrated on the EDM-32. As was explained in the Operational Description part of this report, the individual shade brightnesses are determined by the shape of the ramp driver waveform. Because the ramp driver needs to be improved first, little work has been done on testing the brightness ratios and spacing of the gray shades.

3. Luminance Uniformity

For EDM-32 no uniformity requirements are specified. However, for Phase II, it is desirable to aim for 20% or better. Therefore, uniformity measurements have been performed and are displayed in Figure 31 for the column-to-column brightness. (No measurements have yet been made on row-to- row brightness.)

So far there is not adequate correlation between the measured brightness levels and the column drive voltages (Figure 32). However, several observations can be made in this area. Notice from Figure 31 that brightness levels seem to alternate. This is because the measurements were taken near the top of the panel much closer to the even column connector than the odd column connector. This alternating line problem is a known function of the panel, not the drive scheme. The panel on which these measurements were made has many burnt-out and partially burnt-out lines. This explains some of the non-uniformity.

4. Dimmability

Two methods can be used to dim the display. One is simply to reduce the refresh and scan voltage levels; the other is to slow the frame rate. The present frame period is about 10 ms, so even though the human eye integrates light at lower speeds, this can only be slowed down to 100 ms. No experiments have yet been performed in this area on EDM-32. Experiments have been performed on panels using a non-multiplexed drive and are presented in other reports.

5. Power Consumption

Because the concept of EDM-32 has been changed since the contract was written, the 15-watt power goal does not directly apply to EDM-32. However, some experiments are in process to determine the power usage of the various subassemblies.

6. Lifetime

This parameter is primarily a function of the panel's characteristics, not the drive scheme. However, the drive scheme must minimize heating problems to maximize this parameter. One practical way to do this is to minimize any DC offsets. An effort to decrease the offset voltage between scan pulses is in process.

IV. CONCLUSIONS

The development work done during Phase One of this program has advanced the state-of-the-art in thin film electroluminescent panel fabrication and driver circuitry on a continual basis. The working into the design of the system, each new advance in fabrication or drive technique has caused some slowing of progress towards the end deliverable item but we feel the end product is very much worth the wait.

The diagrams and text of this report describe a drive technique that incorporates almost everything that we feel is important in creating the ultimate drive scheme as it is understood today. The panel and black layer performance measures up quite favorably with other existing efforts, especially when the efficiency of multiplexed drive and the high resolution is considered. The black dielectric layer described here is very thin to avoid an excess voltage drop in the panel and very uniform to avoid even small imperfections that could cause a failure of the very narrow row of column lines used to achieve this resolution.

V. EFFORTS FOR NEXT QUARTER

During the next quarter our effort will be to fabricate additional TVD panels with black layer using the improvements developed in the preceding two quarters.

The circuitry effort will consist of receiving the first monolithic driver chips from Supertex and building them into the system previously described as exploratory development model number one. This system is made with the driver chips in conventional 40 lead dual-in-line packages that will be inserted into wire wrap sockets and cabled to the panel. This system will be capable of RS170 (live television) input and will display 16 shades of brightness over the full 512 by 640 panel.

TABLE 1

ELECTRO-OPTICAL CHARACTERISTICS

Sample No.	Nucleation Surface	P_{in} (Watts)	Thickness (KÅ)	T^*_{sub} (°C)	Adhesion	DR** (%)
3- 4	TFEL	400	--	340	Excellent	1.4
3-10	"	400	4.0	340	Excellent	1.4
4- 1	"	275	3.0	350	Good	1.0
4- 2	"	350	2.4	350	Good	2.3
4- 4	"	450	3.3	350	Excellent	1.4
4- 5	"	550	4.5	350	Excellent	2.1
5- 1	"	400	4.5	330	Excellent	5.8
5- 2	"	350	1.6	330	Excellent	3.01
5- 3	"	400	2.3	330	Excellent	4.5
5- 9	"	350	2.3	330	Excellent	2.69
5-10	"	400	--	330	Excellent	2.40
5-11	"	300	2.2	330	Excellent	3.31

NOTE: Batch no. 5 has higher DR values due to the lower SF_6 gas concentration.

* Substrate temperature recorded at heater thermocouple.
** DR measured with Pritcherd.

TABLE 2

X-RAY ANALYSIS AND SEM OF BLACK LAYER

Sample No.	Structure	Zn^{++}	S^{--}	F^{-}	Zn^{++}/S^{--}	Grain Size Black Layer
1	On glass substrate	19861	1620	Undetectable	12.2598	1350Å
2D	" " "	15536	1684	"	9.2256	2000Å
2L	" " "	24726	1920	"	12.8781	1800Å
3-7	On TFEL structure	13682	8651	"	1.5815	2100Å
3-8	" " "	15840	7562	"	* 2.094	2400Å
3-10	" " "	10982	4108	"	2.6733	2500A

*Low due to ZnS phosphor.

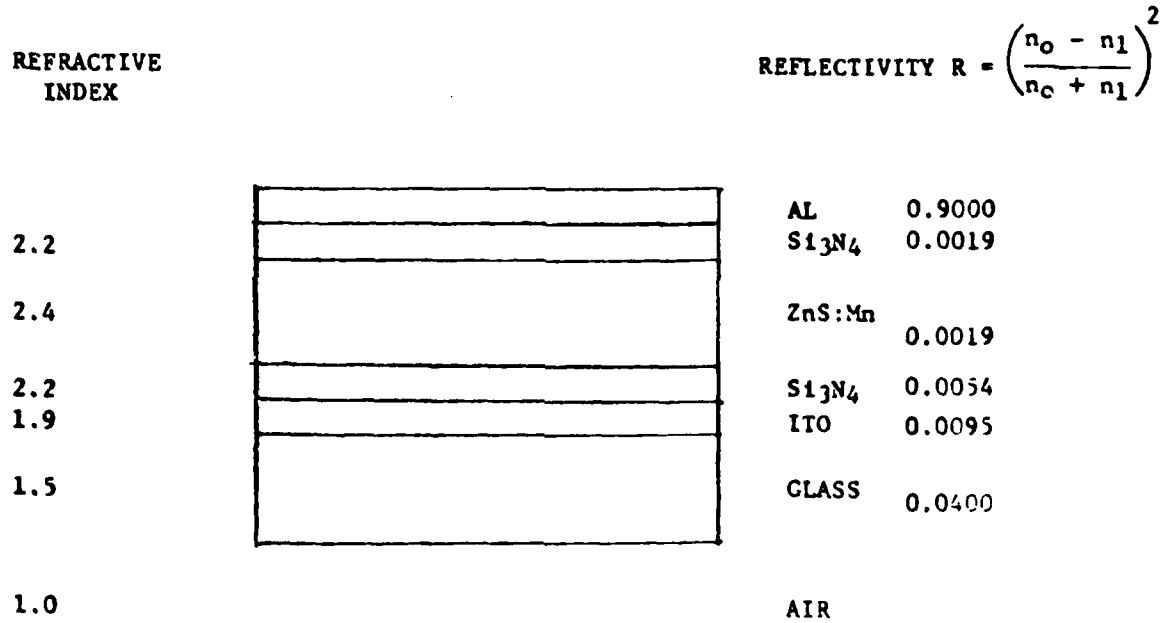


FIGURE 1

PANEL CROSS-SECTION AND INTERFACIAL BOUNDARIES

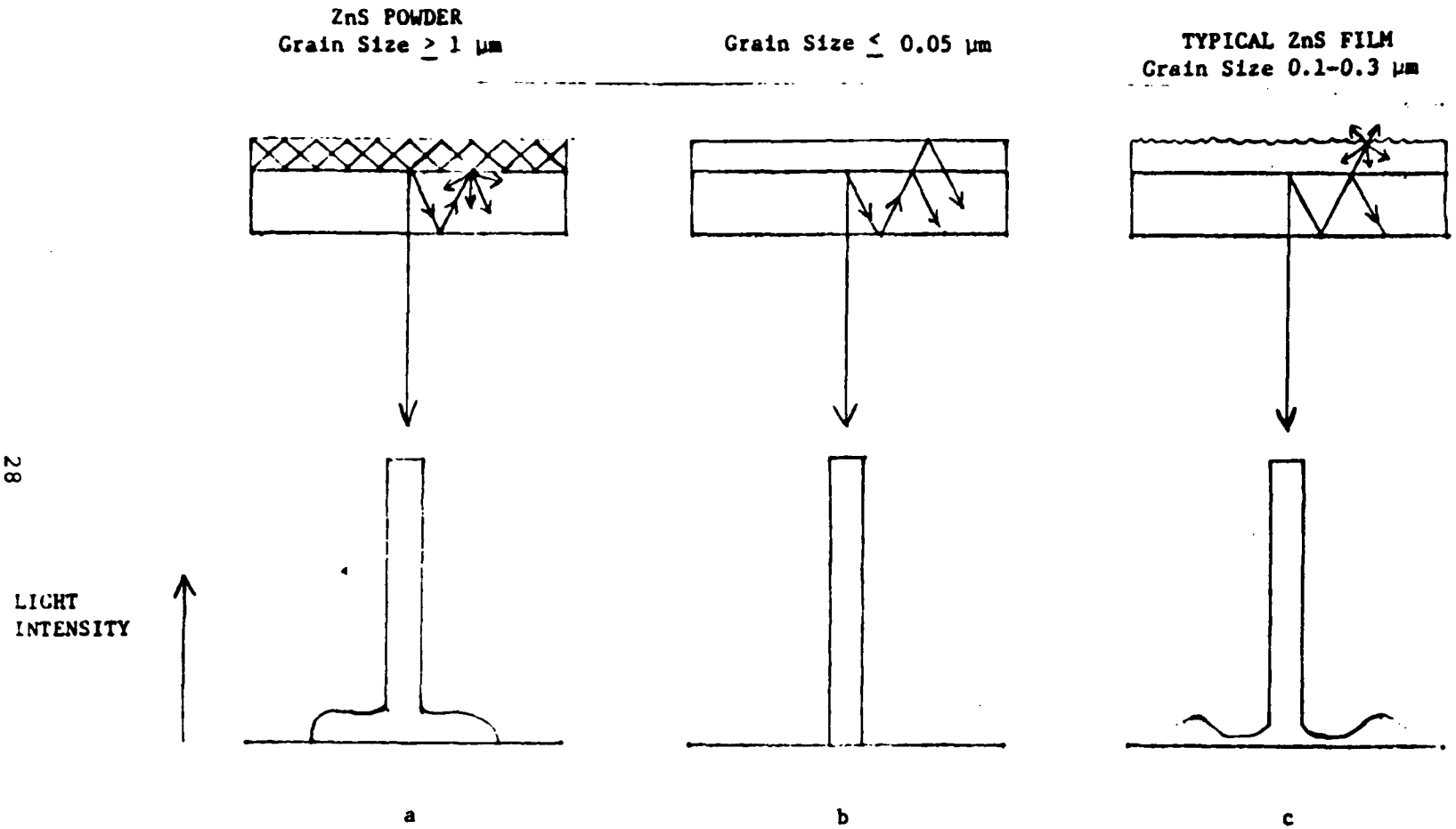


FIGURE 2. INTERNAL LIGHT SCATTERING PATTERN

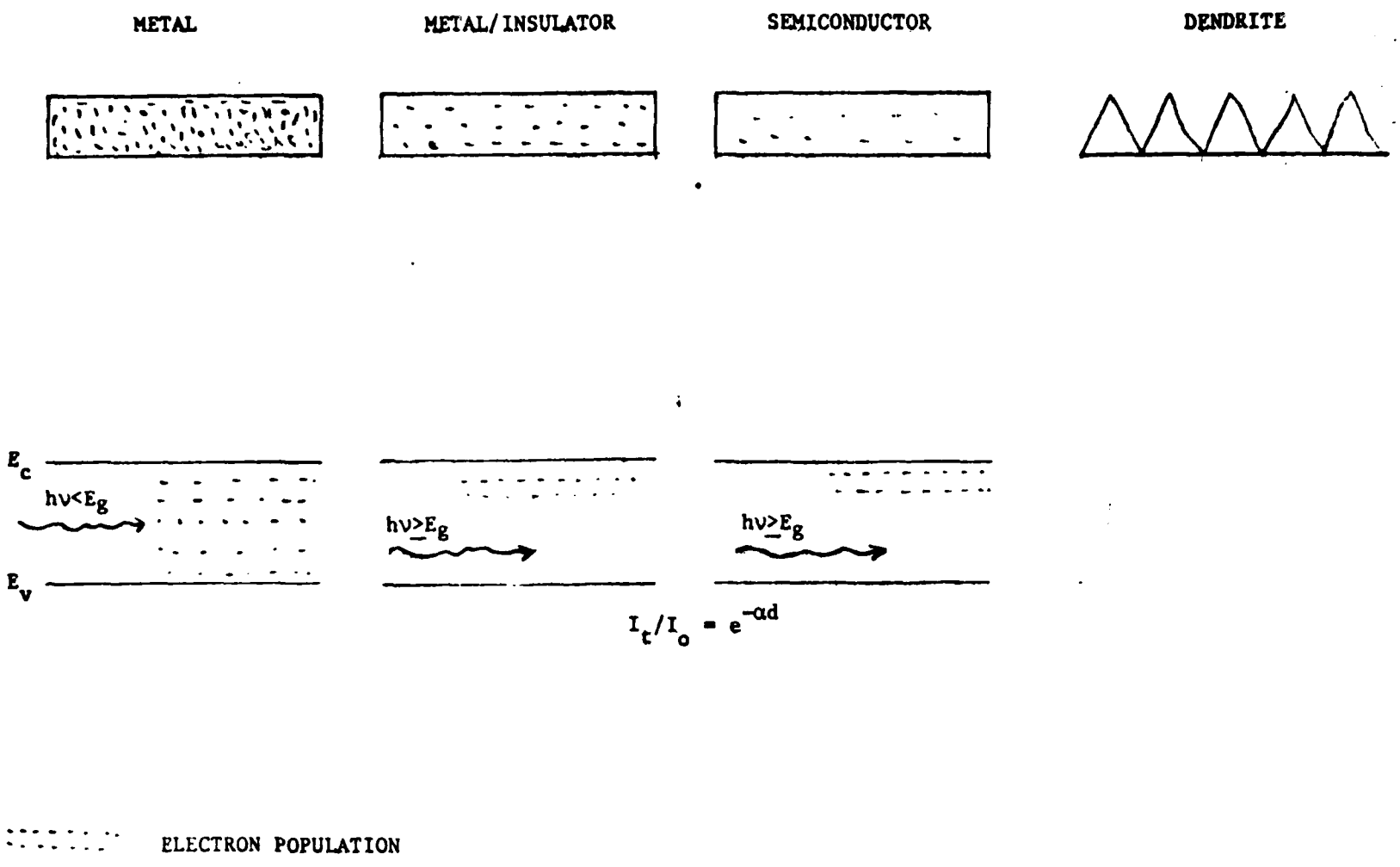


FIGURE 3

REPRESENTATIONS OF LIGHT ABSORBERS

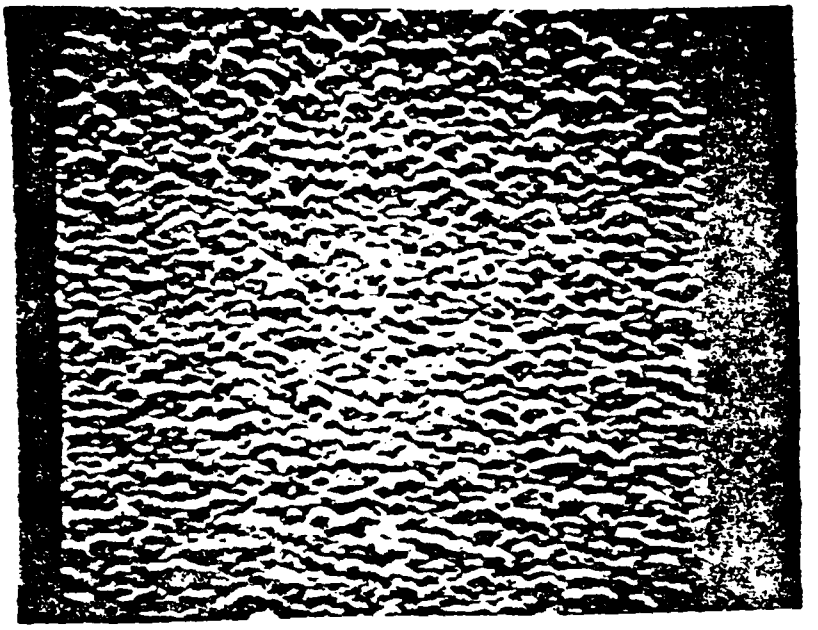


Figure 4

Black Layer on Glass

P_{in} = 400 W

T_{sub} = 230°C

Grain size = 2000Å

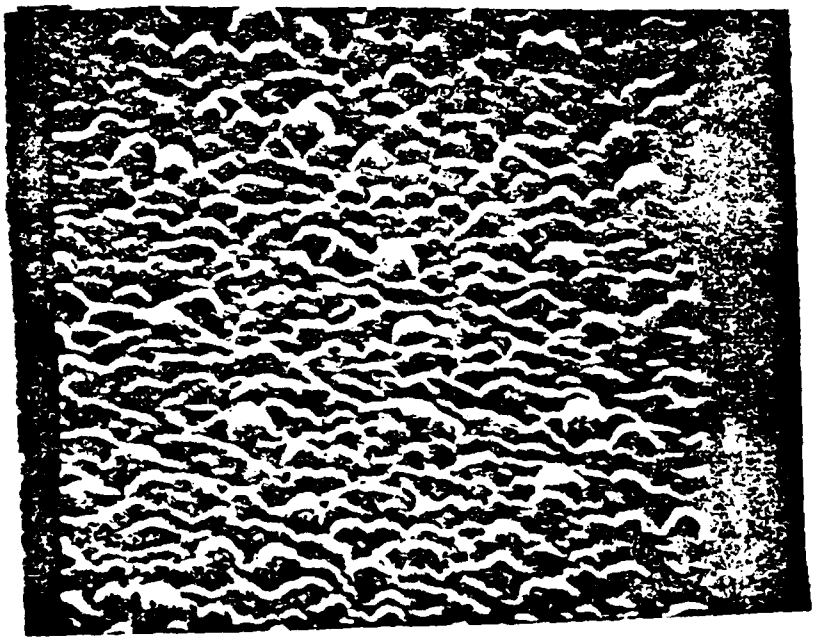


Figure 5

Black Layer on TFEL

P_{in} = 350 W

T_{sub} = 230°C

Grain size = 2400Å

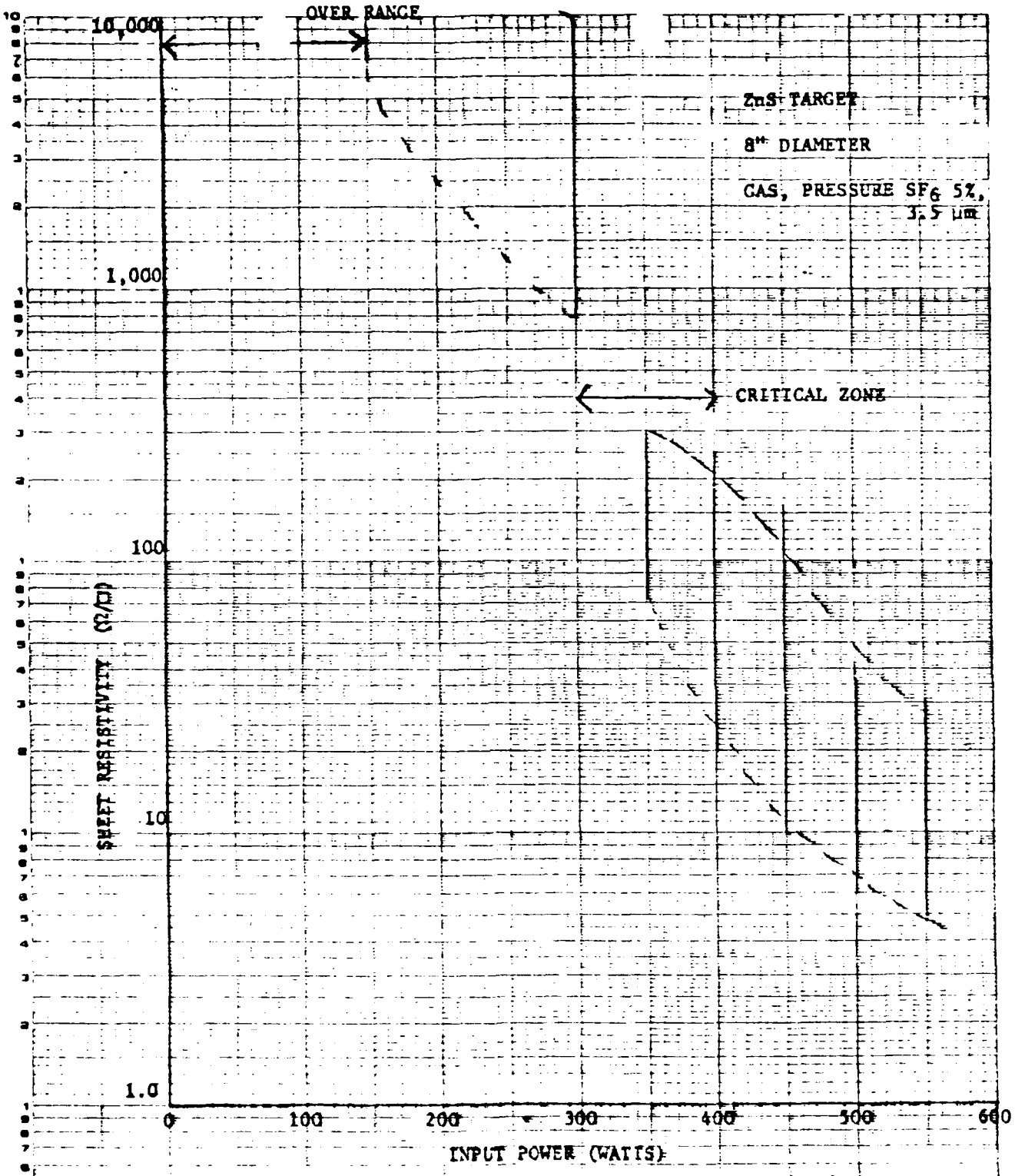


FIGURE 6

SHEET RESISTIVITY VS INPUT POWER

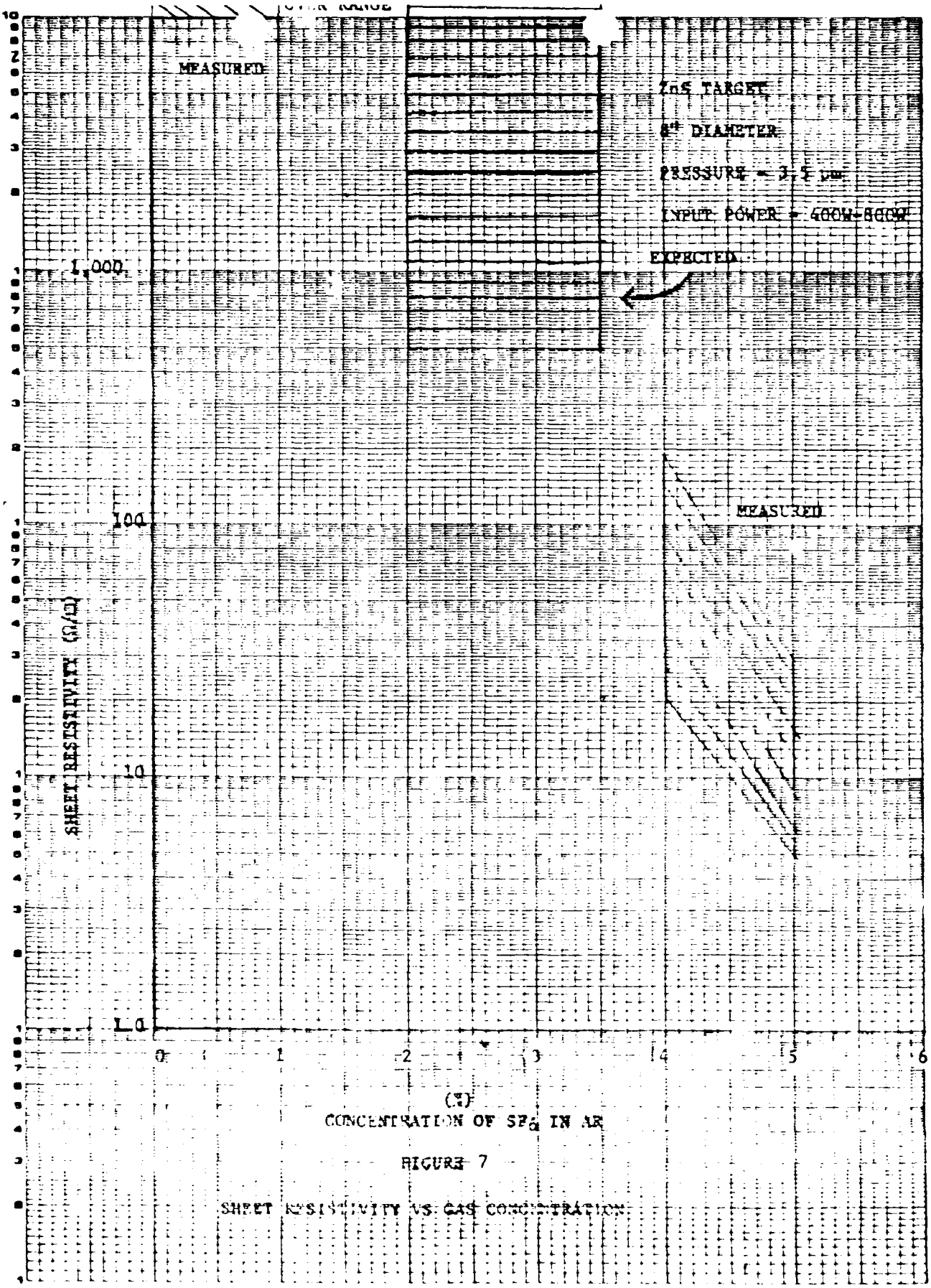
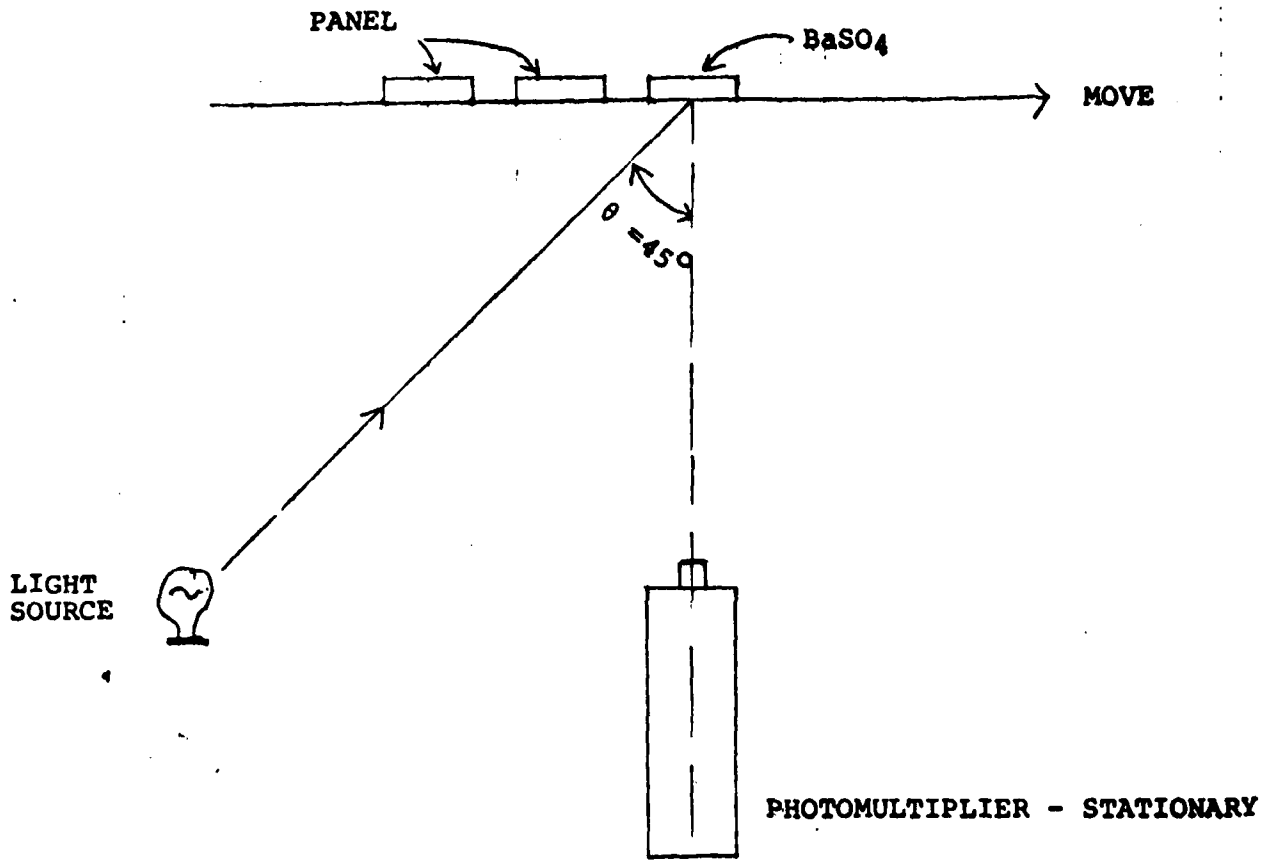


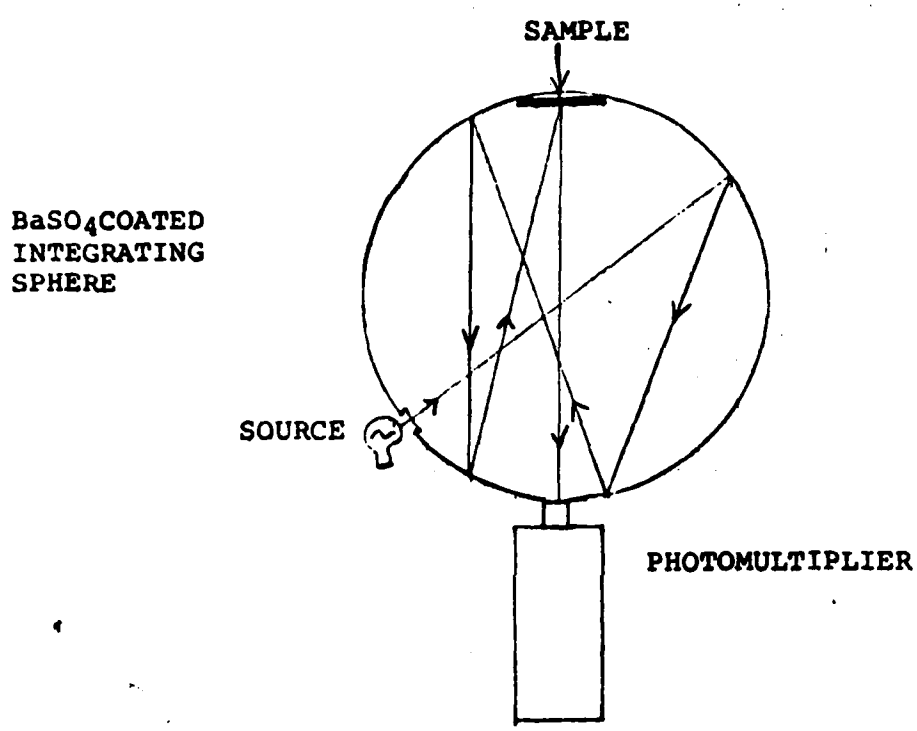
FIGURE 7

SHEET RESISTIVITY VS GAS CONCENTRATION



DIFFUSE REFLECTANCE SET-UP

FIGURE 8



DIFFUSE REFLECTANCE SET-UP WITH INTEGRATING SPHERE

FIGURE 9

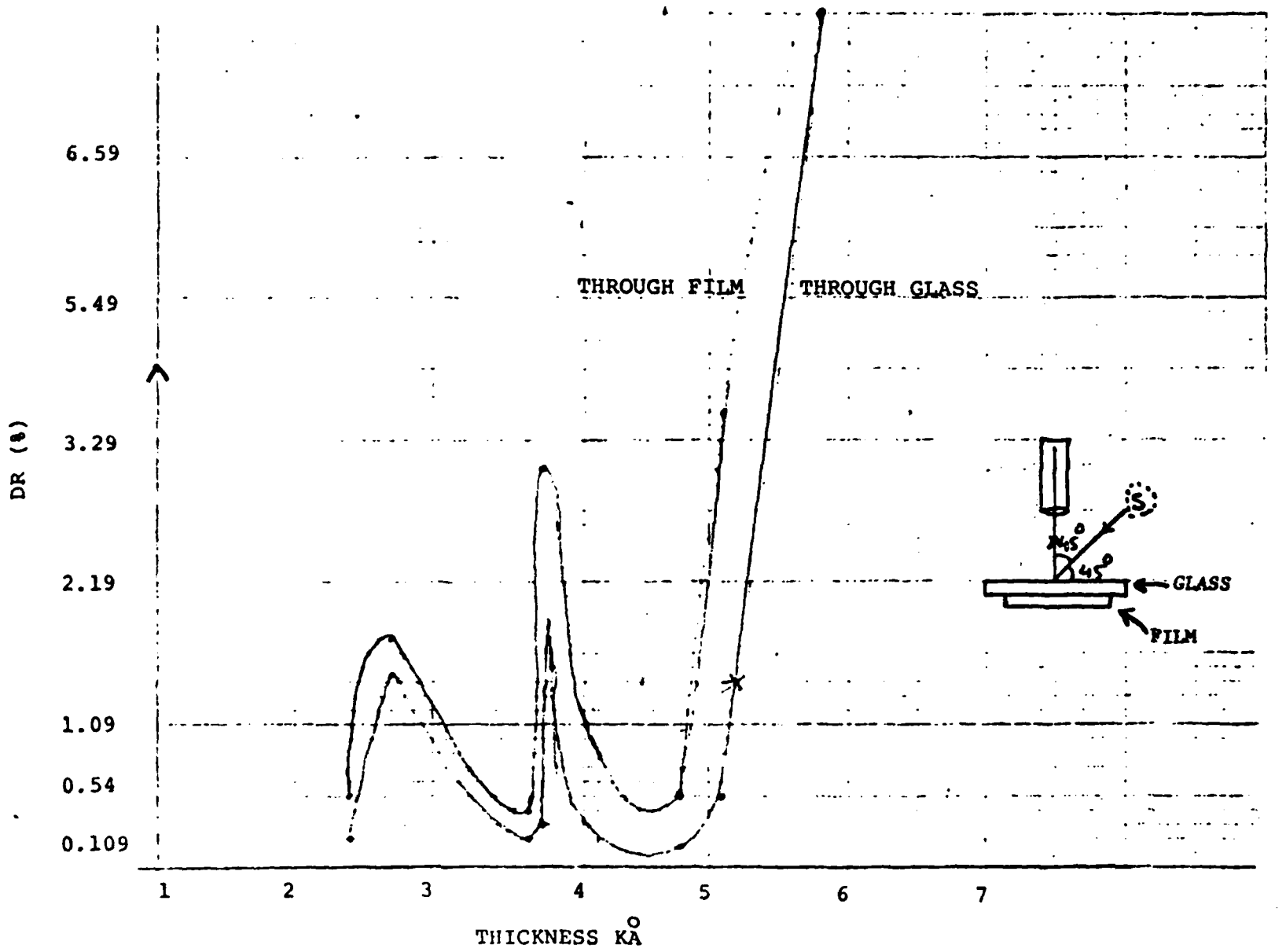


FIGURE 10
REFLECTANCE AS A FUNCTION OF THICKNESS

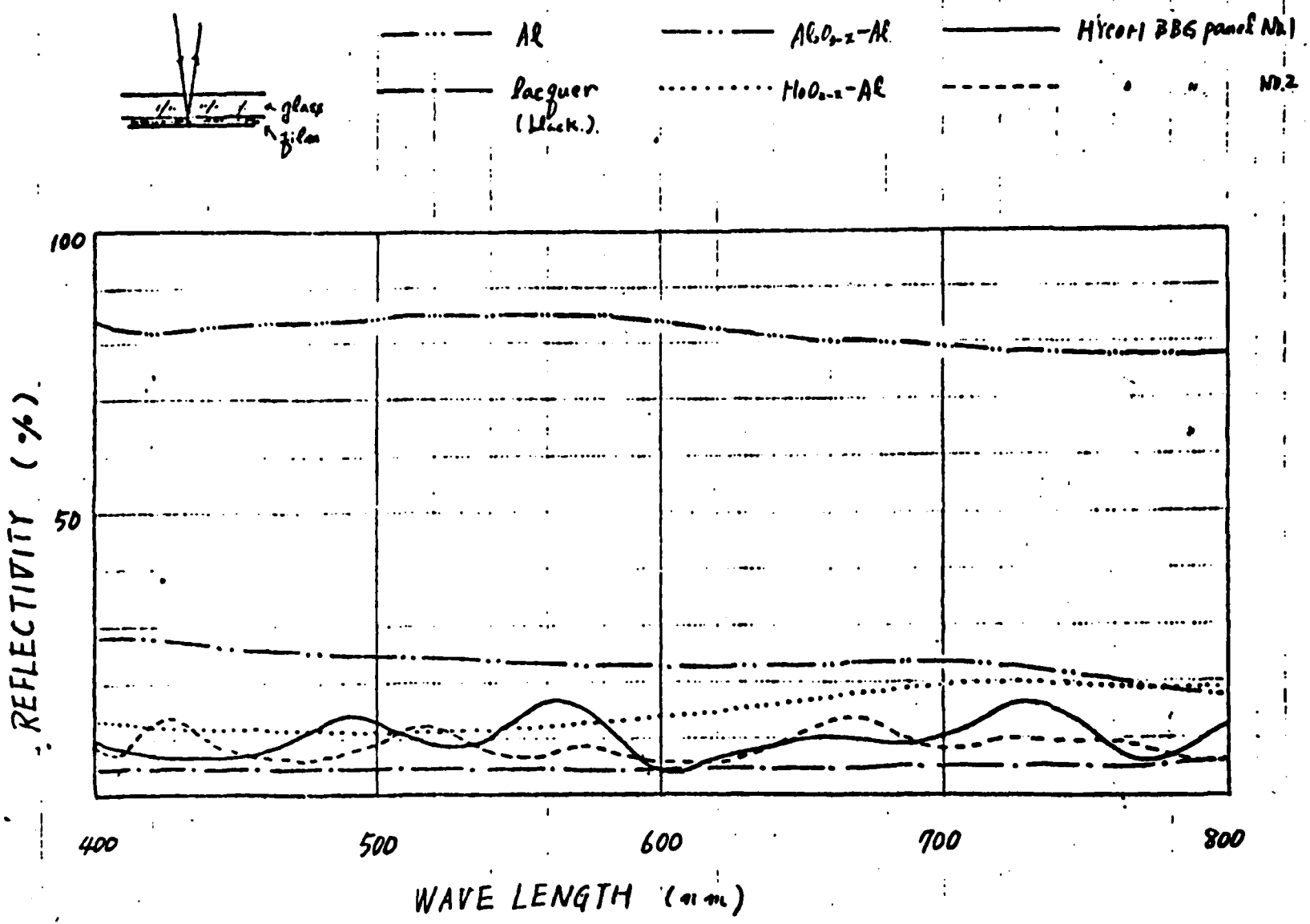


FIGURE 11

REFLECTANCE AS A FUNCTION OF WAVE LENGTH

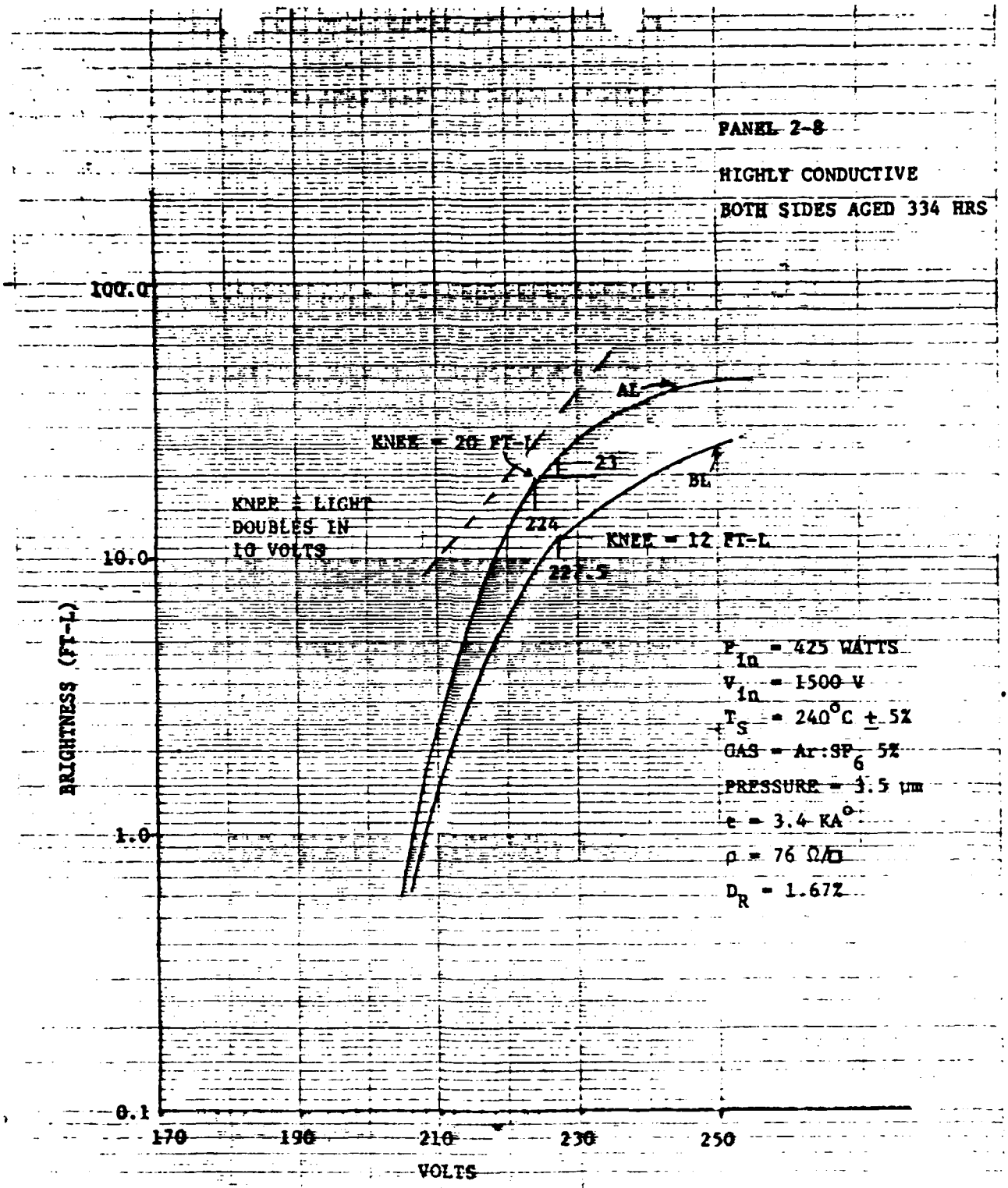

PANEL 2-8
HIGHLY CONDUCTIVE
BOTH SIDES AGED 334 HRS
100.0
10.0
1.0
0.1
BRIGHTNESS (FT-L)
AL
BL
KNEE = 20 FT-L
KNEE = LIGHT
DOUBLES IN
10 VOLTS
KNEE = 12 FT-L
224
227.5
P_{in} = 425 WATTS
V_{in} = 1500 V
T_S = 240°C ± 5%
GAS = Ar:SF_6 5%
PRESSURE = 3.5 μm
t = 3.4 KA°
ρ = 76 Ω/□
D_R = 1.67%
170
190
210
230
250
VOLTS

FIGURE 12

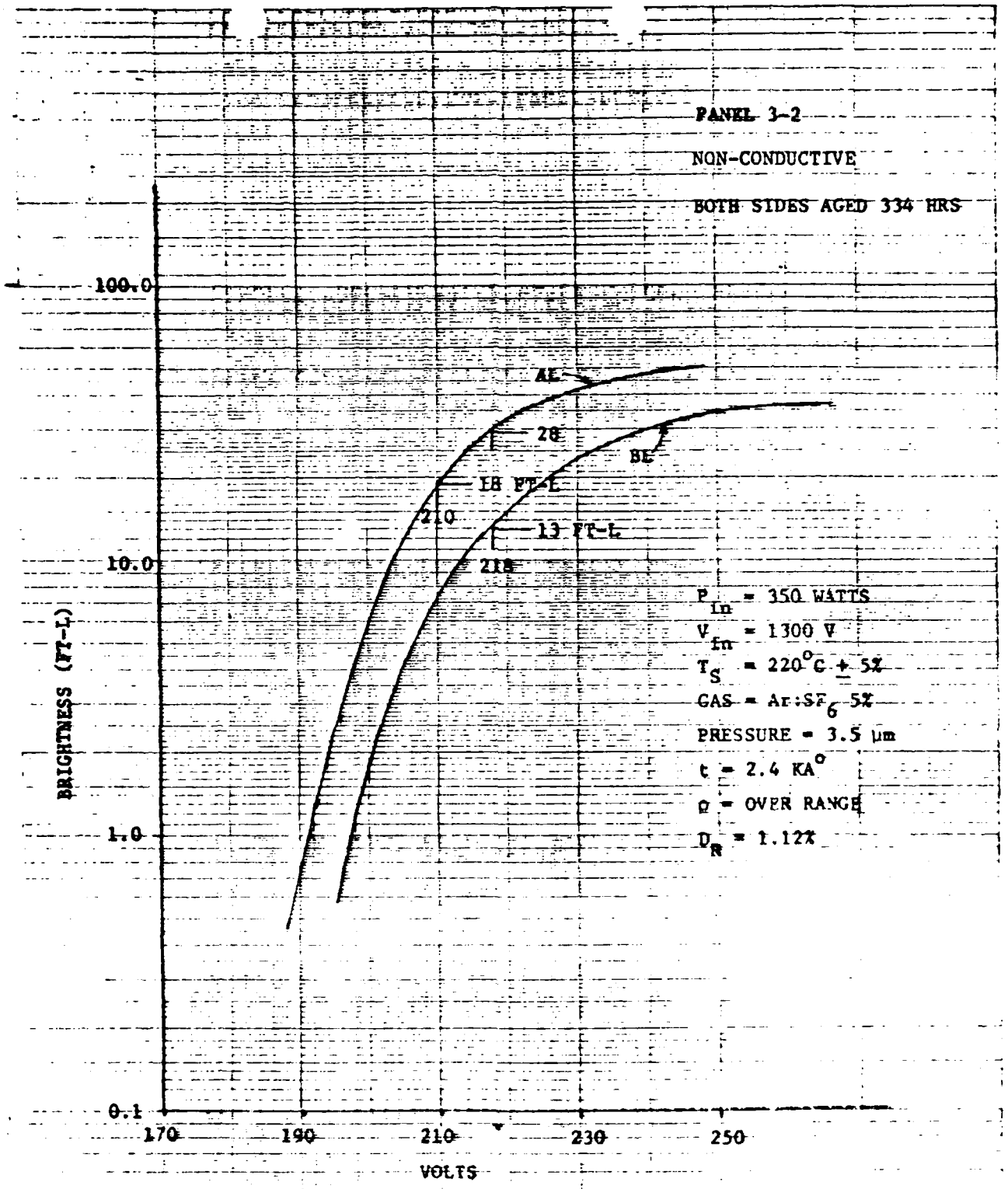

PANEL 3-2
NON-CONDUCTIVE
BOTH SIDES AGED 334 HRS
100.0
10.0
1.0
0.1
BRIGHTNESS (FT-L)
AE
28
BE
18 FT-L
210
13 FT-L
210
P_{in} = 350 WATTS
V_{in} = 1300 V
T_S = 220°C ± 5%
GAS = Ar:SF_6 5%
PRESSURE = 3.5 μm
t = 2.4 KA°
Ω = OVER RANGE
D_R = 1.12%
170
190
210
230
250
VOLTS

FIGURE 13

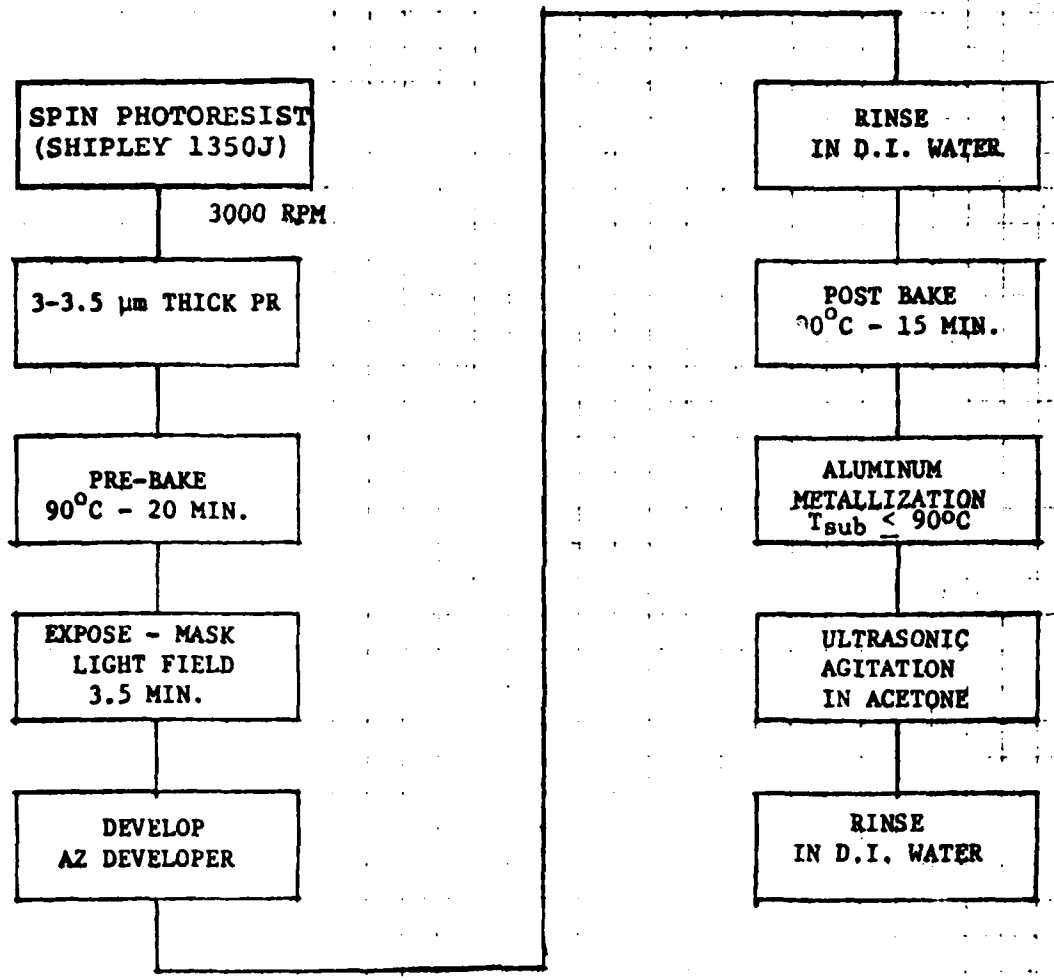
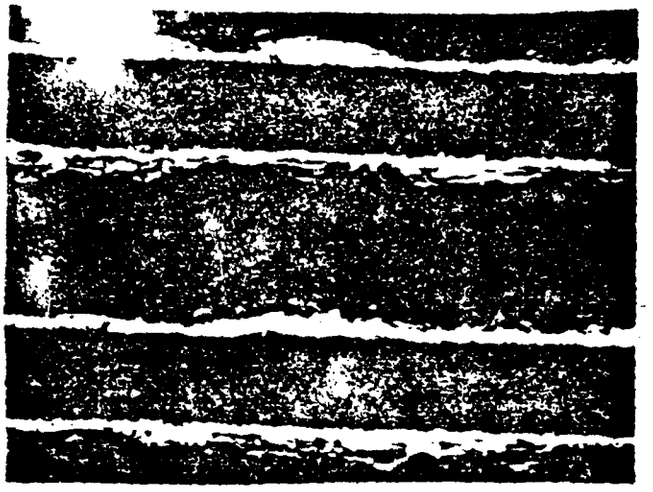


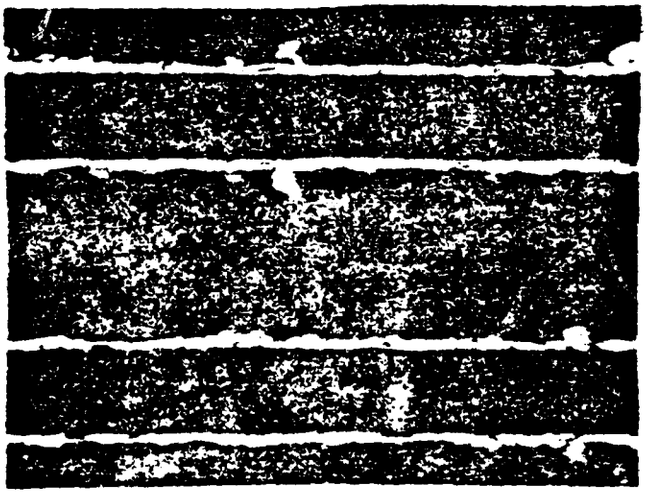
FIGURE 14. LIFT-OFF PROCESS FOR BACK ELECTRODES (ALUMINUM)



6 MIL

FIGURE 15

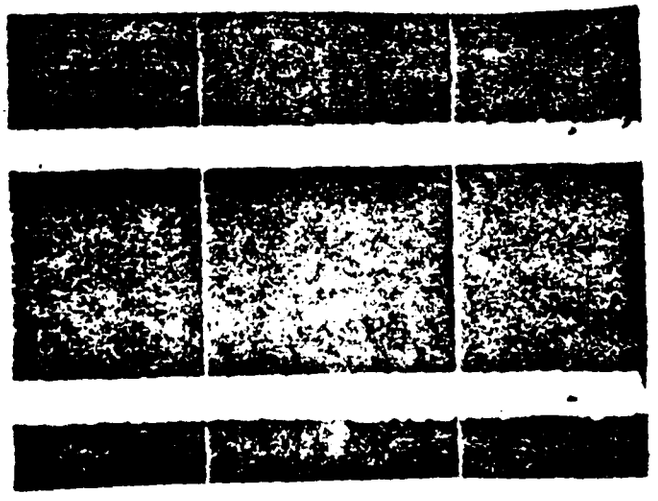
TVD BLACK LAYER ETCHED



6 MIL

FIGURE 16

TVD BLACK LAYER ETCHED



3 MIL

FIGURE 17

LIFT-OFF PROCESSED CONDUCTORS

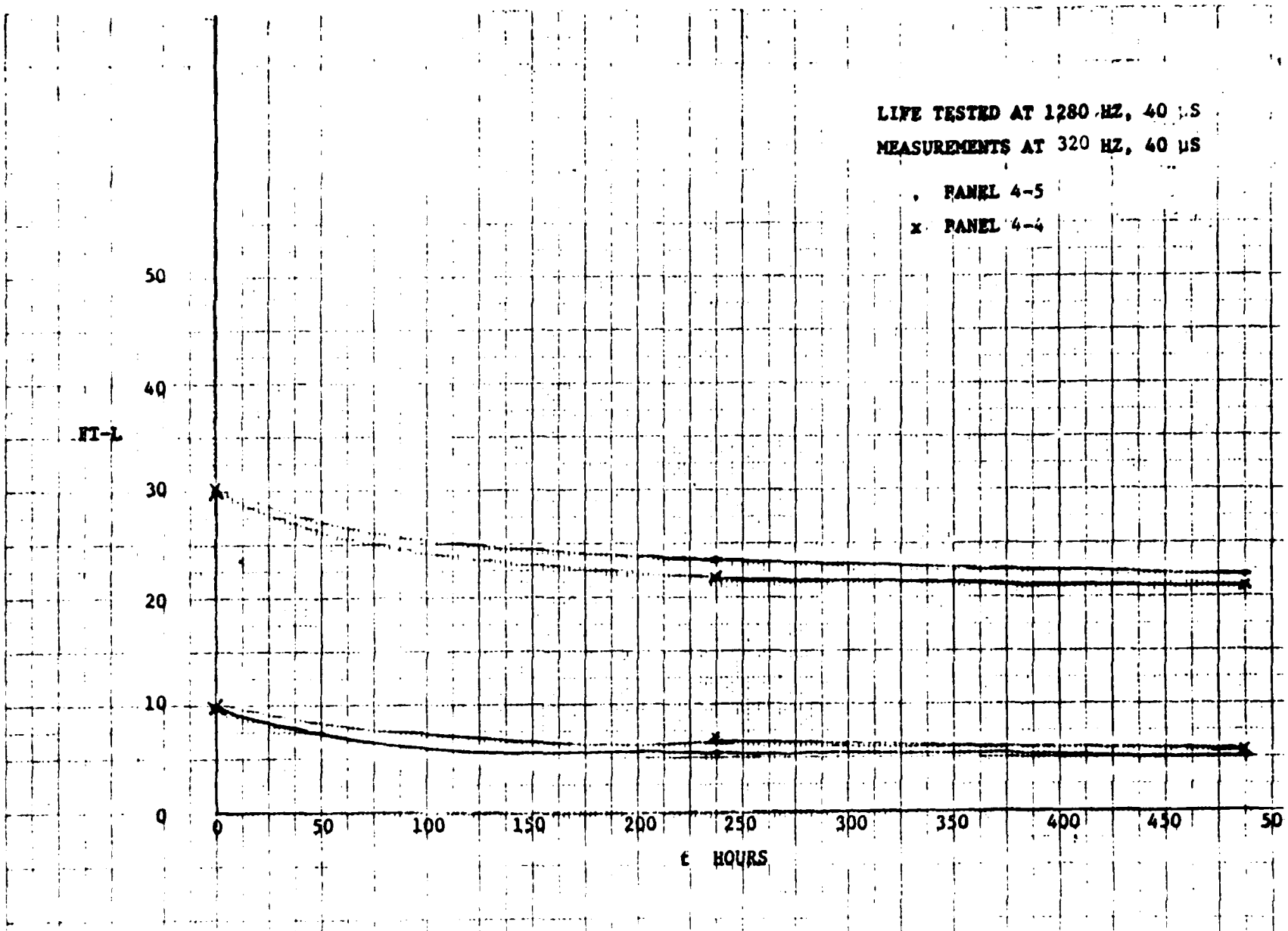
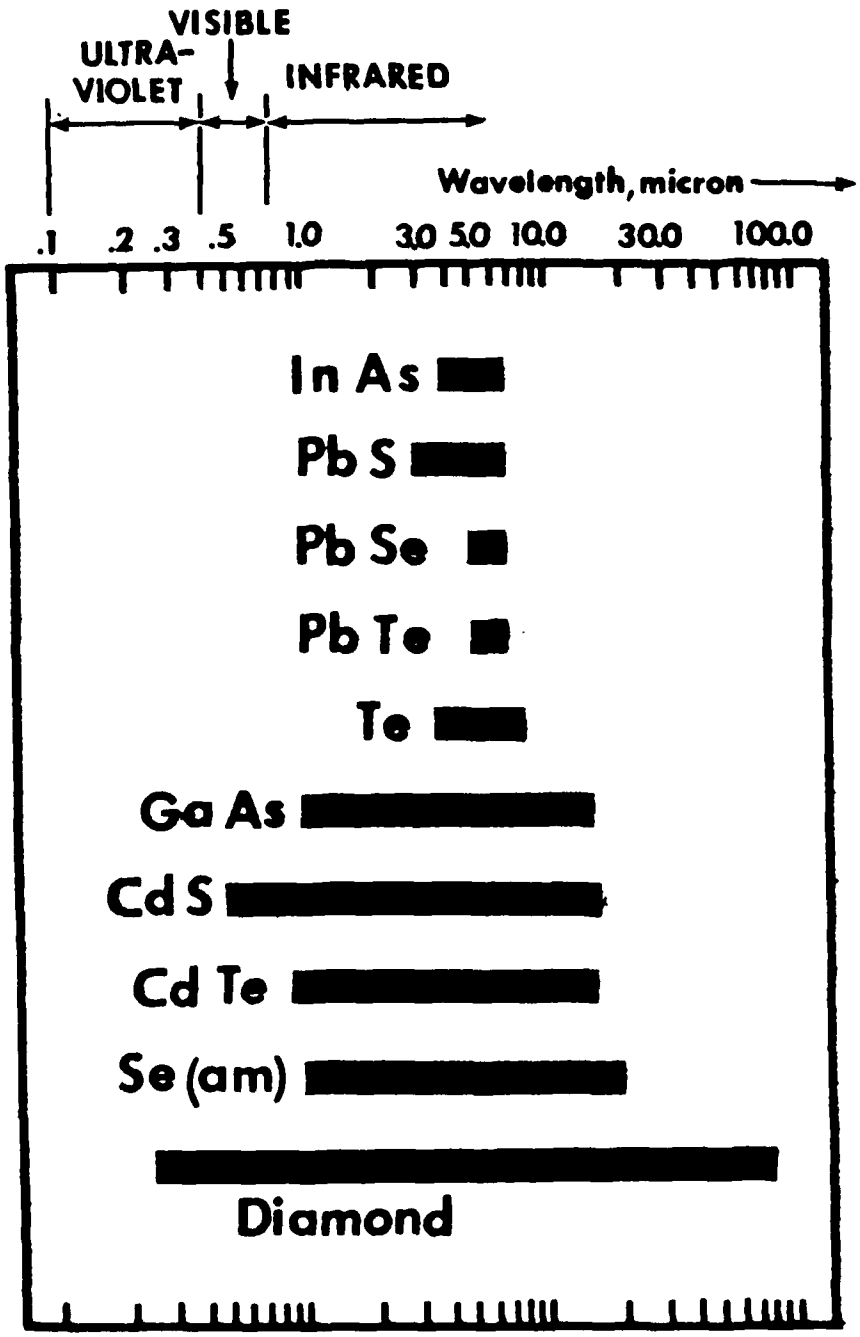


FIGURE 18

LIFE TEST - BRIGHTNESS VS TIME



Transmission regions for various materials.

FIGURE 19

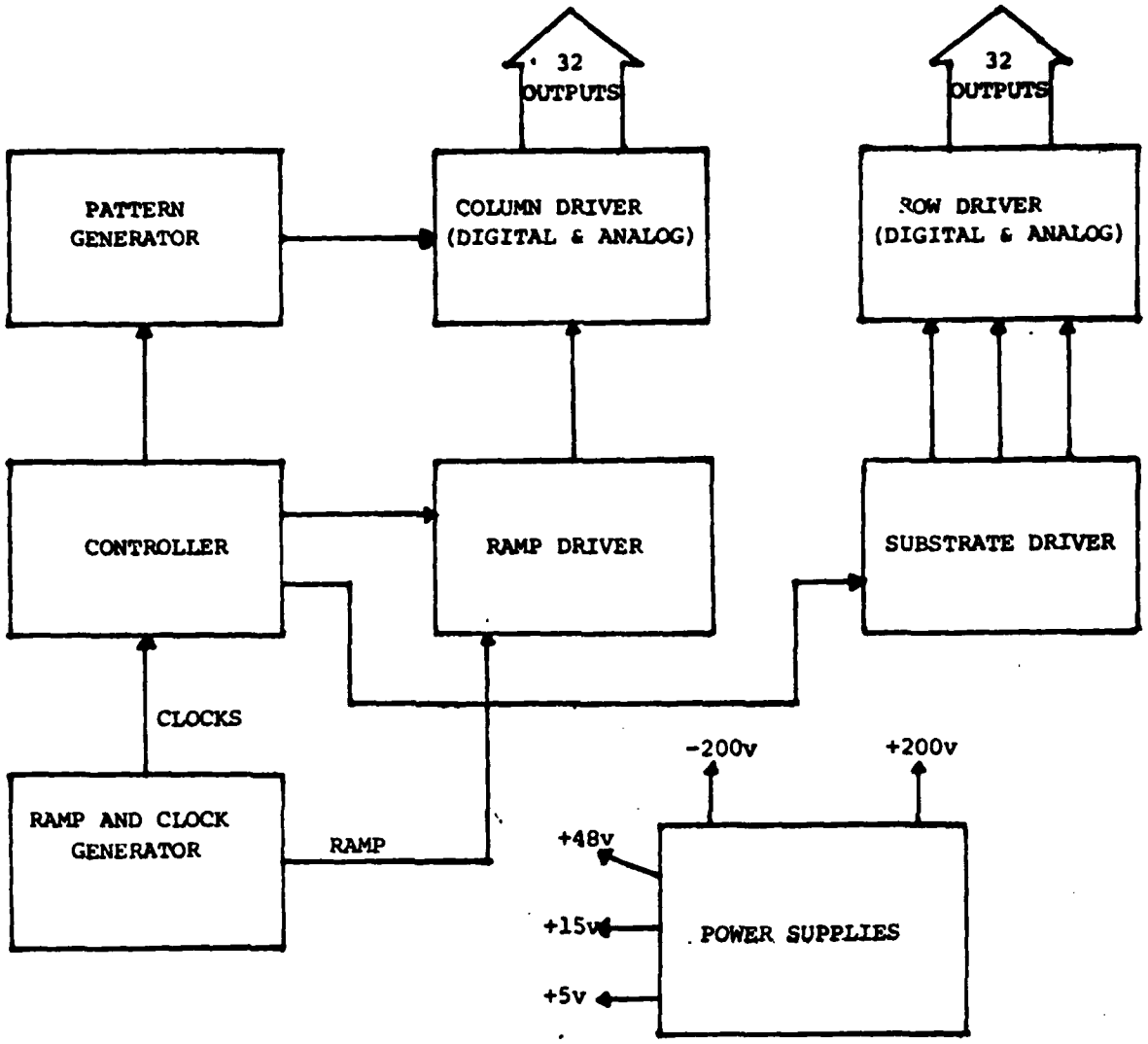


FIGURE 20. GROSS BLOCK DIAGRAM OF EDM-32 DRIVE/SCANNING ELECTRONICS ASSEMBLY

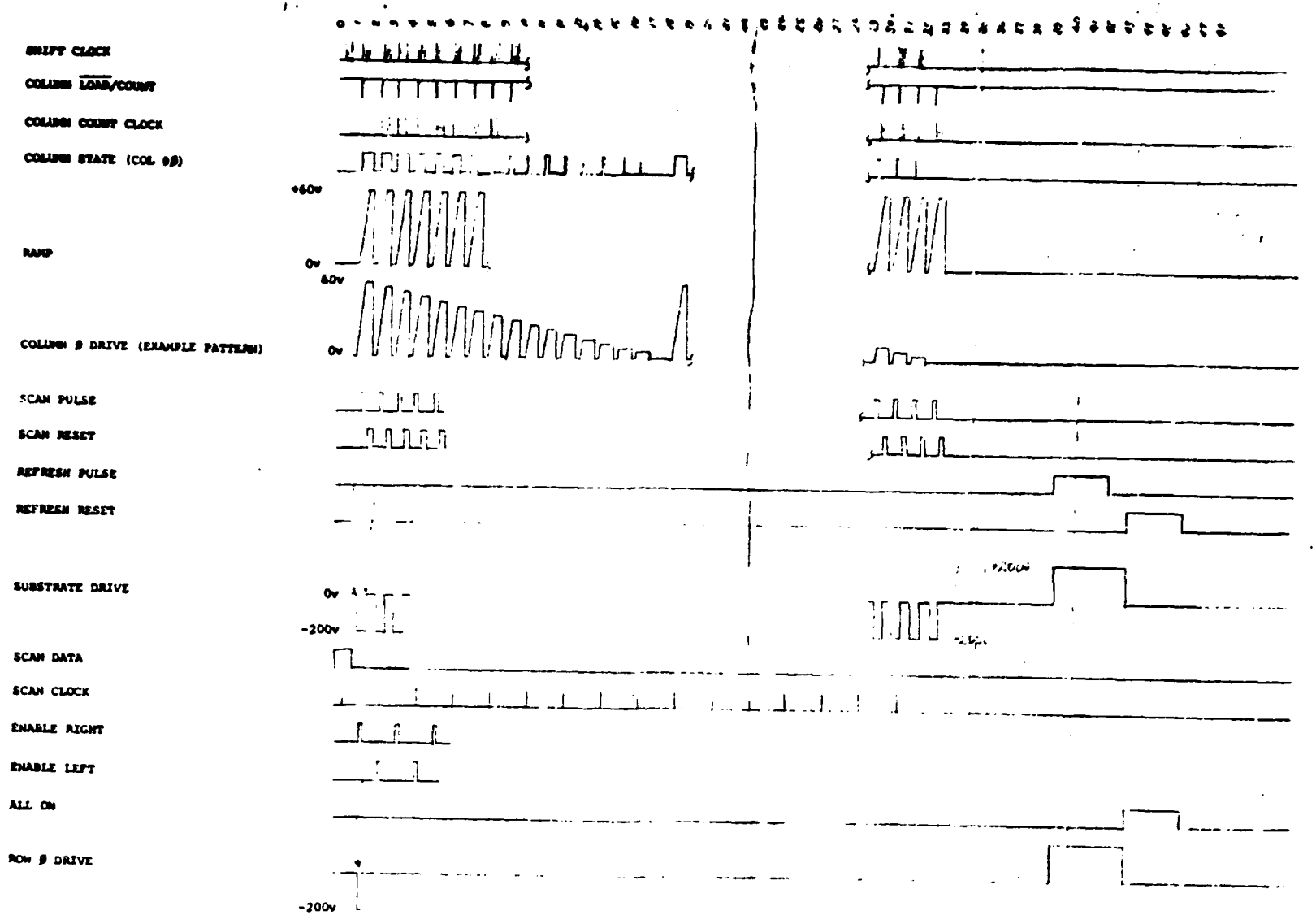


FIGURE 21. EDM-32 DRIVE/SCANNING WAVEFORMS

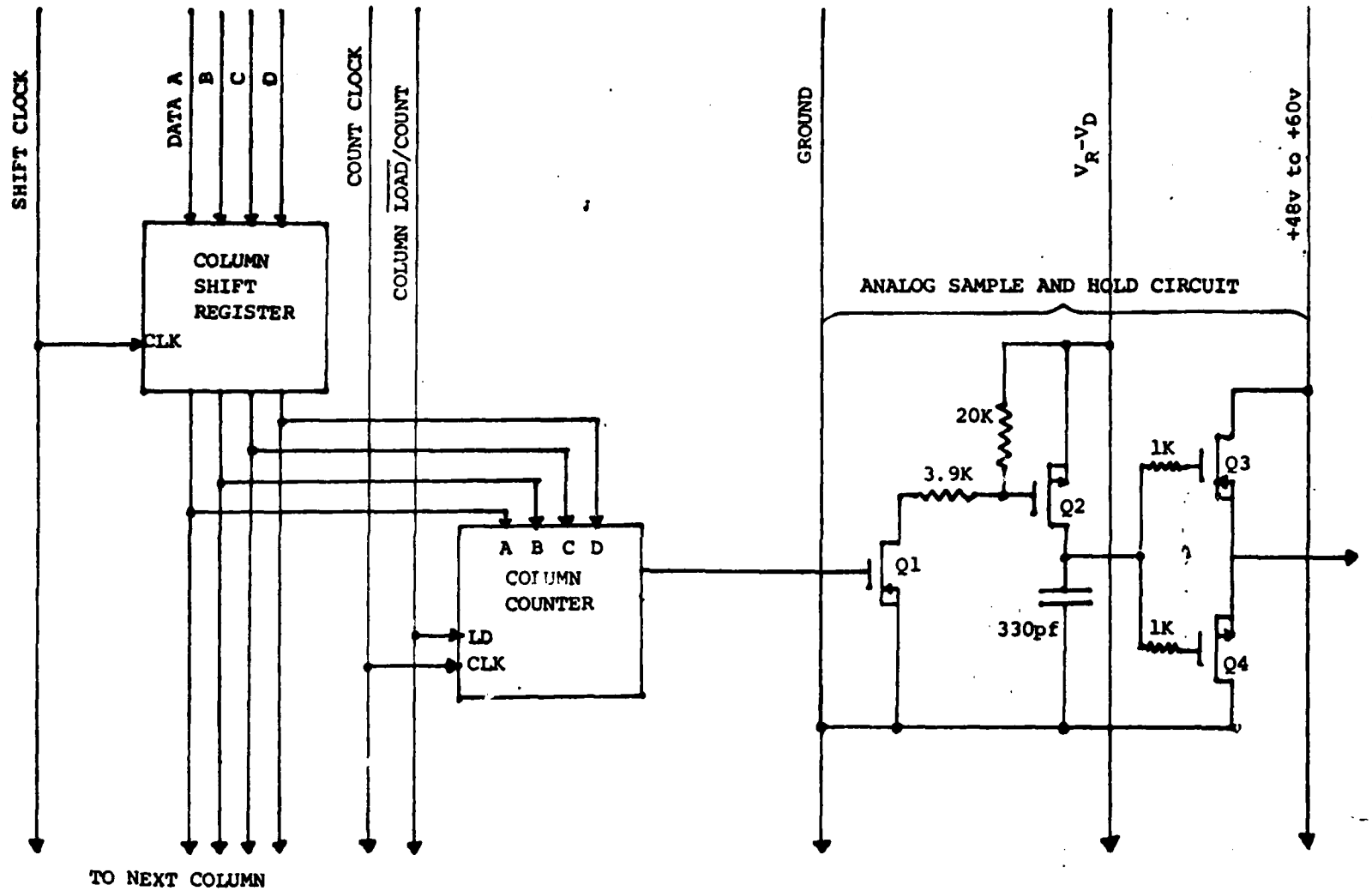


FIGURE 22. COLUMN DRIVER CIRCUIT. (THIS CIRCUIT REPEATED ONCE FOR EACH COLUMN)

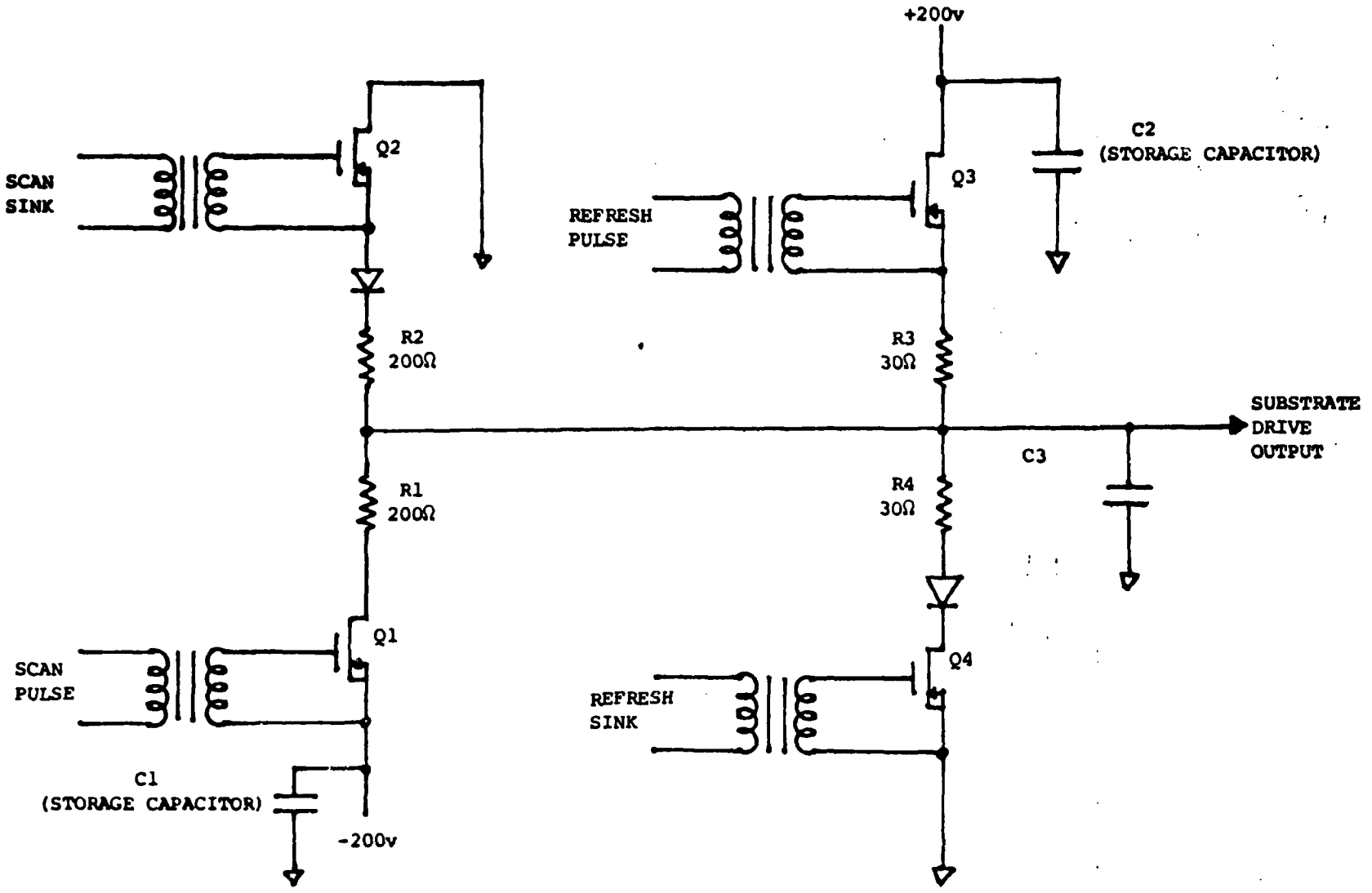


FIGURE 23. SUBSTRATE DRIVER CIRCUIT (ONCE PER SYSTEM)

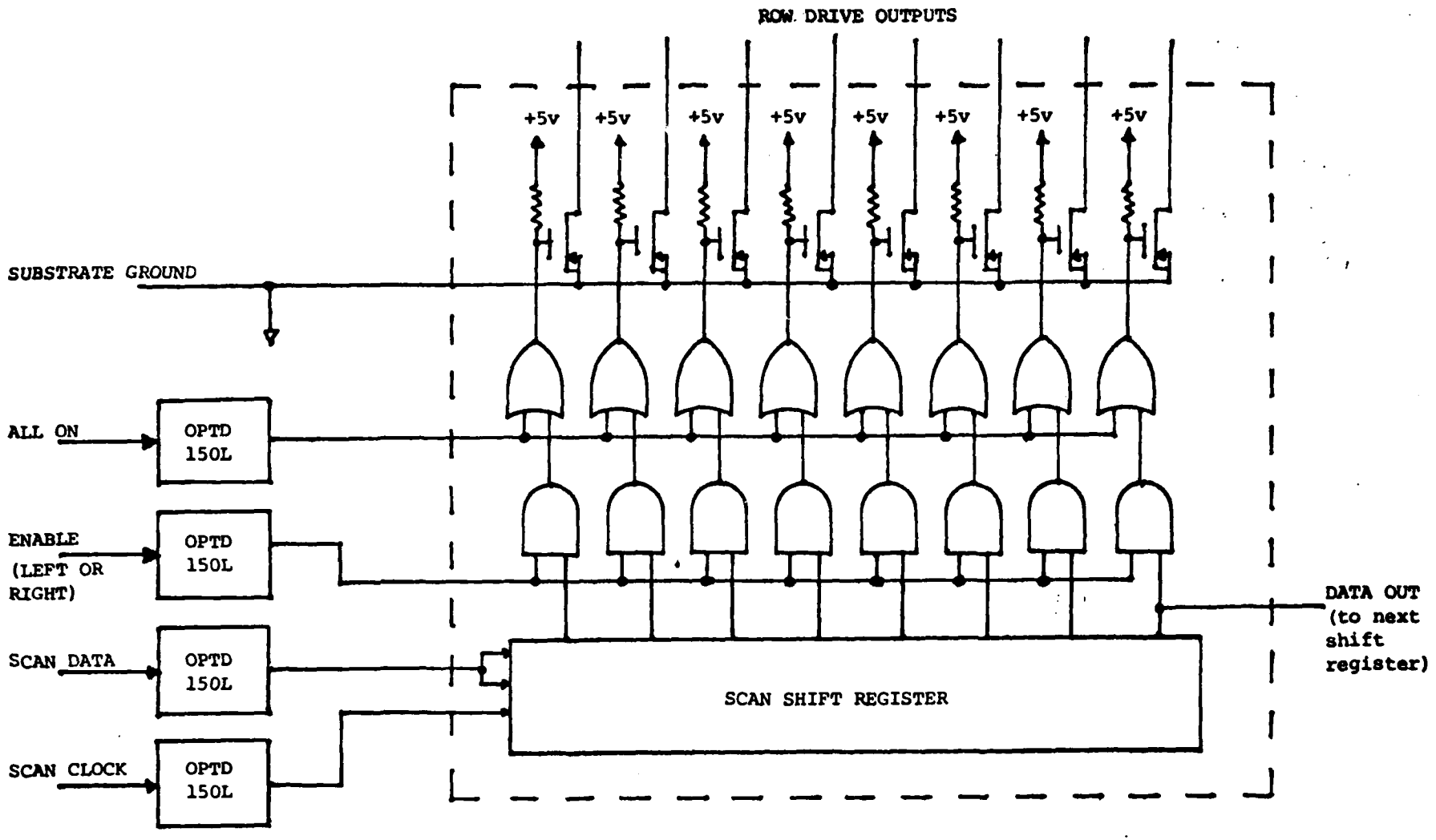


FIGURE 24. ROW DRIVER CIRCUIT. (THE AREA IN DASHED LINES IS REPEATED FOR EACH GROUP OF EIGHT ROWS.)

FIGURE 25
GRAPH OF BRIGHTNESS VS. SCAN AND REFRESH VOLTAGES
SOLID LINES REPRESENT A REFRESH VOLTAGE OF +180v.
DASHED LINES REPRESENT A REFRESH VOLTAGE OF +150v.

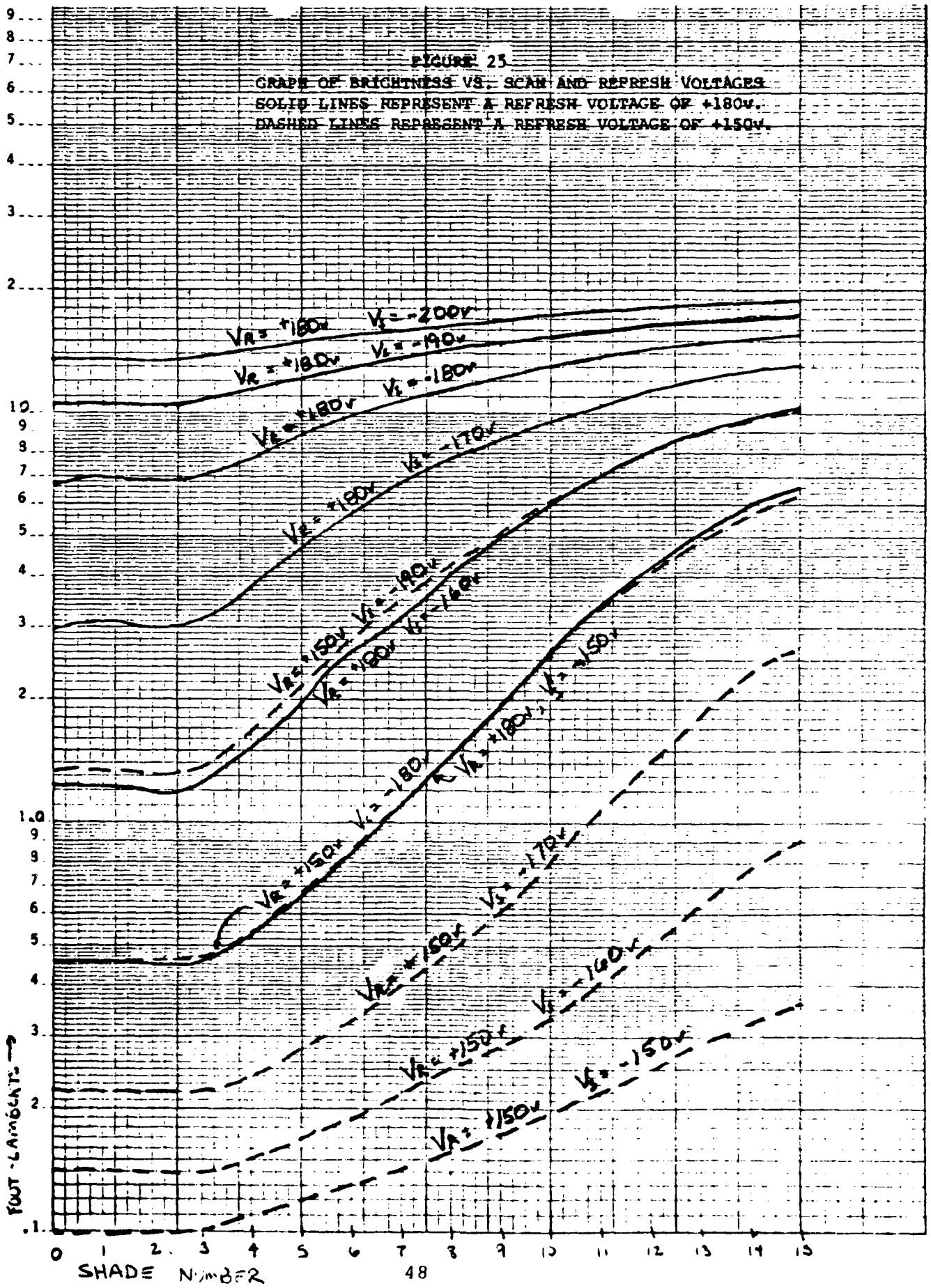
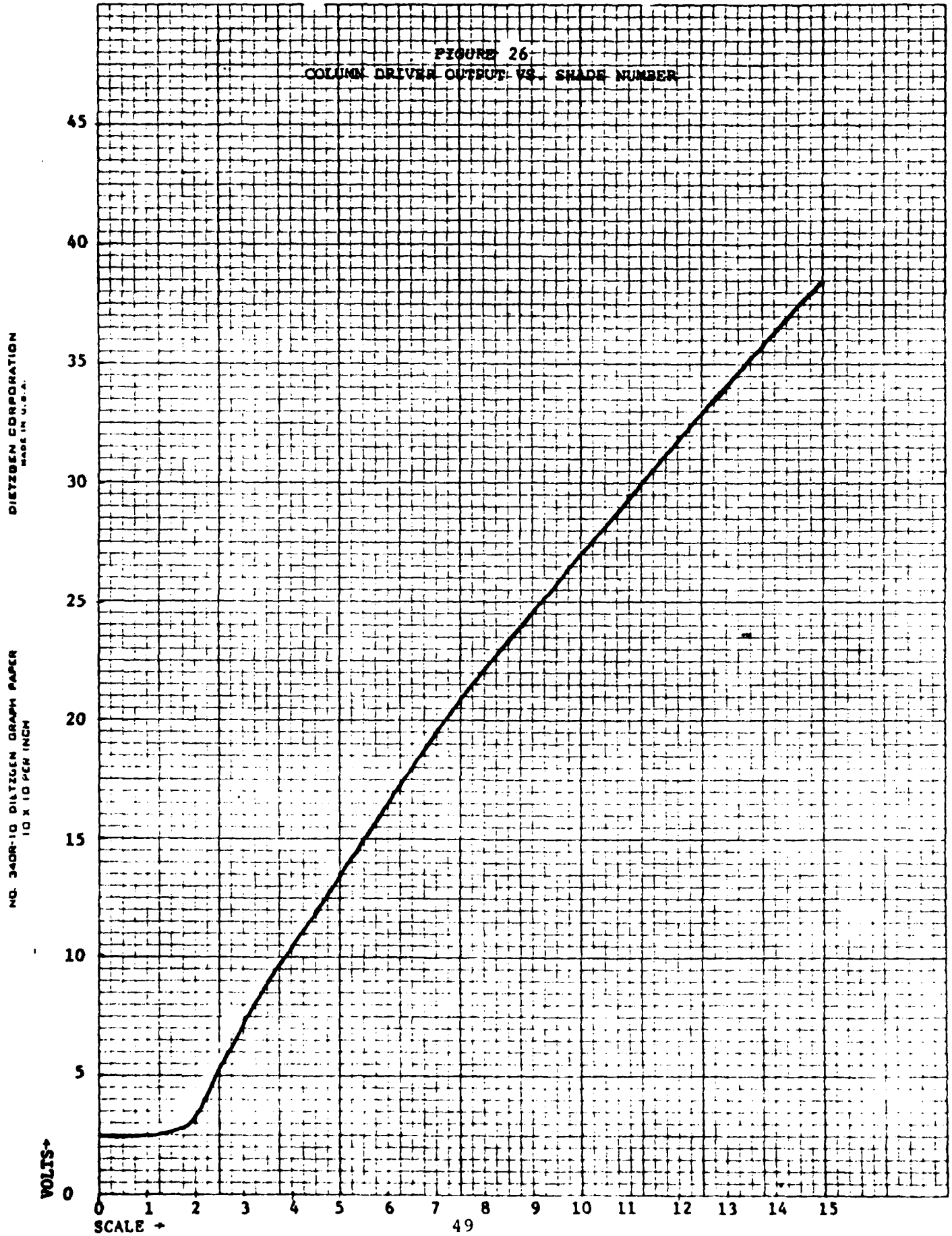


FIGURE 26
COLUMN DRIVER OUTPUT VS. SHADE NUMBER



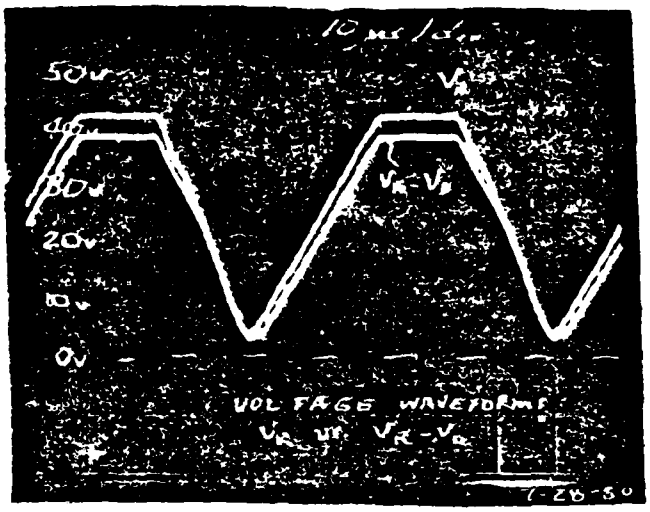


FIGURE 27A. OUTPUTS OF RAMP DRIVER, V_R AND V_R-V_D

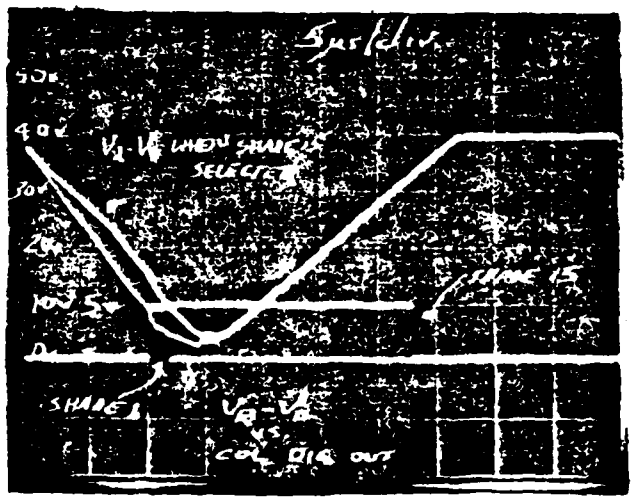


FIGURE 27B. V_R-V_D vs. COLUMN DIGITAL STATE OUTPUT (DOUBLE EXPOSURE)

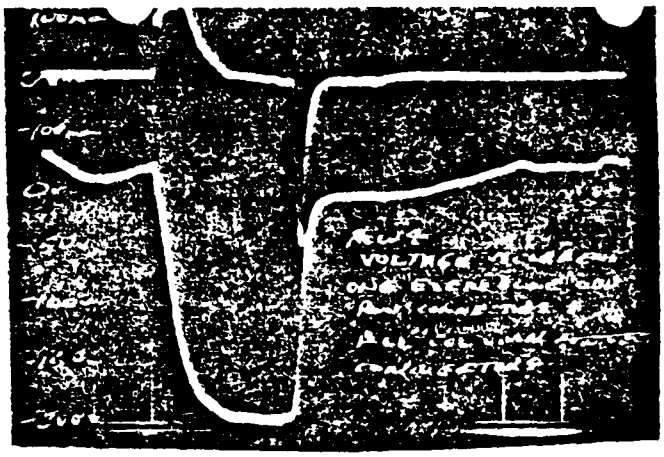


FIGURE 28A. ROW 4 VOLTAGE AND CURRENT WAVEFORMS WITH TWO ROW CONNECTOR AND ALL COLUMN CONNECTORS

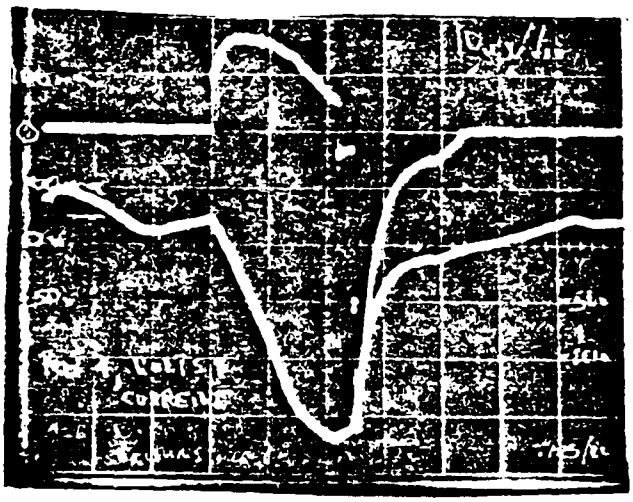


FIGURE 28B. ROW 4 VOLTAGE AND CURRENT WAVEFORMS WITH ALL ROW CONNECTORS AND ALL COLUMN CONNECTORS

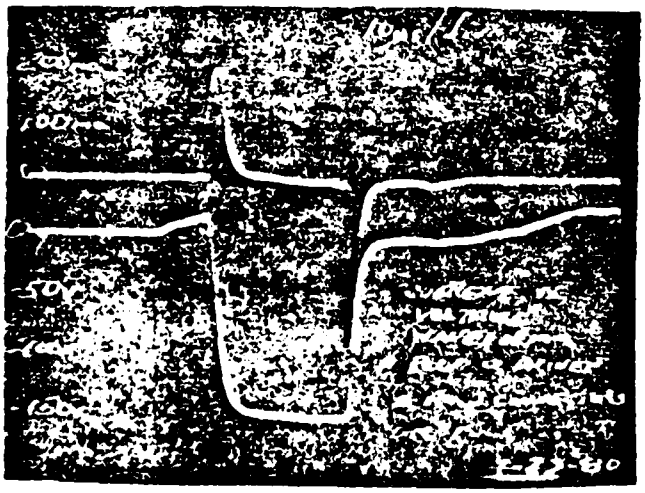


FIGURE 28C. ROW DRIVE VOLTAGE AND CURRENT WAVEFORMS WITH ALL ROW AND COLUMN CONNECTORS AFTER 6K PULLUP RESISTORS ADDED

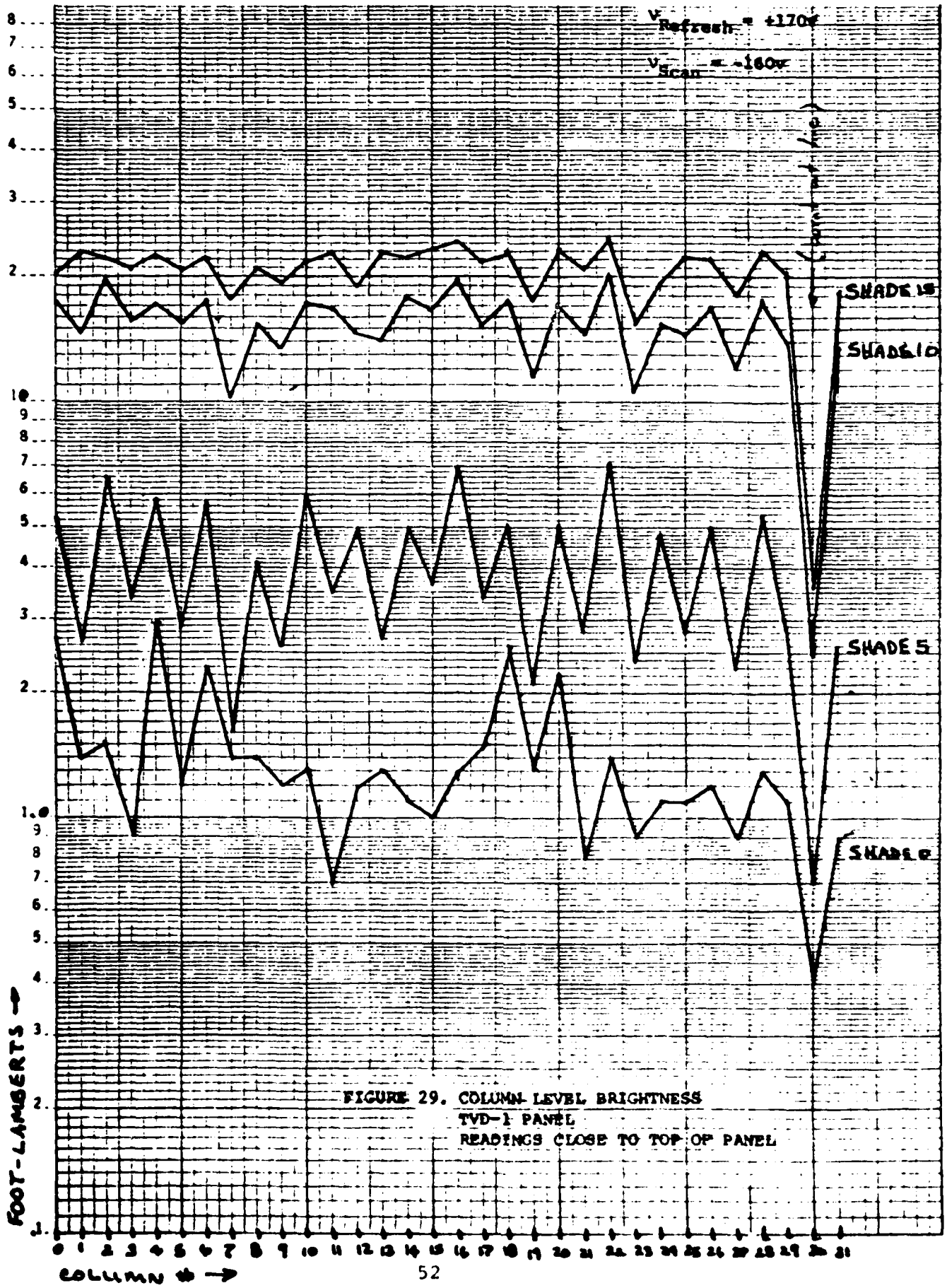
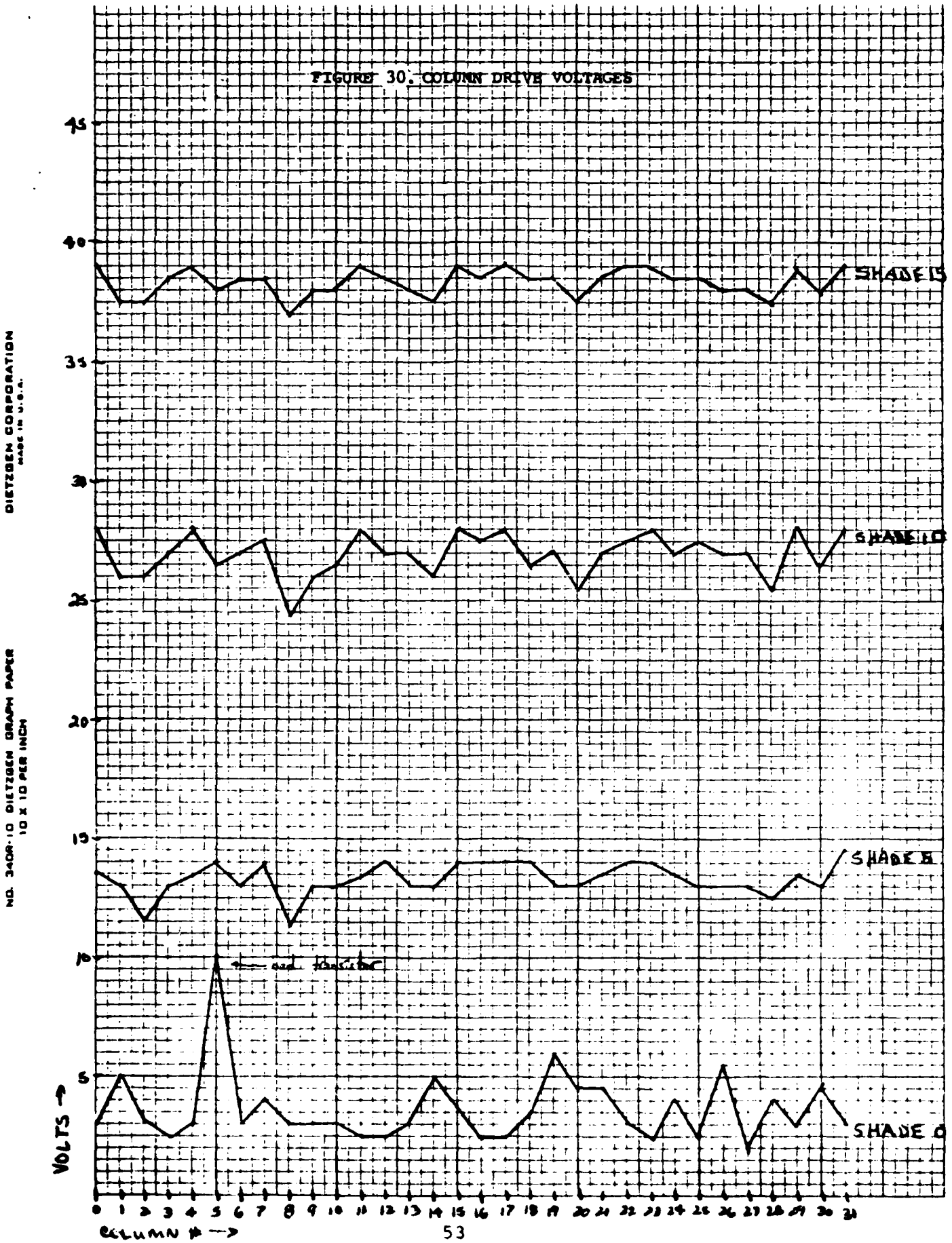


FIGURE 29. COLUMN LEVEL BRIGHTNESS
TVD-1 PANEL
READINGS CLOSE TO TOP OF PANEL

FIGURE 30. COLUMN DRIVE VOLTAGES



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