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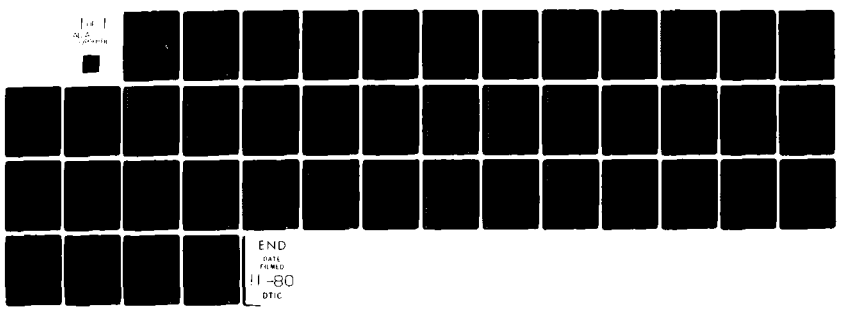

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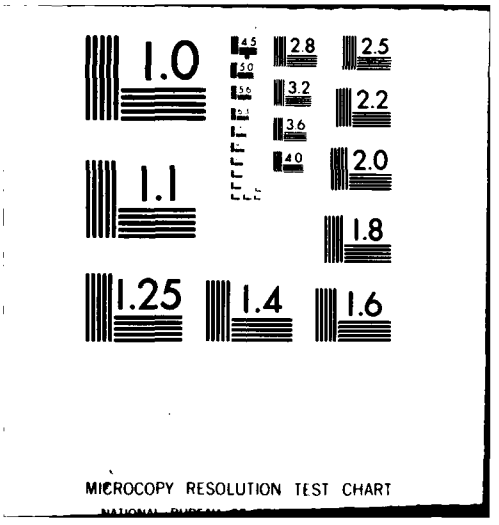
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TECHNICAL DESCRIPTION OF AN ELECTRONIC DISTRIBUTION AND SUMMING ELEMENT

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Rockwell International

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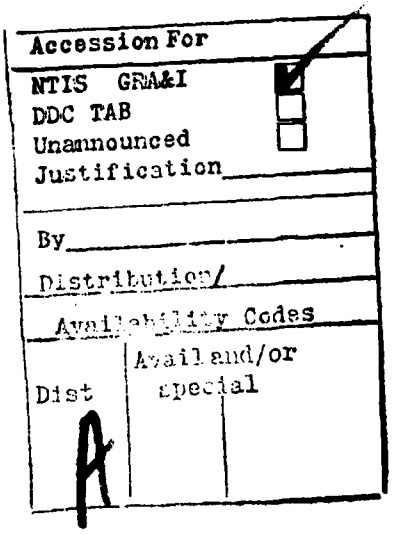

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SUMMARY

The Electronic Distribution and Summing Element (EDSE) consists of one 10-1/2 in. by 11-1/2 in. stitch wired circuit module. ECL 10,000 series integrated circuits provide the operating speed necessary for use of the EDSE in the Acoustic Array Simulator subsystem of the Combat System Technology Laboratory. Demonstration of EDSE performance will be made at Autonetics, and delivery will be to NUSC, New London, Conn, 120 days after receipt of contract.

The use of stitch wiring assures 120 day delivery as required; use of a PC board would involve a substantial schedule risk. ECL 10,000 ICs were chosen over TTL ICs for the following reasons:

1) TTL is definitely too slow for some parts of the circuit at normal temperatures, and for most of the circuit at elevated temperatures,
2) Because of interface incompatibility, a mix of ECL and TTL components would increase the total IC count to an unacceptable level,
3) The ECL components are less susceptible to noise because of their lower input impedance, and
4) The cost difference between ECL and TTL is relatively small, and expected to decrease further.

The input to an EDSE module is the digitized direct output from one target signal or noise generator and the delayed output from all other generators as computed in other EDSE modules in the system. The output is both the digital and analog simulation of two hydrophone signals. The module will weigh 0.9 lb and consume 55 w of power. It will not be mounted in a chassis and is designed to be cooled by laboratory fans.

The EDSE will be tested to verify that it has adequate timing tolerances at its designed operating speed, over the temperature range required, in accordance with the test plan of Appendix C. The EDSE will be tested at Anaheim, to a final acceptance test procedures prepared by Autonetics as described in Appendix C, and delivered to NUSC, New London, Ct. for final acceptance.

The items to be delivered to the government are:

1. One EDSE circuit board
2. Schematic diagram and parts list

3. Final acceptance test procedure
4. Operation and maintenance instructions
5. Final engineering report

INTRODUCTION

This proposal to design, develop, fabricate, and test an Electronic Distribution and Summing Element (EDSE) is in response to solicitation No. N00140-75-R-6336 from the Naval Regional Procurement Office Philadelphia, Newport Division. This solicitation incorporates NUSC TASK ORDER No. TF/LAC-1156 dated 4 February 1975.

The EDSE is a high-speed digital module, to be used repetitively in an Acoustic Array Simulator (AAS) for the Combat System Technology Laboratory (CSTL). The reason for developing this module is to demonstrate that the circuits can be made to operate at the required high speed.

The following discussion describes Rockwell's proposed design, compares the proposed design with other approaches, and briefly analyzes the timing margins and thermal problems involved.

I. BACKGROUND

The CSTL must have the capability to test and evaluate new concepts for sonar design. In order to test a beamformer, it is necessary to generate, for each hydrophone preamplifier in an array, the signal that the corresponding hydrophone would generate if the array were in the water.

The signal from each hydrophone is a composite. It may consist of flow noise, ambient sea noise, auxiliary machinery noise, propulsion machinery noise, interfering distant targets, marine life, personnel generated transients, etc. To perfectly simulate the signals that occur in the ocean would require an infinite number of noise generators. But practically there is no need for a greater number of noise generators than the number of beams to be formed, and the number of beams for a three-dimensional array will not exceed half the number of hydrophones. So even for the greatest number of hydrophones that is now contemplated for any one vehicle, it is practicable to build an array simulator by repetitive use of an Electronic Distribution and Summing Element.

To accommodate the large numbers of beams, large number of hydrophones, large array size, and the wide information bandwidth, the EDSE circuits must operate at a high speed. For the system to be completely programmable, so that it can be used with a variety of array configurations and sound sources, particular attention must be given to component selection and circuit design.

The EDSE module will be the basic building block of the programmable acoustic array simulator in the CSTL. The EDSE module will accept digital data from one of the signal generators (either directly or after passage through a transmission loss circuit), process the data, and then combine it with processed data from other EDSE modules to simulate the outputs of two hydrophones. Both digital and analog hydrophone outputs will be available from the EDSE module. A system containing N modules will allow for N different signal (or noise) sources and provide 2N simulated hydrophone output channels.

II. DETAILED CIRCUIT DESCRIPTION

The component functional groups on the module include the data delay memories, the weighting multipliers, the delay address storage and generation circuitry, and the four output accumulators. A block diagram of the module is shown in Figure 2-1.

Digital data from the source generator is written into data delay RAM A and data delay RAM B at the input sample rate, with register R_1 providing the one word buffer to accomplish the writing. The basic sample rate for register R_1 is 12.5 kHz. Each 8-bit word that is sampled at this 12.5 kHz rate, however, is comprised of two 4 bit words which represent source generator data samples taken at adjacent 40 μs intervals. The input is therefore effectively multiplexed at 2-to-1 to simulate a 25 kHz sample rate to accommodate direct digital connection to the BQS-13 DNA beamformer with no spectral folding. Sufficient storage capacity exists in the data delay memories to accommodate 256 time samples for the 12.5 kHz sample rate on both 4-bit input words. This allows for maximum array dimension of 100 ft. Although the two phase data memory will allow for an effective sample period of 40 μs, the 8-bit delay address from register R_7 is common to both memory phases, thereby providing a 80 μs delay resolution.

In the 80 μs period between input data samples, the data stored in the data delay memories is processed to produce one time sample for each hydrophone in the simulated array. Since a maximum of 2048 hydrophones can be simulated in the array simulator, the data delay RAMs must be accessed 2048 times in 80 μs to accomplish the required processing. This requires a read cycle time of 39 ns for the data RAMs. Each of the 2048 accesses corresponds to an output data sample for one specific hydrophone. The delays which are applied to the data samples to form hydrophone outputs are precomputed externally to the array simulator module by a general purpose computer prior to the actual simulation.

In a load sequence, initiated by the computer, the delays and weighting multiplication factors which were calculated for the array under simulation are latched into Register R_6 and then written into both phases of the delay and coefficient RAMS. Since the EDSE module is replicated many times in the CSTL system, interface hardware on the module must be kept at a minimum. The parallel data bus which loads the data and coefficient RAM must drive 1024 modules in the maximum system configuration. This large drive requirement dictates the use of several bus drivers driving smaller

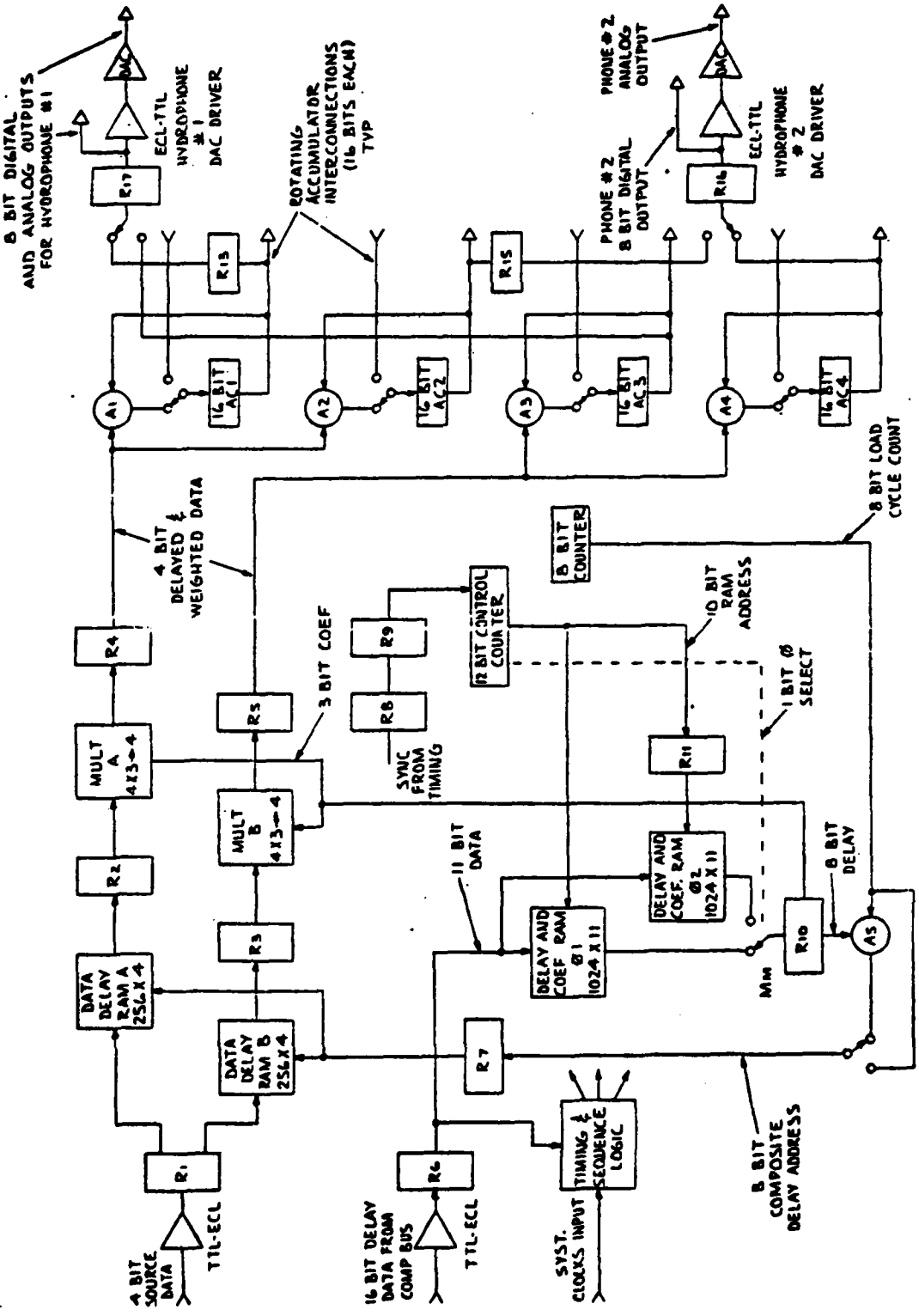

Figure 2-1. Detailed Block Diagram, Electronic Distribution and Summing Element

groups of EDSE modules. It is expected that these drive modules (which are few in number) will contain the majority of the computer interface electronics. This allows the use of a minimum of interface electronics on the EDSE modules themselves. Specifically, this electronics consist of one parallel data register and a data clock line only. Memory write controls and memory addresses for the load process are generated in the timing/sequence logic and the control counter, from timing pulses received from the computer interface and system timing circuitry. The words loaded into this RAM utilize 11 bits out of the 16 bits in the computer word (eight bits of delay address and three bits of weighting coefficient). A total of 2048 11-bit words are stored (one for each of the 2048 maximum hydrophones).

When the load cycle is complete the array simulator module is loaded (one processing mode by the sequence logic. In this mode the delay coefficient RAMs are sequentially cycled by the control counter to select the appropriate delay and weighting coefficient to be applied to the data for each hydrophone.

These RAMs would normally require the same read access speed as is required by the data RAMs; however, it is convenient to split the delay coefficient RAM into two timing phases and multiplex the outputs two to one to effectively reduce the required access time to 78 ns.

As new data is entered into the data RAMs, it is placed in sequentially higher addresses with reset at modulo 256. The delay addresses stored in the delay coefficient RAM represent absolute delays and are therefore relative addresses based upon the address of the last data loaded in the data RAM. The correct absolute address is determined by adding the stored delay address to the current load address. This is accomplished in Adder A_5. Registers R_8 and R_9 delay the load address strobe to synchronize the load address with the current delay address.

The most significant eight bits of the control counter contain the current load address. The least significant 11 bits sequentially select the address for the delay coefficient RAM with the LSB selecting the phase of this RAM. Register R_{11} holds the RAM addresses during both read and write cycles of the delay and coefficient RAMs for one phase. For the other phase of operation the counter itself holds the addresses.

As appropriately delayed data is read out of the data RAMs, it is multiplied by a weighting coefficient corresponding to the weighting factors applied to each hydrophone

in the array being simulated. A 3-bit weighting coefficient is stored with the data delay address in the delay-coefficient RAM. High speed ROM lookup multipliers (Mult A and Mult B) multiply this factor by the words out of the data RAMs prior to the application of these words to the four accumulation networks. There is a two clock time delay from delay address access to data availability at the multipliers. The weighting coefficients stored in the RAM therefore correspond to delay addresses stored in earlier RAM addresses to compensate for this two clock time addressing delay. The multipliers compute rounded 4-bit products from 4-bit data words and 3-bit coefficients.

Four rotating accumulators accept data from the two weighting multipliers. The accumulators consist of a 16-bit register and a 16-bit arithmetic logic unit (A_1 through A_4). Two accumulators feed one hydrophone output. The accumulators combine the weighted, delayed data from each of 1024 sources to form a composite hydrophone output. Accumulators are operated on a 78 ns cycle with two accumulator outputs being multiplexed to simulate one hydrophone output at an effective 25 kHz sample rate. In one 78 ns cycle the data RAMs are accessed twice. Data accessed in the first half of this period is accumulated in A_1 and A_3 and data accessed in the second 39 ns period is accumulated in A_2 and A_4.

At each 78 ns accumulation period the contents of all accumulation registers are rotated to another array simulation module where data from the source feeding that module is added to the accumulated data word for each separate hydrophone. Addresses in the control counter are advanced by one count with each accumulator rotation to select the appropriate hydrophone delay and weighting coefficient. Control counters of different modules are preset to skewed addresses such that each hydrophone accumulator will have received data from each module source when the accumulator rotation is complete. At the end of 1024 rotations the accumulator contents are latched into registers R_{13}, R_{14}, R_{15} and R_{16} of each module in the system and the output multiplexers are switched at 40 μs intervals to simulate a 25 kHz output sample rate. The outputs of registers R_{14} and R_{16} hold the digital data for the two hydrophone outputs on the module. The accumulator registers require a length of 14 bits to accommodate the accumulation of 1024 4-bit numbers. The actual size of these registers is 16 bits due to hardware economy.

The output word size is eight bits which is derived by a hardwired binary scale of the output accumulator. This scale factor is not electrically alterable but may be wired to accommodate divisions of 0, 1, 2, 4, 8, 16, 32, 64, and 128 to adjust the

output scale factor to simulate arrays containing different quantities of hydrophones (this scale factor is indicated with an S on the block diagram). Digital-to-analog converters provide analog output on both hydrophone channels.

III. TIMING ANALYSIS

The Electronic Distribution and Summing Element (EDSE) is a fully synchronous all-digital module. All data transfers from registers, through functional elements, and into registers are initiated by the same edge of a 26 MHz clock. To reduce data delays, the ICs used are MSI, ECL, 10,000 series components.

Three areas on the card have relatively critical timing: the accumulator loop, the coefficient and delay access loop, and the data access loop between R7, R2, and R3.

The times shown in the following sections are worst case, additive delays at operating temperatures. In this analysis the worst case timing margin is 4 ns in the accumulator loop (approximately a 10 percent timing margin) and no timing problems are anticipated since trouble free operation has been experienced with other Autonetics systems having smaller timing margins.

A. COEFFICIENT AND DELAY

The large delay and coefficient RAM is phase split into two 1024 x 11 sections, each receiving 78 ns address periods. The Ø2 address is delayed so that the memories can be alternatively read at a 39 ns rate into R/O. See Figure 3-1. The worst case timing in this RAM area is:

Counter output	-	5 ns
Ø RAM access	-	65 ns
R10 setup	-	2 ns
		72 ns

The timing margin is 6 ns. The R11 to R10 timing is less critical since R11 stores the address before the counter changes. The margin there is 10 ns.

B. DATA RAM TIMING

Data is being accessed at a 39 ns rate from the 256 x 1 RAMs. The manufacturer specifies access times of 20 ns typical and 35 ns maximum. Autonetics intends to select and screen these parts to a 30 ns maximum delay. This will provide a 6 ns safety margin. See Figure 3-2.

The timing for the multipliers from R2 through the ROM to R4 is similar. However the ROMs are rated at 25 ns maximum so the margin is adequate with no component screening.

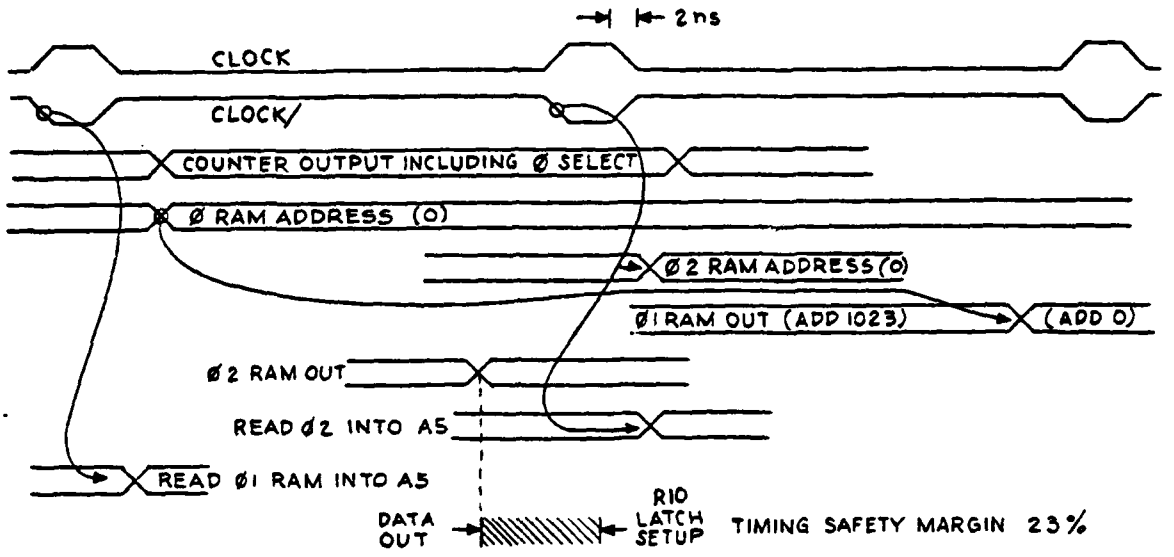

Figure 3-1. Delay and Coefficient RAM Outputs

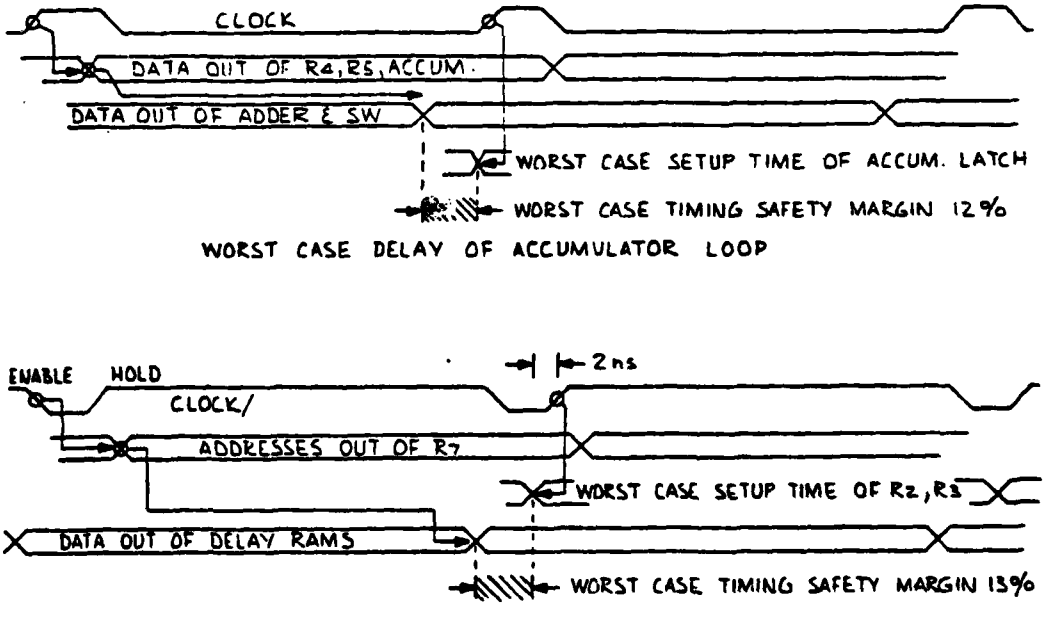

Figure 3-2. Timing and Delay

C. ACCUMULATOR TIMING

This timing loop is the most critical. The arrays of the 16 bit adder are rippled from chip to chip and produce a worst case addition time of 25 ns. The available look-ahead carry generator only works for two chips at a time and gives no improvement over the ripple carry for a 16 bit adder. The output goes through a switch, then into an edge triggered latch. (See Figure 2-1). The worst case timing delays for the latch delay and setup, adder and switch delays totals 35 ns. This leaves a 4 ns safety margin. The timing of other areas of the module is not critical. The adder, A5, in the R10 - R7 timing loop is only eight bits wide and therefore much faster than the accumulator adder.

The control counter, through timing and sequencing logic, controls all switches on the card, counts out the 2048 high speed operations and loads a word into the Data RAM from R1. This entire operation is repeated at the 12.5 kHz basic sample rate.

All register to register timing cycles are very straightforward. Edge triggered latches are used wherever the minimum delay times could cause races or hazards.

The above timing margins appear to be valid across the entire temperature range described in the thermal design section (VI).

IV. TECHNOLOGY TRADEOFFS

The operational speed of the distribution and summing functions as indicated in the task description is such that extremely high speed digital logic elements are required. As shown in Section III of this proposal, typical component timing cycles are on the order of 40 ns, implying clock rates of 25 MHz. Assuming fully synchronous operation of the system as shown in the block diagram of Figure 2-1, the critical timing loop involved with reading the Data RAM requires a register propagation delay, a memory access time and a register setup in this 40 ns period. To maintain acceptable timing margins, ECL components are mandatory in these areas of the circuit. To insure adequate margins, the 256 bit RAMs must be selected for a maximum access time of 30 ns where the maximum data sheet time is stated as 35 ns. (Small fallout is expected from this selection since typical access times are stated as 20 ns). Time multiplexing could be used to reduce speed in these critical areas to a range compatible with TTL components; however, the device count and power requirements would be substantially increased and, therefore, this option was discarded.

Some of the lower speed areas (i.e., the delay address storage RAM) operate at speeds which could possibly be implemented with Schottky TTL devices. This area was critically examined and it was concluded that although the TTL implementation of these areas would be slightly less expensive, the package count would be higher and the power dissipation would be larger.

It was also concluded that it would be desirable to maintain, as much as possible, the same logic family throughout the module. Since noise sensitivity and operation have different characteristics for each logic family, noise margins on the devices are reduced when TTL and ECL logic families are mixed.

The following paragraphs compare Schottky TTL and 10,000 series ECL in each of the parameters of interest. (ECL 10,000 series was chosen over other ECL families because of cost, MSI component availability, second sourcing and speed match to the problem to be solved.)

A. TIME DELAYS

Propagation delays of ECL 10,000 circuits are significantly shorter than comparable Schottky circuits (see Figure 4-1). Basic ECL 10K gates have typical propagation delays of 2 ns, with a 2.9 ns maximum delay. Schottky TTL gates are

3 ns typical and 5 ns maximum. These parameters apply at 25 C only. When operation over a range of temperatures is considered, maximum MECL 10K gate delays increase to 3.3 ns for the standard commercial temperature of -30 C to +85 C, and to 3.7 ns for the military temperature range of -55 C to +125 C.

While propagation delays for Schottky TTL circuits can be expected to increase at temperatures other than 25 C, Schottky TTL data sheets do not guarantee speed performance over the temperature range expected under actual operating conditions.

Further examination of Figure 4-1 shows that the propagation delay advantages of ECL 10K increase as circuit complexity increases. Note, for example, that the standard ECL 10K dual flip-flop offers a 3 ns (typical) and a 4.5 ns (maximum) delay from the clock input to the Q output. Corresponding delays for the fastest Schottky dual flip-flop are 5.0 ns and 7.0 ns.

For MSI circuitry, ECL 10K propagation delays are one half those of Schottky TTL devices (Figure 4-1). The largest function common to both logic families is a 4-bit arithmetic/logic unit (181). Again, the ECL 10K circuit operates nearly twice as fast as the Schottky TTL part.

PROPAGATION DELAY (ns)				
PART	SPEC	ECL	TTL-S	RATIO
Gate	Typ.	2.0	3.0	1.5
	Max.	2.9	5.0	1.7
Flip Flop	Typ.	3.0	5.0	1.7
	Max.	4.5	7.0	1.6
MSI	Typ.	4.0	8.0	2.0
	Max.	6.0	12.0	2.0
LSI ALU	Typ.	8.0	14.0	1.75
	Max.	11.0	22.0	2.0

Figure 4-1. Propagation Delays of ECL 10,000 and Schottky TTL Circuits at 25 C

B. TOGGLE RATES

When toggle rates of flip-flops are considered (Figure 4-2), it can be seen that ECL 10K flip-flops also offer a significant speed advantage. The ECL 10K dual flip-flop toggle rates are typically 160 MHz, and are guaranteed to be at least 125 MHz. The Schottky flip-flop rates are 125 MHz typical and 80 MHz worst case.

C. POWER CONSUMPTION

In a Schottky TTL gate, power dissipation is strongly dependent upon the output logic level. With a high logic level output, the specified power consumption is 12 mW (typical) and 19 mW (maximum) per gate. With a low logic level, 24 mW (typical) and 43 mW (maximum) are required. For a 50 percent duty cycle (between high and low outputs), the specified power is 18 mW (typical) and 31 mW (maximum). (These values are calculated from data sheet current specifications, normalized to 5.0 Vdc instead of the rated 5.25 volts, to provide an accurate comparison with ECL 10K power specifications).

TOGGLE RATES (MHz)				
CIRCUIT	SPEC	MECL		TTL-S
Dual "D" Flip Flop	Min.	125	200	–
	Typ.	160	225	90
Dual J-K Flop Flop	Min.	125		80
	Typ.	140		125
4-Bit Shift Reg.	Min.	150		75
	Typ.	200		110

Figure 4-2. Flip-Flop Toggle Rates of ECL 10,000 and Schottky TTL Circuits

As with any TTL circuit, power requirements of Schottky TTL vary with operating frequency: Power consumption increases exponentially with operating rate. This is because of transient current spikes which flow momentarily during turn-on/turn-off of totem pole outputs. Due to transient currents, the frequency-dependent power dissipation must be added to static or quiescent-state power requirements specified on data sheets.

The total power-vs-frequency curve for two Schottky TTL gates is shown in Figure 4-3. Power dissipation for two ECL 10K gates is also shown. Notice that it is constant with frequency.

In making system power calculations for ECL 10K, power dissipated in external pull-down or line termination resistors have been added to the on-chip gate power dissipation.

For a user, overall system power consumption is often of greater interest than basic data sheet specifications concerning package current requirements. Any other power dissipating components used in a specific system such as pull-up resistors for open collector outputs, must also be taken into account.

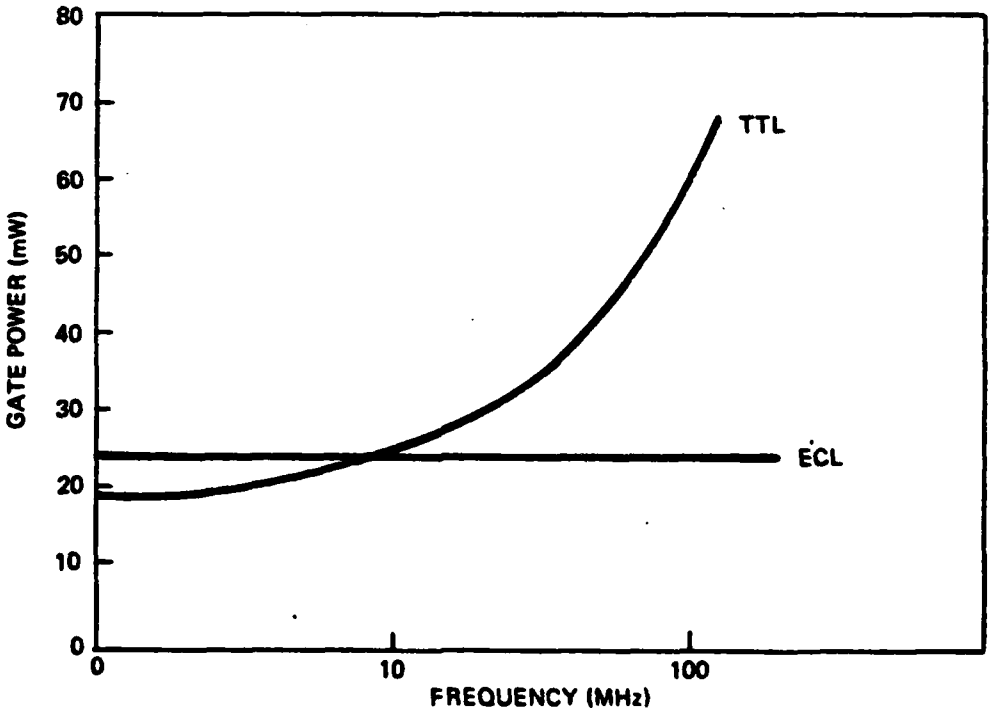

Figure 4-3. Power Dissipation vs Frequency (ECL-TTL)

With ECL 10,000, system power consumption is not dependent upon operating frequency. However, certain power components must be added to the basic power listed on a data sheet. The additional components are: (1) Power dissipated in the output transistor(s) of the circuit, due to currents flowing in signal lines; (2) Power dissipated in off-chip pulldown or line termination resistors. These components are added to the basic ECL gate power of 26 mW (typical), or 36 mW (max), to compute total power dissipation in a system. It is not possible to specify either of these power dissipation components on a data sheet, because they will vary from one system design to another, and will depend on the particular resistor values chosen by a system designer.

As an example of the calculation of total power dissipation for an ECL System consider a single gate driving into a 100 ohm transmission line which is terminated through a 100 ohm resistor to -2.0 Vdc. The line termination resistor (which also serves as a pulldown on the gate output) will dissipate 6.5 mW. The gate output transistor line will dissipate 7.5 mW on-chip at this current level.* Thus, the total in-system gate power including external load is 40 mW (typical), or 50 mW (max).

Looking again at Figure 4-3 to see a comparison of typical total in-system power consumption for ECL 10,000 and Schottky TTL, it can be seen that a crossover point is somewhere around 10 MHz. With other termination schemes for the ECL gates, the crossover would shift upward.**

D. NOISE MARGIN AND NOISE GENERATION

Noise problems, for any logic family, are dependent on generated noise, logic noise immunity, and impedances of interconnecting lines.

The noise margin guaranteed for a logic type can be determined from data sheets. In absolute numbers, ECL 10,000 circuits are guaranteed from 125 mV worst case noise margin, and Schottky-TTL with 300 mV.

The amount of noise generated in a system is related to the signal edge speed (rise/fall times) and signal amplitude. These two factors are key variables when computing "crosstalk" -- spurious signal coupling between signal interconnect lines.

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*50 percent duty cycle.
**MECL System Design Handbook, Second Edition, P. 90.

ECL 10K rise and fall times are controlled to 3.5 ns (typical, 10 percent to 90 percent). Faster edge speeds are less desirable from the viewpoint of crosstalk.

Experimental testing has shown Schottky-TTL has an approximate 3 ns 10 percent to 90 percent edge speed, but this testing has been done at Motorola. It is not specified on Schottky-TTL manufacturer's data sheets.

Logic swings for ECL 10K are typically 800 mV; for Schottky - TTL about 3 volts. Therefore, as seen in Figure 4-4, the signal edge slope for ECL 10,000 is only 183 mV/ns, compared to 800 mV/ns for Schottky TTL. So, considering edge speeds alone, Schottky TTL circuits generate more than four times as much system noise as ECL 10,000. Switching transients at the TTL totem-pole outputs contribute significant additional noise.

It is true that Schottky TTL can operate with higher noise levels on input lines than can ECL. However, Schottky TTL circuitry generates higher levels of noise and has higher input impedances than does ECL; the net result of all these factors is that ECL modules are less susceptible to self generated noise than are TTL modules.

From a noise standpoint, the combination of ECL and TTL on the same module would be very bad. TTL would generate high noise, and ECL would be susceptible to this noise.

CIRCUIT CHARACTERISTICS		
PARAMETER	ECL	TTL-S
Noise Margin	125 mV	300 mW
Logic Swing	800 mV	3.0V
% of Logic Swing	15.6%	10%
Edge Speed	183 mV/ns	800 mV/ns
Rise Time 10-90%	3.5 ns	3.0 ns

Figure 4-4. Circuit Characteristics ECL 10,000 and Schottky TTL Circuits

V. MECHANICAL DESCRIPTION

The following assembly techniques were considered: multilayer printed circuit, wire wrap, stitch wire, and multiwire. Autonetics has vast experience in the first three of these wiring techniques. Since the multiwire technique offers no advantage over stitch wire and we have less experience and less support equipment for this approach, it was discarded. It was felt that a wire wrapped module, while easy to assemble for breadboard operations, gives a "breadboard" unfinished appearance to a module which would be undesirable since it is assumed that this module will be extensively exhibited as a feasibility demonstrator.

A multilayer printed circuit module represents the most desirable and economical assembly for a large production run of a given module type. It is felt that a printed circuit card would be the best "showpiece" for a feasibility model also. Autonetics has had experience in multilayer printed circuit cards and feels that this technique could be used successfully in the construction of this module. The FTAS video generator, as shown in Figure A-1 of Appendix A, is an example of an Autonetics multilayer module utilizing 10,000 series ECL components. However, there are three disadvantages in using a multilayer printed circuit module for a "first of a type" module:

1. Subtle design changes or accidental original wiring errors are difficult to repair on a multilayer PC board. In board construction the inter IC signal connections are constrained, as much as possible, to the outside layers so that cut-track and jumper techniques can be applied to simplify circuit modification. This might result in jumpers on the PC module which would detract from its professional "finished" appearance.
2. The layout and fabrication costs of multilayer PC modules are high, and it would be best if this were done only once after proper circuit operation has been confirmed.
3. Of utmost importance, the fabrication time of multilayer boards is quite long (four to eight weeks). If sufficient schedule time were allocated to precisely check the design, insuring a minimum number of wiring changes, and sufficient time were scheduled for PC board layout and fabrication, a

PC board assembly scheme would be utilized. However, considering the schedule, a stitch wire assembly technique was chosen. Stitch wire assembly will provide rapid board assembly to insure that fabrication and test schedules are met. Machined pin sockets for the integrated circuits will be used, allowing IC removal to facilitate test and troubleshooting.

Planar Stitch-Wire (PSW) is a point-to-point wiring technique used for interconnecting integrated circuits and discrete components on a special printed circuit board. PSW boards provide the same density and low profile as multilayer printed circuit boards and the same low engineering cost, rapid turnaround time and ease in making wiring changes as wirewrapped boards.

PSW uses a continuous wire, through-insulation welding system for bonding the wire to the pads on the board. The technique allows high wiring speeds for both manual and semi-automatic stitch-wire machines and low profile wiring -- typically .100 to .150 inch.

The low profile wiring and component mounting allow PSW boards to be mounted on .5 inch centers with the same number of ICs per square inch as wire-wrapped boards or 6 to 8-layer multilayer boards. A variety of patterns can be used that accept any dual inline package and practically any discrete component and accommodate edge finger type I/O connectors. The board will be supplied with machined socket pins for plug-in component mounting.

A low noise environment compatible with high speed TTL and ECL circuits is provided by the large power and ground planes on opposite sides of the board, the proximity of the wiring to the ground plane, and the use of distributed decoupling capacitors. For very high speed, noise sensitive signals, twisted pair wiring will be used the same as in wire-wrapped cards. A detailed drawing of the module cross section is shown in Figure 5-1 which illustrates the power and ground planes.

PSW boards are wired on the rear of the board using point-to-point or routed wiring. Both manual and semi-automatic stitch-wire machines and wiring services are available either within Autonetics on its own wiring machines, or directly from APAC which is located in the local area of Autonetics. Wiring changes can be made quickly and easily using a manual machine or by hand soldering wires in the plated-thru holes.

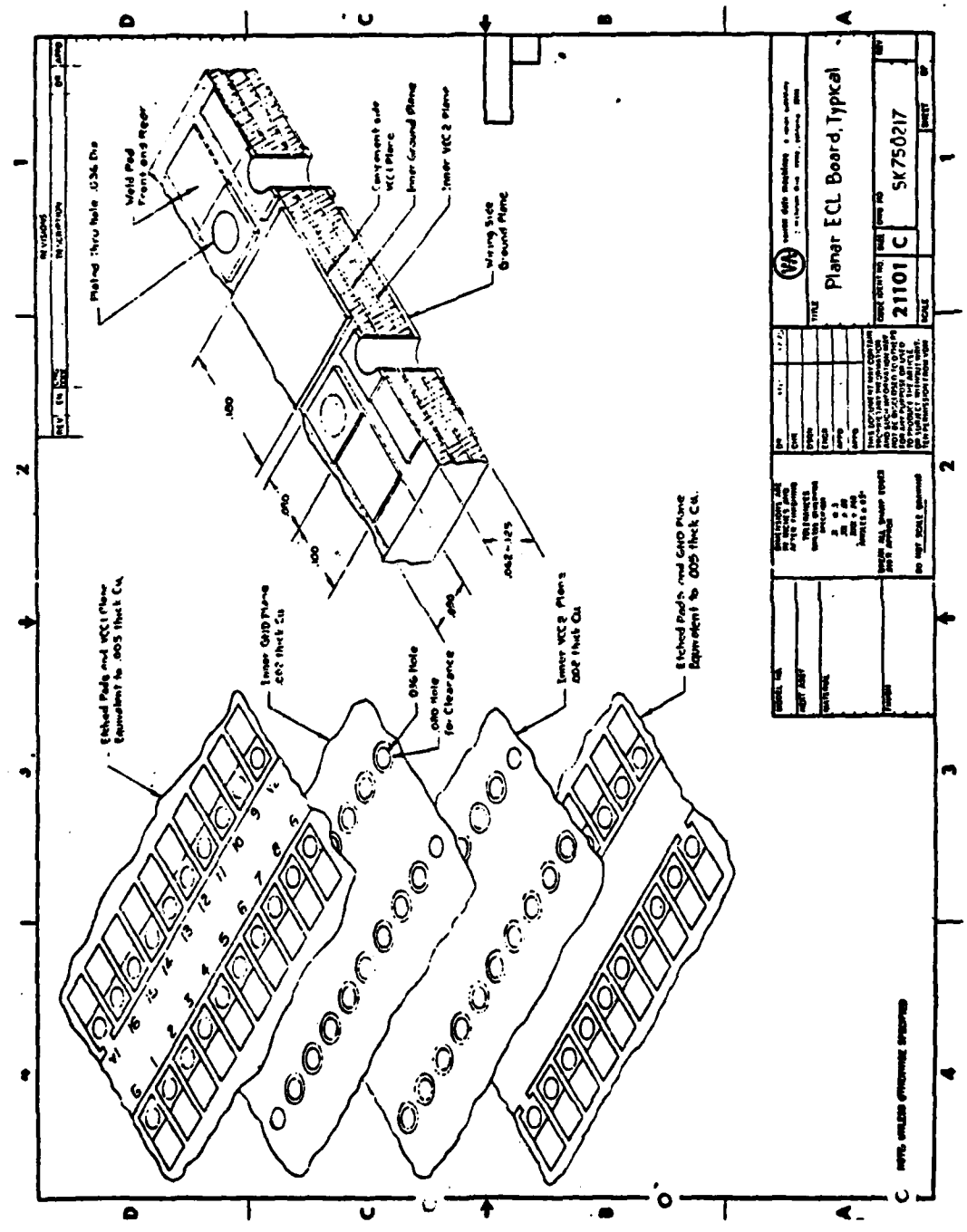


Figure 5-1. Typical Planar ECL Board

Stitch-Wire boards have been used for over four years in all phases of military and commercial electronics including ground, shipboard, airborne and space applications. The high bond strength, typically five pounds, allows PSW boards to be handled with minimum care and to meet the most severe environmental requirements.

Computer aided design programs will be used for wire lists allowing a rapid, economical and accurate transition from design to hardware.

The PSW board configuration in Figure 5-2 shows 18, 24 pin and 139, 16 pin dual in-line packages with five 16-pin spare positions. This configuration represents 133 active devices and 24 integrated resistor packages. Dimensions of the board are 10.50 in. wide x 11.60 in. high x .062 in. thick. The I/O connector configuration consists of two dual 4-pin edge finger connectors (176 pin total) at the bottom of the board (Masterite P/N DD8GR44-DR-H-AH).

Listed below is the tentative schedule of module edge connector interface pins and their function:

Quantity of Pins	Function	Logic Level
108	Rotating Accumulator Data	ECL
16	Dual Hydrophone Digital Outputs	TTL
4	Dual Hydrophone Analog Outputs	Analog (Shielded)
8	Data Input	TTL
16	Computer Interface (Data)	TTL
8	Clocks & Timing Interface	TTL & ECL
4	Power	
4	Ground	
8	Shield Returns (for ECL Data)	ECL

The module will require ±5 volts DC and ±12 VDC power.

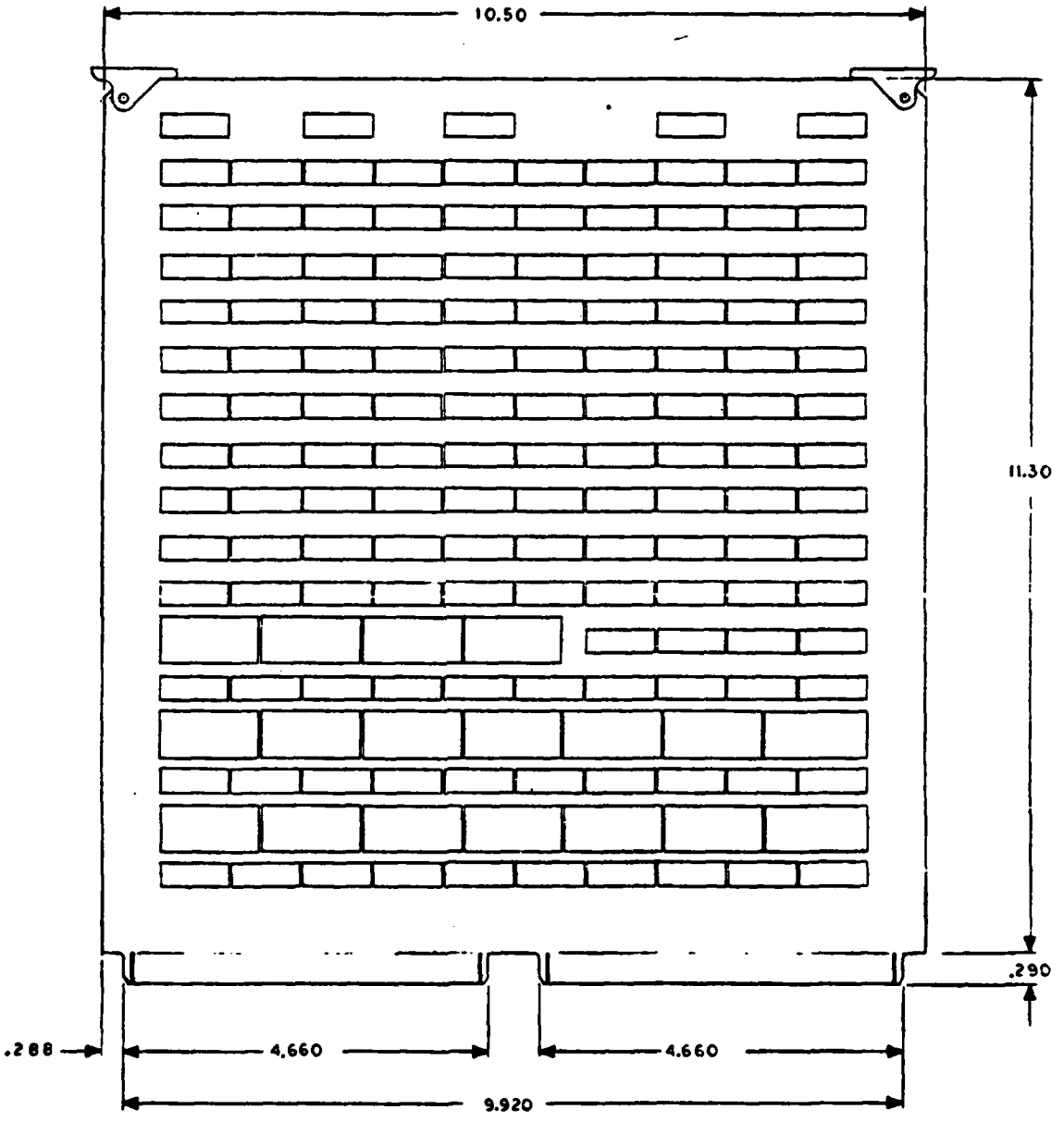


Figure 5-2. PSW Board Configuration

VI. THERMAL CONSIDERATIONS

The Distribution and Summing Module has a power dissipation of approximately 55 watts. A cooling air flow rate of 10 cubic feet per minute in a 25°C environment is required to limit the exhaust temperature to approximately 35°C. This flow rate will equal or exceed the 400 ft/min air velocity which is suggested by the component manufacturer for forced convection cooling.

When the modules are installed in an equipment drawer with close module spacing, economical utilization of space will require the use of 400 Hz fans to provide the necessary supply pressure to achieve this flow rate. The estimated supply pressure is 1.5 in. of water.

With these cooling conditions the average component temperature rise above ambient is 15°C.

Summary of Typical Cooling Situation

Power Dissipation	55 W Per Board
Inlet Temperature	25°C
Exhaust Temperature	35°C
Typical Component T	15°C above Ambient
Cooling Air Flow	10 CFM Per Board
Drawer Pressure	1.5 in. H_2O
Fan Type	400 Hz Aximax or Propimax or equivalent

Detailed thermal analysis is included in Appendix B. This analysis is conservative and represents a maximum worst case thermal situation.

APPENDIX A. RELATED EXPERIENCE AND TESTING FACILITIES

Autonetics has a well known capability in almost every discipline involved in the development and manufacture of electronics products. To describe all those products that are related to the Electronic Distribution and Summing Element would be a gigantic task.

The examples that will be mentioned in the following paragraphs are digital sonar systems that were developed by the same personnel who will, if Autonetics is awarded a contract as a result of this proposal, develop the Electronic Distribution and Summing Element. These are all high speed digital systems.

There are adequate testing and measuring facilities available in the Anaheim plant to test and measure the performance of the Electronic Distribution and Summing Element. Autonetics systems are generally tested at the circuit module level, functional chassis level, subsystem level, and total system level, all with Rockwell testing procedures and facilities.

SIGNAL PROCESSING SYSTEM

PURPOSE

The Signal Processing System is an all-digital machine which provides precision spectral analysis of wide dynamic range audio signals in 12 simultaneous channels. In addition to the basic discrete fast Fourier transform unit, the system includes a digital prefilter to provide broadband and vernier modes. Numerous input, output, and intermediate processes are selectable to provide a range of analysis and display options. Operator input is via a teletype or CRT terminal to the control subsystem minicomputer which in turn provides microprogramming to the system. Displays include annotated electrographic recorders, x-y plotter, high speed printer, or x-y CRT. The system is mechanized with bipolar logic for high-speed arithmetic operations, and MOS shift registers for memory.

FEATURES

Total Digital Processing; Programmable Digital Prefilters

Minicomputer Control Subsystem

Preconditioning

- 12 Remote Amplifiers for 12 analog inputs
- 12-Beam Beamformer for 50 analog inputs

Analysis

- 12 channels selectable from any combination of 24 digital and 12 analog inputs

Mode Selectable

- Full band coverage up to 16 kHz
- Vernier band coverage up to 16 kHz bandwidth
- Selectable prefilter widths up to 20 kHz (100 kHz on one channel)
- F_c variable over 20 kHz (100 kHz on one channel)
- DEMON (AM sideband analysis)

Fast Fourier Transform; High Thruput Speed Continuous or Blocked Data

- Forward or Inverse Transforms

Analysis Filter Bandwidth 0.001 Hz to 4 Hz

3-Frequency/Phase Trackers

Record Annotation for: A/D Overload, Transient Data, Average Channel Energy, (Typical Encoding).

Frequency Markers and Cursors

Automatically Printed Test Records

Outputs:

- Electrographic Recorders
- X-Y Graphical Plotter
- Alphanumeric Printer
- Headphones

Four Formats for each Electrographic Recorder

Post Detection Integration for X-Y Plotter

Audio Processing Channel

Transient Detectors

Self-Test Capability

MOS Memory

Operator Manual Test Capability

Construction to Best Commercial Practice

Figure A-2 is a photo of the Signal Processing System.

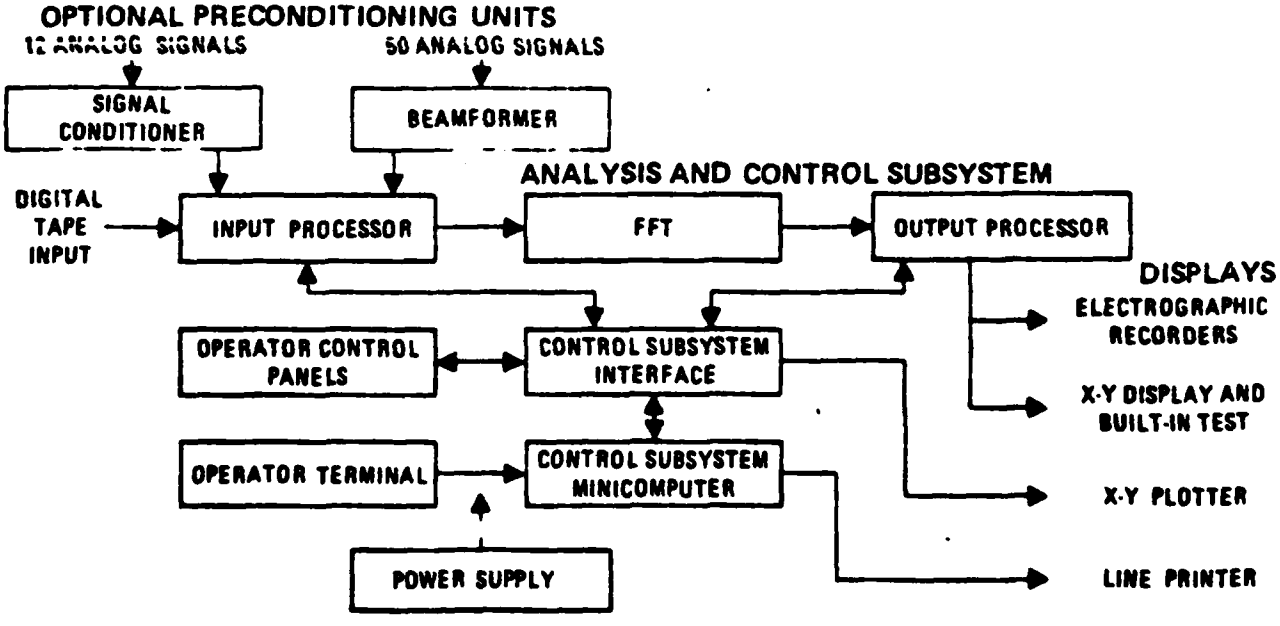


Figure A-1. Block Diagram of SPS

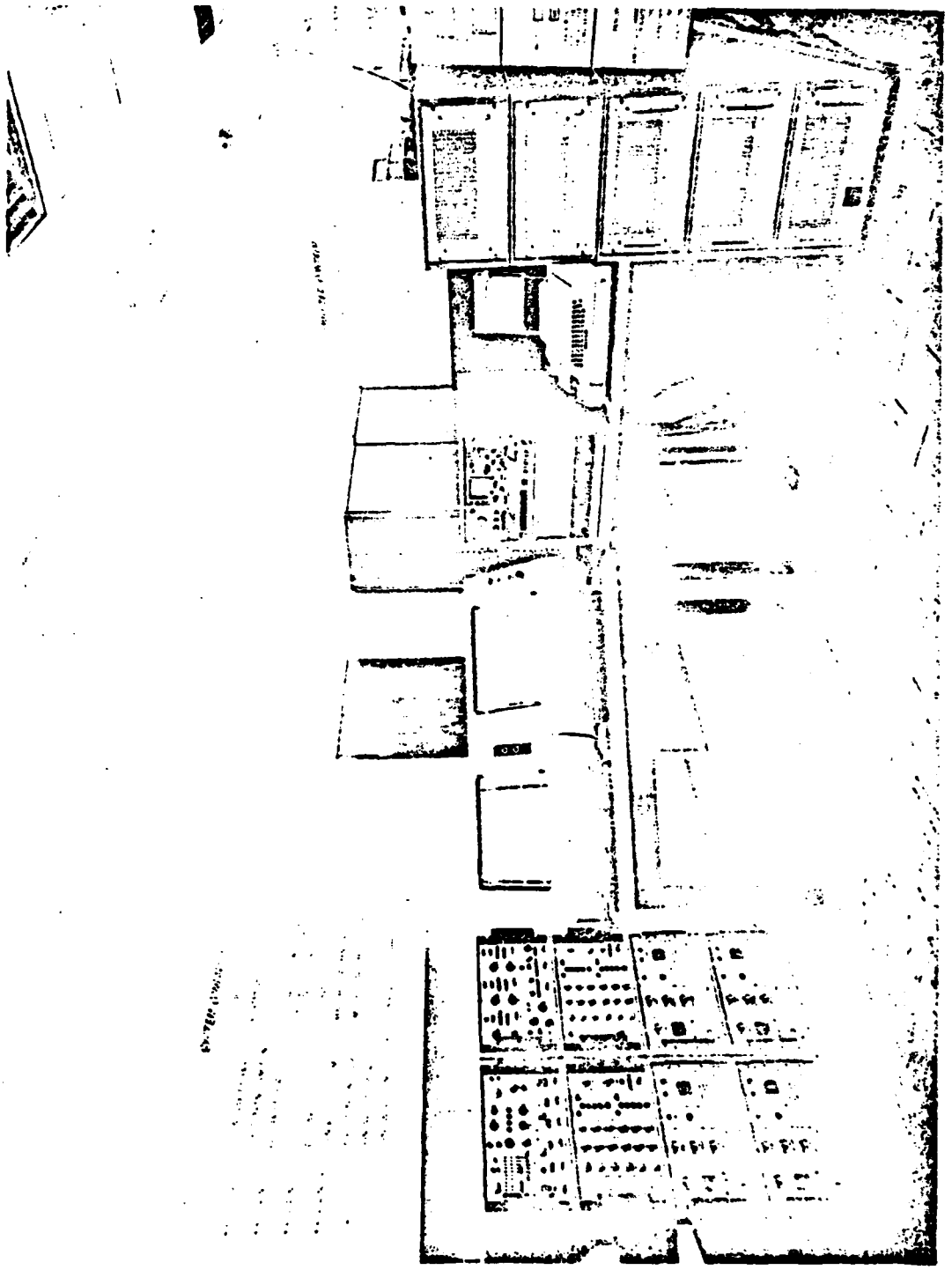


Figure A-2. Signal Processing System

T75-344/301

HIGH-SPEED MULTI-CHANNEL FOURIER ANALYSIS SYSTEM

PURPOSE

The Fast Time Analyzer System is an all-digital electronic processor which provides precision spectral analysis of wide dynamic range audio signals in nine simultaneous channels. The all-digital design provides greater accuracy, dynamic range, stability, linearity and flexibility than analog or other possible designs. A CRT data terminal and a minicomputer control subsystem provide the operator a wide variety of input, output, and intermediate processes. The mechanization includes multi-signal conditioning, mixing, filtering, memory, time-to-frequency transformation and processing for presentation in a variety of display options. MOS shift registers are used in memory, and bipolar logic is used for high-speed arithmetic operations.

Figure A-3 is a block diagram of the system.

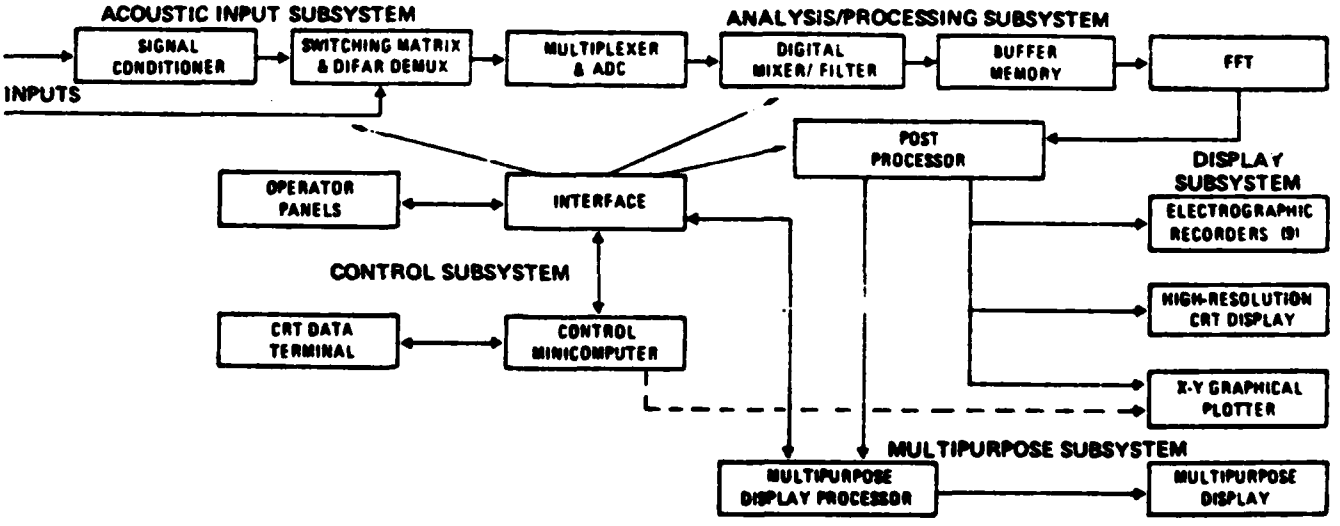


Figure A-3. .Functional Block Diagram of FTAS

FEATURES

All Digital Processing

Programmable Digital Filters; Changed by Software

Minicomputer Subsystem Control; CRT Data Terminal

Preconditioning

- Six amplifiers for six real-time inputs
- Three 3-channel carrier sideband demultiplexers

Analysis

- Nine channels selectable from any combination of 84 recorded and six real-time inputs
- Up to eight-times real-time data analysis

Mode Selectable, each channel

- Full band coverage
- Vernier band coverage
- Splitband (simultaneous Vernier and full band analysis on one channel)
- Selectable prefilter widths
- F_c variable

Processing Options

Fast Fourier Transform High Thruput Speed

- Continuous or blocked data

Interacting Display Consoles; Operator Flexibility

Annotation Records

- Heading, Bearing, Time Code, Frequency, and Cursors

Outputs

- Electrographic Recorders (9)
- X-Y Graphical Plotter
- Multipurpose Display
- High Resolution CRT Display
- Headphones (null-steering)

Six Data Type Formats for each Electrographic Recorder

Post Processing

Short/Long Term Integration
Auto Detection
ALI/Bearing Traces, Tableaus
Audio Null Angle Processing
Manual/Self-Test Capability
MTBF 500 Hours
Construction to Best Commercial Practice

Modular concept permits adaptability to specific requirements.

Figure A-4 is a photo of the FTAS

PROGRAMMABLE TWELVE-BEAM BEAMFORMER

PURPOSE

The twelve-beam beamformer (TBBF) is used to sum the outputs of the hydrophones in an array in such a way as to enhance the signals from distant targets in a particular direction relative to the noise signals. This is done by digitizing the signal from each hydrophone, delaying it by some time determined by hydrophone position and beam steering angle, multiplying it by an appropriate shading coefficient, and summing it with the signals from all the other hydrophones. It is necessary, in the general case to operate with arrays of arbitrary configuration, of differing bandwidths, and it is necessary to change the direction of beams easily and rapidly.

FEATURES

Analog Gain	0-42 dB in 6 dB steps
Sample Rate	Selectable, 20.8 kHz max
Dynamic Range	8 bit digital representation of individual hydrophone signals
Weighting	Arbitrary, independent for each beam
Max Dimension of Array	Corresponds to 256 sample periods
Number of Beams	12, individually steerable by programming

Figure A-5 is a photo of the Programmable Twelve-Beam Waveformer.

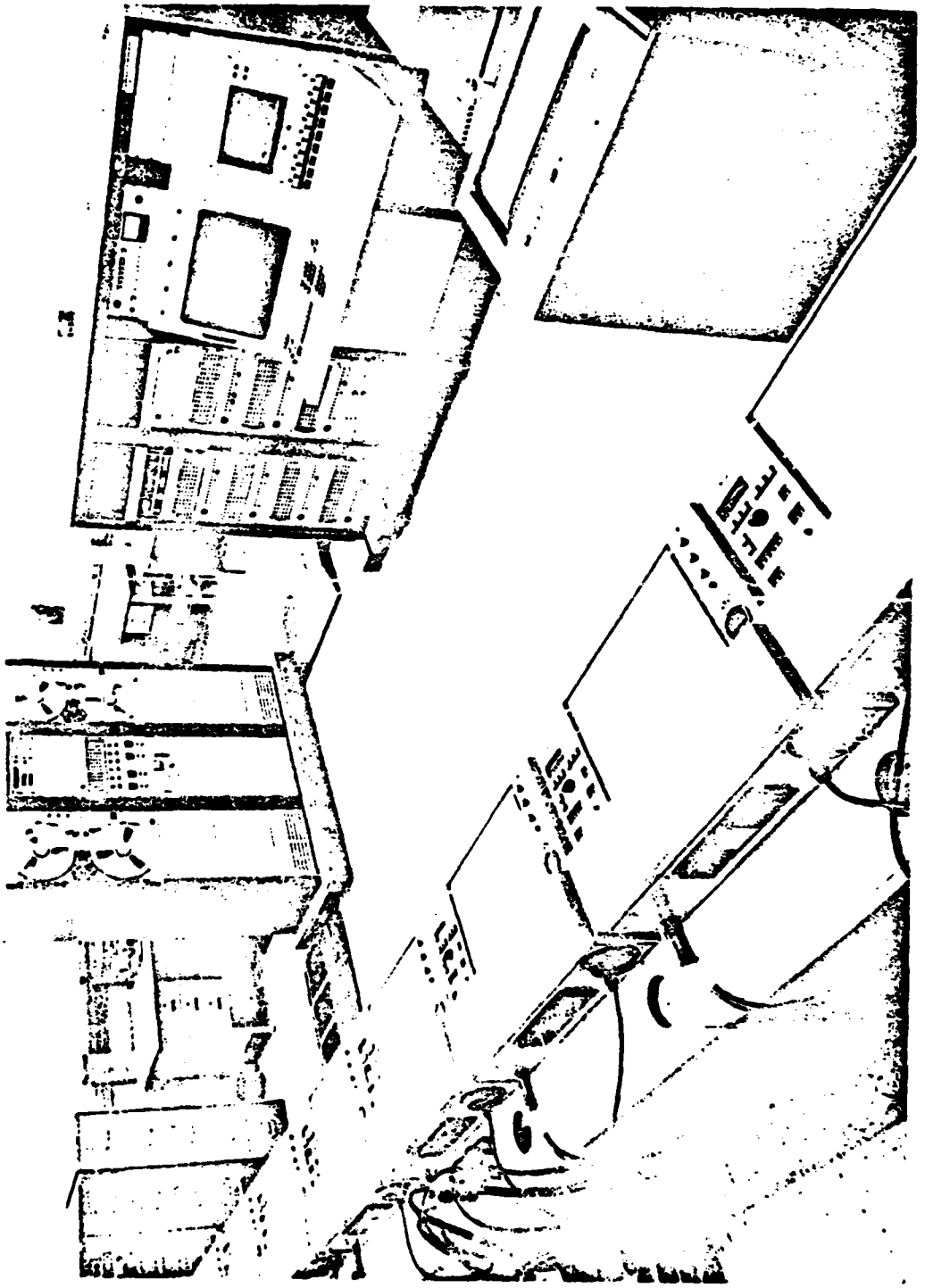


Figure A-4. FTAS

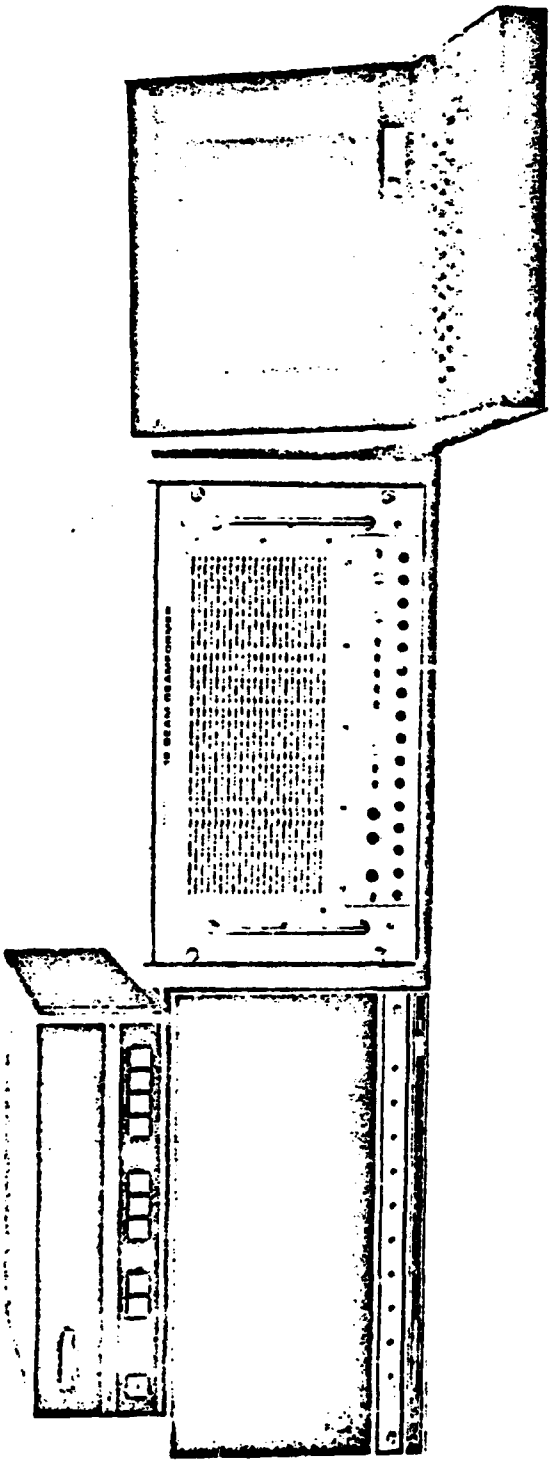


Figure A-5. Programmable Twelve-Beam Beamformer

T75-344/301

VIDEO GENERATOR MODULE FOR FTAS

PURPOSE

The video generator module receives sets of numbers from the computer in TTL logic form, converts them into ECL levels, and then operates on the numbers to furnish four output driving signals to a display: (1) horizontal sync, (2) vertical sync, (3) an on-off video signal which blanks and unblanks the CRT beam, and (4) an intensify signal, which, when on, orders the CRT trace intensified.

FEATURES

- 70 ICs of ECL 10,000 series
- Converts from TTL to ECL 10,000 levels
- Operates at 50 MHz
- Generates signals to form coordinate lines, operator controlled cursors, calibration lines, and alphanumeric characters or a 1600 x 1600 matrix.

Figure A-6 is a photo of the video generator module.

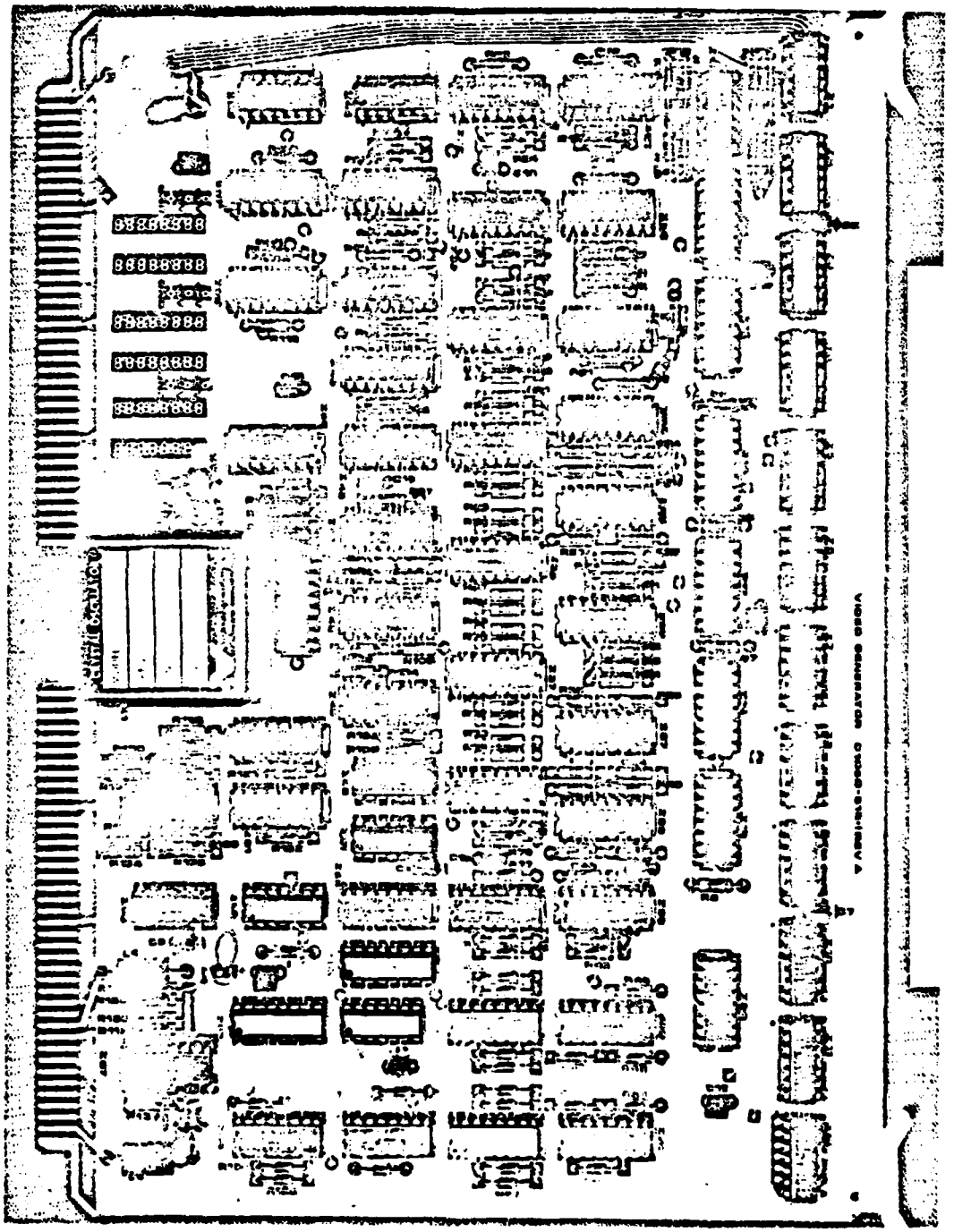
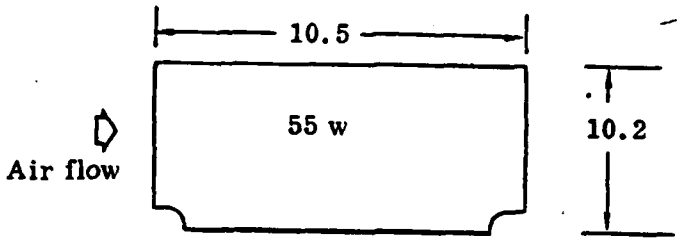
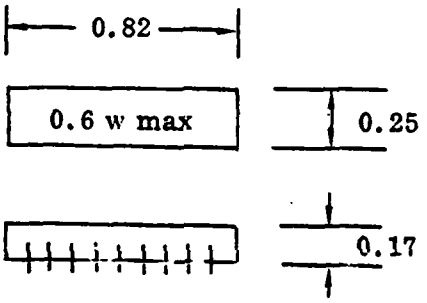


Figure A-6. Video Generator Module

APPENDIX B.
DISTRIBUTION AND SUMMING MODULE THERMAL CALCULATIONS



Approximate Module Size and Power



Approximate 16 Pin DIP Size and Power

Assumptions

1. Module dissipation = 55 w
2. DIP dissipation = 0.6 w max
3. Ambient temperature = 25 C
4. Exhaust temperature = 35 C
5. Component clearance to adjacent board = 0.25 in.

Required airflow for total module

From cooling air heat balance, mass flow,

$$\dot{M} = \frac{q}{c_p \Delta T}$$

$$= \frac{55 \times 3.41}{0.24 \times 10 \times 1.8} = 43.4 \text{ lb/hr per module}$$

and volume flow,

$$Q = \frac{\dot{M}}{\rho} = \frac{43.4}{0.075 \times 60} = 9.6 \text{ CFM per module (Use 10 CFM)}$$

Component ΔT

From manufacturer's data, 16 pin DIP thermal resistance with air flow velocity of 400 FPM is

$\theta_{ja} = 50°C/w$ and

$\theta_{jc} = 25°C/w$

This gives

$\theta_{case\text{-}amb} = 50\text{-}25 = 25°C/w$

and maximum component

$\Delta T = 0.6 \times 25 = 15°C$

With the assumed module spacing, the airflow channel cross-sectional area is approximately

$$A = 10.2 \times 25 = 2.55 \text{ in}^2$$

$$\text{Velocity } V = \frac{Q}{A} = \frac{9.6 \times 144}{2.55} = 542 \text{ FPM}$$

This somewhat exceeds the manufacturer's recommendation of 400 FPM and ensures conservative cooling conditions.

Analytical Confirmation of Manufacturer's Data

Reynolds Number

$$4\,rh = \frac{0.25 \times 10.2}{2(0.25 + 10.2)} = 0.01 \text{ ft}$$

$$\frac{\dot{M}}{A} = \frac{43.4 \times 144}{2.55} = 2450 \text{ lb/ln ft}^2$$

$$N_R = \frac{\dot{M}}{A} \times \frac{4\,rh}{\mu} = \frac{2450 \times 0.01}{0.097} = 521$$

$N_R < 2000$ indicates a laminar flow regime.

Heat Transfer Coefficient

For laminar flow in a rectangular channel, (Compact Heat Exchangers, Kays and London, Figure 6-3).

$$a/b = \frac{0.25}{10.2} = 0.025$$

$$N_{N_u} \approx 7.5 = \frac{4r_h h}{R}$$

$$h = \frac{7.5 \times 0.0149}{0.01} = 11 \text{ Btu/hr ft}^2\text{F}$$

Average Component ΔT

Total exposed area $\approx 10.2 \times 10.5 = 107 \text{ in}^2$

$$\overline{\Delta T} = \frac{q}{hA} = \frac{55 \times 3.41 \times 144}{11 \times 107 \times 1.8} = 12.75^\circ\text{C}$$

This agrees well with manufacturer's data for individual components which gives 15 C ΔT.

Definition of Symbols

- q - Power dissipation, watts or w
- $\dot{M}$ - Mass flow rate, lb per hr
- C - Temperature, degrees Celsius (Centigrade)
- F - Temperature, degrees Fahrenheit
- in. - Length, inches
- ft - Length, feet
- C_p - Specific heat, Btu per lb F
- ΔT - Temperature difference, degrees F or C
- Q - Volume for rate, cubic feet per minute or CFM
- θ_{ja} - Thermal resistance, junction to ambient, degrees C per Watt or C/W
- θ_{jc} - Thermal resistance, junction to case, degrees C per Watt or C/W
- $\theta_{case\text{-}amb}$ - Thermal resistance, case to ambient degrees C per Watt or C/W
- A - Area, square inches or in^2
- V - Velocity, feet per minute or FPM
- N_R - Reynolds Number, dimensionless
- $4r_h$ - Hydraulic diameter, ft
- μ - Viscosity, lb per hr ft or lb/hr ft
- a/b - Aspect ratio, dimensionless
- N_{Nu} - Nusselt Number, dimensionless
- h - Heat transfer coefficient, Btu per hr square ft degree F or Btu/hr ft^2F

APPENDIX C. MODULE TEST PROGRAM

Elementary dynamic tests can be made on the module utilizing a test chassis and commercial test equipment. Data inputs can be simulated with counters, and waveforms can be monitored at various points in the circuit with an oscilloscope and a high speed DAC (15 ns) to verify proper operation. These techniques will be used in the early phases of troubleshooting and wiring debug to verify proper operation of all subcircuits on the module.

Detailed testing which verifies module operation in a simulated system environment is somewhat more difficult since the module must be "programmed" by loading data which, in normal operation, is supplied by a general purpose computer. Another item which makes testing more difficult is the simulation of the interfaces with other modules at the output accumulators since this module normally forms a computational link with many other like modules.

The following detailed test set up (see Figure C-1) will accomplish the module test with a minimum of cost while simulating the actual function of the module within the CSTL system.

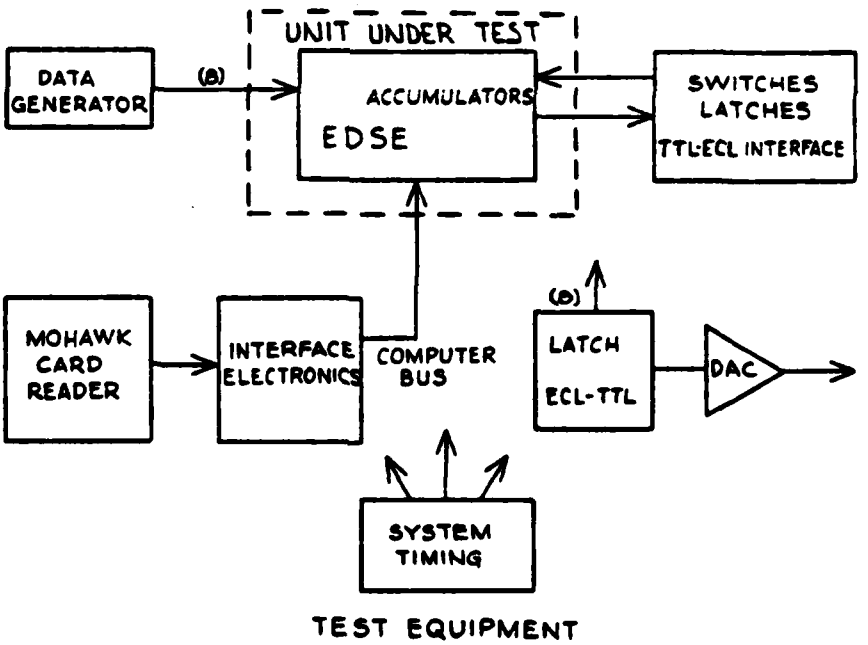


Figure C-1

A computer interface will be simulated with specially constructed test equipment hardware on a wire wrap circuit card. This circuitry will accept data from a Mohawk card reader and will simulate the data bus which will supply computer data to the array simulator modules in the system configuration. The output of this special test circuitry will be in the same form as data which will be received from the CSTL control computer and its associated interface module in the actual system. Delay and coefficient data will be loaded into the array simulator module with a manually executed command to the special test equipment.

An easily recognizable 8-bit (two 4-bit words) digital signal (i.e., ramp) will be generated in the special purpose test equipment and applied to the data inputs of the array simulator module.

An 11-bit ramp or its complement will be loaded into the delay and coefficient RAMs. This will completely test every address and every bit of the 2048 x 11 RAM. During one 2048 operation cycle, all 256 addresses of the Data RAM will be read eight times, once for each of the multiplier factors. The fast DAC will output the sliding and variable slope ramps building in the accumulators, and since the two 4-bit input words are the same, the slow output DACs will have identical final DC values for comparison.

These tests will verify proper operation of all addresses and bits in the RAMs and ROMs. They will also fully test the accumulator, going through the worst case carry time delays.

In addition to verifying basic operation of the module, Autonetics will test the circuit under various environmental conditions. We will inject spurious noise into the power supply lines to check noise immunity. We will also vary the temperature over the extremes mentioned in the thermal design section. While at the elevated temperature, we will measure the actual, worst case timing margins in the critical timing areas, to verify that the margins are at least what were predicted in the timing analysis.

Outputs from both the high and low speed DACs will be observed with an oscilloscope. The ramp inputs simulating the delay and weighting coefficients will be selected such that comparison of the phase and amplitude of the output DAC waveforms will verify correct module operation under dynamic conditions. For this test four external ECL registers and switches in the test equipment will simulate the other accumulators in the future system.

Photographs will be taken to provide a historical record of the acceptance test.