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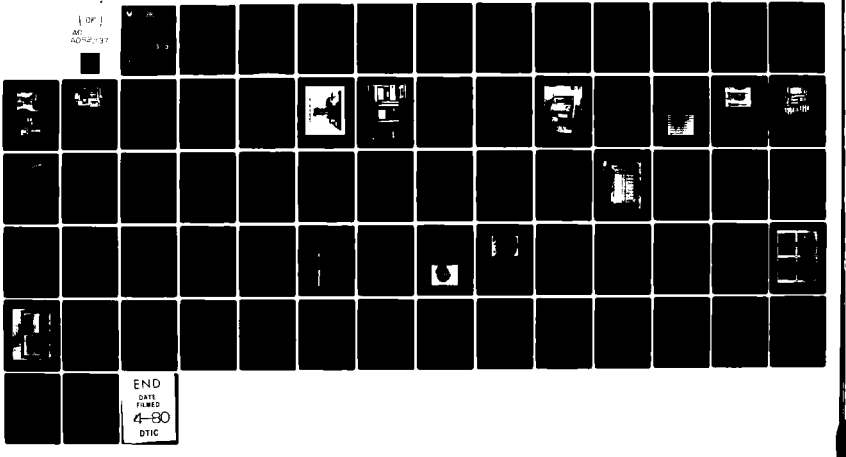

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IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

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In distinct contrast with much of the currently published e-beam direct writing work that seeks to demonstrate improved device performance and packing density capabilities, the object of this program was to develop a manufacturing capability for standard bipolar circuits of conventional design using existing e-beam direct writing equipment. In particular, a pilot-line demonstration of significant yields of conventional 4-5-μm design rule integrated circuits which were fully tested to military specifications for performance, quality and reliability was of paramount importance. Achievement of this objective then establishes a baseline for direct e-beam writing in production and provides a significant stepping stone for implementation of e-beam technology in VLSI circuit fabrication.

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The vehicle used for this demonstration was a standard TTL 256-bit bipolar RAM (SN74S201A) using a single-level metal, junction isolated, Schottky clamped bipolar process. Emphasis was placed on utilizing a new class of high-speed electron resist (TI-309 and TI-313) in combination with selective plasma etching techniques in order to establish economical next generation VLSI processes. A vector scan, laser controlled e-beam direct writing system ~~(EBMIII)~~ developed ~~in our laboratories~~ with fully automatic slice alignment was used for patterning of these devices. To determine that e-beam direct writing yields devices with no degradation in performance or reliability, optically patterned split lot controls were fabricated in parallel and used for comparative testing.

~~On this contract~~ it has been demonstrated that e-beam lithography can be used to fabricate bipolar devices to military specifications with no yield degradation or damage. No conclusive yield improvement results were demonstrated since this device is not limited in yield by lithographic factors, but rather by diffusion processes. This program has established an e-beam lithography baseline process utilizing high-speed electron resists and plasma etching techniques for fabrication of bipolar microcircuits. These processes will allow fabrication of many high density VLSI devices in the near future and have already allowed fabrication of a 1 ~~μm~~ minimum feature size e-beam SBP0400E I^2L 4-bit microprocessor. In general, e-beam technology ~~will allow~~ greater circuit design complexity and flexibility leading to better performance, lower cost, higher ~~reliability~~ integrated circuits.

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SECTION I
INTRODUCTION

Since the invention of the integrated circuit, lithography has been the key factor limiting device yield, feature size and chip size. Major improvements in lithography over the last two decades have resulted in significant cost reduction, better device performance and greater device complexity. Electron-beam writing systems using a computer to generate the pattern by controlling the deflection of the electron beam are attractive for rapid device design, mask fabrication and high yield device processing because they permit delineation of microcircuit patterns from computer data. These e-beam systems are also advantageous for high frequency and high packing density microcircuit fabrication because they permit higher resolution and better dimensional and placement (alignment) accuracy than achievable with photolithographic techniques.

An exploratory e-beam lithography program was started in 1966 at Texas Instruments Limited in Bedford, England. In 1970 the program was transferred to Dallas and during 1972-73 all e-beam patterned microwave transistors (U.S. Army Electronics Command, DAAB05-71-C-3715) were fabricated on a research e-beam machine (EBMI) with 0.5-μm emitter widths and ± 0.2-μm alignment accuracy utilizing computer-controlled registration. These results showed clearly that e-beam direct slice writing had major advantages over other imaging techniques in terms of resolution, dimensional control and alignment accuracy.

The major problem that limited the implementation of e-beam direct writing on the production lines was the long exposure time per wafer and associated overhead time. A long-range program was initiated at Texas Instruments to increase the throughput of this type of instrument. The first step was to develop an electron-beam machine for fabrication of master masks (1X) and reticles (10X). This instrument (EBMII) was implemented in the photomask production facility in 1974 and has been in operation since that time impacting master mask quality and turnaround. This e-beam system (EBMII) allowed a throughput of 2-4, 3 inch masks or reticles per hour and had a resolution of 1-1.25 μm and a pattern overlay accuracy of ± 0.25 μm. For direct slice writing, the resolution and pattern overlay accuracy of EBMII was certainly adequate for the next two generations of device designs, however, a five times improvement in throughput was necessary for economic considerations.

For these reasons, the program was divided into two parallel parts. One part was to begin development of a new high throughput e-beam machine (EBSP) and the other part was to develop the electron resists and the etching processes necessary for fabrication of micrometer and submicrometer design rule devices. This development could take place on EBMIII (duplicate of EBMII) in parallel with the development of the high throughput e-beam machine (EBSP). The first task in this part of the program was to develop the resists and the etching processes for fabrication of 5-μm design rule devices so that the basic e-beam technology could be established on a parity

basis with photolithography. The establishment of a 5-μm design rule, full military specification, e-beam integrated circuit pilot line capability (device vehicle – 256-bit bipolar RAM) was the main thrust of the contract in addition to making improvements in e-beam machine throughput by implementing higher speed electron resists (TI-309 and TI-313), developing automatic slice loading, and showing the feasibility of variable shaped beam (large beam/small beam) writing. Implementation of plasma etching and demonstration of e-beam direct writing 1.25 μm patterning capability for bipolar and NMOS devices were also accomplished as part of this contract. The development of the high throughput e-beam machine (EBSP), with the exception of the automatic loader, was accomplished on an internal program.

SECTION II
TECHNICAL DISCUSSION

A. E-BEAM MACHINE CAPABILITIES

Several different types of e-beam direct writing systems have been developed in the past few years. The approach taken at Texas Instruments was to utilize dynamic focusing and a computer-aided design deflection system to achieve large field coverage (6.35 mm × 6.35 mm) to minimize the step-and-repeat time required. A vector scan system was chosen because it is inherently 3-4 times faster than a raster scan system but the full advantage is only realizable with the elimination of, or compensation for, eddy currents. This has been accomplished on EBMIII with the use of ferrite liners and compensating hardware and software.

A vector scan system is limited in throughput (Figure 1) by the writing rate, the exposure rate, and several overhead factors (pattern overhead, step-and-repeat time, load/unload, automatic alignment). The writing rate is a function of the pattern generator, deflection amplifier and electron optics. The exposure rate is a function of the gun brightness and electron resist sensitivity. The writing rate and the exposure rate must be equal and thus the slower of these two rates will dominate. This relationship (Figure 2) is given by:

$$E \cdot D = \frac{S}{D} \cdot 10^4 \qquad (1)$$

where

E = inverse scan speed (ns/μm)

D = line density (lines/μm)

S = resist sensitivity (μC/cm^2)

I = beam current (nA)

The exposure time (s) is then given by:

$$T_E = E \cdot D \cdot A_G \cdot 10^{-1} = \frac{S}{I} \cdot A_G \cdot 10^3 \qquad (2)$$

where

A_G = area of exposed geometries (cm^2)

As can be seen by Equation (2), the exposure time can vary significantly in a vector scan system depending upon the particular pattern to be exposed. Using both a positive and negative resist, the average area for a typical static or dynamic MOS RAM or bipolar RAM is approximately 25% to 30% of the total chip area.

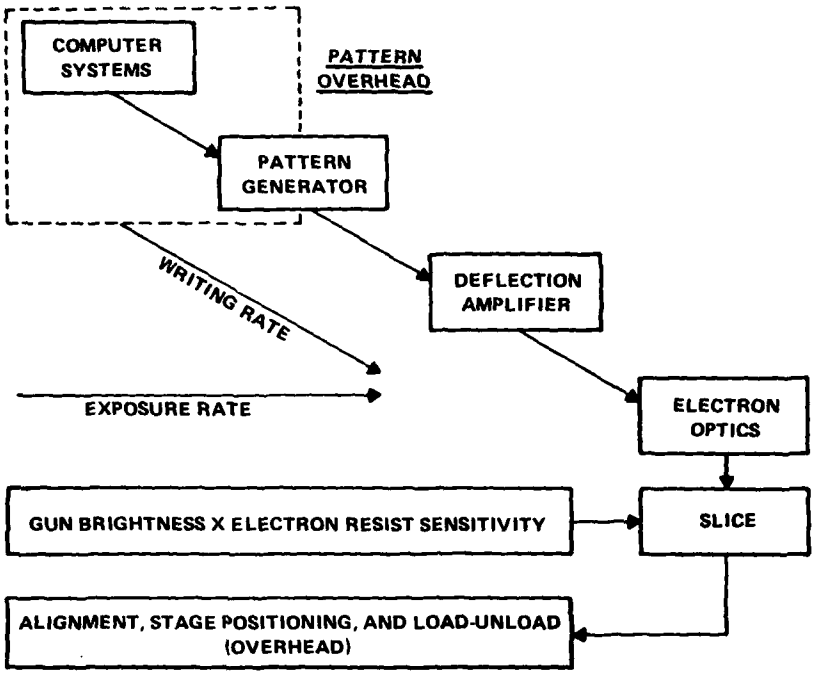

Figure 1. Vector Scan System

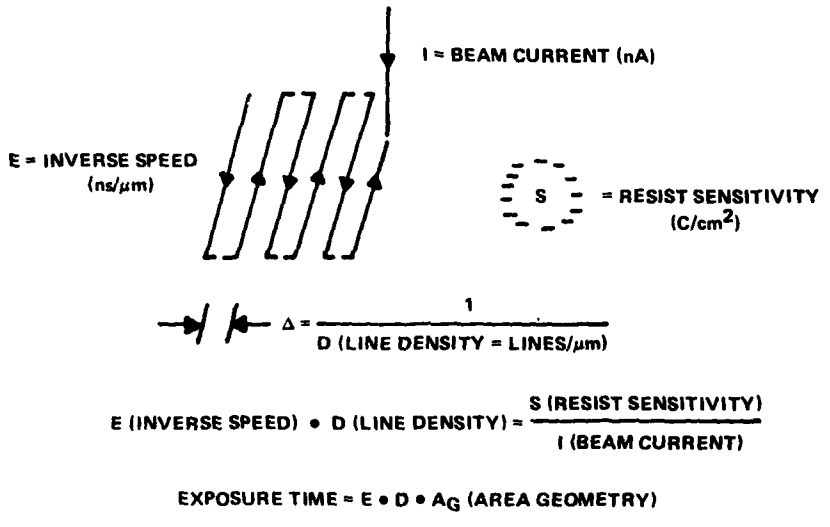

Figure 2. Inverse Speed/Line Density Relationship

The EBMII-EBMIII-type system was designed as a balanced system. The pattern generator electronics (interface), electron optics and deflection amplifier were developed to allow a system bandwidth or 2 MHz allowing beam scan speeds of 5 μm/μs. This is an equivalent "data rate" of 20 MHz for 0.25-μm beam spacing. The optics system allows a resolution of 1.25 μm over a 6.35 mm × 6.35 mm field and submicrometer features over a smaller field size ($\approx$2 mm × 2 mm). Large chip submicrometer devices are accomplished utilizing the laser interferometer capability of the system to "stitch" fields together ("mosaic" approach).

In addition to throughput and resolution, the other key factor of any imaging system is the pattern registration capability. Texas Instruments has developed and has used for several years a fully computer-controlled automatic alignment system on the e-beam machines. Pattern registration for slice printing is accomplished by scanning the electron beam across reference marks in the scribe lines of each chip on the silicon wafer, detecting and amplifying the secondary and back-scattered electrons, and processing this video signal to determine the correct position for the subsequently exposed pattern. This method allows a 3-σ alignment accuracy of ± 0.25 μm and 0.1-second alignment time per chip. A faster three-chip automatic alignment system was used on this contract. In this case, the x-y position of three chip sites is measured using the laser interferometer and the laser-controlled stage is corrected for x-y position, x-y gain, rotation and orthogonality of the chip array. The beam scan field is corrected in gain, rotation and orthogonality from marker measurements at one of the three positions. Subsequent placement of chips by the stage is then accomplished with ± 0.5-μm overlay accuracy.

Alignment data is acquired by scanning the beam over fiducial markers which are etched 4-5-μm deep into the silicon slice at the very first step. This is accomplished with standard photolithography and CF_4/O_2 plasma etching for convenience. It is necessary to use two marker sets because the first set becomes distorted by epi-shift during the growth of the epitaxial Si layer. The second set is optically aligned to the first set and this limits the alignment of the DUF to the remainder of the device to about ± 1.0 μm.

Pattern data for the SN74S201A devices is decomposed on an IBM 370 computer into trapezoidal figures. The decomposed figures are sized to allow for pattern growth during processing. The data is then transferred to EBMIII through the use of magnetic tape.

The EBMIII system is shown in Figures 3, 4 and 5, and a block diagram of the system is shown in Figure 6. The major features of EBMIII are listed in Table I.

The writing time for the EBMIII system is given in Table II. The 200 ns/μm inverse scan rate (or 5 μm/μs scan rate) and 0.25 μm beam spacing requires a beam current of 37.5 nA and a resist sensitivity (measured in micro Coulomb/centimeter^2) of 3 $\mu C/cm^2$. Both TI-309 and TI-313 have usable sensivities better than 3 $\mu C/cm^2$. The TI LaB_6 electron gun is capable of 37.5 nA in a 0.75 μm beam diameter. This is adequate to define geometries 2.5 μm or greater.

Figure 3. Electron Beam Slice Printer

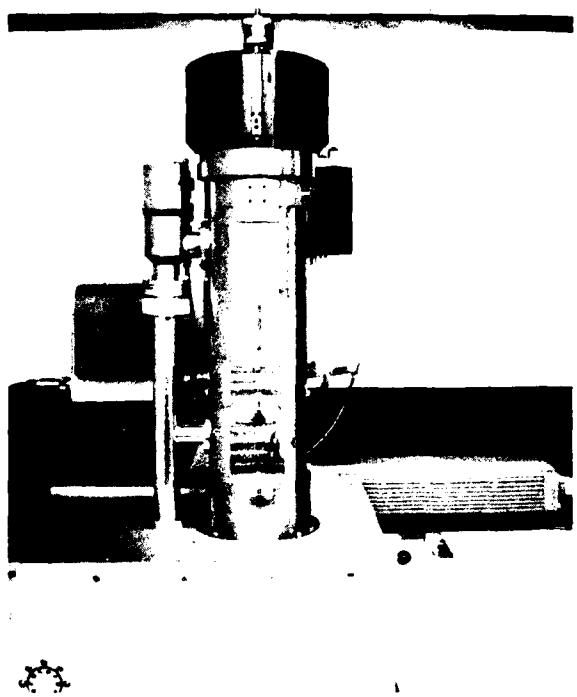

Figure 4. Electron-Beam Machine Electron Optical Column

Figure 5. EBMIII Computer and Peripherals

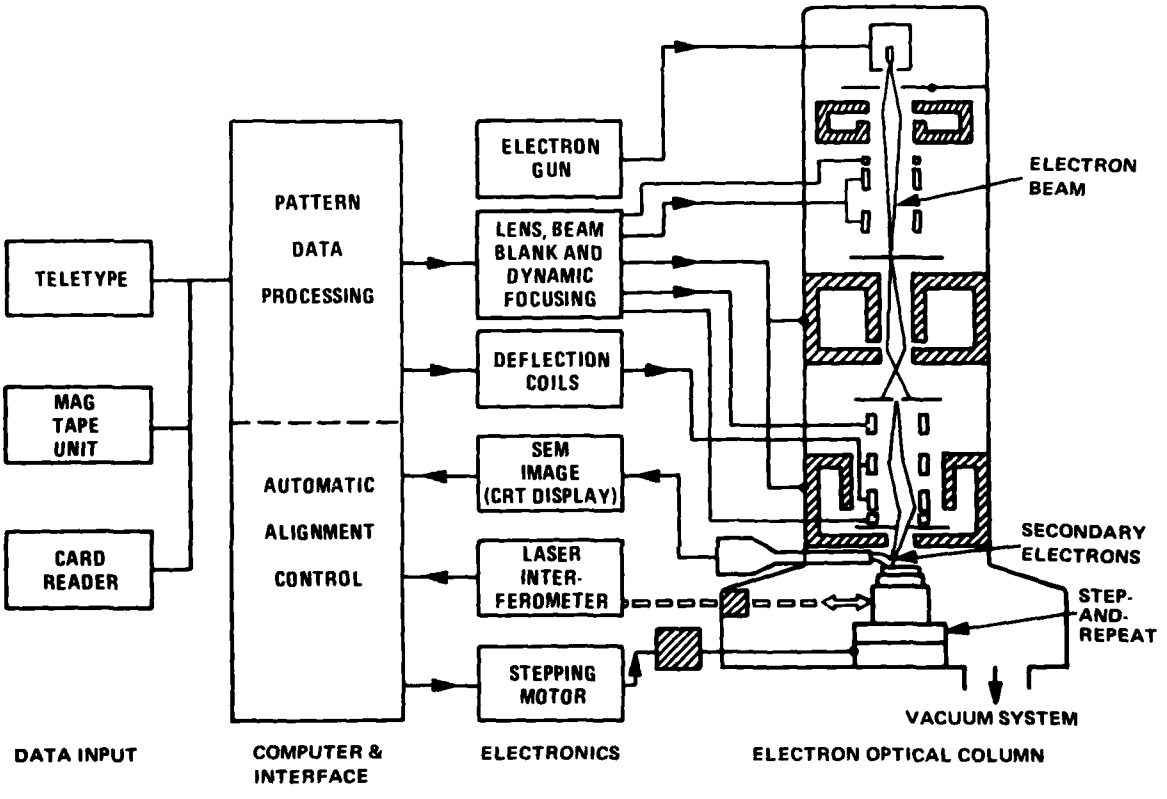

Figure 6. Electron Beam Pattern Generation Schematic

Table I. EBMIII Characteristics

Scan area (field size)	Up to 6.35 X 6.35 mm
Line resolution	6250 Lines at 3 mrads beam semiconvergence angle (1.0 μm over 6.35 mm X 6.35 mm area)
Point resolution (Least significant bit size)	0.125 μm (6.35 X 6.35 mm field)
Pattern nonlinearity	< 0.05% of field size
Figure drafting	Steered beam (vector scan)
Beam diameter	Variable from 0.25 μm to 5.2 μm (Computer controlled option of preset "large" or "small" beam)
Accelerating voltage	15 kV
Objective lens focal length	7.5 cm
Scanning speed	Programmable from 40 μm/ms to 5 μm/μs
Pattern writing time (2.5 $\mu C/cm^2$ resist) (30% area)	24 s/cm^2 + 10-20% overhead
X-Y table stepping speed	1.3 cm/s over 12.5 cm X 12.5 cm
Direct writing pattern registration accuracy (fiducial markers) (every chip alignment)	±0.25 μm
Combination laser and fiducial maker alignment (three chip)	±0.5 μm
Alignment time	~0.1 second for each chip
Data Input	
Complex IC patterns	Magnetic tape after decomposition on IBM 370
Simple devices and test patterns	Card or teletype
Pattern intermix	Capable of intermix of 50 patterns on a single wafer with equal alignment accuracies
Pattern generation capability	All normal photomask geometries

Table II. EMBIII Exposure Time
(Overhead Not Included)
25% Area Coverage

E (ns/μm) D (lines/μm)	Write Time (min) per 3" wafer	I (nA)	S ($\mu C/cm^2$)
E = 200 D = 4	13.3	37.5	3
E = 200 D = 2	6.6	75	3

The exposure time per level (including pattern overhead) for the 256-bit bipolar RAM (3-inch wafer) is given in Table III for E = 200 ns/μm and 0.25 μm beam spacing. The average exposure time is 8.2 minutes, but there is another 7.8 minutes of overhead primarily due to stage stepping time. The load/unload time refers to the new auto-loader developed on this contract. This throughput is not the ultimate capability of e-beam direct writing.

As mentioned previously, a new e-beam system (EBSP)[1] was developed at TI on a parallel program whose throughput is 5 to 10X better than that achieved on EBMIII in the fabrication of the 256-bit bipolar RAM. The EBSP system is shown in Figures 7 and 8 and also as a block diagram in Figure 9.

The throughput capability of this system is shown in Table IV as a function of minimum geometry and as a function of sensitivity of the electron resists required.

One of the key features of EBSP, the automatic loading system, was developed on this contract. In addition, a new x-y table significantly reduces the step-and-repeat time which was becoming one of the key limiting throughput factors on EBMIII.

1. Automatic Slice Loading

A computer-controlled wafer handling system was developed on this contract to increase the throughput of direct write e-beam systems, to eliminate the manual handling with vacuum or mechanical tweezers, and to reduce the large volume of air that had to be evacuated each time a wafer was loaded into or unloaded from the system.

The basic goal of the slice handling system was to add no more than 60 seconds to the total patterning time per wafer. Other design constraints were that the prealignment would be within ± 1.5 degrees and no mechanically induced vibration would be present during slice exposure.

A system was designed and fabricated at TI and a photograph of the completed system is shown in Figure 10. This system allows load/unload of a wafer is about 40 seconds.

Table III. E-Beam Exposure Time for 256 Bit Bipolar RAM (Chip size = 136 mils X 93 mils)

Exposure Conditions on EBMIII

E = 200 ns/μm; D = 4 lines/μm

S = 3 $\mu C/cm^2$; I = 40 nA

Level	Seconds/Chip*	Minutes** per 3" wafer
1. DUF	2.6	14.0
2. Isolation	1.1	5.9
3. Base	1.4	7.6
4. Emitter	0.9	4.9
5. Contacts	1.0	5.4
6. Leads	3.2	17.3
7. P. O.	0.5	2.7
Average	1.5	8.2

*324 Chips/3" wafer (≈63% wafer)
**Includes pattern overhead ≈10%-20%.

Total Time Per Wafer

	minutes
Exposure Time (Average)	8.2
Stage Stepping and Settling	6.8
Auto-Align	0.3
Load/Unload	0.7
	16.0

A schematic of the system is shown in Figure 11. The operating sequence is as follows:

1) A slice is removed from a loaded cassette of unexposed slices (A) and shuttled to the elevator/alignment (B) and aligned to ± 1.5 degrees.

2) The loader vacuum chamber is vented with dry nitrogen and the input vacuum lock is opened.

3) The transport mechanism is rotated to the open port and the unexposed wafer is shuttled into the loader vacuum chamber.

4) The input lock is closed and the loader chamber is pumped to a vacuum of 1×10^{-3} torr.

5) The transport is rotated 90 degrees cw with the unexposed slice facing away from the main chamber vacuum lock.

6) The main chamber vacuum lock is opened and the exposed slice is removed from the work platform and shuttled into the loader vacuum chamber.

7) The transport is rotated 180 degrees ccw and the unexposed slice is shuttled to the work platform within the main chamber and clamped.

8) The main chamber vacuum lock is closed and the auto loader chamber is vented.

9) While an unexposed slice is being removed from the cassette and aligned, the transport is rotated 90 degrees cw so the exposed slice is facing the output lock and the empty shuttle faces the input lock.

10) Both the input and output vacuum locks are opened, the unexposed slice is shuttled into the loader vacuum chamber while the exposed slice is deposited on the output track and transported to the empty cassette.

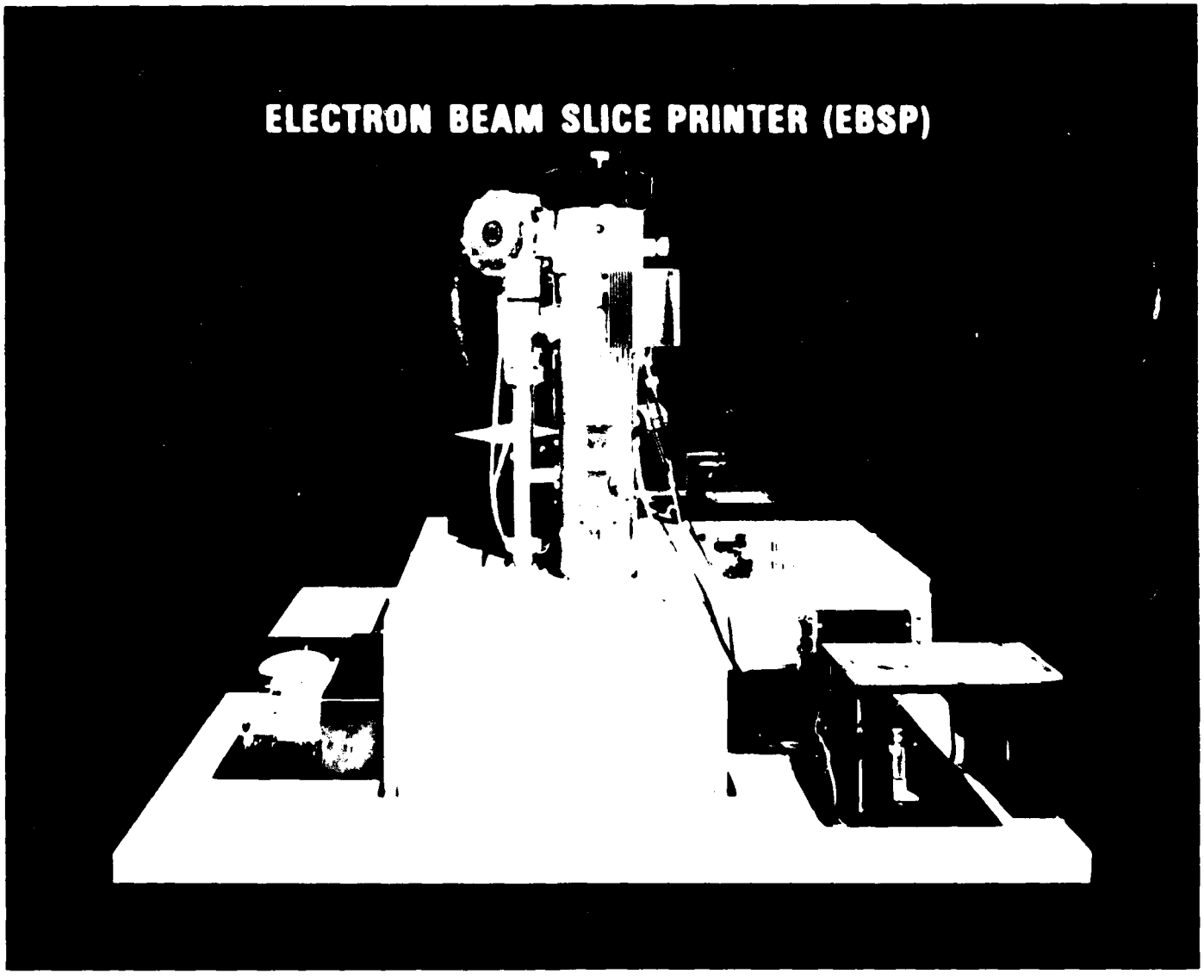

Figure 7. Electron Beam Slice Printer

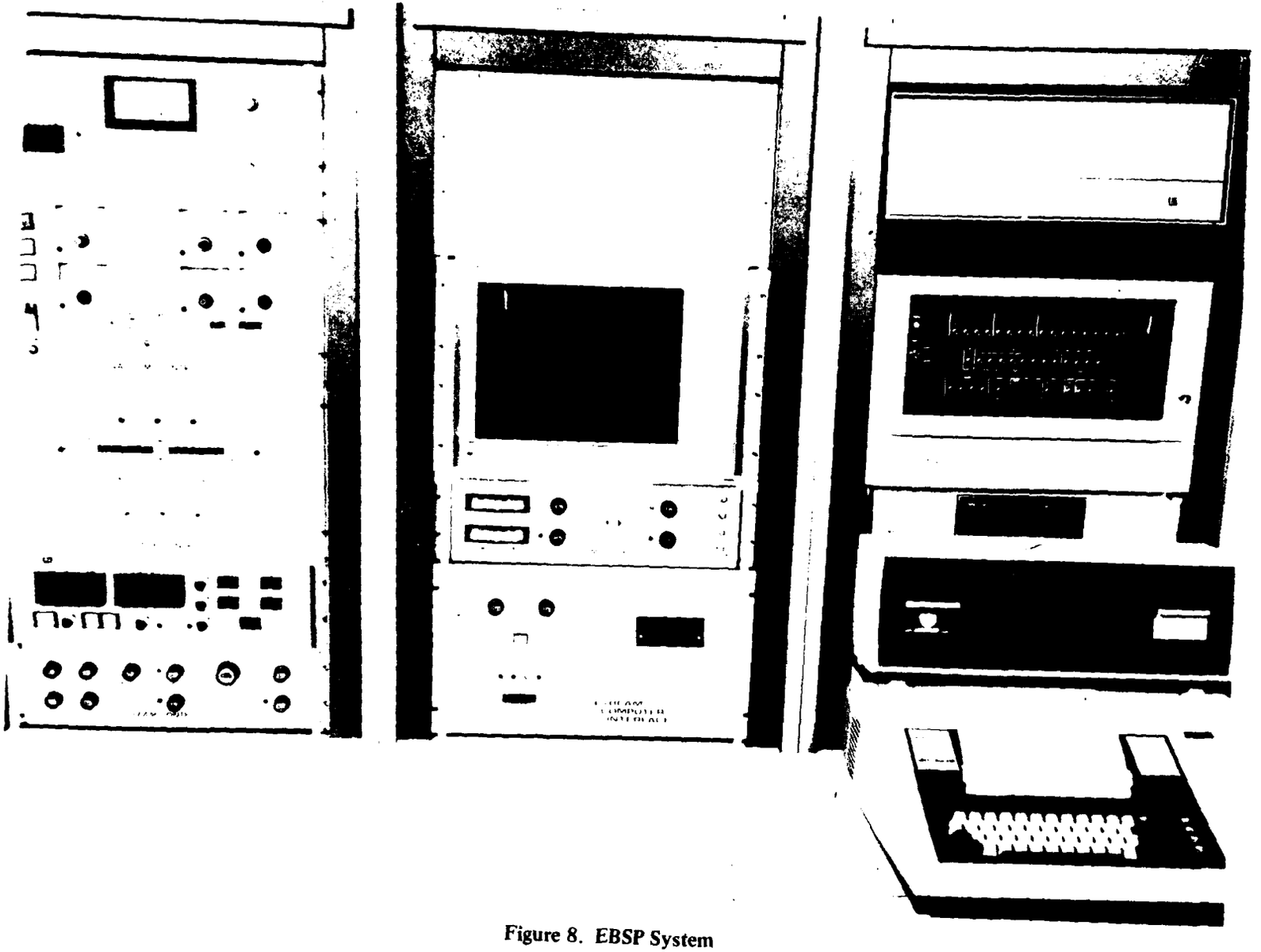

Figure 8. *EBSP System*

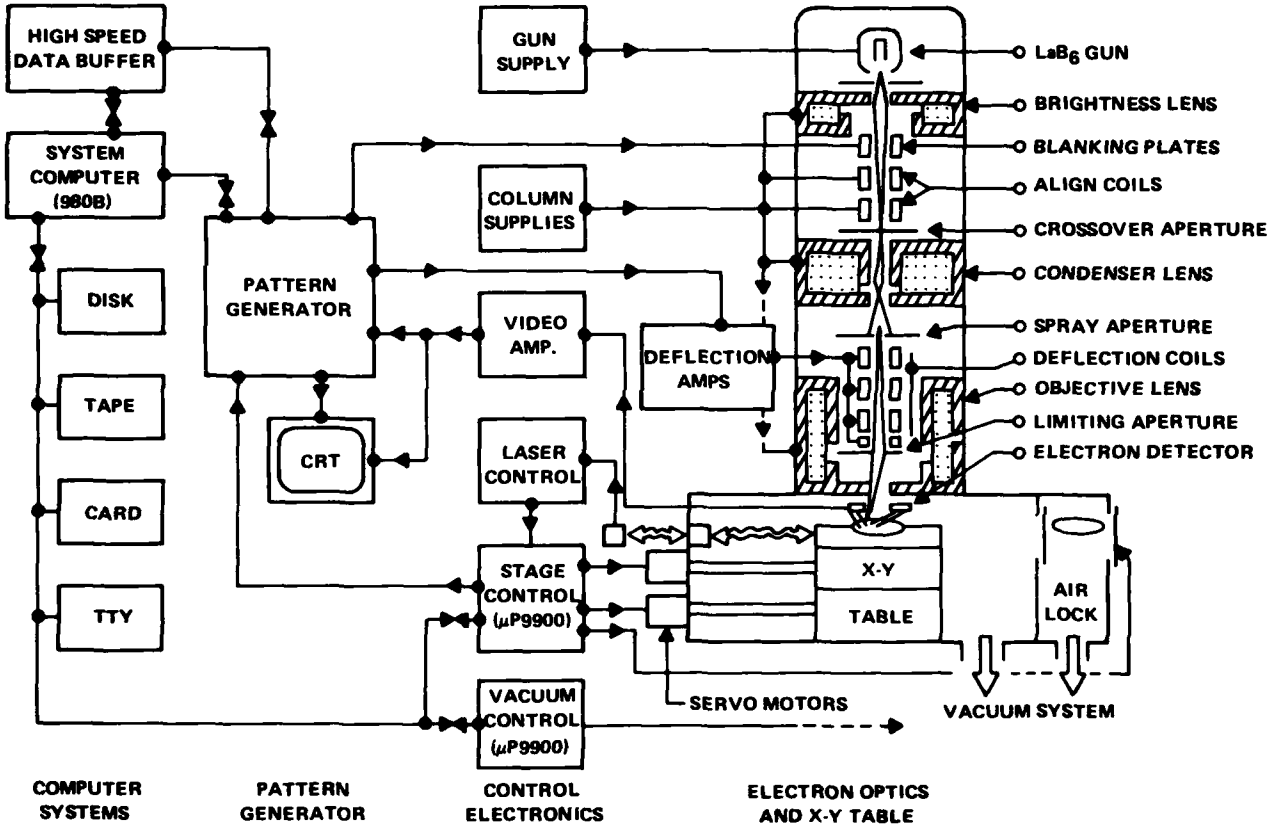

Figure 9. EBSP System–Block Diagram

Table IV. EBSP Throughput Capability

MIN. GEOM. (μm)	E (ns/μm) D (lines/μm)	WRITE TIME (MIN)/ 3" SLICE	THROUGHPUT* 3" SLICES/HR	I nA	REQUIRED RESIST SENSITIVITY μC/cm²
2.5	E = 80 D = 2	2.7	14	125	2.0
1.25	E = 80 D = 4	5.4	8.5	50	1.6
2.5	E = 40 D = 2	1.3	20	125	1.0
1.25	E = 40 D = 4	2.7	14	50	0.8

*Overhead = 1.7 min 25% Area Coverage

2. Automatic Beam (Large/Small) Control for High Density Patterns

Before the start of this contract, the electron-beam slice printer (EBMIII) was limited to exposing geometries greater than 0.1 mil at the same rate as geometries less than 0.1 mil. This results from the fact that for a fixed gun brightness, reducing the electron-beam spot diameter by 2-4X results in a reduction in beam current of 4-16X. This means that a level which can be exposed in 10 minutes (excluding vacuum cycle time) using a 1-μm spot diameter, typical of exposure requiring normal resolution (0.1 mil), would take 40 minutes if exposed with a 0.5-μm diameter spot size. A small change in the spot diameter has a particularly negative impact on throughput.

It was determined that one way to sidestep this fundamental problem of electron optics was to expose all those geometries requiring high resolution with the small spot diameter leaving the remainder to be exposed with the large beam diameter. Since the beam shifts slightly with a change in beam diameter, a realignment of the beam to a set of fiducial marks is necessary after every beam size change. This requires a two-pass process: alignment and exposure of pass one; and a change in beam size, alignment and exposure of pass two. This process will significantly reduce exposure times for high-resolution work, provided that the time required for stepping and alignment is small compared with the time required to expose the entire level with the small beam.

Implementation of this dual-beam processing capability on EBMIII was only a matter of software development because the hardware required to switch between two preset beam diameters already existed prior to the contract. A sort on input geometries using size criteria was necessary to separate one level into two levels with two different resolution requirements. This data processing operation was accomplished on the IBM 370 to take advantage of level documentation available there.

A 1-μm device (50% I²L SBP0400 Microprocessor element) was exposed with the dual-beam technique and showed no image degradation due to two passes.

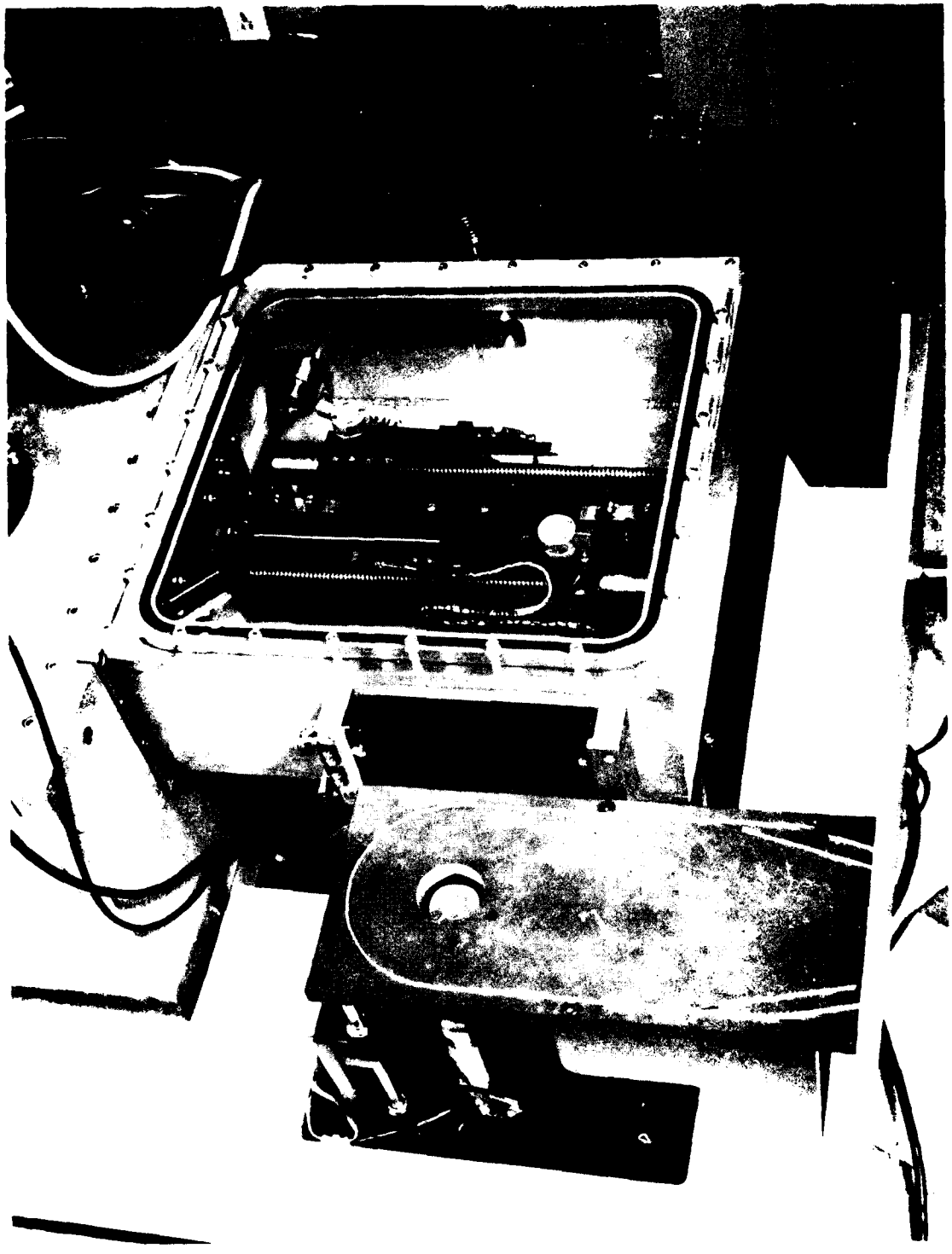

Figure 10. EBSP Auto Loader

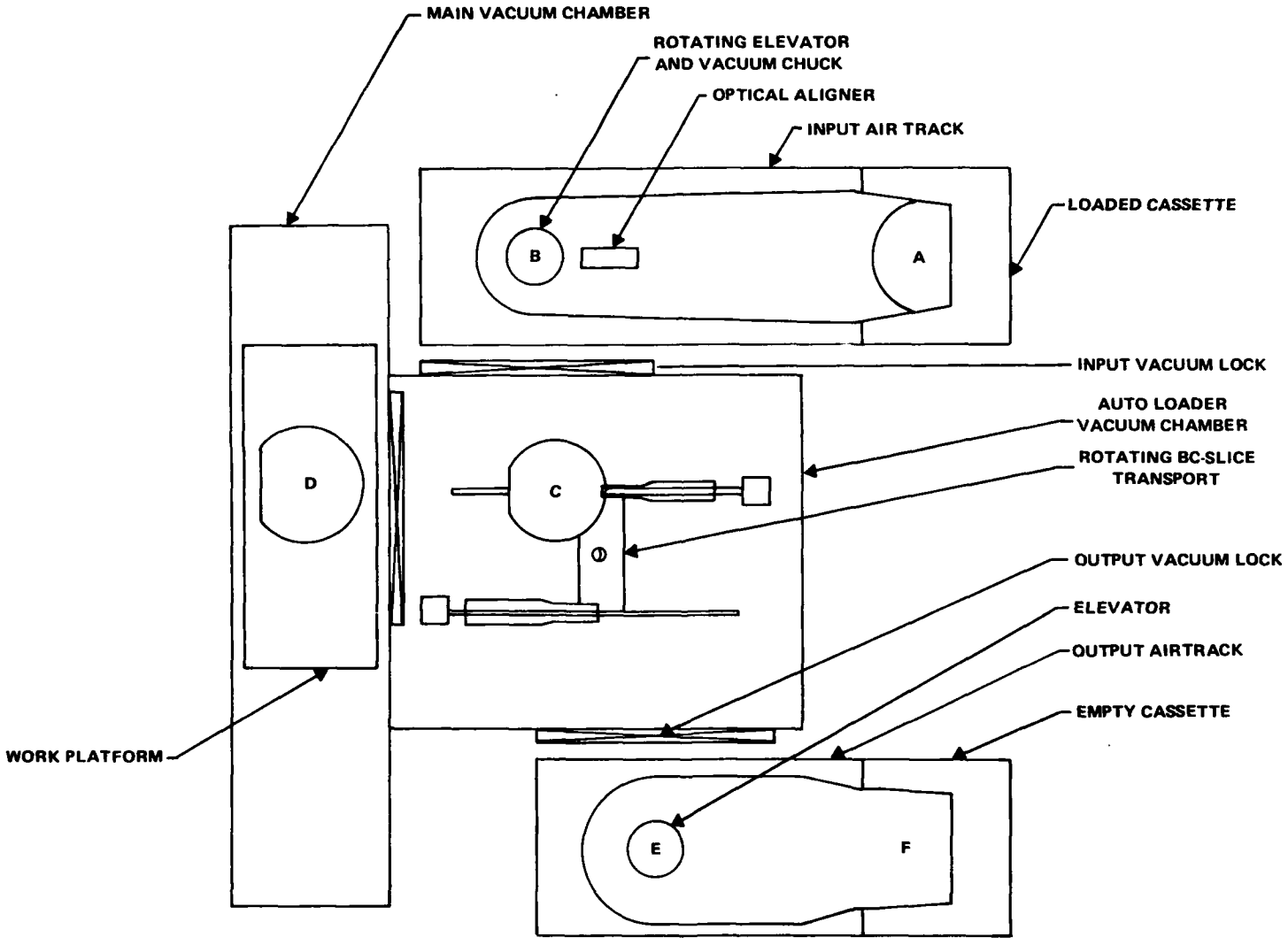

Figure 11. Slice Handling Auto Loader

3. One-Micrometer Device Structures

The electronmicrograph in Figure 12 is a portion of the SBP0400E, a 1.0-μm design rule microprocessor element. Figure 13 is an electromicrograph of the contact level of this device demonstrating the capability of EBMIII to delineate 1.0-μm device structures. These patterns were generated on EBMIII as part of this contract to demonstrate the high resolution, high packing density capability of direct e-beam slice writing. A subsequent internal program at TI developed the technology necessary to fabricate this device[2] on EBMIII.

The SBP0400E is an I^2L microprocessor element containing $\approx$2000 effective gates and requiring 10 mask levels. The minimum feature size is 1.0 μm. The SBP0400E design was obtained by shrinking the full size chip (SBP0400E) from 13.5 mm^2 to 3.4 mm^2.[3] An additional 2 mm^2 was added back to the shrink version to include large bond pads to facilitate testing. A photomicrograph of the completed chip is shown in Figure 14.

The performance of the SBP0400E is illustrated in Figure 15. Clock frequency (19 logic levels) is plotted versus total chip current for both the SBP0400E and SBP0400A. The performance improvement gained by the shrink varies from $\approx$2X at 200 mA chip current to $\approx$3X at 50 mA chip current.

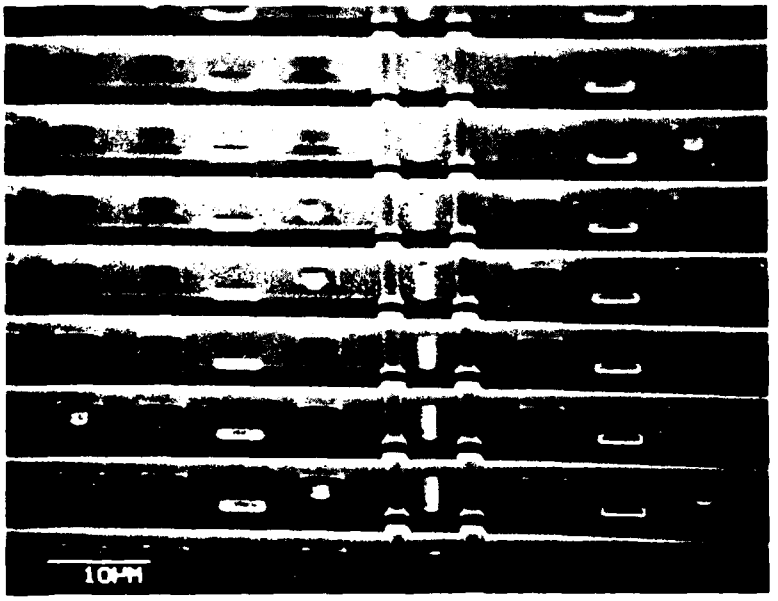

Figure 12. Electronmicrograph of 1.0 μm Design Rule Device Structures on SBP0400E

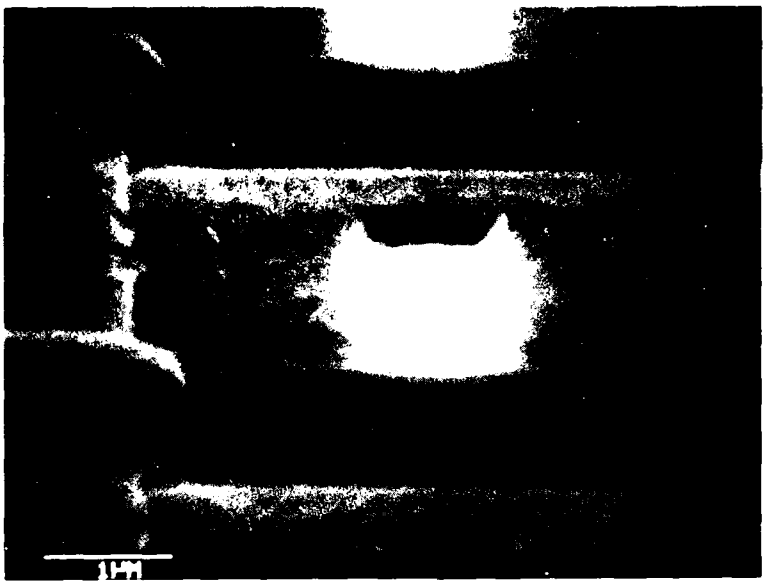

Figure 13. Electronmicrograph of 1.0 μm Injector Contact on SBP0400E

B. E-BEAM RESIST AND ETCHING CAPABILITIES

1. Imaging Materials (Resists)

a. CRITICAL MATERIALS FACTORS

Many of the desired properties and requirements for organic polymeric resist imaging materials are similar regardless of the exposure technology. Some of the more important properties that must be considered are outlined in Table V. Most of these are general, well recognized requirements which have been discussed in numerous review articles[4-7] and will not be repeated here. However, requirements, as they relate to high-resolution applications, introduce many subtle differences in resist design, selection and usage that are not necessarily important in larger geometry technology.

Sensitivity

With the increasing sophistication, complexity and cost of modern exposure systems, a major driving force for cost-effective lithography is improved throughput from increased resist sensitivity. This is particularly true for e-beam and optical projection systems where small fields are stepped serially over the wafer. It generally appears, however, from recent results with newly developed resist materials, that enhanced sensitivity is attained only at the expense of other material properties such as resolution in negative resists or etch resistance in positive resists. Thus the development of devices with 0.5 to 1.25-μm features may result in a change of emphasis from throughput to other properties such as resolution, dry etch resistance, defect density, etc.

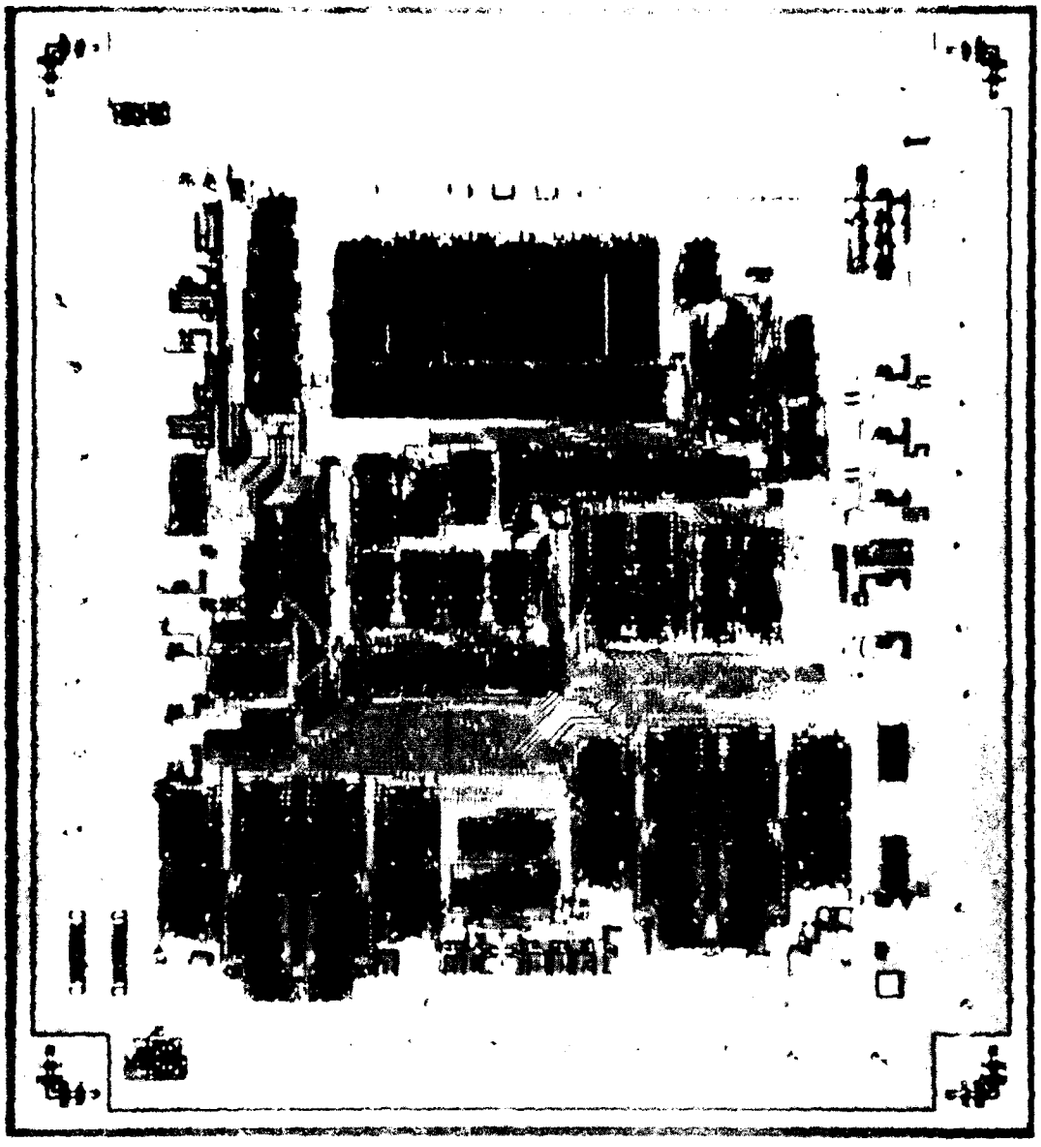

Figure 14. Photomicrograph of All E-Beam Fabricated SBP0400E

Resolution

An obvious resist requirement is for accurate replication and transfer by etching or implanting of patterns with feature sizes as small as 0.5 to 1.25 μm (in some cases the critical size is the spacing between features). There are a number of factors characteristic of the exposure systems which limit resolution such as electron scattering, diffraction, wavelength, defocusing and other distortions or aberrations, standing waves, depth of field and wafer bowing, etc. The primary intrinsic resist properties which affect resolution are contrast and swelling during development.

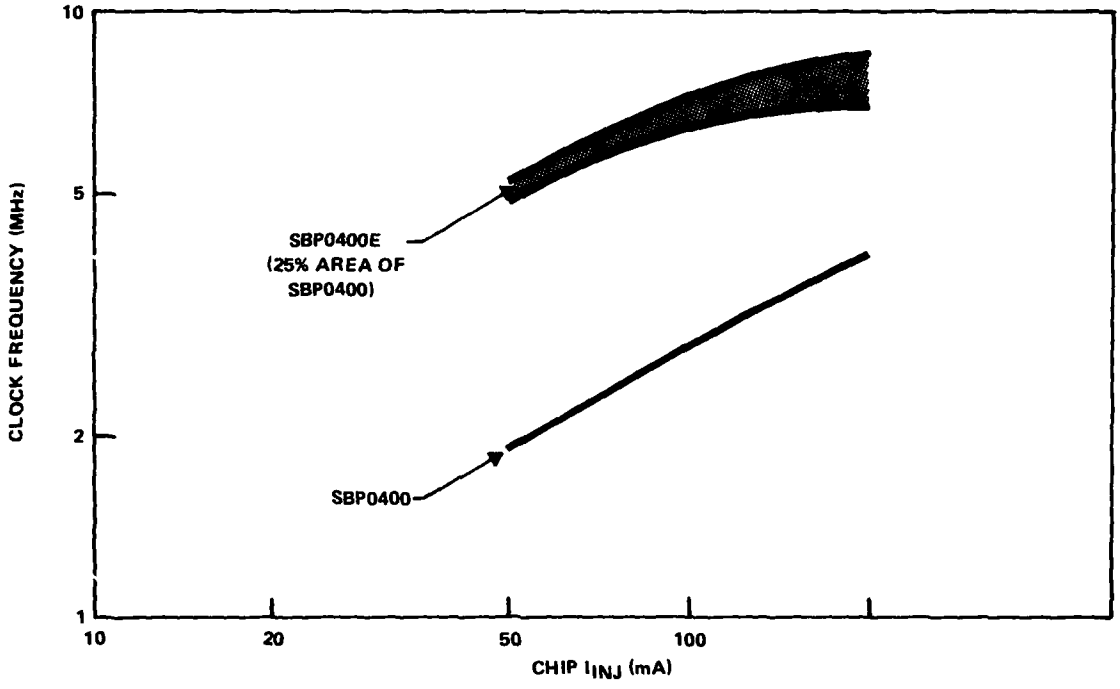

Figure 15. Clock Frequency (19 logic levels) versus Total Chip Current for SBP0400E and SBP0400A

Table V. Critical Factors in Resist Performance

Contrast	Glass Transition Temperature
Resolution	Molecular Weight
Sensitivity	Dispersity
Adhesion	Purity
Etch Resistance	Swelling
Undercutting	Solubility
Defect Density	Filtering
Film Uniformity	Stripping
Step Coverage	Shelf Life
Thermal Stability	Toxicity
Thermal Flow	Implant Masking

The contrast of a resist is directly related to its efficiency in chemical change (i.e., crosslinking, chain scission, gas evolution, chemical rearrangement, etc.) as a function of the dose delivered. Optimization of contrast is done by selection of proper reactive groups and control of polymer structure. Good contrast also requires a narrow molecular weight distribution in many resist systems. Limiting side reactions such as thermal fogging or scavenging of free radicals by oxygen also helps to improve contrast.

The extent of solvent swelling of a resist is determined by such factors as molecular weight, polymer structure, glass transition temperature, thermal history, and solvent solubility parameters. In general, swelling is much worse for negative resists than for positive resists and limits feature spacing to about twice the resist thickness.

Adhesion and Etch Resistance

Pattern transfer to the underlying substrate has been conventionally accomplished using liquid etching techniques which require tenacious adhesion between resist and substrate in order to minimize undercutting while maximizing edge acuity and feature size control. The isotropic nature of most liquid etchants and the resulting undercutting that is obtained make it increasingly difficult to etch patterns reliably as feature sizes approach 1.25 μm. Thus liquid etching will be eventually replaced with dry etching, which requires less adhesion to maintain accurate image transfer. Sufficient adhesion is still required to withstand developing, however, and this becomes increasingly difficult as feature sizes decrease.

With the necessity for dry etching, the extremely difficult requirement of etch resistance or low erosion rates is especially important for new resist materials. Dry etch resistance is generally observed in polymers which possess thermal and radiation stability. High sensitivity in positive resists on the other hand usually requires polymers which are unstable to radiation. This dichotomy presents an extremely difficult problem in the design of high-speed positive resists. Thus, the requirement of high resolution with etch resistance may result in a compromise of resist sensitivity.

Defect Density

With a device technology that requires feature sizes of 1.25 μm or smaller, defects as small as 0.25 μm can be disastrous. Besides the problem of detection of such small defects which requires electron microscopy or other electrical testing, elimination of defects from resist films requires attention to three important factors: thickness, filtration and aging.

For resist materials which are spin-coated from solution, it is well recognized that resist thicknesses of 0.8 μm or greater are required in order to ensure defect densities below one defect per cm^2 after etching. As resist films become thinner, defect densities increase exponentially. Unfortunately, with the currently available materials, 1.25-μm geometries are difficult to achieve in positive resists of thicknesses greater than 1 μm and because of swelling are virtually impossible to obtain in negative resists. The step coverage requirements for thick resist films may be reduced as more planar device technologies or new coating methods are introduced.

Particulate contamination is the major source of resist-related defects. It is necessary to provide multiple filtration at the 0.2-μm level with careful attention to cleanliness and handling of bottles, wafers, pumps or dispensers, solvents, etc., in order to minimize the defect problem.

b. COMPARISON OF MATERIALS

Due to the stringent requirements for an e-beam resist to be used in direct slice writing, no completely satisfactory resist has been developed. Some polymers behave well enough based on several of the criteria, but all fail in at least one area, especially where direct slice writing is concerned.

Positive resists have received the most attention and development. Only two positive e-beam resists, PMMA and PBS, are commercially available, and both fail to meet TI's requirements. An extensive development program at TI has provided a family of resists, TI-303, TI-313 and TI-323, which can be and have been used for device fabrication. Table VI shows the properties of the commercially available PMMA and PBS along with TI-313. TI-313 offers the best advantages where processing requires dry etch processes, such as plasma and reactive ion etching and was used extensively on this contract.

Negative e-beam resists contain a reactive moiety, such as epoxy, vinyl or allyl group, which, on exposure to e-beam irradiation, form a crosslinked gel. Swelling of this gel during developing is the major limitation of most materials considered for e-beam resists. The most widely used commercially available negative e-beam resist is COP. The major shortcomings of COP are marginal dry etch resistance and adhesion.

TI uses a negative resist, TI-309, which was developed internally to match the e-beam exposure system and device processing. Table VI shows a comparison between COP and TI-309. Dry etch resistance makes TI-309 the superior negative resist.

2. **Pattern Transfer (Etching)**

Etching processes for pattern formation in VLSI device layers must meet exacting requirements:

1) Directionality
2) Selectivity
3) Uniformity
4) Process control
5) Freedom from damage and contamination

to enable practical, well-controlled pattern transfer of features 1.25 μm or smaller in size. Traditionally, liquid etchants have been used to pattern Si, Si_3N_4, SiO_2 and metals and more recently barrel or tube-type plasma reactors have been used to etch Si and Si_3N_4 using CF_4/O_2. In either case, the etching has been found to be isotropic, i.e., vertical and lateral etch rates are equal, and undercutting of the masking pattern is substantial. With isotropic etching, 1-μm features cannot be etched into 1-μm films with a spacing any closer than 2 μm. This severely limits the design and packing density of very small devices and requires pattern compensation and sizing to be done.

Texas Instruments has pioneered the development of the parallel plate, radial flow plasma reactor for the expressed purpose of providing improvements in uniformity and process control. A schematic is shown in Figure 16. The combination of depletion of active species as the radial flow

Table VI. Positive and Negative E-Beam Resists

Positive E-Beam Resists

Resist	Sensitivity	Resolution	Dry Etch Resistance	Film Properties	Comments
PMMA	50 $\mu C/cm^2$	<1 μm	Good	Good	Commercially available, flows during baking
PBS	0.8 $\mu C/cm^2$	<1 μm	Poor	Marginal	Commercially available, pinholes in thick films
TI-313	3 $\mu C/cm^2$	1 μm	Good	Good	Internally manufactured

Negative E-Beam Resists

Resist	Sensitivity	Resolution	Dry Etch Resistance	Film Properties	Comments
COP	1 $\mu C/cm^2$	2 μm	Marginal	Swells	Commercially available
TI-309	3 $\mu C/cm^2$	2 μm	Good	Swells	Internally provided

proceeds inwardly, balanced with an electron density which decreases towards the outer walls, results in the capability to etch or deposit films with exceptionally good uniformity and control over an area large enough to etch several dozen 3-inch wafers. As this technology has matured, plasma conditions and reactive etching gases have been formulated to produce practical etch rates for all the important semiconductor films to be patterned. More importantly, it has been shown that the etching can be done with almost perfect directionality, i.e., vertical etch rates can be obtained that are at least ten times greater than the lateral or undercutting rates. This allows submicrometer patterns with very high width aspect ratios to be etched and placed very close to each other. The directionality arises from the enhancement of the reaction of the reactive species which are absorbed on the wafer surface by bombardment of positive ions from the plasma. Slices in contact with the plasma naturally attain a negative potential with respect to the plasma and positive ions with mean free paths on the order of millimeters are accelerated perpendicularly towards the surface. Because the voltages are limited to a few hundred volts, the ions do not have enough momentum to cause sputtering, but can promote dissociation and transfer energy to the surface chemical reactions.

Reactive ion etching is a technique similar to parallel-plate plasma etching except that it requires lower pressure and the slices to be etched are placed on an electrode whose negative bias with respect to the plasma can be independently controlled. Control of the positive ion bombardment energy is clearly an advantage that allows more versatility in the reactant gases that can be used and therefore provides the opportunity to develop processes with a great deal of selectivity.

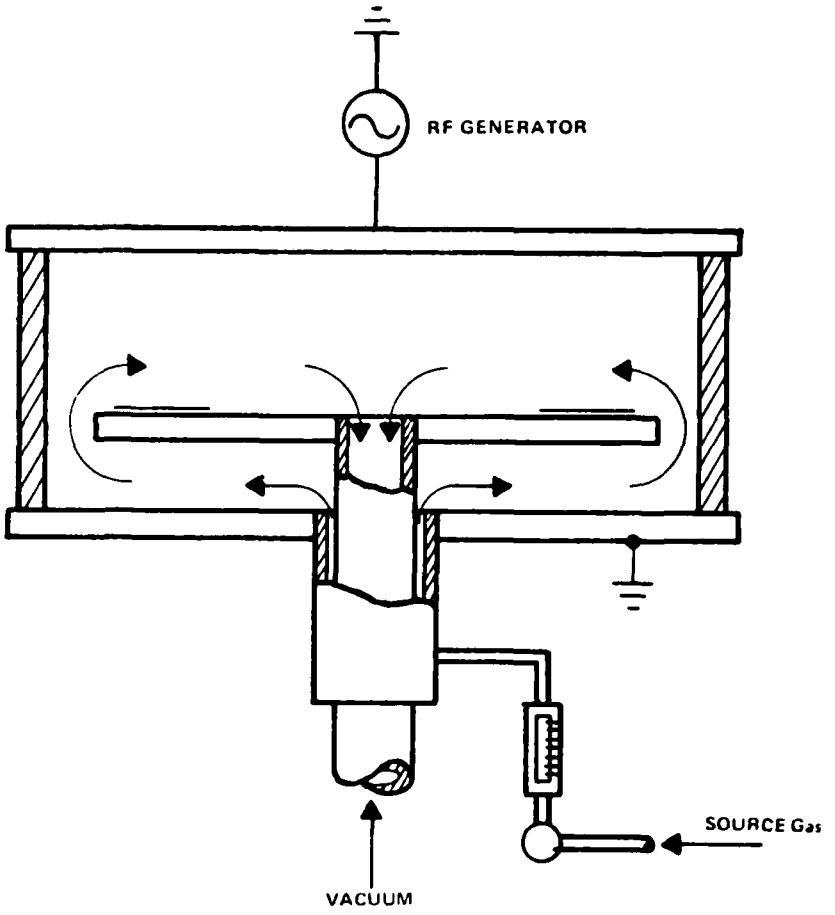

Figure 16. Plasma Etch Machine

Practical implementation of plasma or reactive ion etching requires processes with acceptable differential etch rates (selectivity) between the masking material and the material to be etched, as well as between the material to be removed and the substrate from which it is to be etched. It is therefore significant that Texas Instruments has developed practical processes for selective etching of poly Si on SiO_2, SiO_2 on Si, Si_3N_4 on Si, Si_3N_4 on SiO_2, Mo, Ta and W on SiO_2 and Al on SiO_2 and demonstrated these processes with actual integrated circuit fabrication. For instance, the all e-beam patterned 256-bit bipolar RAM has been successfully produced using a selective oxide plasma etch at every level. Also, both dynamic and static 4K MOS RAMs with all e-beam patterning have been fabricated using selective plasma etching to define the inverse moat in Si_3N_4/SiO_2, the gate in poly Si, and first and second contacts in SiO_2 over Si.

C. DEVICE FABRICATION

1. Device Description

There are many possible bipolar processes that could be used in conjunction with e-beam pattern definition to build memory devices. Among those are dielectric isolation, isoplanar, double-level metal, etc. While all of these processes have merit, the process chosen for this program was the single-level metal, junction isolation Schottky process which is used by Texas Instruments in building the SN54S/74S Random Access Memories.

The particular device selected for this program was the SN74S201A, a monolithic TTL memory featuring Schottky clamping for high performance with fast chip-select access time to enhance decoding at the system level. This device contains a 256-bit fully static random access nondestructive readout memory. The memory, if fully decoded, requires only eight address lines to select one of 256 storage locations. An additional line, write enable, is provided to enable the memory to modify the stored data. Separate data input and data output lines are provided for minimum interaction between input and output functions. Three chip-enable lines are provided to simplify the decoding required to achieve the desired system.

2. Schottky Bipolar RAM Design

a. SYSTEM DESIGN

The basic logic diagram is shown in Figure 17. The memory matrix is organized in an array of 16 rows and 16 columns. The address inputs A, B, C and H go to a 4-to-16 line decoder and determine the memory column selected. The address inputs D, E, F and G go to a 4-to-16 line decoder and determine the memory row selected. The logical operational mode (truth table) is shown in Table VII. The terminal connections for the 256-bit RAM are shown in Figure 18.

b. MEMORY CELL

The SN74S201A utilizes inverted-cell memory elements to achieve high densities. The circuit schematic for the memory cell is shown in Figure 19. The cell is basically two cross-coupled inverters and two sense diodes. Information is written into the cell or read from the cell along the sense lines. The cell is enabled or disabled using the word line. When the word line is low, information can be read from or written into the cell. When the word line is in a high state, the cell is disabled and no information can be read or written.

c. INPUT CIRCUITRY

The circuit schematic for all of the inputs is shown in Figure 20. This input circuitry was designed to give very low high-and-low-level input currents and very high performance. The low input currents allow higher fan-out capability in an entire memory system. The use of Schottky diodes and transistors in the inputs increases the performance over non-Schottky devices. The inputs also have clamping diodes to protect the circuitry in case the input voltage should go negative.

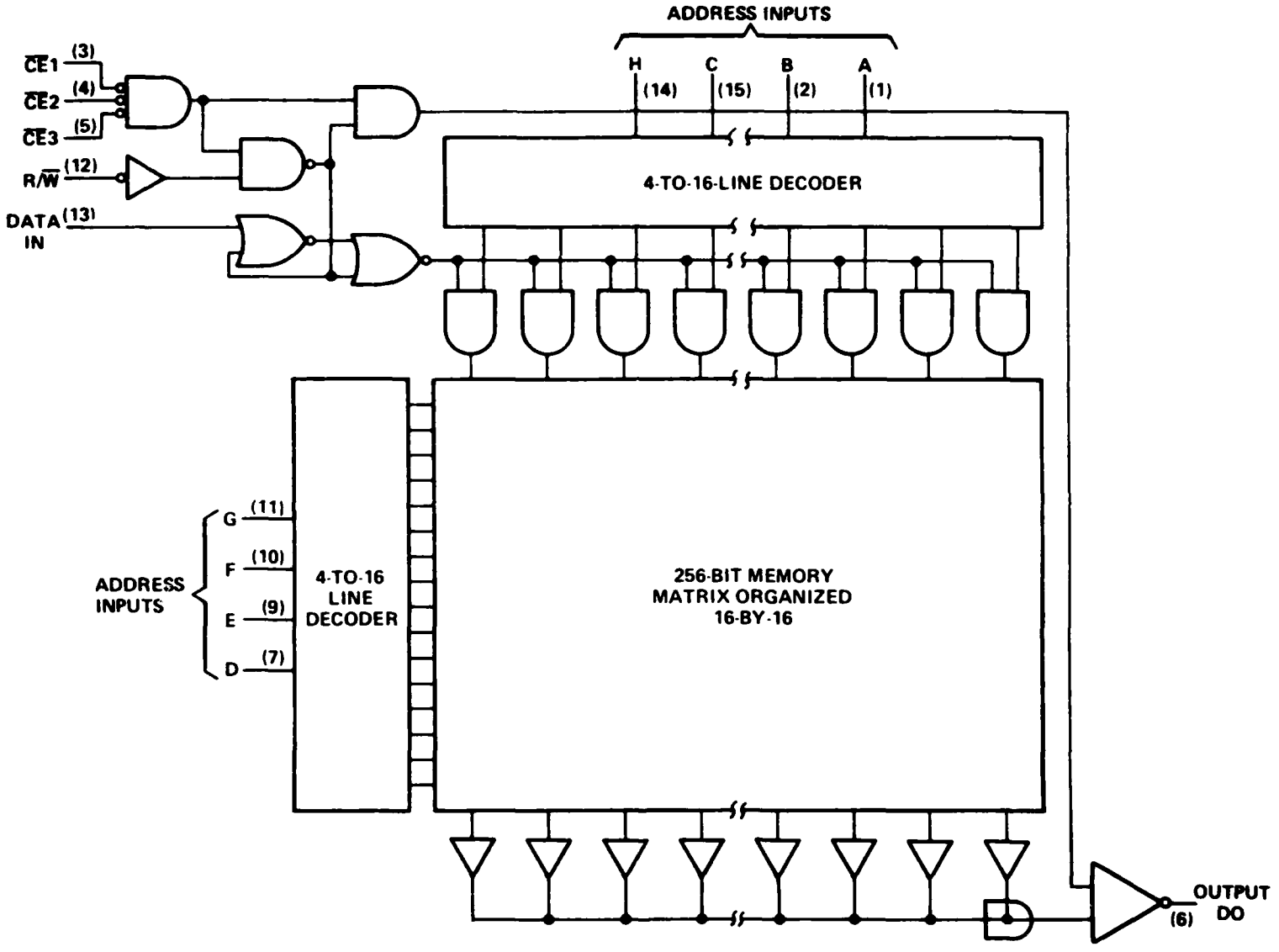

Figure 17. Schottky Bipolar RAM—Logic Diagram

Table VII. Logical Operational Mode

Function	Inputs		Output
	Chip Enable†	Read/Write	
Write (Store Complement of Data)	L	L	H
Read	L	L	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For chip-enable: L = all $\overline{CE}$ inputs low; H = one or more CE inputs High

d. OUTPUT CIRCUITRY

The SN74S201A has a three-state output, shown in Figure 21, that offers the convenience of an open-collector output with the speed of a totem-pole output. This output circuitry permits the output terminal to be bus-connected to other similar outputs, yet it retains the fast rise time characteristics of a TTL totem-pole output.

3. Slice Processing

a. GENERAL DISCUSSION

The process for building the SN74S201A has been well established in the Houston bipolar production facility of Texas Instruments for some years. A photograph of this device, constructed using e-beam lithography, is shown in Figure 22. To facilitate running this device using e-beam lithography, it was necessary to establish the process in the SREL pilot line located in Dallas. To accomplish this, several lots of material were processed in the pilot line using conventional photoresist lithography. These lots had yields of 27% to 30%, which compared favorably with production yields of 30% to 34% at parametric and functional tests. In addition to these runs with photoresist, a control lot using photoresist was run with each e-beam lot. This control lot was very useful for failure analysis and ascertaining if problems were present that were unique to e-beam processing.

b. PROCESS DESCRIPTION

The detailed process for building the SN74S201A is given in Table VIII. Most the process steps shown there are standard production processes. Only those steps relating to the alignment markers and directly to e-beam lithography are nonstandard and will be discussed in detail.

The sketches shown in Figure 23 shown the sectional view of a slice at various process steps. Not exhibitable in these sketches, but listed in Table IX are the oxide thicknesses which had to be etched at the various levels. As shown, these oxides of from 2000Å at contact O.R. to 6400Å at DUF O.R. had to be etched. Since the electron-resist does not adhere well in the standard wet etchant, it was necessary to perform these O.R. levels by a plasma etch process. Referring to Figure 23, it is seen that when the base O.R. is performed that the isolation contact is simultaneously opened.

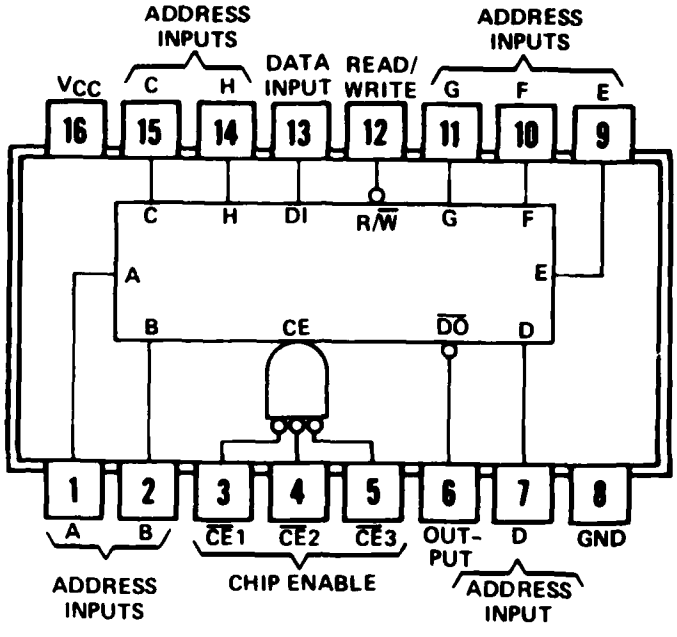

Figure 18. Terminal Connections for 256-Bit RAM

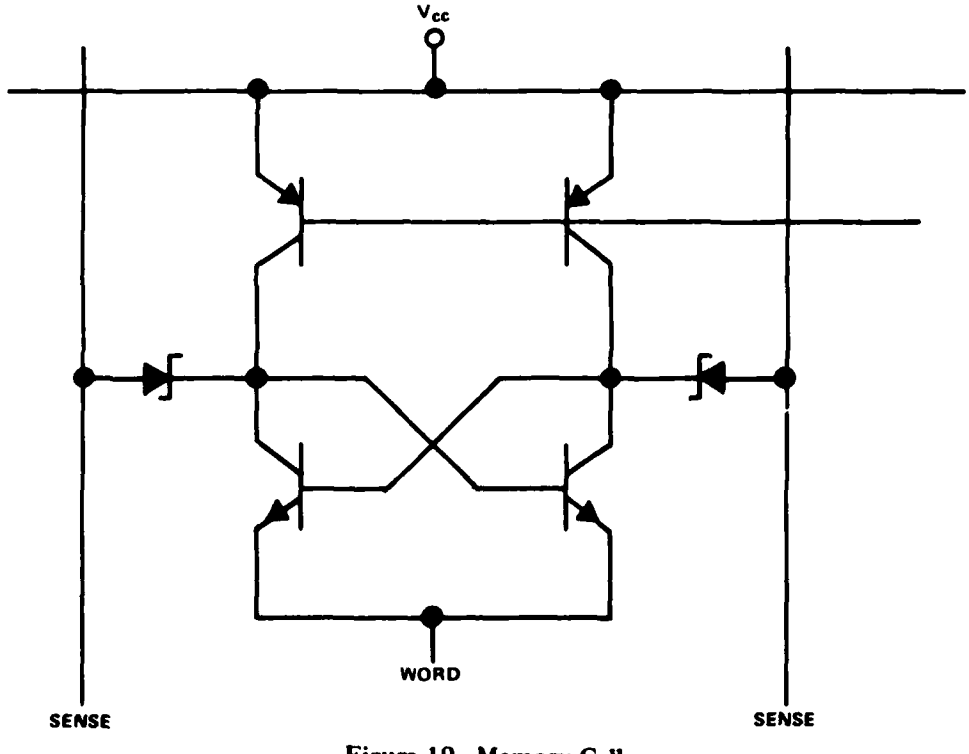

Figure 19. Memory Cell

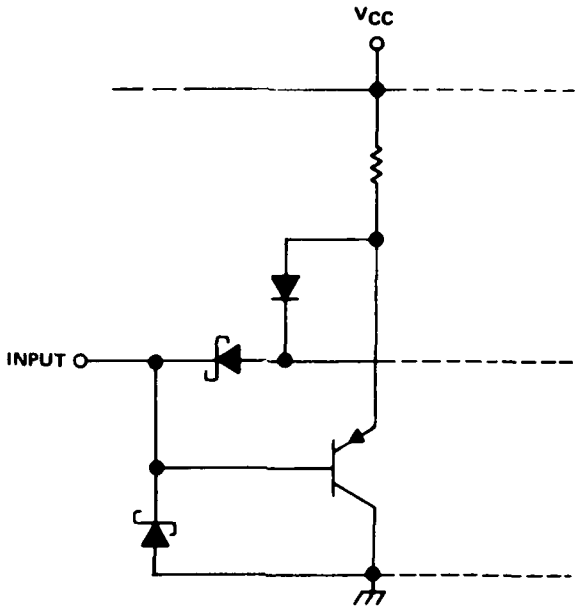

Figure 20. Input Circuitry

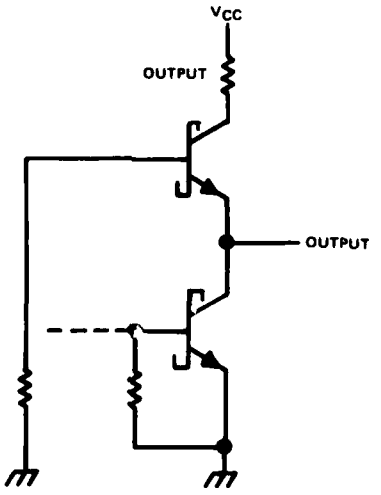

Figure 21. Output Circuitry

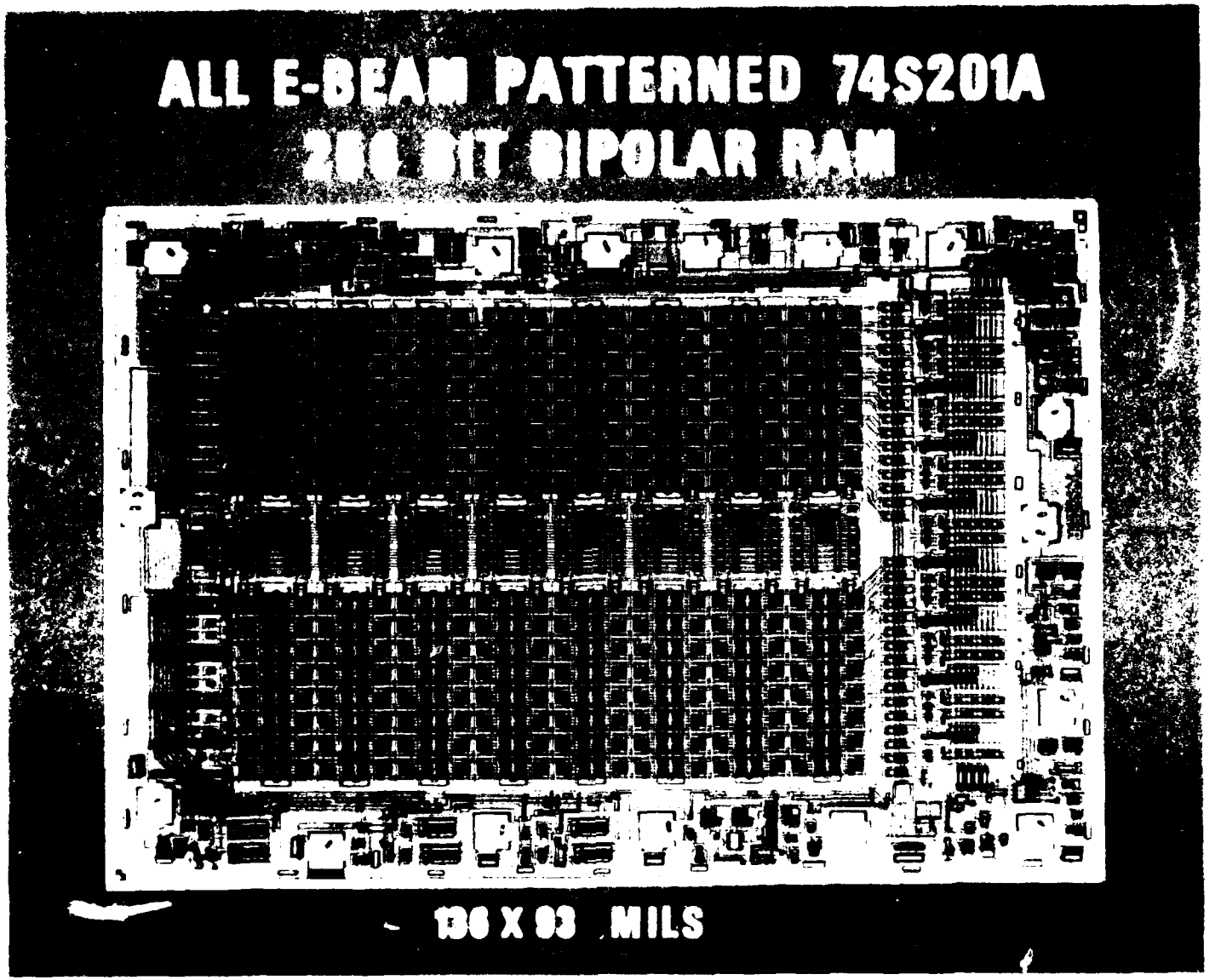

Figure 22. Photomicrograph of a Completed all E-Beam Patterned SN745201A 256-Bit Bipolar RAM

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A

Step				
1	**Substrate**			
	Type:	P		
	Dopant	Boron		
	Resistivity:	10 20 ohm-cm		
	Orientation	1 1 1		
	Dimensions	3"		
2	**1st marker mask**			
	Piranha Clean			
	Spin Swab/Inspect			
	Bake:	30 minutes	Blue M oven	200°C
	Coat:	3 5K RPM	Waycoat III	23 cps for 7KA
	Softbake:	60 minutes plus	Vacuum oven	80°C
	N_2 Dry:	30 minutes plus		
	A&E	Tower 114	8.0 seconds	
	Develop/Rinse/			
	Dry:	Stoddard/Butyl/N_2		
	Inspect			
	Silicon Etch	SREL E-Beam Lab		
3	**First Oxidation**			
	Piranha Clean			
	Spin Swab/Inspect			
	Oxide Temp:	1300 C cycled from 850°C		
	Time:	360 minutes		
	Gas	O_2 4 l/minutes		
	Furnace:	Silicon Tube/Boat		
	Inspect			
	Measure Oxide			
	Thickness:	6400A		
4	**Backside Strip OR**			
	Coat:	5.0K RPM	Waycoat III	23 cps for 6400A
	Softbake:	10 minutes	IMS Oven	65°C
	A&E:	Blank Mask	8.0 seconds	
	Develop			
	Inspect			
	Hardbake:	10 minutes	IMS Oven	125°C
	Etch Backside:	7.6 minutes	Bell 2	30°C
	Rinse:	Cold D1 H_2O	5 minutes	3X
	Spray Rinse/			
	Dry:	5/4 minutes		
	Inspect			
	Piranha Clean			
5	**DUF OR SREL E-Beam Lab**			

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A (Continued)

Step				
6	**DUF Diffusion**			
	Piranha Clean and add "P" type pilots			
	Inspect			
	Deglaze:	30 seconds (Will remove approximately 170Å)	10% HF	Room Temperature
	Spin Arsenic:	1000Å } Linear Circuits		
	Bake:	2 minutes 165°C } Linear Circuits		
	Inspect			
	Deposition	Temp:	1100°C cycled from 850°C	
		Time:	50 minutes	
		Gas:	O_2N_2	O_2 150 cc/min N_2 2.85 l/min
		DUF Window:	1050Å	
		Field Oxide:	7450Å	
	Inspect			
	Strip Pilot:	49% HF	1 minute	
	Measure and Record			
	Resistivity Spec:	23-27 Ω/sq.		
	Steam Deglaze:	Temp:	1000°C cycled from 850°C	
		Time:	15-30-5	
		Gas:	O_2-Steam-N_2	O_2 2 l/min N_2 2 l/min
		DUF Window:	4265Å	
		Field Oxide:	8000Å	
	Strip Pilot and Read			
	Rs Spec:	29-35 Ω/sq.		
	Deglaze:	4.0 minutes	10% HF	Room Temperature
	Avg. Etch Rate			
	Per Minute:	DUF Window:	418Å	
		Field Oxide:	450Å	
	Oxide Left for			
	Drive:	DUF Window:	2500Å	
		Field Oxide:	6200Å	
	Drive:	Temp:	1300°C cycled from 850°C	
		Time:	300 minutes	
		Gas:	O_2 2 l/min	
	Oxide After Drive:	DUF Window:	7000Å	
		Field Oxide:	8300Å	
	Strip Pilot:	Read Rs and Xj Spec:	Rs 12-17 Ω/sq. Xj 35-45 HG Lines	
	Strip Slices	49% HF	3.0 minutes	
	Groove one slice to check if any penetration and/or damage.			
7	**Epi**			
	Piranha Clean			
	Spin Swab			
	Epi:	HCl Etch:	4 HG Lines	
		Thickness:	.10-.11 mils	
		Resistivity:	.28-.32 Ω/cm	
		Evaluate and Record R&T		

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A (Continued)

Step				
8	**2nd Marker Mask**			
	Repeat Step 2, except use 2nd marker mask			
9	**2nd Oxidation**			
	Piranha Clean			
	Spin Swab/Inspect			
	Oxide:	Temp:	1000°C cycled from 850°C	
		Time:	15-70-5	
		Gas:	O_2-Steam-N_2	O_2-2 l/min
				N_2-2 l/min
	Inspect			
	Measure Oxide			
	Thickness:	5400Å		
10	**Backside Strip OR**			
	Repeat Step 4			
11	**Isolation OR SREL E-Beam Lab**			
12	**3rd Marker Mask OR**			
	Piranha Clean			
	Inspect			
	Bake:	30 minutes	Blue M oven	200°C
	Coat:	5K RPM	Waycoat III	23 cps for 6000Å
	Softbake:	10 minutes	IMS Oven	66°C
	A&E:	Tower 114	8.0 seconds	
	Develop			
	Inspect			
	Hardbake:	10 minutes	IMS Oven	125°C
	Etch:	To clear 2nd marker windows		
	Inspect			
	Piranha			
13	**Isolation Diffusion**			
	Inspect			
	Deposition:	Temp:	1100°C cycled from 850°C	
		Source:	BBr_3	
		Time:	25-45-5	
		Gas:	N_2O_2 - $N_2O_2N_2$ - N_2O_2	O_2-200 cc/min
				N_2 Source-30 cc/min
				N_2-7 l/min
	Steam Deglaze:	Temp:	750°C	
		Time:	10-20-5	
		Gas:	O_2-Steam-N_2	O_2-2 l/min
				N_2-2 l/min
	Deglaze:	2.0 minutes	10% HF	30°C
	Measure Rs			
	on Pilot:	4-5 Ω/sq.		

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A (Continued)

Step				
13	**Isolation Diffusion (Continued)**			
	Drive:	Temp:	1100°C cycled from 850°C	
		Time:	30-10-5	
		Gas:	O_2-Steam-N_2	O_2-2 l/min N_2-2 l/min
	Inspect			
	Measure Oxide Thickness:	3200-3400Å		
	Strip Pilot and Read Rs	5-7 Ω/sq.		
	Xj Pilot:	10-11 HG Lines		
14	**Backside Strip OR**			
	Repeat Step 4			
15	**Base OR SREL E-Beam Lab**			
16	**3rd Marker Mask OR**			
	Repeat Step 12			
17	**Base Diffusion**			
	Inspect:	Add "N" Pilots		
	Pre-Heat:	Temp:	700°C	
		Source:	Boron Nitride	
		Time:	10 minutes	
		Gas:	N_2 2 l/min	
	Deposition:	Temp:	950°C	
		Source:	Boron Nitride	
		Time:	45 minutes	
		Gas:	N_2 2 l/min	
	Steam Deglaze:	Temp:	750°C	
		Time:	10-20-5	
		Gas:	O_2-Steam-N_2	O_2-2 l/min N_2-2 l/min
	Deglaze:	2.0 minutes	10% HF	30°C
	Measure Rs on Pilot:	58-66 Ω/sq.		
	Inspect Drive:	Temp:	1050°C cycled from 850°C	
		Time:	30-15-75	
		Gas:	O_2-Steam-N_2	O_2-2 l/min N_2-3 l/min
	Inspect Measure Oxide Thickness.	3200-3400Å		
	Strip-Pilot and Read Rs:	170-190 Ω/sq.		
	Xj Pilot:	4.5-5.5 HG Lines		

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A (Continued)

Step				
18	**Backside Strip OR**			
	Repeat Step 4			
19	**Emitter OR SREL E-Beam Lab**			
20	**3rd Marker Mask OR**			
	Repeat Step 12			
21	**Emitter Pilot Deposition**			
	Inspect			
	Deposition:	Temp:	1000°C	
		Source:	$POCl_3$	
		Time:	5-9-1-4-1	
		Gas:	N_2O_2 - $N_2O_2N_2$ - N_2O_2 - N_2O_2 + Steam N_2O_2	
				O_2 300 cc/min
				N_2 Source-3000 cc/min
				N_2-2 l/min
	Measure Oxide			
	Thickness:	2000Å		
	Strip Pilot and			
	Read Rs:	5-7 Ω/sq.		
	X_j Pilot:	3-4 HG Lines		
22	**Backside Strip OR**			
	Repeat Step 4			
23	**Contact OR SREL E-Beam Lab**			
24	**Piranha**			
25	**Emitter Pilot Anneal/Probe**			
	Anneal:	Temp:	450°C	
		Time:	5-60-5	
		Gas:	Argon H_2 Argon	Argon 4.6 l/min, H_2 0.6 l/min } O_2 Scales
	Probe:	NPNβ_f	30-60	
26	**Emitter Lot Deposition**			
	Repeat Steps 21 thru 24			
27	**Evaporation**			
	Piranha Clean			
	Inspect			
	Platinum Sputter:	500Å		
	Inspect			
	Aqua Regia:	10 minutes		
	Inspect			
	Piranha Clean			

Table VIII. Process Flow for E-Beam SN74S201A/SN74S301A (Concluded)

Step				
27	**Evaporation (Continued)**			
	Spin Swab/Inspect			
	TiW Sputter:	1500Å		
	Aluminum Evap:	Thickness:	25 microinches	
		Substrate Temp:	200°C	
	Measure Aluminum Thickness			
	Inspect			
28	**Aluminum/TiW Removal SREL E-Beam Lab**			
29	**J-100 Clean**			
30	**Sinter/Probe**			
	Sinter:	Temp:	450°C	
		Time:	60 minutes	
		Gas:	O_2N_2	O_2 50 cc/min N_2 2 l/min
	Probe:	NPNβ_f	30-60	
31	**Nitride Deposition**			
	Spray Rinse/Spin Dry:	Cold DI H_2O		
	Inspect			
	Deposition:	Temp:	230°C	
		Thickness:	3000Å	
32	**Nitride OR SREL E-BEAM Lab**			
33	**Etch and Ash**			
	Etch:	8.0 minutes } 100°C		
	Ash:	25 minutes }		
34	**J-100 Clean**			
35	**Multi Probe: CDD Measurements Lab**			

During that O.R. step, the base is opened through the 5600Å field oxide and the isolation oxide. These two oxide thicknesses are listed in Table IX. The multiple oxide thickness that must be opened at emitter O.R. and contact O.R. are also listed in Table IX. Etching through these multiple-thickness oxides without attacking the silicon beneath the thinnest layer once it was removed and while still etching the thickest layers necessitates developing a new plasma etch process. The plasma etch process developed for the e-beam 256-bit bipolar RAM is discussed later.

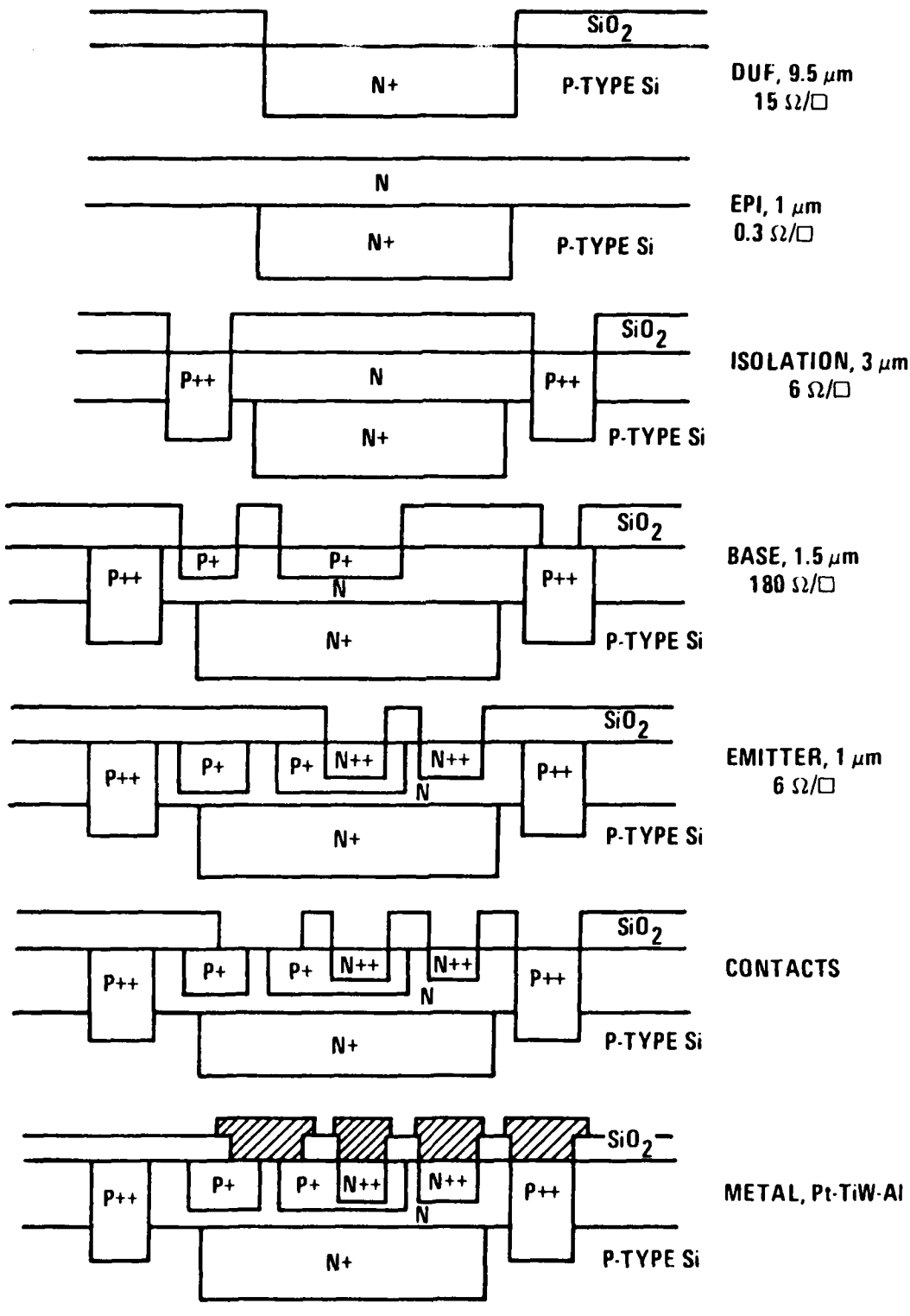

Figure 23. Schematic Structure of the Junction Isolated, Schottky Clamp, Single-Level Metal Bipolar Process used to Fabricate the SN745201A Devices

Table IX. Oxide Thickness for SN74S201A

O.R. LEVEL	OXIDE THICKNESS REMOVED - A
DUF	64000 (1st Ox)
Isolation	5400 (Field Ox)
Base	5600 (Field Ox), 3300 (ISO Ox)
Emitter	330 (Base Ox), 6000 (Field Ox)
Contacts	2000 (Emitter Ox), 4000 (Base Ox), 6000 (Field Ox)

c. ALIGNMENT MARKERS

The first marker and second marker steps of Table VIII were executed to define e-beam alignment markers on the substrate and epitaxial layer respectively. The first marker was used for aligning the DUF or buried layer pattern. Due to epi-shift during growth of the epitaxial layer, the first marker becomes broadened and is consequently unsatisfactory for aligning the subsequent levels. Photographs of a marker before and after the epitaxial process are shown in Figures 24 and 25, respectively, and clearly show why the first marker is unsatisfactory for alignment purposes after the epitaxial layer is grown. Therefore it was necessary to etch a second set of markers in the epi-layer for aligning all other levels. This second set of markers was necessarily optically aligned to the first set of markers. The mark used for affixing these alignment markers were themselves printed with e-beam lithography. Figures 26 and 27 show the placement of the two sets of markers and the markers for optically aligning them to each other. Since the DUF pattern does not have tight tolerance, the subsequent levels are quite easily aligned to it with this approach of two sets of alignment markers. In particular, the alignment of the isolation level to the DUF level has repeatedly been to within ± 1 μm.

In addition to the first and second marker mask, a third mask was generated for clearing the oxide residues which remain on the e-beam markers after etching. These residues are the result of e-beam resist which is cross-linked during the alignment scan and not removed by development. It was necessary to remove this oxide residue to prevent the markers being distorted for the next pattern scan.

d. BACKSIDE STRIP

As noted in Table VIII after each O.R. step, the oxide is removed from the backside of the slices. This is done to prevent the slices from charging up and deflecting the incident electron beam, thus deflecting the IC pattern.

e. E-BEAM RESIST PROCESSING

Design and layout of a bipolar random access memory naturally leads to the selection of a positive resist for patterning all but the metal levels on a vector scan machine like Texas Instruments EBMIII. PBS positive electron resist[3] was first chosen for the oxide patterning steps because of its

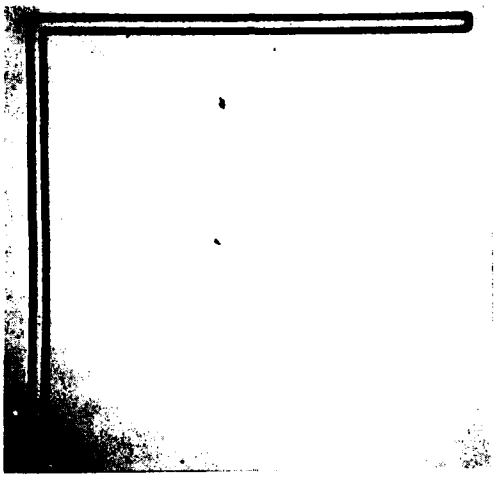

Figure 24. Plasma Etched Alignment Marker Before Epi

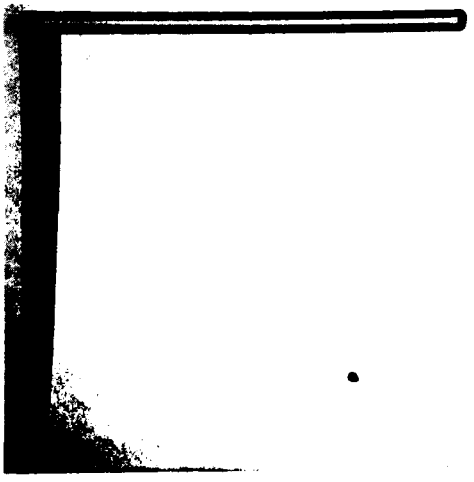

Figure 25. Plasma Etched Alignment Marker After Epi

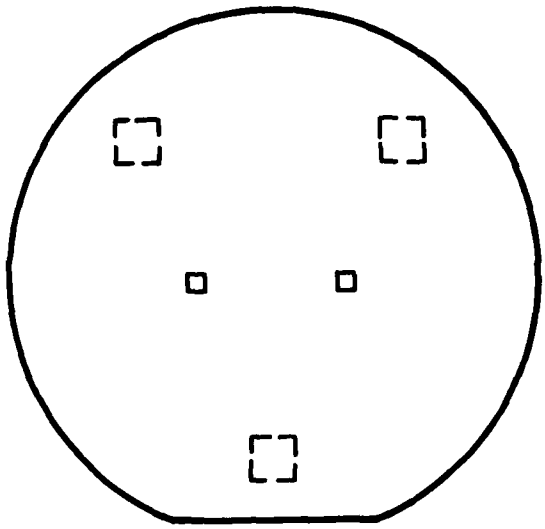

Figure 26. Placement of First Markers

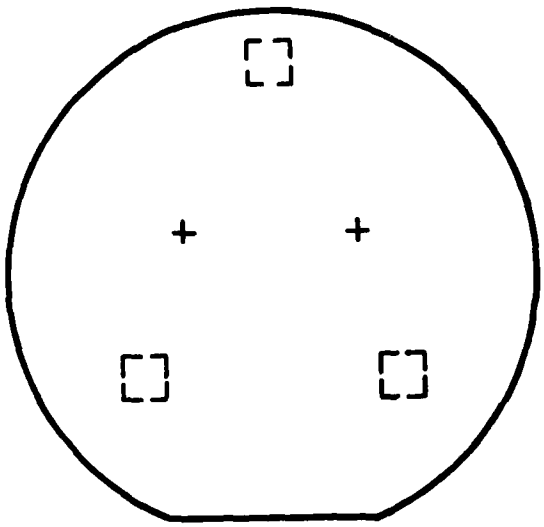

Figure 27. Placement of Second Markers

high sensitivity and commercial availability. Unfortunately, on the initial attempt to construct the SN74S201A, a serious oxide defect problem was discovered that was caused by the failure of PBS resist to provide adequate masking to buffered HF etching. Oxide breakdown to voltage measurements subsequently confirmed that two minutes of HF etching with 4500Å of PBS generated 150-200 defects/cm^2 and even more unexpectedly that with 9000Å of resist 200-250 defects/cm^2 were generated.[8] An example of such a defect is shown in the Scanning Electron Microscope (SEM) micrograph in Figures 28 and 29.

A new high-speed positive resist, TI-313, to be used for oxide plasma etching application was being developed concurrently with the early efforts to make the SN74S201A. The details of monomer synthesis and polymerization have been well established and a high molecular weight (100K MW) narrow dispersivity, copolymer is being provided for formulation into a resist (TI-313). This resist was successfully evaluated for coating thickness, pinhole density, sensitivity, resolution, etch resistance, adhesion, thermal flow and thermal stability.

Xylene is used as a solvent in the formulation of TI-313 to provide the optimum combination of solubility, wettability, evaporation rate and viscosity that produces uniform defect-free coatings by spinning. A solids content in the range of 10-14% is convenient for film thicknesses in the range of 0.3-1.2 μm. A spin speed versus thickness chart for a 10% solution of TI-313 is shown in Figure 30.

Figure 28. SEM of a Pinhole Defect Site

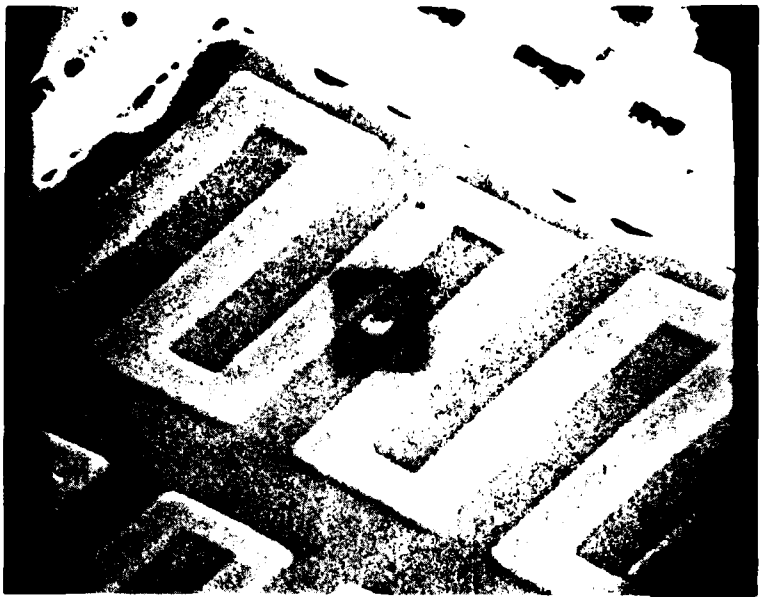

Figure 29. SEM Array Containing Defect Shown in Figure 28

Pinhole studies showed less than 2 defects/cm^2 in 8000Å of TI-313 and its plasma erosion rate during oxide plasma etching was only 175 Å/min. This compares quite favorably with standard photoresists and is much better than PBS. Exposure tests on TI-313 indicate that an exposure in the range 2 to 5 μC/cm^2 can be used for proper feature sizes depending on thickness and development. Figure 31 shows a plot of unexposed thickness remaining as a function of exposure under conditions where development time has been adjusted for equal sized lines and spaces. Doses much in excess of 6 μC/cm^2 lead to significant amounts of cross-linked material not removed by developer. This causes problems in areas that are multiply scanned such as over alignment markers or areas where patterns overlap slightly because of pattern generator errors. Standard practice then was to use half the critical cross-linking dose or about 2 to 3 μC/cm^2.

Patterns were developed in TI-313 by spraying for 90 seconds with a 5:1:1 mixture of 2-ethoxyethanol/2.6-dimethyl-4-heptanone followed by a 15-second rinse with 2-propanol. One of the disadvantages of TI-313 appears to be that the ratio of developing rates of unexposed to exposed resist is very low. Because of a low ratio of developing rates of unexposed to exposed resist, this exposure level of 2 to 3 μC/cm^2 results in longer development times to clear exposed patterns down to the substrate. As shown in Figure 31, this longer develop time results in a loss of 50% of the film thickness in the unexposed areas. Resolution also suffers somewhat from the forced development with usable minimum dimensions on the order of 2 μm for 1 μm resist thickness.

Thermal analyses of TI-313 films have shown that the material cross-links in the region of 170°C and begins thermal decomposition in air at about 190°C. Also patterns in the resist begin to flow at 160°C. The baking of the resist after coating and after development is done in a three-zone, belt oven at temperatures of 100-120-140°C in each zone respectively for 15 minutes.

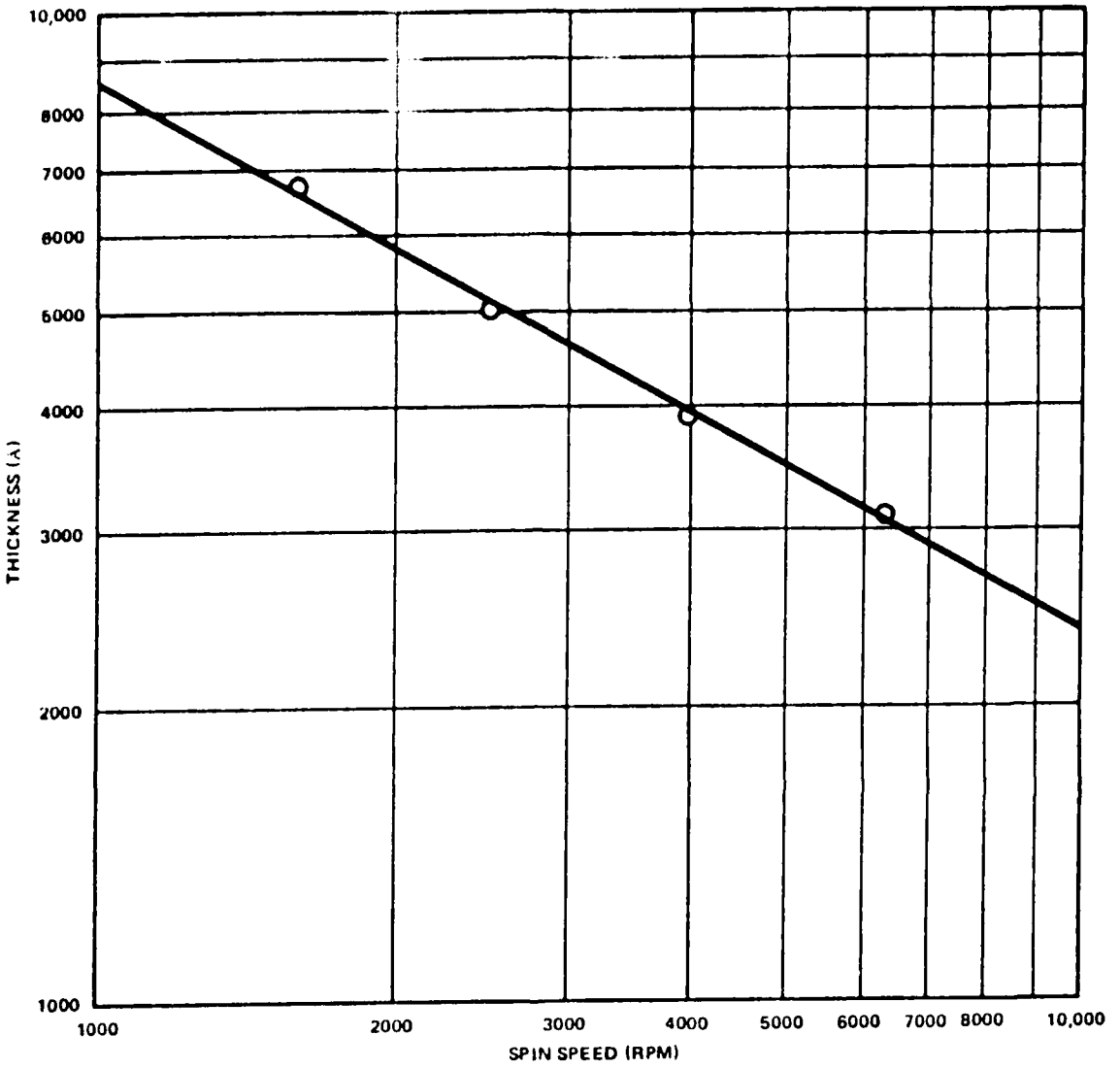

Figure 30. Spin Speed versus Thickness – TI-313 10%

The final process developed for using TI-313 for patterning all levels but leads on the SN74S201A is as follows:

1.	Coat TI-313	10,000Å
2.	Bake	100°-120°-140°C, 15 min
3.	Expose pattern	Dose 2.5 $\mu C/\mu m^2$
4.	Spray, develop, rinse, dry	
5.	Bake	100°-120°-140°C, 15 min
6.	Plasma descum	O_2, 1.5 torr, 100 W, 2 min

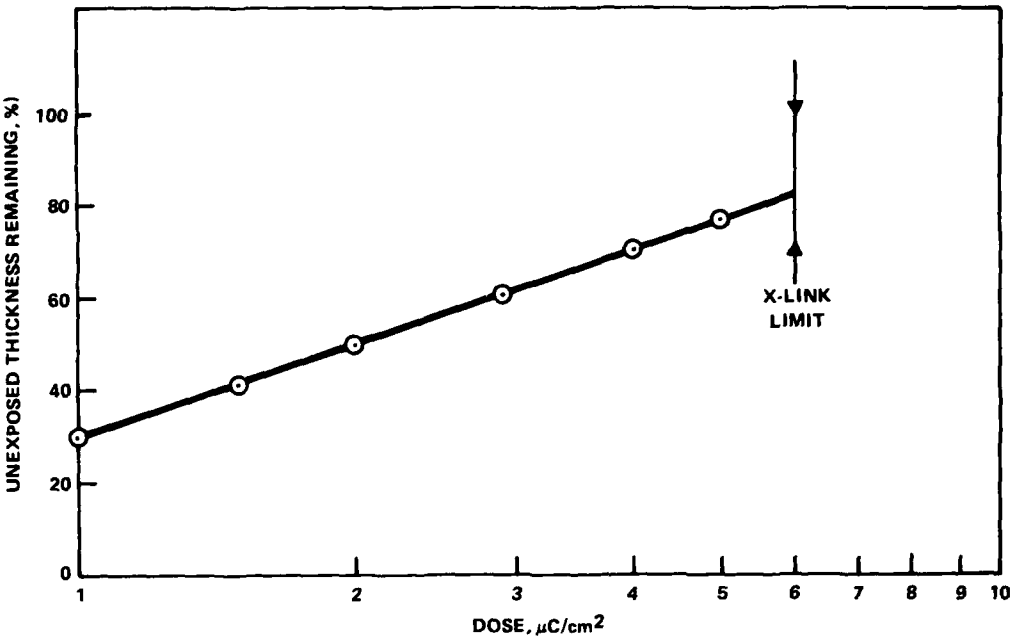

Figure 31. Percent of Unexposed Thickness Remaining as a Function of Exposure Dose where Development Time is Adjusted for Proper Feature Size

For patterning leads, TI-309, a high-speed negative electron-resist was developed in SREL at Texas instruments. This resist was developed for plasma etching of Si, Si_3N_4, poly Si, W, Ti, Mo, Ta, and Al. It is also very effective for masking alkaline aqueous etches for Al. TI-309 is a rubbery material and makes good coatings from xylene solutions. Curves for thickness vs spin speed are shown in Figure 32. The unexposed material is thermally sensitive to cross-linking and must not be heated above 80°C. Resolution and contrast of TI-309 are very good when compared with other negative e-beam resists. Figure 33 shows a plot of line width vs dose for TI-309 where the exposure required for a nominally 200 μinch line is 2.6 $\mu C/cm^2$.

A PtSi/TiW Barrier/Cu-doped Al metallization system was used for forming leads on the SN74S201A. The metal patterns were delineated in TI-309 resist and were etched in an alkaline ferricyanide aqueous etchant. This system has a useful 2.5 μm line and space capability. The SEM in Figure 34 show examples of the good edge definition and step coverage.

The detailed process for patterning the leads of the SN74S201A with TI-309 is as follows:

1.	Coat TI-309	8000Å
2.	Bake	70°C, 15 min
3.	Expose	Dose 2.6 $\mu C/cm^2$
4.	Spray, develop, rinse, dry	
5.	Bake	140°C, 15 min
6.	Plasma descum	O_2, 1.5 torr, 100 W, 2 min

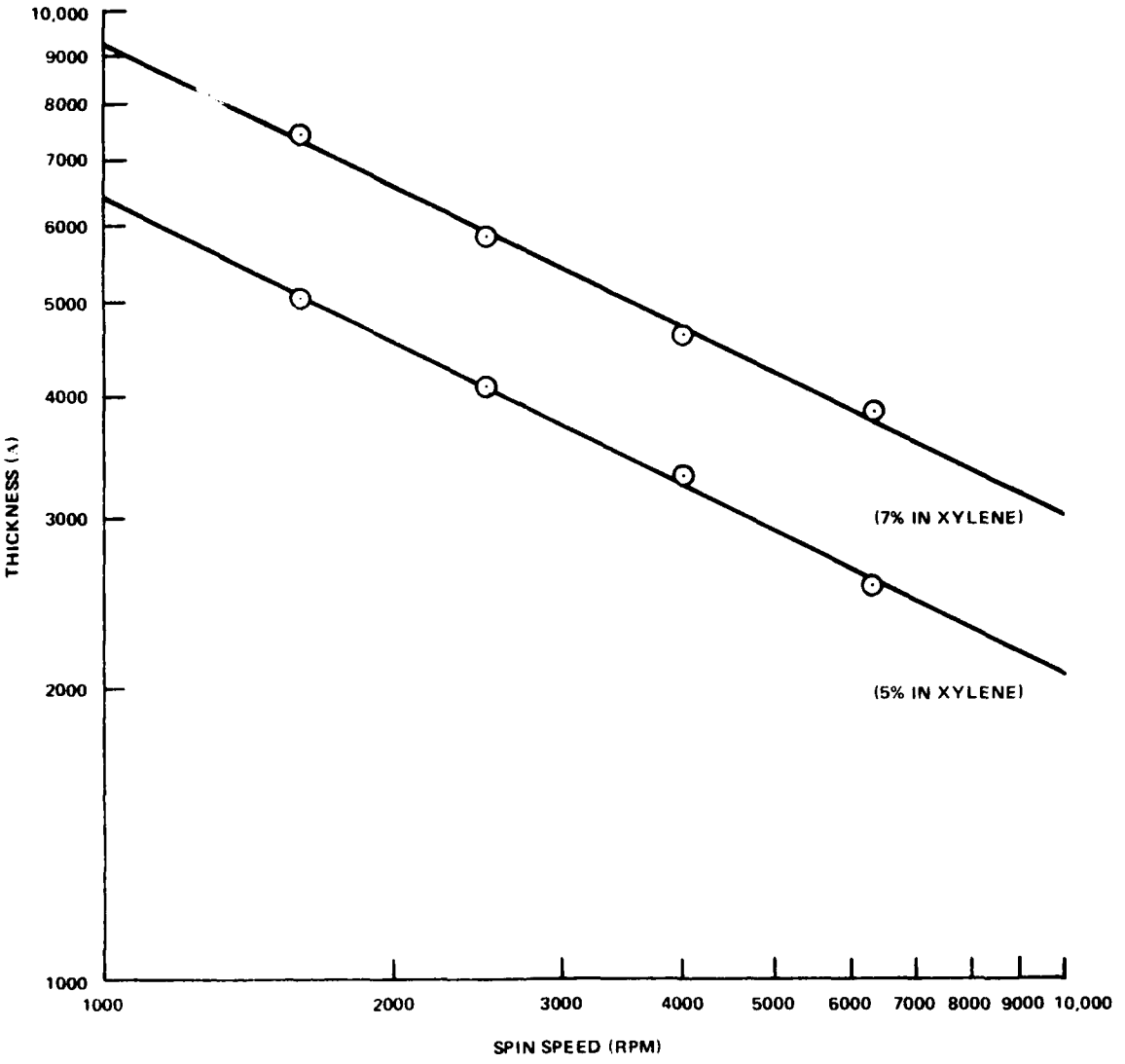

Figure 32. TI-309 Resist

f. PLASMA ETCHING

Despite the useful pattern generation capability of TI-313, its adhesion to SiO_2 is poor and severe undercutting occurs when using TI-313 as a wet etch mask in buffered HF. On the other hand, TI-313 has excellent stability in plasma etching and its removal rates (50Å/min shielded, 175Å/min unshielded) are much lower than PBS or PMMA and are comparable with some negative resists.

To etch the 6000Å of SiO_2 at the DUT and isolation levels, a CF_4/O_2 (4%) plasma etch in a shielded tubular reactor was used (300 W, 1.0 torr). The SiO_2 was etched down to about 1500-2000Å in the plasma and the remaining oxide was etched in buffered HF. This process yields excellent edge profiles as shown in Figure 35.

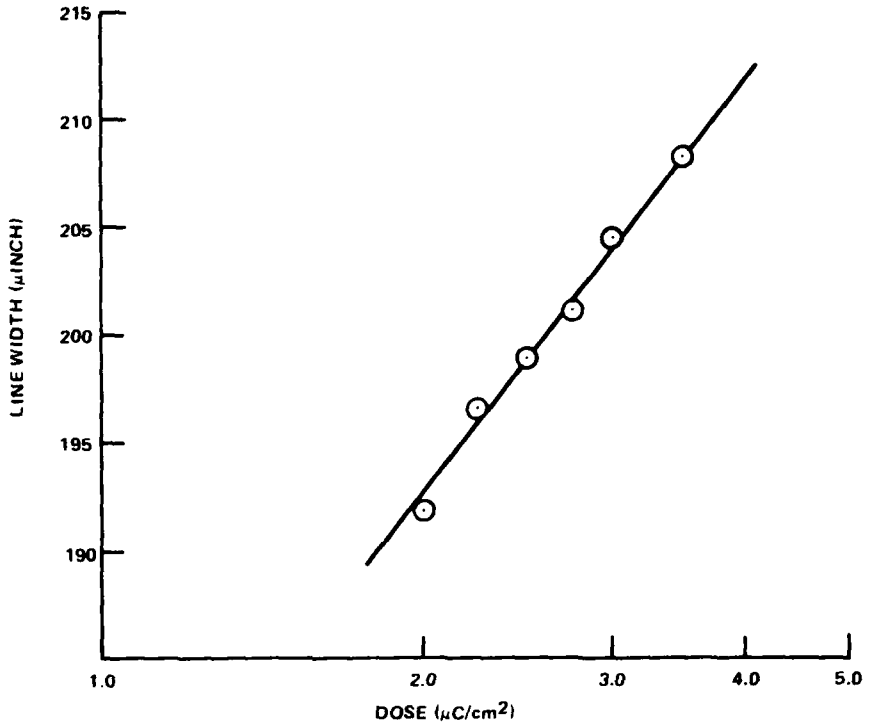

Figure 33. Line Width vs Dose – TI-309 Resist

The CF_4/O_2 plasma etching process cannot be used at the base, emitter or contact levels because there are at least two different oxide thicknesses to etch at each level. When the thinnest oxide has completed etching, the silicon beneath is exposed to the very vigorous CF_4/O_2 plasma and is etched at ten times the rate of the oxide remaining to be etched in other areas. This problem was solved by implementing a C_4F_8/CO_2 plasma etch process which etches Si at only one-fourth the rate of SiO_2. The etching is done in a parallel plate reactor using the flows and conditions outlined in Table X. The process is sensitive to the ratio of C_4F_8 to CO_2. Enough CO_2 must be used to eliminate deposition, but too much CO_2 cuts down on the etch rates. Although the removal rate of TI-313 as shown in Table X is high, it is still low enough to allow etching to completion at any level of the process without using all the resist. Also, the Si rate is low enough to allow for the overetching which must occur to be sure that all windows are open, without fear of etching through any junctions.

To illustrate the effectiveness of the TI-313/plasma etch process as well as the excellent level-to-level realignment accuracy achieved on EBMIII, a series of photomicrographs of the SN74S201A devices after each level of patterning and etching is shown in Figure 35.

4. Material Processed

Of the 11 lots which were started for the confirmatory samples and pilot run, four lots were completed, lots 100, 106, 107, and 110. The material which failed completion were lots 101, 102, 103, 104, and 105 which were lost due to resist removal during plasma oxide etch at either DUF or

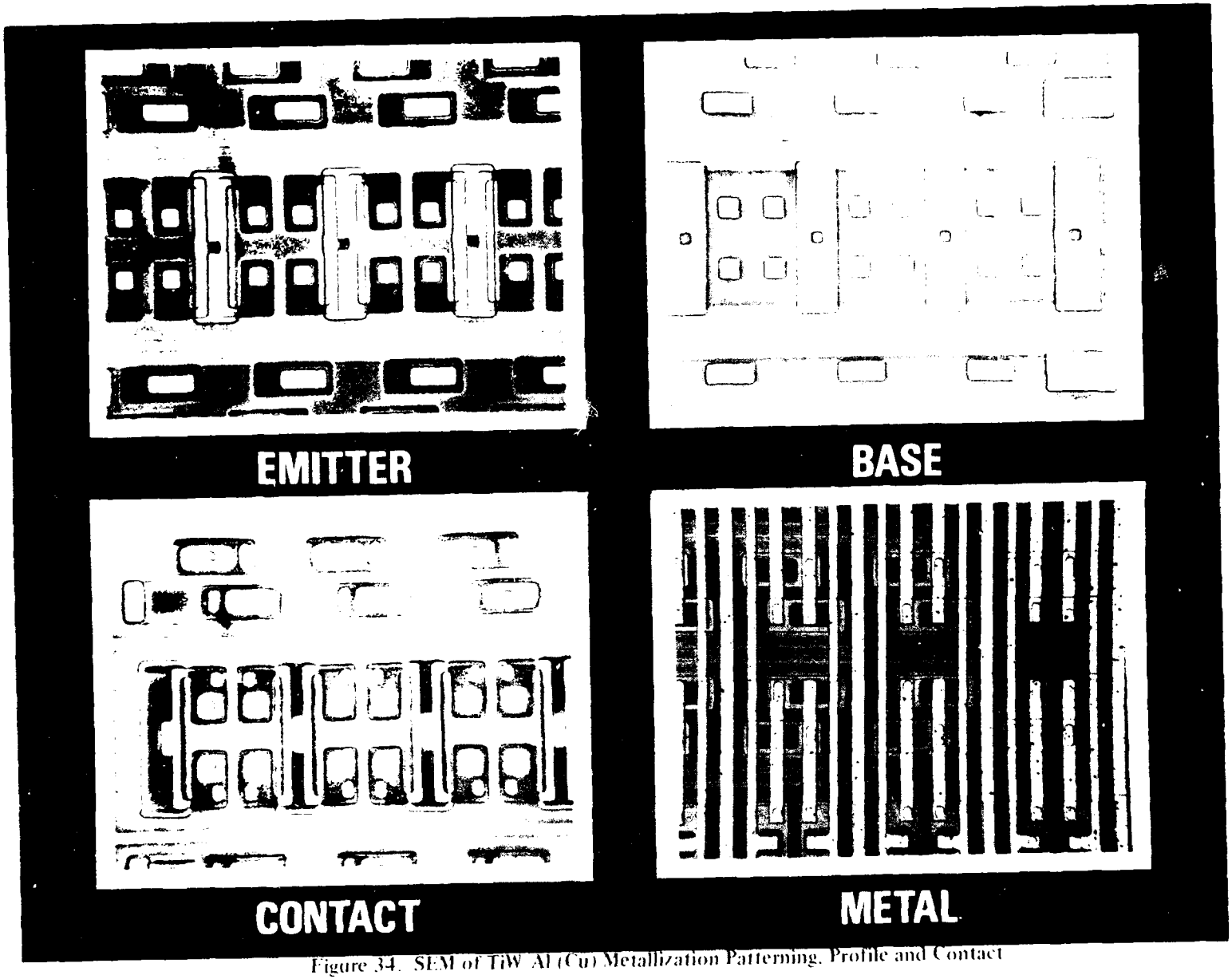

Figure 34. SEM of TiW Al (Cu) Metallization Patterning, Profile and Contact

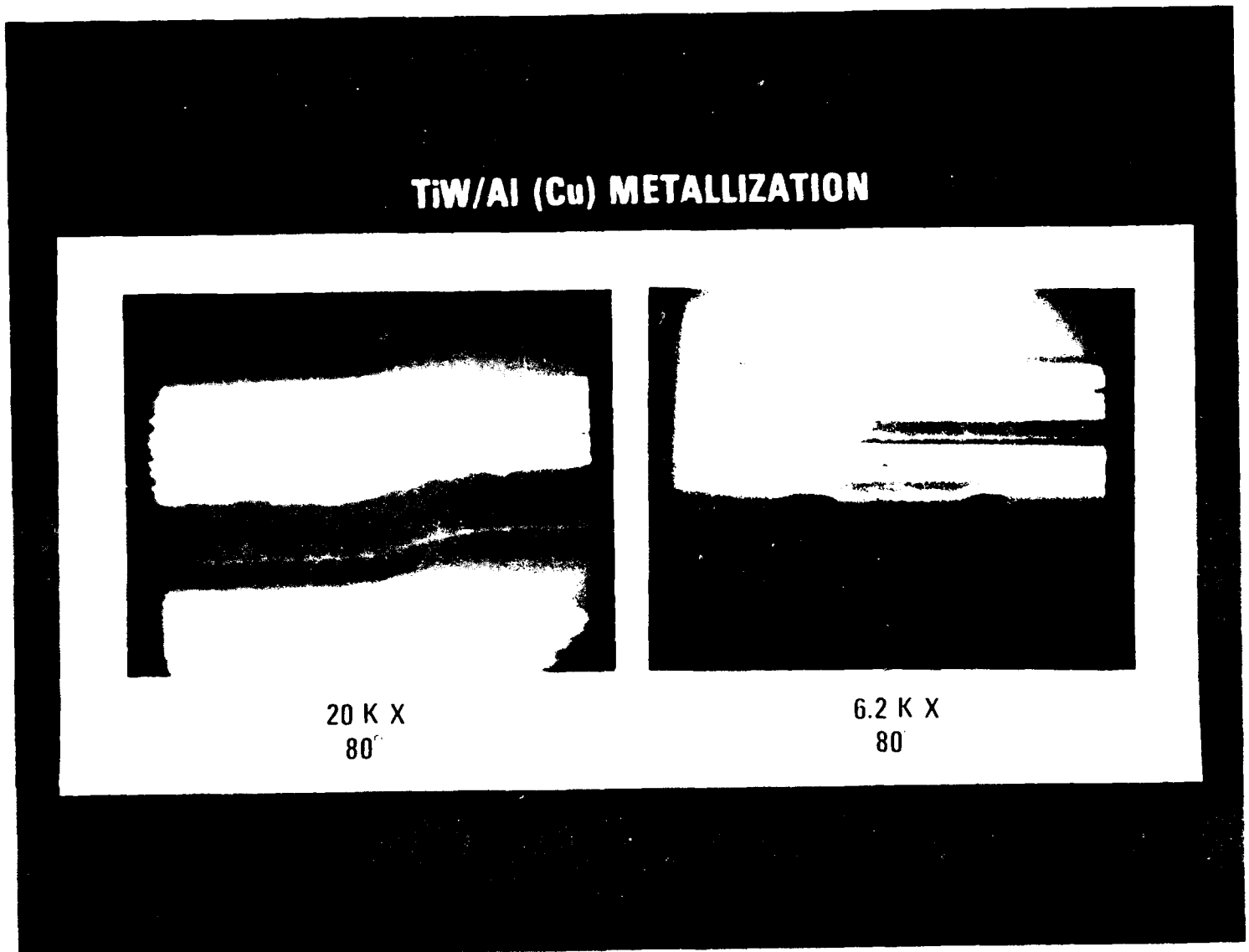

Figure 35. Photomicrographs of SN745201A Memory Area After Each Level of Lithography and Etching

Table X C_4F_8/CO_2 Plasma Etching

Flow Rates	C_4F_8 – 150 cc/min
	CO_2 – 50 cc/min
Pressure	0.35 torr
Power	900 watts
Temperature	55° + 5°C
Etch Rates	SiO_2 – 200 Å/min
	TI-313 – 175 Å/min
	Si – 50 Å/min

isolation O.R. Also uncompleted were lots 108 and 109 which were lost at DUF O.R. because of drift in the slice platform of the e-beam machine during patterning caused by a laser interferometer malfunction, which resulted in the DUF pattern being misaligned on the slice to such an extent that the isolation and subsequent levels could not be aligned to it.

Although lots 106 and 107 were completed, they did not yield devices suitable for testing beyond initial electrical tests. Of the 17 slices which started in lot 106, only 12 were completed and probed with the High Speed Measurements System (HSM). The HSM is a probe system which performs functional and dc parametric measurements tests on the individual bars on the slice. Although the lot yield at this test was only 7.4% for 289 good electrical bars (GEBs), it is significant that one slice had a yield of 40% for 130 GEBs. Table XI lists the bar yield for each of the slices in this lot. Subsequent analysis of the low yielding slices revealed that many of the contacts had not been totally cleared of oxide which prevented the metal from forming contact with the silicon. The photoresist lot which accompanied this e-beam lot had an overall yield of 17%, with the highest slice yield being 26%. The highest individual slice yield for the e-beam material is nearly twice that for the photoresist material, which indicates the capabilities of e-beam lithography.

Lot 106 encountered further problems when the slices went through the diamond saw to cut at the 289 bars for packaging. For this lot, 2% Cu doped Al was used at metal evaporization to ensure adequate step coverage. As the slices were cut with the high-speed diamond saw, the coolant water reacted with the phosphorous-doped emitter oxide forming a dilute phosphoric acid which corroded the bonding pads. The rest of the leads pattern on the slice were protected with the silicon-nitride overcoat. This corrosion made bonding to the pads difficult to impossible. Tests with the numerical exerciser for memories (NEM) resulted in only 117 bars that passed both dc and ac tests. Since the bonds to corroded pads would certainly lead to trouble during environmental tests, these units were not tested further.

To ensure the contacts of lot 107 were open, each slice was carefully inspected at the plasma etch station. After it was determined that all of the contacts were visually open, each slice was hand probed to determine the current gain, beta, of three transistors on each slice. This was to assure that the contacts were indeed electrically open. For comparison, the photoresist material, lot 7, was also hand-probed. The results of these measurements are shown in Table XII. Since the desired beta range is 30 to 60, it is clearly evident from the data in Table XII that lot 107 was not a good lot. It was, however, completed through leads with the hope of getting some good units. When probed

with the HSM, the photoresist lot yielded 2227 GEBs for a lot yield of 29%. The e-beam lot yielded only 40 bars, 36 from slice 47 and 4 from slice 38. On analysis to determine why the current gain of lot 107 was so high, making it yield effectively 0%, it was discovered that during emitter O.R. that along with removing oxide for the emitter pattern over the bar for some reason 0.5 μm of silicon had also been removed. Since the base diffusion was only 1.0 μm to start with, this let the 0.5 μm emitter diffusion penetrate the base, causing CEO shorts or high betas with consequent 0% yield.

Table XI. Lot 106 Yield Data

Slice No.	GEBs HSM	GEBs NEM
1	0	0
16	0	0
4	0	0
30	0	0
29	1	0
31	4	0
18	15	0
25	16	0
22	44	–
17	37	31
28	42	–
27	130	86
12	289	117

Table XII. Current Gain as Measured on Three Devices on Each Slice

E-Beam Lot 107		Photoresist Lot 7	
Slice No.	Beta	Slice No.	Beta
34	420-350-375	8	93-90-81
43	230-175-300	5	92-88-86
35	CEO Short	4	63-60-65
40	CEO Short	3	61-64-62
47	110-110-120	6	56-55-43
33	320-370-340	7	70-72-65
41	210-250-270	9	46-45-48
38	175-165-170	2	94-100-72
		15	75-76-92
		13	54-52-51
		1	73-78-100
		11	58-62-60
		12	86-80-77
		14	85-90-91

Lots 100 and 110 were then the only lots completed which yielded usable parts. From the six slices which comprised lot 100, 170 GEBs were obtained at HSM multiprobe for a yield of 9%. The photoresist material which accompanied this lot had a yield of 20%. These 170 bars were further tested for delivery as First Article Units. A discussion of these tests and their results follows.

Lot 110 had a yield of 23% from 12 slices at HSM multiprobe for 970 GEBs. The associated photoresist lot had a yield of 29% from 14 slices. This e-beam lot gave the units that were further tested as Pilot Production Units. A discussion of these tests is presented in the next subsection.

D. ELECTRICAL AND RELIABILITY TESTING

1. Electrical Testing

Electrical testing for the 256-bit RAM was accomplished using existing automatic test systems at Texas Instruments. The basic equipment used for the tests was the High Speed Measurement (HSM) system and the Numerical Exerciser for Memories (NEM).

The HSM was used to test the memories while they are in slice form. It performed all the dc tests such as I_{CC}, V_{OL}, I_{OH}, etc., and also the functional testing on the memory cells and peripheral circuitry.

The NEM was used to test the memories after they have been packaged. Programming of the NEM is accomplished with a RAM supplying instructions for support as well as test instructions to implement exercise algorithms.

The memories were tested according to U.S. Army Electronics Command specification SCS-517 (April 27, 1978).

2. First Article Units

The 170 GEBs found at HSM multiprobe in lot 100 were packaged and screened as required by SCS-517 (4-27-1978) and METHOD 5004 or MIL-STD-883. After completion of these screening tests, 50 units were selected and further tested according to METHOD 5005 of MIL-STD-883. These units passed all of the electrical measurements at 0°C, 25°C, and 70°C. However, the maximum operating speed of the units was about 20% slower than desired. It is noted that the units were expected to be slow due to the resist being inadvertently removed during the contact oxide etch step. The removal of the resist resulted in the field oxide being reduced in thickness by about 20%. This, in turn, caused the lead capacitance of the circuit to increase by 20% since that capacitance varies inversely as the oxide thickens. This capacitive loading of the circuit was expected to slow the devices switching times. A complete discussion of these tests and their results may be found in "Test of First Article Units" dated July 14, 1978.

3. Pilot Production Units

The e-beam lot 110 was accompanied through processing with lot 10, a photoresist lot. To gain tighter control on this e-beam lot, the photoresist material was plasma etched simultaneously with it. After processing through contact and visually examining every slice to be certain all the contact windows were open, each slice was hand-probed. The results of this probe test for current gain (beta), V_{CBO}, V_{CEO}, and V_{EBO} are shown in Table XIII for the e-beam lot and Table XIV for the photoresist lot. βf was measured on these devices on each slice. The other parameters were measured on only one device per slice. As seen on examination of these data, the e-beam resist and photoresist material are effectively electrically identical. Further, the parameters are exactly in the range they should be for the memories to function properly.

With the assurance that this material should yield properly, it was processed through metal deposition and the lead patterns etched. At this point the material looked quite good visually and it was elected to do a sample test on the HSM multiprobe. Five slices were randomly picked from both the e-beam resist lot and the photoresist lot for this purpose. Both samples of material had a yield of 27%.

In view of these good results, the remainder of the two groups of material were tested on the HSM multiprobe to determine the potential GEBs prior to protective overcoat deposition. The 14 e-beam slices had 1064 GEBs for a yield of 24%. The photoresist lot yield was 29%. This slight difference in yield can be attributed to the fact that the e-beam material experiences considerably more handling than the photoresist material. If the material were processed in a production environment, this would not be the case and the two groups of material would in all likelihood yield the same.

After these post leads pattern tests were completed, a nitride protective overcoat was then deposited on the slices and the bonding pads etched open. During this process step, one of the higher yielding e-beam resist slices was broken. Consequently, when the remaining 13 slices were tested on the HSM multiprobe at post silicon-nitrides O.R., the yield dropped to 23% for 970 GEBs. The photoresist material was processed through silicon nitride without loss and the yield remained at 29% and was not tested further.

The e-beam material was sent on to back-grind and saw to prepare the individual chips on the slices for packaging. Unfortunately, another slice was destroyed at back-grind, leaving a potential of 868 GEBs. These bars were then alloyed down in packaging and the bonding pads on the chips stitched to the package lead pads. From the 868 units submitted, 800 units were returned. The other units were primarily lost at alloying into the package with some units being destroyed by stitching errors.

These 800 units were submitted for precap inspection and the remaining electrical, mechanical, and environmental tests as required by SCS-517 (4-27-78). These remaining tests are discussed in the next portion of this report.

Table XIII. E-Beam Lot 110 Contact Probe Parametric Data

Slice No.	β_f	V_{CBO}	V_{CEO}	V_{EBO}
2	70-70-66	16.4	4.5	5.8
4	62-60-47	21.0	6.1	5.8
6	42-39-47	22.0	7.8	5.8
10	50-55-54	17.8	5.5	5.8
12	45-43-47	21.0	7.2	5.8
14	46-47-46	18.0	6.2	5.8
16	44-45-44	16.8	5.6	5.8
18	52-56-58	19.0	6.0	5.8
22	45-47-45	20.0	6.1	5.8
24	52-52-48	21.0	6.6	5.8
26	34-47-50	23.0	7.5	5.8
28	50-53-48	18.6	5.8	5.8
30	42-48-48	23.0	8.0	5.8
32	50-51-53	20.0	6.4	5.8

Table XIV. Photo Resist Lot 10 Contact Probe Parametric Data

Slice No.	β_f	V_{CBO}	V_{CEO}	V_{EBO}
1	42-43-42	19.5	6.6	5.8
3	57-59-63	18.2	5.8	5.7
5	52-50-48	18.6	6.0	5.7
7	48-57-65	18.0	6.0	5.8
9	49-54-50	18.4	6.1	5.8
11	55-56-58	21.0	6.5	5.8
13	65-53-54	20.0	6.0	5.8
15	52-55-50	23.0	7.6	5.8
17	44-48-42	19.6	6.5	5.8
19	54-57-58	19.0	6.2	5.7
21	53-52-50	20.0	6.7	5.8
23	76-65-61	18.1	5.2	5.8
27	54-57-56	21.0	6.6	5.8
31	58-65-68	18.4	5.2	5.8

4. Performance Tests of Pilot Production Units

a. GENERAL TEST PROCEDURE

The required electrical performance characteristics are specified in Table 1 of SCS-517 and apply over the full recommended ambient operating temperature range.

The Electrical Test Requirements are specified in Table II and Table III of that document. The subgroups of Table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in Table II. All electrical tests were performed on packaged units, dc tests were performed on an HSM and ac tests were performed on a NEM.

The HSM is a dc parametric measurement unit. It is used to perform dc parametric tests and performs functional testing on the memory cells and peripheral circuits. Diagnostic and calibration tests are performed daily and the equipment certified every 10 working days by Quality Control.

All environmental tests and measurements were performed in the Environmental Laboratory of the Quality and Reliability Assurance Department (QRA). All of the equipment in the environmental laboratory is calibrated and certified on a regular basis for use on military programs.

The burn in was performed by Reliability Inc. of Houston, Texas. This company has their own Quality Control personnel and are qualified to perform testing on military programs. All tests were performed in accordance with the test plan "Test of Pilot Production Units" dated 9-20-79.

b. SCREENING

Screening was conducted on all devices in accordance with Class B of Method 5004 of MIL-STD-883 and SCS-517 (April 27, 1978). Three devices for the bond strength test specified in Method 5005 of MIL-STD-883 were randomly selected immediately following the internal visual inspection and prior to sealing. The tests conducted were as follows:

Test	Specification Requirement MIL-STD-883, Method 5004 Class B Method
1. Internal visual	2010, test Condition B
2. Stabilization bake	1008, 24 hrs, test Condition C
3. Temperature cycling	1010, test Condition C
4. Centrifuge	2001, test Condition E Y_1 plane
5. Hermeticity, fine and gross	1014, test Condition B and C_2
6. Burn-in test	1015, 168 hrs, 70°C
7. Final electrical test	Per SCS-517 date April 27, 1978,
a. Static tests	Table II, Subgroups 1,2,3,7,9
25°C	
0°C	
70°C	
b. Functional test	
25°C	
c. Switching test	
25°C	
8. External visual	2009

The internal visual inspection was conducted in the assembly and package area. The stabilization bake, temperature cycling, centrifuge and hermeticity tests were performed in the Environmental Laboratory of the Quality and Reliability Assurance Department.

As discussed previously, 800 units from the pilot run were submitted for the remainder of the test required by SCS-517. When the electrical tests on the 800 units were performed, post internal visual and after capping as required as a part of the stabilization bake test, it was found that only 732 units passed the required tests on the HSM. These 732 units remained good after stabilization bake and were sent on through the remainder of the test. During the hermeticity fine leak test, 19 units failed, leaving 713 units. When these units were tested on the HSM as required, prior to burn-in, only 575 units passed. The 138 devices which failed at this point were lost because of the stresses encountered during the temperature cycling test and the centrifuge test. Of these 575 units which passed the HSM measurements, only 529 had the switching speeds required to pass the NEM measurements which were also made prior to performing the burn-in test. Then only these 529 units were submitted to Reliability Inc. for burn-in at 70°C for 168 hours, as required. When the final electrical tests were performed after burn-in, the NEM passed 523 devices at 25°C and the HSM passed 512 devices at all these temperatures: 0°C, 25°C, and 70°C. This loss at burn-in was very slight, tending to indicate the previous screening test had essentially eliminated the weaker units. These 512 units readily passed the external visual requirements and were submitted for quality conformance inspection.

e. QUALITY CONFORMANCE INSPECTION

After completion of the screening tests, the 512 devices which passed were tested in accordance with SCS-517 and Method 5005 of MIL-STD-883. Tables XV, XVI and XVII list the tests that were performed and the specification requirements. Table XVIII lists the LTPD, sample size, and acceptance number for each test.

Table XV. Group A Inspection

TEST	NAME	SPECIFICATION REQUIREMENT MIL-STD-883, METHOD 5005 CLASS B, METHOD
1.0	*Electrical test* a. Static test 25°C 70°C 0°C b. Functional test 25°C 70°C 0°C c. Switching test 25°C	*Per SCS-517* dated April 27, 1978 and Table 1 of Method 5005, Subgroups 1,2,3,7,8,9

Table XVI. Group B Inspection

TEST	NAME	SPECIFICATION REQUIREMENT MIL-STD-883, METHOD 5005 CLASS B, METHOD
2.1	Physical dimensions	2016
2.2	Resistance to solvents	2015, 2014
2.3	Bond strength Thermocompression	2011, Condition C or D
2.4	Solderability	2003, Soldering temperature of 260 ± 10°C
2.5	Lead integrity Hermeticity a. Fine b. Gross	2004, Condition B_2 1014

Table XVII. Group C Inspection

TEST	NAME	SPECIFICATION REQUIREMENT MIL-STD-883, METHOD 5005 CLASS B, METHOD
3.1.1	Thermal Shock	1011, Condition B
3.1.2	Temperature cycling	1010, Condition C
3.1.3	Moisture resistance	1004
3.1.4	Seal, fine, gross	1014
3.1.5	End point electrical parameters	Per SCS-517, dated April 27, 1978, Table II
3.2.1	Mechanical shock	2002, Condition B
3.2.2	Vibration	2007, Condition A
3.2.3	Constant acceleration	2001, Condition C
3.2.4	Seal, fine, gross	1014
3.2.5	End Point electrical parameters	Per SCS-517, dated April 27, 1978, Table II
3.3	Salt atmosphere	1009, Condition A
3.4.1	High temperature storage	1008, Condition C 1000 hr
3.4.2	End point electrical parameters	Per SCS-517, dated April 27, 1978, Table II
3.5.1	Operating life testing	1005, 70°C storage, 1000 hrs
3.5.2	End point electrical parameters	Per SCS-517, dated April 27, 1978, Table II

Table XVIII. Test LTPD and Sample Size

GROUP	TEST NO.	LTPD	SAMPLE SIZE	ACCEPTANCE NUMBER
A	1,a,1	5	77	1
	1,a,2	7	55	1
	1,a,3	7	55	1
	1,b,1	5	77	1
	1,b,2	10	39	1
	1,c,1	7	55	1
B	2.1	15	25	1
	2.2	4 Devices no failures	4	0
	2.3	15	43 bonds (3 Units)	3
	2.4	15	43 leads (3 Units)	3
	2.5	15	25	1
C	3.1.1 to 3.1.5	15	25	1
	3.2.1 to 3.2.5	15	25	1
	3.3	15	25	1
	3.4.1 and 3.4.2	7	55	1
	3.5.1 and 3.5.2	5	77	1

The specifics of these tests, that is, precisely how they were conducted, what equipment was used and calibration dates, operation doing the tests, and the details of their results are given in the report, "Performance Test Under Laboratory Conditions for Microcircuit 256 Bit Bipolar Random Access Memory," *submitted* April 25, 1979. As reported there, the Group A and Group B tests were completed without failure. From the Group C tests, the subgroup undergoing the thermal shock sequence of test and the subgroup undergoing the mechanical shock sequence of tests, passed all tests without failure. Likewise, the subgroup which went through the salt atmosphere tests passed without failure. All of the devices which went through the 1000-hour high-temperature storage tests were good except for one unit that failed the ac switching test at both 0°C and 70°C. This device did, however, pass all other electrical tests. Similarly, all of the units put on operating life tests passed all tests except one device, which failed the ac switching test at 0°C and 70°C after passing all other electrical tests.

On completion of the required electrical tests on the devices which had been in high-temperature storage and operating life tests, these devices were electrically tested on the HSM and NEM at −55°C and 125°C. Under these extreme temperatures, none of the devices passed. This failure is purely a circuit design problem and is totally unrelated to processing.

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SECTION III
CONCLUSIONS

In distinct contrast with much of the currently published e-beam direct writing work that seeks to demonstrate improved device performance and packing density capabilities, the object of this program was to develop a manufacturing capability for standard bipolar circuits of conventional design using existing e-beam direct writing equipment. In particular, a pilot-line demonstration of significant yields of conventional 4-5-μm design rule integrated circuits which were fully tested to military specifications for performance, quality and reliability was of paramount inportance. Achievement of this objective then establishes a baseline for direct e-beam writing in production and provides a significant stepping stone for implementation of e-beam technology in VLSI circuit fabrication.

The vehicle used for this demonstration was a standard TTL 256-bit bipolar RAM (SN74S201A) using a single-level metal, junction isolated, Schottky clamped bipolar process. Emphasis was placed on utilizing a new class of high-speed electron resist (TI-309 and TI-313) in combination with selective plasma etching techniques in order to establish economical next generation VLSI processes. A vector scan, laser controlled e-beam direct writing system (EBMIII) developed in our laboratories with fully automatic slice alignment was used for patterning of these devices. To determine that e-beam direct writing yields devices with no degradation in performance or reliability, optically patterned split lot controls were fabricated in parallel and used for comparative testing.

On this contract it has been demonstrated that e-beam lithography can be used to fabricate bipolar devices to military specifications with no yield degradation or damage. No conclusive yield improvement results were demonstrated since this device is not limited in yield by lithographic factors, but rather by diffusion processes. This program has established an e-beam lithography baseline process utilizing high-speed electron resists and plasma etching techniques for fabrication of bipolar microcircuits. These processes will allow fabrication of many high density VLSI devices in the near future and have already allowed fabrication of the 1 μm e-beam SBP0400E. In general, e-beam technology will allow greater circuit design complexity and flexibility leading to better performance, lower cost, higher reliability integrated circuits.

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