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IMPROVEMENT IN GaAs DEVICE YIELD AND PERFORMANCE THROUGH SUBSTRATE DEFECT GETTERING

INTERIM TECHNICAL REPORT

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IMPROVEMENT IN GaAs DEVICE YIELD AND PERFORMANCE THROUGH SUBSTRATE DEFECT GETTERING

Interim Technical Report

Prepared by:

T. J. Magee, J. Peng, J. Hong and R. A. Armistead

January, 1980

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The gettering of Cr and front-surfaces defects by mechanically produced back-surface damage in semi-insulating GaAs wafers has been investigated. It has been shown that improved VPE layers can be grown on pre-gettered substrates. Also, the level of Cr outdiffusing from the substrate during epilayer growth and subsequent annealing is substantially reduced when pre-gettered substrates are used. Thermal stability times of back-surface damage at an anneal temperature of 800°C is typically on the order of 2 - 3 hours, corresponding to the point

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at which major back-surface microstructural damage is largely annealed. Increases in the thermal stability period were attained by encapsulating the back surface with an As-doped SiO_2 layer. Subsequent investigations of Au contacts on GaAs showed that Cr was mobile during 350°C alloying, resulting in gettering within alloy damage regions and subsequent outdiffusion into the Au film.

Device structures (FET) fabricated on VPE layers on pre-gettered GaAs wafers showed considerable improvements in both yield/wafer, noise figures at higher frequencies and input capacitance values.

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CONTENTS

Page

1. Introduction 1

 1.1 Background 1
 1.2 Summary of Results 1
 1.3 Publications 2

2. Gettering of Cr by Back-Surface Mechanical Damage. 3

 2.1 Experimental Procedure 3
 2.2 Results 4
 2.2.1 Transmission Electron Microscopy 4
 2.2.2 Secondary Ion Mass Spectrometry 6

3. Back-Surface Gettering and Cr Outdiffusion in VPE GaAs Layers 10

 3.1 Experimental Procedure 10
 3.2 Results 11

4. Alloying of Au Layers and Redistribution of Cr in GaAs . . 18

 4.1 Experimental 18
 4.2 Results 19

5. Performance of FET Structures Fabricated in VPE Layers on Pre-Gettered Substrates 25

6. Conclusions and Future Experiments 31

References. 32

Distribution List 34

FIGURES

Page

Figure 1. Transmission Electron Micrographs of Back-Surface-Damaged Wafers After Annealing; a) 30 min; b) 180 min. . 5

Figure 2. SIMS Profiles of Back-Surface Gettered Cr in GaAs Wafers; a) Control (no induced damage), Cu-doped, annealed 800°C, 1 hr; b) Cr-doped, annealed 800°C, 0.5 hr; c) Cr-doped, annealed 800°C, 2.5 hr; d) Si-doped, Cr layer (front), annealed 800°C, 1 hr. . . . 7

Figure 3. Defect Density and Cr Concentration Profiles of Back-Surface-Damaged Annealed GaAs Substrates. 12

Figure 4. Optical Micrographs of Etch Figures of Annealed Samples; a) Control; b) Gettered. 14

Figure 5. SIMS Profiles of Cr Concentration in Substrates and VPE Layers After Deposition and Annealing; a) After deposition; b) 800°C post deposition anneal (t_{VPE}=1.7 m) 16

Figure 6. Transmission Electron Micrograph of GaAs Under (1000Å thick) Au Contact Layer After Annealing at 350°C For 1 Minute. 21

Figure 7. SIMS Profiles of (1000Å Au/GaAs Structure After Annealing at 350°C; a) t_A=1 min; b) t_A=3 min; c) t_A=10 min.. 22

Figure 8. SIMS Profiles of (4000Å) Au/GaAs Structure After Annealing at 350°C; a) t_A=1 min; b) t_A=10 min.. 24

Figure 9. Profile-VPE/GaAs (Control) Sample.. 26

Figure 10. Profile-VPE/GaAs (Pre-gettered) Sample. 27

TABLES

Page

Table 1. Device Data - Control (Ungettered) Substrate. 28

Table 2. Device Data - Pre-gettered Substrate. 29

1. INTRODUCTION

1.1 Background

In this research program, it has been shown that mechanical and ion-implantation-induced damage at the back surface of GaAs wafers can be effectively used to getter front-surface defects and heavy metal impurities from the bulk material. It was demonstrated that the mechanical damage process could be optimized to produce maximum gettering efficiencies both in terms of front-surface defect annihilation and removal of mobile Cr from the interior of the sample. Comparative analyses of back-surface ion-implanted and mechanically-damaged wafers showed that the rotary abrasive (mechanical) technique was superior to the ion-implantation method for gettering in GaAs in terms of defect/impurity removal rate, back-surface damage retention time, and reverse annealing or "de-gettering" characteristics.

Recent experiments were directed to extending the investigation of defect and impurity gettering in GaAs, with particular emphasis on the gettering of mobile Cr over a wide range of annealing temperatures. The back-surface-gettering technique was then used as a means of improving substrates for growth of epitaxial layers on semi-insulating wafers and as a step introduced in the process line for production of GaAs-FET device structures.

1.2 Summary of Results

The results of investigations conducted during this reporting period are described briefly in the sections to follow.

- Analysis and identification of Cr gettering and reverse annealing effects by back-surface-damage regions.
- Improvement in back-surface-damage stability times using an As-doped SiO_2 encapsulation layer on the back of the wafer.
- Identification of Cr gettering and outdiffusion during alloying (350^oC) of contact structures on GaAs.

- Growth of low-defect-concentration VPE layers on back-surface (pre-gettered) Cr-doped substrates.
- Reduction of Cr outdiffusion into VPE layers grown on pre-gettered Cr-doped substrates.
- Improved electrical properties of VPE layers on Cr-doped substrates.
- Improvement in the electrical parameters and the device yield of FET structures fabricated in VPE layers on pre-gettered (Cr-doped) substrates.
- Identification of low temperature ($\leq 350^{o}C$) Cr-gettering in GaAs.

1.3 Publications

The following research publications were drawn in part or in total from this program of research.

a) "Back-Surface Gettering and Cr Out-Diffusion in VPE GaAs Layers," Appl. Phys. Lett. 35, 277 (1979).

b) "Alloying of Au Layers and Redistribution of Cr in GaAs," Appl. Phys. Lett. 35, 615 (1979).

c) "Gettering of Au by Back-Surface Damage in GaAs," Phys. Stat. Sol. (A) 55, 161 (1979).

d) "Back-Surface Gettering of Cr in GaAs," Phys. Stat. Sol (A) 55, 169 (1979).

e) "Outdiffusion of Cr in VPE GaAs Layers and Back-Surface Gettering," Extended Abstracts, Vol. 79-2, ECS Meeting, Los Angeles, CA , October 14-19, 1979.

2. GETTERING OF Cr BY BACK-SURFACE MECHANICAL DAMAGE

Gettering of impurities in Si by ion-implantation-induced damage or mechanical damage has been reported[1-6] by a number of investigators. In contrast, there have been few detailed studies of impurity gettering by back-surface damage in GaAs. Recently, it was shown [7] by the present authors that Au impurities could be effectively gettered by dislocation lines introduced into the back surface of GaAs wafers. The Au was observed in the form of precipitates pinned along dislocation lines that extended to a depth of $\simeq 1.5$ μm below the level of damage grooves at the back surface. Correlated transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) data showed the gettering process to be effective for annealing periods not exceeding the thermal stability time, or the time in which major microstructural damage is largely annihilated by annealing at a fixed temperature.

Preliminary studies by the authors have shown that Cr can also be gettered by mechanical or ion implantation damage in GaAs.[8] The purpose of these investigations was to extend the previous studies and to determine the gettering behavior of Cr as a function of annealing duration for variable periods, approaching the thermal stability time at 800°C.

2.1 Experimental Procedure

The gallium arsenide samples used in these experiments were obtained from Crystal Specialties Inc. and Monsanto Corporation. The wafers were of (100) orientation ($\pm 1^{\circ}$) and doped with Si or Cr to levels of 0.008 Ω-cm and 10^{8} Ω-cm, respectively. Mechanical damage was introduced at the back surfaces using a 30-μm particle size and a rotary abrasive technique described elsewhere.[7] All anneals were subsequently done in flowing H_2 at 800°C for periods of 0.5 to 6 hours. Samples for TEM analysis were prepared by conventional jet thinning and sectioning techniques on 2.5-mm x 2.5-mm specimens. Bright- and dark-field electron microscopy was used in all cases to examine the structure of control, damaged and annealed samples.

Secondary ion mass spectrometry was used to obtain Cr impurity concentration profiles at the back surfaces of control and back surface damaged, annealed samples. To obtain calibration data for these experiments, GaAs and Si samples were simultaneously ion implanted with Cr and the integrated Cr content measured in the Si by nuclear back scattering techniques.[9] These data were then used to convert the measured Cr signals from SIMS profiles on GaAs and the resulting data correlated with predicted LSS (as-implanted) profiles.

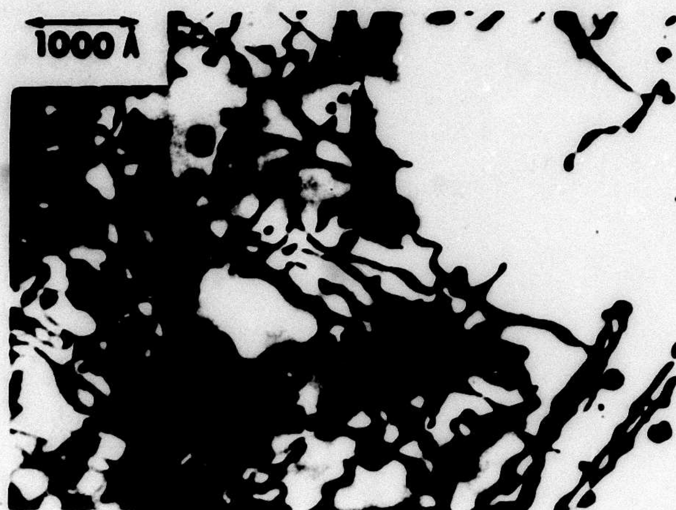
2.2 Results

2.2.1 Transmission Electron Microscopy

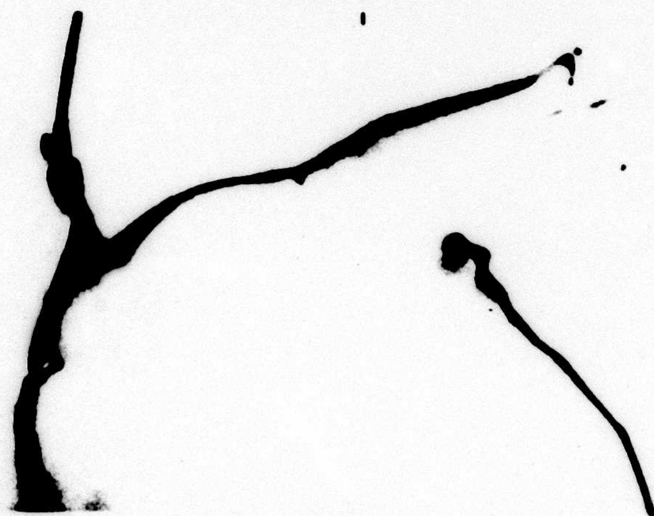
Samples were subjected to rotary back-surface abrasion using a 30-μm particle size, 8000 rpm rotation rate and a total contact time of 30 sec. Specimens were then examined in the electron microscope and micro-structural damage found in the form of laterally continuous forested dislocation nests extending to a distance of $\approx 1.5\ \mu m$ below the depth of damage grooves at the back surface, in agreement with previous results.[7]

Dislocation line structure was observed to be largely annealed after heating for 2 - 3 hours in flowing H_2 at $800^{\circ}C$. Some residual dislocation line structure was found to persist up to anneal periods of 6 hours, but the fractional amount of damage remaining after 3 hours was typically $\leq 10\%$ of the initial dislocation line content.

Figure 1 shows a series of bright-field electron micrographs obtained at the back surfaces of Cr-doped samples subjected to back-surface damage and subsequently annealed at $800^{\circ}C$ for variable periods. It can be observed that the concentration of dislocation lines is considerably reduced as a function of increasing anneal time. Of particular importance, however, is the apparent absence of any identifiable precipitates or impurity segregation sites, either at the edges of dislocation lines or in isolated zones. This result is in sharp contrast to the previous results in which Au was shown reproducibly to nucleate in the form of precipitates pinned along dislocation lines. In all cases, we were unable to clearly



[a]



[b]

FIGURE 1. TRANSMISSION ELECTRON MICROGRAPHS OF BACK-SURFACE DAMAGED WAFERS AFTER ANNEALING; 2) 30 mn; b) 180 min.

identify precipitates in the back-surface damages and annealed Cr-doped samples. From these results, we can infer an absence of Cr precipitation along dislocation lines or a relatively weak strain field from small Cr segregation zones that do not permit adequate resolution to TEM.

To further investigate the possibility of Cr precipitation within the damaged regions, a series of experiments was conducted on selected Si-doped samples shown by SIMS to contain small (unintentional) Cr-doping concentrations of $\leq 10^{16}$ cm^{-3}. Chromium layers of 2-μm thickness were then deposited on the front surfaces by an electroless technique and the uniformity checked by SEM examination. The samples were then heated in flowing H_2 at 800°C for variable periods, as in the previous experiments, and the samples examined at the back surface in the TEM. The micrographs obtained were essentially identical to those shown in Figure 1 and no Cr precipitation was detected, although gettered Cr was clearly detectable by SIMS, as will be discussed in the next section.

2.2.2 Secondary Ion Mass Spectrometry

Figure 2 shows SIMS profiles obtained at the back surfaces of Cr-doped control and mechanically-damaged GaAs samples subjected to anneals at 800°C for variable periods. Also shown for comparison is a representative profile obtained from an annealed, Si-doped (back-surface-damaged) GaAs sample containing a $\simeq$ 2-μm thick Cr layer on the front surface. All SIMS profiles were obtained within homogeneous damage distribution zones at the back surface.

Control (undamaged) samples subjected to 800°C anneals typically show a narrow region of Cr accumulation at the back surface. This is presently thought to be attributable to a slight gettering effect caused by the presence of small amounts of residual defects retained after chemical/mechanical polishing. After annealing of the back surface damaged samples for 1/2 hour, we observe a significant concentration of Cr at the back surface. For all samples, we detected a graded distribution decreasing to background doping levels at depths of $\simeq 1.5$ μm. After annealing for 2.5 hours, the level of gettered Cr is reduced and the concentration gradient

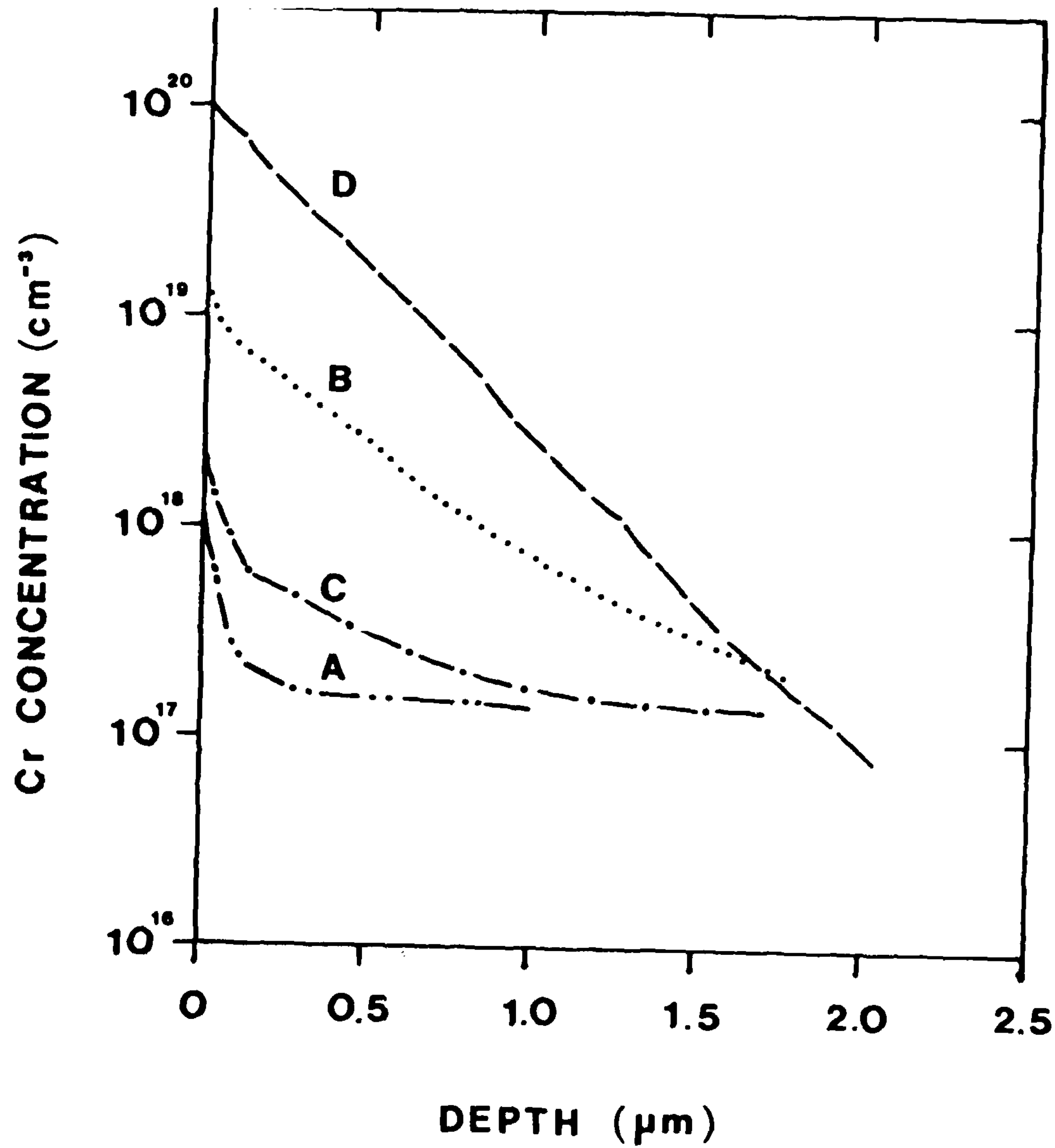


FIGURE 2. SIMS PROFILES OF BACK-SURFACE GETTERED Cr IN GaAs WAFERS; a) Control (no induced damage), Cr doped, annealed 800°C, 1 hr; b) Cr-doped, annealed 800°C, 0.5 hr; c) Cr-doped, annealed 800°C, 2.5 hr; d) Si-doped, Cr layer (front), annealed 800°C, 1 hr.

decreased. For anneal times >2.5 hours, no additional reduction in Cr concentration is observed, and SIMS profiles are essentially identical to the results obtained at 2.5 hours.

For comparative purposes, we conducted a series of experiments on carefully selected Si-doped wafers shown by SIMS profiles to contain small concentrations of Cr. Layers of Cr were then deposited on the front surfaces of both control and back-surface-damaged samples and the specimens annealed at 800°C. Evidence of near-surface Cr gettering was observed at the back surfaces of control samples. In contrast, large accumulations of Cr were observed in back-surface-damaged samples annealed for comparable periods at 800°C (Figure 2), always exceeding the concentration for control samples. In agreement with the previous results, the gettered Cr was detected within a ≈ 1.5-μm thick zone at the rear surface of the sample.

From the data obtained, we observe that the gettered Cr is positioned within a zone approximately equal to the depth of the distributed dislocation line structure at the back surface, as determined by TEM. The Cr concentration is also graded, approximately following the dislocation line gradient found in TEM measurements.[7] At short annealing times ($\leq$ 1 hr) the gettered Cr is relatively stable at the back surface, whereas for annealing periods > 1 hr, the concentration of Cr is reduced as a function of increasing anneal duration. This reverse annealing or "degettering" effect can be directly correlated with the annealing of dislocation line structure reported in reference 7. As the damage is gradually annihilated with increasing anneal time, Cr is released and allowed to move back into the interior of the wafer. After 2.5 hours of annealing, the Cr concentration is relatively stable and no further modifications in SIMS profiles are observed. For anneal periods > 2.5 hours, dislocation lines are also largely annihilated and only small concentrations of residual defects remain at the back surface.

The gettering of Cr from front surface layers is also directly related to the presence of dislocation line structure at the back side of the wafer. This anomalous diffusion of Cr may be related in part to the motion

of As vacancies released from the damaged region during annealing, or to the direct interaction between the strain field at the rear surface and Cr impurities at the front (or both). None of the experiments revealed the precipitation of Cr, in discrete zones or pinned sites along dislocation lines. The results suggest that the gettered Cr is present either in substitutional sites or in complexes not readily resolvable by TEM techniques.

To extend this study, we conducted a series of experiments in which a 2-μm CVD SiO_2 layer doped with As to a level of $\approx 10^{20}$ atoms/cm^3 was used as an encapsulant at the rear surface of the back-surface-damaged wafer. It was found by TEM that the damage thermal stability time at temperatures in the range 700°C to 830°C could be increased by a factor of two, resulting in an apparent maximum of 4 hours available processing time at 800°C. As in the earlier investigations, annealing times in excess of the thermal stability time caused pronounced damage annihilation at the back surface.

To further supplement these data, the thick SiO_2 caps were removed after annealing and SIMS profiles measured to ascertain the effect on Cr gettering. Using 30-μm particles in the rotary abrasive damage procedure, we found that Cr was rapidly gettered after 0.5 to 1 hour of annealing at 800°C. For annealing times exceeding 2.5 hours, we found pronounced de-gettering, or reverse annealing of Cr, corresponding to the point at which damage annealing is pronounced at the back surface. In comparison to the results shown in Figure 2, however, reverse annealing is considerably altered and a longer period of time present before the mobile Cr is de-gettered and allowed to diffuse back into the interior of the GaAs wafer.

3. Back-Surface Gettering and Cr Outdiffusion in VPE GaAs Layers

Semi-insulating (Cr-doped) gallium arsenide has been widely used as a substrate material for the growth of epitaxial layers in fabricating microwave FET structures. To improve the performance of such devices, a buffer layer is commonly inserted between the substrate and active layer to reduce the outdiffusion of impurities into the active layer and to isolate the effects caused by defects propagating into the film at the substrate-epitaxial layer interface.[10] Recent experiments by Tuck et al.[11] using radiotracer techniques showed that Cr diffuses readily into VPE layers during epitaxial growth at substrate temperatures in the range 745°-750°C. Their data suggested that the rapid diffusion of Cr cannot be explained by simple substitutional diffusion and an interstitial diffusion mechanism must be invoked. Separate experiments using secondary ion mass spectrometry (SIMS) and transmission electron microscopy/diffraction (TEM/TED) on Ne ion-implanted or mechanically-damaged back surfaces of GaAs wafers[8,12] have also shown rapid motion and subsequent gettering of Cr at 750°-800°C for anneal times in the range 0.5-1 hour, thereby lending additional support for a non-substitutional diffusion mechanism.

The concentration of point defects and dislocation lines at the substrate-epilayer interface will exercise an important influence on the outdiffusion of Cr and other impurities into the epitaxial layer. Improvements in the quality and microstructural defect content of epitaxial GaAs layers have been previously noted when back-surface-damaged, pre-gettered substrates were used.[13,14] However, to our knowledge, there have been no reports of the effect of (substrate) damage pre-gettering on the outdiffusion of Cr into epitaxial layers during growth. In the next sections, correlated data from TEM and SIMS measurements are presented which show the influence of substrate gettering on the interfacial defect density and distribution of Cr in VPE layers during growth and subsequent annealing.

3.1 Experimental Procedure

The semi-insulating GaAs wafers used in this study were obtained from two independent suppliers and were Cr-doped to achieve resistivities

greater than 10^7 ohm. cm. The wafers were typically oriented 3° off the (100) toward the (110) and were polished on one side.

After cleaning, the polished front surfaces were coated with 2000Å of SiO_2 deposited in a commercial pyrolitic decomposition reactor at 400^oC. The oxide film served as a scratch protection layer during back surface damage operations. A rotary abrasive unit was used to create macroscopic, concentric damage grooves ($\leq$ 30 μm) at the back surface of the wafer. After completion of the damage process, the SiO_2 layer was removed and a 1000Å thick Si_3N_4 encapsulant formed on the front surface at 200^oC by plasma deposition. Anneals were done in flowing H_2 at temperatures in the range 750°-900^oC.

Following the anneal, the Si_3N_4 film was removed and the wafers loaded into a vapor phase epitaxial reactor and heated to the deposition temperature of 720^oC. After a brief vapor etch, undoped epitaxial "buffer" layers were grown on both gettered and control wafers in the same run. The GaAs buffer layers were grown using a standard hydride (AsH_3+HCℓ +Ga) reactor typically utilized for growing epitaxial material (active/buffer) for GaAs MESFET requirements.

Following epitaxial growth, samples were prepared for TEM/TED analysis by conventional jet-thinning techniques and examined in the microscope using bright- and dark-field electron microscopy. SIMS profiling was done in a Cameca IMS-3f ion microanalyzer. To obtain maximum Cr sensitivity, O_2+ bombardment was combined with positive secondary ion mass spectrometry. The Cr concentration levels were determined using standards prepared by ion implanting Cr into both epitaxial layers and semi-insulating GaAs substrates.

3.2 Results

TEM examination of back-surface-damaged samples showed that the rotary abrasive technique produces a heavily-forested, laterally-continuous array of dislocations extending to a depth of ≃1.5 μm below the depth of damage grooves at the back surface. Fig. 3 shows a plot of the measured dislocation

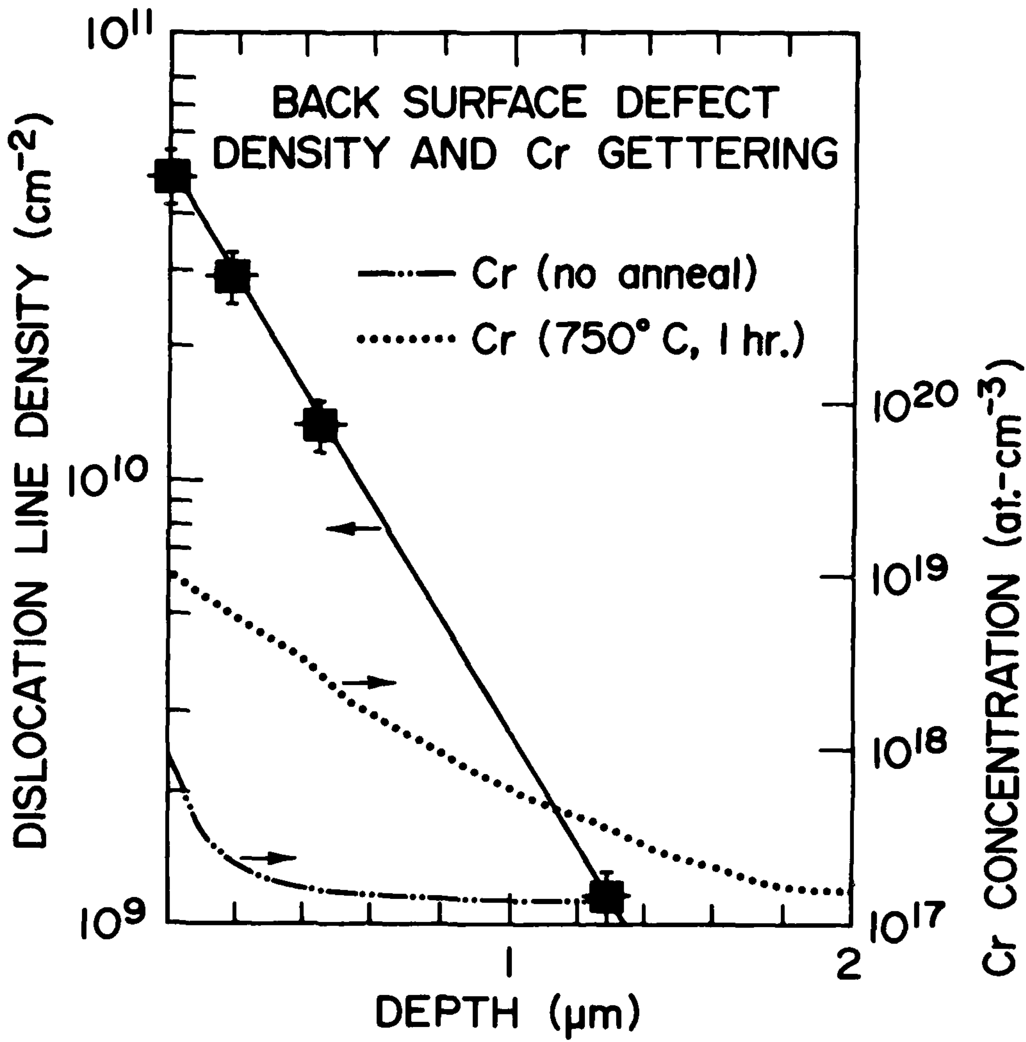


FIGURE 3. DEFECT DENSITY AND Cr CONCENTRATION PROFILES OF BACK-SURFACE DAMAGED ANNEALED GaAs SUBSTRATES.

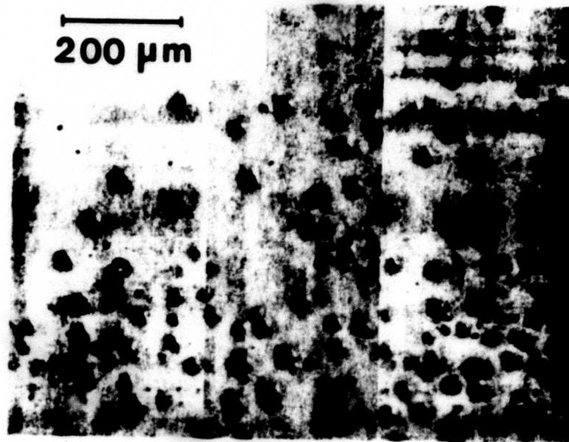
line density as a function of depth from the back surface. Also shown for reference is a SIMS profile of the Cr concentration at the back surface before and after annealing at 750°C for 1 hour. No significant dislocation line structure was observed in any sample at depths >1.5 μm. Correspondingly, the gettered Cr is concentrated within a region approximately equal to the width of the damage region. TEM examinations of the annealed samples show no evidence of precipitation along dislocation lines or in discrete segregation zones, suggesting that the Cr is present either in the form of complexes or regions not readily detectable by conventional TEM techniques.

To further investigate the effect of gettering at the front surface, we annealed for 1 hour at 750°C both control (no back-surface damage) and back-surface-damaged samples. A low-temperature (200°C) plasma-deposited Si_3N_4 layer (1000Å thick) was used as the encapsulant. The Si_3N_4 encapsulants were removed and samples immersed in a $H_2SO_4:H_2O_2:CH_3COOH(3:1:1)$ solution for 2 minutes.

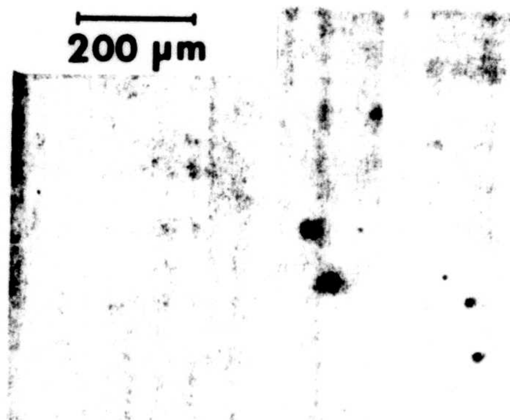
Fig. 4 shows optical micrographs of the front surfaces of annealed control (Fig. 4a) and gettered (Fig. 4b) substrates after immersion in the etch solution. The number of etch figures is considerably reduced in the gettered sample while the control samples consistently showed a density $\geq 2x10^4/cm^2$. These experiments were then repeated for a number of samples with essentially identical results.

Correlated TEM examinations of the front surfaces also showed a reduction in substrate dislocation line density after gettering. To isolate any possible capping effect, unannealed and annealed control (capped) samples, prepared under similar conditions were examined and no appreciable reduction in defect density was observed. Examination of VPE layers grown on gettered and ungettered substrates showed that the defect density in layers grown on gettered substrates was drastically reduced, essentially in agreement with the results of Schwuttke and Yang[13] on epitaxial GaAs layers grown on gettered substrates which were mechanically damaged at the back surface by impact sound stressing.

To determine the influence of gettering on Cr redistribution, SIMS



(a)



(b)

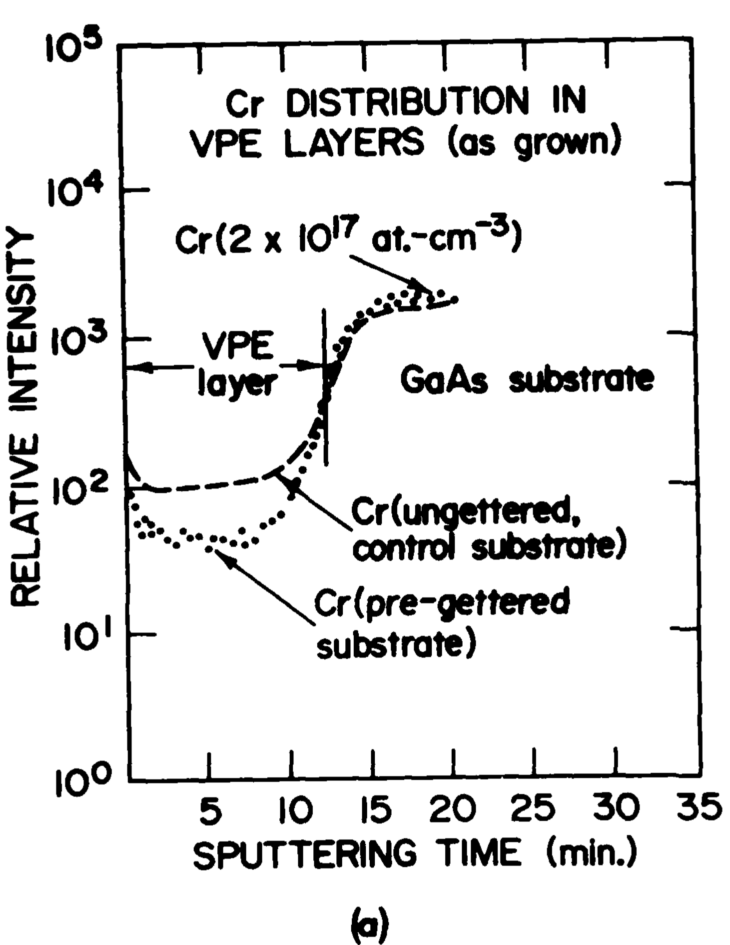
FIGURE 4. OPTICAL MICROGRAPHS OF ETCH FIGURES OF ANNEALED SAMPLES: a) Control; b) Gettered.

measurements were made to obtain Cr concentration profiles on the substrate and epitaxial layers. Fig. 5 shows SIMS profiles of the ^{52}Cr concentration in VPE layers on gettered and ungettered substrates after deposition and annealing. Fig. 5a) shows that Cr has outdiffused rapidly during deposition in layers grown on both gettered and control (ungettered) substrates. However, the level of outdiffused Cr is significantly higher for the epitaxial layer on a control substrate. In all samples examined, the level of Cr was found to be reduced in VPE layers grown on pre-gettered substrates.

Figure 5b) shows the ^{52}Cr distributions in post-deposition annealed (800°C, 30 min.) VPE layers grown on gettered and ungettered (Si_3N_4 capped) substrates. The data suggest that the total Cr content in the VPE layer grown on the ungettered substrate is considerably greater than the Cr content in the epilayer grown on the pre-gettered substrate. Comparing Figs. 5a) and 5b), it can be seen that the outdiffusion of Cr is suppressed in the pre-gettered sample whereas the Cr in the control substrate moves rapidly through the layer to the surface of the sample. The apparent near-surface pileup of Cr in both samples is thought to be a strain-induced effect caused by thermal mismatch between the encapsulant and the GaAs epilayer.[15]

Annealing at temperatures $\geq$ 850°C produces significant Cr diffusion into VPE layers with no noticeable difference between profiles obtained on control or pre-gettered samples. TEM examinations of gettered samples annealed at higher temperatures also show that the back-surface damage is progressively annihilated as a function of increasing temperature and anneal duration. It can then be speculated that the removal of back-surface damage and strain gradients caused by the presence of a graded dislocation line density (Fig.3) will correspondingly remove any apparent suppression of Cr outdiffusion from the substrate into the epitaxial layer.

From the data obtained, we can conclude that back-surface-damage gettering reduces the concentration of microstructural defects at the substrate surface and within the epitaxial layer. Since both point defects and line defects will contribute to enhanced diffusion of an impurity, the outdiffusion of Cr will be reduced during growth of VPE layers on pre-gettered



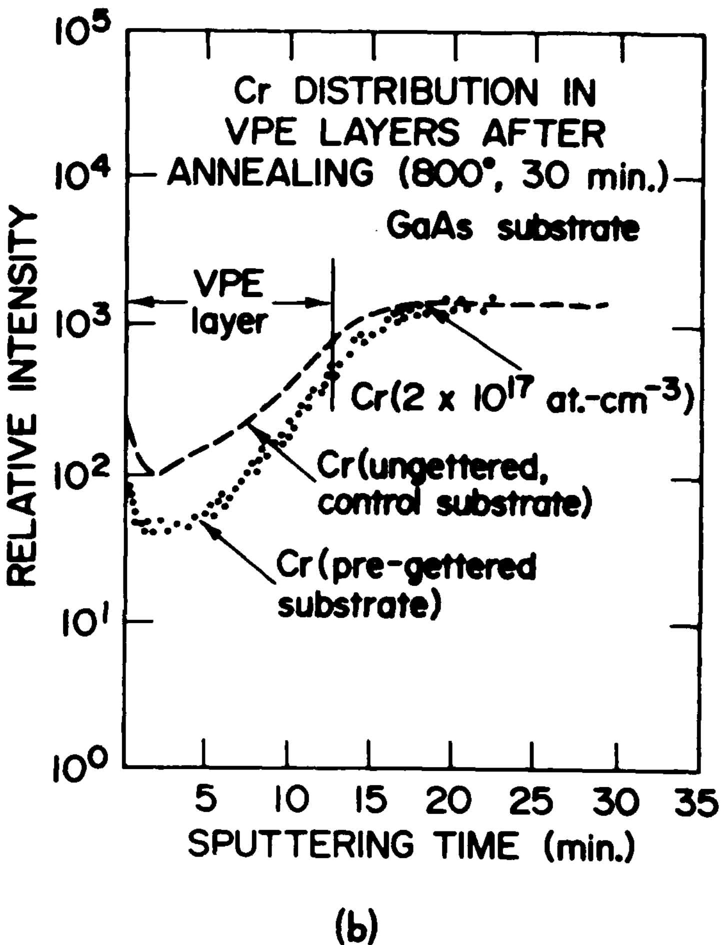


FIGURE 5. SIMS PROFILES OF Cr CONCENTRATION IN SUBSTRATES AND VPE LAYERS AFTER DEPOSITION AND ANNEALING: a) After deposition; b) 800°C post deposition anneal (t_{VPE}=1.7μm).

substrates. During post-deposition annealing, the presence of a strain field gradient produced by the dislocation line density at the back surface will partially suppress the outdiffusion of Cr and will be effective until back-surface damage is annihilated at high temperature anneals.

4. ALLOYING OF Au LAYERS AND REDISTRIBUTION OF Cr IN GaAs

The increasing utilization of GaAs as a material for fabricating microwave field effect transistors (FET), Gunn-effect diodes, and IMPATT diodes has, over the past 15 years, prompted a number of investigations on the annealing behavior of contact structures. In particular, the alloying characteristics of Au-Ge and Au-Ge-Ni structures on n-type GaAs have been widely reported,[16-24] but the problems of thermal aging and the processes which create high resistivity layers near the surface have yet to be satisfactorily resolved.[25-27] The deterioration of contact regions has in the past been ascribed to the indirect effects of strain-induced damage at the interface,[27,28] or to compensation of the Ge dopant by acceptors associated with As vacancies.[30]

Recent studies on VPE layers grown on Cr-doped (semi-insulating) GaAs substrates have shown that Cr out-diffuses readily into the epitaxial layers during deposition and annealing.[11,29] Another investigation has shown that Cr is rapidly gettered into the region of residual damage and interface of Se-implanted (capped) GaAs substrates, suggesting a possible correlation between Cr redistribution and the development of high resistivity layers at the surface after annealing.[30]

To our knowledge, there have been no reported studies of the effect of contact alloying on the redistribution of Cr at annealing temperatures in the range 350-370°C. In this section, data from transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) measurements are presented which show the development of damage structure and redistribution of Cr in n-type LPE layers and semi-insulating substrates after alloying thin Au films at 350°C for varying anneal times.

4.1 Experimental

Semi-insulating GaAs wafers used in this study were of (100) orientation and Cr doped to obtain resistivities $>10^7$ Ωcm. The LPE layers (0.5 μm thick) on semi-insulating substrates were Sn doped to levels of 1×10^{17} atoms cm^{-3}. Gold films were vapor deposited at room temperature on

precleaned samples at initial vacuum levels <10^{-8} Torr. Annealing was done at 350°C in a flowing H_2 environment. In all cases, samples were rapidly removed from the furnace after annealing and placed on a heat sink to achieve fast cooling rates.

After the removal of Au layers, specimens were prepared for TEM analysis using standard jet thinning techniques and examined in the microscope. SIMS profiling was performed with a Cameca IMS-3f ion microanalyzer. The SIMS depth profiles used O_2^+ primary ion bombardment and positive secondary ion spectroscopy. The $^{71}Ga_2^{+}$ molecular Ion (designated ^{142}Ga in the figures) was used to establish the Ga-concentration profile since the singly charged Ga^+-ion yield was too intense to measure with the electron multiplier. The Cr atomic concentration was calibrated using a $^{52}Cr^+$-ion implant into GaAs.

4.2 Results

To examine initial defect content in substrate and LPE layers, we immersed samples in a H_2SO_4:H_2O_2:CH_3COOH(3:1:1) solution for 2 min. Optical microscopy examination showed surface defect densities ≃ 2×10^4 cm^{-2} in all samples tested. After deposition of Au layers, we removed the films and again etched substrates and LPE layers. The results showed no appreciable change in defect density, indicating that no dramatic increases in defect density are produced in these experiments by Au deposition alone. Since etching experiments cannot adequately be used to reveal individual dislocation lines on alloyed surfaces, we used TEM analysis on both alloyed and control samples to obtain additional information on microstructure induced as a result of the alloying process. After Au deposition and subsequent annealing, we found a complex array of dislocations in the form of nests and tangles (Fig. 6). In contrast, we found no evidence of such arrays in control substrates or unannealed Au/GaAs structures. Annealing for periods up to 10 min. at 350°C appeared to increase the amount of damage in direct proportion to the annealing time, essentially in agreement with earlier results of Gyulai et al.[24] obtained by back scattering. Annealing of 4000Å-thick Au films for comparable periods

produced a significant increase in dislocation density, suggesting that the defect density induced by alloying is directly proportional to the initial film thickness.

Examination of samples with deposited Au films of 1000Å thickness on LPE layers also showed the same pattern of complex dislocation net works as shown in Fig. 6 after annealing at 350°C for 1 min. In like manner, additional alloying time increased the amount of damage present within the epitaxial layer.

Recent studies of Cr gettering in GaAs[12,29,30] have shown that Cr can exceed solid solubility in regions containing large amounts of crystalline damage without inducing additional microstructural damage in the lattice. From these results and earlier investigations of damage induced in GaAs as a result of Au alloying, we can conclude that the observed damage in these experiments is associated with Au diffusing into the GaAs during alloying and not correlated with any Cr redistribution.

To obtain the in-depth data on the distribution of Cr within the substrate and Au film, we used SIMS profiling. In Fig. 7 we show chemical profiles of an Au/GaAs structure after deposition of a 1000Å-thick Au layer and annealing at 350°C for periods of 1, 3, and 10 min. In Fig. 7a), we observe that after 1 min. of annealing, the Au has diffused into the GaAs substrate, accompanied by outdiffusion of both Ga and As through the Au layer to accumulate on the surface of the film. These results are in general agreement with earlier sutides using Auger electron spectroscopy profiling.[21,31,32] Of particular importance is the near-surface pileup of Cr and subsequent outdiffusion from the substrate onto the surface of the Au film. In all samples examined we observed similar pileups of Cr within the substrates near the interfacial region. For comparison we also obtained SIMS profiles on unannealed Au/GaAs structures and found no evidence of Cr interfacial pileup or outdiffusion after deposition. After 3 min. of annealing [Fig. 7b)], the concentration of Cr is reduced in the near-surface region and outdiffusion into the Au film is further increased. Ten minutes of annealing produces substantial outdiffusion of Ga [Fig. 7c)] and an apparent annihilation of the sharply defined "knee" in the Cr

FIGURE 6. TRANSMISSION ELECTRON MICROGRAPH OF GaAs UNDER (1000Å thick) Au CONTACT LAYER AFTER ANNEALING AT 350°C FOR 1 MINUTE.

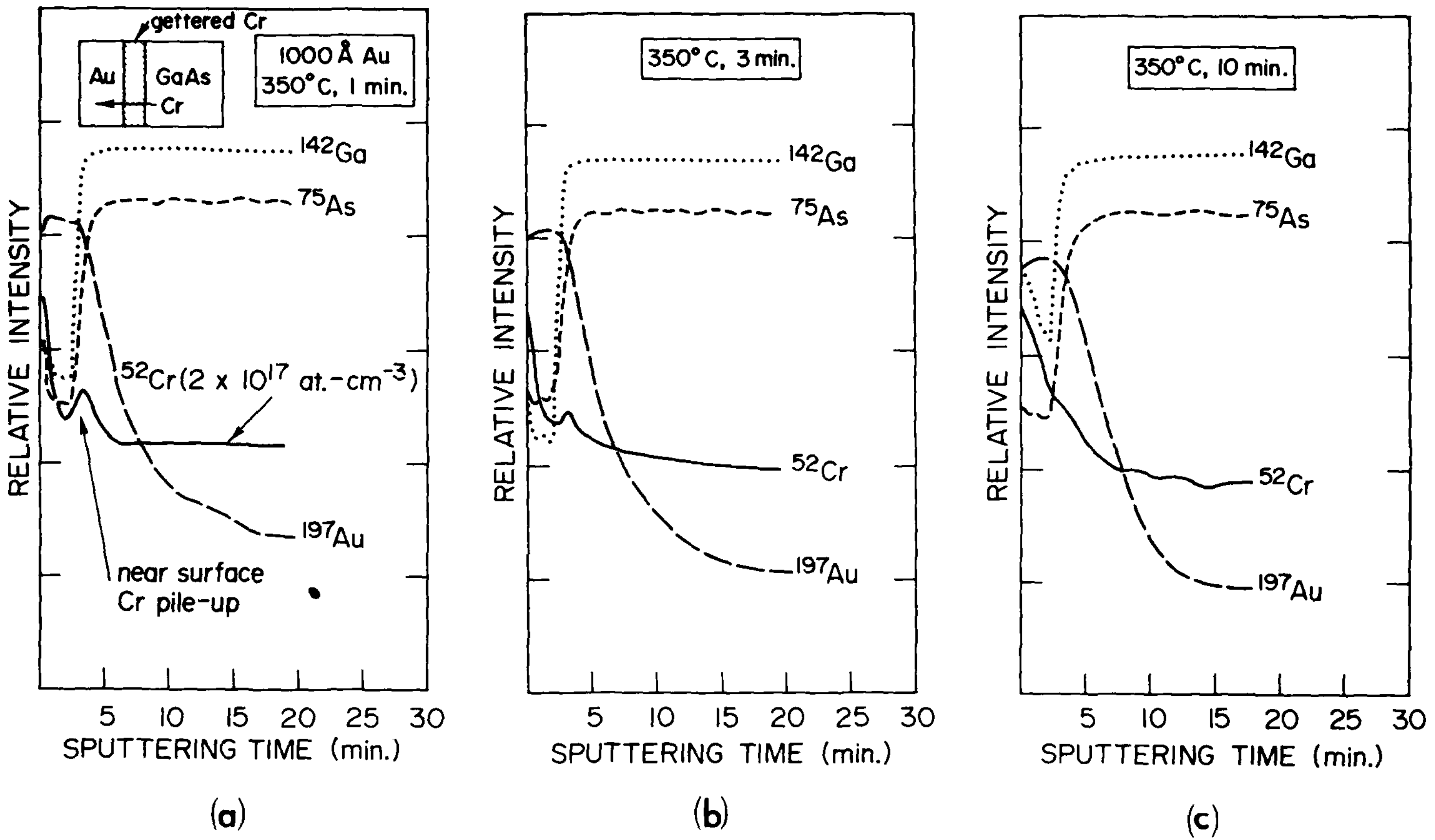


FIGURE 7. SIMS PROFILES OF (1000Å) Au/GaAs STRUCTURE AFTER ANNEALING AT 350°C; a) t_A=1 min; b) t_A=3 min; c) t_A=10 min.

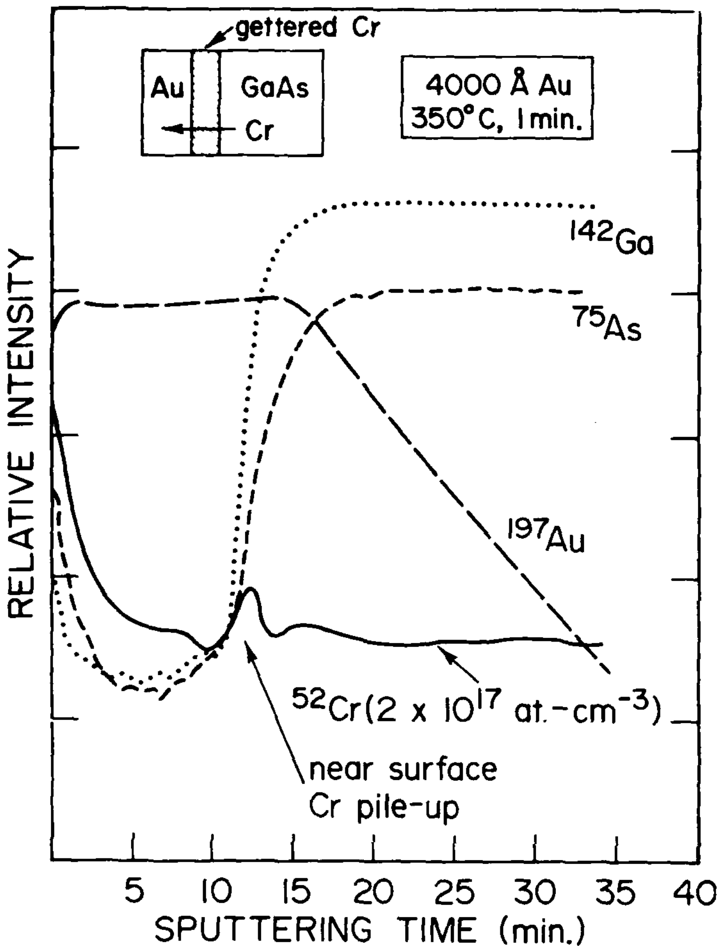
distribution profile observed in Fig. 7a).

Similar experiments conducted on Sn-doped LPE layers on semi-insulating substrates showed that Cr outdiffused readily during deposition, approaching a level of $(1-2)\times10^{16}$ atoms cm^{-3} throughout the epitaxial layer. After deposition of a 1000Å-thick Au film on the LPE layer and annealing at $350^{o}C$ for variable times, we observed essentially the same redistribution of Cr at the near surface region and within the Au film as shown in Fig. 7.

To further investigate the effect of alloying on the redistribution of Cr, we increased the thickness of Au films on semi-insulating substrates to 4000Å annealed at $350^{o}C$ for periods of 1 to 10 min. Fig. 8 shows the resulting SIMS profiles of the Au/GaAs structure after anneals of 1 to 10 min. Qualitatively, we observe a similar pattern of Cr outdiffusion and gettering within the near-surface region, producing a sharply defined "knee" in the Cr-concentration profile after a 1-min anneal [Fig. 8a)].

From the data shown, we can conclude that alloying of Au films on semi-insulating GaAs substrates or LPE layers on (semi-insulating) GaAs produces a region of damage and strain within the GaAs lattice. The concentration of damage increases as a function of initial film thickness for comparable anneal durations at $350^{o}C$. This induced damage can serve as an effective gettering region for Cr (and potentially other impurities).

In all cases, Cr outdiffuses readily into the Au layer at $350^{o}C$ and accumulates at the surface of the film. The data suggest that the degradation or aging of Au-Ge or Au-Ge-Ni contacts on n-type epitaxial layers grown on semi-insulating (Cr-doped) GaAs wafers may be related both to the generation of dislocation lines and the outdiffusion and gettering of Cr at the contact region. Additional studies are currently being done to evaluate the effect of Cr redistribution in near-surface regions on the electrical properties of contact structures.



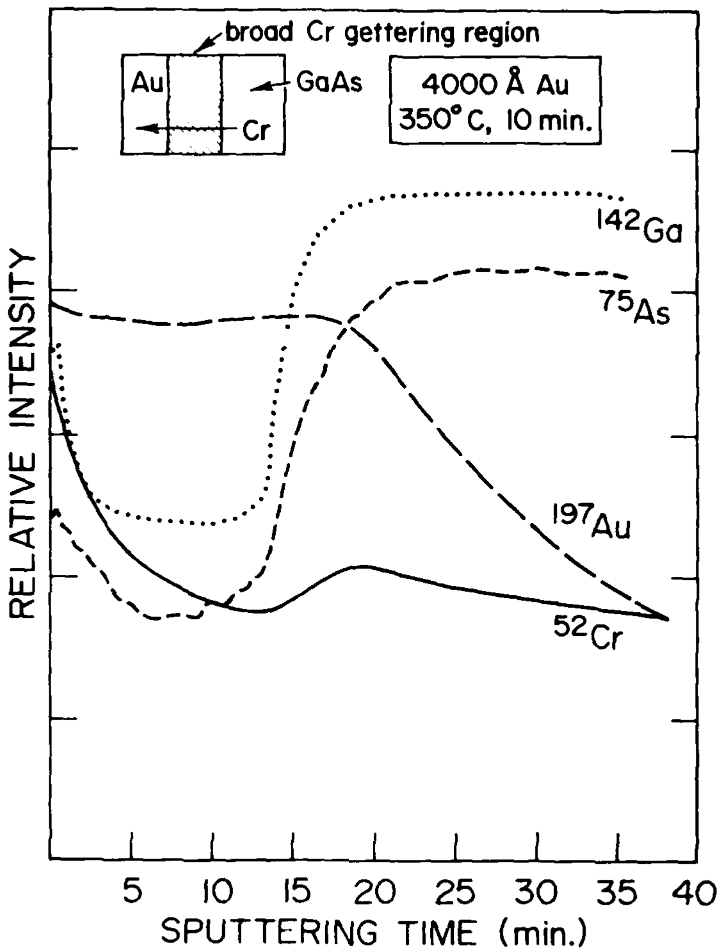


FIGURE 8. SIMS PROFILES OF (4000Å) Au/GaAs STRUCTURE AFTER ANNEALING AT 350°C; a) t_A=1 min; b) t_A=10 min.

5. PERFORMANCE OF FET STRUCTURES FABRICATED IN VPE LAYERS ON PRE-GETTERED SUBSTRATES

In the previous section, it was shown that significantly improved VPE layers are obtained when the epitaxial structures are grown on pre-gettered SI-GaAs substrates. In addition to reducing the substrate defect density at the front surface and within the interfacial region, back-surface-defect pre-gettering techniques were found to significantly reduce the outdiffusion and redistribution of Cr during deposition and subsequent annealing. To ascertain the effectiveness of these techniques for improving the yield and performance of FET devices, it was necessary to evaluate the interface mobility, capacitance and actual performance of FETs fabricated in VPE layers on pre-gettered substrates.

Samples used in this experiment were selected at random for wafer lots with no pre-screening tests performed, thereby assuring that the wafers were representative of as-received material from the supplier. One half of selected wafers was used for control specimens and the other half used for gettering in separate tests. In several sets of experiments, the entire wafer was used for gettering and VPE layer growth. Pre-gettering was accomplished using techniques described in the previous sections and earlier reports. A getter pre-anneal was done at 800°C for 30 minutes on back-surface-damaged samples with a plasma-deposited (low-oxygen-content) Si_3N_4 cap on the front surface. After annealing and removing the Si_3N_4 cap, VPE layers were grown on the substrates in a standard hydride reactor at Avantek, Inc.

Figures 9 and 10 show representative data obtained at Avantek on VPE layers grown on control (not gettered) and pre-gettered Cr-doped substrates. It is apparent that the mobility at the interface on the pre-gettered sample is significantly higher than that observed on the control sample. Tables 1 and 2 present representative comparative data obtained at 6 GHz, 12 GHz, and 18 GHz on FET devices fabricated on control and pre-gettered wafers. The data sheets shown illustrate that FETs in epi-layers on control (non-gettered) substrates. Of particular significance is the reduction (0.7 dB) in noise figure at 18 GHz.

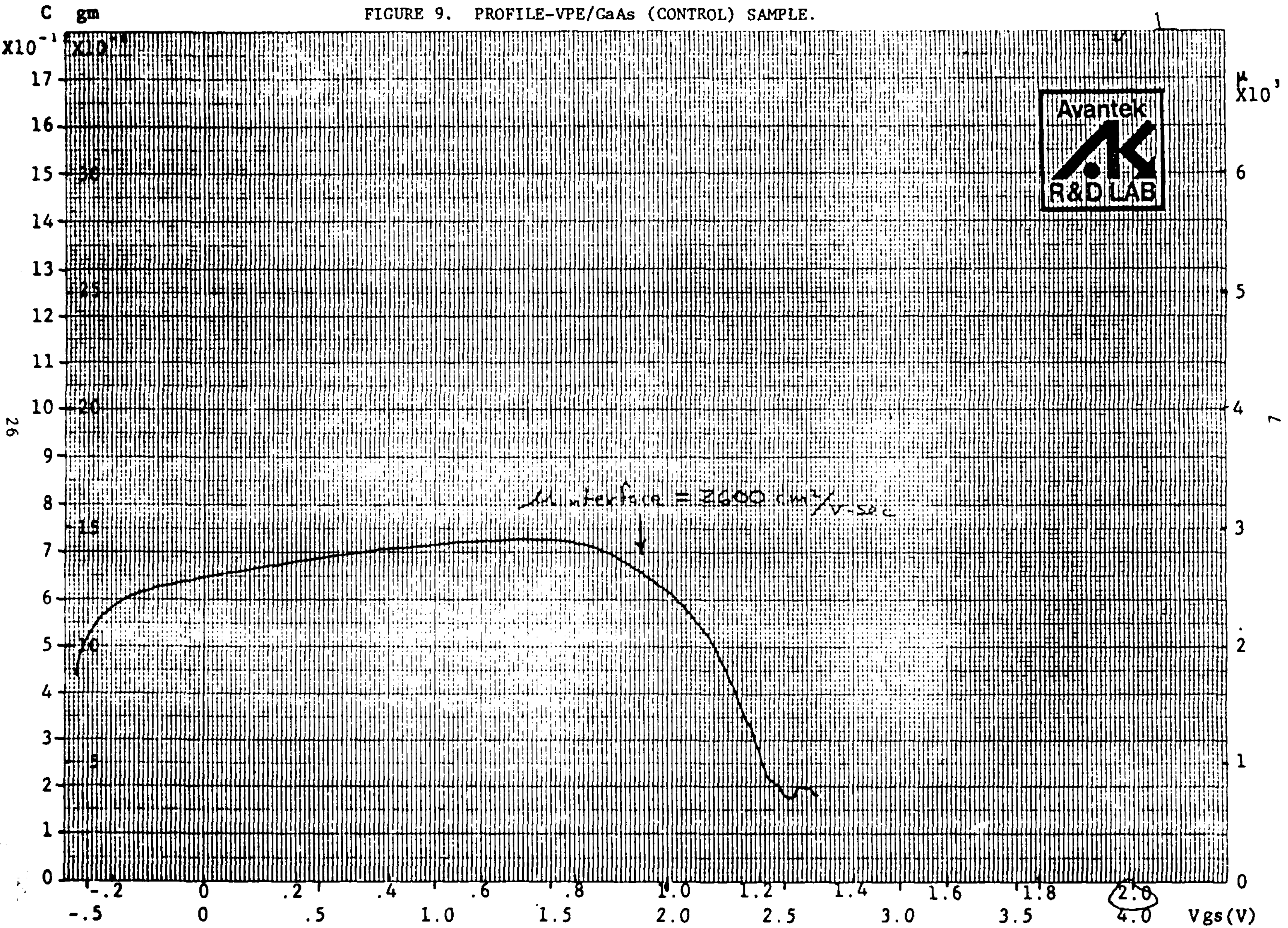
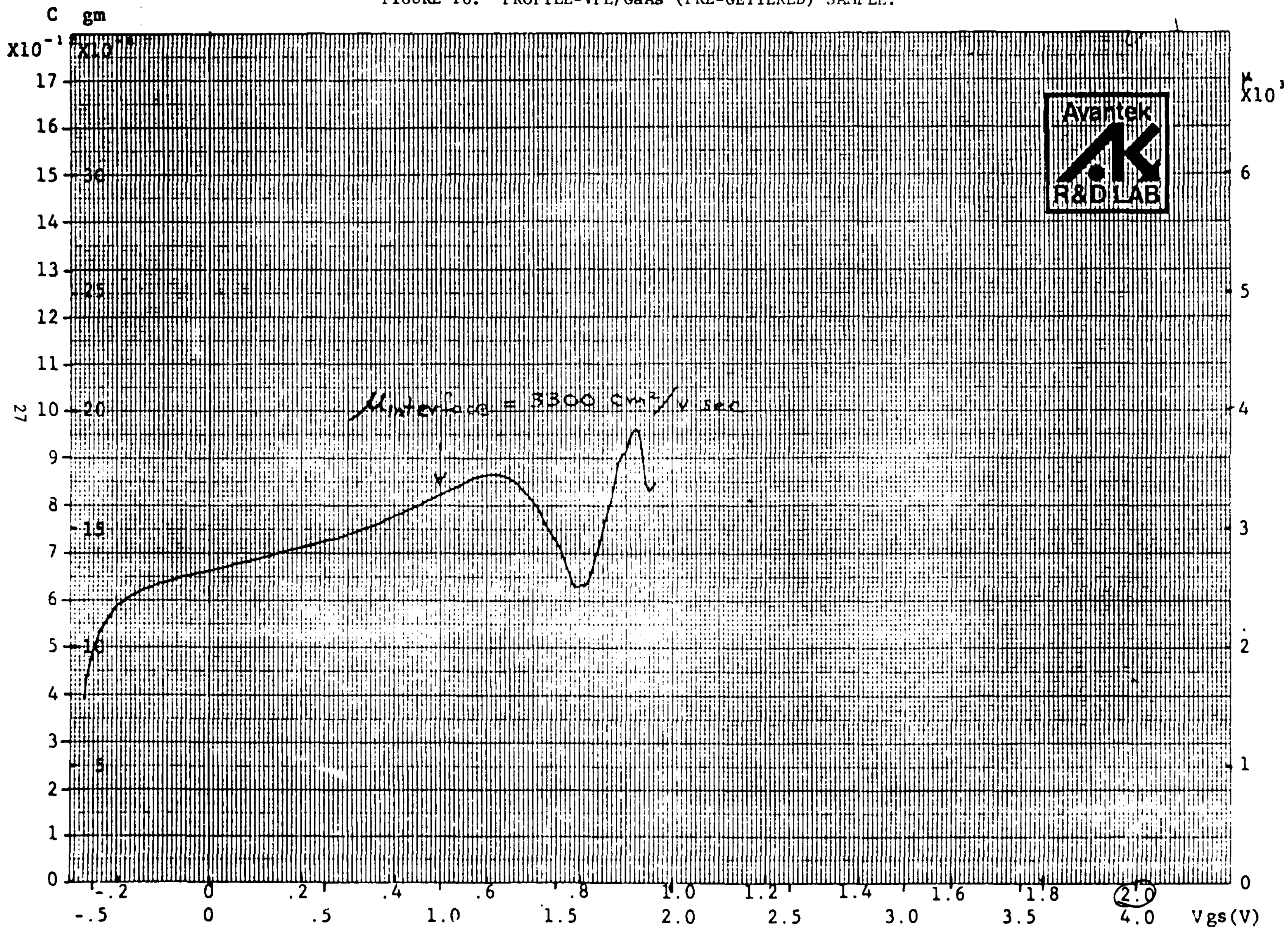


FIGURE 9. PROFILE-VPE/GaAs (CONTROL) SAMPLE.

FIGURE 10. PROFILE-VPE/GaAs (PRE-GETTERED) SAMPLE.



	Test		1	2	3	4	5	6	7	8	9	10
DC	I_{dss} at V_{ds} 3 V		45	46	31	29	30					
	R_{do}		16	16	20	21	20					
	G_{mo} at V_{ds} ____, I_{ds} ____											
	G_{mo} at V_{ds} =3V , I_{dss}		50	49	45	44	45					
	V_p at V_{ds} =3V , I_{ds} =1 mA		1.0	1.1	.78	.74	.78					
	BV_{gs} at I_{gs} =1/(10 μA)		7.2	7.5	10	11	11					
RF	6 GHz,	V_{ds}/I_{ds} (V/mA)	4/8	4/7	4/7	4/8	4/7					
	F_2= 2.65 dB,	F12 (dB)	1.7	1.6	1.65	2.0	1.75					
	DATE	GA (dB)	12.2	12.3	12.2	12.1	12.4					
	6/14/79	F_0 (dB)	1.55	1.45	1.5	1.86	1.61					
		F_∞ (dB)	1.63	1.53	1.58	1.95	1.69					
	12 GHz,	V_{ds}/I_{ds} (V/mA)	3.5/10	4.6/7	6/5	4/6	3.[illegible]/5					
	F_2= ____ dB,	F_{12} (dB)	2.8	2.65	2.8	3	3					
	DATE	GA (dB)	9.8	9.6	8.3	8.6	8.7					
	/ /	F_0 (dB)	2.31	2.11	2.09	2.37	2.31					
		F_∞ (dB)	2.51	2.31	2.37	2.65	2.66					
	18 GHz,	V_{ds}/I_{ds} (V/mA)	7.2/12.5	7.1/9	10/8	7.7/6.5	10/7					
	F_2= ____ dB,	F_{12} (dB)	4.5	3.9	4.6	4.3	4.35					
	DATE	GA (dB)	7	7.8	6.8	6.5	6.7					
	/ /	F_0 (dB)	3.21	2.68	3.28	2.74	2.90					
		F_∞ (dB)	3.74	3.56	3.85	3.29	3.44					

Table 1. Device Data - Control (Ungettered) Substrate

		Test	1	2	3	4	5	6	7	8	9	10
DC		I_{dss} at V_{ds} 3 V	34	34	34	7	7.5					
		R_{do}	21	20	21	54	54					
		G_{mo} at V_{ds} ____, I_{ds} ____										
		G_{mo} at V_{ds} =3V , I_{dss}	43	42	43	25	26					
		V_p at V_{ds} =3V , I_{ds} =1 mA	1.0	1.0	1.0	.36	.36					
		BV_{gs} at I_{gs} -1/10 μA	4.4	12	12	18	18					
RF	6 GHz, F_2= 2.65 dB, DATE 6/14/79	V_{ds}/I_{ds} (V/mA)	3/7	2.5/8	2.5/8	2/6	2/6					
		F_{12} (dB)	1.55	1.6	1.6	1.8	1.8					
		GA (dB)	12.0	12.1	12.4	12.0	11.5					
		F_0 (dB)	1.39	1.44	1.45	1.65	1.63					
		F_∞ (dB)	1.46	1.52	1.53	1.74	1.73					
	12 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds} (V/mA)	2.5/9	3/8	3/7	2.[illegible]/7	/					
		F_{12} (dB)	2.5	2.6	2.55	3.4						
		GA (dB)	10.1	9.6	9.6	8.8						
		F_0 (dB)	2.51	2.06	2.[illegible]	2.56						
		F_∞ (dB)	2.18	2.25	2.21	3.16						
	18 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds} (V/mA)	6/9	6.5/6	[illegible]/9.5	8.3/[illegible]	/					
		F_{12} (dB)	3.8	3.95	4.10	4.70						
		GA (dB)	7.7	6.3	7.3	5.45						
		F_0 (dB)	2.51	2.13	2.57	2.83						
		F_∞ (dB)	2.69	2.62	3.6	3.57						

Table 2. Device Data - Pre-gettered Substrate

The results show that pre-gettering of GaAs substrates yields the following:

- Reduction or annihilation of defects within the substrate and epitaxial layer.
- Reduction of Cr outdiffusion from the substrate during deposition and subsequent annealing.
- Higher interface mobilities.
- Lower NF at high frequencies.
- Lower input capacitance.
- Higher apparent device yields per wafer.

Tests are continuing on a number of wafers to determine the statistical improvement in device yield and performance.

6. CONCLUSIONS AND FUTURE EXPERIMENTS

In this period of the research program, we have shown that Cr is readily gettered by back-surface mechanically-induced damage at temperatures in the range 730°C to 850°C. It has been demonstrated that reverse gettering or "de-gettering" of Cr occurs after extended annealing, corresponding to the time at which dislocation structure at the rear surface of the wafer is gradually annihilated. To extend the useful annealing or gettering time, a thick 2-μm SiO_2 layer, doped with As to a level of 10^{20} atoms/cm^3,was deposited on the back surface prior to annealing to retard the annihilation of damage structure, producing an increase in the damage stability period at gettered Cr retention time.

To investigate the applicability of back-surface-damage techniques for improving the quality of epitaxial layers grown on SI-GaAs substrates, VPE layers were prepared (in a standard hydride reactor) on both control (ungettered) and pre-gettered Cr-doped substrates. It was found that the substrate and epi-substrate interfacial defect density was significantly reduced at the front surface. In addition, Cr outdiffusion from the substrate into the VPE layer was substantially reduced during deposition and subsequent annealing.

Investigations of Au contact layers on substrates and LPE layers have shown that Cr is rapidly gettered and outdiffuses during normal alloying at 350°C. It is presently thought that the low-temperature motion of Cr into alloy damage regions and Au thin film layers are responsible, in part, for the degradation of Au-Ge-Ni contacts on GaAs after low-temperature thermal aging. Additional experiments are presently being conducted to investigate the low-temperature motion of Cr in the presence of lattice damage.

Fabrication of FET device structures in VPE layers grown on pre-gettered substrates showed considerable improvements compared to devices fabricated on control substrates. It is of particular importance that no pre-screening (selection) tests were used and the improvements in device yield/wafer were noted independent of the quality of the starting substrate material when pre-gettering processes were used. Experiments are continuing to determine if the pre-gettering step can be adequately incorporated as a pre-processing procedure to produce routine improvements in GaAs device yield and performance.

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