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RESEARCH ON MICROWAVE JUNCTION GATE FIELD EFFECT TRANSISTORS.(U)
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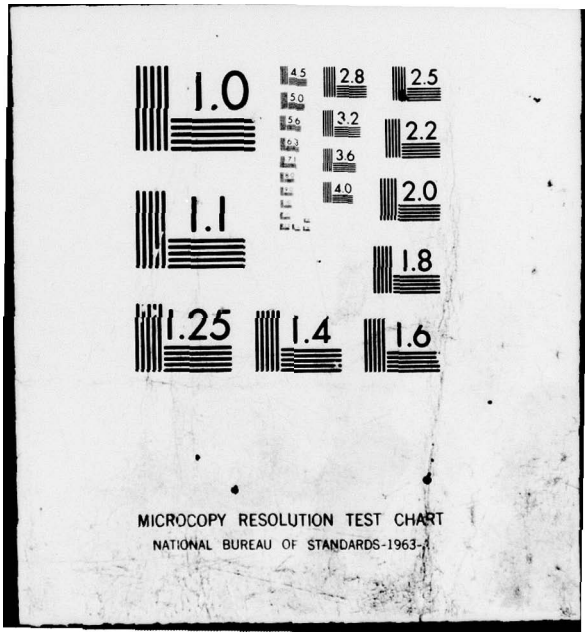
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This program has considered basic problems in the fabrication of junction-gate FET devices. We have shown that $Ga_xIn_{1-x}As$ layers can be grown of the appropriate composition ($x = 0.468 \pm 3\%$) required to obtain a good lattice match to indium phosphide substrates. Additionally, techniques have been developed for in-situ etch of substrates prior to epitaxial growth. Diffusion and masking techniques have been developed for making junctions with no enhanced lateral diffusion. These diffusions are carried out in the absence of an arsenic overpressure, and are limited to n-type layers at the present time.

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RESEARCH ON MICROWAVE JUNCTION GATE FIELD EFFECT TRANSISTORS

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19 December 1979

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ABSTRACT

This program has considered basic problems in the fabrication of junction-gate FET devices. We have shown that $Ga_xIn_{1-x}As$ layers can be grown of the appropriate composition ($x = 0.468 \pm 3\%$) required to obtain a good lattice match to indium phosphide substrates. Additionally, techniques have been developed for in-situ etch of substrates prior to epitaxial growth.

Diffusion and masking techniques have been developed for making junctions with no enhanced lateral diffusion. These diffusions are carried out in the absence of an arsenic overpressure, and are limited to n-type layers at the present time.

1. PROGRAM OBJECTIVES

The aim of this program was to identify and solve basic problems associated with the eventual development of junction gate field-effect transistors. The research program was to be directed at problems associated with the growth and transport properties of mixed compound semiconductors which can be used for the channel layer, and at obtaining an improved understanding of diffusion and masking problems associated with the formation of ohmic contacts and junctions in compound semiconductor material.

2. WORK PERFORMED ON THIS PROGRAM

Work on this program can be divided into two broad areas-materials and junction structures. Although both areas were attacked in parallel, this work will be summarized as two distinctly separate efforts. Details of these efforts have been presented in our quarterly reports, as well as in papers published during the course of this program.

2.1 Materials

We had proposed that films of $Ga_xIn_{1-x}As$ would be most suited for microwave field effect transistors, with the emphasis centered around the composition range where $x \simeq 0.47$. Additionally, it was required to develop techniques for growing extremely thin, high quality films, in

this composition range. We planned to extend our work with the use of metalorganics for this purpose, because of the potential advantages of this approach.

Our work on this program has been pursued along the following lines:

i). We have had considerable past success with substrate etching using HCl gas. Although convenient, this gas tends to be less pure than $AsCl_3$. Techniques have been developed for the use of $AsCl_3$ for substrate etching, prior to epitaxial growth. The mechanism for this etching was also determined during this study (Ref. 1)*. It was shown that the activation energies of the etching reaction and the temperatures at which the etching reaction became mass-transport limited were the same as that reported for HCl gas. GaAs substrate surfaces of both (100) and ($\bar{1}\bar{1}\bar{1}$) orientation were featureless when etched above 870°C, and were faceted with the simultaneous formation of etch pits or hillocks when etched below this temperature. Furtner, etching experiments with $AsCl_3$ and HCl gas resulted in equal etch rates for an HCl gas mole fraction which was three times that of $AsCl_3$ in the input gas stream. This indicates that $AsCl_3$ completely dissociates within the reactor before reaching the substrate. The dissociation of $AsCl_3$ produces HCl gas since chlorine is unstable in an atmosphere of hydrogen at the etching temperature.

ii). The effect of both HCl and $AsCl_3$ on the subsequent growth of GaAs films was next studied and compared. It was shown that layers of 1 μm

*All References refer to publications during the course of this program. Copies of these papers have been sent to the Army Research Office.

thickness could be grown with mobility values comparable to that obtained with thick (> 5μm) layers, grown without in-situ etching (Ref. 2). It was also demonstrated that the introduction of a halogenic component ($AsCl_3$) during layer growth results in a deterioration of the compensation ratio, which was accompanied by a fall in the electron concentration. One of the most plausible explanations for this behavior is that the $AsCl_3$ removes donor impurities faster than acceptor impurities from the source materials. The major acceptor impurity in GaAs grown from TMG and AsH_3 is carbon, whereas the major donor impurity is silicon. The change in Gibbs free energy for the reaction of these impurities with the etchant species (HCl) is negative for silicon, so that only silicon chlorides are stable at growth temperatures. Consequently, silicon is selectively removed during epitaxy in the presence of $AsCl_3$ vapor, resulting in an increase in the compensation ratio. In marked contrast, the principal impurities in the halide transport system are silicon and zinc, both of which have stable chlorides at deposition temperatures. Consequently, increasing the $AsCl_3$ concentration in halide transport systems is a highly successful technique for reducing the free electron concentration with no increase in the compensation ratio.

iii). Many layers of GaInAs were grown on GaAs substrates. It was found that, although the correct composition range was readily achieved, their electronic properties were dominated by the mismatch to the GaAs substrate. Consequently, it was decided to grow these layers on InP

substrate where a perfect match to $Ga_xIn_{1-x}As$ is obtained for $\hat{x} = 0.468$. This phase of the program was plagued with long time delays in obtaining the required substrate materials. Eventually, we obtained 1 boule of twinned n^+InP from Bell labs and 2 slices of Fe-doped InP from Naval Research Labs. We also purchased a variety of both n^+ and semi-insulating (Fe and Cr doped) material. This last material was delivered in late 1979, necessitating a six-month no cost extension to the contract. Much of our recent work has focused on polishing this substrate material (it comes in saw-cut form) and in developing a technology for handling it. This was complicated by the fact that we had a very small amount of material to work with. Nevertheless, we have developed techniques for polishing and handling this material.

iv). An important requirement for good layer growth is the ability to provide an in-situ etch for InP substrates. A technology for doing this has been worked out by us. Here, HCl gas is used as the etchant, both with a PH_3 overpressure as well as in its absence. (The motivation for etching without PH_3 is to keep from growing an unintentional quaternary [GaInAsP] layer at the interface). Both approaches give satisfactory morphology of the substrate, as well as of the subsequent epitaxial layer. The results for in-situ etch are relatively complete; a paper on this topic is in preparation and will be submitted to the Electrochemical Society Journal.

v). Only recently, we have grown $Ga_xIn_{1-x}As$ of the required composition on this substrate material. This is evidenced by the fact that these

layers are seen to have cross-hatch striations, of the type obtained when growth is on GaAs substrates. Additionally, the carrier concentration in these films is about a factor of 10 less than that for films grown at the same time on adjacent GaAs substrates.

Our first films, grown by this technique, had a carrier concentration of $10^{16}/cm^3$ and a mobility of 3780 $cm^2/V\text{-sec}$. Much work needs to be done to adjust growth parameters (arsine and phosphine overpressures and metalorganic flow rates) to obtain films in the $10^{15}/cm^3$ concentration range. We are continuing this effort because of our recent progress, and plan to seek support for this work.

2.2 Junction Structures

Our work in the area of junction studies has covered the gamut from curved junction breakdown theory and the development of doped oxide sources, to the achievement of planar junctions. All of the experimental work was done with GaAs substrates because of its ready availability. However, it should be capable of extension to GaInAs layers, as required.

i). A theory was developed for the breakdown voltage of both cylindrical and spherical junctions. This theory is applicable to breakdown in the curved region around a window in an oxide, and is considerably simpler than previous approaches. Such oxides, suitable for masks in GaAs diffusions, have been developed on earlier programs.

ii). A doped oxide, consisting of $SnO_2 \cdot SiO_2$, was developed for making n-type diffusions. Although p-type diffusions are required for the junction

gate, it was decided to begin our studies with n-type junctions because of our previous work with the growth of SnO_2 layers. Furthermore, these junctions can be used for ohmic contacting to the source and drain regions. In previous studies, these oxides have been prepared by mixing ethyl orthosilicate with tetramethyltin, and using this as a source for pyrolysis. A major drawback of this technique is that the vapor pressures of the two liquid constituents in the bubbler are not equal. This results in large changes in the composition of the mixture with use; data in the published literature show large variations in the diffusion depth under identical oxide deposition conditions and with the same diffusion cycle. To overcome this problem, a new oxide deposition technique was investigated by us. Here, the tin-doped silicon dioxide layers were obtained by the simultaneous oxidation of *tetramethyltin* (TMT) and silane gas. Planar diffusions were achieved (Ref. 3) in the total absence of an arsenic overpressure. This was accomplished by using phosphosilicate glass films as diffusion masks. The planar diffusions were performed by first depositing the phosphosilicate glass film on the gallium arsenide substrate at 400°C using the simultaneous oxidation of silane and phosphine. After deposition, these films were patterned using conventional photolithography. A layer of tin-doped oxide was then deposited to complete the structure. The diffusions were performed at 1000°C for 1 hour, using a 3000 Å thick tin-doped oxide layer with a mask of 3000 Å in thickness.

iii). An anomalous effect was observed (Ref. 4) when deep diffusions were made by this technique. These were ascribed to dopant depletion

which can occur if the doped oxide layer is thin and the diffusion time is large. However, these effects are of little importance in microwave FET fabrication technology.

iv). Arsenic doped SnO_2 layers were also grown during the course of this program (Ref. 5). The aim here was to incorporate the more volatile component of GaAs into the dopant source, and so result in improved diffusions without loss of this element from the GaAs. This was accomplished by the simultaneous pyrolysis of tetramethyltin and arsine gas in oxygen, at a temperature of 450°C.

v). An experimental setup was developed for measurement of the velocity vs electric field characteristics of the grown material. The effectiveness of this method was verified with samples of GaAs grown in our system. A technique for measuring the energy gap of the GaInAs layer (water diode) was used for verifying its composition.

3. PUBLICATIONS

In addition to two talks, the following papers have been prepared, based on work carried out during the course of this program.

1. R. Bhat and S. K. Ghandhi, "Vapor-Phase Etching and Polishing of GaAs Using Arsenic Trichloride", Jour. Electrochem Soc., v. 124, No. 9, p. 1447 (1977).

2. R. Bhat and S. K. Ghandhi, "The Effect of Chloride Etching on GaAs Epitaxy Using TMG and AsH_3", Jour. Electrochem Soc., v. 125, No. 5, p. 771 (1978).

3. B. J. Baliga and S. K. Ghandhi, "Planar Diffusion in Gallium Arsenide from Tin-Doped Oxides", Jour. Electrochem Soc., v. 126, No. 1, (1979).

4. B. J. Baliga, R. Bhat and S. K. Ghandhi, "Anomalous Diffusion From Doped Oxides Due to Dopant Depletion Effects", Solid State Electronics, v. 20, p. 773 (1977).

5. Y. S. Hsu and S. K. Ghandhi, " The Preparation and Properties of Arsenic-Doped Tin Oxide Films", Jour. Electrochem Soc., v. 126, No. 8 (1979).

6. S. Whiteley and S. K. Ghandhi, The Vapor Phase Etching of Indium Phosphide Substrates", in preparation.

A paper on the growth of GaInAs using the metalorganic technique is also planned for such time when the work is complete. Acknowledgment of Army Research Office support will certainly be made in this paper.

4. EDUCATIONAL AND PROFESSIONAL

The educational content of a program is an important one for an academic institution such as ours, whose end goal is to train students in disciplines of importance to the national interest. This program has provided partial support to a number of such students as they worked towards their respective academic goals. These include the following doctoral candidates:

1. R. Bhat
2. Y-S. Hsu
3. S. Whiteley

Of the above, S. Whiteley has been fully supported on this program, and will earn his PhD. in the near future. His thesis will be on the Growth and Characterization of GaInAs Films; a copy will be submitted to the Army Research Office upon completion. R. Bhat was partially supported on this program, earned his PhD., and is currently at Bell Labs. Dr. Y-S. Hsu, who received incidental support only, is currently employed at the General Electric Co.

A number of undergraduates have also worked in an unpaid capacity on this program, as part of their project activities. These students have obtained training in support areas, including the development of electronic measurement techniques, and in the use of device fabrication techniques such as mask making, photolithography, oxide deposition and diffusion.

5. Conclusion

This program has considered basic problems in the fabrication of junction gate FET devices. A number of problem areas have been delineated; some have been solved, yet others have reached a point where solutions are in sight. Our conclusions, based on this work, are as follows:

i). GaInAs is a very promising material for microwave FET devices, and should have a factor of 3 speed advantage to GaAs, assuming comparable technologies.

ii). GaInAs must be grown on a lattice matched substrate in order to achieve this potential. Indium Phosphide is suited for this purpose. However, industry efforts must be stepped up to make this material more readily available, and more defect free. At the present time, we are paying $200.00 per gram for material of dubious quality, and waiting over 6 months for its delivery. We strongly urge DOD funding in support of the production development of this important semiconductor substrate material.

iii). The metalorganic process is ideally suited for the growth of active layers of GaInAs for FET devices, because of the ease of growing thin (< 1μm) layers with excellent morphology. This is extremely difficult with liquid phase epitaxy, where layers are plagued with striations and other growth instabilities.

iv). We have shown that planar n-type junctions can be made in GaAs using open tube diffusions. In our opinion, the p-type diffusions can also be made, using a zinc-doped oxide source. Nevertheless, we are negative about using a high temperature diffusion process to make these junctions. This is because, although we have been able to reduce the massive lateral diffusion effects that ordinarily occur, the process is based on the careful adjustment of interfacial stresses, and will most probably not be practical in a manufacturing environment. We are optimistic, however, about the possibility of forming this junction by a laser-induced process with little or no lateral diffusion effect. We plan to extend our work along these lines in future programs in this important technical area.