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SOLID STATE POWER CONTROLLER VERIFICATION STUDIES, FINAL TECHNICAL REPORT

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FINAL REPORT
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This report documents the design and test of the Solid State Power Controllers (SSPCs) for the B-1 aircraft, ~~by Rockwell International~~. The SSPCs were in qualification testing when the B-1 program was terminated. The testing and completion of the B-1 SSPC program, considered crucial to the advancement of the state-of-the-art in SSPC technology, is concluded and documented in this report. This report documents the accomplishments of the B-1 SSPC program together with the results of the tests completed during the study. Recommendations for future SSPC activities are included in the final section. A proposed MIL-P-81653 specification is attached as Appendix A.

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FOREWORD

This document is the final technical report for the Solid State Power Controller Verification Study. The work was performed by Autonetics Strategic Systems Division of Rockwell International Corporation, Anaheim, California under Air Force Contract No. F33615-78-C-2065.

The work was administered under the direction of the Power Systems Branch (POP), Aerospace Power Division (PO), Air Force Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, by Mr Paul R. Bertheaud (POP-2), Technical Area Manager.

C. E. Young of Rockwell International Corporation was technically responsible. The report was prepared by C. O. Linder with significant contributions by J. K. Brownrigg, P. E. McCollum, W. A. McFall, and G. L. Schmitt.

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SECTION I
SUMMARY

This report documents the B-1 Solid State Power Control (SSPC) development performed by the Strategic Systems Division of Rockwell International. This B-1 activity was the most comprehensive effort to date in SSPC development. Covered within this report are aspects, e.g., safety, nuclear transient radiation, maintainability, etc., that heretofore were not explored. This report also includes: (1) completion of SSPC testing over the temperature range, (2) conduction of selected performance tests, and (3) documentation of B-1 SSPC program accomplishments.

The scope of this report encompasses: (1) Trade-off Studies, (2) SSPC Design, (3) Hybrid Design Considerations, (4) SSPC Assembly Design, (5) Test Results, and (6) Conclusions and Recommendations for advancing and expanding SSPC applicability.

The decision to use SSPCs on the B-1 Aircraft was based on participation and evaluation of SSPC evolution from conception to implementation. The evaluation included numerous trade studies to evaluate risk, size, weight, power, etc. A chronological history of pertinent events is contained in Section III. In addition to documenting the preimplementation studies, Section III contains a retrospect comparison of the Solid State Power Control Assembly (SSPCA) with a hypothetical Electromechanical Power Controller Assembly. Results of the comparison showed that the solid state approach retains a cost advantage, with a potential for further cost economics. The B-1 Power Controllers (PCs) were a "conversion" from mechanical to solid state and consequently suffered penalties due to "unchangeable" constraints, e.g., maintaining the Electrical Multiplexing (EMUX)-Power Controller Assembly (PCA) interface. New systems will not contain these constraints, and a merger toward total power management systems will eventually occur.

The SSPC design was preceeded by trade studies relating to "package" size and "convertible" controllers, i.e., functions that could use solid state (less than 2 A) controllers. Approximately one-half of the power controller applications were convertible with a conversion ratio of approximately 1.5

SSPC to 1 Electro-Mechanical Power Controller (EMPC). The SSPCs were housed in 13 identical assemblies, each capable of holding 60 SSPCs. A common design for the assemblies had a significant life cycle cost advantage over the multiple designs required for the EMPCAs.

The approach taken in the design of the SSPCs was a plug-in printed circuit card containing four SSPC circuits. This circuit card was designated the AC Switch module. Trade studies indicated that the plug-in PC technique provided the best utilization of volume available and was the easiest (most economical) to maintain. The majority of components for an SSPC circuit are contained in two hybrids termed the Control Hybrid and the Power Hybrid. Transformer technology is used to achieve coupling and ground isolation. Each of the four SSPCs on the AC Switch module are completely and functionally independent, except for the primary of the power transformer.

The Control Hybrid provides the isolated interface with EMUX, the secondary power supply for an SSPC, and the logic necessary to generate the control and timed trip-out functions. A significant advancement in SSPC technology was the mechanization of the Control and Time-Trip logic. It is contained on a single Monolithic Complementary Metal Oxide Semiconductor (CMOS)/ Silicon-on-Sapphire (SOS) Large Scale Integrated (LSI) device offering significant potential for cost efficiencies in volume usage of SSPCs. The control logic is such that the SSPC can be configured as normally on or normally off - a first in SSPC application.

The Power Hybrid contains back-to-back Silicon Controlled Rectifiers (SCRs) and associated drive circuitry. The SCRs are matched and tested to the B-1 environment with a special emphasis on radiation requirements. The Power Hybrid also contains a bridge rectifier circuit to accommodate the B-1 dc loads.

In addition to the Control and Power Hybrids, the B-1 SSPCA contains a module of "Logic Hybrids" and one of "Status Hybrids". The application of power control to advanced aircraft, like the B-1, is more than the application and removal of power and provision of "protect" functions. Power is applied or removed in many instances, e.g., the trim control (based on pilot inputs),

the direction the control surface is to move, and the position (limit) of control, as well as redundant control for certain flight safety functions. In the B-1, EMPCs use relay logic; in the SSPCA these applications were mechanized using the "Logic Hybrid", which provided AND-OR functions compatible with the SSPC control input.

Another function used in power control is event statusing, e.g., landing gear interlocks, used in application or removal of power for raising or lowering landing gear. In the SSPCA these signals were isolated and interfaced with EMUX using the "Status Hybrid".

Test results prove the feasibility of SSPCs. At the time of B-1 termination, qualification testing of the prototype SSPCs and SSPCA had been started. However, SSPCA testing had progressed sufficiently to have completed Dielectric Withstanding Voltage (DWV) tests and identified problems that can be anticipated in high voltage/altitude environments. Temperature testing of the SSPC was completed as part of this study.

In conclusion, the B-1 activities significantly advanced the state-of-the-art in power control, especially solid state, as well as showing where additional study and development could be beneficial to both application ease and cost economies. The recommended follow-on activities include:

1) Expanding the range of SSPC capability beyond 2 A.
2) Integrating power controllers and data bus (MIL-STD-1553 Type) into "smart" remote load management centers.
3) Analysis of load management functions with a goal of simplifying the control function(s).

SECTION II
INTRODUCTION

2.1 Background

This study was undertaken as a result of the growing need for the application of SSPCs on future aircraft.

Efforts by the Air Force resulted in the development of SSPCs for the B-1 flight test which paved the way for SSPC implementation on the B-1 production aircraft. Rockwell International performed the work on the SSPC implementation for the B-1, but the work was incomplete at the time of B-1 program termination.

Continuation and completion of the B-1 SSPC program was considered crucial to the advancement of the SSPC state-of-the-art technology. The SSPC work for the B-1 was the most comprehensive effort ever done in the SSPC area and included certain aspects of SSPCs which were never before studied in great detail, e.g., system safety, maintainability, explosive atmosphere requirements, packaging trade-offs, and life cycle cost trade-offs.

2.2 Objective

The objective of the effort was to complete the qualification tests of the SSPC modules and to document the results of the tests and the information accumulated during the development phase.

2.3 Approach

The approach taken was to complete the test effort using material and equipment from the B-1 SSPCA Termination Inventory. The program length was six months and included delivery of two operational and tested AC Switch Modules to the Air Force Air Propulsion Laboratory (AFAPL) along with a final report documenting in detail the B-1 SSPC effort.

SECTION III
POWER CONTROLLER TRADE-OFF STUDIES

3.1 Background

The B-1 aircraft significantly advanced the state-of-the-art of power control and distribution systems. It was the first multiplexed electrical control system (EMUX). EMUX provided automatic load management capability and eliminated 57 miles of control wires. EMUX provided the control to and monitored the status of power controllers which distributed the power throughout the aircraft. In the early B-1 aircraft, a basic PC consisted of a relay, a thermal circuit breaker, and a relay driver (EMUX interface). Thus, in addition to remote control, the PCs provided overcurrent (circuit breaker) protection. The PC elements were used in various mixes of breakers, relays (2 and 4 pole), and drivers to provide control and monitor capability e.g. trim tab, landing gear control, etc.

Aircraft No. 4 contains approximately 1000 circuit breakers. These PCs were housed in 25 enclosures called Power Controller Assemblies (PCAs) located in various equipment bays throughout the aircraft. Each PCA was unique, and was treated as part of the aircraft structure rather than an electronic assembly. The maintenance philosophy was to replace PC elements at the flight line.

Solid State Power Control activities started in 1969 with the circulation of the Power Controller specification, MIL-P-81653. The potential advantages of SSPCs vs EMPCs and the quantity of PCs anticipated for B-1 made B-1 a prime application of SSPCs.

The first EMPC vs SSPC study was performed in 1971. This study concluded that SSPC state-of-the-art was not sufficiently advanced for B-1 use. The main objections were in the areas of leakage current, radiation hardening, weight, volume, and current interrupt capability.

In January 1972, AFAPL contracted with Westinghouse to develop 1 and 1.6 A. SSPCs, with Rockwell International slated to evalute the units. In April 1972, Telephonics submitted 0.5 A SSPCs for B-1 evaluation and the evaluation of these SSPCs was added to the program. In 1972, industry opinions regarding SSPCs were again solicited in an attempt to define requirements for 0.5 A to 35 A. devices. An evaluation of SSPC status concluded that qualified SSPCs would not be available for the first flight of the B-1 Aircraft No. 3. The first prototype SSPCs were developed by Westinghouse and Telephonics circa December 1972 to February 1973. In December 1974, the first draft of a B-1 SSPC specification, L450C2052, was generated.

This procurement specification offered an option in SSPC packaging. The Type 1 contained plug-in "can" units and Type 2 contained module units with three SSPCs per module. This document closely followed requirements of MIL-P-81653 with added B-1 requirements.

In 1974, B-1 Production Cost Acquisition Studies were sponsored by AF B1 SPO. The objective of these studies was to evaluate techniques for reducing the cost of B-1 production aircraft. EMUX, PCAs and SSPCs were subjected to in-depth studies.

Of major impact to SSPC advancement was the SSPC Implementation Study, NA 74-887, Control Study 309-118. This report is attached as Appendix B. This study proposed using SSPCs and EMPCs in mixed or hybrid packaging configurations and presented Westinghouse and Telephonics units as examples. It proposed 50 percent replacement of EMPCs with SSPCs for implementation on Aircraft No. 4. A go-ahead of 1 June 1975 was proposed, with delivery 1 April 1977, based on a 33 month program. Weight reduction due to SSPC changes was 77 pounds. Total weight savings anticipated was 211 pounds due to volume reduction, packaging methods, wiring reduction, and tray changes permitted when using SSPC units.

In November 1975, SSPCs were ready for flight test. However, flight tests for the SSPC circuitry in B-1 Aircraft No. 1 were never achieved because of the magnitude of effort and impact on aircraft schedules. The effort was modified to include in-house bench tests and extended to include Autonetics

new breadboard units. Tests conducted included compatibility, basic operation requirements for the B-1, and endurance. The new 0.3 A. Autonetics breadboard unit was also tested for rupture requirements. All tests were successful. The SSPC procurement specification was completed and SSPC suppliers were notified of the changes to the module packaging technique and all expressed a continued interest.

In December 1975, Contract Change Proposal 328 was initiated to perform long-lead item studies of SSPC options to replace EMPCs $\leq$ 2 A. The seven options studied were:

1) EMPCA, "Line" Maintenance, SSPCA, No line maintenance; SSPC to be plug-in card. EMPCA and SSPCA would be separate Line Replaceable Units (LRUs). (Defined as segregated configuration).
2) Same as Option 1 except SSPCA would be line maintenance with ruggedized SSPC for removal at flight line.
3) Combine EMPC and SSPC into same LRUs as mixed configuration, no flight line maintenance. SSPC would be plug-in module card.
4) Same as Option 3 except use ruggedized SSPC module cards for flight line removal of SSPC or EMPC components.
5) Same as Option 4 except no flight line maintenance for SSPC portion of LRU but EMPCA components would be replaced at the flight line.
6) Same configuration as Option 3 (mixed) except use SSPC canned units of Westinghouse or Telephonics type.
7) Same configuration as Option 4 with flight line maintenance for canned SSPC units and EMPCA components.

Each option was assessed for weight, volume, reliability, development cost, production unit cost, maintenance, support cost and life cycle costs. These studies presented an in-depth review of actual Aircraft No. 3 circuits $\leq$ 2 A to determine what quantity of SSPCs would be required in each aircraft location. Also, it became apparent that a one-to-one replacement of SSPC for EMPC was not a reality in that there were 35 different configurations of circuit breakers, relays, and driver combinations in the aircraft. For

example: normally open, normally closed, 3 Ø, 3 Ø reversing, dc, status, parallel, series, series - parallel, logic, dual output isolation and various circuits sharing the same circuit breaker. This led to the necessity for adding Logic, Status, and Diode Bridge module boards to the SSPCA.

Option 2) was selected as best from weight, volume, and cost considerations. This was a segregated LRU configuration and required approximately 11,000 aircraft wiring changes.

During the study, three SSPCs per 5 in. x 6 in. circuit board were determined to be most effective from weight, volume, and cost considerations with the LRU determined to be 1/2 ATR size. Later finalization of circuit counts showed that four SSPC circuits per board were necesary to minimize LRU types and meet circuit requirements in all areas. To maximize weight, volume, and cost savings, the final configuration selected was three SSPCA (LRU) types with plug-in module cards 5.65 x 6.25 with 3/4 inch centers and four circuits per SSPC card. Each SSPCA would also contain a Logic, Status, and Diode Bridge card.

During the study, Westinghouse Electric, Telephonics, and Rockwell International were presented with the latest developments and requested to provide circuit schematics, board layouts, part count, component identification, circuit detail description (technical), schedules, production unit cost, development costs, and historical background in solid state programs. Each of the designs was assessed from a technical standpoint to assess risk. This risk also became part of the overall schedule to provide for circuit interations in development or test as required.

Rockwell International presented a briefing of the above study and conclusions to the Air Force at Wright Patterson Air Force Base. Conclusions presented were:

1) The canned approach is more costly.
2) The PCB approach is less costly.
3) LRU Removal at flight line (SSPCA) is best weight savings (217 lb).

Based on the best combination of cost, weight, and volume, the recommendations were:

1) Rockwell make SSPC Module available for Aircraft No. 5.
2) Competitive make SSPC module available for Aircraft No. 8.

Autonetics was awarded a contract to provide the SSPCs in July 1976 for implementation on Aircraft No. 5.

One of the early results of this contract was a standard PCA type that could be used in all SSPCA locations in place of the three SSPCA types originally proposed. This unit is described in this report.

The preceding summarized the precontract trade studies leading to SSPC implementation. In the following paragraphs, a retrospect comparison of SSPCs and EMPCs is made to aid in future assessment of SSPC implementations.

3.2 Objective and Approach

The objective of this section is to compare Rockwell International's 0 to 2 A SSPCs developed for implementation on Aircraft No. 5 with EMPCs used in Aircraft No. 1 through 4. The comparison presented is as follows:

1) A description of Power Controller requirements
2) A description of EMPCs and SSPCs
3) A comparison of aircraft usage of 2 A PCs, (EMPCs versus SSPCs)
4) A description of EMPC and SSPC circuit characteristics
5) A comparison of EMPC versus SSPC
6) A description of EMPCAs and SSPCAs
7) A comparison of EMPCAs versus SSPCAs

3.3 B-1 Aircraft PC Requirements (2 A Only)

There are approximately 900 circuits requiring control of current in the 0 to 2 A range on the B-1 Aircraft. The general requirements are listed below:

1) Bus voltage: 230 V, 400 Hz
2) Load current: 0 to 2 A 400 Hz; 0 to 200 mA dc
3) Controller voltage drop: 2.2 V maximum
4) PC Trip for load over-current (>2 A) condition
5) Trip condition indicated by a closed switch ($V \leq 1$ V at 10 mA)
6) Status of PC (open/closed) indicated by an open/closed switch ($V \leq 1$ V at 10 mA)
7) PC controlled by 10 mA, 0 to 5 V dc signal
8) Operating temperature range: -55 to 75°C
9) Operational environment: Manned aircraft
10) Other critical parameters: Reliability, weight, and volume

3.4 Electro-Mechanical Power Controllers

A block diagram of an EMPC is shown in Figure 1.

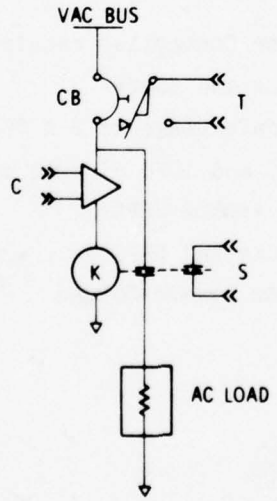

Figure 1. EMPC Block Diagram

The design features of this electromechanical design are

1) Manual resettable circuit breakers that indicate a Trip for load currents greater than, in this case, 2 A. The maximum voltage drop of a Type 1 circuit breaker is 1.4 V.
2) An electronic driver that controls the voltage (230 V, 400 Hz) to the coil of an electromechanical relay. The driver maximum voltage drop is 2.0 V rms. The driver turn-on/off control voltage is a nominal 5 V/0 V dc and the maximum input current is 10 mA.
3) The relay contacts apply the nominal 230 V ac to the load; auxiliary relay contacts are used to provide a signal as to the Status (open/closed) of the relay contacts.
4) The EMPC turn on/off time is 20/40 msec maximum.

3.5 Solid State Power Controllers

A block diagram of an SSPC is shown in Figure 2.

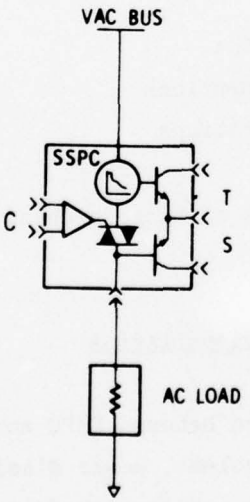

Figure 2. SSPC Block Diagram

The design features are:

1) Electronic, remotely resettable circuit breaker capability that indicates a Trip for load currents greater than 2 A.
2) Electronic control of the SCR switches. The maximum voltage drop, including the sense resistor is 2.2 V rms.
3) The control input on/off signal is a nominal 5 V/0 V dc with a maximum current of 3.3 mA.
4) SSPC turn-on at zero volts and turn-off at zero current is provided.
5) The SSPC has an optional 200 mA dc load capability.
6) The SSPC will operate either normally open or normally closed.
7) A 5 msec delay of the control input signal is provided to prevent inadvertent turn-on/off of the SSPC by noise on the control input line.
8) Turn-on/off of the SSPC is accomplished within 10 msec.

3.6 Aircraft Usage of 2 A PCs

The 2 A aircraft loads that are amenable to mechanization by both EMPCs and SSPCs are:

1) Single phase loads
2) 0 to 200 mA dc loads
3) Three-phase loads with:
4) "ANDed" logic configurations
5) "ORed" logic configurations

Schematic representations of these mechanizations are shown in Figure 3 and 4.

3.7 EMPC and SSPC Circuit Characteristics

Before making a comparison between EMPC and SSPC characteristics, it is necessary to list the weight, volume, power dissipation, and reliability of the components of both PC types, since such features are an important aspect of aircraft operation and availability.

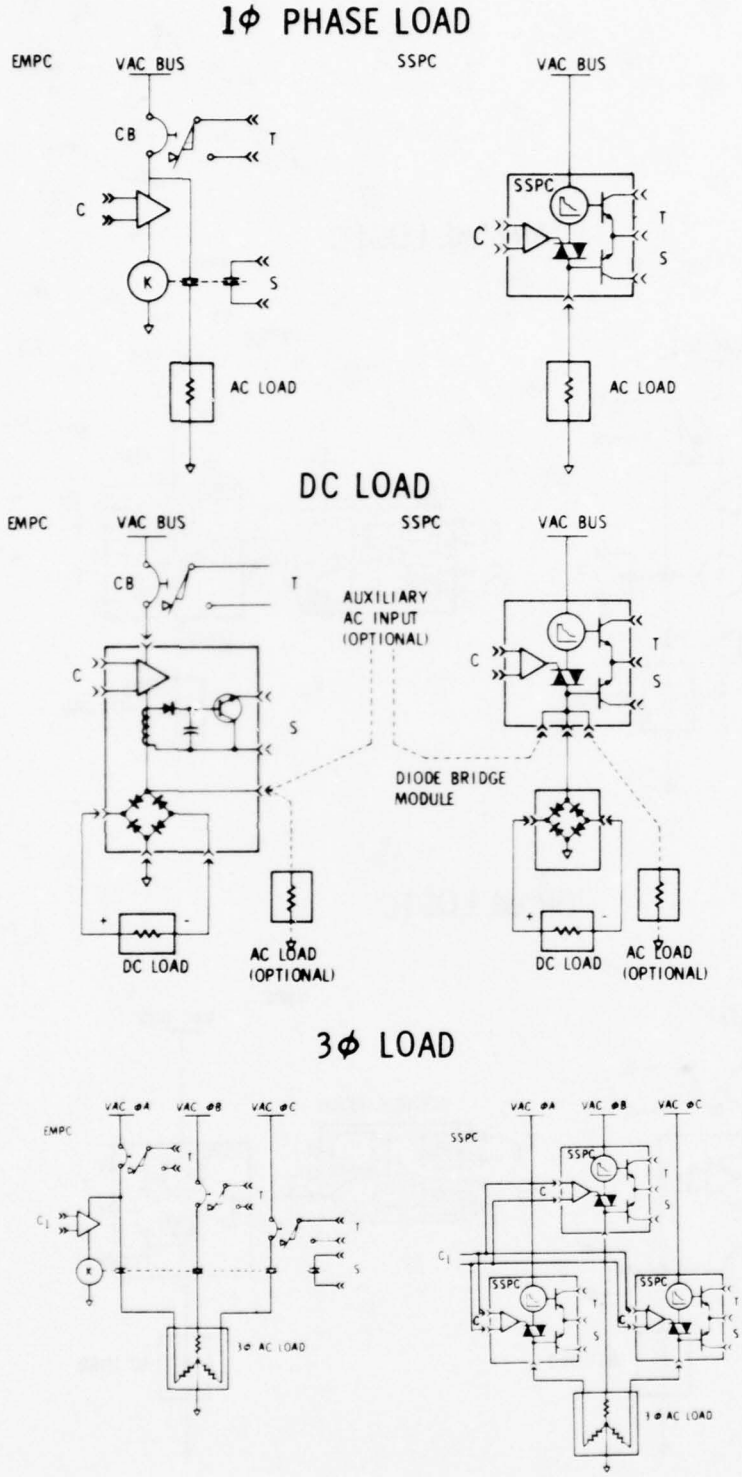

Figure 3. Applications

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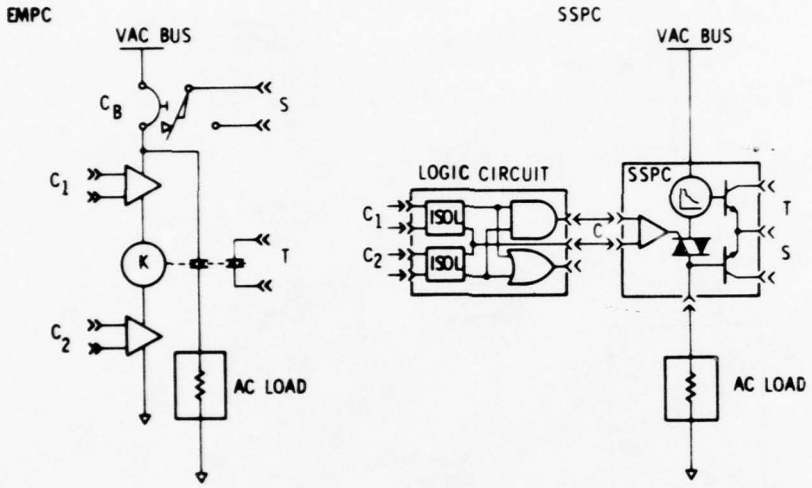


'OR'ed LOGIC

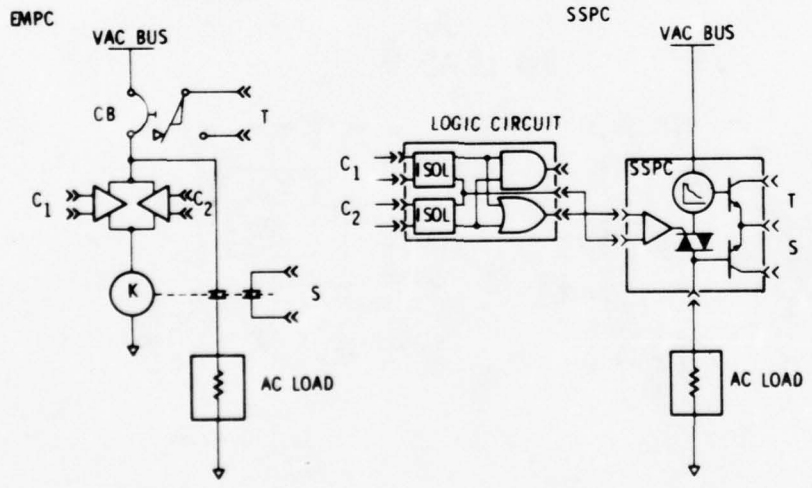


Figure 4. Control Functions

3.7.1 Power Dissipation (2 A)

SSPC

Item	Watts (maximum)
Power Hybrid	2.4
Control Hybrid	0.6
Sense Resistor	0.9
Voltage Sense Resistor	0.3
Transformers	0.4
Total	4.6

For comparison assume the allowed maximum: 5.5 W

EMPC

Item	Watts (maximum)
Circuit Breaker (Type 1)	2.80
Relay (V22A)	5.06
Driver (Type 1)	0.10
Total	7.96

3.7.2 Weight

SSPC

Item	Weight (lb)
1/4 Power Transformer	0.045
Hybrids	0.056
Miscellaneous Components	0.097
Total	0.198

EMPC

Item	Weight (lb)
Relay (V22A)	0.100
Circuit Breaker (Type 1)	0.090
Driver (Type 1)	0.125
Total	0.315

Packaging of the SSPC or EMPC circuits is assumed to be identical, i.e., on printed circuit boards plugged into an LRU Master Interconnect Board (MIB). Therefore, the weight of the boards, the wiring between the MIB and LRU interface connectors, the LRU chassis, etc. which is common to both the SSPC or EMPC design is not needed to make a comparison between the two design approaches. However, it should be noted that the weight of an SSPCA packaged as described and containing 68 SSPC circuits is approximately 31 lb, of which, about 13.4 lb or 43 percent is contributed by the weight of the SSPC electronic parts and 57 percent, or 17.6 lb, by the weight of the boards, wiring between the MIB and LRU connectors, and the LRU chassis.

SSPC

Item	Volume (Cubic Inches)
Power Hybrid	0.586
Control Hybrid	0.658
1/4 Power Transformer	0.492
Inductor	0.167
Capacitor	0.083
Resistor	0.079
Resistor	0.014
Inductor	0.018
Total	2.097

EMPC

Item	Volume (Cubic Inches)
Relay (V22A)	0.61
Circuit Breaker (Type 1)	1.34
Driver (Type 1)	1.43
Total	3.38

3.7.4 Reliability

SSPC

Item	Failures/10^6 hr
Power Hybrid	0.4663
Control Hybrid	3.1115
Fuse	0.1
Capacitor	0.114
Resistor	0.102
Transformers	0.047
Total	3.94

EMPC

Item	Failures/10^6 hr
Circuit Breaker (Type 1)	14.90
Driver (Type 1)	7.14
Relay (V22A)	4.20
Total	26.24

3.7.5 Comparison of EMPC vs SSPC

The previous set of Power Controller characteristics are shown in Table 1 in order to make a comparison.

3.7.5.1 Discussion

The comparison between EMPCs and SSPCs indicates that the SSPC design is superior to the EMPC configuration. Of particular advantage for an avionics system is the higher reliability (almost double) and the lower weight, volume, and power dissipation. Higher reliability means increased aircraft availability. The small difference in weight and volume, when multiplied by the PC usage number of 900, represents a desirable decrease in aircraft weight and space. Lower power dissipation translates into less weight (smaller heat dissipators) and decreased demand on the aircraft cooling supply.

The generation of less electromagnetic interference by switching with full cycle on/off control plus the 5 msec noise filtering of the control input are additional desirable operational features of the SSPC design.

TABLE 1

COMPARISON OF EMPC VERSUS SSPC

Item	EMPC	SSPC	Remarks
Response Time	25 msec	10 msec	
Normally Open/Closed	Yes	Yes	
Voltage Drop	1.4 V	2.2 V	
Remote Reset	No	Yes	
EMI Suppression	Fair	Excellent	Full cycle on/off control
Power Dissipation	7.96 W	5.5 W	
Weight	0.3 lb	0.2 lb	
Volume	3.4 $in.^3$	2.1 $in.^3$	
Reliability	26.2 Failures/ 10^6 hr	3.9 Failures/ 10^6 hr	
Inverse Trip Time	Yes	Yes	
Trip Free	Yes	Yes	
Control Input Filter	No	Yes	
Fail Safe	No	Yes	The SSPC is fused

3.7.6 Power Control Assembly Design

3.7.6.1 Background

During the latter part of 1974, the Strategic Systems Division of Rockwell International was engaged in the assembly of EMPCs for the Rockwell International B-1 Division. During the fabrication cycle, Manufacturing Engineering determined that a large amount of the assembly cost was in the attachment and routing of interconnecting wiring.

Studies were conducted to determine designs that would reduce the amount of wiring. The possibility of eliminating a significant portion of handwiring, plus their suitability for printed circuit board packaging made SSPCs an attractive candidate as the power controller design for Aircraft No. 5.

The following section describes the Aircraft No. 4 EMPCAs and SSPCAs proposed for Aircraft No. 5.

3.7.6.2 EMPCA Description

An EMPCA consists of circuit breakers mounted to the front panel of the LRU and relay drivers and relays that are plugged into connectors. The connectors are permanently mounted to fixed metal panels. Individual wires are used to interconnect the circuit breakers, drivers, and relays together and to the appropriate interface connector. Figure 5 shows a typical EMPCA.

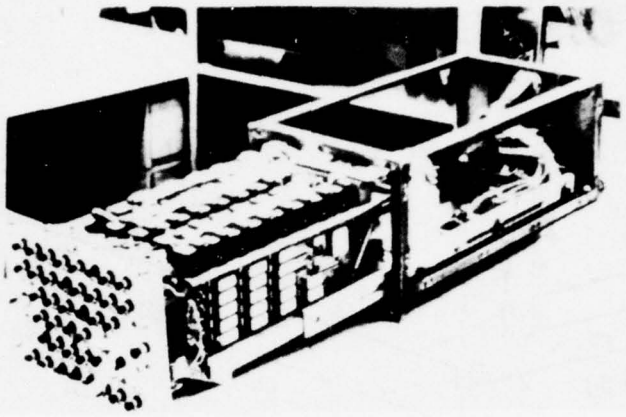


Figure 5. Electromechanical Power Controller Assembly

3.7.6.3 SSPCA Description

An SSPCA consists of 15 identical AC Power Control Modules, a Status module and a Logic module housed in an LRU. Figure 6 shows a typical SSPCA.

Interconnection between the interface connectors and the modules is made via a printed circuit Master Interconnect Board.

Each AC Power Control module consists of four PC circuits rated at 2 A rms. The four PCs on a given module are "hard-wired" to the same phase and share the primary winding on the power transformer. From that point on, they are completely separate, independent power controllers. Each circuit is capable of operating either normally closed (switch ON when control input is zero volts), or normally open (switch OFF when control input is zero volts). The selection of normally open or normally closed mode is accomplished by externally jumpering the NO/NC pin to the desired NO or NC pin on the appropriate SSPC interface connector.

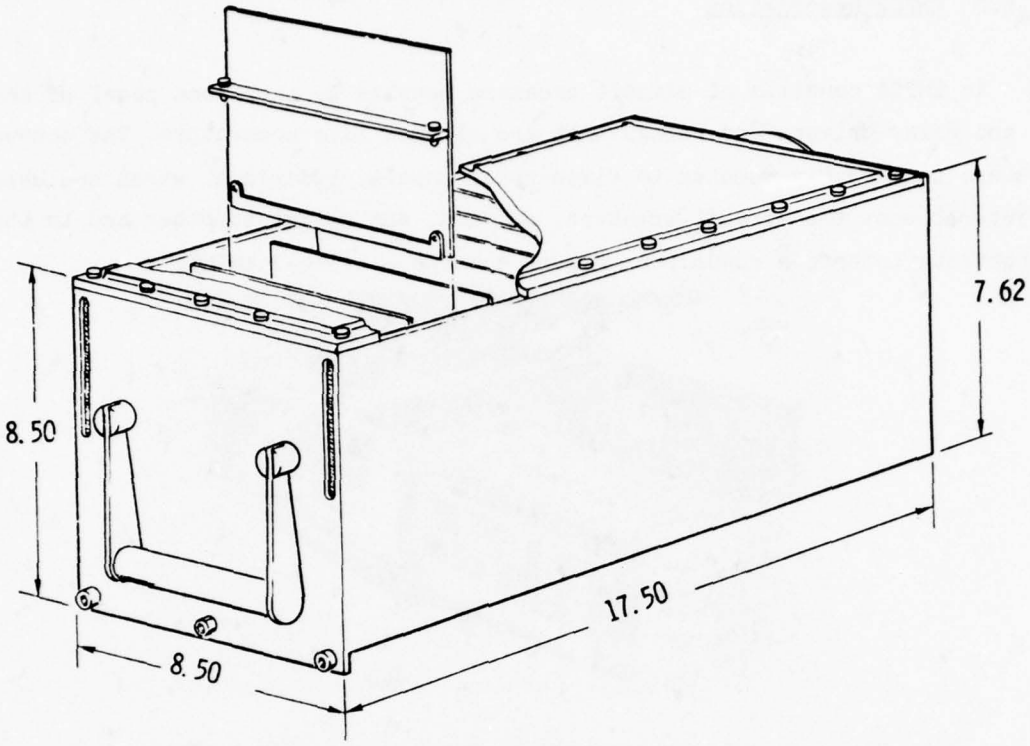


Figure 6. Solid State Power Control Assembly

The Logic module supplies 16 independent circuits that logically combines SSPC control signals in a configuration "AND" or "OR" where two or more commands are required to sequence the same SSPC On or Off.

The Status module contains 26 separate and independent circuits that provide a switch closure under the control of a 5 V dc or 28 V dc input command.

3.7.6.4 Comparison of EMPCA vs SSPCA

Aircraft No. 4 contained EMPCAs of 24 different designs. Early trade studies directed at reducing hardware life cycle costs and increasing aircraft availability indicated in part, that a mix of 14 EMPCAs and 17 SSPCAs for Aircraft No. 5 would reduce life cycle costs of power controllers by 105 million dollars, increase reliability from 24 hr Mean Time Between Failure

to 68 hr and reduce weight, volume, and power required by 105 lb, 6.78 cubic feet and 2310 W respectively. Subsequent apportionment of PCs reduced the number of SSPCAs required to 14 and the number of EMPCAs to 13.

The EMPCA and SSPCA designs described in the preceding section were the result of numerous system trade-offs that assumed ground rules and conditions that are no longer applicable.

To properly compare EMPCAs and SSPCAs, a hypothetical equivalent EMPCA design is defined here. It is assumed that both packaging designs are as identical as possible, differing only where necessary:

1) Each EMPCA and SSPCA shall consist of 60 separate 2 A circuits mounted on plug-in modules; for the EMPCA only, the circuit breakers are mounted on the front panel.
2) The EMPCA is convection cooled; the SSPCA is conduction cooled.
3) Both assemblies use a MIB for interconnection to the interface.
4) The form factor of the assemblies can be optimized to suit the particular assembly requirements; for example, the EMPCA would have a larger front panel to mount the 60 circuit breakers than the SSPCA.
5) Both the EMPCA and the SSPCA would be blind mated plug-in assemblies.
6) An aircraft set would consist of 14 assemblies with a total of 840 PC circuits.

An analysis of the EMPCA and SSPCA configurations indicates that the major difference in packaging between the two is the wiring of the circuit breakers required in the EMPCA. Wiring the circuit breakers would add approximately 2 lb and 130 cubic inches to the EMPCA.

A comparison of an SSPCA and an EMPCA is shown in Table 2.

3.7.6.5 Discussion

The tabulated comparison of EMPCA vs SSPCA designs, indicates that the SSPCA design is superior to the EMPCA configuration in all respects. Though similar packaging methods are used for both designs, significant weight and volume reductions are afforded by using solid state components.

The improvements in operation with respect to reliability, remote reset capability, EMI suppression and immunity to noise is possible with SSPCs.

TABLE 2

COMPARISON OF EMPCA TO SSPCA (840 PCs)

Item	SSPCA	EMPCA
Weight	Baseline	SSPCA + 14 x 2 x 840 x 0.1 = SSPCA + 112 lb
Volume	Baseline	SSPCA + 14 x 130 + 840 x 1.3 = SSPCA + 9 cu ft
Power Dissipation	4620 W	6686 W
Reliability (MTBF)	302 hr	45 hr
Control Input Filter	Yes	No
Remote Reset	Yes	No
EMI Suppression	Excellent	Fair (See para. 3.7.6.5)

The relay in an EMPC circuit applies or removes power to its aircraft load in a random point of the current cycle. Thus on the next turn-on, power may be applied to a saturated inductive load, drawing large amounts of in-rush current and causing a corresponding high level of electromagnetic interference. Since the SSPC turns off nominally at zero load current under full cycle control, power will always be applied to an unsaturated load, and the generation of this type of electromagnetic interference is significantly reduced. The SSPC turns on when the bus voltage is nominally zero; thus, when turning on into a load that requires a finite time to go from a low resistance to a higher resistance, such as lamp filaments, the voltage is applied gradually (sinusoidal, zero to maximum) rather than, possibly maximum, as could be the case with a relay. Thus, less electromagnetic interference would be produced with the SSPC circuit.

Though not discussed in detail here (see Appendix B for details), the moderately higher initial costs of solid state components should be more than offset by the cost of wiring and/or replacing the circuit breakers, the cost to the avionics system of providing more power, weight, and volume for the EMPCAs and the increased life cycle costs and decreased aircraft availability due to the higher EMPCA failure rate.

SECTION IV
SSPC DESIGN

4.1 Power Controller Design Objective

The objective of the Strategic Systems Division Power Controller design was to provide PCs at lower cost than EMPCs but with equal or improved functional characteristics.

The details of how these design objectives were met is presented in the following subsection.

4.2 SSPC Design

Studies to reduce the cost of the B-1 Aircraft were conducted by the Rockwell International B-1 Division with assistance from the Strategic Systems Division. The assistance centered on consideration of a combined Central Integrated Test System/Electrical Multiplexing (CITS/EMUX) redesign. A significant discovery during the study was that the actual usage and mechanizations of the EMUX-PCA interfaces could be modified and appeared to offer considerable cost savings. One basic requirement for this approach was that sufficient volume be available to provide common housing for the PCAs and EMUX hardware. The use of solid state PCs along with PCA repackaging was proposed to provide the needed volume.

Simultaneously, studies of the number and current capacity of the PCs in the B-1 were being conducted as a part of the EMUX-PCA combination study proposal and it was noted that a large portion of the B-1 PC circuits were used for less than 300 mA (see Figure 7). The studies are documented in Volume III of Rockwell International report NA-74-887 and indicated that the solid state low amperage circuits could be mounted on printed circuit modules and interconnected using printed circuit techniques. This method would reduce the hand-wiring significantly since it uses batch process wiring without the need for panel mounted circuit breakers; the circuit breaker function is integral to a SSPC.

The application of SSPCs to B-1 requirements revealed that several additional changes should be included as follows:

1) Control Voltage Threshold Detection - to turn on at ≥ 3 V and turn off at ≤ 2 V. This change would reduce the drain on the EMUX power supplies.
2) Full Cycle Control - to turn on at zero voltage crossing and turn off at zero current crossing with the same slope. It was highly desirable to reduce the level of electromagnetic interference on the aircraft.
3) Control Voltage Pulsewidth Detection - to ignore control signals that change state for less than 5 msec. The actual time of 5 msec was arbitrarily selected as two cycles of the primary power (400 Hz) and longer than the maximum expected duration of a noise pulse.
4) The SSPC should operate either as a normally open (the usual mode) or as a normally closed switch.
5) One SSPC circuit failure could result in only the failure of that particular SSPC; i.e., a circuit configuration that included a DC power supply common to a set of SSPCs could not be used, since its failure would cause additional circuit failures.

4.3 SSPC - Brief Description

The Strategic Systems Division SSPC is a remotely resettable pair of SCR switches with an internally derived circuit breaker capability. Two hybrids, the Control Hybrid and the Power Hybrid, contain the majority of the circuitry required to mechanize the SSPC. A block diagram of an SSPC is shown in Figure 8.

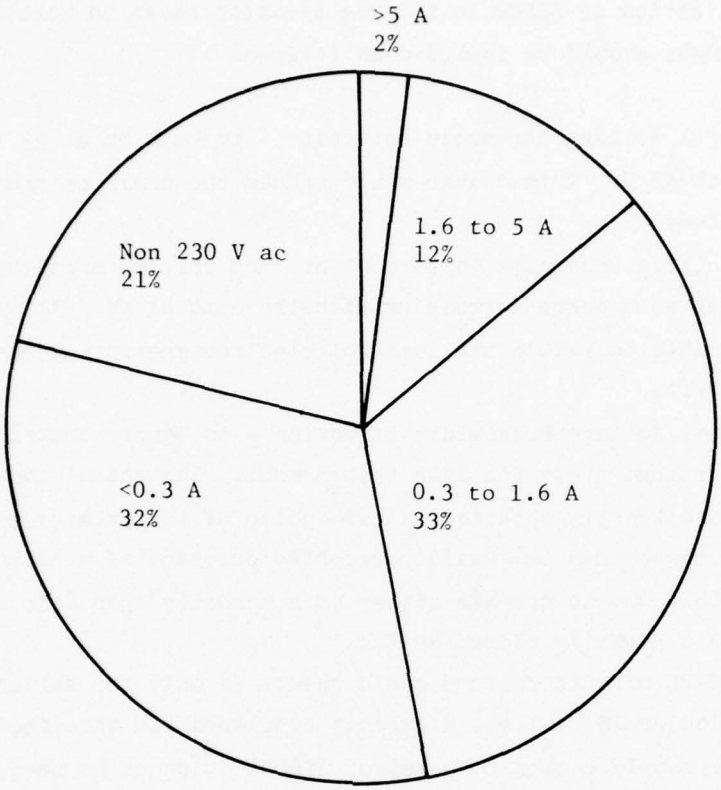


Figure 7. Distribution of Power Controller Loads

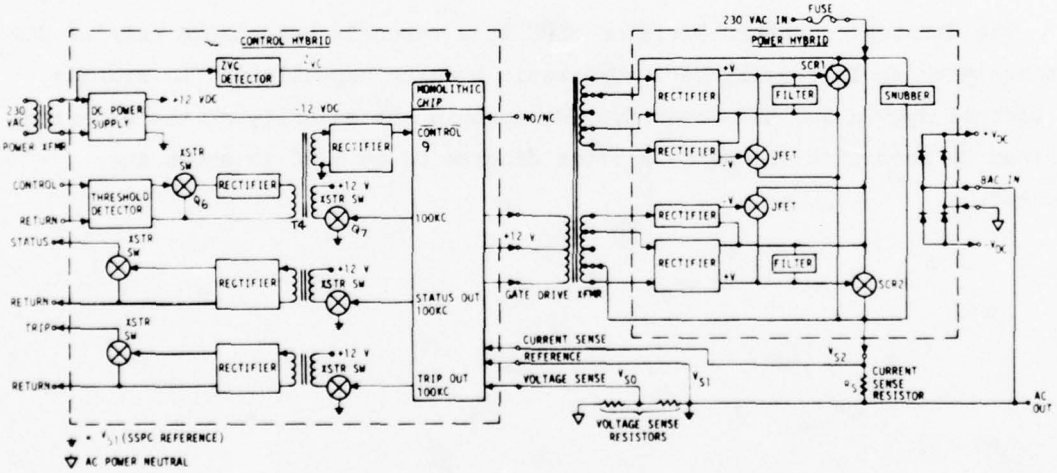


Figure 8. SSPC Block Diagram

The Control Input circuit requires a 3 to 6 V dc level when the SSPC is required to be turned ON and 0 to 2 V for the OFF state (the normally closed mode is the opposite). If the control input is at the nominal 5 V level for ≥5 msec and the Zero Voltage Crossing circuit detects a zero voltage crossing, the Monolithic timing and control integrated circuit chip (Monolithic) enables the 50 kHz drive to the SCRs in the Power Hybrid, applying 230 V, 400 Hz power to the load.

The load current and voltage levels are sensed via their respective resistors and evaluated by the Monolithic. The Monolithic issues a Status true signal when a voltage >160 V ac is applied to the load and a Trip signal when the Monolithic's Analog-to-Digital Converter determines that an overcurrent condition exists. The Monolithic simultaneously turns off the drive to the SCR switches when an overcurrent condition is detected.

Normal SSPC turn off occurs when the zero current crossing circuit in the Monolithic detects zero load current and a 0 to 2 V control input. Normal turn on and turn off occurs on opposite 400 Hz power half cycles.

A fuse that opens at overcurrents between the SSPC Trip levels and the aircraft wiring damage points is in series with the switch as a fail-safe element.

4.4 Control Input Threshold Detector

At SSPC power turn on, the Monolithic drives transistor Q7 at a 100 kHz rate, which in turn applies 12 V, 100 kHz pulses across the primary of transformer T4 (refer to Figure 8). When the Control Input circuitry receives a +3 to +6 V dc level command from EMUX, the SSPC is required to turn ON. This voltage input will cause transistor Q6 to turn on, short circuiting the transfer of energy from the primary of transformer T4 to the secondary. This causes the voltage at pin 9 of the Monolithic to be low (0 to 6 V). The Monolithic will turn on the drive to the SCRs turning the SSPC on.

When the SSPC is commanded OFF (0 to 2 V dc), transistor Q6 opens and the energy from the Q7 winding of T4 is coupled to the rectifier connected to the secondary winding connected to pin 9. The rectifier output voltage at pin 9 will be from 9 to 12 V (CONTROL P high) and the Monolithic will turn off the drive to the SCRs, turning the SSPC off.

The Threshold Detector must turn on the switch control circuitry when the control input signal is 2.5 $\pm$ 0.5 V dc, operate over a temperature range from -55 to 75 °C, not require more than 3.3 mA drive at 6 V dc, and provide greater than 1000 V of electrical isolation between the control input circuitry and the 230 V sections. The component part temperatures range from -55 to 125 °C.

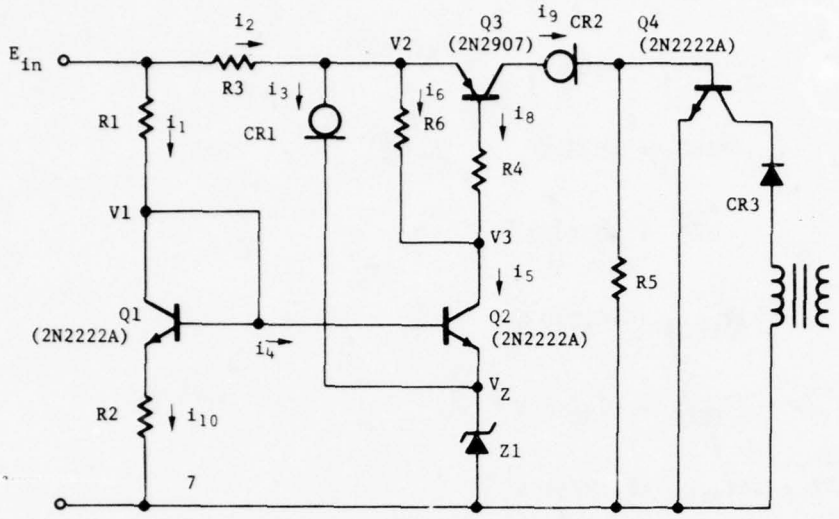
These stringent requirements were solved by a unique combination of bipolar, JFET, and transformer coupled circuitry. Refer to Figure 9.

A worst-case analysis of the Threshold Detector circuit must show that:

1) Q4 is ON when $2.0 \leq E_{in} \leq 3.0$ V
2) At $E_{in} = 6.0$ V, $I \leq 3.3$ mA

Assume the following set of parameters:

1) Component temperatures: -55 to 125 °C
2) Minimum β at -55 °C and specified total dose and neutron exposure:
   23 for 2N2907A
   26 for 2N2222A
3) Base-to-Emitter Voltages:
   V_{BEQ2} = 0.5365 V at 25 °C
   V_{BEQ1} = 0.545 V at 25 °C
   ΔV_{BEQ2} = 3.1 mV/°C
   ΔV_{BEQ1} = 2.1 mV/°C



R1 = 30.9 K ± 1%
R2 = Selected = 53.6 K
R3 = 120 Ω ± 5%
R4 = 5.1 K ± 1%
R5 = 10 K ± 1%
Z1 = LM 113
R6 = 20 K ± 1%
Q1 = 2N2222A
Q2 = 2N2222A
Q3 = 2N2907A
Q4 = 2N2222A
CR1 = CR100
CR2 = CR100
CR3 = 1N4153

Figure 9. Threshold Detector Circuit

4.4.1 Q4 Turn On

The maximum collector current that transistor Q4 is required to "sink" is 10.0 mA. Transistor Q4, a 2N2222A, will therefore be turned on with a base current of $i_b = i_7 = \frac{10}{26} = 0.38$ mA. CR2 will limit i_9 to 1 mA; i_7 will therefore be between 0.9 and 1.0 mA, well in excess of transistor Q4 turn on requirements.

The worst-case analysis will show that the Threshold Detector circuit will supply a minimum of 0.9 mA to transistor Q4 when the Control Input voltage is 3 V. (Refer again to Figure 9.)

Resistor R2 is trimmed at the Control Hybrid assembly level so that transistor Q4 is on at E_{in} = 2.5 V at 25 °C. The measured average magnitudes of resistor R2 has been found to be 53.6 K. At -55°C:

$$E_{in} = 3.0 \text{ V}$$

$$\Delta R1 = -309\ \Omega$$

$$\Delta R2 = -536\ \Omega$$

$$\Delta V3 = +0.0122$$

$$\Delta V_{BEQ1} = +0.210 \text{ V}$$

$$\Delta V_{BEQ2} = +0.248 \text{ V}$$

$$V_1 = V_Z + V_{BEQ2} + \Delta VZ + \Delta V_{BEQ1} = 1.9781 \text{ V}$$

$$i_1 = 33.4\ \mu\text{A}$$

$$i_4 = 33.4\ \mu\text{A} - \frac{V1 - V_{BEQ1}}{R2} = 10.36\ \mu\text{A}$$

$$i_5 = 10.36\ Q2\ \text{min} = 269\ \mu\text{A}$$

If V_{CEQ2} increases at a rate of -2 mV/°C:

$$V3 = 1.5559 + \Delta V_{CEQ2} + V_X$$

$$V3 = 1.7681$$

Assume $i_3 = i_9 = 1$ mA (maximum)

Then $i_2 = i_3 + i_9 + i_5 = 2.269$ mA

and $V2 = E_{in} - i_2\ R3 = 2.728$ V

$$i_e = \frac{V2 - V3}{R6} = 85\ \mu\text{A}$$

and $i_8 = i_5 - 8\ \mu\text{A} = 184\ \mu\text{A}$

$$i_9 = \beta Q3\ i_8\ \text{min} = 4.23 \text{ mA}$$

Since 4.23 mA is much greater than the 0.9 mA required, transistor Q4 will be turned on at -55°C.

4.4.2 Q4 Turn Off

It remains to be shown that transistor Q4 will be off at E_{in} = 2.0 V and +125°C:

$$E_{in} = 2.0 \text{ V}$$

$$\Delta V_{BEQ1} = -0.210 \text{ V}$$

$$\Delta V_{BEQ2} = -0.310 \text{ V}$$

$$\Delta VZ = -0.0122 \text{ V}$$

$$\Delta R1 = +309 \ \Omega$$

$$\Delta R2 = +340 \ \Omega$$

$$V_1 = V_Z + V_{BEQ2} + \delta V_Z + \Delta V_{BEQ1} = 1.435 \text{ V}$$

$$i_1 = 11 \ \mu A$$

$$i_{10} = \frac{V_1 - V_{BEQ1}}{53.6 \text{ K}} = 20 \ \mu A$$

$$i_4 = 11 \ \mu A - 20 \ \mu A = -9 \ \mu A$$

Therefore transistor Q2 (and subsequently transistors Q3 and Q4) will not turn on. The SSPC will be off at V_{in} = 2.0 V and +125°C.

4.4.3 EMUX Current Drain

The maximum current drain on EMUX must not exceed 3.3 mA at E_{in} = 6.0 V:

$$i_{max} = i_1 + i_3 + i_6 + i_8 + i_9$$

The total current $I = i_1 + i_2 + i_3 + i_4$ where E_{in} = 6.0 V at +125°C

$$i_1 = \frac{VR1}{R1} = \frac{E_{in} - V_{BEQ2\ min} - V_Z}{R1_{min}} = \frac{6.0 - 0.177 - 1.21}{30.6\ K} = 0.151\ mA$$

$$i_3 = 1.1\ mA + (-0.075\%/°C)\ (100°C)\ \frac{1.1\ mA}{100} = 1.018\ mA$$

$$i_8 = \frac{VR4}{R4} = \frac{E_{in} - 3.0\ mA\ (120) - V_{EBQ3\ min} - V_{CEQ2\ min} - V_Z}{R4} \simeq 0.798\ mA$$

$$i_9 = 1.1\ mA + (-0.075\%/°C)\ (100°C)\ \frac{1.1\ mA}{100} = 1.018\ mA$$

$$i_6 = \frac{VR6}{R6} = \frac{(E_{in} - VR_3) - (V_{CEQ2} + V_Z)}{R6} = 0.211\ mA$$

$$i_{max} = 0.151 + 2(1.018) + 0.798 + 0.211$$

$$i_{max} = 3.196\ mA \text{ at } E_{in} = 6.0\ V$$

The maximum EMUX current drain does not exceed 3.3 mA.

4.5 Monolithic Timing and Control Circuit

4.5.1 Background

The circuit element that provides the timing and control functions of the SSPC is a digital integrator and controller designated the Monolithic Timing and Control Integrated Circuit or Monolithic.

The initial SSPC designs proposed by Strategic Systems Division used an analog approach. As the study progressed, the number and size of the functions (or the capability to trip at the same time for a fixed overload) was difficult to maintain without the use of precision capacitors relatively large in size. The increased capacitor size spurred studies into a hybrid mechanization of the control circuit but the large number of parts made it costly. Further cost reduction efforts initiated investigation of integrated circuit mechanizations. The first mechanizations used three integrated circuits for digital control, analog trip timing, and zero crossing detectors. However, due to the growing size, stability problems, and nuclear radiation hardness requirements of the analog mechanization, a digital integrator approach was conceived. The digital approach was more promising because it permitted all of the control and trip electronics to be built as a single integrated circuit, thus providing small size with improved reliability. The device could be made as a CMOS using SOS. The use of CMOS on SOS, with its dielectric isolation, provides additional capability to meet the B-1 hardness criteria.

4.5.2 Monolithic Circuit Design

The primary use of the Monolithic is to provide full cycle control of ac power being delivered to an electrical load. This full cycle control is provided by driving a solid state pass element, the SCRs, beginning with the line Zero Voltage Crossing (ZVC) at zero V ac and ending with a complete cycle of the load current at Zero Current Crossing (ZIC) (See Figure 10). While the solid state pass element is on, the Monolithic monitors the load current through the pass element and computes a turn off point (Trip Time) for every value of load current in excess of 110 percent of the rated current. When the load current exceeds the rated current by more than 110 percent for longer than the computed trip time, the drive to the solid state pass element is extinguished without regard to ZIC. A characteristic curve, Figure 11, shows the time allotted before trip or shut down as a function of a load current for a 2 A rated SSPC. Full cycle control is accomplished by timing the enabling and disabling of complementary drive outputs through which the SCRs can be turned on and off.

The Monolithic contains the following analog and digital circuits:

Analog	Digital
ADC Comparator	Up/Down Counter
Gain of 20 Amplifier	Shift Register
Comparator ZIC	Arithmetic Unit Accumulator
R-2R Ladder	Timer 5 msec and 2.5 msec
Switches	Mode Control
Comparator Voltage/Status	200 kHz Oscillator
	Clock Divider
	STAOT Status Logic

Unique to the Monolithic is the ability to combine LSI digital computing and analog signal processing on a single Monolithic CMOS/SOS integrated circuit. The analog signal processing includes conversion from analog to digital with a tracking type or counting converter as well as large (circa ± 5 V) and small (circa ± 50 mV) signal threshold detection circuits with sufficient hysteresis incorporated to eliminate any crossover jitter problems. A block diagram of the Monolithic is shown in Figure 12.

4.5.2.1 Analog-to-Digital Converter (ADC)

The ADC consists of an Analog Comparator, an R-2R resistor ladder, seven analog ladder driver switches, a seven stage Up-Down Counter, a six bit recycling shift register and logic to approximate the absolute value of the shift register output.

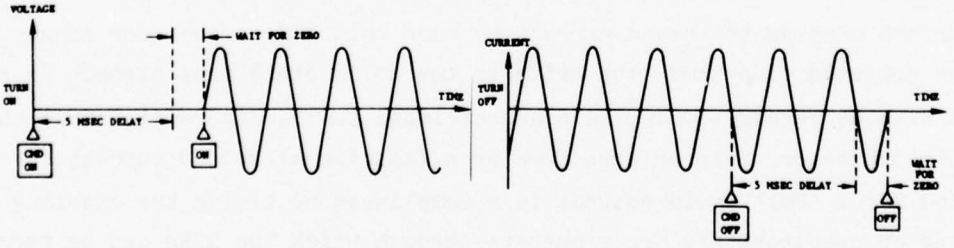


Figure 10. SSPC On-Off Control

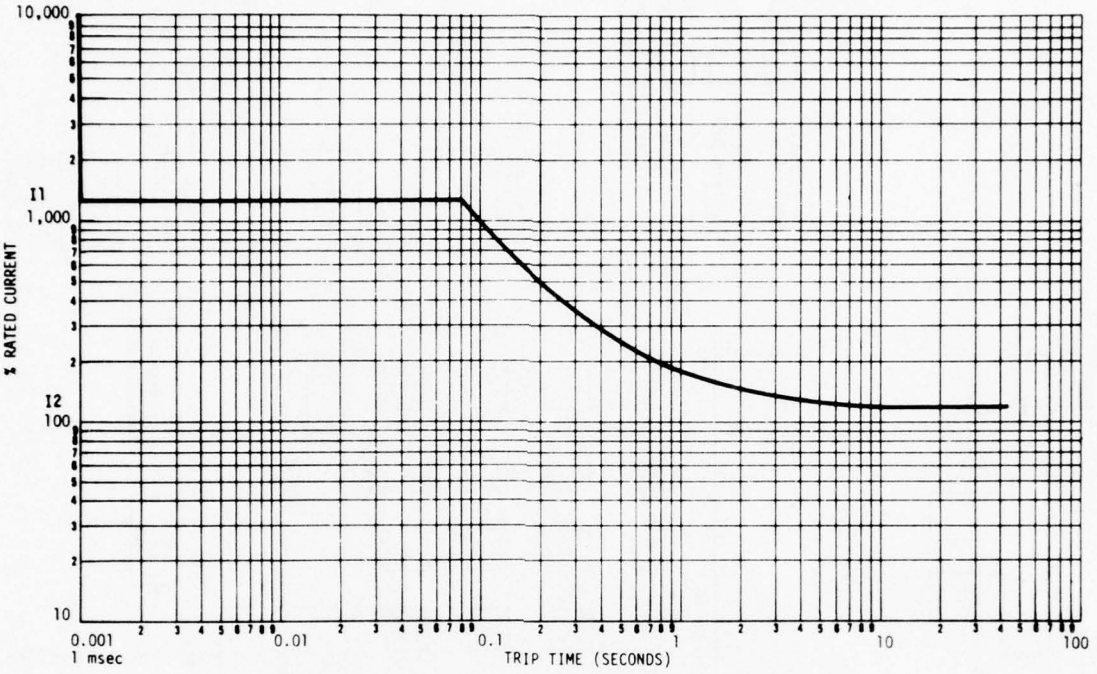


Figure 11. Rated Current versus Trip Time

Figure 12 shows the interconnection of each of the components of the ADC. The ADC tracks the voltage applied to the Sense Input and provides a serial output (I) that represents the absolute value of the Sense Input.

In the comparator, decisions are made as to the magnitude of the Sense Input compared to the output of the R-2R Ladder Network. The comparator then commands the Up-Down Counter to increase or decrease its binary count (and therefore, the output of the ladder) until the two are within the resolution ($\pm$1 bit) tolerance.

Under control of the Shift Load Control (SHLF), the magnitude of the Up-Down Counter is transferred to the Parallel-to-Serial Register (Shift Register) while the sign bit is transferred to a separate flip-flop. When the Shift Register is not loading, it is continuously shifting the least signifi-

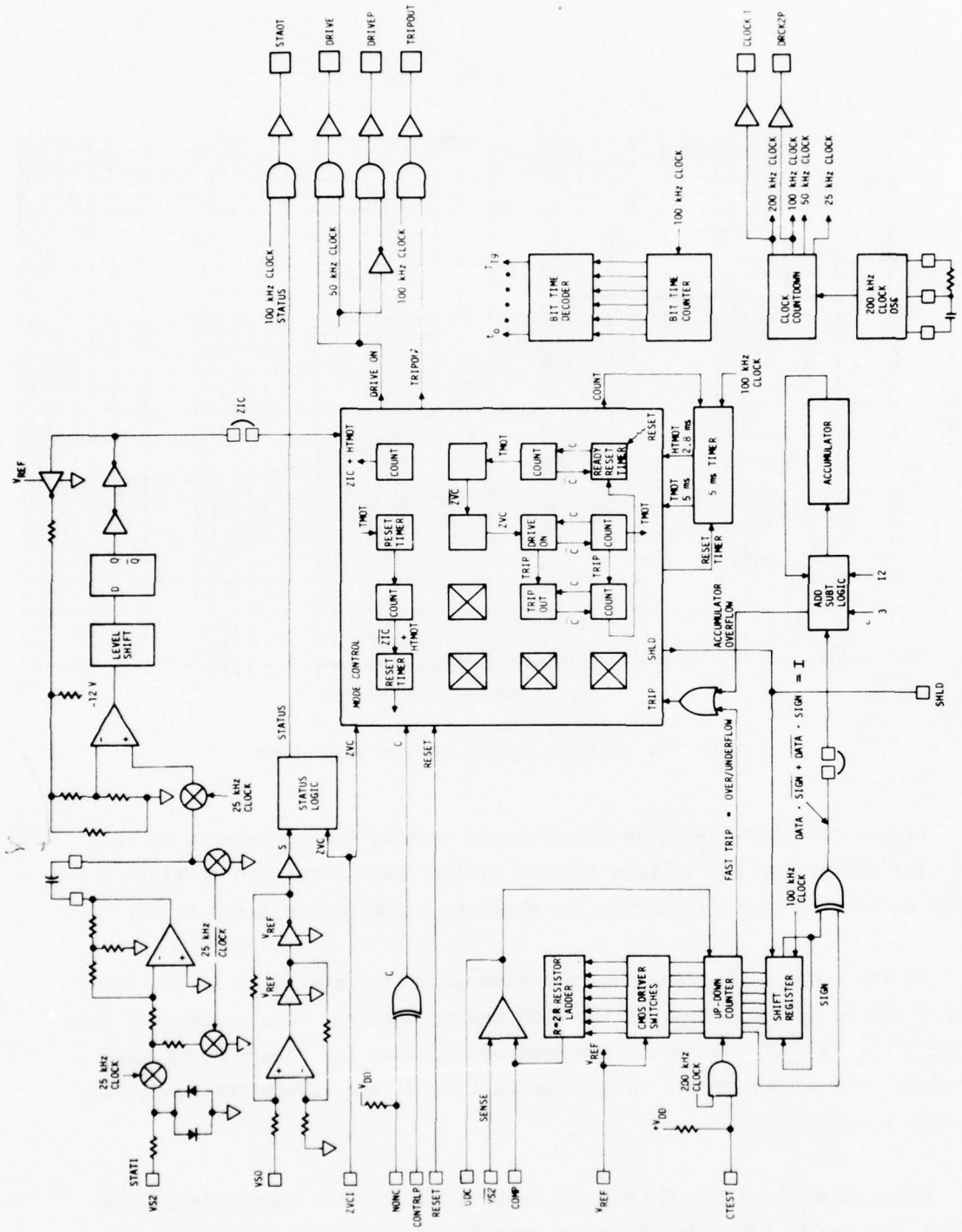


Figure 12. Monolithic Block Diagram

cant bit first into an exclusive OR gate and then back into its most significant bit end. The exclusive OR of the data and the sign provides a serial output that approximates the absolute value of the ADC output.

An unusual feature of the gate input on the CMOS/SOS analog comparator is that it can swing above and below the supply levels owing to the isolation of the input gate oxide and the dielectric provided by the sapphire. Also the protection circuit will afford $\pm$17 V before zener action of the overvoltage protection diodes begins. Consequently, fault surges will not damage the comparator (Sense) input or the low level current input (VS2 STATI) of the gain of 20 amplifier.

The ADC speed is limited by the settling time of the R-2R Ladder Network and the response of the comparator circuit. As previously mentioned, the sapphire affords minimum parasitic capacitance so other device circuit constraints will not be required to enhance speed.

Two unique circuit features in the ADC allow optimum speed-power design trade-offs.

The first feature is the depletion mode N-channel Field Effect Transistors (FETs) in the second level gain stage of the comparator. This provides the large voltage gain required to obtain 80 dB gain into the amplifier output.

The second feature of the ADC is the delay stage, which prevents the large P-channel switch from turning on until the N-channel switch is turned off. A significant power saving results by eliminating the dc path created in normal large inverter switches when both FETs are simultaneously in their linear region of operation. Also, by eliminating the resultant current spike, a higher impedance reference filter may be used in the Monolithic.

Scaling of the ADC is such that "plus full scale" is +6 V and "minus full scale" is 0 V. The resolution or value of the least significant bit is 3/64 V. Any sense input equal to or greater than +6 V or less than or equal to 0 V will cause a Fast Trip.

4.5.2.2 Mode Control

Figure 13 is a logic flow diagram that illustrates the sequence of operations that occur and are controlled by the Mode Control in the Monolithic. The major functions are Turn On, Turn Off, Timed Trip, Fast Trip and Reset After Trip.

4.5.2.2.1 Turn On. When primary power is applied to the SSPC, all mode controls and counters in the Monolithic circuit are reset to a Ready or Standby mode. Once in a Ready mode, the circuit will continuously monitor C and ZVC. The term C is developed in the Monolithic as an exclusive OR of Control P and NO/NC.

Without a jumper at the SSPC external interface between the NO/NC pin and the SSPC reference ground, the NO/NC term is a logic 1 and the SSPC operates as a normally open switch.

With a jumper between the NO/NC pin and SSPC reference ground, the NO/NC term is a logic 0 and the SSPC operates as a normally closed switch.

Control P is the logic inverse of the SSPC Control Input. The following truth table describes the relationship between the terms Control Input, Control P, NO/NC, and C.

Control Input	Control P	NO/NC	C
1	0	0	0
0	1	0	1
1	0	1	1
0	1	1	0

C = 1, Turns on drive lines in prescribed sequence

C = 0, Turns off drive lines in prescribed sequence

NO/NC = 1, Normally open switch

NO/NC = 0, Normally closed switch

Control Input = 1, Input voltage = 3-6 V dc

Control Input = 0, Input voltage = 0-2 V dc

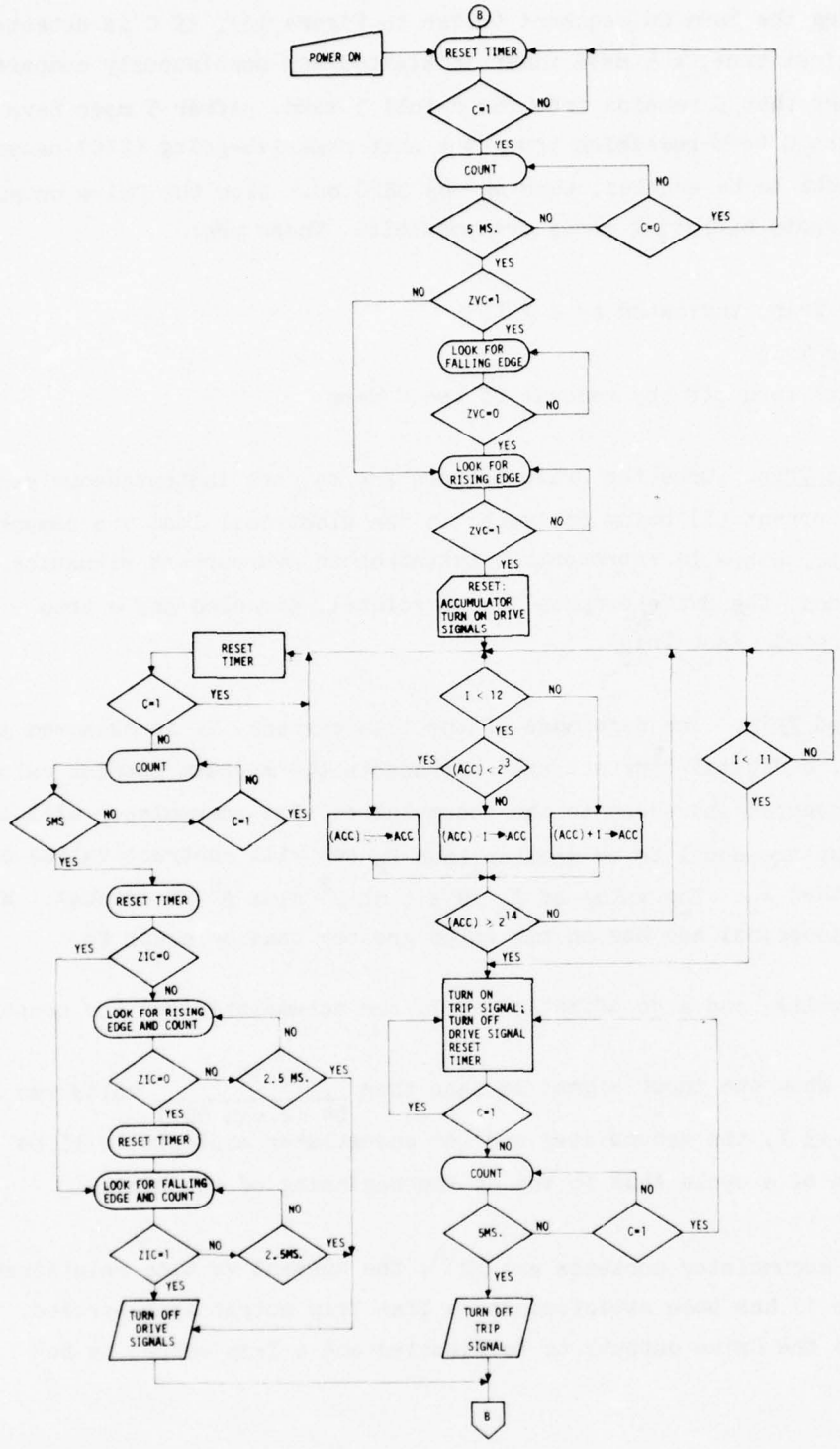


Figure 13. Logic Flow Diagram

Continuing the Turn On sequence (refer to Figure 13), if C is detected as being a logical true, a 5 msec timer is started and continuously compared with C to assure that C remains true for a full 5 msec. After 5 msec have elasped with the C term remaining true, the next negative-going (ZVC) causes the Drive outputs to be enabled, turning the SSPC on. With the Drive outputs on, three alternate operating modes are possible. These are:

(1) Fast Trip, indicated by $I \geq I_1$
(2) Timed Trip
(3) Normal turn off, by removal of the C term

4.5.2.2.2 Fast Trip. Once the Drive outputs are on, the instantaneous sensed values of the current (I) being delivered to the electrical load are compared to a constant I_1, where I_1 represents a catastrophic overcurrent situation. If I_1 is exceeded, the Drive outputs are immediately disabled and a trip output is generated (Fast Trip).

4.5.2.2.3 Timed Trip. The magnitude of the load current, I, is measured and compared to I_2, a digital constant that represents the minimum current value that will be accepted and added to the accumulator. The accumulator will add values of I that are equal to or greater than I_2 and will subtract values of I that are less than I_2. The value of I_2 is set at 2^2 plus 2^0 (5 counts). When the input is sinusoidal and has an rms value greater than or equal to $\frac{15}{64(2 \sin 60°)}$ volts, and a dc offset of +3 V, the accumulated sum (or contents) will increase. When the input signal is less than $\frac{15}{64\ (2 \sin 60°)}$ volts rms and a dc offset of +3 V, the accumulated sum (or accumulator contents) will be less at the end of a cycle than it was at the beginning of the cycle.

When the accumulator contents are $\geq 2^{14}$, the current vs time relationship shown in Figure 11 has been satisfied and a Time Trip output is generated. This will cause the Drive outputs to be disabled and a Trip output to be generated.

After entering the tripped state via Fast Trip or by Timed Trip, the Monolithic circuit must remain in this tripped state and the Trip output must remain true until the C term has been removed. If C is removed, a 5 msec timer is started and continuously compared with C to assure that C remains removed for the full 5 msec. When this is completed, the Trip output is reset, and all mode controls and counters are reset, returning the circuit to the Ready mode.

4.5.2.2.4 Turn Off. To prevent the large in-rush currents involved with saturated magnetic loads, and the subsequent generation of large amounts of electromagnetic interference, it is required that the ac line voltage be disconnected from the load when the load current is 0 $\pm$ 50 mA, with a positive slope. When C is removed, the 5 msec timing sequence starts. Upon completion, the mode control logic begins to look for a negative half-cycle of the load current. The ZIC signal is true during the negative half-cycle and false during the positive half cycle of the load current. When the 5 msec timing sequence is completed, the mode control logic will look for a false ZIC and simultaneously start a 2.5 msec timing sequence (one full cycle of this load current). When the ZIC signal goes from false to true or when the 2.5 msec timing sequence is completed, the Drive outputs are turned off. When the Drive outputs are turned off, all mode controls and counters are reset, returning the Monolithic to the Ready mode.

4.5.2.2.5 Reset After Trip. After entering the tripped state via Fast Trip or by Timed Trip, the Monolithic circuit must remain in the tripped state and the Trip output must remain true until the C term has been removed. If C is removed (false), the 5 msec timer is started and continuously compared with C to assure that C remains false for the full 5 msec. When this sequence is completed the Trip output is set to low (false) and all mode controls and counters are reset, returning the circuit to the Ready mode.

4.5.2.3 Digital Filter and Trip Time Computations

It is convenient to think of the digital filter structure as specifying a hardware configuration made up of a shift and an arithmetic and control unit. Refer to Figure 14.

Realization of a digital filter requires that past values of the output, input, and intermediate sequences be available. This implies a means of delay or storage which, in the Monolithic, has been accomplished by the shift register operating in a recirculating mode. This shift register is inhibited from recirculating when the ADC Up-Down Counter is parallel loaded into the Shift Register every 200 μsec. Two Shift Registers and Arithmetic Logic are used to mechanize the Digital Filter. The I Shift Register is described in the ADC section of this report and is loaded from the ADC Up-Down Counter at the last bit time of the machine cycle.

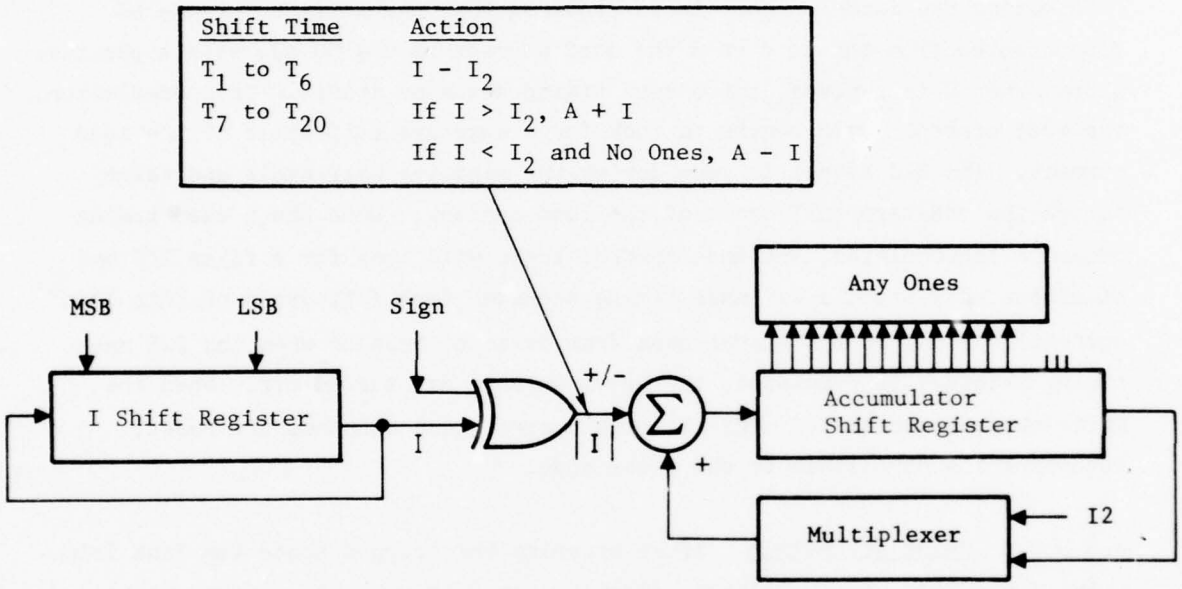


Figure 14. Digital Filter

The I register (6 bits in length) continuously recirculates for the entire 20 bit cycle. The first 6 bit times after the load (T_1 - T_6) are used to subtract I_2 from I. If, at T_6, the carry logic is zero then $I < I_2$ and subtraction for the next 14 bit times may be in order. The value of the Accumulator is checked for 1s in the 11 most significant bits. If the Accumulator contains a value larger than 2^3 in the upper bits positions) the I value is subtracted from the Accumulator and the result put in the Accumulator during bit times 7 through 20. The subtraction process allows the Accumulator to decay to a near zero level if an overload occurs and then disappears.

If, at the end of T_6, the carry logic is true, the $I \geq I_2$ addition is in order, and I, plus the Accumulator contents are stored in the Accumulator. If at the end of T_{20}, the carry logic is true, then the Accumulator has overflowed and the trip sequence is started. The results of the 20 bit shift in a 6 bit shift register are not to be used during the last 8 bit times and the odd shift pulses do not upset the computations.

4.5.2.4 Status

The Status mechanization uses both linear and digital techniques in the Monolithic. The VSO input is used as representative of the load voltage and is compared with the line voltage to indicate that a full wave of voltage is applied to the load. The VSO input is applied to the input of a Comparator circuit (see Figure 12) that employs hysteresis. When Output S is high (+12 V), VSO must go to -5 V before S will be low (0 V). When S is low, VSO must go to +5 V before S is high. The S term thus provides a square wave at the line voltage frequency. A phase relationship between ZVC and S is provided because ZVC switches at zero line voltage and S switches at near peak load voltage.

The phase relationship between ZVC and S is used to verify that both half cycles of the load voltage are present and are at the proper amplitude. The Status logic compares the S term with ZVC. If S is always true (high) when ZVC goes from high to low and S is always false (low) when ZVC goes from low to high, then full wave power is applied to the load and the Status output (STAOT) will be true. If S does not toggle due to improper load voltage amplitude or half cycling of the load voltage, the Status output will be false. Note that the Status output is in no way related to the Control Input command or the mode control. Therefore a shorted switch or a failure of the ac output to switch will be indicated by the state of the Status output with respect to the Control Input command. This provides a form of built-in diagnostic testing.

4.5.2.5 Zero Current Crossing (ZIC)

The VS2 (STATI) input, a voltage that is proportional to instantaneous load current, is amplified with the chopped stabilized X20 Amplifier and the result is compared to a reference. The reference changes in value with the results of the comparison (See Figure 12). When the output (ZIC) is 0 V (logic zero), the input (VS2) must go more negative than -16 mV before the output will switch to positive 12 V (logic 1). When the output is at +12 V (logic 1) the input must go more positive than -15 mV before the output will switch back to 0 V (logic 0). The ZIC term is used in the control logic as a condition for turn off of the pass elements for ac power control.

4.6 Switch Drive Circuit

The SSPC uses a JFET across the SCR gate to cathode to provide a low resistance path for SCR leakage when the SCRs are off, preventing inadvertent turn on at high temperatures. Since the JFETs are off when gate drive is applied, the power loss is small.

A 50 kHz pulse train (or 50 percent duty cycle) from the Monolithic provides gate drive at 50 percent of the power required by dc drive methods.

4.6.1 Monolithic Drive Output

The drive signals from the Monolithic are complementary 50 kHz rectangular outputs when enabled, each having a capability of 3 mA peak. Refer to Figure 15. It must be established that there is enough gain in the 2N2222A transistors to sink the worst-case transformer primary currents and still remain in saturation.

Worst-case analysis of the 2N2222A, including total dose effects, neutron effects, and a temperature of -55°C, show the degraded gain to be β = 26.0. This would allow a maximum collector current of:

$$I_C = \beta I_B = 26.0\ (3\ mA) = 78.0\ mA$$

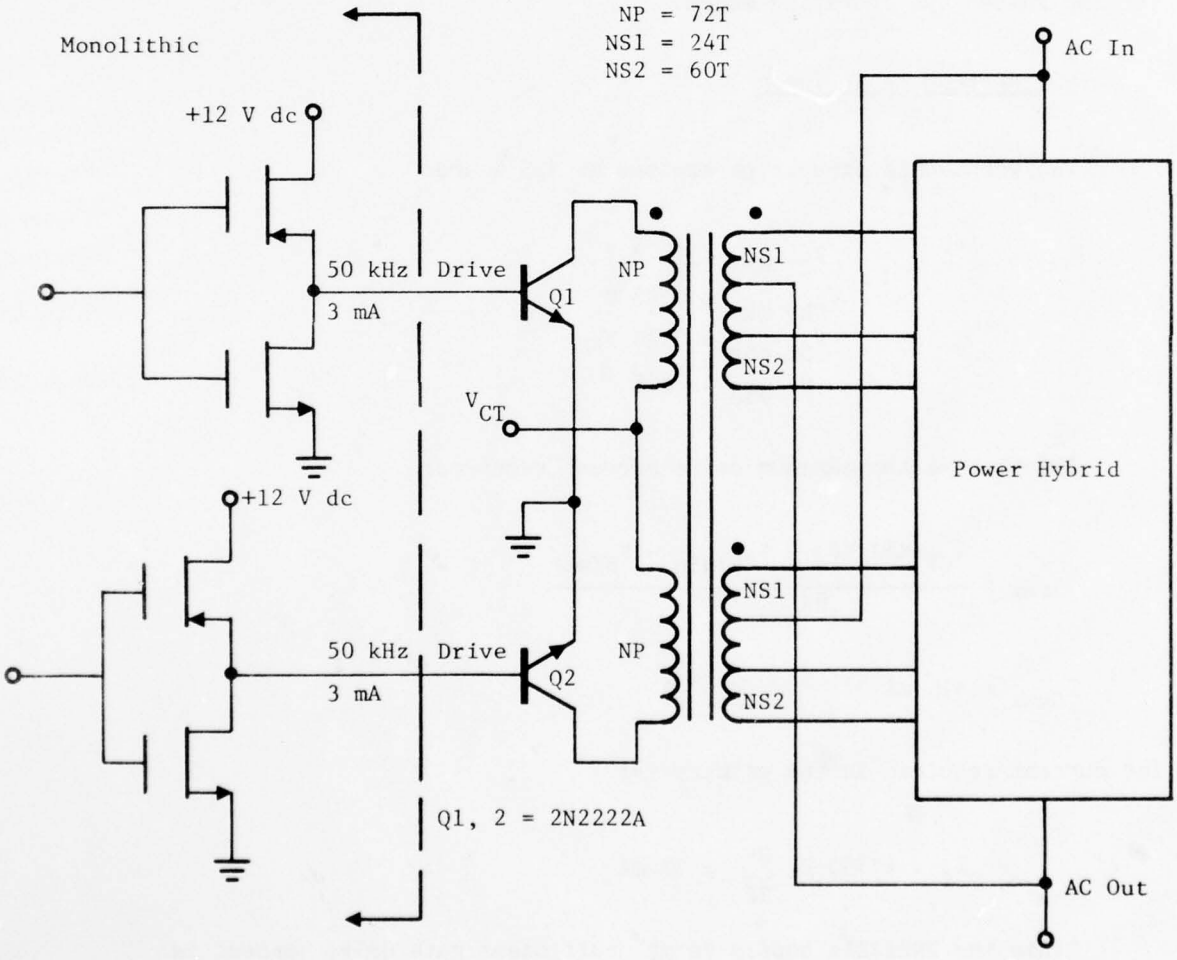


Figure 15. Monolithic Drive Output

Worst-case collector currents (see next section for gate drive requirements) were calculated to be 77 mA, indicating that drive would be maintained.

4.6.1.1 SCR Gate Drive Currents

The drive currents to the SCR switches must be sufficient to turn the switches on over a wide range of operating conditions (see Figure 16). Operation at 125 °C with worst-case circuit parameters and at -55 °C after exposure to neutron radiation are the two limiting conditions. The analysis below will show that the required amount of gate drive current is available for the latter two operating modes.

Switch Turn on at 125 °C

The worst-case circuit parameters at 125 °C are:

$$V_{CT\ max} = 12.3\ V$$
$$V_{CR1\ min} = 0.58\ V$$
$$V_{GK\ min} = 0.34\ V$$
$$R1_{min} = 28.5\ \Omega$$

Calculating the maximum drive current required:

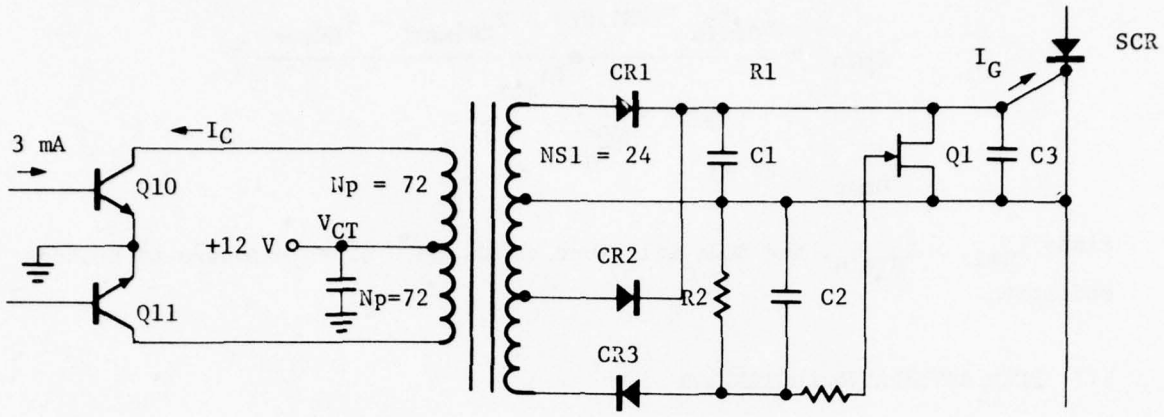
$$I_{Gmax} = \frac{V_{CT}(NS1/NP) - V_{CR1min} - V_{GKmin}}{R1_{min}}$$

$$I_{Gmax} = 115\ mA$$

The current required in the primary is:

$$I_P = (115)\ 2\ \frac{24}{72} = 77\ mA$$

Since the 2N2222As supply 78 mA, sufficient gate drive current is available at 125 °C and worst-case circuit parameters.



R1 = 30 Ω ± 5% CR1, CR2, CR3 = 1N4150 C3 = 0.01 μF ± 10%

R2 = 12 K ± 5% C1 = 0.1 μF ± 10% Q1 = E107 JFET

R3 = 120 Ω ± 5% C2 = 3300 pF ± 10% Q9, Q10 = 2N2222

Figure 16. 1/2 SCR Gate Drive Circuit

Switch Turn On at -55°C

The worst-case circuit parameters are:

V_{CTmin} = 11.1 V

V_{CR1max} = 1.0 V

V_{GKmax} = 1.3 V after exposure to neutron radiation

$R1_{max}$ = 31.5 Ω

I_{GTmin} = 35 mA

The minimum drive current available is:

$$I_{Gmin} = \frac{V_{R1min}}{R1_{max}}$$

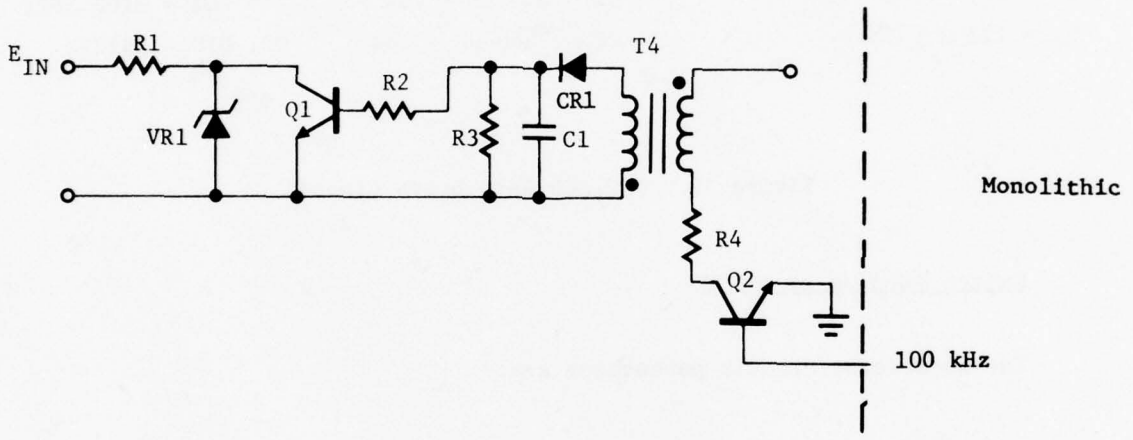
$$I_{Gmin} = \frac{V_{CTmin} \quad (NS1/NP) - V_{CR1max} - V_{GKmax}}{R1_{max}}$$

$$I_{Gmin} = 47 \text{ mA}$$

Since $I_{Gmin} > I_{GTmin}$, the SCRs will turn on at -55 °C after exposure to neutron radiation.

4.7 Trip and Status Indication

The Trip and Status indicators are mechanized with identical circuits:



R1 = 120 Ω ± 5%
R2 = 1 K ± 1%
R3 = 10 K ± 1%
R4 = 1.5 K ± 1%
C1 = 0.1 μF ± 10%
CR1 = 1N4153
Q1,2 = 2N2222A
VR1 = 33V

Figure 17. Trip or Status Indicator Circuit

When the SSPC is On and the Trip or Status input is interrogated with $\leq$ 10 mA, E_{in} must be $\leq$ 1.5 V dc; when OFF, I_{in} must be $\leq$ 0.1 mA at $\leq$ 30 V dc.

The question to be answered: does Q1 have the capability to sink 10 mA with a maximum E_{in} of 1.5 V? The functional question is: does T4 have the capability to couple enough energy to C1 to maintain sufficient current, I_{BQ1}, to keep Q1 on? An equivalent circuit is shown in Figure 18.

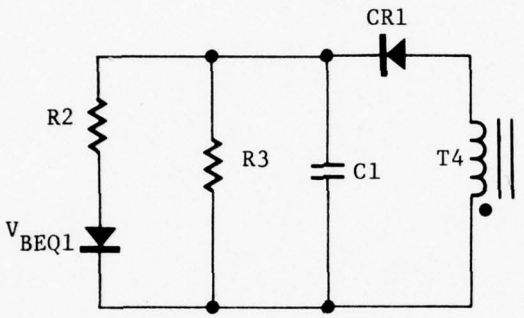


Figure 18. Trip or Status Indicator - Equivalent Circuit

To maintain I_{CQ1} = 10 mA, I_{BQ1} should be $\geq$0.4 mA; use 1.0 mA. Therefore, VR2 min $\simeq$ (1 mA) (1.0 K) = 1.0 V. Assuming C1 can be charged to some value like (1.0 V + V_{BEQ1}), the h_{ie} of transistor Q1 will dictate the discharge time constant, where h_{ie} = 500 Ω. The equivalent resistance is:

$$R_{eq} = R_{2min} + h_{ie} \text{ in parallel with } R_{3min}$$

$$R_{eq} = 990 + \frac{500}{9900} = 1.295 \text{ K}$$

$$V_{Cmin} = 1.0 \text{ V} + V_{BEQ1\ max} \simeq 1.7 \text{ V}$$

$$V_{C(b)} = V_{C(t)} = V_1 e^{\frac{-t}{R_{eq}C}}$$

where $R_{eq}\ C = 1.66 \times 10^{-4}$ sec

Assuming a short flyback discharge and a maximum period time

$$t = 10\ \mu\text{sec and } V_1 = 1.852 \text{ V}$$

The delta energy (ΔE_{C1}) is the minimum energy that transformer T_4 has to supply:

$$\Delta E_{C1} = \frac{V_1^2 - V_{Cmin}^2}{2} = 2.43 \times 10^{-8} \text{ Joules}$$

$$\text{If } I_{Lmin} = \frac{11.4 \text{ V min}}{R4 \text{ max}} [i - e^{t/\tau}]$$

where

$$R4 \text{ max} = 1.485 \text{ K}$$

$$t = 5 \text{ } \mu\text{sec}$$

$$\tau = \frac{L}{R4}$$

then

$$I_{Lmin} = 7.67 \text{ mA.}$$

Therefore, the energy E_{T4}, supplied by transformer T_4 is:

$$E_{T4} = 1/2 \text{ } Li^2 = 2.94 \times 10^{-8} \text{ Joules}$$

Since $E_{T4} > \Delta E_{C1}$, the voltage on C1 will be maintained.

The number of cycles to charge C1 to 1.852 V is:

$$N = \frac{1.543 \times 10^{-7}}{2.94 \times 10^{-8} - 2.43 \times 10^{-8}} = 30 \text{ cycles}$$

4.8 Zero Voltage Crossing Detector (ZVC)

The zero voltage crossing detector provides the proper timing to the Monolithic for the SSPC turn on sequence. The circuit shown in Figure 19 is used as the ZVC detector.

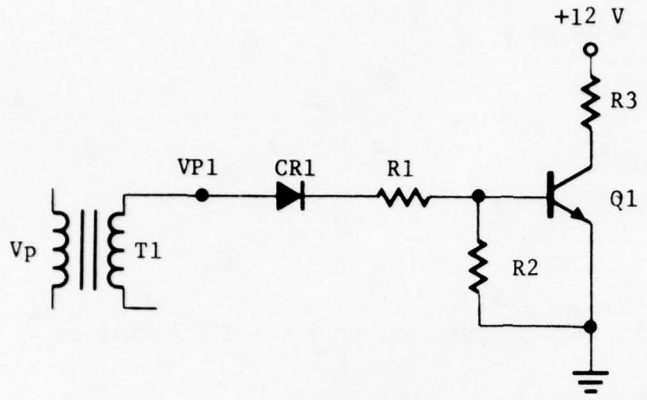


Figure 19. Zero Voltage Detector Circuit

The timing is to be such that turn on of the SSPC must be within ±32 V of the actual zero crossing. The equivalent time from zero crossing is

$$v(t) = V_p \sin 2\pi f$$

where

V_p = line voltage = 160 to 300 V rms

f = 400 ± 22 Hz

Solving for t, the worst-case condition is at 300 V ac and f = 422 Hz. Therefore, t = 28 μsec minimum.

The voltage V_{P1} is 180 deg out of phase with the line voltage. Thus, as a positive V_{P1} approaches zero, transistor Q1 will turn OFF, ZVC will go high, anticipating the positive going zero crossing of the line voltage. The time required to produce ZVC for a 300 V line voltage is:

$$t_{ZVC} = \frac{1}{\omega_{max}} \sin^{-1} \left[\frac{R1_{min} + R2_{max}}{R2_{max} V_{P1\ max}} (V_{BEQ1\ min}) \right]$$

where

$\omega_{max} = 844\ \pi$

$V_{P1max} = 30.09 - 0.4 = 29.69$ V

$R1_{min} = 5049\ \Omega$

$R2_{max} = 5151\ \Omega$

$V_{BEQ1min} = 0.35$ V at 125°C

$V_{CC1min} = 0.4$ V at 125°C

$t_{ZVC} = 8.8$ µsec

The time required by the SSPC to turn on, once the ZVC signal is received is

$$t_{on} = t_d + t_{off} + t_{SCR}$$

where

t_d = maximum decision time for the Monolithic

$t_d = 11.11$ µsec (one clock cycle)

t_{off} = time to turn gate to cathode JFET off

t_{SCR} = turn on time of the SCR

$t_{off} + t_{SCR} = 5.55$ µsec maximum

This makes the maximum turn on time after receiving ZVC

$$t_{on} = 11.11 + 5.55 = 16.66\ \mu sec$$

The SSPC turn on time will occur at

$$t = 16.66 - 8.8 = 7.86\ \mu sec$$

This time represents a voltage of +8.8 V, well inside the ±32 V requirement. Calculations for SSPC turn on for a 160 V line indicate turn on at 0.82 µsec after zero crossing, well within requirements. For the case where t_{ZVC} is at maximum and t_{on} a minimum, the SSPC anticipates the line voltage zero crossing by 22 V, again within requirements.

4.9 SSPC Voltage Drop

The worst-case voltage drop across the SSPC power switch section is limited to 2.2 V rms. The voltage drop is required to include the resistance of the interconnections to the SSPCA interface. The maximum drop occurs at 125°C:

$$V = I_{RMS} [4 \text{ (R connectors)} + 2 \text{ R wire} + \text{R fuse} + \text{R sense}] \text{ max} + V_{SCR}$$

where the maximums are:

R connectors = 0.0338 Ω
R wire = 0.101 Ω (interface to SSPC connector)
R fuse = 0.113 Ω
R sense = 0.2306 Ω
$V_{SCR\ max}$ = 0.915 (pre-neutron)
V = 2.15 V (pre-neutron) and 2.54 V (post-neutron)

The SSPC voltage drop is less than 2.2 V for normal worst-case operating conditions, but is exceeded by 0.34 V after exposure to neutron radiation. However, the switch will continue to operate within all other specified requirements.

4.10 Fuse

The B-1 Aircraft specification requires that each SSPC contain the fail-safe feature of a fuse in the event that the trip circuit fails to perform its intended function during an overload condition. The fuse is required to open within the limits shown in Figure 20 and cannot be a source of ignition, show mechanical failure, or become a source of debris. Additional performance requirements are:

1) Voltage: 160 to 300 V rms, 400 Hz
2) Temperature: -55 to 100°C

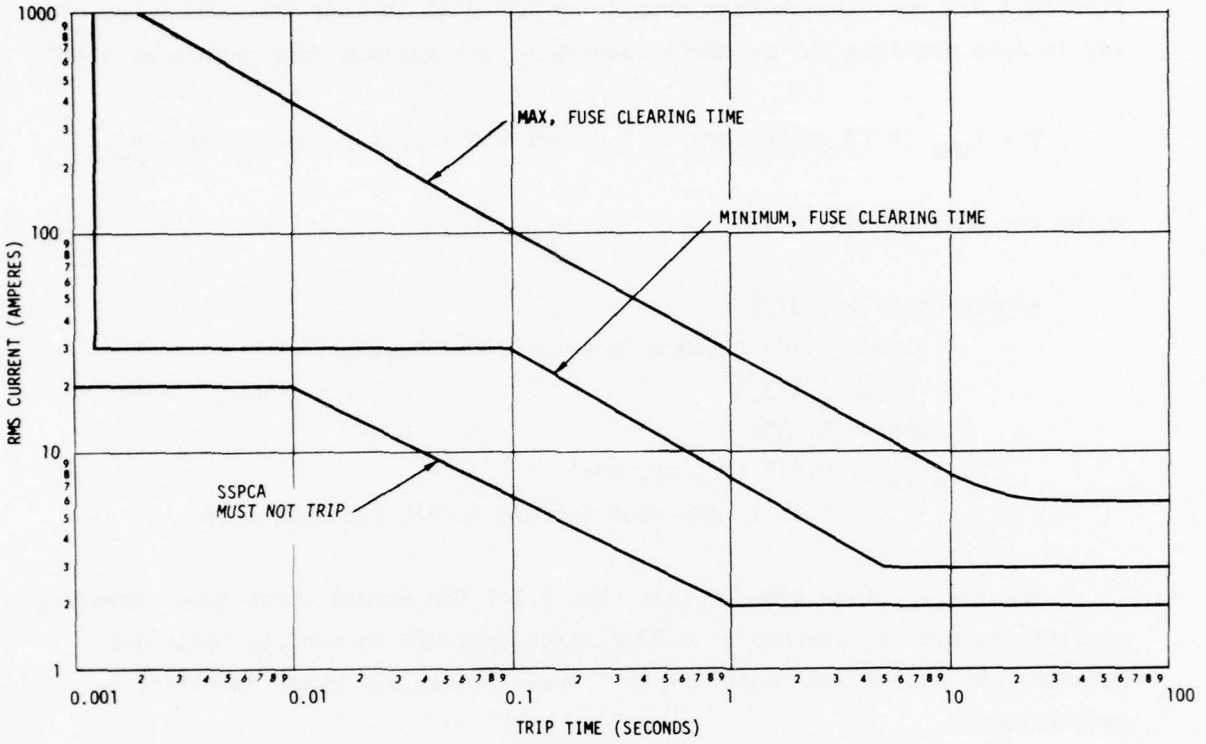


Figure 20. Fuse Current Time Requirements

4.10.1 Fuse Development

When the fuse development effort was initiated, surveys indicated that a fuse with the particular current clearing time (or opening time) required was not available. It was further noted that previous work on developing fuses for a similar application and similar requirements had been unsuccessful.

As can be seen in Figure 21, developing a fuse to the B-1 SSPC requirements requires an increase in the slope of a conventional fuse.

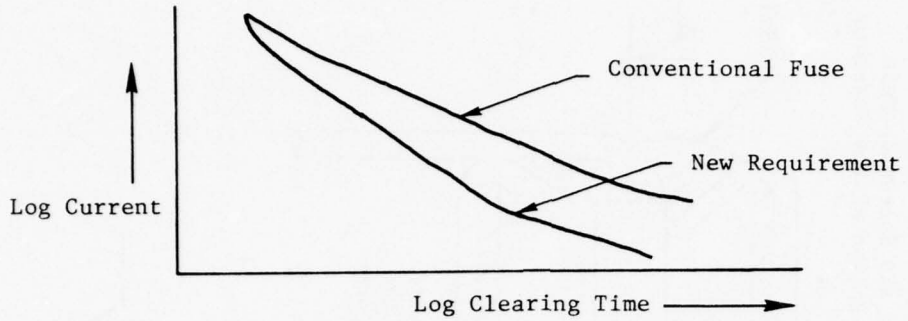


Figure 21. Fuse Slope Characteristics

The reason for the shallowness of the slope of the conventional fuse curve is that sand, which is used to quench the arc at high currents, serves as a good heat conductor and slows down the fuse clearing time at low currents since it expedites heat removal from the fuse element and prevents its reaching fusion temperatures.

The fuse concept described here is a dual-element fuse which physically separates the fuse element sections which control fuse clearing times at different current ranges, e.g., the high current controlling section of the fuse is isolated and surrounded by an appropriate filler such as sand to quench the arcing which is symptomatic of high current fuse blowing. The low current controlling section of the fuse which is heavily affected by the heat conductivity of its environment would also be isolated and surrounded by a suitably conducting substance, see Figure 22.

If the low current clearing times need to be speeded up, the surrounding material could be a gas such as air which would minimize heat loss. More of the electrical energy converted into heat would be retained and used to heat and melt the fuse element thus speeding up the time for the fuse to clear.

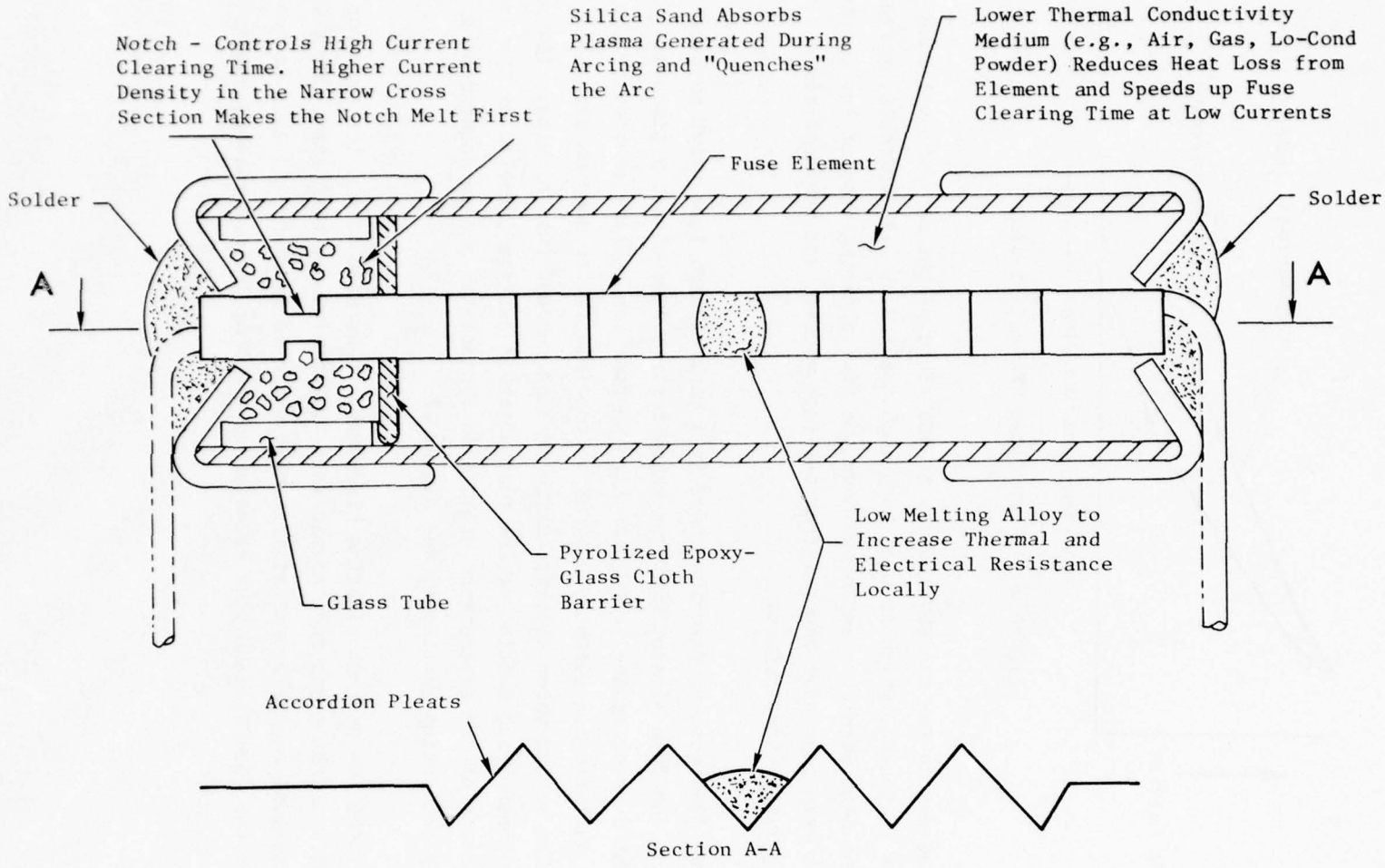


Figure 22. Autonetics Fuse Construction

Other design features which contribute toward a steeper log current-log clearing time curve are as follows:

1) Pleated Fuse Element - Pleating permits a greater length of element to be positioned within the fuse chamber. This is advantageous because at low currents, the hottest area of the fuse element is at the middle section of its length because it is the farthest removed from the end caps which act as cooling heat sinks. Lengthening the fuse element increases the path length and resistance for heat to flow from the hot areas to the heat sinks.

2) Fusible (Tin) Alloy on Element - A few (approximately 12) milligrams of 95 percent tin, 5 percent silver alloy were fused in the middle area of the fuse element length. It was discovered experimentally during the program that this expedited the fusion time at low currents. It is hypothesized that the heating rate is increased in regions where tin-silver has diffused into the copper because in these regions the electrical resistivity has increased, and the thermal conductivity has decreased. The melting range is also lowered because of the tin diffusion.

3) Absence of Organic Materials - Organic materials, i.e., resins in contact with the fuse element, were found to have a drastic cooling effect. The mechanism was thought to be pyrolysis of the resins. This physiochemical phenomenon absorbs large amounts of energy and also produces gases, which on mixing with air already present inside the fuse, are combustible. Combustion of such gas-air mixtures during fuse testing produced destruction of the fuse enclosure when organic materials (e.g., adhesives) were used in construction of the fuse such that they contacted the fuse element. Ignition of the gas-air mixtures was thought to be initiated by heat from the melting fuse element.

4) Tension in the Fuse Element - At medium and high currents, rupturing of the fuse element occurs violently, and enough of the element is destroyed to remove the possibility of the remaining fuse segments reuniting and reestablishing electrical continuity. At low currents (e.g., 5 A for the Rockwell International designed fuse), heating to fusion is slower, and rupturing is not catastrophic so that there is a possibility that the fuse element segments can reunite, particularly if the pleated fuse element is in compression before rupturing.

Reuniting of the element by the fuse segments coming together has even worse consequences if it happens that the element area containing the fused tin-silver alloy is bypassed, as shown in Figure 23.

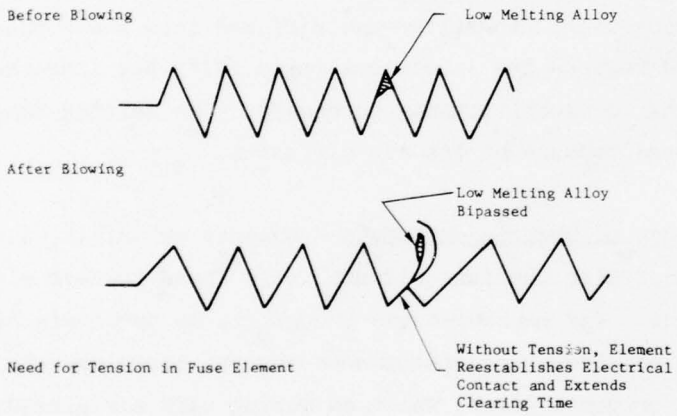


Figure 23. Requirements for Tension in Fuse

The new element thus formed will not readily rupture upon electrical heating because pure copper without the fused tin-silver will stubbornly stay together and require much greater energy (i.e., current-time) to rupture. To avoid reuniting of fuse segments after rupturing at low electrical currents, the pleated element is installed in tension so that there will be a force pulling the element segments apart.

Sufficient tension in the pleated element will only occur if the element is constructed from foil which has been cold rolled to a spring hardness temper.

5) Operation at -55°C - As the fuse is operated at lower currents and more time to clear is necessary (e g., 5 A), a greater amount of heat is lost to the surroundings. This heat loss is particularly severe if the fuse is operated at -55°C. In short, at low temperatures and low currents, the fuse tends to be slow in clearing. To overcome this problem, several insulative materials were tried over the fuse. Ultimately, it was demonstrated that a foamed sleeve (i.e., a shrinkable polyolefin foam sleeve) shrunk over the fuse, minimized heat loss and permitted the fuse to clear well within the specified requirements.

4.10.2 Fuse Manufacture and Test

Several fuse manufacturers were contacted for participation in the fuse development effort. Ultimately, the group dwindled to one company, Bussman Manufacturing, which continued cooperating with Rockwell International throughout the development cycle.

Fuses developed by Rockwell International and manufactured by Bussman were tested. Figure 24 shows the test results.

4.11 SSPC Packaging

Four electrically independent, repairable SSPC circuits are mounted on a four-layer printed circuit board plug-in module. The module has externally mounted aluminum rails for cooling components. The ends of the rails are also used for securing the module to the SSPCA heat exchanger as shown in Figure 25. All modules use MIL-C-55302 connectors.

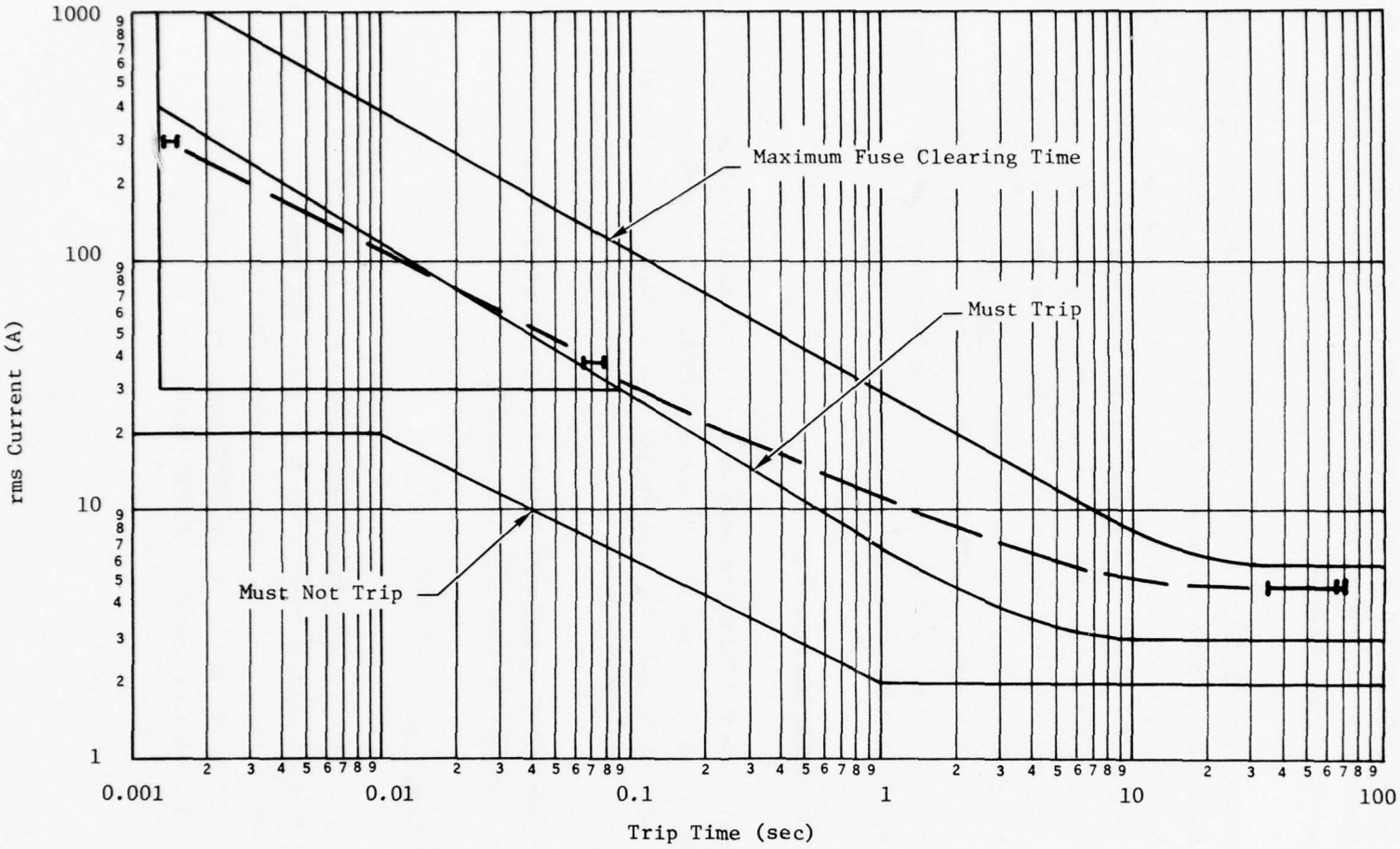


Figure 24. Autonetics Design Manufactured by Bussman,

5 Fuses at Each Current

⊢⊣ Indicates Fuse Clearing Time vs Current

4.11.1 Dielectric Withstanding Voltage (DWV)

The DWV test level at an altitude of 70,000 ft is 800 V rms for 230 V ac conductors and 200 V rms for non-230 V ac conductors. For the SSPC module, the ability to withstand these voltage levels is achieved by separating the conductors from each other. In the SSPC module connector, the non-230 V pins are grouped together (100 mil separation) and segregated from the 230 V pins. The metal-to-metal distance between the 230 V pins and the non-230 V pins is 335 mils (three intermediate pins are removed from the connector).

The metal-to-metal distance between 230 V pins is 234 mils.

4.11.2 Rupture Capacity

The B-1 Aircraft specification requires the SSPC to be tested for rupture capacity with a minimum source resistance of 0.62 ohms (248 V rms/400 A). The minimum resistance of an SSPC = 0.418 ohms. Therefore, the applied rupture current = 248/1.038 = 239 A maximum. The maximum time required for the SSPC to turn off in an overcurrent condition is 1.25 msec. The minimum cross section of copper for a current of 239 A and 1.25 msec is 47 square mils. The cross sectional area for the fusing currents from input to output on the SSPC module is:

1) AC Input: Four module connector pins in parallel are used to bring in the power for the four SSPCs on the module. The fusing current for one pin at 2.5 msec was tested to be 350 A.

2) Printed Wiring Board (PWB): The minimum cross section of the plated copper wiring is 243 square mils.

3) PWB Feedthroughs: The feedthroughs consist of a copper barrel with a 1 mil minimum thickness and a diameter of 33 mils = 207 square mils - however, the barrel is filled with the component leads and solder. Thus, the equivalent conductive cross section is greater than 250 square mils.

4) Power Hybrid: The Power Hybrid package passes a 600 A peak pulse without opening.

5) Sense Resistor: The energy applied to the 0.226 ohm sense resistor for a 1.25 msec surge is 16 W sec. The resistance versus energy chart for the selected resistor indicates that a 5 W resistor will handle the surge. The resistor selected is rated at 7 W.

6) Fuse: The fuse will open at 350 A, 1.25 msec current pulse (refer to Figure 24).

7) Output Pin: One pin is used to conduct the current.

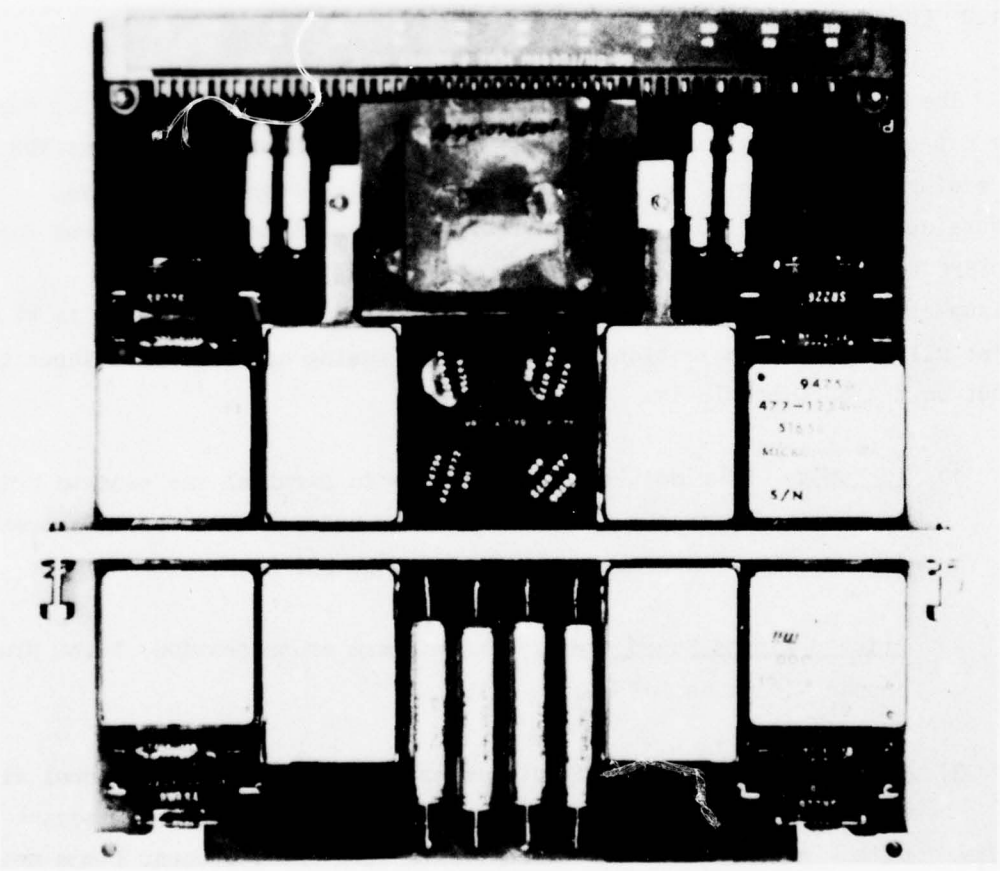


Figure 25. AC Switch Module

Based on the test and analysis of the current path through the SSPC, the latter is expected to pass the imposed rupture current of 239 A rms.

4.12 SSPC Performance Summary

A summary of the SSPC performance parameters is listed below.

Steady State Output	2 A at 230 V, 400 Hz 200 mA at 325 V dc Normally Open or Normally Closed	
Voltage Drop	$\leq$2.2 V rms at 2 A	
Leakage Current	$\leq$2 mA at 75 °C	
DC Offset	$\leq$0.2 V at 2 A	
Voltage Turn-On	0 $\pm$ 32 V	Full Cycle Control
Current Turn-Off	0 $\pm$ 50 mA	Full Cycle Control
Turn On - Turn Off Delay	> 4 msec $\leq$ 10 msec	
Control Input	$\leq$ 3.3 mA at 6 V dc	
Power Dissipation	$\leq$ 2.2 W at I_L = 0 $\leq$ 5.5 W at I_L = 2 A	
Status/Trip	ON: $\leq$ 10 mA at $\leq$ 1.5 V dc OFF: $\leq$ 0.1 mA at 30 Vdc	
Rupture Capability	600 A - Peak	

4.13 SSPC Design - Problems and Solutions

The primary problem in the development of the SSPC was the design and fabrication of the large scale integrated circuit or Monolithic. The Monolithic circuit problems will be discussed in detail. However, a number of secondary problems were also solved in the SSPC design cycle:

1) Minimum SSPC power dissipation was achieved by:
   a) Using 50 kHz rather than dc for SCR gate drive
   b) Providing regulated voltages with a 78 percent efficient PWM power supply
   c) Using low power CMOS for the control element
2) Minimum volume was achieved by mechanizing the potentially space consuming timing and control functions in the 0.180 x 0.140 in. Monolithic chip and using optimally packaged dual SCR chips as the major switch element. This permitted the packaging of the control and switch sections as hybrids.

3) Further reductions in volume were made possible by using printed circuit boards for component wiring and interconnection. This required the extension of printed circuit technology into the area of high currents and voltages. Two ounce copper (2.7 mils thick) of appropriate widths (90 mil for the 2 A lines) were used for the circuit interconnections.

   The required level of DWV was achieved by separating the high voltage pins at the module connector.

4) The unique Threshold Detector circuit design was the solution to the problem posed by EMUX command signal constraints, i.e., minimum available current (3.3 mA), tight threshold (OFF: 0 to 2 V, ON: 3 to 6 V) wide temperature range (-55 to 125°C).

5) The flyback transformer coupled circuits (Control, Trip, Status) provided electrical ground isolation from the 230 V line with minimum power dissipation.

6) A two-section fuse was designed to meet the SSPC fail-safe requirements when a fuse with the required clearing time was not available.

4.14 Monolithic Development Problems and Solutions

Large scale integrated circuits concentrate complex circuitry into a very small area. As a rule, their development usually requires the solution of many problems during the early part of the design and fabrication cycle. The Monolithic was no exception. The problems and their solutions are listed in the following paragraphs.

4.14.1 Original Design

	Problem	Solution
1)	Race condition in Up/Down Counter	Logic change
2)	Sign bit incorrect	Logic change
3)	FET type in SIC amplifier incorrect	Change P FET to N FET
4)	Metallization crossover breakdown	Increase oxide thickness

4.14.2 First Design Iteration

	Problem	Solution
1)	ZIC gain bandwidth	Feedback resistor value change
2)	SCR gate drive overlays	Added logic delay to rise time
3)	Oxide breakdown	Increase nitride passivation layer thickness

4.14.3 Second Design Iteration

	Problem	Solution
1)	Low ZIC threshold	Change comparator threshold
2)	ZIC "Jitter"	Restabilize comparator
3)	ZIC triggers on noise	Add hysteresis and change drive transistors in Control Hybrid
4)	SCR drive overlap	Add logic delay to fall time
5)	V_{SO}, should be RMS, is peak	Change voltage sense resistor values
6)	Clock overlap - N FET overstress	Add logic delays

SECTION V

HYBRID DESIGN

5.0 SSPC Hybrid Design

5.1 Design Objective

The objective of the SSPC Hybrid Design was to provide power control circuitry in the minimum space practical, in order to conserve weight and volume. This section of the report describes the general configuration and operation. The problems encountered and the solutions incorporated are also discussed.

5.2 Control Hybrid

5.2.1 General Description

Figure 26 illustrates, in block diagram form, the Control Hybrid circuit and its relationship within a complete SSPC. Figure 27 shows the Hybrid circuit in schematic form. The circuit performs an interface/control function between a centralized control unit (EMUX) and the SSPC power hybrid that provides 230 V ac, 400 Hz power to aircraft loads. The Control Hybrid contains a power supply, zero voltage crossing detection circuitry, a timing/control monolithic integrated circuit, and various interface circuitry (Control, Status, and Trip). The circuit is mechanized with 90 parts. Nominal Control Hybrid power dissipation is 0.7 W.

5.2.2 Detail Description

5.2.2.1 Power Supply

AC voltage (+35 V peak maximum) is supplied by an external transformer to pins 2 and 3. A pulse-width modulated power supply converts the ac to ±12 V dc. The ±12 V dc is used to: (1) generate the +9 V reference power supply and (2) supply power to the Monolithic.

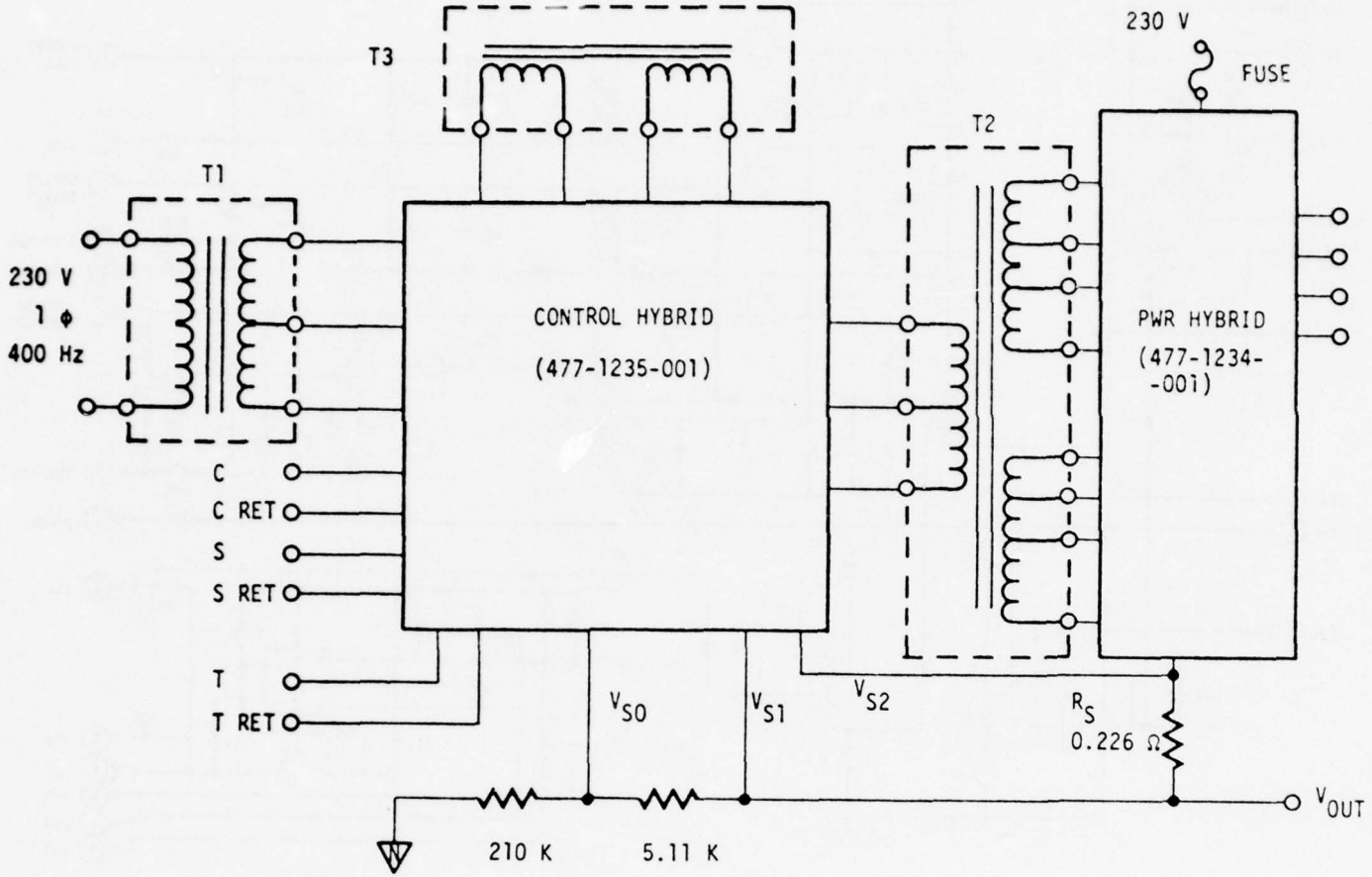


Figure 26. Simplified SSPC Schematic

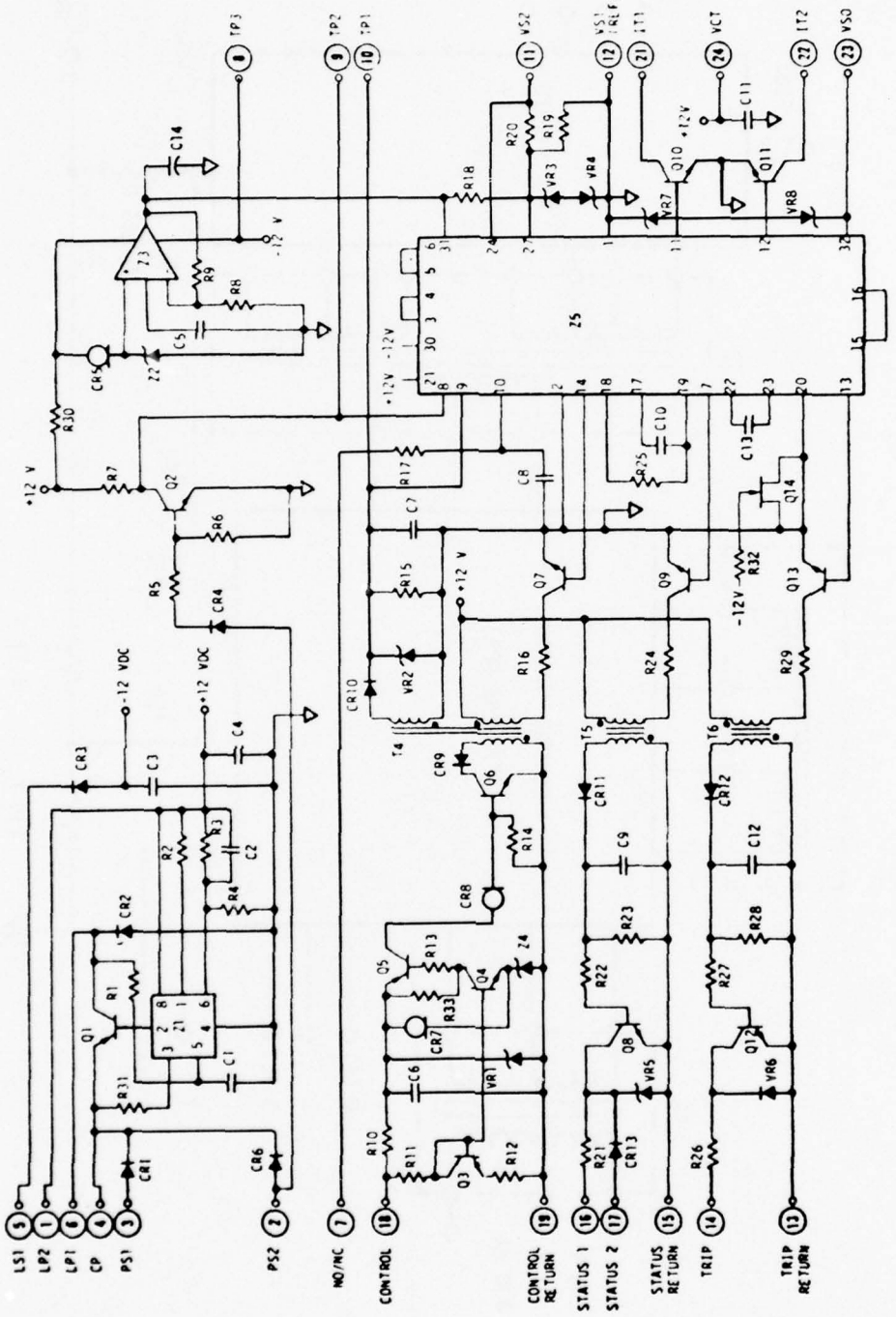


Figure 27. Control Hybrid Schematic

5.2.2.2 Zero Voltage Crossing Detection Circuit

This circuit consists of resistors R5, R6, and R7, transistor Q2, and diode CR4. Its function is to generate 400 pps in synchronization with the negative going zero crossings of the 230 V ac, 400 Hz line. The pulses are used to turn on the SSPC at zero line voltage.

5.2.2.3 Monolithic

This integrated circuit (Z5) contains the major timing and control functions for the SSPC. A functional description of the Monolithic is presented in Section IV.

5.2.2.4 Control

The control circuit consists of resistors R10, R11, R12, R13, and R33, transistors Q3, Q4, Q5, and Q6, diodes CR7, CR8, and CR9, zener VR1, and transformer T4. A control signal of +3 to +6 V dc is received on pin 18 when the SSPC is turned on.

5.2.2.5 Status

The Status circuit consists of resistors R21, R22, and R23, capacitor C9, diode CR13, transistor Q8, zener VR4, and transformer T5. Once the SSPC has turned on, a Status indication must be generated. This is accomplished by coupling energy across T5 by turning Q9 on and off with 100 kHz pulses from the Monolithic, which turns on Q8.

5.2.2.6 Trip

The Trip circuit consists of resistors R26, R27, and R28, capacitor C12, diode CR12, zener VR6, and transformer T6. If a Trip indication is issued by the Monolithic, Q12 is turned on. Circuit operation is identical to the Status circuit.

5.2.3 Packaging

The Hybrid package is a maximum of 1.6 in. long, 1.12 in. wide and 0.35 in. thick and has a capacity of 28 pins. Thus, the unused pin space is used for spacing pins 13 through 19 a minimum of 0.2 in. from the rest of the pins, due to the possible 425 V transient between the two groups. A ceramic base material is used (rather than metal), also due to the previous reason.

The power dissipation of the Hybrid is a maximum of 0.7 W.

5.3 Power Hybrid

5.3.1 General Description

The Power Hybrid circuit is shown in schematic form in Figure 28. The circuit performs the ac switching function and is used to apply 230 V ac, 400 Hz to an aircraft load. The circuit consists of two high voltage, medium current SCRs, associated gate drive circuits and an RC snubber network. The Hybrid contains 28 components and has 12 interface pins. The maximum power dissipated in the circuit is 2.4 W.

5.3.2 Detail Description

5.3.2.1 SCR Switches

The two SCRs are connected in an inverse parallel configuration. When gated ON, the SCRs will conduct a steady-state current of 2.0 A *rms*. If the SCRs are conducting when a load fault occurs, peak currents as high as 28 A for 0.2 sec and as high as 600 A for 1.25 msec will be encountered. When the SCRs are OFF, the maximum instantaneous voltage between pins 8 and 10 is 509 V.

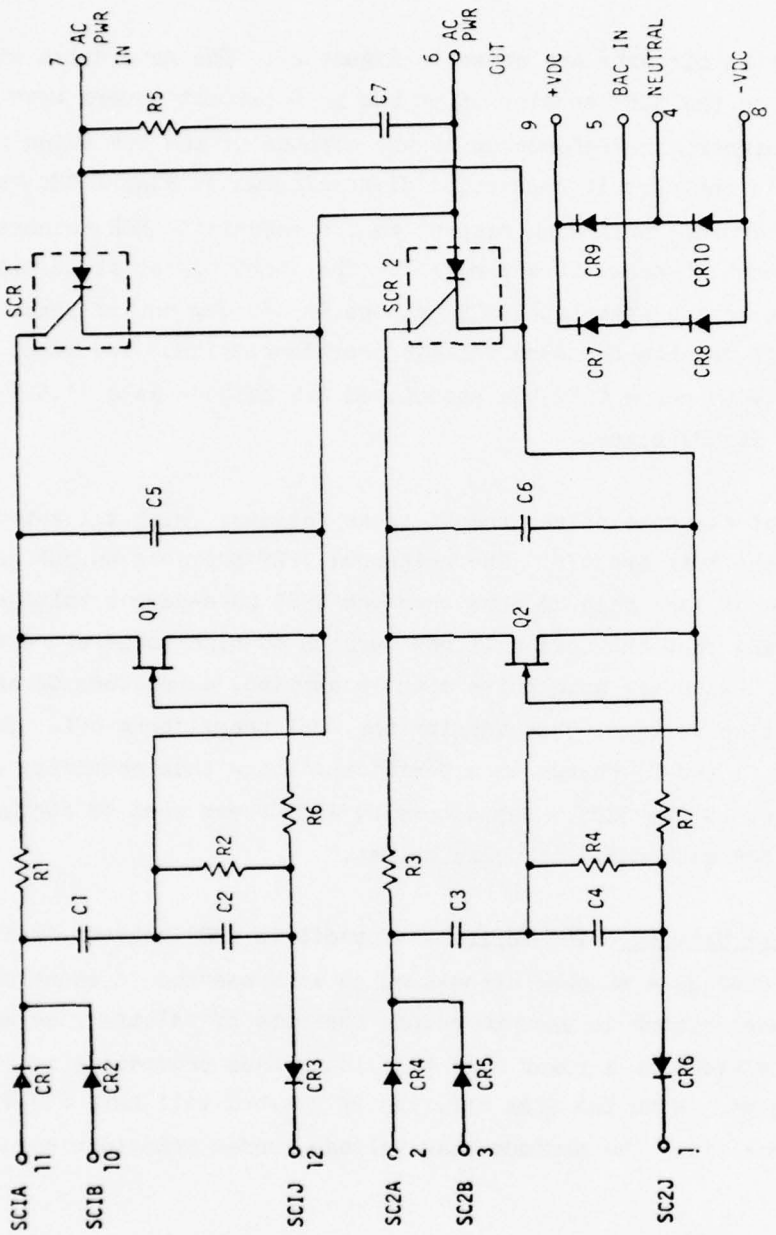


Figure 28. Power Hybrid Schematic

5.3.2.2 Gate Drive Circuit

The gate drive circuits are shown in Figure 28. The gate drive signals required to turn on the SCRs consist of 50 kHz ± 10 percent square wave voltages. All input signals are referenced to the cathode of the SCR being turned on as indicated in the circuit connection diagram shown in Figure 28. The input signal at terminal SCIA with respect to the associated SCR cathode is 3.8 V ± 5 percent, 0-peak, 50 kHz signal. The input signal at terminal SCIB with respect to the associated SCR cathode is 180 deg out of phase with the signal on SCIA and has the same voltage characteristics. The input signal at terminal SCIJ with respect to the associated SCR cathode is a 11.5 V ± 5 percent, 0-peak, 50 kHz signal.

Operation of the gate drive circuit is as follows: With all gate drive signals at 0 V, the SCRs are off. The n-channel JFET provides an SCR gate to cathode impedance of less than 20 ohms when the JFET gate-source voltage is zero, thus insuring that the SCRs will not turn on at high temperature due to leakage currents. With the gate drive signals applied, capacitors C2 and C4 charge to a negative voltage, thus turning the JFET transistors off. In addition, capacitors C1 and C3 charge to a positive voltage thus providing a dc gate drive current to the SCRs. Capacitors C5 and C6 are used to further desensitize the SCR gate nodes to noise spikes.

5.3.2.2.1 Snubber Network. The Resistive-Capacitive (RC) network consisting of R5 and C7 is used as a snubber circuit which is connected in shunt with the SCRs. The snubber network is used to reduce the rate of voltage rise across the switch in the event of a power line transient, thus preventing inadvertent turn-on of the SCRs. With the SCRs off, the RC network will have 230 V, 400 Hz impressed across it. The maximum peak voltage, under transient conditions, is 509 V.

5.3.2.2.2 Power Dissipation. Total power in the Hybrid is 2.4 W for a load current of 2 A. The junction-to-case thermal impedance for the SCRs is 2.0 °C/W. Both SCRs are mounted on a common 0.65 by 0.65 in., beryllia substrate manufactured by Unitrode.

5.3.3 Packaging

The packaging envelope is a maximum of 1.29 in. by 1.29 in. by 0.42 in. The pin spacing is 0.200 in. minimum except for pins 1 through 3 and 10 through 12, due to the high voltage requirements. The package was constructed with a ceramic base rather than a ceramic substrate on a metal base for high voltage breakdown considerations.

5.4 Logic Hybrid

The Logic Hybrid provides the circuitry required to mechanize logical combinations of control input commands to an SSPC.

A unique feature of the Logic Hybrid is that the only power supplied to each circuit is the power furnished by the EMUX input signal. This characteristic satisfies the B-1 Power Controller requirement that a failure in one PC circuit cannot cause a failure in another PC circuit, which would have been the case if a common, external power supply was used.

5.4.1 General Description

An SSPC logic circuit accepts two +4 to +6 V dc level commands from EMUX and provides a two-input "AND" logic output. Two isolated outputs corresponding to each input are also provided. These outputs can be connected together to provide the logical "OR" of the EMUX input commands. Equivalent outputs from other logic hybrids can also be connected to provide the necessary "OR" command. The Logic Hybrid provides these outputs while maintaining isolation between EMUX outputs. Only one output from each Hybrid can be used at any one time ($A \cdot B$ or $A + B$). The output is capable of driving one SSPC control input.

The input voltage is an EMUX +4 to +6 V dc level command. Only one logic circuit will be addressed since the two logic circuits are identical (see Figure 29). The logic A input circuit consisting of resistors R1, R2, R3, R4, transistors Q1, Q2, Q3, zener VR1, and diode CR1 controls the turn-on level. Current limiter, CR1, provides the bias current for the voltage reference, VR1. VR1 provides a temperature compensated voltage reference to insure that

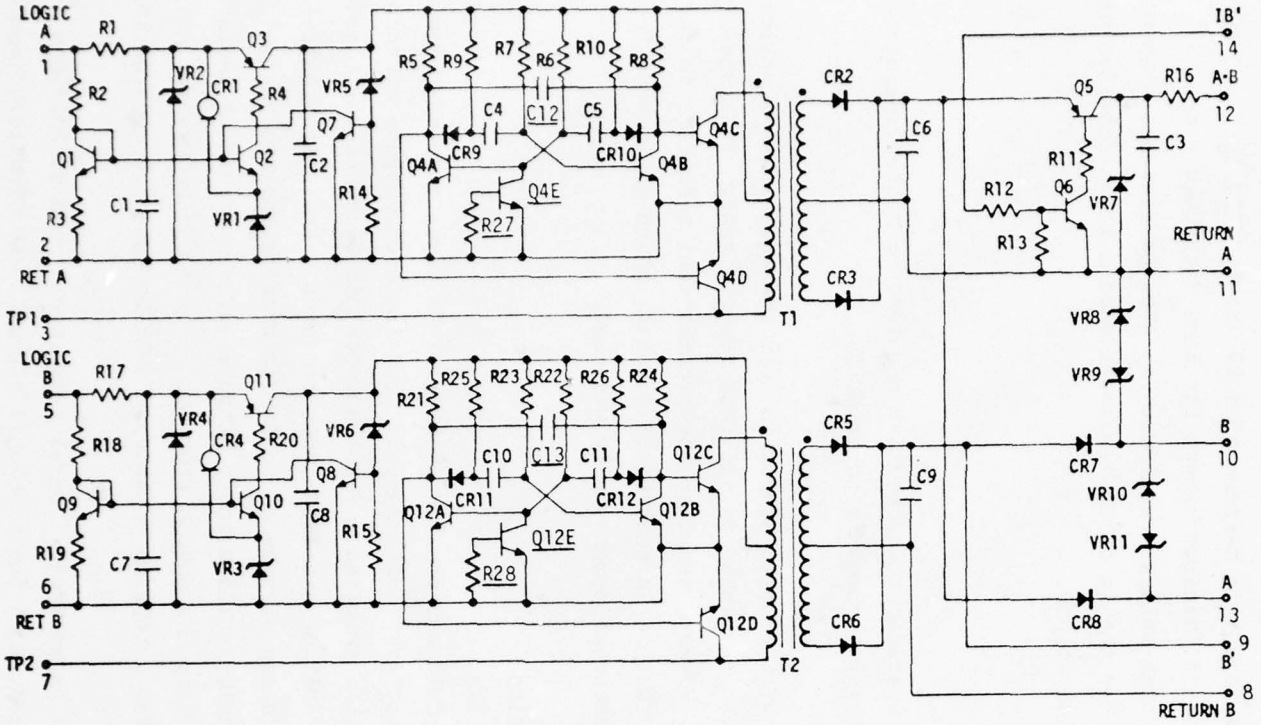


Figure 29. Logic Hybrid Schematic

the circuit will turn-on at an input voltage between +2 and +4 V dc. Transistor Q1 is diode connected to compensate for Q2 base-to-emitter voltage variations with temperature. When the dc input reaches a level sufficient to achieve turn-on, the oscillator consisting of R5 through R10, C4, C5, CR9, CR10, Q4A, and Q4B begins to oscillate. The frequency of oscillation is dependent upon the junction voltages of transistor array (Q4), capacitors C4 and C5, resistors R6 and R7, and the collector voltage of Q3. Nominally, the frequency is 200 kHz with a 50 percent duty cycle. The remaining resistors and diodes (R9, R10, CR9, CR10) provide a base current path for turn-on of transistors Q4A and Q4B. The collector waveforms of Q4A and Q4B have square edges because the base current is not supplied by R5 (or R8). Instead, the current flows through R9 and C4 (or R10 and C5).

The 200 kHz rectangular pulses are applied to the base of transistors Q4C and Q4D. These transistors drive transformer T1. The transformer couples the pulses to the output logic circuit.

The transformer center-tap voltage is clamped at approximately +4.1 V dc, set by VR5, R14, and Q7. The voltage equals the breakdown voltage of the zener (VR5) plus the base-to-emitter voltage of transistor Q7. Clamping the center-tap limits the output voltage to less than +6 V dc. Also, input current requirements are limited. The transformer primary voltage, therefore, is determined by the center tap voltage minus the transistor collector-to- emitter saturation voltage.

The output logic consists of R11, R12, R13, R16, CR7, CR8, Q5, and Q6. The rectified output from logic circuit A is used to deliver power for the "AND" A•B). This output is connected to the emitter of PNP switch Q5. Turn-on of Q5 is controlled by transistor Q6 which is turned on by logic circuit B. The "OR" (A + B) is provided by connecting the diode isolated outputs A and B together.

5.4.2 Packaging

The Logic Hybrid was packaged in a two piece 1.32 in. by 1.32 in. by 0.37 in. metal can. Pin spacing was 0.1 in., since voltages did not exceed 6 V. The power dissipation of the Hybrid is 0.12 W.

5.5 Status Hybrid

The Status Hybrid provides the circuitry required to open or close a solid state switch as a function of a dc input signal. Like the Logic Hybrid, each Status circuit operates from the power furnished by the input signal.

5.5.1 General Description

The Status Hybrid accepts a dc input voltage and provides two isolated output switches (Figure 30). The input voltage required for turn-on is +3 V with the maximum allowable input of +30 V. When the circuit is on, the outputs are capable of sinking 50 mA each. With input voltages less than +2 V, the outputs will appear as a high impedance, which corresponds to the circuit being off.

The input voltage can be either an EMUX +3 to +6 V dc level command or a +28 V dc input from an aircraft relay. The input circuit consisting of R1 through R4, and Q1, Q2, Q3, VR1 and CR1 controls the turn-on point. Current limiter, CR1, provides the bias current for voltage reference, VR1. VR1 provides a temperature compensated voltage reference to keep the circuit turn-on point at an input voltage between +2 and +3 V dc. Transistor Q1 is diode connected to compensate for the base-to-emitter voltage variations with temperature of transistor Q2. When the dc input reaches a level sufficient to achieve turn-on, the oscillator consisting of R6 through R11, and C4, C5, Q4A, and Q4B begins to oscillate. The frequency of oscillation is dependent upon the junction voltages of transistor array (Q4), capacitors C4 and C5, and resistors R7 and R8. Nominally, the frequency is 200 kHz with a 50 percent duty cycle. The remaining resistors and diodes (R10, R11, CR4, CR5) provide a base current path for turn-on of transistors Q4A and Q4B. The collector waveforms of Q4A and Q4B have square edges because the base current does not pass through R6 and C4 (or R9 and C5). Instead, the current passes through R10 and C4 (or R11 and C5).

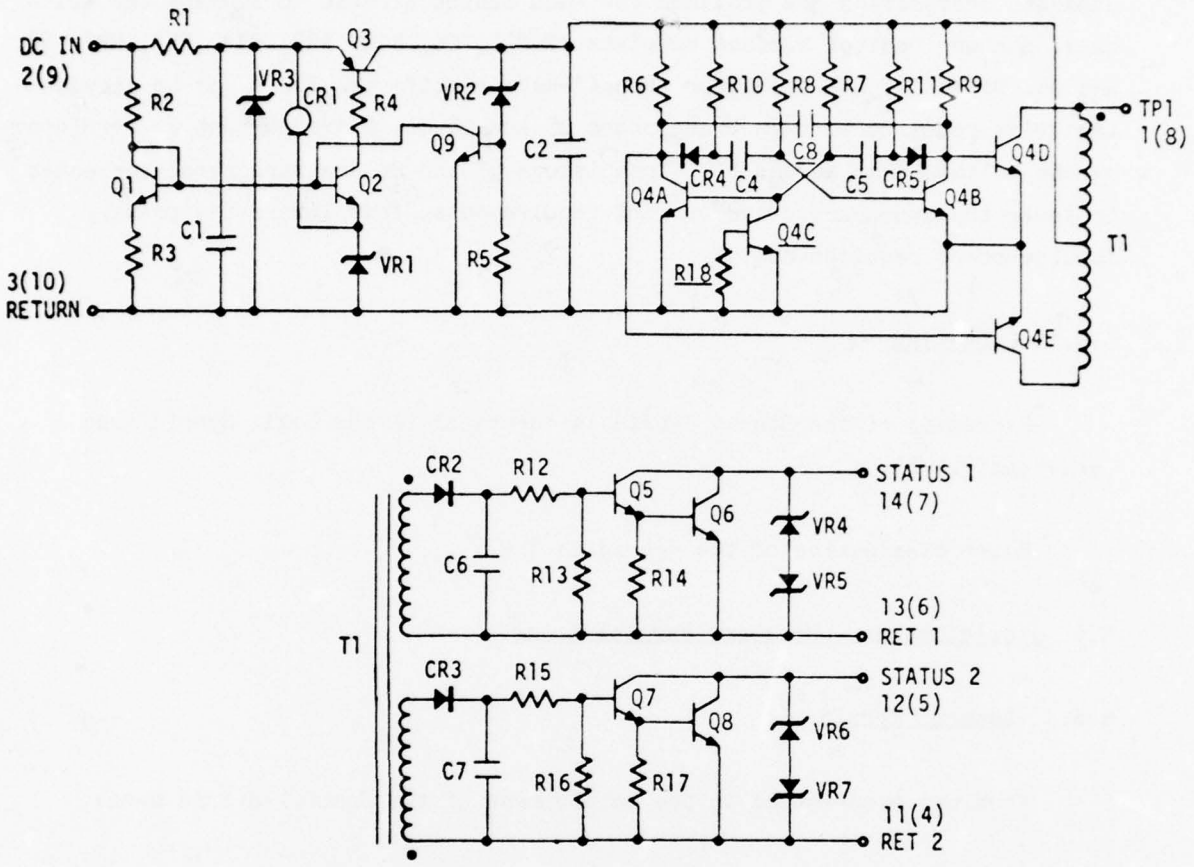


Figure 30. 1/2 SSPC Status Hybrid Schematic

The 200 kHz rectangular pulses are applied to the base of transistors Q4D and Q4E. These transistors drive transformer T1. The transformer couples these pulses to the output switches.

The transformer center-tap voltage is clamped at approximately +3.5 V dc, set by VR2, R5, and Q9. The voltage equals the breakdown voltage of zener VR2 plus the base-to-emitter voltage of transistor Q9. Clamping the center-tap allows the input voltage to reach +28 V dc without adversely stressing the circuit and provides current limiting. The primary voltage, therefore, is determined by the center-tap voltage minus the transistor collector-to-emitter saturation voltage.

The output switches are identical. Both are driven by transformer T1. Separate secondaries are provided for each output circuit to isolate the switches. Status 1 output circuit consists of CR2, C6, R12, R13, R14, VR4, VR5, Q5, and Q6. Diode CR2 and capacitor C6 half-wave rectify the 200 K pps to provide the drive required to turn transistors Q5 and Q6 on. Drive current is developed by the voltage drop across R12. Transistors Q5 and Q6 are Darlington connected to lower the secondary drive current requirements. This lowers the primary input current requirements.

5.5.2 Packaging

Packaging of the Status Hybrid is identical to the Logic Hybrid (see paragraph 5.4.2).

Power dissipation of the Hybrid is 1 W.

5.6 Hybrid Design - Problems and Solutions

5.6.1 Control Hybrid

Problems experienced in the development of the Control Hybrid were:

1) Low voltage output from control transformer T4
2) Failure of transformers to pass the 5000 g centrifuge test
3) Nonhermetic package
4) Incorrect Fast Trip
5) Transformers T5 and T6 cores cracking and/or windings shorting during assembly

The solutions were:

1) A substitute core material (Indiana General Core 6203) was used to fabricate transformer T4, due to the temporary unavailability of the specified material (Magnetics Inc, Core YR40601-TC). The substitute material had a Curie temperature of 140°C, resulting in reduced output above this temperature. The selection of the alternate core material (Ferroxcube Core 1041CT060-3B7), or the original material, solved the problem.

2) Transformers separated from the substrate when the Hybrid was subjected to a centrifuge test level of 1000 g (should pass 5000 g). The solution was to increase the amount of bonding material between the transformers and the substrate.

3) The initial designs of the Control Hybrid had the bottom edge of the metal cover soldered to the ceramic base (a two piece package). This design was inadequate, resulting in many nonhermetic units. The solution was to modify the metal cover by forming a flange on the periphery of the bottom edge. The additional bonding area allowed satisfactory seal of the package.

4) Incorrect Trip at 2A Level - This problem was caused by misinterpretation of the resistor trim instructions by the hybrid vendor. The problem was solved when the trim instructions were reviewed.

5) The solution to the T5 and T6 transformer problem was to change to a core with an O.D. of 0.190 in. (was 0.230 in.). Failures of the early models of the Z5 Monolithic contributed considerably to late delivery of the Control Hybrid. However, these failures cannot be attributed to the Control Hybrid development. These failures are discussed in the Monolithic design section.

5.6.2 Power Hybrid

The development of the Power Hybrid was relatively problem-free. The only problem of note was the failure of the power in, power out pins to pass the 600 A rupture test. The Hybrid supplier initially used staggered 8 mil diameter tungsten feed-throughs (2 per layer x 2 layers) in the ceramic substrate to carry the load current in and out of the Hybrid. A change from this method of interconnection to one using 30 mil pins as the feed-through path through the substrate corrected the problem.

5.6.3 Logic and Status Hybrids

These Hybrids were also relatively free from problems during the development phase. The only problem encountered was during gamma dot radiation testing of the design; the oscillator stalled at 2.73 x B-1 radiation criteria level.

The addition of the C12, C13, R27, R28, and Q4E, Q12E circuitry in case of the Logic Hybrid and C8, R18 and Q4E in the Status Hybrid corrected the problem.

SECTION VI

SSPCA DESIGN

6.1 Introduction

The B-1 cost reduction study indicated that a significant factor in the cost of the EMPCAs was the handwiring required to interconnect the electro-mechanical components. SSPCAs are comprised of plug-in printed circuit modules with replaceable components mounted on aluminum rails for cooling. All modules plug into mating receptacles mounted on the printed circuit MIB. A rack mounted chassis provides the housing for the modules and MIB. Thus, a significant portion of the handwiring in the EMPCA is eliminated by using the batch process printed wiring technique.

The following paragraphs describe how the SSPC, Logic, and Status modules are assembled into a power controller subsystem or SSPCA.

6.2 SSPCA - General Description

6.2.1 SSPCA Description

The B-1 trade studies indicate that an assembly (the SSPCA) containing 15 identical power control modules with four SSPCs per module, a Logic module and a Status module would include the best mix of circuitry required by the B-1 power control system. Figure 6 is a sketch of a SSPCA. Interconnections between the interface connectors and the SSPC, Logic and Status modules described in this section is made via a printed circuit MIB.

In order to provide the five types of circuit mechanization shown in Figure 3 and 4, the inputs and outputs of all the modules are brought out to the SSPCA interface connectors as shown in Figure 31. Some modules are pre-assigned as to function and phase and some may be assigned at the discretion of the user. The combination shown was determined by particular B-1 requirements. From a user standpoint, this results in a very flexible design. Available for selection are:

1) Phase A, B, or C switches
2) DC or ac load power
3) Normally open or normally closed switch
4) Power bus A or B
5) Preassigned (saves wiring) or unassigned circuits

Referring again to Figure 4, in cases of a logic type input, the SSPC is controlled by inputs C_1 and C_2. The latter (C_1, C_2) are nominal 0 to 5 V dc, with a 10 mA maximum current. Note that no power other than that supplied by C_1 and/or C_2 is required to operate an SSPC. In the case of the three phase load (see Figure 3), one signal (C_1) with a maximum available current of 10 mA controls three SSPCs (current requirement is 3.3 x 3 = 10 mA maximum drain).

6.2.2 SSPC Module

Each SSPC module consists of four PC circuits rated at 2 A rms or capable of supplying a maximum of 200 mA dc. The input to the SSPC is a nominal 230 V, 400 Hz.

The four PCs on a given module are hard wired to the same phase and share a common winding on the module power transformer. From that point on, they are completely separate, independent power controllers. Each circuit is capable of operating either normally closed (switch ON when the control input is zero volts), or normally open (switch OFF when the control input is zero volts). The selection of NO or NC is accomplished by externally jumpering the NO/NC interface pin to the desired NO or NC interface pin. The selection of operation as an ac or dc switch can also be made at the SSPCA interface connector (see Figure 31).

The Control Input requirements are 0 to 2 V for OFF and 3 to 6 V for ON. A maximum of 3.3 mA input current is required, which allows three SSPCs to be controlled by one 10 mA EMUX signal for three phase circuit mechanizations.

The detail design of the SSPC is presented in Section IV.

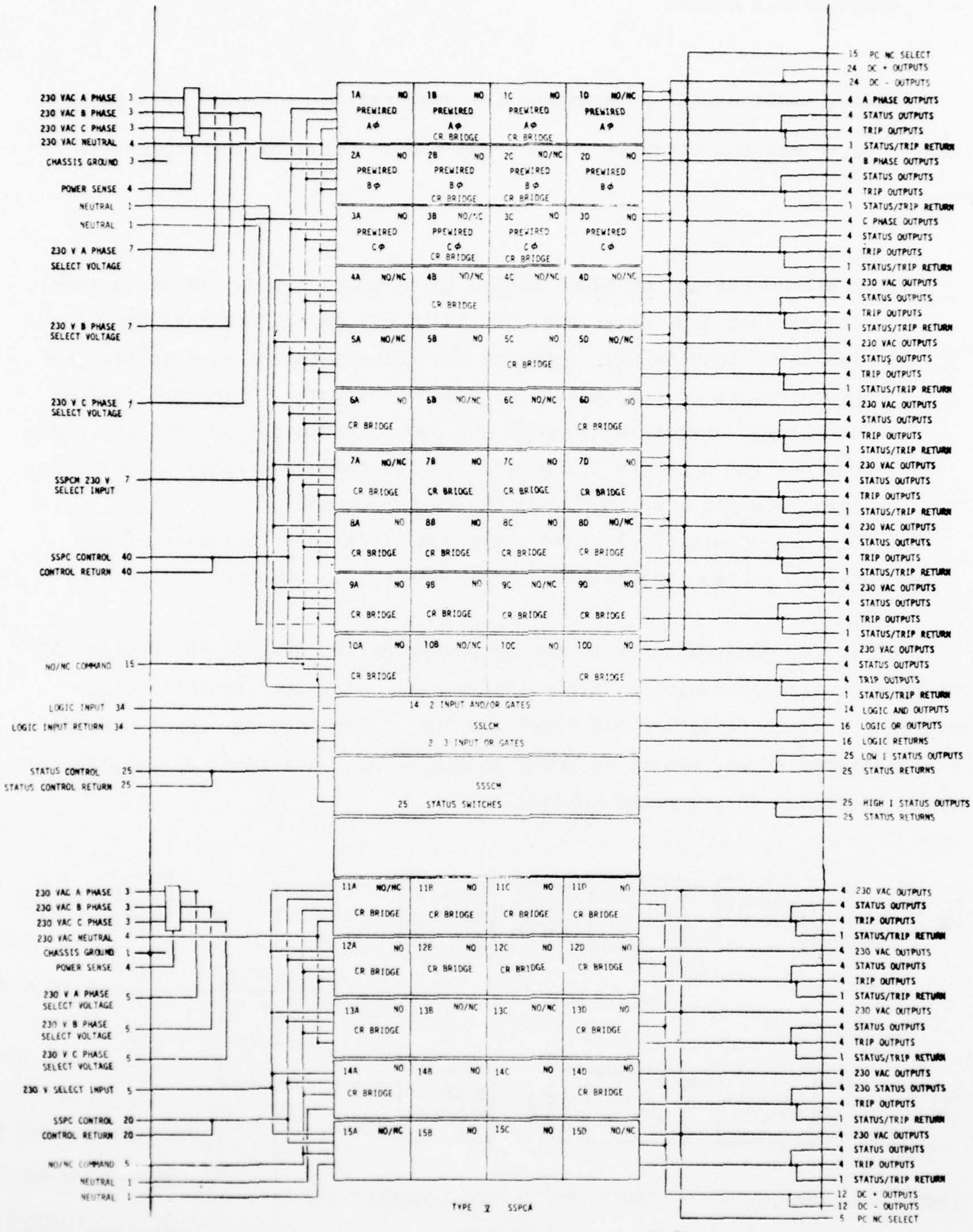


Figure 31. SSPCA Block Diagram

6.2.3 Logic Hybrid Module

Logical combinations of commands are required to mechanize many B-1 Aircraft power control circuits. The requirements for such logic circuits are:

1) The commands are standard EMUX outputs (0 to 6 V dc, 10 mA maximum).
2) The circuit must drive one SSPC (0 to 6 V dc, 3.3 mA maximum).
3) The SSPC circuits have a design requirement that a circuit failure could not cause the failure of another circuit. This implied that each logic circuit would have its own power supply or that the logic circuit would derive its power from the command or EMUX input. The logic circuit developed uses the latter method.
4) Command inputs are to have a minimum electrical isolation of one megohm between inputs and between inputs and outputs.

The above requirements were met by packaging two sets of the unique SSPC Threshold Detector circuit, an efficient 200 kHz oscillator for electrical isolation, a diode rectifier and "AND" and "OR" gates into the Logic Hybrid. A block diagram of the hybrid is shown in Figure 32. A general description of circuit operation is presented in Section V.

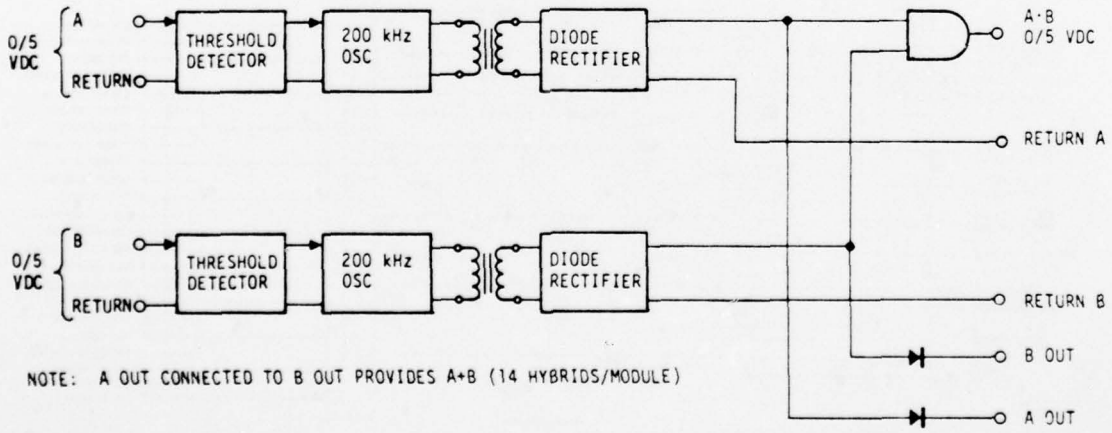


Figure 32. Logic Hybrid Functional Flow Diagram

Seventeen Logic Hybrids are mounted on one plug-in Logic Module per SSPCA. Mechanization of the logic function required is made at the SSPCA interface connector by wiring to the selected Logic Hybrid. Typical examples of "AND" or "OR" configurations are shown in Figure 4.

The 17 hybrids are mounted on aluminum rails that conduct the heat developed to the SSPCA heat exchanger. A six-layer printed circuit board supplies the interconnections to a 150 pin, MIL-C-55302 type, connector.

6.2.4 Status Hybrid Module

A circuit designated the Status Hybrid was required to round out the type of functions mechanized in the B-1 Aircraft power control system. The circuit accepts a 0 to 28 V dc or 0 to 5 V dc (0 V = low, 5 or 28 V = high) and turns on two isolated switches capable of sinking a maximum of 50 mA. The electrical isolation between the input and output is required to be one megohm minimum. A functional flow diagram of one hybrid is shown in Figure 33. A general description of the Status Hybrid circuit is presented in Section V.

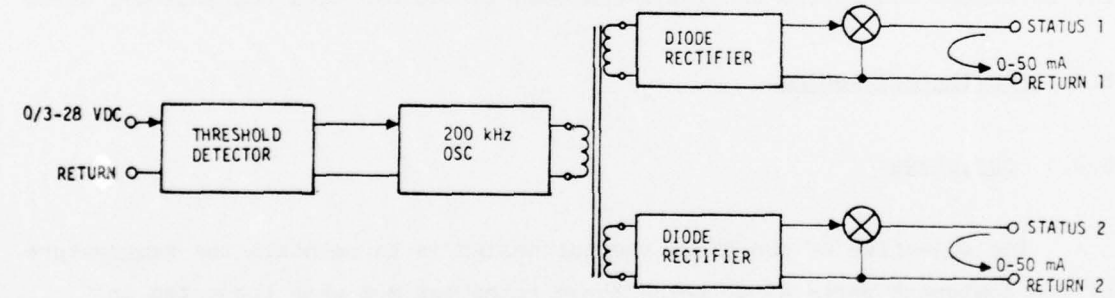


Figure 33. Status Hybrid Functional Flow Diagram

The Status Hybrid circuit mechanization is similar to that of the Logic Hybrid circuit:

1) A modified SSPC Threshold Detector circuit is used for the input stage.
2) The 200 kHz oscillator is coupled to the diode rectifier output via an isolation transformer
3) Circuit power is derived from the input signal.

The plug-in Status module contains 13 hybrids (26 separate circuits) mounted on aluminum rails for cooling. A six-layer printed circuit board interconnects the hybrids to a 150 pin connector. Connection to a particular hybrid is accomplished at the SSPCA interface connector.

6.3 SSPCA Physical Construction

The SSPCAs are rack mounted chassis with rack and panel interface connectors. The chassis housings are light weight, dip-brazed, and bonded assemblies. The assemblies are comprised of machined frames, sheet metal covers and panels, and rail heat exchangers. The plug-in module aluminum cooling rails are mounted to tabs on the heat exchanger by captive screws. Forced air convection cooling through the heat exchanger is used.

The design provides access to all modules (See Figure 6).

All modules plug into mating receptacles mounted on the MIB using Military qualified M55302 type connectors. The MIBs consist of 12-layer printed wiring boards that eliminates conventional wiring between modules. The interface connectors are interconnected to the MIB with conventional wire.

6.4 SSPC Thermal Design

6.4.1 Objective

The objective of the SSPCA thermal design is to maintain the temperature of the component parts at or below their rated maximum when subjected to worst-case temperature conditions and to provide a correspondingly lower part temperature under nominal operating conditions.

AD-A078 238 ROCKWELL INTERNATIONAL ANAHEIM CA AUTONETICS STRATEG--ETC F/G 1/3
SOLID STATE POWER CONTROLLER VERIFICATION STUDIES.(U)
JAN 79 C O LINDER F33615-78-C-2065
UNCLASSIFIED C79-85/201 AFAPL-TR-79-2029 NL

2 OF 3
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6.4.2 Thermal Analysis

6.4.2.1 Thermal Environment

The SSPCA is required to operate in the following steady-state thermal environment:

1) Maximum allowable power dissipation: 305 W
2) Normal in-flight cooling air temperature: 70 to 100 °F
3) Ambient operating temperature: -65 to 160 °F
4) Altitude: 0 to 70,000 ft
5) Cooling air flow = 4 lb/minute/kW x 0.305 kW = 1.22 lb/minute
6) 5 minute emergency = 0 air flow

6.4.3 Component Maximum Thermal Parameters

The maximum allowable junction temperature, power dissipation, and thermal resistance from junction to case of all critical components are shown in Table 3.

6.4.4 Equipment Thermal Packaging

Component Mounting

Heat generating components such as hybrids and transformers are mounted on metal heat rails. These rails conduct heat to the outer edge of the module as shown in Figure 34. Components are bonded to the heat rails using a thermal conductive adhesive. Critical bond line thickness is controlled by adding 0.002 in. diameter glass beads to the adhesive. A thermal conductivity and density comparison of heat rail materials indicates that aluminum and beryllium have the best conductivity and density ratio. From a practical standpoint aluminum was used. Components were mounted near the edges of the modules to decrease the length of the heat rails. The rail thickness is a trade off between the weight of the rails and temperature rise along the rails.

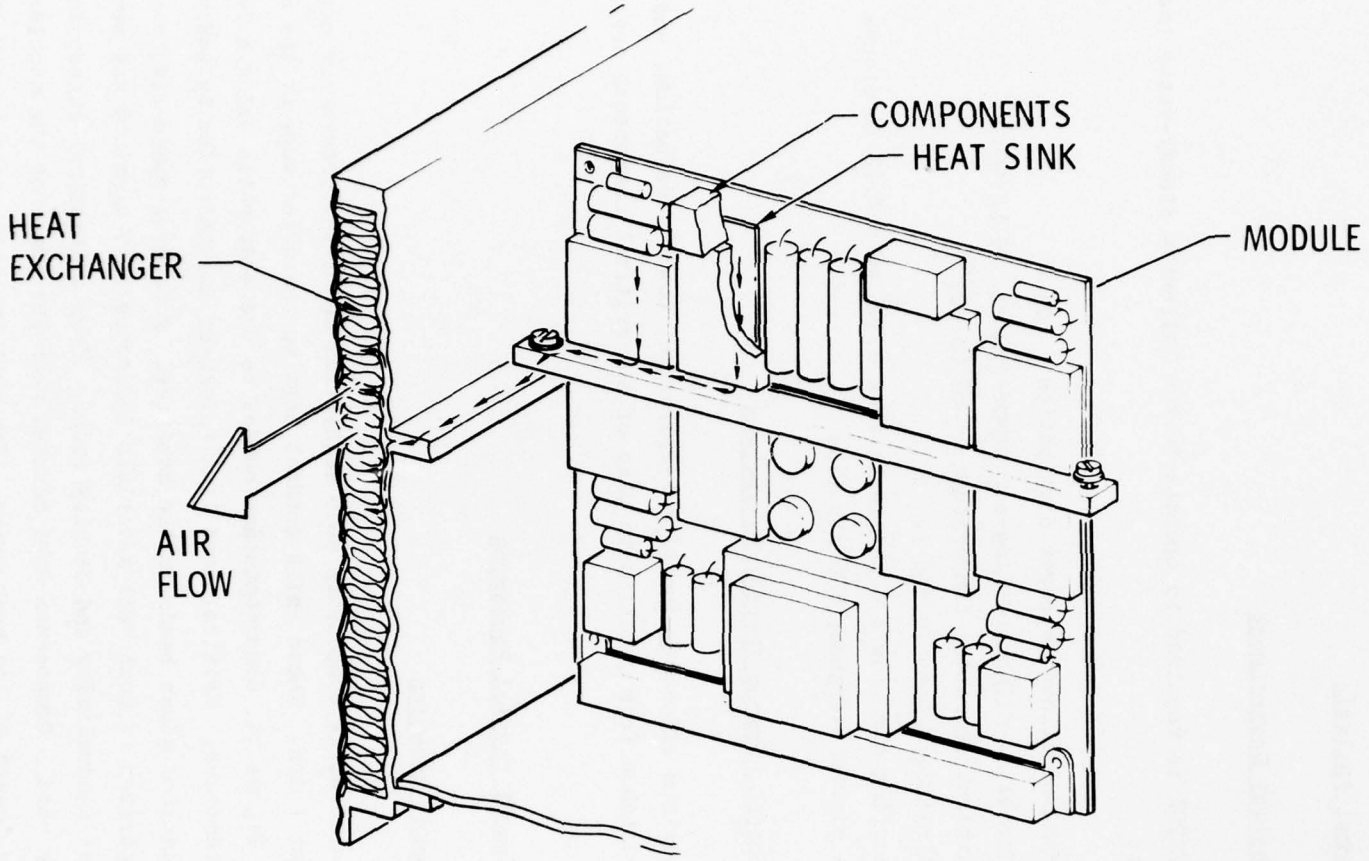


Figure 34. Thermal Path

TABLE 3

COMPONENT MAXIMUM THERMAL PARAMETERS

IID Number	Component Name	Reference Designation	Actual Power Dissipation (W)	Maximum Allowable Temperature °C		Thermal Resistance Rj-c (°C/W)
				Case	Junction	
M39006/01-3043	Capacitor	-	-	150	-	-
RNC55H6491FM	Resistor	-	0.294	150	-	-
RWR84SR226FR	Resistor	-	0.904	150	-	-
RNR70C1963FM	Resistor	-	0.010	150	-	-
446-0766-001	Transformer	T1	1.28	-	130	5.0
446-0767-001	Transformer	T2	----	-	130	5.0
447-1234-001	Power Hybrid	-	2.346	-	125	2.0
477-1235-001	Control Hybrid	-	0.701	-	125	4.0
446-0772-001	Transformer	T3	----	-	130	5.0
447-1237-001	Logic Hybrid	-	----	-	125	4.0
477-1239-001	Status Hybrid	-	----	-	125	4.0

6.4.4.1 Module to Housing Interface

The edges of the modules are clamped to the housing with a screw. This interface joint is critical because of the large number of parameters involved. These parameters include: clamping pressure, conductivity of materials, surface roughness, and cooling air. The use of high clamping force, aluminum-to-aluminum materials, and smooth surfaces will minimize this thermal resistance. With this design, the low pressure air in the interface joint at altitude can be tolerated. The housing is fabricated from 6061 aluminum. The walls are thin and provide a short heat path to the heat exchanger.

6.4.4.2 Heat Exchanger

The heat exchanger consists of aluminum fins dip-brazed between two 0.38 in. x 4.00 in. x 13.07 in. cold plates. The cold plates are used as the SSPCA chassis walls. The cold plates have 12 fins per inch. This fin spacing is the best trade off between heat transfer area, pressure drop, and ease of manufacture. Temperature rise from the coolant to housing wall is about 19 °F, and the static pressure drop is about 0.43 in. of water.

The total pressure drop through the heat exchanger is about 2.0 in. of water, with an 0.86 in. diameter inlet hole. The largest resistances are at the inlet, the cold plates, and the exhaust.

The cooling air is confined to the heat exchanger and does not contact the components. Since the heat exchanger is aluminum, moisture, sand, and dust in the coolant will have no adverse effects. Fin spacing is wide enough so that sand will not become trapped. No protective or thermal control devices are required.

6.4.5 SSPCA Thermal Analysis Results

A thermal analysis was performed of the design (shown in Figure 34) assuming the conditions below:

1) Coolant = 100 °F maximum inlet
2) Air Flow = 1.22 lb/min
3) Load Current = 1.5 A maximum average (The actual load currents are approximately 50 percent <0.3 A and 50 percent 0.3 to 2 A).
4) Total power dissipated = 246 Watts (Refer to Table 4 below).

TABLE 4

MODULE MAXIMUM POWER DISSIPATION

Module			Total Power Dissipation
Type	Number	Power Dissipation	
SSPC	15	15.2 W	228 W
Status	1	16 W	16 W
Logic	1	2 W	2 W
			Total 246 W

The following maximum component part temperatures resulted as a consequence of the analysis and the above conditions:

Module	Component Temperature
SSPC	122 °C
Logic	126 °C
Status	101 °C

Nominal operating temperatures of the component parts will be less than 85 °C, due to the lower temperature coolant and ambient air and to lower power dissipation as shown in Table 5.

TABLE 5

MODULE NOMINAL TEMPERATURE CONDITIONS

Items or Module	Temperature		Power Dissipation		Estimated SSPCA Module Usage
	Nominal	Worst Case	Nominal	Worst Case	
Coolant	80°	100°F	-	-	-
Ambient Air	130°F	160°F	-	-	-
SSPC	-	-	184 W	228 W	80.5%
Logic	-	-	1.7 W	2 W	86%
Status	-	-	9 W	16 W	57%

The interruption of cooling air during the 5 minute emergency period will have an insignificant impact on part temperatures since the SSPCA has a thermal time constant of 1 hour. Calculations indicate that part temperatures will increase by only 3°C during the 5 minute period.

6.5 Reliability Prediction Results

The results of the SSPCA reliability prediction indicate that an MTBF of 3384 hours will meet the required B-1 reliability requirement of 2700 hours. The details of the prediction are summarized in Tables 6 and 7.

TABLE 6

LRU RELIABILITY PREDICTION SUMMARY

LRU Module	Failure Rate x 10^{-6}	Qty	Total Failure Rate
AC Switch	17.0601	15	255.9015
Status Module	13.3350	1	13.3350
Logic Module	15.0914	1	15.0914
MIB and Chassis	11.1734	1	11.1734
Total			295.5013
MTBF 3384 hr			

6.5.1 Prediction Ground Rules

The SSPCA reliability prediction is based on the following set of ground rules:

1) All failure rates are considered constant and are within their useful life period.
2) The infant mortality period has expired through Hybrid burn-in.
3) The failure distribution is assumed to be exponential.

TABLE 7

SSPCA MODULE LEVEL PREDICTION BREAKDOWN

		AC Switch		Status Module		Logic Module		MIB and Chassis	
	F/R*	Qty	F/R	Qty	F/R	Qty	F/R	Qty	F/R
Power Hybrid	0.4663	4	1.8652						
Control Hybrid	3.1115	4	12.446						
Fuse	0.10	4	0.400						
Capacitor CLR	0.114	4	0.456						
Resistor RWR	0.066	4	0.264						
RNR	0.018	8	0.144						
Transformer									
PWR	0.018	5	0.090					2	0.036
50 KHz	0.027	4	0.108						
Circuit Board									
AC	0.822	1	0.822						
Status	0.546			1	0.546				
Logic	0.663					1	0.633		
MIB	4.842							1	4.842
Solder Joints	0.00012	274	0.03288	182	0.0218	221	0.0265	1614	0.1937
Connectors									
PCB AC	0.4452	1	0.4452						
PCB Logic	1.9188					1	1.9188		
PCB Status	3.1872			1	3.1872				
R&P 25	0.1147							1	0.1147
R&P 35	0.155							1	0.155
R&P 160	1.458							4	5.832
Status Hybrid	0.7664			12.5	9.580				
Logic Hybrid	0.7343					17	12.4831		
			17.0601		13.3350		15.0914		11.1734

*F/R = Failure rate in Failures per million hours

4) The environment used is aircraft inhabited.

5) Component quality levels are

   a) MIL-M-38510 class B for all ICs and Hybrids.

   b) JAN TX for all semiconductors.

   c) MIL established reliability level "M" for all resistors and capacitors (discrete).

6) Temperatures used for the prediction were

   a) 60 °C for all Hybrid packages (highest temperature within),

   b) 50 °C MIB temperature, and

   c) 40 °C chassis temperature.

7) The Monolithic CMOS/SOS chip failure rate for the digital section was predicted using the expression:

$$\tau_D = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_p$$

where

$$C_1 = 5.384\ 10^{-4}\ NG^{0.779}$$
$$C_2 = 5.240\ 10^{-4}\ NG^{0.7}$$

$$NG = \text{Number of } \frac{FETS}{4} = \frac{3040}{4}$$

π_Q, π_T, π_E and π_p are all from MIL-HDBK-217B

The failure rate of the linear section of the Monolithic chip was predicted using the linear IC equation of MIL-HDBK-217B with a 20 percent improvement for the CMOS/SOS device. The sum of the two sectional failure rates was taken and a 0.80 factor was applied to account for the use of an uncased die. The resulting failure rate for the Monolithic chip is 0.149 failures per million hours.

8) The LRU contains a full complement of modules and all are operating.

6.5.2 Reliability Block Diagram

The reliability block diagram for the SSPCA LRU configuration is presented in Figure 35. As the diagram indicates, the SSPCA reliability is represented by a single series system. The failure of any component is considered a system failure.

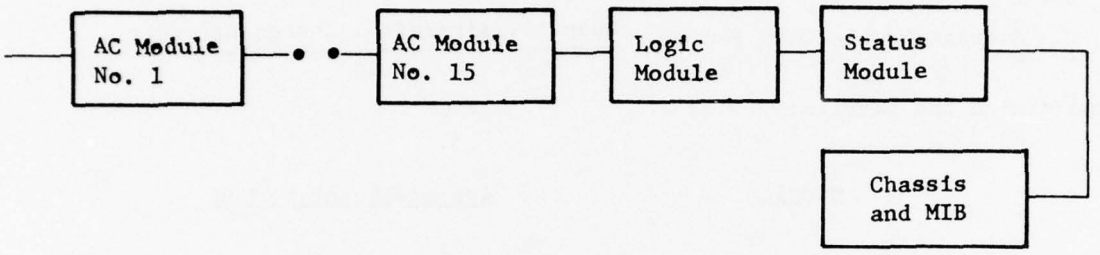


Figure 35. SSPCA Reliability Block Diagram

6.6 Reliability Mathematical Model

The mathematical relationships which describe the model for the SSPCA reliability are presented below. For the model, the MTBF of a series system is the reciprocal of the sum of the component failure rates. This is based on the assumption that electronic equipment failures are exponentially distributed over the useful life of the system. The MTBF Of the SSPCA is then:

$$MTBF = \frac{1}{\sum_{i=1}^{n} \lambda_i N_i DF_i}$$

where λ symbolizes failure rate and λ_i is the failure rate of the i^{th} component. N_i is the quantity of the i^{th} component used in the LRU. DF_i is the duty factor of the i^{th} module.

The SSPCA LRU in its present configuration contains a significant number of spare modules which are accounted for as a duty factor for the modules in the mathematical model. The spares are distributed as follows.

SSPCA Module	Quantity/Aircraft	Spares/Aircraft
AC Switch	210	41
Logic Module	14	6
Status Module	14	2

Since a complement for one aircraft of SSPCA LRUs is 14, the duty factor of a module is given by:

$$\text{Average Module Duty Factor} = \frac{\text{Quantity/Aircraft} - \text{Spares/Aircraft}}{14}$$

and giving the results:

Module	Average Quantity/LRU
AC Switch	0.805
Logic	0.86
Status	0.57

6.7 Nuclear Radiation Analysis

6.7.1 Introduction and Summary

This section contains the highlights of the nuclear radiation analysis performed on the SSPCA.

The analysis is summarized in Table 8. Detailed computer aided dose rate analyses were performed on all questionable circuits. These analyses indicate that the SSPCA is hard to >50 γ_c, where γ_c is the criteria dose rate.

Total dose data were available for all sensitive semiconductor parts except the Monolithic CMOS/SOS. These data indicate that the SSPCA is hard to $>5 \times 10^4$ rad(Si). The Monolithic has not been tested. However, the process has been tested and indicates hardnesses of $>10^5$ rad(Si). The neutron hardness of 5×10^{12} n/cm^2 is limited by the SCRs.

TABLE 8

TREE HARDNESS SUMMARY

Circuit	Hardness Summary		
	Dose Rate	Total Dose	Neutron
Diode Bridge	Hard to > 50 $\dot{\gamma}_C$*	Hard to > 10^5	Hard to > 10^{13} n/cm^2
Control Hybrid	A detailed (computer aided) analysis indicates hard to > 50 $\dot{\gamma}_C$.	The hardness level of > 5×10^4 rad(Si) is controlled by LM108.	Hard to > 5×10^{12} n/cm^2. This hardness level is controlled by LM108 and current regulator diodes.
Power Hybrid	Detailed analysis indicates hard to > 50 $\dot{\gamma}_C$. A maximum perturbation of 1250 µsec can occur from $\dot{\gamma}$ triggering of SCR. A 5000 µsec transient is acceptable.	Hard to > 10^5 rad (Si).	The hardness level of ≈5×10^{12} n/cm^2 is controlled by the L2SR06256 SCR.
Status Hybrid	Detailed analysis indicates that circuit is hard to > 50 $\dot{\gamma}_C$.	Hard to > 10^5 rad (Si).	Hard to > 10^{13} n/cm^2.
Logic Hybrid	Detailed analysis indicates circuit is hard to > 50 $\dot{\gamma}_C$.	Hard to > 10^5 rad (Si).	Circuit hard to > 10^{13} n/cm^2.

*$\dot{\gamma}_C$ = criteria dose rate profile

6.7.2 Parts

6.7.2.1 LM113 Diode

The LM113 is a temperature compensated, low voltage reference diode. The diode is synthesized using transistors and resistors in a Monolithic integrated circuit. A sample of five LM113 diodes was exposed to 10^5 rad(Si) with a maximum of -1 mV shift in V_Z.

The available permanent neutron damage data for the SSPCA diodes are presented in Table 9. Test data were required on any reference diode which could not tolerate a five percent change in V_Z.

6.7.2.2 Current Regulator Diodes

Current regulator diodes are field effect circuit elements that provide a current which is essentially independent of voltage (see Figure 36). These diodes are specially designed for maximum impedance over the operating voltage range. The voltage range is defined by V_K and peak operating voltage.

TABLE 9

WORST-CASE PERMANENT NEUTRON DAMAGE IN DIODES

Part No.	Type	Sample Size	ΔV_Z OR ΔV_R (mV)		ΔI_R (μA)		ΔV_F (V)	
			Meas. Cond. I_Z or I_R (mA)	ϕ	Meas. Cond. V_R (V)	ϕ	Meas. Cond. I_F (mA)	ϕ
1N937B	Ref	10	0.1	-20 @ 1	-	-	-	-
			0.1	-70 @ 10	-	-	-	-
			1.0	-20 @ 1	-	-	-	-
			1.0	-40 @ 10	-	-	-	-
			10.0	-10 @ 1	-	-	-	-
			10.0	+170 @ 10	-	-	-	-
1N4148	SW	10	0.1	0.0 @ 1	10	2E-5 @ 1	1	0.0 @ 1
			0.1	-1000 @ 10	10	1.5E-4 @ 10	1	+0.001 @ 10
			-	-	50	-	10	-
			-	-	50	-	10	-
			-	-	75	+0.01 @ 1	400	0.0 @ 1
			-	-	75	+0.096 @ 10	400	0.0 @ 10
LM113	Ref	5	1.0	0 @ 1.6	-	-	-	-
		5	1.0	+6 @ 10	-	-	-	-

$\phi = 10^{12}$ n/cm^2

The SSPCA uses the CR100 current regulator diode. The CR100 diode is characterized by IP = 1 mA at V_{AK} = 25 V. Radiation data are not available for this diode. The available data are summarized below.

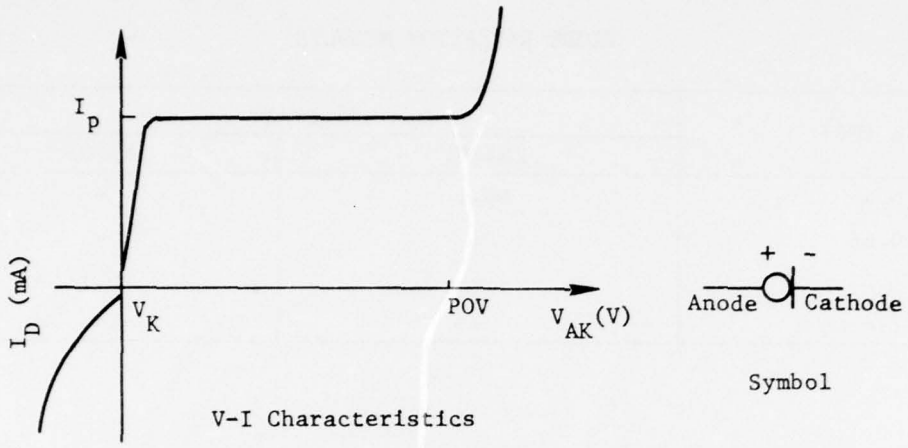


Figure 36. Current Regulator Diode Characteristics

The worst-case primary photocurrent of a 1N5290 diode is plotted in Figure 37 as a function of dose rate. The 10 A photocurrent had a radiation storage time, t_{sr}, of 0.35 μsec. One diode exhibited a t_{sr} of 1.42 μsec at 2.7 x 10^{11} rad(Si)/sec.

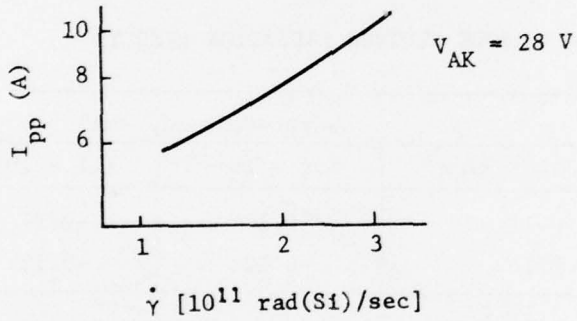


Figure 37. Peak Photocurrent of 1N5290 Diode

(Dose Rate Pulse Width was 45 nsec)

Eight samples each of the 1N5291 and 1N5305 diodes were exposed to Co^{60} radiation. I_p in the V_{AK} range of 10 to 75 V was essentially unchanged [ΔI_p (1N5291 $\leq$ 5 μA, ΔI_p (1N5305) $\leq$ 20 μA] by the maximum dose of 3 x 10^6 rad(Si). V_{AK} for a given I_D outside of the operating I_p did, however, change. The maximum changes at 3 x 10^6 rad(Si) are listed below.

TABLE 10

DIODE RADIATION RESULTS

I_D (mA)	ΔV_{AK} (V)	
	1N5291	1N5305
0.4	+0.2	-
0.66	-22	-
1.4	-	+0.1
2.4	-	-14

Ten samples of the 1N5297 diodes were exposed to neutron radiation. The exposure levels ranged from 1.2×10^{11} to 1.1×10^{14} n/cm^2. The test data are summarized below. The I_p of the one part was less than the specification minimum (0.9 mA) at 1.1×10^{13} n/cm^2.

TABLE 11

DIODE NEUTRON RADIATION RESULTS

V_{AK} (V)	Worst-Case ΔI_P (mA)			
	1.2×10^{11} n/cm^2	4.6×10^{12}	1.1×10^{13}	1.1×10^{14}
4	-0.11	-0.11	-0.17	-0.49
16	-0.1	-0.12	-0.12	-0.48

6.7.2.3 Bipolar Transistors

Primary photocurrents are generated in the emitter-base and collector-base junctions of a bipolar transistor. The collector-base junction produces the dominant photocurrent as shown in Table 12.

TABLE 12

TRANSISTOR I_{ppc} DATA

Part No./Mfgr	Type	Sample Size	Dose Rate Rads(Si)/sec	Pulse Width (nsec)	Ref
2N2222A/TI	NPN	3	10^8	30	1
2N2907A/	PNP	-	1.3×10^{10}	30	1
2N3019/FCH	NPN	3	1.3×10^{11}	30	1
2N3043/MOT	NPN	5	3×10^{10}	65	10
CA3045/RCA	NPN	-	10^7	--	-

Total ionizing radiation primarily causes an increase in the leakage currents and $V_{CE}(sat)$, and a degradation of the gain (β) of a bipolar transistor. The available total dose data on the SSPC transistors are presented in Table 13.

$\Delta \frac{1}{\beta}$ is defined as follows:

$$\Delta \frac{1}{\beta} = \frac{1}{\beta(r)} - \frac{1}{\beta_o}$$

where

$\beta(r)$ = β degraded by total dose

β_o = initial β

$\frac{\Delta 1}{\beta}$ is constant for a given total dose and I_C. For design purposes one assumes β_o is the specification minimum β_{sm}. The minimum degraded gain, β_d, of a 2N3019, for example, carrying an I_C of 100 mA and exposed to 10^5 rad(Si) is obtained as follows:

$$\Delta \frac{1}{\beta} = 1.55 \times 10^{-2} = \frac{1}{\beta_d} - \frac{1}{\beta_{am}} = \frac{1}{\beta_d} - \frac{1}{90}$$

$$\beta_d = 37.6$$

TABLE 13

TOTAL DOSE INDUCED DAMAGE IN BIPOLAR TRANSISTORS

Part No./ Manufacturer	Type	Sample Size	$\Delta\beta^{-1}$		ΔV_{CE}(sat) (mV)		ΔI_{CBO} (nA)		Ref
			Meas. Cond. I_C (mA)	10^4 rads(Si)	Meas. Cond. I_C (mA)	10^4 rads(Si)	Meas. Cond. V_{CB} (V)	10^4 rads(Si)	
2N2222/FCH	NPN	9	1	3.68E-4 @ 1	0.1	+1.0 @ 1	30	0.00005 @ 1	1
			1	1.69E-3 @ 10	0.1	+4.0 @ 10	30	0.00019 @ 10	
			10	7.78E-5 @ 1	0.3	+1.0 @ 1	3	0.00006 @ 1	
			10	6.75E-4 @ 10	0.3	+4.0 @ 10	3	0.0001 @ 10	
			30	1.88E-5 @ 1	1.0	+1.0 @ 1	20	0.00004 @ 1	
			30	4.60E-4 @ 10	1.0	+3.0 @ 10	20	0.00007 @ 10	
2N2907A/MOT	PNP	3	1	2.83E-4 @ 1	1.0	-4.0 @ 1	4	±0.0 @ 1	1
			1	3.42E-5 @ 10	1.0	-4.0 @ 10	4	-0.0002 @ 10	
			10	1.69E-4 @ 1	10	-2.0 @ 1	30	-0.0001 @ 1	
			10	5.72E-5 @ 10	10	-2.0 @ 10	30	+0.0032 @ 10	
			30	1.67E-4 @ 1	-	-	-	-	
			30	9.2E-5 @ 10	-	-	-	-	
2N3019/FCH	NPN	10	1	7.58E-3 @ 10	-	-	-	-	
			1	0.021 @ 100	-	-	-	-	
			100	2.64E-3 @ 10	-	-	-	-	
			100	4.81E-3 @ 100	-	-	-	-	
2N3043/MOT	NPN	5	-	0 @ 3.5	-	-	-	-	

The degraded gain from total dose and neutron effects is obtained by defining $\Delta\frac{1}{\beta}$ to be equal to $\Delta\frac{1}{\beta(\gamma)}$ plug $\Delta\frac{1}{\beta(\phi)}$. The parenthetical symbols represent total dose and neutron effects. For example, the β_d of the 2N3019 (I_C = 10 mA) exposed to 10^5 rad(Si) and 9.6 x 10^{12} n/cm^2 is obtained as follows.

$$\Delta\frac{1}{\beta(\gamma)} + \frac{1}{\beta(\phi)} \simeq 7.58 + 10^{-3} + 1.55 + 10^{-2} = \frac{1}{\beta_d} - \frac{1}{90}$$

$$\beta_d = 29.2$$

Note that $\Delta\frac{1}{\beta}$ was used for the specified I_C value closest to the operating point. Since $\Delta\frac{1}{\beta}$ decreases as I_C increases, one should use a low as opposed to a high I_C value. Table 14 presents the damage induced by neutrons.

6.7.2.4 Silicon Controlled Rectifiers (SCR)

An SCR is a device whose bistable switching action depends on PNPN regenerative feedback. This regenerative feedback can be described by considering the SCR as PNP and NPN transistors connected with common collectors and bases.

Photocurrents are induced in the SCR junctions in the same manner as they are induced in the junctions of diodes and transistors. These photocurrents increase the emitter currents in the transistors. The accompanying increase in the loop gain will turn on the SCR if $\beta_1\beta_2$ approaches unity.

The dose rate required to turn on an SCR is a quasi-hyperbolic function of pulse width (see Figure 38). The pulse width at which the dose rate threshold becomes constant is called the critical pulse width, t_c. The critical pulse width of a 2N1871 SCR is approximately 2 μsec. The corresponding dose rate is approximately 10^6 rad(Si)/sec for a 1 K gate resistor.

TABLE 14

NEUTRON INDUCED DAMAGE IN BIPOLAR TRANSISTORS

Part No./ Manufacturer	Type	Sample Size	$\Delta\beta^{-1}$		ΔV_{CE}(sat) (mV)		ΔI_{CBO} (nA)		Ref
			Meas. Cond. I_C (mA)	10^{12} n/cm^2	Meas. Cond. I_E (mA)	10^{12} n/cm^2	Meas. Cond. V_{CB} (V)	10^{12} n/cm^2	
2N2222A/TI	NPN	10	10.0	1.45E-4 @ 1	110.0	+3 @ 1	40	+0.1 @ 1	1
		10	10.0	-	110.0	-	40	-	1
		10	5.0	4.07E-4 @ 1	260.0	+6 @ 1	28	0.01 @ 1	1
		10	5.0	3.94E-3 @ 10	260.0	+58 @ 10	28	0.27 @ 10	1
		10	250.0	4.28E-4 @ 1	-	-	-	-	1
		10	250.0	4.33E-3 @ 10	-	-	-	-	1
2N2907A/TI		2	1.0	1.14E-3 @ 1	-	-	50	+0.14 @ 1	1
		11	5.0	7.2E-3 @ 10	41.6	135 @ 10	28	+3.9 @ 10	2
		2	10.0	5.53E-4 @ 1	-	-	-	-	
2N3019/	NPN	10	2.0	2.17E-3 @ 1	2.2	+38 @ 1	-	-	1
		10	50.0	1.11E-3 @ 1	55.0	+12 @ 1	-	-	1
		10	1000.0	7.33E-4 @ 1	1100.0	+36 @ 1	-	-	1
2N3019/FA	NPN	8	15.3	1E-3 @ 1	-	-	-	-	3
		8	15.3	1.55E-2 @ 9.6	-	-	-	-	3

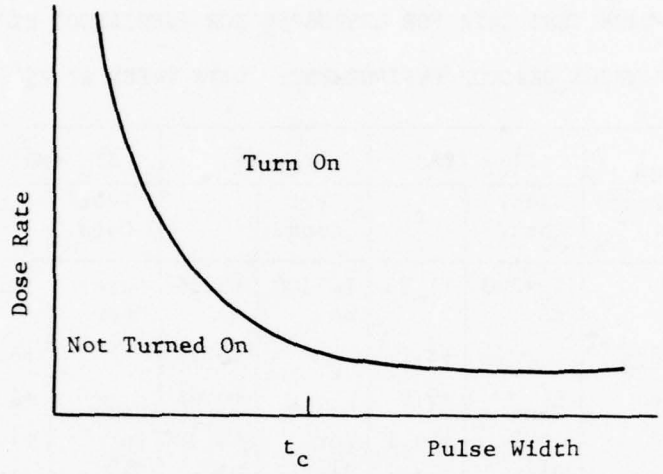


Figure 38. SCR Dose Rate Threshold Characteristics

As a general rule, the dose rate required to turn on an SCR is a function of the gate current required to turn on the SCR. The larger the gate current, the higher the dose rate threshold for turn on.

The SCR (L2SR06256) was exposed to the combined neutron/gamma environment of the TRIGA reactor. The test data are presented in Table 15. The degradation of the switching characteristics is a result of a degradation in the betas of transistors Q1 and Q2. The SCR will switch if $\beta_1\beta_2$ approaches unity as the gate current increases. No amount of gate current can cause the SCR to switch if $\beta_1\beta_2$ does not approach unity.

TABLE 15

WORST-CASE TEST DATA FOR L2SR06256 SCR (UNBIASED) EXPOSED TO TRIGA REACTOR ENVIRONMENT. DATA TAKEN AT 25°

Sample Size	Fluence $\emptyset(10^{12}n/cm^2)$	ΔI_{GT} (mA)		ΔV_{GT} (V)		ΔI_H (mA)		ΔV_F (rms V)	
		Test Cond.	Δ	Test Cond.	Δ	Test Cond.	Δ	Test Cond.	Δ
6	1.11	I_F=200 mA	+1.36	I_F=200 mA	+0.06	Gate Open	+2.1	I_F=200	+0.085
2	4.80		+8.1		+0.14		+6.6		+0.5
4	5.16	Same	+9.9	Same	+0.06	Same	+5.9	Same	+0.42
6	6.27	for	+14.1	for	+0.08	for	+14.0	for	+0.735
4	9.96	all tests	+42.1	all tests	+0.3	all tests	+41.2	all tests	+2.43
6	11.07		+43.1		+0.31		+42.0		+2.52

Total dose data for the SCR are presented in Table 16. The exposure condition for the SCR is presented in Figure 39.

TABLE 16

WORST-CASE SCR L2SR06256 PARAMETER CHANGE FOR A SAMPLE OF 12 EXPOSED TO TOTAL IONIZING RADIATION

Total Dose K rad(Si)	ΔI_{GT} (mA) @ I_F + 200 mA	ΔI_H (mA) @ Gate Open	ΔV_{GT} (V) @ I_F = 200 mA
5	+0.55	+4.6	+0.02
15	+0.4	+6.6	±0.01
50	+0.57	+6.4	+0.01
100	+0.5	+5.5	+0.02

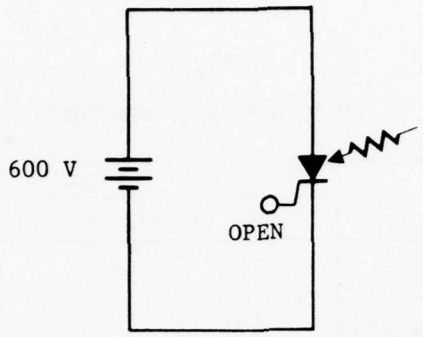


Figure 39. SCR Exposure Configuration

6.7.2.5 Bipolar Linear Integrated Circuits

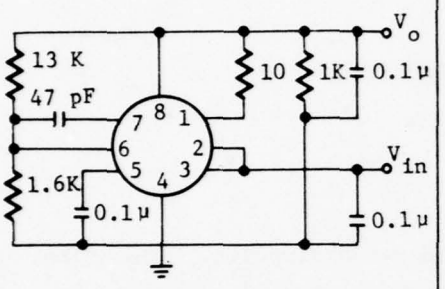
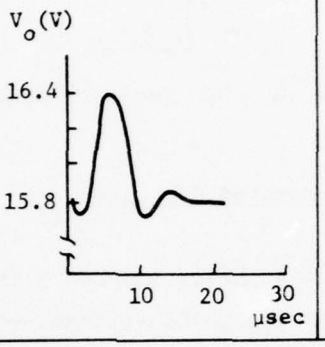
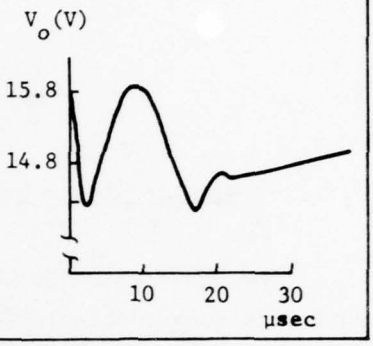
The SSPCA uses the LM105, LM108 and LM113 integrated circuits. Dose rate data were only available for the LM105 voltage regulator. Worst-case data for a sample of four are presented in Table 17 for the basic regulator operating configuration. The regulator at 10^8 rad(Si)/sec gives a positive transient response at the output that is 0.6 V in magnitude and lasts for ≈ 8 μsec. The regulator at 10^9 rad(Si)/sec gives an initial negative transient response at the output that is 1.2 V in magnitude and lasts ≈ 0.2 μsec. The long transient recovery back to the pre-irradiation state lasts for ≈ 1.2 msec.

6.7.2.6 Junction Field Effect Transistor (JFET)

Transient photocurrents are generated in a JFET in much the same manner as they are generated in a diode. The photocurrent sources are: 1) PN junction photocurrents, 2) increased channel conductivity, 3) current leaking through oxide layer, and 4) electron emission from device structure and chip atmosphere. The transients appear as gate and drain-to-source photocurrents (see Figure 40). Secondary photocurrents are also produced.

TABLE 17

LM105 DOSE RATE RESPONSE

Configuration	Output Response	
	10^8 rad(Si)/sec	10^9 rad(Si)/sec
		

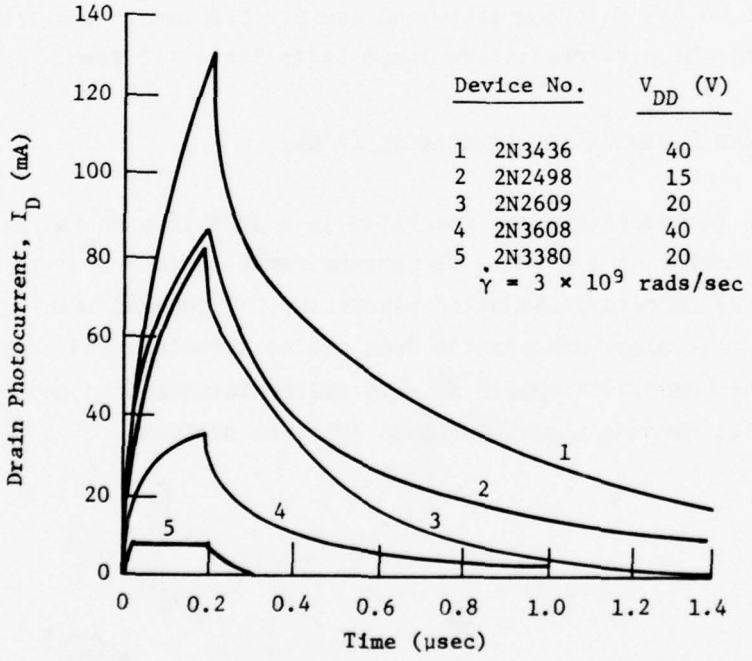


Figure 40. JFET Photocurrents

The gate-to-source leakage current I_{GSS} is the most sensitive parameter of a JFET to total dose (see Table 18). P-channel JFETs are more resistant to radiation than are n-channel JFETs This is probably due to the buildup of an inversion layer in the p-type material of an n-channel JFET. The inversion layer is caused by the accumulation of positive charge in the oxide passivation. In general, total dose effects appear around 5×10^4 rad(Si) but are acceptable below 2×10^5 rad(Si). Above 10^6 rad(Si), the leakage current degrades very rapidly.

TABLE 18

WORST-CASE TOTAL DOSE EFFECTS IN JFETs

Part Number	Sample Size	Meas. Cond.	Ave Parameters								
			$V_{pinch\ off}$ (V)			I_{GSS}			G_m (μυ)		
			0*	10^5	10^6	0	10^5	10^6	0	10^5	10^6
2N4856A	2	ON	-8.56	-8.56	-8.58	<20 pA	20 pA	150 pA	8,400	8,400	8,400
	2	OFF	-8.53	-8.53	-8.27	<20 pA	8.4 nA	400 nA	8,800	8,800	8,800
2N4857	2	ON	-5.03	-5.03	-5.01	<20 pA	50 pA	110 pA	14,000	13,800	13,800
	2	OFF	-3.56	-3.56	-3.44	<20 pA	3 nA	210 nA	13,800	13,800	13,800
2N5545	2	ON	-1.08	-1.08	-1.08	<20 pA	50 pA	700 pA	9,200	9,200	8,900
	2	OFF	-1.10	-1.10	-1.03	<20 pA	500 pA	15 nA	9,300	9,200	9,200

*Dose in rad(Si)

n-channel JFETs are harder to neutron damage than p-channel JFETs.

Empirical data indicate that JFETs are not significantly degraded by 10^{13} n/cm^2 but are completely destroyed by 10^{15} n/cm^2 (see Figure 41).

6.7.2.7 CMOS/SOS

The Monolithic chip uses CMOS/SOS technology. The use of SOS raises the dose rate threshold to the order of 10^{10} rad(Si)/sec. The devices are essentially unaffected by lower dose rates.

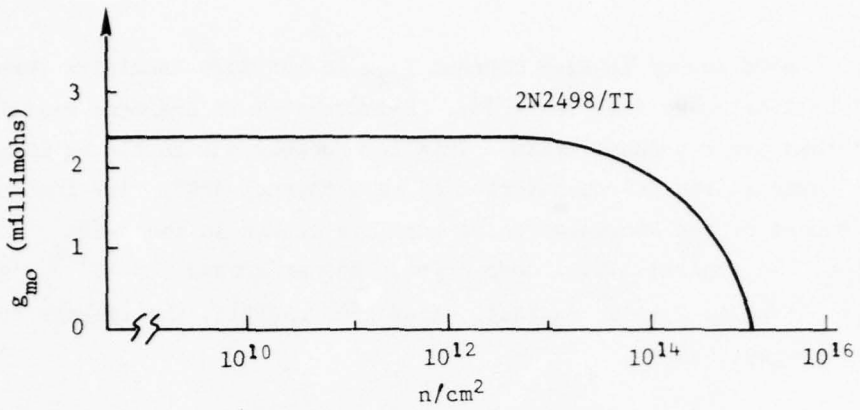


Figure 41. g_{mo} Neutron Degration in JFET

The use of SOS technology may lower the total dose threshold of the device to $<10^4$ rad(Si) if total dose hardening techniques are not employed. Rockwell International has developed techniques which will raise the total dose hardness of CMOS/SOS to $>10^5$ rad(Si). CMOS devices are hard to $>10^{13}$ n/cm^2.

6.8 Electro-Magnetic Pulse (EMP)

An extensive analysis was performed of the SSPCA when exposed to EMP. The EMP requirement is shown in Figure 42.

The analysis shows that the SSPCA design is fully compliant with EMP requirements, i.e., the predicted failure threshold for each semiconductor part is greater than the EMP excitation on that part.

The analysis results also show that the parts with the least worst-case margin are the ZS1008 bridge rectifier diode (margin = +3.8 dB) and the LM108 IC (margin = 8.8 dB).

6.9 Maintainability

Maintainability of the SSPCA and modules can best be described by reviewing their maintainability design requirements. The following requirements are derived from the B-1 Aircraft specifications with respect to maintainability.

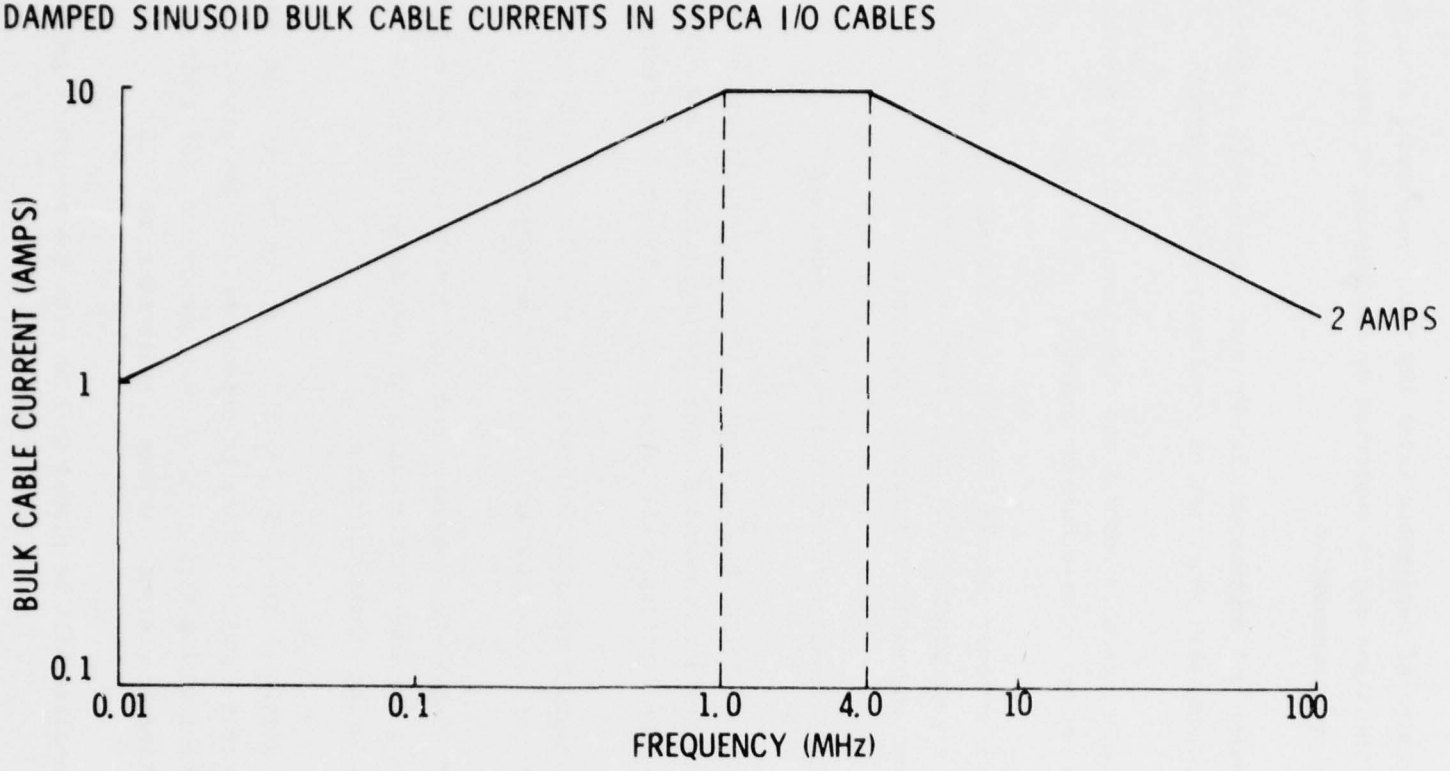


Figure 42. EMP Requirement

1) The design of repairable items and their components shall be such that the items may be supported by replacement of interchangeable parts or subassemblies.

2) Equipment and components that are not structurally or functionally interchangeable shall not be physically interchangeable.

3) Module or assembly removal and replacement shall be possible without removing any other module or assembly in the LRU.

4) When a properly aligned LRU/module or assembly is installed into the next higher assembly, it shall meet the performance requirements without the need for further adjustments.

5) The SSPCA shall not require scheduled overhaul.

6) Equipment design shall prevent incorrect installation of modules or assemblies and connecting cables by mechanical keying methods. Color coding or labeling shall be used to supplement this requirement.

7) Electronic modules or subassemblies shall be plug-in units and electrical connection shall be blind-mated connectors.

8) SSPCA installation hardware and dust covers which are required to be removed for shop maintenance shall employ captive hardware to prevent loss during normal maintenance.

9) All functional parts of the SSPCA shall be contained in separately removable plug-in modules or assemblies with the exception of interconnecting wiring, electrical connectors, SSPCA structure and mounting provisions, current transformers, and MIB.

10) All handles will be placed in line with the center of gravity.

11) All handles will be placed for a comfortable grip while unit is being removed or replaced.

12) No on-aircraft adjustments or calibration shall be permitted.

13) The design shall consider use of MIL-STD parts and items within Government inventories.

14) Fault isolation within the SSPCA shall have a design goal of isolation to a single defective SRU.

15) Failure detection and isolation for each repairable LRU and SRU shall be facilitated by testing with automatic computer controlled test equipment.

16) Support equipment, tools, and test equipment required for repair and overhaul shall be standard Air Force items to the maximum extent possible.

17) Each LRU and SRU shall have sufficient test points at operational and test connectors to allow complete performance verification, fault detection and, if necessary, alignment and calibration.

Additional maintainability features that are desired:

1) Test points shall be accessible and unimpeded by other parts of the equipment.

2) Parts and assemblies shall be placed so that structural members do not prevent access to them.

3) Capacitors and other components which retain heat or electrical potential after equipment is off, shall be located where technicians are not likely to touch them while changing commonly malfunctioning parts.

4) Parts shall be mounted on one side of a surface with associated wiring on the other side.

5) Handles shall be provided for units which weigh more than 10 lb.

A review of the SSPCAs and SSPCs indicates that their designs conform with the above and thus, are highly maintainable.

Using the procedures described in MIL-HDBK-472, the mean corrective maintainance time Mc was calculated using the following formula:

$$M_c = \frac{\Sigma(\lambda_{Mc})}{\Sigma\lambda}$$

where

λ = average part failure rates per 10^{-6} hr

Mc = corrective maintenance time in manhours

Substituting the corrective maintenance times and individual maintenance tasks listed, the mean corrective maintenance items are:

Module or LRU	Mc (hr)
SSPCA	0.973
SSPC	1.389
Logic	1.312
Status	1.190

6.10 System Safety

In normal operation, the SSPCA and the SSPCs pose no hazard to maintenance personnel. In the SSPCA, power is routed from the rack and panel (thus not hand mated) interface connectors rated at 825 V ac rms through wires with 1000 V insulation to the MIB, and then through the MIB to normally inaccessible module connectors. Thus, all high voltage points are normally inaccessible.

Two potential hazards exist under certain operating conditions:

1) During maintenance activities with the SSPCA plugged in and the covers removed, care must be exercised when touching, probing, or otherwise making contact with the hardware inside the SSPCA.

2) With the SSPCA plugged in, each inactivated SSPC circuit at the unloaded end of the system wiring will normally provide no more than a maximum of 2 mA of leakage current. Since more than 5 mA is required to pose a hazard to personnel accidently touching this point of an open circuit, this condition does not constitute a potential hazard. A potential hazard would exist if the SSPC leakage current exceeds 5 mA and if maintenance personnel accidently touch an uninsulated section of the system wiring connected to the out-of-specification SSPC.

SECTION VII
SSPCA AND SSPC TEST RESULTS

The Qualification Tests performed prior to termination of the B-1 contract included SSPCA dielectric withstanding voltage, insulation resistance, bonding resistance, and logic and status circuit tests. These test results are presented in this section together with the SSPC module tests performed as a part of this study.

A brief description of each test is presented together with the test results. The detailed test procedures are shown in Rockwell International document entitled "B-1 Solid State Power Control Assembly (SSPCA) Qualification Test Plan and Procedure", C77-1019/201 except as modified to include testing at -55° and 71°C, and simplified to allow manual rather than automatic testing.

7.1 Dielectric Withstanding Voltage (DWV) Test

7.1.1 Test Procedure

The DWV test requires 1300 V rms at sea level and 800 V rms at 70,000 ft to be applied between each SSPCA interface connector 230 V pin and every other 230 V pin in the interface connector. All conductors, including chassis grounds and connector shells but excluding the pins under test are simultaneously tied to the test voltage return.

The test was repeated for non-230 V pins with test voltages of 900 V rms at sea level and 200 V rms at 70,000 ft. The leakage current was required to be less than 2 mA for a minimum of 1 minute.

7.1.2 Test Results

The SSPCA chassis passed the above tests after the following changes were made:

1) RTV Silicone was injected in 5 pins of the J1 interface connector and 2 pins of the J4 connector to correct a defective pin seal and eliminate arcing between adjacent pins of the connectors.

2) Additional Dow Corning 3140 Silicone was added in several areas where the connecting wires between the interface connectors and the MIB left the MIB.

7.2 Insulation Resistance (IR) and Bonding Resistance Test

7.2.1 Test Procedure

The IR test measured the resistance of each isolated pin in the SSPCA interface connectors to every other pin in the interface connectors and between each pin and chassis. The test voltage was 500 V dc. The insulation resistance shall exceed 100 megohms. The test was performed before and after the DWV tests at an ambient temperature of $75^{\circ} \pm 1.4^{\circ}C$.

The bonding resistance of the chassis, the electrical resistance between the SSPCA interface connector shells and the chassis, and the resistance between the covers and the chassis could not exceed 2.5 milliohms at dc. The bonding resistance test was performed after completion of the IR test.

Test Results

The insulation resistance of all pins exceeded 100 megohms; the bonding resistance was less than 2.5 milliohms. The insulation resistance and bonding resistance of the SSPCA chassis met specified requirements.

7.3 Status Circuit

Test Procedure and Results

A Status circuit was selected at random on the Status module. The circuit requirements and test results are shown below.

TABLE 19

STATUS CIRCUIT TEST RESULTS

Test Number	Input Voltage (Vdc)	Input Current (mA)	Output Voltage (Vdc)	Output Leakage Current (mA)	Test Results	Pass/Fail
1	0 ± 0.3	-	-	≤0.1 mA	0.003 mA	P
2	0 ± 0.3	-	-	≤0.1 mA	0.003 mA	P
		≤10 mA	-	-	0 mA	P
3	2 ± 0.3	-	-	≤0.1 mA	0.003 mA	P
4	2 ± 0.3	-	-	≤0.1 mA	0.003 mA	P
		≤10 mA	-	-	0.647 mA	P
5	3 ± 0.3	-	≤1.5	-	0.8 V	P
6	3 ± 0.3	-	≤1.5	-	0.8 V	P
		≤10 mA	-	-	5.46 mA	P
7	10 ± 0.5	-	≤1.5	-	0.8 V	P
8	10 ± 0.5	-	≤1.5	-	0.8 V	P
		≤10 mA	-	-	7.21 mA	P
9	28 ± 1.4	-	≤1.5	-	0.8 V	P
10	28 ± 1.4	-	≤1.5	-	0.8 V	P
		≤15 mA	-	-	7.94 mA	P

The Status Circuit met its specified requirement.

7.4 Logic Circuit

Test Procedure and Results

A Logic circuit was selected at random on the Logic module for test. The circuit requirements and results are shown in Table 20.

The Logic Circuit met its specified requirement.

TABLE 20

LOGIC CIRCUIT TEST RESULTS

Test Input		Test Requirement		Test Result					
Configuration	Input Voltage (Vdc)	Input Current (mA)	Output[1] Voltage (Vdc)	I_1 I mA	I_2 I mA	I_3 I mA	V_4 Vdc	I_4 I mA	Pass/Fail
2 Input "OR"	4.0	-	3-6	-	-	-	4.3	3.16	P
	-	≤10	-	8.96	4.22	-	-	-	
2 Input "AND"	4.0	-	3-6	-	-	-	4.45	3.19	P
	-	≤10	-	5.46	7.72	-	-	-	
2 Input "OR"	2.0	-	<2	-	-	-	0.001	0	P
	-	≤10	-	0.68	0.69	-	-	-	
2 Input "AND"	2.0	-	<2	-	-	-	0.004	0	P
	-	≤10	-	0.68	0.69	-	-	-	
3 Input "OR"	4.0	-	3-6	-	-	-	4.54	3.21	P
	-	≤10	-	4.99	5.79	5.11	-	-	
3 Input "OR"	2.0	-	<2	-	-	-	0.005	0	P
	-	≤10	-	0.59	0.71	0.68	-	-	

NOTE: (1)The output current (I_4) corresponding to its output voltage (V_4) is required to fall into the cross hatched area **shown in Figure 43 below.**

NOTE: (1) The output current (I_4) corresponding to its output voltage (V_4) is required to fall into the cross hatched area shown in Figure 43 below.

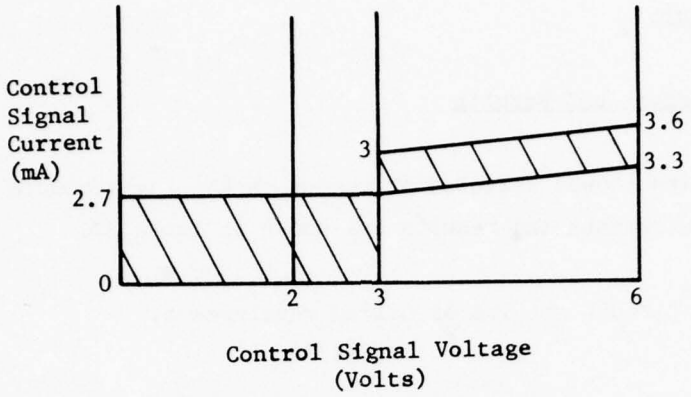


Figure 43. Logic Circuit Output Requirements

7.5 SSPC Verification Tests

Verification tests were performed using selected module level performance tests specified in the SSPCA Qualification Procedures. These tests were performed at -55 °C, +25 °C, and +71 °C. The tests that were conducted and the generalized results are listed in Table 21.

7.5.1 Zero Voltage Turn On/Zero Current Turnoff

The requirement for zero voltage turn-on is that the SSPC must turn on within ±32 V (maximum) of the zero voltage crossover point of the ac line voltage. No difficulties in meeting this requirement were experienced. The full tolerance was taken up at low temperature, with several of the circuits turning on at -32 V. Circuit B on Module No. 1, at high temperature, is shown to have failed due to the inability to measure ZVC because of a failure to turn off when commanded by the control. This is discussed in the Turn-Off Voltage section.

Zero Current Turn-off requires the SSPC to turn off within ±50 mA of the zero current crossover point of the load current. None of the circuits passed this requirement. The cause of these failures was discovered upon examination of the $\frac{dI}{dt}$ rate of the lead current and normal SCR reverse recovery time.

TABLE 21

SSPC VERIFICATION TEST RESULTS

Test Name	Module No. 1 Pass/Fail	Module No. 2	Test Name	Module No. 1 Pass/Fail	Module No. 2
Zero Voltage Turn-On	Pass*	Pass	Waveform Distortion	Pass	Pass
Zero Current Turn-Off	Fail	Pass	Voltage Drop	Pass	Pass
Trip-Out Time	Pass	Pass	Power Dissipation	Pass	Pass
Repetitive Reset	Pass	Pass	Rectified AC Output	Pass	Pass*
Reset Action	Pass*	Pass	High Current Trip Out	Pass	-
Trip Indication	Pass	Pass	Fail Safe	Pass	-
Leakage Current	Pass	Pass	Turn-On/Turn-Off Volt	Pass*	Pass*
DC Offset Voltage	Pass	Pass	Control Input Impedance	Pass	Pass
Transient Spike Over.	Pass*	Fail			

*The asterisk is used - where one circuit on the module failed the test at an extreme temperature. Except for ZIC, 100 percent pass could be met with moderate corrective action.

Detailed requirements, test data, discussion of failures, and, when needed, corrective action will be discussed for each test.

NOTE: (1) Module No. 1 = TLD 0005
(2) Module No. 2 = TLD 0006

The present B-1 SSPC units, when operated at 2 A rms and 400 Hz withstand

$$\left.\frac{dI}{dt}\right|_{t=0} = -7.1 \text{ mA/}\mu\text{sec}$$

Normal reverse recovery time for the SCR being used is on the order of 20 μsec. This would allow (7.1 mA/μsec)(20 μsec) or 142 mA to pass before the SCR could recover sufficiently to completely turn off. Reverse recovery current/time is not normally specified for SCRs of the type used here, although this one was. Considering the size of the SCR used for this application (25 A), the $\pm I_{ZIC}$ limit of ±50 mA may not be achievable despite an effort to tighten the specification.

TABLE 22

ZERO VOLTAGE TURN-ON/ZERO CURRENT TURN-OFF TEST

Module Tests No. 1

Zero Voltage Turn On

Circuit	Turn On Point (V)	P/F
Room Temp		
A	-25	P
B	-24	P
C	-25	P
D	-25	P
Low Temp		
A	-32	P
B	-32	P
C	-30	P
D	-32	P
High Temp		
A	-24	P
B	-	F
C	-22	P
D	-22	P

ZIC

Circuit	ZIC (mA)	P/F
Room Temp		
A	+90	F
B	+80	F
C	+100	F
D	+110	F
Low Temp		
A	+50	P
B	+50	P
C	+50	P
D	+60	F
High Temp		
A	+60	F
B	+60	F
C	+70	F
D	+80	F

TABLE 22 (CONTINUED)

AC MODULE TEST NO. 2

ZVC and ZIC

Circuit	ZVC (V)	P/F	ZIC (mA)	P/F
Room Temp				
A	-24	P	+70	F
B	-24	P	+70	F
C	-23	P	+80	F
D	-24	P	+70	F
Low Temp				
A	-32	P	+50	P
B	-31	P	+60	F
C	-30	P	+60	F
D	-32	P	+55	F
High Temp				
A	-18	P	+80	F
B	-18	P	+80	F
C	-20	P	+85	F
D	-20	P	+75	F

7.5.2 Trip-Out Time

The Trip-Out Time test consists of two parts: (1) non-repetitive tests for trips at 2, 3, 4, 10, and 20 A, (2) pulsed load tests for trip out with various duty cycles at loads of 5, 10, and 20 A. Trip time band limits for (1) are "No Trip", 0.6 to 10 sec, 0.25 to 3.0 sec, 0.04 to 0.6, and 0.01 to 0.2 sec, respectively. Trip time band limits for (2) vary with the duty cycle. No difficulties were encountered in passing these tests.

TABLE 23

TRIP-OUT TIME FOR AC SWITCH MODULE NO. 1 TESTS

Circuit	Trip Time (sec) at					P/F
	2.0 A	3.0 A	4.0 A	10 A	20 A	
Room Temp						
A	N/T	1.00	0.66	0.200	0.100	P
B	N/T	1.04	0.68	0.210	0.104	P
C	N/T	1.16	0.71	0.200	0.102	P
D	N/T	1.12	0.73	0.200	0.104	P
Low Temp						
A	N/T	1.06	0.66	0.190	0.100	P
B	N/T	1.00	0.68	0.20	0.100	P
C	N/T	1.06	0.67	0.190	0.100	P
D	N/T	1.32	0.74	0.20	0.100	P
High Temp						
A	N/T	1.00	0.66	0.20	0.10	P
B	N/T	1.04	0.68	0.20	0.10	P
C	N/T	1.08	0.68	0.20	0.10	P
D	N/T	1.10	0.70	0.20	0.10	P

N/T - No Trip

TABLE 23 (CONTINUED)

AC Switch Module Tests No. 2

Trip Out Time

Circuit	Trip Time (sec) at 2.0 A	3.0 A	4.0 A	10 A	20 A	P/F
Room Temp						
A	N/T	0.84	0.66	0.37	0.100	P
B	N/T	1.12	0.63	0.40	0.104	P
C	N/T	0.88	0.56	0.40	0.100	P
D	N/T	1.10	0.68	0.40	0.104	P
Low Temp						
A	N/T	1.04	0.73	0.20	0.100	P
B	N/T	1.21	0.76	0.21	0.102	P
C	N/T	1.00	0.67	0.20	0.100	P
D	N/T	1.12	0.70	0.210	0.100	P
High Temp						
A	N/T	1.28	0.75	0.19	0.100	P
B	N/T	1.04	0.73	0.20	0.104	P
C	N/T	1.10	0.60	0.19	0.100	P
D	N/T	1.16	0.74	0.200	0.104	P

TABLE 23 (CONTINUED)

AC Switch Module Tests No. 1 Pulsed Load (Part of Trip-Out Time) Test No. and Trip Band Limit (sec)							
Circuit	0.140 to 7.0 1	0.31 to 4.1 2	0.25 to 3.0 3	N/T 4	N/T 5	N/T 6	P/F
Room Temp							
A	0.410	0.71	0.60	N/T	N/T	N/T	P
B	0.410	0.80	0.62	N/T	N/T	N/T	P
C	0.410	0.71	0.60	N/T	N/T	N/T	P
D	0.410	0.70	0.68	N/T	N/T	N/T	P
Low Temp							
A	0.370	0.70	0.630	N/T	N/T	N/T	P
B	0.410	0.72	0.630	N/T	N/T	N/T	P
C	0.440	0.70	0.640	N/T	N/T	N/T	P
D	0.440	0.70	0.680	N/T	N/T	N/T	P
High Temp							
A	0.41	0.70	0.61	N/T	N/T	N/T	P
B	0.45	0.80	0.60	N/T	N/T	N/T	P
C	0.37	0.70	0.61	N/T	N/T	N/T	P
D	0.450	0.70	0.62	N/T	N/T	N/T	P

N/T = No Trip

TABLE 23 (CONTINUED)

AC Switch Module Tests No. 2 Pulsed Load Test No. and Trip Time Limit (sec)							
Circuit	0.140 to 7.0 1	0.31 to 4.1 2	0.25 to 3.0 3	N/T 4	N/T 5	N/T 6	P/F
Room Temp							
A	0.44	0.70	0.61	N/T	N/T	N/T	P
B	0.40	0.78	0.63	N/T	N/T	N/T	P
C	0.45	0.70	0.61	N/T	N/T	N/T	P
D	0.46	0.78	0.66	N/T	N/T	N/T	P
Low Temp							
A	0.4	0.70	0.61	N/T	N/T	N/T	P
B	0.4	0.78	0.66	N/T	N/T	N/T	P
C	0.4	0.70	0.64	N/T	N/T	N/T	P
D	0.42	0.70	0.66	N/T	N/T	N/T	P
High Temp							
A	0.36	0.70	0.72	N/T	N/T	N/T	P
B	0.48	0.78	0.67	N/T	N/T	N/T	P
C	0.40	0.77	0.70	N/T	N/T	N/T	P
D	0.45	0.78	0.66	N/T	N/T	N/T	P

7.5.3 Repetitive Reset

This test requires the SSPC to be tripped and reset 100 times at Trip levels of 4, 7, 10, and 20 A, with each trip being within the time band 0.25 to 3.0 sec, 0.08 to 1.0 sec, 0.04 to 0.6 sec, and 0.01 to 0.2 seconds, respectively. All of the circuits passed these tests.

TABLE 24

REPETITIVE RESET TESTS FOR MODULE NO. 1 AND 2

Module No. 1						Module No. 2					
Repetitive Reset						Repetitive Reset					
Circuit	P/F at Current				P/F	Circuit	P/F at Current				P/F
	4 A	7 A	10 A	20 A			4 A	7 A	10 A	20 A	
Room Temp						Room Temp					
A	P	P	P	P	P	A	P	P	P	P	P
B	P	P	P	P	P	B	P	P	P	P	P
C	P	P	P	P	P	C	P	P	P	P	P
D	P	P	P	P	P	D	P	P	P	P	P
Low Temp						Low Temp					
A	P	P	P	P	P	A	P	P	P	P	P
B	P	P	P	P	P	B	P	P	P	P	P
C	P	P	P	P	P	C	P	P	P	P	P
D	P	P	P	P	P	D	P	P	P	P	P
High Temp						High Temp					
A	P	P	P	P	P	A	P	P	P	P	P
B	P	P	P	P	P	B	P	P	P	P	P
C	P	P	P	P	P	C	P	P	P	P	P
D	P	P	P	P	P	D	P	P	P	P	P

7.5.4 Reset Action and Trip Indication

The reset action and trip indication tests are intended to verify that once tripped, the SSPC will remain tripped for transients on the control line of less than 4.0 msec in duration, but will reset for a pulse greater than 10 msec. In addition, the Trip Indication shall be shown capable of sinking 10 mA with a voltage drop of less than 1.5 V. No difficulty was found with the trip indication; failures in reset action were due to the inability of the SSPC to respond to the control input at an extreme temperature. Once returned to an ambient temperature of +25 °C, normal operation always resumed. Corrective action here would be the selection of a less temperature dependent core material in the control input transformer, to reduce the loss of magnetic properties over the temperature range.

TABLE 25

RESET ACTION AND TRIP INDICATION TEST FOR AC SWITCH MODULE NO. 1 AND 2

AC Switch Module Tests No. 1

Reset Action		Trip Indication		
Circuit	P/F	Circuit	Voltage Drop at 10 mA	P/F
Room Temp		Room Temp		
A	P	A	1.268	P
B	P	B	1.288	P
C	P	C	1.255	P
D	P	D	1.238	P
Low Temp		Low Temp		
A	P	A	1.285	P
B	P	B	1.273	P
C	P	C	1.263	P
D	P	D	1.247	P
High Temp		High Temp		
A	P	A	1.28	P
B	F	B	1.28	P
C	P	C	1.26	P
D	P	D	1.25	P

TABLE 25 (CONTINUED)

AC Switch Module Tests No. 2

Trip Indication			Reset Action (>4 and ≤6)	
Circuit	Voltage Drop at 10.0 mA	P/F	Circuit	P/F
Room Temp			Room Temp	
A	1.245	P	A	P
B	1.260	P	B	P
C	1.255	P	C	P
D	1.248	P	D	P
Low Temp			Low Temp	
A	1.267	P	A	P
B	1.284	P	B	P
C	1.280	P	C	P
D	1.275	P	D	P
High Temp			High Temp	
A	1.255	P	A	P
B	1.278	P	B	P
C	1.268	P	C	P
D	1.263	P	D	P

7.5.5 Leakage Current

The requirement for the leakage current test was to have a leakage of less than 2.0 mA at an SSPC ambient temperature of 71°C from the power switch elements with the full 400 Hz line voltage applied and a 10 ohm load connected from AC Out to Neutral. All circuits passed this test with less than 1 mA being measured.

7.5.6 DC Offset Voltage

With the SSPC on, and the addition of a 10.1 μF capacitor in series with a 300 K resistor connected across the AC In to AC Out terminals, the imbalance of the power switch elements, or dc offset voltage, can be measured. The dc offset is measured at a load current of 0.05, 0.5, and 1.5 A and cannot exceed 0.8, 0.2, and 0.2 V, respectively. All circuits met this requirement.

TABLE 26

DC OFFSET VOLTAGE TEST FOR AC SWITCH MODULE NO. 1 AND 2

Module No. 1

DC Offset

Circuit	DC Offset (mV) at			P/F
	0.05 A	0.5 A	1.5 A	
Room Temp				
A	-30.0	+9.0	+10.9	P
B	-11.4	+7.9	+8.3	P
C	-35.5	+2.0	+4.9	P
D	+76.5	-11.5	-9.1	P
Low Temp				
A	-30.4	+18.0	+19.8	P
B	-7.2	+3.2	+8.1	P
C	-60.0	+2.8	+8.9	P
D	+62.2	-19.0	-21.5	P
High Temp				
A	-20.3	+3.3	+2.7	P
B	-10.4	+4.2	+3.8	P
C	-19.9	+0.9	+1.5	P
D	+60.6	-10.4	-9.5	P

TABLE 26 (CONTINUED)

Module No. 2

DC Offset

Circuit	DC Offset (mV) at			P/F
	0.05 A	0.5 A	1.5 A	
Room Temp				
A	+12.1	+1.9	-0.5	P
B	+0.8	+3.3	+1.9	P
C	+6.7	+2.8	+1.9	P
D	-6.7	+9.0	+4.9	P
Low Temp				
A	+17.9	-1.1	-2.9	P
B	-11.2	+4.2	+5.9	P
C	-0.6	+8.0	+6.7	P
D	+37.0	+7.7	+18.6	P
High Temp				
A	+9.7	+2.4	-0.3	P
B	+4.1	+2.3	+1.8	P
C	+7.9	+1.7	+0.7	P
D	+1.8	+4.0	+2.4	P

7.5.7 Transient Spike Overvoltage

The Transient Spike Overvoltage test consists of applying a +510 V dc and a -510 V dc pulse (with a specific dV/dt rate) with no other power applied while monitoring the AC Out line. Results from the test should indicate, by measuring leakage, that the power switch does not turn on during application of the pulses.

Some difficulty was encountered during performance of this test. The first circuits exposed to this test were destroyed internally. It was hypothesized that the control hybrids involved contained helium, thus lowering the internal breakdown voltage capabilty, with flashover resulting. Later units from which these test results originated experienced no difficulty with flashover, although leakage failures were detected, especially on Module No. 2. A possible corrective action for these failures would consist of a redesign of the snubber network for less variation of parameters with temperature.

TABLE 27

TRANSIENT SPIKE OVERVOLTAGE FOR AC SWITCH MODULE NO. 1 AND 2

Module No. 1

Transient Spike Overvoltage	
Circuit	P/F
Room Temp	
A	P
B	P
C	P
D	P
Low Temp	
A	P
B	P
C	P
D	P
High Temp	
A	F
B	P
C	P
D	P

Module No. 2

Transient Spike Overvoltage	
Circuit	P/F
Room Temp	
A	F
B	F
C	F
D	F
Low Temp	
A	P
B	F
C	F
D	F
High Temp	
A	F
B	F
C	F
D	F

7.5.8 Waveform Distortion

After measuring distortion for "line and load", the difference between the distortion of the 400 Hz line power and the AC Output power must not exceed 6.0 V peak. Measurements were taken at 0.05, 0.5, and 1.5 A. No difficulty in meeting the requirements were encountered.

TABLE 28

WAVEFORM DISTORTION TESTS FOR AC SWITCH MODULE NO. 1 AND 2

AC Switch Module Tests No. 1	
Waveform Distortion	
Circuit	P/F
Room Temp	
A	P
B	P
C	P
D	P
Low Temp	
A	P
B	P
C	P
D	P
High Temp	
A	P
B	P
C	P
D	P

AC Switch Module Tests No. 2	
Waveform Distortion	
Circuit	P/F
Room Temp	
A	P
B	P
C	P
D	P
Low Temp	
A	P
B	P
C	P
D	P
High Temp	
A	P
B	P
C	P
D	P

7.5.9 Voltage Drop

The SSPC is required to meet certain limits for allowable line drop during ON conditions. The voltage drop across the SSPC cannot exceed 1.6, 1.9, and 2.2 V rms at 0.2, 1.0, and 2.0 A, respectively, when measured from AC In to AC Out with a true rms meter. Every circuit tested met this requirement.

TABLE 29

VOLTAGE DROP TESTS FOR AC SWITCH MODULE NO. 1 AND 2

AC Switch Module Tests No. 1

Circuit	Voltage Drop at			P/F
	0.2 A	1.0 A	2.0 A	
Room Temp				
A	0.793	1.069	1.40	P
B	0.832	1.098	1.42	P
C	0.800	1.070	1.40	P
D	0.819	1.085	1.42	P
Low Temp				
A	0.974	1.27	1.62	P
B	0.989	1.30	1.65	P
C	0.991	1.28	1.64	P
D	0.978	1.26	1.62	P
High Temp				
A	0.712	1.025	1.435	P
B	0.757	1.040	1.430	P
C	0.715	1.030	1.435	P
D	0.722	1.020	1.400	P

AC Switch Module Tests No. 2

Circuit	Voltage Drop at			P/F
	0.2 A	1.0 A	2.0 A	
Room Temp				
A	0.820	1.07	1.45	P
B	0.80	1.06	1.42	P
C	0.791	1.06	1.42	P
D	0.805	1.07	1.41	P
Low Temp				
A	0.925	1.18	1.49	P
B	0.920	1.14	1.45	P
C	0.920	1.14	1.46	P
D	0.935	1.15	1.47	P
High Temp				
A	0.675	1.00	1.41	P
B	0.670	0.98	1.37	P
C	0.680	0.98	1.40	P
D	0.685	0.97	1.39	P

7.5.10 Power Dissipation

The requirement for this test is for the SSPC to meet certain maximum power dissipation levels at 0.2, 1.0, and 2.0 A. The levels are 2.25, 2.6, 3.8, and 5.5 W, respectively. All circuits passed this test.

TABLE 30

POWER DISSIPATION TESTS FOR AC SWITCH MODULE NO. 1 AND 2

Power Dissipation

Circuit	Power (W) at			P/F
	No Load	1.0 A	2.0 A	
Room Temp				
A	1.807	2.876	4.607	P
B	1.807	2.905	4.647	P
C	1.807	2.877	4.607	P
D	1.807	2.892	4.647	P
Low Temp				
A	2.074	3.344	5.314	P
B	2.074	3.374	5.374	P
C	2.074	3.354	5.354	P
D	2.074	3.334	5.314	P
High Temp				
A	1.842	2.867	4.712	P
B	1.842	2.882	4.702	P
C	1.842	2.872	4.712	P
D	1.842	2.862	4.642	P

TABLE 30 (CONTINUED)

Module No. 2

Power Dissipation

Circuit	No Load	Dissipation at			P/F
		0.2 A	10 A	2.0 A	
Room Temp					
A	1.634	1.817	2.723	4.553	P
B	1.634	1.813	2.713	4.493	P
C	1.634	1.811	2.713	4.493	P
D	1.634	1.814	2.723	4.454	P
Low Temp					
A	1.93	2.115	3.11	4.91	P
B	1.93	2.114	3.07	4.83	P
C	1.93	2.114	3.07	4.85	P
D	1.93	2.117	3.08	4.87	P
High Temp					
A	1.653	1.788	2.653	4.473	P
B	1.653	1.787	2.633	4.393	P
C	1.653	1.789	2.633	4.453	P
D	1.653	1.79	2.623	4.433	P

7.5.11 Rectified AC Output

To meet the Rectified AC Output test, the SSPC is required to supply fully rectified ac at a current level of 200 mA. In addition, application and removal times of the voltage are required to be less than or equal to 10 msec. All circuits passed this requirement, except for Circuit D on Module No. 2 at $T_A = 55\ ^{\circ}C$. The failure was due to lack of response by the circuit to the control input.

TABLE 31

RECTIFIED AC OUTPUT TESTS FOR AC SWITCH MODULE NO. 1 AND 2

AC Switch Module No. 1 Tests	
Rectified AC Response Must Be ≤10 msec	
Circuit	P/F
Room Temp	
A	P
B	P
C	P
D	P
Low Temp	
A	P
B	P
C	P
D	P
High Temp	
A	P
B	P
C	P
D	P

AC Switch Module No. 2 Tests	
Rectified AC Response Must Be ≤10 msec	
Circuit	P/F
Room Temp	
A	P
B	P
C	P
D	P
Low Temp	
A	P
B	P
C	P
D	F
High Temp	
A	P
B	P
C	P
D	P

7.5.12 High Current Trip Out Time

During this test, the SSPC is to conduct fault currents of 30, 50, 100, 200, 300, and 400 A (±10 percent). Maximum trip times allowed are 0.1, 0.045, 0.015, 0.005, 0.0025, and 0.0015 sec. Some difficulty in generating currents above 200 A was encountered. The maximum current capability of the 400 Hz source being used was found to be 188 A rms, or 266 A peak. All circuits passed the 188 A fault current and "fast tripped" (conducted for one half cycle of the 400 Hz waveform) for each of 30, 50, 100, and 188 A faults.

7.5.13 Fail Safe

Fail Safe testing was performed excluding the explosive atmosphere part of the test. Seven SSPC circuits, with the SCRs shorted, were subjected to seven levels of current. Fuse clearing times were recorded for each of the currents and were to be within certain limits. The currents were 6, 10, 15, 20, 40, 100, and 300 A.

Maximum allowable fuse clearing times were 200, 5, 2, 1.3, 0.4, 0.09, and 0.014 sec, respectively. All fuses tested cleared the faults successfully.

TABLE 32

FAIL SAFE FUSE TESTS

Fail Safe (T_A = +25°C)

Fault Current (A)	Fuse Clearing Time (sec)		P/F
	Maximum Allowed	Actual	
6	200.0	22.0	P
10	5.0	1.85	P
15	2.0	0.60	P
20	1.3	0.36	P
40	0.4	0.085	P
100	0.09	0.020	P
300	0.014	0.00375	P

7.5.14 Control Input Impedance and Turn-on/Turn-off Voltage Tests

The SSPC is required to turn-on and turn-off when certain voltages are applied to the control input. The SSPC must turn on when this voltage is greater than 3.0 V dc and turn off when the voltage is less than 2.0 V dc. It must not respond to a "true" control input ($\geq$3.0 V) when it is applied for $\leq$4.0 msec. Lastly, the control input impedance must be high enough so that the control current will not exceed 3.3 mA when 6.0 V dc is applied. No difficulty in meeting the impedance requirement was met, but the Turn-Off section had failures at extreme temperatures. This is due to the use of an improper type of transformer core material used in the Control Hybrid, that loses part of its magnetic properties at temperature extremes. This causes a failure in the control input section, which results in the "no response to control" mode mentioned earlier. A more suitable material was selected.

TABLE 33

CONTROL INPUT IMPEDANCE TESTS FOR AC SWITCH MODULE NO. 1 AND 2

Control Input Impedance AC Switch Module No. 1 Tests

Circuit	Current Drawn at						P/F
	1.0 V	2.0 V	3.0 V	4.0 V	5.0 V	6.0V	
Current Limits	0-2.7 mA	0-2.7 mA	1-2.7 mA	1-2.9 mA	1-3.1 mA	1-3.3 mA	
Room Temp							
A	0.13	0.67	2.32	2.60	2.88	3.15	P
B	0.16	0.67	2.26	2.55	2.83	3.11	P
C	0.13	0.58	2.31	2.63	2.91	3.18	P
D	0.14	0.65	2.30	2.59	2.86	3.13	P
Low Temp							
A	0.075	0.625	2.37	2.66	2.93	3.21	P
B	0.099	0.662	2.31	2.61	2.88	3.16	P
C	0.060	0.535	2.36	2.69	2.97	3.24	P
D	0.082	0.613	2.34	2.64	2.91	3.18	P
High Temp							
A	0.15	0.65	2.25	2.55	2.83	3.10	P
B	0.18	0.64	2.20	2.50	2.78	3.06	P
C	0.15	0.59	2.25	2.57	2.85	3.12	P
D	0.16	0.62	2.23	2.53	2.81	3.08	P

TABLE 33 (CONTINUED)

Control Input Impedance AC Switch Module No. 2 Tests

Circuit	Current Drawn at						P/F
	1.0 V	2.0 V	3.0 V	4.0 V	5.0 V	6.0V	
Current Limits	0-2.7 mA	0-2.7 mA	1-2.7 mA	1-2.9 mA	1-3.1 mA	1-3.3 mA	
Room Temp							
A	0.146	0.670	2.28	2.56	2.85	3.12	P
B	0.146	0.634	2.28	2.57	2.85	3.12	P
C	0.161	0.650	2.15	2.45	2.73	2.99	P
D	0.146	0.652	2.22	2.52	2.80	3.07	P
Low Temp							
A	0.09	0.66	2.35	2.64	2.92	3.19	P
B	0.09	0.63	2.36	2.65	2.93	3.20	P
C	0.089	0.63	2.20	2.49	2.77	3.04	P
D	0.078	0.590	2.30	2.59	2.87	3.14	P
High Temp							
A	0.162	0.649	2.22	2.52	2.80	3.07	P
B	0.162	0.616	2.21	2.52	2.79	3.07	P
C	0.178	0.631	2.11	2.40	2.68	2.95	P
D	0.162	0.636	2.17	2.47	2.75	3.02	P

TABLE 34

TURN-ON/TURN-OFF VOLTAGE TESTS FOR AC SWITCH MODULE NO. 1 AND 2

Turn On/Off Voltage

$2.0 \leq$ Turn On/Off ≤ 3.0 V

Circuit	Module No. 1 P/F	Module No. 2 P/F
Room Temp		
A	P	P
B	P	P
C	P	P
D	P	P
Low Temp		
A	P	P
B	P	P
C	P	P
D	F	P
High Temp		
A	P	P
B	F	P
C	P	P
D	P	P

7.6 Comments and Conclusions

The module tests of the SSPC circuits indicated that the design conforms to the greater part of the test requirements. However, some difficulties were encountered involving the Control Hybrid. The Control Hybrids used were the devices available at the time of termination of the B-1 contract. At that time, no Control Hybrids had passed the entire set of acceptance tests conducted by the vendor and many lacked the corrective actions detailed in paragraph 5.6.1 of this report. It is expected that 100 percent tested Control Hybrids that had the noted corrective actions incorporated would eliminate all tests deviations except for $\pm$50 mA tolerance required for ZIC. It is concluded that the latter would require specially selected SCRs as a minimum.

The SSPCA chassis passed the Insulation and Bonding Resistance tests with no difficulty and the DWV tests, when several chassis areas, plus several pins in the interface connector devoid of the proper insulation coating were brought up to specification.

The Logic and Status Hybrid tests were also successful.

It is concluded that the SSPC is a reliable, operational design ready for use in a Military Avionics System.

SECTION VIII
CONCLUSIONS

Based on the B-1 aircraft development experience, it is concluded that power controllers, using solid state components for sensing and switching, more closely achieve the requirements of a modern aircraft power control system than electro-mechanical designs. SSPCs with digitally computed trip times and printed circuit board packaging are the solid state design approaches preferred. A detailed list of conclusions follows.

1) Rockwell International initially considered an analog design for providing timing, control, and trip time functions but decided that a digital mechanization provided more promise. It also appeared that a CMOS on sapphire digital device offered the following additional advantages:

   a) Trip time stability
   b) Nuclear hardness to B-1 requirements
   c) Low power dissipation
   d) Small size

These advantages were subsequently confirmed during the development program.

2) As is typical with most LSI circuits, the initial development problems of the Monolithic required several design iterations. The problems were mainly process related (see paragraph 4.17). However, after these design iterations, the problems were solved and the Monolithic was operational and ready for large scale use. Since an LSI circuit is relatively easy to build, it is expected that the cost of the device, in large quantities, will be low.

   The potential for adding functions to the Monolithic chip or modifying existing circuits is available, if required. Adding functions to the chip that were previously performed by circuits in the Hybrids would tend to reduce the cost of the SSPCs.

3) Sensing the load current by means of measuring the voltage across a resistor in series with the line fits in nicely with the power control mechanization selected:

   a) The voltage is read directly by the ADC in the Monolithic.
   b) The sense resistor aids in limiting the magnitude of the rupture currents.
   c) The sense resistor is small, inexpensive, and reliable.

   Hall effect devices were investigated briefly for use as the current sensor, but were ruled out. Their advantage (electrical isolation and sensing of alternating or direct currents) was outweighed by their apparent disadvantages (size and design risk).

4) The Threshold Detector is considered to be an excellent solution for circuits that require a narrow voltage threshold (0-2 V dc "OFF", 3-6 V dc "ON") combined with low input current drain (3.3 mA maximum) and wide temperature operation (-55 to 125°C).

5) The "flyback" transformer scheme (Control Input, Trip and Status output) provides both the required one megohm isolation between Control, Trip and Status circuits, and also isolation of these circuits from the 230 V line. The 100 kHz drive signal is readily available from the Monolithic clock. This type of isolation is simple and reliable and should be considered for use in circuits with similar requirements.

6) Using 50 kHz SCR gate drive reduced drive power dissipation to 50 percent of that required with dc. The 50 kHz signal is also readily available in the Monolithic.

7) The decision to use plug-in printed circuit boards was correct. The plug-in feature makes module replacement easy. The heat rails function both as a method to cool the component parts and to attach the module to the heat exchanger. The plated copper lines were designed wide enough to handle the operating and rupture currents. All plated through holes were completely filled with solder and the component lead to eliminate the possibility of local hot spots. DWV requirements were met by spacing high voltage pins sufficiently far apart. The board material (polyurethane) is an excellent electrical insulator.

8) The module connector is excellent for its stated (moderate current) design applications. However, a connector more suited to the magnitude of rupture currents experienced should be used in future power configurations.

9) Development and fabrication of the Power, Logic, and Status Hybrids were relatively problem-free compared to the Control Hybrid. This was due to the functional complexity of the latter. It would be desirable to reduce the number of parts in the Control Hybrid to make it less expensive to fabricate.

10) Straight through, solid pins in hybrid packages should be used in place of intermediate plated feed-throughs where high currents (rupture level) can be expected. This conforms with normal high current design practice, where sharp (90 deg) turns are to be avoided.

11) The Logic and Status Hybrid designs are excellent solutions to unique circuit requirements. However, it would be desirable to review the system isolation requirements to determine if standard integrated circuits supplemented with simple, individual power supplies could be used in place of custom hybrids.

12) The SSPCA is an effective method of providing a flexible, maintainable, low life cycle cost, power control subassembly. The MIB effectively substitutes a batch produced interconnection method for the conventional handwiring used in EMPCAs. Some failures were experienced during the DWV test of the SSPCA. The problem was found to be external to the MIB - arcing occurred where the conventional wires (the connection between the MIB and the SSPCA interface connectors) were stripped and soldered to the MIB. Proper application of the protective, insulating coating at the point of wire egress, as specified on the assembly drawing, corrected the problem.

No other problems were experienced with the design, fabrication and test of the SSPCA chassis.

SECTION IX
RECOMMENDATIONS

Mechanization of power control circuits with solid state components is recommended in aircraft system applications where size, weight, power dissipation, and electromagnetic interference must be held to a minimum and reliability and operational capability at a maximum. It is further recommended that a solid state power controller designed with the circuit elements listed below is the preferred configuration (see Section VIII Conclusions).

1) A CMOS on sapphire digital device (Monolithic) providing Control and Trip Time Functions.

2) Transformer coupled SCR gate drive

3) Printed circuit board modules

4) Printed circuit MIB

In systems where a moderate (1 W) increase in power dissipation and a wider (0 to 2 V OFF, 4 to 6 V ON) Control Input threshold can be tolerated, a variation of the SSPC design is recommended that retains the Monolithic and transformer coupled switches but uses discrete parts in place of the Control Hybrid. Such a change would further reduce the material costs of the SSPC.

The change would result in a reduction in the number of parts presently used. Approximately 27 parts could be eliminated by performing the following redesign:

1) Add ZVC circuitry to the Monolithic

2) Simplify the 2.5 and 5 msec timers

3) Add +9 V and +12 V regulators to the Monolithic

4) Derive power for SCR gate drive from the rectified unregulated 35 V ac. This would cause an increase in maximum power dissipation of approximately 1 W.

5) Simplify the Control Input threshold circuit in accordance with the modified (0 to 2 V, 4 to 6 V) requirements.

Eliminating the Status circuit would eliminate an additional 10 parts.

The Control Input circuit could be modified to include the capability to perform the AND and OR functions presently performed by the Logic Hybrid. One possible mechanization of the logic functions is with CMOS amplifiers added to, but electrically independent from the Monolithic.

For future, higher current SSPC configurations it is recommended that a module connector specifically designed to withstand the high levels of DWV and rupture currents be used. The distance between pins required for DWV could be achieved by lengthening the conductive path in both the vertical and horizontal directions rather than just the latter. One method is to use a molded plastic connector with each pin in a well. Solid, round, substantial pins that avoid any necking areas (or areas of localized high resistance) should be used. The redesigned connector would provide an additional safety factor with only a moderate increase in cost.

In conclusion, a design change under consideration at the time of B-1 contract termination is highly recommended. Consider the simplified EMUX/PCA interface shown in Figure 44 below:

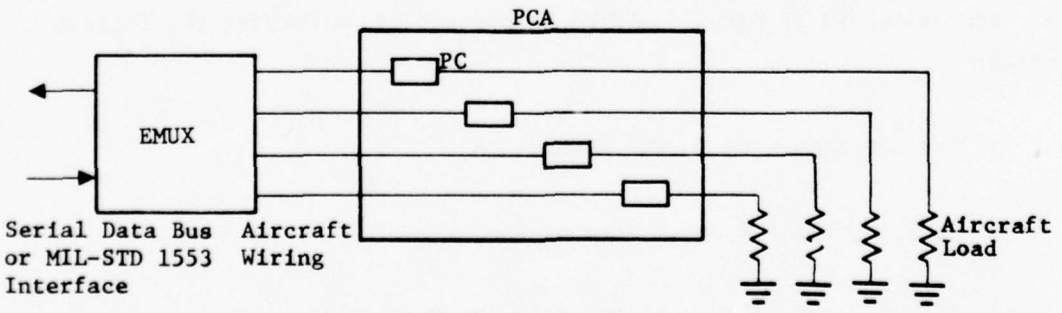


Figure 44. EMUX/PCA Interface

A significant amount of aircraft wiring (in the B-1 the estimate was 5200 wires) could be eliminated by modifying the above interface as shown in Figure 45 below.

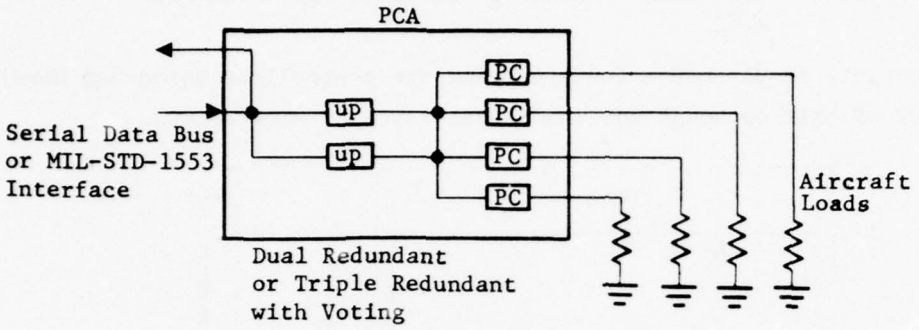


Figure 45. Reduction of Aircraft Wiring

APPENDIX A

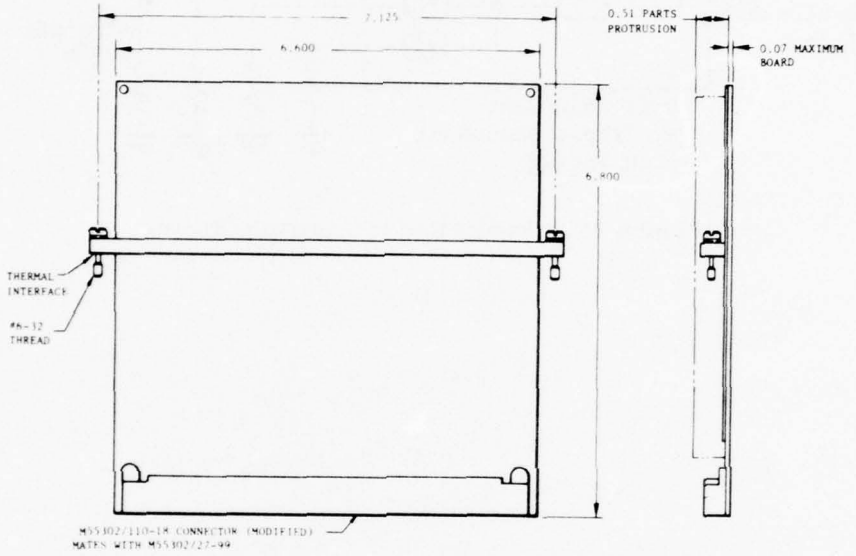
MIL-P-81653 (RECOMMENDED)

MILITARY SPECIFICATION SHEET

POWER CONTROLLER, AC LOAD SWITCHING

SPST, NORMALLY OPEN OR NORMALLY CLOSED 0 THRU 2 AMPERES

The complete requirements for procuring the controllers described herein shall consist of this document and the latest issue of MIL-P-81653.



1 AC OUTPUT D	29 D CONTROL IN	57 *	85 C TRIP
2 *	30 D CONTROL RETURN	58 *	86 B CONTROL RETURN
3 *	31 A TRIP	59 SPARE	87 B CONTROL IN
4 RECTIFIED AC -OUT D	32 S/T RETURN	60 *	88 B CITS STATUS
5 *	33 A STATUS	61 *	89 B STATUS
6 *	34 A CITS STATUS	62 SPARE	90 S/T RETURN
7 RECTIFIED AC +OUT D	35 A CONTROL IN	63 *	91 B TRIP
8 *	36 A CONTROL RETURN	64 *	92 AC INPUT NEUTRAL
9 *	37 SHIELD	65 SELECT IN C	93 *
10 AC OUTPUT C	38 *	66 *	94 *
11 *	39 *	67 *	95 RECTIFIED AC +OUT B
12 *	40 SPARE	68 RECTIFIED AC +OUT C	96 *
13 SPARE	41 *	69 *	97 *
14 *	42 *	70 *	98 RECTIFIED AC -OUT B
15 *	43 SPARE	71 RECTIFIED AC -OUT C	99 *
16 SPARE	44 *	72 *	100 *
17 *	45 *	73 *	101 AC SELECT IN
18 *	46 AC OUTPUT B	74 AC INPUT	1G2 *
19 AC INPUT	47 *	75 AC INPUT	103 *
20 AC INPUT	48 *	76 *	104 SPARE
21 *	49 RECTIFIED AC -OUT A	77 *	1C5 *
22 *	50 *	78 *	106 *
23 *	51 *	79 AC INPUT NEUTRAL	107 SPARE
24 SHIELD	52 RECEIFIED AC +OUT A	80 C CONTROL RETURN	108 *
25 D TRIP	53 *	81 C CONTROL IN	109 *
26 S/T RETURN	54 *	82 C CITS STATUS	110 AC SELECT IN
27 D STATUS	55 AC OUTPUT A	83 C STATUS	
28 D CITS STATUS	56 SELECT IND	84 S/T RETURN	

*PINS REMOVED TO PROVIDE ISOLATION REQUIRED FOR 230V OPERATION.

REQUIREMENTS:

MECHANICAL AND DIMENSIONAL CHARACTERISTICS

Configuration	See Page 1
Dimensions	Inches
Tolerances	±0.03 for two place decimals
	±0.01 for three place decimals
Enclosure	Not applicable
Weight	1 lb
Mounting torque	Not applicable
Leak rate	Not applicable

THERMAL CHARACTERISTICS

Thermal resistance module mounting tab to heat exchanger	0.6 °C/ W with
Heat exchanger temperature	70 °C maximum

ELECTRICAL CHARACTERISTICS (-54 to

General

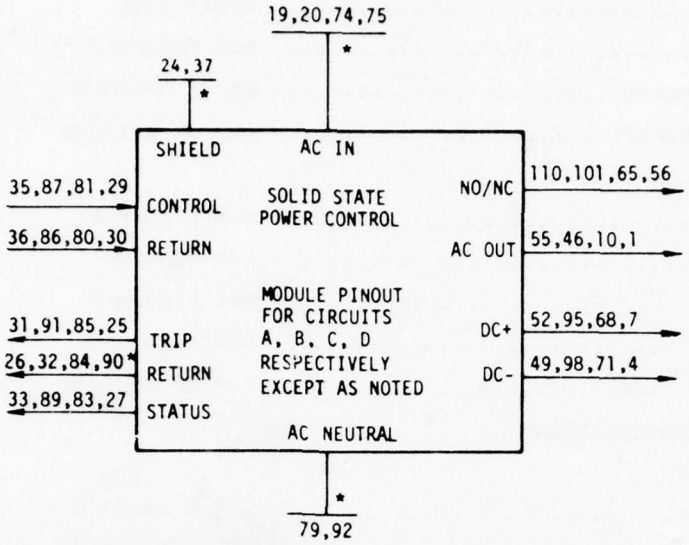
Circuit arrangement	SPST NO or NC (see Figure 1)
Insulation resistance	100 megohms minimum
Dielectric withstanding voltage:	
230 V lines	1300 V rms at sea level
	800 V rms at 70,000 ft
non-230 V lines	900 V rms at sea level
	200 V rms at 70,000 ft
Isolation	
Life (operating hours)	125,000 minimum
Radio interference	applicable
Leakage current	2.0 mA at 75 °C
Power dissipation	
'ON'	5.5 W at 2 A
'OFF'	2.25 W
Common mode rejection	±10 V peak, 1 Hz to 100 kHz

MIL-P-81653 (RECOMMENDED)

Power Circuit

Supply Voltage	
Steady state	see Figure 2
Transients (long term)	see Figure 2
Transients (short term)	see Figure 2
Current	
Rated (no load to 100% rated)	0-2 A 400 Hz
	0-200 mA DC
Frequency (rated)	400 Hz ± 5%
Voltage drop	
No load	1.5 V
100% load	2.2 V
Current limiting	
Ripple current	Not applicable
Rupture capacity	400 A
DC offset voltage:	
No load	1 V
Load	0.2 V, 0.2 A to 2.0 A
Overshoot current	Not applicable
Fail safe current	see Figure 3
Reset immunity	applicable
Transients:	
Operating voltage	10 msec maximum
Spike overvoltage	±510 Vdc
Standby power	±510 Vdc
Response:	
Turn-on time	10 msec maximum
Rise-time	Not applicable
Turn off time	10 msec maximum
Fall time	Not applicable

Trip free	applicable
Trip time	see Figure 3
Zero voltage turn-on	±32 V maximum
Zero voltage turn-off	±50 mA maximum
Control Circuit	
Supply voltage	see Figure 4
Current	see Figure 4
Turn-on current	see Figure 4
Turn-off current	see Figure 4
Removal time to reset	4 msec minimum
Environmental Characteristics	
Module Temperature	
Operating	-55 °C to 71 °C
Storage	-65 °C to 150 °C
Shock	
Mechanical	applicable
Temperature	applicable
Vibration	applicable
Acceleration	100 g
Salt fog	applicable
Humidity	applicable
Operation at temperature extremes	applicable
Temperature - altitude	applicable
Operating ambient:	
Temperature	-65 to 71 °C
Altitude	Sea level to 70,000 ft



*COMMON for all four power controller circuits

Figure 1. SSPC Input/Output Diagram

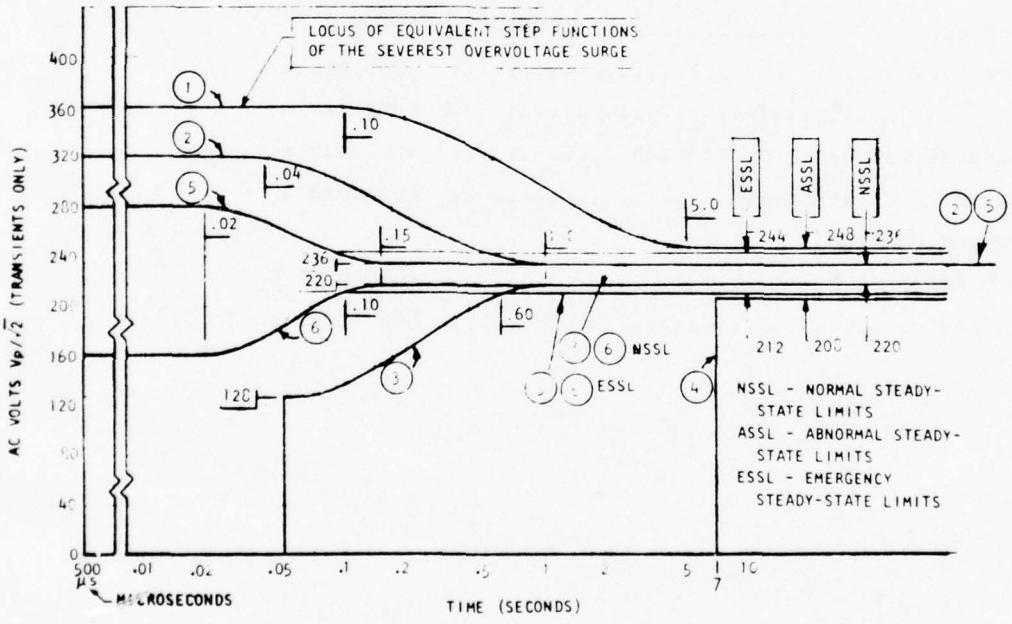


Figure 2. Double Voltage AC Power, Transient Surge AC Voltage Step Function Loci Limits for Category A Equipment

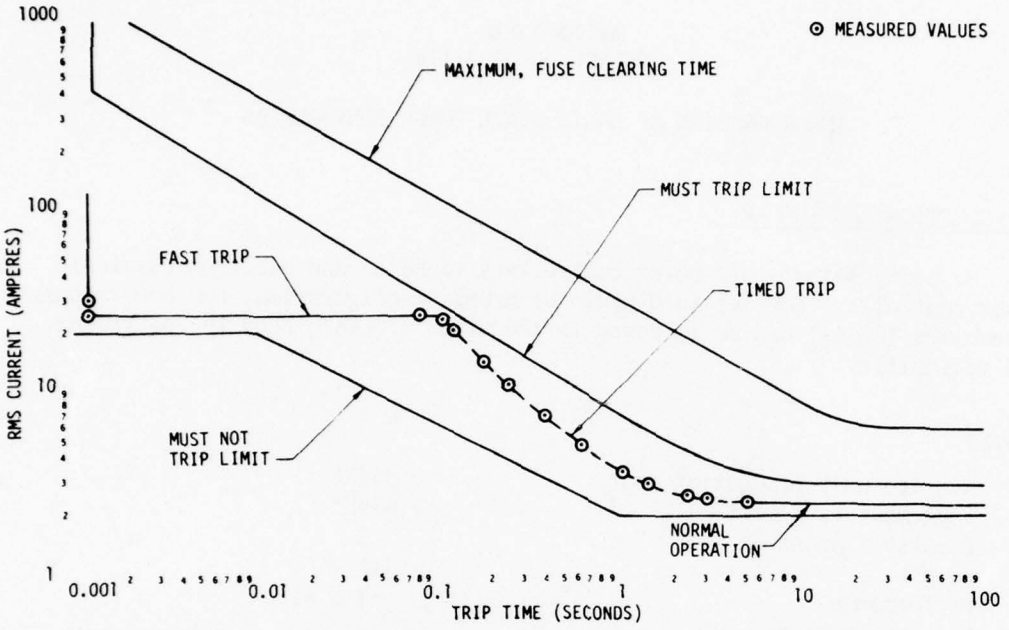


Figure 3. Timed Trip and Fuse Clearing Time Requirements

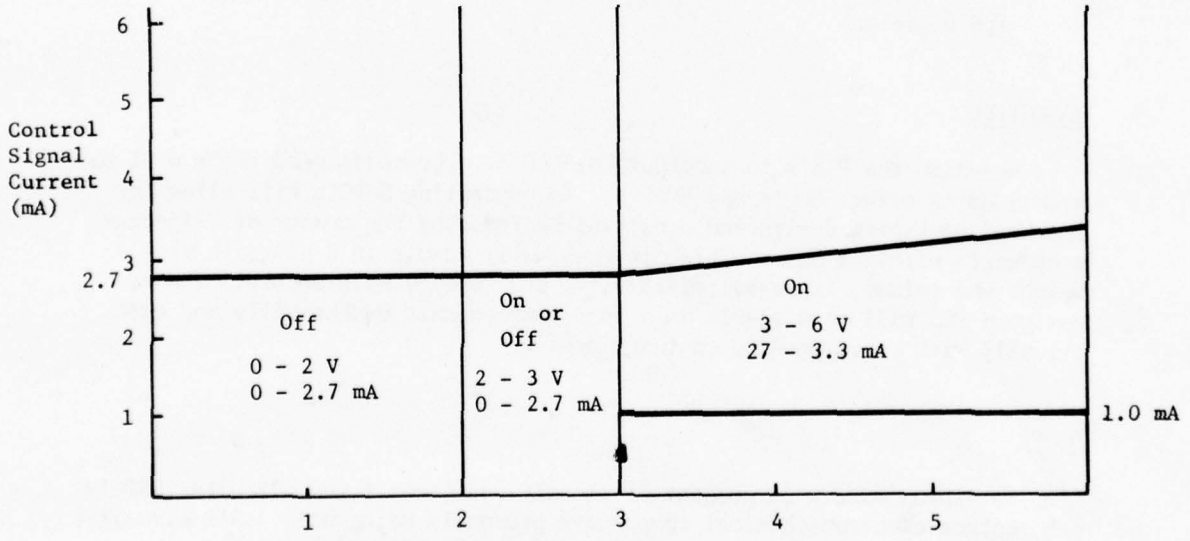


Figure 4. Turn-on/off Voltage Requirements

APPENDIX B
CONTROL NO. 309-118

INCORPORATION OF SOLID-STATE POWER CONTROLLERS

INTRODUCTION AND SUMMARY

By using solid-state power controllers (SSPC's) and electromechanical power controllers (EMP's) in a mixed or hybrid configuration, the power control assemblies (PCA's) can be improved in the areas of cost, density, packaging, and reliability.

IMPACT

Average unit production cost	234K*
Implementation cost	2,929K*
Breakeven point	2
Weight	-211 lb
Performance	+4 n mi
Life cycle costs	
Earliest effectivity	A/V-4

*1,970 dollars

OBJECTIVE

Redesign the PCA's to incorporate SSPC's. The redesigned PCA's will be hybrid units using SSPC's and EMPC's. Incorporating SSPC's will allow for improved packaging design and densities by reducing the number of different components within a unit. This, in turn, will result in a PCA with less weight and volume, improved reliability, and reduced maintenance. The redesigned PCA will also result in a less complex unit mechanically and electrically with corresponding cost savings.

SCOPE

In approximately 50 percent of the air vehicle's 1,200 circuits, SSPC's can replace electromechanical components presently being used. All circuits using SSPC's will require redesign as well as the PCA and its supporting structure and trays.

As presently configured, the central avionic bays have a total of 10 PCA's. Incorporating SSPC's will permit consolidating these into four to six units total. This change would also require a redesign of the bus distribution system to these units.

DESCRIPTION

To incorporate SSPC's into the power distribution system will require a complete redesign of the PCA's from both a packaging and circuit standpoint. The current PCA design concept of changing one component on the air vehicle without removing or electrically disconnecting the PCA will be retained.

Internally, the PCA construction will be simplified. The SSPC being a single unit and replacing a number of electromechanical components and their interconnecting wiring will require a less complex support structure. Figure 118-1 notes the two configurations of SSPC's and their suppliers. Figure 118-2 depicts the physical comparison when replacing an EMPC with a SSPC in a single-phase circuit. Figure 118-3 depicts a three-phase EMPC circuit being replaced by single-phase SSPC's.

As previously noted, the redesigned PCA's will be hybrid units. In figure 118-4, it can be seen that for the EMPC's, as presently being used, the components are spread out and require separate support panels with the circuit breakers on the front panel, relays in the center, and drivers on each side and, in addition, a considerable amount of interconnecting wiring. Because the EMPC's require more maintenance, they are mounted in the front section of the inner chassis with the more reliable SSPC's mounted in the aft section. The upper section of the unit houses the electrical connecters and the internal power distribution components. (Refer to appendix B for more detailed information.)

When incorporating SSPC's, considerably less electrical components are required. Table 118-I makes an air vehicle requirement comparison of components required in the current PCA's versus those required in the proposed design incorporating SSPC's. In addition to the foregoing, because there are fewer EMPC's, there will be much less interconnecting wiring in the redesigned PCA.

The outer chassis of the redesigned PCA will also be a less complicated structure. The blind-mated rack and panel connecters are being replaced with hand-mated MIL-C-38999 connecters. This will eliminate the need for heavy machined front and rear panels which will be replaced by extruded angle welded frames. The support housing for the hand-mated connecters will be formed sheet aluminum. Table 118-II notes usage requirements for some of the major mechanical components of the current and proposed designs.

Some minor changes to secondary supporting structure will be required to provide a new mounting tray. A PCA mounting tray with NAS573-type retention hardware will replace the blind-mated connecter and jackscrew retention-type tray currently being used.

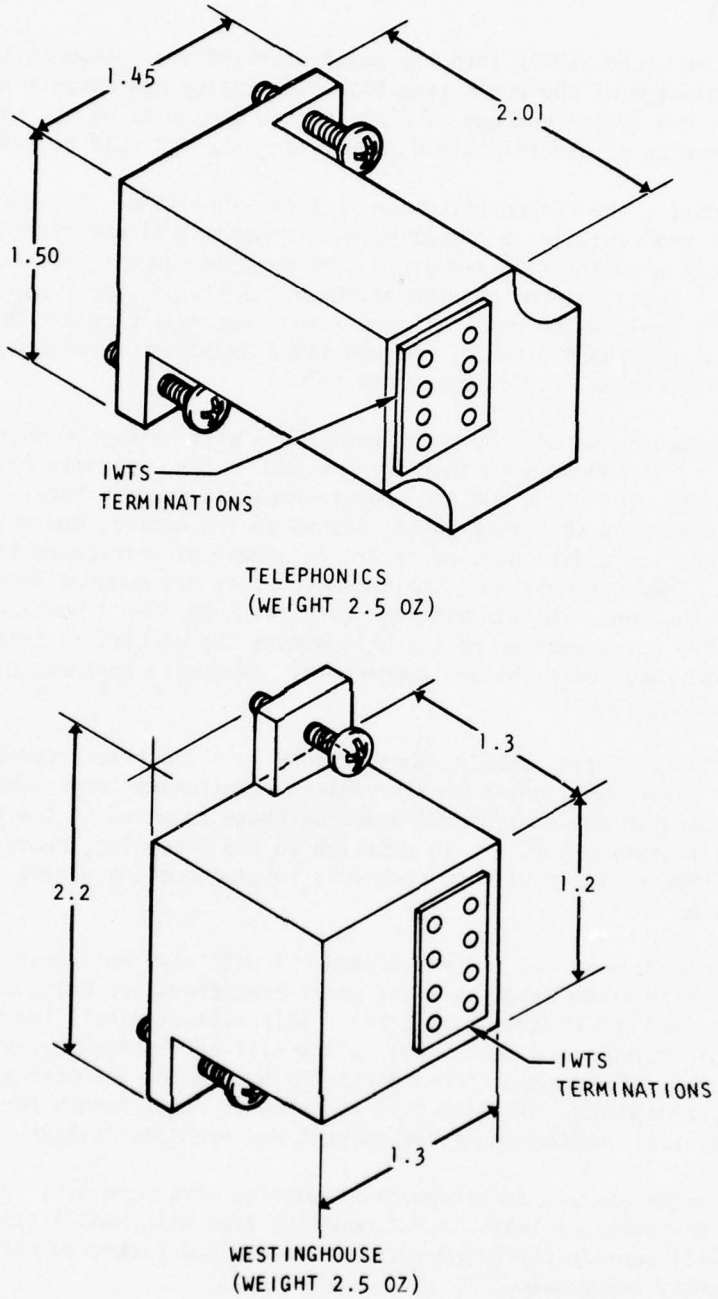
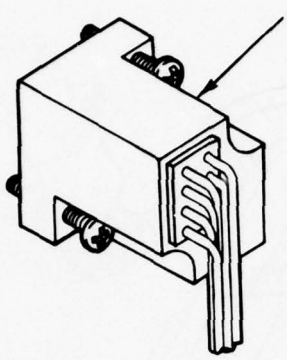


Figure 118-1. SSPC Configuration Currently Under Development (Single-Phase)

THIS



- LESS WEIGHT & VOLUME
- MORE EFFICIENT USE OF VOLUME
- MORE RELIABLE
- SSPC'S CAN REPLACE EMPC HARDWARE IN APPROXIMATELY 670 SINGLE-PHASE CIRCUITS

REPLACES

THESE

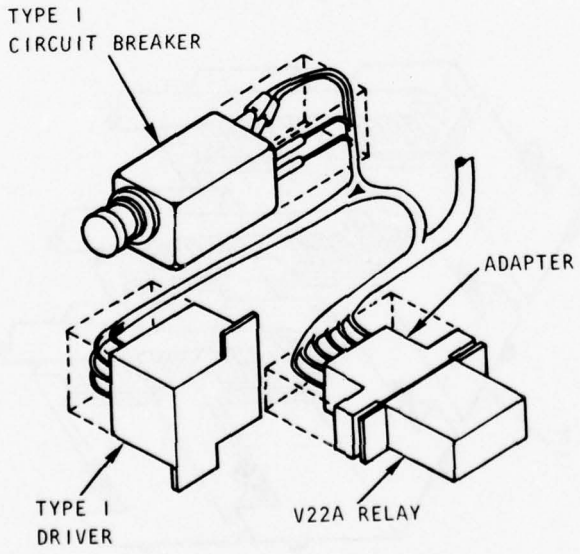
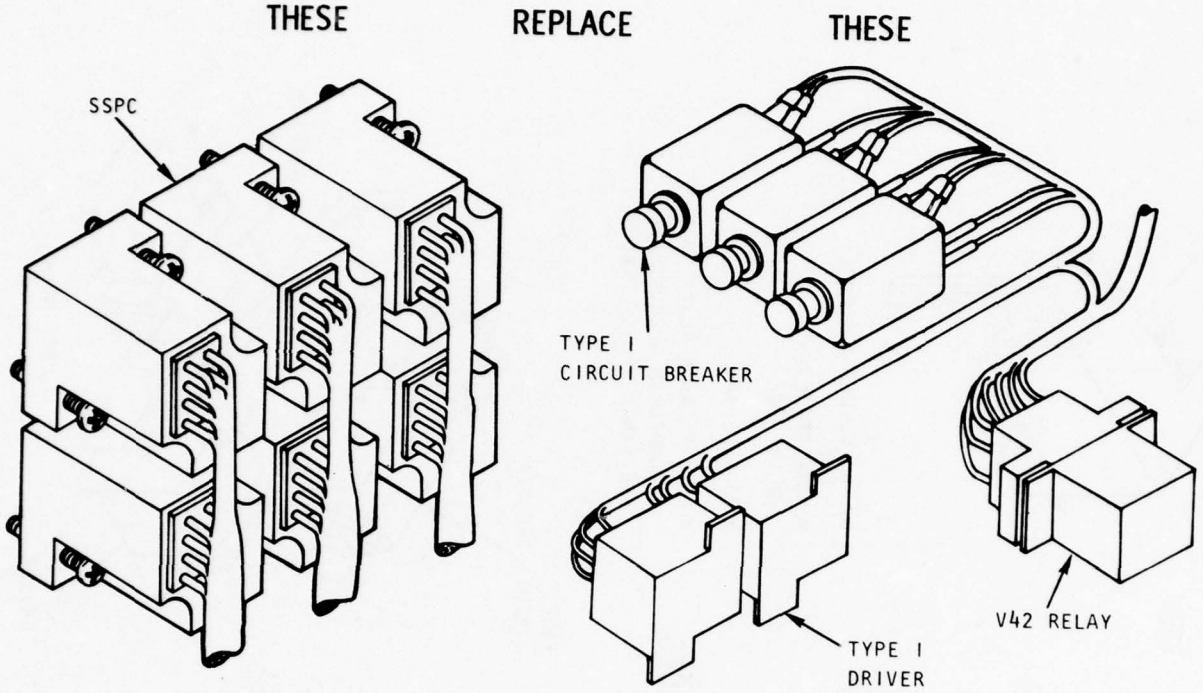


Figure 118-2. SSPC-EMPC Comparison (Single-Phase)



- NO WEIGHT, VOLUME, OR COST REDUCTION BENEFITS WHEN USING 1Ø SSPC'S IN 3Ø CIRCUITS

Figure 118-3. SSPC-EMPC Comparison (Three-Phase)

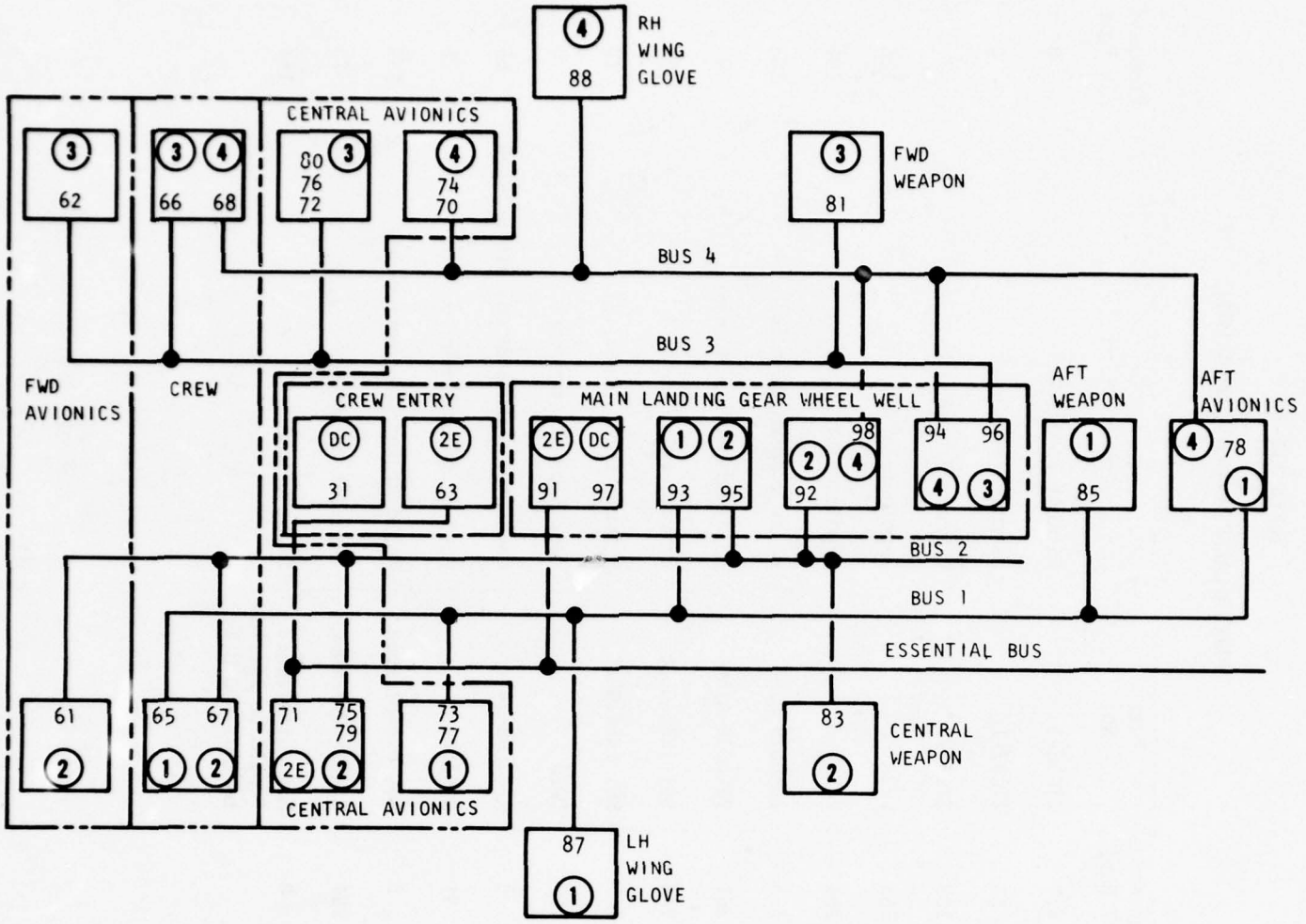


Figure 118-4. Proposed Redesigned PCA-Bus Relationship (A/V-4)

Table 118-I

ELECTRICAL COMPONENT COMPARISON

Current A/V Rqmt	Part No.	Description	Proposed A/V Rqmt
477	2TC36-1	Circuit Breaker	0
64	2TC37-1	Circuit Breaker	0
109	2TC36-2	Circuit Breaker	77
355	V22A	2-pole relay	108
261	V42A	4-pole relay	191
355	20-AB2B-EJA3	Relay adapter (2-pole)	108
261	20-AC2B-AJA6	Relay adapter (4-pole)	191
744	SS1-IR5A-0026	Driver, relay, type I	288
167	SS1-IR5A-0027	Driver, relay, type III	14
59	DPKB	Rack & panel connecter	0
0	MS27508-24	Connecter - Hand-mated, MIL-C-38999	65
31	9002D05-1	Current transformer	25
0	Not established	Solid-state power controller	839
984	LE411-0001-0002	Resistor assembly	70
0	Not established (could be similar to LE417-0010-)	Diode bridge	144

Table 118-II

MECHANICAL COMPONENT COMPARISON

Current A/V Rqmt	Part No.	Description	Proposed A/V Rqmt
34	L5400785	Slide assembly (machined)	0
17	L5400832	Front panel (machined)	0
17	L5400759	Back panel (machined)	0
17	LD181-0003-0001	Jackscrew	0
17	L5403348	Tray (typical)	0
0	L5404541	Tray (typical)	17

In conjunction with the PCA design changes to incorporate SSPC's, the central avionics bay PCA's will be combined to reduce the quantity of units from the current 10 to a total of four to six PCA's. This combining of PCA's will require a change to the power bus distribution system. Figure 118-5 shows the reduction to four PCA's in the central avionics bay and the OCNEE numbers included in each. The PCA OCNEE number bus relationship, shown in figure 118-5, is the same as A/V-3.

WEIGHT

The proposed PCA redesign to incorporate SSPC's will result in a gross weight of -211 pounds per air vehicle. Approximately three-fourths of this is attributed to SSPC being a single unit, substituting for an EMPC made up of various components and their interconnecting wiring. (See figures 118-2 and 118-3.) The remaining one-fourth weight savings is made up by mechanical redesign of the LRU and a change in the PCA support tray. (Refer to appendix A for detail breakdown.)

PERFORMANCE

Aside from having higher reliability (table 118-III), the following are features not available in EMPC's:

1. Trip and reset by EMUX control.
2. EMI reduction.
3. Limits short circuits to low levels.
4. No vibration-induced tripping.

Because of the weight reduction, the air vehicle performance will be improved by the following amounts:

- Subsonic variable penetration +4 n mi
- Supersonic variable penetration +2 n mi

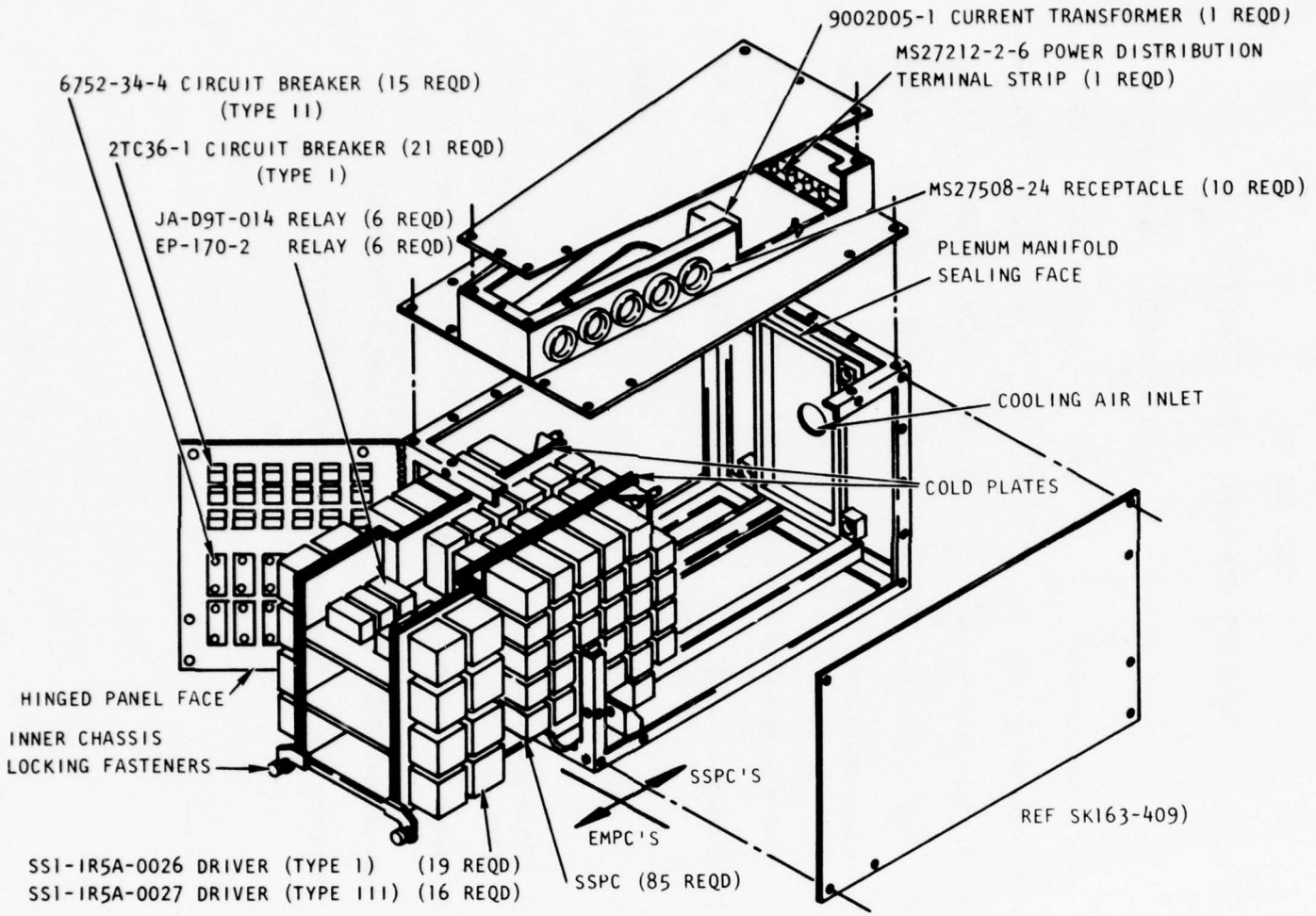


Figure 118-5. Proposed Solid-State Power Control Assembly (Wire Harness Omitted for Clarity)

Table 118-III

RELIABILITY COMPARISON - EMPC VERSUS SSPC

Configuration	Operational MTBF (hr)*		Hardware MTBF (hr)**	
	EMPC	SSPC	EMPC	SSPC
A - Single-phase load	47,148	124,168	22,915	103,018
B - Multiple single-phase load	21,084	41,391	9,832	34,341
C - Single-phase load, "OR" gate	37,994	62,073	20,513	51,520
D - Single-phase load, "AND" gate	37,994	47,259	20,513	25,806
E - Single-phase solenoid load	66,667	121,951	46,490	101,420
F - Three-phase load	29,283	41,391	14,426	34,341
G - Three-phase load, "OR" gate	25,342	25,355 (4 SSPC) 20,704 (6 SSPC)	13,399	15,434 (4 SSPC) 17,704 (6 SSPC)
H - Three-phase load "AND" gate	25,342	26,831	13,399	17,194
I - Three-phase motor reversing	21,070	24,832	10,146	20,602

*Operational MTBF = Loss of function/degraded performance.

**Hardware MTBF = Corrective maintenance/replacement.

RELIABILITY

Mission Reliability*	Quantitative Safety**	Hardware Reliability***
Decrease in failures -4.2	Decrease in failures -2.1	Decrease in CMA's -9000

*Mission failures per 1,000 attempted basic missions.
**Unsafe condition per 10^6 flights.
***Corrective maintenance actions per 10^6 hours

TESTING REQUIREMENTS

The PCA's will not be qualified as a unit. As with A/V-1, 2, and 3, all the components that make up the unit are qualified at the component level. It is planned to environmentally test two complete PCA's for vibration and cooling only - one wheel well and one wing glove. In addition, as soon as production SSPC's become available and A/V-1's test schedule permits, two central avionics bay PCA's will be modified to install SSPC's in noncritical circuits, such as lights, for flight test. Presently, the only SSPC that can be considered for B-1 applications is a single-phase 230-volt, 1.6-ampere unit. Two suppliers (Westinghouse and Telephonics) are currently under contract to AFAPL to develop the unit. Westinghouse will deliver units for test to AFAPL by 1 December 1974. Telephonics will deliver test units sometime in February 1975. To date, there is no qualified SSPC. The proposed A/V-4 production schedule shows that qualified SSPC's must be available no later than 1 April 1977.

Rockwell has done the following SSPC testing to date:

1. EMUX compatibility and weapon bay and position bay lights compatibility, using both Westinghouse and Telephonics SSPC's.

2. Vibration, short-circuit, endurance, and performance tests using Westinghouse plug-in type SSPC's.

The Air Force Aero Propulsion Lab (AFAPL), using B-1 prototype SSPC's, has done some cycling and evaluation tests with motor inductive and resistive loads.

PREVIOUS STUDIES

NA-74-244 is a technical report on the SSPC compatibility considerations. The study was made 8 April 1974 to support an ultimate decision by the Air Force to commit SSPC's for production and use on the B-1.

This study is based on report NA-74-244.

SCHEDULE

The schedule for implementing the proposed redesign of PCA's to incorporate SSPC's is portrayed in figure 118-6. The proposed program, as scheduled, will provide deliverable hardware in time to support A/V-4 manufacturing requirements.

IMPLEMENTATION PLAN

The proposed program is scheduled to begin on 1 June 1975 (A/V-4 contract). A 33-month time period will be required between contract award and final checkout of the last of the 20 redesigned PCA's to be required for A/V-4. Tasks proposed for this period are as depicted in schedule items 7 through 25.

Generation of schematics will begin immediately after contract award, with an estimated 12 months required for completion of this task. Two months of lead time are required between the start of schematic effort and the beginning of the layout task. The start of layout effort is paced by the availability of initial schematics and the completion of a count of the required components by area and bus (schedule item 11). Completion of this count will also allow procurement activity for those components (including SSPC's) required for manufacture of the PCA's to begin (item 22). Procurement lead times for SSPC's are reviewed later in this implementation plan.

Approximately 30 PCA layouts are estimated to be required. These will be produced over a 15-month period beginning on 1 August 1975. Three months after the beginning of this task, the required envelope, termination, and mounting information for the SSPC's will be finalized. Preliminary layouts are scheduled to be released on 1 January 1976. Availability of these preliminary layouts paces the start (1 March 1976) of drawing release (item 17).

A total of 350 PCA drawings are estimated to be required. These drawings will be released over a 14-month period. The last detail drawing is scheduled to be released on 1 November 1976. The start of fabrication effort (item 25) has been timed to coincide with this event. Release of PCA air vehicle installation drawings (item 29) is scheduled to run concurrently with PCA detail and assembly drawing release.

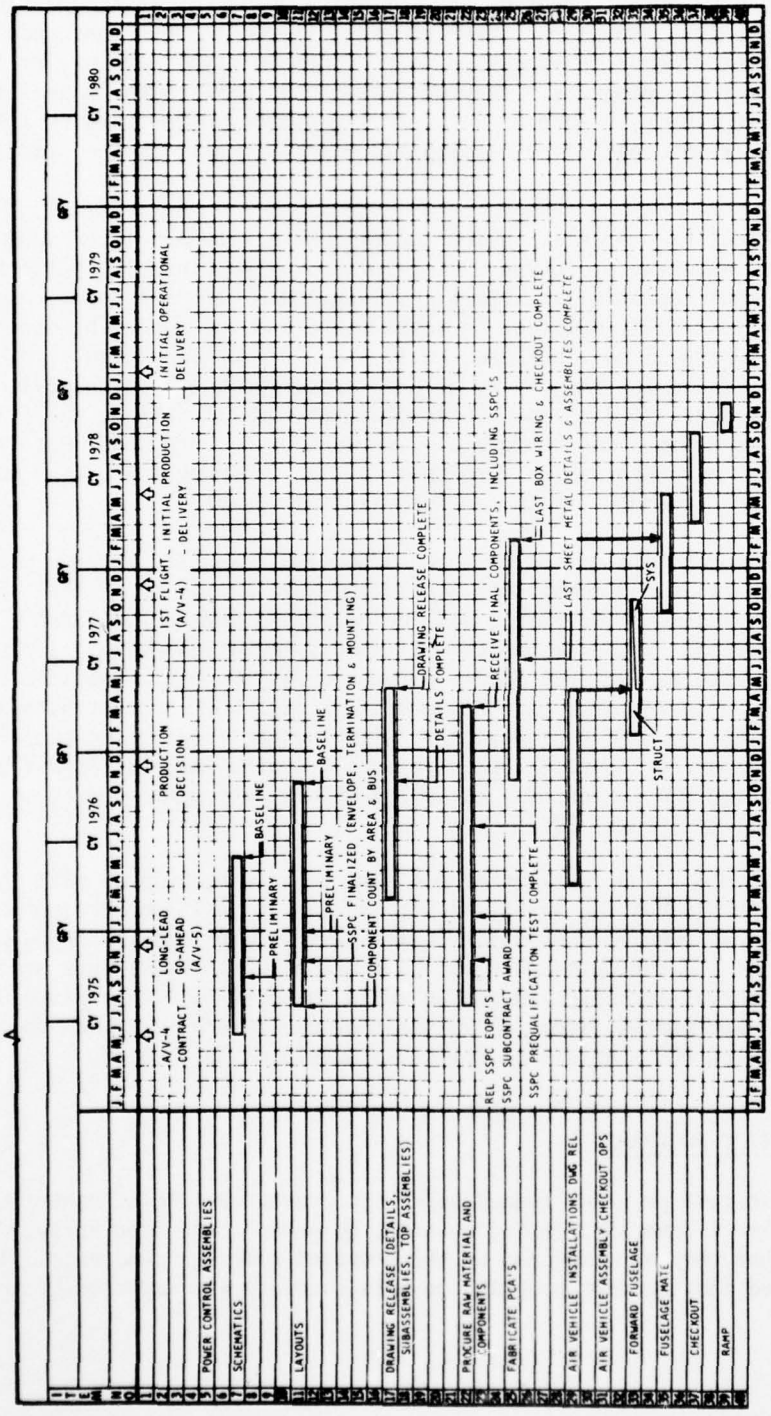


Figure 118-6. Solid-State Power Controllers (SSPC) Schedule

SSPC development programs are currently under way at the Westinghouse and Telephonics companies. These programs are under the cognizance of AFAPL, WPAFB. Westinghouse is scheduled to provide prototype hardware by 1 December 1974 under their programs. They currently have SSPC units in qualifications test. Telephonics is scheduled to provide prototype hardware by 1 February 1975. Their SSPC packaging configuration is currently in the process of being finalized.

Rockwell has recently tested (under contract to AFAPL) breadboard SSPC units plus an early prototype unit furnished by Westinghouse. The test series included EMUX compatibility tests, cycling tests with B-1 loads, and random vibration tests. In addition to these testa and the foregoing development programs, Rockwell has initiated early planning for a program which will ultimately provide for the flying of SSPC prototype units on the B-1 A/V-1. In view of progress to date on SSPC development, qualification, and flight test planning as defined in the foregoing paragraphs, we are confident that flight-worthy SSPC hardware can be furnished in time to support A/V-4 as outlined in the attached schedule and in the following paragraph.

A 20-month time period has been scheduled (item 22) for the procurement of raw materials and components (including SSPC's) for the PCA's. Procurement specifications for SSPC's will be developed during the first 3 months of this period. These documents will specify detailed prequalification and hardening requirements for SSPC's purchased for the B-1. Specifications are scheduled to be released on 1 November 1975 with SSPC subcontracts(s) awarded 3 months later. SSPC subcontractors will then be required to complete prequalification testing to B-1 requirements 6 months later (1 August 1976). All purchased PCA components, including SSPC's, are scheduled to be received at Rockwell by 1 April 1977.

Fabrication and checkout of PCA's will be in accordance with the procedures established for A/V-1, A/V-2, and A/V-3. A 16-month time period (item 25) has been allocated for this activity, with manufacturing checkout of the last PCA scheduled to occur on 1 March 1978. Under this scheduling concept, actual installation of the PCA's in A/V-4 will take place during the fuselage mate period (item 35) as was the case in A/V-1. Final checkout of the installed PCA's will then follow as scheduled in item 37.

CURRENT TEST PROGRAMS

Those test programs funded under the present B-1 RDT&E contract and scheduled after 1 June 1975 (A/V-4 contract go-ahead) have been analyzed to determine whether they are impacted by the proposed redesign candidate. It has been determined that no test programs in this category are impacted by the proposed redesign.

INDEPENDENT OPERATIONS

The proposed PCA design will use both SSPC's and electromechanical components. For this configuration, the AGE required is the same as that proposed for A/V-3. The only difference in the AGE would be a small reduction in the number of adapters for those relay types replaced by solid-state devices.

The self-sufficiency capability of the air vehicle is increased, since no ground support equipment (AGE) is required for on-aircraft testing or fault isolation of SSPC's.

PRODUCTION TRANSITION

Impact to manufacturing is minimal and is limited to tooling new sub-assembly tools, drill plates, and apply tools for power control boxes. These boxes are currently being fabricated complete with electrical systems at Rockwell's Autonetics Division.

Detail fabrication (B-1 Division fabrication), assembly, and installation should benefit by simplified design and deletions.

INTEGRATION IS SCHEDULED FOR A/V-4

LIFE CYCLE COSTS

The change in life cycle cost has been estimated to show the total cost impact of the candidate design changes throughout the life of the weapon system.

Life cycle cost values show the increase or decrease from the baseline design for the research and development, production of 240 air vehicles, and operation of seven wings of 30 aircraft with the candidate design change delta (Δ) is the cost of the alternative less the baseline cost: (+) indicating a cost increase, (-) a cost savings. The RDT&E value includes the research development, test and engineering to develop the new design, and is taken as equal to the implementation cost. It is assumed for purposes of the cost estimate that the first production occurs with A/V-5, so no cost is included for changes to A/V-4. Production costs cover the change in flyaway cost for the total production quantity of 240 aircraft. Support costs include initial spares, recurring spares, aerospace ground equipment (AGE), and maintenance personnel costs. Seven wings of 30 aircraft per wing in normal peacetime operations for a period of 10 years are assumed for the support

cost estimate. Impact on other base operations costs are neglected. Costs are shown for each of the categories described and a total in 1970 and then-year dollars.

	Δ 1970 $	Δ Then-year $
RDT&E	+2,929,000	+4,650,000
Production	-56,160,000	-114,240,000
Support	+2,078,000	+4,389,000
Life cycle cost	-51,153,000	-105,201,000

EXPLANATION

Life cycle cost reduction results from decrease in the production cost through use of solid-state power controllers. Support costs are expected to be higher because of an increase in the cost of the spares used in maintenance.

BUDGETARY AND PLANNING COST ESTIMATES

Cost estimates were prepared at the functional division level.

PRICING ANALYSIS

The following items are presented in tables 118-IV through 118-VI:

1. Summary

   - 1970 $ and then-year $
   - "Was" configuration - Average unit cost of candidate before redesign (recurring cost - 240 A/V)
   - "Is" configuration - Average unit cost of candidate after redesign (recurring cost - 240 A/V)
   - Delta - Difference between "was" and "is"
   - Implementation - Nonrecurring cost of implementing redesign
   - Breakeven - Air vehicle quantity at which point implementation investment is amortized
   - Funding - GFY requirements

2. Detail

   Average production unit (hr/$) multiplied by 1974 rate (direct-indirect-G&A) = 1974 $. 1974 $ multiplied by 1970 factor (inflation factor getting 1974 $ to equivalent 1970 $) = 1970 $. 1970 $ multiplied by 9% fee = average production unit cost in 1970 $.

3. Funding

   1970 $ production unit cost (PUC) is multiplied by 240 air vehicles to get total funding. Funding is spread by GFY. 1970 $ spread is multiplied by inflation factor (getting 1970 $ into then-year $) to equal then-year $ (TY $) funding requirements.

Table 18-IV.

INCORPORATION OF SOLID-STATE CONTROLLERS - SUMMARY

	1970 $	Then-Year $
Average Production Unit Cost		
"Was"	1,070K	2,176K
"Is"	836K	1,700K
Delta	(234K)	(476K)
Implementation Cost	2,929K	4,650K
Breakeven		2
Funding		
1976	.6M	.9M
1977	(.8)	(1.3)
1978	(5.5)	(9.3)
1979	(9.1)	(16.5)
1980	(11.0)	(21.4)
1981	(9.7)	(20.2)
1982	(7.8)	(17.5)
1983	(6.7)	(16.0)
1984	(3.2)	(8.2)
1985	-	-

Table 118-V.

INCORPORATION OF SOLID-STATE CONTROLLERS - DETAIL

	"Was" Configuration				"Is" Configuration			
	Avg Prod. Unit	1974 Rate	1970 Factor	X Fee 109%	Avg Prod. Unit	1974 Rate	1970 Factor	X Fee 109%
Recurring								
Engineering (hr)		16.13	75.5%			16.13	75.5%	
T&E (hr)		15.55	75.5%			15.55	75.5%	
Manufacturing (hr)	140	15.91	75.5%	2K	84	15.91	75.5%	1K
Tooling (hr)	13	16.47	75.5%	-	7	16.47	75.5%	-
Q&RA (hr)	13	16.47	75.5%	-	8	16.47	75.5%	-
SPRS (hr)		16.47	75.5%			16.47	75.5%	
Subcontract ($)		8.06%	75.2%			8.06%	75.2%	
Material ($)	1,080K	20.94%	75.0%	1,068K	844,183	20.94%	75.0%	835K
Tool Material ($)	27	20.94%	75.0%	-	15	20.94%	75.0%	-
Total				1,070K				836K
					Impl	1974 Rate	1970 Factor	X Fee 109%
Nonrecurring								
Engineering (hr)					100K	16.13	75.5%	1,328K
T&E (hr)					11K	15.55	75.5%	141K
Manufacturing (hr)					95	15.91	75.5%	1K
Tooling (hr)					2,547	16.47	75.5%	35K
Q&RA (hr)					122	16.47	75.5%	2K
SPRS (hr)						16.47	75.5%	
Subcontract ($)						8.06%	75.2%	
Material ($)					1,435K	20.94%	75.0%	1,418K
Tool Material ($)					4,439	20.94%	75.0%	4K
Total								2,929K

Table 118-VI.

INCORPORATION OF SOLID-STATE CONTROLLERS - FUNDING

"Was" (Recurring)	PUC	X 240 A/V	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985
Engineering												
T&E												
Manufacturing	2K	.5M										
Subcontract												
Material	1,068K	256.3M										
Subtotal 1970 $	1,070K	256.8M	1.8	12.3	25.7	41.6	50.1	44.4	35.7	30.6	14.6	
Inflation Factor			153.9	160.2	169.8	181.8	194.7	208.6	223.4	239.2	256.2	274.4
Subtotal TY $			2.8	19.7	43.6	75.6	97.5	92.6	79.8	73.2	37.4	
"Is" (Recurring)	PUC	X 240 A/V	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985
Engineering												
T&E												
Manufacturing	1K	.2M										
Subcontract												
Material	835K	200.4M										
Subtotal 1970 $	836K	200.6M	1.5	9.6	20.0	32.5	39.1	34.7	27.9	23.9	11.4	
Inflation Factor			153.9	160.2	169.8	181.8	194.7	208.6	223.4	239.2	256.2	274.4
Subtotal TY $	1,700K	408.0M	2.3	15.4	34.0	59.1	76.1	72.4	62.3	57.2	29.2	
"Is" (Nonrecurring)		Impl	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985
Engineering		1,328K	531K	797								
T&E		141K	56K	85K								
Manufacturing		38K	8K	25K	5K							
Subcontract												
Material		1,422K	313K	953K	156K							
Subtotal 1970 $		2,929K	908K	1,860K	161K							
Inflation Factor			153.9	160.2	169.8	181.8	194.7	208.6	223.4	239.2	256.2	274.4
Subtotal TY $		4,650K	1,397K	2,980K	273K							
Total Delta 1970 $			.6M	(.8)	(5.5)	(9.1)	(11.0)	(9.7)	(7.8)	(6.7)	(3.2)	
Total Delta TY $			.9M	(1.3)	(9.3)	(16.5)	(21.4)	(20.2)	(17.5)	(16.0)	(8.2)	

APPENDIX A

WEIGHT ANALYSIS

BACKGROUND (REF NA-74-244)

BASIC A/V PCA WEIGHTS (Electromechanical PCA's)

2,318 components	308 lb	
3,307 packaging	400	
Internal wiring	176	
Total 25 LRU's	884 lb	wt empty (35.0)
3 weapon launcher PCA's (73-74-63)	210	useful load (35.0)
Gross PCA's	1,094 lb	A/V-3 & Subs

DEFENSIVE SUBSYSTEM (Ref TFD-74-690)

(6-6-4)	KK6970-1	16	
(6-6-4)	KK6970-2	16	in projections
(5-5-2)	KK6980-1	12	
Total EMPCA's 31 LRU's		1,138 lb	production baseline with defensive subsystem

LRU BREAKDOWN FOR PRODUCTION (31 LRU's)

	Wt empty	Useful load
2,318 components	325	73
3,307 packaging	417	74
Internal wiring	186	63
	928	210

EMPCA's Production baseline Gross weight: 1,133 lb

COMPONENT WEIGHT REDUCTIONS EMPC TO SSPC

A/V-3 circuit breakers that can change (1.6 amps) - 573 out of 1,300

Production circuit breakers that can chg $\frac{573}{1,200} = \frac{X}{1,400} = 669$

Wt that changes is

$$\frac{669}{1,400} = \frac{X}{1,138} \qquad x = 545 \text{ lb EMPC can be SSPC}$$

For 573 circuit breakers replaced by 839 SSPC's for A/V-3

weight 573 = 136 lb 839 = 118 lb

$$\frac{118}{136} = \frac{X}{545} \qquad X = 473 \text{ lb SSPC wt}$$

weight EMPC to SSPC 545-473 = 72 lb

PACKAGING WEIGHT REDUCTIONS DUE TO VOLUME
(Based on IWTS Connection Concept for SSPC's)

A/V-3 total volume = SDM 3-22-74)

AD 1034	1.38		
AD 1352	0.21	40,729 cu in	23.57 cu ft
AD 1353	0.21	25 LRU's	EMAC
22 LRU's	21.77		

Production baseline volume = A/V-3 + 6 LRU's at 35 lb/cu ft
EMPC and 254 lb which is +7.26 ft
or 12,545 cu in. Prod vol = 53,274 cu in

For production 11,000 cu in EMPC changes to 7,110 cu in SSPC

Weight that changes is $\frac{11,000}{53,274} = \frac{X}{1,138} = 235$ lb EMPC

$$\frac{11,000}{235} = \frac{7,110}{X} = 152 \text{ lb rev wt SSPC}$$

weight due to SSPC vs EMPC vol = -83. lb
(235-152 = 83 lb)

REMOVALS (Based on status 35.0)

Weight empty - 25 LRU's	Weight		
EMPC components	308		
PCA packaging	400		
Internal wire & connections	176		
Trays	41		
(3) SRAM PCA's (useful load)			
Components	73		590
Packaging	74		785
Internal wire & connections	63		1,180
Defensive subsystem (projections)			
+3 LRU's TFD-74-690			
Components	17	(2)	750
Packaging	17	(1)	1,590
Internal wire & connections	10		

Total removals 31 LRU's - Status 35.0 with projections

Weight empty	(-969)	(685.9)
Useful load	(-210)	(851.6)

ADDITIONS

	Weight	Horiz
Weight empty (14 LRU's)		
SSPC components	252	
PCA packaging	318	
Internal wire & connections	167	672
Trays	15	
Useful load - 3 LRU's		
Components SSPC	60	
Packaging	59	851.6
Internal wire & connections	60	

Defensive subsystem projected 3 LRU's

Components	14	(2) 750
Packaging	13	(1) 1590
Internal wire & connections	10	

Total additions - 20 LRU's

Weight empty	(+789)	(687.4)
Useful load	(+179)	(851.6)

CONTROL NO. 309-118 Δ WEIGHT

Weight empty	-180 lb
Useful load	-122,278 in.-lb
Useful load	-31 lb
	-26,400 in. lb
Gross weight Δ	-211 lb
Moment	-148,678 in.-lb

WEIGHT REDUCTION DUE TO REDESIGN OF PCA's

9002D05-1	Current xfmr	0.19 lb/ea x -6 = -1.14 lb
L5400794	Handle	0.34 lb/ea x -6 = -2.04
L5400783	Air duct	0.06 lb/ea x -25 = -1.50
L5400785	Slides	0.80 lb/ea x -34 = -27.20
L5400785	Slides	0.80 lb/ea x -34 = +20.40
	Slides replacement	0.60 x 34 = +20.40
L5408012	Panels	0.43 lb/ea -6 = -2.58
Connecters	Rock and panel to MIL-C-38999 53 reqd = -22.79	
	53 at 0.254 + 0.172 = 0.426 53x185 = 9805	
Connecters	9805/128 = 77 at 0.1133 + 0.1363 = 0.25 lb/ea = + 1925	
	MS27474 24-35	
	Total	-17.60 lb

AD-A078 238 ROCKWELL INTERNATIONAL ANAHEIM CA AUTONETICS STRATEG--ETC F/G 1/3
SOLID STATE POWER CONTROLLER VERIFICATION STUDIES.(U)
JAN 79 C O LINDER F33615-78-C-2065
UNCLASSIFIED C79-85/201 AFAPL-TR-79-2029 NL

3 OF 3
AD
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END
DATE
FILMED
1-80
DDC

WEIGHT REDUCTION DUE TO TRAY CHANGE

Eliminate rack and panel connection from PCA LRU.

L5403348 Typ tray for blind-mated connecters
2.40 lb/ea, 17 reqd = -40 80 lb

L5404541 Typ new tray 1.10 lb/ea
1.10 x 13 reqd = +14.30 lb

Δ Weight = -26.50 lb

TASK 309-118 SUMMARY

393	Components	-72 lb	0.819	326
491	Packaging	-83-18 = -101 lb	0.794	390
249	Internal wiring (249 lb assume 5% decr)		-12 lb	237
41	trays	-26		15
-1,179 lb	Total	-211 lb		+968 lb

APPENDIX C
GLOSSARY OF TERMS

SSPC	Solid State Power Control
SSPCA	Solid State Power Control Assembly
EMPCA	Electromechanical Power Controller Assembly
PC	Power Controller
PCA	Power Controller Assembly
A	Ampere
EMUX	Electrical Multiplexing
SCR	Silicon Controlled Rectifier
CMOS	Complementary Metal Oxide Semiconductor
LSI	Large Scale Integrated
SOS	Silicon-on-Sapphire
LRU	Line Replaceable Unit
msec	Millisecond
mA	Milliampere
W	Watt
V	Volt
MIB	Master Interconnect Board
hr	Hour
lb	Pound
Hz	Hertz
μA	Microampere
ZVC	Zero Voltage Crossing
ADC	Analog to Digital Converter
FET	Field Effect Transistor
LSB	Least Significant Bit

MSB	Most Significant Bit
ZIC	Zero Current Crossing
DWV	Dielectric Withstanding Voltage
RC	Resistive Capacitive
in.	Inch
PCB	Printed Circuit Board
MTBF	Mean Time Between Failure
JFET	Junction Field Effect Transistor
IR	Insulation Resistance

*U.S.Government Printing Office: 1979 — 657-084/269