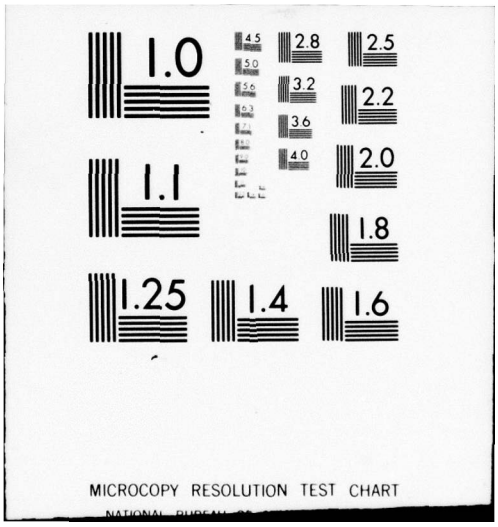
AD-A069 325 NAVAL RESEARCH LAB WASHINGTON DC F/G 9/5
A BROAD-BAND PASSIVE-REDUNDANT UHF AMPLIFIER CIRCUIT.(U)
MAY 79 D C ROHLFS, R E GARBACK, B N NAVID
UNCLASSIFIED NRL-MR-3997 NL

| OF |
AD
A069325

END
DATE
FILMED
7-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
7.1
8.0
9.0
MICROCOPY RESOLUTION TEST CHART

NRL Memorandum Report 3997

A Broad-Band Passive-Redundant UHF Amplifier Circuit

D. C. ROHLFS, R. E. GARBACK, AND B. N. NAVID

Radar Techniques Branch
Radar Division

May 8, 1979

NAVAL RESEARCH LABORATORY
Washington, D.C.

(14) NRL-MR-3997

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

(9) **REPORT DOCUMENTATION PAGE**

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: Memorandum Report 3997
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (and Subtitle): A BROAD-BAND PASSIVE-REDUNDANT UHF AMPLIFIER CIRCUIT.

5. TYPE OF REPORT & PERIOD COVERED: Interim report on a continuing NRL problem.

6. PERFORMING ORG. REPORT NUMBER

(10) 7. AUTHOR(s): D. C. Rohlfs, R. E. Garback, B. N. Navid

8. CONTRACT OR GRANT NUMBER(s)

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Research Laboratory, Washington, DC 20375

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE 62712N, Project ZF12-151-001, NRL Problem R12-25.701

11. CONTROLLING OFFICE NAME AND ADDRESS

(12) 33p.

(11) 12. REPORT DATE: May 1979

13. NUMBER OF PAGES: 32

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Deputy Chief Naval Material (Technology & Laboratories), Headquarters, Naval Material Command, Washington, DC 20360

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

(16) F12151

Approved for public release; distribution unlimited.

(17) ZF12151001

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Parallel redundant circuit
Self-healing circuit
Reliability
Passive-redundant circuit

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A Passive-Redundant UHF amplifier circuit which acts as its own fault sensor and automatically adjusts and compensates for individual amplifier degradation is described. It is essentially a parallel circuit, operating to maintain a constant output, whether one amplifier fails completely or both degrade gracefully. The circuit was designed for 435 MHz and tested for operation over the frequency range of 400 to 470 MHz. It is suitable for use in stages of a system where power transfer is not critical.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

251 950

CONTENTS

A BROAD-BAND PASSIVE-REDUNDANT UHF AMPLIFIER CIRCUIT

INTRODUCTION

The Naval Research Laboratory has been investigating the feasibility and cost effectiveness of the maintenance-free concept in achieving an operational availability for a radar far in excess of that of any system currently in the fleet.

With present or projected technology, the most promising system designs of achieving the long MTBF (Mean Time Between Failures) required involve considerable redundancy and self-healing architecture.

In terms of implementation, there are basically two types of redundant circuits: 1) a circuit in which there is a separate monitor to detect component/module failure; and 2) a circuit in which there is no such separate monitor. In this case, the redundant circuit itself acts as its own sensor and automatically adjusts and compensates for circuit degradation.

This paper is a description of a passive-redundant (PR) amplifier circuit of the second type suitable for use in stages of a system where power transfer efficiency is not critical.

QUALITATIVE CIRCUIT DESCRIPTION

The basic circuit contains two amplifiers, one power splitter, one power canceller, one power combiner, one directional coupler having a coupling factor equal to the gain of the primary amplifier, and the necessary phase compensating sections (Fig. 1).

The circuit is designed to maintain a constant output signal should a failure or degradation occur in the primary amplifier. It can even tolerate a moderate amount of degradation in both amplifiers as described below. A qualitative description is given in this section with a theoretical analysis given in Appendix A.

The input to the circuit is at the input terminal of the power splitter. Here the signal divides with half going to the primary circuit and half going to the compensating circuit. The signal in the primary circuit is amplified by Amp. A. A fraction of the output from this amplifier is coupled to the power canceller while the rest of the signal is connected to the circuit output through the power combiner.

Note: Manuscript submitted March 12, 1979.

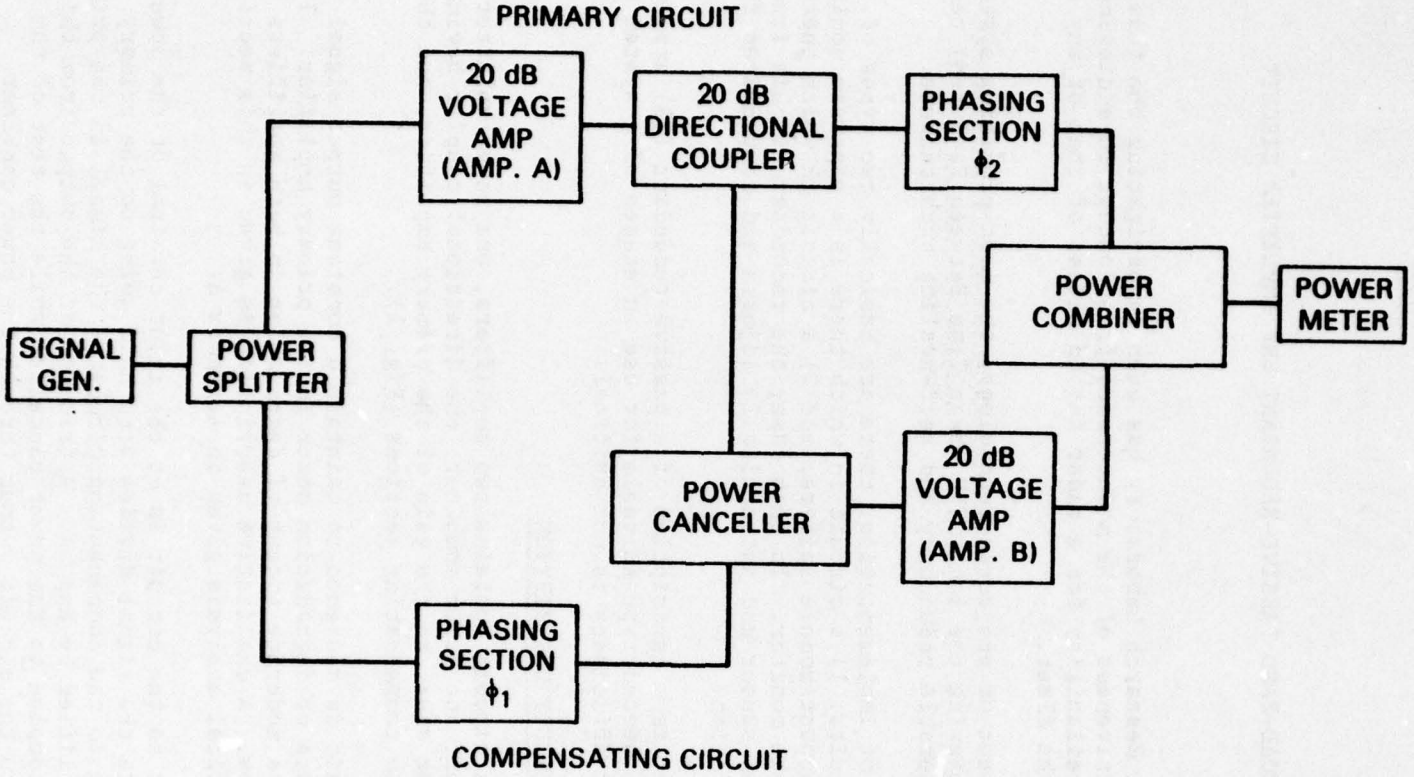


Fig. 1 — Basic block diagram of passive-redundant circuit

When Amp. A is operating normally, the output from the power canceller is zero and Amp. B does not contribute to the circuit output. However, if Amp. A degrades, an output exists from the canceller which is amplified by Amp. B. Assuming this latter amplifier is operating normally, its output is added to the power from the primary circuit at the power combiner to maintain the PR circuit output constant.

If both amplifiers incur degradation, the PR circuit can no longer maintain full output. The degradation, however, will be graceful (Fig. 2). This figure shows the PR circuit output loss as a function of the degradation in each amplifier. These curves are based on Eq. (6).

For example, assuming no phase change in either amplifier, a circuit output loss of no more than 1 dB can be maintained even if each amplifier degrades by as much as 3.5 dB. With a phase change as much as 45^{o} in Amp. B only, each amplifier could still degrade by 2.7 dB to maintain the same output loss of no more than 1 dB.

RELIABILITY

Parallel redundant circuits are, in general, either of two types: parallel stand-by or parallel operating. The Passive-Redundant (PR) circuit, however, does not belong to either class but is a hybrid of the two. A simple comparison of the way each circuit operates will demonstrate this fact.

When a stand-by system is turned on, only one of its two amplifiers is activated, with the second dormant. When the active amplifier falls below a predetermined threshold, it is deemed to have failed, is removed from the circuit and the second amplifier is inserted in its place, fully activated.

When a parallel operating system is turned on, both amplifiers are fully activated. Each remains fully activated as long as its output exceeds the predetermined threshold. Moreover, the contribution of each amplifier is independent of the other.

The PR circuit initially behaves as a stand-by system, i.e., only one amplifier is operating. As the active amplifier begins to degrade, the second amplifier becomes partially activated. There is no waiting for a threshold to be crossed.

It follows that the expected time to failure (MTBF) for the PR circuit will be less (no more) than that of the equivalent parallel stand-by circuit and more (no less) than that of the equivalent parallel operating circuit. Hence, the MTBF of the PR circuit is bounded by the MTBF's of the two comparison circuits. Therefore, if M_3 is the expected time for a single amplifier to degrade by 3 dB, the MTBF of the PR circuit lies between 1.5 M_3 and 2.0 M_3.

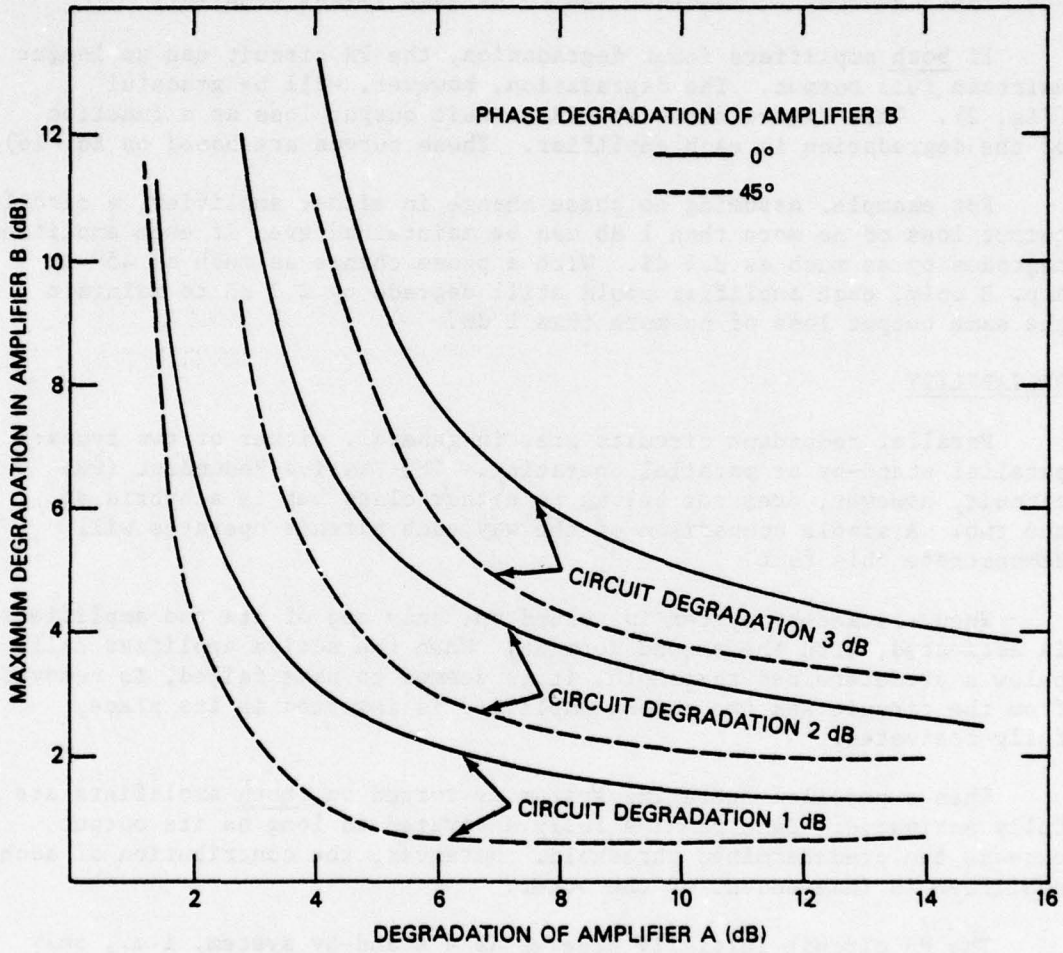


Fig. 2 — Allowable individual amplifier degradation for given circuit degradation

There is an inherent reliability advantage of the PR circuit over either of the other two circuits which is not apparent from the preceding discussion. This is due to its "load-sharing" feature and manifests itself in changing the definition of failure for a single amplifier when it is part of the circuit. This can be seen from an example.

Suppose an amplifier voltage gain of G is required in a given stage of a system but a 3 dB degradation can be tolerated. Assume that the design will be implemented either with a single amplifier or with one of the three redundant circuits of this section. Whatever circuit is used, it will be considered to be a "success" if its gain satisfies the preceding criterion and a "failure" if it does not.

If the circuit is implemented as a single amplifier, loss of more than 3 dB gain constitutes a failure for that amplifier. If the circuit is implemented either as a parallel stand-by or a parallel operating circuit, the definition of failure for an individual amplifier is unchanged from the previous case; if its gain degrades by more than 3 dB, it is a "failure". When both amplifiers fail, the circuit itself will degrade by more than 3 dB and be deemed a failure.

For the PR circuit, however, incorporation of the two amplifiers into the circuit alters the definition of failure for these amplifiers. This is shown graphically in the solid top curve of Fig. 2. The coordinates of any point on the curve are acceptable definitions of failures for each amplifier pair. For example, Amp. B will fail if its gain falls by 9.5 dB after Amp. A has degraded by 5.0 dB, but it will also be considered a failure if its gain falls by only 8.0 dB after Amp. A has degraded by 5.7 dB, etc.

Further, from Fig. 2, using the same curve, there is one point at which both amplifiers have the same loss, namely, 6.75 dB. As a second approximation then, each amplifier in the PR circuit can be considered to be operational only if it has degraded by no more than 6.75 dB. This will lead to a conservative estimate for the circuit's MTBF. With this assumption, the MTBF of the PR circuit lies between 1.5 M_6 and 2.0 M_6, where M_6 is the expected time for a single amplifier to degrade by 6.75 dB. The results are summarized in Table 1.

It is certainly true that M_6 is always greater than M_3. The exact relationship depends upon the failure mechanisms of the amplifier used in implementing the PR circuit and the derived stochastic failure model process. For example, if it is assumed that the MTBF for an individual amplifier is linear with degradation threshold (for small values of degradation), then $M_6 \approx 2\ M_3$ and the MTBF for the PR circuit would lie between 3.0 M_3 and 4.0 M_3. Hence, it would be considerably better than either of the two classical parallel redundant circuits.

More generally, with the appropriate stochastic failure model and the use of the entire curve in Fig. 2, instead of merely one point

(6.75, 6.75) a more accurate MTBF can be obtained. It will, of necessity, be somewhat greater than that obtained by the argument in the previous paragraph.

The derivation of the statistical model is not relevant to this report and will be left to a future paper. Nevertheless, it appears that with very mild assumptions about the failure process, the MTBF for the PR circuit should exceed that of a stand-by system with the same failure definition.

The 3 dB criterion for failure was chosen for illustration only. Similar conclusions would hold for any other threshold.

TABLE 1

Expected Time to Fail for
Parallel Redundant Circuits

	Expected Time to Degrade (MTBF) by:	
	3.0 dB	6.75 dB
Single Amplifier	M_3	M_6
Parallel Operating	$1.5\ M_3$	$1.5\ M_6$
Parallel Stand-by	$2.0\ M_3$	$2.0\ M_6$
Passive-Redundant	$1.5\ M_6$ to $2.0\ M_6$	Not relevant

TEST CIRCUIT

A block diagram of the test circuit using commercially available components is shown in Fig. 3. Operationally, it is equivalent to the circuit in Fig. 1. It was designed for broadband operation from 400 MHz to 470 MHz.

The list of components is shown in Table 2. Extensive tests were made on each component to determine its characteristics such as coupling factor, phase shift, and gain/loss. The amplifier gains, coupling factor of the directional coupler, and the circuit losses determined the final configuration of the test circuit.

The power outputs from the circuit (Fig. 3) with each of the two amplifiers operating alone, were made equal by the use of a 4.0 dB fixed attenuator (Attn. 1) in the primary circuit. The amplitudes of the two signals arriving at the power canceller were then made equal by using a 3.0 dB fixed attenuator (Attn. 2) in the coupled output line of the directional coupler.

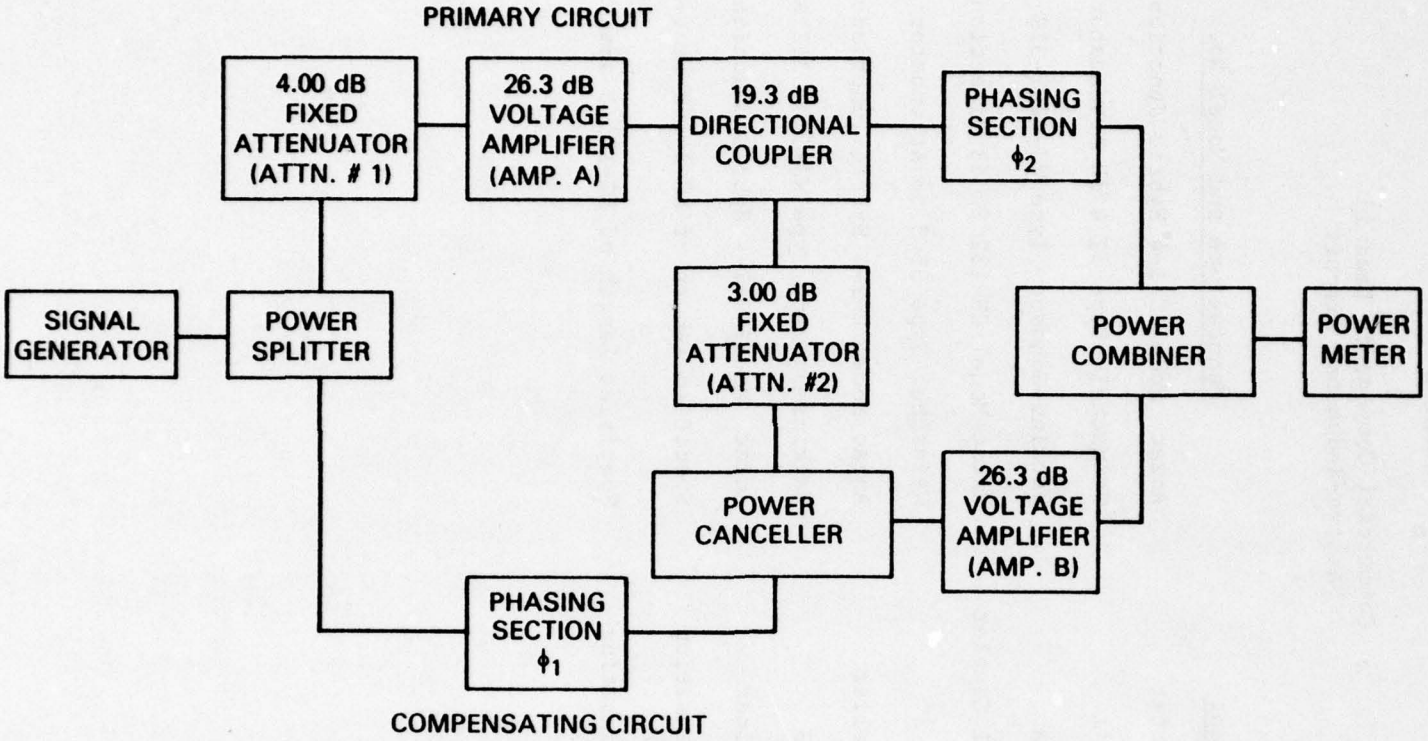


Fig. 3 — Block diagram of experimental implementation of passive-redundant circuit

TABLE 2

Commercial Components Used in
Passive-Redundant Circuit

Component	Manufacture and Model No.
Power Splitter	Anzac Model H-1-4 Hybrid Junction
Attenuator 1	Weinschel Type 3T 4 dB Attenuator
Amplifier A	Watkins-Johnson Type WJ-6201-312 Amplifier
Directional Coupler	Anzac Model CH-132 20 dB Directional Coupler
Attenuator 2	Weinschel Type 3T 3 dB Attenuator
Power Canceller	Anzac Model H-1-4 Hybrid Junction
Amplifier B	Watkins-Johnson Type WJ-6201 312 Amplifier
Power Combiner	Anzac Model H-1-4 Hybrid Junction
Phase Compensating Line ($\emptyset_1$)	Specified length of RG-141/U semi-rigid coax
Phase Compensating Line ($\emptyset_2$)	Specified length of RG-141/U semi-rigid coax

The delay time (phase) of the two signals arriving at the power canceller were made the same to satisfy the requirements of the canceller as used in this circuit. (Equalizing the phase at one frequency may not meet the phase requirement over the entire frequency range, hence, time delay was used). To perform the adjustment, the signal delay time from the PR circuit input terminal through the primary circuit to the power canceller was determined. Then the length of the phasing section ($\emptyset_1$) was cut to give the same delay time to the signal at the second input terminal of the power canceller. A minimum output signal at the canceller resulted when ($\emptyset_1$) was properly adjusted. A similar measurement and adjustment was made at the power combiner to fix the length of phasing section ($\emptyset_2$). In this case, proper adjustment resulted in maximum output.

Figure 4 is a photograph of the test circuit.

THEORETICAL CONSIDERATIONS

A mathematical derivation of the output of the PR circuit is developed in Appendix A. The attenuators, phase shifters, directional couplers, power splitter, power canceller and power combiner are modeled as ideal elements. Each amplifier is considered to be an ideal 20 dB amplifier in series with an ideal attenuator and ideal phase shifter.

A normalized power output, P'_{out}, is given by Eq. (A36) and is repeated below as:

$$P'_{out} = 10^{\frac{\alpha}{10}} + 10^{\frac{\alpha_2}{10}} + 10^{\frac{\alpha+\alpha_2}{10}} - 2 \times 10^{\frac{\alpha}{20}+\frac{\alpha_2}{10}} \cos(\Delta_1 + \theta)$$

$$- 2 \times 10^{\frac{\alpha}{10}+\frac{\alpha_2}{20}} \cos(\beta - \Delta_2 + \Delta_1) + 2 \times 10^{\frac{\alpha+\alpha_2}{20}} \cos(\beta - \Delta_2 - \theta) \quad (1)$$

where α = amplitude degradation (dB)of Amplifier A.

α_2 = amplitude degradation (dB) of Amplifier B.

θ = phase degradation (rad) of Amplifier A.

β = phase degradation (rad) of Amplifier B.

Δ_1 = phase difference (rad) of inputs to power canceller when $\theta=0$.

Δ_2 = phase difference (rad) of inputs to power combiner when $\theta=\beta=0$.

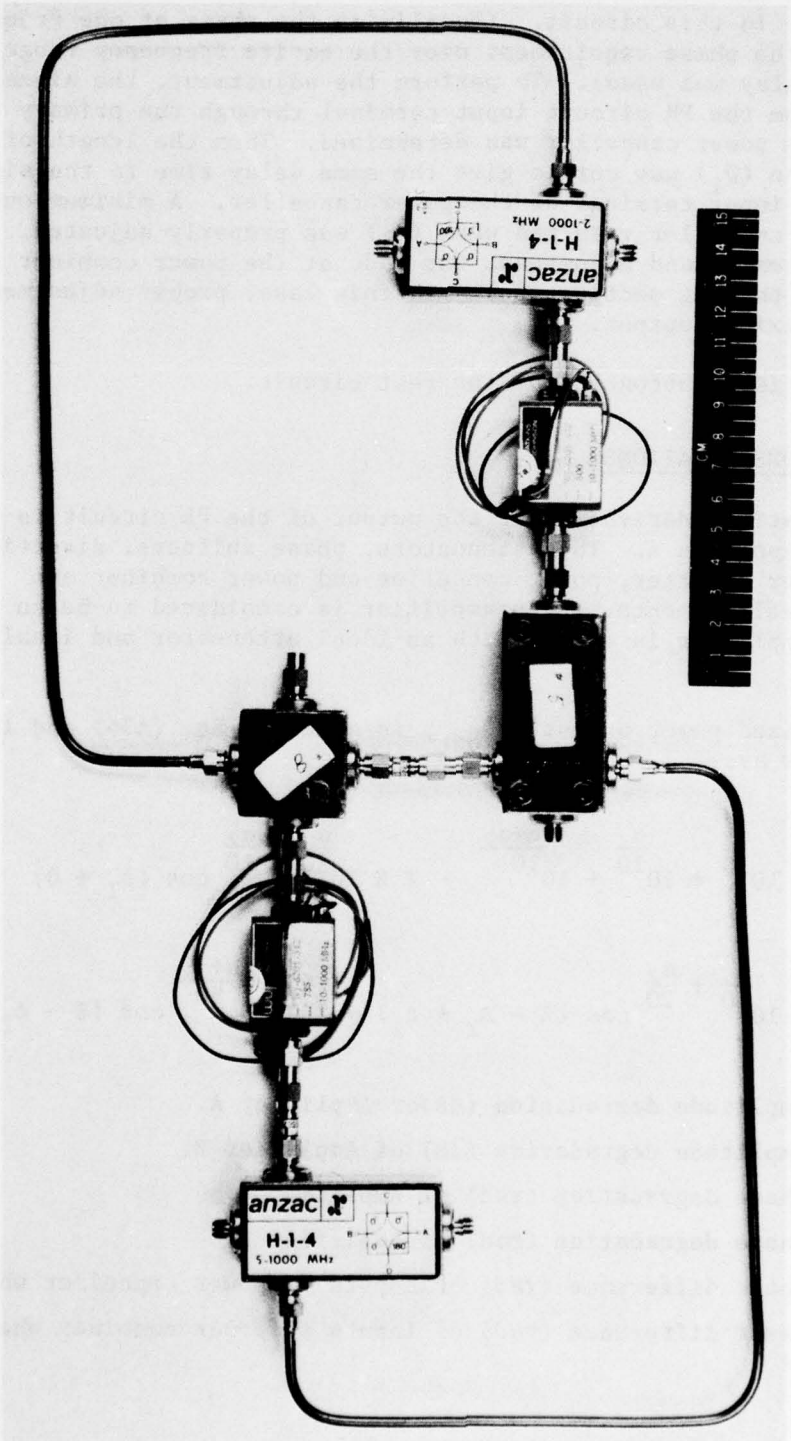


Fig. 4 — Photograph of the passive-redundant circuit

It is possible to explain the operation of the PR circuit completely by analyzing Eq. (1). It should be noted that this equation includes the effects of both amplitude and phase degradation in each amplifier as well as the effect of misadjustment in the phase compensation networks.

It is convenient to make the following substitutions in Eq. (1):

$$D_1 = 10^{\frac{\alpha}{20}}$$

$$D_2 = 10^{\frac{\alpha_2}{20}}$$

After some algebraic manipulation, Eq. (1) becomes:

$$P'_{out} = \{D_1 + D_2 - D_1 D_2\}^2 - 2 D_1 D_2 \{[1 - \cos(\beta - \Delta_2 - \theta)] - D_2 [1 - \cos(\theta + \Delta_1)] - D_1 [1 - \cos(\beta - \Delta_2 + \Delta_1)]\} \quad (2)$$

If perfect adjustments in the phase compensating networks are attained ($\Delta_1 = 0 = \Delta_2$), Eq. (2) becomes:

$$P'_{out} = \{D_1 + D_2 - D_1 D_2\}^2 - 2 D_1 D_2 \{[1 - \cos(\beta - \theta)] - D_2 [1 - \cos\theta] - D_1 [1 - \cos\beta]\} \quad (3)$$

It follows that the power output, P'_{out}, is completely symmetric in the parameters for each amplifier, i.e., the interchange of D_2 with D_1 and β with θ in Eq. (3) does not change the value of P'_{out}.

a. Special Cases of Amplifier Degradation

Seven special cases of Eq. (3) will be considered.

Case I: Amplifier A is perfect ($\alpha = 0 = \theta$).

Hence,

$D_1 = 1$ and using Eq. (3),

$$P'_{out} = 1 - 2 D_2 [(1 - \cos \beta) - 0 - (1 - \cos \beta)]$$
$$P'_{out} = 1 \qquad (4)$$

Thus, if Amplifier A is operating normally, the output power from the circuit is independent of the state of Amplifier B.

Case II: Amplifier B is perfect ($\alpha_2 = 0 = \beta$).

By the comment on symmetry or direct substitution into Eq. (3), noting that $D_2 = 1$ in this case,

$$P'_{out} = 1 \qquad (5)$$

Thus, if Amplifier B is operating normally, the output power from the circuit is independent of the state of Amplifier A and is the same as for Case I. The results of Cases I and II really establish the validity of the circuit design.

Case III: Amplifiers A and B suffer amplitude, but not phase, degradation ($\alpha \neq 0 \neq \alpha_2$, $\theta = 0 = \beta$)

$$P'_{out} = (D_1 + D_2 - D_1 D_2)^2 \qquad (6)$$

The solid lines in Fig. 2 are a parametric plot of Eq. (6).

Case IV: Amplifier B suffers both amplitude and phase degradation; Amplifier A suffers amplitude degradation only ($\theta = 0$).

$$P'_{out} = (D_1 + D_2 - D_1 D_2)^2 - 2 D_1 D_2 (1 - \cos \beta) (1 - D_1) \qquad (7)$$

The dotted lines in Fig. 2 are a parametric plot of Eq. (7) for $\beta = \pi/4$ (45^o).

Case V: Amplifier A suffers both amplitude and phase degradation; Amplifier B suffers amplitude degradation only ($\beta = 0$). This case is symmetric to Case IV.

$$P'_{out} = (D_1 + D_2 - D_1 D_2)^2 - 2 D_1 D_2 (1 - \cos \theta) (1 - D_2) \qquad (8)$$

Case VI: Both amplifiers suffer phase but not amplitude degradation ($\alpha = 0 = \alpha_2$)

$$P'_{out} = 3 + 2\,[\cos(\beta - \theta) - \cos\beta - \cos\theta] \tag{9}$$

A plot of this case is shown in Fig. 5.

Case VII: Amplifier B maintains amplitude integrity ($\alpha_2 = 0$) but all other parameters of circuit degrade.

$$P'_{out} = 1 + 2D_1\,[D_1\,(1 - \cos\beta) + \cos(\beta-\theta) - \cos\theta] \tag{10}$$

A parametric plot of this more general case is shown in Fig. 6.

b. Effect of Open-Circuit Failures

A common class of failures in UHF circuits are those which result in open circuits. These include breaks in coaxial lines or poor connections. The effect of open circuits occurring at five critical points (Fig. 7) in the PR circuit are readily analyzable.

For this purpose, it is best to use the voltage output equations (A12, A11, A10), which are repeated with slight modifications below:

$$V_{out} = \frac{V_6}{\sqrt{2}} + \frac{V_5}{\sqrt{2}}$$

$$\frac{V_6}{\sqrt{2}} = \frac{5}{\sqrt{2}}\,D_1\,V e^{j(\delta_3 + \theta + \omega t)}$$

$$\frac{V_5}{\sqrt{2}} = 5\,D_2\,(V_3 - V_2)\,e^{j(\delta_4 + \beta)} \tag{11}$$

where,

δ_i = phase shift (rad) introduced in the circuit path corresponding to l_i ($i = 1, 2, 3, 4$). It does not include the phase shift introduced by the amplifier in that path.

Open circuits at the critical points are equivalent to setting certain of the voltages V_2, V_3, or V_6 equal to zero.

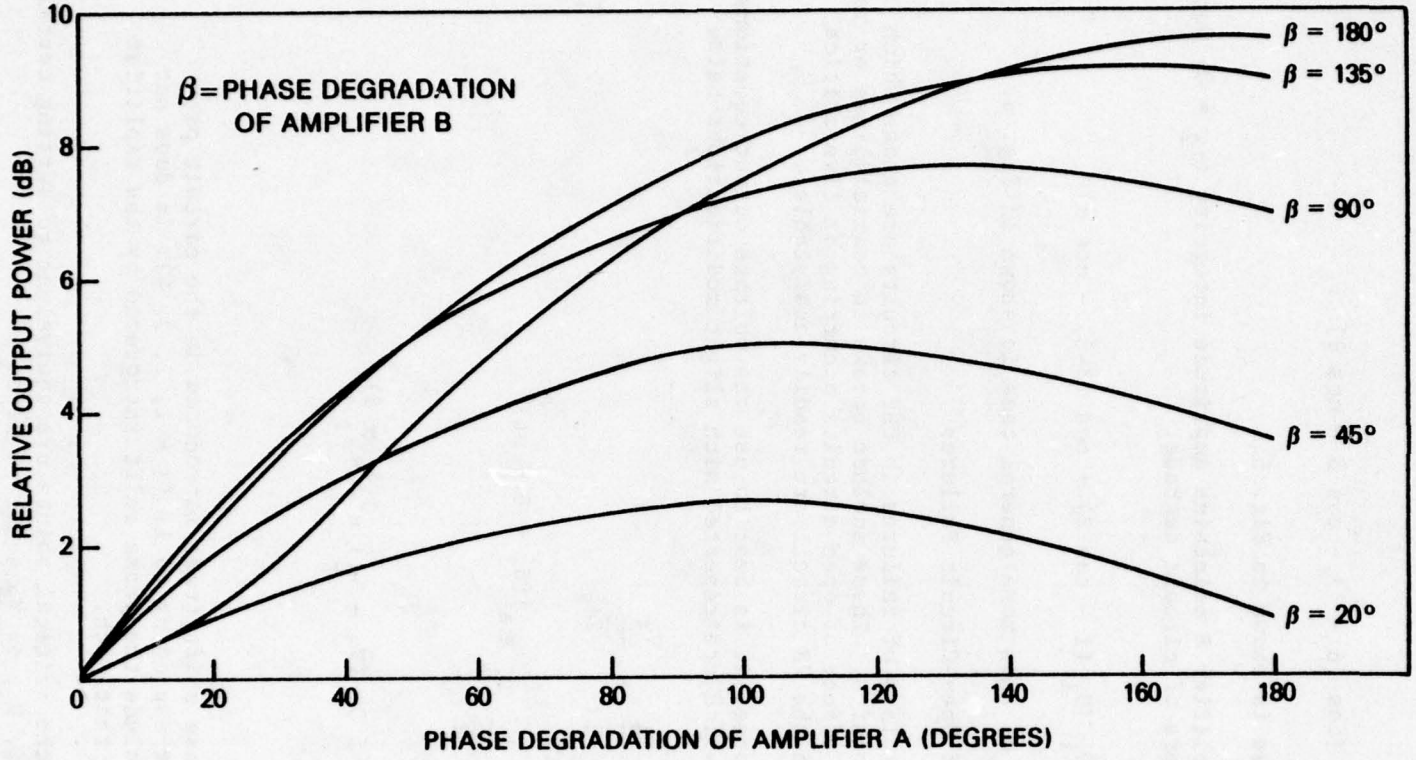


Fig. 5 — Relative output of PR circuit as a function of amplifier phase degradation when there is no amplitude degradation in either amplifier

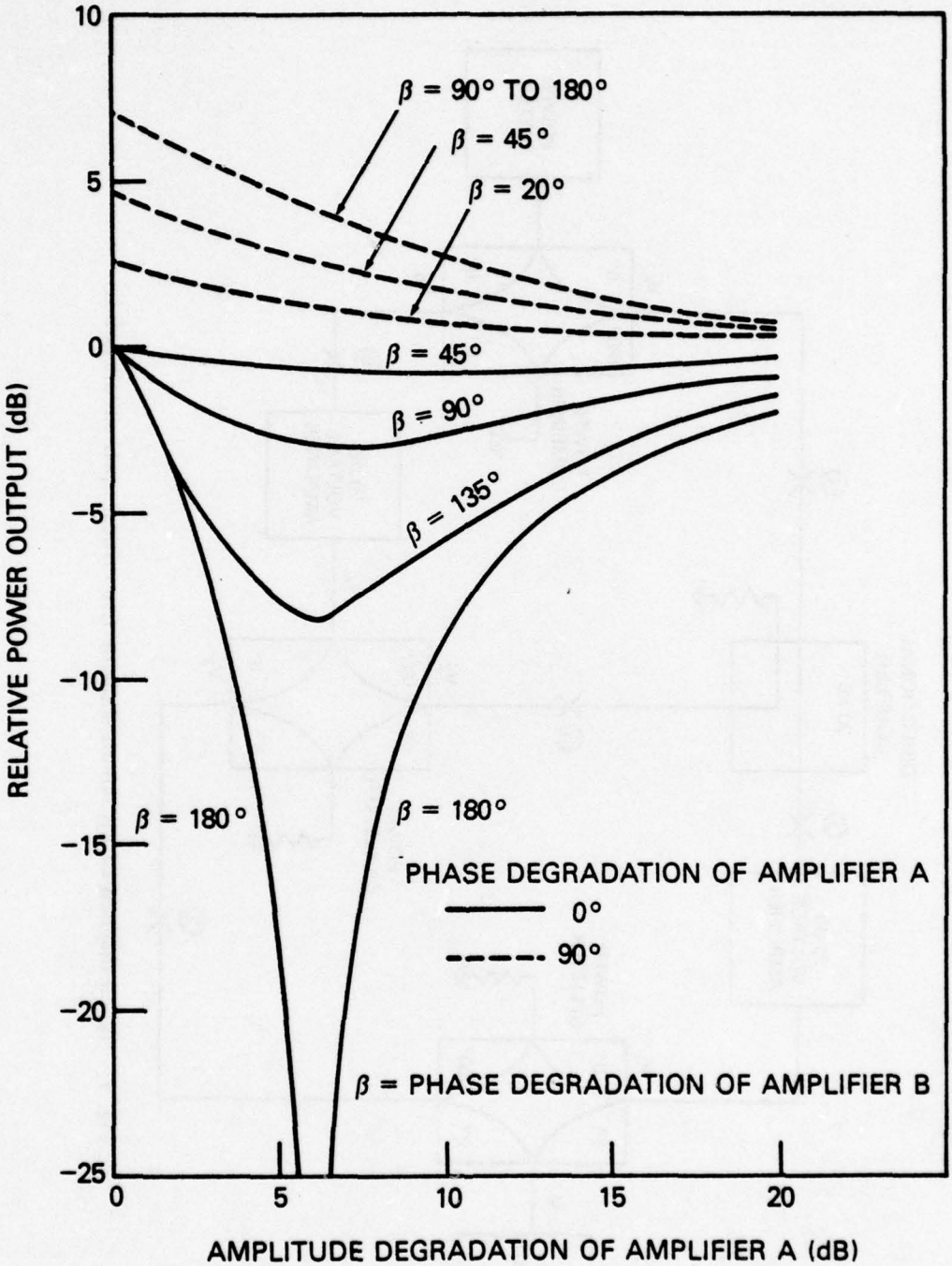


Fig. 6 — Relative output of PR circuit when there is no amplitude degradation of amplifier B

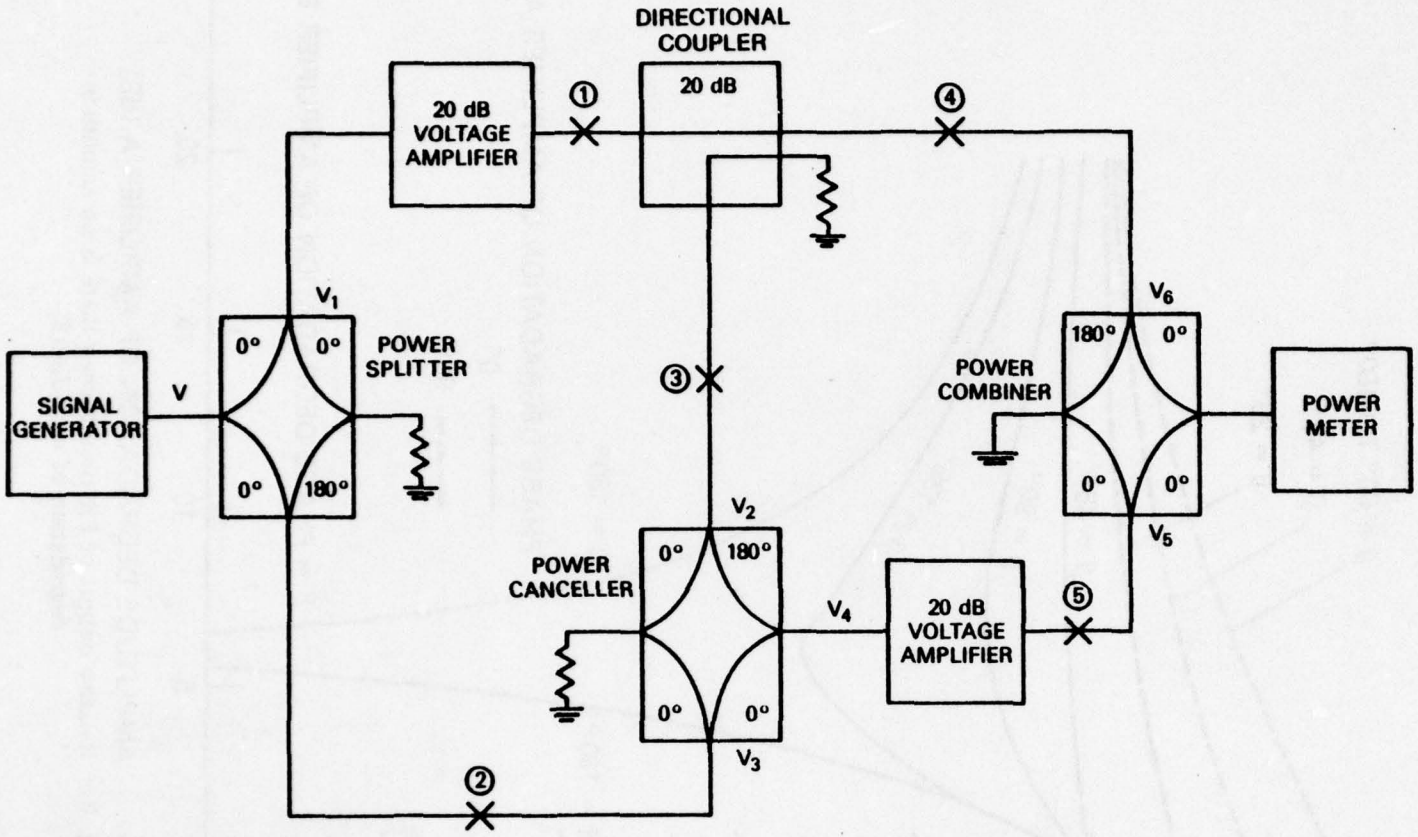


Fig. 7 — Block diagram of PR circuit showing five critical open circuit points

Case I: Open circuit at Point 1

$$V_6 = V_2 = 0$$

$$V_{out} = 5\, D_2\, V_3\, e^{j(\delta_4 + \beta)}$$

$$V_{out} = \frac{5}{\sqrt{2}}\, D_2\, V\, e^{j(\delta_2 + \delta_4 + \beta + \omega t)} \qquad (12)$$

For correct phase adjustment and normal operation of the second amplifier,

$$V_{out} = \frac{5}{\sqrt{2}}\, V\, e^{j\, \delta_3 \omega t}$$

Hence, the open circuit will have no effect on the output voltage [Eq. (A31)].

Case II: Open Circuit at Point 2

$$V_3 = 0$$

$$V_{out} = \frac{5V}{\sqrt{2}} \left[D_1\, e^{j(\delta_3 + \theta)} - D_2\, e^{j(\delta_1 + \delta_4 + \theta + \beta)}\right] e^{j\omega t} \qquad (13)$$

For correct phase adjustment and normal operation of both amplifiers,

$$V_{out} = 0$$

Case III: Open Circuit at Point 3

$$V_2 = 0$$

$$V_{out} = \frac{5V}{\sqrt{2}} \left[D_1\, e^{j(\delta_3 + \theta)} + D_2\, e^{j\,(\delta_2 + \delta_4 + \beta)}\right] e^{j\omega t} \qquad (14)$$

For correct phase adjustment and normal operation of <u>both</u> amplifiers

$$V_{out} = 2 \left[\frac{5V}{\sqrt{2}} \; e^{j(\delta_3 + \omega t)} \right]$$

Hence, the output power will increase by 6 dB.

<u>Case IV</u>: Open Circuit at Point 4

$$V_6 = 0$$

$$V_{out} = \frac{5V}{\sqrt{2}} \; D_2 \; [e^{j\delta_2} - D_1 \; e^{j(\delta_1 + \theta)}] \; e^{j(\delta_4 + \beta + \omega t)} \qquad (15)$$

For correct phase adjustment and normal operation of the <u>first</u> amplifier, $V_{out} = 0$.

<u>Case V:</u> Open Circuit at Point 5

$$V_5 = 0$$

$$V_{out} = \frac{5VD_1}{\sqrt{2}} \; e^{j(\delta_3 + \theta + \omega t)} \qquad (16)$$

For correct phase adjustment and normal operation of the <u>first</u> amplifier, the open circuit will have no effect on the output voltage.

From the foregoing analysis, it is clear that the most critical points so far as circuit reliability is concerned are (2) and (4). Open circuits at these locations produce complete circuit failure; open circuits at other points result in only partial or even no change in circuit output. The same conclusions would hold if short circuits occurred at these points in place of the open circuits.

It should be noted that the foregoing analysis was for ideal conditions. In practice, deviations from these predictions will occur due to mismatches induced by the failures at the critical points.

CHARACTERISTICS OF THE TEST CIRCUIT

The measured frequency response for each amplifier is shown in Fig. 8. With a 5.0 mV input signal, the output is 102.7 mV at the midband frequency of 435 MHz. This is a circuit gain of 26.3 dB. The output varies $\pm$ 0.13 dB over the entire range of 400 to 470 MHz.

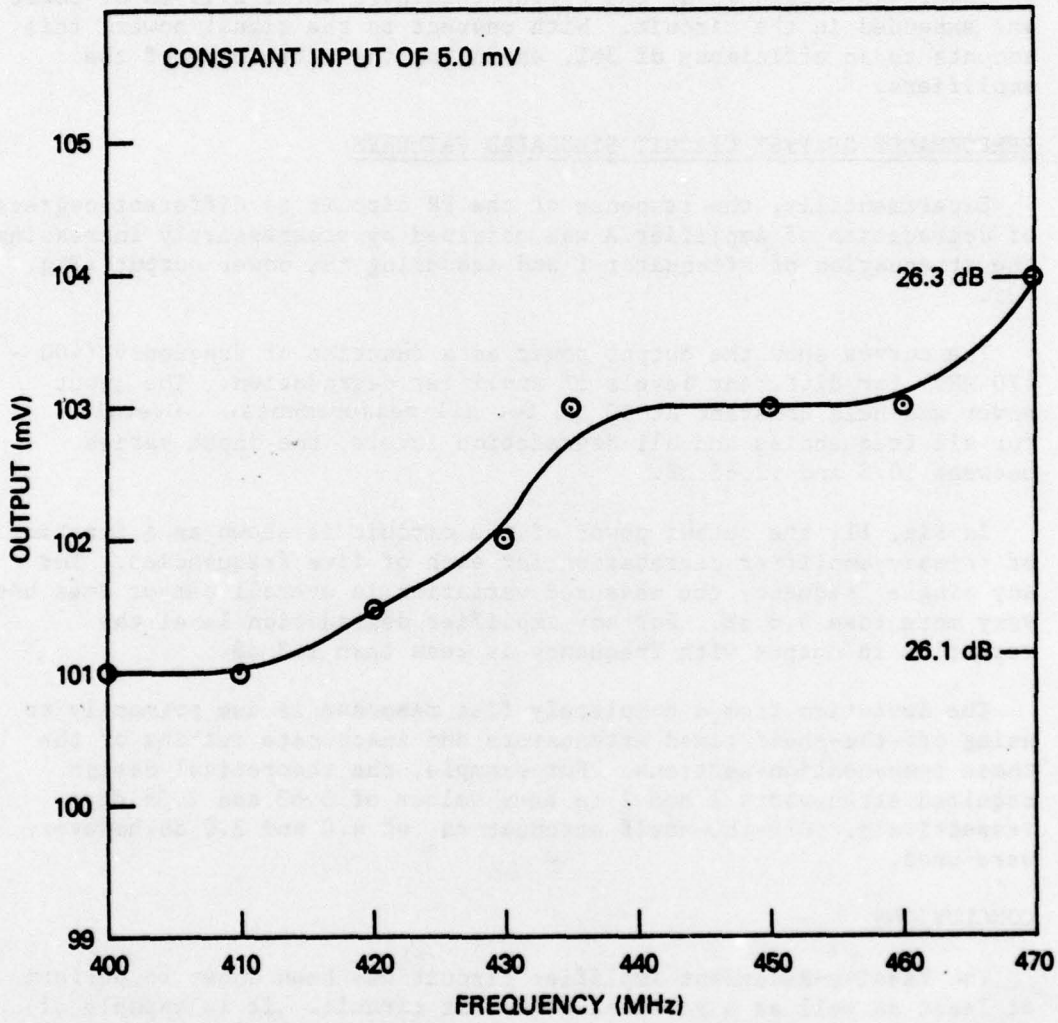


Fig. 8 — Frequency response of single amplifier

There is considerable loss in gain in the complete PR circuit as compared to the single amplifier. With no degradation in Amp. A, measurements on the PR circuit varies from 10.8 dB at 400 MHz to 12.1 dB at 460 MHz (Fig. 9). This represents a response of $\pm$ 0.65 dB over the entire frequency range.

The signal power dissipated in the PR circuit is therefore quite large. With 50 μW of power applied to the input terminals, 1.24 mW of power was available at the output terminals while 2.19 mW of power was expended in the circuit. With respect to the signal power, this amounts to an efficiency of 36%, excluding the efficiency of the amplifiers.

PERFORMANCE OF TEST CIRCUIT SIMULATED FAILURES

Experimentally, the response of the PR circuit to different degrees of degradation of Amplifier A was obtained by progressively increasing the attenuation of Attenuator 1 and measuring the power output (Fig. 10).

The curves show the output power as a function of frequency (400 - 470 MHz) for different levels of amplifier degradation. The input power was held constant at 50 μw for all measurements. Overall, for all frequencies and all degradation levels, the input varies between 10.8 and 12.65 dB.

In Fig. 11, the output power of the circuit is shown as a function of primary amplifier degradation for each of five frequencies. For any single frequency the measured variation in overall output does not vary more than 0.6 dB. For any amplifier degradation level the variation in output with frequency is less than 1.3 dB.

The deviation from a completely flat response is due primarily to using off-the-shelf fixed attenuators and inaccurate cutting of the phase compensation sections. For example, the theoretical design required Attenuators 1 and 2 to have values of 3.63 and 2.38 dB, respectively. Off-the-shelf attenuators of 4.0 and 3.0 dB,however, were used.

CONCLUSIONS

The Passive-Redundant amplifier circuit has been shown to perform at least as well as a parallel redundant circuit. It is capable of performing its own fault detection and subsequent compensation without auxiliary circuitry. It maintains a constant output, whether one amplifier fails completely or both degrade gracefully. The circuit studied in this report operated over the frequency range of 400 - 470 MHz. There is a loss of power through the system and the circuit is best used in an application where power transfer is not critical.

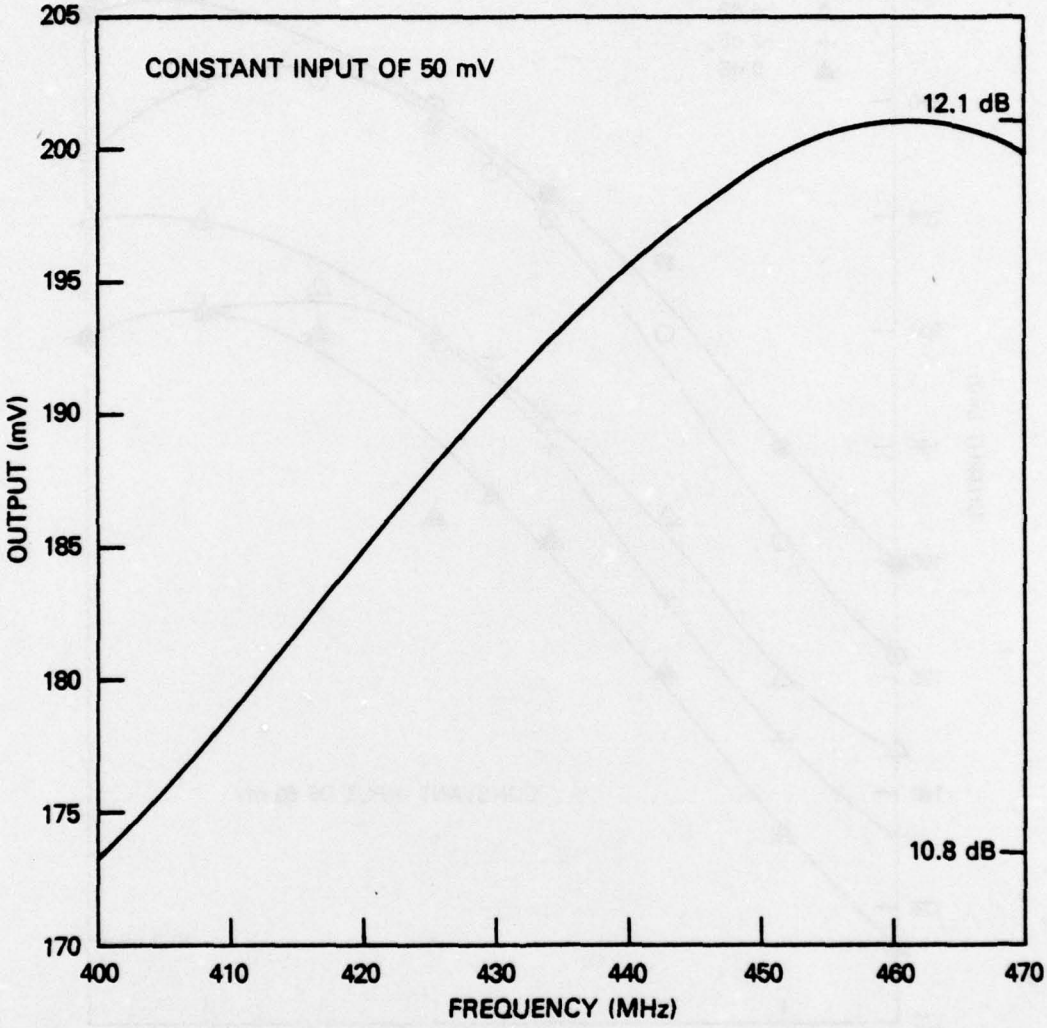


Fig. 9 — Frequency response of passive-redundant circuit with no degradation

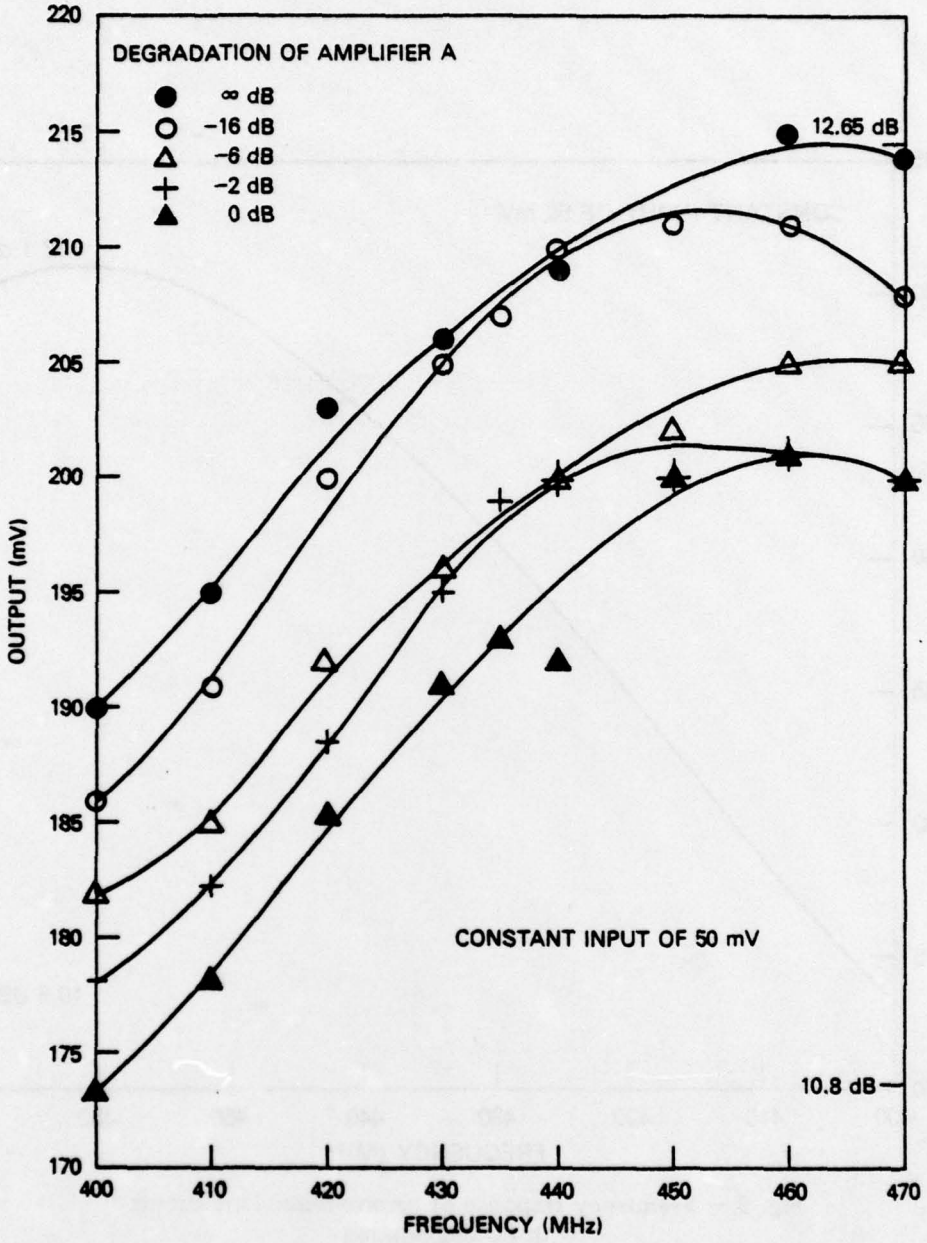


Fig. 10 — Frequency response of passive redundant circuit with various levels of primary amplifier gain degradation

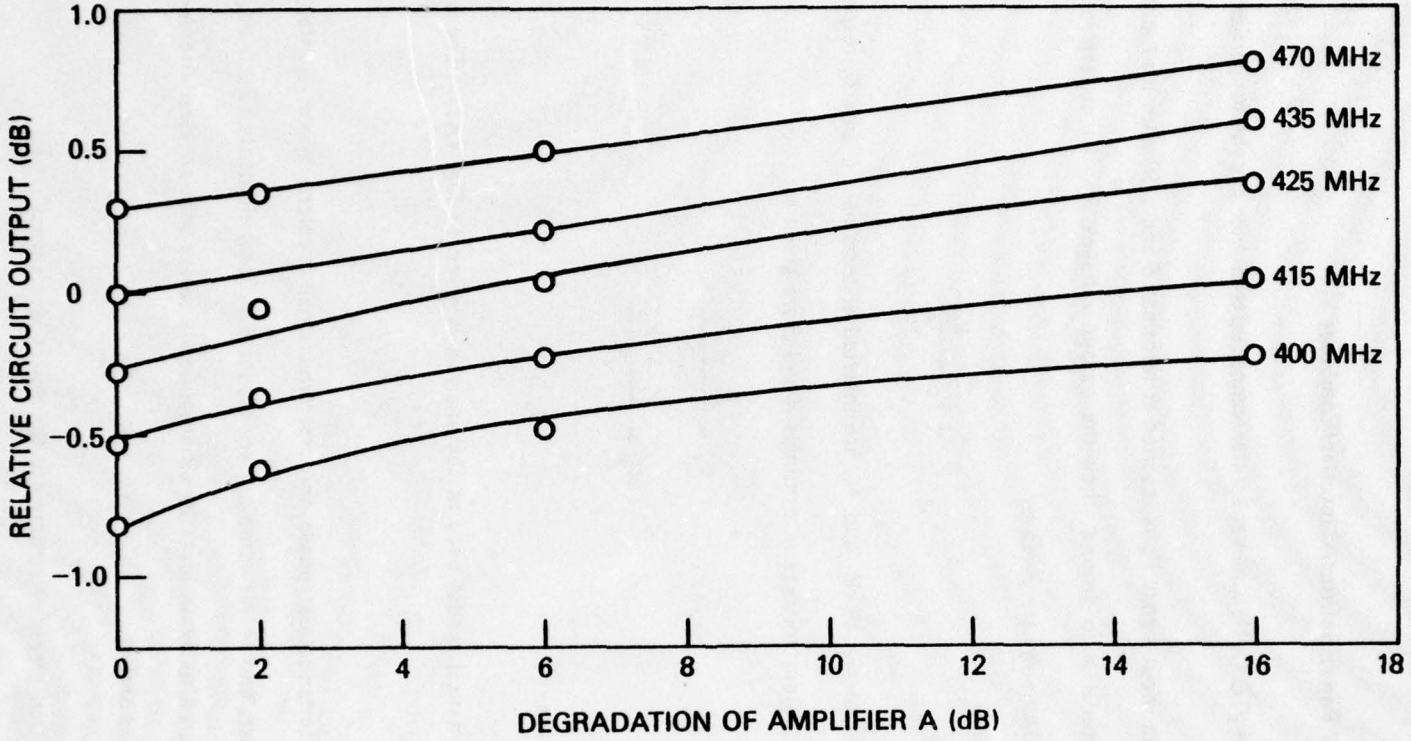


Fig. 11 — Measured circuit output as a function of primary amplifier gain degradation

APPENDIX A

DERIVATION OF OUTPUT POWER

A.1 Properties of Power Splitter/Canceller/Combiner

Referring to Fig. (A1), a power splitter/canceller/combiner has the properties:

1. If an input signal V_B is inserted at terminal B and a 50 ohm load is inserted from terminal A to ground, then the output voltages V_C, V_D at terminals C and D, respectively, are given by

$$V_C = V_D = \frac{V_B}{\sqrt{2}} \tag{A1}$$

2. If input signals V_C and V_D are inserted at terminals C and D, respectively, then the output voltages at terminals A and B are given by:

$$V_A = \frac{V_C - V_D}{\sqrt{2}} \tag{A2}$$
$$V_B = \frac{V_C + V_D}{\sqrt{2}}$$

A.2 Output Voltage

The mathematical model used in the analysis is given in Fig. (A1). The basic assumptions are:

1. All attenuators, phase shifters, directional couplers, power splitter, power canceller, and power combiner are modeled as ideal elements. Each amplifier is considered to by an ideal 20 dB amplifier in series with an ideal attenuator and ideal phase shifter.

2. Neither amplifier saturates at the power levels used.

The basic parameters of the circuit are:

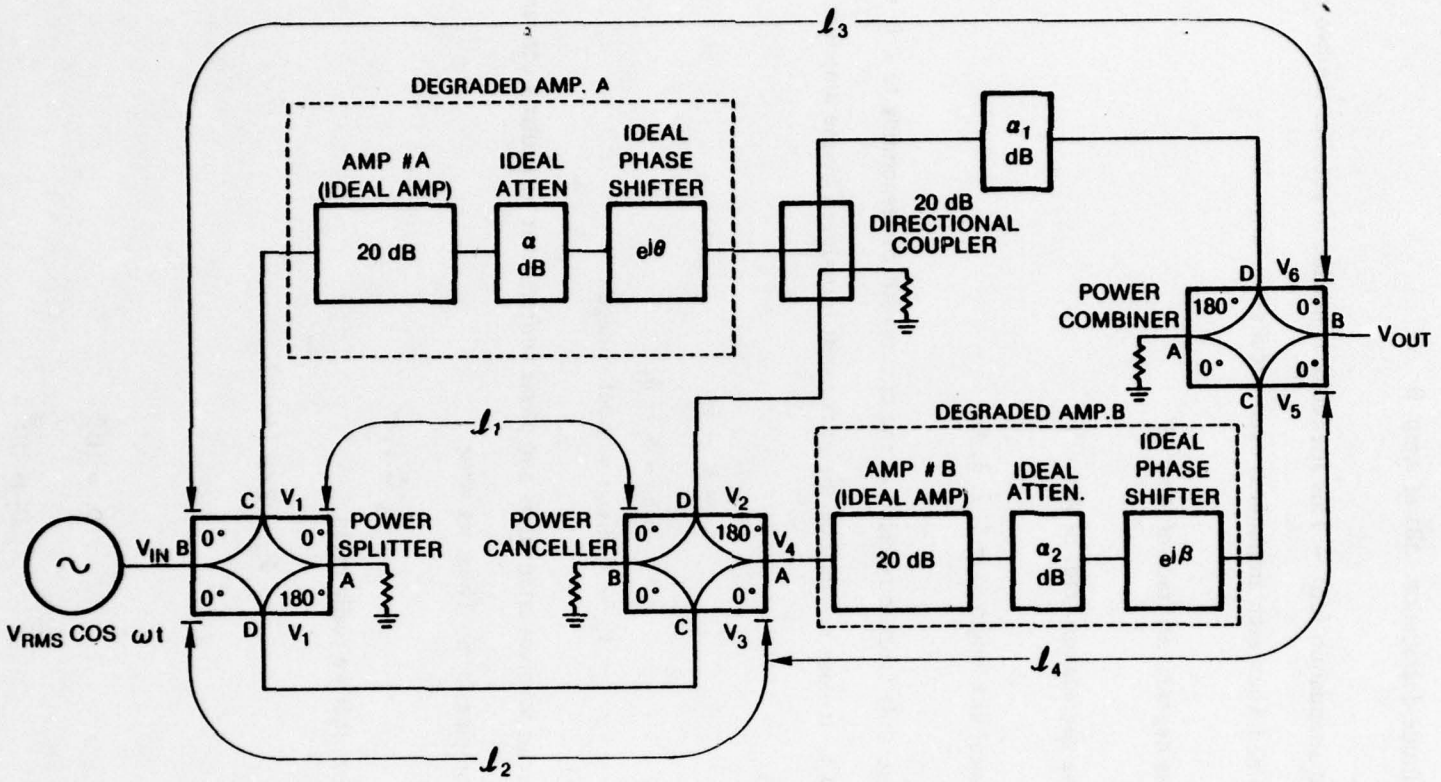


Fig. A1 — Ideal parallel redundant amplifier

α = amplitude degradation (dB) of Amp. A

α_2 = amplitude degradation (dB) of Amp. B

α_1 = fixed attenuation (db) — This attenuator is needed to equalize the two outputs obtained when each amplifier is open circuited in turn

θ = phase degradation (rad) of Amp. A

β = phase degradation (rad) of Amp. B

l_i = physical line length ($i = 1, 2, 3, 4$)

δ_i = phase shift (rad) introduced in the circuit path corresponding to l_i ($i = 1, 2, 3, 4$,). It does not include the phase shift introduced by the amplifier in that path.

$$\Delta_1 \stackrel{\Delta}{=} \delta_1 - \delta_2 \tag{A3}$$

$$\Delta_2 \stackrel{\Delta}{=} \delta_3 - \delta_2 - \delta_4$$

$$V_{in} = V \cos \omega t = \text{input voltage} \tag{A4}$$

Since the PR circuit involves attenuators and phase shifters, it is particularly convenient to express voltages in complex form. Thus, we write

$$V_{in} = Ve^{j\omega t}$$

where, it is understood, that we really mean

$$V_{in} = \text{Real } (Ve^{j\omega t})$$

Further, let

$$D_1 = 10^{\frac{\alpha}{20}}$$

$$D_2 = 10^{\frac{\alpha_2}{20}}$$

$$D_3 = 10^{\frac{\alpha_1}{20}} \tag{A5}$$

Referring to Fig. (A1), it follows that

$$V_1 = \frac{V}{\sqrt{2}} e^{j\omega t} \tag{A6}$$

$$V_2 = D_1 V_1 10^{\frac{20-20}{20}} e^{j(\delta_1 + \theta)}$$

or

$$V_2 = D_1 V_1 e^{j(\delta_1 + \theta)} \tag{A7}$$

$$V_3 = V_1 e^{j\delta_2} \tag{A8}$$

$$V_4 = \frac{V_3 - V_2}{\sqrt{2}} \tag{A9}$$

$$V_5 = 10^{\frac{20}{20}} D_2 V_4 e^{j(\delta_4 + \beta)}$$

or

$$V_5 = 10 D_2 V_4 e^{j(\delta_4 + \beta)} \tag{A10}$$

$$V_6 = 10 D_1 D_3 V_1 e^{j(\delta_3 + \theta)} \tag{A11}$$

Finally,

$$V_{out} = \frac{V_5}{\sqrt{2}} + \frac{V_6}{\sqrt{2}} \tag{A12}$$

In terms of the intermediate voltages,

$$\frac{V_5}{\sqrt{2}} = 5 D_2 (V_3 - V_2) e^{j(\delta_4 + \beta)} \tag{A13}$$

and, anticipating the setting of $D_3 = \frac{1}{\sqrt{2}}$ [Eq. (A24)],

$$\frac{V_6}{\sqrt{2}} = \frac{5 D_1}{\sqrt{2}} V e^{j(\delta_3 + \theta + \omega t)} \tag{A14}$$

Hence

$$V_{out} = \frac{5 D_1}{\sqrt{2}} V e^{j(\delta_3 + \theta + \omega t)} + 5 D_2 (V_3 - V_2) e^{j(\delta_4 + \beta)} \tag{A15}$$

where, the first term is the contribution from the primary circuit and the second term is the contribution of the secondary circuit. This equation is useful in determining the effects of short circuits on the system.

Using Eqs. (A6), (A8) and (A9),

$$\frac{V_5}{\sqrt{2}} = \frac{5D_2V}{\sqrt{2}}\left[e^{j\delta_2} - D_1 e^{j(\delta_1+\theta)}\right] e^{j(\delta_4+\beta+\omega t)} \tag{A16}$$

Thus, keeping D_3 undetermined,

$$V_{out} = \frac{5V}{\sqrt{2}}\left[\sqrt{2}\,D_1D_3e^{j(\delta_3+\theta)} + D_2e^{j(\delta_2+\delta_4+\beta)} - D_1D_2e^{j(\delta_1+\delta_4+\theta+\beta)}\right] e^{j\omega t} \tag{A17}$$

This is the most general form for the output voltage.

It can also be written as

$$V_{out} = \frac{5V}{\sqrt{2}}\,De^{j(\delta+\omega t)} \tag{A18}$$

where

$$D^2 = (\sqrt{2}\,D_3D_1 + D_2 - D_1D_2)^2 +$$
$$2D_1D_2\Big\{D_2\Big[1-\cos(\theta+\Delta_1)\Big] + \sqrt{2}\,D_3D_1\Big[1-\cos(\beta+\Delta_1\cdot\Delta_2)\Big]\times$$
$$-\sqrt{2}\,D_3\Big[1-\cos(\theta-\beta+\Delta_2)\Big]\Big\} \tag{A19}$$

$$\tan\delta = \frac{\sqrt{2}\,D_3D_1\sin(\theta+\delta_3) + D_2\sin(\beta+\delta_2+\delta_4) - D_1D_2\sin(\theta+\beta+\delta_1+\delta_4)}{\sqrt{2}\,D_3D_1\cos(\theta+\delta_3) + D_2\cos(\beta+\delta_2+\delta_4) - D_1D_2\cos(\theta+\beta+\delta_1+\delta_4)} \tag{A20}$$

and, as before,

$$\Delta_1 \triangleq \delta_1 - \delta_2$$
$$\Delta_2 \triangleq \delta_3 - \delta_2 - \delta_4$$

Either of the two Equations (A17) or (A18) can be used to determine the circuit output, making allowance for a very general class of misadjustments. For proper phase adjustment, however, the equations are much simpler.

Let

$V_{1,out}$ = output voltage when Amp A is open-circuited ($D_1 = 0$) and Amp B is normal ($D_2 = 1, \beta = 0$)

$V_{2,out}$ = output voltage when Amp B is open-circuited ($D_2 = 0$) and Amp A is normal ($D_1 = 1, \theta = 0$)

$V_{3,out}$ = output voltage when Amp B has degraded partially ($D_2 \neq 0$) and Amp A is normal ($D_1 = 1, \theta = 0$)

For proper circuit operation

$$V_{1,out} = V_{2,out} = V_{3,out}$$

But

$$V_{1,out} = \frac{5V}{\sqrt{2}} e^{j(\delta_2 + \delta_4 + \omega t)} \tag{A21}$$

$$V_{2,out} = 5VD_3 e^{j(\delta_3 + \omega t)} \tag{A22}$$

$$V_{3,out} = \frac{5V}{\sqrt{2}} \left[e^{j\delta_3} + D_2 e^{j(\beta + \delta_2 + \delta_4)} - D_2 e^{j(\beta + \delta_1 + \delta_4)} \right] e^{j\omega t} \tag{A23}$$

From Eqs. (A21) and (A22),

$$D_3 = \frac{1}{\sqrt{2}} \quad (\alpha = 3dB) \tag{A24}$$

$$\delta_3 = \delta_2 + \delta_4$$

Hence, substituting into Eq. (A23),

$$\delta_1 = \delta_2$$

Thus, when the phase is properly adjusted in the circuit,

$$\Delta_1 = \Delta_2 = 0 \tag{A25}$$

and

$$V_{out} = \frac{5V}{\sqrt{2}} \left[D_1 e^{j\theta} + D_2 e^{j\beta} - D_1 D_2 e^{j(\theta + \beta)} \right] e^{j(\delta_0 + \omega t)} \tag{A26}$$

where

$$\delta_0 = \delta_3 = \delta_1 + \delta_4 = \delta_2 + \delta_4 \tag{A27}$$

Similarly,

$$V_{out} = \frac{5V}{\sqrt{2}} D e^{j(\delta + \omega t)} \tag{A28}$$

where

$$D^2 = (D_1 + D_2 - D_1 D_2)^2 + 2D_1 D_2 \Big\{ D_2[1 - \cos\theta] + D_1[1 - \cos\beta] - [1 - \cos(\theta - \beta)] \Big\} \tag{A29}$$

and

$$\tan\delta = \frac{D_1\sin(\theta+\delta_0) + D_2\sin(\beta+\delta_0) - D_1D_2\sin(\theta+\beta+\delta_0)}{D_1\cos(\theta+\delta_0) + D_2\cos(\beta+\delta_0) - D_1D_2\cos(\theta+\beta+\delta_0)} \tag{A30}$$

As long as the circuit is operating normally, i.e. ($D_1 = 1$, $\theta = 0$) and/or ($D_2 = 1$, $\beta = 0$), it can be seen from Eq. (A26),

$$V_{out} = \frac{5V}{\sqrt{2}}\, e^{j(\delta_0+\omega t)} \triangleq V_{norm} \tag{A31}$$

i.e.

$$D = 1,\ \delta = \delta_0$$

A.3 Power Output

The output power, P_{out}, across a load of Rohms is given by

$$P_{out} = \frac{25V^2D^2}{4R} \tag{A32}$$

where D^2 is defined in Eqs. (A19), (A29), (A31). If P_{norm} is the output power when the circuit is operating normally, then $D = 1$ and

$$P_{norm} = \frac{25V^2}{4R} \tag{A33}$$

It is convenient to define a normalized power output

$$P'_{out} = \frac{P_{out}}{P_{norm}} \tag{A34}$$

In general, then

$$P'_{out} = D^2 \tag{A35}$$

Lastly, a general expression for P'_{out} can be given as

$$P'_{out} = 10^{\frac{\alpha}{10}} + 10^{\frac{\alpha_2}{10}} + 10^{\frac{\alpha+\alpha_2}{10}} - 2\times 10^{\frac{\alpha}{20}+\frac{\alpha_2}{10}}\cos(\theta+\Delta_1)$$
$$- 2\times 10^{\frac{\alpha}{10}+\frac{\alpha_2}{20}}\cos(\beta+\Delta_1-\Delta_2) + 2\times 10^{\frac{\alpha+\alpha_2}{20}}\cos(\beta-\theta-\Delta_2) \tag{A36}$$