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AUTOMATIC NULL STEERING/SURVEILLANCE ARRAY SYSTEM
(ANSAS) FOR GLOBAL POSITIONING SYSTEM (GPS) APPLICATION

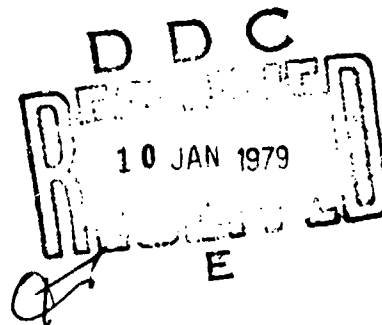
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cont. in the microprocessor drive Phase-Amplitude adjustments (Complex Weights) at the antenna elements such that a reduction in interference occurs after the summation of the antenna outputs.

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1. INTRODUCTION

This report describes the results of a developmental effort by the External Reference Navigation Branch, Navigation Division, of the Avionics Research and Development Activity to automate an anti-jam manpack antenna (AJMA) system, previously developed by this Activity, for the NAVSTAR Global Positioning System (GPS) manpack user equipment.¹ Using the correlation/nulling technique developed for the AJMA system, the Automatic Null Steering/Surveillance Array System (ANSAS) provides protection to GPS receivers against jamming by modifying the spatial antenna patterns in a manner that minimizes the interference. By designing a microcomputer controlled phased array network and combining it with the AJMA correlation/nulling technique, the capabilities of the AJMA have been extended to include its application in a dynamic environment.

2. BACKGROUND

The External Reference Navigation Branch was requested by the US Army Satellite Communications Agency to develop an AJMA system.² Following completion of the project, a recommendation was made that the required manual, azimuthal scanning and manual control of the correlator to sense then null, the jammer, respectively, be automated.

3. OBJECTIVE

The objective of this program was to develop an automatic null steering/surveillance array system (ANSAS) for GPS application which would provide to the ground GPS user a maximum field-of-view coverage in all directions other than in the direction of a dynamic jammer. In the jammer direction, only a substantially reduced gain would be available for its reception. In the absence of a jammer, ANSAS would continually provide a limited, azimuthal jammer surveillance scan of $\pm 22^\circ$ about the centerline of the directive beam of a broadside, planar phased array while maintaining complete upper hemispherical, omnidirectional coverage of GPS satellites. Upon the detection of a jammer, the ANSAS not only would provide an automatic null of the interference but also would maintain a null "tracking" of the jammer within the scan range of the phased array.

4. ANSAS CONFIGURATION

This section describes the theory of operation of ANSAS and system description.

a. Theory of "Nulling" Operation. The technique that is used in the ANSAS configuration is identical to the technique used in the AJMA system. The ANSAS configuration reduces directional interference by sensing signals in two channels, one channel containing the desired GPS satellite signals

¹"Anti-Jam Manpack Antenna (AJMA) for Global Positioning System Application," Gray, J.; DeSantis, C., AVRADCOM Technical Report TR-78-11, May 1978.

²SAMSO/YEA letter to USAECOM Avionics Laboratory, Navigation Technical Area, 25 May 1976, subject: AJ and Multipath Tasks.

(OMNI) and any unwanted jammer signals and the other channel containing only the unwanted signals (jammer). The selectivity to signal types in the jammer channel is achieved by using a highly directional, beam steered, phased array. The OMNI channel obtains signals from a near upper-hemispherical, omnidirectional coverage antenna. The jammer channel contains attenuator and phase controls (a "weighting" network) to produce a signal, which when "added" to the OMNI signal, just cancels the interfering signal in the combined ANSAS output. The result is a sharp null in the overall radiation pattern of the ANSAS in the direction of the jammer. The null depth attainable with the ANSAS directly increases the J/S power ratio of the existing GPS receiver.

Being an adaptive antenna system, ANSAS modifies its own radiation pattern by means of an internal feedback control. This operation requires active feedback circuitry that controls both the "weighting" network and the null "tracking" electronics according to an optimization criteria. To make the ANSAS adaptive, the output signal (postcorrelator) is compared with a "test" signal (precorrelator) to produce an error signal which drives the direction in which the weighting network will modify the ANSAS radiation pattern.

The criteria used in sensing the signals in the omni and jammer channels by ANSAS is the key to understanding how the nulling/correlation technique is applied. The primary characteristic of the GPS which permits the use of the ANSAS is the a priori knowledge that the GPS received signal level is always below the thermal noise level. This GPS signal characteristic enables ANSAS to employ amplitude-only sensors which can be power activated devices. Any above noise signals that are detected are treated as if they were interference sources, and appropriately nulled by ANSAS.

b. System Description. A block diagram of the various components of the ANSAS is shown in Figure 1. ANSAS is shown to consist of three major subsystems: The Antenna system, the Microwave Receiver system, and the Steerable Null Antenna Processor (SNAP) system. This section will describe, in general, the operation of ANSAS with respect to these three major subsystems. Specific details of the individual subsystems will be covered in subsequent sections in this report.

Beginning with the GPS omni antenna, all signals received by this antenna will be directed to the microwave receiver's correlator where they are combined with the weighted signals received by the phase array. The resulting combined correlator signal (postcorrelator) then goes to a sensor which converts the post correlator power to a voltage, ready for use by the SNAP system. The post correlator signal is not allowed to input to the GPS receiver until the SNAP system senses that the interference has been "nulled."

Meanwhile, the signal received by one half of the phased array goes through a weighting filter which controls the amplitude and phase of the signal inputs. The remaining half of the phased array goes through a scanning network, which through commands issued by the SNAP system, enables the beam steering of the phased array. The input of the scanning network is then combined with the remainder of the array in the weighted filter. This weighted signal (precorrelator) then goes to the correlator to be combined with the GPS omni signal. The power of the precorrelator signal is also detected and converted to a voltage for input to the SNAP system.

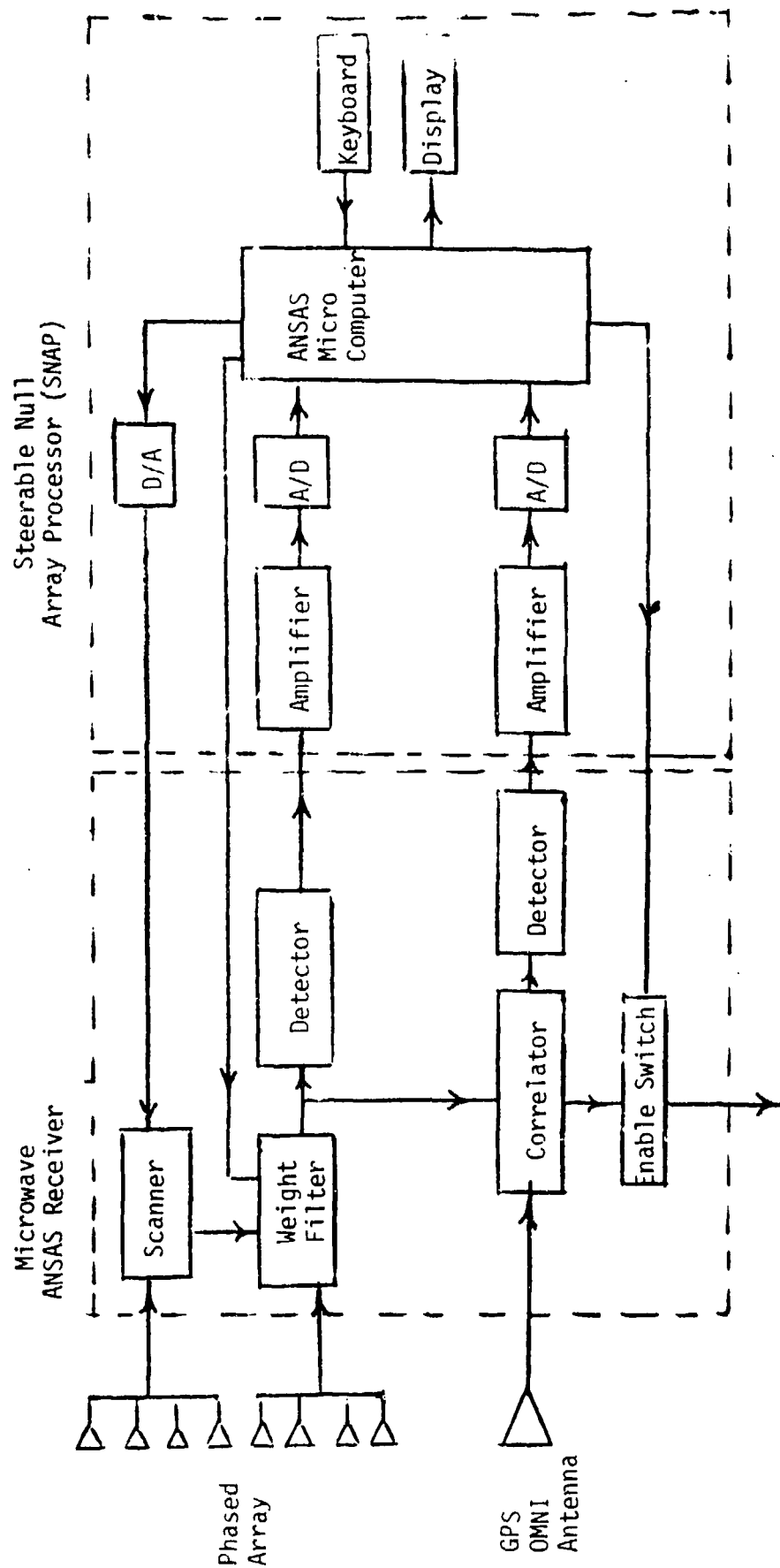


Figure 1. ANSAS block diagram

When the pre and postcorrelator signals are inputted to the SNAP system, they are amplified and converted to digital signals for use by the microcomputer. The microcomputer calculates the error signal and determine the proper weighting filter/scanning values required to null the interference. When the proper values are chosen, a command is issued to generate the signals required to change the settings of the scanning network, weighting network, and an enable switch.

5. ANTENNA SYSTEM DESCRIPTION (ELECTRICAL/MECHANICAL)

This section describes the antennas used in the ANSAS configuration. The description includes all the electrical, mechanical, and radiation pattern characteristics of the antennas.

a. GPS Omni Directional (OMNI) Antenna. The GPS antenna used for the ANSAS system to provide reception of the desired GPS satellites was developed in-house. This antenna is a narrow-band, dual frequency (1227 MHz, 1575 MHz), spherically shaped antenna. Designed to receive right-hand circularly polarized (RHCP) signals, it has an input VSWR (50) 1.5:1, gain (horizon) ≈ 0 dBIC and, in general, meets or exceeds the specifications for the GPS user equipment.³ This unit (Figure 2) stands 15-cm high, measures 8 cm in diameter, and weighs less than 0.5 kg.

Elevation and azimuthal radiation patterns of the OMNI only portion of the ANSAS were taken in an anechoic chamber and are shown in Figure 3a and b. The resulting pattern (Figure 3a) shows approximately at ≥ 0 dB upper hemispherical coverage, except for a -5 dB level at 180°. Its azimuthal pattern (Figure 3b) is approximately uniform, circular at ≈ 0 dB; maximum deviations of -3 dB at 0° and -7 dB at 180°. The OMNI has, therefore, been shown to meet the GPS antenna specifications which call for a uniform, upper hemispherical, coverage (gain of ≈ 0 dB) as well as omni directional coverage.

b. Phased Array. An in-house development of a lightweight, portable, RHCP, narrow beam-width (3 dB $\approx 25^\circ$), 1575-MHz center frequency, directional array was required to design the ANSAS.

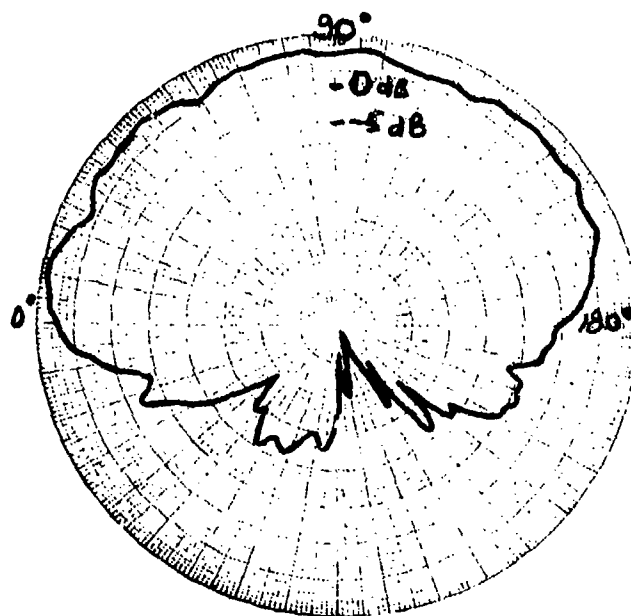
Printed circuit board techniques were used in designing the array antenna. The number of antenna elements (aperture size) employed in this array determines the beamwidth; the excitation and the phase relationship between the individual elements determine the directivity of the beam and sidelobe level.

In order to produce an effective, simple adaptive array with a narrow beam, highly directive steering capability while maintaining a reasonable, lightweight size, an eight element "four by four" array was designed (Figure 4). Two rows of four single element RHCP microstrip radiators were fabricated; each radiator resonating at 1.575 GHz (BW_{3dB} ≈ 35 MHz). The antenna array was masked on teflon-fiberglass ($\epsilon_r \approx 2.56$) printed circuit boards of 0.62-mm thickness. It uses a parallel feed network whose two-way power splits and equal line lengths produces equal power and equal phase to the feed points of each row of four antenna radiators. All the radiators were etched on one side of a

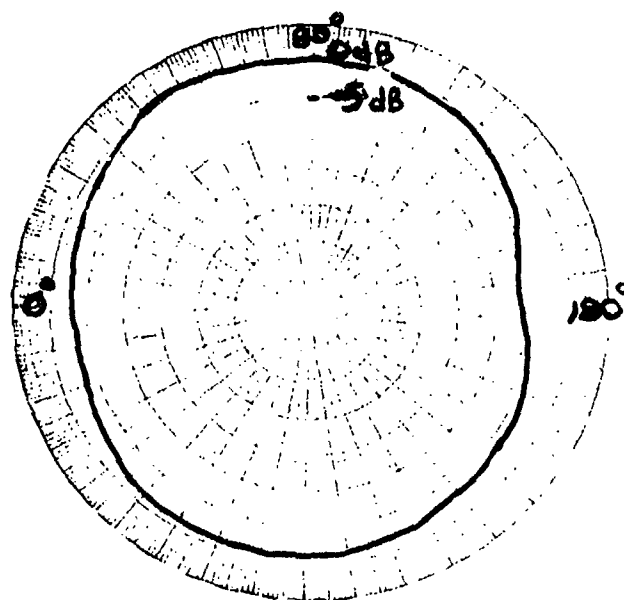
³System Specification for GPS User System Segment, SS-US-101B, 30 Sep 1974, Code Ident 12436.



Figure 2. GPS omni-directional (OMNI) antenna
(scale = inches)



a - elevation plane



b - azimuthal plane

Figure 3. Measured radiation pattern, ANSAS GPS spherical (OMNI) antenna only, 1575-MHz, right-hand circular polarization

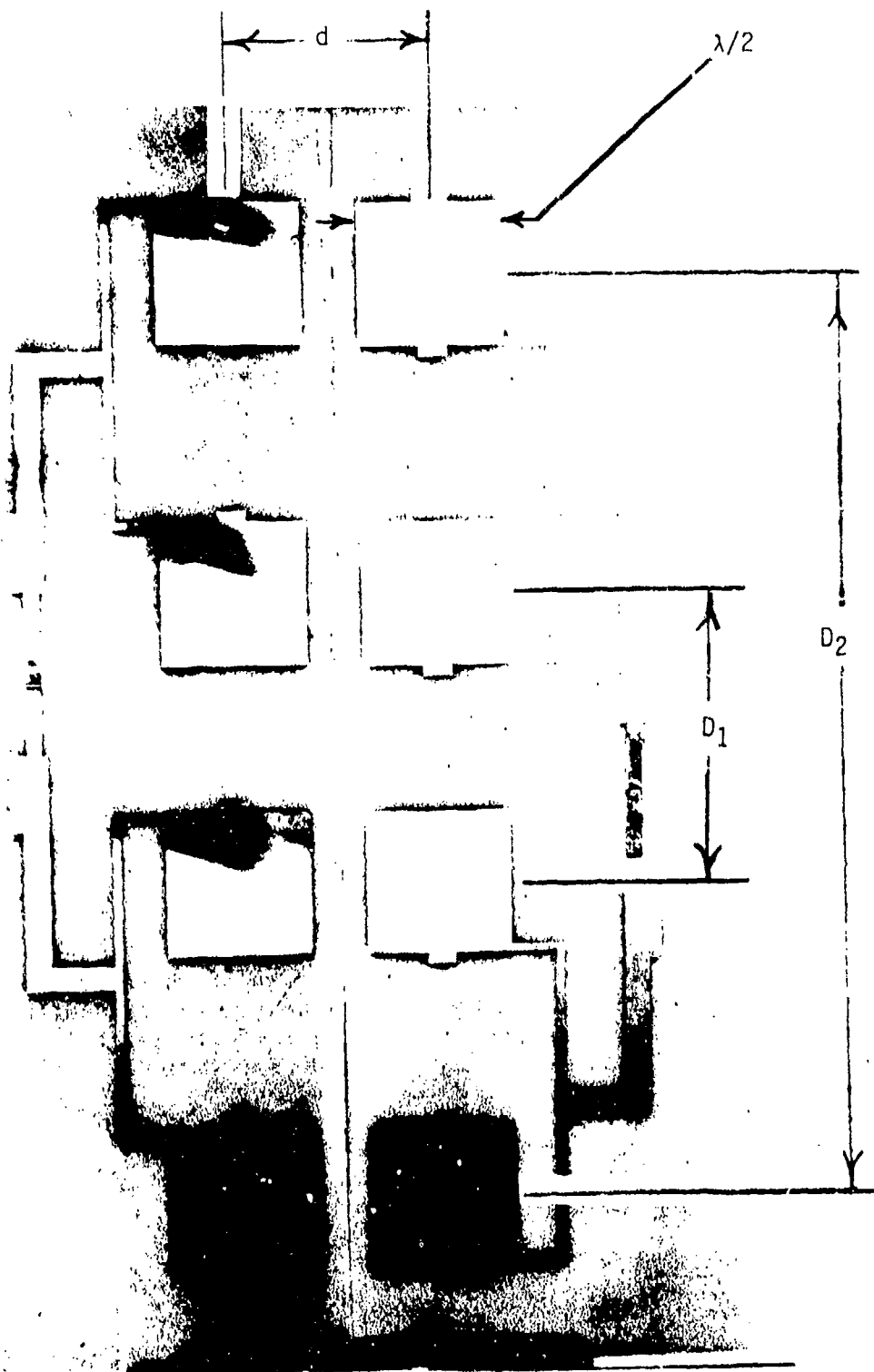


Figure 4. ANSAS phased array
(scale = inches)

microwave printed circuit board, the reverse side serving as the ground plane. A coaxial, ground plane mounted feed drives the array at its center point. Each radiator measures approximately 7.6 cm ($\lambda/2$) and acts as a crossed-dipole element. Array dimensions are 40.64 by 40.64 by 0.625 cm and the weight is less than 0.25 kg.

Depending upon the relative position of the elements with respect to each other and the signal frequency, the antenna array gain will be greater in some directions than in others.

Based upon previously derived designs,¹ the "optimum gain" spacings between the elements were calculated to be $D_1 = 0.3125\lambda$, $D_2 = 1.0\lambda$ for each vertical row of elements. (D_1 and D_2 are vertical spacings between individual radiators.)

A constraint was imposed in limiting the spacing between the two rows of elements to 0.6λ to minimize any mutual coupling between the individual radiators.

If the output signal from each element is delayed with respect to a reference element by a given amount, the direction in which maximum gain occurs can be changed. The result is a directional antenna with a main beam that can be pointed in any direction simply by changing the delays.

A computer simulation program for the array was written such that parameter trade-offs could be evaluated and the performance of the selected configuration estimated. The results of the simulation would represent the "Array Factor" of the phased array as a function of position in azimuth and elevation. The design equations considered only the far field pattern of the antenna radiators. The "Array Factor" is independent of the radiation characteristics of the individual radiators, depending only on the geometry of the arrangement as well as the relative phases and amplitudes of excitation.

A further constraint was imposed on the design of the array in order to simplify the design equations. Each row of elements was fixed with a common delay, thus reducing the design problem to an interferometer calculation. Several theoretical radiation patterns were made for various spacing between the two vertical rows using the following equations:

For elevation pattern:

$$E_e = 2E_0 [\cos (kD_1 \cos \theta) + \cos (kD_2 \cos \theta)]$$

For azimuth pattern:

$$E_a = \frac{E_e}{2} \cos \left(k \frac{d}{2} \sin \theta + \frac{\phi}{2} \right)$$

where

E_0 = amplitude of electric field

E_e = amplitude of E_0 in elevation plane

E_a = amplitude of E_0 in azimuth plane

$k = 2\pi/\lambda$

θ = polar angle

λ = wavelength

D_1, D_2 = vertical spacings between individual radiating elements

d = horizontal spacing between two rows of four radiating elements each

ϕ = phase (delay) between the two rows of elements

Calculated versus measured radiation patterns of the array for various spacings between the two vertical rows of radiators are shown in Figure 5a-k. It can be seen that the theoretical and experimental patterns correlate well.

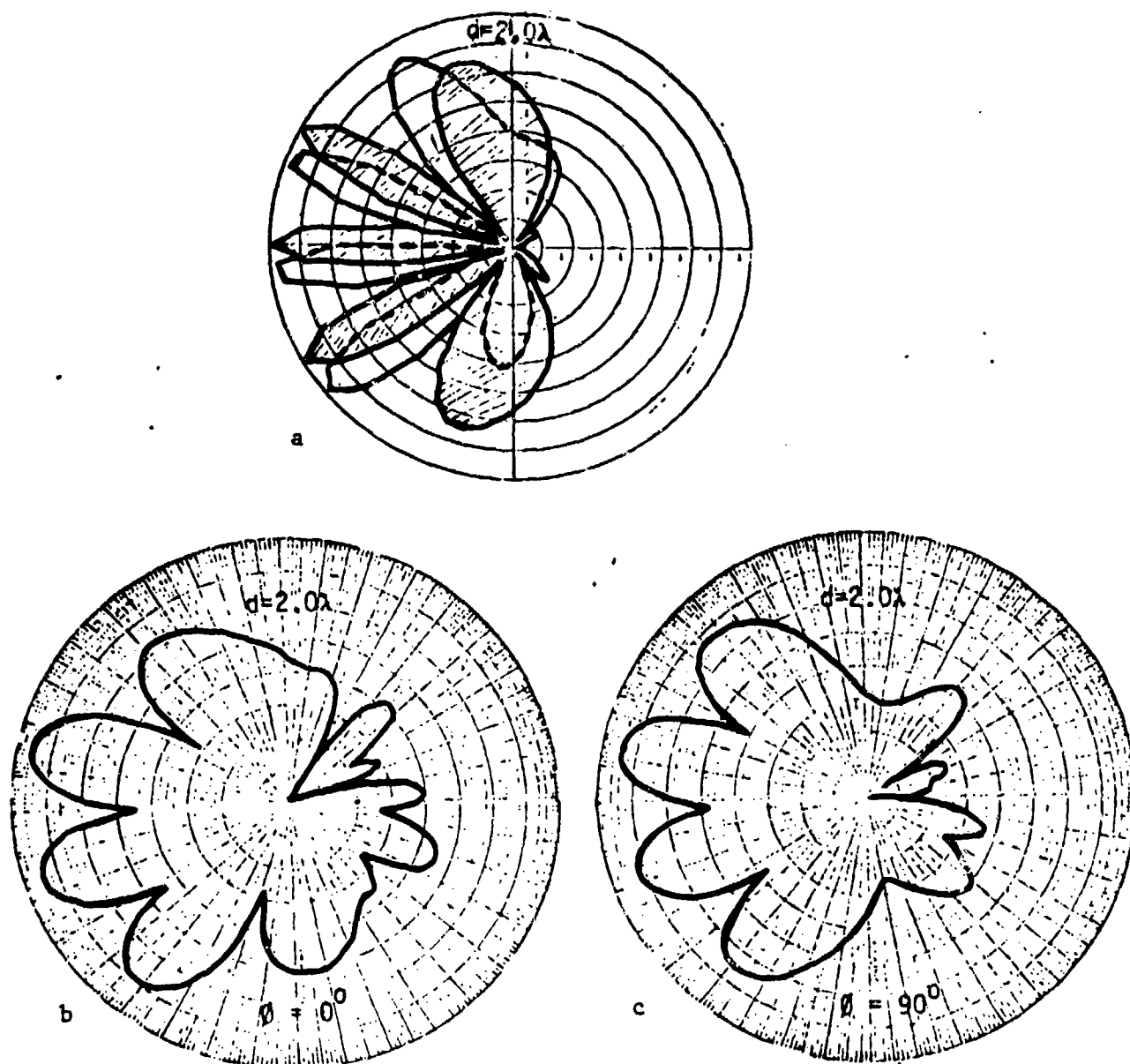
The shape of the beam pattern (and the width of the main beam) varied with steering direction. Because of array symmetry, the beam pattern revolves around the array axis. As the distance between the two rows of radiators was increased, sidelobes become evident.

The phased array design chosen for the ANSAS is shown in Figures 5g-k. Figure 5g predicts a beam direction (polar angle) of $\theta \approx 30^\circ$ for a $\phi \approx 90^\circ$ phase shift. Measured beam deviation, shown in Figure 5h and i is $\theta \approx 22^\circ$ for a $\phi = 90^\circ$ phase shift. As can be seen in Figure 5i, a sidelobe was developed when the phase shift was made; however, it will be below (≤ -10 dB) the main lobe and will not significantly affect the performance of ANSAS. Throughout the phase shift process, the elevation pattern measured in Figure 5k, remained unchanged.

6. MICROWAVE RECEIVER

Following reception of the GPS and interference signals by the OMNI and phased array antennas, the signals are processed by a microwave receiver, developed in-house, and shown in Figures 6 and 7. Half of the phased array signal goes to a scanning network consisting of a voltage controlled, varactor tuned, microstrip phase shifter. By linearly increasing the voltage from 0 to 4 volts DC, the phase of the input signal shifts from 0 to 90° . This control voltage is obtained from the SNAP system. Since the control voltage supplied by the SNAP was designed to be quantized in 0.4-volt steps, the phase varies discretely in 10° increments. A 90° phase causes the phased array beam to shift from the array centerline direction to 22° off center. (NOTE: It was demonstrated during laboratory tests that, depending upon which half of the array the scanning return was connected to, either a $+22^\circ$ or -22° phase shift off the centerline was achieved. By having scanning returns in both arms of the array, a $+22^\circ$ scan may, therefore, be obtained.)

Prior to combining the "weighted" signal through a -3 dB, 180° phase shift hybrid coupler, a sample of the attenuator output signal (the precorrelator signal) is measured through a -10 dB directional coupler. At the output of the



(a-i) Azimuth patterns of a 2 by 4 element array before and after a 90° phase shift is applied between the four element arrays. First the calculated patterns are shown followed by the measured patterns. Distance between antennas for the measured patterns is indicated at the top of each pattern, phase at the bottom. For the calculated patterns, the unshaded region indicates the result of the 90° -phase shift.

(j-k) Elevation pattern of a 2 by 4 element array first calculated, then measured.

Figure 5. Azimuth patterns of a 2 by 4 element array before and after a 90° phase shift is applied between the four element arrays

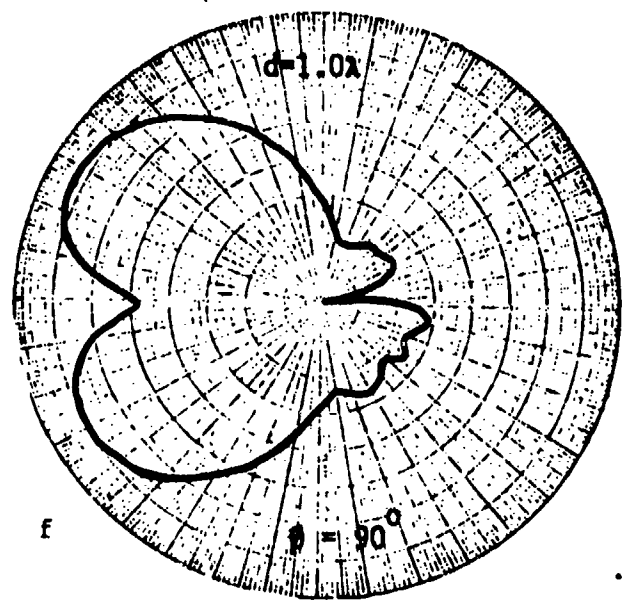
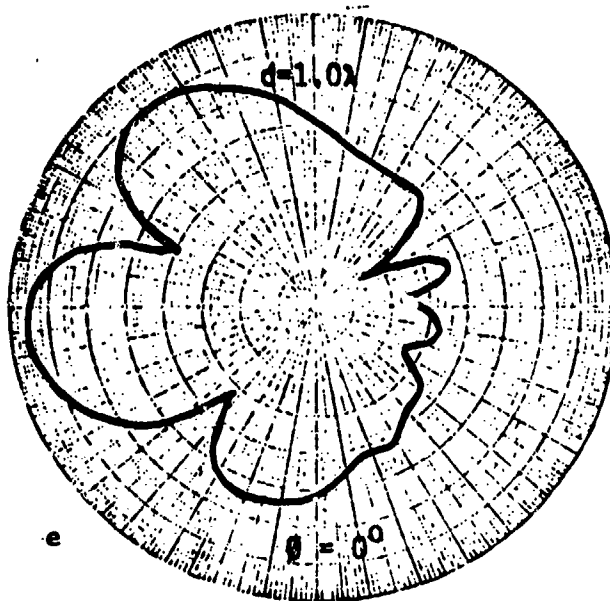
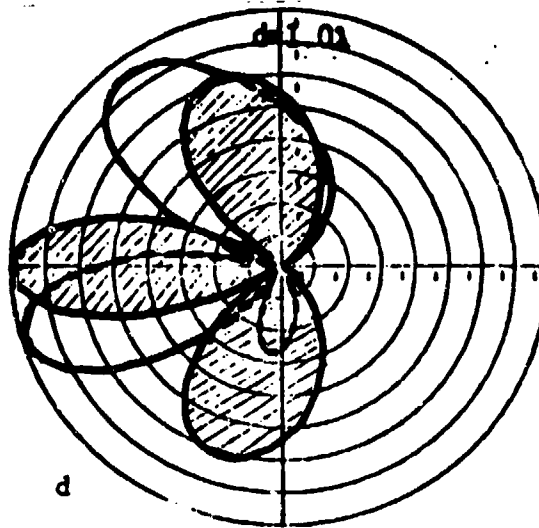


Figure 5 - Continued

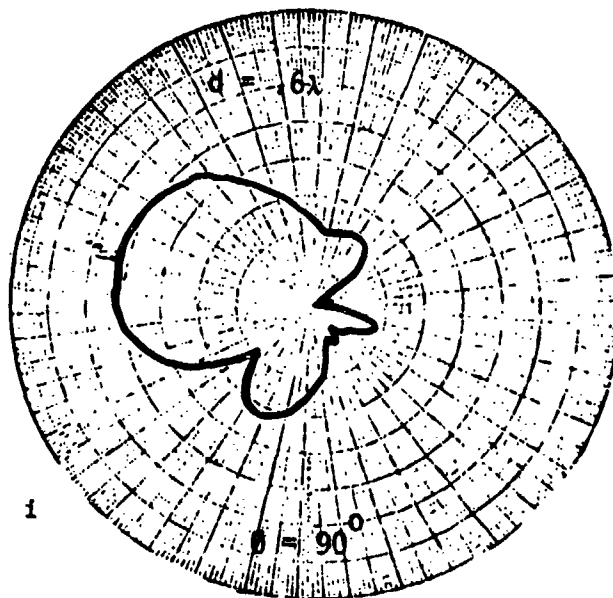
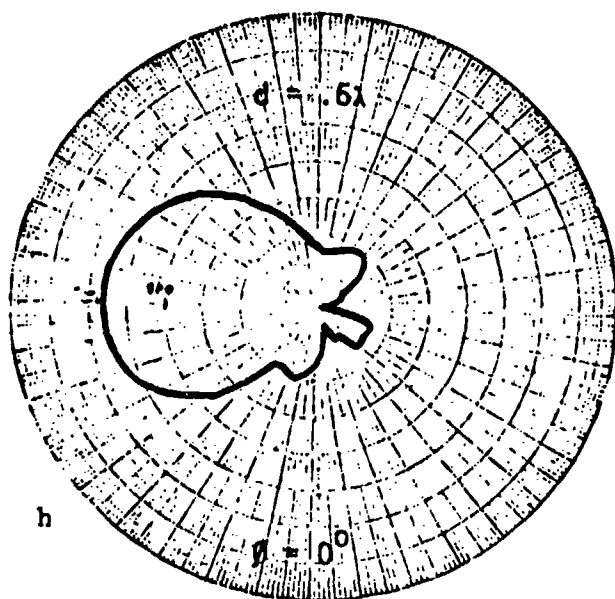
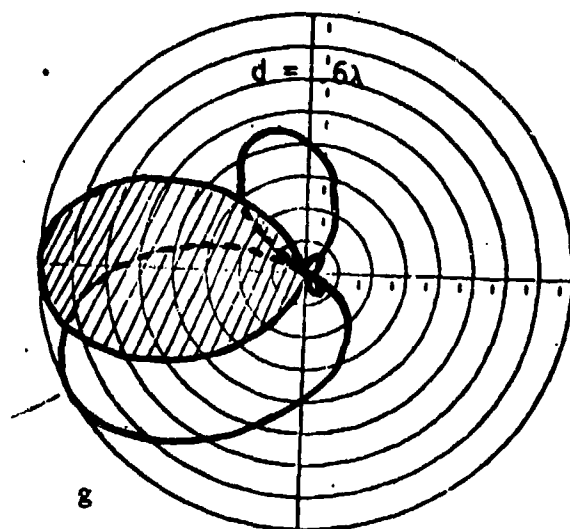


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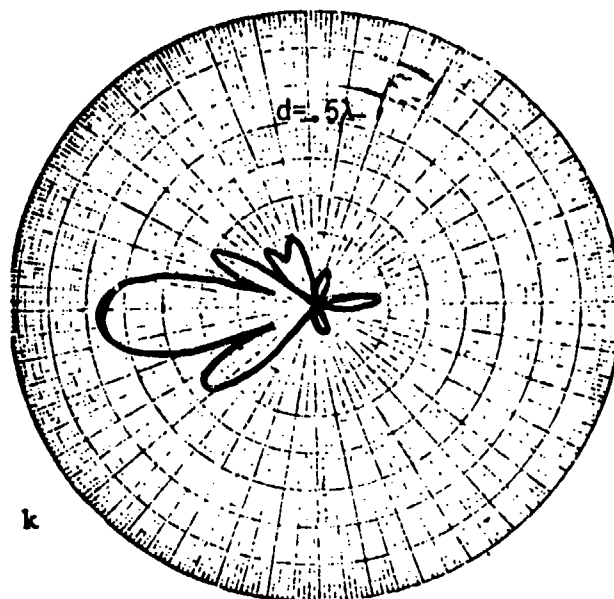
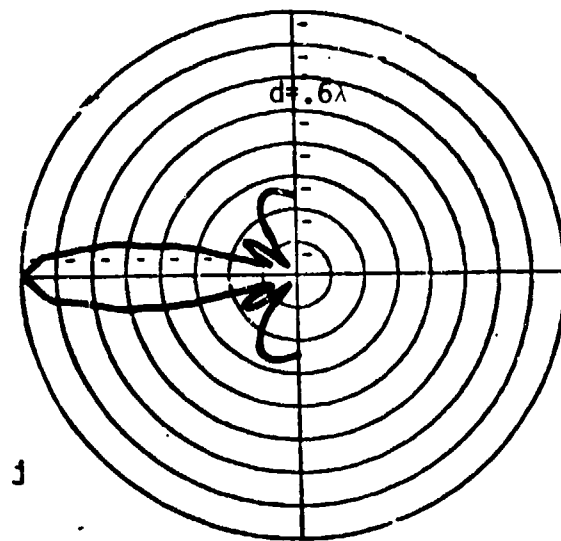


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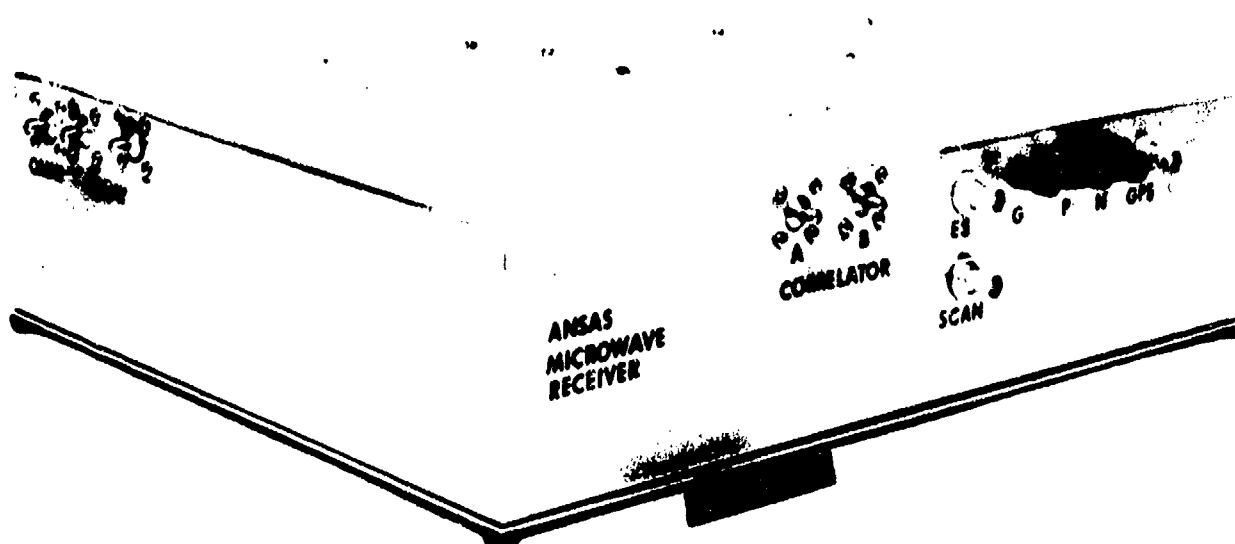


Figure 6. External view of ANSAS microwave receiver
(scale = inches)

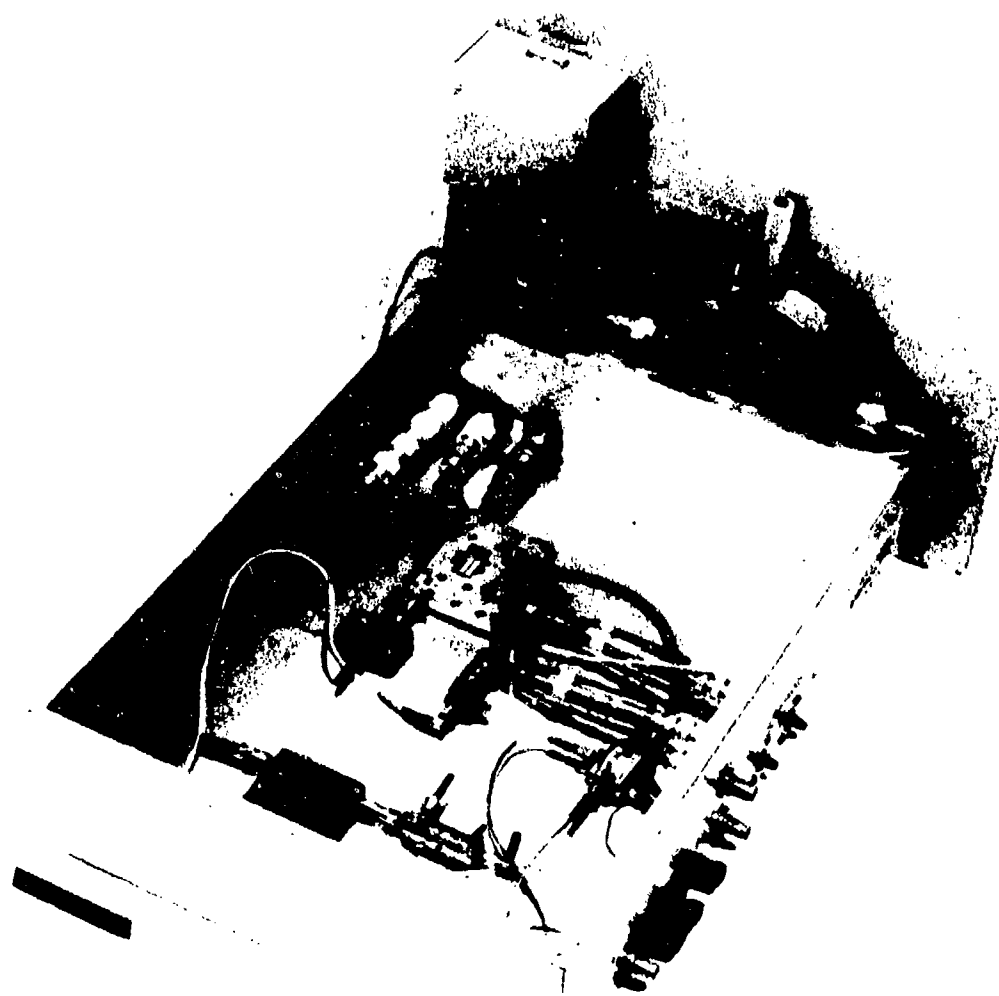


Figure 7. Internal view of ANSAS microwave receiver
(scale = inches)

-10 dB coupler is connected to one of a matched pair of Schottky diode detectors. These square law devices, having an operating range of -50 to +20 dBm, provide the power level readings required by the SNAP system to complete the feedback control mechanism required by ANSAS. (NOTE: These detectors would eventually be replaced by the appropriate signal level detectors existing in the GPS receiver.)

The -3 dB, -180° phase shift hybrid coupler is the heart of the correlator; it is here where the OMNI signal is combined with the weighted phased array signal. By supplying a 180° phase shift, the array signal is essentially inverted. If proper weighting is applied, any signal sensed by the phased array will see an inverted image of itself in the correlator. The result must be a total cancellation of the array's signal at the correlator's output. To determine if the proper weighting is applied, a -10 dB directional coupler is connected to the correlator's output. A sample of the correlator's output signal (the post-correlator signal) is detected by the other half of the matched pair, Schottky diode detectors, and relayed to the SNAP system for processing.

Following assembly of all the components, a constant phase shift was inserted in the phased array channel to equalize the delays in this channel with that of OMNI channel (i.e., "balance" the channels). An RF switch controlled by the SNAP system was also inserted. This enable switch remains closed and prevents the post-correlator signal from entering the GPS user equipment, until nulling has been achieved.

Theoretically it is possible to obtain an infinite cancellation of the interfering signal if the phase and amplitude of the phased array antenna are correctly adjusted. In practice, the null depth is limited by the dispersion of the two channels and the sensitivity of the controlling mechanism.

The microwave receiver measures approximately 33 by 43 by 10 centimeters, weighs 3.1 kg and draws 2 watts power for operation.

7. STEERABLE NULL ARRAY PROCESSOR (SNAP)

SNAP was developed in-house and is the heart of the null steering system. It accepts the sensed power outputs obtained from the correlator system, performs the mathematical operations required by the control algorithms, and outputs "weight" drive signals in real time.

In manual mode, inputs by the operator, through the keyboard, are converted by fixed arithmetic routines to the desired steered "weight" values.

In automatic mode, the algorithms residing in memory determine the weight alterations required to perform the desired nulling and surveillance. The effect of weight alterations on the performance of ANSAS are monitored and evaluated, then optimized via a selected performance criteria, and displayed.

a. SNAP Hardware . The SNAP system hardware, not including the mainframe and power supply, consists of essentially three printed circuit boards. The first board is the microcomputer, consisting of the microprocessor, auxiliary chips necessary for timing and input/output selection, PROM to store permanent programs, a minimal configuration of RAM for temporary data storage and some general purpose input and output interface chips. On a separate board go the

components needed for the specialized functions of the system, namely, the analog to digital converters (A/D), digital to analog converters (D/A), and amplifiers. The last board is an encoded keyboard with display to input commands to the microcomputer and read content of memory. Figures 8 and 9 present the developed SNAP hardware.

b. Microcomputer Hardware. A fixed point limited accuracy computer having an 8-bit microprocessor handles the control requirements of the ANSAS. The INTEL 8080A microprocessor was selected due to its simplicity, speed, and power consumption. It is a complete 8-bit parallel control processing unit (CPU). Relative ease in understanding its operation coupled with its extensive line of interface chips greatly reduced the complexity of the hardware design required.

As seen in the block diagram (Figure 10), the microcomputer is basically divided into three functional sections: the CPU, the memory, and the I/O interfaces. The CPU receives input data through an eight (8) bit bidirectional data bus. This data bus is used not only for receiving data, but also outputting data from the CPU and for addressing memory. Since more than one 8-bit data source exists, a three state bus structure was implemented throughout the design to allow easy selection (enabling/disabling) of the desired input sources. Data was latched using peripheral devices that were three state logic compatible to the bus structure. Using such a bus structure simplifies the wiring on the microcomputer board, and minimizes the number of connectors needed between the microcomputer and the other boards in the SNAP system.

All program storage is in the PROM section of the board. The control program is stored here and is decoded and executed by the processor. System states and temporary values are stored in the RAM section. These values include the A/D inputs and "sorting" tables.

c. SNAP Software. A computer listing of the ANSAS control program is presented in the Appendix. This program was assembled, edited, and debugged using the INTEL MCS-80 software development system and resides entirely in a 1k PROM chip within the microcomputer.

The software was written to perform computational and data manipulation, access input measurements from the microwave receiver and issue respective output commands, generate a self-test on the SNAP I/O board to ascertain if the system is malfunctioning, and interface with the human operator through the built-in SNAP keyboard and display.

The microcomputer program resides primarily in the programmable read-only memory (PROM), since the same program is always executed. Random Access Memory (RAM) is needed for intermediate results calculations (scratch-pad) and temporary storage of tables. A power maximization search technique of processor adjustment was implemented in deriving the proper "weighting" values for the microwave receiver.

The algorithm developed for ANSAS is based on the optimization of the signal-to-jammer (S/J) ratio of the ANSAS output by setting an a priori threshold level initially for the expected GPS signal level.* Once the a priori level is established, it serves as the convergence criteria whose limit the weighing and scanning networks attempt to approach.

*For the laboratory tests, the a-priori threshold for the GPS signal was set at the noise level of the power detectors.

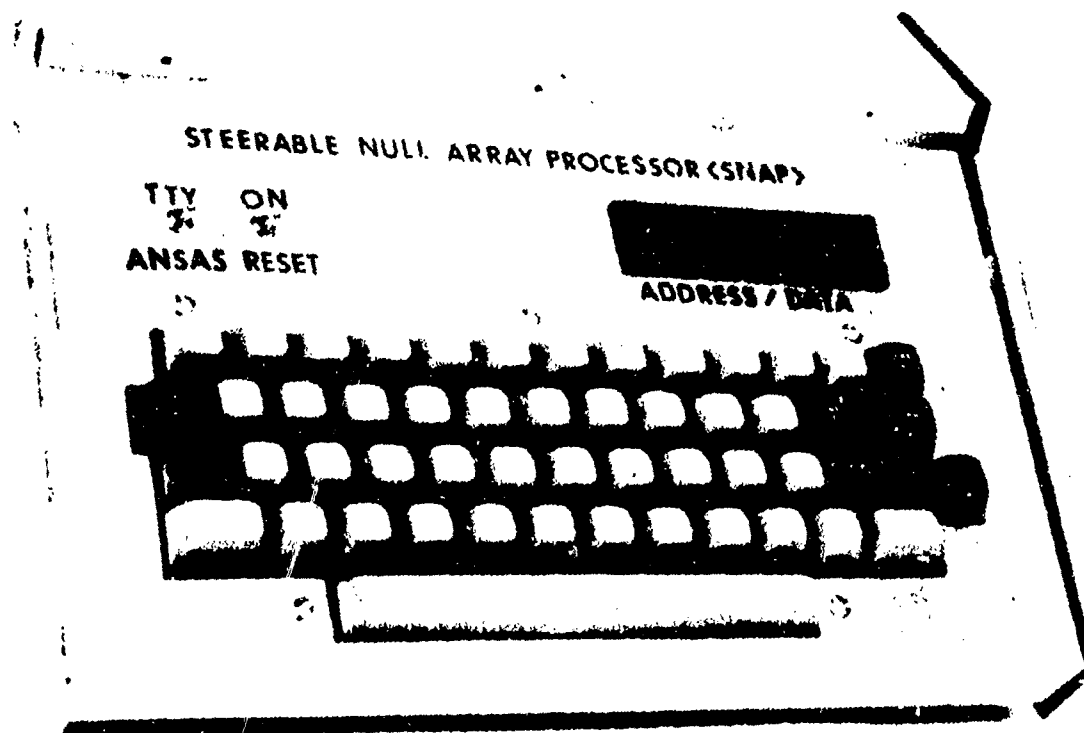


Figure 8. External view of the steerable null array processor (SNAP)

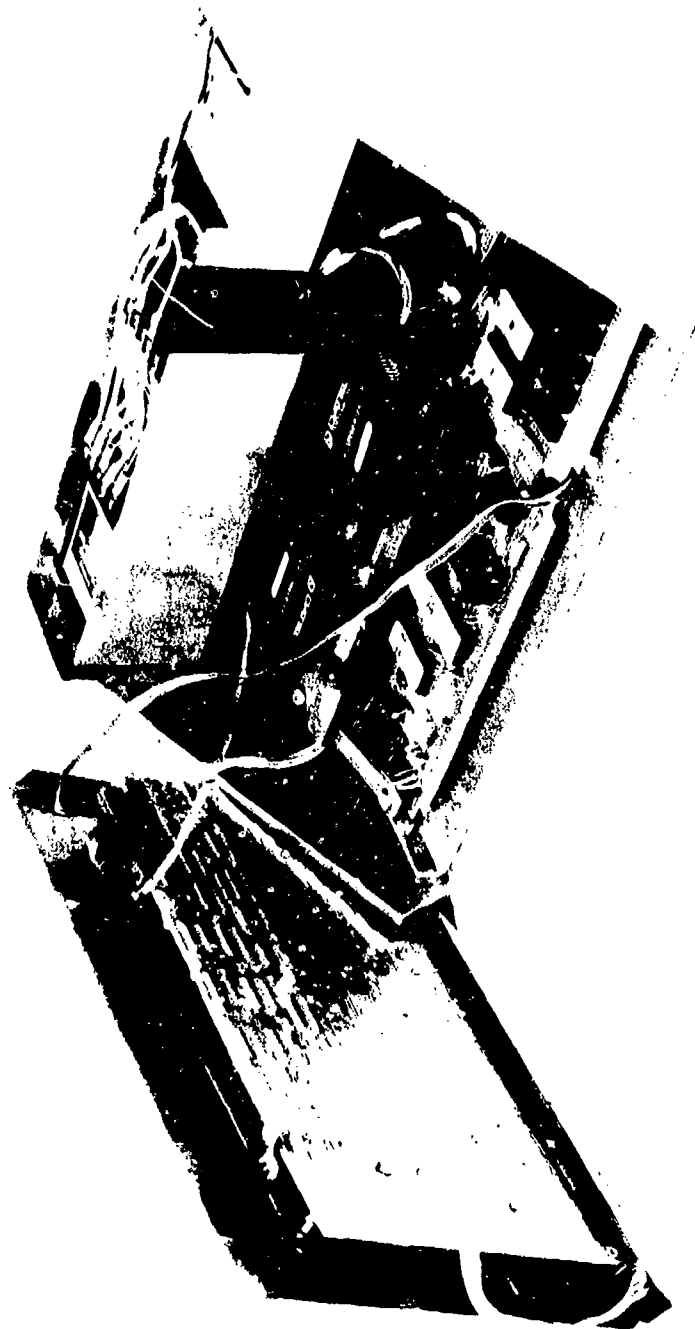


Figure 9. Internal view of the steerable null array processor (SNAP)

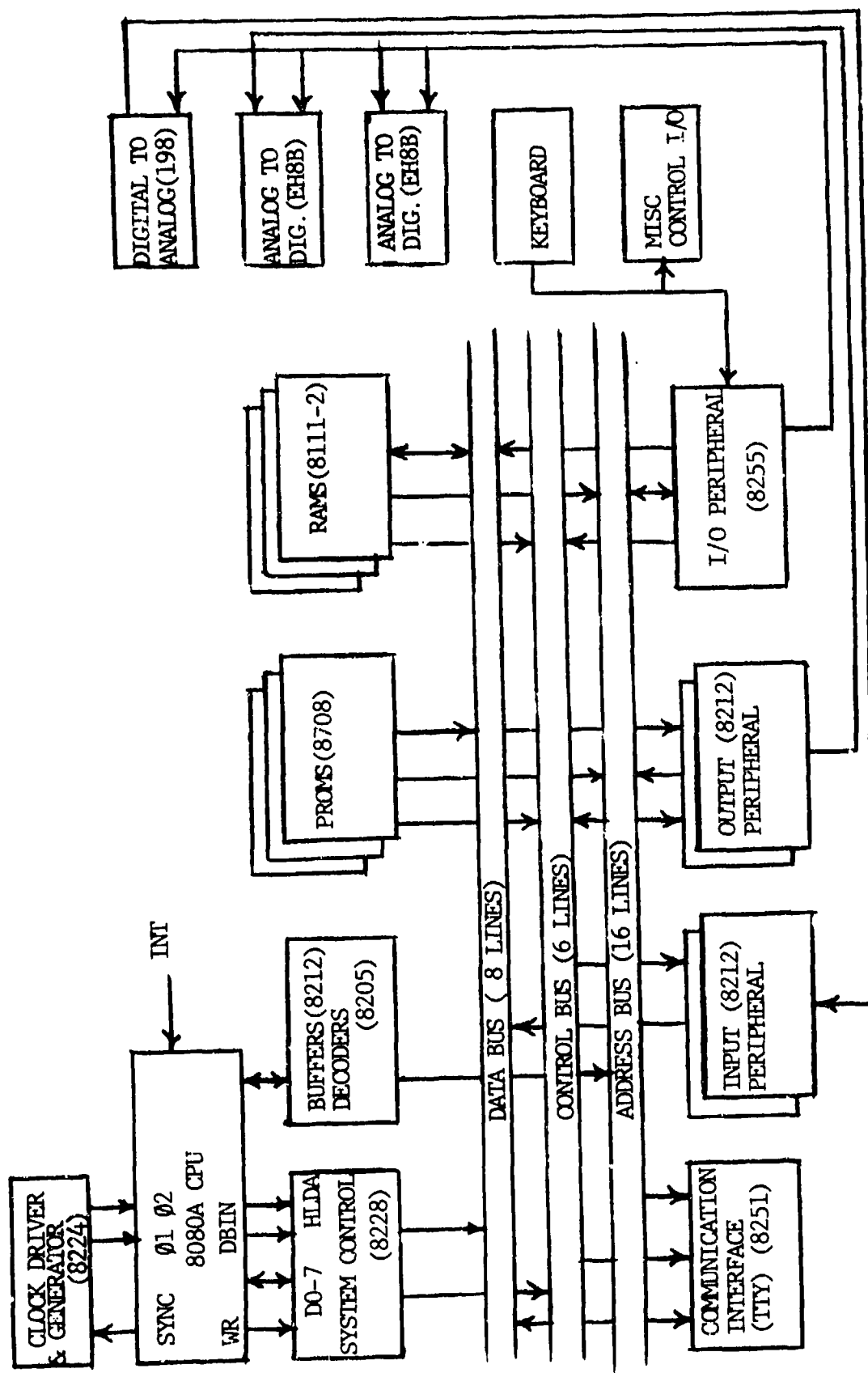


Figure 10. Block diagram of snap system

The search technique initially generates a "sorting" table of measured J/S ratios versus angle of scan of the phased array. If no interference is present, the system continues its survey of the environment. Upon detection of an interference source, the optimum beam orientation is determined. Then it sequences the weighting filter to obtain the setting which most nearly approaches the established convergence criteria thereby representing the desired "null" condition. Based upon a 32 step attenuation, 10-step phase control weighting filter (representing 22° scan capability), the maximum time required to lock in and "null" the interference is ≈ 54.4 msec. After nulling has occurred, the system is capable of monitoring the J/S and, if warranted by an increase in the J/S, steering the beam to "track" the interference thereby maintaining the null.

The SNAP system weighs approximately 3 kg, measures 30.5 by 25.5 by 20 cm and draws 41 watts power.

8. ANSAS LABORATORY TESTS

The ANSAS that was tested is shown in Figure 11, with the OMNI mounted on top of a tripod and the phased array located orthogonal to the OMNI and below it.

The first series of tests revealed the array's surveillance/scanning capability as depicted in the array's azimuthal radiation pattern. Figure 12a-c show that the direction of the center of the beam moved as the electrical phase of the array was automatically scanned from +90° to 0°. The results show a surveillance scan of +22° about the centerline of the array in the azimuthal plane for the array's 16 dB directive beam ($BW_{3\text{ dB}} = 55^\circ$). When the scanning network was placed in the other half of the phase array, the result, as shown in Figure 12 was a surveillance scan of -22° about the centerline of the azimuthal plane as the scan swept from 0° to -90°.

The second series of tests capitalized on the success of the previous tests by combining the steering capabilities of the array with the null-forming characteristics of the correlator system to produce a null-steering configuration. As can be seen in Figure 13a-c, not only can a null be formed in the steering direction, but also "tracked" to counter a dynamic jammer source. Greater than a -20 dB null was maintained throughout the entire scanning range. The -3 dB beamwidth of this null is 95°, the -10 dB beamwidth is 40°.

The elevation pattern for ANSAS throughout this series of tests remained unaffected by the null steering.

Figure 13d shows the depth of the null in the elevation plane. Compared to the GPS omni only elevation pattern shown in Figure 3, this pattern reveals a -24 dB null resulting from ANSAS.

9. CONCLUSIONS

The work described in this report has shown the effectiveness of an automatic null-steering/surveillance array system and its applicability to GPS. This system utilizes a microcomputer controlled, low noise, microwave correlator and phased-scanned array to null a dynamic jammer while retaining most of

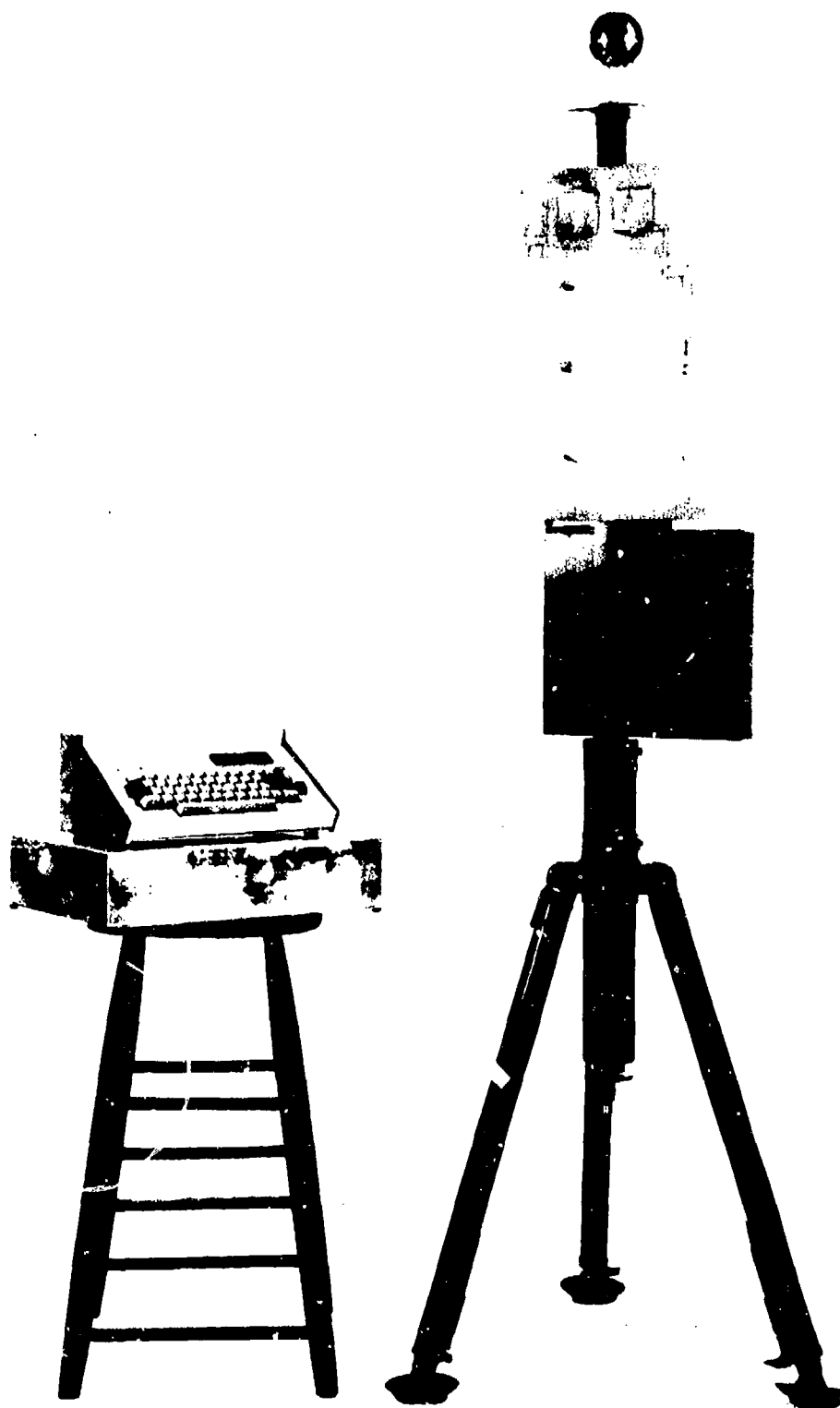


Figure 11. Automatic null steering/surveillance array system (ANSAS)

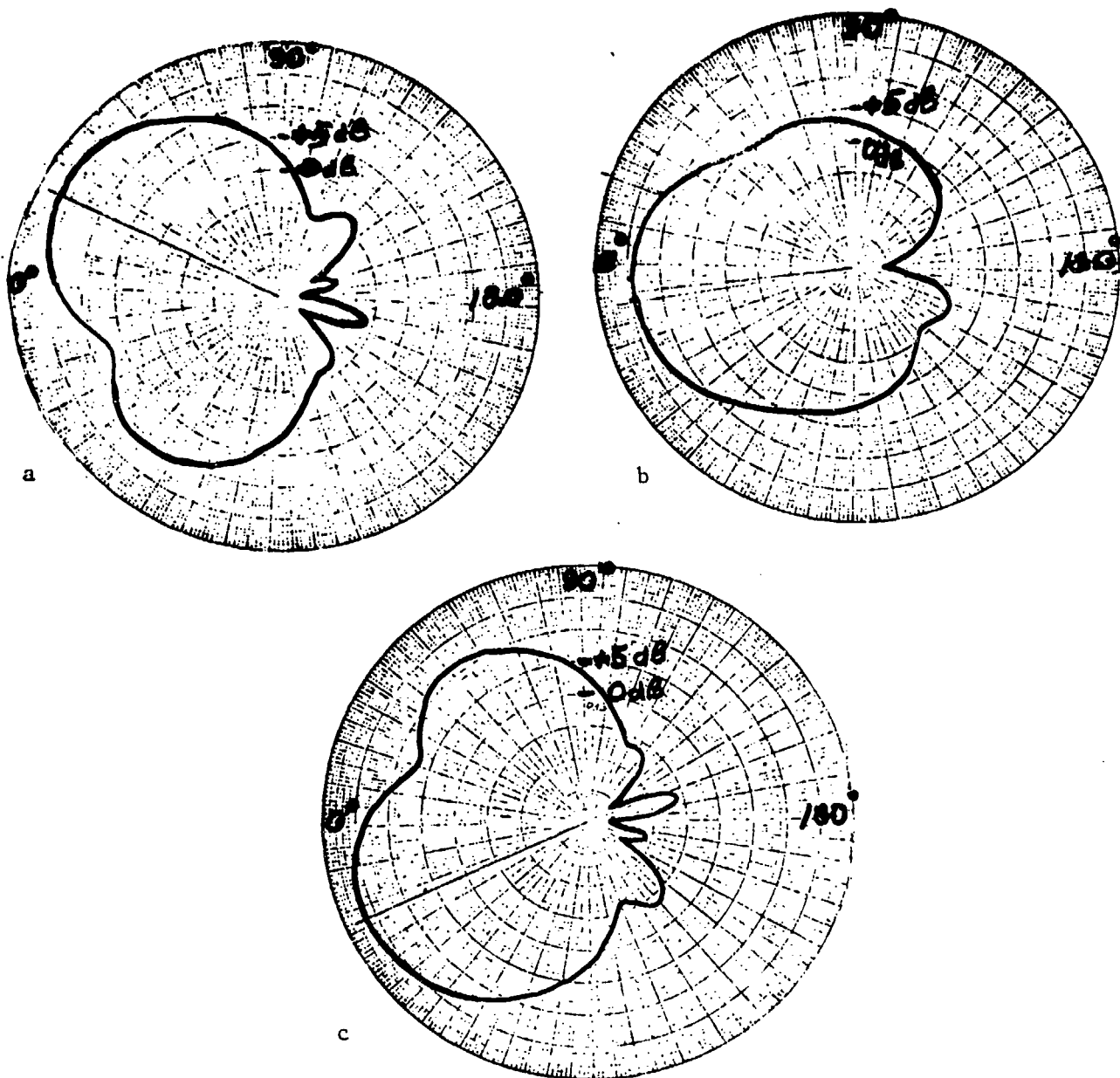


Figure 12. Measured radiation patterns, ANSAS phased array only, 1575-MHz, right-hand circular polarization, azimuthal plane for

- a. phase shift = $+90^\circ$
- b. phase shift = 0°
- c. phase shift = -90°

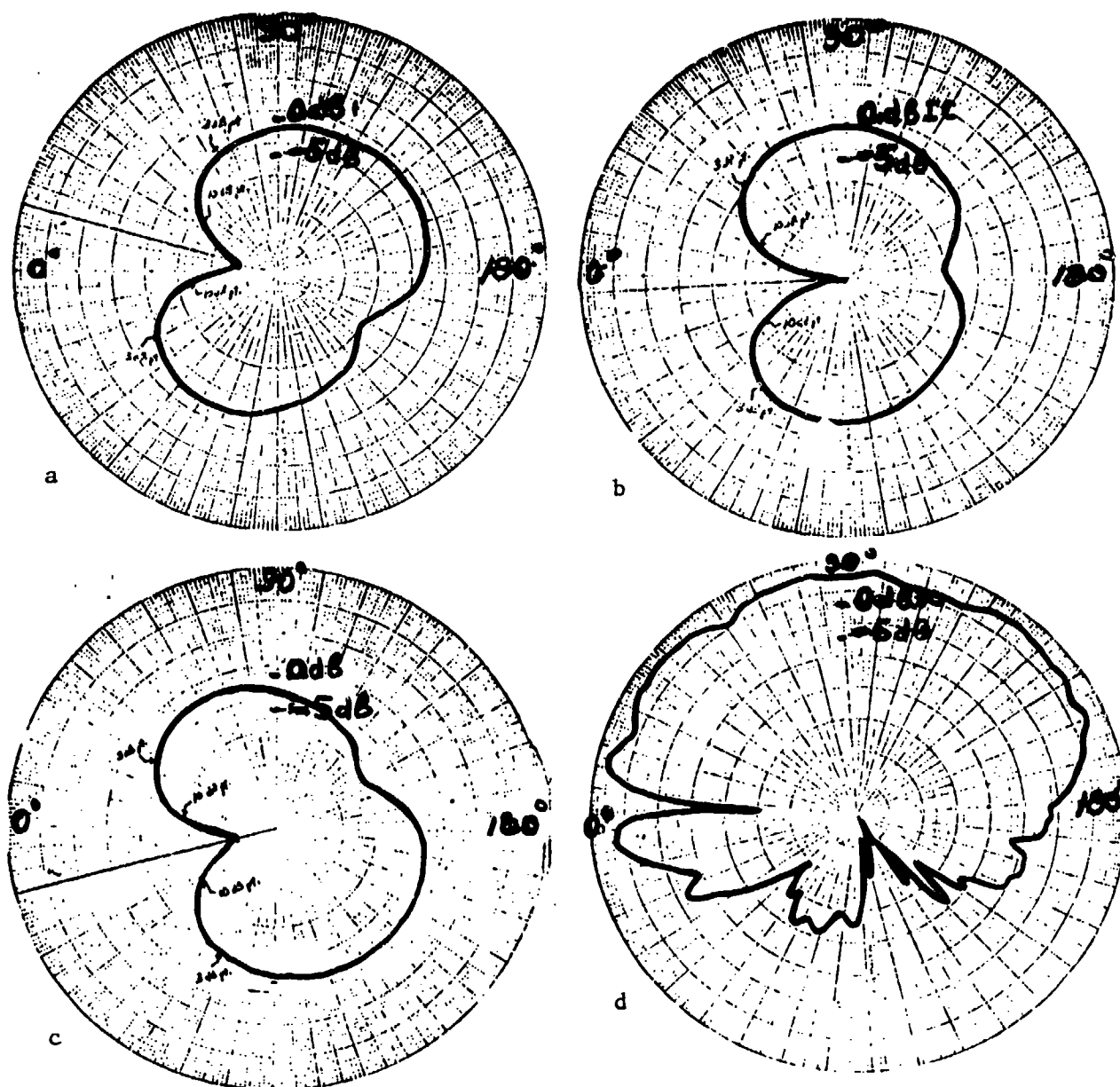


Figure 13. Measured radiation patterns, ANSAS, 1575-MHz, right-hand circular polarization, azimuthal plane for
 a. phase shift = $+90^\circ$
 b. phase shift = 0°
 c. phase shift = -90°
 d. measured radiation pattern, ANSAS, 1575 MHz, right-hand circular polarization, elevation plane

the required GPS elevation and azimuthal coverage. Tests have shown surveillance/null steering scan coverage of $\pm 22^\circ$ off beam centerline while maintaining ≥ 20 dB null depths at -3 dB null beamwidths of 95° .

Insertion loss of ANSAS is ≈ 4 dB and was primarily due to employing a 3 dB, 180° phase shift coupler for the correlator system in the microwave receiver.

ANSAS's operation is based upon the relative jammer signal levels in the omni and array antennas being of equal amplitude and phase for cancellation of the jammer to occur. This equalization of amplitude and phase, in the presence of a dynamic jammer, is achieved automatically through microcomputer controlled correlator and phasing networks. Since ANSAS's performance is not dependent upon absolute signal levels, the successful performance of ANSAS at one signal level would necessarily make it successful for all signal levels.

10. RECOMMENDATIONS

The results from this limited development effort indicate that the objective and technique investigated have great potential for solving the possible jammer threat susceptibility of GPS. The next step in exploiting this potential is to verify its operation with a GPS receiver. The sensors presently used by ANSAS could be replaced by power detectors employed by the GPS receiver, thereby improving the sensitivity of ANSAS to low power jammers.

Insertion loss of ANSAS could be reduced to 2 dB by incorporating a 180° phase shift coupler at the output of the array. Vector summation of the signals can then be achieved in a direction coupler whose directivity matches the array gain (≤ 1 dB loss for a coupling of ≥ 10 dB).

The concept and technique developed in this exploratory development program should be expanded to provide full scan, multi-interference mode capability and implemented into a small, integrated, field deployable unit.

11. ACKNOWLEDGMENT

The authors wish to express their appreciation to Mr. Charles Schelling of the R&D Tech Support Activity for the design of the mechanical support assembly used with the ANSAS.

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APPENDIX. ANSAS COMPUTER PROGRAM

ANSAS REVISION 12 TO A012, EDIT DATE 31 AUG 1978

TTY MONITOR MODE

TTY MONITOR COMMANDS REMAIN AS LISTED IN THE
SYSTEM DEVELOPEMENT HANDBOOK.

TO ENHANCE THE OPERATION OF 'SNAP' FOR FUTURE TESTING
AND DEVELOPEMENT THE FOLLOWING PAPER TAPE CAPABILITIES
ARE INCLUDED FOR USE IN TTY MONITOR MODE ONLY. !. !.

READ PAPER TAPE-PROCEDURE-

1. RESET SYSTEM
2. <R><CR>
3. START PAPER TAPE READER
WHEN READ OPERATION IS COMPLETED
SYSTEM SIGN-ON MESSAGE WILL BE PRINTED...

PUNCH PAPER TAPE-PROCEDURE-

1. RESET SYSTEM
2. <P><PROGRAM NAME><CR>
(PROGRAM NAME MUST BE LESS THEN 16 CHAR'S)
AND MUST NOT INCLUDE A ":", (SEMICOLON)...
3. <START ADDRESS><.><END ADDRESS><CR>
START PUNCH BEFORE DEPRESSING CR, WHEN DATA HAS
BEEN PUNCHED FROM MEMORY THEN THE SYSTEM SIGN-ON
WILL BE PRINTED...

ANSAS MONITOR MODE - COMMAND DISCRPTION

***COMMAND C<CR>

THE CLEAR COMMAND CLEARS ALL IO PORTS AND DOES A
RETURN TO THE COMMAND MODE, SYSTEM RESET.

***COMMAND D(STARTING ADDRESS)<CR>

DUMP THE CONTENTS OF SUCCESSIVE MEMORY
LOCATIONS STARTING AT SPECIFIED ADDRESS. CONTINUE ON EACH
DEPRESSION OF THE SPACE BAR. TERMINATE WITH ESCAPE

***COMMAND E(STARTING ADDRESS)<CR>

ENTER HEX DATA INTO MEMORY AT START ADDRESS
AND CONTINUE UNTIL ESCAPE . .
SEQUENCE IS (DATA)<CR> . CHANGE DATA .
(00)<SPACE> . NO DATA CHANGE.

***COMMAND G(DESTINATION ADDRESS)<CR>

THIS COMMAND DOES A JUMP TO THE MEMORY ADDRESS
GIVEN AS DESTINATION. IF STACK POSITIONING IS MAINTAINED
THEN A NORMAL RETURN CAN BE USED. .

***COMMAND H(1ST HEX VALUE)<CR>(2ND HEX VALUE)<CR>

THIS COMMAND WILL FORM THE SUM OF TWO HEX
FOUR CHARACTER NUMBERS AND INDICATE THIS SUM IN THE
THE DISPLAY WITH A "AA" IN THE LOW DISPLAY. WHEN A

N

SPACE BAR IS ENTERED THE DISPLAY WILL INDICATE THE DIFFERENCE BETWEEN THE TWO HEX NUMBERS WITH BY A "55" IN THE LOW DISPLAY. THE DISPLAY WILL LOCK TO THE SUM OR DIFFERENCE OF THE TWO - FOUR CHAR HEX NUMBER UNTIL THE ESCAPE KEY IS PRESSED.

***COMMAND . O

THIS COMMAND WILL SET THE RF SWITCH CONNECTION FROM A TTL HIGH TO A TTL LOW LEVEL (ON).

***COMMAND . R<CR>

THIS COMMAND WILL INPUT BOTH A & B SIGNAL VALUE TO THEIR RESPECTIVE ANALOG TO DIGITAL CONVERTER AND SET THE PHASE AND THE DB OUTPUT FOR EACH OF 32 DB VALUES AND EACH OF 10 PHASE (0-90 DEGREE) VALUES. THE FINAL OUTPUT WILL BE DISPLAYED AND IN THIS VERSION WAIT FOR A <CR> BEFORE SETTING THE RF SWITCH TO THE ON POSITION. THE TIME REQUIRED TO COMPLETE THE RUN LOOP (32 TIMES 10) MAY BE PRESET BY SETTING THE DELAY VALUE INTO MEMORY LOCATION 'DLY'. THIS SETTING MAY BE FROM 0 TO 0FFFFH. THE NORMAL ANALOG VALUE SAMPLE IS TAKEN AND IS REPRESENTED IN 1 TO 256 PARTS OF THE TRUE VALUE. THUS 1/256TH OF THE INPUT IS REPRESENTED AS 1. THE INITIAL RUN COMMAND WAITS FOR THE INPUT TO BE GREATER THEN (X) PARTS OF THE TOTAL INPUT BEFORE PROCEEDING TO SAMPLE AND SET THE RF SWITCH TO THE ON POSITION. I.E IF THE INPUT VOLTAGE IS ALLOWED TO SWING FROM 0 TO PLUS 5 VOLTS, THEN $[(X)*5]/256$ IS REPRESENTATIVE OF THE VALUE THE INPUT MUST EXCEED BEFORE THE RUN COMMAND WILL CYCLE AND SET THE RF SWITCH-ON

PROVISION IS MADE FOR CONTINUOUSLY MONITORING THE ANALOG INPUTS AFTER THE RF SWITCH IS CLOSED TO PREVENT ANY LOADING OR DEGRADATION OF THE INPUT ONCE THE NULL OR LOWEST VALUE WAS FOUND. THE USER MAY WRITE A PROGRAM AND PLACE IT IN RAM AND PUT THE ENTRY ADDRESS IN LOCATION 'TYPE'. THE PROGRAM MAY CONTAIN CALLS PROVIDING STACK INTEGRITY IS MAINTAINED IF THE USER WISHES TO RETURN TO THE EXIT POINT.

IF 'TYPE' IS USED THEN THE NORMAL RUN WOULD OCCURE AND THE CALL TO USER ROUTINE WOULD RESULT. IF 'TYPE' IS NOT USED THEN A NORMAL RETURN OCCURS WHILE WAITING FOR AN ESCAPE FROM 'RUN' MODE.

THE RUN COMMAND MAY BE TERMINATED ANY TIME WITH AN ESCAPE KEY.

***COMMAND . T(VALUE)<CR>

N

THIS COMMAND WILL ENABLE THE INTERNAL TIME DELAY
WHOSE PERIOD WILL BE DETERMINED BY THE VALUE 0 TO FFFF
IN HEXADECIMAL, (0 TO 65,000).

***COMMAND. Z<CR>

THIS COMMAND WILL WRITE ZEROES INTO ALL
OF RAM MEMORY AND DO A SYSTEM RESET.

NUMERICAL COMMAND LIST...

1. THIS IS THE STEP TEST MODE. THIS ENABLES AN INPUT
SAMPLE TO BE TAKEN ONCE AND THE OUTPUT SET ACCORDING
TO THIS SINGLE SAMPLE...
2. THIS ENABLES THE VALUE ENTERED TO BE SUBSTITUTED
FOR WHAT WAS RECEIVED IN ANALOG PORT A.
THE VALUE IS HANDLED AS IF IT WERE RECEIVED,
THE OUTPUT IS SET ACCORDINGLY.
3. THIS IS THE SAME AS TEST 2, EXCEPT SUBSTITUTION
OCCURES WITH ANALOG PORT B DATA.
4. THIS TEST ALLOWS THE DAC OUTPUT TO PRODUCE A RAMP.
5. THIS TEST ALLOWS THE LATCH OUTPUT TO PRODUCE A
BINARY VALUE SEQUENCING FROM 0 THROUGH 31.
6. THIS TEST COMBINES TEST 4 AND 5 ABOVE...
7. THIS TEST RESETS THE PHASE ATTENUATION POINTER
VALUE TO THAT WHICH IS INTERNAL. THIS TABLE
POINTER IS LOCATED IN 'TABLE' IN RAM MEMORY
AND MAY BE ALTERED TO INDICATE WHERE THE USER
TABLE IS LOCATED.
THE USER TABLE ADDRESS SHOULD BE ENTERED INTO
ADDRESS TABLE LOW BYTE AND TABLE+1 HIGH BYTE.
9. THIS ROUTINE WILL DISABLE INTERNAL TIMER
AND CLEAR THE SYSTEM FOR FURTHER USE.
0. THIS WILL SET THE RF SWITCH CONNECTION
FROM AN TTL LOW TO A TTL HIGH LEVEL (OFF).

* * * * *
THE USER MUST ASSURE PROPER VALUES ARE INSERTED INTO
THE FOLLOWING LOCATIONS.

- DIFF -THE DESIRED VALUE ANALOG-B INPUT SHOULD ATTAIN
(13C0) BEFORE PROCESSING CAN OCCURE. DIFF IS INITIALIZED
TO ZERO (0), AND MAY BE SET FROM 0 TO 255.
- DLY -REPRESENTS THE DELAY BETWEEN ANALOG SAMPLE PERIODS
(13C1) AND IS INITIALIZED TO ZERO (0). THE PERIOD MAY
BE SET FROM 0 TO 65,000 TIMES () MICROSECONDS.
- TYPE -TYPE RUN IS PRESET TO SAMPLE 320 TIMES, WHICH
(13C6) CORRESPONDS TO 32 DB STEPS, TIMES 10 PHASE STEPS.
THE OUTPUT IS SEQUENCED AFTER EACH SAMPLE. THE
LOWEST INPUT VALUE SAMPLED IS THEN USED TO ACCESS
A TABLE AND THE FINAL OUTPUT IS SET
THE RF SWITCH IS THEN TURNED ON AND PROCESSING
IS TERMINATED.
THE USER MAY WRITE THEIR OWN ROUTINE TO CONTINUE

N

SAMPLING OR PROCESSING SIMPLY BY INSERTING A JUMP
TO USER ROUTINE IN LOCATION 'TYPEX'.

TABLE -THIS LOCATION CONTAINS THE ADDRESS OF THE TABLE
(13C9) THAT IS TO BE USED DURING 'RUN' OR 'STEP' SEQUENCE.
SEQUENCES. IF DESIRED THE USER SHOULD INSERT
THE ADDRESS OF HIS 'TABLE' IN LOCATION TABLE.

* * * * *

COMMAND	FORMAT	FUNCTION
C	C<CR>	CLEAR SYSTEM AND I/O PORTS
D	D(ADRS)	DUMP HEX DATA FROM MEMORY
E	E(ADRS)<CR>	ENTER HEX DATA TO MEMORY
G	G(ADRS)<CR>	GO, DO ROUTINE AT ADRS GIVEN
H	H(VALUE)<CR>(VALUE)<CR>	DISPLAY HEX SUM/DIFFERENCE
O	O	TURN-ON RF SWITCH CONNECTION
R	R<CR>	RUN ANSAS PROGRAM
T	T(VALUE)<CR>	ENABLE AND SET DELAY PERIOD
Z	Z<CR>	ZERO RAM MEMORY AND RESET.
1	1<CR>	STEP (RUN) MODE
2	2(VAL-A)<CR>	SUBSTITUTE VALUE FOR ANAL A
3	3(VAL-B)<CR>	SUBSTITUTE VALUE FOR ANAL B
4	4<CR>	INCREMENTAL VALUES-PHASE
5	5<CR>	INCREMENTAL VALUES-ATTEN
6	6<CR>	INCR VALUE OF PHASE & ATTEN
7	7<CR>	SET PATT TABLE POINTER
9	9<CR>	DISABLE TIMER
0	0	TURN-OFF RF SWITCH

ERROR NUMBER EQUATES

01 COMMAND ERROR ESCAPE AND RE-ENTER COMMAND
02 FORMAT ERROR, (CORRECT COMMAND FORMAT)
03 DATA KEY DEPRESSED (NON-HEX PRESS CORRECT KEY)
(XX) ASCII VALUE OF KEY PRESSED, (PRESS ESCAPE)

SYSTEM MEMORY ASSIGNMENT

(IN TTY - MODE)
8708--EPROM 0000-03FF SDK MONITOR
(IN ANSAS - MODE)
8708--EPROM 0000-03FF GPS MONITOR
8111A-RAM 1300-13FF *GPS USER SUPPORT
8111A-RAM 1200-12FF " " "
8111A-RAM 1100-11FF " " "

USER MEMORY CHANGES BEYOND 13C0H MAY REQUIRE
USER TO RESET DUE TO STACK/DATA MODIFICATION.

SYSTEM EQUATES

CWDS EQU 00 ; PORT B CLR, RESET PC0 (DUAL)
CWLS EQU 01 ; SET PC0
TRDY EQU 01 ; ANAL OR TTY RDY FOR PRINT

N

```

RBR      EQU      02      ; TTY RDR BUF RDY
OFST      EQU      03      ; TABLE OFFSET
OFRF      EQU      04      ; TURN-OFF RFSW
ONRF      EQU      05      ; TURN-ON RFSW
EINT      EQU      09      ; ENABLE KBD INT, SET PC4 (DUAL)
CR        EQU      0DH      ; CA-RAHJ RETURN
HI        EQU      10H      ; BLANK-4, NOT
CWDR      EQU      11H      ; ON HI-LO DISPLAY
ESC       EQU      1BH      ; ESCAPE KEY
SPC       EQU      20H      ; SPACE KEY
CKBS      EQU      20H      ; KBD STATUS MASK (PC5)
PMAS      EQU      7FH      ; PARITY MASK
ICWM      EQU      0B0H      ; INITIAL CMD WORD (MODE-1/MODE-0)
KBD       EQU      0F4H      ; KEYBOARD DATA
PORTB     EQU      0F5H      ; PORTB DATA OUTPUT
KBDS      EQU      0F6H      ; KBD STATUS PORT
CONT      EQU      0F7H      ; MODE SELECT AND CONTROL
CNVEN     EQU      01DAH      ; FOR BINARY CONVERSION
CO        EQU      01E3H      ; TTY CONSOLE OUT
CROUT     EQU      01EEH      ; CR OUTPUT
ECHO      EQU      01F4H      ; COPY CHARAT
GETCH     EQU      021BH      ; GET TTY CHAR
GETHX     EQU      0222H      ; GET HEX CHAR
HILO      EQU      029CH      ; IS HI < LO ?
NMOUT     EQU      02C3H      ; NUM OUT
BUFS      EQU      139FH      ; DATA BUFFER
RUFT      EQU      13A0H      ; HOLD BUFFER
STAK      EQU      13AEH      ; POINTER VALUE
DIFF      EQU      13C0H      ; DESIRED INPUT OFFSET
DLY       EQU      13C1H      ; DESIRED DELAY FOR SAMPLE
TIMEX     EQU      13C3H      ; INTERNAL TIMER
TYPEX     EQU      13C6H      ; TYPE RUN DESIRED
TABLE     EQU      13C9H      ; TABLE FOR TEST/RUN
LO32      EQU      13CCH      ; 32 CYCLE TEMP STORE
LO10      EQU      13CDH      ; 10 CYCLE TEMP STORE
ADCA      EQU      0FF00H      ; ANAL PORT A
ADCB      EQU      0FF01H      ; ANAL PORT B
DAC       EQU      0FF02H      ; DAC OUTPUT PORT
DBS       EQU      0FF03H      ; DB (0-32) OUTPUT
SADC      EQU      0FF10H      ; STROBE ADC, START CONVERSION
ALE       EQU      0FF11H      ; LOW DISPLAY-A
BLE       EQU      0FF12H      ; MIDDLE DISPLAY-B
CLE       EQU      0FF13H      ; HIGH DISPLAY-C

```

; INITIALIZATION ROUTINE

```

      ORG 00
ZERO:  MVI A, ICWM
      OUT CONT
      MVI A, EINT
OHH:   OUT CONT

```

; ROUTINE TO FETCH A COMMAND FROM THE KEYBOARD

```

INIT:  LXI SP, STAK      ; LIST WHERE WE ARE.
      LXI H, CTAB        ; WHERE WE'RE GOING

```

N

```
TST:    LXI D,OFST      ;SOMETIME REQUIRED OFFSET
        MVI B,PMAS      ;TABLE DIVIDER
        CALL KBDR       ;GET KEYBOARD DATA
        MOV C,A         ;TEMPORARY HOLD AREA.
CNXT:    MOV A,M         ;GET IT
        CMP C           ;CHECK IT
        JZ FND          ;GOT IT
        CMP B           ;IS THIS JUNK ENDED YET?
        JZ GOOF         ;IT'S ILLEGAL!
        DAD D           ;GO FA ROTHER.
        JMP CNXT        ;CHK ANOTHER
```

```
FND:    CALL ONDS      ;WHERE WERE GUNG
        INX H           ;GET LOW
        MOV E,M
        INX H           ;GET HIGH
        MOV D,M
        PUSH D          ;GET BENT
        RET             ;GO
```

```
ERR:    PUSH H          ;SAVE H IF NEEDED
        LXI H,0B00BH    ;A REGISTER IS ERR #
        CALL DSPE       ;SHOW-IT
        POP H           ;RESTORE CONDITION
        RET
```

```
GOOF:    MVI A,CWLS     ;COMMAND WORD LOSS (ERR)
        CALL ERR
        JMP INIT
```

```
ONDS:    MVI A,CWDR
        OUT PORTB
        JMP DSPE
```

ROUTINE TO DISPLAY A REG AND HL

```
DSP:    XRA A           ;ZERO ACCUMULATOR
DSPE:    STA ALE         ;SHOW A IN LOW
        SHLD BLE        ;SHOW HL IN UPPER
        RET
```

ROUTINE TO INPUT FROM KEYBOARD, DATA IN A REGISTER

```
KBDR:    IN KBDS        ;CHECK INT STATUS
        ANI CKBS        ;STATUS MAS'
        JZ KBDR         ;WAIT
KBDD:    IN KBD         ;GET DATA
        ANI PMAS        ;MASK OFF PARITY
        CFI ESC
        JZ INIT
        RET
```

ROUTINE TO DISPLAY HEX DATA FROM MEMORY IN DISPLAY

```
DUMP:    CALL ADRS
MOR:     MOV A,M
        CALL DSPE
```

N

```
CALL RETWT
INX H          ; MODIFY DATA WINDOW
JMP MOR       ; LOOP- IT
```

; ROUTINE TO ENTER HEX DATA FROM KEYBOARD TO MEMORY

```
ENTER: CALL ADRS
      CALL RETWT
LOOP:  MOV A, M
      CALL DSPE
      CALL HEXE
CAK:   CALL DSPE
      MOV B, A
      CALL RETWT
      CPI SPC
      JZ MDIF
      CPI CR
      JNZ CAK
      MOV M, B
MDIF:  INX H
      JMP LOOP
```

; ROUTINE TO FETCH 4 HEX CHAR FOR MEMORY ADDRESS IN HL REG

```
ADRS:  CALL HEXE
      MOV H, A
      CALL HEXE
      MOV L, A
      RET
```

; ROUTINE TO FETCH 2 HEX CHARS IN A REG

```
HEXE:  CALL NYBE
      RRC
      RRC
      RRC
      RRC
      MOV B, A
      CALL NYBE
      ORA B
      RET
```

; ROUTINE TO FETCH 1 HEX CHAR IN A REG

```
NYBE:  CALL KBDR
      SUI 30H
      JC ESET          ; IT WAS LESS THAN ZERO
      ADI 0E9H
      JC ESET
      ADI 06
      JP ALP
      ADI 07
      JC ESET
ALP:   ADI 0AH
      RET
ESET:  MVI A, OFST      ; OFFSET FOR NON HEX CHAR
      CALL ERR
      JMP NYBE         ; GO BACK FOR NEW ONE
```

N

; ROUTINE TO DISPLAY AND GO TO USER ADDRESS

GO: MVI A, CWLS
OUT PORTB
CALL ADRS ; GET THE ADDRESS
CALL RETWT
PUSH H
JMP DSP ; ONLY RET IS RESET

; ROUTINE TO CALCULATE HEX SUM/DIFF TWO 4-HEX CHAR #.

; AA DISP INDICATES HL REG CONTAINS SUM OF #'S
; 55 DISP INDICATES HL REG CONTAINS DIFF OF #'S

ARITH: MVI A, CWLS
OUT PORTB
CALL ADRS ; 1ST #
CALL DSPE
CALL RETWT
XCHG
CALL ADRS ; 2ND #
CALL DSPE
CALL RETWT
CALL ONDS
PUSH H ; SAVE COPY
DAD D
XTHL ; SWAP SUM WITH COPY
MOV A, L
SUB E
MOV L, A
MOV A, H
SBB D
MOV H, A ; HL=DIFF
POP D ; DE=SUM
MVI B, 55H
SHON: MOV A, B
XCHG
CMA ; AA=ADD/55=SUB
MOV B, A
CALL DSPE
WAIT1: CALL KBDR
CPI SPC ; SPACE - SHOW MORE
JZ SHON
JMP WAIT1 ; WAIT FOR CHAR KEY

; ROUTINE TO FETCH ANALOG TO DIGITAL DATA

INADC: STA SADC
NOP
LHLD ADCA
RET

; TURN ON ANAOUT CONTROL

ONANA: MVI A, TRDY
OUT CONT
RET

N

TURN ON RF SWITCH

OH: MVI A, ONRF
JMP OHH

CLRO: LXI H, 0000
CALL RETWT
CALL DSP
SHLD DIFF
SHLD DAC

NINE: MVI A, 0C9H
STA TYPEX
STA TIMEX
JMP ZERO

OFSW: MVI A, OFRF
JMP OHH

RUN: LXI H, 0000
SHLD DAC
LDA DIFF
MOV B, A ; B=OFFSET
XCHG
CALL ONANA ; WITH DE=00
CALL TYPEX ; 1ST USER RETURN

WAIT2: MOV A, B
CALL INADC
CMP H
JC RUNO ; ADCB>OFFSET
CALL KSI ; IF ESCAPE ?
JMP WAIT2 ; IF NOT LOOP

RUNO: MOV C, L ; ADCA=L
MOV B, H ; ADCB=H

RUN1: CALL TIMEX ; DELAY ?
CALL INADC
SHLD BLE
MOV A, L
CMP C ; OLD 1 OF 32
JNC RUN2 ; 2ND>1ST
MOV C, L ; 2ND<1ST SAVE
MOV A, E
STA LO32 ; ??

RUN2: MOV A, H
CMP B ; OLD 1 OF 10
JNC RUN3 ; 2ND>1ST
MOV B, H ; 2ND<1ST SAVE
MOV A, D
STA LO10

RUN3: XCHG ; VAL->DE, CNT->HL
MOV A, L

N

```

        CPI 0F8H
        JZ YES
        ADI 8
        MOV L, A
        JMP RUN4
;
YES:     MVI L, 00
        MOV A, H
        CPI 0F0H
        JZ YESX
        ADI 18H
        MOV H, A
        JMP RUN4
YESX:    LHLD L032
        CALL TYPEX      ; LAST USER CHANCE
        CALL DOIT
        JMP OH
;
RUN4:    CALL DOIT
        XCHG
        JMP RUN1
;
TIME:    CALL ADRS
        CALL DSP
        CALL RETWT
        SHLD DLY
        MVI A, 0C3H
        STA TIMEX
        LXI H, TIME0
        SHLD TIMEX+1
        JMP INIT
;
ZERO:    LXI H, 0
        MVI A, 14H
        MOV B, L
RND:     MOV M, B
        INX H
        CMP H
        JNZ RND
        JMP ZERO
;
; TABLE ACTIVATOR, ONE SAMPLE-SET
SETIT:   CALL ONANA
        CALL INADC
DOIT:    MOV A, L
        ANI 0F8H
        RRC
        RRC
        RRC
        MOV E, A
        MOV A, H
        LXI H, TABLE      ; PATT
        MVI C, 0BH         ; FOR TEN LOOPS
LUPP:    DCR C

```

N

```

        JZ DOND
        CMP M
        JNC NXTT          ; AD=M
        INX H              ; AC=M
        INX H
        JMP LUPP
NXTT:   DCX H              ; ONCE TO MANY
        JMP DOND
DOND:   INX H              ; >TABLE
DOND:   MOV D, M           ; FETCH PHASE
        XCHG
        CALL DSPE
        SHLD DAC
        RET

```

; ROUTINE TO SAMPLE ONE TIME AND SET OUTPUT

```

ONE:    CALL SETIT
        JMP INIT

```

; ROUTINE TO SUBSTITUTE KEYBOARD VALUE FOR ANAL A VALUE

```

TWO:    CALL INADC         ; FETCH ACTUAL VALUES FOR A & B
        CALL HEXE
        MOV L, A           ; KEYBOARD VALUE SUBSTITUTED
        PUSH H
        LXI H, 0ADCAH     ; GET DUMMY
        JMP SHIN          ; SHOW INPUT VALUE

```

; ROUTINE TO SUBSTITUTE KEYBOARD VALUE FOR ANAL B VALUE

```

THREE:  CALL INADC
        CALL HEXE
        MOV H, A
        PUSH H
        LXI H, 0ADCBH

```

```

SHIN:   CALL DSPE
        CALL RETWT
        POP H
        CALL DOIT
        JMP INIT

```

; INCREMENT DAC VALUE (PHASE INCREASES)

```

FOUR:   LXI H, 0DAC0H
MR1:    CALL ADRG
        STA DAC
        JMP MR1

```

; INCREMENT DB VALUE (0 TO 31)

```

FIVE:   LXI H, 0DB31H
MR2:    CALL ADRG
        STA DBS
        JMP MR2

```

; INCREMENT DAC AND DB VALUE

```

SIX:    MVI A, 0ABH

```

N

MR3: SHLD DAC
CALL KSTAT
INR H
INR L
JMP SIX

; ROUTINE TO SET INTERNAL PHASE POINTER

SEVEN: LXI H, PATT
SHLD TABLE
JMP INIT

ADRG: CALL KSTAT
INR B
MOV A, B
RET

; WAIT FOR CARRIAGE RETURN (CR)...

RETWT: CALL KBDR
CPI CR
RZ
CPI SPC
RZ
MVI A, RBR
CALL ERR
JMP RETWT

; WAIT-NOT FOR KEYBOARD STATUS

KSTAT: CALL DSPE
KSI: IN KBDS
ANI CKBS
JZ TIMEX ; CHECK TIMER
JMP KBDD

TIMEO: PUSH H
LHLD DLY
LAPSE: MOV A, L
ORA H
JZ DONE
DCX H
JMP LAPSE
DONE: POP H
RET

; ROUTINE TO RUIN PERFECTLY GOOD PAPER TAPE
; BY PUNCHING INTEL FORMAT HOLES IN IT...

ORG \$+400H
PUNCH: LXI H, BUFS ; GET HEADER INFO
HEO: CALL GET
MOV M, A
CPI CR
JNZ HEO
CALL GETHX ; GET DATA ADRS
MOV H, B

```

N
    MOV L, C
    CALL GETHX
    MOV D, B
    MOV E, C
    CALL LEAD      ; PUNCH LEADER HOLES
    PUSH H
    LXI H, BUFT
    CALL CROUT
HO:  MOV C, M      ; SHOW NAME
    CALL GET2
    CPI CR
    JNZ HO
    POP H
PO:  MVI C, 3AH
    CALL CO
    LXI B, HI
    PUSH H
P1:  INR B
    DCR C
    JZ P2
    CALL HILO
    INX H
    JNC P1
P2:  POP H
    PUSH D
    MVI D, CWDS
    MOV A, B
    CALL POUT
    MOV A, H
    CALL POUT
    MOV A, L
    CALL POUT
    XRA A
    CALL POUT
P3:  MOV A, M
    CALL POUT
    INX H
    DCR B
    JNZ P3
    XRA A
    SUB D
    CALL POUT
    POP D
    CALL CROUT
    DCX H
    CALL HILO
    INX H
    JNC P0
    MVI C, 3AH
    CALL CO
    MVI H, ONRF
P4:  XRA A
    CALL POUT
    DCR H

```

N

JNZ P4
CALL LEAD
RST CWLS

ROUTINE TO OUTPUT TAPE LEADER

LEAD: MVI B, 40H
LEO: MVI C, CWDS
CALL CO
DCR B
JNZ LEO
RET

ROUTINE TO GET AND ECHO CHAR

GET: CALL GETCH
GET2: CALL ECHO
MOV A, C
INX H
RET

ROUTINE TO OUTPUT 2 ASCII CHAR'S

POUT: PUSH B
MOV C, A
ADD D
MOV D, A
MOV A, C
CALL NMOUT
POP B
RET

ROUTINE TO READ THE INTEL
FORMATTED TAPE YOU PUNCHED.

READ: CALL GETCH
CPI CWDS
JZ READ

CPI 3AH
JZ STLNE
CALL ECHO
JMP READ

ROUTINE TO PACK SARDINES IN A CAN

BYTE: CALL GETCH
CALL CNVEN
ADD A
ADD A
ADD A
ADD A
MOV B, A
CALL GETCH
CALL CNVEN
ADD B
MOV B, A
ADD D
MOV D, A
MOV A, B

N

RET

; ROUTINE TO STORE DATA LINE AS RECEIVED

STLINE: MVI D, CWDS
CALL BYTE

ANA A

JNZ STLO

RST CWLS

STLO: MOV E, A

CALL BYTE

MOV H, A

MOV C, A

CALL NMOUT

CALL BYTE

MOV L, A

MOV C, A

CALL NMOUT

CALL BYTE

; HERE, WE GO, LOOP-D-LOOP

LOOP: CALL BYTE

MOV M, A

INX H

DCR E

JNZ LOOP

; ROUTINE TO PICK-UP LAST AND

; CHECK INTEGRITY OF ALL. . . .

CALL BYTE

XRA A

ADD D

JNZ ERROR

CALL OK

JMP READ

; ROUTINE TO SHOW ERROR CONDITION

ERROR: MVI C, SPC

CALL ECHO

MVI C, 2AH

CALL ECHO

JMP READ

OK: MVI C, SPC

CALL ECHO

MVI C, 4FH

CALL ECHO

MVI C, 4BH

CALL ECHO

RET

ORG \$-400H

LIST

; 039D	0D	0A	41	4E
; 03A1	31	31	0D	0A
; 03A5	0000	CADR:	DW	0000
; 03A7	4101		DW	XCMD
; 03A9	1D01		DW	SCMD

N

03AB	2D07	DW	RCMD
03AD	8E06	DW	PCMD
03AF	FD00	DW	MCMD
03B1	B300	DW	ICMD
03B3	9500	DW	GCMD
03B5	5E00	DW	DCMD
0020	0608	LSGNON	
0042	010800	NCMDS=8	
0045	21B703	CTAB	
0054	21A503	CADR	
03F7	54		

ANSAS COMMAND LIST

CTAB:	DB	'C'	; CLEAR I/O PORTS AND SYSTEM
	DW	CLRO	
	DB	'D'	; DUMP HEX MEMORY
	DW	DUMP	
	DB	'E'	; ENTER HEX DATA TO MEMORY
	DW	ENTER	
	DB	'G'	; GO, EXECUTE ROUTINE
	DW	GO	
	DB	'H'	; HEX SUM/DIFFERENCE
	DW	ARITH	
	DB	'O'	; RF SWITCH ON
	DW	OH	
	DB	'R'	; THE RUNNER
	DW	RUN	
	DB	'T'	; ENABLE TIME DELAY
	DW	TIME	
	DB	'Z'	; ZERO MEMORY/RESET
	DW	ZERO	
	DB	31H	; STEP RUN MODE
	DW	ONE	
	DB	32H	; SUBST VALUE FOR (A)
	DW	TWO	
	DB	33H	; SUBST VALUE FOR (B)
	DW	THREE	
	DB	34H	; STEP PHASE
	DW	FOUR	
	DB	35H	; STEP ATTN
	DW	FIVE	
	DB	36H	; STEP PHASE AND ATTN
	DW	SIX	
	DB	37H	; SET PATT TABLE POINTER
	DW	SEVEN	
	DB	39H	; DISABLE TIMER, CLEAR I/O
	DW	NINE	
	DB	30H	; TURN OFF RFSW
	DW	OFSW	
	DB	07FH	

PHASE TABLE APPROX FOR 10 STEP, 0 TO 90 DEGREES

PATT: DW 0000H

N

DW	0A18H
DW	1430H
DW	1E48H
DW	2860H
DW	3278H
DW	3C90H
DW	46A8H
DW	50C0H
DW	5AD8H
DW	0FFF0H
DW	'0A'
DB	'12'
END	

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