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COMPARISON STUDY OF THE FIVE TRANSISTOR-TRANSISTOR-LOGIC (TTL) --ETC(U)

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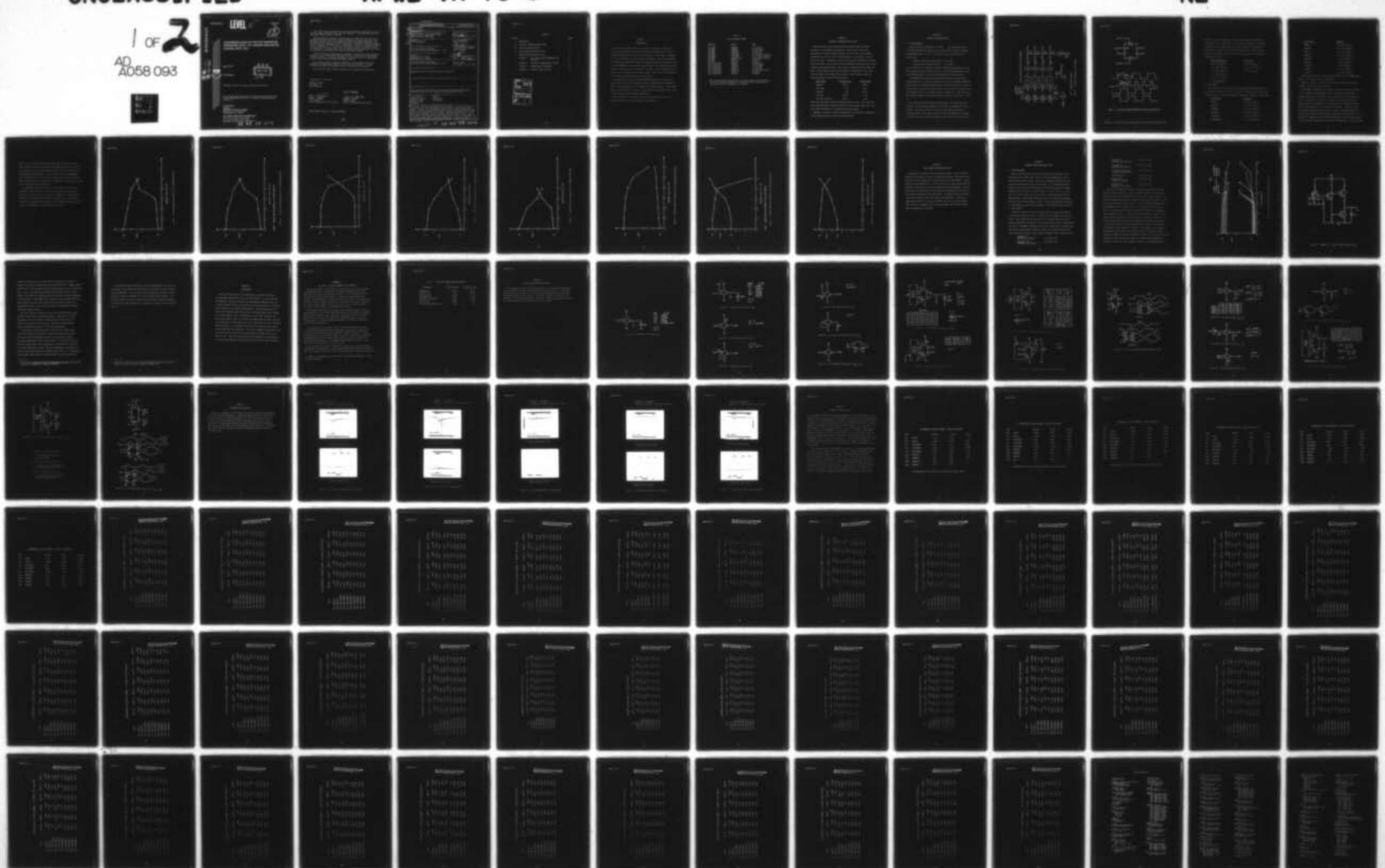

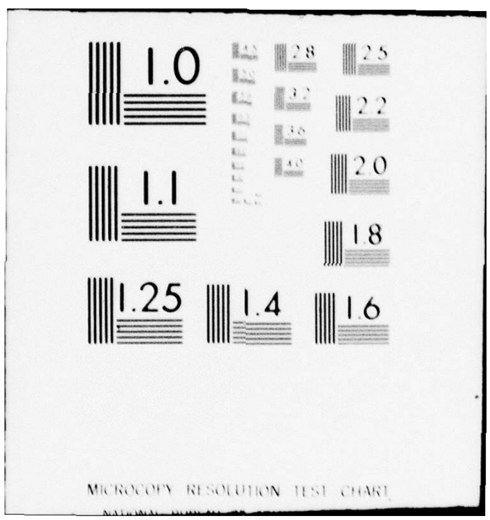
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COMPARISON STUDY OF THE FIVE TRANSISTO TRANSISTOR-LOGIC (TTL) FAMILIES AND EMIT COUPLED LOGIC (ECL)

May 1978

Final Report

Approved for public release; distribution unlimited.

This research was sponsored by the Defense Nuclear Agency un Subtask Z99QAXTB029, Work Unit 62, Radiation Characterizatio of MSI/LSI.

Prepared for
Director
DEFENSE NUCLEAR AGENCY
Washington, DC 20305

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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This technical report has been reviewed and is approved for publication.

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Bipolar Systems	Test Methods
Radiation Tests	
Dose Rate	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the radiation test response of the five transistor-transistor-logic (TTL) technologies and the emitter-coupled-logic (ECL) technology. The five TTL technologies evaluated were Standard, High Speed, Low Power, Low Power Schottky, and Schottky. Quad dual input NAND (TTL) or NOR (ECL) gates and dual D flip-flops from each technology were tested. The devices were characterized for gamma dose-rate logic upset, total gamma dose survivability, and neutron fluence survivability. The data has been analyzed to provide a comparison of each logic technology's radiation response.

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CONTENTS

SECTION I

INTRODUCTION

The objective of this study was to provide a comparative analysis of the radiation response of the TTL (transistor-transistor-logic) and ECL (emitter-coupled-logic) devices listed in table 1. This table is comprised of the five TTL families and two types of ECL gates. The five TTL families are Standard, High Speed, Low Power, Low Power Schottky, and Schottky. Quad dual input NAND (TTL) or NOR (ECL) gates and Dual D flip-flops from each TTL family and ECL type were characterized. The three types of radiation tests performed on these devices were gamma dose-rate logic upset, total gamma dose survivability, and neutron fluence survivability.

The experimental low power Schottky NAND gates listed in table 1 were produced under an Air Force Weapons Laboratory (AFWL) contract F29601-73-C-0048, "Bipolar MSI (Medium Scale Integration) Hardening Study." These NAND gates are dielectrically isolated, and have shallow junctioned arsenic doped emitters and diode photocurrent compensation.

The difference in performance and circuit operation of the five TTL families and the ECL gates is presented in appendix A.

Table 1

LIST OF DEVICES TESTED

Function	Device	Type
TTL NAND	SN5400J	TI Standard
TTL NAND	SN54H00J	TI High Speed
TTL NAND	SN54L00J	TI Low Power
TTL NAND	SN54S00J	TI Schottky
TTL NAND	SN54LS00T	TI Low Power Schottky
TTL NAND	SN74LS00J	TI Low Power Schottky
TTL NAND	Experimental*	TI Low Power Schottky
ECL NOR	950459	Fairchild
ECL NOR	MC10102L	Motorola
TTL D Flip-Flop	SN5474J	TI Standard
TTL D Flip-Flop	SN54H74J	TI High Speed
TTL D Flip-Flop	SN54L74J	TI Low Power
TTL D Flip-Flop	SN54S74J	TI Schottky
TTL D Flip-Flop	SN54LS74J	TI Low Power Schottky
ECL D Flip-Flop	952859	Fairchild
ECL D Flip-Flop	MC10131L	Motorola

* The devices labeled "Experimental" were produced by Texas Instruments (TI) for experimental purposes. The devices contain arsenic doped emitters and are not commercially available.

SECTION II

ELECTRICAL CHARACTERIZATION TESTS

The test devices were electrically characterized before they were subjected to the radiation environments. The electrical tests were performed on a Fairchild 5000 integrated circuit tester. All the NAND and NOR gates listed in table 1 were subjected to approximately the same electrical tests. Likewise, all the D flip-flops were subjected to similar electrical tests. The electrical tests performed on the devices were output voltage, power supply current, input current, propagation delay times, and short circuit output current (not performed on ECL devices). The output high and output low voltages were measured on the TTL devices with the following source and sink currents applied:

Device Type	Source Current	Sink Current
Standard	400 μA	16 mA
High Speed	1 mA	20 mA
Schottky	1 mA	20 mA
Low Power	100 μA	2 mA
Low Power Schottky	400 μA	4 mA

These sink and source currents represent a fanout of ten. The electrical tests were performed on the ECL devices with each output loaded with a 50-ohm resistor connected to a minus-two-volt power supply.

Appendix B contains a detailed description of the electrical characterization tests performed on the TTL and ECL devices.

SECTION III

TRANSIENT RADIATION TESTS

1. TEST PROCEDURES

Figure 1 shows the schematic of the general test setup used for the transient radiation logic upset tests. The TTL load is used to simulate an approximate fanout of ten. The values of R_L for the different TTL families are:

Standard, High Speed, and Schottky - $R_L = 200\Omega$

Low Power and Low Power Schottky - $R_L = 800\Omega$

A 0.1 µF capacitor is applied in parallel with the power supplies to hold them constant during the radiation pulse. Fifty-ohm terminators were used at the oscilloscopes to reduce reflections down the coaxial cables.

The LH0033C unity gain line drivers were used with a divide-by-two resistive divider to provide the necessary drive for the 50-ohm terminated coaxial cables. The NAND and NOR gates were irradiated with both inputs DC biased either at their input high voltage or their input low voltage to get the necessary output low and high voltages, respectively. The D flip-flops were biased dynamically during the radiation pulse as illustrated in figure 2.

The transient radiation tests were performed at the AFWL Flash X-ray facility. The pulse width produced by this FXR is approximately 20 nanoseconds. The output voltage of the devices was monitored during the radiation pulse. Logic upset threshold for the TTL NAND gates is defined as 0.8 volt for the output low voltage and 2.0 volts for the output high

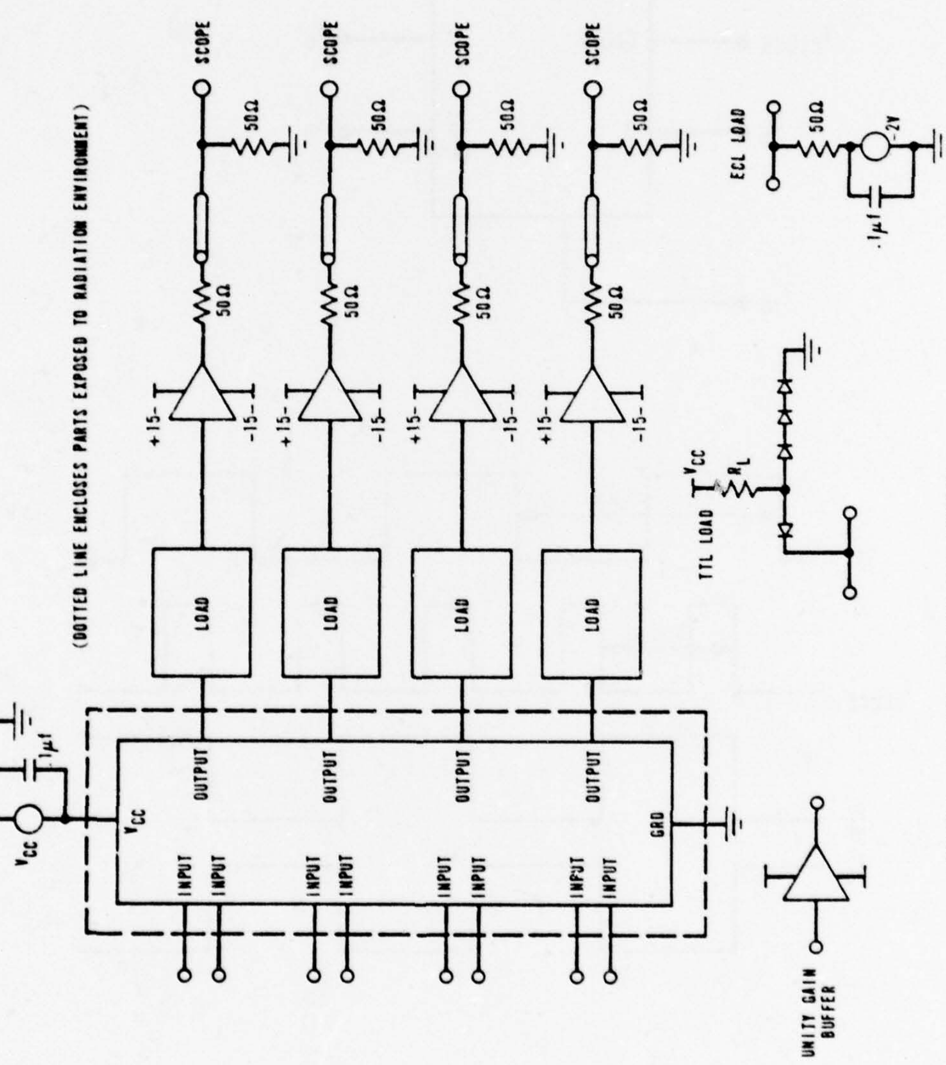

FIGURE 1. TRANSIENT RADIATION TEST SCHEMATIC

Figure 1. Transient Radiation Test Schematic.

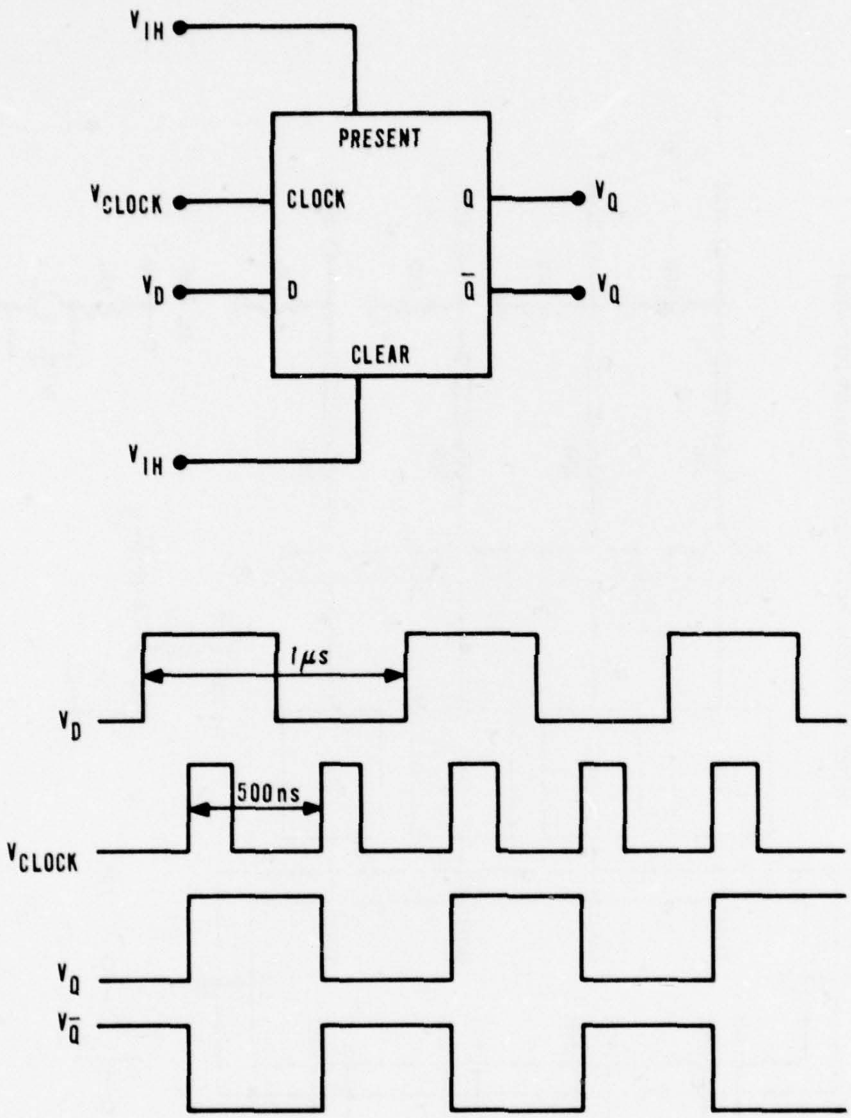

FIGURE 2. D FLIP-FLOP BIAS CONDITIONS DURING THE TRANSIENT RADIATION TESTS

Figure 2. D Flip-Flop Bias Conditions During the Transient Radiation Tests

voltage. For the ECL NOR gates the logic upset threshold is defined as - 1.100 volts and - 1.500 volts for output high and output low voltages, respectively. The D flip-flops logic upset threshold occurs when the radiation pulse causes the flip-flop to change state. Three devices of each device type were tested. The devices were tested at the following transient dose rates:

NAND and NOR Gates	D Flip-Flops
1.8×10^8 rad(Si)/s	2×10^8 rad(Si)/s
3.6×10^8 rad(Si)/s	4.4×10^8 rad(Si)/s
7.2×10^8 rad(Si)/s	7×10^8 rad(Si)/s
1.4×10^9 rad(Si)/s	
3.2×10^9 rad(Si)/s	
6×10^9 rad(Si)/s	

2. TEST RESULTS

All three devices of each particular type exhibited approximately the same transient radiation response. The largest tested transient dose-rates at which all the tested devices operated without logic upset are shown below:

Device Type	Dose-Rate
SN5400J	7.2×10^8 rad(Si)/s
SN54H00J	7.2×10^8 rad(Si)/s
SN54S00J	7.2×10^8 rad(Si)/s
SN54L00J	3.6×10^8 rad(Si)/s
SN54LS00T	3.6×10^8 rad(Si)/s
Experimental	3.2×10^9 rad(Si)/s

Device Type	Dose-Rate
950459	3.6×10^8 rad(Si)/s
MC10102L	3.6×10^8 rad(Si)/s
SN5474J	4.4×10^8 rad(Si)/s
SN54H74J	4.4×10^8 rad(Si)/s
SN54S74J	4.4×10^8 rad(Si)/s
SN54L74J	2×10^8 rad(Si)/s
SN54LS74J	2×10^8 rad(Si)/s
952859	4.4×10^8 rad(Si)/s
MC10131L	4.4×10^8 rad(Si)/s

Graphs illustrating the complete photoresponse of the TTL NAND and ECL NOR gates are shown in figures 3 through 10.

Appendix C contains oscilloscope photographs showing the radiation response of some of the devices tested.

The Standard, High Speed, and Schottky TTL devices are more resistant to the transient ionizing radiation than the Low Power and Low Poser Schottky TTL devices. The higher current densities of the Standard, High Speed, and Schottky TTL devices will sweep out the hole-electron pairs generated during the transient radiation pulse more efficiently than the lower current densities of the Low Power TTL devices. Similarly, since ECL operates at high current densities, the ECL D flip-flops exhibit the same failure threshold as the Standard, High Speed, and Schottky TTL D flip-flops. However, the ECL NOR gates exhibited a lower failure threshold than the Standard, High Speed, and Schottky TTL NAND gates. This discrepancy may be due to the failure thresholds being defined too conservatively. The experimental arsenic doped emitter TTL NAND gates produced by Texas Instruments were an order of magnitude harder to the transient ionizing radiation than the equivalent Low Power Schottky devices (SN54LS00T). These experimental gates are dielectrically isolated and have extremely small geometries and diode photocurrent compensation. These factors result in the increased dose-rate hardness.

The NAND gates are harder than the D flip-flops of the same TTL technology. The D flip-flop is softer to the radiation pulse because after the clock pulse, the D flip-flop is a memory device (see figure 2). Therefore, the D flip-flop will be more susceptible to a perturbation caused by the transient radiation pulse than the NAND gate, whose output is directly dependent on the input during the pulse.

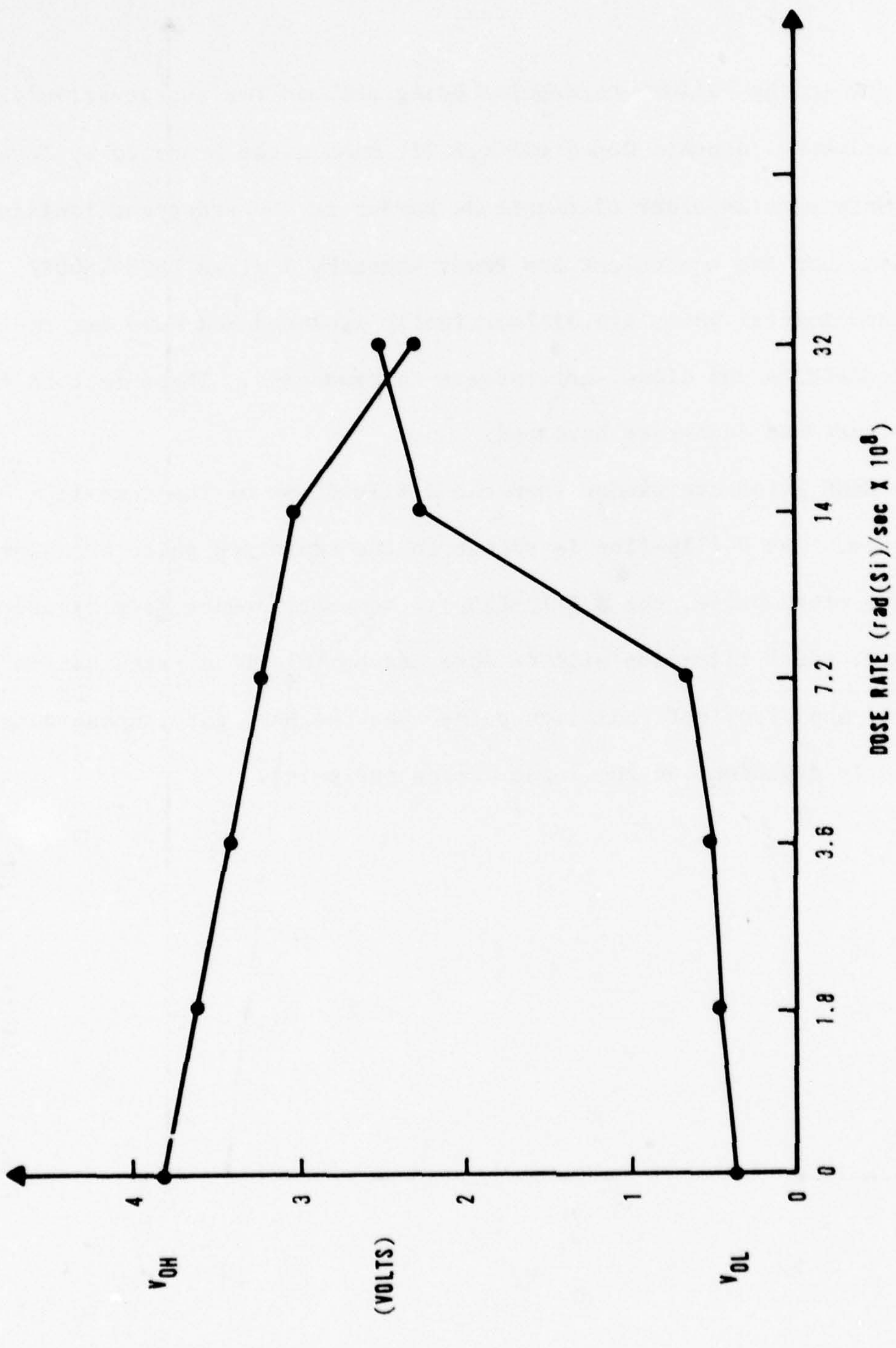

Figure 3. Transient Radiation Response of TTL SN5400J Nand Gate

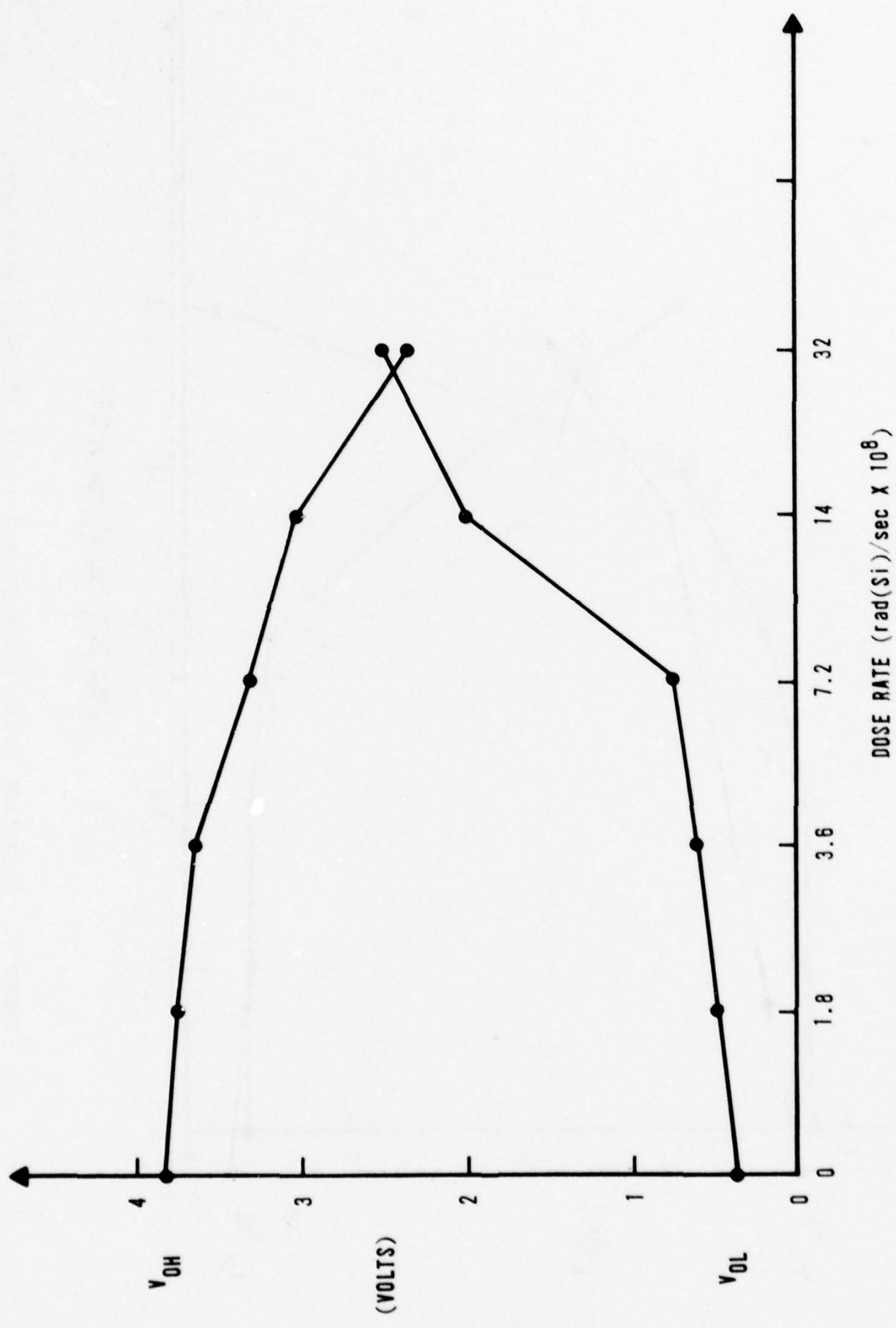

FIGURE 4. TRANSIENT RADIATION RESPONSE OF TTL SN54H00J NAND GATE

Figure 4. Transient Radiation Response of TTL SN54H00J Nand Gate.

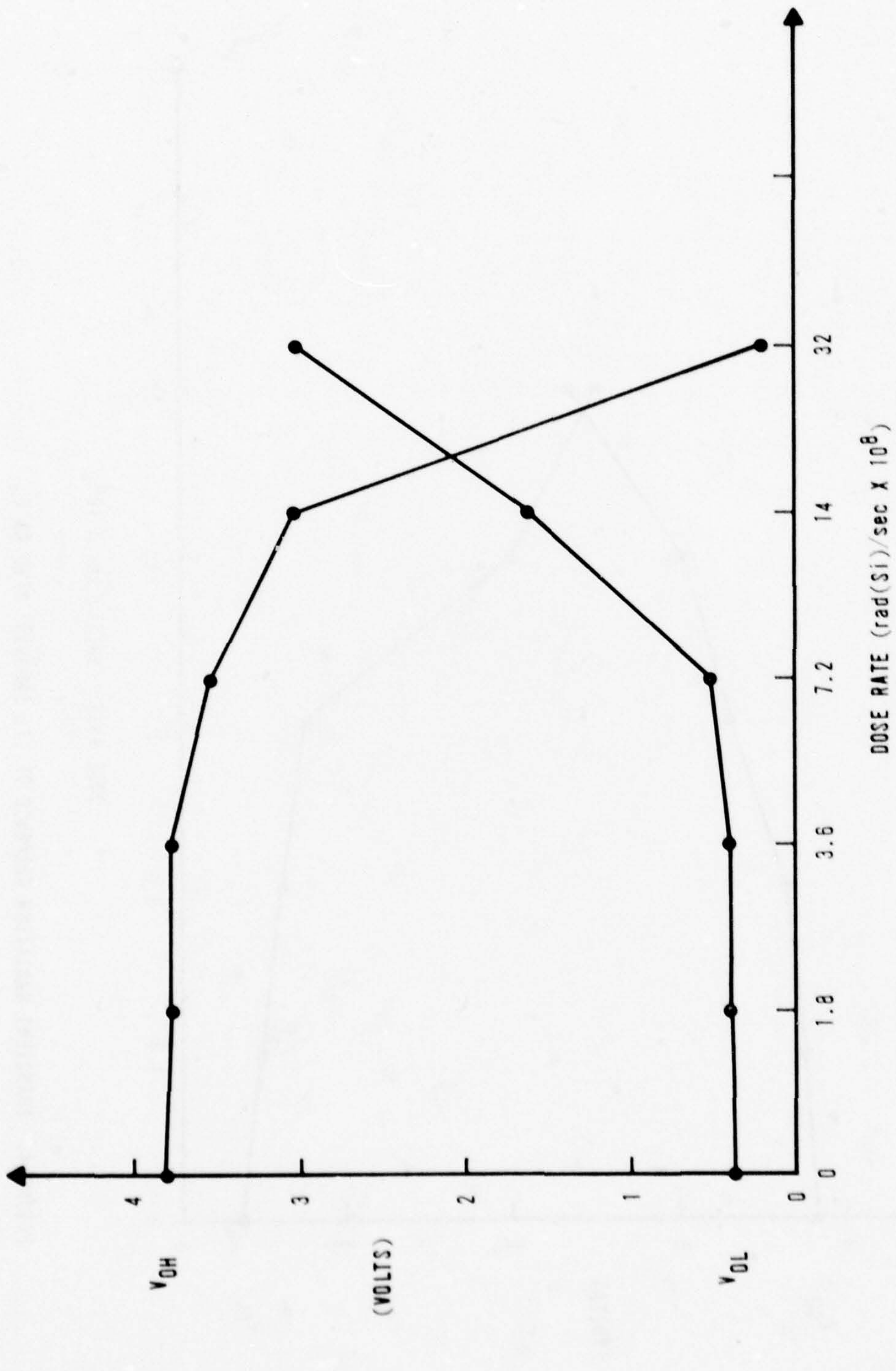

Figure 5. Transient Radiation Response of TTL SN5400J Nand Gate.

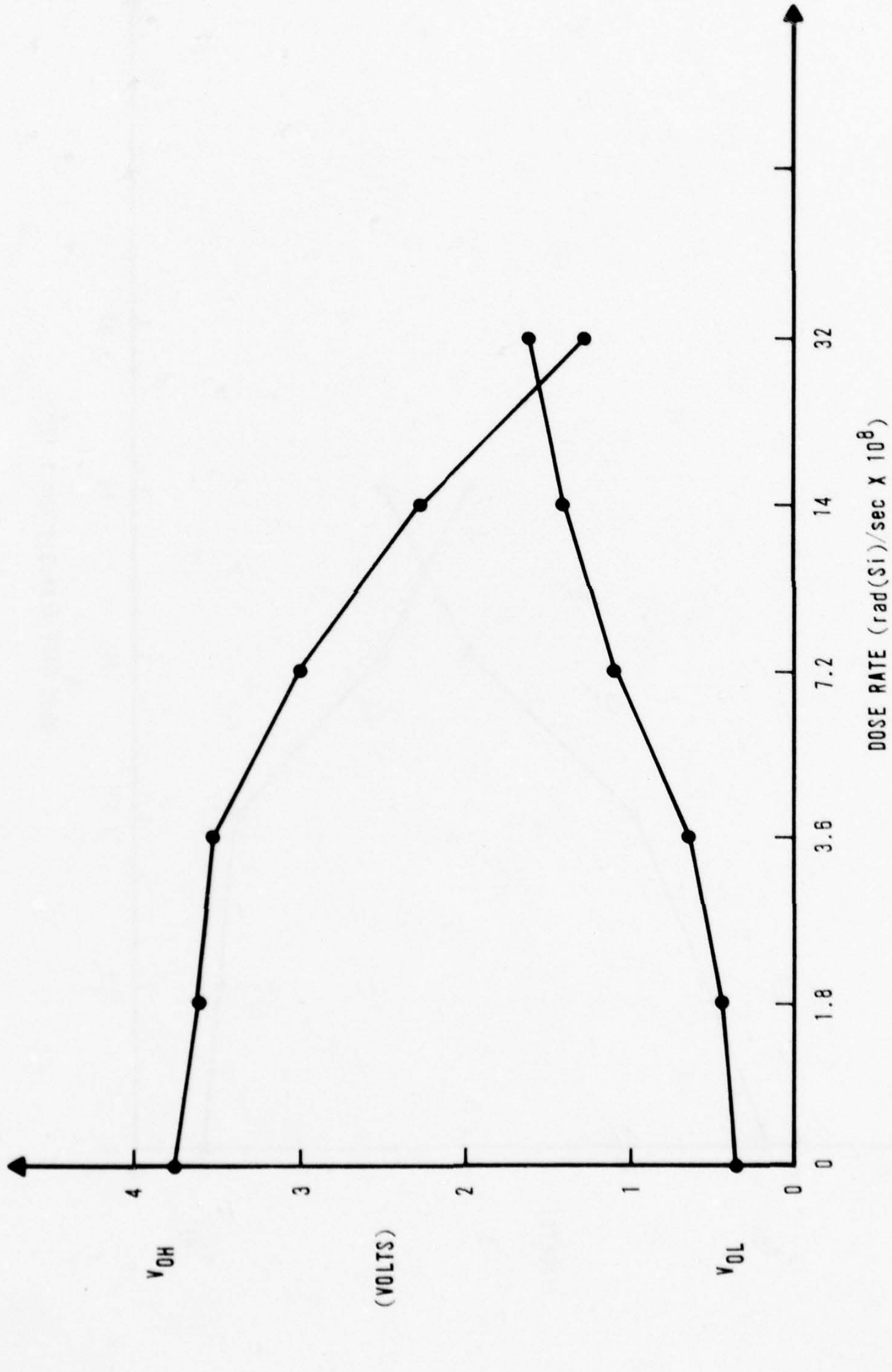

Figure 6. Transient Radiation Response of TTL Sn54L00J Nand Gate

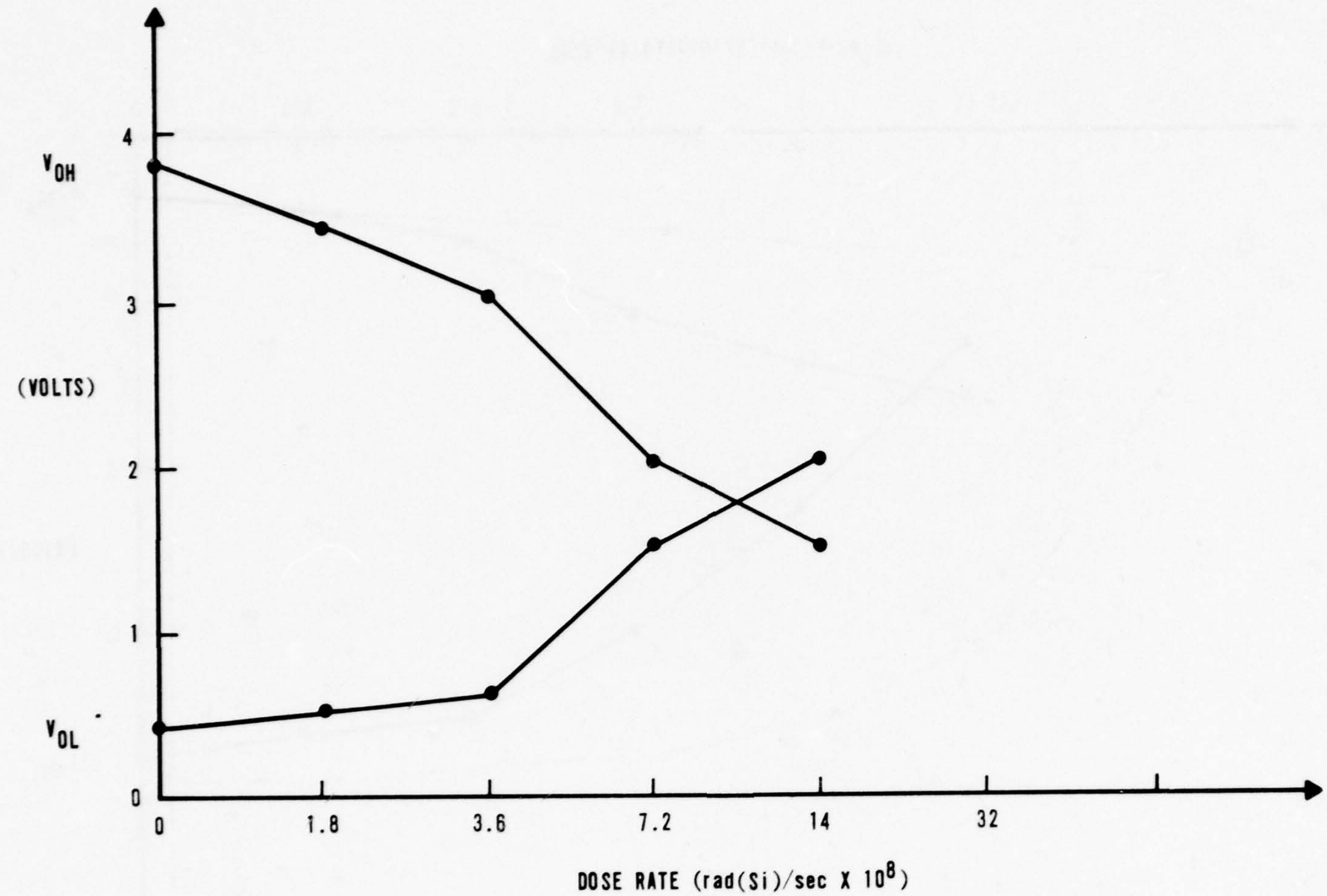

Figure 7. Transient Radiation Response of TTL SN54LS00J Nand Gate.

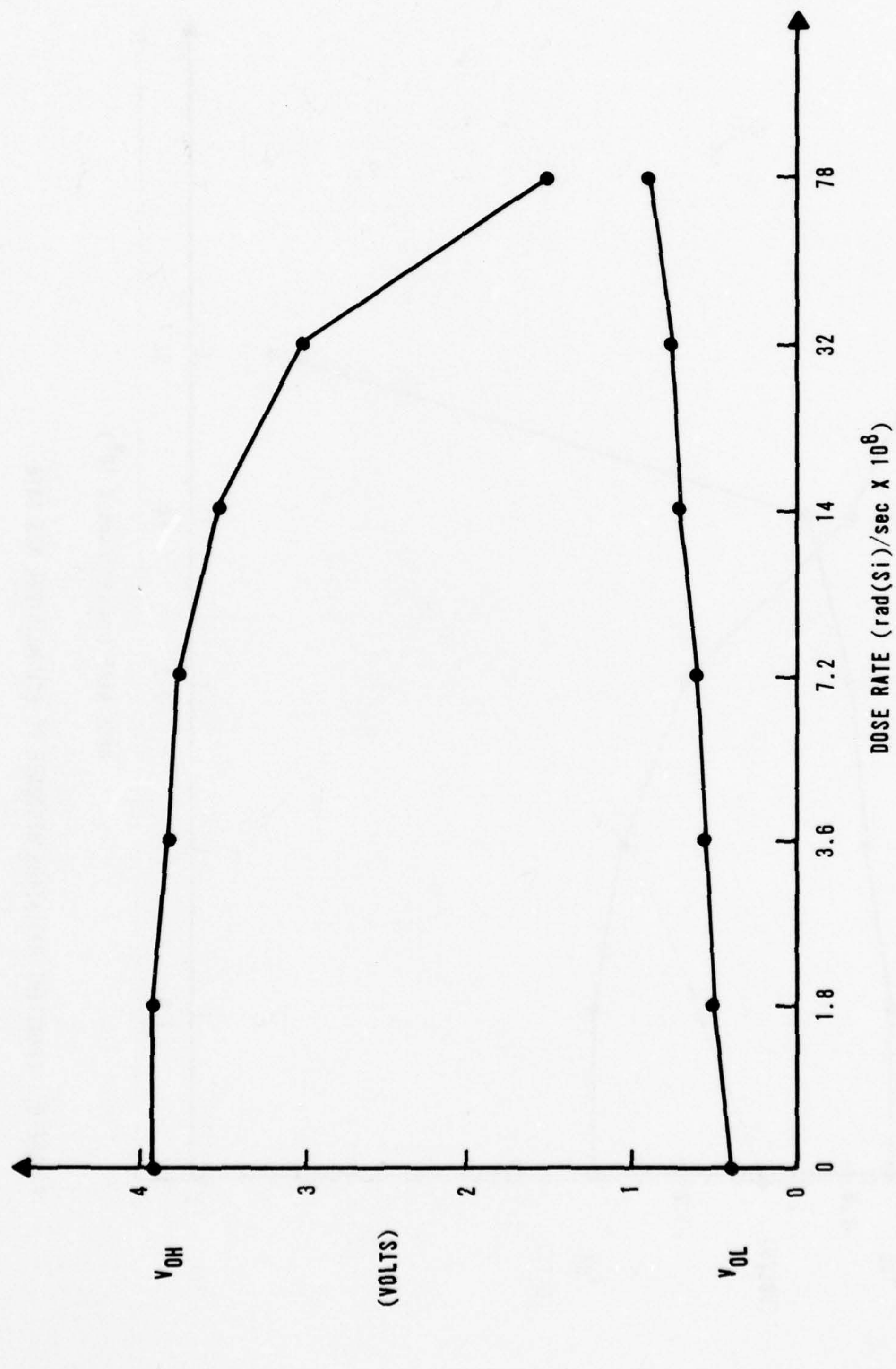

Figure 8. Transient Radiation Response of TTL Experimental Nand Gate.

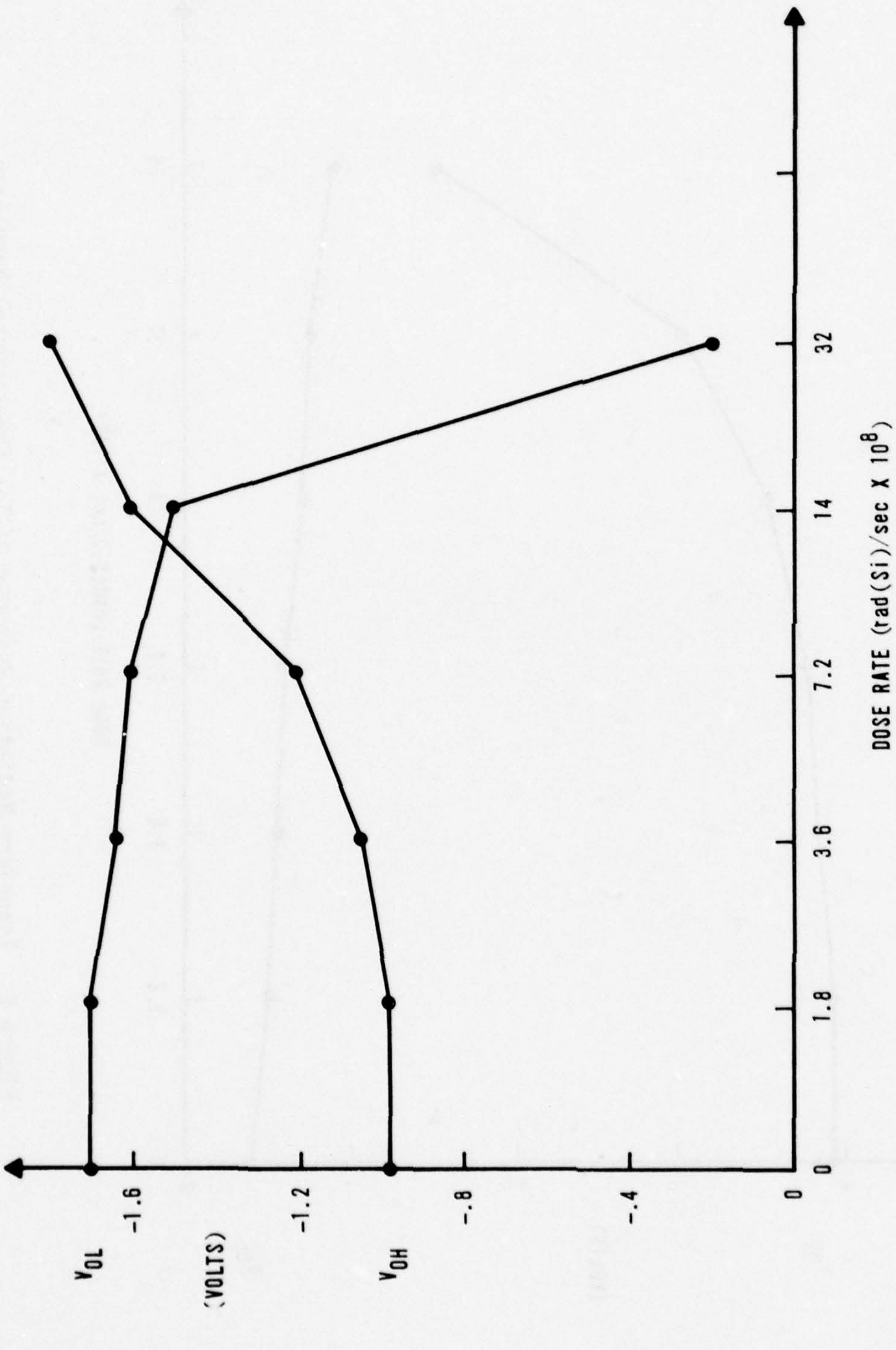

FIGURE 9. TRANSIENT RADIATION RESPONSE OF ECL MC10102L NOR GATE

Figure 9. Transient Radiation Response of ECL MC10102L NOR Gate.

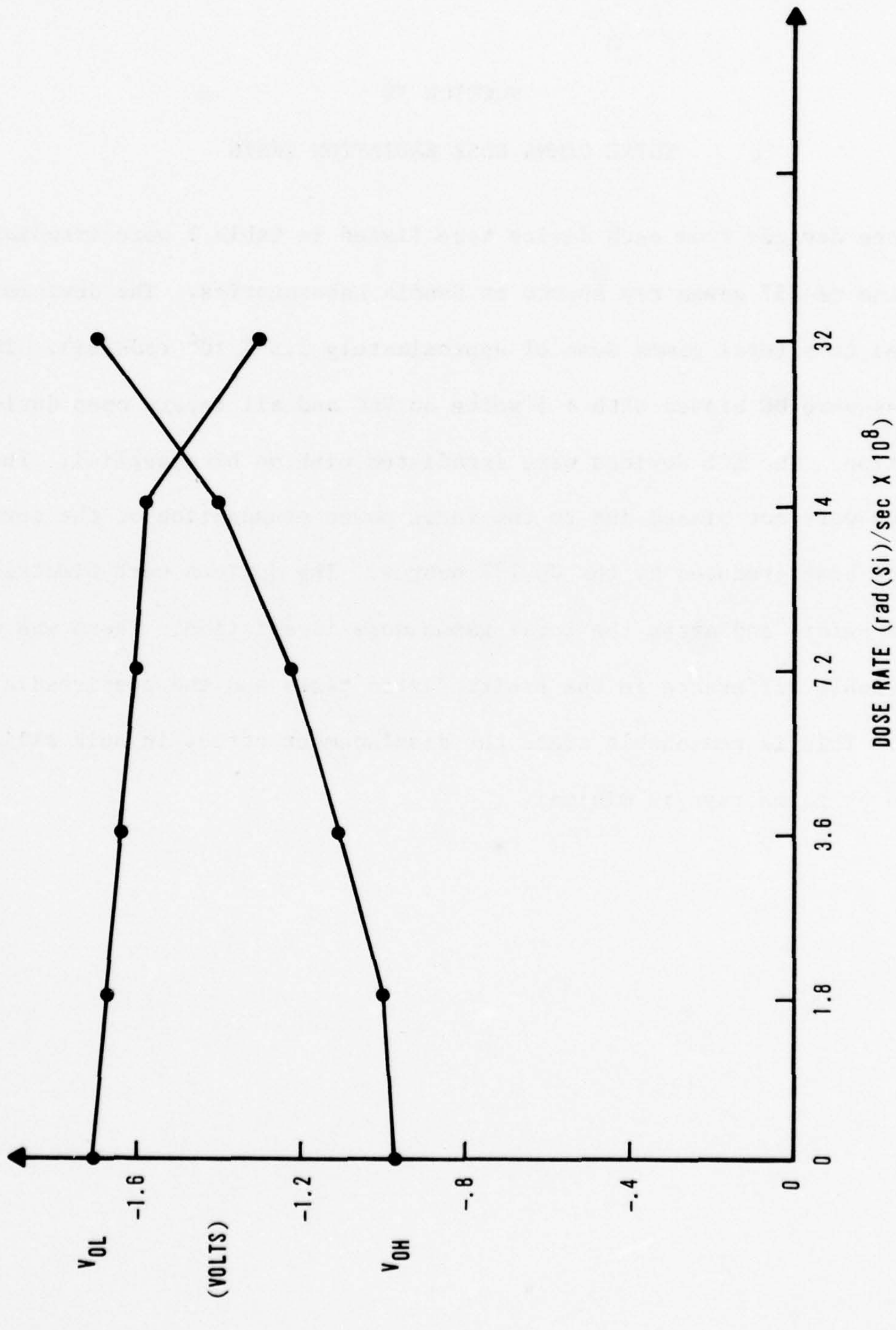

Figure 10. Transient Radiation Response of ECL 950459 NOR Gate.

SECTION IV

TOTAL GAMMA DOSE RADIATION TESTS

Three devices from each device type listed in table 1 were irradiated with the Cs-137 gamma ray source at Sandia Laboratories. The devices were exposed to a total gamma dose of approximately 1.5×10^6 rads(Si). The TTL devices were DC biased with + 5 volts on VCC and all inputs open during the radiation. The ECL devices were irradiated with no bias applied. The ECL devices were not biased due to the large power consumption of the devices and the heat produced by the Cs-137 source. The devices were electrically tested before and after the total gamma dose irradiation. There was no appreciable difference in the preirradiated tests and the postirradiated tests. This is reasonable since the displacement effect in bulk silicon caused by gamma rays is minimal.

SECTION V

NEUTRON FLUENCE RADIATION TESTS

1. TEST PROCEDURES

Three or four devices from each device type listed in table 1 were irradiated with the fast burst reactor at Sandia Laboratories in incremental neutron fluence levels. After each incremental radiation dose was reached, the devices were electrically tested. The cumulative neutron fluence levels at which the devices were electrically tested were approximately 2.8×10^{12} n/cm^2, 6.9×10^{13} n/cm^2, 1.4×10^{14} n/cm^2, 7.3×10^{14} n/cm^2, 1.2×10^{15} n/cm^2, and 2×10^{15} n/cm^2. These fluence levels are 1 MeV equivalent. Approximately 80 devices were irradiated simultaneously with no electrical bias applied to them. Output voltage failure thresholds for these tests are the same as defined for the transient radiation tests.

2. TEST RESULTS

Appendix D contains the neutron fluence test data that were gathered on the devices listed in table 1. These data are presented in the form of tables. Upon examination of these data, it is apparent that the neutron fluence survivability threshold for a particular device type is approximately the same for the NAND or NOR gates as for the D flip-flops of the same type. The largest tested neutron fluences at which all the tested devices will operate before the output voltage failure threshold occurs are shown below:

Standard TTL (SN5400J and SN5474J)	=	1.4×10^{14} n/cm^2
High Speed TTL (SN54H00J and SN54H74J)	=	4.6×10^{14} n/cm^2

Schottky TTL (SN54S00J and SN54S74J)	=	1.2×10^{15} n/cm^2
Low Power TTL (SN54L00J and SN54L74J)	=	1.4×10^{14} n/cm^2
Low Power Schottky TTL (SN54LS00T and SN54L574J)	=	1.4×10^{14} n/cm^2
Experimental TTL	=	7.3×10^{14} n/cm^2
Fairchild ECL (950459 and 952859)	=	4.6×10^{14} n/cm^2
Motorola ECL (MC10102L and MC10131L)	=	4.6×10^{14} n/cm^2

All the TTL devices failed when the output low voltage became larger than the failure threshold. Figure 11 provides graphs of the averaged output voltage of the different TTL families versus neutron fluence. The Fairchild 5000 was not allowed to measure greater than 1.638 volts for the output low voltage for the TTL devices. As can be seen from this figure, the degradation of the output voltage is very gradual until the device fails. At the point of failure, the output low voltages rise suddenly. These output low voltage failures in the TTL devices are a result of the neutron-caused beta degradation of Q1 shown in figure 12. When beta is decreased sufficiently by the neutron radiation, the sink current being forced at the output will cause transistor Q1 to come out of saturation and enter the linear region of operation. As a result of the transistor entering the linear region, the collector-emitter voltage (V_{CE}), which equals the output low voltage, increases to failure. Since the sink current simulates a fanout of ten, the output low voltage failure thresholds are correct for this worst case condition. However, if the NAND gates were

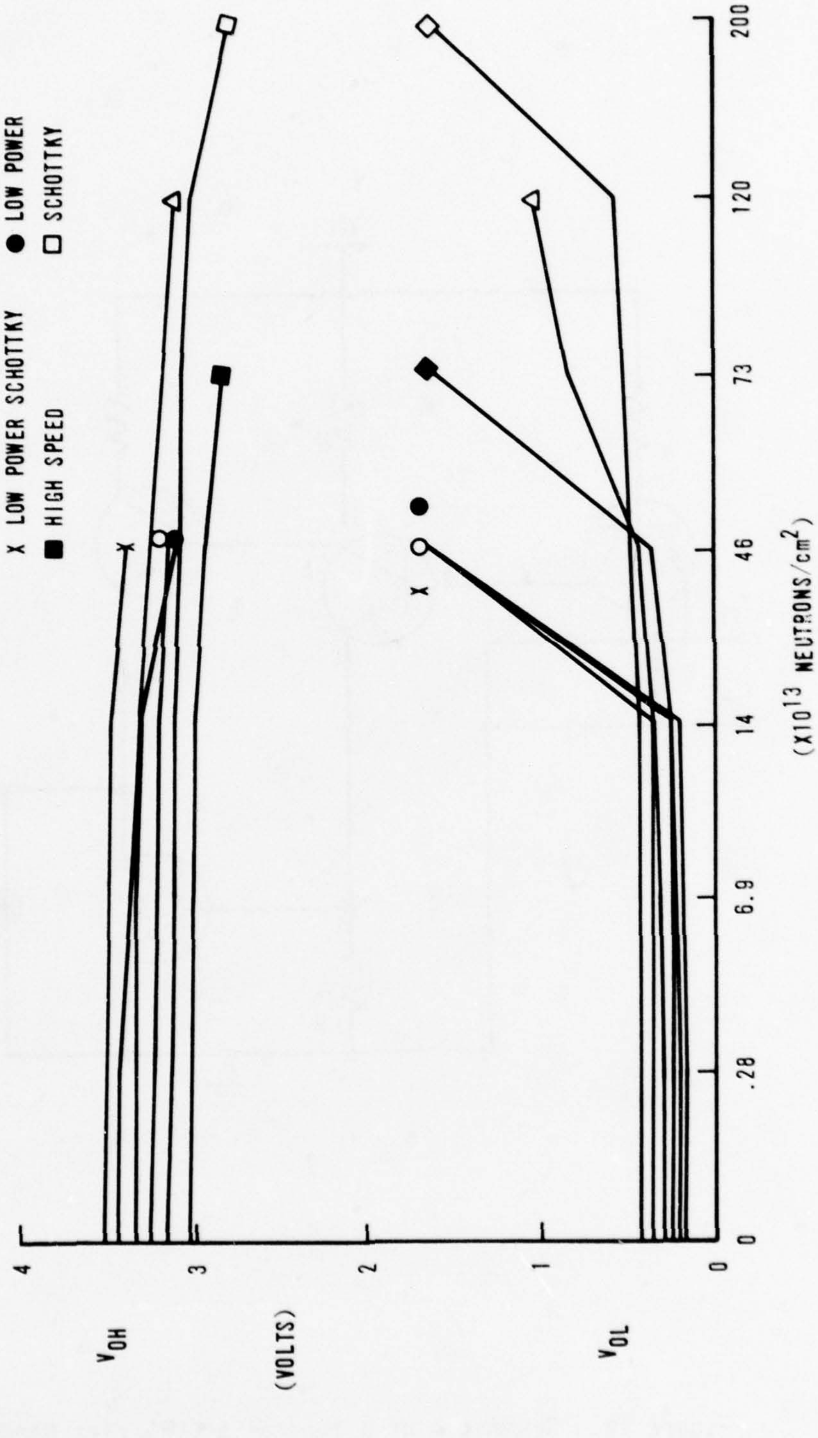

Figure 11. TTL Output Voltage Versus Neutron Fluence.

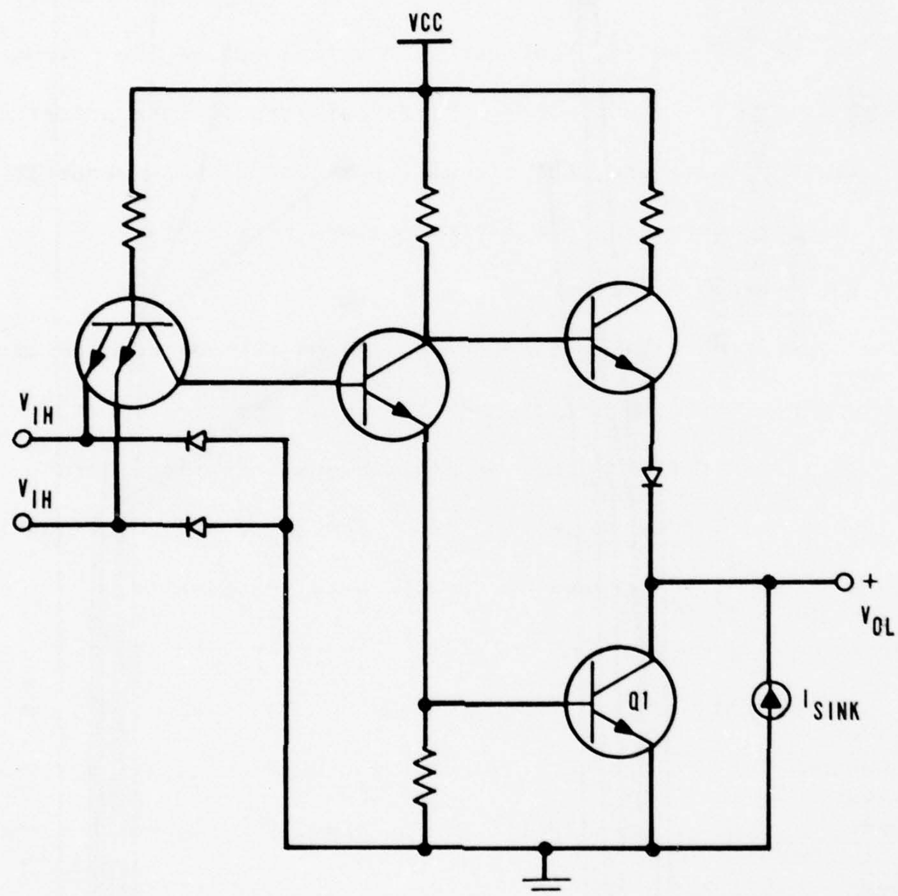

Figure 12. Schematic of a Typical 5400 Series Nand Gate.

tested with a smaller sink current, which is equivalent to a smaller fanout, the output low voltage would not have failed until a higher neutron fluence level. This conclusion cannot directly apply to the TTL flip-flops because one of the internal gates, which does not have the same circuit design as the 5400 series NAND gates, may fail before the output NAND gates of the flip-flop. In ECL gates, the transistors operate primarily in the linear region; therefore, the circuit operation is more sensitive to degradations in beta, and the neutron-caused beta degradation ultimately causes the voltage failures.

The other electrical parameters tested on the devices (power supply current, input current, and propagation delay times) did not deviate appreciably from their maximum or minimum specifications before the output voltage changes caused failure. The input and power supply currents generally decreased due to the beta degradation.

As shown above, the High Speed TTL, Schottky TTL, and ECL gates operated at larger neutron fluences than the lower power TTL devices. The neutron-caused displacement damage in these devices results in decreased recombination lifetime in the base. If the emitter areas and the base transit times of the transistors of the different TTL families are assumed approximately equal, then the recombination rate/carrier is less for devices which operate at higher currents (ref. 1). This explains why the higher-power devices are more resistant to neutron radiation.

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1. Larin, Frank, Radiation Effects in Semiconductor Devices, New York, NY, John Wiley and Sons, Inc., 1968, pp 159-169.

The Texas Instruments Experimental arsenic doped emitter TTL gates were much harder to the neutron radiation than the equivalent Low Power Schottky devices (SN54LS00T). The very sharp arsenic doped emitter profile in these devices is primarily responsible for the increased neutron hardness. The resulting abrupt emitter-base region width decreases the amount of emitter-base depletion region recombination, resulting in increased neutron hardness (ref. 2).

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2. Gwyn, G.W., and Gregory, B.L., "Designing Ultrahard Bipolar Transistors", Sandia Laboratories Technical Report, September 1971.

SECTION VI

CONCLUSIONS

This report shows that, of the commercially available TTL devices, the High Speed and Schottky devices are the hardest to all the radiation environments. However, as shown by the Experimental NAND gate data, the Low Power Schottky devices can be made very hard with dielectric isolation, small geometries, and arsenic doped emitters. The ECL devices were not harder than the higher-power TTL devices, even though their power consumption is much higher. This is probably due to the linear operation and small noise margin of ECL. As expected, the NAND gates were more resistant to the transient radiation pulse than the D flip-flops, since the flip-flops are memory devices. A variation in the electrical testing of the output voltage would have been beneficial. The output voltage of the devices could have been tested for various fanout sink currents instead of just for a fanout of ten. This would have provided more information to the designer on neutron survivability of the gates for less than worst case conditions.

APPENDIX A

TTL AND ECL CIRCUIT PERFORMANCE AND OPERATION

The Five TTL families and ECL gates can be classified as either saturating or nonsaturating logic. The Standard, Low Power and High Speed TTL circuit families belong in the saturating logic category. The TTL Schottky, TTL Low Power Schottky and ECL circuit families belong in the nonsaturating logic category. Nonsaturating logic differs from saturated logic in that the gates in the latter category contain transistors which saturate during circuit operation. As a result, excess charge is stored in the base of the saturated transistor resulting in slower response and propagation delay time.

The Low-Power TTL gate uses less power than the Standard TTL gate, which is shown in figure 12 of the text. This lower power results in slower propagation delay times as compared to the standard TTL technology. Similarly, the High Speed TTL devices use more power than the Standard TTL devices to gain the increased speed. The power consumption and speed are primarily controlled by the resistors in these gates.

The Schottky (S) and Low Power Schottky (LS) TTL technologies are similar to the Low Power and High Speed TTL technologies, respectively. However, the S and LS TTL technology gates contain Schottky clamped transistors to prevent them from entering the saturation region of operation. This results in decreased propagation delay time for a given current due to the absence of base excess charge caused by saturation. The Schottky clamped transistors operate at the edge of saturation when they're in a given state.

The ECL devices are capable of much faster speeds than the TTL technologies. The ECL gates are designed for a small output voltage swing, high power consumption, and linear transistor operation to attain increased speeds over other technologies.

Table A-1 of this appendix illustrates the power speed relationships of these TTL and ECL families.

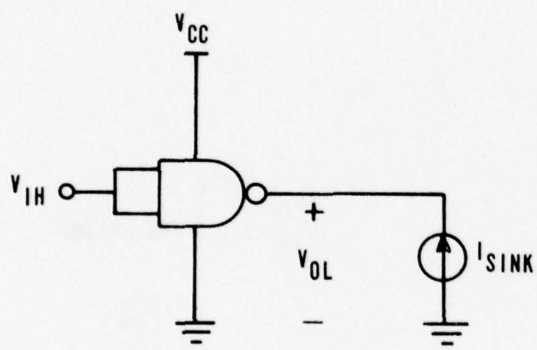
Table 1. TTL AND ECL POWER SPEED RELATIONSHIPS

Technology	Typical P_D Gate	Typical t_p Gate
Standard TTL	10 mW	10 ns
Low Power TTL	1 mW	33 ns
High Speed TTL	22 mW	6 ns
Low Power Schottky TTL	2 mW	9.5 ns
Schottky TTL	19 mW	3 ns
ECL (Fairchild 95K series)	25 mW	2 ns

APPENDIX B

ELECTRICAL CHARACTERIZATION TESTS

This appendix contains a detailed description of the electrical characterization tests performed on the TTL and ECL devices listed in table 1 of the text. These tests were performed at the Air Force Weapons Laboratory on the Fairchild 5000/5800 Integrated Circuit Tester. Figures B1 through B12 contain the tests performed on the TTL NAND gates and D flip-flops. Figures B13 through B19 contain the tests performed on the ECL NOR gates and D flip-flops.

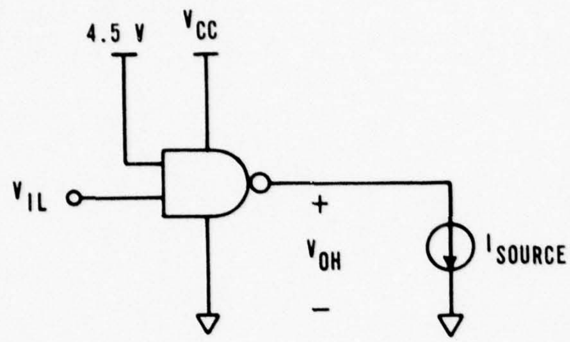


I_{SINK}	TTL TYPE
16 mA	STANDARD
20 mA	HIGH SPEED
20 mA	SCHOTTKY
2 mA	LOW POWER
4 mA	LOW POWER SCHOTTKY

$V_{CC} = 5V$

$V_{IH} = 2V$

Figure 31. TTL Output Low Voltage (V_{OL})

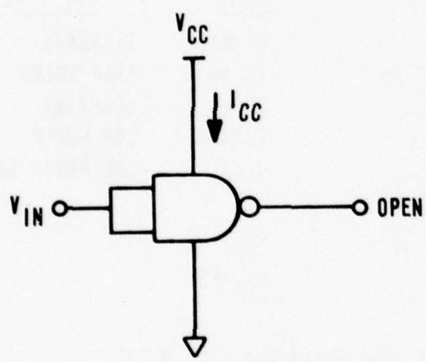


I_{SOURCE}	TTL TYPE
400 μA	STANDARD
1 mA	HIGH SPEED
1 mA	SCHOTTKY
100 μA	LOW POWER
400 μA	LOW POWER SCHOTTKY

V_{IL} = .4 V

V_{CC} = 5 V

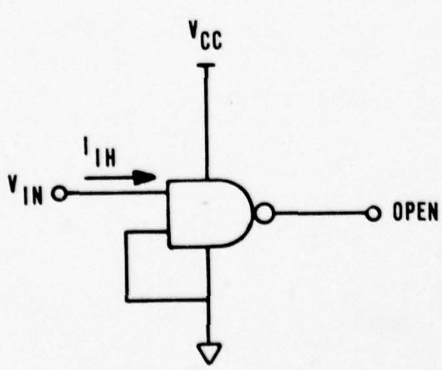
Figure B2. TTL Output High Voltage (V_{OH})



V_{CC} = 5.5 V

V_{IN} = 5.5 V AND GROUND

Figure B3. TTL Power Supply Current (I_{CC})



V_{CC} = 5.5 V

V_{IN} = 5.5 V AND 2.4 V

Figure B4. TTL Input High Current (I_{IH})

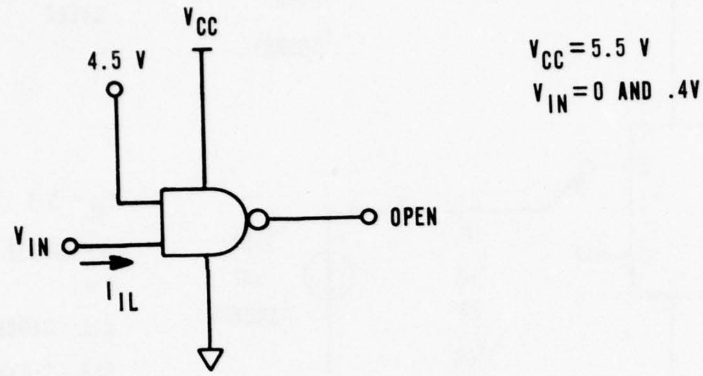


Figure B5. TTL Input Low Current (I_{IL})

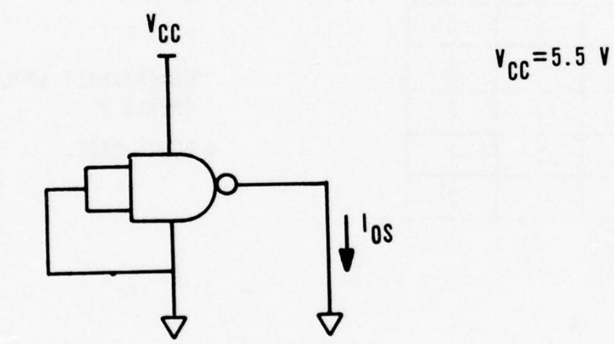


Figure B6. TTTL Short Circuit Output Current (I_{OS})

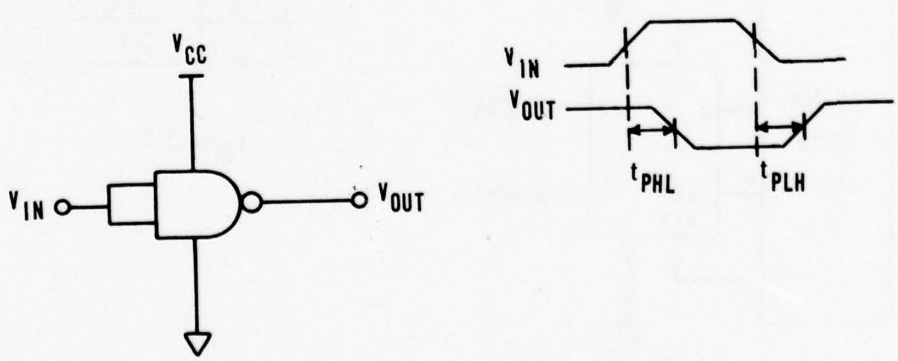
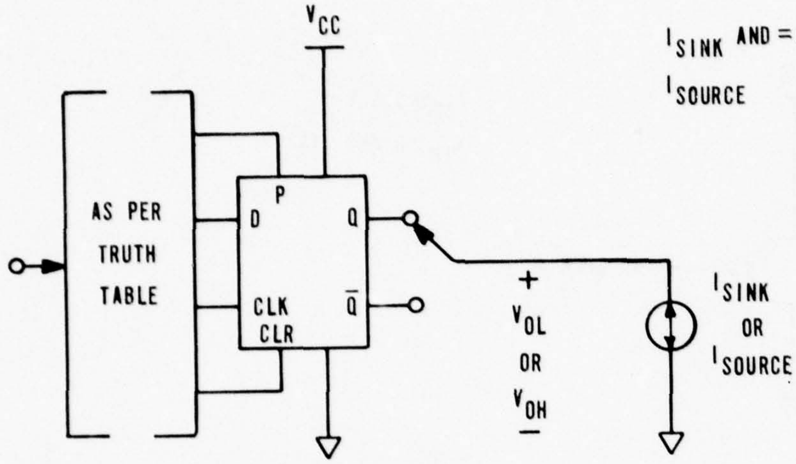


Figure B7. TTL Propagation Delay Times (T_{PHL}, T_{PLH})



I_{SINK} AND = SAME AS TTL NAND GATES
I_{SOURCE}

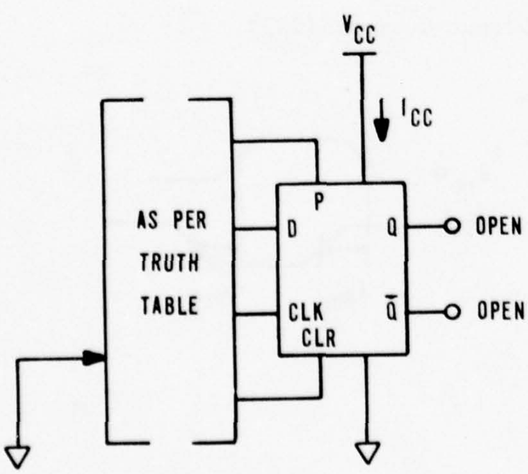
V_{CC} = 5 V
P = PRESET
D = D
CLK = CLOCK
CLR = CLEAR

TRUTH TABLE

P	CLR	CLK	D	Q	Q
0	1	X	X	0	1
1	0	X	X	1	0
1	1	1*	0	0	1
1	1	1*	1	1	0

0 = .8 V
1 = 2 V
*MOMENTARILY APPLY .4 V THEN 2 V
+ DON'T CARE

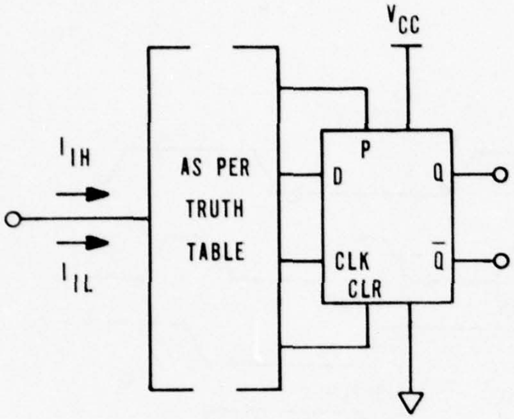
Figure 38. TTL F/F Output Voltage (V_{OL} and V_{OH})



TEST	APPLY GND	OPEN
I_{CC}	CLK, D, P	CLR
I_{CC}	CLK, D, CLR	P

V_{CC}=4.5 V

Figure 39 TTL F/F Power Supply Current (I_{CC})



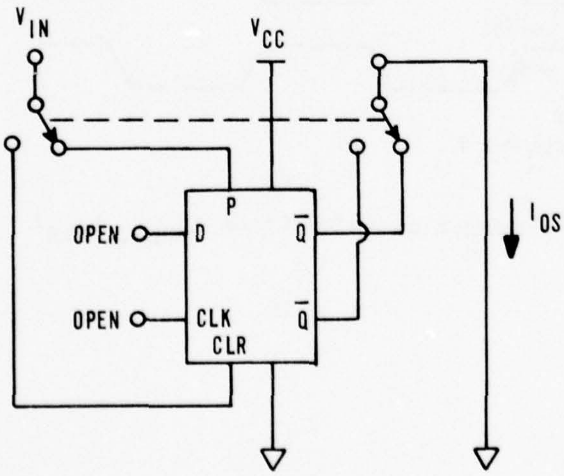
APPLY 2.4 V AND 5.5 V TEST I_{IH}	APPLY 4.5 V	APPLY GND
CLK	CLR, D	P
CLK	P, D	CLR
P	CLR, D	CLK
CLR	P	D, CLK *
D	P, CLK	CLR

APPLY .4 V TEST I_{IL}	APPLY 4.5 V	APPLY GND
CLK	CLR	P, D
P	CLR	CLK, D
CLR	CLK, D, P	
D	CLR, CLK	P

$V_{CC} = 5.5$ V

*MOMENTARILY APPLY GND THAN 4.5 V

Figure B10 TTL F/F Input Current (I_{IN}, I_{IL})



$V_{CC} = 5.5$ V

$V_{IN} = GND$

Figure B11. TTL F/F Short Circuit Output Current (I_{OS})

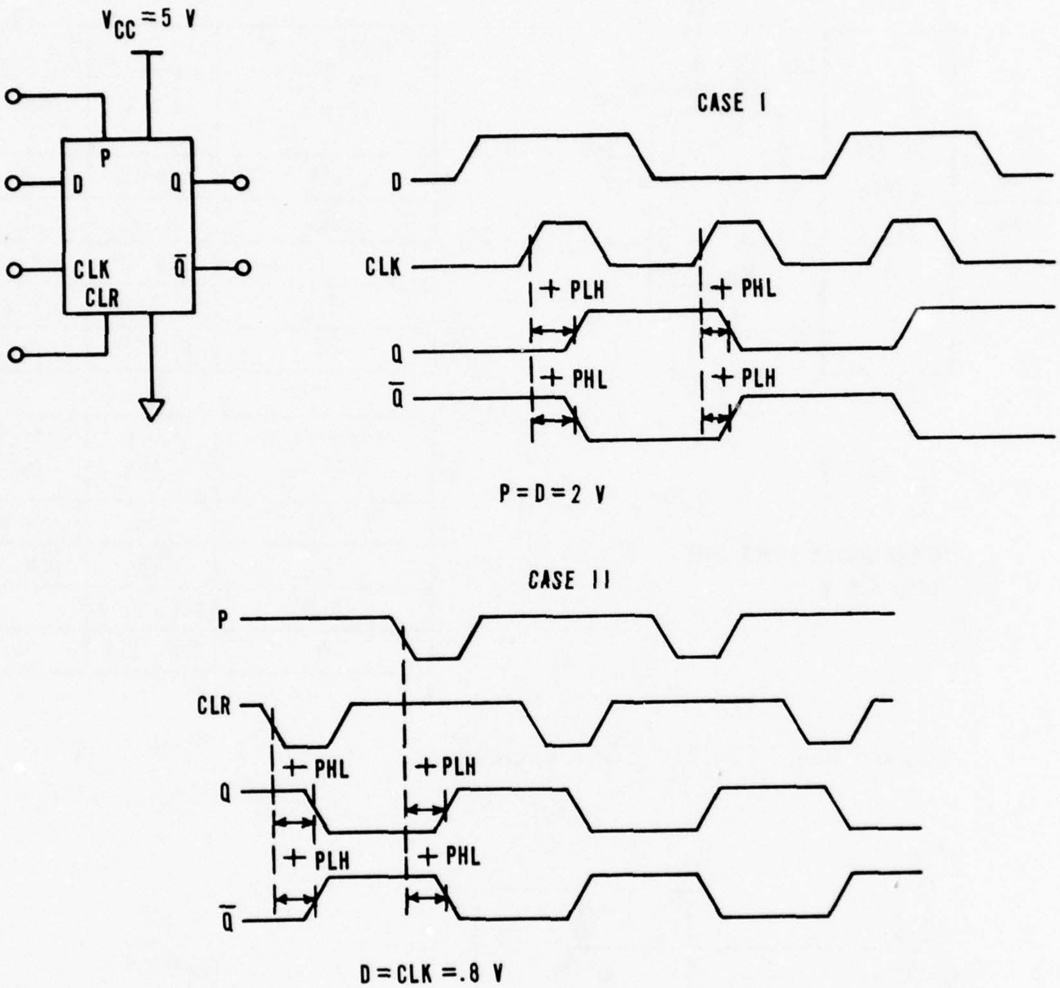
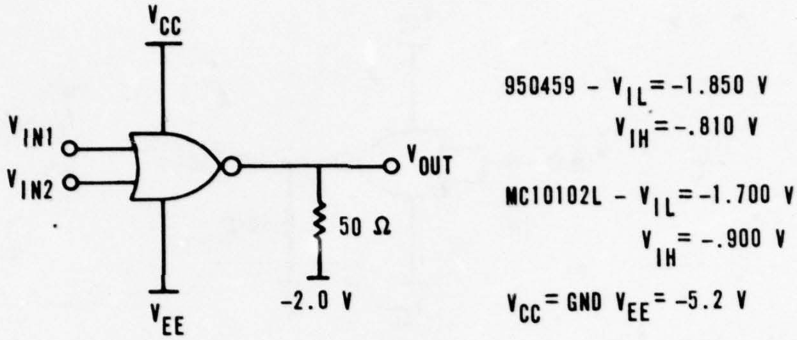


Figure B12. TTL F/F Propagation Delay Times (t_{PHL}, t_{PLH})



	V_{IN1}	V_{IN2}	V_{OUT}
CASE I	V_{IL}	V_{IH}	V_{OH}
CASE II	V_{IH}	V_{IL}	V_{OH}
CASE III	V_{IH}	V_{IH}	V_{OL}

Figure B13. ECL Output Voltage (V_{OH}, V_{OL})

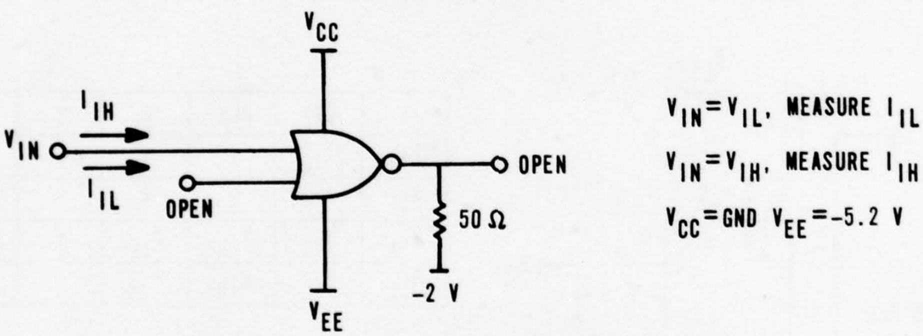


Figure B14. ECL Input Current (I_{IL}, I_{IN})

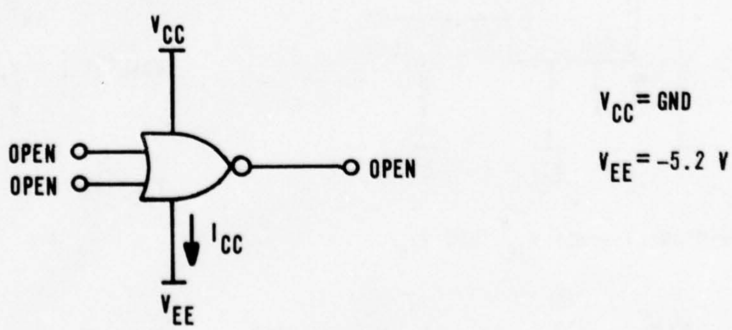


Figure B15. ECL Power Supply Current (I_{CC})

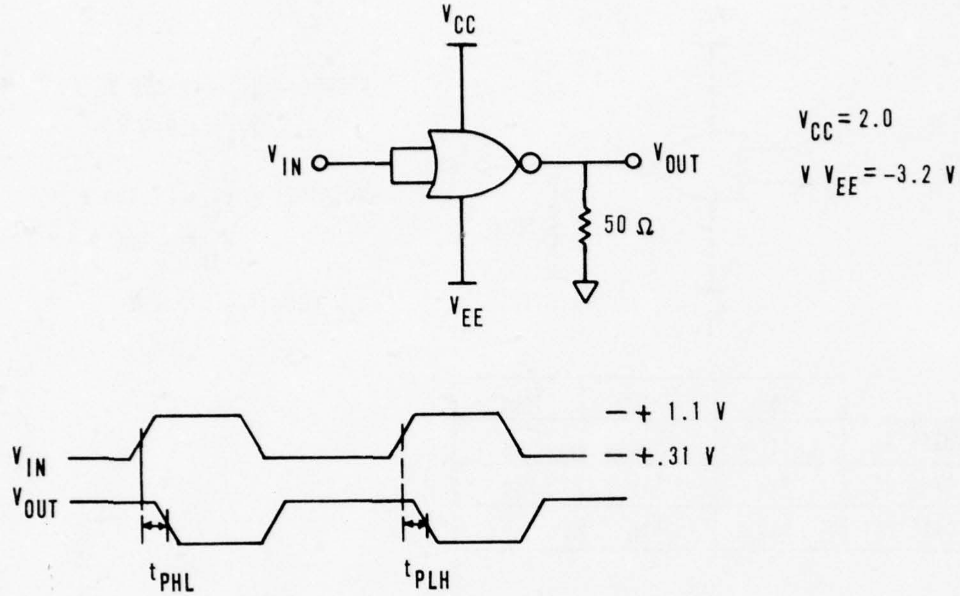
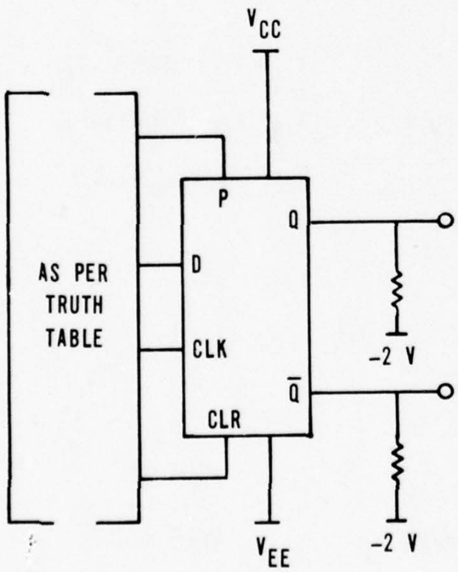


Figure B16. ECL Propagation Delay Time (t_{PHL}, t_{PLH})



P	CLR	CLK	D	Q	$\bar{Q}$
V_{IH}	V_{IL}	X	X	0	1
V_{IL}	V_{IH}	X	X	1	0
V_{IL}	V_{IL}	V_{IH}*	V_{IL}	0	1
V_{IL}	V_{IL}	V_{IH}*	V_{IH}	1	0

952859 – V_{IL} = 4.850 V
V_{IH} = -.810 V

MC10131 L – V_{IL} = -1.700 V
V_{IH} = -.900 V

V_{CC} = GND V_{EE} = -5.2 V

*MOMENTARILY APPLY V_{IL} THEN V_{IH}

Figure B17. ECL F/F Output Voltage (V_{OH}, V_{OL})

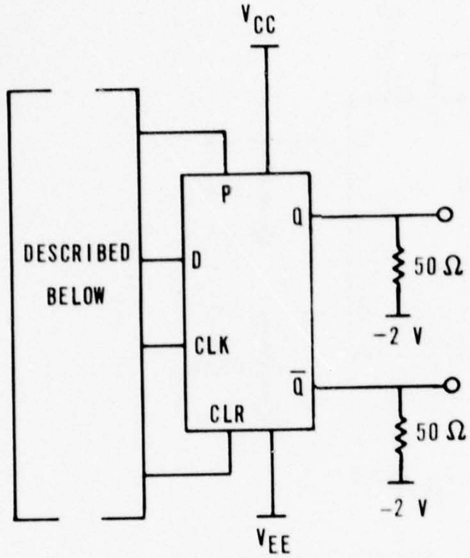


Figure 318. ECL F/F Current Measurements (I_{CC}, I_{IH}, I_{IL})

A. Measure Icc (Power Supply Current

1. All inputs and outputs open
2. Vcc = GND, Vee = 5.2v
3. Measure at Vee

B. Measure IIL (Input Low Current)

1. All inputs = VIL and outputs open.
2. Measure each input separately.
3. Vcc = GND, Vee = 5.2v

C. Measure IIH (Input High Current)

1. All inputs - VIH and outputs open.
2. Measure each input separately.
3. Vcc = GND, Vee = -5.2v

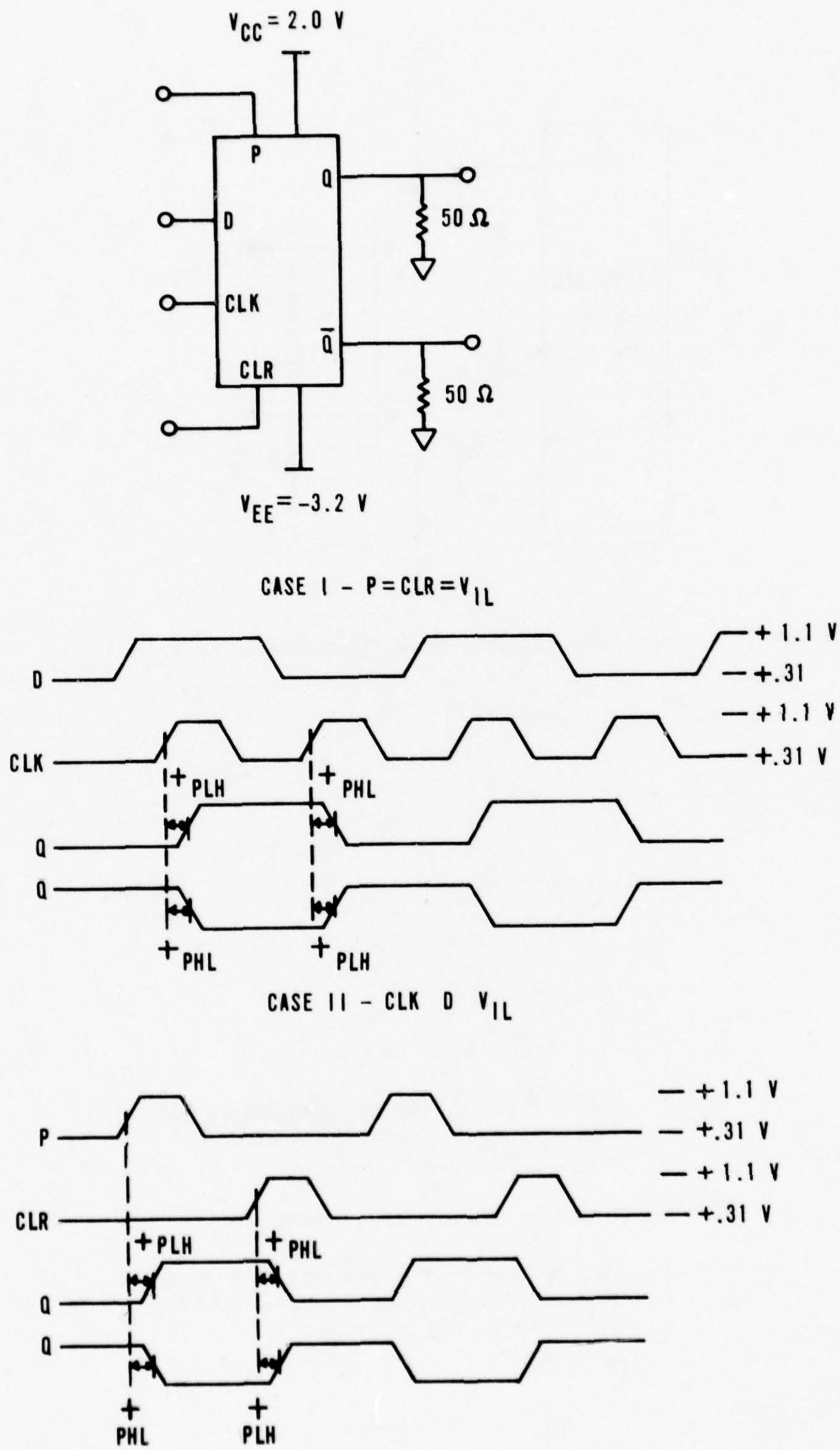


Figure B19. ECL F/F Propagation Delay Time (t_{PHL}, t_{PLH})

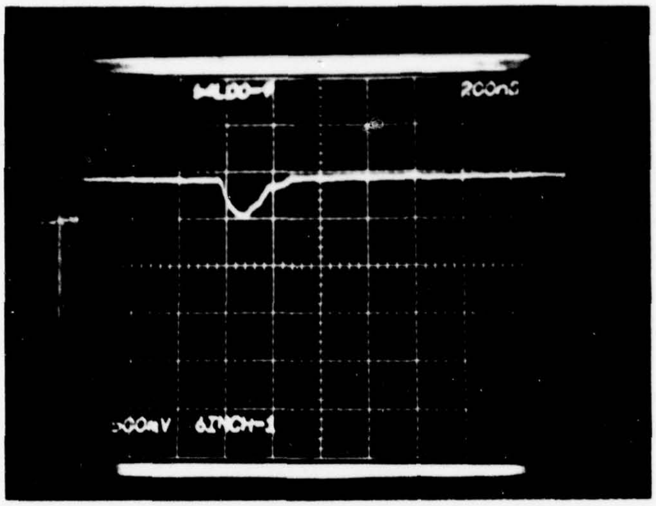
APPENDIX C

PHOTORESPONSE PHOTOGRAPHS

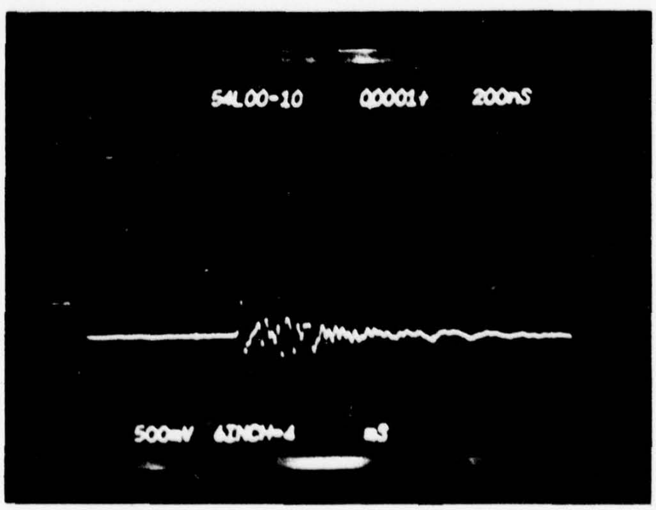
Figures C-1 through C-5 of this appendix illustrate the output photoresponse of the five TTL family NAND gates. These photographs illustrate characteristic dose-rate response of each TTL technology. As can be seen by these pictures, the Low Power and Low Power Schottky TTL technologies have a longer recovery time than the higher power Standard, High Speed and Schottky TTL technologies. The high current densities of the Standard, High Speed, and Schottky technologies more rapidly sweepout the hole-electron pairs generated during the transient radiation pulse.

Horizontal = 200 ns/div

Vertical = 0.5 v/div = 1 V div at the device



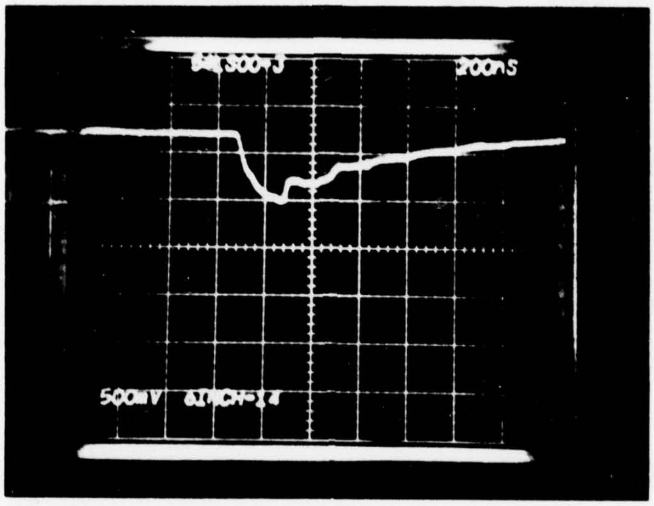
Output High Voltage (V_{OH})



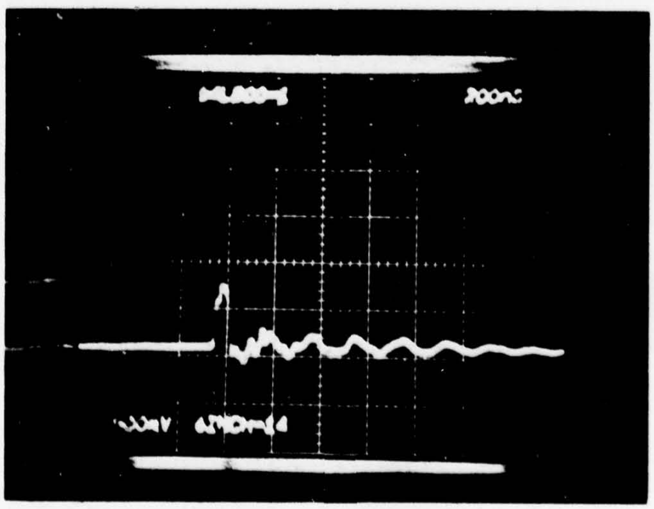
Output Low Voltage (V_{OL})

Figure C-1. TTL Low Power NAND Gate Photoresponse.

Horizontal = 200 ns/div
Vertical = 0.5 v/div = 1 V/div at the device



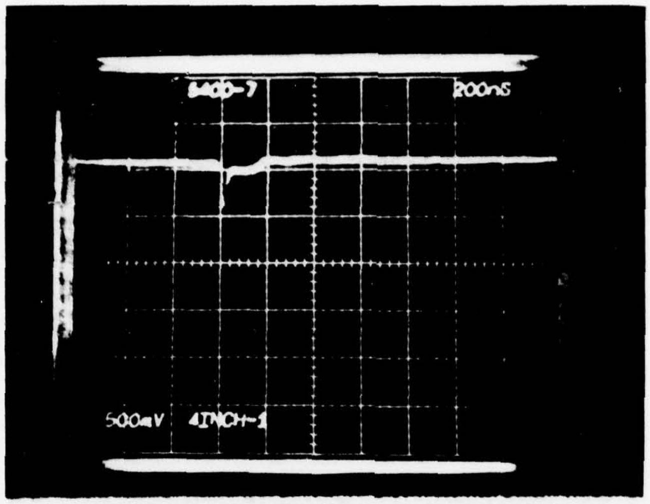
Output High Voltage (V_{OH})



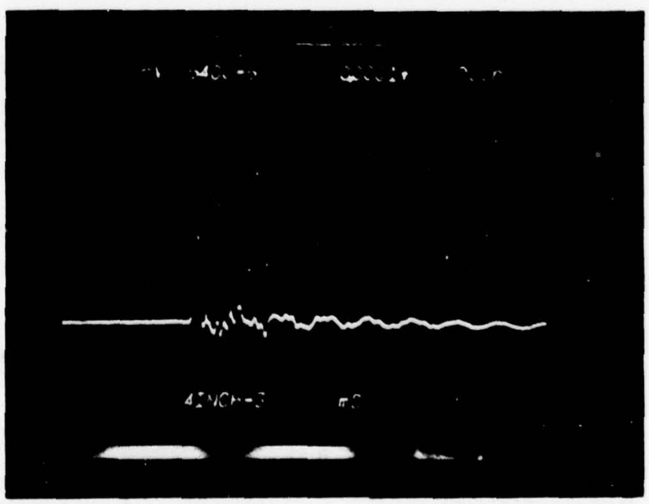
Output Low Voltage (V_{OL})

Figure C-2. TTL Low Power Schottky NAND Gate.

Horizontal = 200 ns/div
Vertical = 0.5V/div = 1V/div at the device



Output High Voltage (V_{OH})

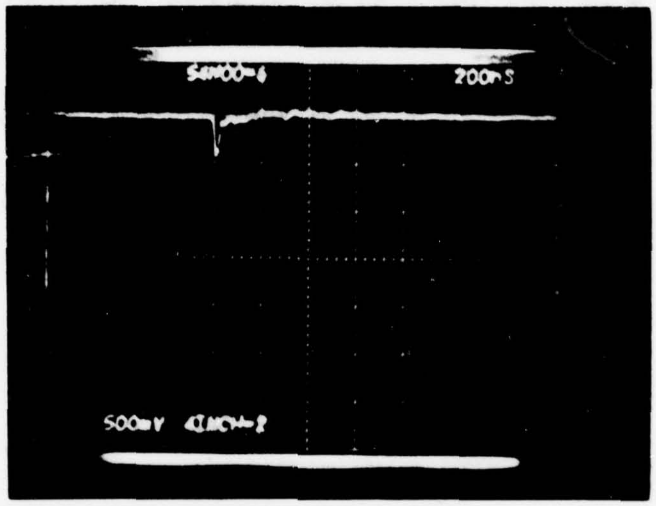


Output Low Voltage (V_{OL})

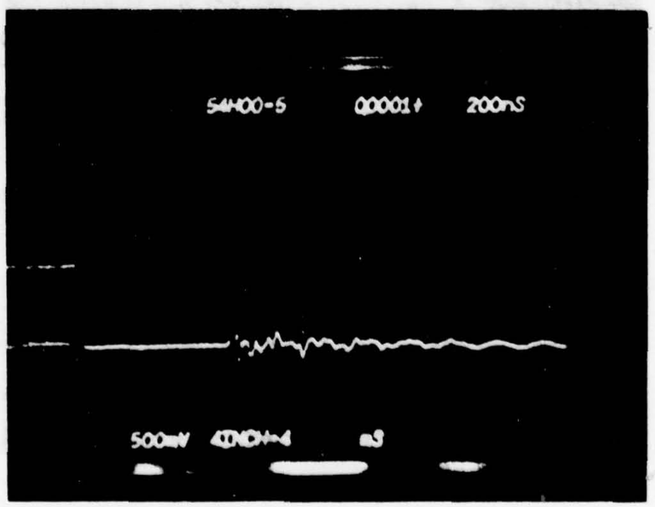
Figure C-3. TTL Standard NAND Gate Photoresponse

Horizontal = 200 ns/div

Vertical = 0.5 V/div = 1.V/div at the device



Output High Voltage (V_{OH})

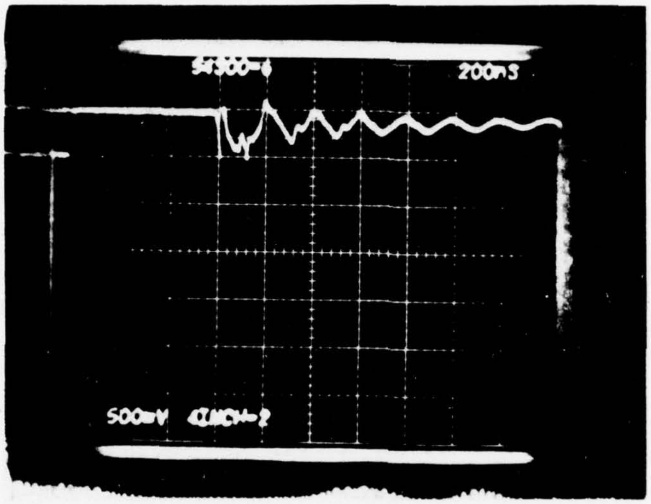


Output Low Voltage (V_{OL})

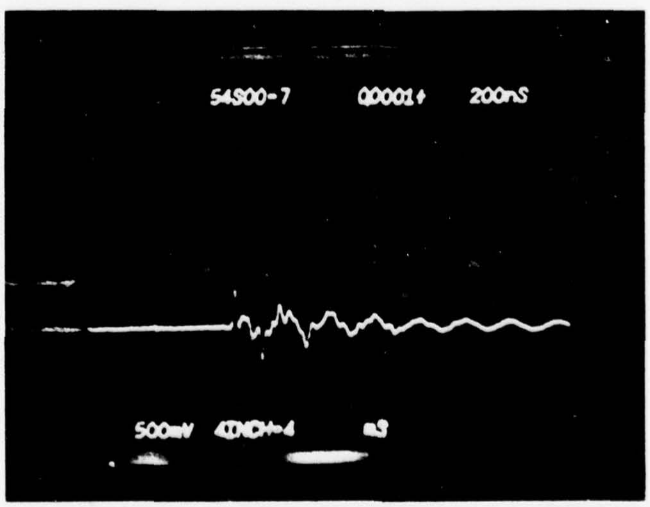
Figure C-4. TTL High Speed NAND Gate Photoresponse.

Horizontal = 200 ns/div

Vertical = 0.5 V/div = 1 V/div at the device



Output High Voltage (V_{OH})



Output Low Voltage (V_{OL})

Figure C-5. TTL Schottky NAND Gate Photoresponse.

APPENDIX D

NEUTRON FLUENCE TEST DATA

This appendix contains the test data gathered on each device exposed to the neutron fluence irradiation. The data resulted from the electrical tests performed on the Fairchild 5000 integrated circuit tester following each incremental neutron irradiation. The data are presented in tables illustrating the specific electrical parameter measurements for each cumulative neutron fluence level. The units for each cumulative neutron fluence level are n/cm^2. Each electrical parameter listed shows the worst case measurement for that parameter. For example, each SN5400J NAND gate packaged dip contains four NAND gates. Hence the SN 5400J output low voltage measurements (V_{OL}) shown on the table are the highest or worst case measurements of the four gates on that device. The Fairchild 5000 was not allowed to measure a voltage greater than 1.638 volts for the output low voltages of the TTL devices. However, this is sufficient since failure has already occurred at this point.

The measurements made on the SN54L00J devices do not include measurements made at 4.6×10^{14} n/cm^2 fluence level due to an error. However, measurements were made on the SN54L74J devices at this level. The measurements on the latter device showed that it failed at 4.6×10^{14} n/cm^2. Thus, these data indicate that the output failure threshold for the low power TTL technology lies between 1.4×10^{14} and 4.6×10^{14} n/cm^2. Also note that the ECL NOR gates were tested at only the higher neutron fluence levels. Since data had already been gathered on the ECL D flip-flops, time was saved by irradiating first at higher neutron fluences. The propagation delay time measurements shown on the tables are not valid for the cumulative neutron fluences at which the output voltages failed.

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE 950459

TEST		PRE RAD	.57E+15	1.0E+15
VOL	(VOLTS)	-1.661	-1.596	-1.528
VOH	(VOLTS)	- .9197	- .9776	-1.191
ICC	(MILLIAMPS)	52.92	47.21	39.83
I1L	(MILLIAMPS)	1.712	1.716	1.789
I1H	(MILLIAMPS)	2.195	2.510	2.792
TPHL	(NANOSEC)	4.12	2.97	1.05
TPHL	(NANOSEC)	3.70	2.42	1.97
TPLH	(NANOSEC)	3.80	3.90	*
TPLH	(NANOSEC)	3.77	3.72	*

* Measurements are not valid due to the shift in output voltage.

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE 950459

TEST		PRE RAD	.57E+15	1.0E+15
VOL	(VOLTS)	-1.688	-1.627	-1.559
VOH	(VOLTS)	- .9287	- .9776	-1.552
ICC	(MILLIAMPS)	48.07	43.80	37.82
I1L	(MILLIAMPS)	1.569	1.566	1.584
I1H	(MILLISMPS)	1.968	2.218	2.489
TPHL	(NANOSEC)	3.65	2.85	1.75
TPHL	(NANOSEC)	3.40	2.57	1.57
TPLH	(NANOSEC)	3.72	3.75	*
TPLH	(NANOSEC)	3.55	3.65	*

* Measurements are not valid due to the shift in output voltage.

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE 950459

TEST		PRE RAD	.57E+15	1.0E+15
VOL	(VOLTS)	-1.696	-1.581	-1.509
VOH	(VOLTS)	- .9233	-1.012	-1.305
ICC	(MILLIAMPS)	52.36	45.70	37.49
IIL	(MILLIAMPS)	1.772	1.769	1.973
IIH	(MILLIAMPS)	2.315	2.672	2.932
TPHL	(NANOSEC)	3.35	2.35	1.07
TPHL	(NANOSEC)	3.77	2.10	1.00
TPLH	(NANOSEC)	4.12	3.82	*
TPLH	(NANOSEC)	3.67	3.77	*

* Measurements are not valid due to the shift in output voltage.

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE MC10102L

TEST		PRE RAD	.57E+15	1.0E+15
VOL	(VOLTS)	-1.713	-1.690	-1.665
VOH	(VOLTS)	- .8993	- .9516	-1.117
ICC	(MILLIAMPS)	21.10	19.32	18.50
I1L	(MICROAMPS)	35.04	31.66	27.69
I1H	(MILLIAMPS)	.1426	.1623	.3066
TPHL	(NANOSEC)	3.00	2.60	2.50
TPHL	(NANOSEC)	2.80	2.45	2.00
TPLH	(NANOSEC)	1.00	1.25	1.60
TPLH	(NANOSEC)	1.00	1.40	1.90

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE MC10102L

TEST		PRE RAD	.57E+15	1.0E+15
VOL	(VOLTS)	-1.702	-1.672	-1.642
VOH	(VOLTS)	- .9310	-1.016	-1.1520
ICC	(MILLIAMPS)	20.82	19.12	18.38
IIL	(MICROAMPS)	70.45	65.50	61.28
IIH	(MILLIAMPS)	.1400	.2371	.3924
TPHL	(NANOSEC)	3.00	2.50	1.90
TPHL	(NANOSEC)	3.20	3.00	2.40
TPLH	(NANOSEC)	1.20	1.42	1.60
TPLH	(NANOSEC)	1.50	2.00	2.70

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE MC10102L

TEST		PRE RAD	.57E+15	1.07E+15
VOL	(VOLTS)	-1.732	-1.701	-1.640
VOH	(VOLTS)	- .9090	-1.010	-1.276
ICC	(MILLIAMPS)	20.97	19.50	18.37
I1L	(MICROAMPS)	38.99	35.63	31.51
I1H	(MILLIAMPS)	.1164	.2115	.3028
TPHL	(NANOSEC)	2.70	2.53	2.50
TPHL	(NANOSEC)	2.70	2.95	2.90
TPLH	(NANOSEC)	1.30	1.75	1.90
TPLH	(NANOSEC)	1.00	2.00	2.30

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN5400J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1496	.1505	.1696	.1972	.2733	1.6380
VOH (VOLTS)	3.234	3.233	3.212	3.197	3.145	3.126
ICC (MILLIAMPS)	5.00	5.00	4.99	4.96	4.92	4.86
IOS (MILLIAMPS)	38.60	38.56	37.72	37.04	25.57	18.12
IIL (MILLIAMPS)	1.130	1.129	1.124	1.120	1.104	1.089
IIH (MICROAMPS)	9.72	9.62	7.70	6.36	2.87	1.63
TPHL (NANOSEC)	5.22	5.35	5.62	5.47	7.62	8.82
TPHL (NANOSEC)	5.52	5.65	5.65	5.70	8.16	9.25
TPLH (NANOSEC)	14.85	14.90	13.12	12.40	11.2[illegible]	10.22
TPLH (NANOSEC)	14.75	14.80	13.30	12.05	11.55	10.60

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN5400J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1876	.1879	.2156	.2439	1.6380	1.6380
VOH (VOLTS)	3.163	3.162	3.125	3.113	3.036	3.009
ICC (MILLIAMPS)	4.62	4.62	4.60	4.59	4.53	4.46
IOS (MILLIAMPS)	35.99	35.98	34.49	33.28	15.0[illegible]	10.32
IIL (MILLIAMPS)	1.034	1.037	1.026	1.026	1.012	.989
IIH (MICROAMPS)	2.01	1.98	1.51	1.16	.32	.14
TPHL (NANOSEC)	6.87	6.82	7.47	7.57	12.57	15.25
TPHL (NANOSEC)	6.95	7.02	7.62	8.00	13.1[illegible]	16.75
TPLH (NANOSEC)	14.67	14.65	12.92	12.15	10.80	20.72
TPLH (NANOSEC)	14.70	14.42	12.90	11.85	11.15	20.72

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN5400J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1361	.1392	.1604	.1825	.3023	1.6380
VOH (VOLTS)	3.240	3.224	3.214	3.201	3.134	3.118
ICC (MILLIAMPS)	5.38	5.37	5.36	5.34	5.23	5.22
IOS (MILLIAMPS)	34.99	34.24	34.17	33.63	23.97	16.69
IIL (MILLIAMPS)	1.208	1.200	1.200	1.196	1.180	1.161
IIH (MICROAMPS)	12.07	11.64	9.06	7.07	2.58	1.31
TPHL (NANOSEC)	5.47	5.62	5.95	6.05	8.72	10.15
TPHL (NANOSEC)	5.55	6.07	6.22	6.05	9.02	10.82
TPLH (NANOSEC)	20.35	19.22	14.85	13.25	11.07	10.70
TPLH (NANOSEC)	20.42	18.77	14.85	13.22	11.40	10.70

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN5474J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2412	.2382	.2577	.2880	1.6380	1.6380
VOH (VOLTS)	3.271	3.241	3.224	3.232	3.155	3.150
ICC (MILLIAMPS)	20.55	20.51	20.45	20.36	20.07	19.76
IOS (MILLIAMPS)	36.29	36.09	35.03	31.22	17.95	12.87
IIL (MILLIAMPS)	4.531	4.518	4.504	4.491	4.438	4.389
IIH (MICROAMPS)	2.80	2.76	2.33	1.86	1.50	.48
TPHL (NSEC-CLOCK)	19.90	20.22	19.60	7.80	21.97	40.00
TPHL (NSEC-CLEAR)	24.95	25.15	24.52	25.30	28.02	40.00
TPLH (NSEC-CLOCK)	15.20	15.60	15.40	12.80	15.20	21.50
TPLH (NSEC-PRESET)	21.37	22.02	21.50	21.80	25.40	32.70

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN5474J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2647	.2676	.2816	.3124	1.6380	1.6380
VOH (VOLTS)	3.319	3.239	3.266	3.279	3.193	3.180
ICC (MILLIAMPS)	18.99	18.64	18.92	18.85	18.61	18.37
IOS (MILLIAMPS)	33.92	32.02	32.80	30.33	17.45	12.59
IIL (MILLIAMPS)	4.203	4.124	4.187	4.174	4.128	4.082
IIH (MICROAMPS)	2.20	2.12	1.90	1.61	1.40	.59
TPHL (NSEC-CLOCK)	20.00	19.80	18.92	15.50	21.70	40.00
TPHL (NSEC-CLEAR)	24.57	24.47	23.75	24.10	27.50	40.00
TPLH (NSEC-CLOCK)	14.60	14.70	14.50	11.10	14.90	21.30
TPLH (NSEC-PRESET)	20.57	21.10	20.67	21.00	24.50	29.30

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN5474J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2676	.2719	.2983	.3264	1.6380	1.6380
VOH (VOLTS)	3.247	3.224	3.195	3.206	3.098	3.089
ICC (MILLIAMPS)	20.10	20.05	19.96	19.91	19.53	19.29
IOS (MILLIAMPS)	34.87	34.64	33.12	27.88	14.40	10.25
IIL (MILLIAMPS)	4.402	4.392	4.374	4.368	4.309	4.253
IIH (MICROAMPS)	2.10	1.14	.96	.78	.50	.14
TPHL (NSEC-CLOCK)	19.70	19.40	19.40	16.60	22.70	40.00
TPHL (NSEC-CLEAR)	24.47	24.47	24.00	23.50	29.30	40.00
TPLH (NSEC-CLOCK)	13.90	14.40	14.10	10.60	15.10	28.40
TPLH (NSEC-PRESET)	21.17	20.40	19.90	21.40	26.40	34.80

MEASUREMENTS ON DEVICE NUMBER 1. DEVICE TYPE SN54L00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.73E+15
VOL (VOLTS)	.1635	.1641	.1927	.2304	1.6[illegible]83
VOH (VOLTS)	3.238	3.234	3.160	3.103	2.743
ICC (MILLIAMPS)	.65	.65	.64	.64	.6
IOS (MILLIAMPS)	10.71	10.51	6.01	4.09	.9
IIL (MILLIAMPS)	.150	.150	.149	.148	.163
IIH (MICROAMPS)	.36	.35	.26	.20	.0[illegible]
TPHL (NANOSEC)	35.20	35.30	38.97	41.82	60.92
TPHL (NANOSEC)	36.70	36.57	40.70	44.77	60.9[illegible]
TPLH (NANOSEC)	19.35	18.32	41.90	44.30	60.92
TPLH (NANOSEC)	19.20	19.10	40.20	44.50	60.9

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54L00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.73E+15
VOL (VOLTS)	.1533	.1544	.1771	.2015	1.6[illegible]80
VOH (VOLTS)	3.248	3.244	3.175	3.126	2.778
ICC (MILLIAMPS)	.44	.44	.44	.44	.4
IOS (MILLIAMPS)	9.11	9.10	7.05	4.94	1.1[illegible]
IIL (MILLIAMPS)	.103	.103	.102	.101	.0[illegible]7
IIH (MICROAMPS)	.48	.46	.37	.26	.1
TPHL (NANOSEC)	38.40	38.67	40.30	41.90	54.3[illegible]
TPHL (NANOSEC)	40.67	40.77	37.60	44.60	59.27
TPLH (NANOSEC)	22.60	20.37	13.37	41.90	60.0[illegible]
TPLH (NANOSEC)	22.60	20.70	14.22	42.60	60.0[illegible]

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN 4L00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.73E+15
VOL (VOLTS)	.1555	.1559	.1804	.2051	1.6[illegible]80
VOH (VOLTS)	3.255	3.251	3.179	3.126	2.752
ICC (MILLIAMPS)	.44	.44	.43	.43	.4[illegible]
IOS (MILLIAMPS)	8.99	8.96	7.40	5.05	1.11
IIL (MILLIAMPS)	.103	.102	.101	.101	.0[illegible]6
IIH (MICROAMPS)	.44	.42	.33	.28	.1[illegible]
TPHL (NANOSEC)	37.00	36.95	39.60	41.32	56.55
TPHL (NANOSEC)	36.42	38.77	41.40	44.30	60.70
TPLH (NANOSEC)	24.30	23.22	14.22	44.15	60.00
TPLH (NANOSEC)	24.50	22.50	13.70	44.80	60.00

MEASUREMENTS ON DEVICE NUMBER 1. DEVICE TYPE SN54L74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1728	.1712	.1889	.2083	1.6380	1.6380
VOH (VOLTS)	3.625	3.610	3.562	3.505	3.052	2.701
ICC (MILLIAMPS)	1.19	1.18	1.17	1.16	1.14	1.12
IOS (MILLIAMPS)	6.93	6.74	6.28	4.53	1.64	1.08
IIL (MILLIAMPS)	.296	.293	.292	.290	.286	.282
IIH (MICROAMPS)	.62	.61	.52	.44	.40	.16
TPHL (NSEC-CLOCK)	151.00	153.00	160.00	169.00	235.00	310.00
TPHL (NSEC-CLEAR)	112.00	113.00	118.00	123.00	243.00	850.00
TPLH (NSEC-CLOCK)	124.00	125.00	127.00	127.00	872.00	872.00
TPLH (NSEC-PRESET)	47.00	48.00	47.00	49.00	27.00	850.00

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54L74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1672	.1631	.1783	.1907	.9271	1.6380
VOH (VOLTS)	3.613	3.610	3.560	3.508	3.162	2.750
ICC (MILLIAMPS)	1.65	1.65	1.64	1.63	1.60	1.57
IOS (MILLIAMPS)	7.95	7.91	7.60	5.97	2.42	1.60
IIL (MILLIAMPS)	.396	.395	.393	.392	.385	.379
IIH (MICROAMPS)	1.50	1.38	1.26	1.15	.92	.55
TPHL (NSEC-CLOCK)	181.00	122.00	127.00	134.00	176.00	224.00
TPHL (NSEC-CLEAR)	90.00	92.00	94.00	102.00	133.00	708.00
TPLH (NSEC-CLOCK)	98.00	100.00	101.00	104.00	872.00	871.00
TPLH (NSEC-PRESET)	42.00	43.00	42.00	44.00	90.00	850.00

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN54L74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.1871	.1863	.2037	.2272	1.6380	1.6380
VOH (VOLTS)	3.645	3.644	3.572	3.502	3.055	2.675
ICC (MILLIAMPS)	1.12	1.12	1.11	1.10	1.04	1.06
IOS (MILLIAMPS)	6.17	6.12	5.74	4.19	1.60	1.07
IIL (MILLIAMPS)	.272	.270	.268	.267	.262	.257
IIH (MICROAMPS)	.41	.38	.32	.28	.22	.11
TPHL (NSEC-CLOCK)	147.00	148.00	154.00	165.00	231.00	850.00
TPHL (NSEC-CLEAR)	109.00	110.00	115.00	250.00	262.00	850.00
TPLH (NSEC-CLOCK)	126.00	128.00	127.00	300.00	872.00	850.00
TPLH (NSEC-PRESET)	48.00	46.00	47.00	47.00	232.00	850.00

MEASUREMENTS ON DEVICE NUMBER 1. DEVICE TYPE SN54H00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16
VOL (VOLTS)	.2619	.2627	.2819	.2863	.3465	.4584	1.6380
VOH (VOLTS)	3.119	3.116	3.092	3.090	3.049	3.029	2.978
ICC (MILLIAMPS)	11.25	11.26	11.16	11.13	10.98	10.85	10.71
IOS (MILLIAMPS)	51.60	51.91	51.28	50.89	51.24	55.71	55.61
IIL (MILLIAMPS)	1.453	1.453	1.438	1.438	1.419	1.405	1.381
IIH (MICROAMPS)	3.56	3.46	3.10	2.88	1.68	1.27	.59
TPHL (NANOSEC)	5.27	5.17	5.50	5.20	6.70	6.37	10.37
TPHL (NANOSEC)	5.40	5.55	5.60	5.55	6.95	6.72	11.30
TPLH (NANOSEC)	10.05	9.82	9.27	8.75	8.02	7.10	6.12
TPLH (NANOSEC)	10.05	9.90	9.35	8.80	8.60	7.33	6.27

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54H00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16
VOL (VOLTS)	.2343	.2360	.2481	.2601	.3197	1.2799	1.6383
VOH (VOLTS)	3.122	3.114	3.104	3.100	3.0[illegible]6	3.011	2.953
ICC (MILLIAMPS)	12.84	12.85	12.77	12.73	12.5[illegible]	12.40	12.20
IOS (MILLIAMPS)	50.27	50.59	49.96	49.56	49.8[illegible]	54.23	54.08
IIL (MILLIAMPS)	1.659	1.651	1.649	1.643	1.624	1.604	1.561
IIH (MICROAMPS)	5.16	5.05	4.46	3.99	1.9[illegible]	1.20	.39
TPHL (NANOSEC)	6.32	6.32	6.57	6.62	8.7[illegible]	8.50	14.05
TPHL (NANOSEC)	6.27	9.90	7.00	6.62	8.92	8.95	15.37
TPLH (NANOSEC)	10.12	10.15	9.70	9.20	8.47	7.57	8.30
TPLH (NANOSEC)	9.80	9.90	9.60	9.32	8.72	7.75	8.60

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN=4H00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16
VOL (VOLTS)	.2393	.2399	.2583	.2689	.3324	1.0285	1.6380
VOH (VOLTS)	3.120	3.119	3.076	3.091	3.040	3.025	2.966
ICC (MILLIAMPS)	11.25	11.27	11.13	11.14	11.00	10.87	10.71
IOS (MILLIAMPS)	51.49	51.81	51.17	50.81	51.13	55.57	55.45
IIL (MILLIAMPS)	1.448	1.451	1.424	1.435	1.420	1.404	1.367
IIH (MICROAMPS)	2.80	2.72	2.40	2.16	1.08	.73	.29
TPHL (NANOSEC)	5.27	5.22	5.60	5.42	7.10	6.87	11.50
TPHL (NANOSEC)	5.30	5.60	5.77	5.45	7.30	7.32	12.67
TPLH (NANOSEC)	9.82	9.80	9.17	8.77	7.75	7.10	7.52
TPLH (NANOSEC)	9.95	9.92	9.22	9.00	7.97	7.07	7.42

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN54H74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2399	.2392	.2495	.2695	.4321	1.6380
VOH (VOLTS)	2.938	2.905	2.882	2.882	2.819	2.520
ICC (MILLIAMPS)	32.73	32.67	32.59	32.44	31.80	51.73
IOS (MILLIAMPS)	63.01	62.84	62.21	61.45	58.60	56.29
IIL (MILLIAMPS)	5.607	5.602	5.604	5.606	5.587	5.553
IIH (MICROAMPS)	7.20	7.17	5.66	4.17	1.62	.33
TPHL (NSEC-CLOCK)	10.90	11.20	10.45	10.92	10.06	10.62
TPHL (NSEC-CLEAR)	22.37	22.32	21.95	22.70	24.82	38.20
TPLH (NSEC-CLOCK)	26.80	30.00	25.00	29.60	19.90	16.00
TPLH (NSEC-PRESET)	14.47	14.25	13.75	14.17	12.57	10.52

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54H74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2469	.2407	.2539	.2671	.3798	1.6380
VOH (VOLTS)	2.906	2.883	2.867	2.873	2.868	2.641
ICC (MILLIAMPS)	35.33	35.28	35.16	35.02	34.42	46.40
IOS (MILLIAMPS)	66.39	66.19	65.45	64.58	61.63	59.19
IIL (MILLIAMPS)	6.148	6.142	6.144	6.142	6.125	6.088
IIH (MICROAMPS)	14.00	8.97	7.33	5.85	1.91	.83
TPHL (NSEC-CLOCK)	9.90	9.95	9.62	10.37	9.02	9.10
TPHL (NSEC-CLEAR)	20.55	20.32	20.25	21.02	21.62	19.70
TPLH (NSEC-CLOCK)	26.20	24.00	27.40	27.60	17.50	14.60
TPLH (NSEC-PRESET)	14.25	14.00	13.52	14.57	12.80	8.87

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MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN54H74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2359	.2420	.2495	.2668	.4260	1.6380
VOH (VOLTS)	2.930	2.905	2.904	2.900	2.833	2.727
ICC (MILLIAMPS)	35.25	35.20	35.06	34.92	34.30	39.15
IOS (MILLIAMPS)	64.32	63.43	63.42	62.65	59.84	57.45
IIL (MILLIAMPS)	5.767	5.744	5.758	5.758	5.749	5.712
IIH (MICROAMPS)	14.00	9.54	7.99	6.45	2.81	1.04
TPHL (NSEC-CLOCK)	14.30	14.02	13.25	14.00	12.47	10.00
TPHL (NSEC-CLEAR)	20.92	20.80	20.42	22.15	22.25	20.00
TPLH (NSEC-CLOCK)	9.72	10.52	9.87	10.60	8.92	9.52
TPLH (NSEC-PRESET)	29.60	29.50	25.00	22.00	17.70	16.12

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN54S00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16	.20E+16
VOL (VOLTS)	.3999	.4027	.4152	.4166	.4[illegible]27	.4806	.5216	1.5000
VOH (VOLTS)	3.460	3.460	3.449	3.449	3.393	3.384	3.318	3.240
ICC (MILLIAMPS)	12.79	12.79	12.73	12.72	12.66	12.49	12.36	12.18
IOS (MILLIAMPS)	51.01	50.88	50.76	50.49	50.81	55.22	54.95	56.52
IIL (MILLIAMPS)	1.636	1.638	1.630	1.631	1.620	1.614	1.601	1.586
IIH (MICROAMPS)	.07	.09	.09	.08	.07	.09	.09	.07
TPHL (NANOSEC)	2.95	2.87	2.95	2.55	3.07	2.20	3.87	5.82
TPHL (NANOSEC)	3.32	3.12	3.22	3.00	3.51	2.65	3.80	6.40
TPLH (NANOSEC)	8.77	8.70	8.77	8.32	7.87	7.15	6.90	7.62
TPLH (NANOSEC)	9.22	8.72	8.62	8.42	8.12	7.22	6.80	7.65

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54S00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16	.20E+16
VOL (VOLTS)	.4167	.4185	.4344	.4368	.4400	.5116	.5846	1.6380
VOH (VOLTS)	3.442	3.422	3.415	3.430	3.363	3.344	3.256	3.164
ICC (MILLIAMPS)	13.09	13.08	13.01	13.02	12.87	12.74	12.60	12.38
IOS (MILLIAMPS)	50.67	50.54	50.41	50.13	50.3[illegible]	54.75	54.95	55.81
IIL (MILLIAMPS)	1.664	1.666	1.650	1.657	1.6[illegible]6	1.636	1.624	1.606
IIH (MICROAMPS)	.07	.05	.07	.09	.07	.09	.07	.07
TPHL (NANOSEC)	2.72	2.92	2.95	2.67	3.0[illegible]	2.27	3.87	7.22
TPHL (NANOSEC)	3.17	3.25	3.22	3.27	3.4[illegible]	2.67	3.80	7.57
TPLH (NANOSEC)	8.70	8.60	8.45	8.20	7.55	6.77	6.90	7.1[illegible]
TPLH (NANOSEC)	8.70	8.65	8.37	8.00	7.9[illegible]	6.95	6.80	7.22

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN54S00J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16	.20E+16
VOL (VOLTS)	.4144	.4195	.4302	.4367	.4[illegible]39	.5211	.5841	1.6380
VOH (VOLTS)	3.472	3.449	3.434	3.459	3.401	3.389	3.318	3.232
ICC (MILLIAMPS)	11.63	11.59	11.51	11.56	11.43	11.32	11.20	11.00
IOS (MILLIAMPS)	50.84	50.73	50.60	50.34	50.60	54.93	55.17	55.94
IIL (MILLIAMPS)	1.475	1.466	1.450	1.469	1.457	1.449	1.437	1.420
IIH (MICROAMPS)	.08	.08	.09	.11	.1[illegible]	.11	.10	.10
TPHL (NANOSEC)	3.05	3.07	3.07	2.72	3.10	2.50	3.62	6.32
TPHL (NANOSEC)	3.25	3.47	3.22	3.17	3.30	2.80	3.52	6.82
TPLH (NANOSEC)	8.97	8.80	8.52	8.17	7.92	7.17	6.85	7.32
TPLH (NANOSEC)	8.60	8.80	8.45	8.12	7.9[illegible]	7.00	6.90	7.25

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN54S74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16	.20E+16
VOL (VOLTS)	.4431	.4367	.4480	.4582	.5109	.5520	.6064	1.6380
VOH (VOLTS)	2.834	2.795	2.784	2.782	2.748	2.761	2.707	2.350
ICC (MILLIAMPS)	37.24	37.20	37.11	36.97	36.35	35.90	35.37	34.42
IOS (MILLIAMPS)	83.84	82.47	82.10	82.47	80.73	78.06	74.24	68.54
IIL (MILLIAMPS)	6.488	6.480	6.467	6.457	6.379	6.354	6.310	6.225
IIH (MICROAMPS)	.38	.37	.36	.28	.23	.16	.11	.10
TPHL (NSEC-CLOCK)	4.55	5.97	6.20	5.70	7.30	7.52	20.00	20.00
TPHL (NSEC-CLEAR)	13.57	13.30	13.27	14.75	14.15	11.52	6.22	9.65
TPLH (NSEC-CLOCK)	7.80	7.90	7.60	7.72	7.70	7.75	7.55	8.07
TPLH (NSEC-PRESET)	13.82	13.45	13.02	14.17	13.25	11.67	10.97	10.92

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54S74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15	.12E+16	.20E+16
VOL (VOLTS)	.4440	.4464	.4537	.4654	.5199	.5594	.6253	1.6380
VOH (VOLTS)	2.848	2.801	2.785	2.780	2.766	2.771	2.740	2.389
ICC (MILLIAMPS)	35.95	35.92	35.81	35.64	35.00	34.57	34.02	35.09
IOS (MILLIAMPS)	84.56	83.25	82.87	83.20	80.73	77.67	73.66	67.79
IIL (MILLIAMPS)	6.287	6.284	6.270	6.252	6.146	6.148	6.104	6.028
IIH (MICROAMPS)	.27	.26	.26	.23	.18	.13	.12	.10
TPHL (NSEC-CLOCK)	5.65	5.62	6.62	6.70	9.70	7.67	7.60	7.50
TPHL (NSEC-CLEAR)	13.92	13.72	13.65	14.65	14.27	12.65	6.42	12.72
TPLH (NSEC-CLOCK)	7.70	7.85	7.80	7.60	7.70	7.72	8.02	8.07
TPLH (NSEC-PRESET)	13.65	13.35	12.70	12.85	12.87	11.85	10.72	10.20

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN54LS00T

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.3245	.3259	.3411	.3647	1.6380	1.6380
VOH (VOLTS)	3.580	3.577	3.566	3.535	3.4[illegible]0	3.351
ICC (MILLIAMPS)	.66	.66	.65	.64	.62	.61
IOS (MILLIAMPS)	14.46	14.46	14.28	14.13	13.56	12.92
IIL (MILLIAMPS)	.159	.159	.157	.156	.151	.148
ITH (MICROAMPS)	.40	.39	.39	.39	.35	.32
TPHL (NANOSEC)	14.15	14.40	15.12	16.07	20.17	25.37
TPHL (NANOSEC)	13.70	13.82	14.72	15.75	20.0[illegible]	25.40
TPLH (NANOSEC)	16.92	16.92	17.07	17.32	18.42	19.90
TPLH (NANOSEC)	16.97	17.15	17.25	17.15	18.32	19.95

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54LS00T

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.3210	.3228	.3367	.3599	1.4930	1.6380
VOH (VOLTS)	3.591	3.580	3.577	3.547	3.475	3.388
ICC (MILLIAMPS)	.68	.68	.67	.67	.65	.63
IOS (MILLIAMPS)	14.59	14.59	14.44	14.29	13.77	13.19
IIL (MILLIAMPS)	.161	.162	.160	.159	.154	.150
IIH (MICROAMPS)	.03	.05	.06	.06	.07	.06
TPHL (NANOSEC)	14.25	14.15	14.77	15.82	18.95	23.87
TPHL (NANOSEC)	13.85	13.82	14.62	15.60	19.42	4.25
TPLH (NANOSEC)	17.00	16.70	16.57	17.12	18.10	19.35
TPLH (NANOSEC)	17.20	16.92	16.77	16.80	17.57	19.35

MEASUREMENTS ON DEVICE NUMBER 3. DEVICE TYPE SN54LS00T

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.3343	.3367	.3536	.3796	1.6380	1.6380
VOH (VOLTS)	3.582	3.578	3.564	3.532	3.439	3.341
ICC (MILLIAMPS)	.63	.64	.63	.62	.60	.59
IOS (MILLIAMPS)	14.27	14.28	14.14	13.99	13.40	12.79
IIL (MILLIAMPS)	.152	.153	.151	.150	.145	.142
IIH (MICROAMPS)	.06	.06	.06	.05	.05	.05
TPHL (NANOSEC)	14.47	14.70	15.52	16.35	20.90	26.60
TPHL (NANOSEC)	14.07	14.32	15.27	15.95	21.07	26.65
TPLH (NANOSEC)	17.65	17.32	17.67	17.65	18.90	20.67
TPLH (NANOSEC)	17.52	17.42	17.67	17.62	18.90	20.92

MEASUREMENTS ON DEVICE NUMBER 4, DEVICE TYPE SN54LS00T

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.3321	.3335	.3516	.3719	1.6380	1.6380
VOH (VOLTS)	3.569	3.564	3.547	3.524	3.428	3.318
ICC (MILLIAMPS)	.69	.70	.69	.68	.66	.65
IOS (MILLIAMPS)	14.80	14.80	14.63	14.51	13.86	13.12
IIL (MILLIAMPS)	.168	.169	.167	.166	.161	.157
IIH (MICROAMPS)	.03	.05	.03	.04	.05	.06
TPHL (NANOSEC)	14.20	14.42	14.92	16.11	20.12	26.15
TPHL (NANOSEC)	13.50	14.05	14.85	15.92	20.25	26.22
TPLH (NANOSEC)	16.85	16.52	16.70	16.52	18.35	19.95
TPLH (NANOSEC)	16.70	16.75	16.80	16.90	18.10	19.85

MEASUREMENTS ON DEVICE NUMBER 5, DEVICE TYPE SN54LS00T

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.3175	.3196	.3342	.3553	.8435	1.6380
VOH (VOLTS)	3.591	3.582	3.574	3.554	3.470	3.395
ICC (MILLIAMPS)	.70	.71	.70	.69	.68	.66
IOS (MILLIAMPS)	14.59	14.62	14.46	14.33	13.82	13.28
IIL (MILLIAMPS)	.168	.169	.166	.166	.161	.157
IIH (MICROAMPS)	.07	.04	.06	.06	.07	.07
TPHL (NANOSEC)	13.92	13.95	14.47	15.27	18.52	23.12
TPHL (NANOSEC)	13.32	13.40	14.10	15.05	18.45	23.52
TPLH (NANOSEC)	17.10	17.25	17.15	17.45	18.30	18.97
TPLH (NANOSEC)	17.52	17.35	17.50	17.02	17.72	19.42

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE SN54LS74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2647	.2800	.3191	.3709	1.6380	1.6380
VOH (VOLTS)	3.442	3.427	3.397	3.400	3.2[illegible]3	3.119
ICC (MILLIAMPS)	4.58	4.58	4.51	4.48	4.33	4.22
IOS (MILLIAMPS)	18.90	18.89	18.35	17.88	15.77	10.46
IIL (MILLIAMPS)	1.055	1.055	1.047	1.043	1.021	1.000
IIH (MICROAMPS)	.61	.60	.24	.19	.17	.15
TPHL (NSEC-CLOCK)	26.72	26.80	26.80	27.60	37.00	42.50
TPHL (NSEC-CLEAR)	32.57	32.32	31.90	34.47	45.40	55.00
TPLH (NSEC-CLOCK)	22.30	20.40	18.90	19.70	28.20	33.00
TPLH (NSEC-PRESET)	27.30	26.60	23.80	24.00	26.60	27.47

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE SN54LS74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2800	.2924	.3332	.3845	1.6380	1.6380
VOH (VOLTS)	3.439	3.425	3.393	3.391	3.253	3.116
ICC (MILLIAMPS)	4.55	4.55	4.49	4.46	4.32	4.21
IOS (MILLIAMPS)	17.67	17.64	17.13	16.68	14.57	10.13
IIL (MILLIAMPS)	1.039	1.039	1.036	1.035	1.017	.996
IIH (MICROAMPS)	.62	.57	.47	.39	.29	.15
TPHL (NSEC-CLOCK)	27.85	27.40	26.17	27.10	35.90	43.80
TPHL (NSEC-CLEAR)	32.75	32.82	34.60	34.27	43.90	55.57
TPLH (NSEC-CLOCK)	23.60	21.60	19.00	19.10	27.80	32.32
TPLH (NSEC-PRESET)	27.60	28.30	24.50	25.30	26.70	27.00

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE SN54LS74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2390	.2509	.2778	.3107	1.6380	1.6380
VOH (VOLTS)	3.466	3.455	3.428	3.441	3.365	3.316
ICC (MILLIAMPS)	4.60	4.59	4.55	4.50	4.3[illegible]	4.27
IOS (MILLIAMPS)	17.34	17.32	16.77	16.38	14.75	13.78
IIL (MILLIAMPS)	1.017	1.017	1.017	1.016	1.007	.983
IIH (MICROAMPS)	1.50	1.38	1.29	1.14	1.10	.61
TPHL (NSEC-CLOCK)	26.10	26.15	25.60	26.05	31.50	36.25
TPHL (NSEC-CLEAR)	33.62	33.80	32.55	33.62	29.02	43.00
TPLH (NSEC-CLOCK)	23.50	22.50	20.70	20.70	24.10	29.70
TPLH (NSEC-PRESET)	28.90	28.30	25.20	24.80	25.50	25.82

MEASUREMENTS ON DEVICE NUMBER 4, DEVICE TYPE SN54LS74J

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	.2392	.2485	.2747	.3089	1.6380	1.6380
VOH (VOLTS)	3.466	3.448	3.427	3.434	3.375	3.321
ICC (MILLIAMPS)	4.62	4.62	4.56	4.53	4.40	4.28
IOS (MILLIAMPS)	17.30	17.27	16.74	16.32	14.68	13.70
IIL (MILLIAMPS)	1.024	1.026	1.022	1.025	1.018	.996
IIH (MICROAMPS)	.32	.27	1.25	1.07	.96	.58
TPHL (NSEC-CLOCK)	23.00	21.50	19.30	18.30	22.90	28.60
TPHL (NSEC-CLEAR)	32.10	32.00	31.15	33.95	38.20	42.20
TPLH (NSEC-CLOCK)	24.72	24.30	23.30	24.10	30.70	35.02
TPLH (NSEC-PRESET)	28.30	28.10	25.40	25.20	25.90	25.75

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE 952859

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.732	-1.747	-1.733	-1.708	-1.647	-1.525
VOH (VOLTS)	-.939	-.955	-.960	-.954	-.971	-.991
ICC (MILLIAMPS)	71.53	71.13	69.69	69.24	67.50	60.48
IIL (MILLIAMPS)	1.81	1.81	1.80	1.82	1.83	1.86
IIH (MILLIAMPS)	2.25	2.25	2.25	2.27	2.30	2.40
TPHL (NSEC-CLOCK)	3.75	3.15	3.32	3.55	2.27	1.70
TPHL (NSEC-CLEAR)	3.60	3.95	3.97	4.02	3.07	2.42
TPLH (NSEC-CLOCK)	4.02	4.42	4.40	4.37	3.45	2.28
TPLH (NSEC-PRESET)	7.52	4.82	4.62	5.62	3.85	2.97

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE 95[illegible]859

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.740	-1.736	-1.718	-1.684	-1.592	-1.434
VOH (VOLTS)	-.943	-.956	-.963	-.974	-.995	-1.058
ICC (MILLIAMPS)	65.69	63.16	61.70	60.68	61.1[illegible]	48.96
IIL (MILLIAMPS)	1.83	1.77	1.77	1.79	1.84	1.91
IIH (MILLIAMPS)	2.28	2.20	2.21	2.24	2.33	2.48
TPHL (NSEC-CLOCK)	3.67	3.52	3.60	4.05	2.45	1.52
TPHL (NSEC-CLEAR)	4.20	4.10	4.10	4.20	2.85	4.00
TPLH (NSEC-CLOCK)	4.60	4.62	4.35	4.25	2.70	1.80
TPLH (NSEC-PRESET)	5.42	5.40	4.72	4.55	3.2[illegible]	3.07

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MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE 952859

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.745	-1.734	-1.716	-1.681	-1.599	-1.438
VOH (VOLTS)	-.958	-.957	-.960	-.964	-.988	-1.044
ICC (MILLIAMPS)	66.43	64.96	63.75	63.53	63.47	51.16
IIL (MILLIAMPS)	1.79	1.83	1.84	1.86	1.82	1.96
IIH (MILLIAMPS)	1.99	2.29	2.30	2.33	2.39	2.55
TPHL (NSEC-CLOCK)	4.32	3.37	3.50	3.67	2.32	1.42
TPHL (NSEC-CLEAR)	4.10	3.75	3.95	4.02	2.75	1.30
TPLH (NSEC-CLOCK)	4.62	4.72	4.42	4.37	2.77	1.65
TPLH (NSEC-PRESET)	5.30	5.02	4.67	4.50	3.32	2.20

MEASUREMENTS ON DEVICE NUMBER 1, DEVICE TYPE MC10131L

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.753	-1.753	-1.753	-1.717	-1.662	-1.592
VOH (VOLTS)	-.866	-.873	-.906	-.907	-.909	-1.056
ICC (MILLIAMPS)	35.94	35.71	34.50	34.22	32.53	31.09
IIL (MICROAMPS)	16.00	16.37	27.50	39.18	75.22	133.02
IIH (MILLIAMPS)	.02	.02	.03	.05	.10	.12
TPHL (NSEC-CLOCK)	3.35	2.57	3.12	4.05	2.62	2.32
TPHL (NSEC-CLEAR)	3.35	3.67	3.92	4.65	3.72	3.27
TPLH (NSEC-CLOCK)	5.65	5.70	5.07	5.17	4.23	3.65
TPLH (NSEC-PRESET)	5.52	5.30	5.17	5.32	3.95	3.67

MEASUREMENTS ON DEVICE NUMBER 2, DEVICE TYPE MC10131L

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.759	-1.760	-1.759	-1.727	-1.653	-1.608
VOH (VOLTS)	-.870	-.873	-.913	-.919	-.990	-1.115
ICC (MILLIAMPS)	35.71	35.48	34.28	34.00	32.0[illegible]	30.90
IIL (MICROAMPS)	18.82	19.82	30.41	41.23	70.3[illegible]	131.15
IIH (MILLIAMPS)	.02	.02	.03	.04	.0[illegible]	.11
TPHL (NSEC-CLOCK)	2.87	2.70	3.50	3.87	2.45	2.30
TPHL (NSEC-CLEAR)	3.32	3.87	4.00	4.75	3.4[illegible]	3.32
TPLH (NSEC-CLOCK)	5.72	5.75	5.35	5.17	4.15	3.77
TPLH (NSEC-PRESET)	5.86	5.35	5.40	5.40	4.0[illegible]	3.80

MEASUREMENTS ON DEVICE NUMBER 3, DEVICE TYPE MC10131L

TEST	PRE RAD	.28E+13	.69E+14	.14E+15	.46E+15	.73E+15
VOL (VOLTS)	-1.721	-1.721	-1.713	-1.679	-1.606	-1.557
VOH (VOLTS)	-.912	-.917	-.954	-.967	-1.068	-1.130
ICC (MILLIAMPS)	36.97	36.77	35.40	34.96	32.53	30.73
IIL (MICROAMPS)	60.65	62.56	77.06	93.83	150.68	239.86
IIH (MILLIAMPS)	.08	.08	.09	.11	.17	.21
TPHL (NSEC-CLOCK)	3.17	3.02	3.60	4.22	2.72	2.20
TPHL (NSEC-CLEAR)	3.42	3.67	3.50	4.72	3.75	3.10
TPLH (NSEC-CLOCK)	5.52	5.60	5.40	5.12	4.07	3.25
TPLH (NSEC-PRESET)	5.47	5.47	5.37	5.27	4.42	3.42

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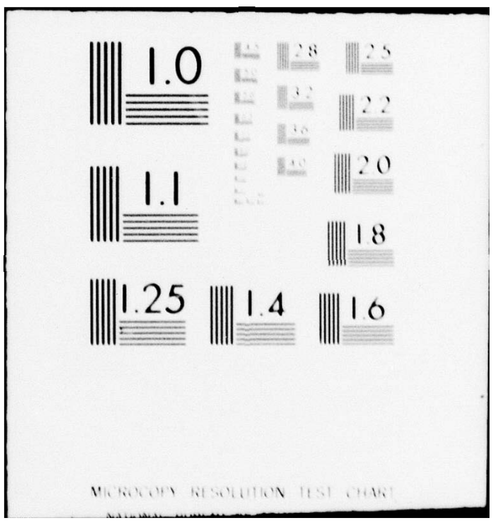
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