AD-A056 179 TELEPHONICS HUNTINGTON N Y F/G 17/2
RECOMMENDED DESIGN APPROACH OF GENERAL PURPOSE MULTIPLEX SYSTEM--ETC(U)
1977 N62269-76-C-0394

UNCLASSIFIED NL

1 OF 2
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LEVEL II

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CORPORATION

15 N62269-76-C-Ø394

1977

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PHASE I REPORT
RECOMMENDED DESIGN APPROACH OF GENERAL PURPOSE MULTIPLEX SYSTEM (GPMS) ADVANCED DEVELOPMENT MODEL.

Phase I Report.

11 1977

12 151p.

PREPARED BY TELEPHONICS
FOR
U.S. NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PA.

GPMS
ADVANCED DEVELOPMENT MODEL
RECOMMENDED
DESIGN APPROACH

CONTRACT #N62269-76-C-0394
NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PA.

[redacted]

1977

Telephonics

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* In Text

INTRODUCTION

This document describes the Telephonics design approach for the Advanced Development Model of the GPMS Multiplex Terminal (MT). It summarizes and describes the results of the System Definition Phase (Phase A) of the job and represents the information presented and the decisions agreed to at the Design Briefing, held at Telephonics on 11/21/77 and 11/22/77.

The "GPMS Recommended Design Approach" is submitted in accordance with the GPMS SOW and Data Item #UDI-S-90505.

SECTION 1.0

PROGRAM OVERVIEW

1.1 HISTORY

The evolution of the GPMS design is summarized in the following chart:

GPMS - X	GPMS - II	GPMS ADM
• 3 Data Terminals	• 3 Polling Terminals	• 1 MUX Terminal
• 1 CCU	• 2 CCU's	• 1 CCU
• 2 "IM's" per DT	• 8 IM's	• 6 IM's
• 4 IM address capacity	• 16 IM address capacity	• 16 IM address capacity
• 2 data busses (Ports)	• 4 data busses (Ports)	• 4 busses (Ports)
• 1 control bus	• No separate control bus	• No separate control channel
• Blocking	• Non-blocking	• Non-blocking
• Hard-wired "processing"	• Special purpose ONL and general purpose OFL (two languages).	• Same general purpose machine for ONL & OFL (software allocates tasks).
• No standard DT/IM interface	• Standard DT/IM interface	• Standard DT/IM interface
• Lab environment	• Lab environment	• Flightworthy Design/fab.
• Polling Contention only	• P.C./1553A *compatible*	• Environmentally qualified
• New peripheral requires hardware changes in "front end" logic. New IM.	• New peripheral requires software changes in both ONL and OFL. NO hardware mods other than new IM.	• PC/1553A compatible
• Dedicated IM Card Slots.	• Universal IM Card Slots.	• New peripheral requires change in OFL software only. No hardware mods other than new IM.
		• Universal IM Card Slots.

1.2 GOALS

The goals of the ADM program are listed below. They are the result of both customer requirements and Telephonics system analysis of desirable and/or essential features.

- FLIGHTWORTHY, QUALIFIED TERMINAL DESIGN
- GPMS & 1553A COMPATIBLE
- PER MIL-G-85013(AS), PRELIMINARY
- * MODULAR DESIGN
- * NON-BLOCKING CAPABILITY
- * 4 PORTS
- * 270V D.C. PRIMARY POWER
- * STAND-ALONE DT OPERATION

* RESULT OF SYSTEM ANALYSIS

1.3 CONSTRAINTS

The external constraints imposed upon the ADM design are listed below.

- "MINIMUM" SIZE, WEIGHT, POWER
- MIL-STD-883 & MIL-S-19500 FOR ELECTRONIC COMPONENTS *
- FLIGHTWORTHY DESIGN (QUAL TEST PER MIL-STD-810C):
  - TEMP/ALT: METHOD 504.1, PROC. I, CAT. 6 (-62°C to +95°C; SL to 70,000 FT.)
  - SHOCK: METHOD 516.2; PROC. III, FIG. 516.2-1 (CRASH SAFETY FOR FLIGHT VEHICLE EQUIPMENT)
  - VIBRATION: METHOD 514.2, FIG. 514.2-2 (AS MODIFIED BY SOW)
- EMI PER MIL-STD-461: METHOD RS03 (AS MODIFIED BY SOW)

* WHERE FEASIBLE

SECTION 2.0

DESIGN OVERVIEW

2.1 SYSTEM & TERMINAL BLOCK DIAGRAMS

A typical GPMS system configuration is shown in figure 1, and a terminal (MT) block diagram in figure 2.

2.2 MECHANICAL LAYOUTS

A layout of the ADM MT box and a typical PC card are attached as part of Appendix 1.

2.3 TEMP/ALT PARTITIONING

Thermal analysis (see sec. 3.7.4) indicates the necessity for the following operating schedule.

2.3.1 SL TO 35,000 FEET

a) No external cooling air required.

b) Fan circulates air at cabin ambient.

c) Fan is outside basic box envelope.

d) Typical of LAMPS helicopter and A7 operation.

2.3.2 35,000 TO 70,000 FEET

a) External cooling air @ 3.4 lbs/min/KW required.

b) Typical of F18 and B1 operation.

2.3.3 QUALIFICATION TESTING PER ABOVE PARTITIONING

a) For tests up to and including 35,000 feet chamber air is circulated by fan.

b) For tests from 35,000 through 70,000 feet conditioned air is piped to the unit in the chamber.

SECTION 3.0

DETAIL DISCUSSION

SECTION 3.1

DESIGN CONSIDERATIONS

3.1.1 DESIGN GOALS

- GPMS should be partitioned into 3 inique functional modules.
- GPMS partitioning should lead to a set of "modular" building blocks.
- GPMS should have the capability to meet present as well as future system requirements.
- Changes in future system requirements should be accomplished by reprogramming of the protocol routines rather than hardware changes.
- One unique design should be simultaneously capable of operating in Polling Contention, Command Response and Bus Control Interface Unit Modes.
- GPMS partitioning should allow implementation of Blocking or Non-Blocking system configurations.
- GPMS Modules should be capable of operation in Remote Terminal or "stand alone" (smart peripheral) applications.
- GPMS Modules should be capable of implementing the Cable Control Unit (CCU) for Polling Contention systems.

3.1.2 GPMS DESIGN APPROACH

- GPMS has been partitioned into 3 unique modules.
- The system-analysis and resulting redesign effort on the GPMS has resulted in three modules which form a basic set of system building blocks.
- The modules are capable of operation as part of a Remote Terminal or as a "stand alone" unit.
- The modules have firmware programmable protocol routines.
- Future changes to MIL-STD-1553 or MIL-G-85013 (AS) will be accomodated by reprogramming the ONL Module. No hardware redesign is required.
- The GPMS system accomodates imminent changes to MIL-STD-1553A such as Broadcast mode and the accept-reject status word for Dynamic Bus Allocation.
- The Port module can be used as the "front end" of the Cable Control Unit (CCU) for Polling Contention systems.

3.1.3 BLOCKING VS. NON BLOCKING OPERATION

A. BLOCKING TERMINAL DEFINITION

In a multi data bus system, the remote terminal shall transmit and receive messages on only one data bus at a time. If the remote terminal receives a valid command word on a previously unused data bus, it shall immediately terminate operation on the current data bus and respond to the command on the new data bus. Communication will continue on this data bus until a valid command word is received on another data bus or until completion.

B. NON BLOCKING TERMINAL DEFINITION

In a multi data bus system, the remote terminal shall transmit and receive messages on all data busses (up to a maximum of four) simultaneously. Each data bus shall be capable of responding to valid command words and transmitting and receiving messages irrespective of data traffic on the other data busses communicating with the remote terminal.

C. ANALYSIS

The GPMS-ADM design is modular, and therefore, capable of operation in either the blocking or non-blocking mode. Considerable savings in size and weight can be realized by utilizing the blocking, rather than the non-blocking configuration. It is not necessary to make the design conform to either exclusively since both are available via the modular design.

3.1.4 MODULAR SYSTEM APPROACH

Based on system functional requirements, appropriate tradeoffs between blocking and non-blocking systems can be made. Block diagrams of both the blocking and non-blocking system are shown in Figures 3 and 4 respectively. It should be pointed out at the outset that while the non-blocking system offers increased system versatility and higher data bandwidths, it does impose the penalties of increased cost and size. An approximate idea of the relative real estate and relative cost of various system configurations (exclusive of interface modules) in both blocking and non-blocking modes is shown in Table 3-1 of the SEM, Phase I report.

The block diagrams (Figure 3 and Figure 4) reveal the major difference between the blocking and non-blocking systems. The blocking system consists of a "dumb" port electronics module with the "smarts" for protocol contained in a single central processor (ONL). On the other hand, the non-blocking system consists of a "dumb" port electronics module and processor (ONL module) for each channel (i.e. distributed processing) each of which is capable of doing 1553 command response or MIL-G-85013(AS) polling-contention protocol routines.

From this discussion, it becomes obvious that a desirable system approach would require that the Port and ONL processor modules be of identical designs for both the blocking and non-blocking modes. In this manner, reconfiguring a system (or designing a new system) would involve a minimum amount of change.

A blocking system would consist of the desired number of Port modules along with a processor module. A non-blocking system would consist of a different number and mix of the identical component modules. System logistics, maintainability and cost would be minimized. Therefore, Telephonics has developed a fully modular GPMS system design. New GPMS systems can be implemented with a suitable mix of the standard GPMS modules. The modular standard GPMS modules will allow blocking systems to be implemented without having to carry the additional size and cost burden of non-blocking capability.

This modular design allows the use of the three unique modules to configure the following systems:

- 1, 2, 3 or 4 Port Non-Blocking
- 1, 2, 3, or 4 Port Blocking
- Remote Terminal
- Stand Alone
- CCU

3.1.5 LSI

3.1.5.1. PORT

LSI has the inherent advantage of saving valuable real estate while simultaneously decreasing maintainability and logistics costs. In the case of standard LSI, reduced costs can sometimes be realized. Custom LSI becomes cost effective only for large volume requirements or where system size requirements dictate its use.

After careful consideration, it was determined that the only area where LSI seemed feasible was the Manchester Encoder/Decoder. A standard CMOS/SOS LSI chip is available from Harris Semiconductor. Analysis of the remaining functions on the Port module revealed that it would be impractical to use present day custom LSI technology for these functions. The remaining functions can be divided into two groups: 1) Standard MSI chips and 2) Random logic SSI chips. Each of the MSI chips has high functional density and, as a consequence, generates a relatively large amount of heat. It was determined that concentrating these functions in an LSI chip would cause a reliability problem due to the large concentration of heat producing elements in such a small volume. This group of chips may lend itself to a custom LSI when the CMOS/SOS technology comes of age. This technology promises to allow high speed operation of CMOS circuits which were previously frequency limited. The CMOS circuits are inherently low power devices. Therefore, CMOS/SOS technology combines high density, high speed and low power. The Harris

Manchester Encoder/Decoder CMOS/SOS LSI is an example of the advantages of this new technology .

3.1.5.2 ONL/OFL

Where possible, standard LSI integrated circuits have been used. The decision against using custom LSI at this time was predicated on the present state of the art in that field. The problem of high heat concentrations reducing reliability has been previously discussed. Again, when CMOS/SOS technology becomes available to the custom LSI market, some of the MSI functions might be effectively condensed into an LSI integrated circuit.

3.1.6 SEM

The developers of current and future aircraft have a need for standard input/output modules for use on avionic equipments. These modules would simplify maintenance and reduce the initial cost of avionics. Such modules would also provide the basic components necessary to build unique terminals for armament systems, avionics systems, and other special applications. The impact of SEM upon this terminal development would impact future versions of the F-18 and F-16 programs.

The SEM program's prime objective is the definition, design, and packaging study of electronic functions that can be utilized in a variety of applications. Standardization of the GPMS terminal modules for utilization in a wide variety of avionic equipments and armament considerations are important candidates for SEM. Therefore, this study program was initiated to define the GPMS current advanced development multiplex terminal model. In addition, the initial phase of the program investigated various technologies, packaging concepts and compared all known criteria against such requirements as size, weight, cost, thermal properties, power, reliability, and vulnerability characteristics. A projection of the impact of future technology on the proposed SEM modules was also investigated. A comprehensive analysis was conducted, based on the afore mentioned criteria, to establish optimum SEM designs.

In line with the SEM program objectives an intital analysis of the current GPMS system was conducted. SEM requirements for flexibility, versatility, and applicability to current, as well as, future system applications guided this (ADM) design. Careful attention to systems analysis insured that GPMS - ADM would not only be capable of forming the basic building blocks for all current multiplex Data Bus Systems, but also have the flexibility to satisfy future system requirements. At the conclusion of the design phase, a partition analysis was made to insure that the SEM modules would form "modular" building blocks for avionics system designers. The resulting three GPMS modules meet all the primary requirements of the SEM program.

A detailed discussion of the SEM concept and philosophy may be found by referring to the SEM, Phase I report.

SECTION 3.2

THEORY OF OPERATION

3.2.1 BUS CONTROL UNIT (BCU)

Operation of the BCU is described by the flow chart shown in Figure 5.

3.2.2 MULTIPLEX TERMINAL (MT)

The MT is divided into two major functional blocks. They are the "front end" or DT (Data Terminal), which consists of the Port and Processor (CPU) cards, and the Interface Module (IM) section. The DT is the multi-channel communication link with the MUX bus system while the IM's provide the interfaces to the various peripheral devices. The transfer of data and controls between the DT section and each IM is accomplished via a "standard" interface circuit so that each IM is designed with the same circuitry for intra-MT communication. This interface is described in section 3.3.1.

The Port module (card) design is based on the use of the "Harris chip" (HR3209) which is a MOS circuit that performs individual word checks (receive and transmit) to detect sync, count bits check and generate parity, and format conversion. In general, the Port performs the following functions:

- Serial/Parallel - Parallel/Serial Data Conversion.
- Word Level Testing i.e. Parity, Manchester Coding...Etc.
- Terminal Address Recognition.
- Processor Interrupt After Valid Command.
- Excess Transmission Turn-Off

The basis of the Processor design is the Advanced Micro Devices AM2901 microprocessor. A unique feature of this device is its microprogrammability. The following excerpt from the AMD Microprogramming Handbook * succinctly summarizes the operation and advantages of this technique:

"Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental microoperations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinguished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered and more organized with regard to the control function field. In its simplest definition, a microprogram control unit consists of the micro-program memory and the structure required to determine the address of the next microinstruction".

A2901 chip is a "four bit slice" of a processor. Therefore, two of these chips, in cascade, are used to make up the eight bit processor required for the ADM MT function. Refer to Figure 7. The 2901 is the Arithmetic Logic Unit (ALU), performing the necessary processing functions under the control of 48 bit micro-instructions contained in the "uP Control Store" memory. The 2910 (uP Program Controller) contains the program counter which advances the uP Control Store after each instruction is accomplished. Part of the micro-instruction (5 bits) is fed back to the 2910 to control its mext action on each step (increment or jump).

* AMD Microprogramming Handbook & AM2910 Emulation by John R. Mick & Jim Brick; 2nd Edition; 1977.

Each CPU section operates in either one of two major modes. When not occupied with main MUX line activity the CPU falls back to off-line (OFL) processing, the major task being to scan IM's for service requests and load the Bus Service Request (BSR) File (FIFO) as they occur. This is needed in a polling contention system only. Since OFL activity is non-real-time the hardware used exclusively for this activity is shared by all processors. The (Central) Memory/Timing card contains a PROM which lists the OFL macro-instructions for each CPU.

A macro-instruction is read out of the memory via the IM Data Bus,mapped to a u Control PROM starting location by the Mapping PROM and then steered to the Program Counter in the 2910 which causes the processor to perform the routine. This goes on continuously until an interrupt occurs. An interrupt is generated by the Port as the result of either a command word when operating as a Command Response (CR) system or a poll when functioning in a Polling Contention (PC) configuration.

In the PC mode a match of the Terminal Address field information in a Bus Control Unit (BCU) bus offer causes the Port to generate the Port Interrupt Vector (PIV) word (seven bits) which is converted in the Mapping PROM to the starting address of the Poll Response (ONL) macro. When operating in the CR mode the same type of terminal address match together with Subaddress/Mode and Word Count information is used to generate a PIV containing sufficient intelligence to yield the appropriate macro starting address (in the uP Control Store) and the designation of the referenced IM when converted in the Mapping PROM. It should be noted that this second type of command word (and resultant PIV) also occurs in the PC mode after a terminal has accepted the offered MUX cable to set up a communication link with a second MT. Some of the distinctive characteristics of the ADM MT and its CPU design are as follows:

a) Terminal design is modular i.e. many system configurations are possible.

b) Terminal can be configured as a blocking or non-blocking system.

c) Manchester protocol can be Command/Response or Polling/Contention.

d) Processor is micro programmable for flexibility.

e) Even though high speed is required, power has been minimized using lower power Schottky devices.

f) Box size has been minimized by use of high density IC's, multilayer boards, and micro processor design techniques.

g) Software requirements are minimized by having a single processor design and micro level instructions.

h) High speed u processor capable of bus formatting and IM routines.

i) Processor can service more than one Port in a blocking configuration.

j) Architecture is general purpose.

k) 2901/2910 offer flexible data and program control.

The Central Memory/Timing module (Mem/Tim) is a single card containing the functions which are shared by all processor sections. Refer to Figure 8. The "Bus Service Request" (BSR) file is a FIFO memory which is used to store the service request flags from the IM's. It is loaded during OFL processing and is used by all CPU's during PC polls for peripheral servicing.

The PROM (1K x 8) stores the OFL macro-instructions which specify the OFL processing for the processors. The RAM (256 x 8) is a temporary scratchpad with miscellaneous functions. The "Reject Reply" register produces a canned cable rejection response when required by one of the CPU's. The "Board Status" register circuit maintains a performance status word (for all boards) which is transmitted on demand.

Communication between the Mem/Tim elements and the CPU's is via the same standard interface used by the IM's and described in section 3.3.1. Summarizing its features we have:

a) Standard IM Interface

b) Contains Polling Contention/Dynamic Bus Allocation Bus Service Requests.

c) Macro instructions are stored in PROM.

d) RAM provides large scratch pad.

e) Real time counter for long time outs.

f) Master clock source for processors.

SECTION 3.3

IM DESIGN

3.3.1 DEFINITION OF STANDARD INTERFACE

Information transfer between Data Terminal and IM's.

1) Data will be transferred between IM's and DT via the 8 bit data bus, using two 8 bit bytes per message.

2) Data Terminal will provide all the control signals to IM's via the 16 bit address bus, plus a Read, Write and VA (Valid Address) control signal. The Read signal is sent by the DT to acquire data from the IM. The Write signal is used to input data to the IM. The Valid Address signal is used to inhibit data and address bus receivers and decoders during address changes in order to prevent excessive switching currents during that time.

3) ADDRESS FORMAT

A15	A11		A7 A6	A0	
E/I	IM ADDRESS	SUB ADDRESS	BYTE ID	BYTE COUNT	FROM PROC TO IM.

A7 A6
- 00 = Data Valid
- 01 = Data Invalid
- 10 = Status
- 11 = Command

From diagram, A15 is external or internal storage i.e., IM's and their associated memory are external. On-Line/ Off-Line processor memory is internal. A14 - A8 is a a 7 bit message code containing a 4 bit IM address and a 3 bit sub address. A7 and A6 are used for byte identification as follows:

00 = Data Valid which states that the information DT received from the MUX bus is correct with respect to parity and quantity.

01 = Data Invalid. This means that the IM has a choice as to whether to disregard the message or possibly generate a character which signifies that an error was present.

10 = Status is a request for IM Status (such as IM busy) to be sent from IM on the Data Bus to the DT and then to the MUX bus if A5 is concurrently logic "1". If A5 = logic "0" the status information was only necessary for internal use.

The format of the data bus signal during a Status Request in shown below in two forms:

A. IM STATUS

```
              BUSY                      From IM      (when A5 on address
   "0"       ----------------           to PROC.      bus is logic 0.)
 If idle    | 1 0 0 0 0 0 0 0 |
             ----------------
              BYTE 0
```

B. BUS STATUS

```
                                       BUSY      (when A5 on address
Format of     ----------------------------------      bus is logic 1).
IM contri-  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 |
bution to     ----------------------------------     From IM
PROC. Bus          BYTE 0            BYTE 1          to PROC.
Status Word.
```

The first form is IM Status Request. This occurs when A5 of the address bus is logic 0. The IM then outputs a byte 0, as shown, onto the data bus. This is for internal use only and is transmitted to the MUX bus. The second form occurs when a Bus Status Request (A5 of address bus = logic 1), is made causing the two data bytes as shown above to be outputted by the IM onto the data bus.

11 = When A7 and A6 are 11, this signifies a command. Used in conjunction with A1 through A5 these commands initiate action in the IM's.

A5 through A1 are used in conjunction with the Byte ID bits to provide byte count in the case where data is being transferred; type of Status (internal or external)p all the different commands for the IM's; and Built In Test Control.

Bit A0 determines whether byte 0 or byte 1 of data is being applies to the DB. The first byte transferred, B0, always contains the most significant bits.

SAMPLE WORD FORMATS

BYTE ID

00 = DATA VALID

01 = DATA INVLAID

10 = STATUS

11 = COMMAND

From PROC. to IM.

E/I — BYTE 1/BYTE 0

1/0	IM #	MESSAGE #	BYTE ID	BYTE COUNT	1/0

INT add Bus gene request form.

A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

A/D STATUS

1/	X X X X	10	1/0	/0

Sample o above.

$\overline{A5}$ MEANS STATUS NEED NOT GO ON MUX BUS (ONLY INT. USE).

ANALOG IM COMMAND

1/	X X X X	0 1 0	1 1	1/0	

INT. Adc Bus (Sam

ANALOG INPUT CHANNEL

"1" TAKE IN ANALOG SIG. ON CHAN. 010.

"1"=SET MUX LATCH. "0"=CLEAR" "

A/D COMMAND

A8 A7 A6 A5

1/	X X X X	1 1	ON/OFF

INT. Adc Bus (Sam

A8 and A6 and A7 and WRITE = SAMPLE CMD.

A9 and A6 and A7 and READ = PUT B0 THEN B1 ON DB.

A6 and A7 and A5 and READ = GIVES BIT.

3.3.2 IM DESIGN CONSIDERATIONS

3.3.2.1 A/D IM (Refer to Fig. 9)

An investigation of the available A/D converters revealed that accuracy and speed force the price and size upwards. Although A/D converters have become smaller and more economical in recent years, they have not reached the point where it would be practical for each analog channel to have its own A/D converter. Currently, reasonably priced 12 bit A/D converters, in the 2 to $300 range, are about 2" x 4" x .5" in size. Hybrids are becoming available and are smaller; approximately 1 3/4" x 1 1/8" x 1/4", but still as costly. Thus the decision to use a central A/D board in stead of distributed A/D's was made.

A 12 bit hybrid manufactured by Analog Devices was selected for the Central A/D. Since a variety of DC and AC signals will have to be digitized in the system a sample and hold is necessary to provide the A/D with stable information for a period long enough for A/D conversion. The sample and hold, also manufactured by Analog Devices, was selected to the compatible with the 12 bit A/D. It will be capable of acquiring a time varying or DC signal in 6 usec. to within .01% accuracy. The Aperture Time jitter (uncertainty), ta, is given as 15 nanoseconds. This jitter causes the sample to have amplitude variations, referred to as "aperture error". The definition is:

$AE = ta \frac{dv}{dt}$ where $\frac{dv}{dt}$ is the slope of the input signal.

If the input signal is 400 Hz: $V = E \sin WT$

$$\frac{dv}{dt} = EW \cos Wt = EW,$$

since Cos WT = 1 at the 0 voltage crossing point which is the fastest rise time of a sine wave.

$$Ae = 15 \times 10^{-9} \times 10 \times 2 \times \pi \times 400$$

$$Ae = 3.769 \times 10^{-4} \quad (0.38 \text{ mv.})$$

Since ½ LSB = 2.5mv it is seen that the possible Aperture Error that can occur during the acquisition of a 400 Hz sine wave is negligible .

The A/D board is set up such that the voltage droop that appears on the sample and hold output capacitor will be minimized because the A to D conversion takes place as soon as the "hold" mode of the sample and hold has stabilized. This is desireable because the voltage on the hold capacitor at this time would be within ½ LSB of the input voltage to the sample and hold and therefore provide minimal error in the signal voltage to be converted. Once the conversion is complete the digitized signal is automatically fed to an output latch which is applied to the data bus upon a command.

3.3.2.2 ANALOG IM (Refer to Fig. 10)

The analog IM is actually two IM's on the same board. One will be used to channel subscriber equipment signals through an analog multiplexer onto the analog bus which connects to the A/D input. The other will receive and convert digital information from the data bus to analog values, pass it through a demultiplexer and place the analog information in to hold circuitry long enough to be used by the subscriber to which it was sent.

OP-12 operational amplifiers manufactured by PMI were selected as the channel input buffers. They are configured to receive differential analog signals while at the same time minimizing the effects due to input offset voltage and current. Their input offset voltage is typically 0.4 mv over the full military temperature range which along with other excellent parameters insure minimal error over a wide range of operating temperatures.

The DG 508A multiplexer has a maximum "on" resistance of 500 ohms. The offset error produced by this resistance is dependant on leakage current through the "on" switch into the seven other off switches plus the current into the A/D sample and hold. The leakage current plus the sample and hold input current is approximately 0.8 ua. Therefore the offset voltage due to current flowing through the on resistance of the multiplexer = $[.5 \times 10^{-6} + .33 \times 10^{-6}] \times 500 = .415$ mv. which is much less than ½ LSB and therefore suitable for this application.

The selection of the D/A converter was based on trade offs between physical size, accuracy, cost, speed and power consumption. The National DA 1200 comes in a dual width DIP package, is low in cost, has a setting time ofless than 2.5 usec, low power consumption and ½ LSB linearity, thereby making it a good choice.

The output of the D/A converter is conditioned through an operational amplifier, demultiplexed through a differential multiplexer and fed to sample and hold storage circuitry. To minimize the gain and offset errors caused by these three series elements, the final output is fed back and compared to the output of the D/A at the input to the operational amplifier. Since the op-amp is configured as a unity gain follower, the final output will closely approximate the D/A output voltage ± the op-amp offset error.

3.3.2.3 SYNCHRO TO DIGITAL IM (Refer to Fig. 11)

Certain trades offs were considered concerning the decision to "make or buy" the S/D converter. Purchaseable units are available from several sources. They have excellent accuracy and can operate over the full military temperature range. Unfortunately all are costly and physically large. Since the ADM system contains a central A/D board a "make" decision was logical to avoid having redundant functions in the system. In other words, the S/D converter must also make an analog to digital conversion. Using the central A/D in conjunction with simultaneous sampling of the sine and cosine outputs of a Scott-T input, 3 wire, angular information.

An error analysis revealed the necessity of maintaining the sine to cosine ratio throughout the D/S and S/D conversion. Using only cosine information would result in large errors at the "0" crossing point. Using the tangent of the angle (Sine/Cosine) should result in better than 0.1% accuracy.

3.3.2.4 UHF - (SERIAL) DATA IM (Refer to Fig. 12)

Data bus and address bus interfaces present low loading to busses because all data bus interfaces are presented through 7833 party line transceivers. No other tri-state devices are connected directly to the data bus from the IM.

Read, Write, and Address enables from the microprocessors are differential for noise cancellation.

Low power Schottky devices are used where possible to lower power consumption while maintaining speed.

Latches which contain frequency data will only be updated during the time when the UHF radio is not requesting this data.

The UHF Radio clocks in the frequency information from the IM at a rate of 800 HZ. There are 24 clock pulses followed by a dead space of 8 clock times. This occurs continuously. The information is held in three 8 bit latches. The 24 clock pulses cause a scan of the latches to occur. This information is fed out serially to the radio. The latches are updated by the computer during the 8 clock time dead space which lasts for about 10 milliseconds. During this same dead time the latches will be read back with the computer for the purposes of BIT. This information can be compared with the data which went to the latches as a test of performance.

3.3.2.5 SOSTEL IM (Refer to Fig. 13)

Each Current Source has an address designated by bits Ao to A5 on the computer address bus. Bit Do of the data bus controls the on-off information for the addressed current source. A "Write" pulse is issued and that current source responds by following Bit Do providing the op code 00 was used on the address bus.

To read a particular current source, one must address that current source and use an op code of "01". A write pulse is then issued which starts a 50 usecond test pulsein all current sources. At the end of the test pulse, the addressed current source is read with the A/D coding circuit.

It is then necessary to issue a read pulse together with a data message. The coded voltage information will then be applied to the data bus so that the computer can absorb it.

The data bit which directs the on-off information is fed back to the computer on the data bus along with the coded voltage information to provide BIT.

3.3.2.6 TACAN IM

The original requirement called for an IM to control the AN/ARN-84 TACAN (see Figure 14). At the design briefing Telephonics was directed by NADC to replace this with an IM to drive the discrete controls on the UHF (ARC 159) radio. A block diagram of this latter Interface Module is shown in Figure 15.

SECTION 3.4

SOFTWARE REQUIREMENTS

3.4 SOFTWARE REQUIREMENTS

3.4.1 INTERNAL PROCESSOR

3.4.1.1 FEATURES OF INTERNAL PROCESSOR

- Combined OFL and ONL into one processor (ONL/OFL)
- Only 1 programming language to master
- ONL program fixed.
- OFL changes as IM's change
- User uses macro instruction rather than micro instruction programming.
- Macro instructions increase flexibility
- Use of macro instructions leads to less complex programming requirements.
- Emulation of partial instruction set of popular microprocessors (i.e. 8080 etc.)

3.4.1.2 TYPICAL ONL PROGRAMS

- Response to Poll
- External initiated receive data
- External initiated transmit data
- Internal initiated receive data
- Internal initiated transmit data
- BCIU (Capture)
- Receive - No data
- Transmit - No data
- Broadcast

3.4.1.3 TYPICAL OFL PROGRAMS

- Power on reset
- Bus service request routines
- Self test routines
- Data manipulation routines

3.4.2 SUPPORT

- Hand encoding of microcode (not required by user)
- Possible use of assembler for macro instruction.

SECTION 3.5

BIT

3.5 BIT ANALYSIS

3.5.1 PHILOSOPHY

3.5.1.1 ONL/OFL processor will test non processor functions and update terminal flag as required.

3.5.1.2 Computer will test ONL/OFL processor

3.5.2 DESIGN APPROACH

3.5.2.1 TYPES OF TESTING

a) Computer initiated test of processor

b) ONL/OFL self test of functions while in progress

c) ONL/OFL self test of functions using pseudo data.

3.5.2.2 TEST ANALYSIS OF FUNCTIONAL GROUPS

a) Port

- Wrap around test by ONL/OFL processor during normal operation.

b) ONL/OFL

- Test by external computer
  - Send message
  - Retrieve manipulated message

c) Central Timing

- PROM's
  - OFL read and compare pseudo data
- Scratch Pad RAM's
  - OFL write and read pseudo data
- Bus service request file
  - ONL/OFL test during normal operation

d) <u>IM's</u>

- Digital

  - ONL/OFL test during normal operation (wrap around test)

- Analog

  - ONL/OFL test write and read pseudo data

SECTION 3.6

POWER SUPPLY DESIGN

3.6 POWER SUPPLY DESIGN

As previously stated switching type power supplies are the most desirable to use in systems having high current and moderately stringent regulation requirements. As seen from the figure 18, the power bus feeds a bridge power oscillator in series with a regulator circuit. The multitapped outputs of the oscillator are full wave rectified and filtered to provide the various low voltage requirements of the ADM system. An isolated output of the power oscillator provides the feedback voltage to control the series regulator, maintaining the output voltages constant, as the load conditions, and input line voltage varies. Power return and system ground are thus kept isolated.

Regulation of from 1-2% on the 5 volt output, and 0.1% on the low current outputs should be achievable using this configuration.

Output short circuit protection is accomplished as follows: An output short on any supply causes a collapse in the flux field of the power oscillator transformer thereby eliminating the necessary feedback to maintain oscillation. This automatically reduces the output current to a negligible level.

A 50ms storage capacity which enables the power supply to continue normal operation for a 50ms loss of input power, is included in the design.

3.6.1 POWER ALLOCATION

	POWER IN WATTS				
BOARD	+5	+15	-12	+15	-15
PORT 1	5.45	4.16	0.6		
* PROCESSOR 1	18.0				
PORT 2	5.45	4.16	0.6		
* PROCESSOR 2	18.0				
PORT 3	5.45	4.16	0.6		
* PROCESSOR 3	18.0				
PORT 4	5.45	4.16	0.6		
* PROCESSOR 4	18.0				
A/D IM	2.5			0.06	0.6
ANALOG IM	5.0			1.08	1.02
S/D IM	2.0			0.02	0.165
SOSTEL IM	5.0	1.7			0.33
UHF IM DATA	5.0	.03			.04
UHF DIS IM	5.0	.03			.04
MEM/TIM	6.25				
TOTAL	124.6	18.4	2.4	1.16	2.195

* Two cards.

3.6.2 CENTRAL VERSUS DISTRIBUTED

Distributed power supply systems are used primarily when a high degree of regulation at a given point is required. This tends to reduce ground loop problems due to different IR drops on the power lines to each of the system modules.

Using today's technology, highly regulated power supplies are no longer required and the relatively constant nature of logic type loads places the stress on the line regulation capabilities of the supply. In the ADM system almost 90% of the power is consumed by the 5 volt logic. Based on the preceding the decision to go to a central power supply system followed. The most critical voltages, ± 15V used for the A/D converter, will be highly regulated at the central supply. The minimal current requirement of less the 0.2 amps will produce negligible IR drops in the power lines to the A/D thereby making A/D on board regulation unnecessary.

3.6.3 USE OF 270 VOLTS

The use of 270 volt DC power on the aircraft offers many advantages starting from basic power generation and ending with the size and type of component used in the system power supply.

Generation of 270 VDC requires generators which are smaller, lighter and far less complex than equivalent 400 Hz. generators. Switching to redundant back up power in a DC system is readily accomplished through the use of a diode as compared to far more complex systems required for AC power back up.

The trend in present day technology is toward higher packaging density thereby requiring greater efficiency and smaller volume in power supplies. This has led to the increased use of switching type regulated power supplies which in turn enhance the use of DC input power thereby eliminating the need for input rectification.

SECTION 3.7

MECHANICAL PACKAGING DESIGN

3.7.1 BOX DESIGN

The transfer of heat out of the box is the primary problem in the mechanical design. Heat is transferred from the components on each PC card through a metal overlay which is in direct contact with the card clamps mounted to the box walls. The box is of hollow wall construction with Kintex corrugated filler which allows free passage of air to carry the heat from the side-walls to the outside ambient. As stated in section 2.3 a fan will used to provide the necessary air-flow when the box is to be used at altitudes up to 30,000 feet. Between 30,000 and 70,000 feet (the upper specification limit) the unit will rely on ECS air supplied at the rate of 3.4 #/min/KW.

The package is divided into two major compartments; namely a card area, which occupies approximately two thirds of the box with the remaining third for the power supply. The dividing wall between the two compartments forms a plenum which allows cooling air to flow over the finned, power supply heat sink to which are mounted that unit's high power dissipation components.

The cards plug into connectors on a backplane and signals and power are communicated by front panel mounted connectors as follows:

QTY	# PINS	FUNCTION
1	6	Power
4	98	IM/Peripheral Communication
4	TWINAX	MUX Bus

The backplane will be constructed as a metal-phenolic-metal "sandwich" with one metal plate serving as the five volt bus and the other as the ground plane. This technique is being used to ensure the maximum five volt and ground conduction path areas (minimum resistance) as well as minimizing the inductance presented to the high frequency signals existent in the box. A drawing package is included as Appendix 1.

3.7.2 PC CARD CONFIGURATION

The printed circuit card dimensions are approximately 5 x 7 with approximately 34 square inches of useful area. Thermal analysis indicates the need for metal overlays on each card to transfer heat generated by the IC's to the air-cooled side-walls via the card guides. A typical card layout is included as part of Appendix 1.

3.7.3 WEIGHT ESTIMATE

NAME	WGT. EST. LBS.
Side Walls (2)	3.3
Back Plane (1)	2.45
Backplane Angles (2)	.12
Front Panel	.96
Handles (2)	.32
Connector I/O	.32
Covers Top & Bottom	.96
P.S. Estimate	7.00
Large Caps (4)	1.2
Wiring	3.0
PC Cards (19)	7.41
Rear Cover	.28
Card Guides (28)	.90
Misc. Hardware	1.5
TOTAL -	30 lbs.

3.7.4 THERMAL CONSIDERATIONS

A four part thermal analysis was performed which is summarized below. The complete analysis is included as Appendix 2.

SUMMARY OF THERMAL ANALYSIS:

Assuming a total of 300 watts dissipated in the box, four analyses were conducted as follows. An ambient air temperature of 71°C was used for the calculations.

a) Using a fan and maintaining the 3/4 ATR box size, what is the maximum operating altitude?

FAN RPM	AIR FLOW(CFM)	TEMP. P.S. H.S. (°C)	MAX.ALT.(FT)
13,000	65	100	30,000
19,000	95	103	50,000
22,500	105	110	55,000

As can be seen from the figures in the table there is very little to be gained in attempting to move from the 19,000 rpm to the 22,500 rpm fan, and, inasmuch as this last is available only as an AC unit its use is ruled out.

b) How much bigger (than 3/4 ATR) must box grow in order to meet the 70,000 foot altitude with all other parameters held constant? An increase of one inch in box width yields the following:

FAN RPM	AIRFLOW(CFM)	TEMP. P.S. H.S. (°C)	MAX.ALT.(FT)
13,000	150	78 (LIM)	S.L.
22,000	175	78 (LIM)	S.L.
22,000	175	105	70,000

The first two conditions listed allow no operation above sea level pressure. Allowing a heat sink temperature of 105°C raises the operating ceiling to 70,000 feet, but the fan required is available with an AC motor only, making it unsuitable for ADM use.

c) Keeping the configuration described in a) what are the allowable power dissipation levels for operation from sea level to 70,000 feet?

FAN CFM	MAX. DISS. (W)
65	116
95	170
105	188

The relatively low (compared to the box design) allowable power levels are a result of the 70,000 foot altitude requirement. Obviously, full spec operation is impossible without some special provisions.

d) Is operation up to an altitude of 70,000 feet possible if 90°F ECS air is supplied at a rate of 3.4 lbs/min/KW? This portion of the analysis yielded a power supply heat sink temperature of 79°C indicating satisfactory operation.

Therefore, the conclusions were to provide a .050" inch thermal overlay on each PC card, utilize a fan for operation up to 30,000 feet and use aircraft (ECS) $90^{o}F$ forced air for system operation up to 70,000 foot altitude. The fan assembly is detachable from the basic 3/4 ATR box envelope.

SECTION 4.0

RELIABILITY & MAINTAINABILITY

4.1 MTBF

An MTBF for the MT has been calculated using the failure rate data in MIL-HDBK-217B and an Airborne Inhabited, 50°C environment.

Assuming a series reliability model, the resulting calculated MTBF is 2376 hours. Refer to Table 4.1 for the failure rate of each sub-assembly.

While this figure indicates the hardware MTBF of the entire box, it does not accurately reflect the reliability of the design. When operating in the GPMS mode, a failure in the circuitry of one of the four channels (i.e. Port or CPU 1, 2) would not incapacitate the MT, but only shift the load normally handled by that channel to the others. Therefore, throughput rate might be affected, but box operations would continue. Only one of the four port/CPU channels must operate to allow mission success.

There are two areas where a failure would disable the entire box. They are the Power Supply and the Memory/Timing PC board. The design of both the Power Supply and Memory and Timing circuits has taken into account their system criticality and has minimized failures within these functions to the maximum extent possible.

In determining the mission success of the ADM, a reliability model indicated in Figure 4.1 was developed. This model uses a typical I/M (SOSTEL) with a failure rate of 17.28 failures per million hours.

The resulting probability of mission success for a two hour mission is .99991.

The calculated mission success clearly substantiates the actual reliability of the ADM by demonstrating the probabilistic ability to perform the intended function.

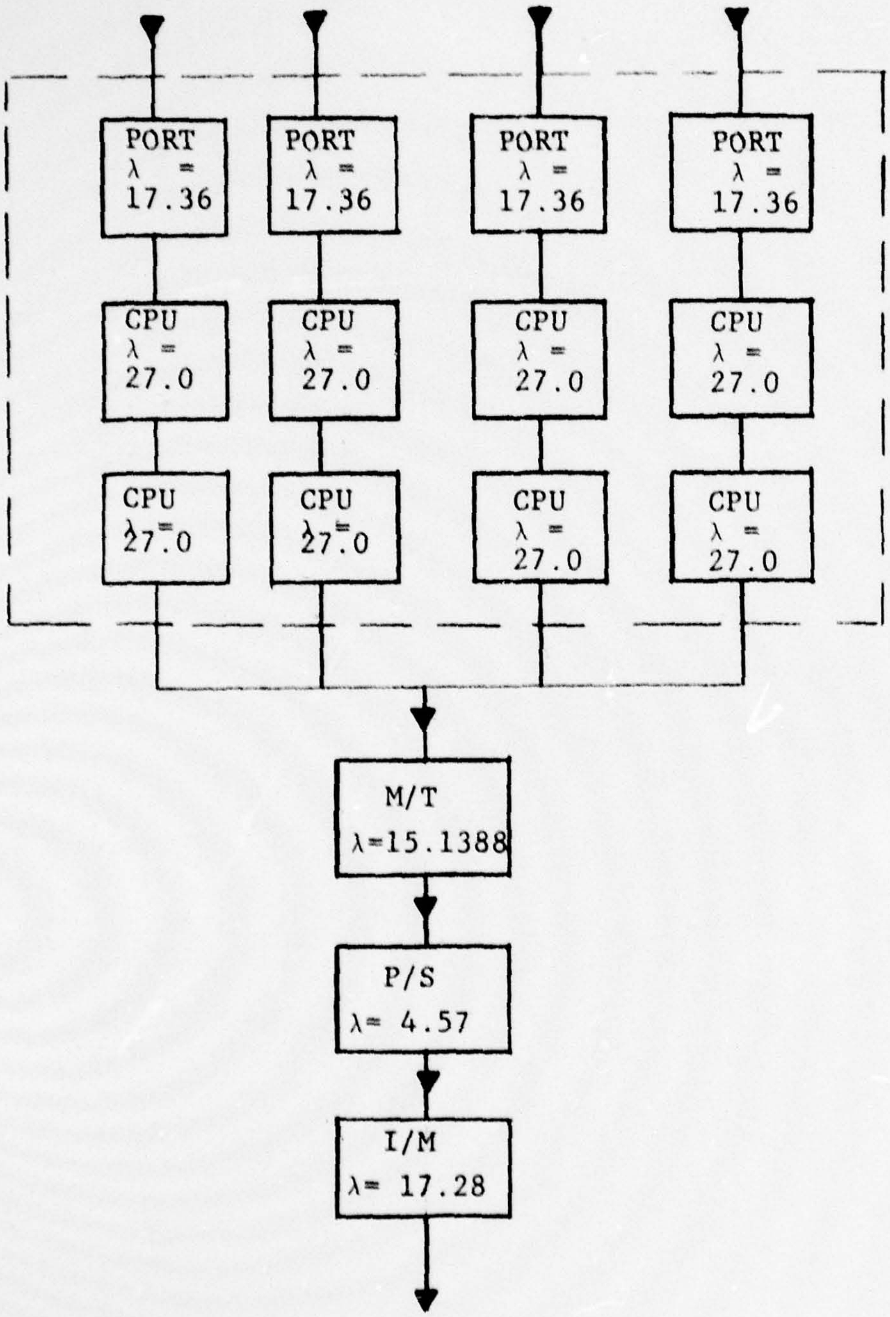

PORT
λ =
17.36
PORT
λ =
17.36
PORT
λ =
17.36
PORT
λ =
17.36
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
CPU
λ =
27.0
M/T
λ=15.1388
P/S
λ= 4.57
I/M
λ= 17.28

FIGURE 19

PART NAME	BOX QTY(n)	λ, FAILURE/10^6 HRS. @ Ta = 90°C	nλ
1. Port	4	17.36	69.44
2. CPU-1	4	27	108
3. CPU-2	4	27	108
4. MEM/TIM	1	15.138	15.138
5. SOSTEL IM	1	17.28	17.28
6. S/D IM	1	5.176	5.176
7. Analog IM	1	31.464	31.464
8. UHF Data IM	1	7.462	7.462
9. UHF DIS IM	1	7.462	7.462
10. A/D IM	1	46.84	46.84
11. Power Supply	1	4.57	4.57
	—		420.8

1) Items 1 through 10 are P.C. cards.

2) $\text{MTBF} = \frac{1}{420.8} \times 10^6 = 2376$ hours.

TABLE 4.1

CALCULATIONS

1) For "one of four" operational input parts and CPU

$$4p-6p^2+4p^3-p4$$

$= 3.9994-5.9982001 + 3.9982003- .9994013$

$= .999999$

2) Probability of Mission Success

$= P_1 \cdot P_2 \cdot P_3 \cdot P_4$

where time (t) - 2 hours

$P_{2,3,4} = e^{-\lambda t}$

$= 0.99999x0.9996x.099999x0.99996$

$= \underline{0.9991}$

..2 PART DERATING GUIDELINES

art derating and redundancy considerations are the most significant actors in determining overall system MTBF or Reliability. By decreasing electrical and thermal stresses at the component or part evel, the designer can preserve the inherent reliability of the parts.

Parts shall be selected and derated as listed below:

APACITOR TYPES	MIL SPEC	MINIMUM VOLTAGE DERATING
Ceramic	MIL-C-39014	.5
ica	MIL-C-39001	.5
Paper/Film	MIL-C-14157	.5
Solid Electrolyte	MIL-C-39003	.5
on-Solid	SHALL NOT BE USED	----

5-58

Telephonics

A DIVISION OF INSTRUMENT SYSTEMS CORPORATION

DIODE TYPES	DERATING FACTOR** OPEN MTG.	PARAMETER
General Purpose, Switching	.30	Power
	.50	PIV
	.50	Surge Current
	.50	Forward Current
Zener	.30	Power
	.50	Forward Current
Reference	.30	Power
	.50	Forward Current

TRANSISTOR TYPES	DERATING FACTOR** FACTOR	PARAMETER
General Purpose	.30	Power
	.50	Current
	.60	Voltage
Power	.30	Power
	.50	Current
	.60	Voltage
Switching	.50	Power
	.50	Current
	.60	Voltage

MICROCIRCUIT TYPES	DERATING FACTOR** OPEN MTG.	PARAMETER
Digital	.80	Fanout/Output Current
	.75	Supply Voltage
	.75	Operating Frequency
Linear	.80	Supply Voltage
	.75	Output Current
	.75	Operating Frequency

** Derating Factor = $\frac{\text{Maximum Allowable Stress}}{\text{Rated Stress}}$

APPLICATION NOTES

a. Do not exceed the maximum current rating of the capacitor; series limiting resistors should be utilized for charge/discharge circuits. Ceramic capacitors should be limited to 50 ma charge/discharge currents. Solid tantalum capacitors should employ a 3 ohms/volt series limiting resistor.

b. Maximum voltage includes superimposed AC and DC pulse voltages.

c. Manufacturer's recommendation for ripple currents must be strictly observed. Reverse bias should be prevented in AC applications by application of a sufficient forward DC bias.

d. Loss of pressurization should not cause the failure of any capacitor, particularly air dielectric types. Circuit manufacturer's notes for additional voltage derating should be consulted.

RESISTOR TYPES	MIL SPEC	MAXIMUM* STRESS RATIO
Composition	MIL-R-39008	.5
FILM	MIL-R-39017	.5
FILM	MIL-R-55182	.5
Wire Wound	MIL-R-39007	.5

$* \dfrac{\text{Maximum Allowable Stress}}{\text{Rated Stress}}$

APPLICATION NOTES

a. Voltage shall not exceed 80% of the manufacturer's rating.

b. If power resistors are mounted in proximity the maximum power dissipation shall be reduced by 20%.

APPLICATION NOTE

Tr[illegible]nsient protection must be provided for integrated circuits. Power derating shall be achieved by means of appropriate fan-in, fan-out and lo[illegible]ding.

TRANSFORMERS AND INDUCTORS GENERIC TYPE	MAXIMUM HOT-SPOT TEMPERATURE RISE
MIL-T-27	30°C
Class S	40°C
T	35°C

APPLICATION NOTE

S[illegible]rrounding components must not be heated beyond their specified operational temperatures.

4.3 SUBSYSTEM FAULT HAZARD ANALYSIS

4.3.1 INTRODUCTION

This document is a preliminary submittal of the Subsystem Fault Hazard Analysis for The ADM.

4.3.2 PURPOSE

The purpose in performing the Ss/HA is to identify and minimize, or eliminate where possible potential hazards to the safety of the ADM and its operating personnel. This analysis has been performed in accordance with the process described in MIL-STD-882. Formats and Steps (I, II and III, IV) of MIL-STD-882 are used.

4.3.3 ANALYSIS PROCEDURE AND RESULTS

A. PROCEDURE

The preliminary analysis was prepared to the second tier subsystem level. The block diagram on page 78 is the Ss/HA summary sheet and shows the ADM as the first time subsystem.

The ADM was subdivided into two second tier subsystems by WRA which comprise the second tier subsystem.

The potential hazards to the ADM and operating personnel in each mission phase were then listed and the system features designed to protect against each hazard were carefully evaluated. Check lists are being completed for all applicable hazards. Finally, each potential hazard was categorized as to severity to the system.

B. RESULTS

As can be seen from Table 4.3-2 there are no potential hazards with a hazard severity greater than Category II.

The severity category assigned to each potential hazard reflects the Telephonics design concept for the ADM. Typically, the use of flame retardent materials throughout the subsystem as well as limiting the ability of the power supplies to furnish current into a short circuit reduces the hazard to a category 1 severity.

The potential electrical hazard to personnel during ground operation has been similarly controlled by design. All contacts and terminals having potentials in excess of 70V RMS will have barriers provided to prevent accidental contact by personnel. In addition such terminals will be identified and marked. This potential hazard can be controlled provided operating personnel exercise reasonable caution and observe the precautions designed by Telephonics. Therefore, the potential electrical hazard to personnel has been designated Category II.

The interim Hazard Analysis submission will be submitted using the sub-system Hazard Analysis Form which is attached.

Hazard Analysis Consideration Checklist was used with the following protective measures taken:

1. Protection of personnel from shock hazards by grounding external conducting paths, protecting and labeling internal high voltage points.

2. Protection against handling hazards by rounding corners and edges and controlling exterior surface temperatures.

3. Provide crash safety by providing mounting withstanding 30G loads.

4. Prevention of internal failure damage by over-voltage and over-current protection in power supply.

5. Fail safe circuit design such that circuit failure does not overload power supply.

6. Component packaging is in accordance with level A of MIL-STD-794.

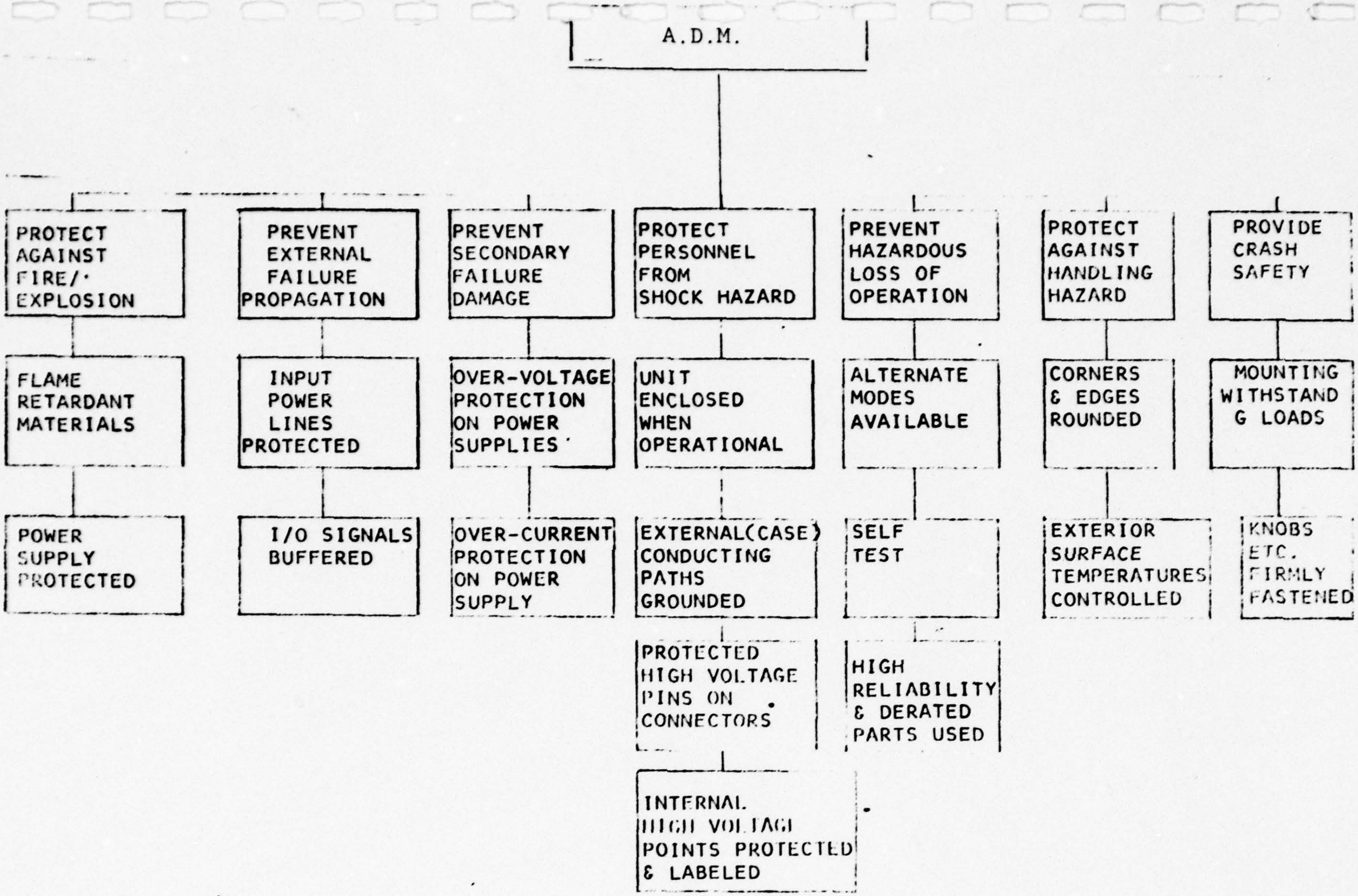
7. Training pertaining to safe maintenance of the system is conducted to all personnel responsible with system maintenance.

8. Resistance to mechanical shock damage.

9. System environmental constraints.

10. Protection against fire/explosion by usage of flame retardant materials and internally protected power supply.

11. Prevention of external failure propagation by protection of input power lines and I/O signals buffering.



BLOCK DIAGRAM

COMPONENT HAZARD ANALYSIS

MISSION PHASE	PERSONNEL SHOCK HAZARD	HANDLING HAZARD	CRASH SAFETY	INTERNAL FAILURE	FAIL SAFE DESIGNS	STORAGE	TRAINING PERTAINING TO SAFE MAINTENANCE OF SYS	POWER LINE TRANSIENTS	RESISTANCE TO SHOCK	SYSTEM ENVIRONMENTAL CONSTRAINTS	FIRE/EXPLOSION	EXTERNAL FAILURE PROPAGATION
1. Maintenance	II	I		I	I	I	I	I	I	I	I	I
2. Ground Operational	II	I		I	I	I	I	I	I	I	I	I
3. Flight Operational	I	I	II	I	I			I	I	I	I	I

HAZARD LEVELS

Category I Negligible - Will not result in personnel injury or system damage.

Category II Marginal - Can be counteracted or controlled without injury to personnel or major subsystem damage.

Category III Critical - Will cause personnel injury or major system damage or will require immediate corrective action for personnel or system survival

Category IV Catastrophic - Will cause death or severe injury to personnel or system loss.

HAZARD ANALYSIS CONSIDERATION
CHECK LIST

TABLE 4.3-2

4.4 MAINTAINABILITY

- Designed for maintenance at organizational, intermediate and depot levels as defined in OP NAVINST 4790.2A
- Repair at organizational level will be limited to simple removal of WRA.
- Repair at intermediate level shall be simple replacement of SRA's
- SRA's and WRA's shall be removed with no special tool and with minimum time.
- MTTR calculation
- Continual design review to insure conformance with calculations and design goals.
- Corrective action implementation
- Trade Studies
- Comparison of allocated repair times with actual repairs.

SECTION 5.0

TEST & SUPPORT

Figure 20 illustrates the test set-up to be used to support and demonstrate ADM system operation. All required software and hardware (other than that marked "GFE") will be made available by Telephonics.

SECTION 6.0

RECOMMENDATIONS

6.1 TEST/CONTROL PANEL

Figure 21 illustrates the control and display panel of a proposed ADM system support device which would aid in operation and trouble-shooting. A full proposal will be submitted under separate cover.

6.2 INCORPORATE BCU FUNCTION IN MT

In an effort to concentrate the design, fabrication and test efforts in the more fruitful area (that of the MT) Telephonics recommends eliminating the fabrication of a separate BCU with the function included in the MT software. See figure 22 for the block diagram and flow chart.

APPENDIX 1

DRAWING PACKAGE

APPENDIX 2

THERMAL ANALYSIS

1. FAN INLET TEMP AS A FUNCTION OF ALTITUDE & CFM

ALTITUDE	PRESSURE (P)	TEMP (PER CURVE B, MIL-E-5400 CLASS 2)		
K, FT	PSIA	°C	°F	°R
S.L.	14.7	71.	160.	620.
50.	1.68	35.	95.	555.
70.	0.646	10.	50.	510.

$$Q = w c_p 60 (T_F - T_\infty)$$

$$Q = \rho_F \, CFM \, c_p 60 (T_F - T_\infty) = 300 \text{ WATTS} \times 3.413 = 1023.9 \ \frac{BTU}{HR}$$

WITH $\rho_F = \dfrac{2.7 \times P}{T_F}$, lb/ft³

T_∞ = AMB TEMP, °R

T_F = FAN INLET, °R

$$Q = \frac{2.7P}{T_F} CFM \, 14.4 (T_F - T_\infty)$$

$$\frac{Q}{2.7 P \, CFM \, 14.4} = 1 - \frac{T_\infty}{T_F}$$

$$\frac{T_\infty}{T_F} = 1 - \frac{Q}{2.7 P \, CFM \, 14.4}$$

$$\frac{T_\infty}{T_F} = 1 - \frac{1023.9}{2.7 \times 14.4 \, P \, CFM} = 1 - \frac{26.3}{P \, CFM}, \ °R/°R$$

At S.L., P = 14.7 psia & $T_\infty = 71°C = 620°R$

$$\frac{T_\infty}{T_F} = 1 - \frac{1.79}{CFM}, \quad °R/°R$$

CFM	50	100	150	200
T_∞/T_F	.964	.982	.988	.991
T_F, °R	643	631.3	627.5	625.6
T_F, °C	83.9	77.4	75.3	74.2
$T_F - T_\infty$ (°C)	12.9	6.4	4.3	3.2

At 70K, P = 0.646 psia & $T_\infty = 10°C = 510°R$

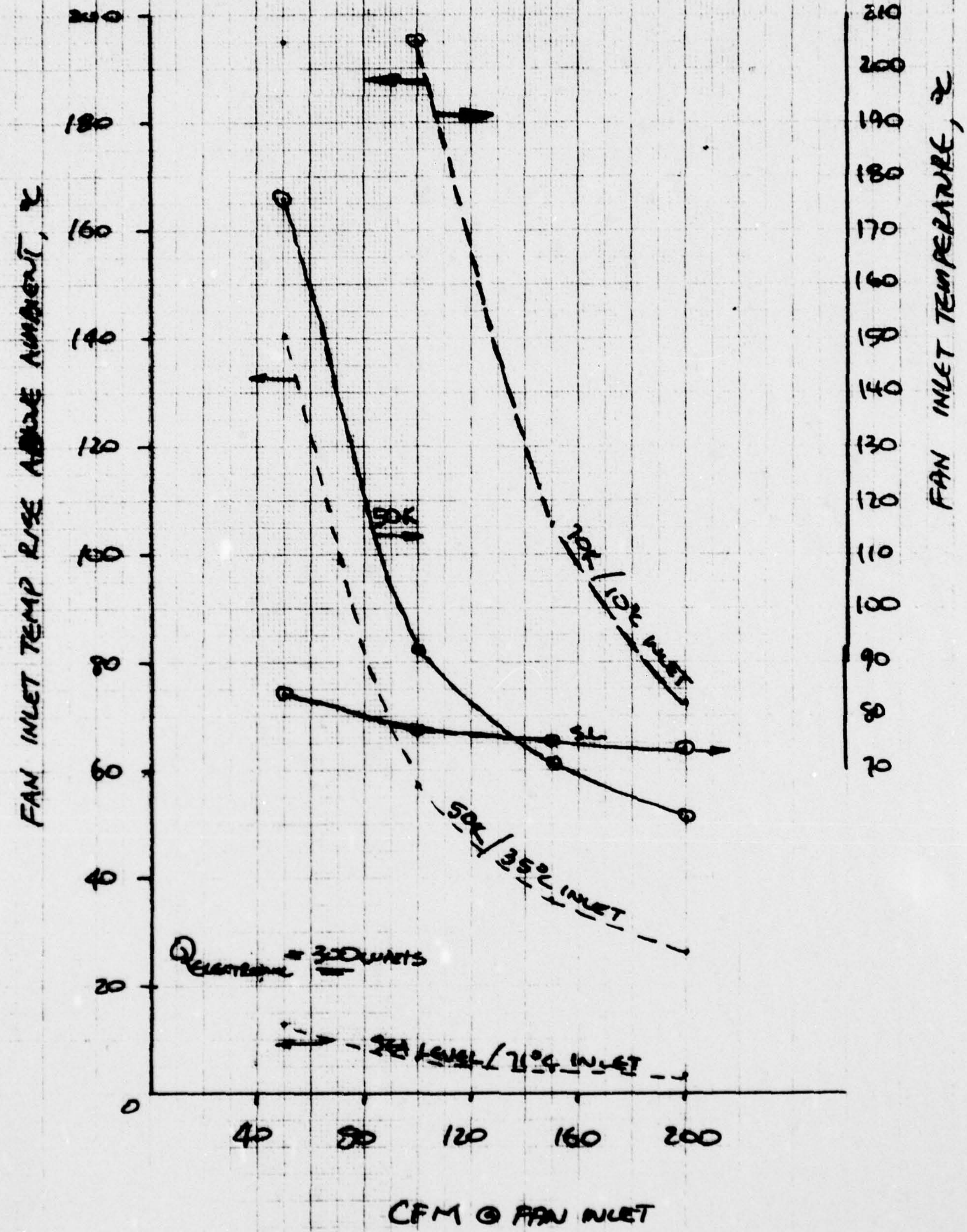
$$\frac{T_\infty}{T_F} = 1 - \frac{40.71}{CFM}, \quad °R/°R$$

CFM	50	100	150	200
T_∞/T_F	.186	.593	.729	.796
T_F, °R	—	860.	700	640.3
T_F, °C	—	204.6	115.5	82.4
$T_F - T_\infty$ (°C)	—	194.6	105.5	72.4

At 50K P = 1.68 psia & $T_\infty = 35°C = 555°R$

$$\frac{T_\infty}{T_F} = 1 - \frac{15.65}{CFM}, \quad °R/°R$$

CFM	50	100	150	200
T_∞/T_F	.687	.844	.896	.922
T_F, °R	807.9	658.	619.7	602.1
T_F, °C	175.5	92.2	70.9	61.2
$T_F - T_\infty$ (°C)	140.5	57.2	35.9	26.2


FAN INLET TEMP RISE ABOVE AMBIENT, °C
FAN INLET TEMPERATURE, °C
CFM @ FAN INLET
50K
70K / 10°C INLET
SL
50K / 35°C INLET
SEA LEVEL / 71°C INLET
Q ELECTRONIC = 300 WATTS
0
20
40
60
80
100
120
140
160
180
200
40
80
120
160
200
70
80
90
100
110
120
130
140
150
160
170
180
190
200
210

J.N.

AT 70K,

$Q = ?$ TO LIMIT FAN INLET TEMP

$T_\infty = 10°C$
$T_F \leq 85°C$ } $\Delta T = 85 - 10 = 75$

@ 100CFM, $\frac{75}{194.6}$ (300 WATTS) = 115.6 WATTS

$T_\infty = 10°C$
$T_F \leq 125°C$ } $\Delta T = 125 - 10 = 115°C$

@ 100CFM, $\frac{115}{194.6}$ (300 WATTS) = 177.3 WATTS

$T_\infty = 10°C$
$T_F \leq 100°C$ } $\Delta T = 100 - 10 = 90°C$

@ 100CFM, $\frac{90}{194.6}(300) = 138.7$ WATTS

AT 70K,

IF FAN INLET TEMP IS LIMITED TO (°C)	REQUIRED CFM AT FAN INLET
85°C	193.0
100°C	170.0
125°C	142.0

AT 90K,

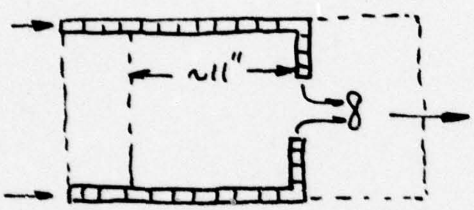
85°C	114.0
100°C	94.0
125°C	79.0

* BASED ON 300 WATT LOAD

FOR PURPOSES OF DESIGN TRADE-OFF, CONSIDER FIN HEIGHT = 0.375"

DESIGN a ... INTERNAL FAN, MAX ALTITUDE? @ 300 WATTS

(.006" THK) FPI	FFA_f	HTA_f	D_{HYD}
6	.00247	.045	.0187
10	.00241	.065	.0125
12	.002375	.075	.0106
	(FT^2/in)	(FT^2/in^2)	(ft.)



LET CARD "HEAT" = 165 WATTS

P/S "HEAT" = 135 WATTS

300 WATTS

[$\eta_{P/S} = 55\%$]

AT 12 FPI (CARD AREA ONLY)

1 PASSAGE HIGH, 6.3" WIDE

$HTA = 6.3 \times 11 \times (.075) = 5.2\ FT^2/WALL$

$FFA = 6.3 \times .002375 = .015\ FT^2/WALL = 2.15\ IN^2/WALL$

TOTAL FLOW }

$$R_e = \left(\frac{W/2}{FFA}\right)\frac{D_{HYD}}{\mu} = \frac{.0635\ CFM \times 60}{\frac{2.15 \times 2}{144}} \times \frac{.0106}{.047}$$

$= 28.64\ CFM_{TOTAL}$

CFM/2 = CFM per side → 100/2 150/2 200/2

CFM per side →	100/2	150/2	200/2
Re →	2864.	4296.	5728.
j →	.0037	.0035	.0033
f →	.0115	.010	.0094

$$h = j\left(\frac{\omega 60}{FFA}\right)\frac{c_p}{P_r^{2/3}} \quad , \text{BTU/hr ft}^2\text{°F}$$

$$h = \frac{j(.0635)\,CFM_s\,60 \times .24}{.019 \times .788} = 77.36\, j\, CFM_s$$

$$\eta_f = \frac{\tanh\left\{\sqrt{\frac{2h}{Kt}}\,H\right\}}{\sqrt{\frac{2h}{Kt}}\,H} \qquad H = .375'' = .03125'$$

$$\Delta T_{AIR} = \frac{1.9 \times \sout{300/2}\ 165}{\omega c_p 60}, \text{°C}$$

$$T_{H.S} = T_{\infty} + \Delta T_{AIR}/\eta$$

h →	14.3	20.3	25.5	
η_f	0.848	0.800	0.762	
$hFFA\eta_f$	63.1	84.4	101.	
$\omega c_p 60$	45.7	68.6	91.4	
NTU	1.38	1.23	1.105	
$\eta = 1 - e^{-NTU}$	0.75	0.71	0.67	
ΔT_{AIR}, °C	3.4 ~~6.2~~	2.3 ~~4.2~~	1.7 ~~3.1~~	(NOTE: AT S.L.)
T_{HS}, °C	75.5 ~~79.3~~	74.2 ~~76.9~~	73.5 ~~75.6~~	

AIRFLOW/SIDE →	50 CFM	75 CFM	100 CFM
$\left(f\frac{HTA}{FFA}\right)_{CARD\ SECTION}$ →	4.	3.5	3.3

$$(\sigma \Delta P)_{CARD\ SECTION} = \frac{0.226\left(f\frac{HTA}{FFA}\right)_{CARD\ SECTION}}{(2.15)^2}\left(.0635 \times \frac{CFM_{TOTAL}}{2}\right)^2$$

2.0	3.9	6.5	"H_2O

NOTE: TRY DOUBLE DECKER, i.e. 2 PASSAGES = 2 × .375 = 0.75"

$FFA = 6.3 \times .002375 \times 2 = .03\ ft^2/WALL = 4.3\ in^2/WALL$

$HTA = 10.4\ FT^2$

CFM PER SIDE

$$R_e = \frac{.0635\, CFM_s\, 60}{.03}\ \frac{.0106}{.047} = 28.6\, CFM_s$$

0.11 .61

CFM_s →	50	75	100
T_{HS}, °C	75.4 ~~79.1~~ °C	74.4 ~~77.3~~	73.7 ~~76~~
$f\frac{HTA}{FFA}$	5.9	4.7	4.0
$(\Gamma \Delta P)_{CARD\ SECTION}$ ("H_2O)	0.73	1.3	2.0

NOTE: TRY 8 FPI ... SINGLE PASSAGE

AT 8 FPI, $FFA_f = .00244\ FT^2/IN$

$HTA_f = .055\ FT^2/IN^2$

$D_{HYD} = .0125\ FT$

$FFA = .00244 \times 6.3 = .0154\ FT^2 = 2.22\ IN^2$

$HTA = .055 \times 6.3 \times 11.0 = 3.81\ FT^2$

$$R_e = \frac{.0635\ CFM_s\ 60 \times .0125}{.0154 \times .047} = 65.8\ CFM_s$$

CFM_s →	50	75	100
R_e	3290.	4935	6580
j	.0039	.0037	.0035
f	.0125	.011	.0098

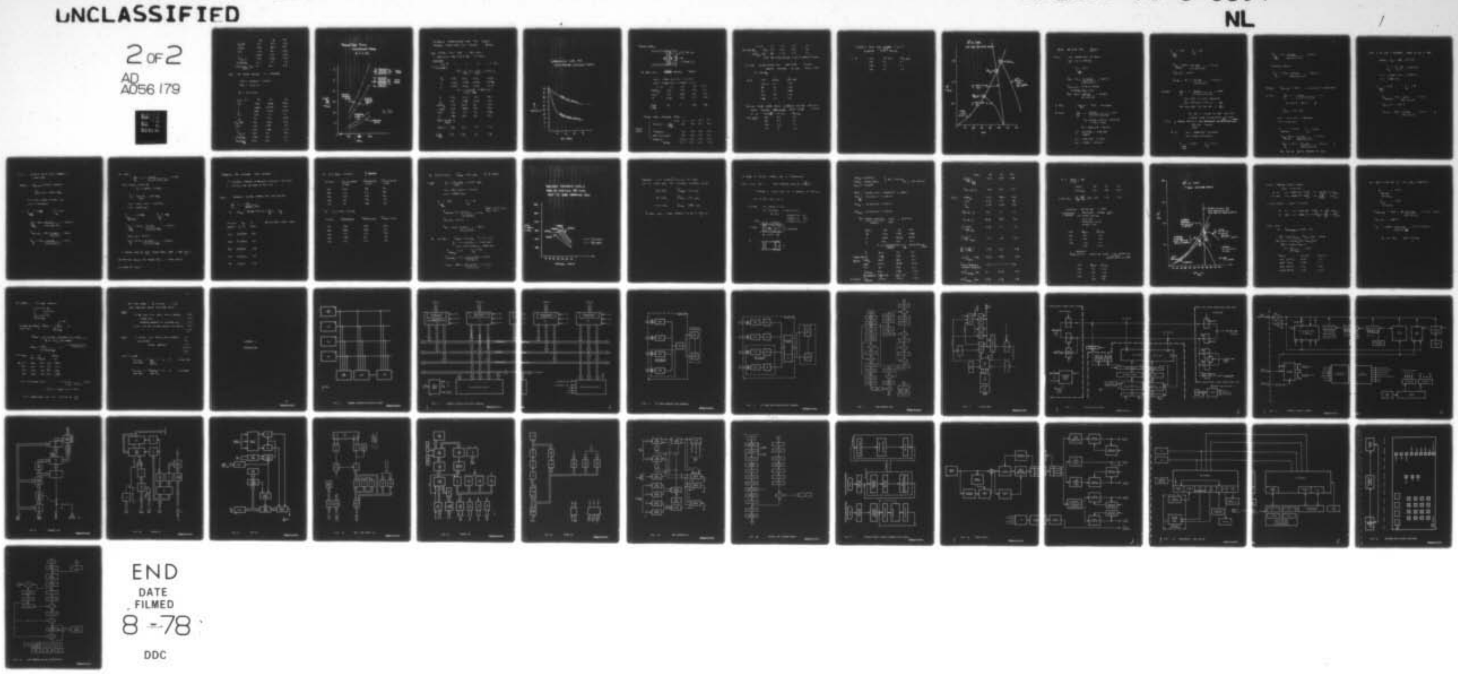
$$h = \frac{j(.0635)\ CFM_s\ 60 \times .24}{.0154 \times .788} = 75.35\, j\ CFM_s$$

	50	75	100
h =	14.7	20.9	26.4
η_f	0.84	0.79	0.76

AD-A056 179 TELEPHONICS HUNTINGTON N Y F/G 17/2
RECOMMENDED DESIGN APPROACH OF GENERAL PURPOSE MULTIPLEX SYSTEM--ETC(U)
1977 N62269-76-C-0394

UNCLASSIFIED NL

2 OF 2
AD
A056 179



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DATE
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8-78
DDC

	50.	75.	100.
$h\eta_f$ HTA	47.	62.9	76.4
$\dot{w}c_p$ 60	45.7	68.6	91.4
NTU	1.03	.92	0.84
η	0.64	.60	0.57
T_{HS}, °C	76.3	74.8	74.0
f HTA/FFA	3.1	2.7	2.4
$(\sigma\Delta P)_{CARD\ SECTION}$, "$H_2O$	1.4	2.8	4.5

NOTE: TRY DOUBLE DECKER, i.e. 2 PASSAGES

FFA = .0308 FT^2 = 4.44 in^2

HTA = 7.62 FT^2

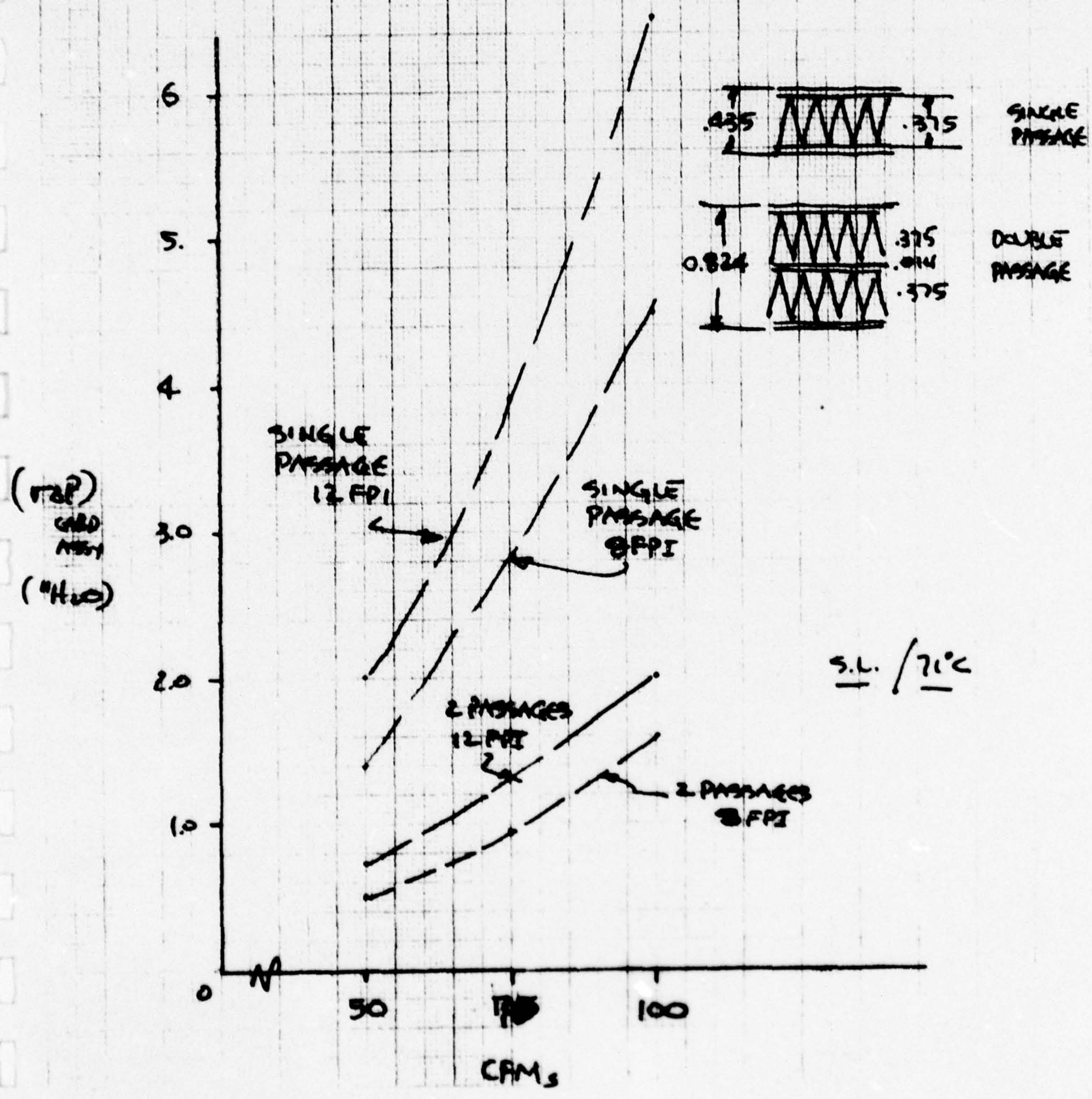
Re = 32.9 CFMs

CFMs →	50	75	100
Re	1645	2468	3290
j	.0055	.0043	.004
f	.018	.0145	.0125
h	10.4	12.2	15.1
η_f	.67	.64	0.59
$h\eta_f$ HTA	53.1	59.5	67.9
NTU	1.16	0.87	.74
η	0.69	0.58	0.52
T_{HS}, °C	75.9	75.	74.3
f HTA/FFA	4.45	3.6	3.1
$(\sigma\Delta P)_{CARD\ CAGE}$	0.51	.94	1.4

PRESSURE DROP STUDY

SINGLE/DOUBLE PASSAGE

8 → 12 FPI



DETERMINE EFFECTIVENESS MAP FOR SINGLE PASSAGE 0.375" HIGH FIN DESIGN ... 8FPI

MAX SYSTEM FLOW RATE ... 8.0 lb/min

∴ MAX FLOW PER COLD PLATE .. 4.0 lb/min

CARD ASSY

$w_s \rightarrow$ FLOW/COLD PLATE: 1, 2, 3, 4 lb/min

$$Re = \frac{w}{.0154} 60 \times \frac{.0125}{.047} = 1036.2\,w$$

	1	2	3	4
Re	1036	2072	3109.	4145.
j	.0067	.0046	.0040	.0038
f	.0255	.0155	.0130	.0115

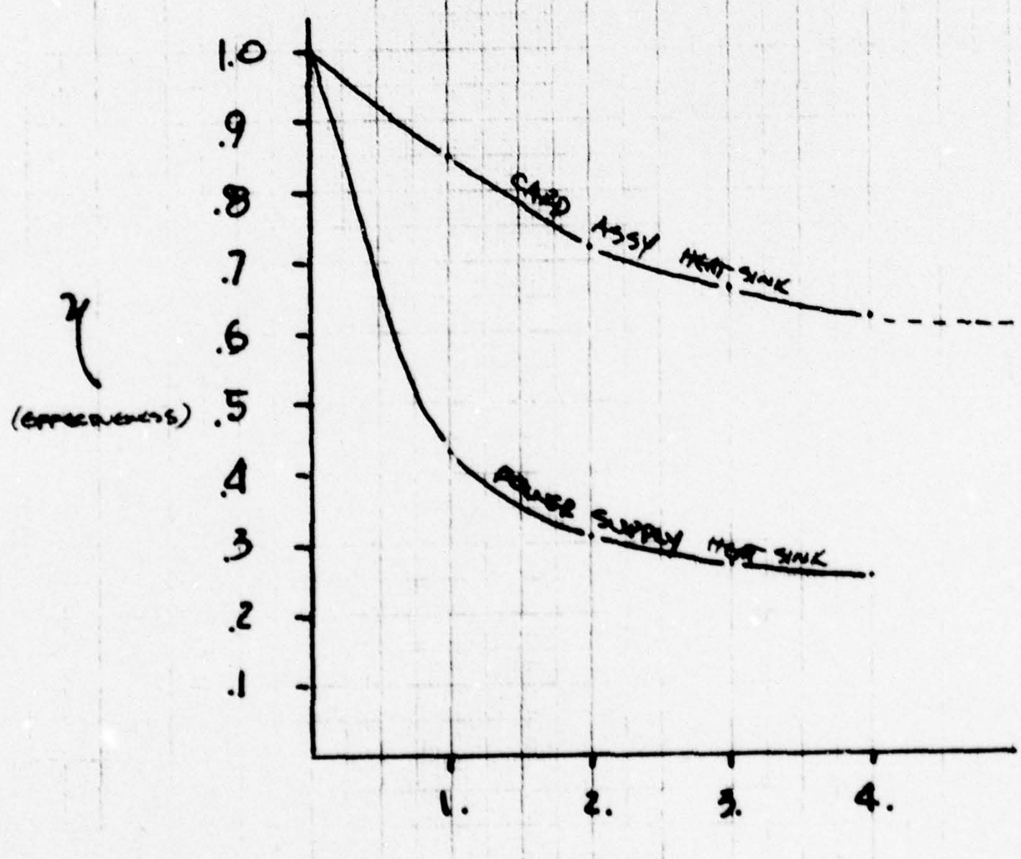
$$h = j \frac{w}{.0154} \frac{60(.24)}{.788} = 1186.6\, jw$$

	1	2	3	4
h	7.95	10.9	14.2	18.0
η_f	0.91	0.88	0.85	0.82
$hHTA\eta_f$	27.6	36.5	46.	56.2
wc_p60	14.4	28.8	43.2	57.6
· NTU	1.92	1.27	1.06	0.98
η	0.85	0.72	.66	0.62

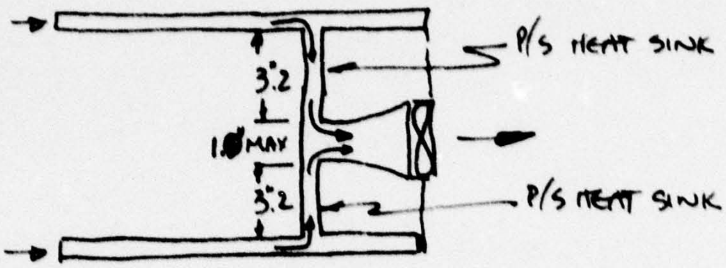
$$\Delta T_{AIR} = \frac{1.9 \times 165}{wc_p60}, °C$$

	1	2	3	4
ΔT_{AIR}, °C	21.8	10.9	7.3	5.4
$f\frac{HTA}{FFA}$	6.3	3.8	3.2	2.8

EFFECTIVENESS MAPS FOR
SINGLE PASSAGE (.375" HIGH) DESIGN



POWER SUPPLY . . .



P/S HEAT SINK . . . SINGLE PASSAGE (8 FPI)

HTA = .055 × 6.3 × 3.2 = 1.11 ft²

FFA = .0024 × 6.3 = .0154 ft² = 2.22

$w \rightarrow$	1.0	2.0	3.0	4.0
$hHTA_{H}$ =	8.0	10.6	13.4	16.4
$w c_p 60$	14.4	28.8	43.2	57.6
η	0.43	0.31	0.27	0.25
$f \frac{HTA}{FFA}$	1.8	1.1	0.93	0.81

SYSTEM TOTAL PRESSURE DROP . . .

VELOCITY HEADS . . .

	$w \rightarrow$	1.0	2.0	3.0	4.0
VELOCITY HEADS . . .	FRICTION . . $f \frac{HTA}{FFA}$	8.1	4.9	4.1	3.6
	CONTRACTION	0.5	0.5	0.5	0.5
	TURN (WITH VANE)	0.5	0.5	0.5	0.5
	EXPANSION	1.0	1.0	1.0	1.0
	TOTAL	10.1	6.9	6.1	5.6

	$\omega_s \rightarrow$	1.0	2.0	3.0	4.0
@ .0635 lb/ft³	CFM_s	15.7	31.5	47.2	63
	$\sigma \Delta P_{TOTAL}$, "H_2O	.46	1.27	2.5	4.1

(FOR PRELIMINARY ESTIMATE, IGNORE "σ" CORRECTION AT SEA LEVEL)

CONSIDER GLOBE MOTOR FAN VAX-3-BD C-5240

28 VOLTS, 13000 RPM 42 WATTS DIA = 3" L = 3 3/16"

@ .075 lb/ft³

A → CFM	ΔP, "H_2O	ΔP @ .0635
63 MIN	1.6	1.35
80	1.25	1.06
90	1.0	0.85
100	0.5	0.42
110	0.0	0.0

CONSIDER GLOBE MOTOR FAN(S) 2 PARALLEL CONNECTED STAX-3-X

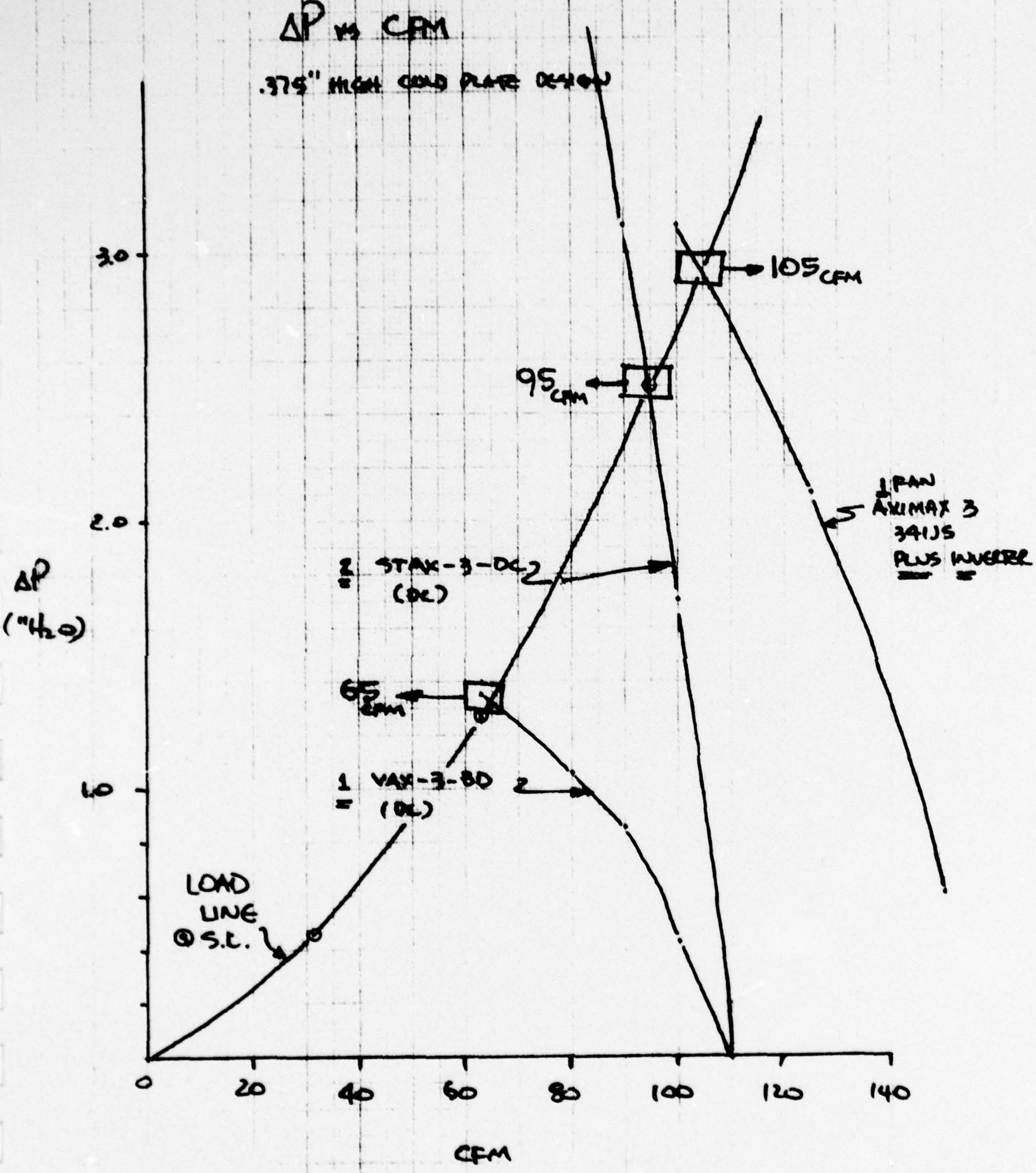
27 VOLTS 19000 RPM 88.4 WATTS/FAN DIA = 3" L ≈ 3.5" C-5259

B →	CFM / TWO FAN	ΔP "H_2O	ΔP @ .0635
NOTE: 2 FANS	80	5.0	4.2
	90	3.7	3.1
	100	2.0	1.7
	110	0	0.0

AXIMAX 3 3413S PLUS INVERTER (DC?)

22,500 RPM   POWER ~ 155 WATTS

C →	CFM	ΔP "H2O	ΔP @ .0635
	100	3.7	3.1
	125	2.5	2.1
	150	0.7	0.6


ΔP vs CFM
.375" HIGH COLD PLATE DESIGN
3.0
2.0
1.0
ΔP
("H2O)
0
20
40
60
80
100
120
140
CFM
105 CFM
95 CFM
65 CFM
2 STAX-3-DC 2
(DC)
1 VAX-3-3D 2
(DC)
1 FAN
AXIMAX 3
341JS
PLUS INVERTER
LOAD
LINE
@ S.L.

WITH VAX-3-BD FAN, 65 CFM

@ S.L. $\omega_T = .0635 \times 65 = 4.1$ lb/min

$\frac{\omega_T}{2} = \omega_s = 2.05$ lb/min

$\therefore \eta_{CARD\ ASSY} = 0.71$

$$T_{HS} = 71 + \frac{1.9 \times 165/2}{2.05 \times 14.4 \times .71} = 78.5°C$$

$$T_{AIR\ IN\ P/S} = 71 + 5.3 = 76.3°C$$

@ 2.05 lb/min, $\eta_{P/S} = 0.3$

$$T_{P/S} = 76.3 + \frac{1.9 \times 135}{4.1 \times 14.4 \times 0.3} = 90.8°C$$

@ 50K $T_{AIR\ INTO\ FAN} = 150°C$ UNACCEPTABLE

@ 30K $\frac{T_{\infty}}{T_F} = 1 - \frac{1023.9}{2.7 \times 14.4 \times 4.36 \times 65} = .907$

$$T_{\infty} = 56.5°C = 133.7F = 593.7°R$$

(CLASS 2 MIL-E-5400)

$$T_F = 654.6°R = 90.3°C$$

$$\rho = \frac{2.7 \times 4.36}{654.6} = .018 \text{ lb/ft}^3$$

$\therefore \omega_T = .018 \times 65 = 1.17$ lb/min

$\omega_s = 0.585 \sim .59$ lb/min

$\eta_{\text{CARD ASSY}} = 0.9 \qquad \eta_{P/S} = 0.6$

$$T_{HS\,\text{CARD ASSY}} = 56.5 + \frac{1.9 \times 165}{1.17 \times 14.4 \times 0.9} = 77.2\,°C$$

$$T_{AIR\,IN\,P/S} = 75.1\,°C$$

$$T_{HS\,P/S} = 75.1 + \frac{1.9 \times 135}{1.17 \times 14.4 \times 0.6} = 100.5\,°C$$

@ 40K

$$\frac{T_{\infty}}{T_F} = 1 - \frac{1023.9}{2.7 \times 14.4 \times 2.72 \times 65} = 0.851$$

$$T_{\infty} = 47°C = 116.6°F = 576.6°R$$

$$T_F = 677.6°R = 103.1°C$$

MAX ALLOWABLE FOR THIS FAN IS **85°C**

∴ THIS FAN IS LIMITED TO APPX 30,000 FT

A SPECIAL MOTOR WINDING PERMITS 100°C TEMP!!

WITH **2** PARALLEL STAX-3-DC (~~OR EQUIVALENT SUCH AS~~ [illegible] [illegible])

95 CFM MINIMUM

@ S.L. $\quad w_T = .0635 \times 95 = 6.03\ \text{lb/min}$

$w_S = 6.03/2 = 3.015\ \text{lb/min}$

$\eta_{\text{CARD ASSY}} = 0.66 \qquad \eta_{P/S} = 0.27$

$$T_{HS\ \text{CARD ASSY}} = 71 + \frac{1.9 \times 165}{6.03 \times 14.4 \times 0.66} = 76.5\ ^\circ C$$

$T_{\text{AIR IN P/S}} = 74.6\ ^\circ C$

$$T_{HS\ P/S} = 74.6 + \frac{1.9 \times 135}{6.03 \times 14.4 \times 0.27} = 85.5\ ^\circ C$$

@ 50K, $T_{\text{FAN INLET}} = 99^\circ C$ NO GOOD, FAN IS LIMITED TO 85°C

@ 40K $$\frac{T_{\infty}}{T_F} = 1 - \frac{1023.9}{2.7 \times 14.4 \times 2.72 \times 95} = 0.9$$

$T_F = 642\ ^\circ R = 83.4\ ^\circ C$ OK

$\rho_{FAN} = .0114\ \text{lb/ft}^3$

$\omega_T = .0114 \times 95 = 1.083\ \text{lb/min}$

$\omega_S = 0.54\ \text{lb/min}$

$\eta_{\text{CARD ASSY}} = 0.91$ $\eta_{P/S} = 0.63$

$$T_{HS\ \text{CARD ASSY}} = 47 + \frac{1.9 \times 165}{1.083 \times 14.4 \times 0.91} = 69.1\ ^\circ C$$

$$T_{HS\ P/S} = 67.1 + \frac{1.9 \times 135}{1.083 \times 14.4 \times 0.63} = 93.2\ ^\circ C$$ OK

THIS 2 FAN SET PERMITS OPERATION TO 40K

NOTE: IF FAN LIFE IS ACCEPTABLE, SYSTEM CAN GO TO 50K

@ 50K, T_{FAN} = 99°C = 670.2°R

$$\rho_{FAN} = \frac{2.7 \times 1.68}{670.2} = .0068 \text{ lb/ft}^3$$

ω_T = .0068 × 95 = 0.646 lb/min

ω_S = .323 lb/min

$\eta_{CARD\ ASSY}$ = 0.95 $\eta_{P/S}$ = 0.8

$$T_{HS_{CARD\ ASSY}} = 35 + \frac{1.9 \times 165}{.646 \times 14.4 \times .95} = 70.5°C$$

$T_{AIR\ IN\ P/S}$ = 68.7°C

$$T_{HS\ P/S} = 68.7 + \frac{1.9 \times 135}{.646 \times 14.4 \times .8} = 103.2°C$$ ok

WITH 1 AXIMAX 3 341JS (PLUS INVERTER ?)

CFM = 105.

@ 50K, $T_{FAN\ INLET} \cong 90°C = 654°R$

$\rho_{FAN\ INLET} = .0069$ lb/ft3

$w_T = 105 \times .0069 = 0.725$ lb/min

$w_S = 0.363$ lb/min

$\eta_{CARD\ ASSY} = 0.95$ $\eta_{P/S} = 0.77$

$$T_{HS_{CARD\ ASSY}} = 35 + \frac{1.9 \times 165}{.725 \times 14.4 \times .95} = 66.6°C$$

$$T_{AIR\ IN\ P/S} = 35 + \frac{1.9 \times 165}{.725 \times 14.4} = 65°C$$

$$T_{HS_{P/S}} = 65 + \frac{1.9 \times 135}{.725 \times 14.4 \times .77} = 97°C$$

AT 60K,

$$\frac{T_\infty}{T_F} = 1 - \frac{1023.9}{2.7 \times 14.4 \times 1.04 \times 105} = 0.759$$

$T_\infty = 23.5°C = 534.3°R$

$T_F = 704°R = 117.8°C$

$$\rho_F = \frac{2.7 \times 1.04}{704} = .004 \text{ lb/ft}^3$$

$\omega_T = 105 \times .004 = .419$ lb/min

$\omega_S = .2094$ lb/min

$\eta_{HS \text{ CARD ASSY}} = 0.985$ $\quad\quad$ $\eta_{HS \text{ P/S}} = .88$

$$T_{HS \text{ CARD ASSY}} = 23.5 + \frac{1.9 \times 165}{.419 \times 14.4 \times .985} = 76.3°C$$

$T_{AIR \text{ IN P/S}} = 75.5°C$

$$T_{HS \text{ P/S}} = 75.5 + \frac{1.9 \times 135}{.419 \times 14.4 \times .88} = 123.8°C$$

IT APPEARS THAT AT <u>55K</u>, POWER SUPPLY HEAT IS APPX <u>110°C</u> !

P/S HEAT SINK SHOULD NOT EXCEED THIS ... IN FACT SHOULD

BE LIMITED TO 100°C !

DETERMINE MAX ALLOWABLE HEAT DISSIPATION ....

1st CRITERIA (BEFORE ESTABLISHING ELECTRONIC PART TEMP) IS LIMITING MAX AIR TEMP TO FAN INLET .....

STEP 1 ... ESTABLISH ALTITUDE CRITERIA FOR INLET FAN TEMP

$$\frac{T_\infty}{T_F} = 1 - \frac{Q}{38.88\ P\ CFM}$$

or,

$$Q_{MAX} = 38.88\ P\ CFM \left(1 - \frac{T_\infty}{T_F}\right), \quad \frac{BTU}{HR}$$

PER MIL-E-5400 CLASS 2 CURVE A

ALTITUDE (1000 FT)	T_∞ °C / °R	P (PSIA)
30K	56.5/593.7	4.36
40K	47.0/576.6	2.72
50K	35.0/555.	1.68
60K	23.5/534.3	1.04
70K	10.0/510.	0.65

AT $T_F \leq 85°C = 645°R$ .... [illegible]

ALTITUDE	Q_{max} @ 65CFM (WATTS)	Q_{max} @ 95CFM (WATTS)	Q_{max} @ 105 CFM (WATTS)
30K	257.	376.	416.
40K	214.	313.	346.
50K	174	254.	281.
60K	132.	193.	213.
70K	101.	148	164.

AT $T_F \leq 100°C = 672°R$

ALTITUDE	Q_{max} @ 65CFM	Q_{max} @ 95CFM	Q_{max} @ 105 CFM
30K	376.	550.	608
40K	286.	418.	462
50K	217.	317.	350
60K	158.	231.	255.
70K	116	170	188.

AT 65 CFM FLOW, $Q_{MAX} = 101$ WATTS & $T_F = 85°C$

@ 70K

$$\rho_F = \frac{2.7 \times 0.65}{645} = .00272 \text{ lb/ft}^3$$

$$\omega_T = 65 \times .00272 = .177 \text{ lb/min}$$

$$\omega_s = .0884 \text{ lb/min}$$

$$\eta_{CARD\ ASSY} = .995 \qquad \eta_{P/S} = .95$$

$Q_{CARD} = .55 \times 101 = 55.6w$
$Q_{P/S} = 45.4w$

$$T_{CARD\ ASSY} = 10 + \frac{1.9 \times 55.6}{.177 \times 14.4 \times .995} = 51.7°C$$

$$T_{AIR\ IN\ P/S} = 51.4°C$$

$$T_{P/S} = 51.4 + \frac{1.9 \times 45.4}{.177 \times 14.4 \times .95} = 87°C$$

AT 65 CFM, $Q_{MAX} = 116$ WATTS & $T_F = 100°C$

$$\rho_F = 2.7 \times 0.65/672 = .00261 \text{ lb/ft}^3$$

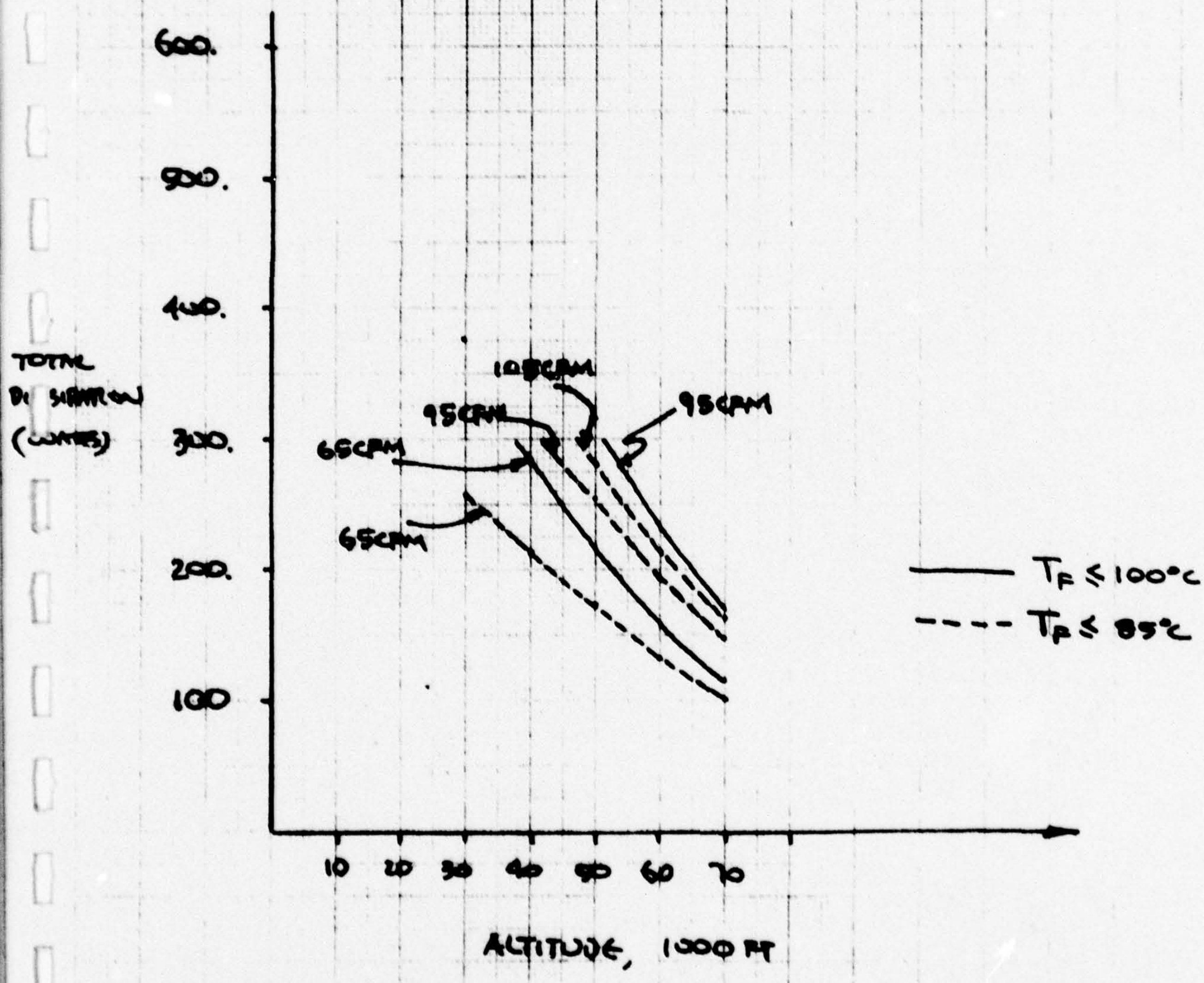
$$\omega_s = 65 \times .00261/2 = .085 \text{ lb/min}$$

$$\eta_{CARD\ ASSY} \sim 1.0 \qquad \eta_{P/S} \doteq .95$$

$$T_{CARD\ ASSY} = 10 + \frac{1.9 \times (116 \times 0.55)}{.17 \times 14.4 \times 1.0} = 59.5°C$$

$$T_{HS\ P/S} = 59.5 + \frac{1.9(116 \times .45)}{.17 \times 14.4 \times .95} = 102.1°C$$

ALLOWABLE DISSIPATION LEVELS
BASED ON LIMITING FAN INLET
TEMP TO SAFE OPERATING LEVEL



THEREFORE, WITH CRITERIA OF LIMITING P/S HEAT SINK TO 100°C MAX, THE ALLOWABLE DISSIPATION LEVELS,

65 CFM Q_{MAX} = 110 WATTS

95 CFM Q_{MAX} = 170 WATTS

105 CFM Q_{MAX} = 188 WATTS

AT ABOVE LEVELS, SYSTEM OPERATION CAN GO TO 70K ALT.

IN ORDER TO DESIGN CHASSIS FOR A "REASONABLE"

NOISE LEVEL FAN .... BACK PRESSURE MUST BE MINI(MI)ZED !!

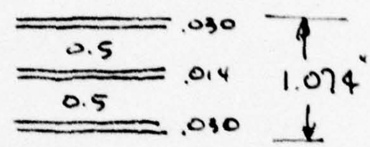
∴ CONSIDER A DOUBLE DECK (I.E. 2 PASSAGES OF 0.5" HIGH

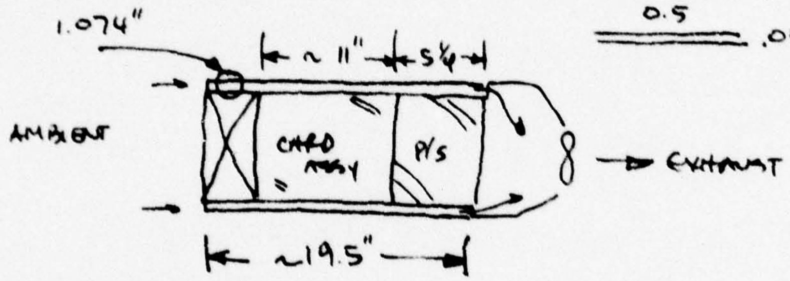
FIN ON EACH SIDE WALL)

CONSIDER FIN HEIGHT = 0.5"

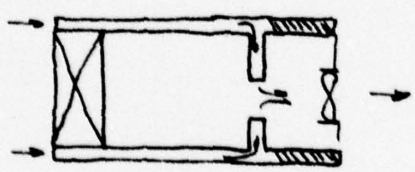
FIN THICKNESS = 0.008" TO 0.01"

8 FPI





OR



$HTA_f = 0.16\ FT^2/in^2$ } FOR 1" HIGH FIN

$FFA_f = .00644\ FT^2/in$ } (OR 2 0.5" HIGH FINS)

$D_{HYD} \cong .0132\ FT$

$FFA = .00644 \times 6.3 = .04057\ FT^2 = 5.84\ in^2$

$HTA_{CARD\ ASSY} = .16 \times 6.3 \times 11 = 11.09\ FT^2$

$HTA_{P/S} = .16 \times 5.25 \times 6.3 = 5.29\ FT^2$

$HTA_{ENTRY} = .16 \times 3.25 \times 6.3 = 3.276\ FT^2$

$$Re = \frac{(.0635 \times CFM_s)\,60}{.04057} \times \frac{.0132}{.047} = 26.4\ CFM_s$$

CFM_s	50	75	100
Re	1319.	1978.	2638
j	.00391	.00366	.00357
f	.016	.013	.012

$$h = j\left(\frac{.0635\,CFM_s}{.04057}\right)60 \times \frac{.24}{.788} = 28.6\,j\,CFM_s,\ \frac{BTU}{hr\,ft^2\,°F}$$

		50	75	100
	h,	5.6	7.9	10.2
(BRAGDON .008)	η_f	0.73	0.67	0.62
CARD ASSY	$hHTA\eta_f$	45.3	58.7	70.1
	$w c_p 60$	45.72	68.58	91.44
	NTU	.99	0.86	0.77
	$\eta_{CARD\ ASSY}$	0.63	0.58	0.53
	$\Delta T_{AIR\ CARD\ ASSY}$, °C	$\frac{6.86}{2} = 3.43$	$\frac{4.57}{2} = 2.29$	1.71
@ SEALEVEL	$T_{HS\ CARD\ ASSY}$	76.4°C	74.9°C	74.2°C

	CFMs	50	75	100
	$\left(f \frac{HTA}{FFA}\right)_{CARD\ ASSY}$	4.37	3.55	3.28
	$T_{AIR\ IN\ P/S}$, °C	74.4	73.3	72.7
(P/S)	$h_{HTA\ Y_f}$	21.6	28.0	33.5
	NTU	0.47	.41	.37
	$\eta_{P/S}$	0.38	0.34	0.31
	$\overline{\Delta T}_{HS\ P/S}$, °C	2.8	1.9	1.4
	$T_{HS\ P/S}$, °C	81.8	78.9	77.2
	$\left(f \frac{HTA}{FFA}\right)_{P/S}$	2.09	1.7	1.56
	$\left(f \frac{HTA}{FFA}\right)_{ENTRY}$	1.29	1.05	0.97
	$\sum \left(f \frac{HTA}{FFA}\right)$	7.75	6.3	5.8
	$\sigma \Delta P_{FRICTION}$, "H2O	0.52	0.95	1.55
	Velocity losses due to contraction & expansion	1.5 →		
	$\sigma \Delta P_{CONTR/EXP}$, "H2O	0.1	0.23	0.4
	$\sigma \Delta P_{SYSTEM}$, "H2O	0.62	1.18	1.95

$\sigma \sim \frac{.0635}{.0765} = .83$

CFM_s	50	75	100
CFM_{TOTAL}	100	150	200
@ SEA LEVEL; $\Delta P_{SYSTEM} = \frac{\sigma \Delta P}{.83}$, "$H_2O$	0.75	1.42	2.35

GLOBE FAN VAX-4.5-GR C-5404

(TRANSFORMER REQUIRED)

RPM = 8000, VOLTAGE 115V D.C

INPUT POWER = 207 WATTS

DIA = 4.8"

DIA(FLANGE) = 5.75"

LENGTH = 6.4"

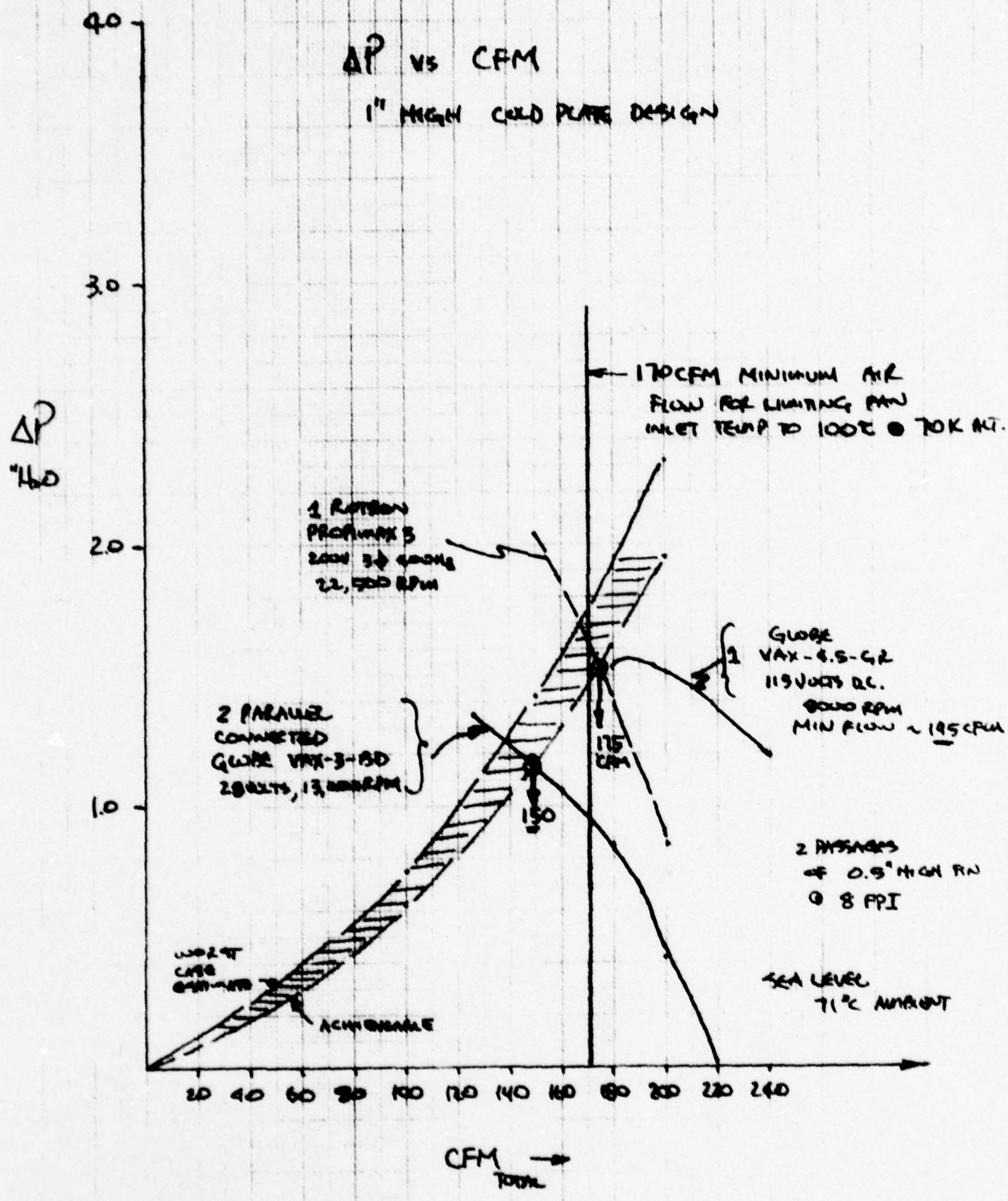
CFM	$\Delta P_{@.075}$	$\Delta P_{@.0635}$
195	1.8	1.53
210	1.75	1.45
240	1.40	1.19
	("H_2O)	("H_2O)

ROTRON PROPIMAX 3 341JS 200VOLTS 3φ 400 Hz INPUT POWER = 80 WATTS

22,500 RPM

6000 HRS LIFE @ 100°C FAN INLET

CFM	$\Delta P_{@.075}$	$\Delta P_{.0635}$
150	2.4	2.04
175	1.8	1.53
200	1.0	0.85
	"H_2O	"H_2O


ΔP vs CFM
1" HIGH COLD PLATE DESIGN
4.0
3.0
2.0
1.0
ΔP
"H2O
170CFM MINIMUM AIR FLOW FOR LIMITING FAN INLET TEMP TO 100°C @ 70K ALT.
1 ROTRON PROPIMAX 3
22,500 RPM
GLOBE VAX-4.5-GR
115VOLTS DC.
8000 RPM
MIN FLOW ~ 195CFM
2 PARALLEL CONNECTED GLOBE VAX-3-BD
175 CFM
150
2 PASSAGES of 0.9" HIGH FIN @ 8 FPI
WORST CASE ESTIMATE
ACHIEVABLE
SEA LEVEL
71°C AMBIENT
20 40 60 80 100 120 140 160 180 200 220 240
CFM TOTAL

SINGLE PASSAGE (.375") DESIGN

FLOW ~100 CFM

AT S.L. $\omega = .0635 \times 100 = 6.35 \frac{lb}{min}$ → $\frac{6.35\ lb/min}{0.3\ KW} = 21.2 \frac{lb}{min\ KW}$

AT 50K $\omega = .0068 \times 100 = .68 \frac{lb}{min}$ → $\frac{0.68}{0.3\ KW} = 2.3 \frac{lb}{min\ KW}$

1" HIGH DESIGN, FLOW ~ 170 CFM

AT S.L., $\omega = .0635 \times 170 = 10.8 \frac{lb}{min}$ → $\frac{10.8}{0.3} = 36. \frac{lb}{min\text{-}KW}$

AT 70K, $\omega = .00261 \times 170 = 0.444 \frac{lb}{min}$ → $\frac{.444}{0.3} = 1.48 \frac{lb}{min\text{-}KW}$

ECS FLOW

AT $T_{AIR\ EXHAUST} = 160°F$, MAX

$$Q = \omega c_p (T_{AIR\ OUT} - T_{AIR\ IN}) 60, \quad BTU/HR$$

$$300 \times 3.413 = \omega (.24) [160 - T_{AIR\ IN}] 60$$

$$71.1 = \omega (160 - T_{AIR\ IN})$$

$$\omega = \frac{71.1}{160 - T_{AIR\ IN}}, \quad lb/min$$

$T_{AIR\ IN}$	ω, lb/min	lb/min·KW
0°F (-17.7°C)	0.44	1.47
50°F (10°C)	0.65	2.17
90°F (32.2°C)	1.02	3.40
125°F (51.7°C)	2.03	6.77

AT 90°F INLET AIR & 1.02 lb/min (TOTAL FLOW)

$\eta_{CARD\ ASSY}$ = 0.92
@ 0.51 lb/min

$\eta_{P/S}$ = 0.67
@ 0.51 lb/min

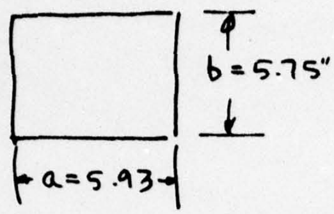
$$T_{CARD\ ASSY} = 90°F + \frac{3.413 \times 165}{1.02 \times 14.4 \times .92} = 131.7°F \ (55.4°C)$$

$T_{AIR\ IN\ P/S}$ = 128.3°F

$$T_{P/S} = 128.3 + \frac{3.413 \times 135}{1.02 \times 14.4 \times .67} = 175.1°F \ (79.5°C)$$

@ 1.02 lb/min $\Delta P \sim 0.2''H_2O$

PC BOARD . . . 10 WATTS MAXIMUM



PC BOARD RISE ABOVE CARD EDGE } $\Delta T_{MAX} = \dfrac{1.9\, Q\, a}{8 K A_{eff}}$, °C (Q: WATTS)

$$\Delta T_{MAX} = \left(\frac{1.9 \times 10 \text{ watts} \times 5.93 \text{ inches} \times 12 \text{ inch/ft}}{8\ K\ b\ t\ (\%\ \text{coverage})}\right), °C$$

t: CONDUCTOR THICKNESS (CONTIGUOUS!!!)

$$\Delta T_{MAX} = \frac{29.4}{K\ t\ (\%\text{coverage})}, °C$$

% coverage	t (inches)	K (BTU/hr ft °F)		ΔT_{MAX} (°C)
30%	.003	220.	(Cu)	148.5
30%	.004	220.	(Cu)	111.4
30%	.050	100.	(Al)	19.6
50%	.050	100.	(Al)	11.8

WITH LOK-TAINER CLIPS . . . . $\sim 15 \dfrac{°C \cdot inch}{watt} \times \dfrac{1}{5.75\, inch} = 2.6°C/W$

$$\therefore \Delta T_{CLIP} = \frac{10 \text{ watts}}{2} \times 2.6 = 13°C$$

WITH "WEDGE" LOCKS CAN LIMIT CLIP RISE TO 2°C

∴ FOR MAX BOARD .. @ 10 WATTS , ALUM

MAX CARD RISE ABOVE COLD PLATE TEMP....

BEST

PC BD RISE WITH 50 MIL ALUMIN OVERLAY ...	11.8°C
WEDGE LOCK . . . . - - - -	2.0°C
SPREADING GRADIENT AT COLD PLATE WALL....	2.0°C
(NOTE: DIPS ARE INTIMATE CONTACT WITH OVERLAY)	15.8°C
	~16°C

WORST

PC BD RISE WITH 50 MIL ALUM OVERLAY ..	11.8
"LOK-TAINER" - - - - - - - - -	13.0
SPREAD GRADIENT	2.0
	26.8 °C
	~27°C

10 WATT PC BOARD

$$\therefore T_{\substack{\text{DIP MTG} \\ \text{SURF TEMP}}} = T_{\substack{\text{CARD} \\ \text{ASSY} \\ \text{HEAT SINK}}} + 16 \text{ , °C}$$ "WEDGE LOCKS"

$$T_{\substack{\text{DIP MTG} \\ \text{SURF TEMP}}} = T_{\substack{\text{CARD ASSY} \\ \text{HEAT SINK}}} + 27 \text{ , °C}$$ "LOK TAINER"

APPENDIX 3

ILLUSTRATIONS

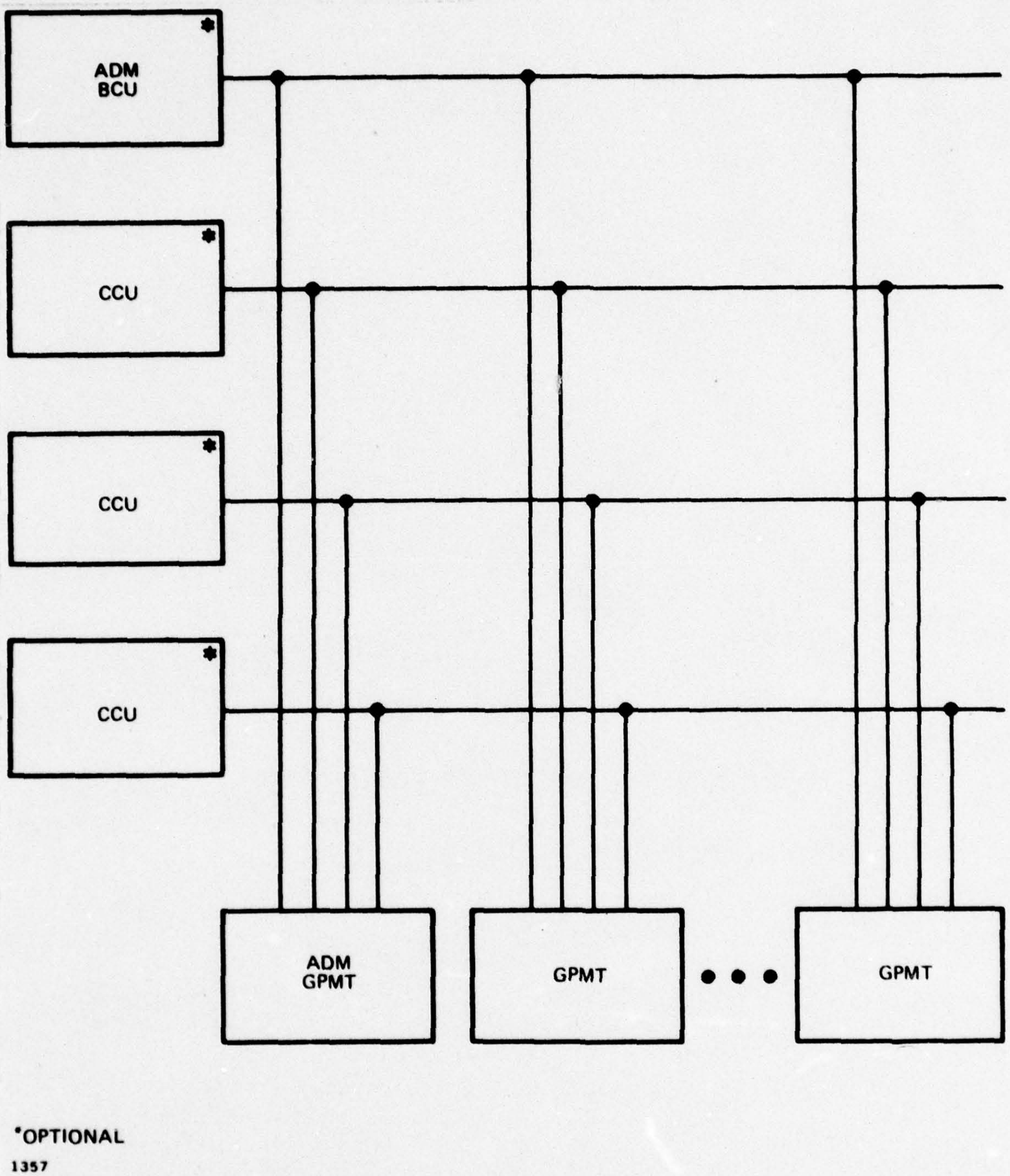


FIG. 1 GENERAL PURPOSE MULTIPLEX SYSTEM

Telephonics

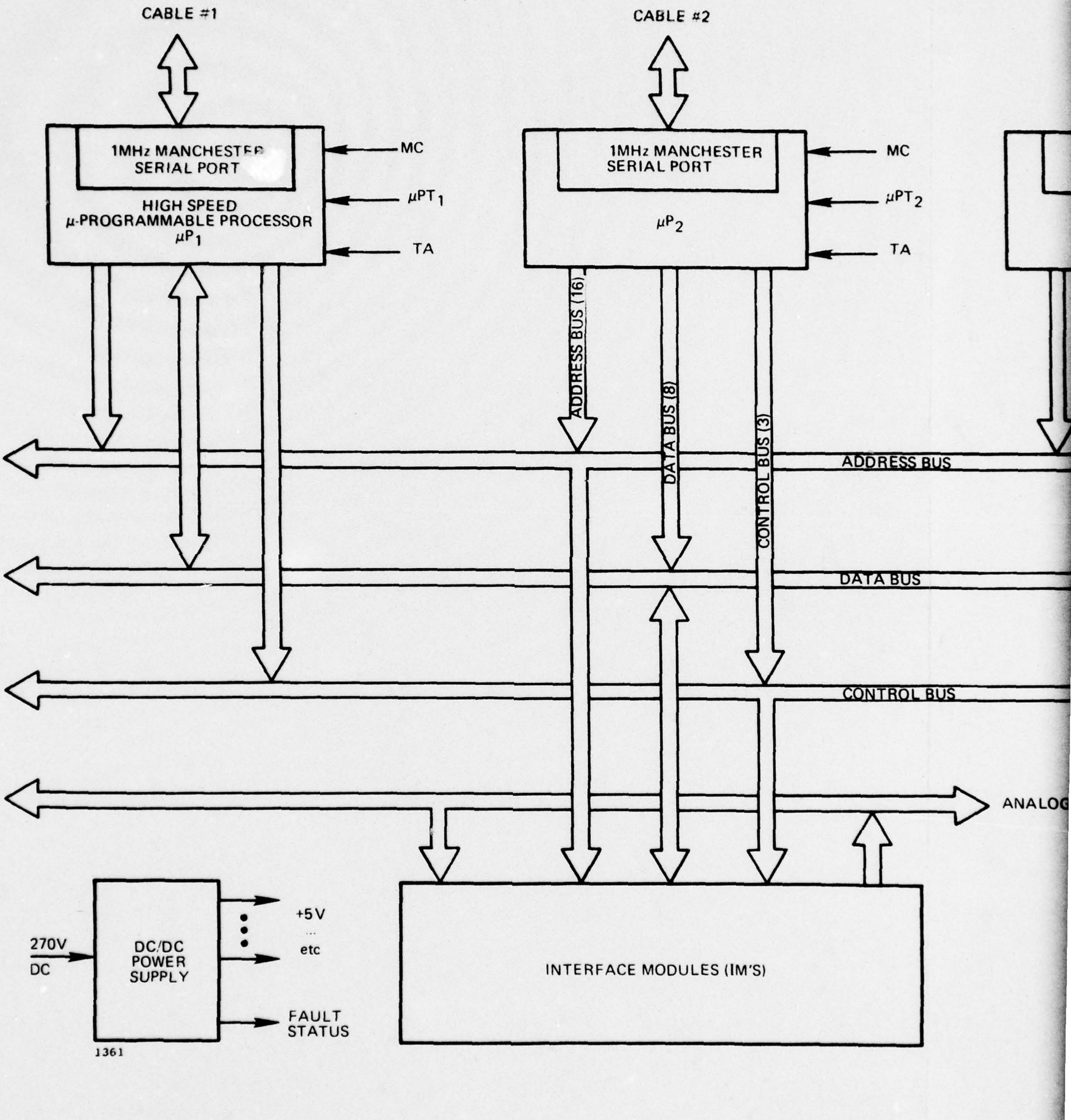
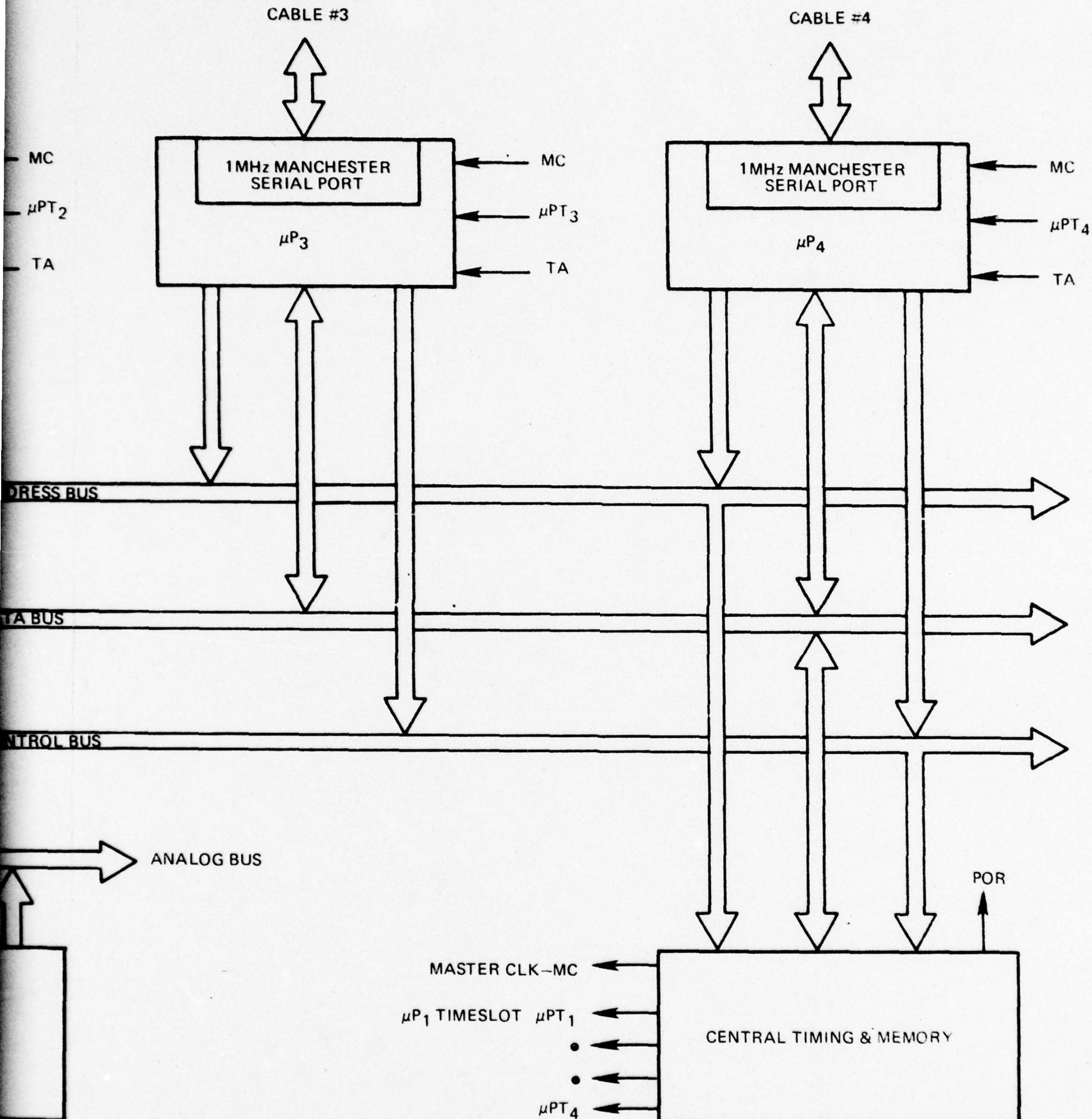


FIG. 2 GENERAL PURPOSE MULTIPLEX TERMINAL

Telephonics


CABLE #3
CABLE #4
MC
µPT2
TA
1MHz MANCHESTER SERIAL PORT
µP3
MC
µPT3
TA
1MHz MANCHESTER SERIAL PORT
µP4
MC
µPT4
TA
DRESS BUS
TA BUS
NTROL BUS
ANALOG BUS
POR
MASTER CLK–MC
µP1 TIMESLOT µPT1
µPT4
CENTRAL TIMING & MEMORY

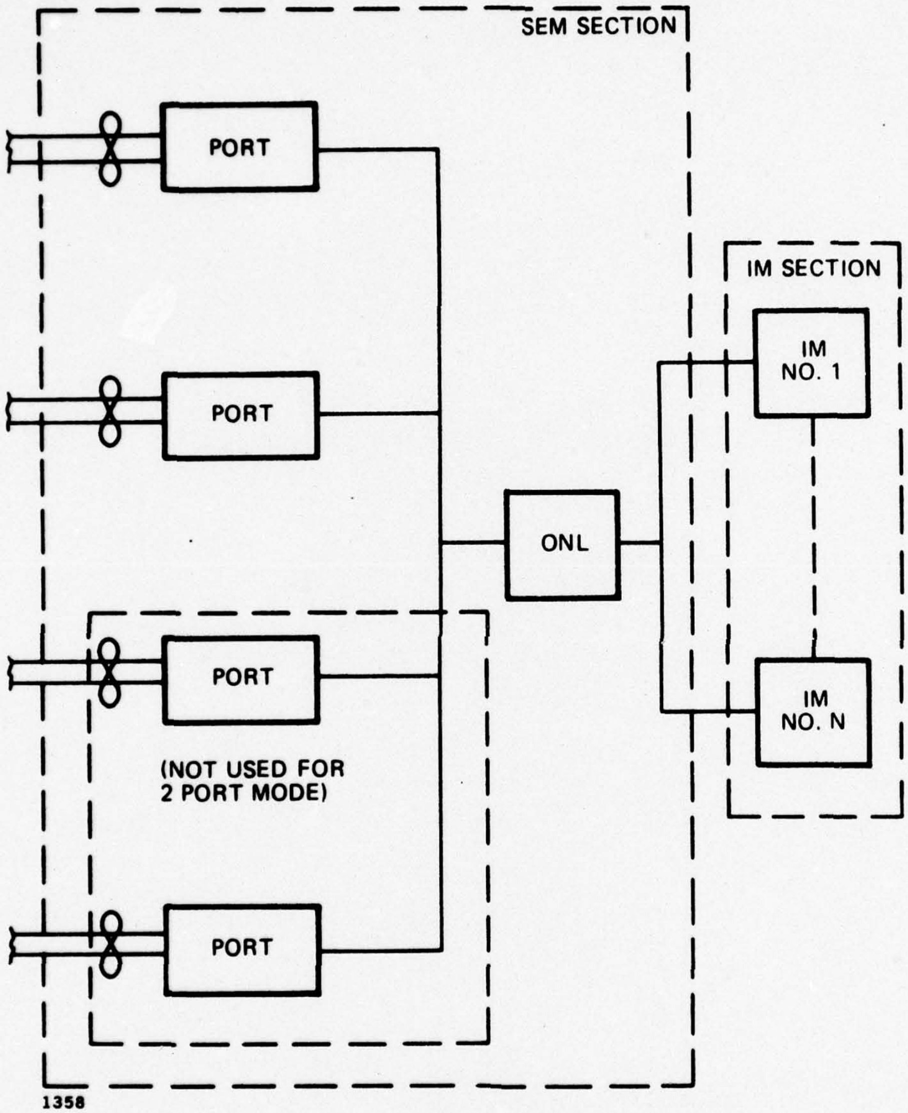


FIG. 3 2/4 PORT BLOCKING DATA TERMINAL

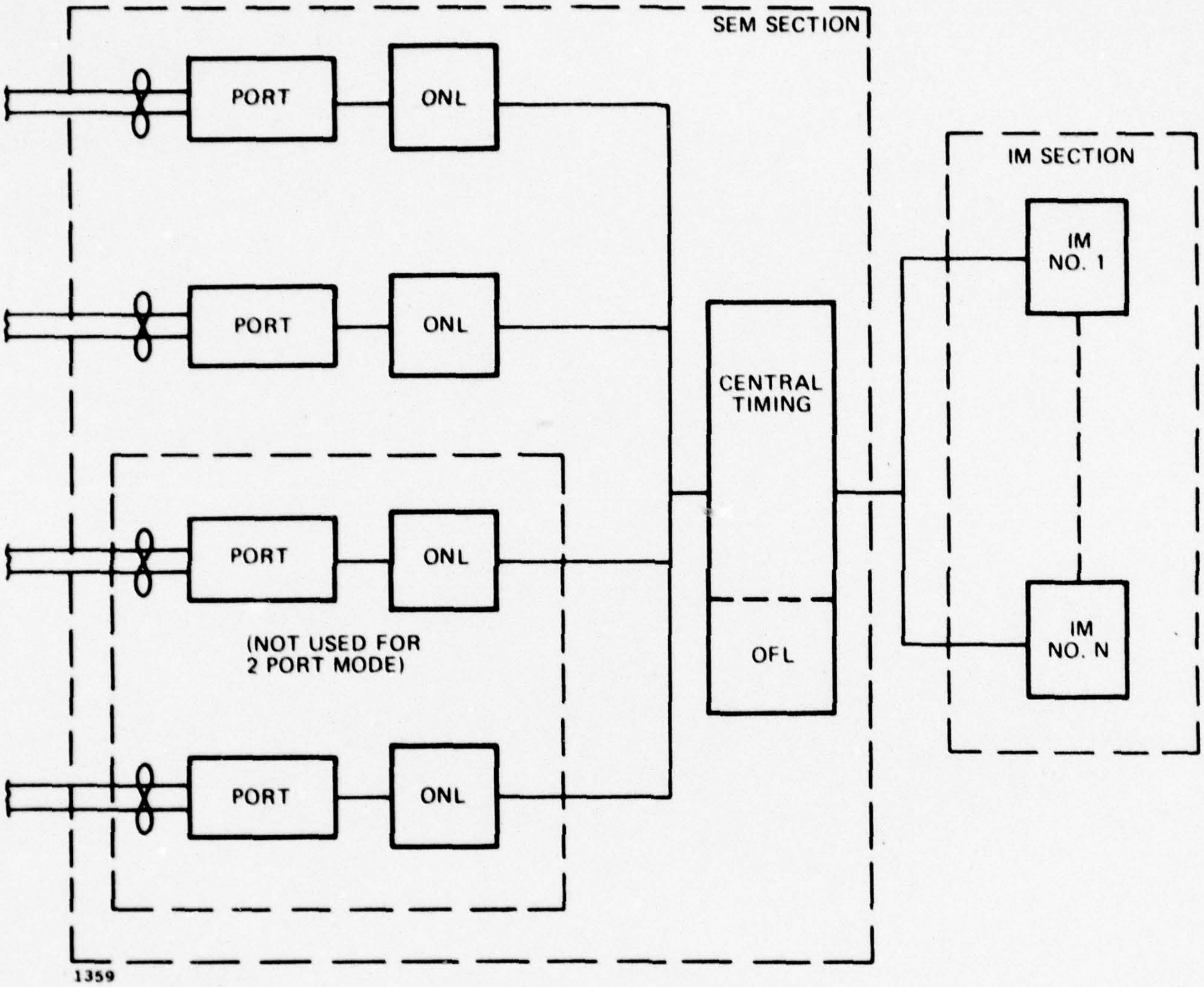


FIG. 4 2/4 PORT NON BLOCKING DATA TERMINAL

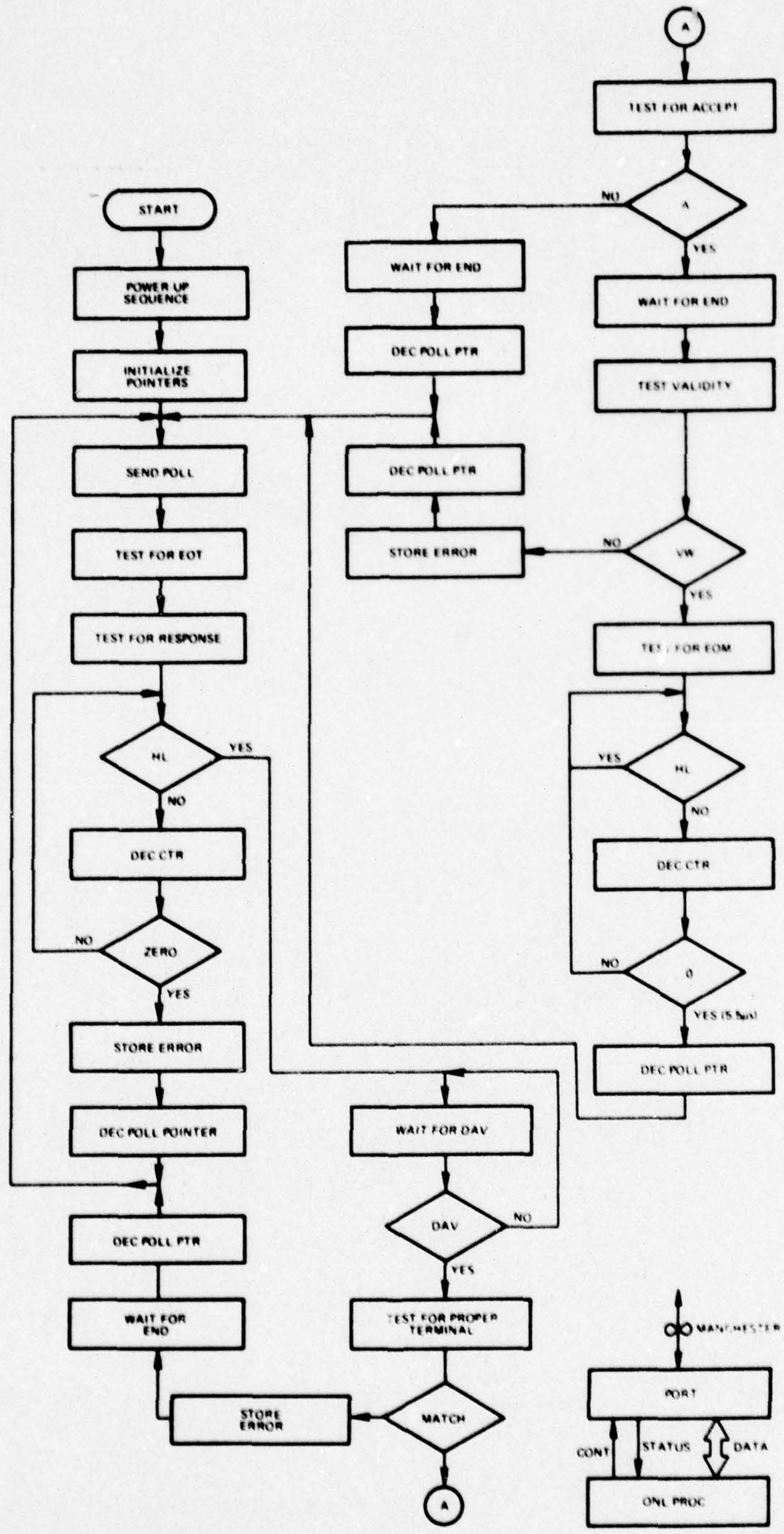


FIG . 5 BUS CONTROL UNIT

Telephonics

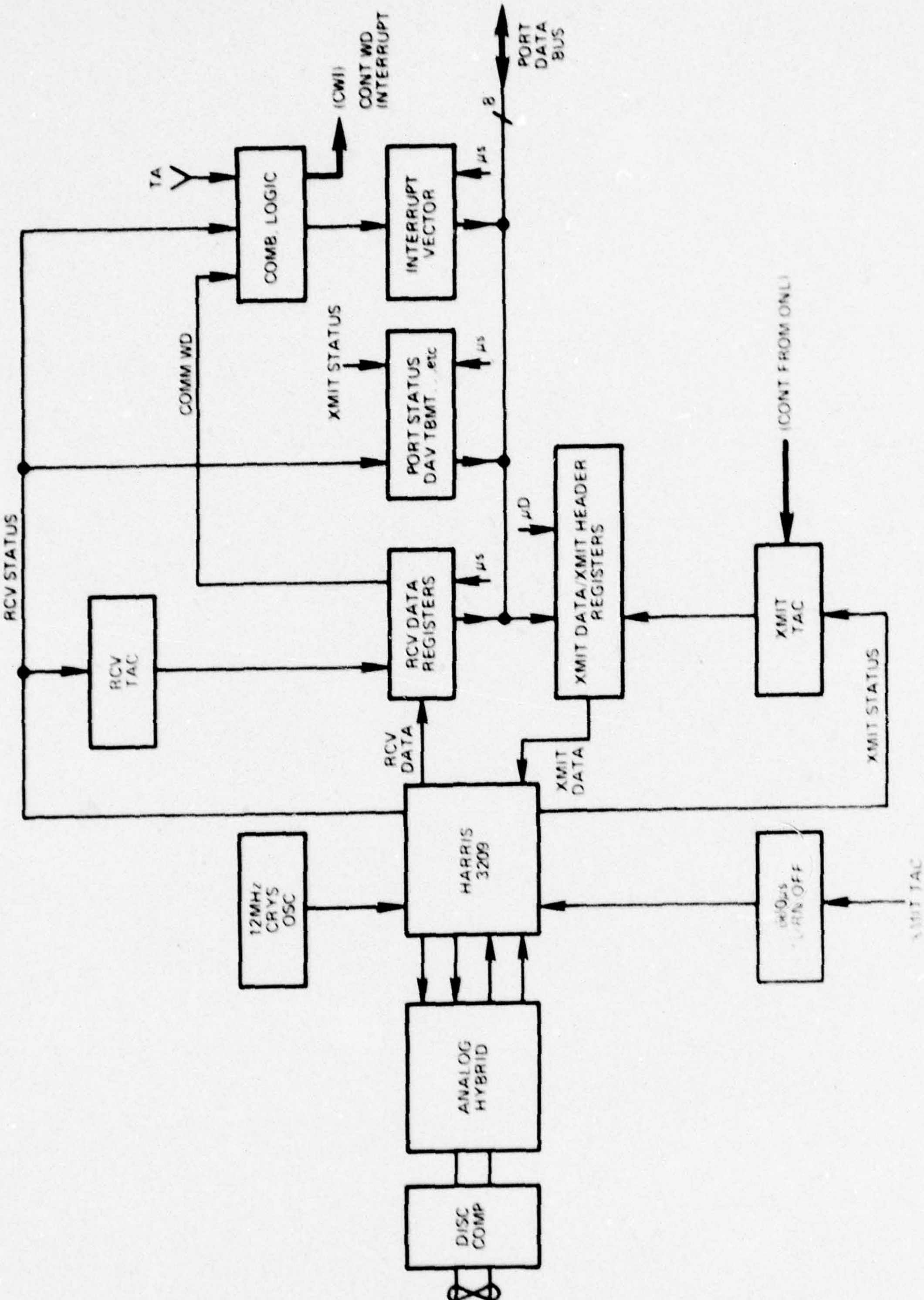


FIG. 6 8 BIT PORT

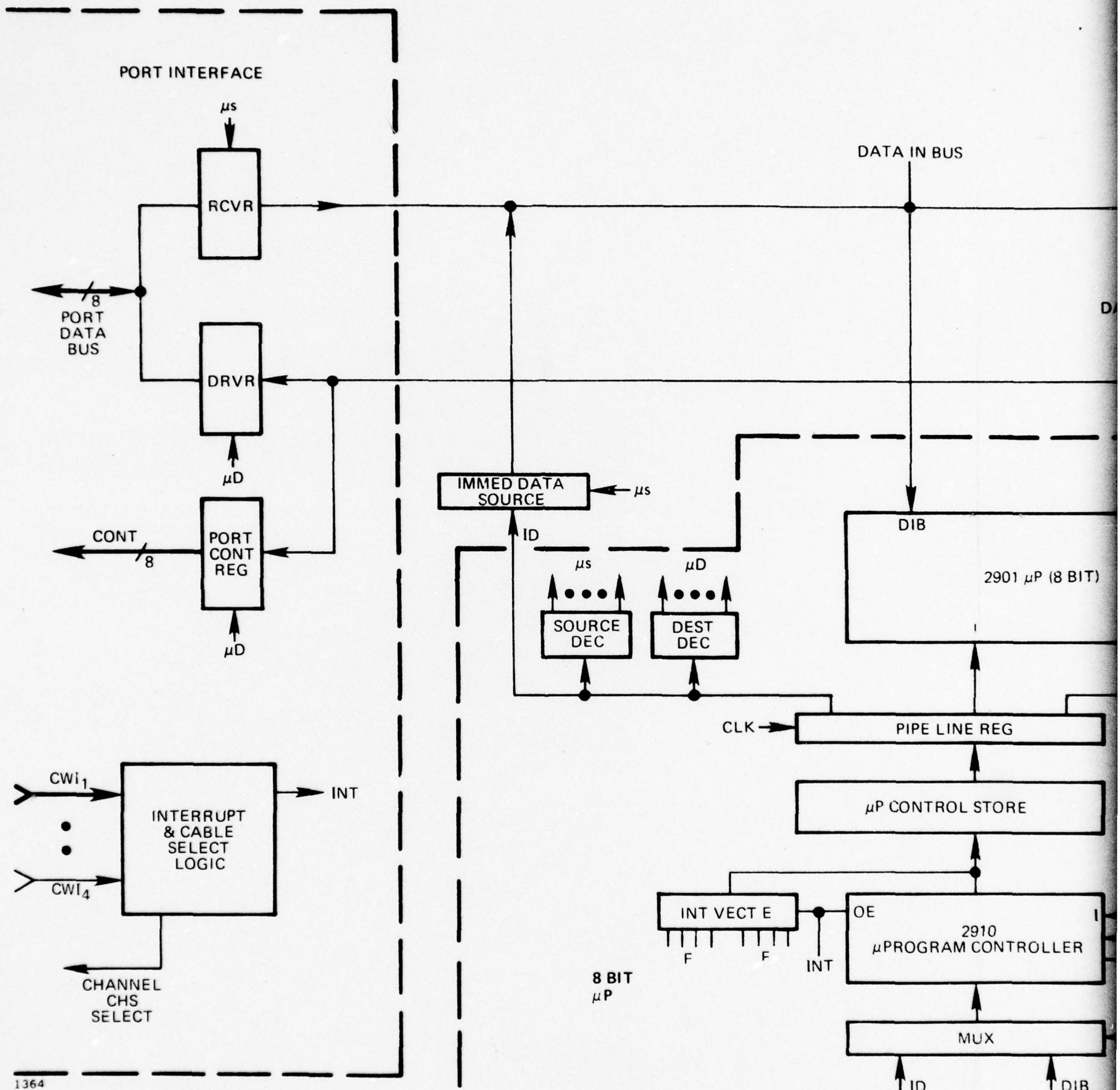
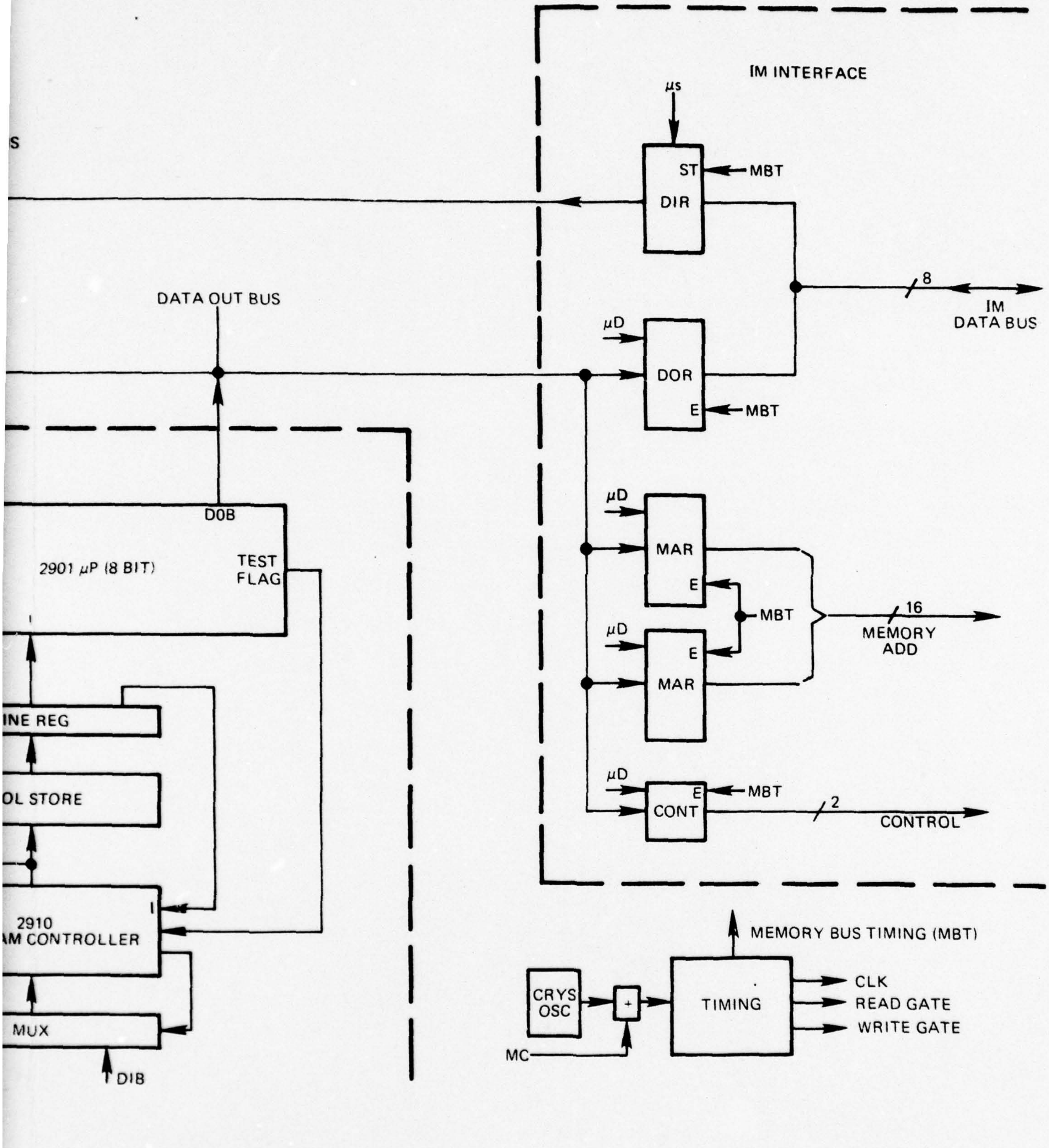


FIG. 7 8 BIT ONL/OFL PROC.



IM INTERFACE
μs
ST
MBT
DIR
8
IM
DATA BUS
DATA OUT BUS
μD
DOR
E
MBT
μD
DOB
MAR
E
MBT
16
MEMORY
ADD
μD
E
MAR
2901 μP (8 BIT)
TEST
FLAG
INE REG
OL STORE
μD
E
MBT
CONT
2
CONTROL
2910
AM CONTROLLER
MEMORY BUS TIMING (MBT)
CRYS
OSC
+
TIMING
CLK
READ GATE
WRITE GATE
MC
MUX
DIB

2

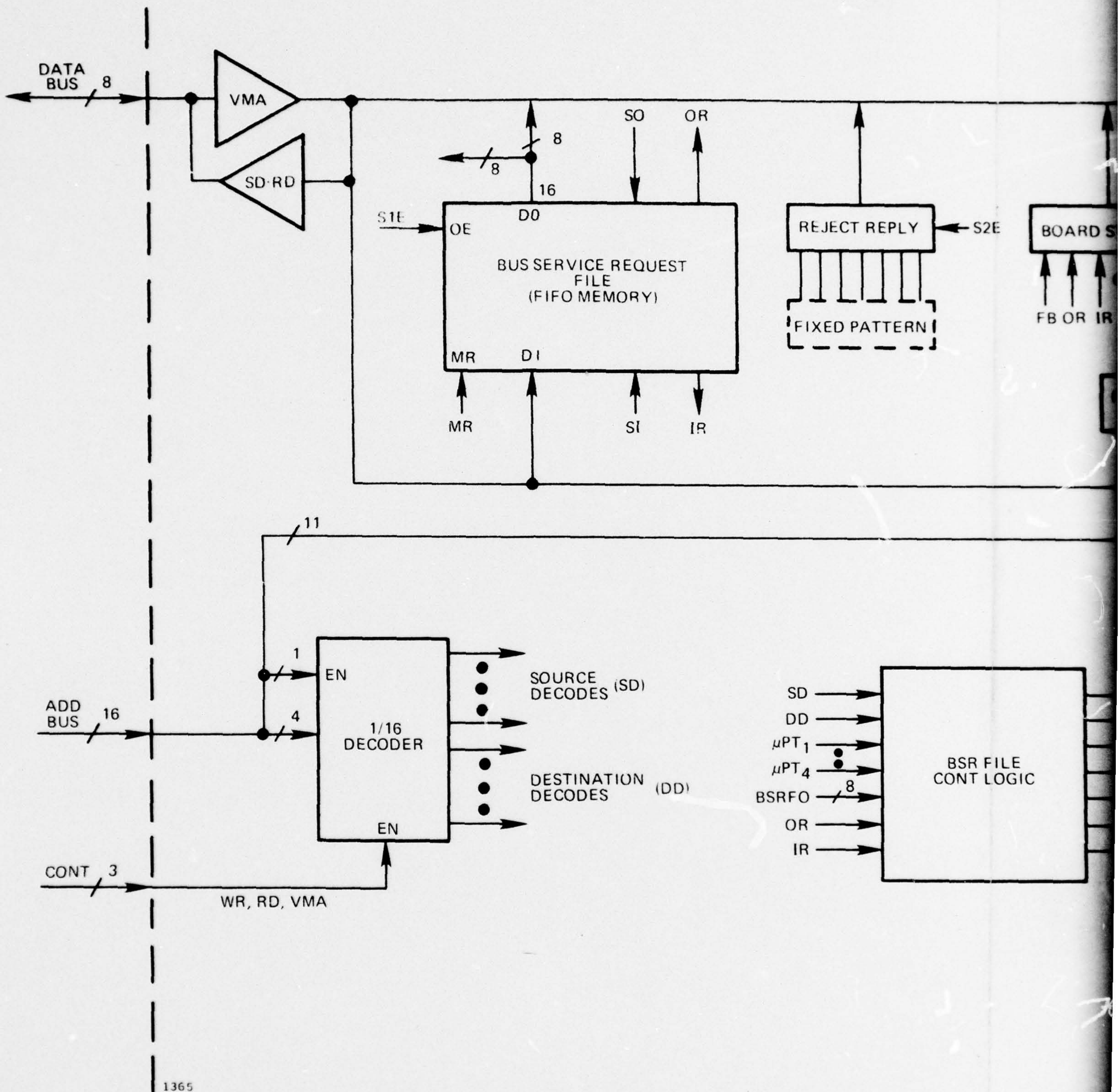
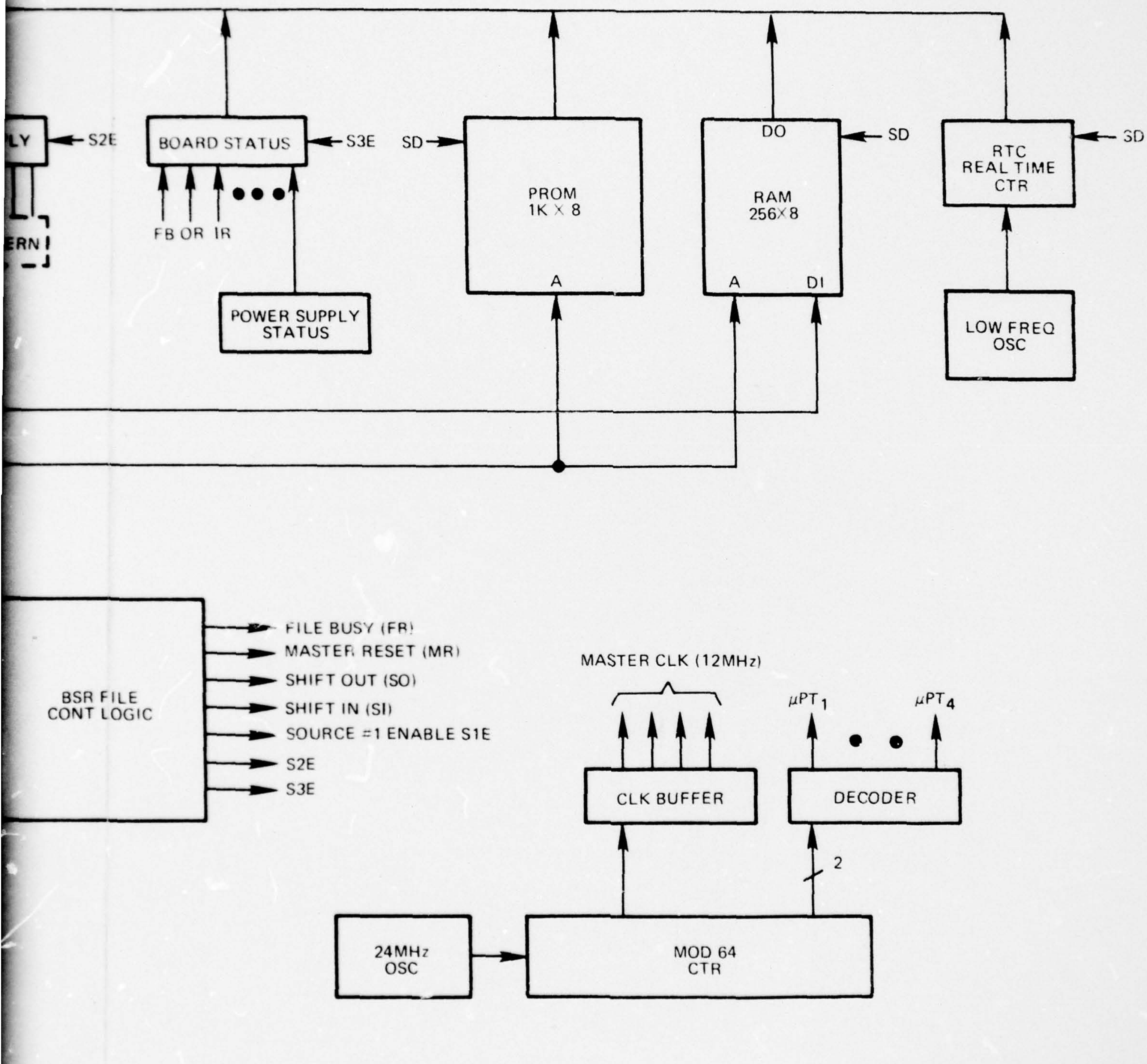


FIG. 8 CENTRAL TIMING & MEMORY



LY
S2E
BOARD STATUS
S3E
SD
PROM
1K × 8
DO
SD
RAM
256×8
RTC
REAL TIME
CTR
SD
ERN
FB OR IR
A
A
DI
POWER SUPPLY
STATUS
LOW FREQ
OSC
BSR FILE
CONT LOGIC
FILE BUSY (FB)
MASTER RESET (MR)
SHIFT OUT (SO)
SHIFT IN (SI)
SOURCE #1 ENABLE S1E
S2E
S3E
MASTER CLK (12MHz)
μPT 1
μPT 4
CLK BUFFER
DECODER
2
24MHz
OSC
MOD 64
CTR

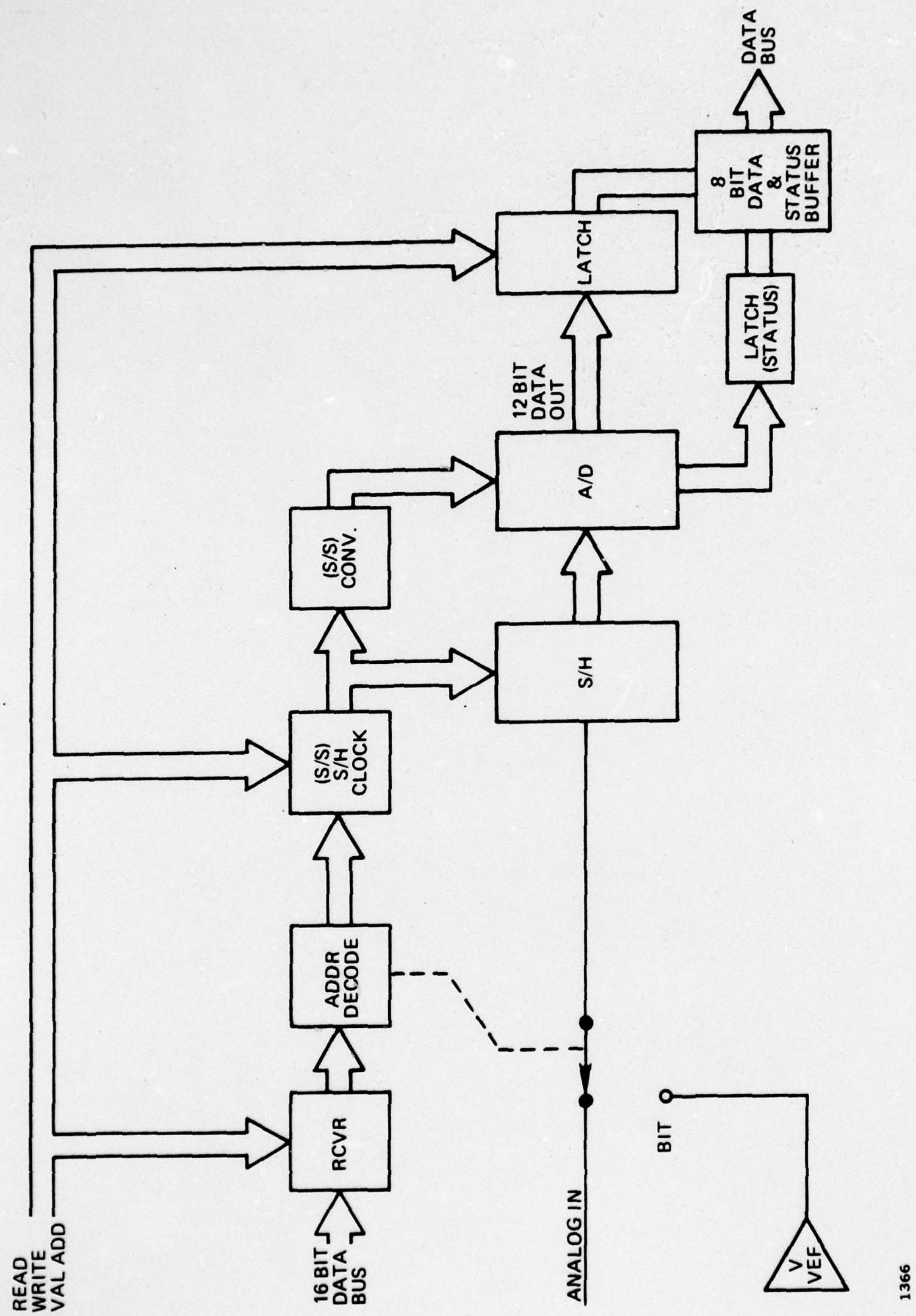


FIG. 9 CENTRAL A/D

Telephonics

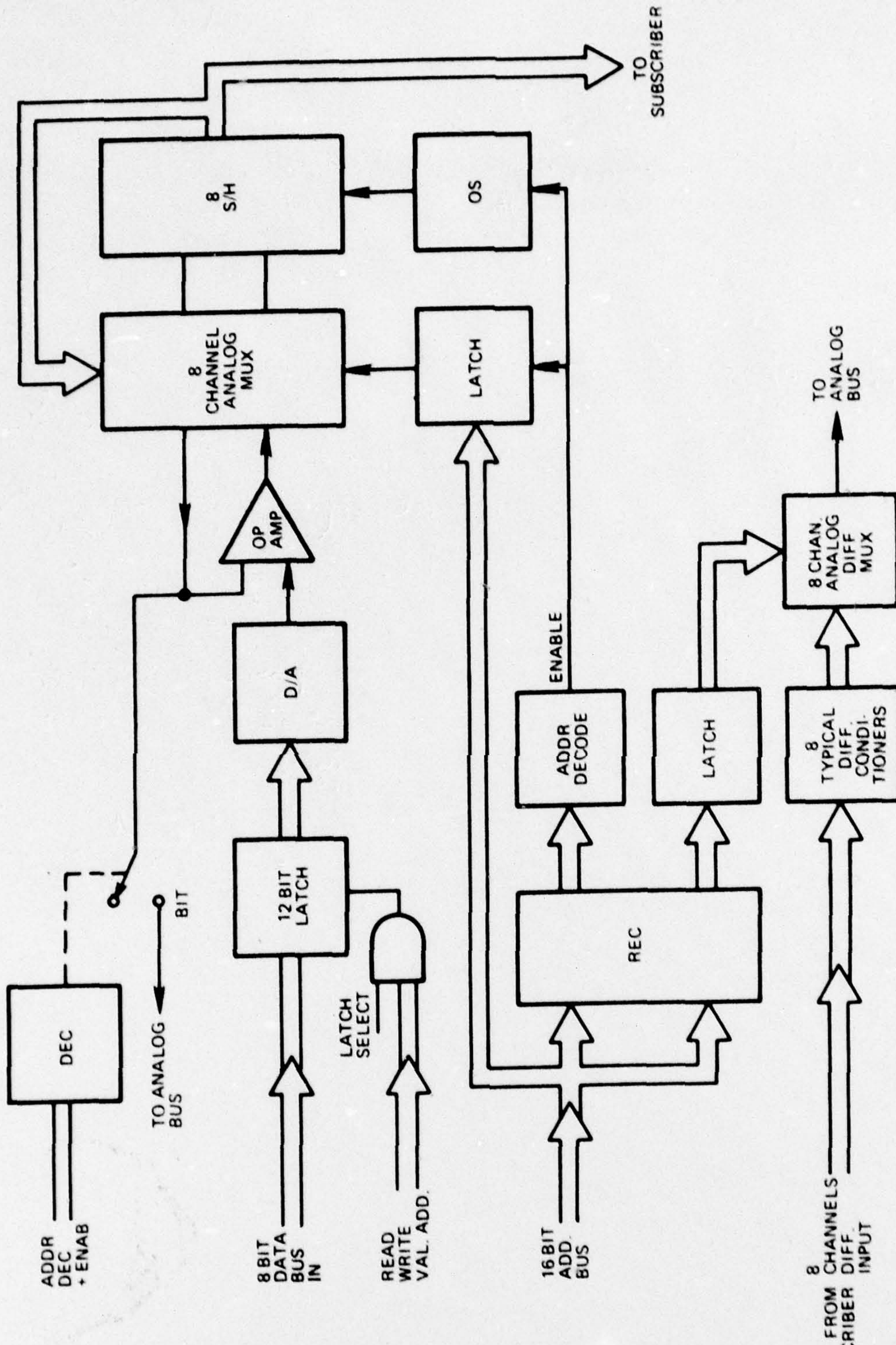


FIG. 10 ANALOG IM

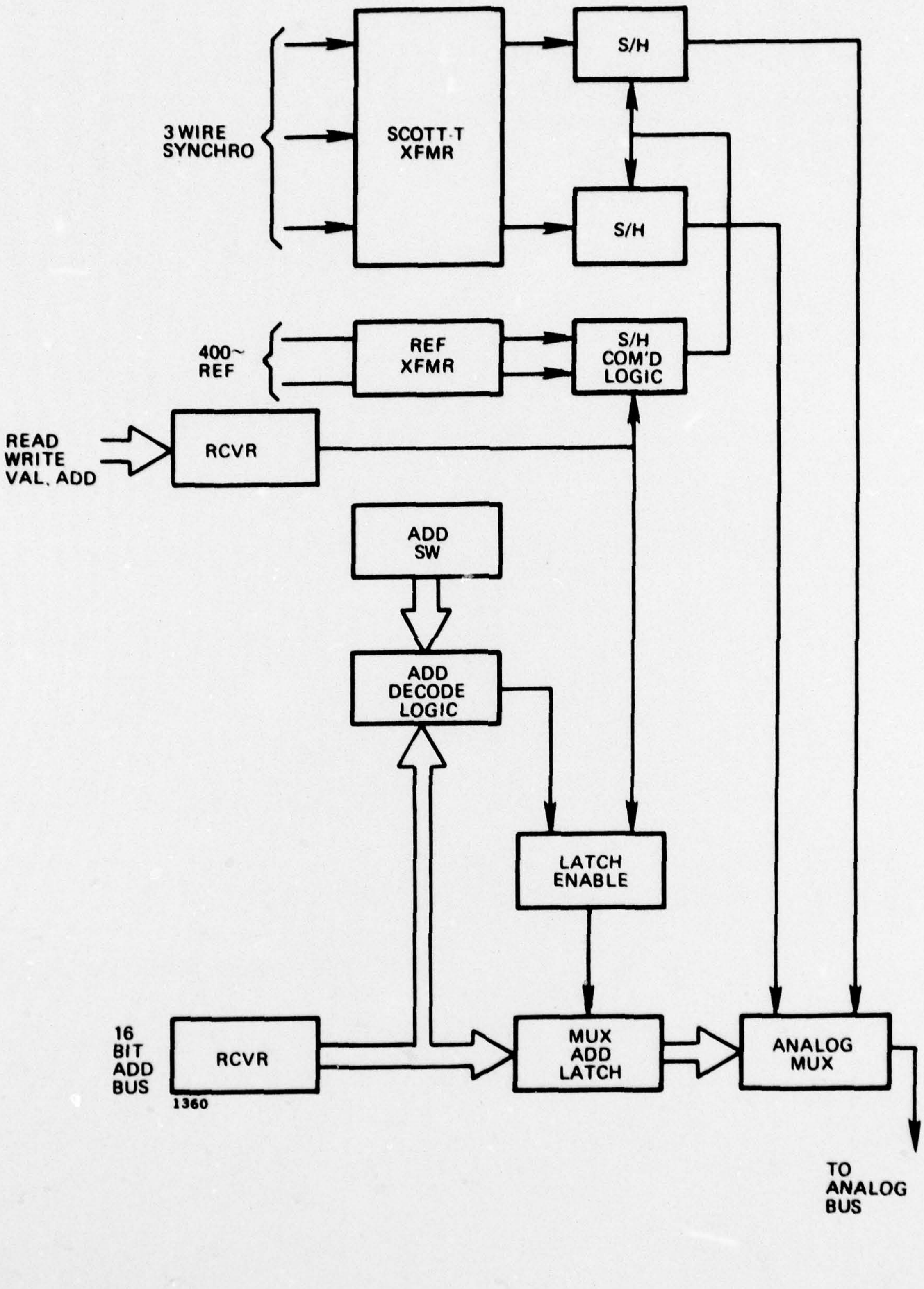


FIG. 11 S/D IM

Telephonics

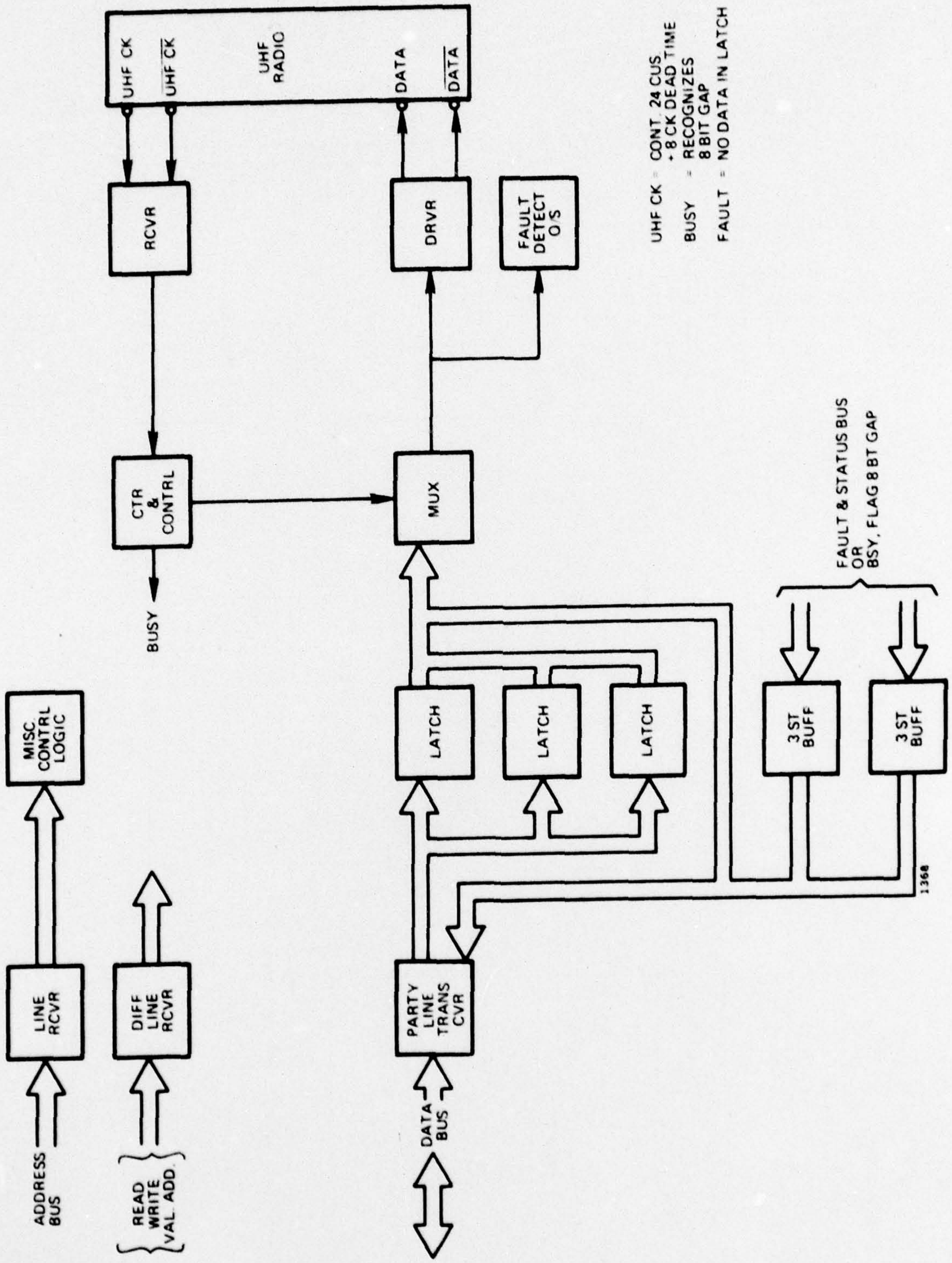


FIG. 12 UHF - SER (DATA) IM

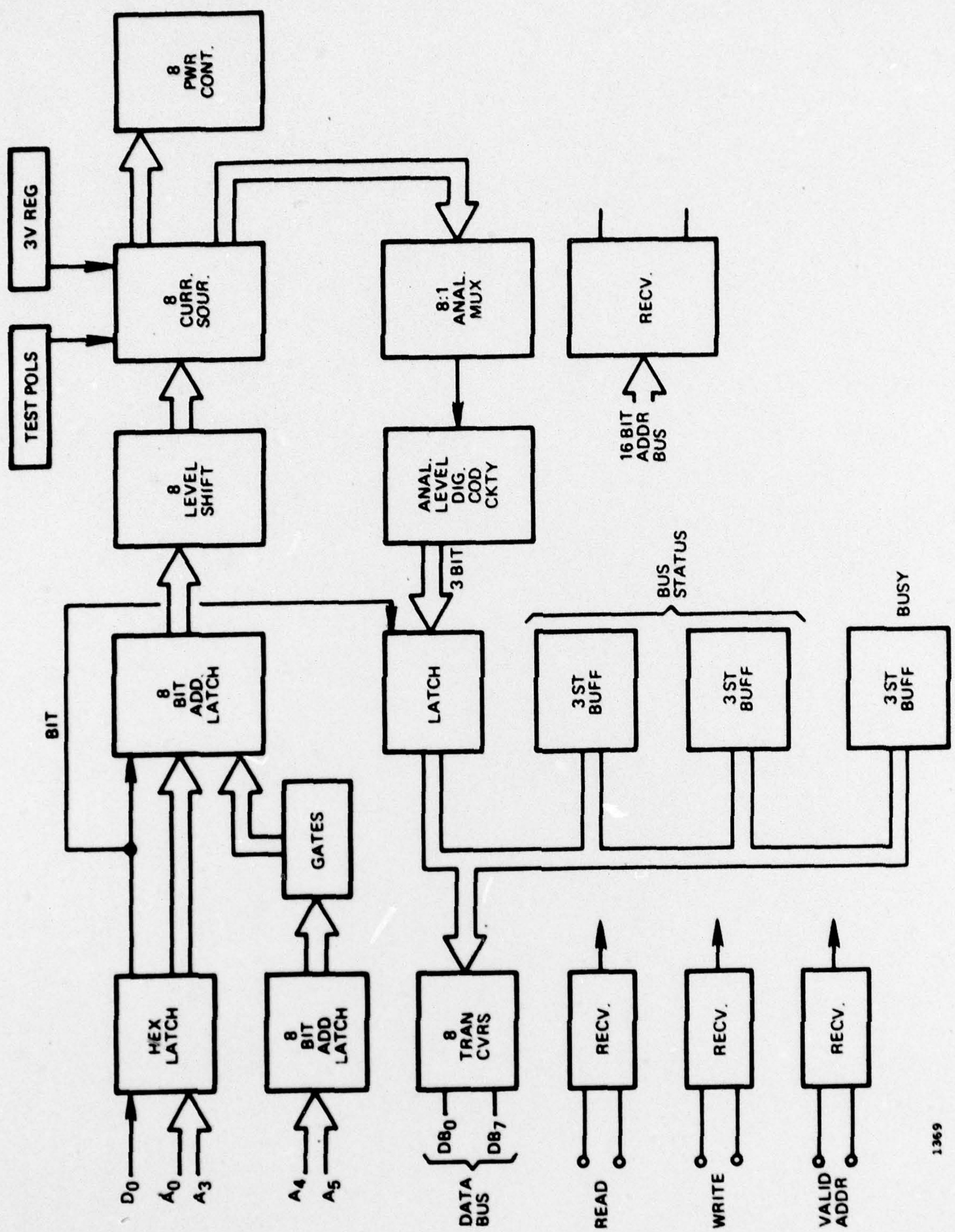


FIG. 13 SOSTEL IM

Telephonics

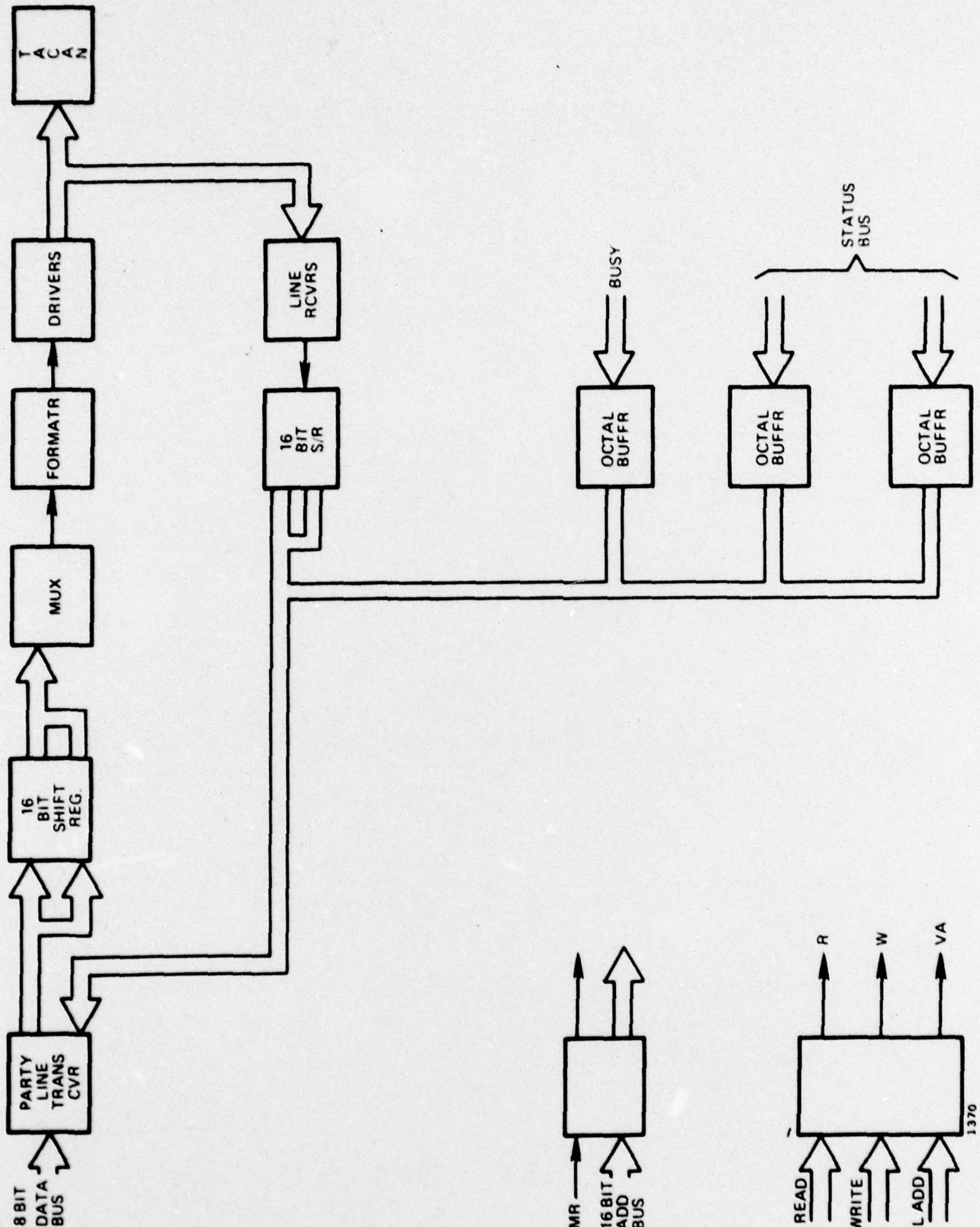


FIG. 14 TACAN IM

Telephonics

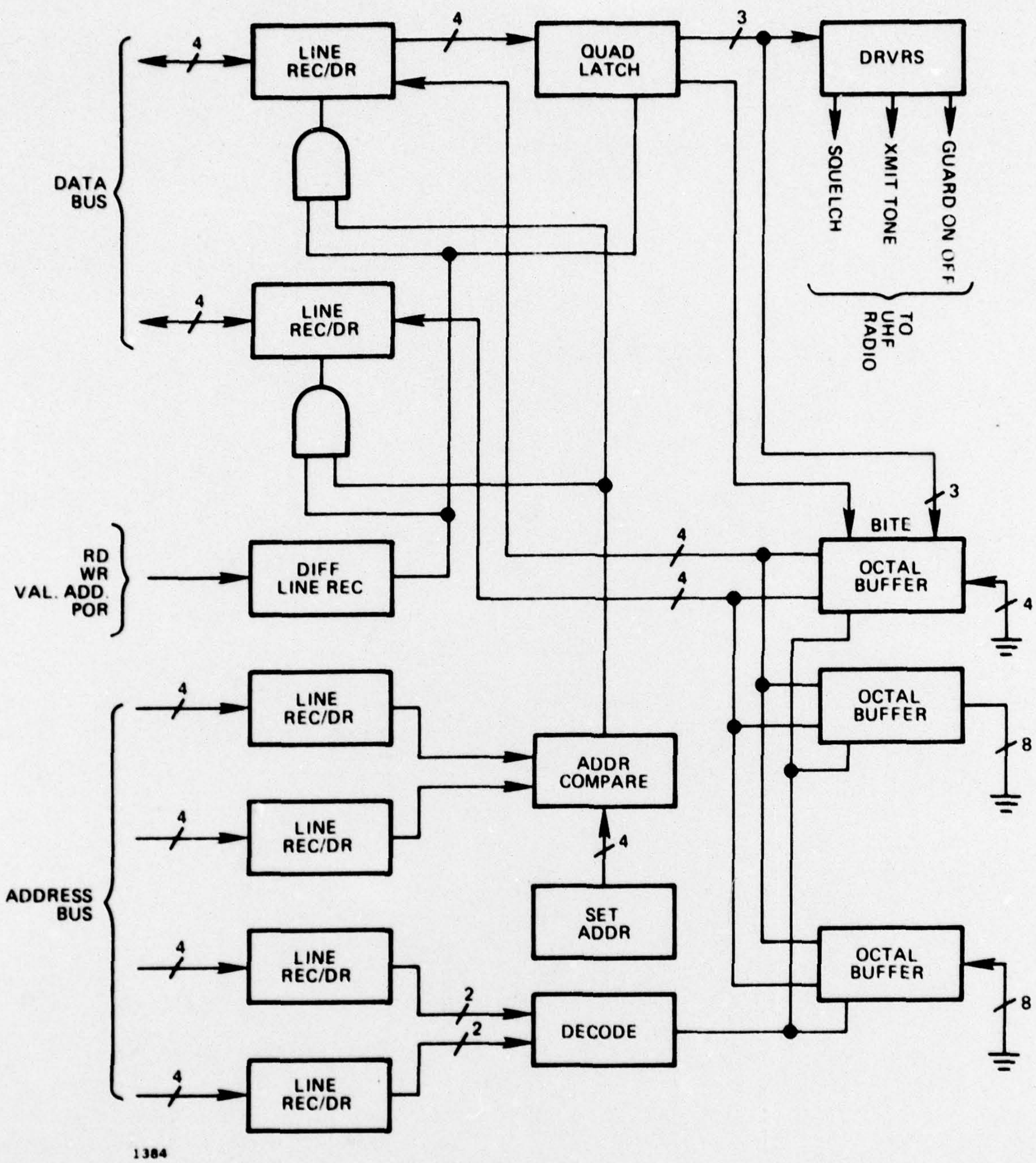


FIG. 15 UHF DISCRETE IM

Telephonics

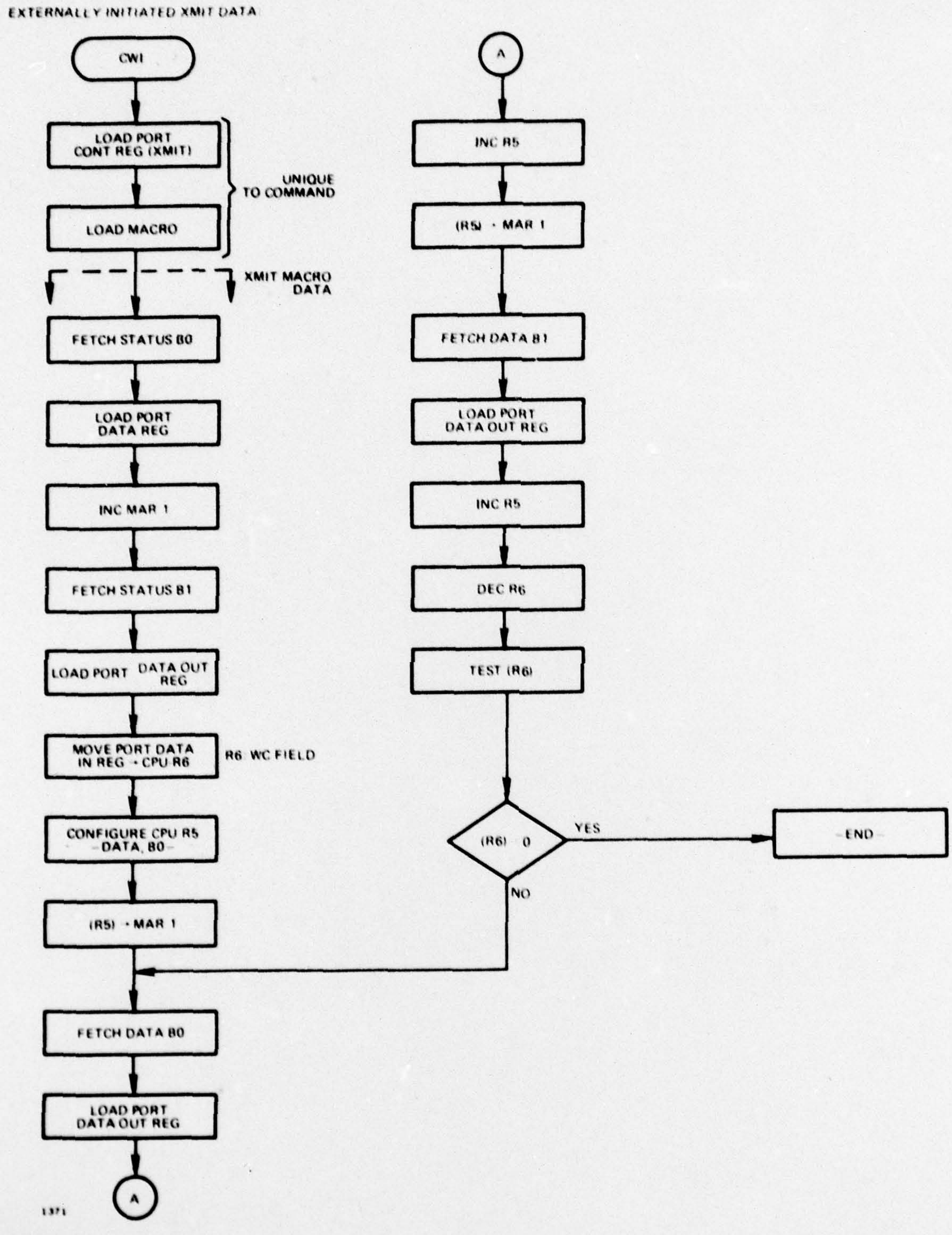


FIG. 16 TYPICAL ONL PROGRAM MODULE

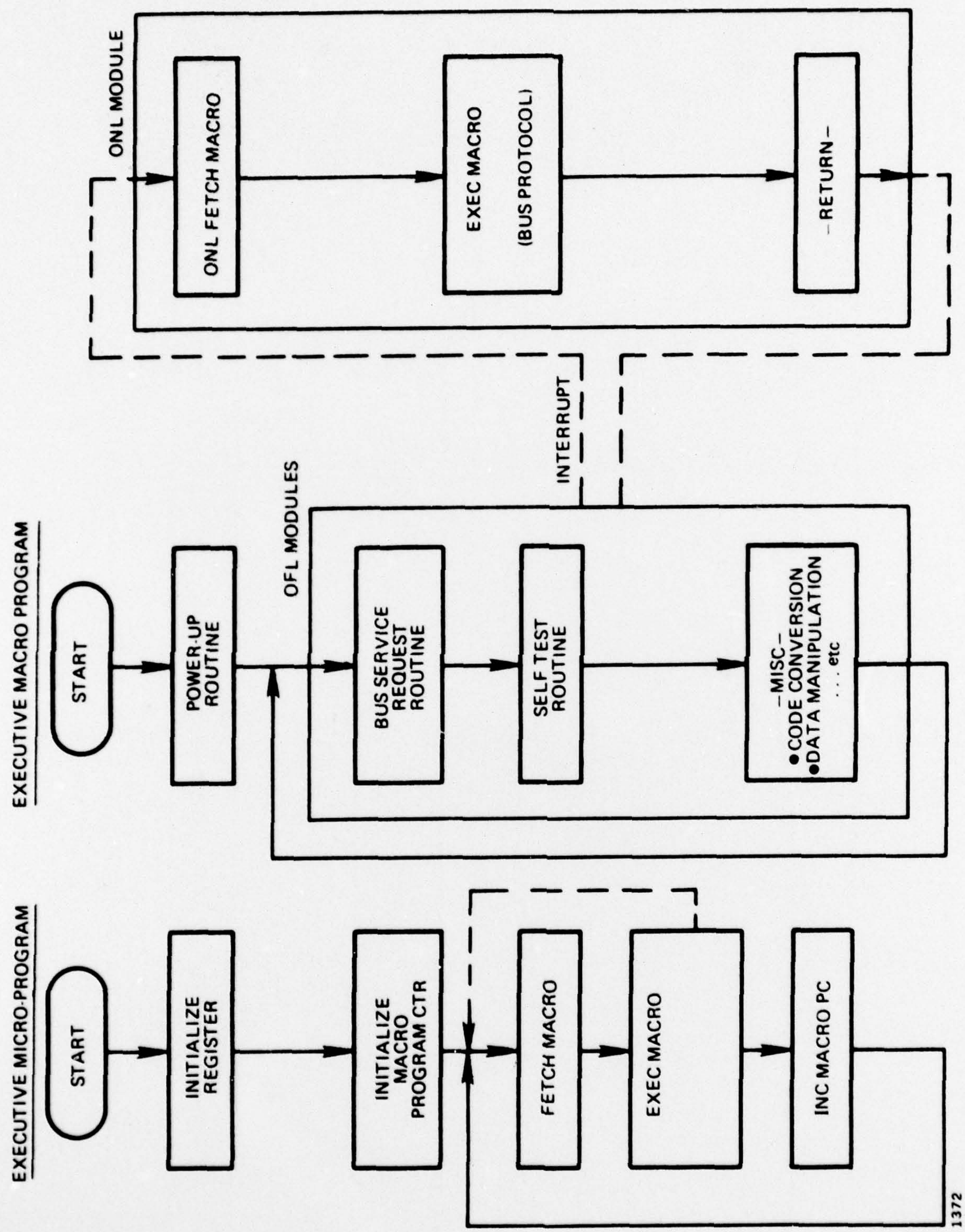


FIG. 17 TYPICAL MICRO & MACRO PROGRAM FLOW CHARTS

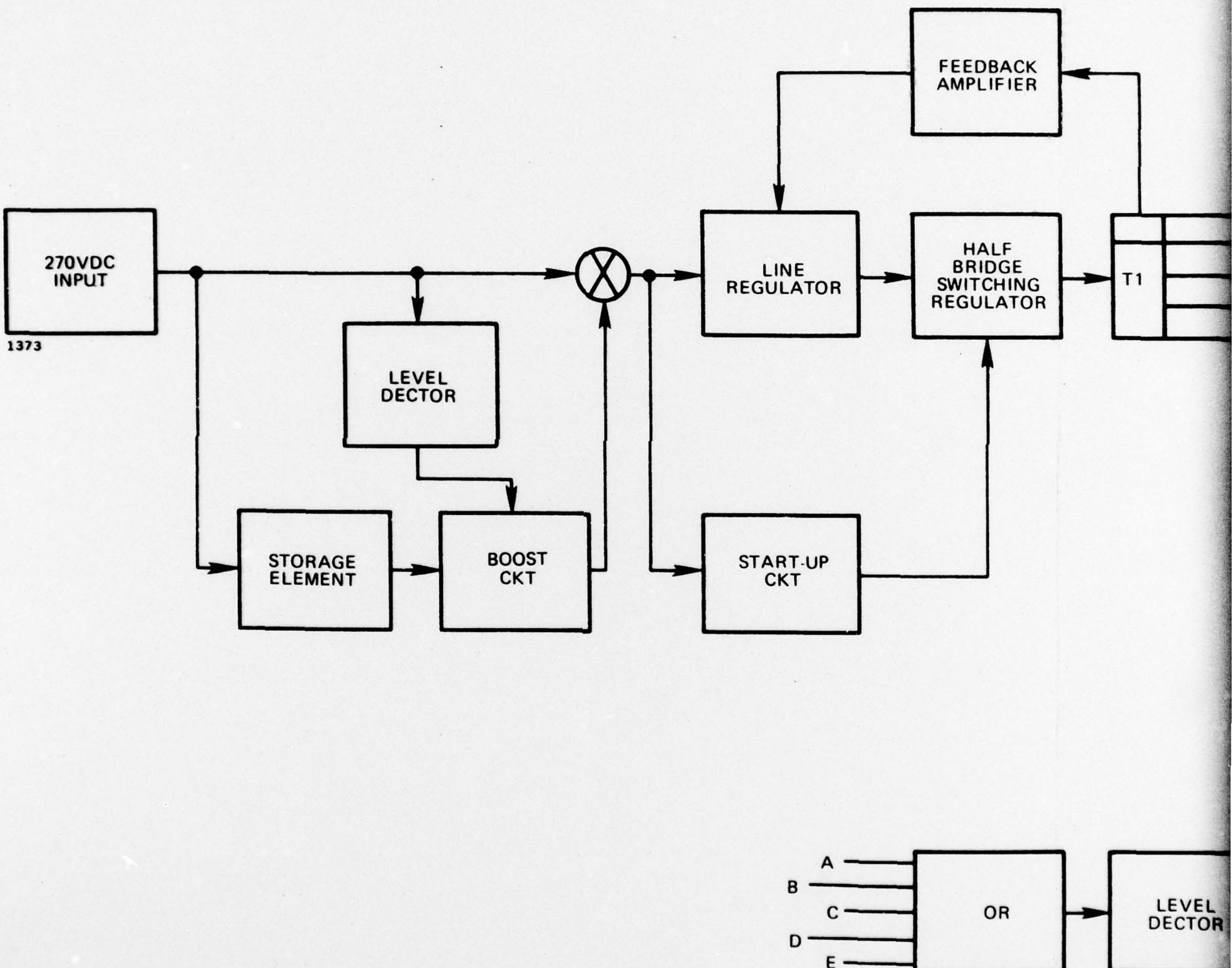
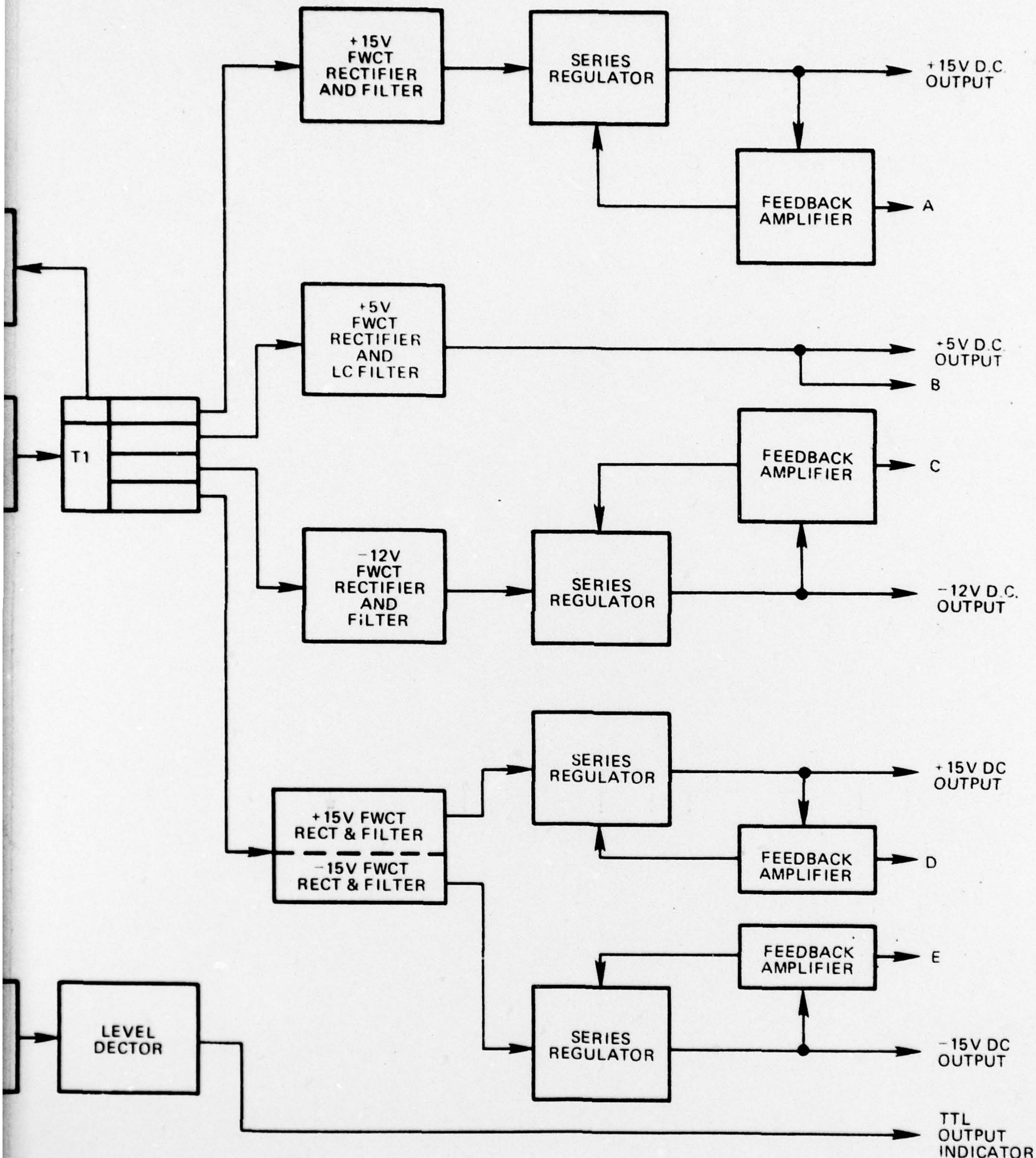


FIG. 18 POWER SUPPLY

1

Telephonics


+15V
FWCT
RECTIFIER
AND FILTER
SERIES
REGULATOR
+15V D.C.
OUTPUT
FEEDBACK
AMPLIFIER
A
+5V
FWCT
RECTIFIER
AND
LC FILTER
+5V D.C.
OUTPUT
B
T1
FEEDBACK
AMPLIFIER
C
−12V
FWCT
RECTIFIER
AND
FILTER
SERIES
REGULATOR
−12V D.C.
OUTPUT
SERIES
REGULATOR
+15V DC
OUTPUT
+15V FWCT
RECT & FILTER
−15V FWCT
RECT & FILTER
FEEDBACK
AMPLIFIER
D
FEEDBACK
AMPLIFIER
E
LEVEL
DECTOR
SERIES
REGULATOR
−15V DC
OUTPUT
TTL
OUTPUT
INDICATOR

2

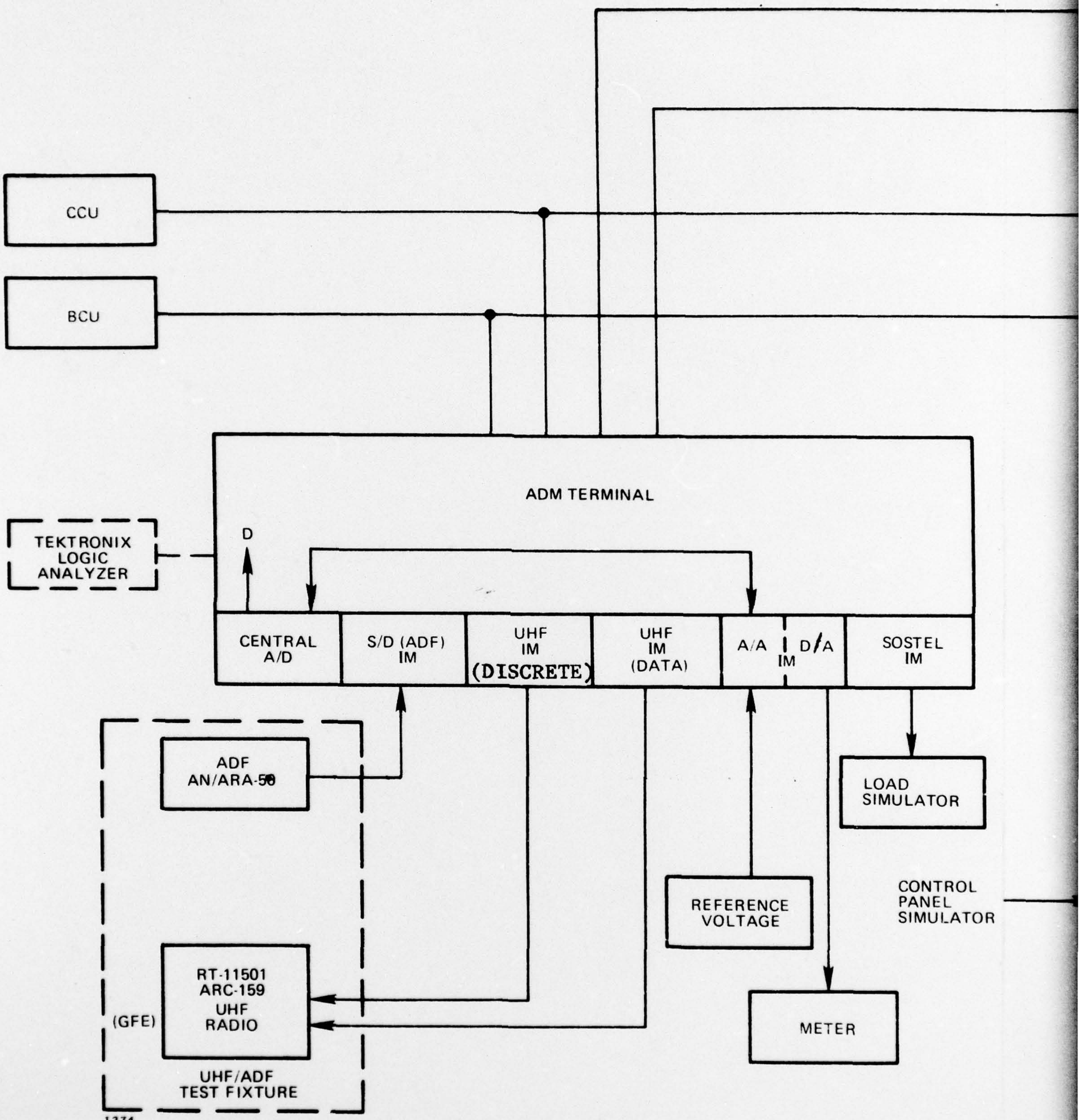
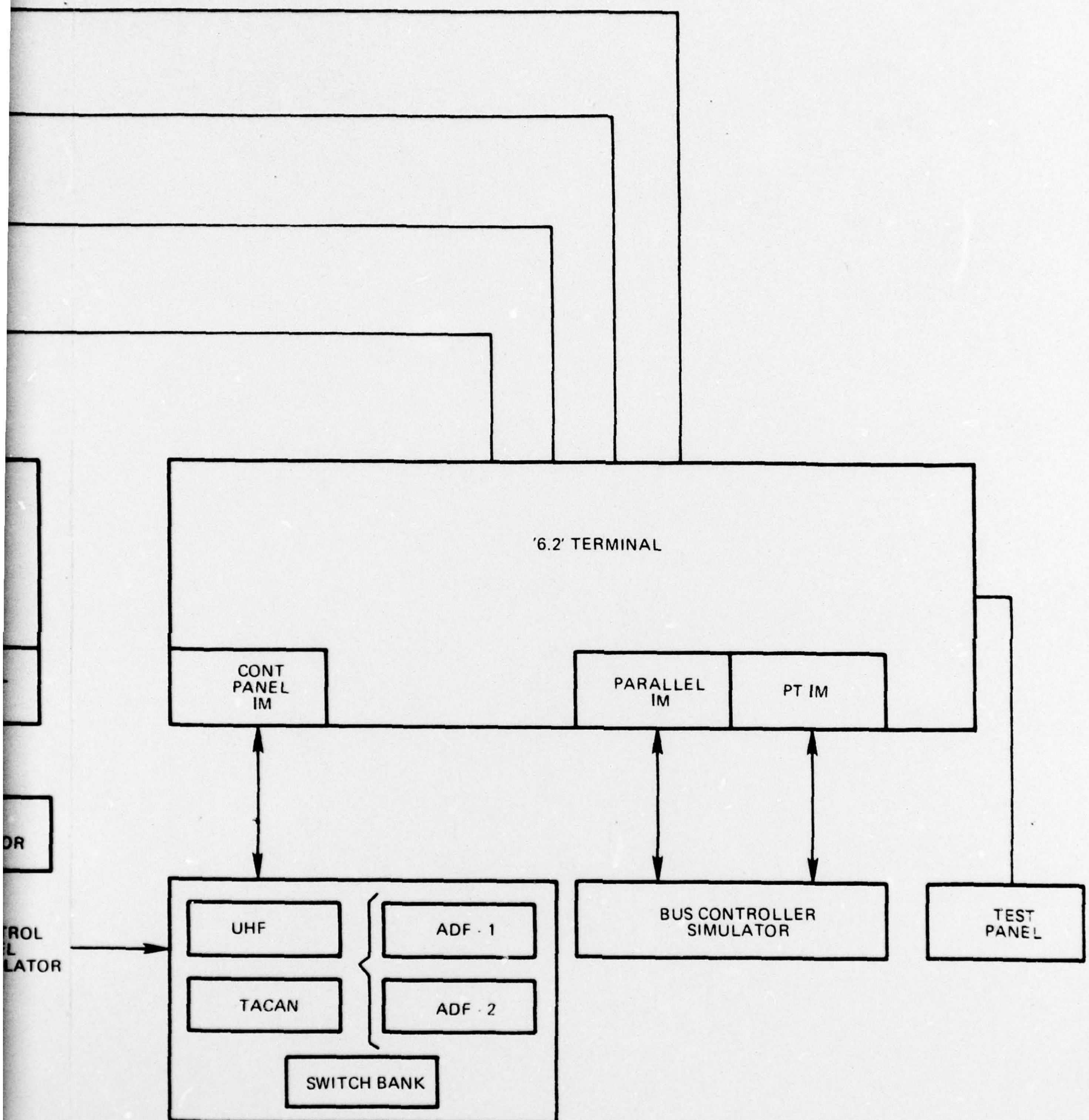


FIG. 20 TELEPHONICS TEST SET-UP



'6.2' TERMINAL
CONT PANEL IM
PARALLEL IM
PT IM
OR
TROL
EL
LATOR
UHF
ADF - 1
TACAN
ADF - 2
SWITCH BANK
BUS CONTROLLER SIMULATOR
TEST PANEL

2

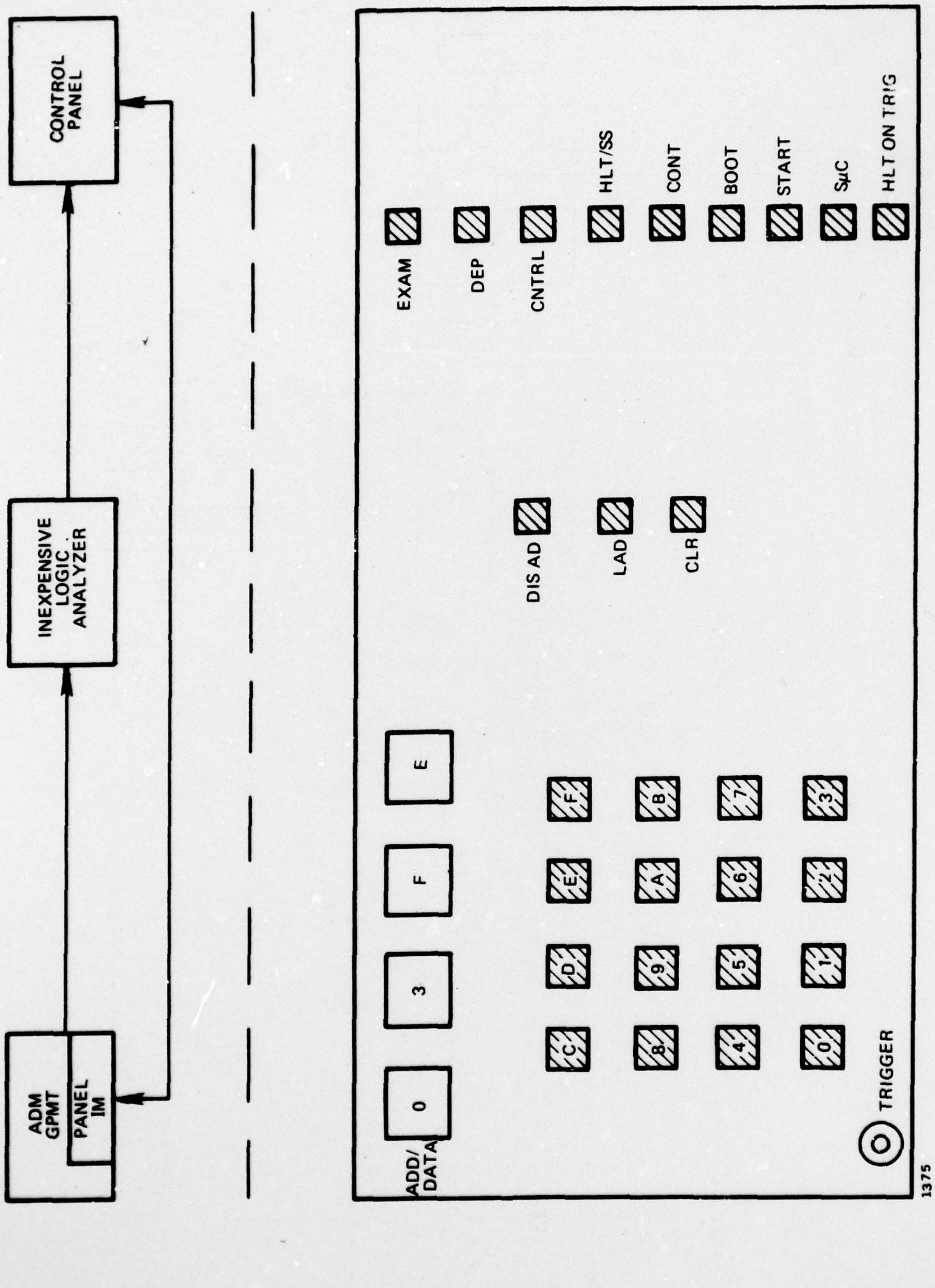


FIG. 21 PROPOSED ADM SUPPORT EQUIPMENT

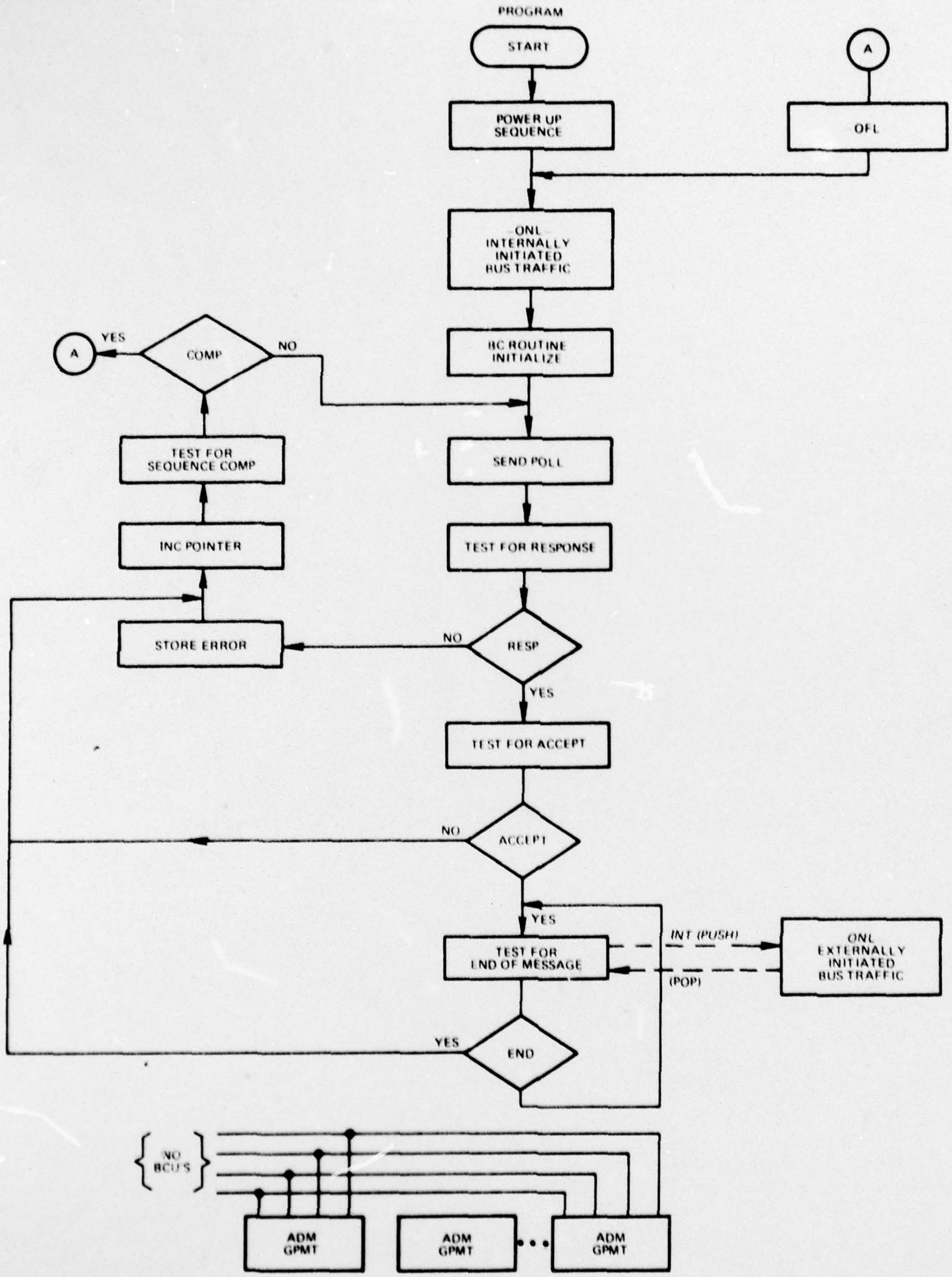


FIG. 22 ADM TERMINAL μP AS A BCU/ONL/OFL