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PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL (1--ETC(U)
FEB 78 P MUSCIANESI, J IRVINE, J RANGHELLI DAAB07-77-C-0146
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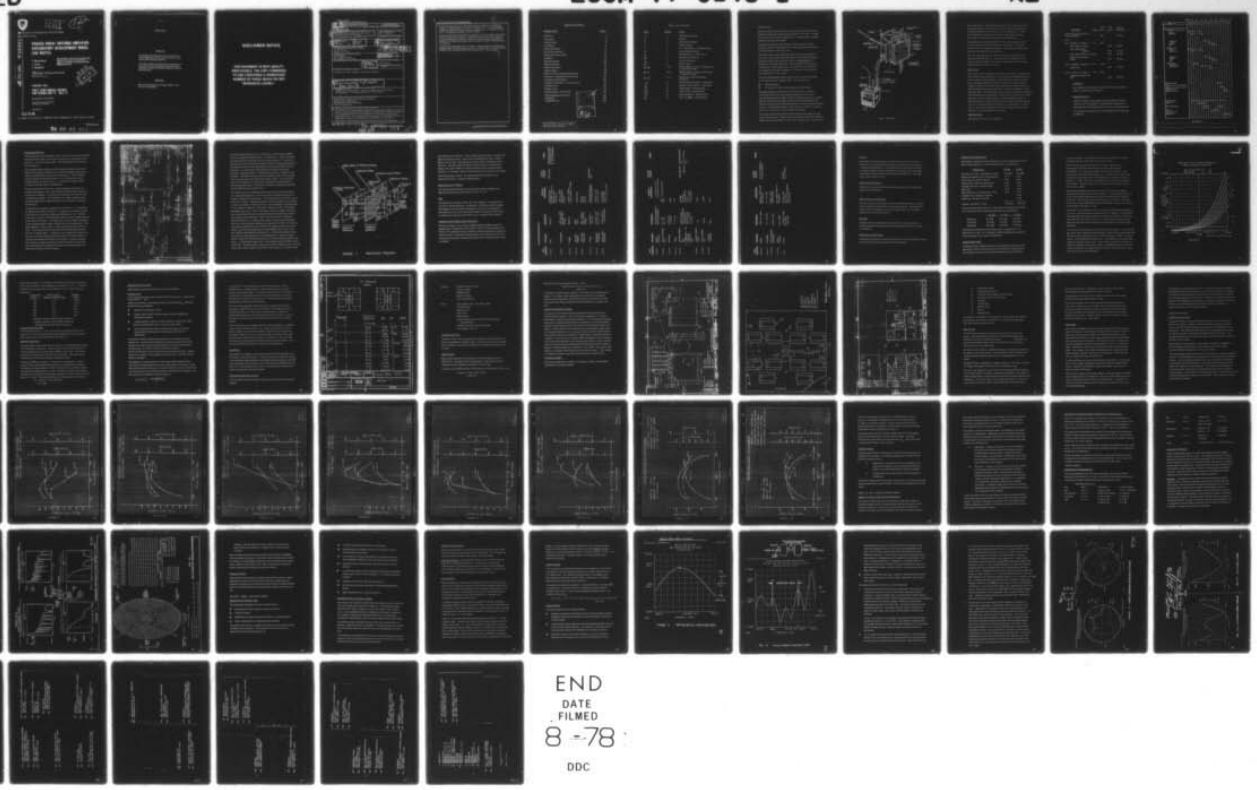

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Research and Development Technical Report

ECOM -77-0146-1

PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL (100 WATTS)

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FEBRUARY 1978

FIRST SEMI-ANNUAL REPORT FOR PERIOD JUN 77 - DEC 77

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CORADCOM was formerly ECOM. Since this report was funded under an ECOM contract, it is being published as an ECOM report.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Phased Array Antenna (non-electronic scanning)
Troposcatter Communication
Microwave Solid State Amplifiers
C-Band Communications

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Phased Array Antenna Amplifier Exploratory Development Program will provide analysis, design and construction techniques to fabricate a scale model for a mechanically steerable phased array antenna amplifier for troposcatter communication system applications. The ultimate goal of this analysis is to determine the technical capabilities, limitations, constraints and cost feasibility for a 1kw system.

Implementation of this program requires analysis in two major technical areas:

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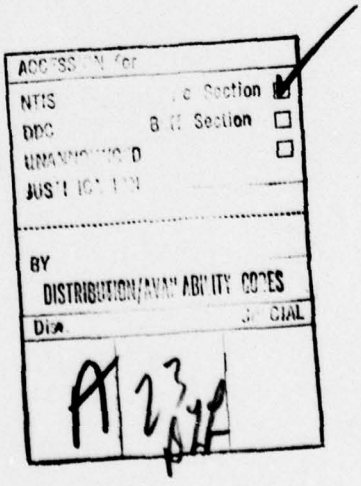
Matstup (Printed) antenna and solid state high power generation and combining. During this reporting period - June 1977 to December 1977 - low loss combining techniques coupled with efficient amplifier design attained 8.9 watts @ 4.7 Ghz with a 1 db bandwidth covering 4.4 Ghz to 5.0 Ghz.

Computer programs were generated and validated to aid in the design of the antenna dipole excitation pattern required to achieve the 30 dbi gain and 15 db sidelobes. These programs also provided the capability to analyze antenna perfor mance degradation vs. amplitude and phase errors introduced as a result of fabrication and RF excitation.

During the next reporting period, a 38 inch by 38 inch antenna array employing an amplitude taper will be fabricated and tested. Assembly and test of the basic power modules will be in progress and the IPA amplifier chain will be complete.

TABLE OF CONTENTS



The statement on the side of page 28 should be deleted per Mrs. O'Brien, Army Electronics Command

LIST OF ILLUSTRATIONS

INTRODUCTION

This semi-annual report describes the Phased Array Antenna Amplifier Program awarded under ECOM Contract #DAAB-07-77-C-0146. Included in this document are system configuration, key tradeoff analysis, and data supporting 100 watt system design.

Technical improvements which offer near term solutions to specific limitations of this 100 watt system will be specified herein and addressed in the Final Report: CLIN 0002, A003.

The Phased Array Antenna Amplifier Exploratory Development Model (100 Watts) contract requires the description of the engineering analysis, design and construction techniques to fabricate a scale model for a mechanically steerable phased array antenna amplifier for troposcatter communication system applications. The ultimate goal of this analysis is to determine the technical capabilities, limitations, constraints and cost feasibility for a 1 kw system.

Successful implementation of this program requires analysis and design in two "state of the art" technical areas. The two areas are:

- Matstrip antenna
- "C" band (4.4-5 GHZ) solid state high power generation

The design approach for this 100 W scale model is shown in Figure 1. The system consists of a control cabinet housing the low level solid state intermediate power amplifier (IPA) and required system power supplies. Remotely located from the control cabinet is the DUPLEX antenna array. This unit houses the twelve high level amplifiers, receive antenna and transmit antenna. The operating frequency for this system is continuous coverage of the 4.4 to 5.0 GHz band. No remote tuning is employed.

The design of the transmit portion of this system provides highly desirable system characteristics. The transmit chain employes 14 identical amplifiers (basic power modules BPM), two in the control cabinet IPA, 12 at the antenna.

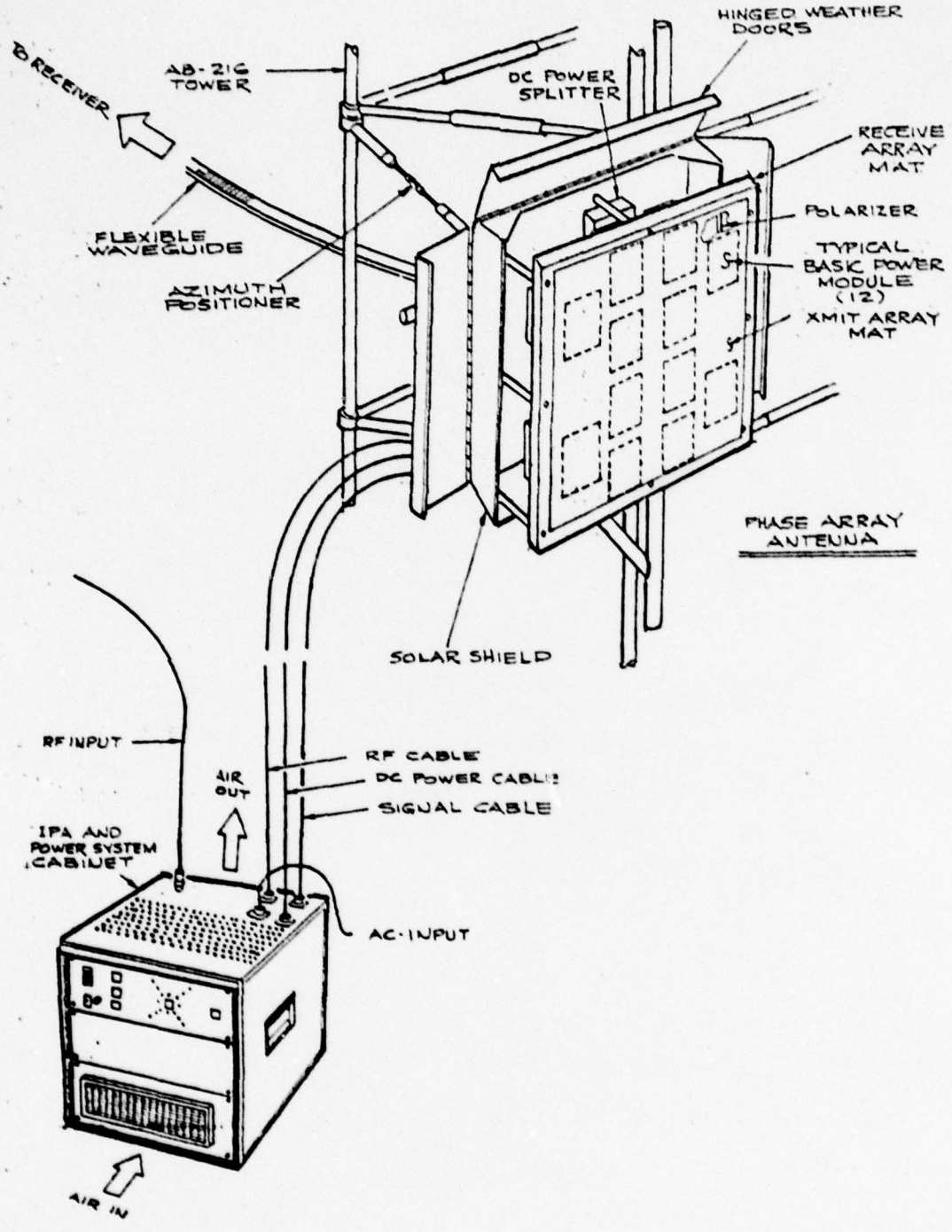


Figure 1. System Pictorial

The 12 feed points on the transmit antenna array (each antenna basic power module illuminating a restricted area) allows for a graceful degradation of transmitter performance versus basic power module failures. Thus several modules may fail prior to a loss of 3 dB in effective radiated power (ERP) or severe transmit antenna pattern degradation.

The modularization (interchangeability) of basic power module provides for lower costs and simpler maintenance considerations. The system operates from low voltage power supplies, thus the hazards of high voltage generation and distribution are eliminated.

The 100 W scale model system will provide full duplex operation with an ARMY AN/GRC-143 radio set. Thus this system will operate from the 100 mw nominal AN/GRC-143 transmitter output and provide a waveguide interface for the AN/GRC-143 receiver.

OBJECTIVES

The objective of this exploratory development scale model is to demonstrate the Cost and technical feasibility of a (Non-electronic scanning) phased array transmit/receive antenna amplifier. This system is to employ solid state devices and highly efficient low voltage power generation to increase the reliability of tactical troposcatter communications by a gradual reduction in ERP as individual amplifier modules fail as opposed to catastrophic communications outage. The primary goal of this program is to generate information and tradeoff analyses culminating in a design concept for a low cost, reliable, high power (1 kw) solid state phased array antenna amplifier system for tactical deployment. The final report for this program will contain a design plan for a 1 kw model along with a detailed cost comparison for 10 and 100 units vs. the cost for comparible quantities of the presently use Klystron Amplifier and 10 feet parobolic dish antenna.

DELIVERABLES

The deliverables and delivery schedule is:

Description	Qty.	CLIN No.	CDRL No.	Delivery Schedule
100W solid state Phased Array Antenna Amplifier	1	0001		450 days
Data				
Data — Exhibit A, Category 5	1 lot	0002		
Tech. Report (monthly)			A001	Monthly
Tech. Report (semi-annually)			A002	240 days
Tech. Report (final) 1 kw system			A003	510 days
Engineering Evaluation Report			A004	360 days
Data — Exhibit B, Category E	1 lot	0003		
Design Plan			B001	190 days
Data — Exhibit C, Category T	1 lot	0004		
Engineering Design Test Plan			C001	360 days

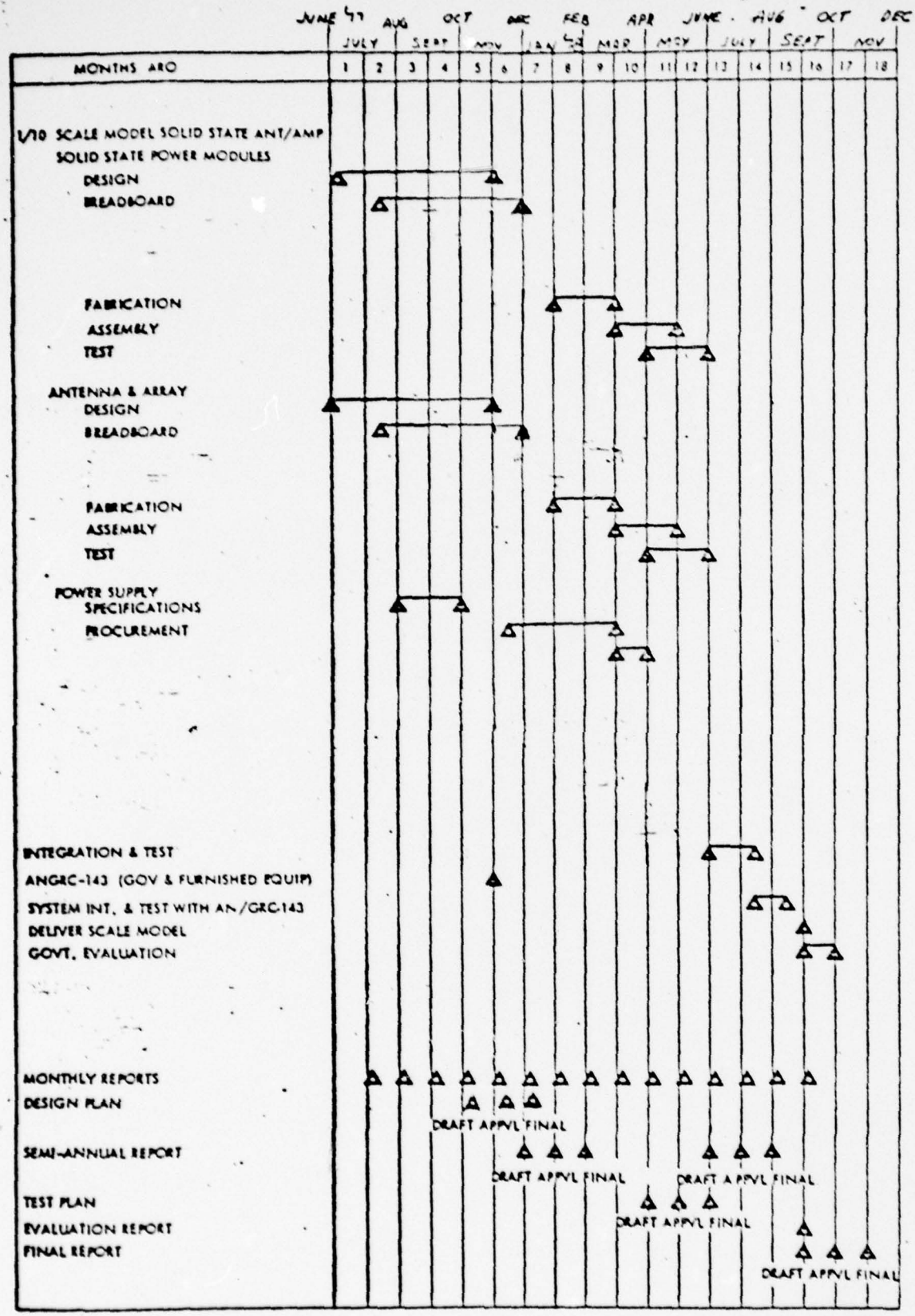
SCHEDULE

The schedule for this program is consistent with the deliverables of Section 1.2 and is shown in Figure 2.

PROGRAM STATUS

Analyses, computer aided design (CAD) and breadboard testing in critical areas are in progress. The information resulting from these tasks has provided the inputs for the 100W system Design Plan.

The following list summarizes work accomplished and investigations in progress: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1/10 SCALE MODEL SOLID STATE ANT/AMP
SOLID STATE POWER MODULES
DESIGN
BREADBOARD
FABRICATION
ASSEMBLY
TEST
ANTENNA & ARRAY
DESIGN
BREADBOARD
FABRICATION
ASSEMBLY
TEST
POWER SUPPLY
SPECIFICATIONS
PROCUREMENT
INTEGRATION & TEST
ANGRC-143 (GOV & FURNISHED EQUIP)
SYSTEM INT. & TEST WITH AN/GRC-143
DELIVER SCALE MODEL
GOVT. EVALUATION
MONTHLY REPORTS
DESIGN PLAN
DRAFT APPVL FINAL
SEMI-ANNUAL REPORT
DRAFT APPVL FINAL
DRAFT APPVL FINAL
TEST PLAN
EVALUATION REPORT
FINAL REPORT
DRAFT APPVL FINAL

FIGURE 2.

A. System

- system block diagram complete
- system budgets established
- thermal analysis complete
- system MTBF complete
- RF/DC interlock requirements identified
- 3 dB ERP degradation analysis complete

B. Amplifier

- combined two driver stages (p/o BPM) ($P_o \geq$ 2.9W @ 22% efficiency)
- combined two final stages (p/o BPM) ($P_o \geq$ 8.9W @ 20% efficiency)
- P.S. requirements defined
- Alumina vs. Epsilam-10 substrate evaluation complete; Alumina selected
- BPM parts selected
- BPM thermal analysis complete
- BPM heat sink selected
- BPM layout complete
- IPA layout complete
- BPM chassis machined

C. Antenna — Transmit, Receive

- computer simulation programs complete, tested
- six antenna amplitude distribution designs analyzed
- final array layout chosen
- balun design complete
- fabrication/assembly tolerance in progress
- single vs. dual laminate tradeoff complete; dual laminate selected
- second harmonic response analysis complete

- antenna layout in progress
- thermal analysis complete
- solar shield design complete
- honeycomb material, radome material surveyed
- wind and ice load analysis complete (100W)
- matstrip material chosen/characterized
- antenna weight analysis complete
- sub-array testing in progress
- one-piece vs. sectionalized construction; one-piece construction chosen

D. Control Cabinet

- P.S. requirements defined
- P.S. vendor survey complete
- BITE circuitry details defined and breadboard complete
- control cabinet layout complete
- control cabinet weight analysis complete
- control cabinet thermal analysis complete
- P.S. cables requirements complete
- BITE circuitry board configuration defined

FINAL REPORT

A requirement of this program is to apply the scale model analysis/data of the Evaluation Report towards a Final Report. This Final Report will determine the design/costing concepts of a 1 kw system with regard to current technological limitations and alternatives.

This report will provide cost correlation analysis comparing a 1 kw solid state phased array system to current field deployed power amplifier/antenna systems.

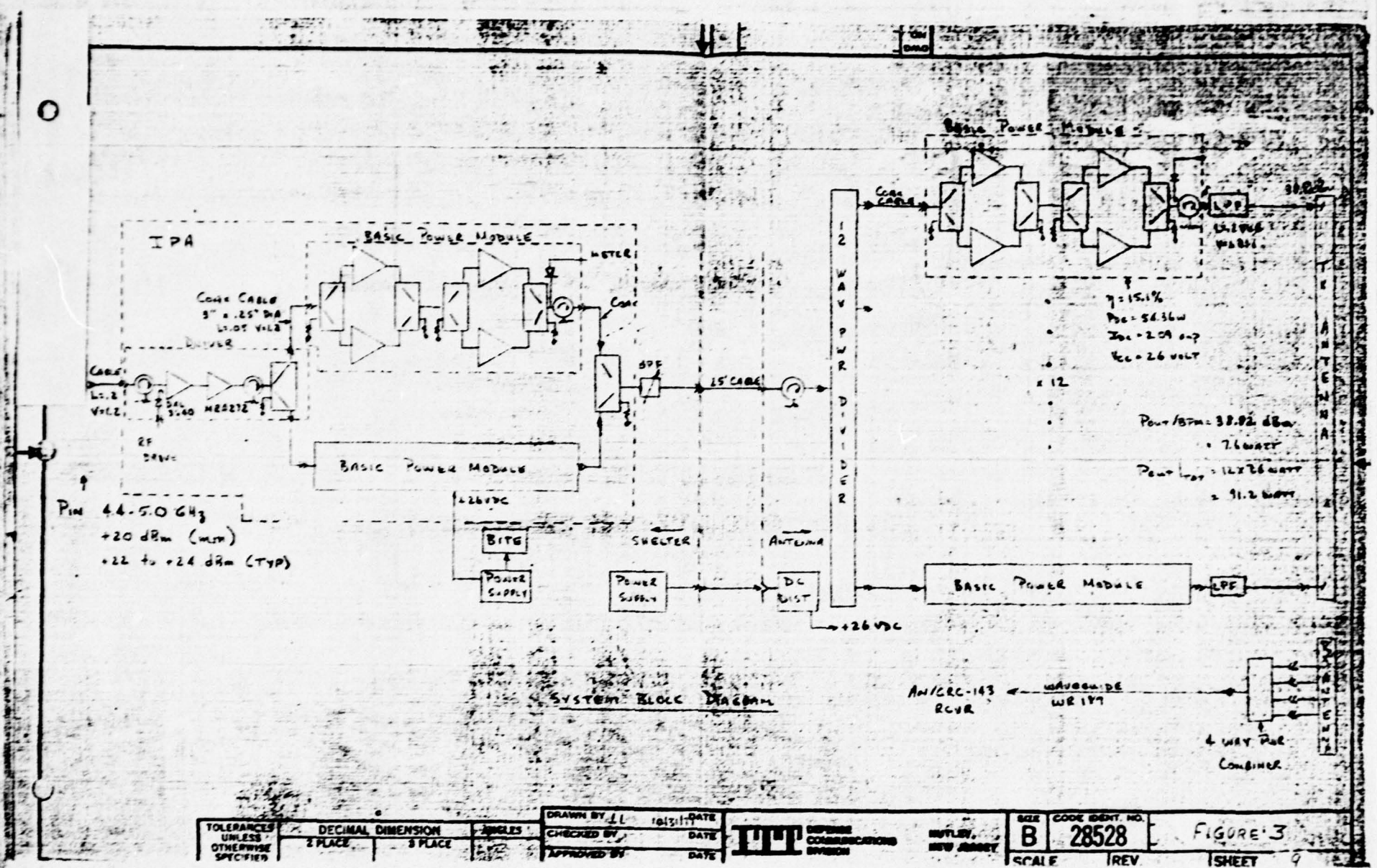
SYSTEM DESCRIPTION

The Phased Array Antenna Amplifier system consists of a transmitter amplifier matrix and antenna array, and a receiver antenna array which operates over the full 4.4 - 5.0 GHz frequency range. The block diagram of the system is shown in Figure 3.

The transmitter matrix consists of an IPA amplifier mounted in the control cabinet which provides the RF drive for 12 parallel amplifiers (basic power modules) mounted directly in back of the antenna array. These 12 BPM's provide a nominal 9 watts each to achieve 100 watt output power which is spatially added by the transmit array. An Antenna Array gain at 30 db provides the +80 dBm effective radiated power

The IPA is further broken down into a driver amplifier which drives two parallel BPM amplifier. Thus, the transmitter amplifier matrix consists of 14 basic power modules (12 mounted on the antenna and two in the IPA) and a single driver amplifier. This repeated use of a single amplifier design was incorporated into the system for both low cost and ease of maintenance considerations.

The RF input to the system is a minimum 100 mw in the 4.4 - 5.0 GHz band provided by the AN/GRC-143 radio set. An isolator is provided on the input to the IPA driver to meet the system input VSWR spec of 1.5:1. The IPA driver output is split by a 3 dB quadrature hybrid into the two signals required to drive the two IPA BPM's. The output power of the two BPM's is detected and the combined detector voltage is used to drive a front panel meter. This meter indication is used to adjust, via the front panel, the gain of the IPA driver. This assures that the proper RF level is obtained from the IPA to drive the 12 antenna BPM's. A tunable four pole bandbass filter follows the IPA and is provided to minimize the noise contribution to the AN/GRC-143 receiver from the IPA and AN/GRC-143 transmitter. Isolators with high power loads are included in the BPM to protect the output transistors from power reflected from the bandpass filter when the transmit frequency and filter are not tuned to the same frequency.



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				CHECKED BY	DATE
				APPROVED BY	DATE

ITT Defense Communications Division, Nutley, New Jersey

SIZE	CODE IDENT. NO.	FIGURE 3
B	28528	
SCALE	REV	SHEET 9

The RF equipment discussed so far is mounted in a control cabinet, together with power supplies and BITE circuitry. A 25-foot coax cable is provided to take the RF output from the BPF up to the antenna amplifiers. An isolator is provided at the input to the antenna amplifier matrix to provide a good terminating impedance for the 25-foot cable and thus assure a good VSWR at the bandpass filter. A 12-way power divider then splits the power into 12 equal amplitude, equal phase signals. Each BPM has a nominal 11 dB gain over the full band. An RF detector in the output of each BPM is used to drive the BITE circuitry and provide an indication of the amplifier status. A low pass filter with a cut-off frequency of 5.15 GHz and a minimum of 50 dB attenuation at frequencies greater than 8.8 GHz follows each BPM to attenuate 2nd harmonics from the BPM final stage transistor pair.

The antenna consists of orthogonal transmit and receive arrays, each with its own ground plane (Figure 4). Each array design is identical in terms of the number of dipoles and amplitude taper. The transmit array has 12 feeds, one for each of the 12 BPM's. The minimum gain of the transmit antenna is 31.05 dB @ 4.4 GHz (31.59 dB @ 4.7 GHz and 32.13 @ 5.0 GHz) resulting in a minimum ERP of +80.65 dBm (81.2 dBm @ 4.7 GHz and 81.7 dBm @ 5.0 GHz). The sidelobe amplitude of the array is -18 dB. The receive array has a slightly lower gain due to the fact that this array is positioned behind the transmit array and has a more complex feed arrangement. Some of the receive power combining is performed in the array, resulting in four outputs, which are then combined by a four way hybrid summer resulting in one output for the AN/GRC-143 receiver. The system is powered from two +26 VDC power supplies located in the control cabinet. The first power supply has a 30 amp capability and is used to power the 12 BPM's located behind the antenna array. A DC power distribution cable carries the 25 amps required up to a DC distribution box. Remote sensing of the DC voltage at the distribution box assures a constant operating voltage for the BPM's. A second power supply with a 7 amp capability powers the BITE circuitry and the IPA. The BITE circuitry monitors the status of important system elements and provides system shutdown in the event of power supply over or under voltage.

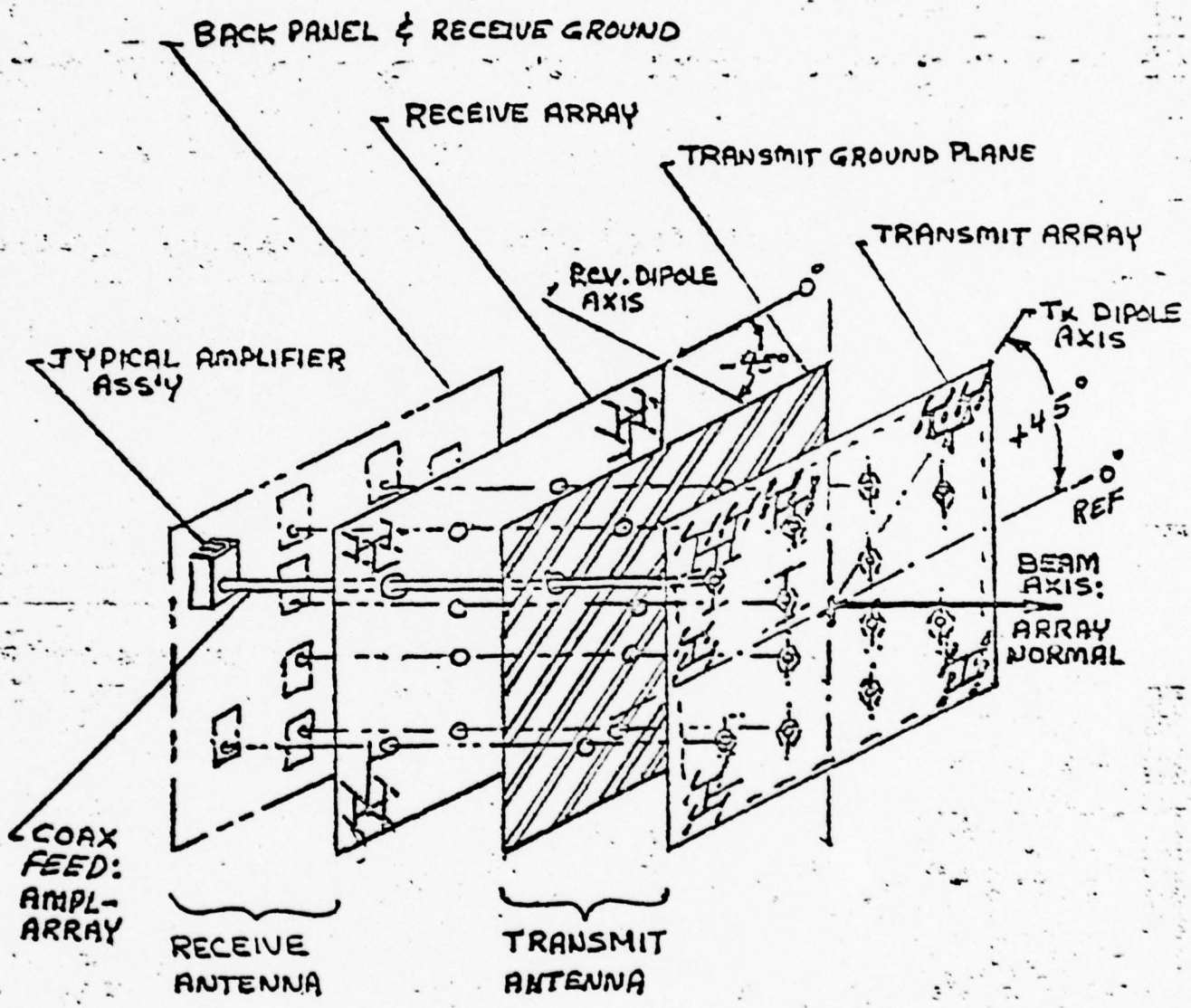


FIGURE 4 ANTENNA CONCEPT

Each BPM has an RF detector. If any transistor fails in a BPM, a red LED will light, indicating the failure. If four of the 12 antenna BPM's fail, a system failure LED will light, indicating that the system ERP has dropped by greater than 3 dB. When the system ON-MAINT switch is placed in the maintenance position, this mode "latches" the status of the BPM to give continuous status indication. In this mode, repair or examination may be performed at the antenna

The following pages compare the required system performance vs. the expected performance, denoting limiting elements.

SYSTEM CHARACTERISTICS

The following paragraphs discuss system characteristics resulting in the expected performance summary table. (Sheets 13-15)

SIZE

The antenna array consists of three, 38" X 38" laminates. This equates to a 10.0 sq. ft. antenna aperature. An additional .5 inch border will be required for mounting to the outer frame resulting in a total area of 10.56 square ft. Projecting to the 1 kw array, this antenna design is consistent with the 100 sq. ft. requirement since only nine of these 10 sq. ft. sections will be required.

TEMPERATURE INDEPENDENT OPERATION

The 100 watt Phased Array Antenna Amplifier shall be designed to meet all specifications at temperatures from -65°F to $+125^{\circ}$F with solar loading of 360 BTU/ft.^{2}/Hr. Equipment built by ITTDCD for military deployment is tested for this environment. Wind and ice loading analysis of the antenna array has been performed and indicates compliant performance under 50 mph wind and 0.5 inch ice loading.

SYSTEM PERFORMANCES

RFQ Paragraph	Parameter	Specification	Expected Performance	Limiting Element	Action
3.4.1.1	Size	10 sq. ft.	Array aperature 38" x 38" = 10 sq. ft. Total 39" x 39" = 10.56 sq. ft.	100W frame	1KW employs 9-38" x 38" aperatures 100 sq. ft. still attained.
3.4.1.2	Temperature	-65^{o}F to $+125^{o}$F Solar 360 BTU/ ft.^{2}/Hr.	-65^{o}F to $+125^{o}$F Solar 360 BTU/ ft.^{2}/Hr.	-	-
3.4.1.3	Weight	Minimum	Antenna - 136 lbs. Control cabinet - 152 lbs.	-	-
3.4.1.4	Structural Interface	AB216 Tower	AB216 Tower	-	-
3.4.1.5	Input/output Connectors	Input - Type N Output WR-187 UG/149	Type N WR-187 UG/149	-	-
3.4.1.6	Cooling	Forced air or convection	Forced air-control cab. convection-elsewhere	IPA thermal rise	
3.4.1.7	Mechanical Positioning	AZ $360^{o} \pm 0.5^{o}$ EL $\pm 5^{o} \pm 0.2^{o}$	AZ $360^{o} \pm 0.5^{o}$ EL $\pm 5^{o} \pm 0.2^{o}$		
3.4.2.1	Antenna gain/ Beamwidth	30 dBi (min)/5^{o} max beamwidth	Tx 31.05 dBi Rx 30.22 dBi 4.4^{o} max. beam width		

RFQ Paragraph	Parameter	Specification	Expected Performance	Limiting Element	Action
3.4.2.2	Duplex Operation	No BER degradation in Rcvr performance	0.2 dB receiver NF degradation essencially		
3.4.2.3	Antenna Polarization	Tx + 45° Rx - 45°	+45° -45° No BER degradation	-	-
3.4.2.4	Sidelobes	15 dB max 18 dB goal	18 dB	-	-
3.4.2.5	VSWR	1.5:1 max	1.5:1	-	-
3.4.2.6	Amplifier Matrix				
	P_{in}	100 MW (nom.)	100 MW	TRW MRA-271	Investigate trade-off
	P_{out}	100 watt (objective)	91.2 watt		
	Transistors quant.	25 transistors	24 transistors	MRA-272	P_o vs. EFF vs. V_{DC}
	Efficiency	20% (15% goal)	11.8%		
	Bandwidth	4.4 - 5.0 GHz	4.4 - 5.0 GHz		
	ERP	+ 80 dBm	+ 80.65 dBm		
3.4.2.7	Amplifier Matrix VSWR	1.5:1	1.25:1	-	-
3.4.2.8	Spurious Radiation	-80 dB	-80 dB	-	-
3.4.2.9	Parasitic Oscillation	None	None	-	-

RFQ Paragraph	Parameter	Specification	Performance	Limiting Element	Action
3.4.2.10	MTBF	4000 Hrs. (min.)	3473 Hrs. (MIL-qualified devices)	Transistor efficiency, thermal resistance	-
3.4.2.11	Bandwidth	4.4 - 5.0 GHz	4.4 - 5.0 GHz	-	-
3.4.2.12	System Degradation Alarm	@ ERP - 3 dB	@ ERP - 3 dB 4 BPM failures	-	-
3.4.1.13	Failure Indicator	Ind. module	Ind. Module LED's on front panel	-	-
3.4.3	Power	120/230 V ± 10% 50 - 60 Hz 1KW (max)	115/230 ± 10% 50 - 60 Hz 1050 VA (excluding fan) 1208 VA total	See spec 3.4.1.6 above	

WEIGHT

The weight of the antenna structure is estimated to be 136 lbs. Component weights have been reduced wherever possible consistent with other electrical or mechanical requirements. Thermal analysis was performed on the BPM to compute transistor junction temperatures as a function of heat sink weight (and thermal resistance) before selecting the present heat sink. The weight of the control cabinet is 152 lbs.

STRUCTURAL INTERFACE

The phased array antenna will include the necessary hardware to mount the antenna on an AB-216 tower.

INPUT/OUTPUT CONNECTORS

The input connector to the phased array antenna amplifier system is a coaxial Type N connector mounted on the top of the control cabinet. The output of the system is WR-187 waveguide with a UG/149 flange which can be connected directly to the AN/GRC-143 receiver.

COOLING

Cooling of the mast mounted antenna array will be by means of convection. Thermal analysis for the control cabinet indicates that a fan will be required to cool the IPA.

MECHANICAL POSITIONING

A mechanical positioner will be part of the phased array antenna amplifier system and will fully satisfy the requirements of the specification.

ANTENNA GAIN/BEAMWIDTH

The minimum transmit and receive antenna gains are calculated to be 31.05 dB and 30.22 dB respectively. The contributing factors are listed below.

Antenna Gain	Tx: dB	Rx: dB
Directivity (4.4 GHz): including taper (CAD)	+33.5 dBi	+33.5 dBi
Phased and amplitude error loss (estimated)	-0.77	-0.54
Polarization loss (30 dB isolation)	-0.01	-0.01
Aperture filler dielectric material loss	-0.22	-0.36
Corporate feed loss: matstrip (meas.)	-0.77	-1.09
Balun loss	-0.50	-0.50
Input VSWR loss (1.5:1 VSWR spec. limit)	-0.18	-0.18
Combiner loss: external to matstrip		-0.40
Cable loss: external to matstrip		-0.20
Net gain = directivity - losses	+31.05 dBi	+30.22 dBi

These net antenna gains pertain to 4.4 GHz where the directivity is 33.5 dBi. At 4.7 GHz and 5.0 GHz the antenna performance is as listed below:

	4.4 GHz	4.7 GHz	5.0 GHz
Directivity	33.5 dBi	34.04 dBi	34.58 dBi
Tx net gain	31.05 dBi	31.59 dBi	32.13 dBi
Rx net gain	30.22 dBi	30.76 dBi	31.30 dBi

The half power beamwidth for the antenna array is computed to be 4.4° maximum at 4.7 GHz. At 4.4 GHz and 5.0 GHz the beamwidth is computed to be a maximum of 4.5° and 4.2° respectively.

DUPLEX OPERATION

To assure that use of the phased array antenna amplifier results in no BER degradation of the AN/GRC-143 receiver, the noise power contributions of the transmitter must be calculated for frequencies as close as 100 MHz to

the receive frequency. The mechanism of this noise contribution is through coupling between the transmit and receive antenna arrays.

There are three sources of noise power contributions which must be investigated; the AN/GRC-143 transmitter, the IPA, and the antenna matrix BPM's. To reduce the contribution of the first two sources, a four-pole bandpass filter with 40 dB rejection at $f_o \pm 100$ MHz has been incorporated into the system following the IPA. This reduces the noise power of these two sources by 40 dB. Thus, the major contributor of noise power is the antenna matrix BPM's. The only reduction in this noise power is from the transmit to receive array isolation.

Noise figure degradation versus antenna isolation as a function of bandpass filter rejection and BPM gain is shown in Figure 5. For the antenna isolation of 35 dB, the noise figure degradation is less than 0.2 dB for BPM noise figures up to 15 dB. The calculated receiver antenna gain is 30.2 dB min. Therefore, to assure no receiver BER degradation with 30 dB antenna isolation, the maximum allowable BPM noise figure is 12 dB.

Noise power out of the BPM at 4.6 Ghz was measured while driving the amplifier at 4.7 Ghz. The noise power was measured to be -137 dBm/Hz. Assuming 30 dB isolation between the Transmit and Receive antenna, this results in a noise power of-167 dBm/Hz at the receiver input. For a 5.5 dB noise figure receiver, this additional noise power would correspond to approximately a 3.8 dB noise figure degradation.

Noise power data had been previously taken on individual stages. It was found that <u>one</u> device of four (MRA272) had approximately 10 dB more noise power output than the other devices, particularly under low drive conditions (-0.5 dB). Upon examination, it was found that this transistor was in the BPM and was situated on the higher loss leg of the Lange coupler. Therefore, this transistor was a large contribution to the BPM total noise power output. Depending upon how the next lot of transistors perform, the remaining BPM's could have lower noise power outputs and result in less receiver degradation.

RECEIVER NOISE FIGURE DEGRADATION
VERSUS ANTENNA ISOLATION

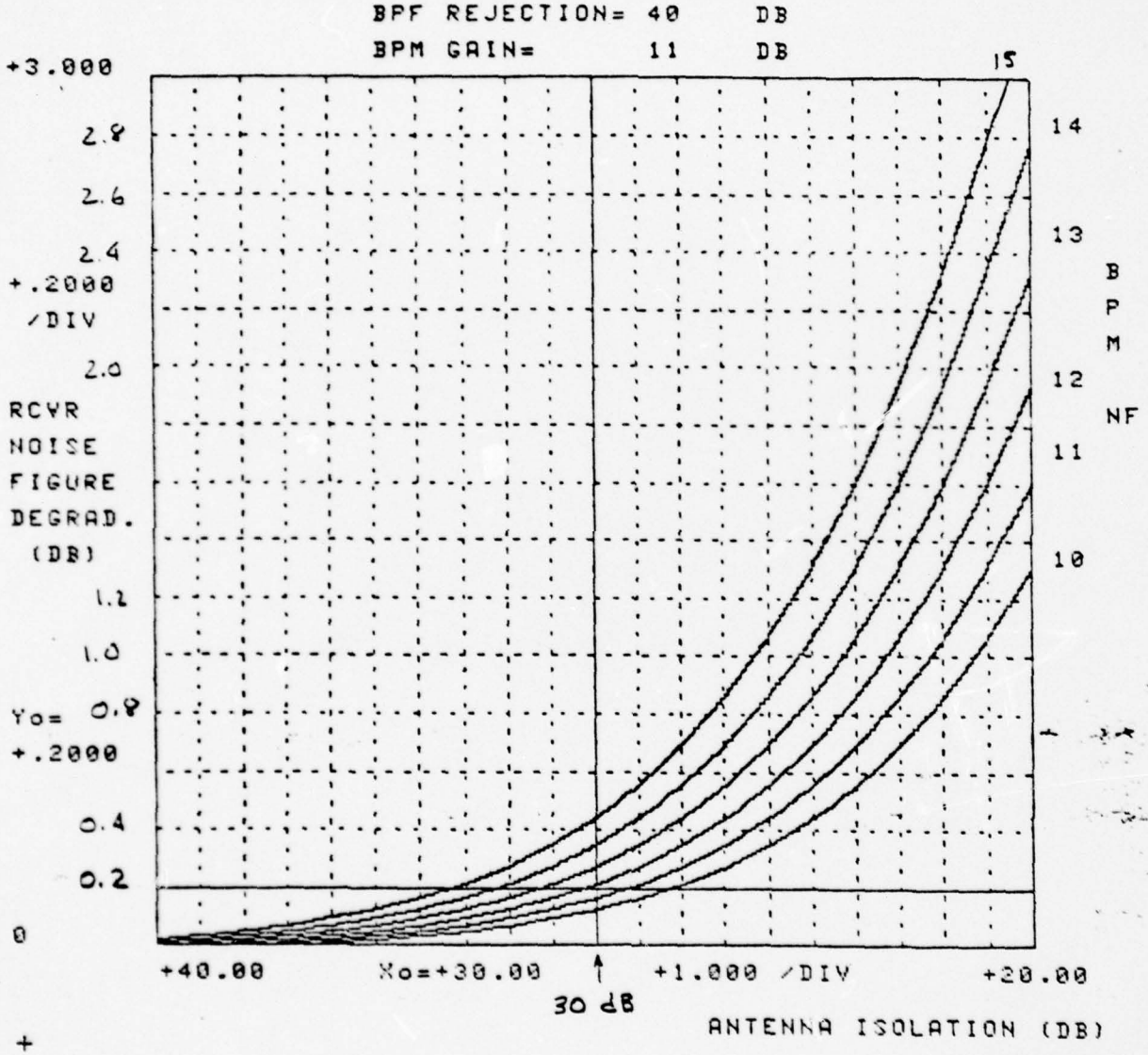


FIGURE 5

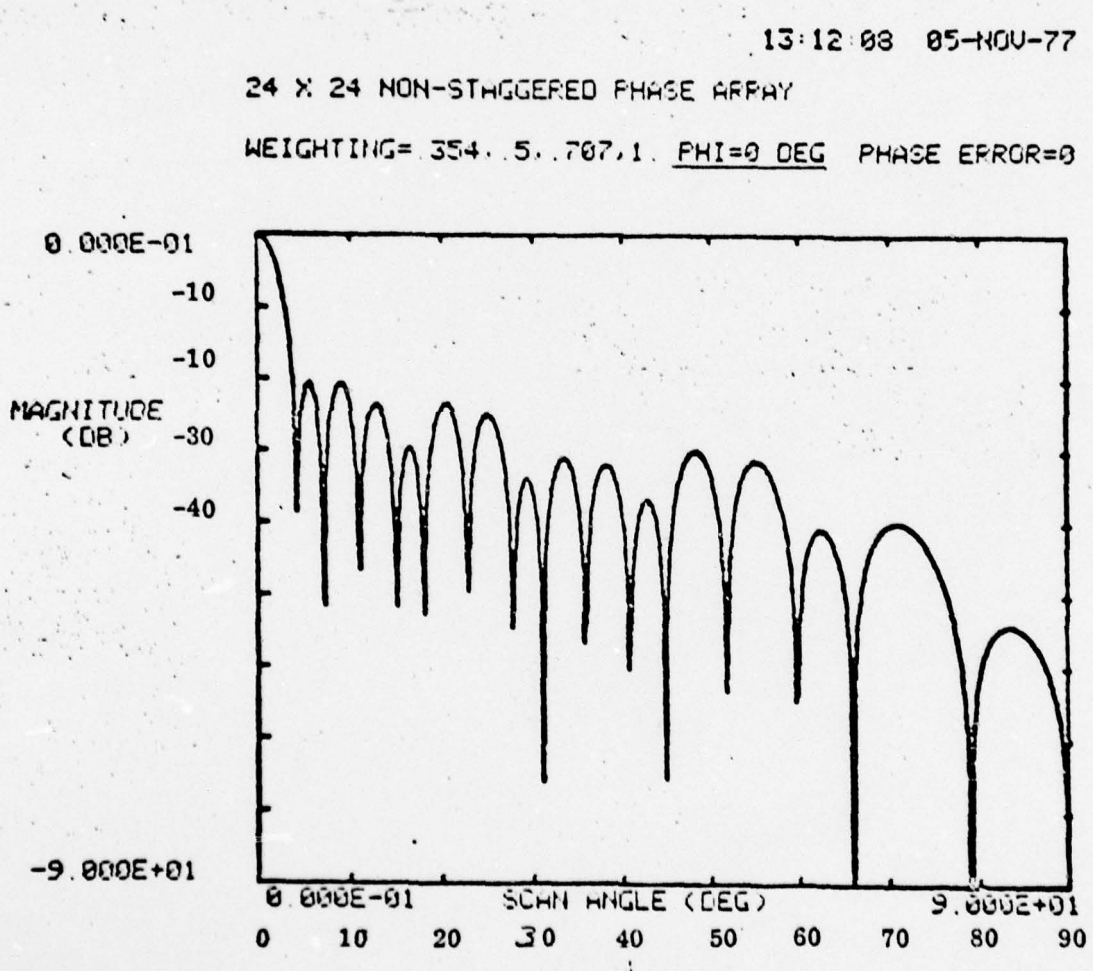

13:12:08 05-NOV-77
24 X 24 NON-STAGGERED PHASE ARRAY
WEIGHTING= .354, .5, .707, 1. PHI=0 DEG PHASE ERROR=0
0.000E-01
-10
-10
MAGNITUDE (DB)
-30
-40
-9.000E+01
0.000E-01
SCAN ANGLE (DEG)
9.000E+01
0 10 20 30 40 50 60 70 80 90

Fig 6

ANTENNA POLARIZATION

The transmit signal polarization will be 90 ± 1° from the receive signal polarization with the transmit signal polarization at +45° and the receive signal polarization at -45°.

SIDELOBES

The computed sidelobe amplitude for the antenna array is less than -20dB for all azimuth angles. Figure 6 shows the computed pattern at phi = 0° for the case of 12 equal phase excitations.

ANTENNA VSWR

The calculated antenna VSWR is 1.45:1. The contributions are listed as:

Balun	1.10:1
Power divider (1.05:1), cascaded (RMS)	1.10:1
Dipole - divider (2 x 2 array with divider)	1.20:1
Total worst case	1.45:1

AMPLIFIER MATRIX

The amplifier matrix total power output is 91.2 watts (49.6 dBm) which is 0.4 dB down from the 100 watt objective. This number is based upon 12 basic power modules each delivering 7.6 watt to the transmitter array inputs. It should be noted that the effects of the antenna VSWR of 1.5:1 have been included in the antenna gain calculations.

The DC-RF efficiency for the amplifier matrix is 11.8% assuming 22% collector efficiency for the bipolar transistors. Any further improvements in system efficiency will have to come from improved transistor performance. To obtain the system efficiency goal of 15% in the present system configuration, the transistor collector efficiency required is 28%. To obtain system efficiency of 20%, the required transistor collectors' efficiency is 38%.

Improvements in transistor gain also improve system efficiency since it reduces output power of the driver stages. Furthermore, if the total gain of a MRA 272, MRA 271 chain was increased 3 dB, only one BPM would be required in the IPA. This change would increase the system efficiency to 13.6% even with the 22% collector efficiency. Improvements in both transistor gain and efficiency together

begin to look promising. For example, with the higher gain transistors operating at 25% collector efficiency, the resulting system efficiency is 15.5%. A collector efficiency of 32% would provide a system efficiency of 20%. These results are summarized:

COLLECTOR EFF	TOTAL GAIN OF MRA 271 & MRA 272 (dB)	SYSTEM EFF
22%	12.1	11.8% *
22%	15.1	13.6%
28%	12.1	15%
38%	12.1	20%
25%	15.1	15.5%
32%	15.1	20%

12 dB gain assumed current system configuration

15 dB gain assumes single IPA BPM configuration

* Present projected 100W Model performance

AMPLIFIER MATRIX VSWR

The input VSWR spec of 1.5:1 max. will be met by providing an isolator at the input to IPA. This assures that if the IPA input impedance varies as a function of the RF gain control, the input VSWR will be less than 1.5:1.

SPURIOUS RADIATION

The major spurious signal which must be addressed is the 2nd harmonic generated in the TRW MRA 271 transistor. The level of this spurious from a combined pair of these transistors has been measured at ITTDCD to be -28 dBc. This would correspond to the spruious level at the output of the BPM. This signal must be attenuated by at least 52 dB to meet the -80 dBc specification.

Following the BPM is an isolator, a low pass filter and the antenna. Both the isolator and low pass filter have been measured at the 2nd harmonic frequency. The isolator provides as little as 2.5 dB of loss while the low pass filter provides a minimum of 50 dB attenuation at 8.8 GHz. In addition, the gain of the transmit antenna has been computed at 2nd harmonic frequencies and can be within 3 dB of the gain at 4.4 - 5 GHz. The resultant 2nd harmonic transmitted level is therefore:

$$P2 = -28 \text{ dBc} - 2.5 \text{ dB} - 50 \text{ dB} - 3 \text{ dB}$$

$$= -83.5 \text{ dBc}$$

PARASITIC OSCILLATIONS

There will be no parasitic oscillations in any of the amplifiers.

SYSTEM MTBF

A 100 W scale model system has a computed MTBF of 3473 hours, assuming MIL qualified devices. This

number is based upon current bipolar transistor performance (Θ_{jc}, efficiency) and the following assumptions:

- Bipolar device efficiency of 22%.
- Bipolar device thermal resistance based upon best available data which will be updated.
- A single transistor failure in a BPM constitutes a failure of that BPM (versus a partial failure mode - loss of one output stage.)
- Worst case analysis of system 3 dB ERP degradation versus BPM failure (without consideration of BPM position within the array (statistical)).

The analysis indicates that the limiting element is the transistors junction temperature. These thermal calculations are based upon presently available thermal information/measured bipolar efficiency data and will be updated as new information of transistor thermal resistance is received.
The DC-RF efficiency used in the calculations is 22% and historically, improvements can be expected. If the efficiency increases to 26%, 4,000 hour system MTBF is obtainable.

The definition of a system failure is a 3 dB drop in antenna amplifier ERP.
The number of antenna matrix basic power module failures that result in a 3 dB drop in ERP has been determined. To do this, both the loss of power and the loss of antenna gain due to loss of dipoles and beam squinting must be computed. The first component is straightforward and is given by:

$$P = 10 \log \left[1 - \frac{\text{no. of failures}}{12} \right]$$

To compute the loss of antenna gain, a computer program was written to calculate the dipole element pattern by direct integration of the sinusoidal current along the dipole length. A vectorial summation of all array elements is performed at any fair field point providing a non-approximate analysis for any shape array, and grid or error pattern. The bore sight gain is computed including loss of gain due to beam squinting.

The loss of antenna gain due to BPM failures was analyzed and the results are shown in Figure 7 for up to four total failures. The gains listed are the computed directivity at 4.7 GHz and do not include losses. Included is a drawing of the antenna array with the distribution of the 12 BPM's. The total loss in ERP is also shown and is a maximum of 3.06 dB for any three BPM failures.

It was found that the loss of antenna gain due to beam squinting was a negligible component of the total loss of gain. As a result, the loss in gain due to the failure of BPM's 5, 9, and 10 for example, is equal to the loss of gain due to the failure of BPM's 6, 9, and 12. Because of this, the antenna array can be broken down into four inner (A) and eight outer (B) BPM's. The loss in ERP has been listed versus the number of failures of these A and B modules. Thus the system MTBF calculations are based upon four BPM failures.

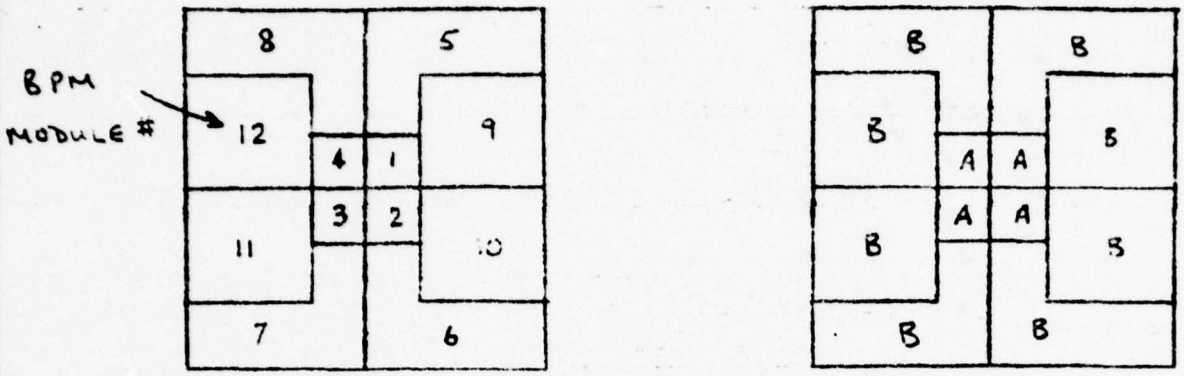
BANDWIDTH

All the BPM's are designed to exploit the ultimate bandwidth capabilities of the TRW MRA 271 and 272 transistors. Because the devices are internally matched to 50 Ω input and output impedance, only minimal external matching is required. Tests on samples of the TRW devices have shown that they instantaneously cover the 4.4 to 5.0 GHz frequency band. Thus, no retuning will be required for the system to operate over the entire passband.

SYSTEM DEGRADATION ALARMS

The front panel of the control cabinet includes the following controls and status displays.

Tx Antenna Array



Failures	A	B	Directivity @ 4.7 GHz	ΔG	ΔP	ΔERP
	0	0	34.04 dB	—	—	—
1 Failure	1	0	33.96	.08 dB	.38 dB	.46 dB
	0	1	33.51	.53 dB	↓	.91 dB
2 Failures	2	0	33.89	.15 dB	.79 dB	.94 dB
	1	1	33.41	.63 dB	↓	1.42 dB
	0	2	32.91	1.13 dB	↓	1.92 dB
3 Failures	3	0	33.83	.21 dB	1.25 dB	1.46 dB
	2	1	33.33	.71 dB	↓	1.96 dB
	1	2	32.79	1.25 dB	↓	2.50 dB
	0	3	32.23	1.81 dB	↓	3.06 dB
4 Failures	4	0	33.79	.25 dB	1.76 dB	2.01 dB
	3	1	33.26	.78 dB	↓	2.54 dB
	2	2	32.68	1.36 dB	↓	3.12 dB
	1	3	32.09	1.96 dB	↓	3.72 dB
	0	4	31.42	2.62 dB	↓	4.38 dB

DRAWING NUMBER

NUTLEY, NEW J

DEFENSE COMMUNICATIONS DIVISION

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	PHASED ARRAY – ΔERP
USED ON		CODE IDENT. NO. 28528	DWG. SIZE A	FIGURE 7
PREPARED BY DATE				
CHECKED BY DATE				SHEET 25

D6216 A REV. 5/73

Controls:	System ON-MAINT switch
	RF drive control
	Bandpass filter
	Lamp test switch
	Circuit breaker/reset
Status:	Power supply 1 and 2 over/under voltage
	IPA BPM output
	Input RF drive
	BITE clock
	System failure
	Meter reading of total RF output or total IPA output switch selectable
	Normally off LED for each antenna BPM
	Power supply 1 and 2 on

FAILURE INDICATOR

The failure of any of the 12 antenna BPM's will cause a red LED on the front panel corresponding to that BPM to light. The BITE circuitry will be adjusted such that failure of any of the four transistors in the BPM will cause the LED to turn on.

PRIME POWER

Supply voltage required for the phased array antenna amplifier system is 115/230 volt ± 10% (RMS), 50-60 Hz single phase. Total DC input power is estimated from the subsystem contributions to be 798 watts.

Assuming a power supply efficiency of 80% and a power factor (lag) of 95% (1.053):

$$\text{AC power} = 1.25 \times 1.053 \times 798 \text{ VA}$$
$$= 1050.4 \text{ VA}$$

The blower in the control cabinet requires 158 VA.

$$\text{Total AC power} = 1050.4 + (115\text{V} \times 1.25 \times 1.1\text{A})$$
$$= 1208.4 \text{ VA}$$

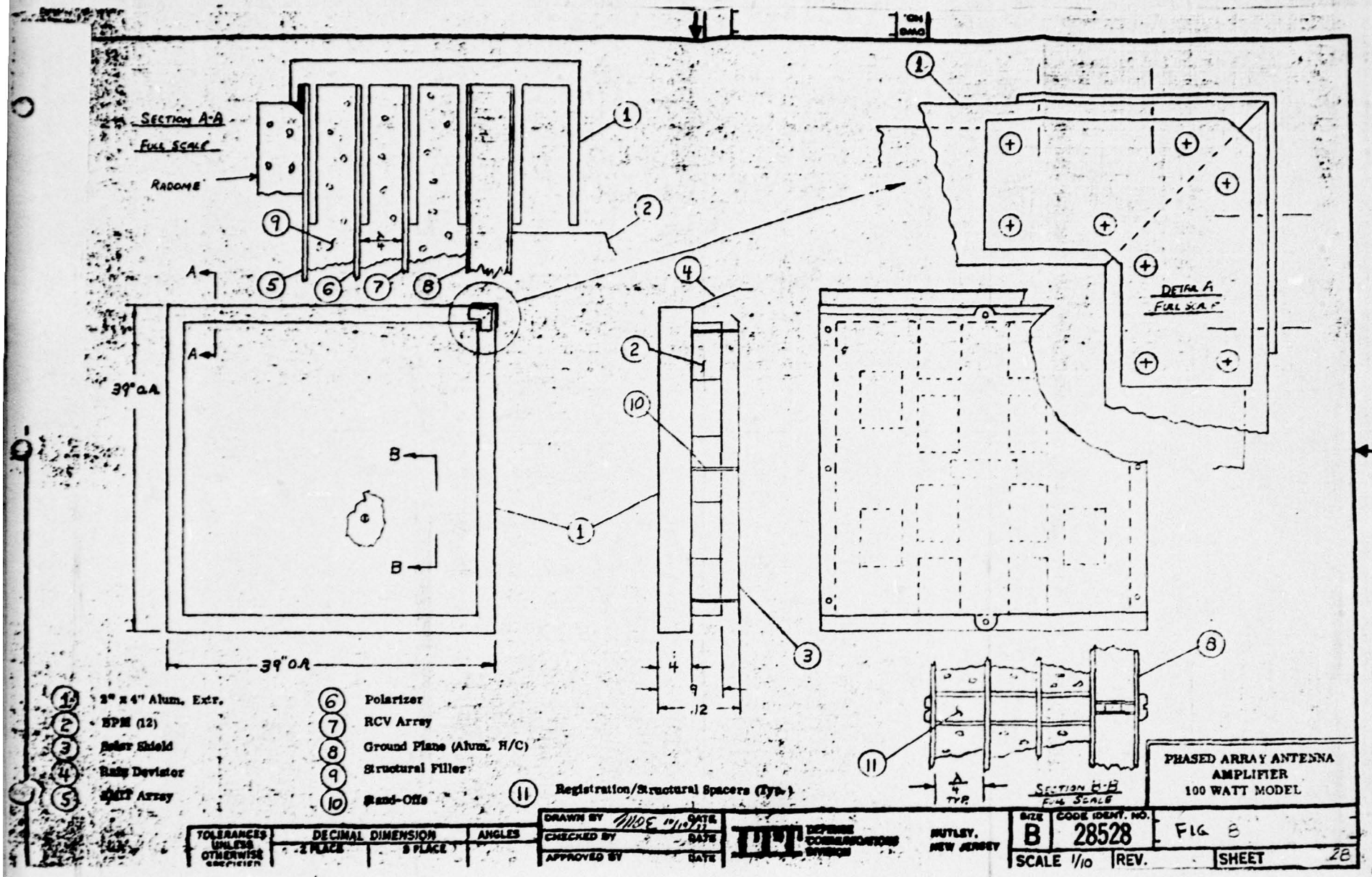
As efficiency of bipolar devices improves, the prime power requirements are reduced. For example, when device efficiency increases to 28% within the present system configuration, DC-RF system efficiency increases to 15% and total system prime power (including IPA blower) decreases to less than 1,000 watts.

ANTENNA MECHANICAL DESIGN

The antenna consists of three Teflon impregnated fiberglass printed circuit boards (transmit, polarizer, receive) structurally supported by a 0.50 inch thick aluminum honeycomb ground plane (Figure 8). Critical dimensional spacing and structural integrity between boards are maintained by accurately machined dielectric material spacers and low loss foam or honeycomb filler bonded to the boards. The deliverable 100 watt model could be disassembled for experimental work whereas final field units (1 kw system) would be bonded for added strength. This composite laminate is enclosed by a support frame to which the positioner is integrated. Twelve basic power modules (BPM) including heat sinks are mounted to the rigid rear ground plane as are transmit power splitters, receive combiner and coax/waveguid transition, BITE board and DC distribution block as shown in Figure 9. Behind the basic power modules is a solar shield. The pur pose of this element is to minimize BPM thermal rise due to solar radiation. A rain deviator is provided to minimize water entry onto the basic power module matrix.

CONTROL CABINET

The control cabinet shown in Figure 10 is housed in a shelter. The following components are mounted internally:



1. 2" x 4" Alum. Extr.
2. EPM (12)
3. Solar Shield
4. Rudy Deviator
5. RCV Array
6. Polarizer
7. RCV Array
8. Ground Plane (Alum. H/C)
9. Structural Filler
10. Stand-Offs
11. Registration/Structural Spacers (Typ.)

PHASED ARRAY ANTENNA AMPLIFIER
100 WATT MODEL

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	DRAWN BY MDE 10/10/77 DATE	CHECKED BY DATE	APPROVED BY DATE	ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	FIG 8
									SCALE 1/10	REV.	SHEET 28

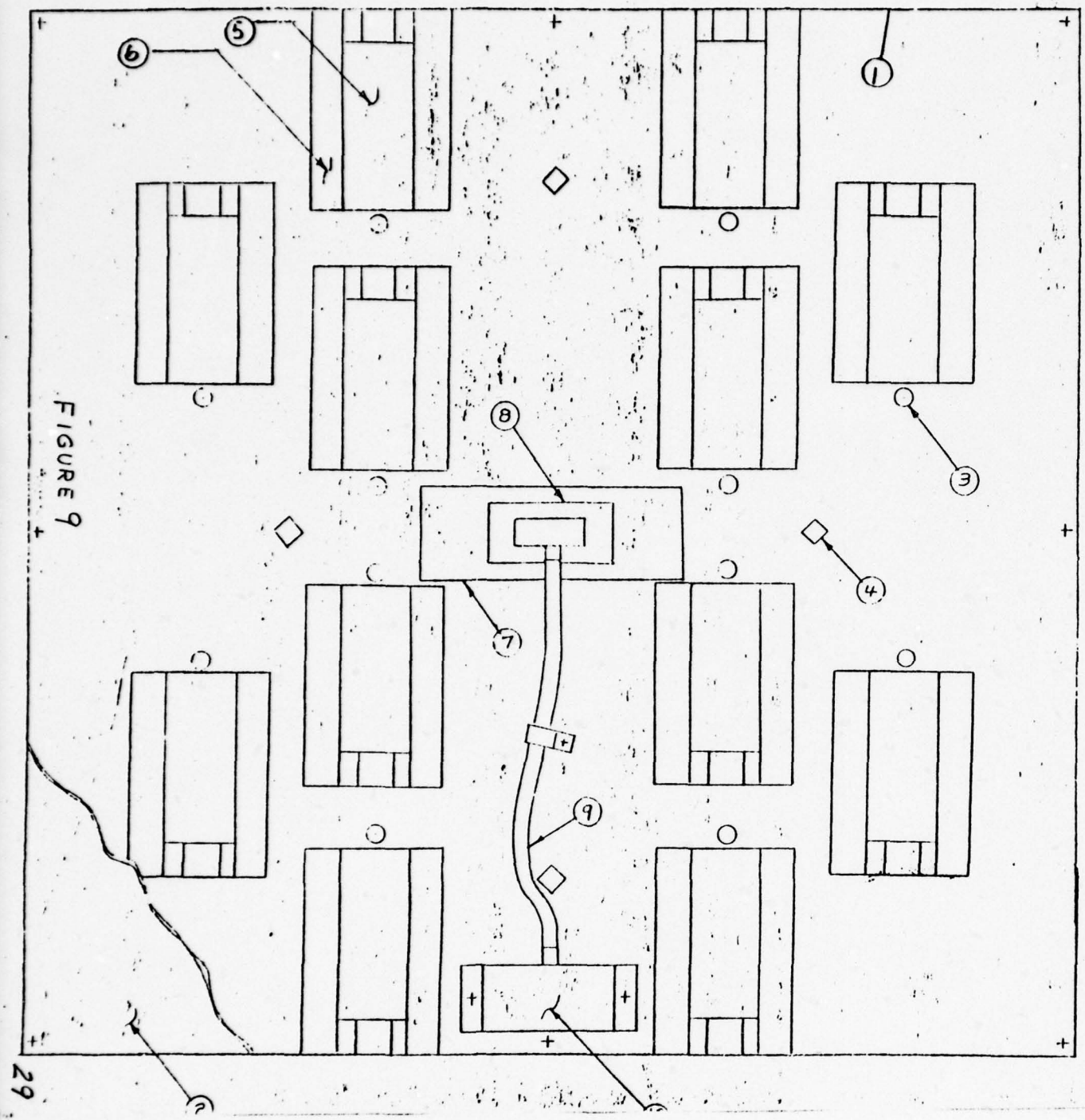


FIGURE 9

(10) WG/Coax Adaptor
(9) RF Coax Cable
(8) Combiner
(7) Power Splitter
(6) Heat Sink (12)
(5) BPM (12)
(4) Receiver Output (4)
(3) Amplifier Input (12)
(2) Solar Shield
(1) Alum. Honeycomb .50" thk.

REAR GROUND PLANE ASSEMBLY

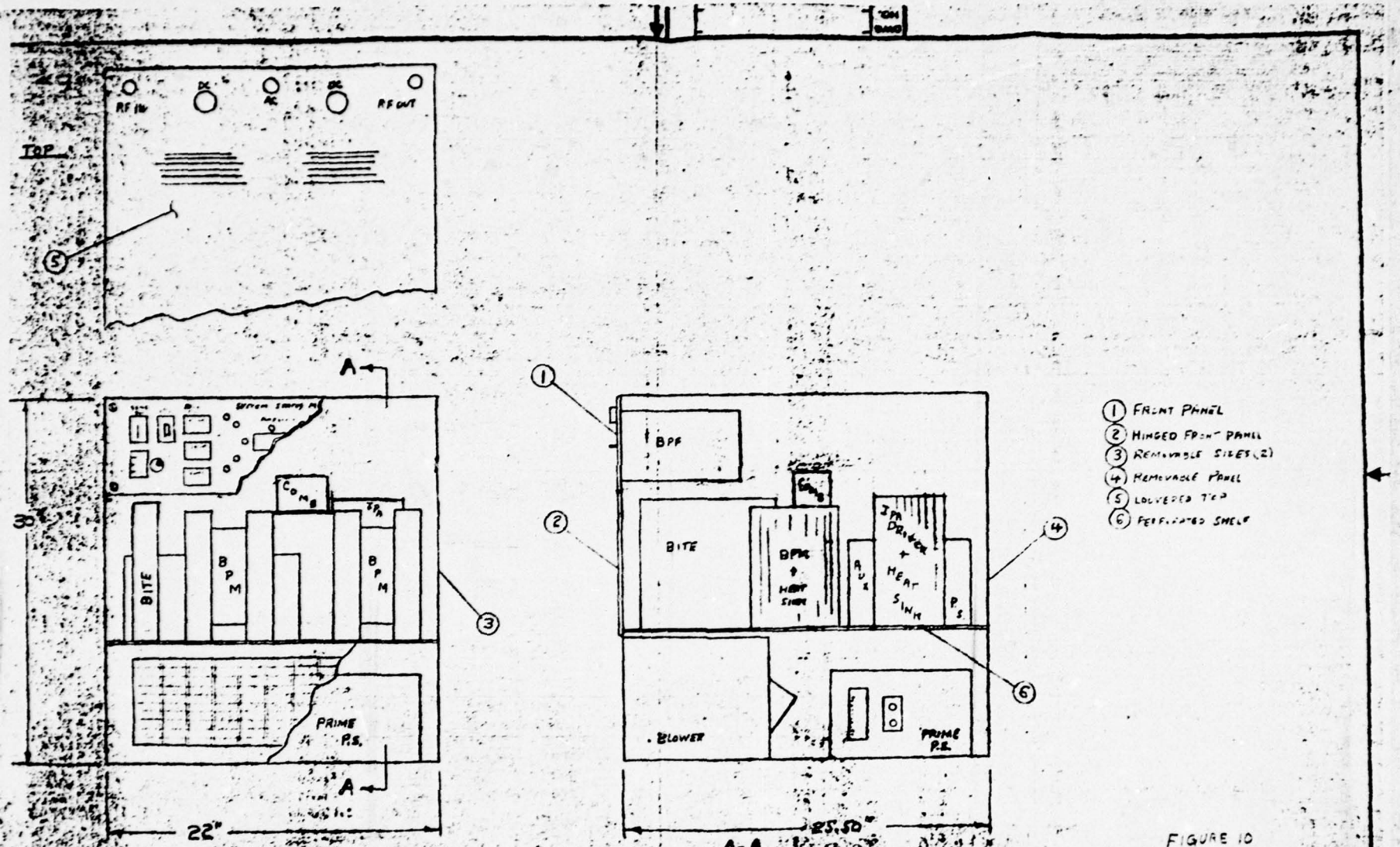


FIGURE 10

TOLERANCES UNLESS	DECIMAL DIMENSION	ANGLES	DRAWN BY	DATE	DEFENSE COMMUNICATIONS DIVISION	BUTLER, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	CONTROL CABINET
			CHECKED BY	DATE					

DRAWING 10 80

- Prime power supply
- Auxilliary power supply
- Two basic power modules (with heat sinks)
- IPA driver module (with heat sink)
- Combiner
- Control panel
- BITE circuitry
- Blower
- Bandpass filter

Accessibility to components is accomplished by means of removable panels on both sides and rear as well as a removable 8-3/4" high front blank panel. The control cabinet weight is 152 lbs.

BITE SYSTEM

The BITE system consists of RF detection circuitry in each basic power module. This circuitry detects the status of each BPM and transmits the information to the control cabinet front panel, Additionally, the system status indicator detects status of all antenna BPM's and displays a failure when four or more BPM's fail.

The BITE circuitry employs a multiplexing scheme for transmittal of data from the antenna to the control cabinet. This significantly reduces the quantity and weight of the interconnecting cables and is very advantageous for the 1 kw system.

The BITE circuitry is designed for "failsafe" operation. If any cable, connector, or voltage is interrupted, the system reverts to the failure mode.

The power cable required to provide DC power to the antenna BPM's originates in the control cabinet. The weight, voltage drop and flexibility of this cable are a prime consideration to reduce system costs and increase system efficiency and maintenance. A study was made on wire voltage drops based on a 30-foot run using various wire sizes tc handle a total requirement of 30 amperes with a

two-way line drop of .5V. Additionally, the line drop for a 50°C ambient was calculated to note what impact the ambient would have.

A second analysis was made on wire weight based on a 30-foot run using the same wire sizes used in determining line drops.

The conclusions gained from the above analysis and tradeoffs show that a cable using a total of 12 no. 8 AWG wires, (6 to and 6 from the load) would provide a line drop of less than 0.2 volts, a weight which is 40% lower than the next reasonable size and number of wires, and would provide reasonable flexibility for the cable. A standard military connector is available to handle the size and number of no. 8 AWG wires.

AMPLIFIERS

Twelve identical amplifiers are used to derive the required 100 watts of power output at the antenna. Each basic power module (BPM) consists of two hybrid added power stages driven by another pair of hybrid added low level stages. Integral with each BPM is a low loss output isolator to protect the output stages from accidental mismatch conditions. Following the isolator is a tubular low pass filter designed to reject the second harmonic of the 4.4 to 5.0 GHz input signal. TRW MRA-271 type bipolar transistors are used as the power output stages. They consist of five parallel-combined chips with internal input and output impedance matching. The driver for these stages is a TRW MRA-272. This is a single chip version of the MRA-271.

In order to properly drive each of the 12 antenna matrix BPM's to its full output power, an IPA module consisting of a driver and two hybrid combined BPM's is used. The BPM's are identical to those at the antenna, thus a total of 14 BPM's are used in this system.

The IPA driver module is a two-stage amplifier. The input stage is a GaAsFET and the output stage is a TRW MRA-272. The driver output is split two ways in order to provide the required RF drive to the IPA BPM's. A GaAsFET was selected for the input stage because of its high gain, stability, bandwidth, and ease of controlling gain.

The amplifiers are all constructed using a combination of microstrip, stripline and lumped element circuit techniques. An extensive investigation was conducted to determine the optimum substrate material for the circuit networks. Insertion loss, bandwidth and cost were the drivers. The materials considered were 99.5% Alumina, Teflon fiberglass, and Epsilam 10. Alumina was selected for the circuit elements, and Teflon fiberglass for the hybrid combiners and splitters. A detailed description of this investigation follows.

SUBSTRATE MATERIAL

MATERIAL EVALUATION

Though ITTDCD has used several different substrate materials, Alumina has been the most popular. Recently, DCD has studied less expensive materials for use in the PA[3] modules including Epsilam-10 (3M), Teflon fiberglass, and fused quartz. Teflon fiberglass and fused quartz are unacceptable because their low dielectric constant makes them incompatible with the 3 dB hybrids. The hybrids must launch into a material with a higher dielectric constant, so that the interface does not radiate.

Since Epsilam-10 is less expensive than Alumina, an extensive comparison of the two materials was performed. The two differ mainly in loss tangent, thermal coefficient of expansion, and α_T (loss in dB/m).

Two identical single resonator filters were constructed on the respective substrate material. All measurements were performed on an HP 8542B Automatic Network Analyzer. After an initial measurement was made, both filters were subjected to temperature and humidity extremes. After each environmental stress, the filters were retested at room temperature. The results show that Epsilam-10 is more lossy than Alumina due to a substantially lower Qu and its tendency to absorb moisture. This excess loss and undesirable tendency to alter characteristics via water absorption far outweigh its cost advantage. Thus Alumina was chosen as the substrate material.

SUBSTRATE BONDING

Previous programs at ITTDCD have extensively investigated the substrate/carrier interface. One major concern is the separation of the bond between these elements as a result of environmental factors. The standard technique employed at DCD has been Alumina epoxied to a Kovar carrier. This was reliable over environmental extremes, but increased weight and cost.

The Global Positioning Satellite (GPS) program at DCD had, as a prime consideration, weight. Thus, an investigation of reliable and lightweight substrate bonding techniques ensued. The results of this analysis led to a technique of bonding Alumina to aluminum. This technique was subjected to repeated thermal cycles (>40) without separation. As a result, ITT Procedure PS1051 is the standard techniques used to bond Alumina to aluminum.

For the Phased Array Antenna Amplifier program, this technique has allowed DCD to reduce the weight of a basic power module by approximately .5 pounds. Additionally, the expense of machining Kovar has been eliminated.

The construction approach for the amplifier provides for a "stepped" profile heat sink. The machined heat sink is used as the base of the BPM. This profile is used to mount the substrates and transistors directly to the heat sink. Thus, no carriers are used and the thermal resistance from the transistor case does not include a carrier interface. This approach optimizes transfer of heat from the transistor to the ambient and increases overall performance.

TRANSISTORS

Three transistor types are used in the amplifier chain. The power output stages and their lower power drivers are TRW devices, MRA-271 and MRA-272 respectively. The IPA's first stage is a GaAsFET while its second stage is an MRA-272. Both bipolars and GaAsFET's were considered for this application. Power output, gain, efficiency, bandwidth and cost were evaluated before selecting the TRW bipolar devices. At the present time, these bipolars have a

significant advantage in output power and cost ($/watt) over available FET's. Improvements in both types of devices are expected and the comparison is being continually updated to reflect the latest devices.

Samples of the MRA-271 and 272 type transistors have been evaluated. Tests performed included:

- P_{out} vs. frequency
- P_{out} vs. drive
- P_{out} vs. collector voltage
- Phase vs. frequency and collector voltage
- Phase vs. drive
- Dynamic phase tracking

These tests were performed for both single stage amplifiers and two combined driver stages and two combined power stages.

Analysis of test data Figures 11 through 16 show that the two transistor's performances vary as a function of frequency. If a constant drive level vs. frequency were set for this system, performance could be as shown in Figure 17 These curves are a composite projection of BPM performance based upon Figures 11 through 16 at a constant input drive level. Obviously the loss of efficiency at the low end and -2.0 dB falloff in P_{out} at the high end is not desirable.

Based upon this analysis and the AN/GRC-143 output drive level variation of $\sim$ 4 dB (+20 dBm to +24 dBm), an input gain control was added. This has conveniently been incorporated by adjusting the bias of the IPA driver GaAs FET stage. As a result of this design, the operator would set the RF gain control to produce a fixed total output power at each operating frequency. Thus at 4.4 GHz the drive would be reduced to provide operation of the BPM's (Figure 18) at their optimum P_{out} to improve overall efficiency without sacrificing total power output.

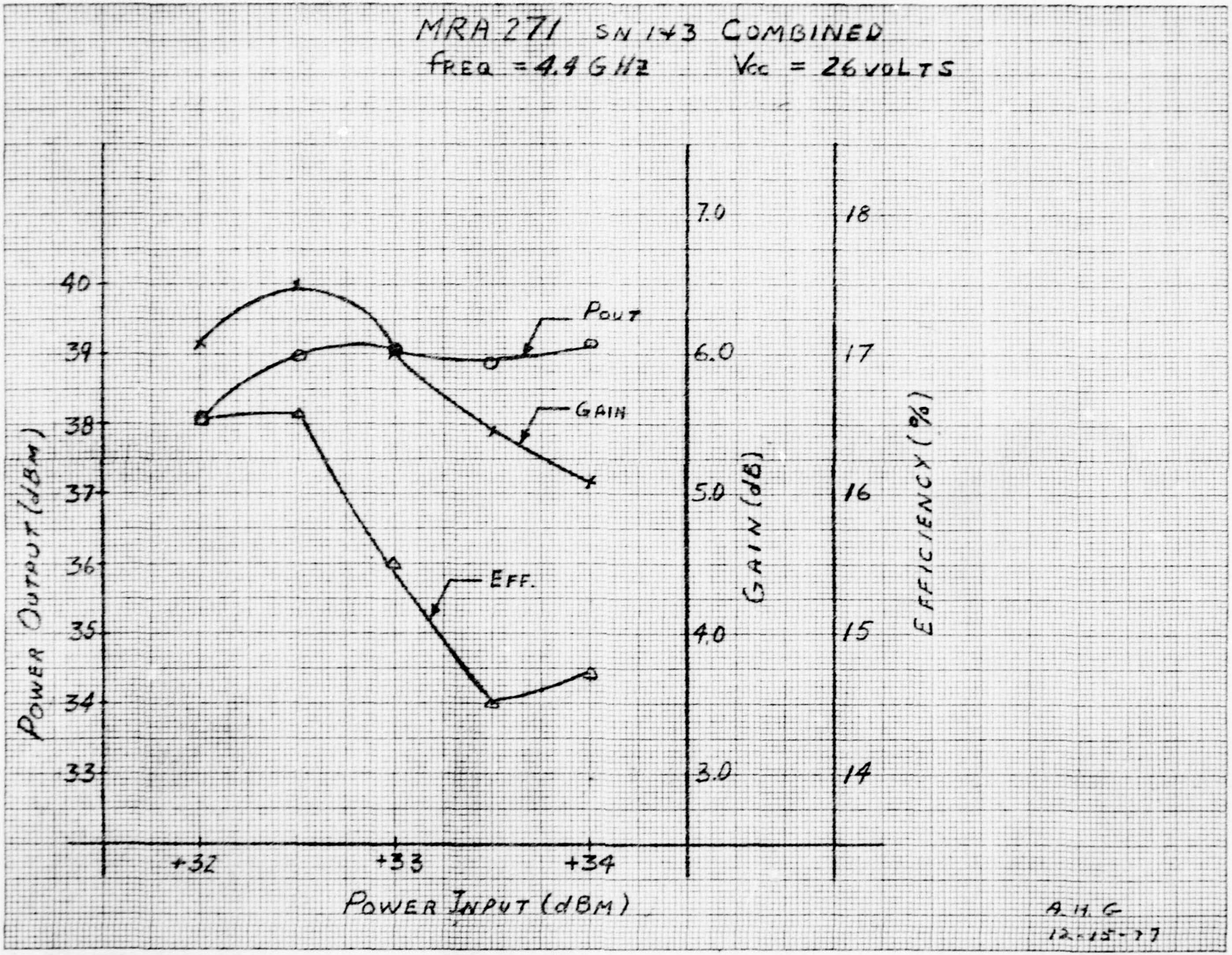


FIGURE 11

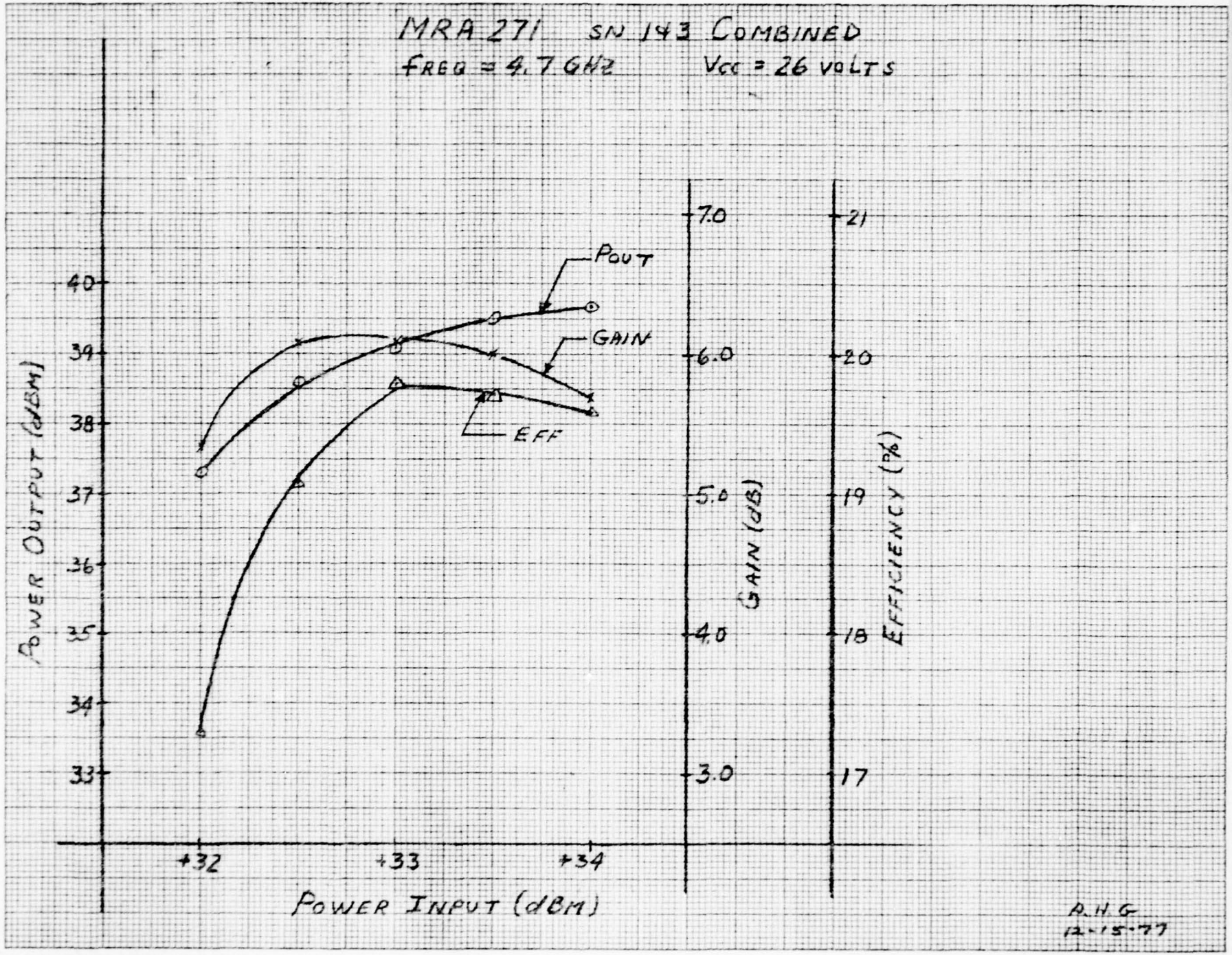


FIGURE 12

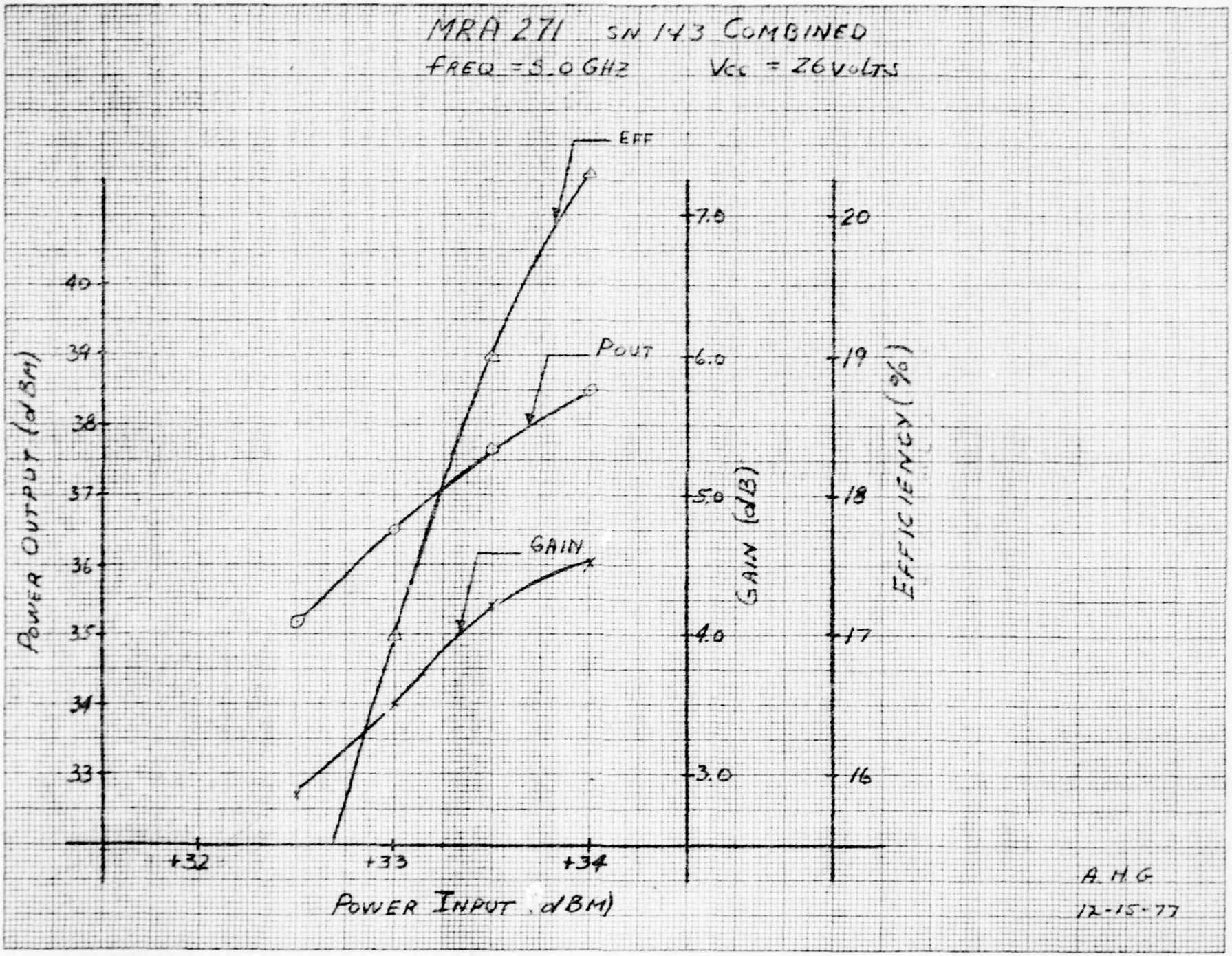


FIGURE 13

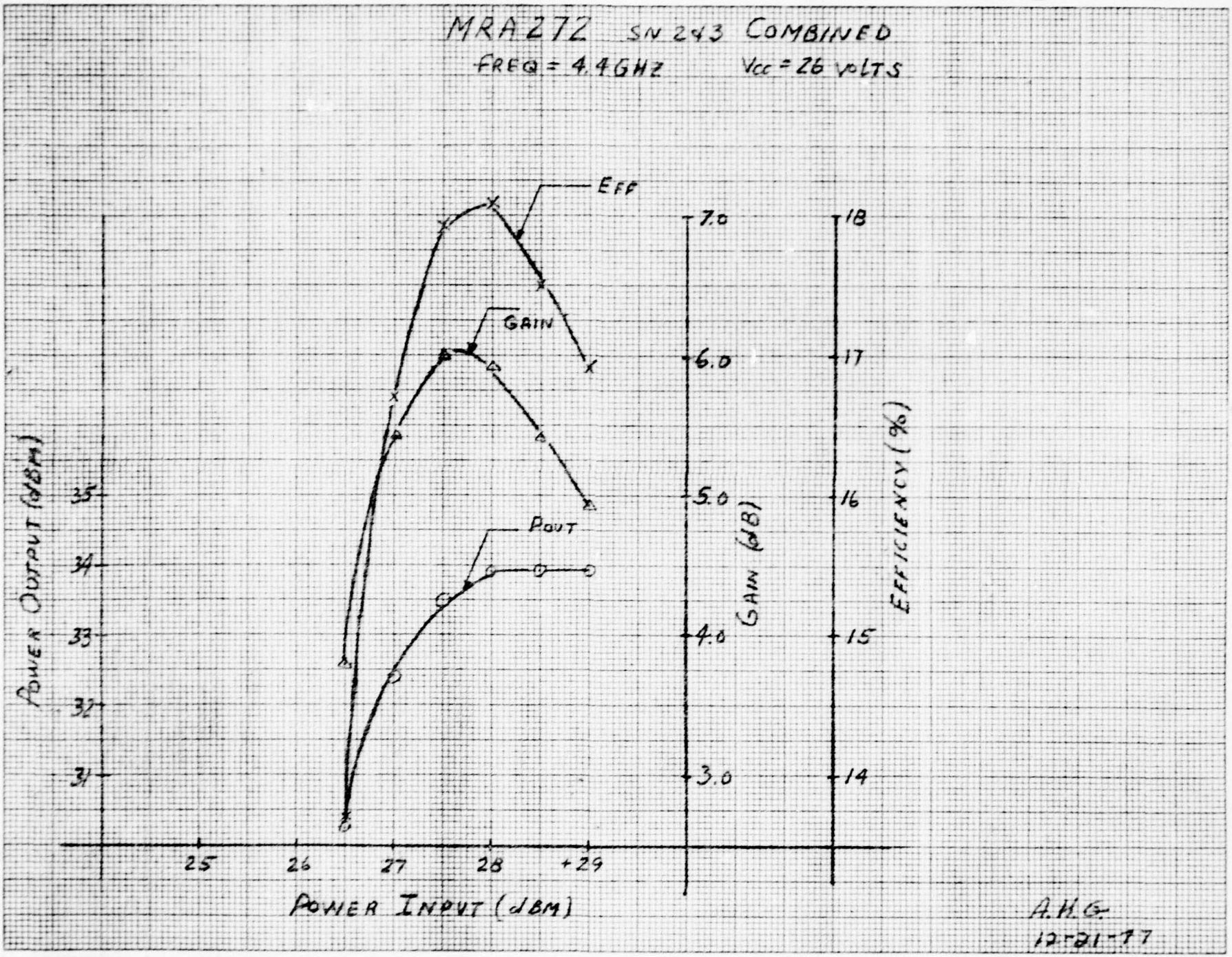


FIGURE 14

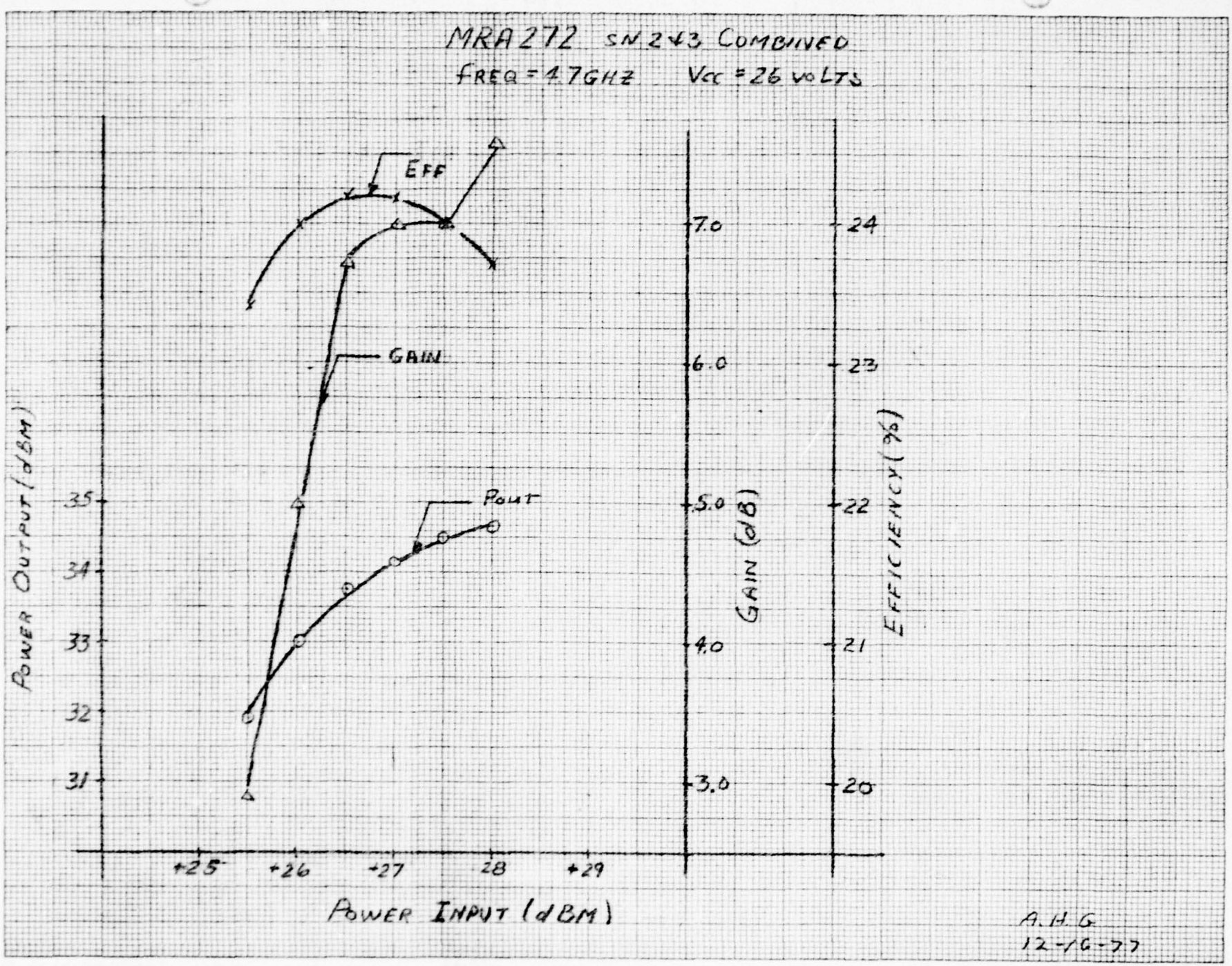


FIGURE 15

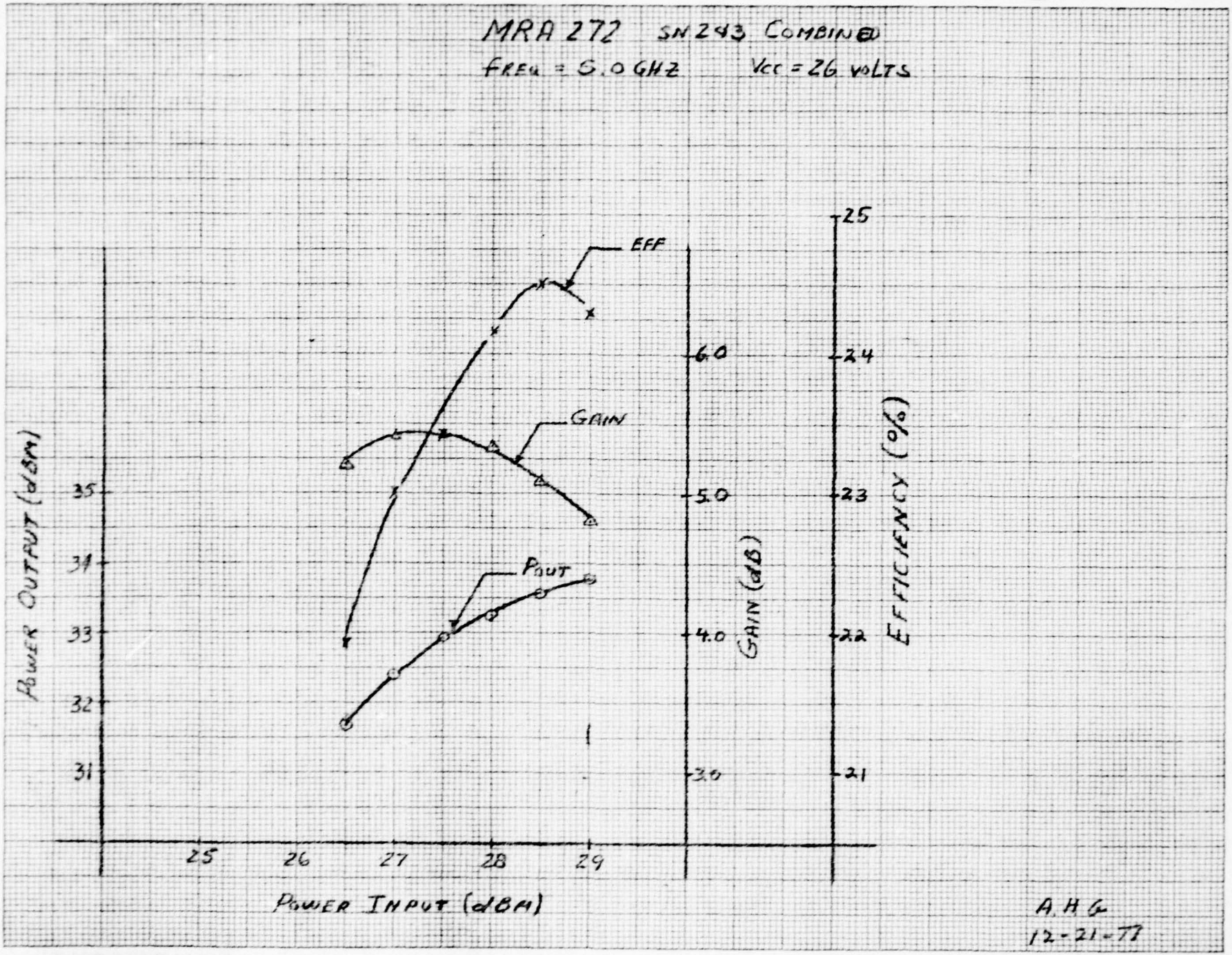


FIGURE 16

PROJECTED BPM PERFORMANCE

MRA 272 SN 243
MRA 271 SN 143
V_{CC} = 26 VOLTS

BASED UPON CURRENTLY AVAILABLE DEVICES AND CONSTANT INPUT DRIVE OF +28.2 dBM

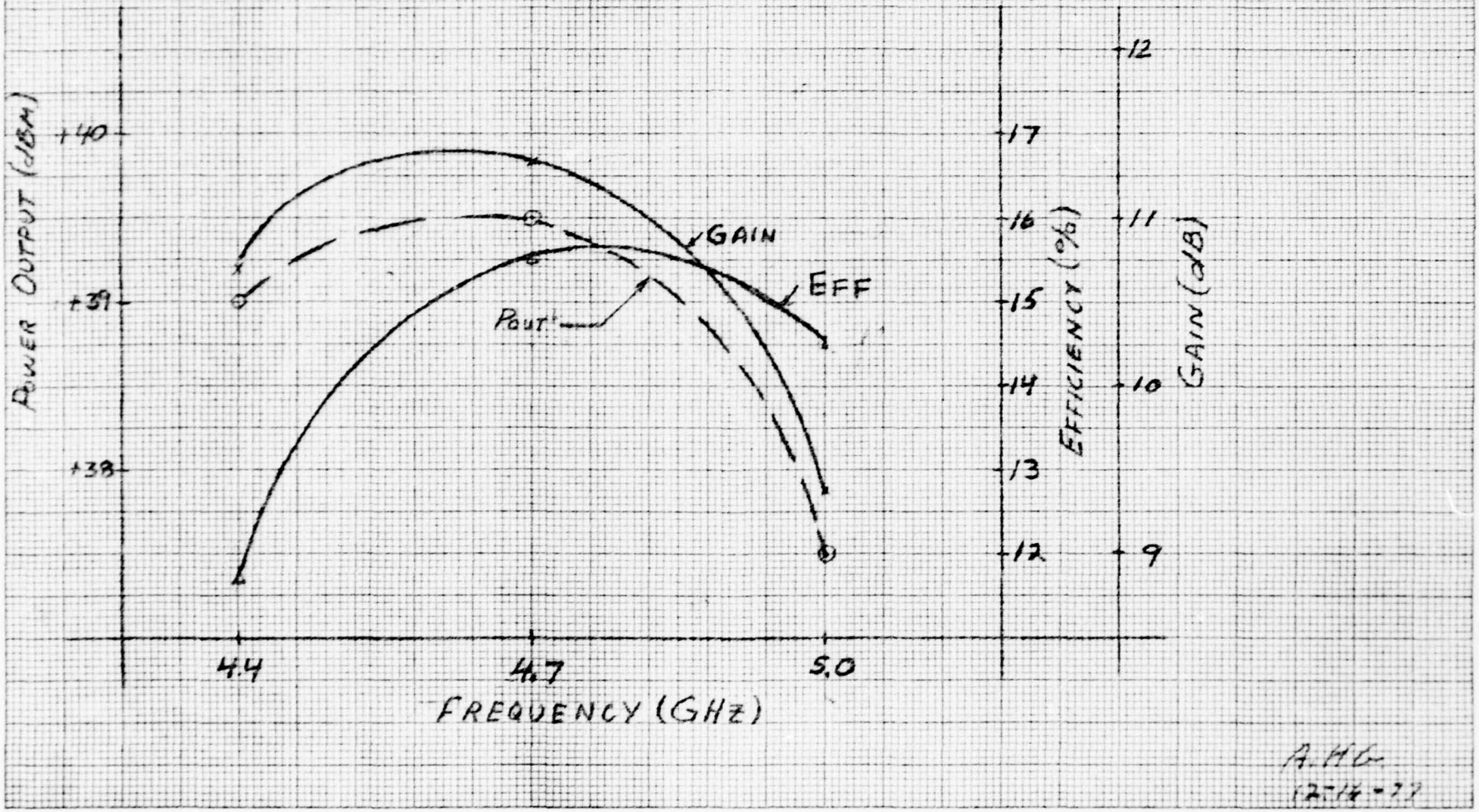
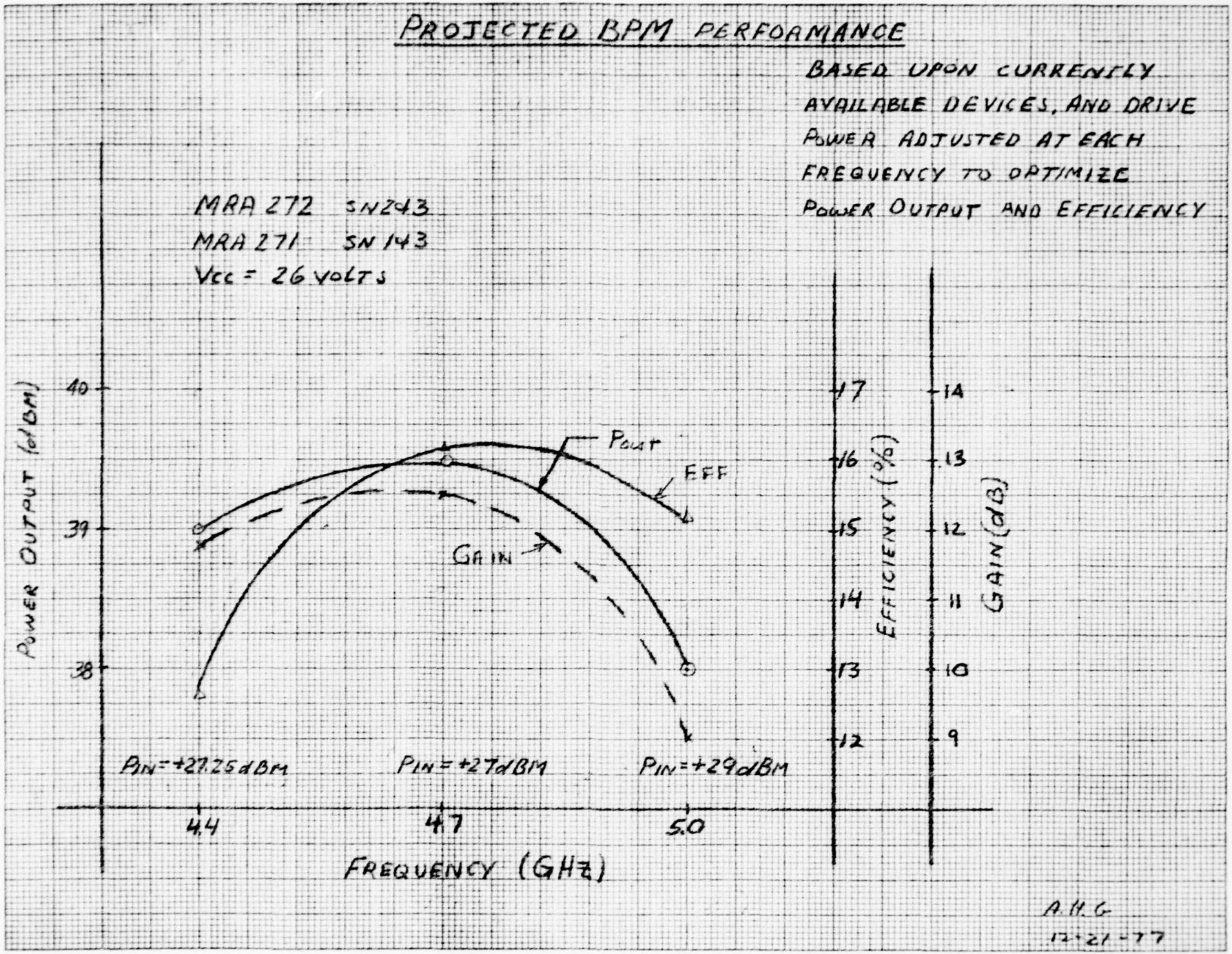


FIGURE 17

A. H. 12-14-77

PROJECTED BPM PERFORMANCE

BASED UPON CURRENTLY AVAILABLE DEVICES, AND DRIVE POWER ADJUSTED AT EACH FREQUENCY TO OPTIMIZE POWER OUTPUT AND EFFICIENCY



A.H.G
12-21-77

FIGURE 18

The curves and analysis presented are for a limited sample of devices. However, the flexibility of setting drive level to avoid hard saturation (4.4 GHz) or overcome lower gain 5.0 GHz provides a system with more uniform performance vs. frequency. Thus system narrowband performance would follow curves of Figure 18 rather than 17

Though most data is shown at collector voltage of 26 VDC, ITT recognizes that device performance will vary with collector voltage. During the evaluation phase of the BPM, overall performance (P_{out}, EFF, gain) will be evaluated under collector voltage variation.

ANTENNA DESIGN

During the design phase of this program, several alternate approaches were considered for the antenna. The matstrip configuration was chosen with the following tradeoffs analyzed:

- single laminate (incorporating receive and transmit dipole arrays on one laminate) versus a dual laminate design (one receive, one transmit separated by a polarizer laminate).
- one piece construction (per laminate) versus sectionalized construction.

The antenna design selected for the scale model system is a dual layer design with one piece construction for each laminate. The following paragraphs discuss each choice.

SINGLE VS. DUAL LAMINATE ANTENNA DESIGN

SINGLE VS. DUAL LAYER ANTENNA SELECTION

The choice of single versus dual layered antenna configuration weighed the immediate needs of this R & D program against the long-term needs of future production programs. Viewed in terms of program goals, the dual layer antenna is the logical choice for developing a one-tenth size antenna-amplifier

that demonstrates the feasibility for space-addition of low power modules for solid-state troposcatter amplifier systems. Conversely, the single layer structure is the logical choice for a 1 kw antenna-amplifier system due to lower weight and cost plus ease of maintenance.

The antenna is required to be dual polarized: two independent arrays superimposed in a single aperture, independent access and distribution networks, efficient radiation of two uncoupled pencil beams of orthogonal polarizations. Two alternatives for the practical realization of a dual antenna system using printed circuit techniques are:

A) Single layer: a single (thin) printed circuit sheet containing two dipole arrays with their associated distribution circuits (corporate feeds), positioned above a single ground plane. The risk feature of this structure is the attainment of a printed layout which accommodates two orthogonal array-feed systems with a minimum of cross coupling.

B) Dual layer: a structure in cross-section of three (thin) printed circuit sheets positioned above a ground plane, and superimposed one above the other. Two sheets each contain one printed planar dipole array with corporate feed; the third sheet contains a printed "polarized" ground plane, i.e., transparent to one polarization and totally reflecting to the orthogonal polarization. The difficult aspect of this structure is the three-dimensional interlacing of two independent (dual) antenna systems with a minimum of cross coupling.

In the development of the 1:10 scale antenna, the dual layer design provides a known basis of antenna performance on which to build an integrated amplifier system. That basis is the expertise acquired by ITT in developing similar antenna configurations at X-band. Performance consistent with the needs of this program were attained at X-band.

ONE-PIECE VS. SECTIONALIZED CONSTRUCTION-VENDOR SURVEY

An area of investigation and study early in the program was the consideration of fabricating single large array sheets (38" X 38") or sectionalizing to smaller sheets (2,3,4, etc.) to form the large single array. Manufacturers with capabilities to supply and process large laminates had to be located. This was accomplished.

The single large board approach has certain obvious advantages such as decreased handling, simpler alignment procedures, and electrical continuity. A sectionalized, piece-part approach would serve to compound problems such as continuity, tolerance/registration, and system integrity.

Several prospective array materials were investigated and evaluated during the initial survey. As a result of this analysis and the advantages stated above, the single piece approach will be implemented.

For the Final Report, analysis will be provided on the design feasibility of a single laminate dual array antenna design for a full scale 1KW model. Cost, weight, and complexity comparisons will be provided between the two approaches.

ANTENNA DESIGN

PERFORMANCE REQUIREMENTS

The following tabulation shows the antenna performance as required by ECOM Specification DS-EH-0238A (A), 16 Aug. 76; and ITT's current estimate determined by performance budgets derived from analysis and measured results.

	ECOM DS-EH-0238A (A)		
Item	Para.	Specification	Current Estimate
Size	3.4.1.1	10 sq. ft. max.	10 sq. ft. (aperture)
RF connectors	3.4.1.5	Rx:WR-187;Tx:Type N	As required
Frequency	3.4.2.1	4.4 to 5.0 GHz	As required
Gain	3.4.2.1	30 dBi min:Tx	31.05 dBi
		30 dBi min:Rx	30.22 dBi

Item	Para.	Specification	Current
Beamwidth	3.4.21	5^{o} max., E & H Plane, Tx and Rx	4.2^{o} - 4.4^{o}
Polarization	3.4.2.3	Transmit: $+45^{o}$	As required
		Receive: -45^{o}	As required
Sidelobes	3.4.2.4	15 dB max. 18 dB goal	18 dB max.
VSWR	3.4.2.5	1.5:1 max. Tx & Rx	1.5 max. Tx & Rx

CAD ARRAY PROGRAMS

Computer aided design played a key role in determining which array design would be chosen for the 100 watt system. Two computer programs were written during this antenna development and can be extended to the 1 kw system. Based upon the analysis of the CAD, an array layout evolved which meets or exceeds all requirements of the specification. Additionally these programs allowed analysis of the transmit antenna design under conditions of unequal phase and amplitude excitation. This provided ITT with the information to establish system BPM amplitude and phase budgets for expected antenna performance.

Program I Calculates and plots relative far field amplitude in dB versus angular position, usually scan angle (Θ) with the second coordinate angle (Φ) held constant. Fine incrementing of the angle and interconnection of points in plotting provide a continuous curve; a point by point tabulation can be an alternative output. Since this type pattern is a cross-section of the volume of space into which the antenna radiates, many patterns are required to determine the full spatial response. Characteristically, principle planes of concern are identified and plotted according to the antenna type and system application, thus, an assumption or pre-knowledge is needed to select the pattern coordinates to be plotted. The program incorporates the following:

- Dipole element pattern — represented by an analytic equation derived for sinusoidal excitation.
- Ground plane pattern — represented by an image dipole array.
- Array factor — calculated by vectorial summation of all dipole elements.
- Illumination — amplitude and phase of current at each dipole can be specified and applied in the vector sum; this includes error functions of which the random type can be generated by the program.

Figure 19 shows plots generated by Program I.

Program II Calculates and plots a three-dimensional far field pattern of amplitude versus both angular coordinates and, also calculates antenna directivity, an aspect of gain. The 3-D pattern plot is analogous to a topological or contour map which represents elevation at a location specified by longitude and latitude; here field amplitude is plotted versus spatial position and where the plane of the map represents the surface of the far-field hemisphere the surface of constant distance from the antenna center. The computer output to a teletype terminal is used for this plot by equating the two orthogonal spatial coordinates ($SIN\,\Theta\,COS\,\Phi$, $COS\,\Theta\,SIN\,\Phi$) with row-column locations, and the amplitude with an alphanumeric symbol suitably defined in a key-code table. Thus, this program output surveys the full extent of the radiated space at a selectable number of discreet points, a feature which compliments Program I by providing the "pre-knowledge" for choosing a particular cross-section to be plotted in the amplitude versus scan angle format. Program II, in addition, calculates directivity as the ratio of boresight power to the sum of the power at all points averaged over the full surface. The directivity output is printed as a number in dB following the pattern plot. The program features:

- Calculation of the dipole element pattern by direct integration of the (sinusoidal) current along the dipole length. This allows direct use of the program for harmonic analysis as well as fundamental analysis over any bandwidth.

- Calculation of ground plane effect by image dipole array at twice the ground plane spacing; again this provides extended bandwidth and harmonic analysis capability.
- Calculation of array, or lattice, factor by vectorial summation of all array elements at any far field point in space thereby providing a non-approximate base for analyzing any shape array, or grid; or error pattern.
- Provision for specification of any amplitude and phase excitation in the dipole array; this includes generation of random excitations.
- Calculation of directivity or gain.
- Variable incrementing of the coordinate space angles for finer steps at the broadside main beam angles.

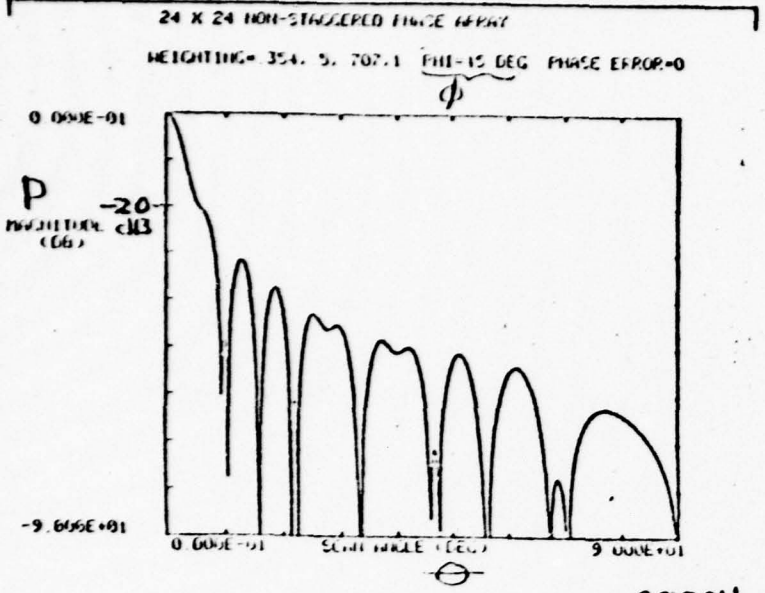
Program II - Output Format

The contour map produced by this program is shown in Figure 20. Displayed is a series of typed alphanumeric symbols which have the following meanings:

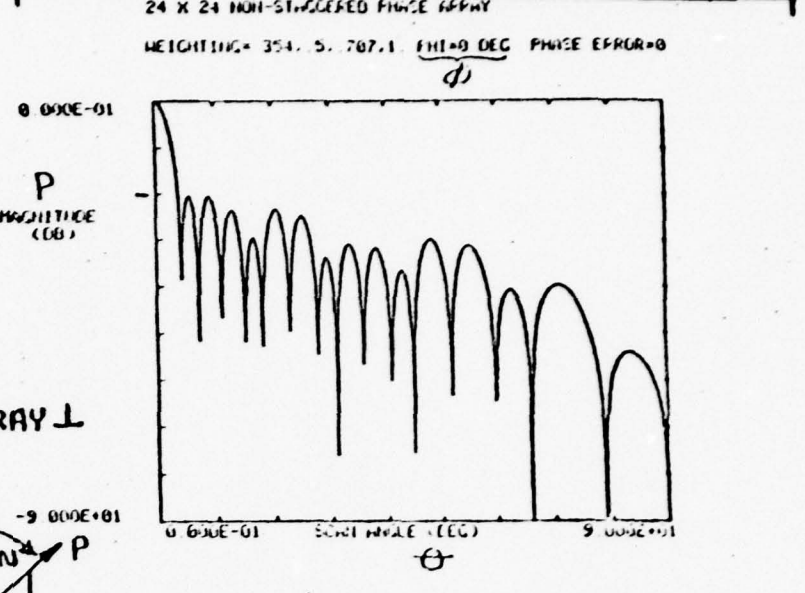
- Value of the symbol is assigned, arbitrarily, to a range of powers calculated by the program in dB. Each program run establishes a table of symbol versus power; all positive dB are loss ratios.
- Location of a symbol in the printed array corresponds to a unique pair of coordinate angles: Θ, Φ. The coordinate pair is systematically stepped over a full hemisphere using the following angular ranges: $0^\circ \leq \Theta \leq 90^\circ$ $0^\circ \leq \Phi \leq 360^\circ$. In cases of known symmetry a lesser range is used.
- Gain is outputed as a single numeric, in dB, referenced to the angular position: $\Theta = 0^\circ$; $\Phi = 0^\circ$. This is the axis normal to the array and the nominal center of the main pencil beam. Thus, the gain reflects losses due to beam squint as well as due to beamwidth and sidelobe

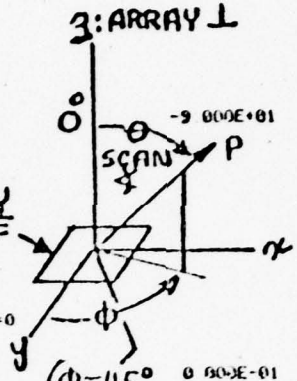
DIPOLE AXIS

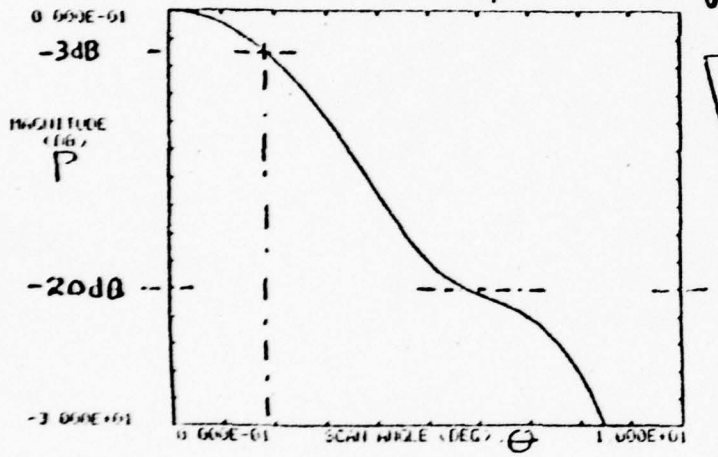
INTER-CARDINAL PLANE

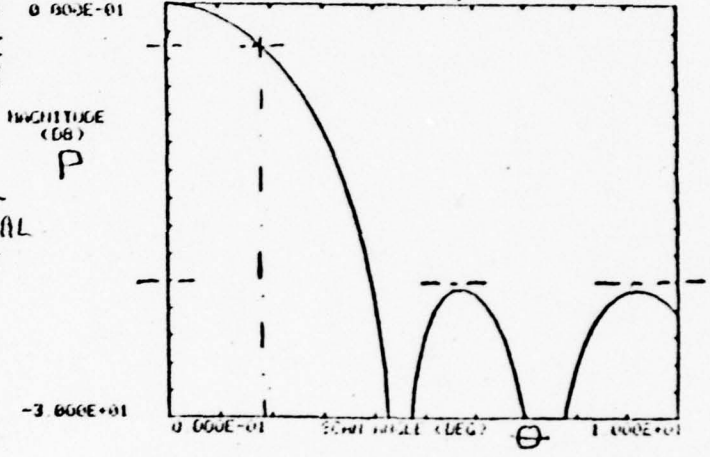


HORIZONTAL OR VERTICAL PLANE









PA³ 51-34 MIL
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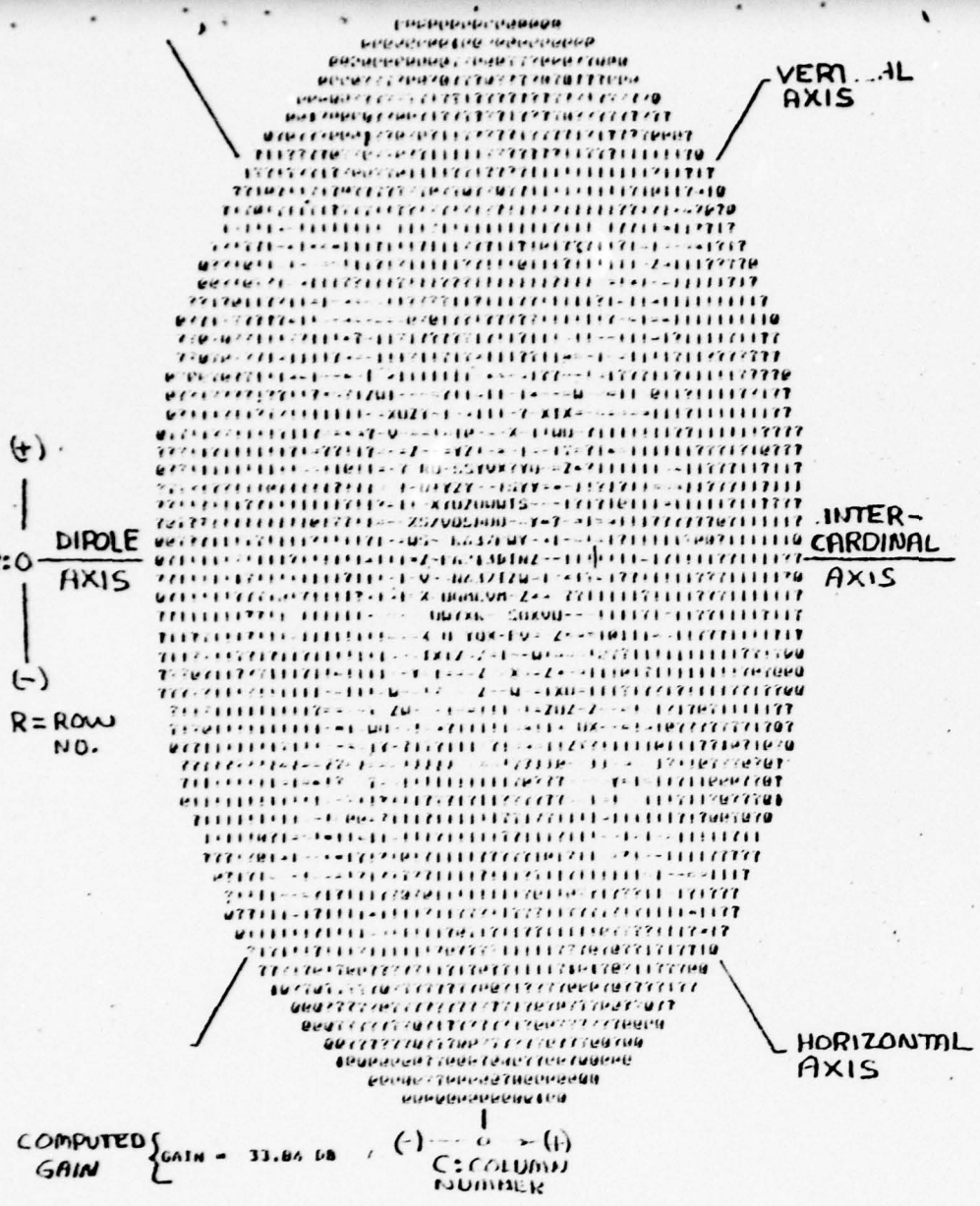
FIGURE 19 : COMPUTED PATTERNS-4 STEP TAPER (NO ERRORS)



SPACING BETWEEN ELEMENT CENTERS = 1.600 IN.
FREQUENCY = 4.700 GHZ
HALF DIPOLE LENGTH = 0.250 WAVELENGTHS AT 4.7 GHZ
DIPOLE TO IMAGE SPACING = 0.500 WAVELENGTHS AT 4. HZ
NUMBER OF ELEMENTS = 576
* ANGLE INCREMENT AT CENTER = 1.910 DEG.

RMS AMPLIFIER PHASE ERROR (UNIFORM DISTR.) = 20.00 DEG.
1 SIGMA AMPLIFIER AMPLITUDE ERROR (GAUSSIAN DISTR.) = 1.50 DB
1 SIGMA ELEMENT PHASE ERROR (GAUSSIAN DISTR.) = 20.00 DEG.
1 SIGMA ELEMENT AMPLITUDE ERROR (GAUSSIAN DISTR.) = 0.30 DB

VOLTAGE WEIGHTING FACTORS FOR GROUPS OF 4 DIPOLES

0.500 0.500 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.500 0.500

0.500 0.500 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.500 0.500

0.354 0.354 0.500 0.500 0.707 0.707 0.707 0.707 0.500 0.500 0.354 0.354

0.354 0.354 0.500 0.500 0.707 0.707 0.707 0.707 0.500 0.500 0.354 0.354

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0.354 0.354 0.707 0.707 1.000 1.000 1.000 1.000 0.707 0.707 0.354 0.354

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0.500 0.500 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.500 0.500

0.500 0.500 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.354 0.500 0.500

PLOTTING FUNCTION

POWER VS SPACE *S: θ, Φ

KEY TO DD VALUES OF CHARACTERS ON PLOT

0 1 2 3 4 5 6 7 8 9

-10 ..
0 0011223344556677889999
10 AABBCCDDEEFFGGHIJKLMM
20 NNOOPPQQRRSSTTUUVVWWXXYYZZ
30 [illegible]
40 [illegible]
50 [illegible]
60 [illegible]
70 [illegible]
80 [illegible]
90 [illegible]

$\Phi = 45 + \tan^{-1}\frac{C}{R}$ DEG

$\theta = 1.91^{*}\sqrt{C^2+R^2}$ DEG

R ≡ ROW NO. OF PLOT

C ≡ COLUMN NO. OF PLOT

* PROGRAM CALL-OUT

*** ROW NUMBER 2 ***

AMPLIFIER PHASE ERRORS (DEG.)

15.52 10.26 11.12 -16.60 17.44 -13.34 9.09 19.79 5.50 -11.28 -13.29 17.62

AMPLIFIER AMPLITUDE ERRORS (DB)

0.75 -0.56 0.95 0.22 0.25 -0.18 1.09 -0.04 -0.38 -0.04 -0.44 -0.23

FIG. 20

CAD-PROGRAM II CONTOUR ANTENNA PATTEI

A

J

structure. The dB output is a positive number for the increase in power of the array compared to a single isotropic radiator of zero dB power.

Thus, the data format shows the usual pattern characteristics of amplitude versus coordinate scan angles. Beam peaks, nulls, sidelobes can be located by "reading" their amplitudes from the key-code table; beam location, beam-width, sidelobe or null location can be read by counting their grid position and de-incrementing according to the projection scheme.

Program Validation

Both programs were validated by applying cases of known solution: uniform illumination of a square array which has a well known analytic solution; multiple beam pattern at the 2nd harmonic whose solution was hand-calculated. Both cases showed equivalent results between the program and derived solution.

TRANSMIT ARRAY ELECTRICAL DESIGN

SELECTION OF ANTENNA TYPE

The requirements affecting the choice of antenna type are:

- Specifications for gain, sidelobe, polarization and size.
- Twelve (12) inputs
- Simultaneous transmit and receive operation in a common aperture
- Future requirements for economic manufactureability

The antenna type chosen is a printed circuit dipole array in an ITT developed technique termed "matstrip". The features of matstrip which make it particularly suited for this application are:

- Corporate feed and dipoles printed on a single sheet.
- Dipole elements are singularly polarized and inherently isolated from quadrature polarizations.
- Array functions with both solid (reflection of all polarizations) and semi-transparent (reflection of only one polarization) ground plane.
- Dual polarization can be achieved by stacking arrays in a common aperture.
- Corporate feed technique allows amplitude tapering and accommodates multiple inputs with no special techniques, i.e., focusing or phasing problems.
- Scaleable and modular to attain any aperture size.
- Flat form factor provides convenience in integrating amplifiers into antenna.
- Highly reproducible due to printing techniques.

RECEIVER ARRAY ELECTRICAL DESIGN

The receive array requirements differ from the transmit array only in polarization (-45^{o} off horizontal) and number of inputs 4. The polarization will be attained by 90^{o} rotation of dipoles in an array very similar to the transmit array. The main difference being the combining of the former 12 inputs into four outputs by replacing the original balun with two-way combiners and extending the corporate feed to sum the 12 equal outputs into four balun outputs.

The scheme provides an identical aperature taper as for transmit and, consequently, identical directivity and sidelobes. However, the net gain is reduced from the transmit case by the added line loss of the extended feed in the matstrip.

The components and design plan for the receive array are basically the same as transmit, except the final dipole matching is done with the receive array located between the transmit array and the background panel.

ELEMENT TEST RESULTS

Because of the similarity of the receive antenna and transmit antenna, design and test of antenna elements apply to both configurations. These elements are corporate feed lines, baluns, power divider, and dipole design.

Corporate feed lines: for the matstrip material, the insertion loss per unit length had to be determined for the 4.4 - 5.0 GHz band. Testing on an Automatic Network Analyzer HP 8542, using two identical circuits differing only in length, established this parameter to be .04 dB/inch. Corporate feed losses included in the antenna budgets are based upon this result.

BALUN DESIGN

The balun design uses a proprietary technique wherein the marriage of a power divider with an infinite balun concept provides special symmetry conditions that result in a low VSWR and unusually quiet (non-radiating) transformation from a grounded coax mode to an ungrounded two-wire mode. This design has been successfully employed at X-band where VSWR's of 1.15 maximum were achieved with maximum losses of 0.5 dB.

A breadboard design has been tested and modified for impedance matching. A single balun VSWR less than 1.10 has been achieved; this exceeds the design goal of 1.15 VSWR. The completed design uses a revised connector design of a simple construction using standard connector components, which achieved a 1.02 to 1.03 VSWR over the 4.4 - 5.0 GHz range.

Figure 21 shows final balun VSWR and impedance data for the 4.4 - 5.0 GHz frequency range. Actually what is shown is the frequency response of a pair of baluns "back to back", i.e., from a coax input into a balun with a pair of two parallel conductor feed line outputs, which are re-combined into a second balun with a coaxial output. Thus, the "back to back" test circuit uses two baluns separated by lengths of line of approximately three wavelengths; consequently, what is measured is the interaction of two balun VSWR's combining with all possible

phases. For this condition, the peak VSWR results from a phasing condition wherein the individual balun VSWR's combine as a product; hence, for a total VSWR of 1.15, the individual balun VSWR is: $\rho_{BALUN} = \sqrt{\rho_{TOT}} = \sqrt{1.15} = 1.07$; allowing for tolerances, a maximum VSWR of 1.10 can be expected from a typical balun assembly.

POWER DIVIDER

Two-way and four-way dividers are required for this application. The four-way is considered in the dipole development because it is closely integrated into a 2 X 2 dipole array. The significant design parameters are impedance (for a given material and thickness) and phase length. Additionally, the impedance levels of input and output lines need be specified.

A breadboard model has been completed. A maximum VSWR of 1.19 (Figure 22) was achieved for a composite circuit of two baluns and two power dividers arranged "back to back". Using worst case phasing and a balun VSWR of 1.08, the divider VSWR (P_D) is:

$$1.19 = P_T = 1.08 \times 1.08 \times 1.08 \times P_D \times P_D, \quad P_D = 1.19 - (1.08)(1.08)$$

$$P_D = 1.01$$

DIPOLE DESIGN

The dipole presents four basic design problems:

- Impedance-bandwidth characteristics which are resonant (highly frequency dependent); the important parameters are the dipole length to width ratio and dipole length.
- Feedline-dipole junction reactances can attain significantly large values and distort the basic dipole impedance. This requires an essentially experimental solution because of the difficulties in calculating reactances.
- Impedance variation due to mutual coupling in an array environment. Since this is a non-scanning array, only the broadside beam (0° scan)

BALUN PAIR - BACK TO BACK

51-34412, J.RANGHELLI 12-9-77

BALUN DEVELOPMENT
NEW CONNECTOR; NEW ARTWORK
.134XFM; PORT 2

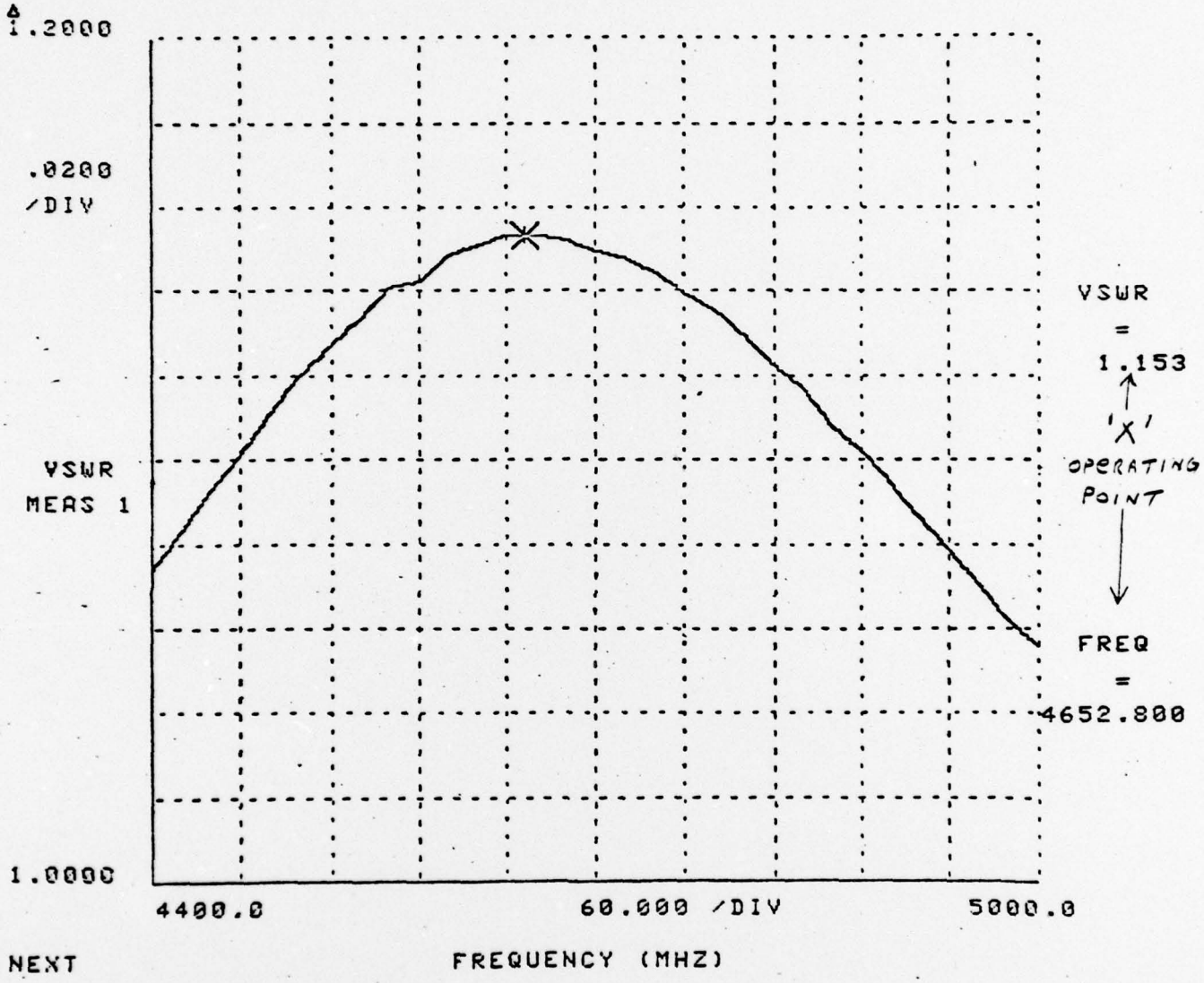

FIGURE 21 : MATCHED BALUN - MEASURED DATA

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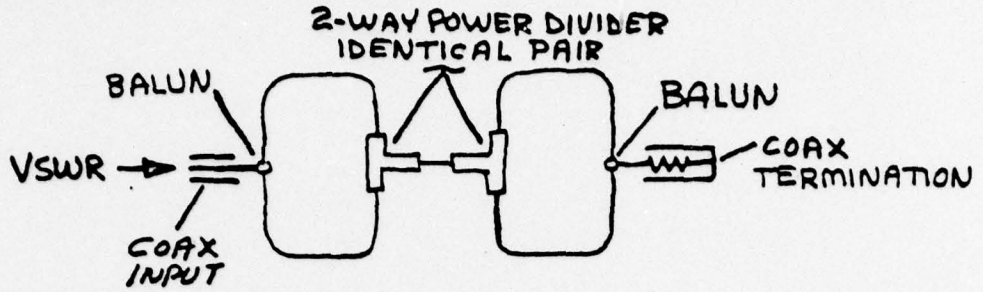

J1-34412,JRANGHELLI 12-10-77

2-WAY POWER DIVIDER DEVELOPMENT

INITIAL DESIGN WITH NEW BALUN:.134XFM

MOD:L2=.50,W2=.12;P1

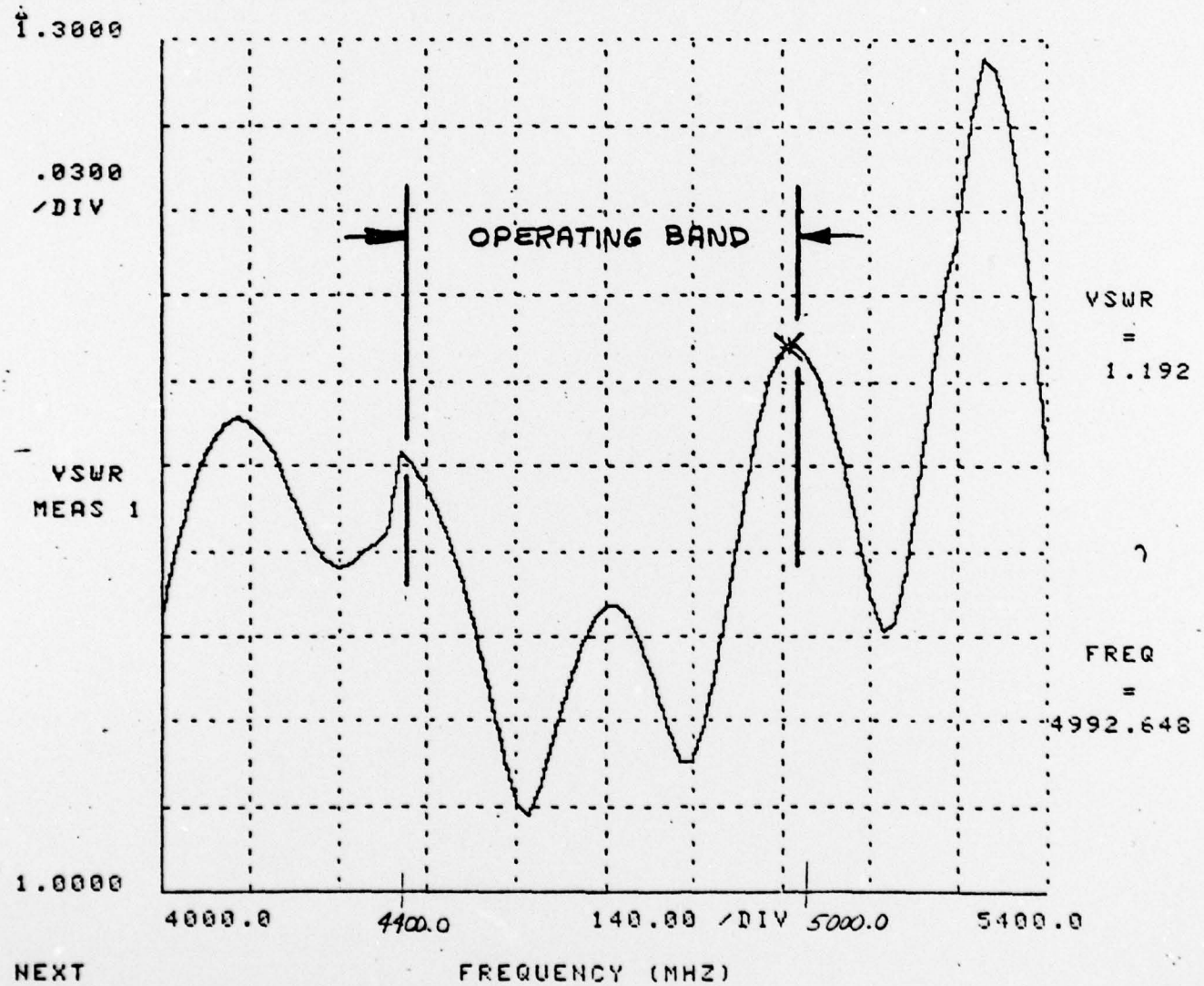

FIG. 22 2-WAY DIVIDER MEASURED DATA

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57

position need be considered. Calculated solutions usually deal with the variation of impedance with scan assuming a matched impedance at 0^{o} scan. The 0^{o} match is usually achieved experimentally because of the difficulties cited above. This is further complicated in this application by the presence of a compound aperture containing other polarizations, feed lines, and polarization filters. Consequently, an important task will require the experimental matching of the dipole impedance in a total array environment; this includes, besides the PCB's, the radome and interlayer filler materials.

- Pattern characteristics effect gain, sidelobes, beamwidth and polarization. Factors effecting patterns are dipole length, length/width ratio, and feed line location.

The dipole development will be done in the following steps:

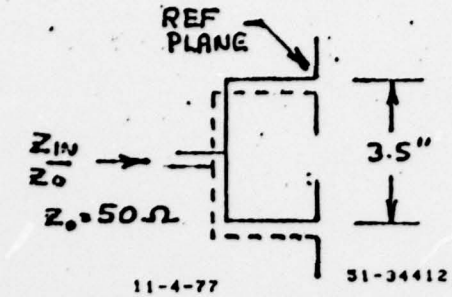
1) Preliminary dipole matching and pattern examination. This will provide a starting point design for the array matching by optimizing the dipole parameters: length and length/width, and testing feed line junction effects. It employs two dipoles fed from a balun and spaced greater than a wavelength apart oriented (coaxial) for minimum coupling. Effectively, this presents a single dipole impedance at the balun input. The patterns measured in this arrangement will show: single dipole H-plane pattern, two dipole interference E-plane pattern, and spurious radiation effects of the balun and feed lines.

   To date, a two dipole (1 X 2) breadboard (as described) has been fabricated and initially matched to a 1.40:1 VSWR. Figure 23 shows impedance data. A reasonable estimate indicates a balun dipole impedance of 1.20:1 maximum VSWR is feasible; however, final matching must be done in the array environment.

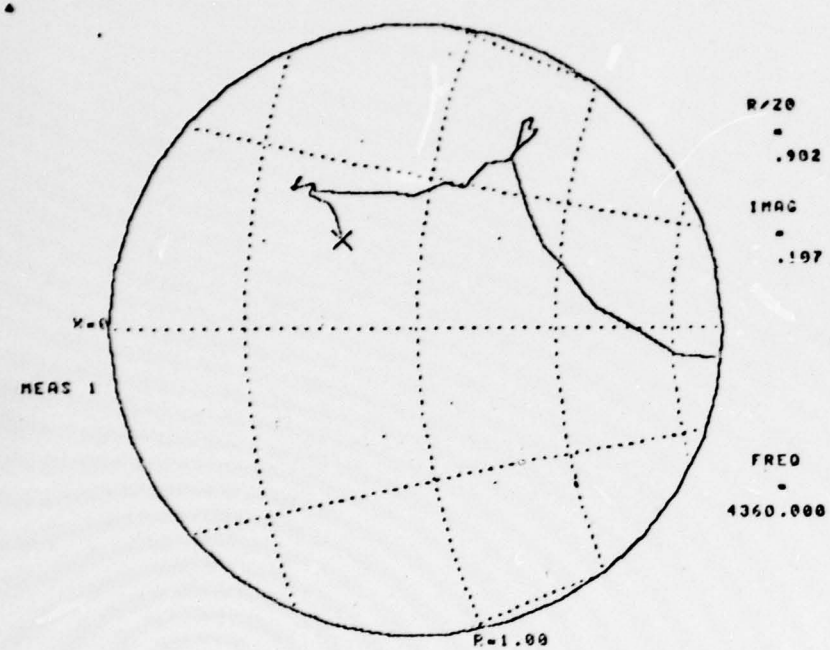
2) A 2 X 4 dipole array with each balun output feeding a 2 X 2 array of dipoles fed from a four-way divider and in a single polarization, was implemented as the next step in development of the dipole array. The need for this step

is to develop the four-way feed with dipole terminations including the most important mutual coupling and feed line effects. The goals will be to attain 1.2:1 maximum VSWR at the input to the four-way divider, and to attain pattern characteristics which show no anomalous effects: main lobe assymmetrics, spurious sidelobes, cross-polarization. To date, initial matching has resulted in the data of Figure 24A this includes the balun VSWR. Comparison to the 1 X 2 data of Figure 23 shows very similar performance indicating small mutual coupling effects and an optimum four-way divider design. Also, the single match point frequency response shows that additional tuning for a ripple response, i.e., three equal VSWR peaks at low, mid, and high frequencies, will reduce the maximum VSWR of 1.4 to 1.2 which is our design goal. A preliminary indication of loading effects of radomes or multi-layer assembly is shown in Figure 24B here a foam spacer and the 1 X 2 dipole PCB covered the 2 X 4 array all in direct contact. The resulting match of the 2 X 4 array is seen to have improved over Figure 24A however, though this is not the final arrangement, what is significant is that no excessive effects were noted. Additional matching and pattern measurements will be implemented in the next development phase.

3) The final step is the measurement of dipole impedance and patterns in a "large array" configuration, simulating the actual full size array environment. Applied here, this includes loading of the cross-polarization and polarization filter-type ground plane, inter-layer spacers and radome. The construction will consist of a stack of three laminates: two arrays cross polarized and one filter-ground plane, situated above a solid ground plane. Each array will contain an active central balun with each output feeding a pair of 2 X 2 dipole arrays (with four-way divider), as in step 2. Each polarization will thus be a 4 X 4 array of 16 dipoles with a corporate feed consisting of a balun, two-way power divider, and four-way power divider representative of every type component used in the full array. This stacked configuration has been tested and preliminary data indicates 1.55:1 VSWR and isolation between polarization of 28.5 dB worst case, typically 32 dB. Field testing of this arrangement is in process prior to final optimization of array design.



51-34412,J.RANGHELLI 11-4-77
PHASED ARRAY;PRELIM DIPOLE MEAS U/GPND
MAT-STRIP CO-AXIS DIPOLE PAIR;MOD BALUN
MOD:L=.875;NOTCH IN



51-34412,J.RANGHELLI 11-4-77
PHASED ARRAY;PRELIM DIPOLE MEAS U/GPND
MAT-STRIP CO-AXIS DIPOLE PAIR;MOD BALUN
MOD:L=.875,ORIG U

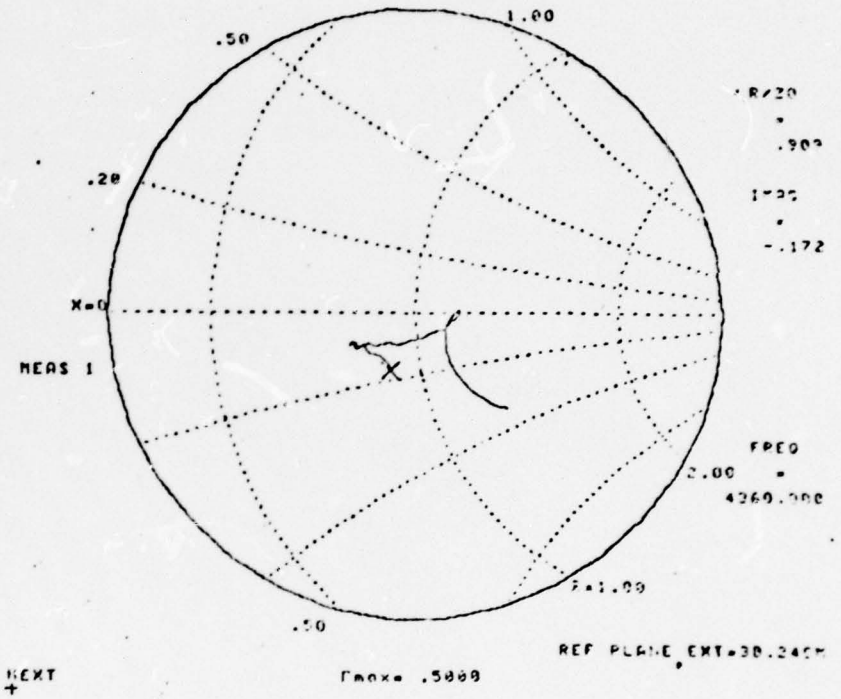


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FIGURE 23 : DIPOLE IMPEDANCE - MEASURED RESULTS

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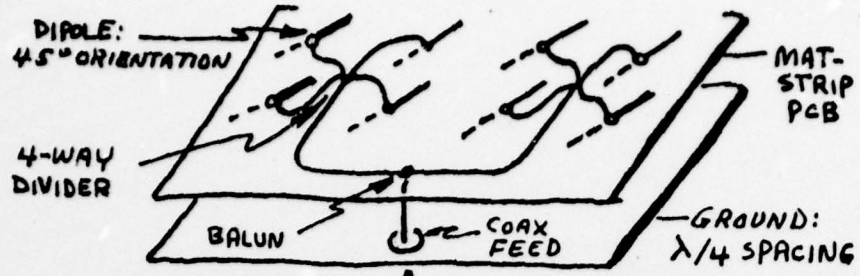

VSWR

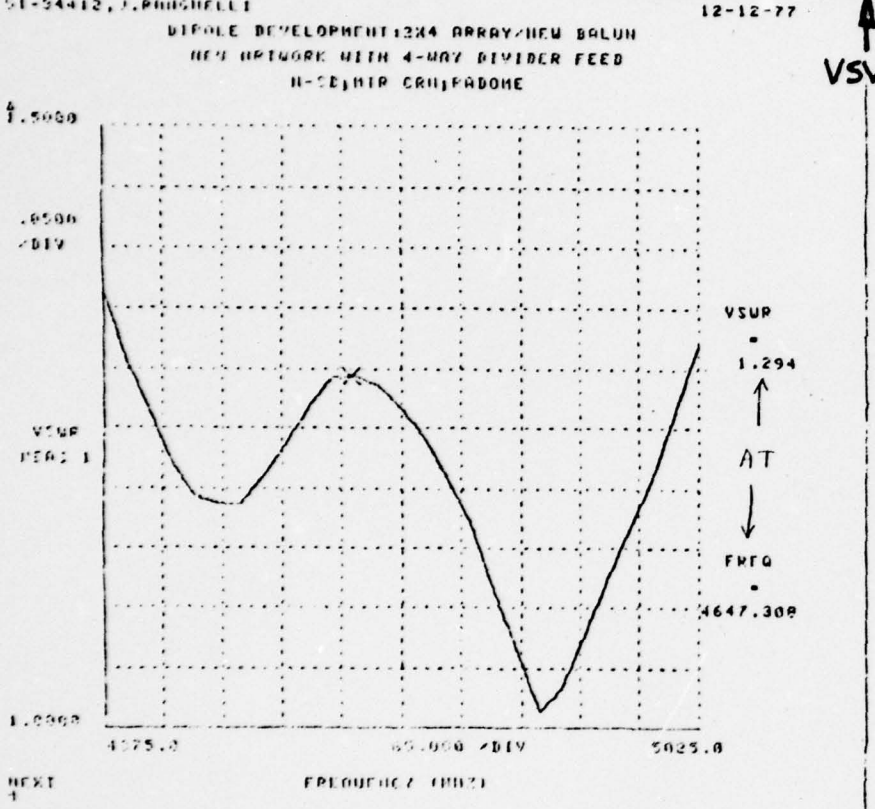

FIG. 24B : 2X4 DIPOLE ARRAY + RADOME

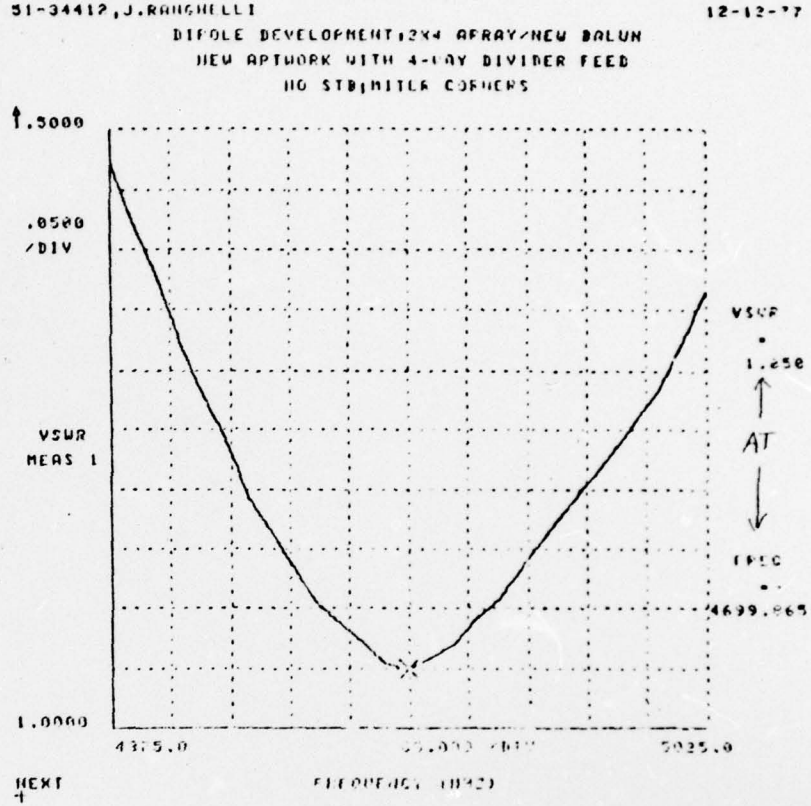

FIG. 24A : 2X4 DIPOLE ARRAY

NEXT REPORTING PERIOD ACTIVITY

During the next reporting period, January - June 1978, testing of the Antenna Array will be in progress and assembly of the BPM & IPA Driver Modules will be in progress. All material for system construction will be on order, and assembly at the Control Cabinet will be progressing.

The major technical accomplishments will be:

a. Matstrip (printed) Antenna performance

b. Construction/Test of the BPM, characterizing phase performance 'Turn on' slope, efficiency, full band width performance and total noise contribution.

From this information, the goals of the system will be reviewed and recommendations for device improvements to meet future system needs (IKW) defined.

CONCLUSIONS:

The analysis of the system requirements, coupled with the amplifier data available, indicates that implementation of a IKW system is dependent upon three crucial items:

a) AC-RF Efficiency
b) Reliability
c) Antenna Weight

Current transistor performance is the limiting element for these three items. Device efficiency, gain and power output are the parameters which must be improved before a IKW System is viable.

The AC-RF efficiency is crucial to enable system deployment with existing Army GRC-143 AC Generators.

Reliability is tied directly to device junction temperature and thus gain and efficiency.

Antenna weight is heavily dependent upon quantity of amplifiers and weight of heat sinks. Improvements in device power output and efficiency will reduce antenna weight such that antenna array erection on AN 1803 mast is possible.

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