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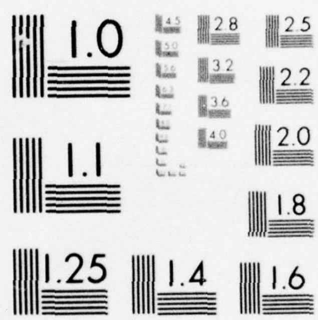

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A 10 kw LIGHTWEIGHT DC CONVERTER (TECHNOLOGY FEASIBILITY STUDY FOR LIGHTWEIGHT MEGAWATT RANGE CONVERTER

POWER ELECTRONICS ASSOCIATES, INC.
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This technical report has been reviewed and is approved for publication.

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Lightweight	Converter
Secondary Current Source	High Power Conditioner

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The technology for an ultra-reliable, lightweight, high power dc converter is presented and supported by test data of a small 10 kW feasibility model. Reliability and a high efficiency near 97 percent are derived from a process of natural current commuration of fast switching thyristors in series resonant circuits. Lightweight is the result of an internal frequency near 10 kHz. The feasibility of 150 kW single modules with one set of thyristors is indicated. The salient features of this converter technology are highlighted.

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FOREWARD

This final report was submitted by Power Electronics Associates, Inc., under contract number F33615-76-C-2050 in June 1977, and describes work performed during the period August 1975 to December 1976. This effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio, under Project 3145, Task number 314532, and Work Unit number 31453214 with Michael P. Dougherty, AFAPL/POD-1 as Project Engineer. Dr. Francisc Schwarz of Power Electronics Associates, Inc., was technically responsible for the work.

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SECTION I

INTRODUCTION

The purpose of this work was to investigate and experimentally demonstrate the feasibility of a reliably operating light weight converter to process kilowatts of electric power, and with the promise to operate in the megawatt range.

The system was studied as a voltage transforming and stabilizing dc to dc converter. Yet, its internal structure and mechanisms were to be suited for direct three phase ac to dc conversion without the use of a heavy low pass input filter.

The reliability of operation was to be demonstrated by the continued converter operation in the presence of severe disturbances, such as short circuited output terminals. This reliability should be also indicated by operation of the switching elements at a low and, unconditionally, predictable stress and thus a low heat dissipation level at the required switching frequencies.

The light weight of the system is rooted in the high internal frequency of 10 kHz at full power, since the weight of magnetics and filters is, roughly, inversly proportional to the frequency of converter operation for a given power level.

A 10 kW converter system was constructed. Its test verified the proposed functional concepts and the expected performance. An efficiency of the inverter which drives the high voltage transformer of up to 97 percent could be derived from the test data. The inverter was successfully integrated with the light weight 10 kW transformer-rectifier-filter for a dc output voltage of 10 kV and with an internal frequency of 10 kHz.

The system aspects of an ac or dc to dc converter and the therewith associated external characteristics are treated in section II. Special attention is given to potential ripple suppression in the currents of an ac generator and in the load using methods of active, nondissipative, filtering; the available mechanisms for potential systems stabilization are indicated.

The important frequency limiting phenomena, especially in switches, are treated in section III. The method used to overcome the now classical limitations of static power converters to below 1 kHz and to attain 10 kHz with existing components, is presented. The potential for use of yet higher frequencies is indicated. The method can be applied to any type of available and future fast switching elements, such as thyristors, transistors and vacuum spark gap switches.

The used power circuit and its characteristic features are presented in section IV. Design of the 10 kW converter is treated in section V, followed by the presentation of test results of the experimental model in section VI.

An analysis of the experimentally obtained results is contained in the conclusions of section VII. The results are related to the characteristics of the components which perform the individual converter functions and are used to project estimates of their usefulness in the construction of larger converter systems, as intended.

The above referred to analysis is based on a differentiated approach to power and energy densities of the major converter components reflecting the actual stresses which are being, intrinsically, imposed on the respective devices.

The road to the construction and demonstration of larger power units, such as 200 kW and beyond seems to have been cleared by the successful completion of the 10 kW system. Newly available GATT type thyristors appear to allow construction of up to 0.15 MW modules with one set of switches in one single bridge.

SECTION II

SYSTEM ASPECTS

The converter links the load to its dedicated source of electric energy. The converter's purpose is to

(a) transfer the electric energy to the load;

(b) transform the pattern of the voltage waveform of the source of electric energy, the generator, to another pattern as required by the load, such as a three phase ac to dc transformation;

(c) perform a voltage scaling function;

(d) stabilize the average load voltage so that it remain within preset limits of tolerance during conditions of steady state operation;

(e) limit the harmonic content that is "seen" by the generator and by the load, respectively, and which is caused by:

(e1) possibly, an inherent conflict between the intrinsic characteristics of generator and load, respectively, and the

(e2) internal functional mechanism of converter operation;

(f) facilitate over all system stability by reconciliation of conflicting dynamic characteristics of the source and the load;

(g) provide specified generator terminal conditions between cycles of operation, such as possibly a path for continued current flow, as required by certain sources of electric dc energy

The number of above enumerated functions which the converter has to perform will depend on the respective characteristics of the generator and on the load. This is discussed with reference to an example in which a three phase generator feeds a dc load.

1. AC to DC Conversion.

First, it is stated, that the polyphase generator technology produces a machine which is meant to generate sinusoidal ac voltage waveforms in its individual phases. These phases are meant to supply current of the same waveforms to the load, which if possible, should be in phase with the voltage, or at least, should not be lagging the voltage appreciably. The desired harmonic spectrum of the current i_s of the individual phases of the generator is shown in figure 1(a). The dc load requires, ideally, a harmonic content of its load

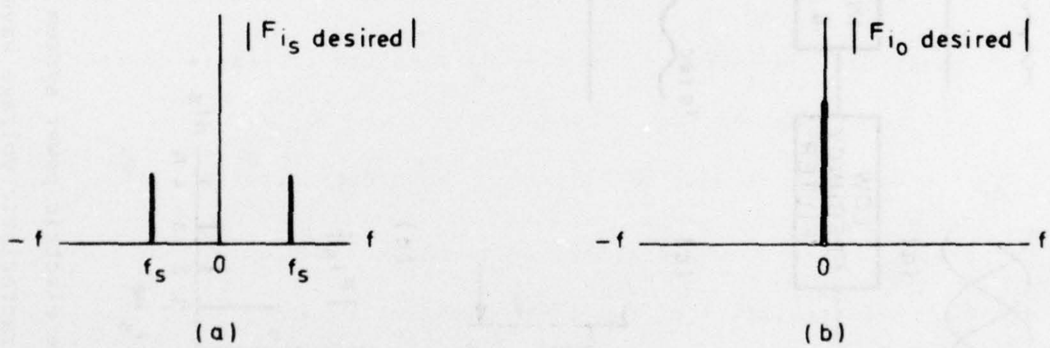


Figure 1.

Desired harmonic spectra of the current (a) i_s of each phase of a polyphase generator and (b) i_o of the dc load.

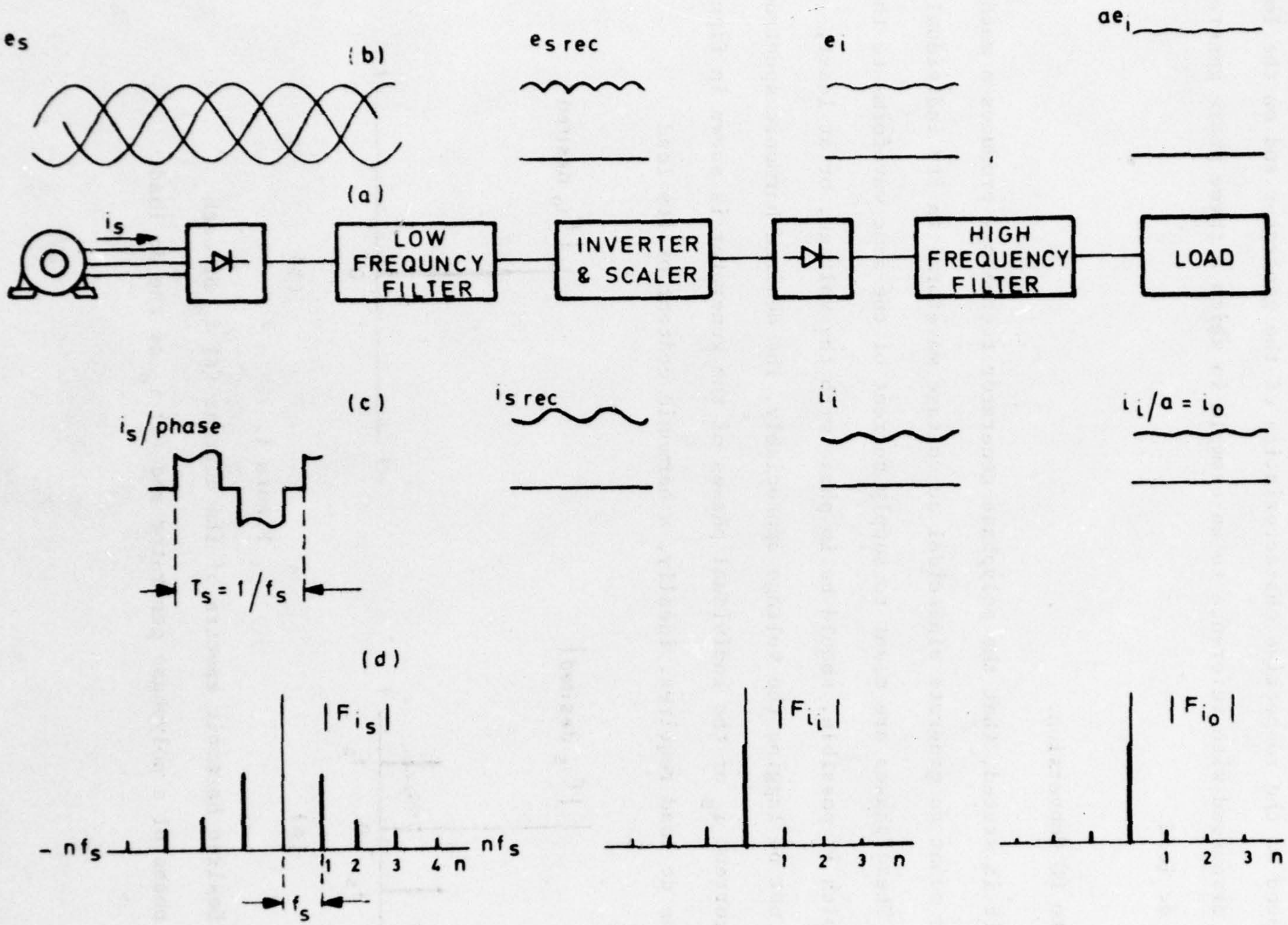


Figure 2

(a) Complete electric power system consisting of a three phase generator, (b) the characteristic voltage waveforms, (c) the characteristic current waveforms, (d) the frequency spectra of the current waveforms in (c).

current i_o with no other spectral line than that at f = 0, as shown in figure 1(b). The converter should thus transform the composite action of the individual waves of the generator phases to a smooth dc in accordance with its functions stated in (b). This above described functions of waveform transformation is independent of the voltage scaling function, as stated under (c) above. The various aspects which are characteristic for the chosen example are now discussed with reference to figure 2. The three phase generator, shown in figure 2(a), emits the well known three phase voltage waveforms e_s. shown in figure 2(b) which is transformed to its rectified waveform $e_{s\ rec}$, filtered to the form e_i and eventually scaled to the voltage ae_i. The letter "a" designates the scaling factor of a function which is performed within the inverter-scaler; this is the function cited in (c) above. The current waveform in each phase, the composite current i_{srec} of the rectified phases, its filtered form i_i and, eventually, its scaled form $i_i/a = I_o$ which is the load current are shown in figure 2(c). The frequency spectra of the current waveforms shown in figure 2(c) are indicated in figure 2(d) by $|F_{i_s}|$, $|F_{i_i}|$ and $|F_{i_o}|$ as functions of the order number n=1,2,..... of the spectral frequencies nf_s, where f_s is the single phase frequency of the three phase generator.

The classical function of the low frequency filter indicated as part of figure 2(c) is to "remove" the harmonic content of the voltage waveform $e_{s\ rec}$, so as to smooth the voltage e_i and the thereto pertaining current i_i, before inversion for the purpose of voltage scaling takes place. The high frequency filter removes only the harmonic content that has been generated by the process of inversion and rectification.

It means, that all of the reconciliatory functions between the desired spectra shown in figure 1(a) and (b) should be performed by the full wave rectifier bridge in conjunction with the therewith associated low frequency filter.

No known rectifier-filter can perform that function, even if weight and size were of no concern. The currently accepted "ideal" is a low pass filter with an infinitely large inductor L_i in its conventional L_iC_i configuration as indicated in figure 3. The infinitely large inductor L_i would cause a

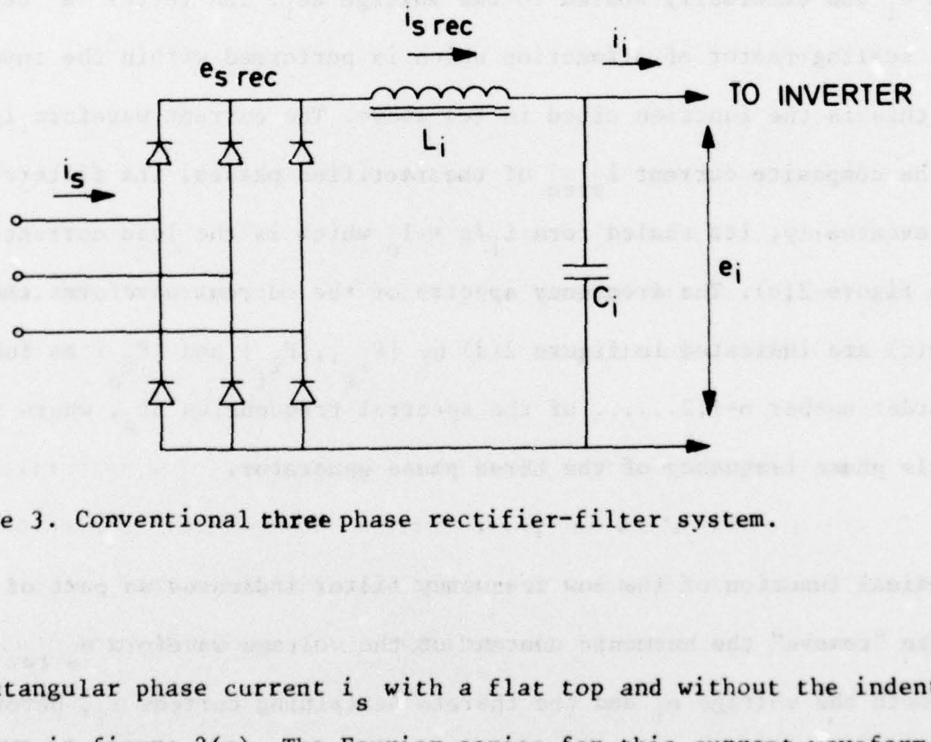


Figure 3. Conventional three phase rectifier-filter system.

rectangular phase current i_s with a flat top and without the indentation shown in figure 2(c). The Fourier series for this current waveform is given by

$$i_s(t) = (2\sqrt{3}\ I_{so}/\pi)\{\sin\omega_s t - \frac{1}{5}\sin 5\omega s_t + \frac{1}{7}\sin 7\omega_s t - \ldots\ldots\} \qquad (1)$$

where I_{so} is given by

$$I_{so} = P_o/\eta_s e_{sp}\sqrt{6} \tag{2}$$

and

P_o = the intended output power of the system;

η_s = the over all efficiency of the electric power system, except that of the generator;

e_{sp} = the rms voltage of the individual phases of the ac generator.

The "infinitely large" inductor will guarantee a smooth current $i_{s\,rec}$ and result in an equally smooth form of the load current i_o. Yet, it creates the harmonic content of the current in the individual phases of the generator which are quantified in equation (1).

If on the other hand there were a rectifier-low-frequency-low-pass-filter combination which would allow the phase currents i_s to remain sinusoidal then the generator would get its desired current waveform and a near infinite filter capacitor C_i could smooth the voltage e_i, as desired by the load.

It was the purpose of the preceding argument to show that no known rectifier filter combination could satisfy the requirements that were stated with reference to figure 1, even if infinitely large filter components could be afforded.

The low pass filters of the reality of technology consist of components of the minimum acceptable size. The inductors are, usually, sufficiently large to provide a continuous current $i_{s\ rec}$ so that the current in one diode pair of the full wave bridge rectifier as shown in figure 3 would not be interrupted and reinitiated during a work cycle of that diode pair. The purpose of this restriction is to avoid current peaking in the diodes in the filter capacitor and, possibly, in the generator, all of which would contribute to undue instantanuous stresses on components and to their heating.

The needed kVA rating of the dedicated generator can be estimated from the relation

$$kVA_{required} = \frac{P_o}{\eta_s\,(p.f.)} \tag{3}$$

where

$$p.f. = \frac{\frac{1}{T}\int_0^T e_s i_s\,dt}{e_{s\ rms}\, i_{s\ rms}}$$, being the power factor, as defined in the time domain [1], and where

$$i_{s\ rms} = \left(\frac{1}{T}\int_0^T i_s^2(t)dt\right)^{\frac{1}{2}}$$

so that i_s can be any function of time and need not be considered as being the composite of its Fourier components.

The power factor p.f. of a rectifier-filter with an "infinitely" large inductor is approximately .955. Yet, this power factor decreases rapidly with the decreasing size of L_i. Power factors of 0.7 and less are, therefore, commonplace in these type of systems and are the cause for use of a commensurately larger generator.

The converter which operates from an input voltage e_i can be equipped with the property of a nondissipative type active filter which would remove the low frequency content of e_i. This converter can thus reduce the burden that is, otherwise, imposed on the low pass input filter. This can be restated in the following way: If

$$e_i \simeq e_{i\,av} \{1 + m \sin 6\, \omega_s t\} \qquad m << 1 \tag{4}$$

then the maximum possible attenuations a_d of the normalized ripple amplitude m and caused by this active filters is approximated by

$$a_d \simeq (f_F/6f_s)/\pi \tag{5}$$

for the given conditions [2], where

$f_F = 2f_i$

f_i = the average frequency of inverter operation.

The total attenuation of the peak to peak ripple of, approximately, 11 percent of the rectified waveform $e_{s\,rec}$ is given by

$$100\, v_{orpp}/v_{o\,av} \simeq 11/a_{pi}\, a_d \qquad (6)$$

where

v_{orpp} = the peak to peak ripple of the output voltage

$v_{o\,av}$ = the average value of the output voltage

a_{pi} = the attenuation of the passive input filter as shown in figure 3.

The two attenuation factors a_{pi} and a_d are considered to be independent of each other because it concerns the attenuation of a passive network followed by the effect of a pulse modulation process, by way of approximation.

The pulse modulation process which is incorporated in the converter operation [2] serves the dual purpose: (1) to stabilize the output voltage by performing pulse width (PW), pulse frequency (PF) or mixed PW-PF modulation (PW-PFM) to contribute to the attenuation of the low frequency ripple contained in

$e_{s\ rec}$ and (3) to, possibly, contribute to the dynamic stability of the over all electric power system by performing the appropriate variations of this process of pulse modulation, as needed. The physical structure of the power circuit and its intrinsic mode of operation, preserve the functional integrity of the system as a whole independent of externally imposed adverse conditions. The above discussed example illustrates the functions (a) through (g) of the converter as stated as the outset of this section.

Means to attempt a reconciliation of the inherent conflict between an ac generator and a dc load are currently being investigated [3]. The discussion of these means is beyond the scope of this treatise.

2.2 DC to DC Conversion.

In this case power is derived from a dc source, as shown in figure 4. All properties, required of a converter and listed in (a) through (g) at the outset of this section apply, except (b), which does not apply in this case, since dc is converted to dc, even though the voltage of the source of electric energy may vary and, possibly, oscillate in a damped or undamped manner.

The functions of the converter which include output voltage scaling and stabilization could be extended to include maximum power point tracking of the source and if required, dynamic stabilization of the system as a whole. There is no other function in the power system which lends itself as suitably for the purpose of system stabilization as the application of a control signal

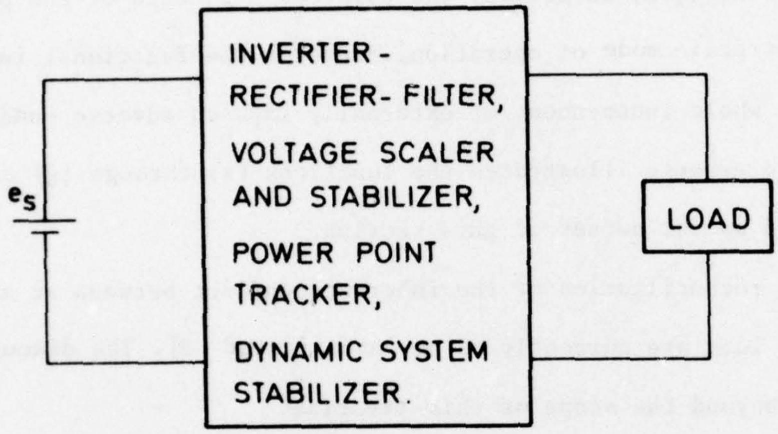


Figure 4. DC converter system in block diagram form.

to a very high impedance electronic mechanism which controls the rate and the rate of change of transfer of energy. It controls, namely, the pulse modulation process which in turns governs the power system behavior as a whole. The functional mechanism of any dc to dc converter, for brevity referred to as dc converter, is described with reference to figures 5(a) and (b). The current i_s of the dc source of electric energy with the voltage e_s passes through a high frequency (H.F.) input filter on its way to the inverter and pulse modulator. This inverter consists of a set of switches and other thereto pertaining nondissipative elements such as inductors and capacitors. The inverter generates a high frequency (kHz) carrier current i_1 as shown in figure 5(b). This carrier

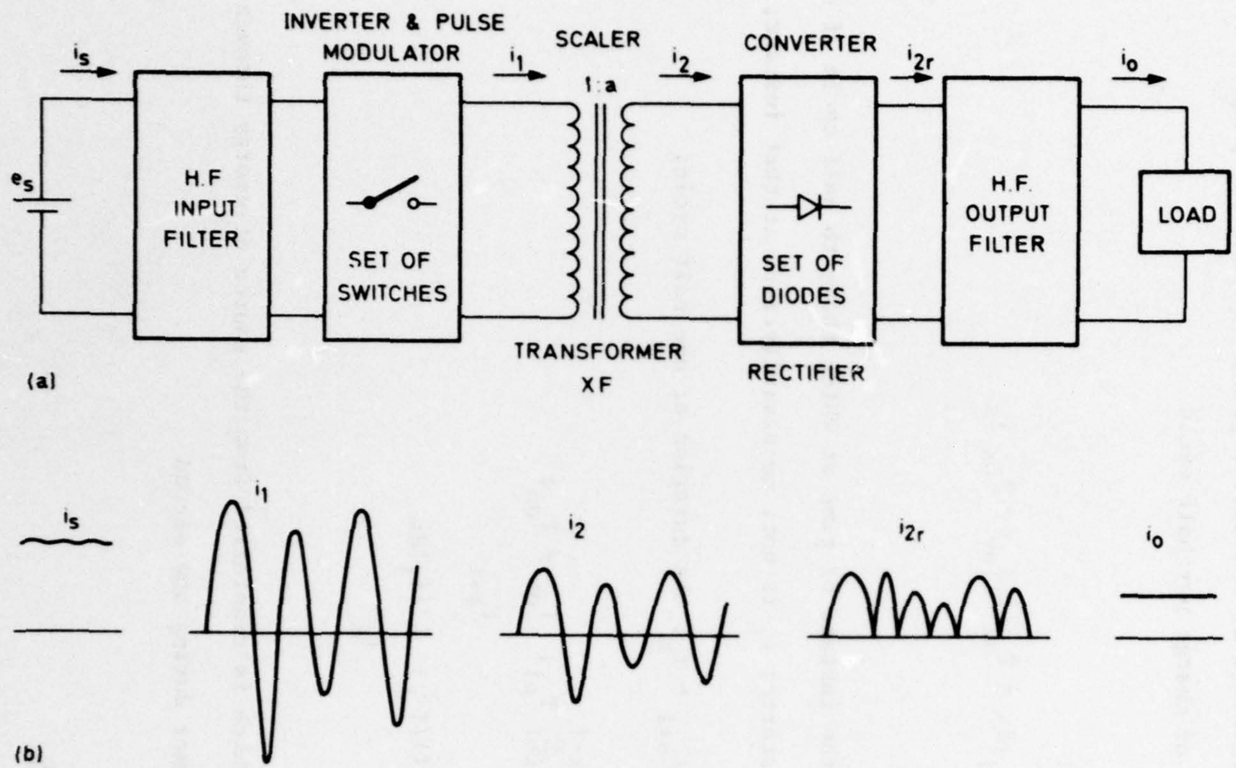


Figure 5. DC converter: (a) functional block diagram, (b) current waveforms.

current is being modulated in frequency and in amplitude, while it is being generated. The referred to modulation process serves the purpose of control of the transfer of charge per half cycle

$$A_k = \int_{t_k}^{t_{k+1}} |i_1| dt = T_{ok} |i_1|_{av} = T_{ok}\ i_s \tag{7}$$

where:

t_k = the instant of time at which the k-th half cycle of operation starts; i_1 is not, necessarily, zero at that instant;

T_{ok} = $t_{k+1} - t_k$, the duration of one half cycle;

t_k = $\sum_{i=1}^{k-1} T_{oi}$; $T_{om} \neq T_{on}$;

$|i_1|_{av}$ = $(1/T_{ok}) \int_{t_k}^{t_{k+1}} |i_1| dt$

The charge A_s which is tranferred from the source of energy through the inverter to the transformer during one second

$$A_s = \sum_{k=1}^{F} A_k \tag{8}$$

where

F = the number of half cycles with duration T_{ok} per second, even through $T_{om} \neq T_{on}$

The magnitude of the average current $i_{s\ av}$ during the second in which all A_k of equation (7) are being summered up,

$$|i_{s\ av}| = |A_s| \tag{9}$$

The "absolute magnitude" signs in equation (9) are meant to emphasize that Amperes are being equated to Coulombs per second which is, dimensionally, correct.

The carrier current i_1 is processed by the high frequency transformer XF with a voltage step-up ratio 1:a which performs the function of a scaler. The secondary transformer circuit includes the rectifier which consists of a set of diodes in form of a diode bridge. This bridge converts the scaled current

$$i_2 = i_1/a \tag{10}$$

to its rectified form i_{2r}. The high frequency (H.F.) output filter removes the harmonic content at double the average inverter frequency and beyond. Thus

$$f_F = 2f_i \tag{11}$$

where

f_i = the average inverter frequency;

f_F = the pulse repetition rate F as defined with reference to equation (8)

The input filter and the output filters of the converter perform an analogous function: they isolate the high frequency operation of the dc converter from the low frequency characteristic of the source and of the load. In that sense, they provide short circuit paths for the high frequency components which are being generated by the internal functional mechanism of the converter.

The listing of the converter's functions which were enumerated at the outset of this section is now repeated and identified in terms of the preceding discussion of figure 5:

(a) the converter, clearly, transfers the electric energy from the source to the load;

(b) not applicable for a dc to dc conversion;

(c) voltage scaling is performed by the transformer XF;

(d) the average load voltage is stabilized by letting the electric charge per cycle;

$$A_k/T_{ok} = \text{constant}; \tag{12}$$

if a constant Z_L is assumed, even though e_s may vary during every pulse interval T_{ok};

(e1) modify relation (12), if so desired, to shift part or all of the burden of the harmonic content which is generated by variations of e_s to the source, or to the load according to a preset pattern; yet, let A_s as defined in (8) be a constant;

(e2) remove the harmonic content at the average frequency f_F and beyond by use of the input and the output filters;

(f) contribute to the dynamic stability of the electric power system by introduction of appropriate effects of the current carrier modulation process;

(g) not treated in this section.

The purpose of high internal frequencies is the reduction of the physical sizes of

(1) the transformer XF;

(2) the input and the output filters;

(3) all reactive components which are needed for the inversion and for the pulse modulation processes.

The physical weight of the above named power components is, roughly, proportional with the inverse of the frequency f_i of the inverter operation, everything else being equal. A figure of merit FM can be formulated in an attempt to quantify the significant aspects of this causal relationship between the physical weight W_p and some of the other conditions.
The figure of merit

$$FM = \frac{P_o f_i}{W_p (1-\eta_s) f_s} \quad . \tag{13}$$

All symbols, used in equation (13) have been defined before. This figure of merit modifies the more commonly used power density P_o/W_p, expressed in kW/kg by *introduction of the relative power loss* $(1-\eta_s)$ and by the frequency ratio f_i/f_s. It is observed that if for a change of the inverter frequency f_i from f_{i1} to f_{i2} and of the corresponding physical weight from W_{p1} to W_{p2}

$$(W_{p1}-W_{p2})/W_{p1} \simeq (f_{i2}-f_{i1})/f_{i1} \tag{14}$$

then the figure of merit will not change substantially if

$$W_{p2} \simeq (f_{i1}/f_{i2})\, W_{p1} \quad . \tag{15}$$

Relation (15) is meant to express only a gross approximation.

The same figure of merit can be applied to any of the individual passive components of the converter system, especially to the transformer XF, the filter components, and other reactive components.

The quest for increasingly higher frequencies of operation is an obvious result of the desire to reduce the physical weight of power equipment, especially in the case of air or space born equipment.

A number of phenomena which can cause an increase of power losses and in doing so imperil the integrity of the functional mechanism of converters, tend to limit the upper limits of internal frequencies of converter operation. These are treated in the following section III.

SECTION III

FREQUENCY LIMITING PHENOMENA

Skin and proximity effects in conductive elements, parasitic effects associated with the individual components, and the physical limits of functional concepts supply most of the frequency limiting phenomena.

The presence of skin and proximity effects in magnetic components and capacitors requires the careful application of design techniques which are well known from the areas of radio and radar engineering. The significant frequency ranges which are being encountered are:

(a) the low frequency region of conventional and advanced electrical power engineering, say, from zero to near 1 kHz;

(b) the intermediate region of internal frequencies of advanced dc converter technology, from 10 to 50 kHz;

(c) the high frequency region caused by the switching phenomena in power semiconductors within fractions of microseconds, which cause appreciable frequency components in the order of MHz.

Sizable energies are involved in all of these frequency ranges. The significance of the effects of abrupt switching in power circuits is discussed with reference to figure 6.

Opening of switch S_f in the circuit shown in figure 6(a) causes the forcible interruption of the current i_f flowing through inductor L The magnetic field which is maintained in the inductor L and is caused by the current i_f before its interruption cannot be sustained without this current. The magnetic energy ε_m which is associated with this field can,likewise, not vanish and tends to be reconverted to electric energy ε_e.

This energy reconversion process from ε_m to ε_e seeks to maintain current flow through the opening switch S_f. A mechanical switch will arc under

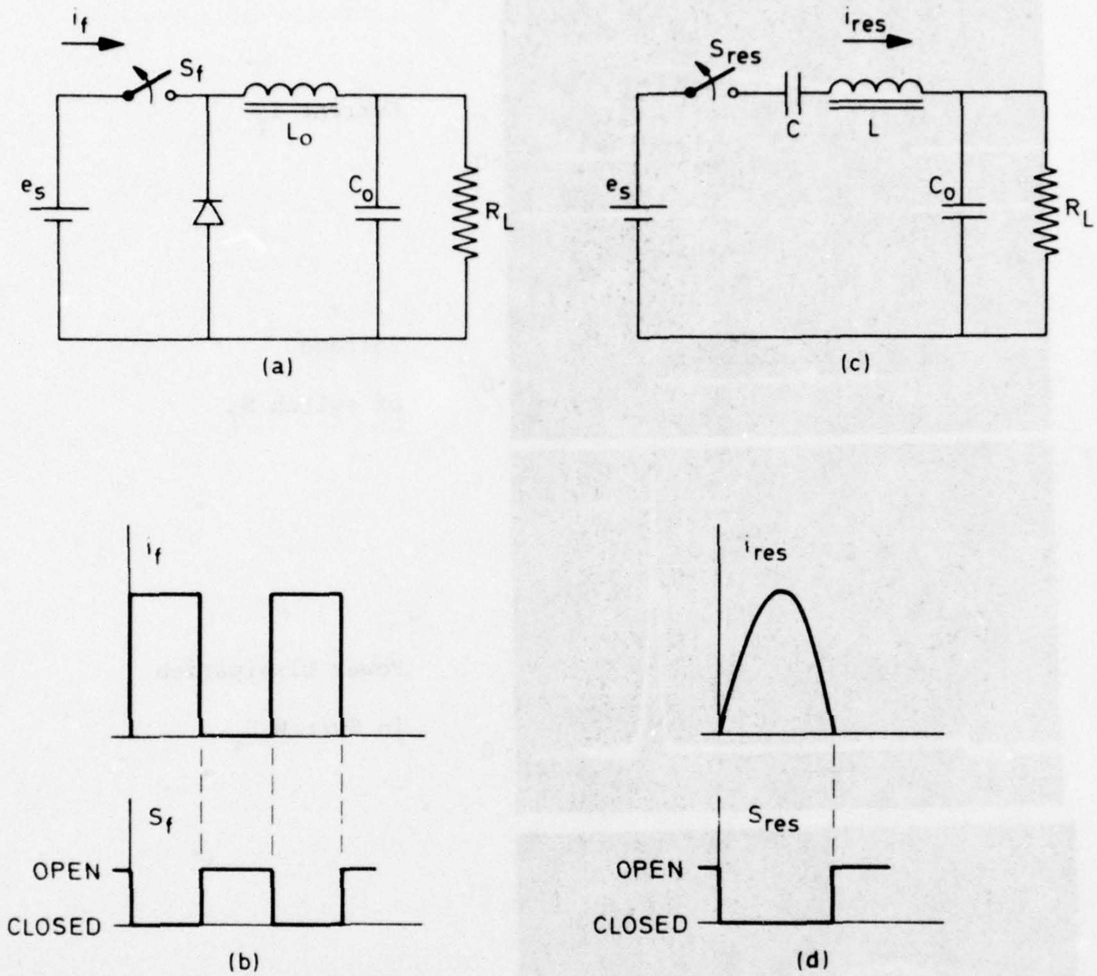


Figure 6. Power electronic switching circuits which incorporate intended and parasitic inductive elements in series with the switching elements for (a) forced interruption of the switched current, (b) the thereto pertaining current form i_s in the switch S_f and (c) switching at the instant of natural termination of the switch current i_{res} in a resonant circuit, (d) the thereto pertaining current form i_{res} in the switch S_{res}.

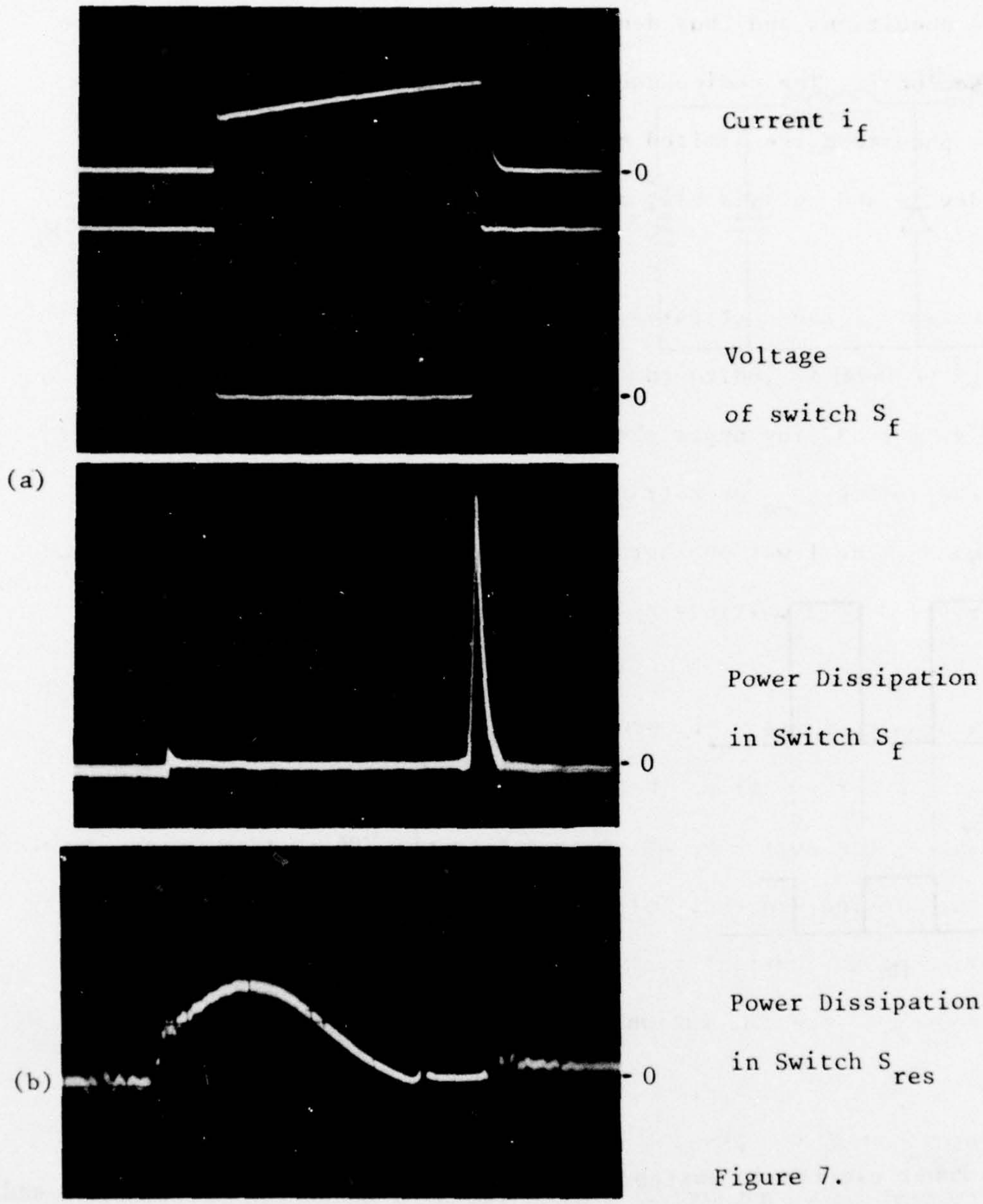


Figure 7.

Oscilloscope trace of: (a) current voltage and power dissipation waveforms of a switching transistor operating under conditions of forced current interruption as discussed with reference to figures 6(a) and (b); (c) the power dissipation of a switching transistor which processes a resonant current as described with reference to figures 6(c) and (d).

these conditions and thus demonstrate visibly the stresses that are imposed on it. The semiconductor switch undergoes similar stresses whose phenomena are limited to the concerned lattice structure of the device and not visible, but not less severe.

The extent of these stresses as translated into conversion of electric energy to heat is indicated by the photographs of curve traces shown in figure 7(a). The upper photograph of this figure shows current i_f and the voltage v_{ce} of a transistor which performs the function of switch S_f. The lower photograph in figure 7(a) shows the $v_{ec}\ i_f$ product as provided by a multiplying (Philips) oscilloscope.

It is seen that the $v_{ce} i_f$ product has a moderate value for conditions of settled current flow. There is a narrow peak at the instant of closing of the switch S_f which is due to the finite time which is needed for the closing process. Falling of the voltage v_{ce} across the switch and rise of the current i_f is the cause for this narrow peak of the v_{ce} i_f product at the initiation of the current pulse.

The area under the peak of the $v_{ce}\ i_f$ product at the termination of the current pulse appears to exceed the area under the remainder of the $v_{ce}\ i_f$ curve for this current pulse. It is obvious that most of the heat dissipations in the switch is not caused by the process of conduction, but by the processes of current termination. The power loss in the switch

$$P_d = v_{cess}\ i_{fss}\ (T_k/T_{ok}) + f_F\ (\varepsilon_s + \varepsilon_T) \tag{16}$$

where

v_{cess} = the voltage drop over the conducting transistor under conditions of settled current flow;

i_{fss} = the transistor current under the same conditions;

T_k = the pulse width;

ε_s = the energy dissipation caused by the turn on process;

ε_T = the energy dissipation during the opening phase of the switch.

Equation (16) demonstrates the frequency dependence of the switching losses. Each switching device is limited in its capability to dissipate heat. This limitation imposes one ceiling on the repetition rate f_F with which it can switch a current i_f.

Another, more subtle limitation on the tolerance of the $v_{ce}\ i_f$ peak is imposed by the internal distribution of current density within the lattice of the semiconductor device. This internal distribution of current density can exceed the heat tolerance of the material on that spot and can thus cause damage to the device. This damage increases rather sooner than later and can cause a break down of the device, often referred to as "secondary" break down.

The above described phenomena are the primary cause for limitation of the internal frequency of operation of power converters. This limitation increases with the increasing magnitude of currents that are being processed by the switching elements [4].

The preceeding description of the difficulties of the opening of switches in inductive circuits does not reveal a new phenomenon, but reiterates a well known process. The argument is not limited to semiconductor switches but remains valid for any type of switches, whether they are mechanical in structure, gas filled or vacuum tubes with spark gap ignition.

The current i_{res} in the circuit shown in figure 6(c) assumes a sinusoidal form when switch S_{res} closes at the instant of time t=0 and if $i_{res}(0)=0$, as indicated in figure 6(d). It is assumed that the initial conditions on capacitors C and C_o and on the inductor L are appropriate for that purpose. The current i_{res} rises with a limited di_{res}/dt at the time where the switch S_{res} is closed This di/dt is determined by

$$di_{res}/dt = (e_s - v_{co} - v_c)/L \quad \text{at } t=0 \tag{17}$$

where

v_{co} = the voltage on capacitor C_o at t=0;

v_c = the voltage on capacitor C at t=0

Likewise is

$$di_{res}/dt(T_o) \simeq - di_{res}/dt(0) \qquad (18)$$

if

$$T_o = \pi\sqrt{LC}$$

and if the bulk of the electric energy, present in the circuit is not removed during the time interval T_o. The switch closes at time t=0 and does not commutate a (diode) current of appreciable magnitude as could be the case in the circuit shown in figure 6(a). The $v_{ce} i_{res}$ product in the switching element associated with the circuit of figure 6(c) near the time t=0 is, therefore, minute compared to the one described with reference to the circuit shown in figure 6(a).

Yet, the real problem could arise at the time $t=T_o$ when the switch S_{res} is opened. The resonant current

$$i_{res}(T_o) = 0 \qquad \text{when } t = T_o \tag{19}$$

as indicated in figure 6(d).

The $v_{ce}\ i_{res}$ product is there, necessarily zero at that time. This fact is verified by the photograph of the $v_{ce}\ i_{res}$ curve trace, shown in figure 7(b). A larger amplification of the $v_{ce}\ i_{res}$ product was used this time because of the absence of the substantial spike which appears in figure 7(a). The effect of the sinusoidal current on the shape of the power dissipation curve in figure 7(b) is clearly discernible. The small spikes which resemble electric noise at the termination of the pulse are comparable to the maximum magnitude of the $v_{ce}\ i_{res}$ product. The area under these spikes can be termed minute compared to the area under the dissipation curve under conditions of settled current flow.

It appears that the opening of a switch in an inductive circuit at a time when the switch current is zero, has the advantage of minimum power dissipation during the opening process of the switch. The preceeding statement is nothing else, but the reiteration of a fact that has been well known from the early days of electric science. The disappearence of the substantial dissipation spike shown in figure 7(a), removes the frequency dependent part from equation (16) for all practical purposes. The power loss in the switching elements becomes thus, practically, independent of the internal converter frequency (4), (5). The above explained advantage of the use of series resonant circuits for purpose of converter operation was used for the technical approach for development of a converter technology which would tolerate relatively high internal frequencies.

SECTION IV

THE DC CONVERTER WITH SERIES RESONANT CIRCUITS

A dc converter system was chosen which utilizes a modulated current carrier as discussed above for purpose of controlled power transfer and combines this function with the advantage of switch operation in resonant circuits.

1. The Power Circuit

The essential features of the power circuit of a dc converter which employs series resonant circuits are shown in figure 8. The shown simplified schematic illustrates the above referred to type of dc converter in its half bridge configuration. Two switch pairs consisting of one thyristor CR1i and an anti-parallel diode D1i (i = 1,2) are used to close and open in alternating succession two series resonant circuits. Each of these two circuits connects to the junction of capacitors C11 and C12, and includes the inductor L_1, the primary

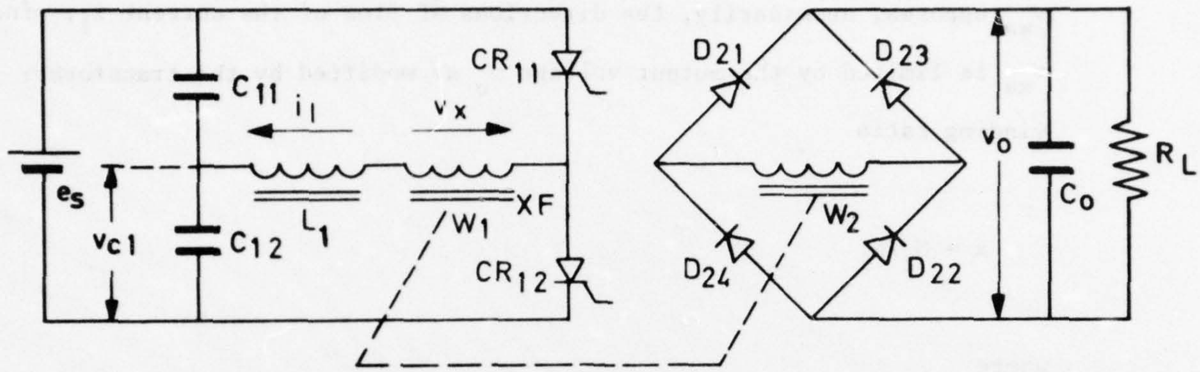


Figure 8. Simplified schematic of a dc converter which employs a series resonant circuit.

winding W_1 of the transformer XF, and one of the above identified switch pairs. The first switch pair CR11-D11 connects the described circuit to the possitive terminal of the source of electric energy with voltage e_s; the second switch pair CR12-D12 connects the same circuit to the negative terminal of the same source.

The output voltage v_o of the converter is assumed to be of constant magnitude at this time. The secondary winding W_2 of the transformer XF switches abruptly within the rectifier bridge consisting of diodes D2j (j = 1,2,3,4). This transformer reflects a voltage v_{xa} back into the primary circuit which always apposes the directions of flow of the resonant current i_1. The polarity of this voltage v_{xa} opposes, necessarily, the directions of flow of the current i_1, since v_{xa} is limited by the output voltage v_o as modified by the transformer winding ratio

$$a = N_2/N_1 \tag{20}$$

where

N_i = the number of turns in winding W_i of transformer XF.

The above stated limitation that

$$|v_{xa}| = v_o/a \tag{21}$$

is due to the fact that the voltage on the secondary winding W_2 of transformer XF rises under the impact of the voltage that is impressed on the primary winding of the same transformer until it is, forcibly, limited by the secondary diode bridge to the voltage v_o of capacitor C_o. The size of this capacitor as reflected into the primary circuit, namely

$$a^2 C_o = C_2 >> C_1 = C11 + C12 \cdot \tag{22}$$

Capacitors C_1 and C_o are so dimensioned that the voltage v_o over C_o will

$$v_{orpp\ max} < 2e_s \frac{C_1/a}{C_o} \qquad (23)$$

Inequality (23) follows from the application of the simple rule that

$$\Delta Q = (C_1/a^2)\ 2ae_s = C_o\ v_{orpp} \qquad (24)$$

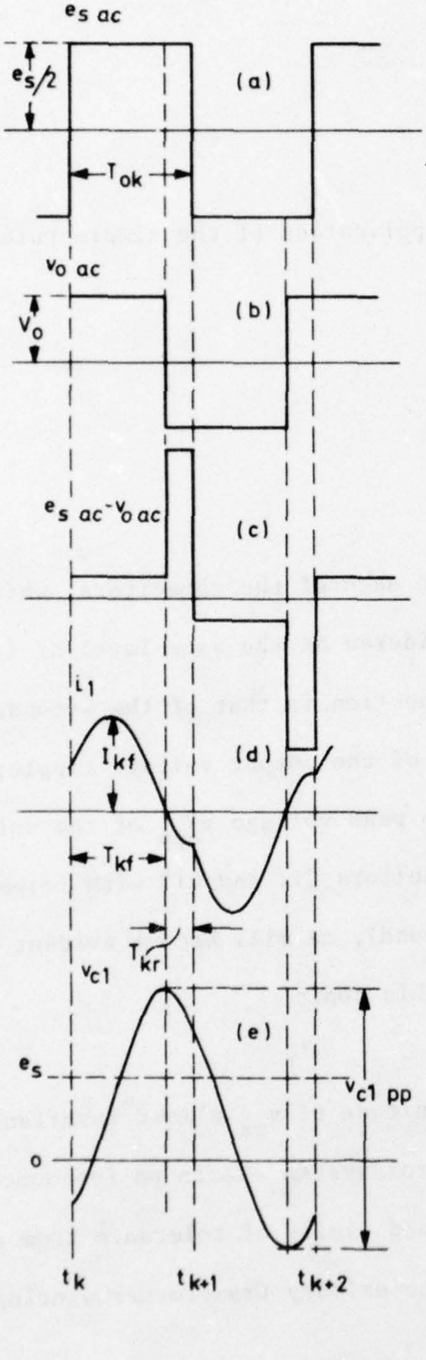
where

ΔQ = the change in charge in each of the capacitors, which is equal if they are considered at the same level of impedance which, in the case in question, is that of the secondary circuit;

v_{orpp} = the peak to peak value of the output voltage ripple;

$2e_s$ = the approximate peak to peak voltage v_{cpp} of the voltage v_{cl} of the junction of capacitors C11 and C12 with respect to the reference node (ground), as will become evident from the further discussion of this topic.

The inequality (22) renders the magnitude of v_{xa} almost invariant with the tacit understanding that a control system exerts an influence on i_2 so that v_o remain within prescribed limits of tolerance from a nominal value V_o. The voltage v_x on the primary transformer winding W1



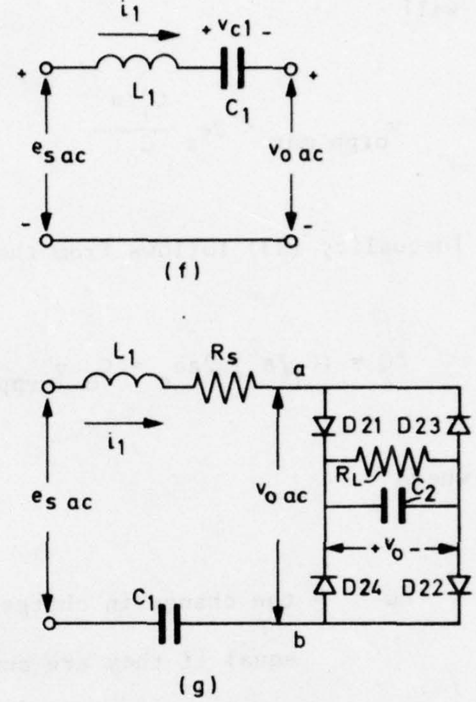


Figure 9.

(a) Equivalent source voltage e_{sac}; (b) equivalent load voltage v_{oac}; (c) net excitation voltage $e_{sac} - v_{oac}$ of resonant circuit; (d) resonant current i_1; (e) capacitor voltage v_{c1}; (f) double excited L_1C_1 circuit; (g) equivalent circuit of series capacitor inverter-converter.

presents itself then as a square wave with amplitude v_{xa} as given by equation (21) and a frequency which is dictated by the pattern of operation of the switches CR11-D11 and CR12-D12.

The operation and the philosophy of the power circuit shown in figure 8 is briefly explained with reference to figure 9.

The series resonant circuit consisting of inductor L_1 and the (Thevenin) equivalent capacitors $C_1 = C_{11}+C_{12}$ is indicated in figure 9(f). This resonant circuit is driven on one port by a square wave $e_{s\ ac}$ with amplitude $e_s/2$ and on the other port by a square wave $v_{o\ ac}$ with amplitude v_o. These square waves are indicated in figures 9(a) and (b) respectively. The amplitude $e_s/2$ stems from the fact that the resonant elements of the circuit in figure 8 "see" Thevenins equivalent of e_s when "looking" into the junction of capacitors C_{11} and C_{12} toward the source. This equivalent source has the voltage $e_s/2$ if $C_{11} = C_{12}$. The square wave $e_{s\ ac}$ is generated by connecting the resonant circuit with inclusion of the transformer XF in continuing succession and abruptly to the positive terminal of the source with voltage e_s, thus creating a potential $e_s - e_s/2$, or to the negative terminal of the same source and creating a potential $0 - e_s/2$. The negative voltage $-_{es}/2$ is defined with respect to the same terminals of the LC circuit as the possitive voltage $+e_s/2$ was defined for the positive amplitude of $e_{s\ ac}$.

The cause of the voltage $v_{c\ ac}$ which appears on the terminals of the primary winding W_1 of the transformers XF was explained above in the context of circuit operations with respect to figure 8. The winding ratio N_2/N_2 is here assumed to be unity so that for the sake of simplicity $v_{xa} = v_o$, with the tacit assumption that all components are ideal.

Square waves $e_{s\ ac}$ and $v_{o\ ac}$ have the same frequency under conditions of cyclic stability, yet they differ by a "phase shift" which amounts to a "phase angle" $\psi_{rk} = \omega_o T_{kr}$ as indicated in figures 9(a) through (e). Under the assumed conditions of cyclic stability is $\psi_{rk} = \psi_{rk+1}$.

The net driving voltage of the resonant circuit $e_{s\ ac} - v_{o\ ac}$ is indicated in figure 9(c). The ensuing resonant current i_l is indicated in figure 9(d). Finally the capacitor voltage v_{c1} which was defined before is depicted in figure 9(e).

Slope and magnitude of the resonant current i_1 can be derived immediatly from the net driving voltage $e_{s\ ac} - v_{o\ ac}$. Under conditions of cyclic stability the energy exchange ε_{sk} between the two equivalent sources and the resonant circuit must be zero over each closed cycle of operation, or half cycle of the resonant current. It means that

$$\varepsilon_{sk} = \int_{t_k}^{t_{k+1}} (e_{s\ ac} - v_{o\ ac}) i_1 \, dt = 0 \qquad (25)$$

The transfer of energy from the source to the load is controlled by adjusting the "phase angle" ψ_{rk} which is predominantly governed by the natural half period of the resonant circuit T_o and by the externally controlled instant of time t_k at which the appropriate thyristor is being energized.

The current i_1 is conducted by thyristor CR11 during the time interval T_{kf} as indicated in figure 9(d). The capacitor voltage v_{c1} reaches its crest when $i_1 = 0$ at the end of the above referred to time interval T_{kf}. The net voltage $e_{s\,ac} - v_{o\,ac}$ then apposes the flow of current through the diode D11 and energy is being returned from the resonant circuit to its driving "sources". This return of energy increases with increasing phase angle ψ_{rk} and this in turn requires that the energy which is accepted during the interval T_{kf} decrease for unchanged $e_s/2$ and v_o. Decrease of the energy accepted by the resonant circuit in this time interval requires, thus a decrease of the amplitude of i_1. The "phase angle" ψ_{rk} thus controls the amplitude of i_1 and by implication the average $|i_1|_{av}$ of the absolute value of i_1 which is being transferred to the load.

Another way to describe this control process of i_1 is to state that the amplitude of i_1 and the average of its absolute value

$$|i_1|_{av} \text{ increases for } T_{ok} \rightarrow T_o, \text{ or } \psi_r \rightarrow 0 \qquad (26)$$

and

$$|i_1|_{av} \text{ decreases for } T_{ok} \to 2T_o \text{, or } \psi_{rk} \to \pi \qquad (27)$$

It means that

$$|i_1|_{av} \to \infty \qquad (28)$$

if the inverter frequency of operation

$$f_{io} = 1/(T_{ok} + T_{ok+1}) \to f_o = 1/2T_o = 1/2\pi\sqrt{L_1C_1} \qquad (29)$$

is tuned to near the natural frequency of the resonant circuit, assuming ideal conditions for simplicity of explanation.

Conversely,

$$|i_1|_{av} \to I_i \qquad (30)$$

if the inverter frequency of operation

$$f_i = 1/(T_{ok} + T_{ok+1}) = 1/2hT_o < f_o = 1/2T_o \qquad (31)$$

where

I_i = an average current which is a function of h

h > 1, an arbitrary constant.

The converter frequency is detuned from the natural frequency of the resonant circuit in the case which is characterized by relation (31). Detuning is achieved by appropriate choice of the instants of time t_k at which the thyristors are being energized. Detuning of f_i from f_o increases the apparent impedance of the resonant circuit and reduces the transfer of energy from the source to the load.

The "phase angle" ψ_{rk} which governs the ratio f_i/f_o, controls the magnitude of $|i_1|_{av}$ and, in effect, the power flow toward the converter's load.

The "mechanism" by which ψ_{rk} controls the rate of flow of charge $A_k = |i_1|_{av} T_{ok}$ for the kth cycle toward the load is further explained with reference to figure 10. All time intervals are expressed in radians β by use of the formerly implied, transformation

$$t \rightarrow \beta/\omega_o \tag{32}$$

The angle ψ_{rk} is in figure 10(a) near its minimum

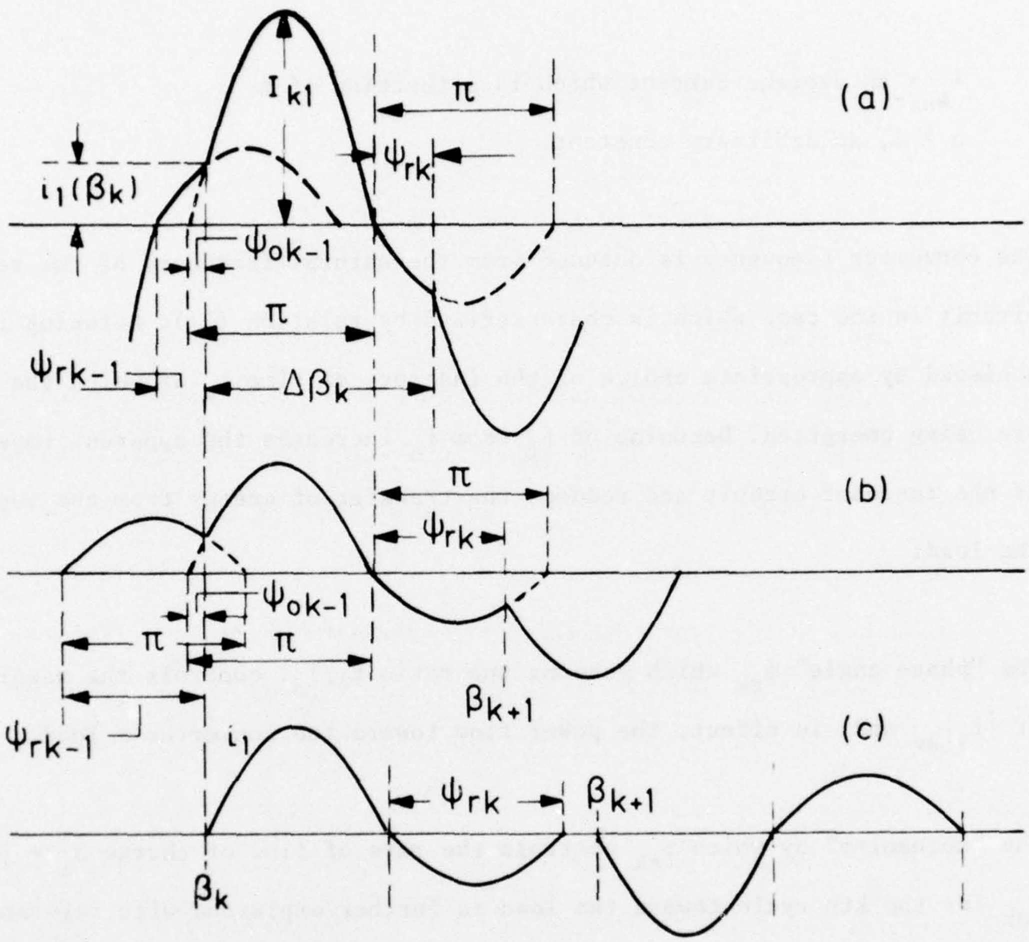


Figure 10

The resonant current i_1: (a) for $\psi_{rk} \rightarrow \psi_{rk\ min}$; (b) $\psi_{rk} \rightarrow \pi$; (c) $\psi_{rk} = \pi$ and $\Delta\beta_k > 2\pi$.

$$\psi_{rk} \min = T_{off}\, \omega_o \tag{33}$$

where

t_{off} = the required turn-off time of thyristors CR1i.

The amplitude Ik1 of i_1 is for these conditions near its maximum steady state value, as determined by design. Figure 10(b) indicates i_1 when $\psi_{rk} \simeq 2/3\pi$. The capacitor C_1 loses the charge ΔQ_k which corresponds to the ampere-seconds during the time interval ψ_{rk-1} prior to ignition of the thyristor CR1i at time β_k. The initial inductor voltage v_L (β_k) is therefore smaller than in the case illustrated in figure 10(a). This mechanism can be also recognized by a study of figures 9(d) and (e) in this context. The amplitude I_{k1} depends, largely, on $v_L(\beta_k)$. It is seen that I_{k1}, as indicated in figure 10(b), has appreciably decreated with respect to its magnitude in figure 10(a). So has the average $|i_1|_{av}$ of the absolute value of i_1. It also appears by visual comparison of figures 10(a) and (b) that a smaller amount of ampere-seconds of i_1 in figure 10(b) stretchs over a larger time interval $\Delta\beta_k = \beta_{k+1} - \beta_k$.

The amplitude I_{k1} reaches for invariant e_s and v_o, its minimum where $\psi_{rk} \geqslant \pi$ and $\Delta\beta_k > 2\pi$, as indicated in figure 10(c). The transfer of charge toward the load is for $\psi_{rk} \geqslant \pi$ governed by a pulse frequency modulation process because the charge per cycle

$$\int_{\beta_k}^{\beta_k + 2\pi} |i_1| d\beta = \Delta_{k\ min} \quad \text{for } \psi_{rk} \geqslant \pi \tag{34}$$

is independent of the pulse repetition rato f_F and the average current

$$|i_1|_{av} = f_F \, \Delta_{k\ min} \tag{35}$$

for conditions of cyclic stability for any e_s and any v_o within design limits, provided $\psi_{rk} \geqslant \pi$.

It is noted in passing that the waveforms of the current i_1 in figures 10(a) and (b) illustrate cases of the mixed pulse amplitude-pulse frequency modulation (PA-PFM).

A more detailed treatment of this tropic is found in the literature [6],[8].

The above described process of power transfer and control embodies the characteristics of a converter which were enumerated at the outset of section II, including the capacity to modify the harmonic content of the source voltage by means of active filtering. It embodies, furthermore, the advantageous process of terminating resonant currents through its controllled switching elements at the instants of time when $i_1 = 0$ which was discusses in the preceeding section 3. These characteristics allows the construction of high power converters with capacities in the multikilowatt range with employ internal frequencies of 10 kHz with presently available materials. The ongoing improvement of materials, devices and circuits could raise this frequency of hardware type equipment within the following 5 to 10 years, to 50 kHz and beyond.

2. The Electronic Protection and Control System.

a. General Principles.

The power circuit of the dc converter shown in figure 8 is governed by an electronic system which performs two distinct and totally separated functions: (1) the protection of the power system against the possible effects of untimely firing of any of the thyristors CR1i and (2) the control of transfer of energy to the load.

The two above named parts of the electronic system are named in the shown order, because of their relative significance for the converter operation as a whole. The transfer of energy through the converter is controlled by the application of trigger signals to the appropriate thyristors at the appropriate instants of time t_k, as discussed throughout sections II and III. These instants of time t_k determine the frequency of operation f_i of the current carrier i_1 for everyone of its succeeding half cycles with duration T_{ok} as discussed with reference to figures 9 and 10.

The converters which use forced current commutation for the turn-off of their thyristors provide an ohmic closed circuit for the conduction of current from the positive terminal of the source of electric energy through the thyristor(s) and back to the negative terminal of the source. It means, that the integrity of the system relies on the presumed certainty that this thyristor will be turned off before the current in this circuit would reach a magnitude which could not be handled by the turn-off mechanism [9]. In other words: a once initiated state of conduction of a "load current" i_{th} carrying thyristor has to be terminated by a mechanism of the converter which is limited to a maximum thyristor current value $i_{th\ max}$. If for any reason that turn-off mechanism would not work, then it is hoped that the inverter fuse will.

In the case of the occurence of a short circuit condition as described above, it becomes irrelevant wheter firing of the complementary thyristor which would also provide a short circuit path for the source current would take place or would be avoided. The integrity of the conventional system which employs forced commutation of thyristor currents thus depends on satisfying both of the following two conditions:

(a) that the thyristor current i_{th} would not rise above a preset maximum value i_{th} under any regular or irregulat conditions of operation;

(b) that the complementary thyristor in series with the current carrying thyristor would not be fired as long as the current carrying thyristor has not completed its cycle and the thereupon following turn-off time has elapsed.

The converter which employs the series resonant circuit shown in figure 8 places the series capacitor $C_1 = C_{11} + C_{12}$ in the path of "load current" i_{th} flow through the conducting thyristor. No mechanism, other than the aposing voltage v_{c1} of the series capacitor is needed to turn-off $i_{th} = |i_1|$. And this voltage v_{c1} feeds on i_{th} so that the conducting thyristor will, unfailingly, terminate the current conductions under all conditions of operation.

The preceeding argument was made to show that it suffices to comply only with requirement described above in (b) in order to safequard the integrity of the series capacitor converter, indicated in figure 8. Requirement (a) is, unconditionally, satisfied by an inherent circuit property: the presence of the series capacitor C1. Avoidance of excessive voltage and current stresses is discussed in subsection 4.2.3.

b. The Electronic Protection System.

The electronic protection system prevents firing of thyristors CR1i as long as the companion thyristor has not terminated its cycle of conduction and has regained its forward blocking capability [10].

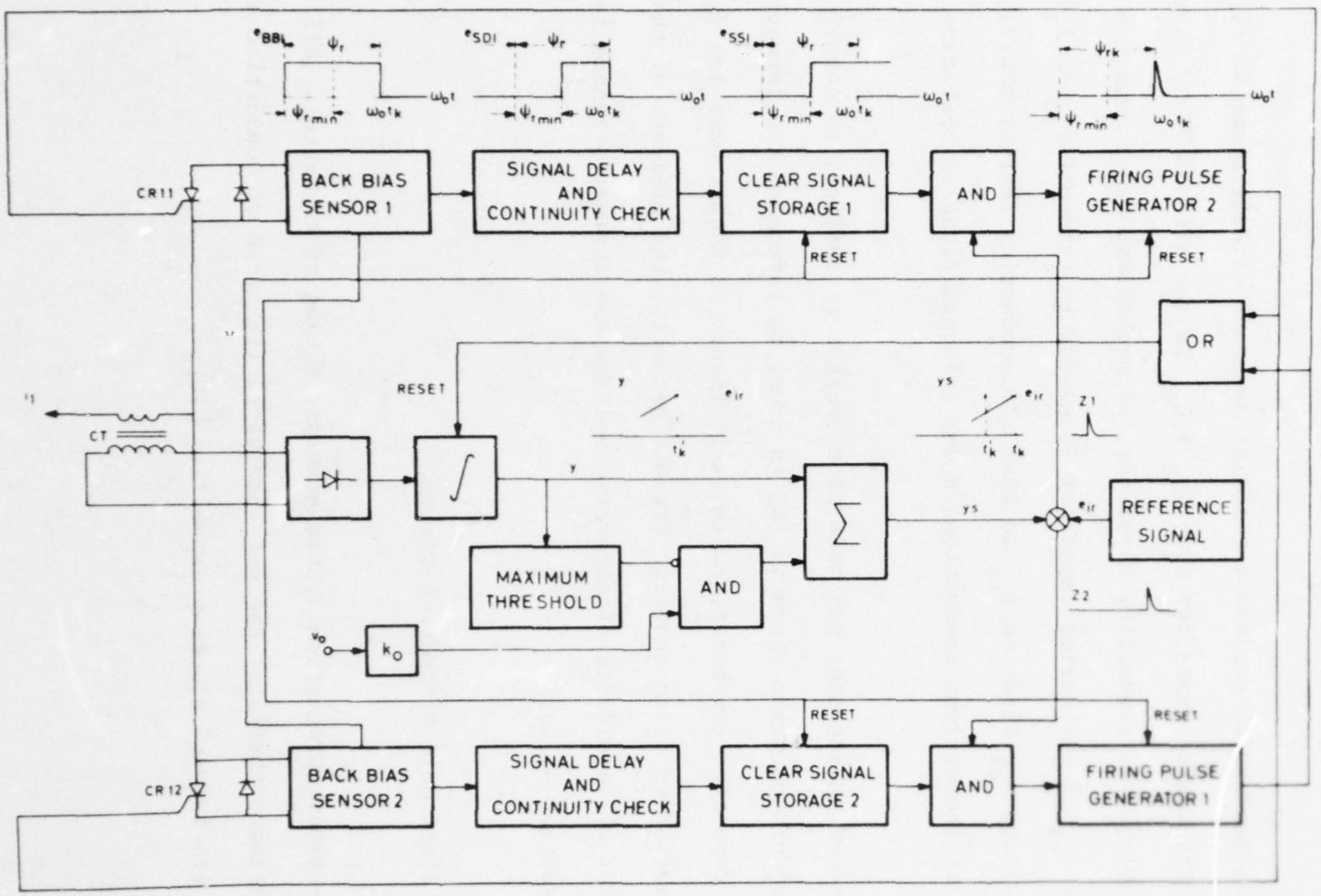


Figure 11. Block diagram of the protection and of the control systems.

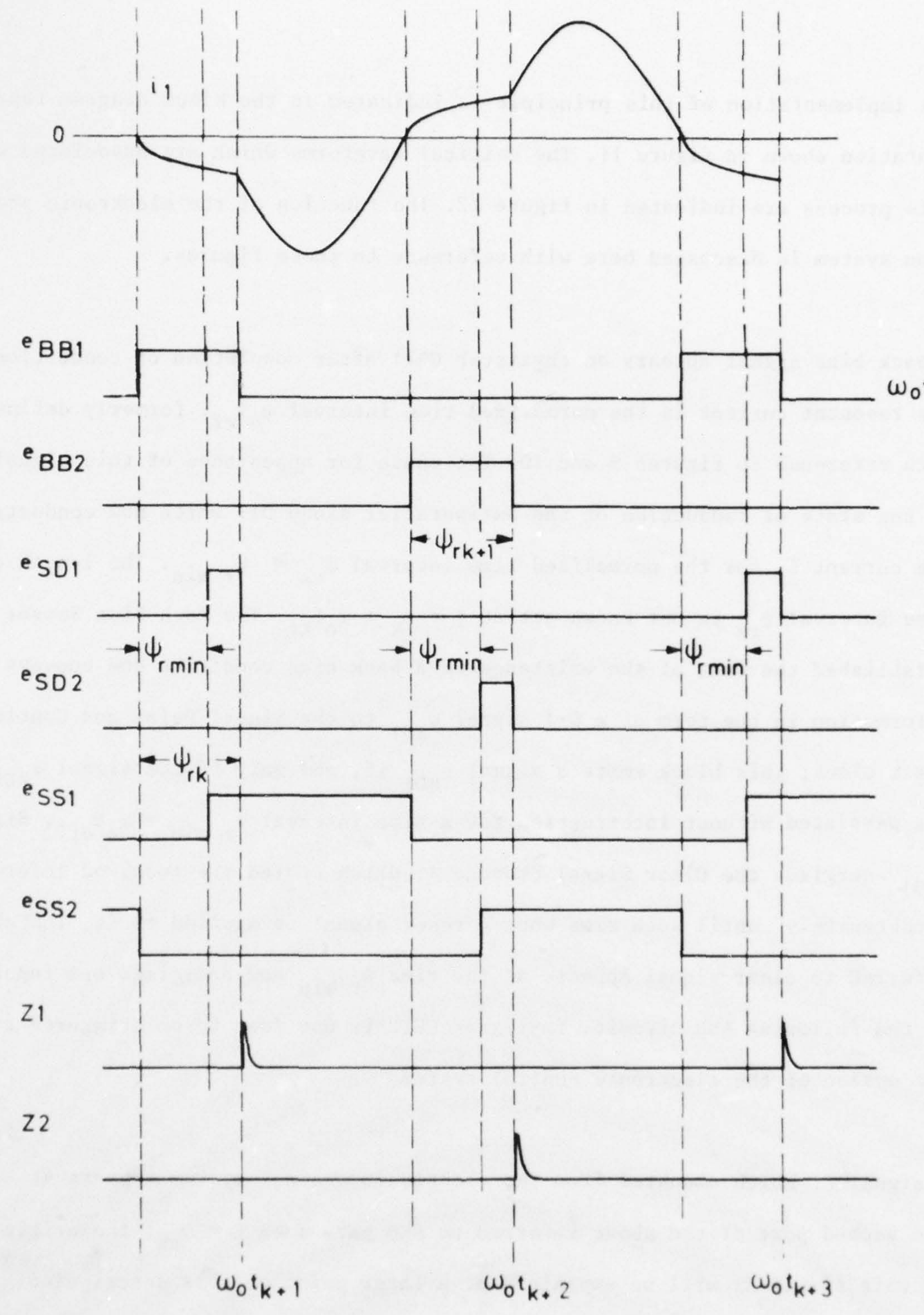


Figure 12. Critical signal waveforms of power control system.

The implementation of this principle is indicated in the block diagram representation shown in figure 11. The critical waveforms which are associated with this process are indicated in figure 12. The function of the electronic protection system is discussed here with reference to these figures.

A back bias signal appears on thyristor CR11 after completion of conduction of the resonant current in the normalized time interval $\omega_o T_{kf}$, formerly defined with reference to figures 9 and 10. The cause for appearance of this signal is the state of conduction of the antiparallel diode D11 which now conducts the current i_1 for the normalized time interval $\psi_{rk} \geqslant \psi_{r\,min}$. The length of this time interval ψ_{rk} is not known yet at $t = t_k + \omega_o T_{kf}$. The Back Bias Sensor 1 established the fact of the existence of a back bias condition and conveys this information in the form of a 0-1 signal e_{BB1} to the Signal Delay and Continuity Check block; this block emits a signal e_{sD1} if, and only if the signal e_{BB1} has persisted without interruption for a time interval $\psi_{r\,min} = \omega_o t_{off}$. Signal e_{sD1} energizes the Clear Signal Storage 1, which stored the received information "indefinitely" until such time when a reset signal is applied to it. The above referred to clear signal appears at the time $\psi_{r\,min}$ and energizes one input port of the following AND circuit. Thyristor CR12 is now free to be triggered at the option of the electronic control system.

A signal Z1 which emanates from the electronic control system appears at the second port of the above referred to AND gate when $\beta = \psi_{rk}$; the origin of this signal Z1 will be explained at a later point of this description.

Coinciduce of signals e_{sD1} and Z1 at the AND port energizes the Firing Pulse Generator 2 which then fires CR12; this thyristor will conduct current i_1 until i=0, at which time diode D12 continues conduction of this current. The ensuing back bias condition of thyristor CR12 is detected by the Back Bias Sensor 2. Analogous signal processing as explained concerning signal e_{BB1} ensues and thyristor CR11 is, eventually, fired.

It is stressed that the protection system acts completely independent from the control system, in its approval for access of the firing signals of the control system to the respective gates. Condition (b) stated in subsection a. is thus satisfied and the system can perform.

c. The Electronic Control System.

The series capacitor converter which was introduced with reference to figure 8 can be provided with the output characteristics of a voltage limited current source [6],[8].

The principle of control is based on the functional philosophy of the "Analog signal to discrete time, interval converter (ASDTIC)" [2],[12],[13]. This type of converter control is now in increasing use because it provides a high degree of static and dynamic stability to the therewith controlled pulse modulaters and is largely temperature insensitive due to an internal auto-compensating mechanism. It is often - incompletely - referred to as a "two loop" control system which does not characterize its inherent feature. A replica $k_i i_1$ of the resonant current i_1 is derived via a current transformer CT from the resonant circuit. This replica is rectified to the form $k_i|i_1|$ and fed into an integrater, as indicated in figure 11.

The signal processing operation which follows is, abundantly, described in the literature [2],[8],[12],[13]. If the attenuated output voltage signal

$$k_o v_o < (k_o v_o)_{nom} \tag{36}$$

is smaller than the nominal value $(k_o v_o)_{nom}$ of this signal then the signals Zi(i=1,2) are generated at the instants of time when

$$k_i \int_{\beta_k}^{\beta_{k+1}} |i_1| d\beta = e_{ir} \, \Delta\beta_k \tag{37}$$

It follows that

$$(1/\Delta\beta_k) \int_{\beta_k}^{\beta_{k+1}} |i_1| d\beta = |i_1|_{av} = e_{ir}/k_i \tag{38}$$

The average of the absolute value of i_1 is thus a constant, whatever the shape of i_1 and whatever the length of the time interval $\Delta\beta_k$. It means that the output current i_o of the system indicated in figure 8 is, arbitrarily, determined by adjusting

$$e_{ir}/ak_i = i_o = |i_2|_{av} = |i_1|_{av}/a \tag{39}$$

The peak to peak voltage of C_1

$$V_{c1pp} = \int_{t_k - T_{(k-1)r}}^{t_k + T_{kf}} |i_1| dt \tag{40}$$

where

$$\int_{t_k - T_{(k-1)r}}^{t_k + T_{kf}} |i_1| d\beta \simeq |i_1|_{av} T_{ok} \tag{41}$$

for conditions of cyclic stability.

It follows from (40) and (41) that

$$v_{c1pp} = |i_1|_{av} \, T_{ok}/C_1 = e_{ir} \, T_{ok}/C_1 k_1 \qquad (42)$$

where equation (38) is included into the consideration. Equation (42) states that v_{c1pp} can vary as much as T_{ok} for the case of continuous current. This variation is limited to

$$T_o + t_{off} \gtrsim T_{ok} \geqslant 2T_o \qquad (43)$$

which is less than two to one [6]. In practice the ratio

$$T_{ok\,max}/T_{ok\,min} \simeq 2/(5/4) = 1.6 \qquad (44)$$

If $k_o v_o > (k_o v_o)_{nom}$, then the maximum Threshold Sensor in figure 11 removes the blocking signal from the AND circuit which will then let the $k_o v_o$ signal go out to the summer Σ. The effect is that the e_{ir} level is modified. The current $|i_1|_{av}$ is then reduced to a value so that a preset value v_o is maintained. The current source characteristic of the converter is modified and assumes the characteristic of a voltage limited current source.

SECTION V

DESIGN OF THE 10 kW CONVERTER

1. General Requirements.

Certain specific requirements were formulated to demonstrate the feasibility of a reliable light weight dc converter. A number of critical functional characteristics had to be demonstrated that would justify the expectation that a converter with the capacity of handling megawatts of power could be constructed, based on the demonstrated principles.

The critical characteristics had to hold the promise that this converter

(a) *would operate with a high degree of* reliability;

(b) could be constructed with a high power density, expressed in kW/kg.

The requirement of reliability includes:

(a1) applications of a functional concept that holds a minimum of uncertainties; this includes a progressive overload and short circuit capability of the output terminals;

(a2) minimization and enforcement of an absolute and predictable limit on all ratios

$$i_{max}/i_{av} \text{ and } v_{max}/v_{av} \qquad (44)$$

for all converter and component functions;

(a3) a well controlled limitation of heat development in all parts of the converter.

The high power density requires:

(b1) a relatively high internal frequency of operation, such as 10 kHz

(b1) demonstration of successful converter operation at that frequency.

The following basic requirements were formulated:

Input:	Voltage, e_s	600 VDC, to be supplied from a battery bank;
	Current, i_s	~ 20 ADC
Output: For Test Purpose Only:	Voltage, v_{o1}	250 VDC, to be dissipated in a resistive load
	Current, i_{o1}	40 A
For Integration with HV Transformer:	Voltage, v_{o2}	250 VAC, square wave with a frequency between 5 and 10 kHz;
	Current $\lvert i_{o2}\rvert_{av}$	1 A, in phase with above square wave.

Voltage Ripple	v_{orms}	1% of $v_{o\,av}$
Duty Cycle	d	120 seconds "on" as a maximum, followed by 15 minutes "off".

2. The Power Circuit Design.

The lower limit for the composite efficiency of the converter and of the high voltage transformer was, as a precautionary measure, assumed to be

$$\eta_{min\ comp} \simeq 0.83 \qquad (45)$$

The amplitude v_x of the square wave $e_{s\,ac}$ which is imposed on the transformer was estimated to be [6]

$$v_{xa} \simeq \eta\, e_s/2 = (0.83)(300) = 250 \text{ V} \qquad (46)$$

An average current

$$|i_1|_{av} = P_o/v_{xa} = 10^4/250 = 40 \text{ A}_{av} \qquad (47)$$

appeared necessary in order to transfer 10 kW to the load.

The peak to peak voltage of capacitor C_1

$$v_{c1pp} > |i_1|_{av} T_{ok}/C_1 \tag{42}$$

The voltage

$$v_{c1pp} > 2e_s \tag{48}$$

in order that the system operate properly [6]. It follows from (42) and (48) that

$$C_1 > |i_1|_{av} T_{ok}/2e_s = 40 \cdot 50 \cdot 10^{-6}/1200 \simeq 2\mu F \tag{49}$$

where

$$T_{ok\,min} = 1/2f_i = 50 \cdot 10^{-6} \text{ seconds}$$

The series inductance

$$L_1 = (T_o/\pi)^2/C_1 = (40 \cdot 10^{-6}/\pi)^2/2 \cdot 10^{-6} = 80\ \mu H \tag{50}$$

assuming that [6]

$$T_o/t_{off} \simeq 4$$

The size of the output capacitor C_o is governed by the output current i_o, the filter frequency f_F and the acceptable peak to peak output voltage ripple v_{orpp}. The node equation for the positive terminal of the output filter capacitor C_i can be written as:

$$i_2 = i_c + i_o = Cdv_{co}/dt + i_o \qquad (51)$$

where

i_c the capaciter current leaving the above defined node

$di_o/dt \simeq 0$ for purpose of estimate of C_o with the understanding that $v_{orpp} << 1$.

From equation (51) follows that for a normalized frequency $f_n = 1/\pi$

$$v_{co}(\beta) = v_{co}(0) + (I_2/C_{on})(1-\cos\beta-2\beta/\pi) \qquad (52)$$

if

$$i_2 = I_2 \sin\beta$$

$$C_{on} = f_n C_o / f_F$$

The maximum of v_{co} occurs when β_{max} = arc sin $2/\pi$, as found from (51). The minimum of v_{co} occurs when $\beta_{min} = \pi -$ arc sin $2/\pi$.

Introduction of these values into (52) yields:

$$v_{orpp} = v_{co\ max} - v_{co\ min} \tag{53}$$

$$v_{orpp} = (2I_2/C_{1n})\{\cos \arcsin 2/\pi + (1/\pi) \arcsin (2/\pi) - 1\} \tag{54}$$

$$v_{orpp} \simeq .421 I_2/C_{on} = .421\ \pi i_o/2C_{on} \tag{55}$$

$$\frac{v_{orpp}}{v_{oav}} = .661\ i_o/v_{oav}\ C_{on} \tag{56}$$

or

$$C_{on} = .661\ i_o/v_{orpp} \tag{57}$$

The percentage ripple pc of the rms value $v_{or\ rms}$ of the output voltage ripple is related to the peak to peak voltage v_{orpp} by

$$v_{or\ rms} = v_{orpp}/2\sqrt{2} \tag{58}$$

Introduction of (58) into (59) yields:

$$C_{on} = \frac{.661\ i_o\ 10^2}{2\sqrt{2}\ pc\ v_{oav}} \simeq \frac{24\ i_o}{pc\ v_{o\ av}} \tag{59}$$

where

$$pc = 100\ v_{o\ rms}/v_{oav}$$

For $i_o = 1$ and $pc = 1$:

$$C_{on} = 24 \cdot 10^{-4} \tag{60}$$

The value of the actual output capacitor is found by application of the frequency transformation

$$C_o = C_{on} f_n / f_F \tag{61}$$

where

f_n = the normalized frequency $1/\pi$;

f_F = the filter frequency of 20 kHz at full power.

The output characteristic was calculated with the use of equation (61) and

$$C_o \simeq 24 \cdot 10^{-4}/\pi \cdot 20 \cdot 10^3 \simeq .04\ \mu F \tag{62}$$

A capacitor value of 0.1 μF was chosen for that purpose for reasons of practically, to yield an rms ripple of, approximately, 0.4 percent at full power operation.

The idelized model powered from a rectified sine wave with amplitude I_2 was chosen in order to attain the above carried out approximation.

The input capacitor C_i is calculated in an analogous manner, even though the charge accepted by the converter is smaller than the charge A_k which is processed by the converter within the same time interval T_{ok}. The input capacitor

$$C_i \simeq (10^4/250)^2 \; C_o \simeq 64 \; \mu F \tag{63}$$

The design of the system as a whole was, basically, oriented toward a very generous interpretation of the 2 "on" 15 "off" minute duty cycle which was stated in the general requirements (1) above.

3. The Power Capacitors.

The series capacitor C_1 = C11+C12 processes all of the resonant current i_1. The rms value $i_{1\ rms}$ is given by [1],[6]

$$i_{1\ rms} = \rho_i |i_1|_{av}. \tag{64}$$

The current form factor $\rho_i \simeq 1.25$ for full power conditions of operation [6]. The value

$$i_{1\ rms} \simeq (1.25)(40) = 50 \; A_{rms} \tag{65}$$

This rms current is equally divided between capacitors C11 and C12, respectively. The current in capacitor C11 is then

$$i_{1c1\ rms} = \frac{1}{2} i_{1\ rms} = 25\ A_{rms} \tag{66}$$

High quality capacitors, made of extended aluminium foil and polypropylene dielectric material (Components Research, Santa Monica, CA) were used for the indicated purpose. These oil impregnated, 1500 VDC capacitors are provided with heave screw type terminals to accomodate the above referred to currents. Test of these capacitors indicated a loss factor

$$\tan \delta \simeq 2\cdot 10^{-4} \tag{67}$$

for test conditions of a current density $d_{is} = 50\ A_{rms}/\mu F$ and a frequency of 50 kHz. The power loss P_{dcs} in the two series capacitors is approximated by

$$P_{dcs} \simeq (50)(660/\sqrt{2})\ 2\cdot 10^{-4} \simeq 4.5\ \text{Watts}. \tag{68}$$

The temperature rise of these capacitors which operate at one quarter of their rating was only a few degrees Celsius. The capacitors weigh approximately 200 g per unit. The power density d_{es} of the series capacitor

$$d_{is} = \frac{1}{2}(1.5\cdot 10^{3})^{2}\ 10^{-6}/0.2 \simeq 5.6\ J/kg \tag{69}$$

The output filter capacitor C_o for 10 kVDC consists of four series elements, each rated in excess of 3 kV. Oil impregnated metallized film on polypropylene was used for this purpose (Component Research). These elements of the .1 μF, 10 kVDC capacitor weighed, approximately, 50 grams before their potting into one block. The energy density of this capacitor can be described by

$$d_{eo} = \varepsilon_{co}/kg = \frac{1}{2}\, 0.1 \cdot 10^{-6} \cdot 10^{8}/0.05 = 100 \text{ J/kg} \tag{70}$$

The rms current

$$i_{co\ rms} \simeq 2\pi f_F\, C_o\, v_{or\ rms} \tag{71}$$

or

$$i_{co\ rms} \simeq 2\pi \cdot 20 \cdot 10^{3} \cdot 10^{-7} \cdot 40 \simeq 0.5\ A_{rms} \tag{72}$$

The current density d_{io} per microfarad is given by

$$d_{io} = 0.5/0.1 = 5 \text{ Ampères per } \mu F \tag{73}$$

An ordinary laboratory type capacitor is being used as input filter capacitor for purpose of isolating the resonant circuit from the high frequency impedance characteristic of the source of electric energy, the storage battery and the supply lines. The used capacitor has an electric value of 100 μF.

An rms current $i_{ci\ rms}$ of approximately

$$i_{ci\ rms} \approx 1/2\ i_{l\ rms} \approx 25\ A_{rms} \tag{74}$$

is accomodated by this 100 μF capacitor with a current density

$$d_{ii} = 25/100 = 0{,}25 \text{ Ampères per } \mu F \tag{75}$$

The preceeding presentation distinguishes clearly between the energy densities and the current densities of the series capacitor C_l, the output capacitor C_o and the input capacitor C_i respectively. Each of these capacitors has a different function at a specific impedance level, a specific frequency of operation (10 or 20 kHz) and needs to be designed and dimensioned, accordingly. The constraints which are being imposed on the design of each of these capacitors are different and will, therefore, yield different energy densities.

4. The Series Inductor.

The value for the series inductor L_l was determined in subsection 5.2. to be 80 μH. The inductor was designed for continuous operation to allow the necessary time intervals for the investigation of the experimental high voltage transformer. This inductor is, therefore, considerably bulkier than it needed to be for the specified duty cycle and, furthermore, because of a disadvantageous input voltage v_o vs. output power P_o ratio.

The inductor was fabricated with the use of two Arnold molybdenium permalloy iron powder cores, of toroidal shape with an outside diameter of 5 inches and a net cross-section of ~ 0.8 square inches. The relative permeability $\mu_r=14$. Two inductors were connected in series for simplicity, each with an inductance of, approximately 40 μH and a number of N_L of turns

$$N_L \simeq L_1 I_{kf}/A_c B_{max} = 40\cdot 10^{-6}\cdot 65/5.34\cdot 10^{-4}\cdot 0.13 \simeq 38 \tag{76}$$

Length and cross-section of the wire for both inductor halves were adjusted such that

$$R_{T\,ac} \simeq \frac{1.4}{58}\ \frac{\text{length of wire in meters}}{\text{cross-section in mm}} \simeq 20 \text{ mohms} \tag{77}$$

so that each inductor winding would dissipate, approximately

$$i^2_{1\,rms}\, R_{T\,ac} \simeq 2500\cdot 20\cdot 10^{-3} \simeq 50 \text{ Watts} \tag{78}$$

The factor 1.4 in equation (77) accounts for an estimated rise of resistance by 30 percent, due to the rise of the average temperature of the winding by up to 75 °C and for the ohmic losses which are caused by skin and proximity effects at the operating frequency of 10 kHz.

No detailed analysis of the trade-off aspects for the design of this inductor is presented here, since the primary objective of this effort was to demonstrate the feasibility of a concept, including its reliability of operation.

5. The Thyristors.

One pair of thyristors, each with a current carrying capacity of 150 A_{av}, a forward and reverse blocking voltage of 1000 VDC and an rms current tolerance of 225 A_{rms} was used. These thyristors have a wafer of one inch diamter; their conduction is initiated by a center ring gate. The turn-off time is guaranteed to be less than 12 μsec. for the appropriate back bias conditions for a junction temperature of 125 ^{o}C. The rate of rise of the anode to cathode voltage after turn-off has to be limited to 1000 V/μsec. for the first 350 Volt rise and then in succession to 500 and to 300 V/μsec.

These thyristor characteristics appeared unequaled at the time of their selection for this purpose (1975). Newer thyristors with considerably improved characteristics are currently available. The described thyristors handle, easily, the 50 A_{rms} and peak voltages up to 800 VDC. The thyristors were attached to undersized cool plates, jointly with their antiparallel diodes. Individual RLC networks are being used to limit the rate of rise of anode to cathode voltage to approximately 200 V/μsec.

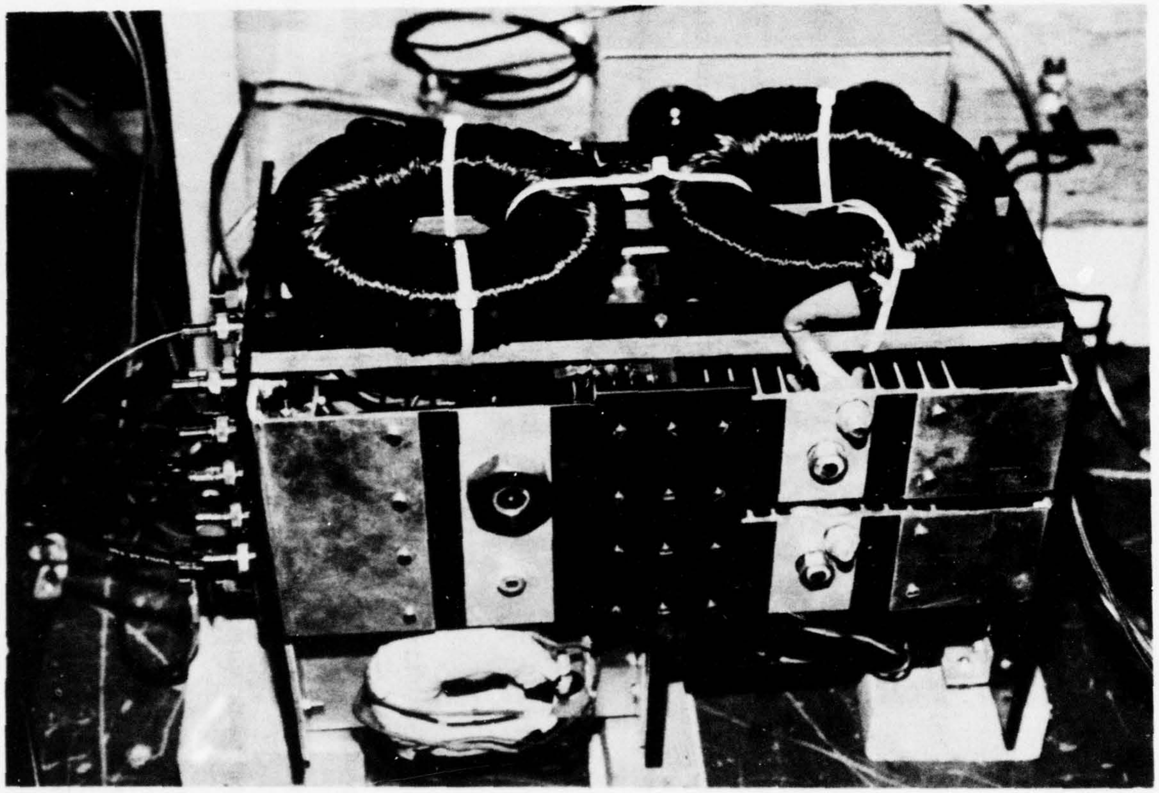


Figure 13. The power system of the light weight 10 kW converter

6. System Construction.

The frame of the power system consists of the aluminium cool plates for the semiconductor devices. These cool plates with vertical fins are interconnected by nonconductive materials. The assembly forms a rectangular box, shown in figure 13. Two 5" fans force air vertically up through this rectangle which is "crowned" by the two described inductor halves. The power assembly weighs 10.2 kg with exclusion of the fans. Again, no serious attempt was made to optimize the components or the associated structure.

The control electronics are mounted on two boards so that all components which are mounted on printed circuits are, readily, accessible. The electronics are energized by closely regulated power supplies at 20, 15, -10 and -15 Volts. The power for that purpose is derived from a 117 VAC single phase line. All signals which emanate from the power system are conveyed by shielded coaxial cables to the control electronics to avoid the intrusion of the dreaded common mode effects into the high impedance circuits of the control electronics. A carefully engineered system of sequentially interlocking functions avoids the penetration of faulty and spurious signals, which are even being anihilated after they would penetrate into the logic system. Analog logic is used for that purpose in preference to digital logic because of a high level of rejection of disturbances. A photograph of the control electronics is shown in figure 14. The assembled converter system is illustrated in figure 15.

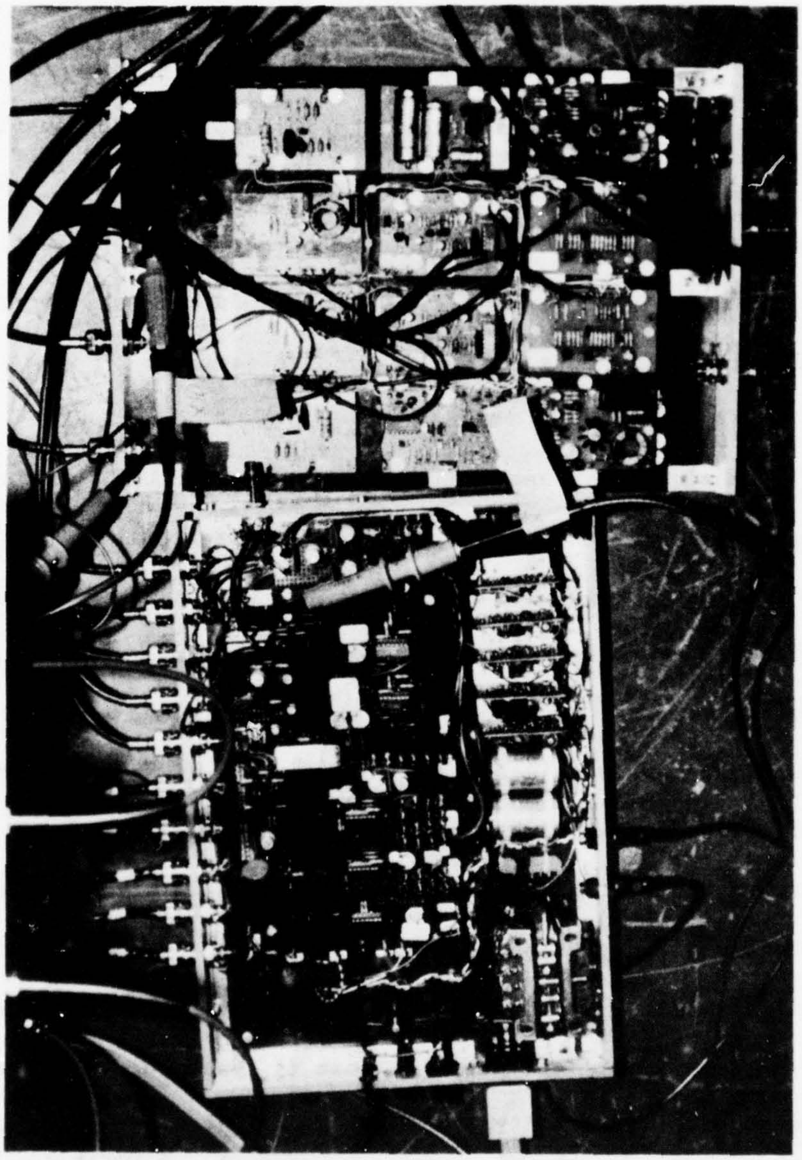


Figure 14. The control electronics of the 10 kW converter.

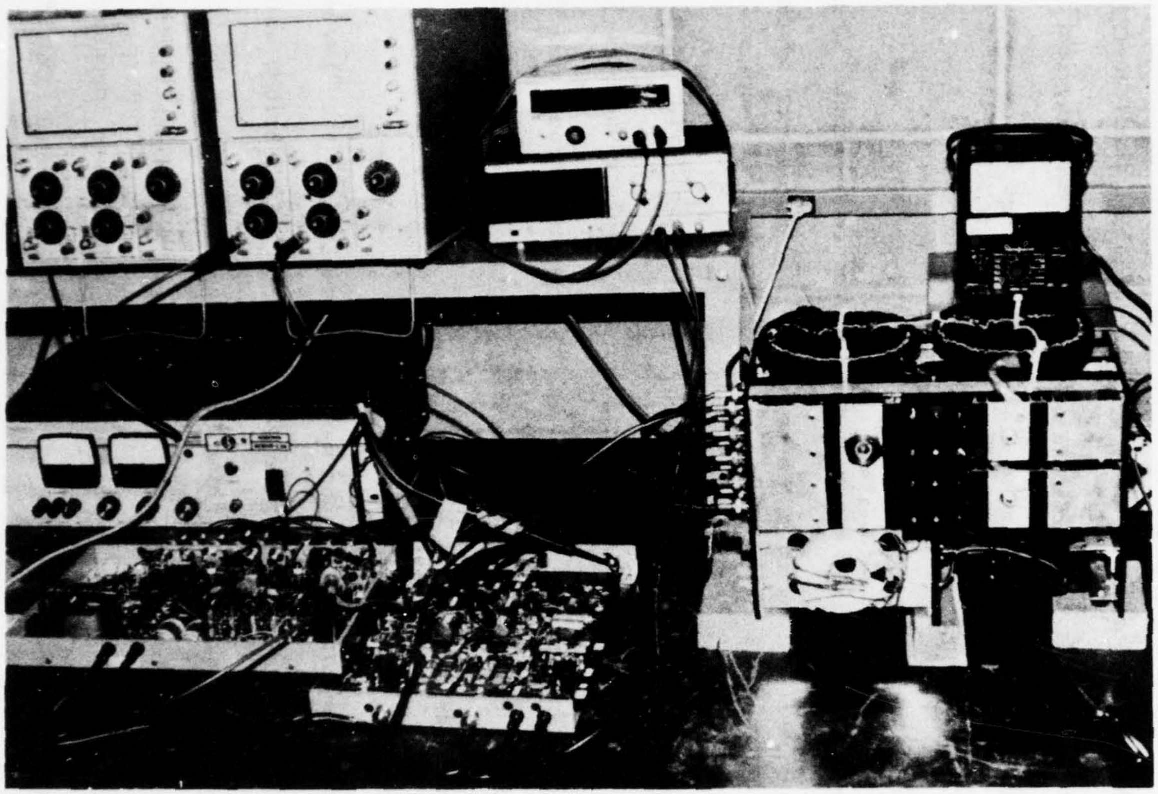


Figure 15. Test set-up for the 10 kW converter

SECTION VI

RESULTS

A lead-acid battery was used as source of electric dc energy for the test of the converter. This battery consists of assemblies with individual nominal voltages of 96 VDC.

The test was carried out in, essentially, six steps. One of the above referred to battery assemblies after another was added to provide the supply voltage e_s in successive steps from 100 to 600 VDC for purpose of system check-out.

The output terminals of the converter were, initially, short circuited for test of the converter with the average of the absolute value $|i_l|_{av\ max}$ of the resonant current i_l; the converter was then powered from a 100 VDC source. Proper operation of all critical converter functions was verified for the above described conditions.

A resistive load of 7.3 ohm was then connected to the "low voltage" output terminals of a floating full wave diode rectifier bridge which simulated the primary winding of transformer XF, indicated in figure 8. It means that the output rectifier bridge, the output filter C_o and the load were, physically, brought into the primary circuit at the appropriate impedance level, for purpose of systems check-out and test. The high voltage transformer with rectifier bridge and filter for an output of 10 kV was to be connected subsequent to successful check-out of the inverter part of the converter system.

The results of the low output voltage test are summarized in Table I. All indicated values are given in their average form. They are, therefore, designated by capital letters and thus related to the same symbols with lower case letters in the preceeding text. Distinction is made between dc output power P_{odc} and

Table I

TEST RESULTS OF THE 10kW CONVERTER

E_s VDC	I_s ASC	V_{o2} VDC	I_{o2} ADC	R_L OHM	P_s WATT	P_{odc} WATT	P_{oac} WATT	$100\,\delta_{dc}$ %	$100\,\delta_{ac}$ %	dv/dt v/μsec.
100	2.7	41	5.61	7.3	270	231	248	85.5	91.8	15
200	5.9	90	12.33	7.3	1180	1110	1137	94.0	96.3	25
295	9.0	137	18.76	7.3	2655	2570	2626	96.8	98.9	40
475	15.3	233	30.55	7.3	7267	6812	6904	93.7	95.1	120
560	20.1	250	42.10	5.94	11256	10525	10651	93.5	94.6	180

the ac output power $P_{o\,ac}$. An estimate of the ac output power is calculated as follows:

$$P_{o\,ac} \approx P_{odc} + 3\,v_D I_{o2} \qquad (79)$$

where

v_D = the voltage drop ($\sim$ 1V) in each diode of the output rectifier bridge;

A factor three (3), rather than two (2) is used for the diode bridge pair, $3\ v_D \approx 3$ V, in (79) to accomodate the switching losses at 10 kHz.

It was necessary to lower the load resistance R_L from 7.3 to 5.94 ohms when it became apparent that the six battery assemblies in series could not sustain an input voltage of 600 VDC but reduced their output voltage to 560 VDC when a load current of 20.1 Amperes was drawn. An ac output power of 10.65 kW was attained at this point with an efficiency of 94.6 percent, as calculated from the test data.

The above given test data are compared to those obtained by tests performed by the contractor in a comprehensivly equipped laboratory. A pair of calibrated wide band wattmeters with a cut-off frequency of 100 kHz and with an accuracy of 2 percent of the full scale value were used for that purpose. Tracking of the two wattmeters of the same make (Marek, Hamburg) and the same type was observed on both sides of the systems for correction of possible errors. The residual error is estimated to be less than 0.2 percent.

Two sets of data are given in Table II. One set of data was taken with capacitor values of .02 μF in the dv/dt limiting network for each of the two thyristors. The maximum rate of rise was then limited to

$$(dv/dt)_{max} \simeq 500 \text{ V/}\mu\text{sec. for } e_s = 520 \text{ VDC} \tag{80}$$

which is 50% of the concerned stress capability of the thyristor, as stated in subsection 5.5. The power loss $P_{dv/dt}$ in both dv/dt networks can then be approximated by

$$P_{dv/dt} \simeq 2\tfrac{1}{2}\,(520)^2(.02\cdot 10^{-6})\; 2\cdot 10^4 \simeq 108 \text{ Watt} \tag{81}$$

Table 2

CONVERTER's TEST DATA WITH SIMPLE AND WITH AUGMENTED dv/dt NETWORKS

C_d	E_s	I_s	V_{o2}	I_{o2}	P_s	P_{odc}	$P_{o\ ac}$	$100\ \delta_{dc}$	$100\ \delta_{ac}$	dv/dt
μF	VDC	ADC	VDC	ADC	WATT	WATT	WATT	%	%	V/μsec.
0.02	520	21.72	248	43.54	11294	10798	10928	95.6	96.8	500
0.06	520	21.70	243	43.53	11284	10578	10708	93.7	94.9	160

The first set of data in Table II gives the test results which were obtained with a "light" dv/dt-network that contained a capacitor $C_d = .02\ \mu F$.

The dv/dt networks were then augmented for purpose of preemting any adverse effect on the thyristor operation that could be caused by a condition of resonance between the parasitic effects of the source, the battery, the supply line and the input filter capacitor. Such a condition of resonance could cause added voltage overshots to the input filter and with it, more severe voltage stresses on the thyristors.

These augmented dv/dt-networks include capacitors $C_d = .06\ \mu F$, which have three times the "normally" needed values. The added power loss $P_{dv/dt}$ which is caused by the increase of C_d from its design value $.02\ \mu F$ for the full power operation reflects itself in the data of the second line in Table II:

$$P_{dv/dt} + \simeq 2\tfrac{1}{2}\ (560)^2\ .04 \cdot 10^{-6} \cdot 2 \cdot 10^4 \simeq 250 \text{ Watt} \qquad (83)$$

The concern about possible overshots for the above described reasons appeared unfounded.

The "heavy" dv/dt-networks proved to be the most noticeable hot spot of the which was constructed for the 2-15 minute duty cycle. Even though, the syste could be operated continuously for 30 minutes without damage to it.

The capability of the system to operate for lengths of time beyond the presc duty cycle proved welcome during the prolonged tests which were associated w the development work of the high voltage transformer. This high voltage tran former with its rectifier stack was integrated with the described converter with the high voltage filter. The therewith associated voltage divider was i tegrated with the control electronics and operation of the thus integrated s established. The short circuit capability of the system without damage to it and without even blowing a fuse proved invaluable for the integration work.

SECTION VII

CONCLUSIONS

1. The Demonstrated Technology

The feasibility of a highly reliable and light weight multikilowatt dc converter was demonstrated. The characteristic operation of this type of converter allows internal operating frequencies in the order of 10 kHz. This internal frequency which is attained with available components exceeds the "state of the art" of converters with these power capacities by more than an order of magnitude.

The high power frequency reduces weight and size of apperatus by approximately an order of magnitude over the state of the art with the added features of (a) voltage control capability, (b) active filtering according to the needs of source and load, and (c) performing necessary functions of stabilization.

The high degree of efficiency (up to 97% for the inverter) which is, almost, inherent in the presented type of converter adds to its reliability and reduces the need for elaborate and heavy cooling mechanisms. The high degree of reliability is emphasized by the converters capability to endure repeatedly the suddenly occuring short circuit conditions at its output terminals.

The feature of resonant type internal circuits allows the use of any fast switching elements, such as conventional or GATT [14] thyristors, transistors, spark gap triggered vacuum tubes and related devices at considerably higher frequencies than otherwise attainable.

There is no appearent indication of an upper limit for the power level of the presented system. One of the key elements is the current carrying capability of the switching elements. The converter technology is, usually, developed around the therewith imposed limitations.

2. Switching Elements: Available and in Development.

The introduction of a high power frequency concept into the high power (MW) converter design has had a major impact on high voltage transformer technology and led to a drastic improvement of transformer power density [15].

The continued improvement of fast switching thyristor technology seems to increase the expectations in that direction where a few years ago there were only speculations based on exploratory work in its early phases. A powerful fast switching thyristor of the GATT type [14] has, recently, become available. This thyristor has forward and reverse voltage blocking capabilities of ~ 1 kV, a current switching capability of ~ 1 kA_{rms} and a turn off time of 10 μsec. without and of 5 μsec. with assistance in the gate turn off process. These four terminal devices have a "snow flake" type gate structure; they are mounted inside a "hockey puck" frame with relativly large double side cooling areas. Further development of those devices to higher blocking voltages such as ~ 3 kV appears more subject to the expectations of a lucrative market than being impeded by serious physical or technical limitations. The 2.6 kV thyristor for 900 A_{rms} with the inner ring gate is, presently, used in installed equipment for high voltage dc (HVDC) transmission lines up to 1.4 GW. The above cited fast switching transistor can be viewed as derived from the inner ring gate thyristor by application of the "snow flake" structure. This development can be, also, viewed as a first step toward the fast switching multikilowatt thyristor in the context of multimegawatt ac to dc conversion and its converse, involving higher internal frequencies [3].

It is believed that it should be possible to construct a one MW converter with the employ of six sets of presently available thyristors in full bridge configurations [8]. The number of thyristor sets would not be affected by the input voltage or by the use of one half or full bridge configurations in the converter. Yet, the apparently ongoing development of these thyristors toward a 2.6 kV blocking voltage could cut the number of needed sets from six to two for a megawatt converter.

The triggered spark gap switch appears to hold the promise to perform the switching function within its limited life span for appreciable currents and blocking voltages [16].

3. Capacitors.

The brief analysis of capacitors requirements contained in subsection 5.3. reveals the necessity to differentiate between the functions of these capacitors and the therewith associated needed indivudual characteristics.

The main three functions of these capacitors which are used as input filters, as series capacitor and as output filter differ in (a) impedance level and (b) rms current carrying capacity per microfarad. The above named two conditions (a) and (b) have profound effects on the applied technology in terms of thickness of the dielectric material, current capacity of the "plates" which are implemented in the form of metallized dielectric or solid foil and the type internal and external structure of the current carrying terminals. These effects translate themselves, necessarily, into different energy densities d_e for each of the above named three functions, depending upon the applied maximum voltage $v_{c\ max}$, the current density per microfarad d_i and the concerned frequency of operation.

Zero order approximations can be obtained by extrapolation of the capacitor weight for larger converters, by use of a differentiated approach as referred to above; simplification of this process by referral to indiscriminate energy densities of capacitors would yield less than that.

The series capacitor which was used for construction of the presented system has an energy density d_{es} of 5.6 J/kg, as given by equation (69). Yet, the usable part of this energy density $d_{es\ max}$ as limited by the current density d_{is} of the same capacitor is 50 $A_{rms}/\mu F$ as cited with reference to equation (67). The useful energy density is calculated from

$$d_{es\ max} = 1/2\ (v_{ci\ max})^2\ 10^{-6}/0.2 \qquad (84)$$

in analogy to (69). The peak voltage amplitude

$$v_{cl\ max} = \sqrt{2}\ i_{cs\ rms\ max}/2\pi f_i\ C_s \qquad (85)$$

where

$C_s = 1\ \mu F$

$i_{cs\ rms\ max} = 50\ A_{rms}$ at 10 kHz.

The useful maximum capacitor amplitude thus becomes

$$v_{cl\ max} \simeq 70\ 10^6/6.28\cdot 10^4 \simeq 1100\ V \qquad (86)$$

The useful energy density in (84) is then given by

$$d_{es\ max} = 1/2\ (1100)^2\ 10^{-6}/0.2 \simeq 3\ J/kg. \qquad (87)$$

This relativly low energy density emphasizes the need for a departure from oversimplifications of this matter. Yet, the impact on the converter technology is not as significant as may appears on the surface. The capability of this capacitor to transfer electric power P_{cs} in a 10 kHz system is given by

$$P_{cs} \simeq 1/2\ v_{cl\ max}{}^2\ C_s\ 2f_i \simeq 12\ kW \qquad (88)$$

The power density d_{ps} of this type of capacitors is thus

$$d_{ps} = P_{cs}/kg = 12/0.2 = 60 \text{ kW/kg} \tag{89}$$

It means that approximately 16 kg of the currently used type of capacitor is needed for each MW of a series capacitor power converter, or approximately .035 lbs./kW.

The size of the output capacitor depends on the permissible output voltage ripple. In the case of the presented converter it was shown that for an output voltage ripple $v_{or\ rms} = 0.4 \cdot 10^{-2}\ V_o$ it was necessary to apply an energy storage ratio

$$\varepsilon_o/\varepsilon_s = 5/0.3 \simeq 16 \tag{90}$$

where

$\varepsilon_o = \frac{1}{2}\ 0.1 \cdot 10^{-6} \cdot 10^{8} = 5$ Joules, the energy stored in the output filter capacitor C_o;

$\varepsilon_s = \frac{1}{2}\ 2 \cdot 10^{-6}(550)^2 \simeq 0.3$ Joules, the peak energy stored in the series capacitor $C_s = C_1 = 2\ \mu F$

$$550 \simeq 70/6.28 \cdot 10^4 \cdot 2 \cdot 10^{-6} = \sqrt{2}\ i_{1\ rms}/2\pi f_i\ C_1$$

The ratio $\varepsilon_o/\varepsilon_s$ in (90) can be changed as a function of

$$\varepsilon_o/\varepsilon_s = 64/0.1\ k_\varepsilon \tag{91}$$

where

k_ε = a constant which indicates how many times the output voltage ripple can exceed the value of a 0.1 percent rms ripple.

The relative weight ratio

$$W_{T_o}/W_{T_s} = (\varepsilon_o/d_{eo})(d_{es}/\varepsilon_s) = 16(.75/100) = 0.12 \tag{92}$$

where

W_{T_o} = the needed weight of the output filter capacitor C_o;

W_{T_s} = the needed weight of the series capacitor C_1;

$0.75=(1/4)3$ = the maximum energy density of C_1 for an amplitude of 550 V, thus one quart of $d_{es\ max}$ in (87).

The relative weight ratio (92) depends in each case on the chosen value of k_ε in (91). The numbers used in (92) are based on the materials of the constructed model which, in turn did only partially use the power capacities of the used components. The output capacitor was designed and constructed for the specific purpose for which it was used. The series capacitor C_1 was used only at one quarter of its energy density $d_{es\,max}$ given by (87) and employed only part of its peak energy storage capability $d_{es} = 5.6$ J/kg given by (69). If all of the available energy storage capability of C_1 had been used, then

$$(W_{T_o}/W_{T_s})_{max} = (5/100)(5.6/1.2) \simeq 0.32 \qquad (93)$$

It means that the weight of the output filter capacitor could become comparable to that of the series capacitor, even though the energy density ratio d_{eo}/d_{es} of the two types of capacitors is approximately $100/5.6 \simeq 18$. The necessary derating of C_1 was left out of the consideration for purpose of simplicity at this time.

A similar situation arises for the input filter capacitor C_i. The ratio (93) is (a) increased because of the lower input voltage level e_s and (b) decreased because of the, probably, less stringent input current ripple requirements.

All functional requirements will have to be known before a meaningful prediction for the weight of a large converter can be made. It is the purpose of the above argument to highlight the diversity of considerations which concern the converter design and to develop the concerned technology.

4. Magnetics.

The high frequency converter with its present base line at 10 kHz made a drastic reduction of weight and size of the power transformer possible, thus opening the road to a reliable light weight converter for power transfer, control, active filtering and dynamic stabilization.

The series inductor L_1 and the dv/dt coils should be given continued attention for purpose of further increase of their power density, even though the system, as described here, is feasible with application of existing materials and techniques. The above referred to attention should be, primarily, directed toward the development of new concepts for magnetic energy storage with the use of existing materials. Superconductivity should be excluded from consideration of frequencies in excess of 10 kHz. The above referred to concepts are distinguished from other more conventional, attempts to attain higher energy densities by the application of cooling methods. A study on how to reduce intrinsically the dissipated heat per Joule of stored magnetic energy should preceede a "cooling" study, which should, indeed, be used to cool an intrinsically more efficient process.

5. General Recommendations.

It appears productive for the purpose of yet higher power densities to further increase the internal frequencies of dc converters. Present semiconductor technology may allow frequencies up to 20 kHz at the MW level with use of proven circuit concepts, as the one presented here.

More advanced circuit concepts may allow the application of even higher frequencies with existing components and materials [17].

The interface requirements of the converter with its intended source and load, respectively, can add considerably to strengthen the purposeful direction of the power converter development.

The US semiconductor industry should be **exhorted** and supported in a drive for fast switching thyristors with large power capacitors to secure the capability for construction of equipment for long life operation.

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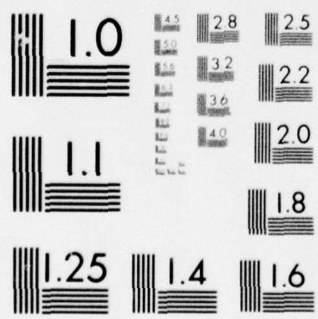

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