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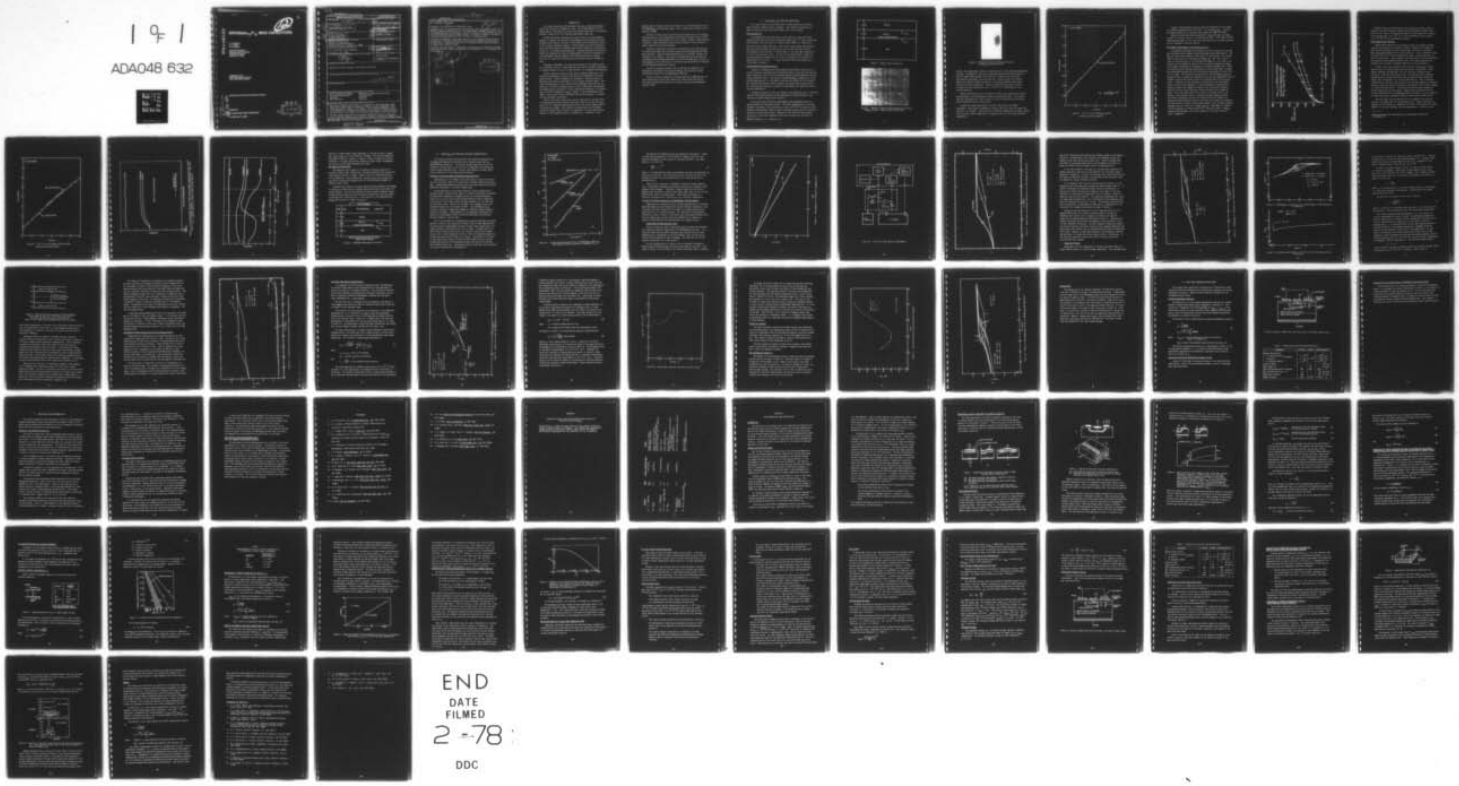

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GPO/GaAs$_{1/2}$P$_{1/2}$ MOS CAPACITORS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report presents the results of a program to investigate the surface passivation properties of a dielectric thermally grown on GaAs$_{\frac{1}{2}}$P$_{\frac{1}{2}}$. Oxide films were grown at 700°C in dry oxygen. Ion microprobe analysis of the oxide composition indicates that the bulk of the oxide is arsenic deficient and that there is an arsenic-rich insulator-semiconductor interface region.

Current-voltage characteristics showed a Frenkel-Poole type of conduction with a transient behavior due to electron trapping. Dielectric strengh

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20. ABSTRACT (Continued)

averaged 1.75 x 10^6 V/cm for unannealed films.

Depletion-type C-V characteristics were observed, and are a result of the low minority carrier generation rate in the wide bandgap $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$. Hysteresis in the C-V characteristics is attributed to electron trapping in states which are not in equilibrium with the bias sweep voltage. The static dielectric constant of the oxide was determined to be 6.3 from the C-V characteristics.

Interface trap density in the upper portion of the bandgap was determined to be about 8 x 10^{11} $cm^{-2} - eV^{-1}$ using the capacitance differentiation method. A significant illumination effect on this trapping behavior was observed due to emptying of electron traps.

Interface analyses based on conductance-voltage data were inconclusive because existing analytical models are apparently not adequate for III-V compound MOS interfaces.

I. INTRODUCTION

This report describes work performed from June 1, 1977 to September 1, 1977 on NVL Contract No. DAAK70-77-C-0122. The primary objective of this program was to investigate the surface passivation properties of a dielectric thermally grown on the III-V compound semiconductor $GaAs_{1-x}P_x$.

Surface passivation insulators are used as barriers to environmental exposure to improve the stability and performance of semiconductor devices. Thermally grown SiO_2 has resulted in the highest quality passivation layers in the silicon technology; however, limited research has been performed to study the effectiveness of thermally grown native insulators as passivation layers for III-V compound semiconductors. Although many device applications require an extremely low dielectric/semiconductor interface state density, all semiconductor devices benefit from surface passivation insulators which act as a barrier to contamination and decrease junction leakage currents.

Therefore, development of a passivating dielectric for GaAsP surfaces will be useful, not only in GaAsP devices, but also in ultimately developing a suitable dielectric for use in GaAs and other III-V compound semiconductors.

Thermal oxide has previously been grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ (Reference 1) and electrical measurements on these films were used to determine an optimum growth process. Coerver (Reference 2) conducted a literature survey to determine the possible constituents of the insulator grown at 700°C. This study indicated that the only possible solid compounds which can form the dielectric at 700°C are β-Ga_2O_3 (gallium oxide), $GaPO_4$ (gallium phosphate) and $GaAsO_4$ (gallium arsenate). Further experiments (Reference 2) indicated that the film is composed of (Ga_2O_3 + $GaPO_4$), or gallium-phosphate-oxide (GPO). These results further indicated that gallium phosphate is probably the major molecular constituent.

Some of the initial electrical results on MOS devices indicated that this phosphate-containing thermal oxide might prove more useful for application to III-V compound semiconductor devices than oxides composed mainly of crystalline β-Ga_2O_3. Such crystalline oxides result during thermal oxidation of GaAs, and are usually not acceptable for device applications because of high leakage currents or instabilities. Therefore, it was

apparent that a further study of the dielectric and interface properties of the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ structure was needed. Such a study forms the basis of this research program.

Section II of this report describes the characteristics of the $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ starting material and the experiments performed to thermally grow a native dielectric on this semiconductor for use as a gate insulator in MOS capacitor structures. Some preliminary results from an analysis of the dielectric atomic composition are also presented.

Section III describes the electrical characteristics of MOS capacitor structures fabricated with a thermally grown gallium-phosphate-oxide (GPO) gate insulator. Current-voltage characteristics of the gate insulator are included in this section. The results of capacitance-versus-voltage and conductance-versus-voltage measurements are also presented here, as well as some comments on the difficulties in analyzing such characteristics obtained on wide-bandgap semiconductor devices.

Section IV contains a design study to evaluate the feasibility of fabricating a gate-controlled diode on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ for evaluating surface recombination velocity at the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ interface.

Finally, Section V summarizes the report and some recommendations are given pertaining to future work required to further study and improve the surface passivation properties of thermally grown gallium-phosphate-oxide on GaAsP.

II. GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS CAPACITOR FABRICATION

This section describes the fabrication of MOS capacitors utilizing a gate insulator thermally grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$. The electrical properties of these structures are discussed more fully later in this report.

Starting Material

The semiconductor material used in this study was n-type (tellurium-doped) epitaxial gallium arsenide phosphide ($GaAs_{1-x}P_x$)* of <100> orientation. The epitaxial layer was grown on a heavily doped n-type ($\rho \approx 0.003$ Ω-cm) gallium arsenide (GaAs) substrate. There was a graded region approximately 35 microns thick between the epitaxial layer and the substrate in which the phosphorus mole fraction, x, varied from x = 0 at the GaAs substrate to x = 0.5 at the epitaxial layer. On top of this graded region a region of constant phosphorus composition (x = 0.5) is then grown to a thickness of approximately 37 microns. A cross section of the starting material is illustrated in Figure 1.

Starting Material Characterization

Figure 2 is a Nomarski-contrast photomicrograph which illustrates the surface structure associated with dislocation arrays in the starting material. These features are due to lattice mismatch between the GaAs substrate and the $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ epitaxial layer. The region of graded phosphorus composition, which was mentioned earlier, is included to minimize the effects of this mismatch. The resulting dislocation arrays, however, are common when a semiconductor of a given lattice constant is grown on a semiconductor of differing lattice spacing (Reference 3).

Although dislocation arrays are present in the epitaxial layer, reflection electron diffraction patterns of the semiconductor surface (Figure 3) are indicative of good single-crystal material.

Four-point-probe resistivity measurements were attempted during the characterization of the GaAsP surface. The donor concentration of the semiconductor was chosen to be relatively low ($<3 \times 10^{17}$ cm^{-3}) to provide a semiconductor surface which could be readily depleted during electrical characterization of the interface region. Because of the relatively high surface resistivity, stable and repeatable probe point contacts are difficult to

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*Grown by Epidyne, Inc., Hawthorne, CA

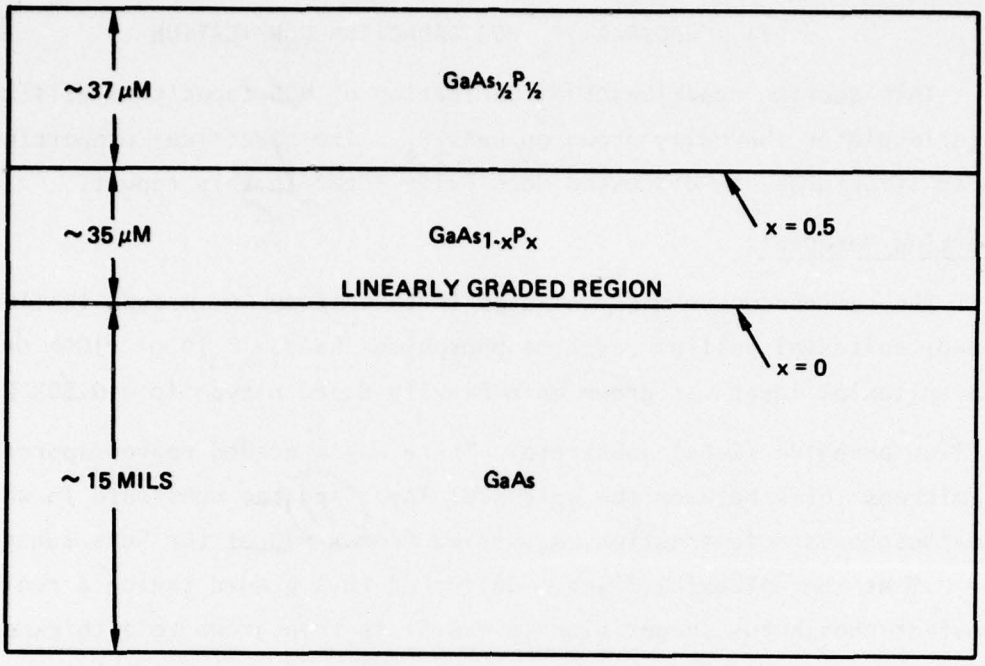

Figure-1. $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Starting Material

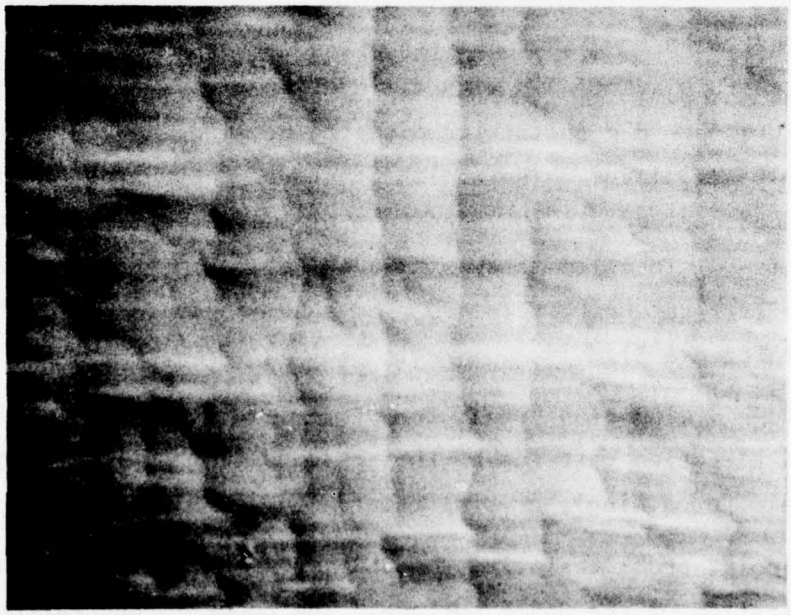

Figure-2. Nomarski Contrast Photomicrograph of Starting $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Surface. Magnification Ratio ≈150X.

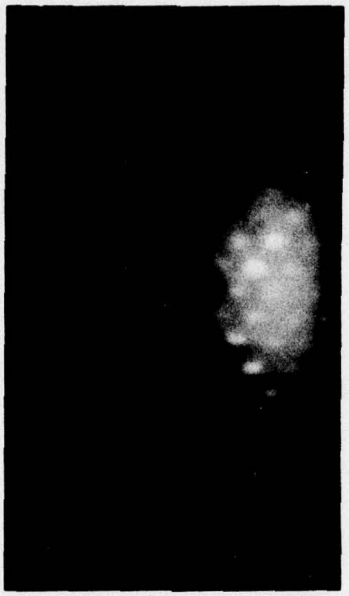

Figure-3. Reflection Electron Diffraction Pattern of $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Starting Material

achieve. This measurement problem is characteristic of many compound semiconductor surfaces. Consequently, four-point-probe measurements were discontinued in favor of capacitance-voltage (C-V) profiling of Schottky barrier diodes fabricated on the $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ starting material. Figure 4 shows $1/C^2$ plotted against the applied reverse voltage for a Al-$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Schottky diode fabricated on the starting material. From the slopes of these types of plots, a uniform carrier concentration of 2.7×10^{17} cm^{-3} is determined for the starting material.

Before introduction into the oxidation furnace, the samples were cleaned and degreased in trichloroethane, acetone, and deionized water. No chemical etch was used because of initial results showing increased surface structure along dislocation arrays after etching.

Dielectric layers were grown in an open tube using a dry oxygen atmosphere. The oxidation temperature used was 700 ± 5°C, and the oxygen flow rate was 1.0 liter/min. This particular oxidation temperature was chosen because of the initial results (Reference 1) suggesting this as the optimum oxidation temperature.

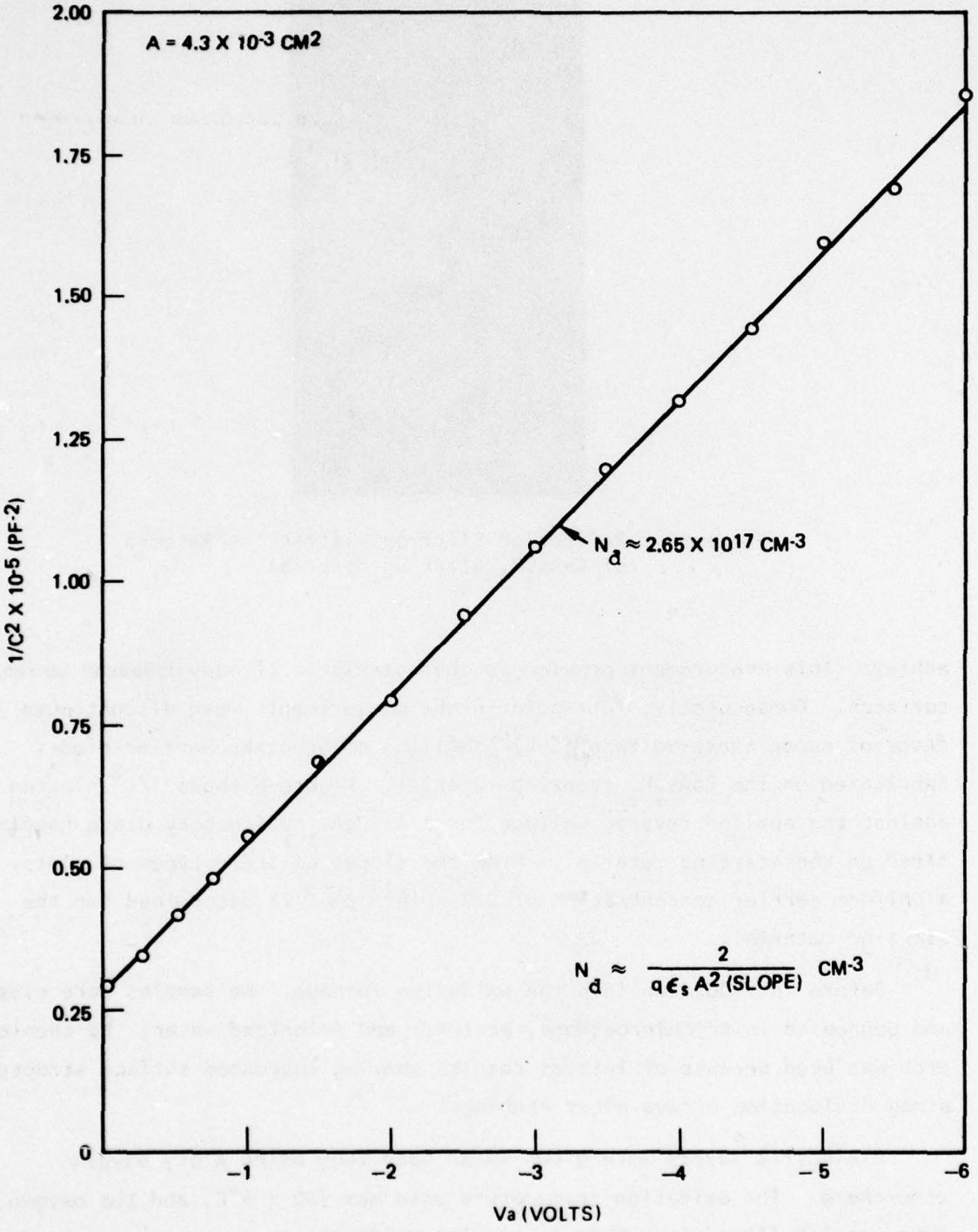

Figure 4. $1/C^2$ vs V for Al-$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Schottky Diode on Starting Material

Figure 5 (from Reference 4) gives curves for GPO growth in dry oxygen for different phosphorus mole fractions, x, of the $GaAs_{(1-x)}P_x$. The film thicknesses chosen for the present study ranged from 1000 Å to 2500 Å.

Some post-oxidation annealing experiments were performed in nitrogen at 700°C for various times, or in forming gas at 450°C. The effect of these annealing experiments on the electrical characteristics of the MOS structures will be discussed in the next section.

Ellipsometry Measurements to Determine t_{ox} and η

Ellipsometry measurements were made on the grown films and the results were analyzed using a computer program developed by NBS (Reference 5). The data of Figure 5 were obtained using results of this program. The average index of refraction for films grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ was 1.64. This value is close to the value given in the literature for $GaPO_4$ (η = 1.6), and is consistent with the hypothesis that the film is primarily composed of $GaPO_4$. The thickness determined by ellipsometry correlated reasonably well (±15%) with surface profile (Dektak) measurements on etched oxide steps, although both measurement methods can only be considered approximate for these films at this stage. The uncertainty associated with the ellipsometry analysis program is that it assumes an insulating film of uniform composition, which is evidently not the case, based on the ion mircoprobe data to be discussed later. In addition to the uncertainty associated with the ellipsometer results, there is also ambiguity in step measurements on etched oxides because a grainy layer appears to remain on the surface after chemical etching in any of several different etching solutions (e.g., NH_4OH and NH_4F). This layer could either be an arsenic-rich region which is not soluble in the etchants used or a chemically-unstable $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ surface. Preliminary indications are that the observed graininess is due to an unstable surface following etching in solutions which remove the dielectric. The surface can be readily re-stabilized, however, with a suitable chemical treatment such as a short dip in $H_2SO_4:H_2O_2:H_2O$. Development of chemical etching technology for these dielectrics is continuing (under a company-sponsored IR&D program), and a brief summary of the present results is given in Appendix A.

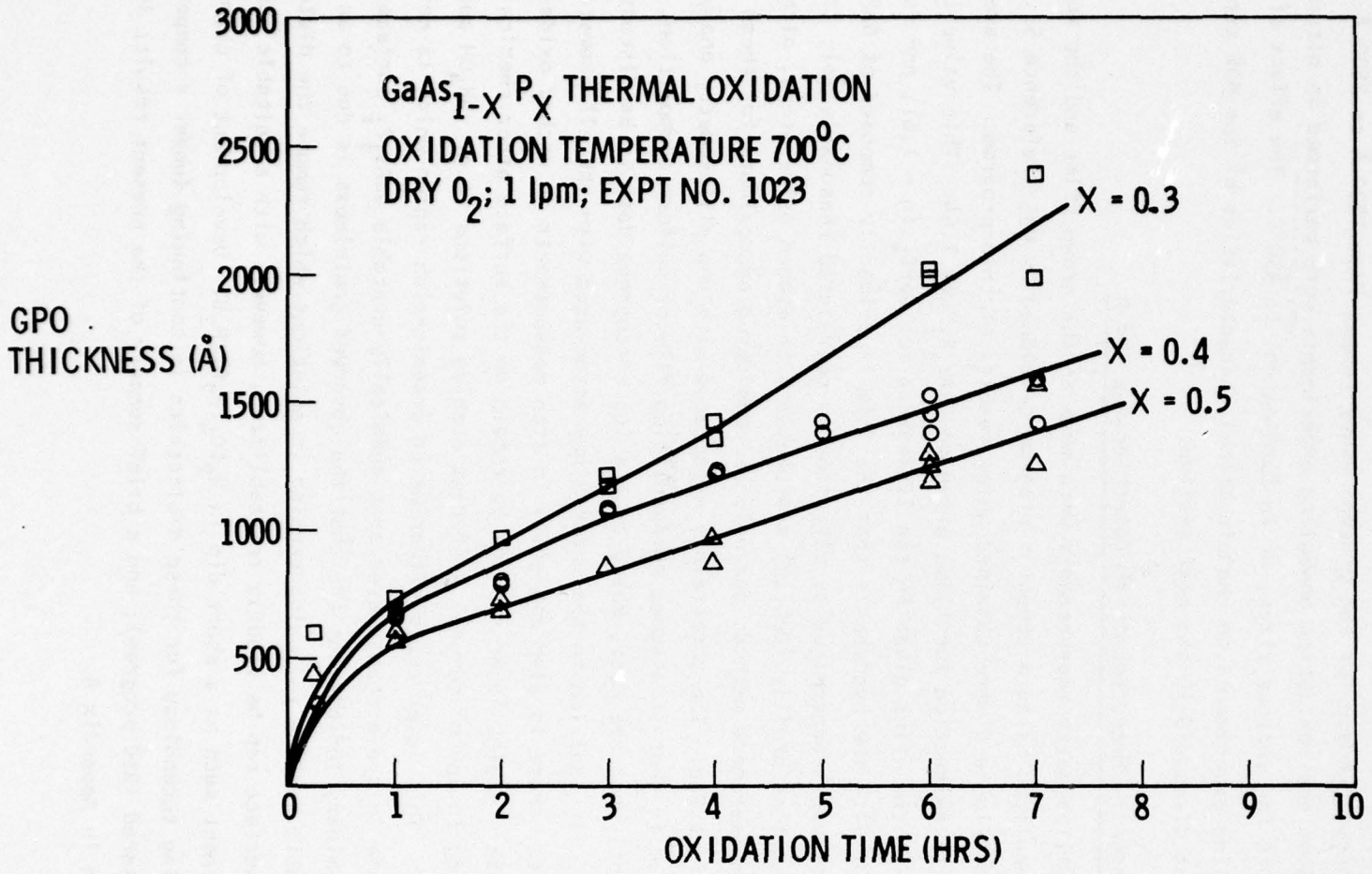

Figure 5. Gallium-Phosphate-Oxide Growth Curves for 700°C Dry Oxidation (from Reference 4)

Schottky diodes were fabricated on the oxidized and etched surface to determine the redistribution of dopant during the thermal oxidation step. A plot of $1/C^2$ versus V (Figure 6) indicates a slight depletion of impurity at the surface from 1.55×10^{17} cm^{-3} in the semiconductor bulk to about 1.3×10^{17} cm^{-3} at the semiconductor surface.

Oxide Compositional Analysis

Compositional analysis of the dielectric grown over $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ was made using an ion microprobe mass analyzer (IMMA).* Basically, this apparatus uses the SIMS (secondary ion mass spectroscopy) technique for analyzing small areas (beam diameters from <2 μm to 500 μm). In this technique a beam of 20 KeV $^{18}O_2^+$ ions is used to bombard the sample, causing sputtering of ions from the surface. These secondary sputtered ions are then mass analyzed and detected using a quadrupole mass filter. Continuous sputtering and detection thus provides an elemental depth profile into the sample.

Figures 7 and 8 are elemental profile data for the $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ starting material and for a sample oxidized for 370 minutes, respectively. These figures represent raw IMMA data, with the logarithm of detector count plotted as a function of sputtering time. To determine actual elemental concentration as a function of depth into the sample certain correction factors must be applied to the raw data (Reference 6). These corrections include factors relating to the sensitivity of the mass detector to different elements, and to the relative sputtering efficiencies of the various elements in a given substrate matrix. In addition, sputtering rates through non-uniform samples may vary with depth. Because these corrections have not yet been determined for the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ material system, it is only possible to obtain qualitative information about the compositional depth profile.

Figure 8 shows that the grown GPO film is composed of two distinct regions. The region near the surface (Region I) is arsenic deficient, as expected for film growth at a temperature of 700°C. The arsenic-rich region (Region II) near the interface with the semiconductor is similar to that

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*Applied Research Labs IMMA operated by the Aerospace Corporation, El Segundo, CA.

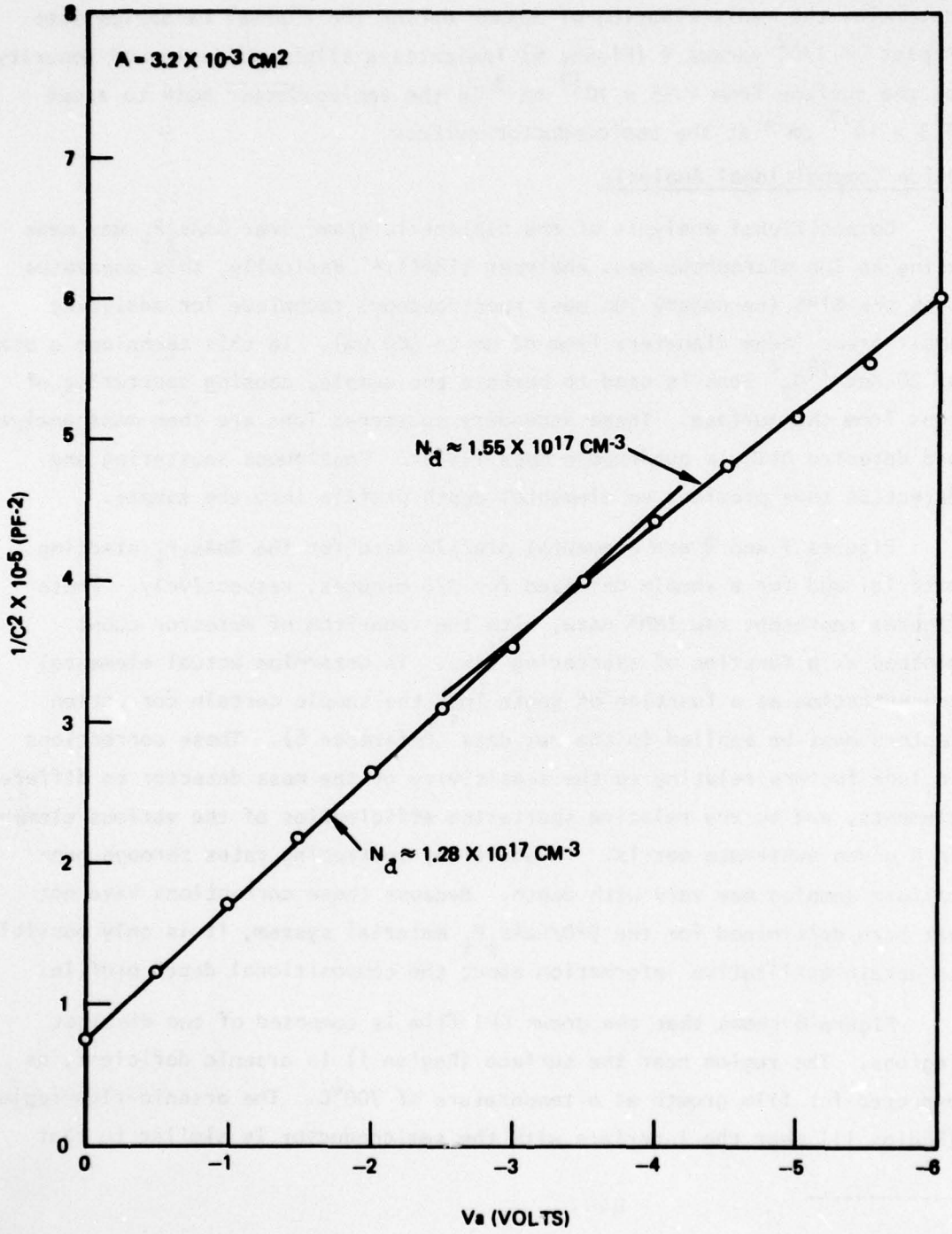

Figure 6. $1/C^2$ vs V for Al-$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Schottky Diode Oxidized and Etched Surface

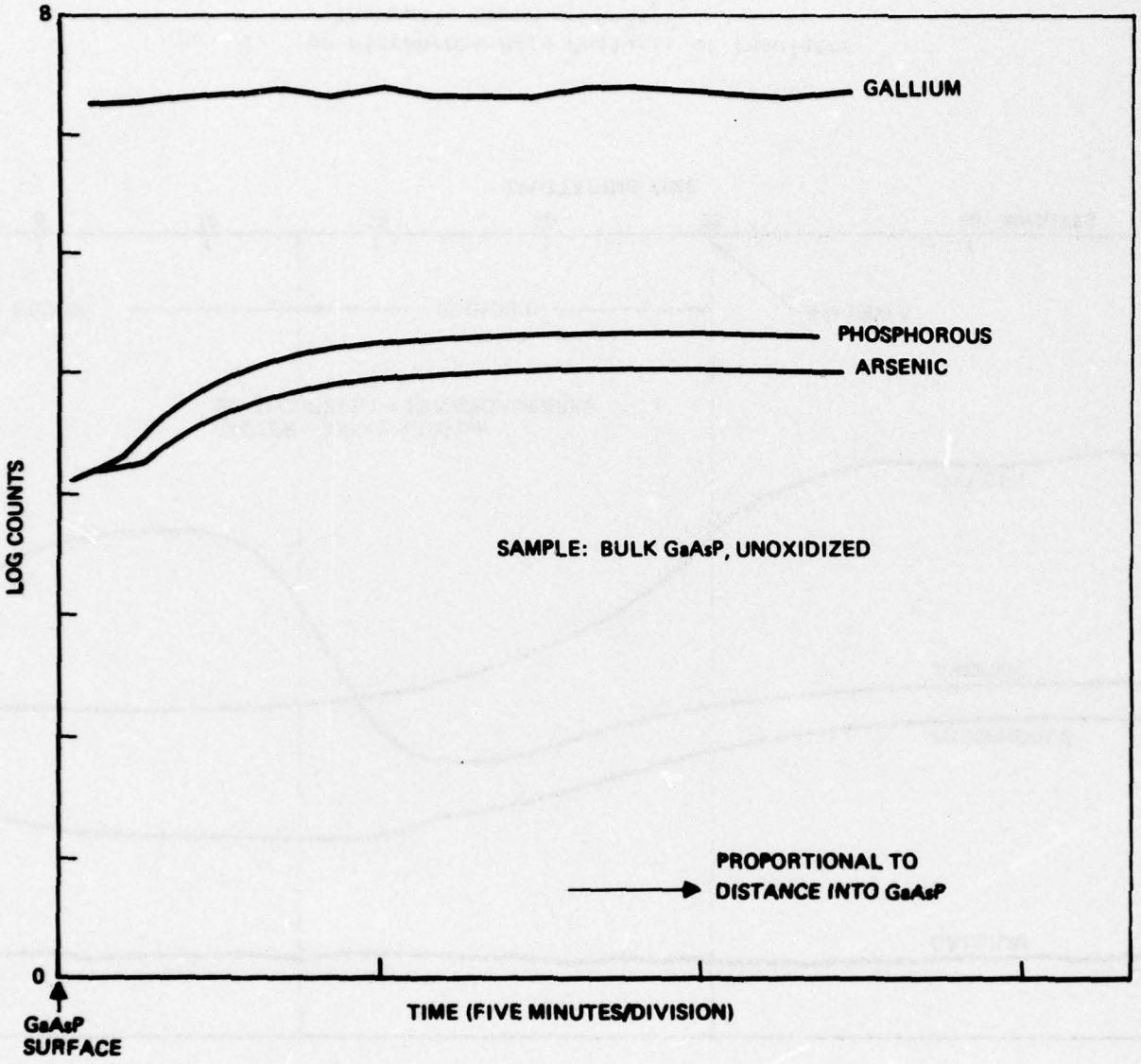

Figure 7. Ion Microprobe Mass Analyzer data showing element concentrations for a GaAsP sample prior to thermal oxidation. This is uncorrected experimental IMMA data, i.e., relative sensitivity factors have not been applied.

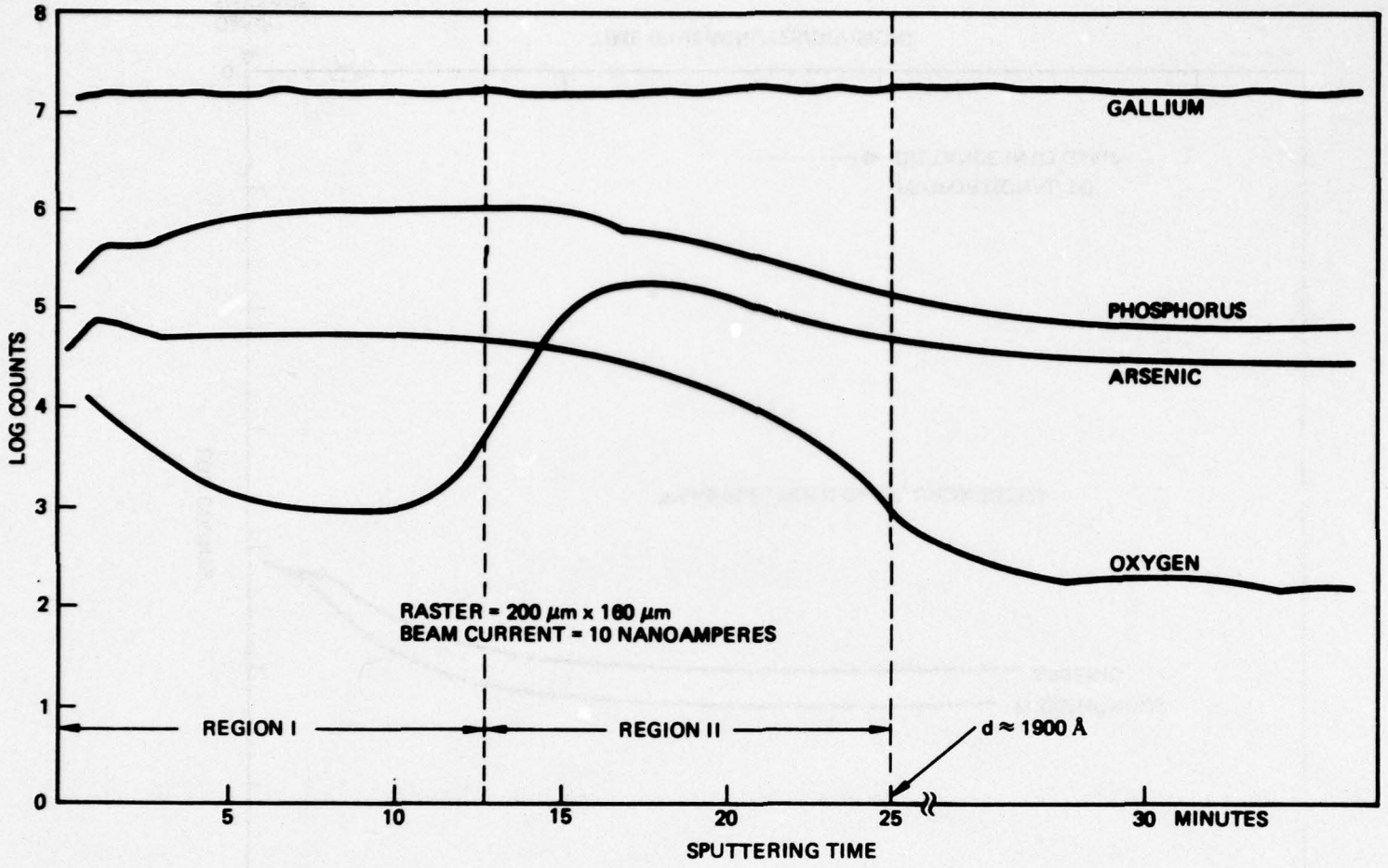

Figure 8. Ion Microprobe Mass Analysis of Insulator Thermally Grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$

observed in oxides grown on GaAs (Reference 7), and may be due to trapped As_2, As_2O_3, As_2O_5, or to the formation of $GaAsO_4$. The constant phosphorus and oxygen in bulk of insulator is taken as further evidence that gallium phosphate is the major constituent, because all other oxides of phosphorus are volatile at the growth temperature of 700°C.

MOS Capacitor Fabrication

MOS capacitors were formed on the samples by vacuum evaporation of aluminum through a metal shadow mask. The gate electrodes were squares with sides nominally 650 μm in length. However, due to an unavoidable bowing of the shadow mask during evaporation, the gate areas were variable, and each device analyzed was measured with a Filar microscope attachment to determine exact values.

Residual oxide formed on the GaAs substrate during oxidation was removed by lapping and indium was then soldered and pulse-alloyed to form ohmic substrate contacts. The pulsing technique for ohmic contact formation alloys through localized heating and avoids possible deleterious interface effects associated with a sintering step. A cross-section of the completed GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS structure is shown in Figure 9.

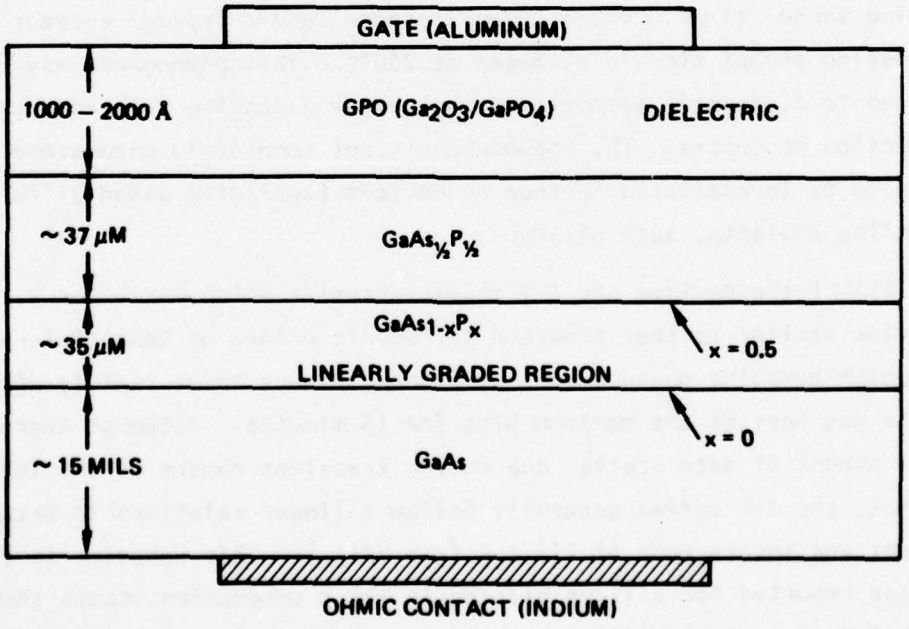

Figure 9. GPO/GaAsP MOS Capacitor Structure

III. GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS CAPACITOR ELECTRICAL CHARACTERISTICS

This section discusses the electrical and interface characteristics of $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS capacitors fabricated with a thermally grown Gallium-Phosphate-Oxide dielectric. The current-voltage characteristics of the dielectric are described, as well as the a-c capacitance and conductance versus voltage characteristics. Finally, some comments are made regarding the analysis of III-V compound MOS structures.

Dielectric Current-Voltage and Breakdown Characteristics

Measurements of d-c leakage current were used as a means for evaluating the film quality before a more detailed interface characterization was made. Leakage measurements were made using a shielded probe and a Keithley Mode 610C electrometer in the fast feedback mode.

As was mentioned in the previous section, several different post-oxidation anneal variations were made in an effort to determine the effects of fabrication procedures on leakage current and interface properties. Figure 10 is a plot of the current-voltage characteristics of capacitors with dielectric films grown during the same oxidation run, but which had varying anneal times. There is an increase in d-c leakage current with increasing anneal time in nitrogen at 700°C. This phenomenon may be related to dielectric composition changes or annealing related changes in conduction processes. The phenomenon is not completely understood, and needs to be investigated further on devices fabricated using different annealing ambients, such as argon.

All of the devices had I-V characteristics which exhibited a transient behavior similar to that reported for anodic oxides on GaAs (Reference 8). The point-by-point measurements of Figure 10 were taken rapidly after the sample was kept at the maximum bias for 15 minutes. Although there is a small amount of data scatter due to the transient nature of the leakage current, the I-V curves generally follow a linear relationship between log current and square root of field ξ ($\xi = V/t_{ox}$). This behavior is similar to that reported for silicon nitride in which conduction occurs through Frenkel-Poole emission (field-enhanced thermal excitation) of electrons from coulombic-type traps. Plasma-grown oxides on GaAs have also exhibited this type of characteristic (Reference 9).

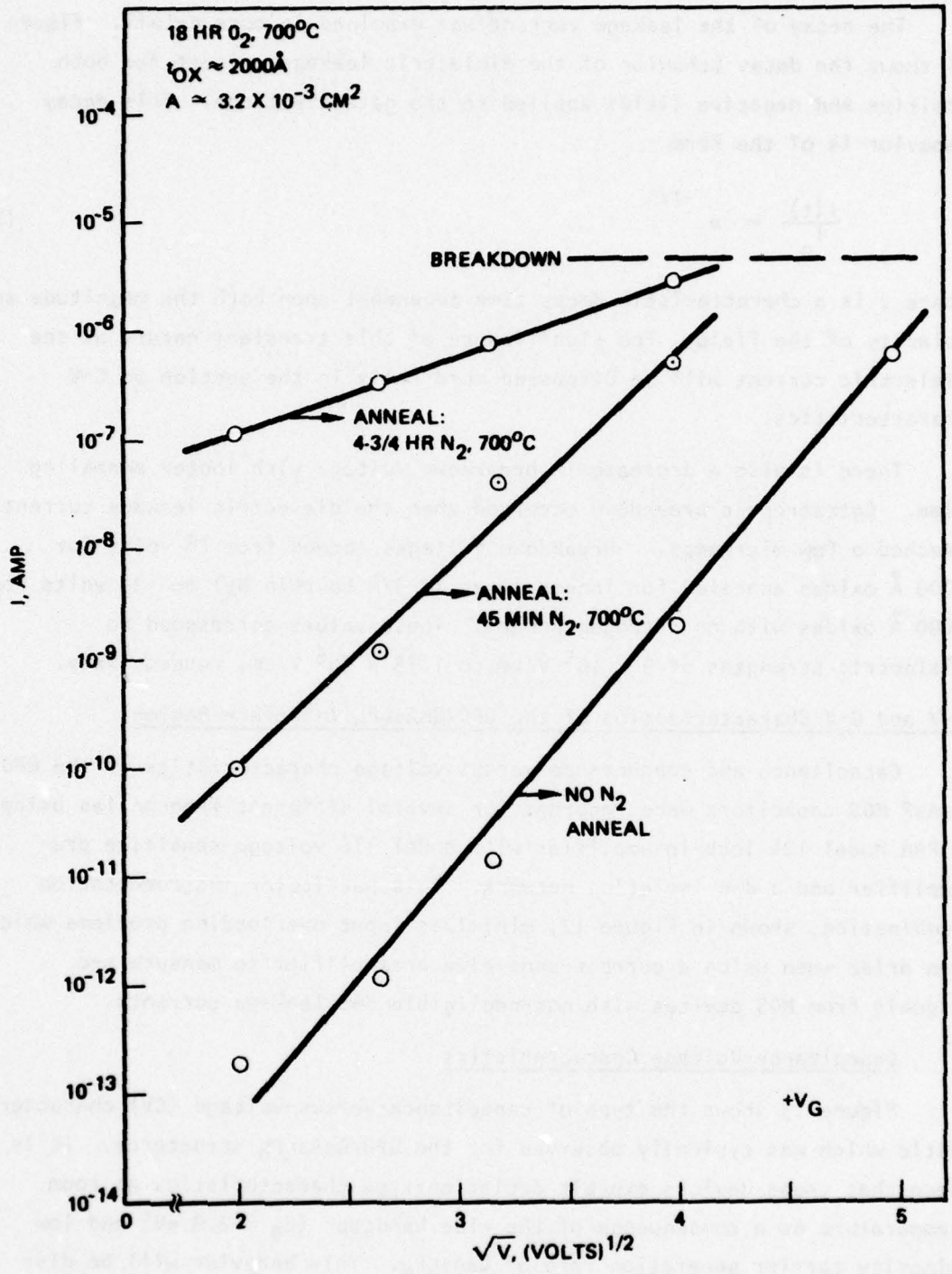

Figure 10. Current-Voltage Characteristics of GPO/GaAs$_{1-x}$P$_x$ Capacitors Fabricated with Various Annealing Procedures (V_G = +)

The decay of the leakage current was examined in more detail. Figure 11 shows the decay behavior of the dielectric leakage current for both positive and negative fields applied to the gate electrode. This decay behavior is of the form

$$\frac{I(t)}{I_o} \propto e^{-t/\tau} \qquad (1)$$

where τ is a characteristic decay time dependent upon both the magnitude and polarity of the field. The significance of this transient nature of the dielectric current will be discussed more fully in the section on C-V characteristics.

There is also a decrease in breakdown voltage with longer annealing time. Catastrophic breakdown occurred when the dielectric leakage current reached a few microamps. Breakdown voltages ranged from 18 volts for 2000 Å oxides annealed for longer times (4-3/4 hours in N_2) to ~35 volts for 2000 Å oxides with no nitrogen anneal. These values correspond to dielectric strengths of 9×10^5 V/cm to 1.75×10^6 V/cm, respectively.

C-V and G-V Characterization of the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Interface Region

Capacitance and conductance versus voltage characteristics of the GPO/GaAsP MOS capacitors were recorded for several different frequencies using a PAR Model 124 lock-in amplifier with Model 116 voltage-sensitive preamplifier and a d-c isolation network. This particular instrumentation combination, shown in Figure 12, minimizes input overloading problems which can arise when using a current-sensitive preamplifier to measure a-c signals from MOS devices with non-negligible d-c leakage currents.

Capacitance-Voltage Characteristics

Figure 13 shows the type of capacitance-versus-voltage (CV) characteristic which was typically observed for the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ structures. It is seen that these devices exhibit depletion-type characteristics at room temperature as a consequence of the wide bandgap (E_g = 2.0 eV) and low minority carrier generation rate of $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$. This behavior will be discussed in more detail in a later section.

The C-V characteristic of Figure 13 also illustrates a hysteresis effect which was observed when the devices were tested in the dark. Also shown in Figure 13 is the effect of an intense microscope light in removing

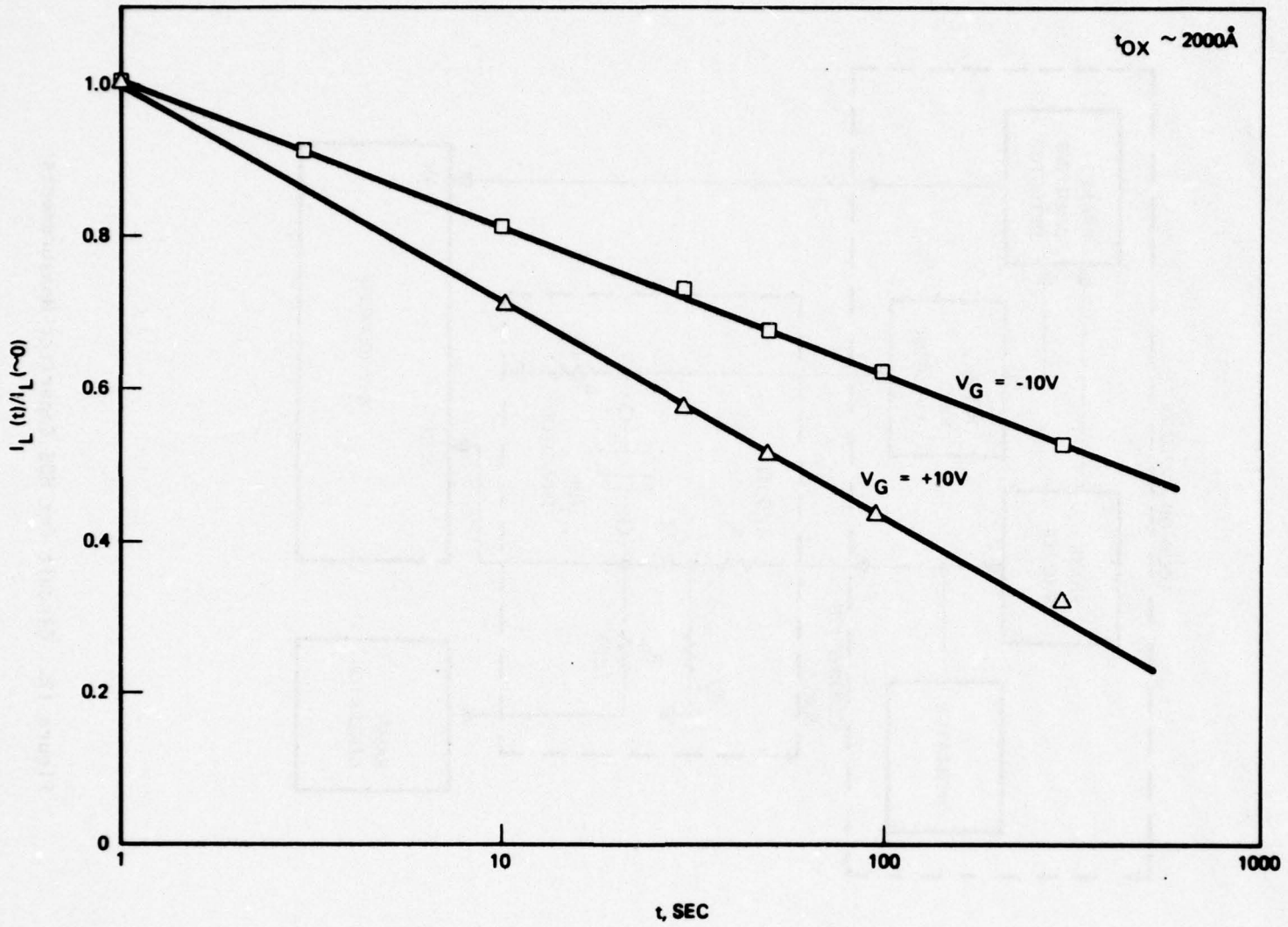

Figure 11. Decay Behavior of Dielectric Leakage Current

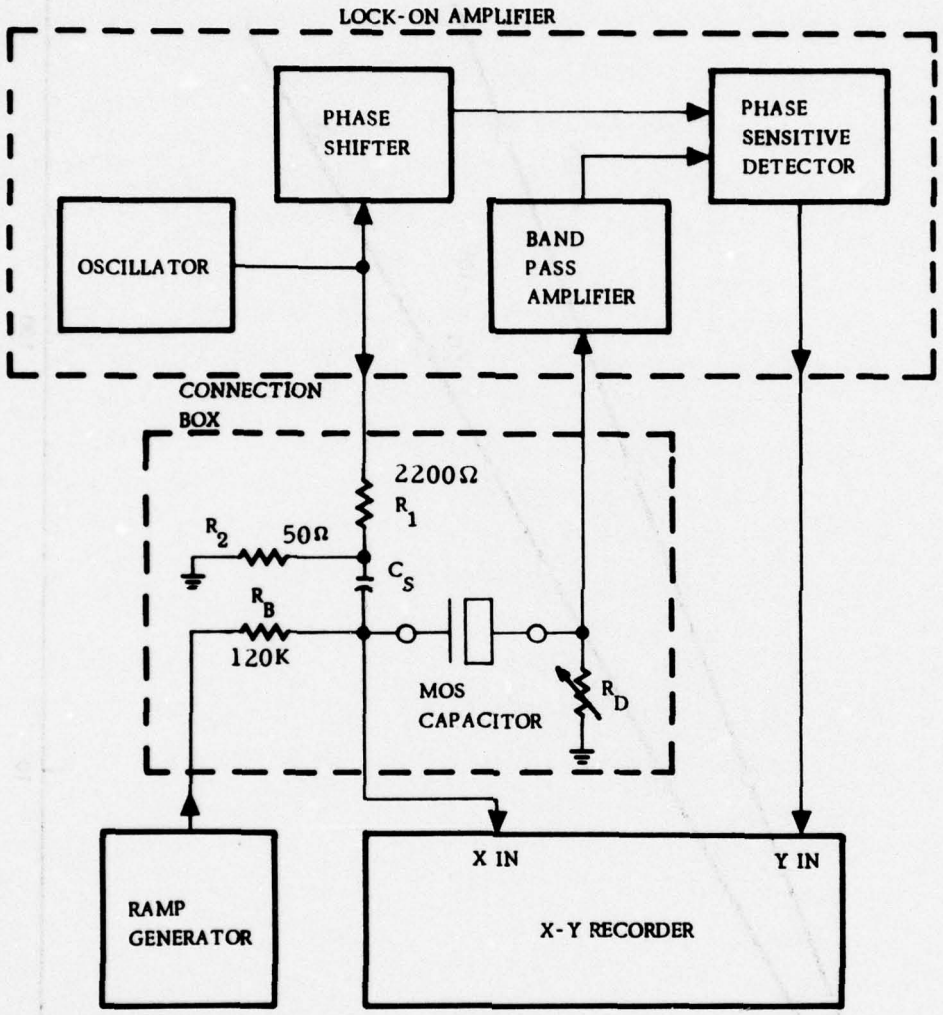

Figure 12. Circuit for MOS Capacitor Measurements

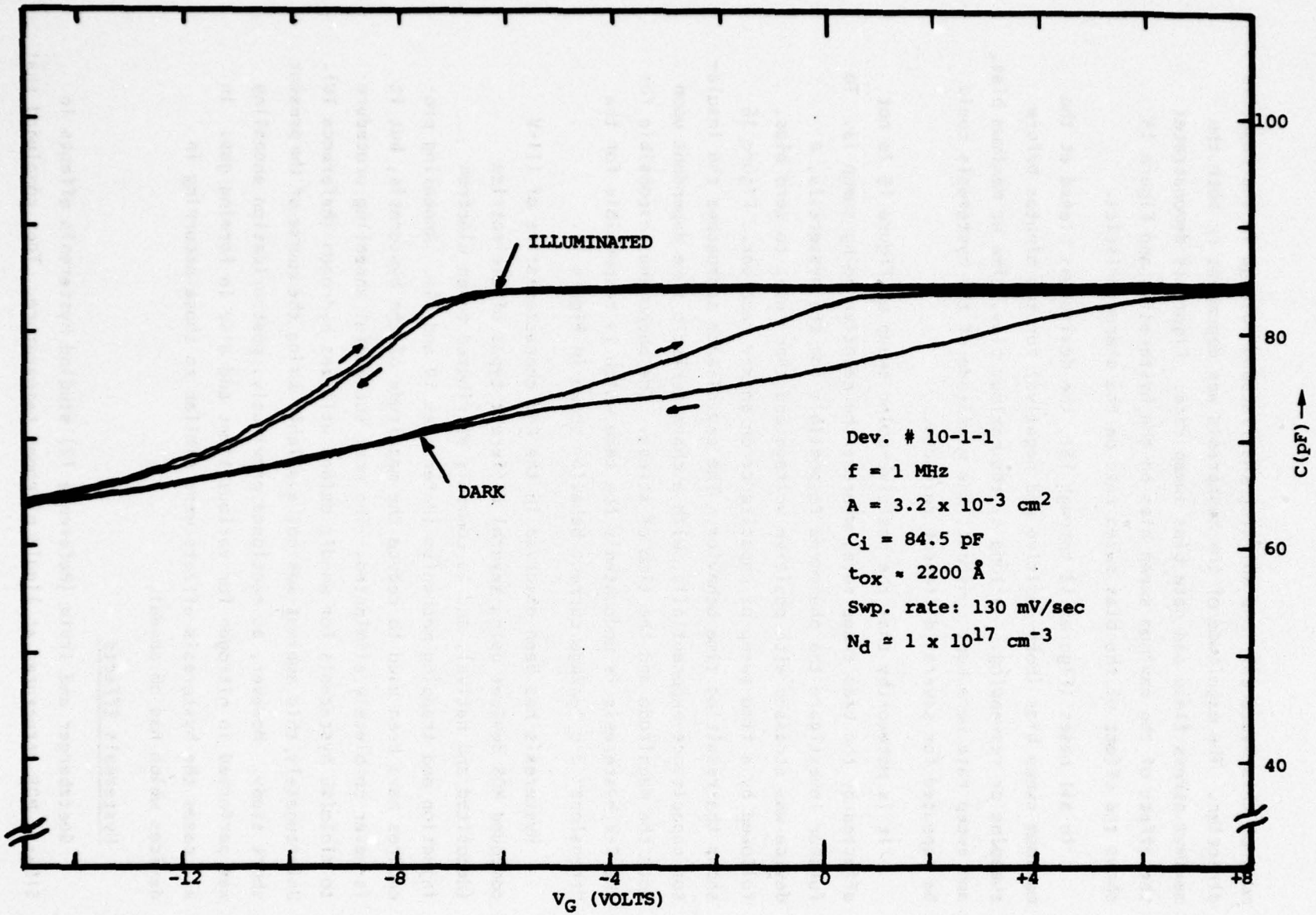

Figure 13. Capacitance-versus-Voltage Characteristic of GPO/ $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS Structure

most of this hysteresis and shifting the flatband voltage in the negative direction. The magnitude of the hysteresis was dependent on both the maximum stress field and gate bias sweep rate. Figure 14 demonstrates the effect of the maximum sweep bias on the hysteresis, and Figure 15 shows the effect of the bias sweep rate on the characteristics.

In all cases (Figures 13 through 15), the device was biased at the maximum sweep bias (both positive and negative) for two minutes before sweeping or resweeping. As long as the maximum bias, time at maximum bias, and sweep rate were kept constant, the magnitude of the hysteresis could be repeated for several different retraces.

It is noteworthy that the positive-going sweep of Figure 15 is not affected by the bias sweep rate, whereas the negative-going sweep is. To further investigate the phenomena responsible for the hysteresis, a device was stressed with positive voltage and then reset to zero bias, followed by a time sweep of capacitance on an x-y recorder. Figure 16 shows the resulting time behavior. The capacitance approaches the insulator capacitance exponentially, with a characteristic time dependent upon both the magnitude and the time of stress. The phenomena responsible for the C-V hysteresis is undoubtedly the same which is responsible for the "transient" d-c leakage current behavior shown in Figure 11.

Hysteresis has been observed in the C-V characteristics of III-V compound MOS devices using several different types of dielectrics (deposited and native), and is commonly attributed to an electron injection and trapping mechanism (References 10 and 11). Annealing procedures have been used to reduce the magnitude of the hysteresis, but it is never completely eliminated. The most successful annealing procedure to minimize hysteresis for anodic oxides utilizes hydrogen (Reference 10). Unfortunately, this ambient was not available during the course of the present short study. However, as mentioned previously, post-oxidation annealing was performed in nitrogen for various times and also in forming gas. In all cases the hysteresis effects were similar to those occurring in devices which had no anneal.

Hysteresis Effects

Goetzberger and Irvin (Reference 12) studied hysteresis effects in SiO_2-Si MOS structures at liquid nitrogen temperature. They concluded that

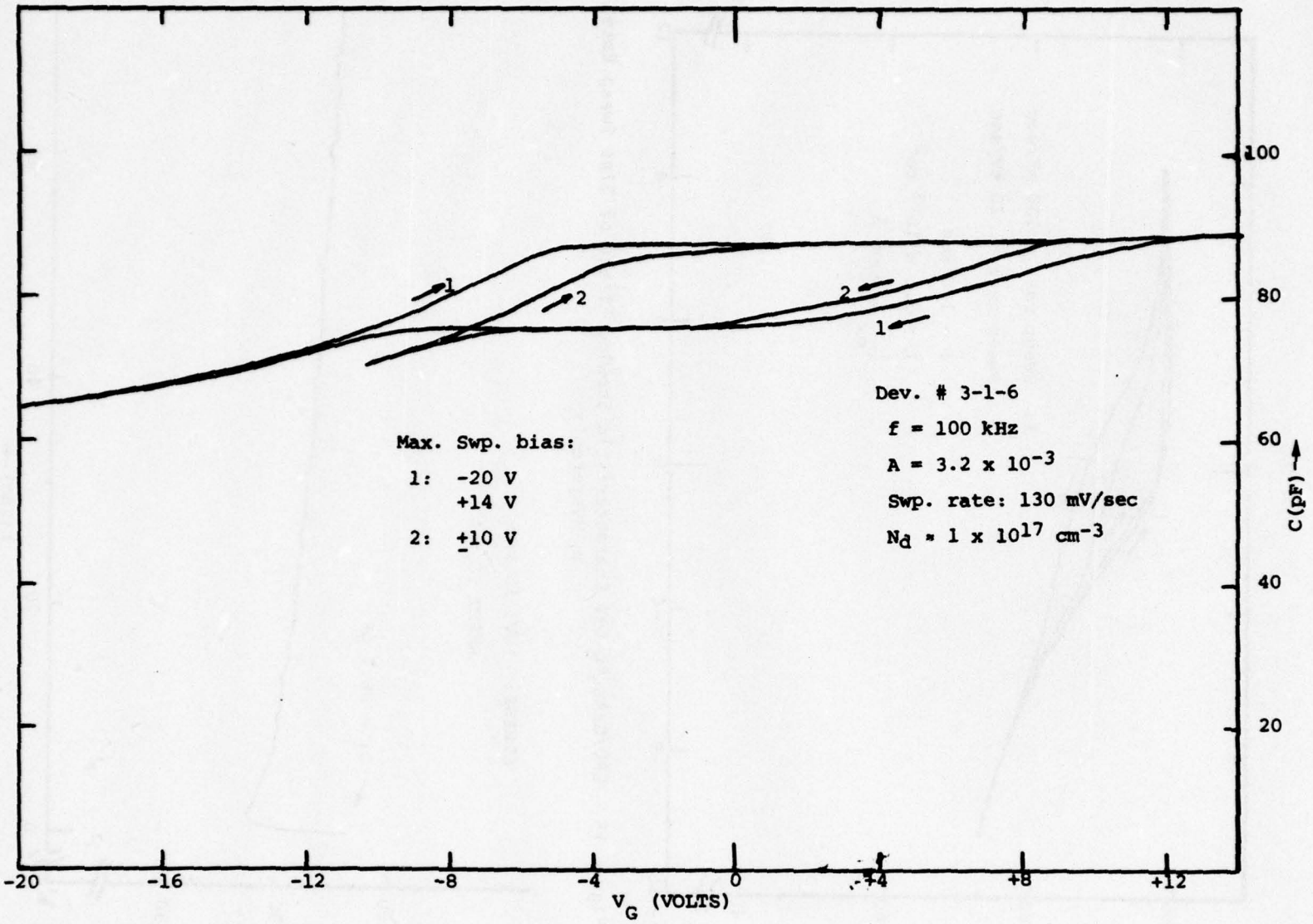

Figure 14. GPO/GaAs$_{\frac{1}{2}}$P$_{\frac{1}{2}}$ C-V Characteristics Showing Effect of Maximum Sweep Bias on Hysteresis

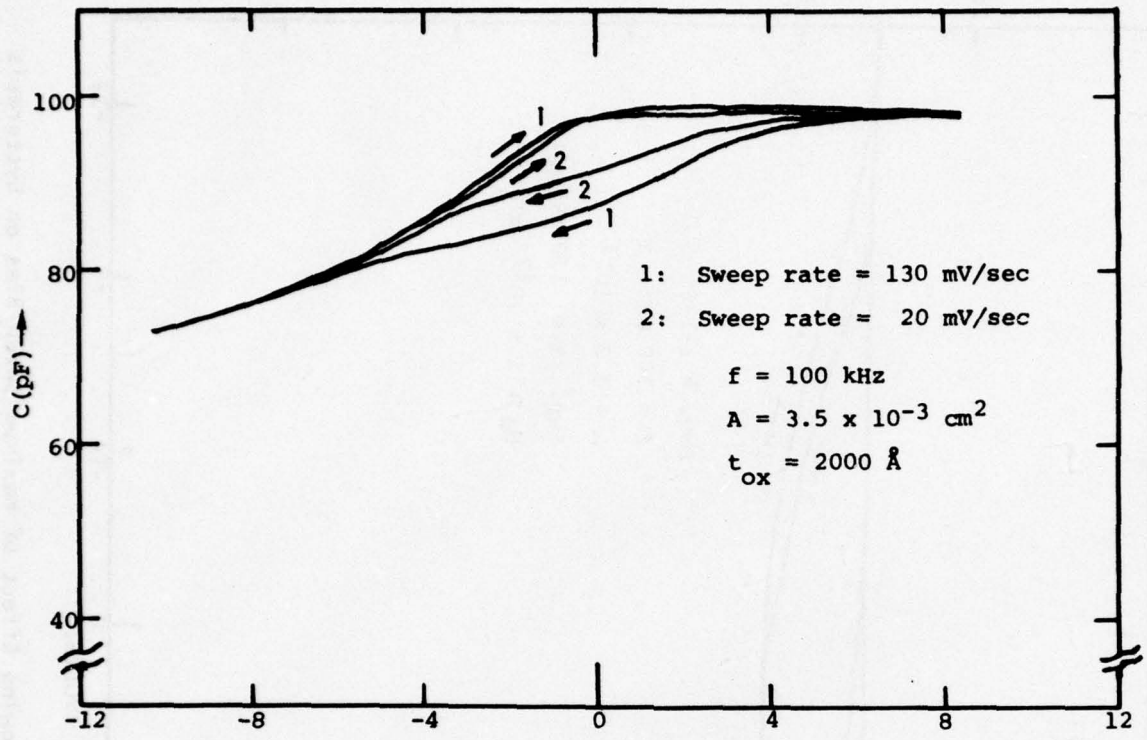

Figure 15. GPO/GaAs$_{½}$P$_{½}$ C-V Characteristic Showing Effect of Bias Sweep Rate on Hysteresis

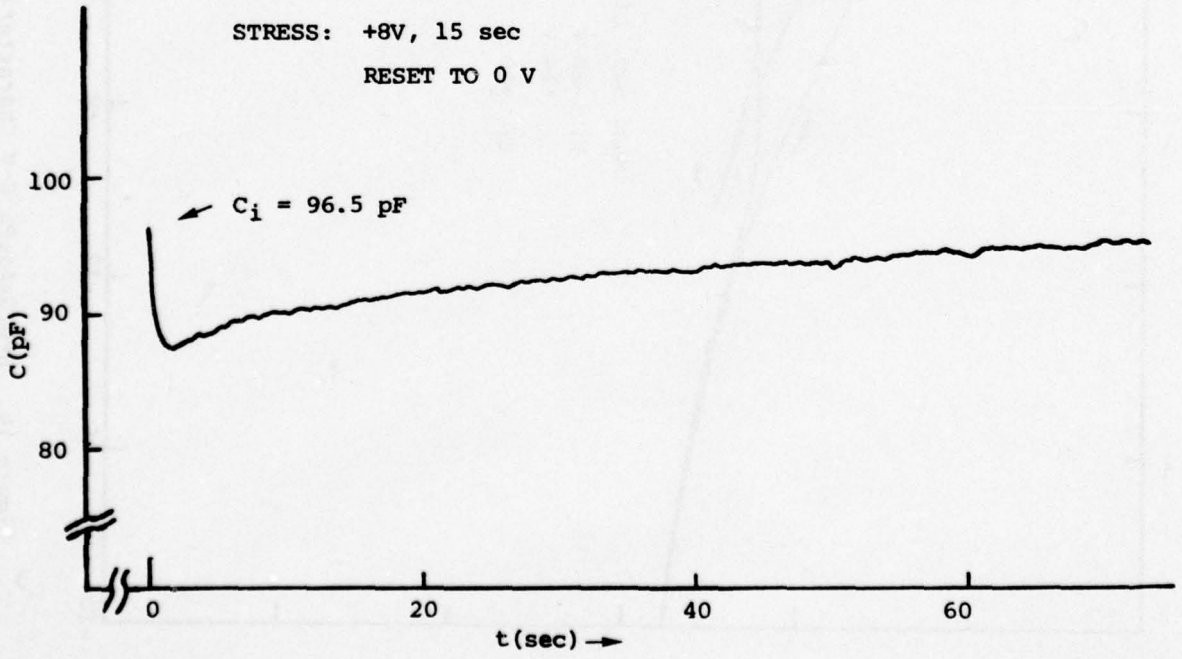

Figure 16. Zero-Bias Capacitance as a Function of Time Following Positive-Bias Stress

the hysteresis in devices with available minority carriers (e.g., inverted surfaces) was due to the fact that charge exchange in all interface states except those close to the band edges can occur only by capture of free carriers because emission rates are very low at 77°K.

As shown in the band diagram of Figure 17, there are three regions of surface state response. States near the band edges are able to emit electrons or holes and thus can follow a change in bias. Based on recombination generation statistics, the capture time constant for electrons by states is of the form

$$\tau_c = \frac{1}{c_n n_s} \tag{2}$$

where c_n is a constant and n_s is the free electron density at the surface. It is seen that the capture time constant is determined by the surface concentration of carriers.

The emission time constant of the traps is given by

$$\tau_e = \frac{e^{-(E_T/kT)}}{c_n n_i} \tag{3}$$

where E_T = energy of the interface state level and n_i is intrinsic carrier concentration. Similar expressions exist for hole capture and emission.

For a given temperature and semiconductor (i.e., n_i), there is a limiting state energy (E_n and E_p in Figure 17) beyond which states are unable to follow the d-c voltage variation because their emission rate is too low. When this occurs, hysteresis will be present in the C-V characteristics. It is believed that a similar type reasoning applies in the present case of a wide bandgap semiconductor ($GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$) where the minority carrier generation rate is low at room temperature. For the sake of illustration only, assume thermal equilibrium exists at room temperature (such is probably not the case) and assume a majority carrier (doping) concentration of 1×10^{17} cm^{-3} and intrinsic carrier concentration for $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ of 10^3 cm^{-3} (Reference 2). Using the well-known relation

$$n_i^2 = p\,n$$

which is valid in the case of thermal equilibrium, a minority carrier (hole) concentration of $p = 10^{-11}$ cm^{-3} is obtained. Such a number is

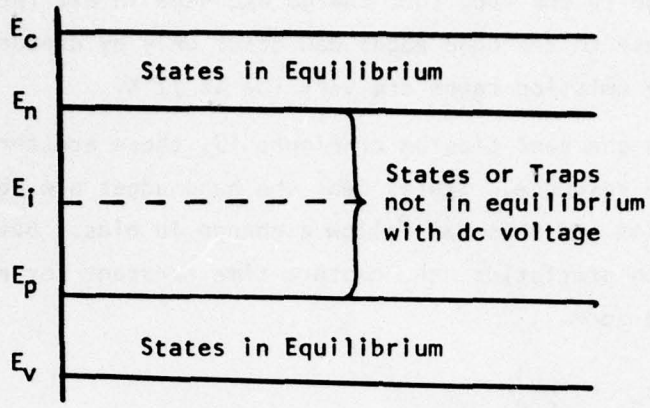

Figure 17. Band Diagram Showing Regions of State Response. States above E_n can stay in equilibrium by electron emission, and those below E_p by hole emission. States in the midgap region exchange charge only by capture.

statistically meaningless, of course, but it illustrates that the minority carrier concentration is very small in a wide bandgap semiconductor at room temperature. Therefore, the effects of minority carriers can be neglected in $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$.

When positive bias is applied to the MOS structure, majority carriers (electrons) accumulate at the interface, and traps or states are filled by a capture process governed by Equation (2). As the interface is depleted of electrons, these traps remain filled until they are emptied by some thermal or optical process. If the emission of these trapped electrons does not occur at a rate faster than the gate voltage sweep rate, then a hysteresis will be observed in the C-V characteristic. There will exist a time, however (Figure 16), when the trapped electrons are emitted from these states and the hysteresis disappears. If the sweep rate were infinitesimally small, there would be no hysteresis at all.

Because holes do not exist in significant numbers at room temperature in $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$, they cannot charge states or traps even at large negative voltages. (In fact, no inversion layer exists.) This may be the reason that the positive-going sweep of Figure 15 is insensitive to sweep rate. The increase in hysteresis with maximum bias voltage, shown in Figure 14, is due to electron injection and trapping at positive voltage and field-enhanced electron detrapping at negative bias.

The effect of illumination on the device is to generate electron-hole pairs and also to increase the emission rate of trapped carriers. As illustrated in Figure 13, the hysteresis disappears in this case because electrons are now emitted at a rate faster than the sweep rate, and are, therefore, available to follow the bias voltage variation. The negative flatband voltage shift with illumination is apparently due to the emptying of electron traps and states, leaving net positive fixed charge trapping in the oxide. The emptying of states with illumination is apparent in Figure 13 from the increased slope in the depletion region. A comparison of the ideal C-V characteristic with the illuminated curve shows very little interface state effects, as expected. This will be discussed later.

It has been observed (Reference 13) that the lower half of the band-gap in (111) GaAs is free of interface states. It is possible that such may also be the case in (100) $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$, although no direct experimental evidence is available. If such is the case, this nonsymmetric state distribution, in addition to the lack of holes, may explain some of the observed trapping and hysteresis behavior (e.g., Figure 15) of the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ devices.

Conductance-Voltage Characteristics and Frequency Effects

Capacitance and conductance versus voltage characteristics were recorded for frequencies from 100 Hz to 1 MHz. The devices were stress-biased the same in each case to reduce or eliminate ambiguities due to the hysteresis previously discussed. Figure 18 shows the C-V and G-V characteristics for a device at 5 kHz. The C-V characteristics were identical for all frequencies in the range from 100 Hz to 1 MHz. These are similar to results observed on GaP MOS devices (Reference 11). The fact that there is no dispersion in the accumulation regime also indicates that the dielectric probably does not contain a highly conductive region near the interface with the semiconductor (Reference 10).

The lower curve in Figure 18 is a plot of a-c conductance as a function of gate voltage. The increase in conductance beginning at +6 volts is associated with an increase in d-c conductivity in this voltage range. The a-c conductance curve of Figure 18 does not exhibit a well-defined peak with voltage as is usually observed for SiO_2-Si MOS devices.

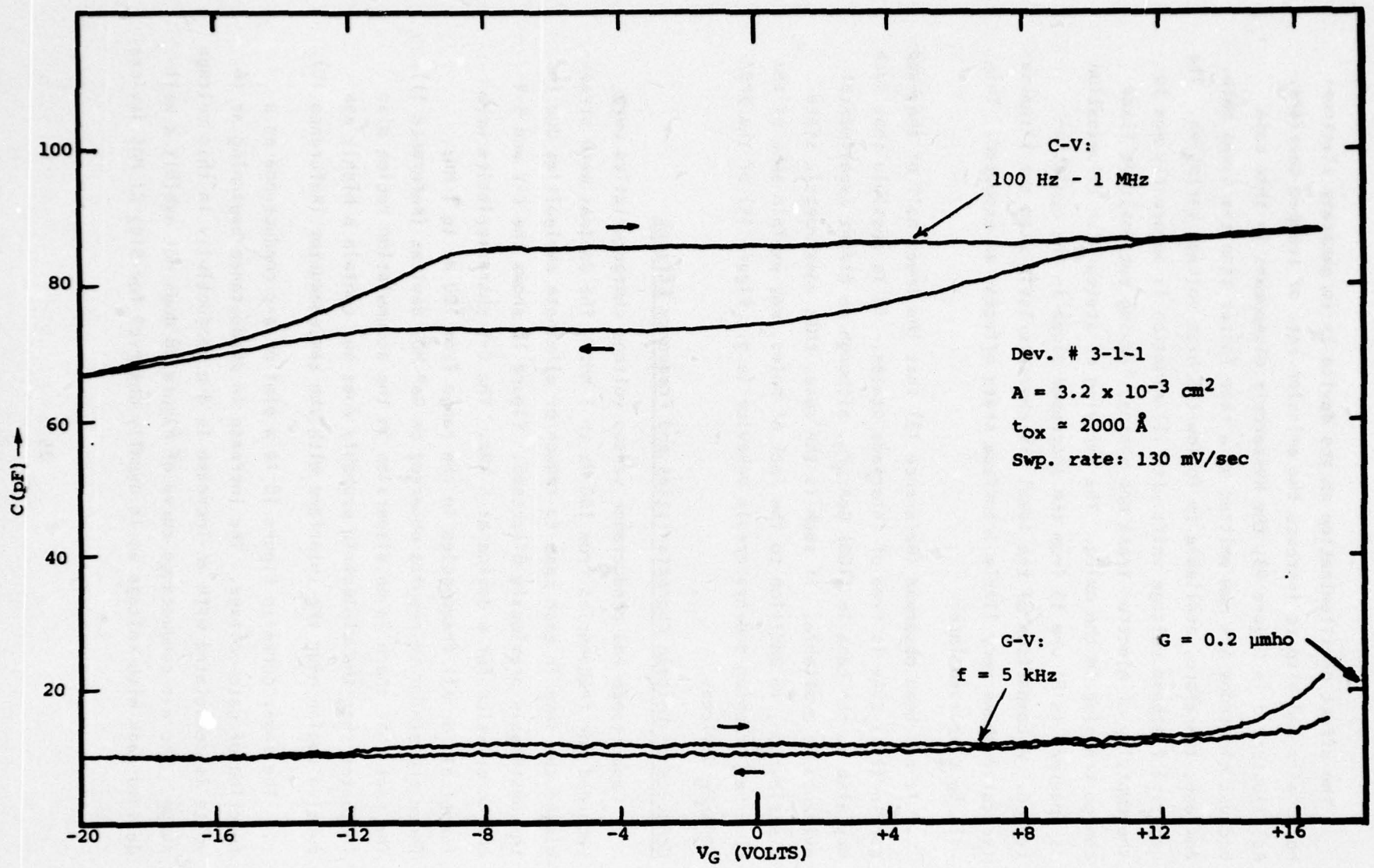

Figure 18. A-C Capacitance and Conductance-Versus-Voltage of GPO/GaAs$_{\frac{1}{2}}$P$_{\frac{1}{2}}$ MOS Device

Interface State Density Determination

It is apparent from the preceding discussion that a determination of interface state density using characteristics of the type shown in Figures 13 through 15 is extremely difficult. The validity of interface state values obtained using conventional analytical techniques, such as the a-c conductance (Nicollian-Goetzberger, Reference 14) and quasi-static (Reference 15), is questionable.

The fact that the C-V characteristics are identical from 100 Hz to 1 MHz suggests that there are almost no interface states which follow the a-c signal in this frequency range.

The nature of the traps causing the C-V hysteresis is not completely understood, but it is informative to compare ideal and experimental characteristics to obtain an idea of the magnitude and energy distribution of the electron traps. Figure 19 is a comparison of the ideal and experimental C-V characteristics from the same device whose C-V is shown in Figure 18. The experimental curves have been shifted along the voltage axis so that flatband voltages coincide with the ideal curve.

The ideal characteristic in Figure 19 was generated by modifying the procedure given in Sze (Reference 16) to neglect minority carrier contributions (for reasons given previously) to the semiconductor space-charge capacitance. This results in a space-charge capacitance of

$$C_{sc} = \sqrt{\frac{\varepsilon_s N_D q^2}{2kT}} \; \frac{(e^{u_s} - 1)}{[e^{u_s} - u_s - 1]^{1/2}} \qquad (4)$$

where

$\varepsilon_s = \varepsilon_{rs} \varepsilon_o = 10.3 \varepsilon_o$ for $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$

N_D = ionized impurity concentration

and

$u_s = \frac{q \psi_s}{kT}$ is the reduced surface potential.

The curve generated for a doping concentration of 9×10^{16} cm^{-3} gave the best fit to the experimental curve measured during illumination of the device. The deviation between the curves at large negative voltage is due to optically generated holes which are contributing to the capacitance.

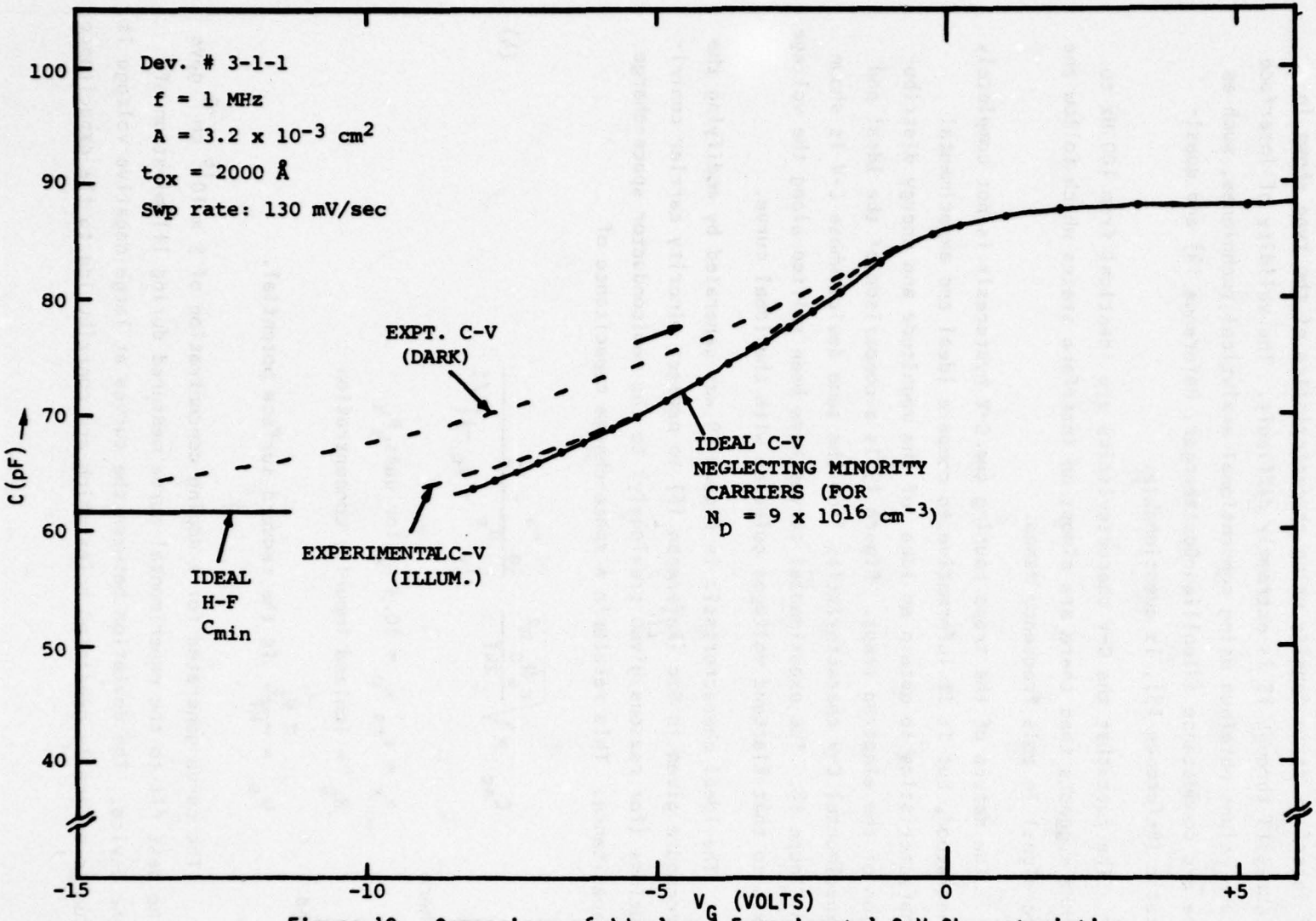

Figure 19. Comparison of Ideal and Experimental C-V Characteristics

illumination empties almost all of the electron traps which depend on surface potential, and results in device characteristics which allow the most appropriate ideal curve to be chosen for comparison with experimental curves generated without illumination. The positive-going sweep of the experimental "dark" curve was chosen for comparison with the ideal curve because traps that are full during sweeping in this direction are not sensitive to the bias sweep rate (see Figure 15). These traps or states represent those levels which can remain in equilibrium with the bias voltage sweep.

A differentiation procedure first suggested by Terman (Reference 17) can be used to approximate the density of interface states or traps. Comparing the ideal and experimental curves of Figure 19, values of the voltage shift, ΔV, versus V are obtained. From these values of ΔV, the charge in the states at a given surface potential can be determined by

$$Q_{ss} = C_i (\Delta V) \quad \text{coul/cm}^2 \tag{5}$$

where C_i = insulator capacitance per area

ΔV = voltage shift between ideal and experimental curves

The density of states is then obtained by graphical differentiation;

$$N_{ss} = \frac{1}{q} \left(\frac{\partial Q_{ss}}{\partial \psi_s} \right) \text{ states/cm}^2\text{/eV} \tag{6}$$

where ψ_s is the surface potential in volts. Figure 20 is a plot of approximate state density as a function of energy in the upper portion of the bandgap for the experimental curve of Figure 19. The estimated values of the density average about 7.5×10^{11} $cm^{-2} - eV^{-1}$. Although this particular technique for determining state density is subject to many limitations and uncertainties (Reference 18), it provides a good approximation for state densities above about 5×10^{11} $cm^{-2} - eV^{-1}$. A possible source of error using this method is the presence of interface potential fluctuations caused by trapped oxide charge. These fluctuations tend to overestimate the density.

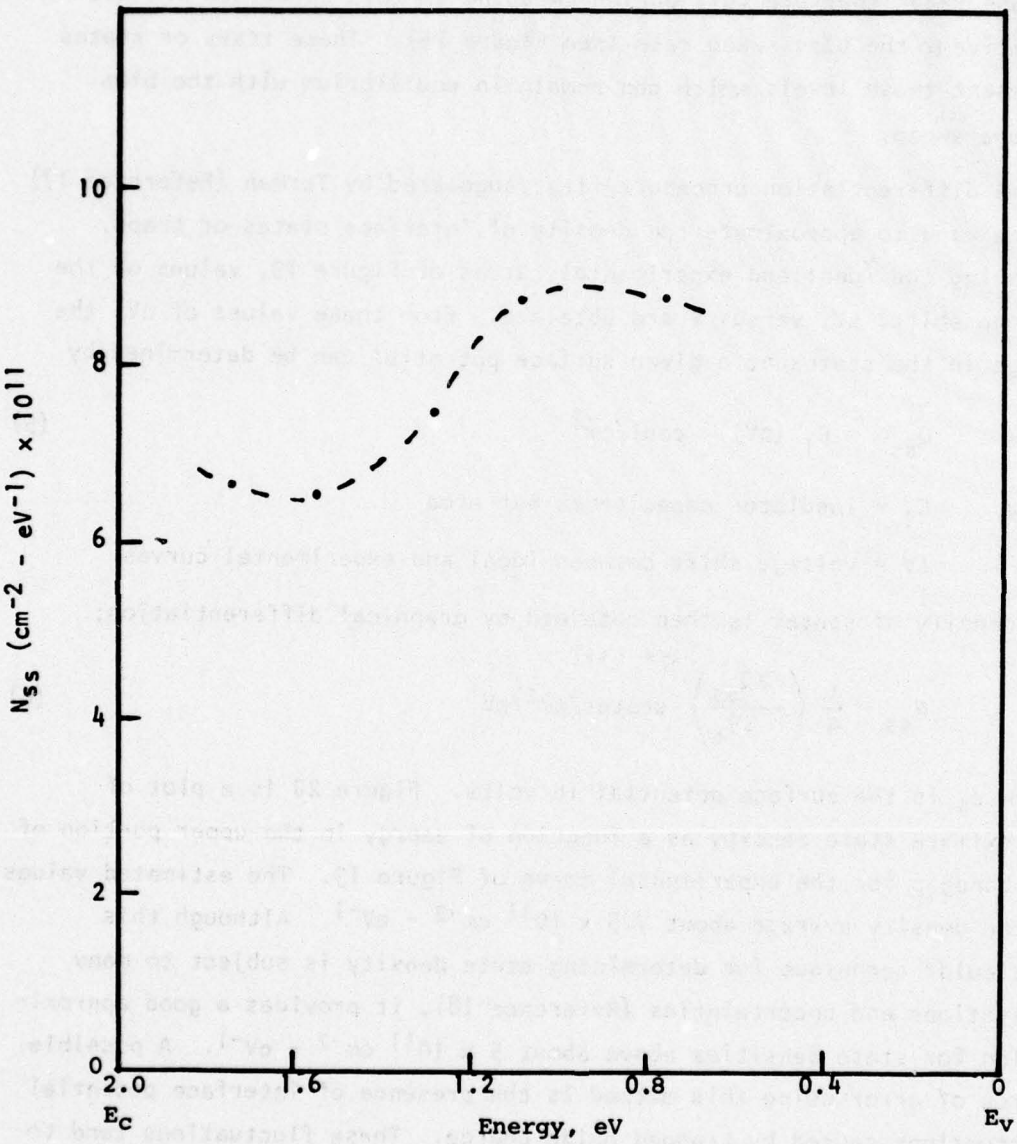

Figure 20. Approximate Interface Trap Density Versus Energy

An attempt was made to apply the a-c conductance analysis technique (Reference 14) to the experimental G-V data using an MOS capacitor equivalent circuit which includes the effects of oxide leakage and substrate resistance. The equivalent parallel interface state conductance was then extracted from the measured conductance values. Plots of G_p/ω versus ω (Figure 21) did not yield definable peaks as in SiO_2-Si devices, but resulted in a dip in the curve at about 1 kHz. This plot is also different in shape from those which have resulted for Si_3N_4-GaAs devices in which electron trapping effects predominated (Reference 19). It is not possible to accurately determine interface trap density from Figure 21, because existing models (References 14 and 19) do not explain the behavior of the data. Other effects, such as dielectric leakage current, may affect the measured a-c conductance values. It is apparent that further investigations need to be undertaken to provide an adequate understanding of these problems.

Dielectric Constant

The static dielectric constant of the GPO insulator was determined from the capacitance in the accumulation region of the C-V characteristic. Using this capacitance value and the measured capacitor area and insulator thickness, the dielectric constant (ε_r) of the film ranged from 6.2 to 6.5. This range of dielectric constant is close to that determined for other native oxides on GaAs (References 9 and 11).

The high dielectric constant of these films indicates that thicker oxides can be used to decrease the dielectric leakage current when the GPO is used as an MOS gate insulator.

Bias-Temperature Stability

The effects of bias-temperature stress on these devices was evaluated and the results are shown in Figure 22. The major effect of a negative voltage B-T stress appears to be a change in the nature of the traps responsible for the C-V hysteresis. For positive voltage B-T stress, the hysteresis decreases further but the curve also shifts toward more-positive gate voltage. The direction of this shift is opposite to that expected for positively charged mobile ions and may be due to electron injection and trapping in the oxide during stress.

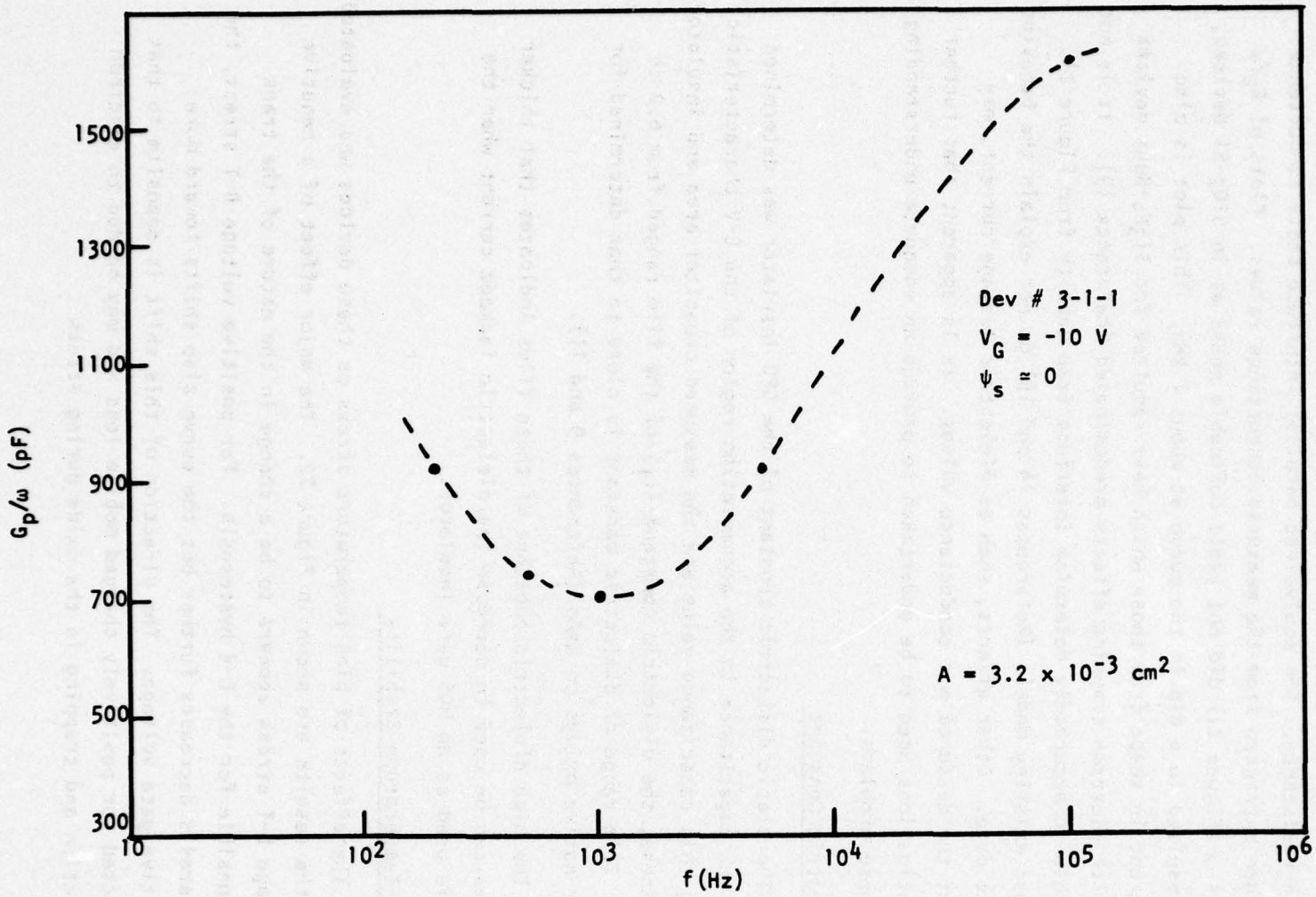

Figure 21. Equivalent Parallel Conductance Versus Frequency

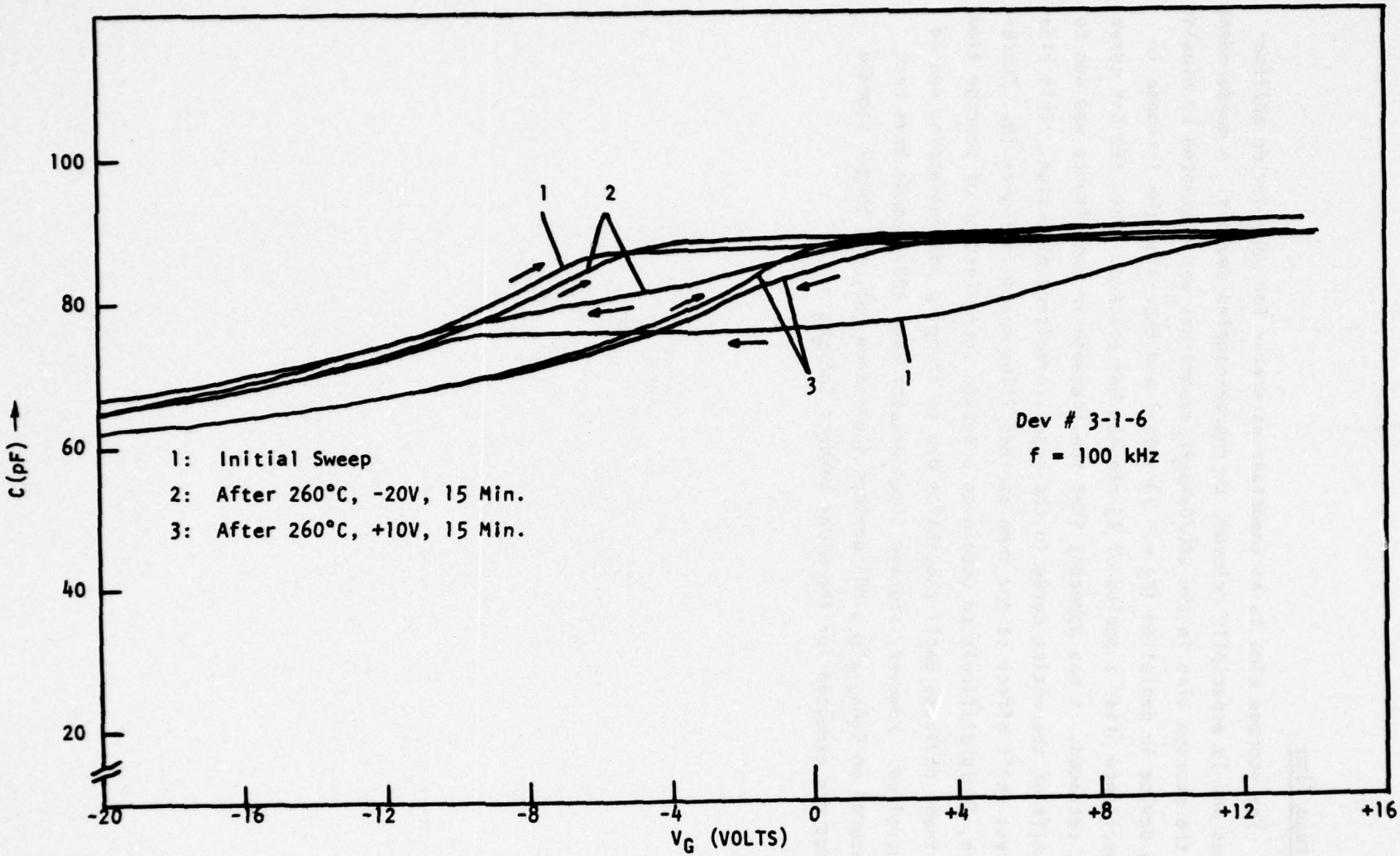

Figure 22. Effect of Bias-Temperature Stress on GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS Capacitors

Storage Time

The storage time is an important parameter for many device applications and is especially relevant to charge-coupled devices. A measurement of the storage time in the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ capacitors was attempted by biasing the device in depletion (V_G = - 20 volts) and observing the increase in capacitance after a period of 15 minutes had elapsed. When the C-V curve was retraced, it was apparent that the increase in capacitance was due to a shift of the entire curve in the negative-voltage direction. This bias-stress shift effect is the same as that illustrated in Figure 14. Therefore, it is difficult to obtain an accurate determination of storage time in these devices, until the shifts due to trapping and detrapping can be controlled. However, storage times greater than 400 seconds have been measured on $GaAs_{0.6}P_{0.4}$ MOS devices (Reference 20), and longer storage times are expected for the wider bandgap $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$.

IV. GaAsP GATE CONTROLLED DESIGN STUDY

This design study establishes the feasibility of fabricating a gate controlled diode for evaluating a key semiconductor parameter--the surface recombination velocity. Appendix B gives technical rationale for the recommended design values.

Surface Recombination Velocity

By definition, s_o is the *surface recombination velocity of a surface without a surface space-charge region* (Appendix B, Reference 1). This definition is compatible with the measurement of $I_{gen,s}$. $I_{gen,s}$ is the reverse-bias current of a gate controlled diode, measured by biasing the gate so that the semiconductor surface transitions between accumulation and depletion, as shown in Figure 23.

The analysis in this study defines the surface recombination velocity as

$$s_o = \frac{2\, I_{gen,s}}{q\, n_i\, A_s}$$

$$s_o = \frac{4.167 \times 10^{14}\, I_{gen,s}}{A_s} \qquad (7)$$

where $[I_{gen,s}]$ = surface generation current as defined in Figure 3 of Appendix B;

$[A_s]$ = area of the depleted substrate under the gate; cm^2

The surface recombination velocity of a semiconductor surface is not an experimental parameter, i.e., s_o cannot be measured directly--both experimental measurements *and* theoretical computation must be used to arrive at a value for s_o.

Gate Controlled Diode Design-Goal Parameter Values

Figure 23 illustrates the concepts defined by this gate controlled diode design. Table I gives design-goal parameter limits for the GaAsP gate controlled diode.

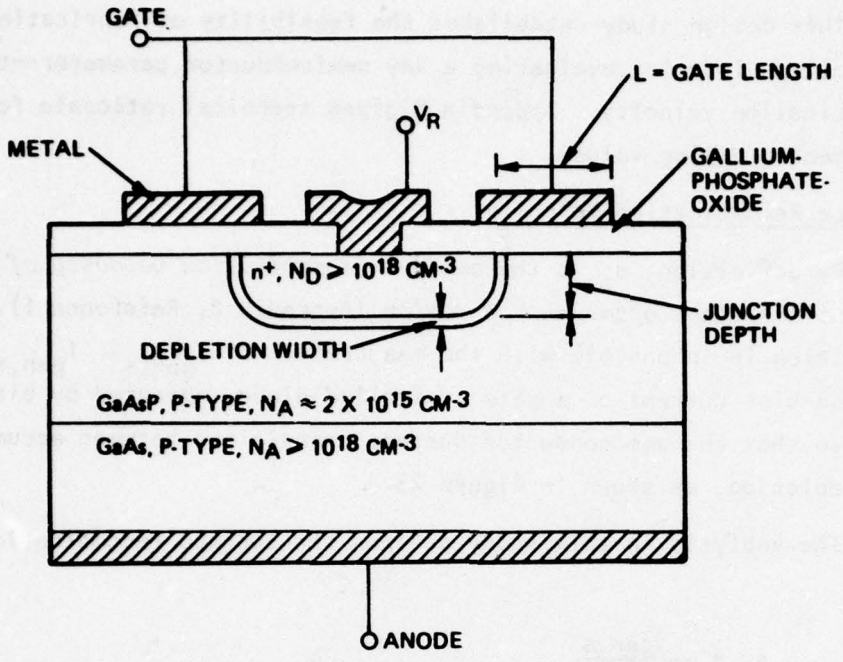

Figure 23. Design of GaAsP Gate Controlled Diode, with Design Target Values

Table 1. GaAsP Gate Controlled Diode Design Goals

PARAMETER	MINIMUM	TARGET	MAXIMUM	UNITS
Doping Concentration				
n^+ implant/diffusion (GaAsP)	1×10^{18}	-	5×10^{18}	cm^{-3}
p-type epi (GaAsP)	1×10^{15}	2×10^{15}	1×10^{16}	cm^{-3}
p^+ substrate (GaAs)	1×10^{18}	-	5×10^{18}	cm^{-3}
Junction Depth	1	4	7	microns
Gate Length = L	-	25	-	microns
Gallium-Phosphate-Oxide Thickness	800	1000	3500	Å
Epi Thickness (must be > L)	12	-	100	microns
Substrate Thickness	250	-	350	microns
Metal Thickness	7000	10,000	12,000	Å

Evaluation of the Effectiveness of GPO-GaAsP Surface Passivation

The predicted benefit of surface passivation, using Gallium-Phosphate-Oxide, is to decrease the surface recombination velocity, s_o, and reduce the surface component of junction leakage current. To test this theoretical prediction, the surface recombination velocity must be related to the surface component of leakage current in a GaAsP p-n junction which has been passivated by thermally grown Gallium-Phosphate-Oxide. This research challenge can be met by fabricating and evaluating a gate controlled diode.

V. CONCLUSIONS AND RECOMMENDATIONS

This section summarizes some of the major results of this program and suggests areas where further investigations are needed in order to ultimately develop thermally grown dielectrics on III-V compounds to the point where they can be utilized in device applications.

Dielectric and Interface Properties

This work has shown that a Gallium-Phosphate-Oxide dielectric can be thermally grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ without severe decomposition of the semiconductor surface. Ion microprobe measurements have shown that the bulk of this dielectric is arsenic-deficient, and that there is an arsenic-rich region at the interface with the semiconductor. The effect of this arsenic-rich region on the electrical characteristics of the MOS devices is not known, although similar electrical behavior has been observed in GaP MOS devices in which no arsenic-rich layer exists (Reference 11).

The d-c leakage current of the devices was significantly decreased, if no post-oxidation nitrogen anneal was performed. The effect of other annealing ambients, particularly hydrogen and argon, should be investigated to determine if further improvements can be obtained.

A dielectric constant of 6.3 was determined for the GPO layer. This suggests that thicker GPO layers (>2500 Å) can be used in MOS applications. The use of thicker layers will reduce gate oxide leakage and increase device operating voltage.

The depletion-type capacitance-voltage characteristics of the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS capacitors is most likely due to the low minority carrier generation rate in the semiconductor. There is some question as to whether dielectric leakage currents of the magnitude measured for these devices could result in deep depletion characteristics. Very recent results in which strongly illuminated devices demonstrated inversion-type C-V characteristics, suggest that this is not the case.

The interface properties of these devices can very likely be improved by performing processing variations which were beyond the scope of this program. There is a high probability that hydrogen annealing following oxidation will remove a substantial amount of the C-V hysteresis,

as in GaAs MOS devices. In addition, the effect of different gate electrode metals, such as chromium should be investigated to determine their effect on interface trapping. Preliminary work (Reference 1) had indicated the importance of the gate metal used.

Some comments are in order regarding the significant effects of illumination on the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS capacitor characteristics. Such a large sensitivity of the oxide or interface traps is not expected because of (1) the thickness of the aluminum gates of these structures (1 μm) and (2) the diffusion length of minority carriers of only a few microns. However, as mentioned, recent results on thick oxide devices indicate that inversion of the surface may be possible simply by illuminating the device with high intensity white light. The reason for this behavior is not completely understood, but should be investigated further. Photoemission studies on devices with transparent gate electrodes should be conducted to provide more information on the nature of the interface traps and their energy levels.

Interface Analysis Methods

The types of characteristics displayed by the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ MOS devices (and most other III-V compound MOS devices) present several difficulties when an analysis of interface properties is attempted. It is probable that many of the traditional methods employed for the analysis of SiO_2-Si interfaces may not be applicable in the case of wide bandgap semiconductor devices.

Evaluation using the quasi-static technique requires that thermal equilibrium conditions exist in the device and that the dielectric leakage current be negligible. Because depletion-type C-V curves are observed at room temperature, it is not certain that the first of these requirements is met, in every case, in the present devices. Additional theoretical research, directed toward the question of nonequilibrium and its resulting effects on device characteristics, will provide new information useful in MOS device development.

It is possible that the low temperature technique (Gray-Brown, Reference 21) may be useful for examining states in the vicinity of the Fermi level. This method does not necessarily rely on the existence of thermal equilibrium conditions, but only involves observing voltage shifts at a given surface potential when the device temperature is lowered.

A recent report (Reference 22, September 1977) has discussed a method by which hysteresis effects may be separated from the MOS capacitor measurements. This technique involves using a narrow bias-voltage swing about a given center bias voltage to obtain a C-V curve without hysteresis. The differential capacitance method can then be used to analyze the C-V data for interface state density. This analysis approach should be helpful in analyzing the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ devices when the results are compared with the interface trap values given in this report.

Application of Gallium-Phosphate-Oxide to III-V Compound Semiconductor Devices

The usefulness of Gallium-Phosphate-Oxide as a dielectric for device applications is a matter of strong interest. The hysteretic nature of the devices used in this study is probably not indicative of the ultimate stability that can be achieved for the GPO/$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ interface. As mentioned earlier in this report, it is probable that a suitable post-oxidation anneal can provide devices that possess interface properties equalling or surpassing those of other native insulators on III-V devices. Process development beyond the scope of this program is needed for this improvement. The advantages that this thermal-oxide/semiconductor combination possesses, such as high dielectric constant, ease of oxide formation, high temperature operation, as well as potentially long storage times and excellent interface properties are strong justifications for further research in this area. This initial program has provided the technical data necessary for planning subsequent research.

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APPENDIX A

Chemical Etching of Gallium-Phosphate-Oxide Dielectrics Thermally Grown on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$

The following is a table of recent results on the chemical etching of thermally grown insulators on $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$. This research was supported by a company-sponsored IR&D project entitled "GaAs Surface Passivation." The Principal Investigator for this project is Dr. R. K. Pancholy.

	Etchant	Temp.	Approx. GPO Etch Rate	Notes
(1)	1:1 $HNO_3:H_2O$	R.T. 70°C	~150 Å/min.	Leaves grainy surface. Etches $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ Surface..
(2)	NH_4OH	R.T.	~1000 Å/min.	Oxide flakes off in layers. Slightly grainy surface remains. Graininess increases with air exposure.
(3)	1:1 $NH_4OH:H_2O$	R.T.	To Be Determined	Same As Above
(4)	5:1:1 $H_2SO_4:H_2O_2:H_2O$	R.T.	--	Etches $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ surface.
(5)	NH_4F	R.T.	~100 Å/min.	Oxide flakes off. Slightly more surface graininess after etch than NH_4OH. Does not attack photoresist.
(6)	Shipley AZ Photoresist Developer	R.T.	>2000 Å/min.	This is a metal hydroxide-based solution.
(7)	20:5:1 H_3PO_4:Acetic:HNO_3	60°C	--	Attacks $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$. This is a common aluminum etchant.

APPENDIX B

GATE CONTROLLED DIODE DESIGN STUDY

INTRODUCTION

The objective of this design study is to determine the feasibility of fabricating a gate controlled diode to measure the surface recombination velocity of a GaAsP semiconductor surface following surface passivation by using thermal oxidation methods to form a Gallium-Phosphate-Oxide (GPO) dielectric. This study shows that only surface accumulation and surface depletion conditions are necessary to determine the surface recombination velocity. Surface inversion is not required for the analytical approach described in this study.

SURFACE PASSIVATION ON GaAsP

Due to high interface state densities, high surface recombination velocity, and charge-trapping-induced instabilities, devices fabricated with deposited insulators have not successfully utilized the inherent bulk GaAsP and GaAs properties such as high electron mobility in the development of semiconductor devices such as MOS FETs. The inherent advantages of GaAsP and GaAs can be fully realized following the development of improvements in material and device fabrication processes. A major improvement required for GaAsP and GaAs is the development and demonstration of a *high-quality native surface passivation dielectric.*

Thermal oxidation of $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ has been shown to result in the formation of an amorphous layer of $GaPO_4$ and crystalline β-Ga_2O_3. The relative composition ratio of the native oxide has been examined for a 700°C oxidation procedure of $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ and has been shown to be 3 $GaPO_4$ + 2 Ga_2O_3 by volume. The composite $GaPO_4$+ Ga_2O_3, called *Gallium-Phosphate-Oxide,* has exhibited good dielectric and interface properties.

An important long-term goal of this surface passivation approach is to *achieve a low surface recombination velocity so that p-n junction surface recombination current can be minimized.* Theoretically, this result can be obtained by achieving a low interface state density, N_{st}.

The origin of high surface recombination velocity can usually be traced to a high density (N_{st}, traps/cm^2) of carrier traps at the surface

of a semiconductor. Many of these traps act as recombination centers, and minority carriers reaching the semiconductor surface can recombine at these centers very rapidly. This process increases the surface component of p-n junction leakage current. To a first approximation, for a given impurity carrier concentration, the surface recombination velocity, s_o, is monotonically proportional to the surface state density, N_{st}.

The magnitude of s_o for mechanically worked semiconductor surfaces (i.e., sand-blasted or lapped) is in excess of 10^4 cm/sec. Chemical etch treatments can reduce the value of s_o to less than 100 cm/sec. Silicon surfaces, passivated by a silicon dioxide layer as in planar technology, with surface state densities of $N_{st} \leq 10^{10}$ states/cm^2, result in typical recombination velocities less than 10 cm/sec. *Thermally oxidized GaAsP surfaces, passivated with Gallium-Phosphate-Oxide, have shown effective total state densities of* $<2 \times 10^{10}$ *states/cm*^{2}. The key to improving the performance of GaAsP and GaAs devices is to passivate the semiconductor surface, preferably with a thermally grown native dielectric, to achieve low values of surface recombination velocity. GaAsP gate controlled diode structures have not been fabricated and evaluated. Consequently this study to evaluate the feasibility of fabricating and evaluating a GaAsP gate controlled diode, for the measurement of surface recombination velocity, is based on an extension of data and theory which exists for silicon gate controlled diode structures. In summary, *the predicted benefit of a low interface state density is to decrease the surface recombination velocity, s_o, and reduce the surface component of junction leakage current.* To test this theoretical prediction --

- The surface recombination velocity must be measured and related to the interface state density, N_{st};
- The surface recombination velocity must be related to the surface component of leakage current in a GaAsP p-n junction which has been passivated by thermally grown Gallium-Phosphate-Oxide.

This research challenge can be met by fabricating and evaluating a gate controlled diode, as described below.

EXPERIMENTAL DEVICE STRUCTURES FOR SURFACE EVALUATION

The three experimental structures customarily employed in the study of surface effects and of the characteristics of surface space-charge regions are illustrated in Figure 1. These structures are (a) the metal-insulator-semiconductor capacitor structure; (b) the gate or field-plate controlled p-n junction; and (c) the metal-insulator-semiconductor surface field-effect transistor.

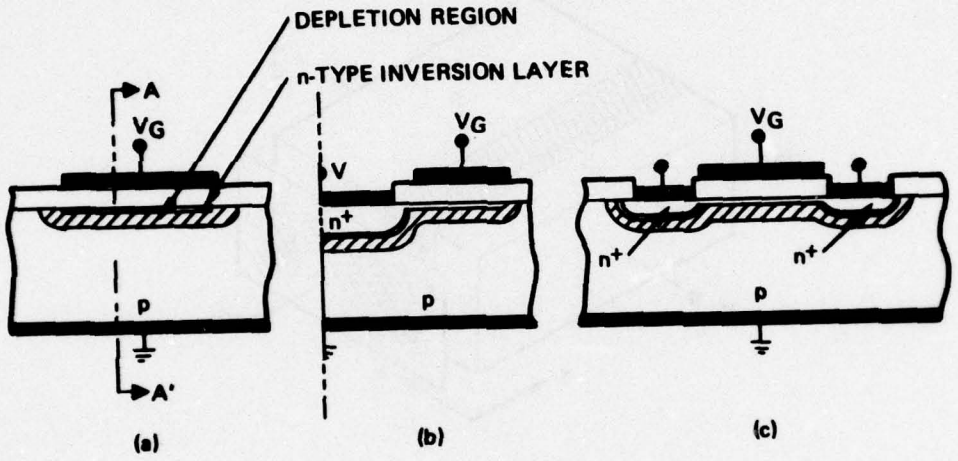


Figure 1. Experimental MOS Device Structures Used to Study Surface Effects (Reference 1)

(a) The metal-insulator-semiconductor capacitor structure.
(b) The gate-controlled p-n junction.
(c) The metal-insulator-semiconductor surface field-effect transistor

In all cases $V_G >> 0$; an electrical bias condition used to form a depletion region and an inversion layer under the gate.

GATE-CONTROLLED-DIODE

The gate controlled diode structure, as described by Grove (Reference 1), is shown in Figure 2(a). Although Figure 2 refers to a diode having a p-type substrate, this discussion is equally valid for a diode with an n-type substrate if appropriate changes in the polarity of the applied voltages are made. The n-type region, n^+, is assumed to be much more heavily doped than the substrate. The surface of the substrate within the dashed frame in Figure 2(a) is shown in a more idealized form in Figure 2(b).

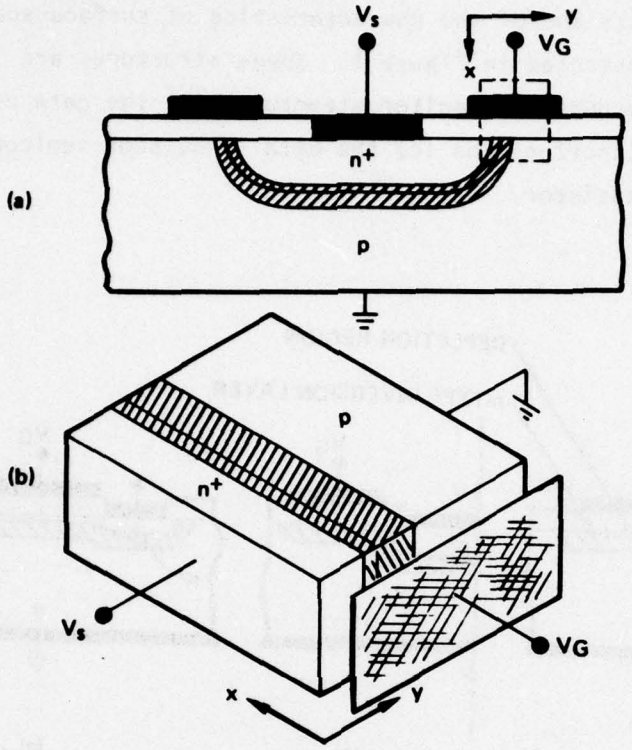


Figure 2. Gate Controlled Diode Structure (Reference 1)

(a) Cross-section illustration of Gate Controlled Diode.
(b) Idealized representation of the portion of the surface enclosed by the dashed frame in (a).

Reverse current of p-n junctions is due to electron-hole pairs generated through the action of recombination-generation centers within the depletion region. Thus, the magnitude of the reverse current depends on the total number of such centers included within the junction depletion region.

The reverse current versus gate voltage characteristics of a gate-controlled p-n junction is depicted in Figure 3. When the surface under the gate is *accumulated*, only those centers which are within the depletion region of the metallurgical p-n junction contribute to the generation current [Figure 3(a)]. When the surface under the gate is *depleted*, centers within the surface depletion region also contribute to the generation current which is, therefore, larger than in the first case [Figure 3(b)]. This contribution to the generation current is related to the

width of the surface depletion region, x_d. Thus, when the surface is *depleted* and x_d is increasing with increasing gate voltage, this current component increases as indicated by the dashed line in Figure 3.

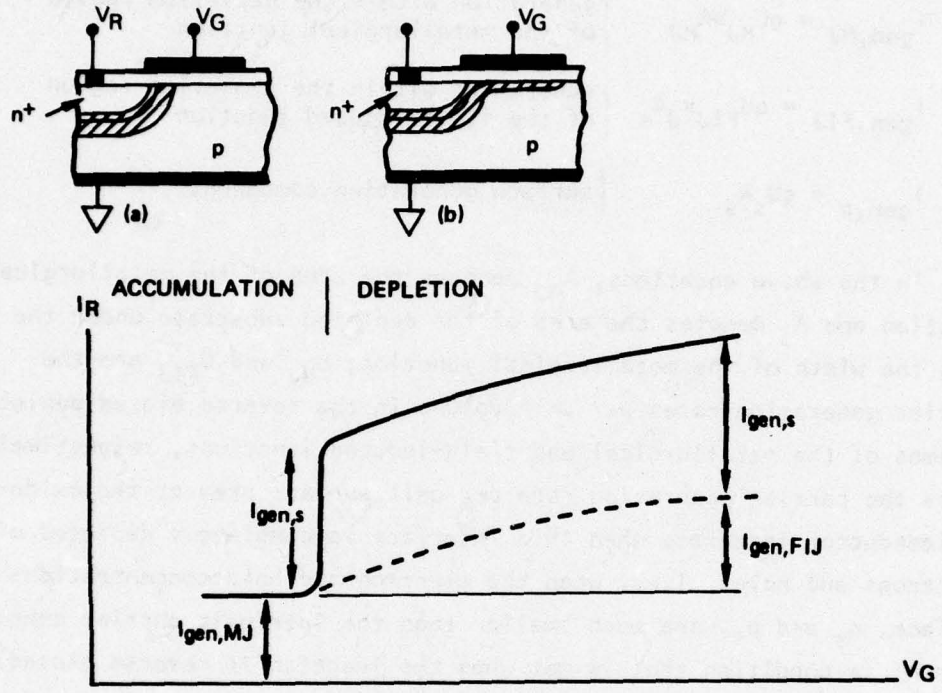


Figure 3. Gate controlled diode leakage current versus gate voltage; showing the changes in reverse current of an n^+p gate controlled diode resulting from changes in the surface space-charge region (Reference 1). In this illustration, only the gate voltage is varied; the p-n junction is maintained at a fixed reverse bias. The transition between accumulation and depletion surface conditions allows the measurement of $I_{gen,s}$. Surface inversion is not a necessary condition for the measurement of $I_{gen,s}$.

When the surface is *depleted*, recombination-generation centers at the oxide silicon interface provide yet another contribution to the total generation current. This contribution will result in a sharp increase in the reverse current versus gate voltage characteristics, as illustrated in Figure 3. This description has been verified by experimental measurements on *silicon* gate controlled diodes (Reference 1).

The generation current may consist of one or more of the following three components, depending on the nature of the surface space-charge region:

$$I_{gen,MJ} = qU_{MJ}WA_{MJ} \quad \left\{\begin{array}{l}\text{generation within the depletion region}\\ \text{of the metallurgical junction}\end{array}\right. \tag{1}$$

$$I_{gen,FIJ} = qU_{FIJ}x_dA_s \quad \left\{\begin{array}{l}\text{generation within the depletion region}\\ \text{of the field-induced junction}\end{array}\right. \tag{2}$$

$$I_{gen,s} = qU_sA_s \quad \left\{\text{surface generation component}\right. \tag{3}$$

In the above equations, A_{MJ} denotes the area of the metallurgical junction and A_s denotes the area of the depleted substrate under the gate; W is the width of the metallurgical junction; U_{MJ} and U_{FIJ} are the carrier generation rates per unit volume in the reverse biased depletion regions of the metallurgical and field-induced junctions, respectively. U_s is the carrier generation rate per unit surface area at the oxide-semiconductor interface when this interface is completely depleted of both electrons and holes, i.e., when the electron and hole concentrations at the surface, n_s and p_s, are much smaller than the intrinsic carrier concentration n_i (a condition that is met when the junction is reverse biased).

The generation rate per unit volume in a reverse-biased depletion region is given by Reference 1:

$$U = \frac{n_i}{2\tau_o} \tag{4}$$

with $\tau_o = 1/\sigma v_{th}N_t$ for centers with an assumed energy level $E_t = E_i$. Here N_t is the concentration (per unit volume) of bulk recombination-generation centers, and σ is their capture cross section, assumed, for simplicity, to be approximately the same for electrons and holes.

For a completely depleted surface, the carrier generation rate per unit area is given by Reference 1:

$$U_s = \frac{n_i s_o}{2} \tag{5}$$

where the surface recombination velocity, s_o is

$$s_o = \sigma v_{th}N_{st} \quad \left\{\text{surface recombination velocity}\right. \tag{6}$$

for centers with energy level $E_t = E_i$ where the thermal velocity of carriers, $v_{th} \approx 10^7$ cm/sec, and N_{st} is the density (per unit area) of surface recombination-generation centers.

The three current components can be expressed as

$$I_{gen,MJ} = \frac{q\, n_i}{2\tau_{oMJ}} WA_{MJ}, \tag{7}$$

$$I_{gen,FIJ} = \frac{q\, n_i}{2\tau_{oFIJ}} x_d A_s, \tag{8}$$

and

$$I_{gen,s} = \frac{1}{2} q n_i s_o A_s. \tag{9}$$

COMPARISON OF SURFACE RECOMBINATION VELOCITY EXPRESSIONS FOR EITHER A DISCRETE-LEVEL, OR A CONTINUUM (UNIFORM DISTRIBUTION) OF SURFACE STATES

For silicon gate controlled diodes, the assumed condition of $E_t = E_i$ is in good agreement with experimental measurements of the temperature dependences of the three current components, all of which have the same temperature dependence as the intrinsic carrier concentration, n_i (Reference 2). However, it is important to note that a *continuum* of states distributed in energy would lead to similar results, since only those states that are within approximately one kT from the middle of the energy gap are efficient generation centers. For *uniform distributions* of states of density D_t (cm^{-3} ev^{-1}) and D_{st} (cm^{-2} ev^{-1}) in the bulk and at the surface, respectively, the effective lifetime τ_o is

$$\tau_o = \frac{1}{\sigma v_{th} (\pi k T D_t)}, \tag{10}$$

and the surface recombination velocity s_o is

$$s_o = \sigma v_{th} (\pi k T D_{st}). \tag{11}$$

Such states would also lead to current components which have the same temperature dependence as n_i. This analysis leads to an important conclusion--*single-level states located at energy E_i and a continuum or uniform density of states will have approximately the same effect.*

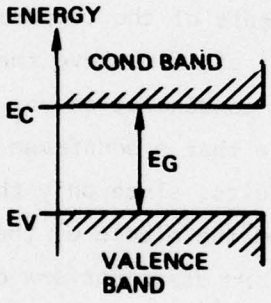
P-N JUNCTION REVERSE-BIAS VOLTAGE DEPENDENCE

In Equation (7) the depletion region width, W, depends upon the value of reverse bias applied to the p-n junction. Also, in Equation (8), the depletion width of the field-induced junction, x_d, is dependent upon reverse bias.

It is evident from Equations (7), (8) and (9) that, whereas both bulk generation current components should depend on the magnitude of the reverse bias through W and x_d, the surface generation current should be independent of the reverse bias.

INTRINSIC CARRIER CONCENTRATION, n_i

Figure 4 gives the bandgap energies of the five most-used semiconductor materials.



MATERIAL	BANDGAP ENERGY
Ge	0.7 eV
Si	1.1 eV
GaAs	1.4 eV
$GaAs_{1-x}P_x$	1.4 TO 2.25 eV*
GaP	2.25 eV

*EXACT VALUE DEPENDS UPON X, THE PHOSPHORUS MOLE FRACTION

Figure 4. Bandgap Energies for Ge, Si, GaAs, GaAsP, and GaP

For any semiconductor, the carrier concentration n_i, due to thermal generation of carriers, is related to the characteristic bandgap energy of the semiconductor. This "intrinsic" carrier concentration is calculated according to

$$n_i = (N_c N_v)^{1/2} \exp\left(\frac{-E_G}{2kT}\right) \tag{12}$$

where

$$N_c = 2[2\pi m_n kT/h^2]^{3/2} \tag{13}$$

$$N_v = 2[2\pi m_p kT/h^2]^{3/2} \quad (14)$$

m_n = effective electron mass

m_p = effective hole mass

h = Planck's constant

k = Boltzmann's constant

T = absolute temperature

The above equations yield results which are in close agreement with experiment. Equation (12) shows that the value of n_i is strongly (exponentially) dependent upon the bandgap energy. Equation (12) is plotted in Figure 5 for GaP, GaAs, Si, and Ge.

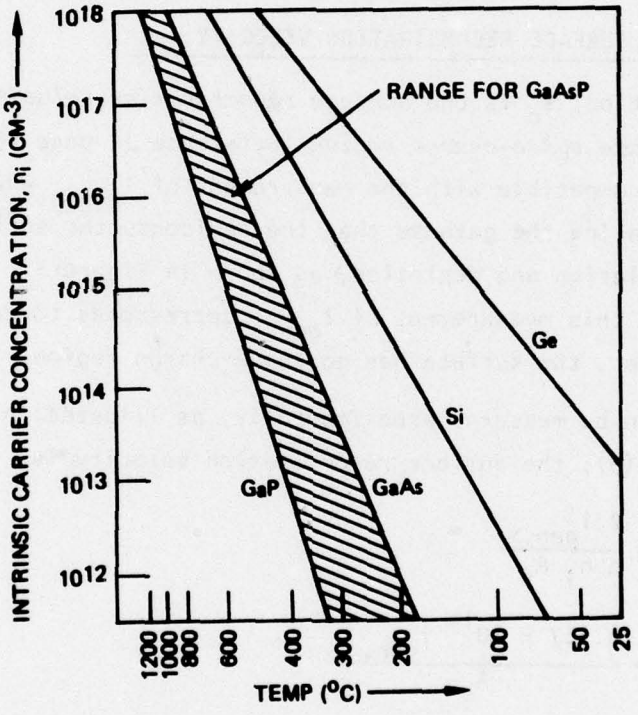


Figure 5. Intrinsic Carrier Concentration Versus Temperature

For the semiconductor of interest,

$$n_i \approx 3 \times 10^5 \text{ carriers/cc} \quad (15)$$

for $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ at room temperature. This is a very low value in comparison with other semiconductor materials. For comparison, Table I lists the room-temperature value of n_i for GaAsP, GaAs, silicon, and germanium.

Table 1

Room-Temperature Intrinsic Carrier Concentration for Germanium, Silicon, GaAs, and $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$

Material	Approximate n_i, Carriers/cc
Ge	$\sim 2 \times 10^{13}$
Si	$\sim 1.5 \times 10^{10}$
GaAs	$\sim 9 \times 10^{6}$
$GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$	$\sim 3 \times 10^{5}$

MEASUREMENT OF SURFACE RECOMBINATION VELOCITY, s_o

By definition, s_o is the *surface recombination velocity of a surface without a surface space-charge region* (Reference 1, page 139). This definition is compatible with the measurement of $I_{gen,s}$ when $I_{gen,s}$ is measured by biasing the gate so that the semiconductor surface transitions between accumulation and depletion, as shown in Figure 3. To a first approximation, this measurement of $I_{gen,s}$ corresponds to near-flat-band conditions, i.e., the surface has no space-charge region.

$I_{gen,s}$ can be measured experimentally, as illusted in Figure 3. From Equation (9), the surface recombination velocity is

$$s_o = \frac{2\, I_{gen,s}}{q\, n_i\, A_s} \tag{16}$$

$$s_o = \frac{4.167 \times 10^{14}\, I_{gen,s}}{A_s} \tag{17}$$

where $[I_{gen,s}]$ = surface generation current as defined in Figure 3; amperes

$[A_s]$ = area of the depleted substrate under the gate; cm^2

DENSITY OF SURFACE STATES AND CAPTURE CROSS SECTION

For simplicity, the capture cross section is assumed to be the same value for electrons and holes (Reference 1, page 301). The determination of the capture cross section, σ, requires an independent measurement, or estimate, of N_{st}, the density (per unit area) of surface recombination-

generation centers. These surface recombination-generation centers, originally described theoretically by Tamm and Schockley (Reference 3 and Reference 1, page 144), are called *surface states*, or *interface states*.

Theoretical estimates of the density of surface states yield values of the same order as the density of the surface atoms, $N_{st} \sim 10^{15}$ cm^{-2}. This high value of surface state density has indeed been observed on very clean semiconductor surfaces obtained by cleaving samples under high vacuum. However, germanium and silicon samples after exposure to air for only a few minutes show surface state densities of the order of only $N_{st} \sim 10^{11}$ cm^{-2}, and thermally oxidized silicon surfaces can show densities yet another order of magnitude smaller. The cause of such a reduction is evidently brought about by the presence of a very thin oxide layer which can be grown on germanium, silicon and GaAsP.

Upon irradiation, the magnitude of s_o as well as the density of surface states has been found to increase. The determination of σ requires an independent measurement, or estimate, of N_{st}, using capacitance-voltage methods. Figure 6 shows a comparison between measured values of s_o and independently estimates values of the surface state density, N_{st}, of thermally oxidized silicon samples (Reference 4). The straight-line

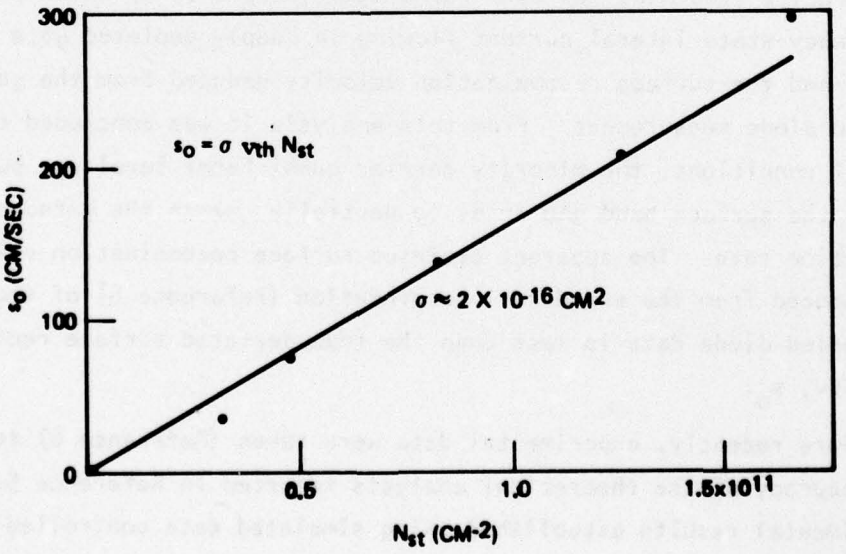


Figure 6. Comparison Between Surface Recombination Velocity s_o and Surface-State Density, N_{st}, for Silicon Surfaces (Reference 4)

relationship observed is in agreement with Equation (6), with the slope corresponding to the capture cross section. This method can be used to determine the capture cross section for GPO-GaAsP interface states. The states are assumed to be distributed in a planar sheet at the GPO-GaAsP interface, i.e., $(D_{st})^{1/2} > (D_{\tau})^{1/3}$. However, for a very rough approximation, it can be assumed that, for a thin region near the interface, $(D_{st})^{1/2} \approx (D_{\tau})^{1/3}$. From Figure 20, $N_{ss} = D_{st} \approx 8 \times 10^{11}$ cm^{-2} eV^{-1}. Using this value, and an effective liftime of $10^{-9} < \tau_o < 10^{-8}$ sec, Equation 10 can be used to obtain a predicted value of the capture cross section for GPO-GaAsP surface states, i.e., $\sigma = 10^{-9}$ to 10^{-8} cm^2.

DETERMINATION OF SURFACE RECOMBINATION VELOCITY WITH IMPROVED ACCURACY

The theoretical description above, from Reference 1, is based upon the following simplifying assumptions:

- The capture cross section, σ, is approximately the same value for holes and electrons at the semiconductor surface.
- The value of s_o is assumed to be independent of gate length, L, or the area of the depleted substrate under the gate, A_s, i.e., $s_o \neq f(L)$.

These simplifying assumptions are, of course, not strictly accurate. A more precise treatment has been formulated (Reference 5) which considers the steady-state lateral current flowing in deeply depleted gate controlled diodes and the surface recombination velocity deduced from the gate controlled diode measurement. From this analysis it was concluded that, under typical conditions, the minority carrier quasi-Fermi level was positioned within the surface band gap so as to partially quench the gated surface generation rate. The apparent depleted surface recombination velocity, s_o', deduced from the standard interpretation (Reference 6) of the gate controlled diode data is less than the true depleted surface recombination velocity, s_o.

More recently, experimental data were taken (Reference 6) to evaluate the accuracy of the theoretical analysis reported in Reference 5. The experimental results established using simulated gate controlled diode structures affirm that the apparent s_o' value resulting from the constant quasi-Fermi level interpretation of gate controlled diode data is gate-length dependent and typically less than the true s_o value. A detailed correlation of experiment with theory, however, requires that accurate and independent values be used for the surface electron and hole capture cross sections and that the surface state related lateral field effect be taken into account.

The gate-length dependence upon apparent-to-true s_o is shown in Figure 7.

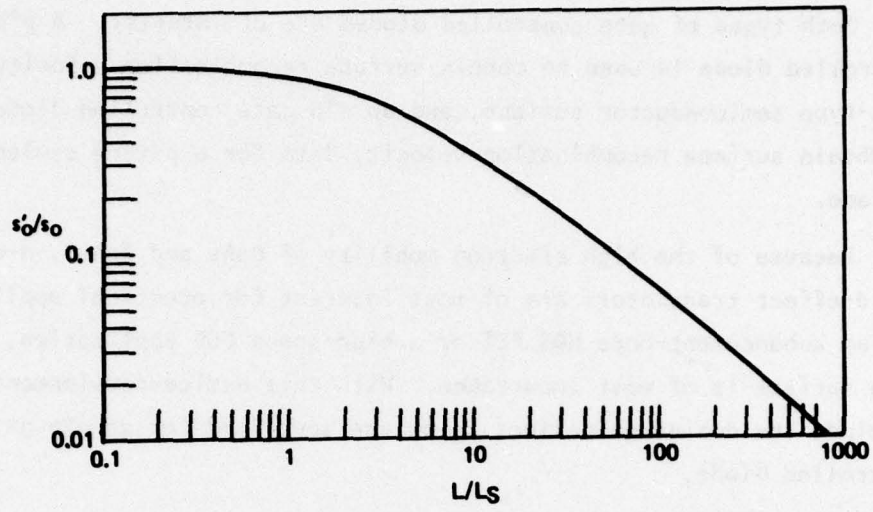


Figure 7. Apparent-to-true depleted surface recombination velocity ratio expected in the surface controlled limit (depletion region generation negligible) as a function of gate length, L, normalized by L_S (Reference 5).

In Figure 7, L_S is a scaling parameter defined for mathematical convenience. For a p-type bulk device,

$$L_S = [(\mu_n/qs_oN_A)(kT/q)^2(K_s\varepsilon_o/W)]^{1/2} \qquad (18)$$

In the above equation, the notation is the same as in Reference 5.

The dependence upon gate length has been established recently, for silicon gate controlled diodes, subsequent to much earlier work (References 7 - 13). This theoretical work, which more accurately defines the surface recombination velocity, is believed to be applicable to gate controlled diodes fabricated on wide-bandgap semiconductors such as GaAsP and GaAs.

DESIGN AND ANALYSIS OF GaAsP GATE CONTROLLED DIODE

GaAsP gate controlled diodes have not been fabricated, although the characterization of a gate controlled diode, with appropriate data analysis, is the most straightforward method for analyzing the effectiveness of a surface passivation dielectric.

p^+n and n^+p Gate Controlled Diodes

Both types of gate controlled diodes are of interest. A p^+n gate controlled diode is used to obtain surface recombination velocity data for an n-type semiconductor surface, and an n^+p gate controlled diode is used to obtain surface recombination velocity data for a p-type semiconductor surface.

Because of the high electron mobility of GaAs and GaAsP, n-channel field-effect transistors are of most interest for practical applications. For an enhancement-mode MOS FET or a high-speed CCD application, the p-type surface is of most importance. With this device-development objective in mind, the design guidelines below are specified for an n^+p gate controlled diode.

Doping Concentration

The doping concentration of the n^+ region is not critical. A design-goal range of $10^{18} \leq N_D \leq 5 \times 10^{18}$ cm^{-3} has been established for the following reasons:

- This degenerate value can be easily obtained in practice.
- Using common practice, ohmic contacts can easily be made to a semiconductor having this doping concentration.

A design-goal acceptor doping concentration range of $1 \times 10^{15} \leq N_A \leq 1 \times 10^{16}$ cm^{-3} has been established for the GaAsP gate controlled diode. A design-goal value of $N_A \approx 2 \times 10^{15}$ cm^{-3} has been established for the target doping concentration of the p-type substrate for the following reasons:

- This range of doping concentration can be obtained in practice.
- The semiconductor surface can be depleted with electric field values which can be supported by the Gallium-Phosphate-Oxide dielectric.
- This range of doping concentration is compatible with MOS capacitor fabrication and capacitance-voltage analysis methods commonly used to investigate the dielectric-semiconductor interface.

- For this range of doping concentration, the calculated junction breakdown voltage (>10 volts) is higher than required for obtaining the needed experimental data from the gate controlled diode.

Junction Depth

A design-goal value of 4 ± 3 microns has been established for the junction depth of the gate controlled diode for the following reasons:

- The lower limit (1 micron) can be achieved using ion implantation and low-temperature (<800°C) diffusion, where as the upper limit can only be achieved using very long, high-temperature diffusion cycles.
- This range of junction depths will place the horizontal (bulk) part of the junction deep enough into the semiconductor to minimize, although not prevent, surface recombination-generation from affecting the bulk junction characteristics.
- This range of junction-depth values is approximately the effective values of diffusion length at an unpassivated GaAs surface (1 to 3.5 μ), and the effective values of diffusion length in bulk GaAs (~5 μ). These values, from Reference 14, are the best available values for GaAs, and it is expected that these values will be found to approximately describe a GaAsP surface, where the bulk value (~5μ) is expected to correlate with a *well-passivated* GaAsP surface.
- This range of junction-depth values is appropriate for use with scanning electron microscopy, to characterize the s_o through the use of an independent experimental method.

Junction Depletion Widths

The calculation of GaAsP junction width is analogous to the calculation of the depletion width for silicon junctions, since the relative dielectric constants are approximately the same for the two materials (11.35 for $GaAs_{\frac{1}{2}}P_{\frac{1}{2}}$ and 11.7 for silicon). Also, for doping concentrations of $N_A \approx 2 \times 10^{15}$ cm^{-3} and $N_D \approx 2 \times 10^{18}$ cm^{-3}, the built-in voltage of the zero-biased junction is approximately 1.356 volts for GaAsP and 0.793 volts for silicon. For the design-goal doping concentrations, the calculated depletion width for the GaAsP gate controlled diode is ~0.9μ for a junction bias of 0 volts, and ~2.6μ for a junction reverse bias of 10 volts. These values are, as desired, less than the junction diffusion depth.

Gate Length

A design-goal value of 25 μ has been established for the gate length, L, of the gate controlled diode. This value of L is approximately ten times the junction depletion width for a reverse bias of 10 volts--a condition which assumes that the gate controlled diode junction leakage current will be dominated by surface effects, thereby permitting an accurate determination of the surface recombination velocity. A large value of gate length produces large values of $I_{gen,s}$ which are easily measured. However, if the gate length is larger than ~$2L_S$ [Equation (18)], the apparent value of surface recombination velocity is strongly dependent upon gate length, as described by Figure 7. Through a curve translation procedure (Reference 6), experimental values of $L_S \approx 0.455$ mils have been found to be ~1.5 times the value of L_S for simulated silicon gate controlled diodes having acceptor doping concentrations in the range of $10^{14} < N_A < 10^{16}$ cm^{-3}. For a GaAsP gate controlled diode having approximate values of $N_A = 2 \times 10^{15}$ cm^{-3} and $\mu_h \approx 200$ cm^2/volt-sec, $L_S \approx 0.1$ mil = 2.5 μ. Consequently, for L = 25 μ, the ratio of apparent-to-true surface recombination velocity is expected to be ~0.3, i.e., a correction factor of ~3 will be needed to account for gate-length dependence.

Surface Depletion Depth

Although the depletion characteristic C-V curves for typical GaAsP MOS structures (gate region of gate controlled diode) indicate no inversion, it is instructive to calculate the theoretical conditions corresponding to inversion.

The difference between the Fermi potential energy and the intrinsic potential energy can be calculated from $p = n_i \exp[E_i - E_F)/kT]$. If $p = N_A$ and $n_i \approx 3 \times 10^5$ cm^{-3}, $q\phi_f = E_i - E_F \approx 0.6$ eV. At the onset of strong inversion, ϕ_s (inv) = +1.2 volts.

When biased in the inversion regime, the MOS capacitor maintains a fixed depletion width, independent of applied bias. This depletion width is given by Grove (Reference 1, p. 268) as

$$x_{dmax} = \left[\frac{2\varepsilon_s \phi_s (inv)}{qN_A}\right]^{1/2} \qquad (19)$$

Using the values given above, x_{dmax} = 0.868 micron. This value ensures that, using the design-goal values for acceptor doping concentration, the gate controlled diode can be used to determine the surface recombination velocity for a 0.8-micron-thick layer of the GaAsP semiconductor surface.

Depletion-Region Charge in the Semiconductor

The charge in the depletion region for $x_d = x_{dmax}$ is given as $Q_B = qN_A x_{dmax} = 2.78 \times 10^{-8}$ coulombs/cm^2.

Gate Insulator Capacitance per Unit Area

Assuming the GPO dielectric constant ≈5 and the GPO thickness ≈1000 Å, the capacitance per unit area is $C_o \approx 4.44 \times 10^{-8}$ F/cm^2 for the GPO gate insulator. (A thicker GPO insulator can be used if desired.)

Flat-Band Voltage

The flat-band voltage cannot be accurately calculated because it is an experimental variable; however, estimates can be used to predict bounds for the flat-band voltage. The flat-band voltage depends upon the metal-semiconductor work function, ϕ_{MS}, and the effective surface state charge, Q_{ss}:

$$V_{FB} = \phi_{MS} - \frac{Q_{ss}}{C_o} \tag{20}$$

ϕ_{MS} depends upon the type of metal used, and the substrate doping concentration and dopant type. For chromium and n^+ GaAs, $\phi_{MS} \approx 0.6$ volt; for aluminum and p^+ GaAs, $\phi_{MS} \approx 0.154$ volt. For other metal systems, including gold-germanium-nickel tri-metal systems, and p^+ GaAs substrates, ϕ_{MS} can have values of $-1 \leq \phi_{MS} \leq 1$ volt. The value of fixed charge $Q_{ss} = q N_{ss}$ is also an experimental variable. Typically, $10^{10} \leq N_{ss} \leq 10^{12}$ cm^{-2}. For $N_{ss} = 10^{10}$ states/cm^2, $Q_{ss}/C_o = \pm 0.036$ volt; for $N_{ss} = 10^{11}$ states/cm^2, $Q_{ss}/C_o = \pm 0.36$ volt; for $N_{ss} = 10^{12}$ states/cm^2, $Q_{ss}/C_o = \pm 3.6$ volts. For this range of values, the flat-band voltage can have any value in the range of $V_{FB} \approx \pm 4.6$ volts.

Threshold Voltage

The threshold voltage, V_T, is the gate voltage required to deplete the surface of the n^+p gate controlled diode to a depth of $x_d = x_{dmax} = 0.865$ micron. The threshold voltage is given by Grove (Reference 1, p. 42) as

$$V_T = -\frac{Q_B}{C_o} + \phi_s(inv) + V_{FB} \qquad (21)$$

The theoretical threshold voltage, assuming no bulk-dielectric charge trapping or other effects, is $V_T = +0.6 + 1.2 + V_{FB}$. Because of the wide range of values which are possible for V_{FB}, the threshold voltage can lie in the range of $-2.8 \leq V_T \leq +6.4$ volts. This range of voltages requires a maximum Gallium-Phosphate-Oxide dielectric stress of $E = 6.4 \times 10^5$ volts/cm, which is safely below the dielectric strength of Gallium-Phosphate Oxide.

Design-Goal Parameter Values

Figure 8 illustrates the concepts defined by this gate controlled diode design. Table 2 gives design-goal parameter limits for the GaAsP gate controlled diode.

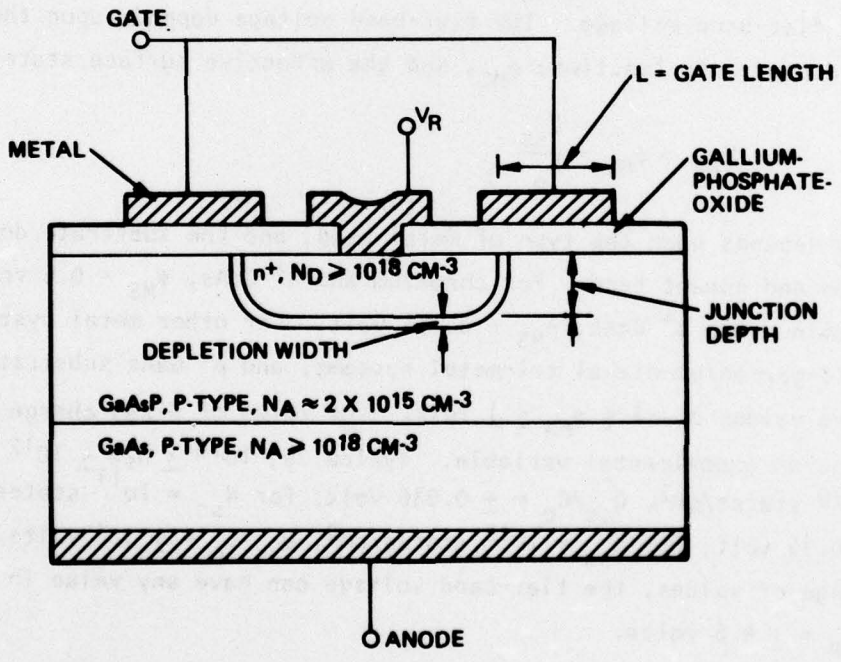


Figure 8. Design of GaAsP Gate Controlled Diode, with Design Target Values

Table 2. GaAsP Gate Controlled Diode Design Goals

PARAMETER	MINIMUM	TARGET	MAXIMUM	UNITS
Doping Concentration				
n^+ implant/diffusion (GaAsP)	1×10^{18}	-	5×10^{18}	cm^{-3}
p-type epi (GaAsP)	1×10^{15}	2×10^{15}	1×10^{16}	cm^{-3}
p^+ substrate (GaAs)	1×10^{18}	-	5×10^{18}	cm^{-3}
Junction Depth	1	4	7	microns
Gate Length = L	-	25	-	microns
Gallium-Phosphate-Oxide Thickness	800	1000	3500	Å
Epi Thickness (must be > L)	12	-	100	microns
Substrate Thickness	250	-	350	microns
Metal Thickness	7000	10,000	12,000	Å

GaAsP Gate Controlled Diode Fabrication

Fabrication of a GaAsP gate controlled diode can be accomplished using straightforward device-fabrication procedures.

Ion implantation of tellurium is recommended for the donor doping (n^+ cathode). Silicon nitride capping and thermal annealing will ensure electrical activation of the implanted tellurium.

Thermal oxidation of GaAsP will ensure the formation of a device-quality dielectric (Gallium-Phosphate-Oxide).

Aluminum metallization is recommended for forming the gate contact. Using photolithography, selective etching of the aluminum and Gallium-Phosphate-Oxide will be required to define the gate metal geometry and provide contact openings through the Gallium-Phosphate-Oxide. This will require some process-development work to ensure compatibility of materials and etchant chemistry.

Standard tri-metal (gold-germanium-nickel) deposition, definition (using either photoresist lifting or photolithographic metal etching) and sintering, will be required to form ohmic contacts to the cathode of the gate controlled diode.

Finally, the bottom of the wafer must be lapped and soldered, using indium, to ensure a good ohmic contact to the substrate (anode) of the gate controlled diode.

CORRELATION AND COMPARISON OF SURFACE RECOMBINATION VELOCITY VALUES USING TWO EXPERIMENTAL METHODS

Although surface recombination velocity, s_o, is a very important semiconductor surface parameter, s_o is not an experimental parameter, i.e., s_o cannot be measured directly--both experimental measurements *and* theoretical computation must be used to arrive at a value for s_o. Consequently, for added confidence and correlation, surface recombination velocity can be determined using two independent experimental methods:

1. Reverse-biased current measurement of a gate controlled diode or the measurement of carrier flow through a simulated gate controlled diode, from which s_o can be calculated (described above).
2. SEM electron-beam irradiation of a p-n junction to determine the effective diffusion length, from which s_o can be calculated (described below).

The results of the first method (gate controlled diode) can be verified by using the second experimental method (scanning electron microscopy) to independently determine the surface recombination velocity. The SEM electron-beam irradiation of a p-n junction is described below.

MEASUREMENT OF SURFACE RECOMBINATION VELOCITY USING SCANNING ELECTRON MICROSCOPY

The surface recombination velocity of p-n junction structures can be determined from the dependence of the minority-carrier diffusion length on the depth from the surface, employing scanning electron microscopy. This method has been used successfully to determine the surface recombination velocity at GaAs surfaces (Reference 14).

The experimental configuration used in determing the surface recombination velocity is shown in Figure 9. The current generated at the junction is determined as a function of the position of the excitation point (electron beam penetration ξ) on a plane $x = \xi$ constant, i.e., for a given accelerating voltage; the procedure is then repeated for various values of accelerating voltages, i.e., for various values of ξ.

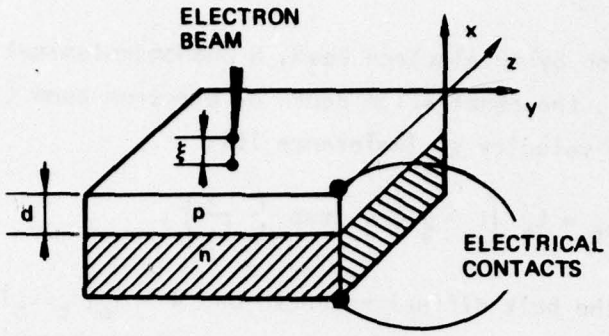


Figure 9. Experimental Configuration (Reference 14)

For ξ = constant, the effective diffusion length, L_{eff} (as defined in Reference 16), can be determined as a function of (y,z) from the relation

$$I(y,z) = I_o \exp[-(d - \xi)/L_{eff}] \qquad (22)$$

where d is the junction depth and I_o is the injection current which can be taken as a constant for a given beam current and energy. I_o can be evaluated from the electron beam energy by multiplying the electron beam energy by the generation efficiency. The generation efficiency (approximately 30% for GaAs) can be determined using a p-n junction perpendicular to the surface and employing the procedure described in Reference 15. Although such a procedure might lead to a certain error in obtaining the absolute value of L_{eff}, it provides a simple way to detect variations of L_{eff} from point-to-point on a given plane, x = constant.

In Figure 10(a), variations of L_{eff} are shown on planes parallel to the surface measured for different penetration depths of the electron beam for a junction depth of d = 6 μm (i.e., curve 7 corresponds to a penetration depth of 3.5 μm and curve 1 to a depth of 0.15 μm). The variation of L_{eff} increases with decreasing penetration depth down to the smallest penetration depth employed (i.e., 0.15 μm). This type of variation in L_{eff}, increasing with $\xi \to 0$, indicates the presence of recombination inhomogeneities at the surface (x = 0).

The decrease in the average value of L_{eff} with decreasing penetration depth has been attributed to the increasing influence of surface recombination velocity (Reference 16). Using theoretical treatments of electron-

hole excitation by an electron beam, a phenomenological model was developed relating L_{eff}, the penetration depth of electron beam ξ, and the surface recombination velocity s_o (Reference 16):

$$L_{eff}^2 = L_b^2 \left(1 - \frac{S}{S+1}\right) \exp\left(-\frac{\xi}{L_b}\right), \tag{23}$$

where L_b is the bulk diffusion length and $S = s_o(\tau_b/L_b)$; τ_b is the lifetime of the minority carriers; and s_o is the surface recombination velocity.

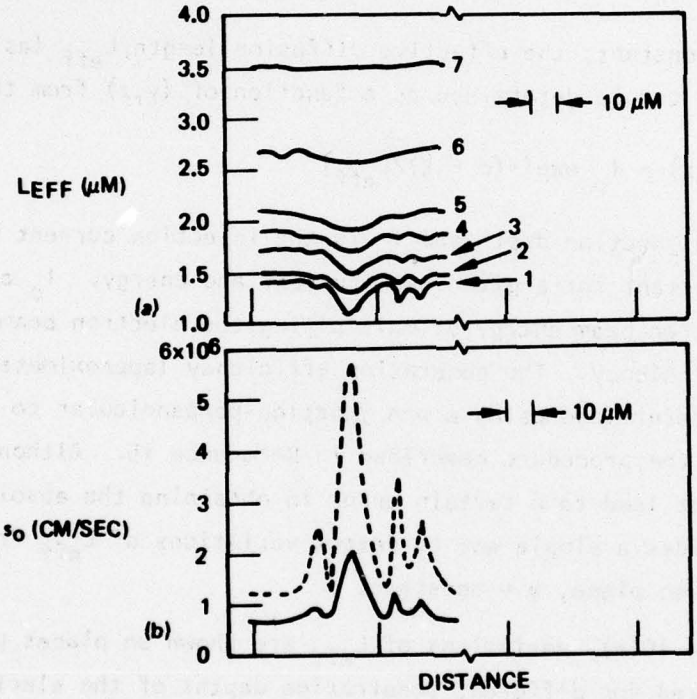


Figure 10. Parallel to the GaAs surface electron beam (data from Reference 14). Beam penetration depth (solid line) and from Hackett's analysis (dashed line).

Applying Equation (23) to the data of Figure 10(a), the solid line of Figure 10(b) is obtained showing variations of the surface recombination velocity along a given GaAs surface. Both Equation (23) and Hackett's current equation (Reference 17) yield similar qualitative behavior of the surface recombination velocity along the scanning path, although the value of surface recombination velocities obtained with Hackett's equation differ by a factor of 2 or 3 from the values obtained from Equation (23).

Junction geometry and excitation volume were not taken into consideration in obtaining Equation (23); however, this simplified treatment still yields results for GaAs surfaces in good agreement with results obtained by other methods.

SUMMARY

This design study establishes the feasibility of fabricating a gate controlled diode for evaluating a key semiconductor parameter--the surface recombination velocity. The objective is to measure the surface recombination velocity of a GaAsP semiconductor surface following surface passivation by using thermal oxidation methods to form a Gallium-Phosphate-Oxide (GPO) dielectric on the semiconductor surface. Surface inversion is not required. Only surface accumulation and surface depletion conditions are necessary to determine the surface recombination velocity.

By definition, s_o is the *surface recombination velocity of a surface without a surface space-charge region* (Reference 1, page 139). This definition is compatible with the measurement of $I_{gen,s}$ when $I_{gen,s}$ is measured by biasing the gate so that the semiconductor surface transitions between accumulation and depletion.

The analysis in this study defines the surface recombination velocity as

$$s_o = \frac{2\, I_{gen,s}}{q\, n_i\, A_s}$$

$$s_o = \frac{4.167 \times 10^{14}\, I_{gen,s}}{A_s}$$

where [$I_{gen,s}$] = surface generation current as defined in Figure 3;

[A_s] = area of the depleted substrate under the gate; cm^2

The surface recombination velocity of a semiconductor surface is not an experimental parameter, i.e., s_o cannot be measured directly--both experimental measurements *and* theoretical computation must be used to arrive at a value for s_o. Consequently, for added confidence and correlation, surface recombination velocity can be determined using SEM electron-beam irradiation of a p-n junction to determine the effective diffusion length, from which the surface recombination velocity can be calculated. The results of the

gate controlled diode method can be verified by using the scanning electron microscopy method to independently determine the surface recombination velocity.

The predicted benefit of surface passivation, using Gallium-Phosphate-Oxide, is to decrease the surface recombination velocity, s_o, and reduce the surface component of junction leakage current. To test this theoretical prediction, the surface recombination velocity must be related to the surface component of leakage current in a GaAsP p-n junction which has been passivated by thermally grown Gallium-Phosphate-Oxide. This research challenge can be met by fabricating and evaluating a gate controlled diode.

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