AD-A048 616 COBER ELECTRONICS INC STAMFORD CONN F/G 9/5
HIGH VOLTAGE NANOSECOND PULSE GENERATOR.(U)
NOV 77 J BAJDA, S GEIGER DAAB07-77-C-2641
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Research and Development Technical Report

ECOM-77-2641-2

HIGH VOLTAGE NANOSECOND PULSE GENERATORS

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November 1977

Second Triannual Report for Period 1 May 1977 to 30 Aug. 1977

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Prepared for:

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US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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(19) **REPORT DOCUMENTATION PAGE**

READ INSTRUCTIONS BEFORE COMPLETING FORM

(18) 1. REPORT NUMBER: ECOM-77-2641-2

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE (and Subtitle): High Voltage Nanosecond Pulse Generator.

(9) 5. TYPE OF REPORT & PERIOD COVERED: [redacted] Triannual Report. NO. 2, 1 May [redacted] 30 Aug [redacted] 77

6. PERFORMING ORG. REPORT NUMBER

(10) 7. AUTHOR(s): Joseph Bajda, Stephen Geiger

(15) 8. CONTRACT OR GRANT NUMBER(s): DAAB07-77-C-2641

9. PERFORMING ORGANIZATION NAME AND ADDRESS:
Cober Electronics
7 Gleason Avenue
Stamford, Connecticut 06902

(16) 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62705 1L762705AH94 B1.01 (17) E1

(11) 11. CONTROLLING OFFICE NAME AND ADDRESS:
US Army Electronics Command
ATTN: DRSEL-TL-BG
Fort Monmouth, NJ 07703

12. REPORT DATE: Nov [redacted] 77

(12) 13. NUMBER OF PAGES: 29 p.

14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release: Distribution Unlimited

DDC RECEIVED JAN 11 1978 F

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Pulse Generation
Switching
Spark Gap
Blumlein
Avalanche Transistor

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
This Second Triannual Report describes work performed during the period 1 May 77 to 30 Aug 77 to develop three high voltage nanosecond pulse generators. The objective of the development is a set of pulse generators of small volume, low weight, and high efficiency. Testing of the power supply and modulator for Task A Pulse Generator, operating either single pulse or 15 Hz at a pulse width of 125 ns, pulse voltage of 30 kV, and pulse current of 1200 amps, has been initiated. The design of an SCR-magnetic modulator for Task B Pulse Generator, →

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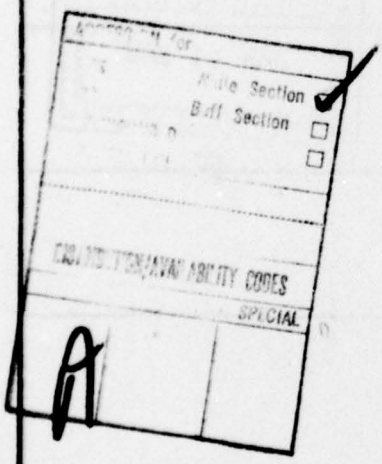
providing a 5 kV, 4 A, 100 ns pulse to the load, has been completed. Switches to meet the ultra high speed requirements for Task C Pulse Generator were evaluated in test circuits.



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I. INTRODUCTION

This report covers work done during the period 1 May 1977 to 30 Aug. 1977 on Contract DAAB07-77-C-2641 to develop a set of high voltage nanosecond pulse generators. The work is being performed by Cober Electronics in Stamford, Connecticut for the U.S. Army Electronics Command, Ft. Monmouth, New Jersey. The work is directed toward fulfilling the requirements of Technical Guidelines entitled "High Voltage Nanosecond Pulse Generators" dated 27 July 1976. Listed below are the requirements for Task A, Task B, and Task C.

Task A

a.	Output Voltage	30KV
b.	Peak Current	1200A
c.	Prr	15Hz and single pulse
d.	Pulse Width (50%)	125ns
e.	Rise Time (10% to 90%)	20ns max.
f.	Fall Time (90% to 10%)	40ns max.
g.	Pulse Energy Output	4.5 joules
h.	Pulser Efficiency	90% min. (resistive load)
i.	Life	10^6 pulses min.
j.	Weight	2.0kg max.

k.	Volume	360cm^3 max.
l.	Form Factor	Cylindrical
m.	Maximum Outer Diameter	6.5cm

Task B

a.	Output Voltage	5kV
b.	Peak Current	4A
c.	Prr	10,000Hz
d.	Pulse Width (90%)	100ns
e.	Rise Time (10% to 90%)	10ns max.
f.	Fall Time (90% to 10%)	20ns max.
g.	Pulser Efficiency	90% min. (resistive load)
h.	Pulse Energy Output	0.0023 joules
i.	Life	1000 hrs. min.
j.	Weight	2.0kg
k.	Volume	360cm^3 max.

Task C

a.	Output Voltage	1kV
b.	Peak Current	1) 15A to charge up C_L = 30pF in 2 nsec 2) 20mA during flat top portion of pulse
c.	Prr	15,000Hz
d.	Pulse Width (50%)	20ns
e.	Rise Time (10% to 90%)	2ns max.
f.	Fall Time (90% to 10%)	4ns max.
g.	Pulser Efficiency	90% min.

h.	Life	1000 hrs. min.
i.	Weight	2.0kg max.
j.	Volume	360cm^3 max.

II. TASK A

Breadboards of the power supply and modulator for the Task A pulse generator have been constructed. Before going to 30kV in oil or other encapsulant, testing at reduced voltage on the power supply and modulator breadboards has been initiated.

Presented in Figure 1 and Figure 2 are schematic diagrams for the power supply and modulator for the Task A pulse generator. The 30kV, 1200A, 125ns pulse will be formed by discharging a Blumlein circuit with a triggered spark gap. A ringing-choke dc-to-dc converter will charge the Blumlein circuit capacitors to 30kV by transforming the 28 volt input.

A. Task A Power Supply

In the Task A power supply, ringing-choke transformer T_1 will charge the Blumlein circuit capacitors to 30kV by converting the 28 volt input. To achieve maximum efficiency and minimum volume, the power supply was designed to provide a uniform charging current during approximately the full interpulse period (67msec for a Prr = 15Hz). The 30kV output will be formed by connecting the three secondary windings of transformer T_1 in series. Each secondary will consist of approximately 2500 turns of AWG38 wire wound around a separate

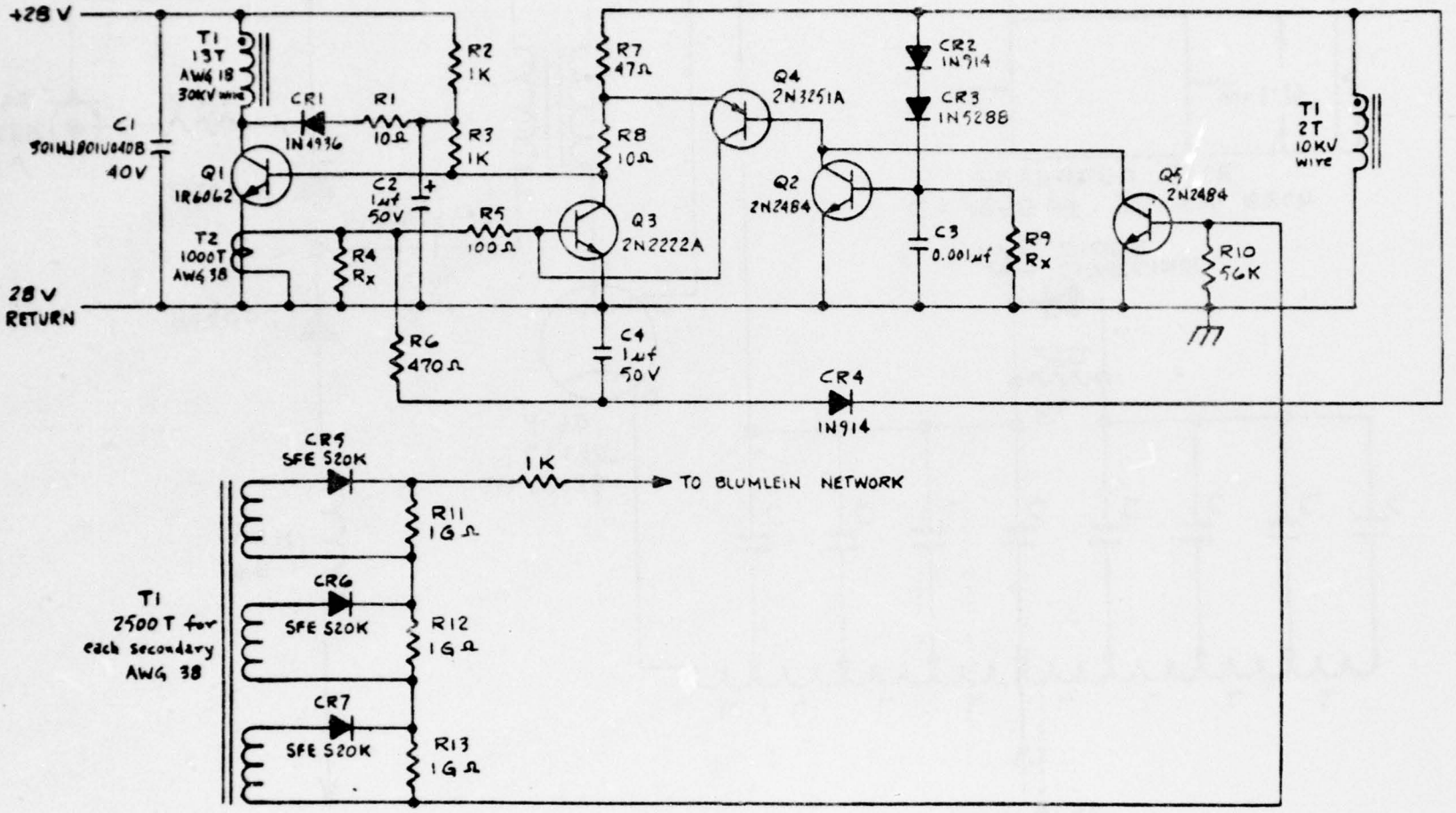

FIGURE 1
TASK A POWER SUPPLY

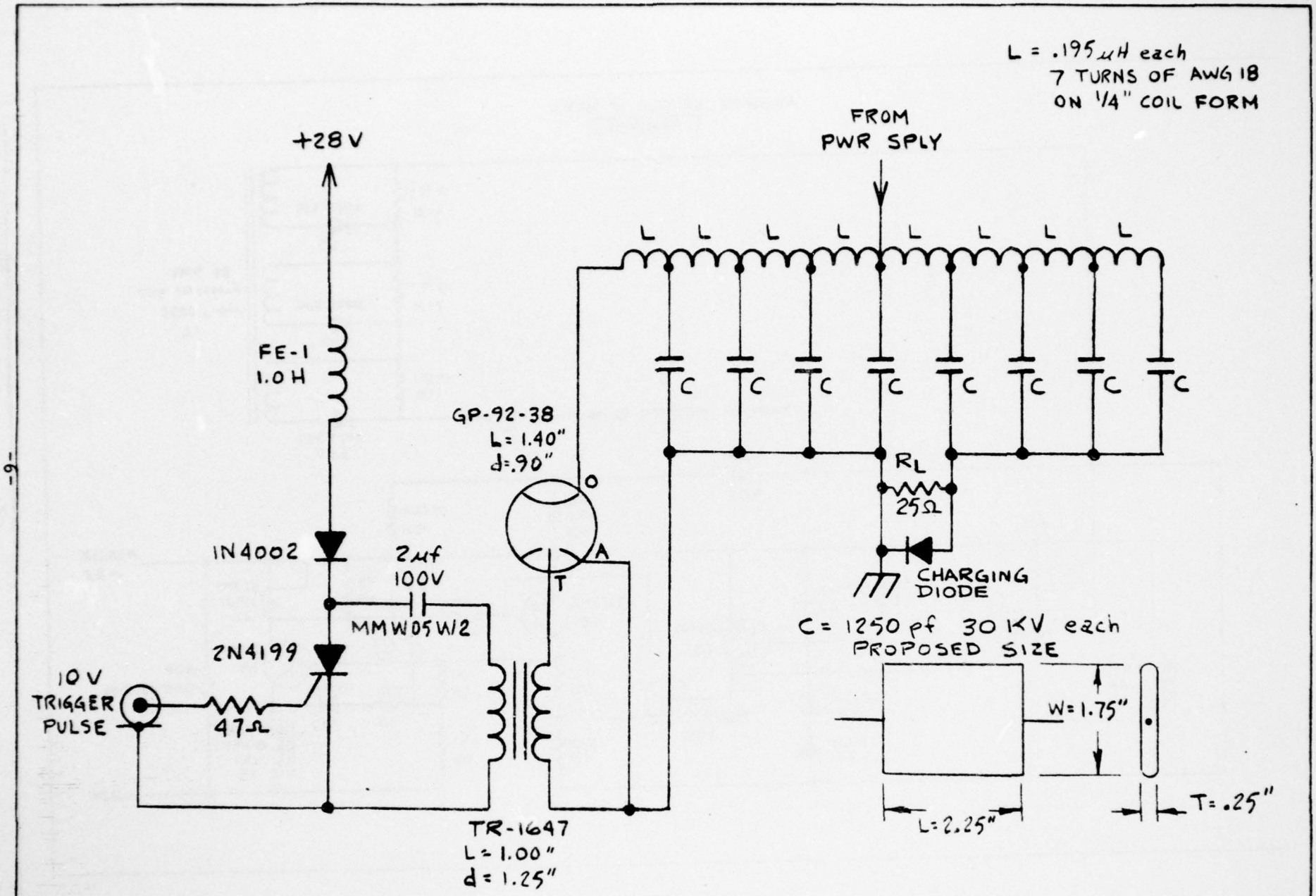

FIGURE 2
TASK A MODULATOR

molypermalloy powder toroid core. The primary winding will pass through the center window of all three cores and will be insulated to withstand the 30kV potential difference.

Testing on the Task A power supply breadboard was begun by modifying it for 10kV operation. The primary and control windings were wound on one of the three toroids to be used in the 30kV design. The intent of the testing was to operate the converter into a resistive load at a third of the final average output voltage (i.e. at 5kV) and at full current (i.e. at 5mA). When charging the Blumlein circuit capacitors, the charging voltage will rise linearly to 30kV during the interpulse period. As a result, the average output voltage is half the peak output voltage. The first toroid had a shorted secondary turn and had to be discarded. Using a second toroid, the converter was started. When operating the converter at 4kV, audible corona at the terminations of the fine secondary wire was noticed. An attempt to install corona rings at the low voltage and high voltage terminations resulted in an open in the secondary winding of the second toroid. Four new toroids wound with corona rings have been ordered. Until these cores are received, the third toroid is presently in the breadboard.

The Task A power supply was initially designed using

a high voltage Darlington transistor as the output switching device. A device with a high voltage rating was chosen for reliability reasons in the face of unknown switching spikes. This concern proved to be unfounded. To improve efficiency, low voltage transistors, which have faster switching speeds and lower saturation voltage, have been ordered and will be evaluated. Minor changes were made in the control circuit. Turn-off circuitry for the output transistor switch was modified so as to gain faster turn-off speed.

B. Task A Modulator

The 30kV, 1200A pulse, having a pulse width (50%) of 125ns, will be formed by discharging a Blumlein circuit with a triggered spark gap. Each network of the Blumlein circuit has a 12.5 ohm impedance. To approach the 20nsec rise time and 40nsec fall time requirement, each network has four sections. The high voltage trigger pulse will be formed by discharging a capacitor with an SCR. The capacitor is resonant charged to 56 volts from the 28 volt input. A trigger transformer, having a 1:250 turns ratio, applies the high voltage pulse to the trigger electrode of the spark gap.

The 1250 pF, 30kV capacitors in the Blumlein circuit have a significant effect on the size of the pulse generator for Task A. Capacitors, wound with mica

dielectric and foil electrodes, were received. The measured size of each capacitor was approximately 2-5/16" x 1-13/16" x 3/16". When a sample from the set of capacitors purchased was hipot tested at 30kV in air, leakage current flowing through the capacitor was insignificant when compared to the 5.0μA corona leakage current flowing through the air.

Testing on the modulator breadboard for Task A pulse generator was begun using a laboratory high voltage power supply to charge the Blumlein circuit capacitors through a current limiting, charging resistor. Preliminary tests on the Blumlein circuit are being performed at a 10kV voltage level. The intent of this testing is to evaluate the fidelity of the output pulse before going to the 30kV voltage level. To ensure reliable firing at the 10kV voltage level, the E.G.&G. GP-91 triggered spark gap, having a static breakdown voltage of 12.5kV, has replaced the GP-92-38, having a static breakdown voltage of 38kV. A pulse current transformer monitors the pulse current through the ground connection of the 25 ohm load, constructed from 2 watt carbon composition resistors.

An open circuit voltage of 10kV was measured at the secondary of the trigger transformer. The trigger transformer output was applied to the trigger electrode of the

GP-91 triggered spark gap to discharge the Blumlein circuit at a pulse repetition rate of 15Hz. Pulse currents of approximately 400A were measured through the 25 ohm load with the Blumlein circuit charged to 10kV. The modulator is undergoing further evaluation and refinement.

III. TASK B

Tests were conducted to evaluate the operation of an ITT 7621 hydrogen thyratron at reduced filament power. An SCR-magnetic modulator has been designed and will be evaluated.

A. Thyratron Evaluation

A test breadboard was constructed to evaluate operation of an ITT 7621 hydrogen thyratron at reduced filament power. Normally, this thyratron is supplied with a common, internal connection of reservoir heater lead and filament heater lead. The 7621 thyratron was modified such that the reservoir heater leads and filament heater leads were brought out separately. At a filament heater voltage of 6.3 volts, filament heater current was 1.65A. At a reservoir heater voltage of 6.3 volts, reservoir heater current was .45A.

The 7621 thyratron served as a discharge switch for a pulse forming network (PFN) charged to 8kV. The PFN was designed to provide a 100ns pulse to a 1250 ohm load. The pulse repetition rate was 5KHz. Filament heater voltage was reduced to 5.0 volts which resulted in a filament heater current of 1.5A. Reduction in the filament heater voltage resulted in a gradual in-

crease in the delay and eventual disappearance of the high voltage pulse. In discussions with engineering personnel at ITT, mention was made that filament heater power in the 7621 thyratron affects the heating of the hydrogen reservoir. Triggering of the grid electrode is affected. Further evaluation of this breadboard has been deferred in favor of designing and evaluating an SCR-magnetic modulator to meet the requirements of Task B pulse generator.

B. SCR-Magnetic Modulator

To meet the requirements for the Task B pulse generator, an SCR-magnetic modulator has been designed. Presented in Figure 3 is a schematic diagram of the SCR-magnetic modulator. A brief discussion of the operation and features of the SCR-magnetic modulator follows.

The cycle of the SCR-magnetic modulator begins by resonant charging low voltage storage capacitor C_2 to 56 volts from the 28 volt input by applying an input trigger to SCR_1. Upon completing the charging of capacitor C_2, an input trigger is applied to SCR_2 to resonant discharge capacitor C_2 through saturating transformer T_1. Saturating transformer T_1 transfers the energy from capacitor C_2 to the PFN capacitors and steps up the low voltage input to 10kV. Upon completing the

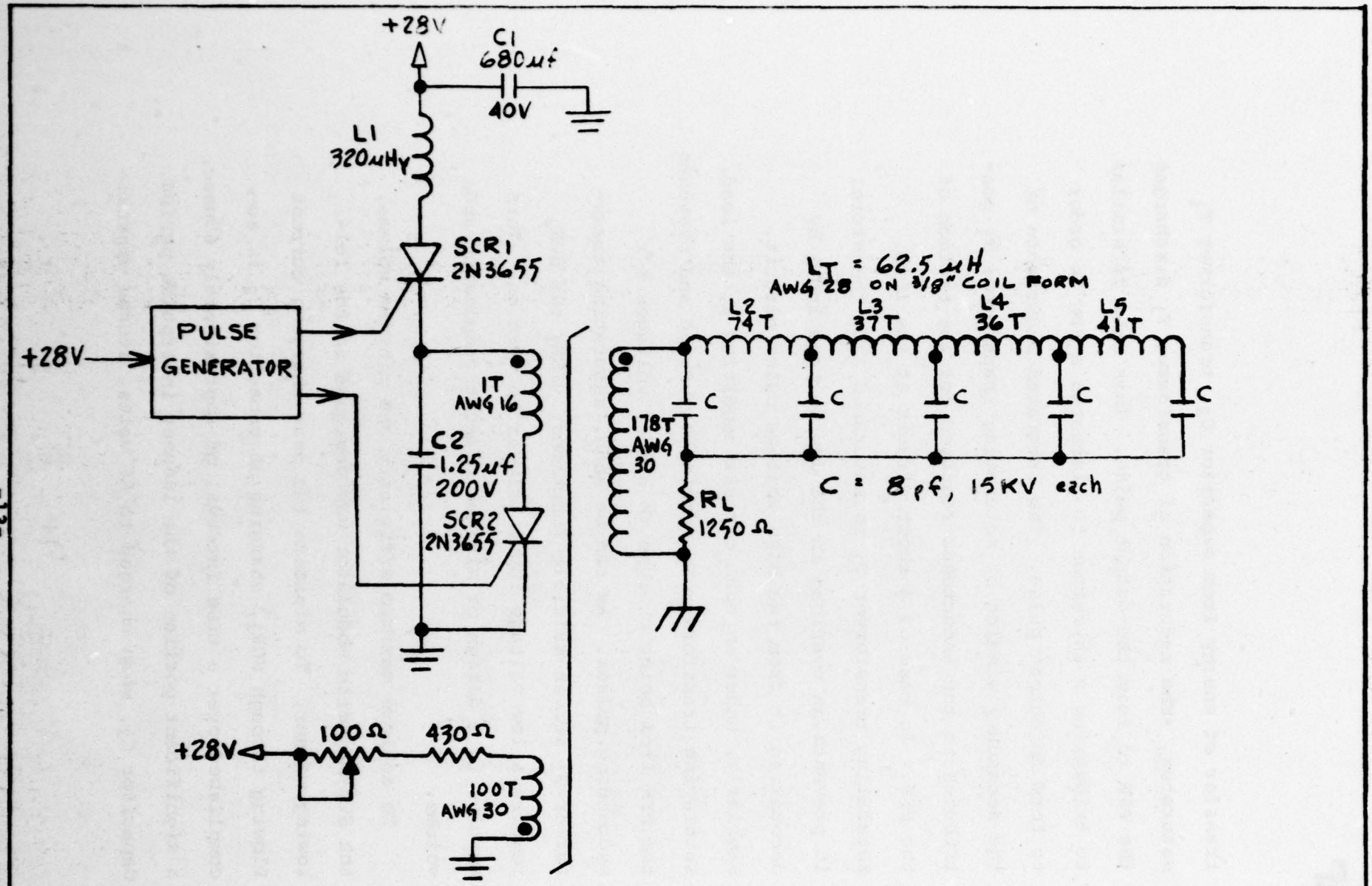

FIGURE 3
TASK B MODULATOR

transfer of energy from capacitor C_2, transformer T_1 saturates. The saturation of transformer T_1 discharges the PFN to form the output pulse. This step is similar to triggering a thyratron to discharge a PFN in order to form an output pulse. The saturated inductance of the secondary winding of saturating transformer T_1 contributes to the inductance required for one section of the PFN. In case of a short circuit at the load, saturating transformer T_1 is saturated and, therefore, it prevents an overload in the low voltage input by decoupling it from the high voltage pulse circuit. Similarly, under an open circuit condition at the load, saturating transformer T_1 remains saturated and prevents the PFN from being charged to higher voltages for succeeding pulses. As can be seen, saturating transformer T_1 serves multiple functions. SCR_1 and SCR_2 require a low voltage input trigger to turn on. This results in a design of minimal circuit complexity and volume.

To achieve maximum efficiency and minimum volume, the SCR-magnetic modulator was designed in the following manner. To minimize the peak charging current flowing through SCR_1, charging of capacitor C_2 is accomplished over a time interval of approximately 63μsec, a significant portion of the 100μsec interpulse period. Capacitor C_2, when charged to 56 volts, stores approxi-

mately the energy required to charge the PFN capacitors to 10kV in order to form a 100nsec pulse into a 5kV, 4A load. Capacitor C_2 is a subminiature, low dissipation factor, metallized polypropylene unit. Saturating transformer T_1 is wound on a tape wound toroid core using a grain-oriented 50% nickel - 50% iron alloy having a 1/2 mil strip thickness. The very square hysteresis loop of this core is utilized to quickly discharge the PFN when the voltsecond capacity of transformer T_1 is reached. For maximum efficiency, the design of saturating transformer T_1 will be such that the core flux will reach saturation at the moment capacitor C_2 is completely discharged. The low voltage and high voltage termination of the secondary of saturating transformer T_1 are separated by approximately one inch. An adjustable bias through the dc control winding of saturating transformer T_1 compensates for component tolerances by setting the core flux to a specific level. To meet the 10nsec rise time and 20nsec fall time requirement, the PFN has five sections. Total network inductance is 62.5μH. Total network capacitance of 40pF is divided equally between five miniature ceramic capacitors. Total component volume is less than the specified requirement of 360 cm^3.

IV. TASK C

Three commercially available devices were evaluated to determine which was the most suitable candidate as a switch to meet the ultra high speed requirements of the Task C pulse generator. The VMP22 VMOS FET, the 2N5271 avalanche transistor, and the GA301 nanosecond SCR were evaluated in test circuits using these devices in a series arrangement. Presented is a brief discussion of the test results.

Figure 4 shows the test circuit for the VMP22 VMOS FET. A desirable characteristic of the VMOS FET,when compared to the avalanche transistor and nanosecond SCR, is that the input gate controls the output pulse width. Each VMP22 device was stressed at 100 volts by applying 200 volts to the series combination. When a TTL input was applied to the MH0026 clock driver, a positive 200 volt pulse was observed at the drain of FET Q_2. The transition time from 200 volts to 0 volts was approximately 8nsec. The measured rise time of the input pulse to the gate of FET Q_1 was also 8nsec. Further evaluation of the VMOS FET as an ultra high speed switch requires the design of a high speed driver, using discrete components, to charge the VMOS FET input capacitance.

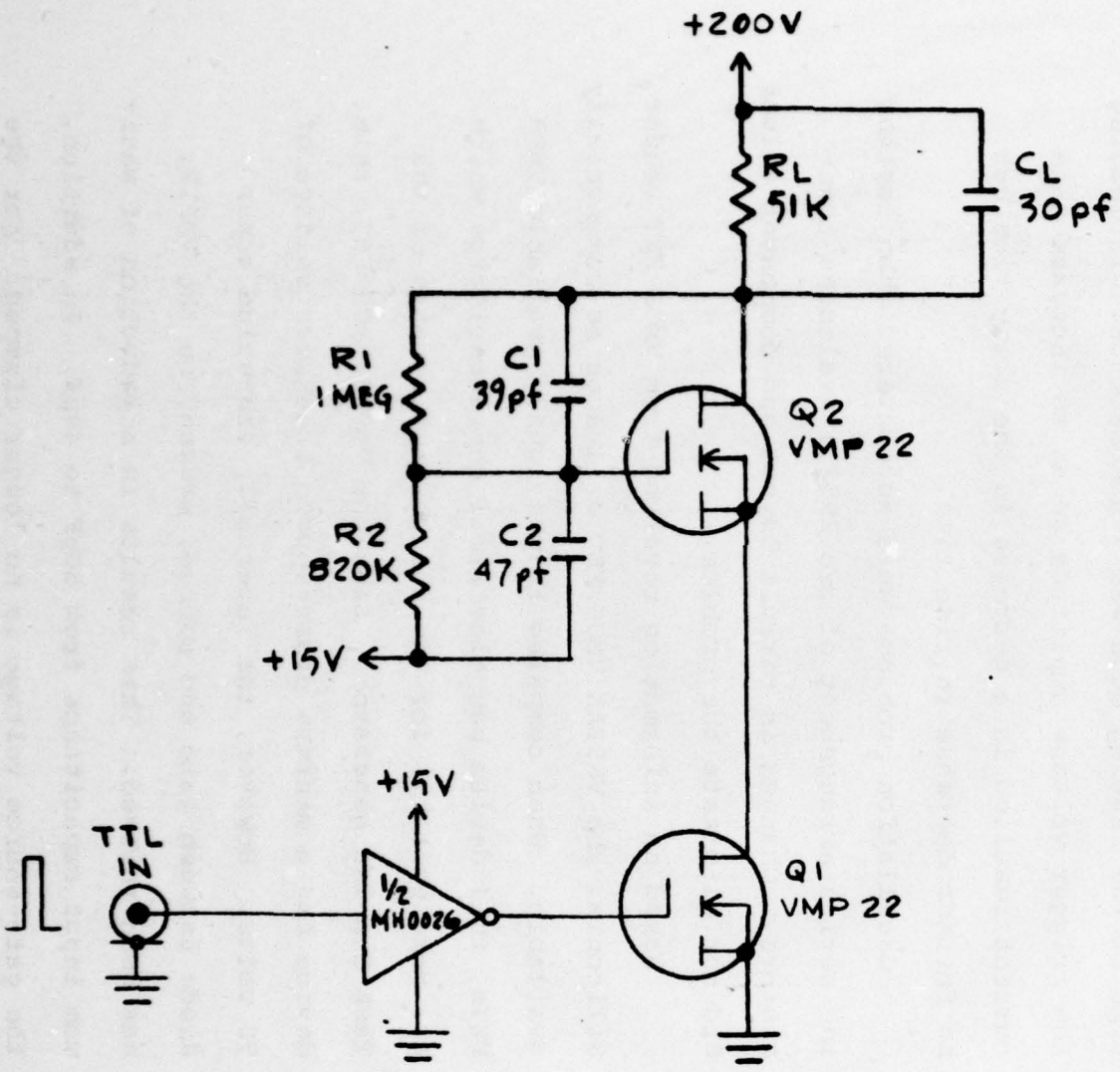

FIGURE 4

MOS POWER FET TEST CIRCUIT

Figure 5 shows the test circuit for the GA301 nanosecond SCR. Each GA301 SCR was stressed at 100 volts by applying 200 volts to the series combination. Upon applying a trigger pulse to the gate of SCR_1, a discharged pulse having a peak amplitude of 200 volts was observed across the 51 ohm load. The measured rise time of the leading edge was 7 nanoseconds. Increasing the trigger voltage amplitude so as to increase gate current resulted in a decrease in the delay time but no further decrease in rise time.

Oscillation problems were encountered when testing the series arrangement of two 2N5271 avalanche transistors. Changes in circuit layout and component values did not eliminate the problem.

Based on information received from VMOS FET vendor Siliconix, the VN98AK VMOS FET will soon be commercially available. When compared to previously available VMOS FETs, this device has electrical characteristics which are more suitable for the switch requirements of the Task C pulse generator. Like the VMP22 VMOS FET, this device has a minimum drain-source breakdown voltage of 90 volts. However, the internally connected zener diode between gate and source, present on the VMP22, has been removed. This results in a reduction of maximum input capacitance from 50pF to 40pF. In addition, the gate-source voltage is no longer clamped. For the

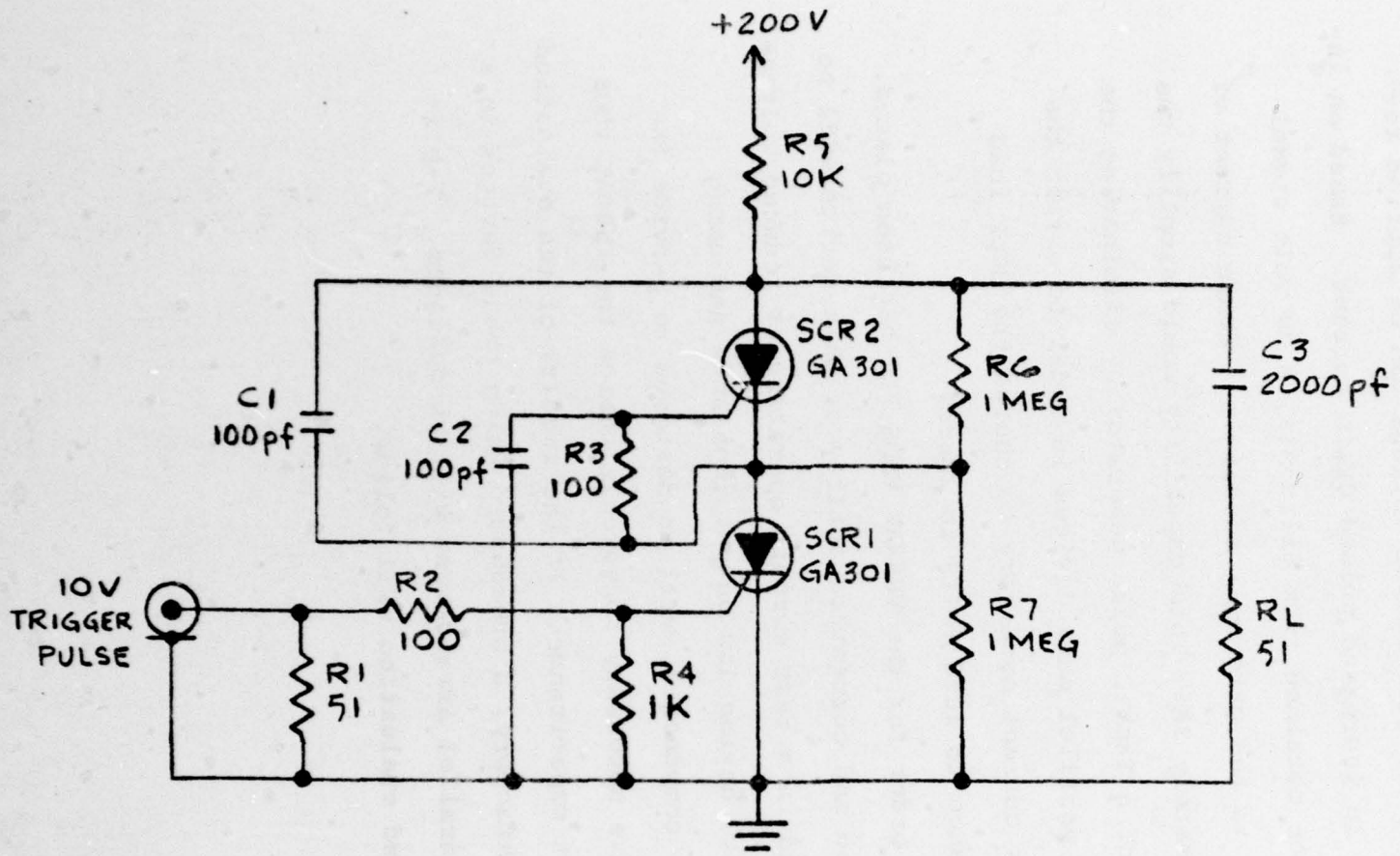

FIGURE 5

NANOSECOND SCR TEST CIRCUIT

low duty cycle requirement of the Task C pulse generator, higher pulsed gate-source voltage can be applied resulting in increased pulsed drain current. Based on information obtained from Siliconix, a 30 volt signal applied to the gate will result in a drain current of approximately 9A. This capability would simplify the design of a Task C pulse generator by eliminating the need to parallel many devices in order to obtain the 15A peak current necessary to charge the 30pF load capacitance to 1000 volts in 2nsec.

An order for the VN98AK VMOS FET has been placed. The speed and current capability of this device will be evaluated in a test circuit operating at reduced voltage. A circuit, having low output impedance and using discrete components, will be designed to provide the gate drive necessary to quickly charge the VN98AK VMOS FET input capacitance. If the results of the evaluation are satisfactory, a breadboard using these devices in a series-parallel arrangement will be designed. Fabrication and evaluation will follow.

V. CONCLUSIONS

A breadboard of the Task A pulse generator, consisting of power supply and modulator, has been fabricated. Total component size approaches the specified requirement of 360cm^3. Tests on the power supply and modulator breadboard have been initiated. Breadboard tests on the power supply, using one of the three toroids to be used in the 30kV transformer design, resulted in a 4kV output at 4mA into a resistive load. Breadboard tests on the modulator at 10kV resulted in a pulse current of approximately 400A at a pulse width of 125ns.

A breadboard design of an SCR-magnetic modulator for the Task B pulse generator has been completed. The design utilizes a saturating transformer to transform the low voltage input to high voltage and subsequently to discharge a pulse forming network. Total component volume is less than 360cm^3.

Commercially available devices were evaluated in a series configuration to determine which was most suitable as a switch for the Task C pulse generator. For the VMP22 VMOS FET, a transition time of 8ns was measured for a 200 volt voltage swing. The transition time is presently limited by the gate drive circuitry. Further

evaluation of the VMP22 and other VMOS FETs as high speed switches requires the design of a discrete component, high speed driver.

VI. PLANNED WORK FOR THE NEXT PERIOD

Breadboard testing of the Task A pulse generator will continue. The power supply and modulator will be individually tested and then integrated at the 10kV voltage level. Following this, the Task A pulse generator will be encapsulated and evaluated at the 30kV voltage level. To meet the requirements of the Task B pulse generator, a breadboard of an SCR-magnetic modulator will be constructed and evaluated. To meet the requirements of the Task C pulse generator, an approach using VMOS FETs will be emphasized. Based on vendor information, the VN98AK VMOS FET will soon be commercially available. This device will be evaluated and, if satisfactory, a breadboard using these devices will be designed and evaluated.