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TOPOLOGICAL CIRCUIT LAYOUT

by

W. M. vanCleemput

(see back page for 1473)

October 1976

Technical Note No. 99

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Departments of Electrical Engineering and Computer Science

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ABSTRACT

In this report the topological and geometrical aspects of the circuit layout problem are compared. A circuit layout procedure, based on topological factors, is presented. Whereas most circuit layout procedures are concerned mainly with geometrical aspects, the method described in this report attempts to find a topologically feasible solution to the problem first. From this topological layout, a physical layout is obtained in a second phase. This method can be especially useful for problems where a complete (100%) layout is mandatory.

INDEX TERMS: Circuit topology, computer-aided design, design automation, integrated circuit layout, printed circuit layout, topological layout.

TOPOLOGICAL CIRCUIT LAYOUT

1. Introduction

In this paper the major characteristics of the topological and the geometrical aspects of the circuit layout problem will be investigated. Because of the inherent complexity of the circuit layout problem, most solutions perform the placement of components first and then route the connections independently. This may result in routing failures that could have been prevented. The topological approach takes into consideration the topological aspects of the circuit layout problem and can result in more optimal layouts. Such a layout procedure will be presented in section 6. This procedure is useful mainly for problems which cannot be handled easily with the classical placement/routing methods. Such is e.g. the case in the layout of integrated circuits, where components may be of varying sizes and shapes and where the number of interconnection layers is severely limited.

2. Geometrical versus Topological Aspects

The topological aspects of the circuit layout problem are related to the relative positions of components, terminals and interconnections. This includes the order in which the terminals of a component appear on its physical boundary as well as the possibility of routing connections over the area used by the component. The requirement that the external connections have to appear on the outside boundary of the circuit in a prespecified order is also a topological characteristic of the circuit layout problem. Sometimes, the order of terminals is not completely imposed upon the designer: e.g., the inputs of a three-input AND gate are interchangeable. Assigning nets to logically equivalent pins is known as the pin assignment problem. A good circuit layout procedure should perform this pin assignment in function of an optimal layout.

Sometimes several logically equivalent components (e.g. NAND gates) are grouped together in a single physical component. Assigning groups of nets to these logically equivalent subcomponents is known as the gate assignment problem. Again, in a good layout procedure, this should be done in function of the layout. The logical equivalence of terminals and subcomponents influences the layout of the circuit topologically.

The geometrical aspects of the circuit layout problem are related to parameters that can be measured. For layout problems one usually does not use the ordinary Euclidian metric, but rather the so-called Manhattan geometry, in which only vertical and horizontal line segments are allowed. The size of individual components, the thickness of conductor lines and the size of a printed circuit board or an integrated circuit chip are examples of geometrical parameters.

An important geometrical characteristic is the concept of finite wiring capacities. These occur when the number of connectors in a given area is limited by geometrical considerations. Such is e.g. the case for the number of wires one can route between two adjacent terminals of a component.

Finite wiring capacities also occur when components can only be placed in fixed locations of a printed circuit board. Such a restriction usually results in a less-routeable board since topologically feasible connections might be unrouteable due to geometrical constraints.

3. The Classical Approach

Most procedures for solving the circuit layout problem first position the components thereby minimizing an objective function. This function should be a measure of the quality of the final layout. Usually the total wirelength is the parameter one tries to minimize. This tends to cluster together heavily connected components and to shorten the longest wires, which are desirable side-effects. Once the placement is obtained, it is frozen and the routing of connections has to be performed within this fixed-component topology.

Gate assignment is usually done before the placement phase while pin assignment is often deferred until the interconnection routing phase.

The routing of interconnections is frequently done sequentially using algorithms such as Lee's [Le61] or Hightower's [Hi69a]. Sequential routing inherently raises the question of selecting the order in which interconnections should be routed. This problem was studied by Abel [Ab72]. In this study it was concluded that router performance, measured in function of the ideal total wirelength, is independent of the order in which the connections are routed. This conclusion is valid only when the number of geometrical obstructions far exceeds the number of topological obstructions (the terms geometrical and topological obstruction will be explained in more detail, later in this section).

When finite wiring capacities are a limiting factor then geometrical obstructions tend to be the main reason for routing failures. In printed circuit board layout, routing completion is desirable but not essential. In IC layout however, all connections must be routed completely. Since there is no technological need for placing components in fixed locations, finite wiring capacities are not the main reason for routing failures.

Algorithms that allow some degree of parallellism in the routing phase were proposed in [HS71] and [MS72], but these algorithms are applicable only to a restricted class of problems. The cellular routing technique, proposed by Hitchcock [Hi69b] allows some flexibility in the relative position by interconnections but the position of an interconnection with respect to the already placed components is not determined in function of an optimal layout.

In the classical approach, both the topological and the geometrical aspects of the circuit layout problem are not fully taken into account. In the routing phase it may be impossible to route a connection in a given routing plane. This failure may be cuased by one of the following:

1) Congestion: An interconnection cannot be routed because of because of limited wiring capacities (geometrical obstruction).
2) Topological obstruction: some connections may be routed in topologically different ways. However, choosing a particular topological embedding may reduce the ability to route other connections. This problem is illustrated in Fig. 1, where four components, labeled A, B, C and D connected by two nets {2,7}

and {1,3,4,5,6,8}. The layout shown in Fig. 1(a) shows the possibility of embedding both nets in the same plane. In Fig. 1(b) the net {1,3,4,5,6,8} has been embedded differently, thereby making it impossible to embed {2,7} in the same plane.

3) Inherent non-planarity: No embedding in the plane exists. This only occurs when no interconnections are allowed under or over the area used by components.

The classical approach has proven successful in the layout of multilayer printed circuit boards with a regular structure. When multiple interconnection layers are available and when a given interconnection can be realized in more than one layer (through the use of vias), then the occurrence of topological obstructions is not of a critical nature. Furthermore, total completion of all interconnections, although desirable, is not essential for printed circuit boards.

However, for problems with components of varying size and shape and one or two layers of interconnections the classical approach has often failed to produce satisfactory solutions, especially when 100% routing completion is desired.

4. The Topological Approach

The main concern in solving the circuit layout problem is to embed the connections in one or more planes, such that no two connections intersect. This criterion shows a striking similarity with the planarity concept in graph theory: a graph is planar if it can be embedded in the plane such that no two edges intersect.

The topological approach is based on graph-theoretical concepts and first constructs a graph model for the circuit. This graph represents the topological aspects of the circuit as faithfully as possible, while neglecting all geometrical information. This graph then is embedded in one or more planes. If some of the connections remain unembedded, one attempts to route them by making use of technological properties that could not be modelled by the graph. The final step consists of transforming the topological layout into a physical layout, that takes into account the geometrical properties.

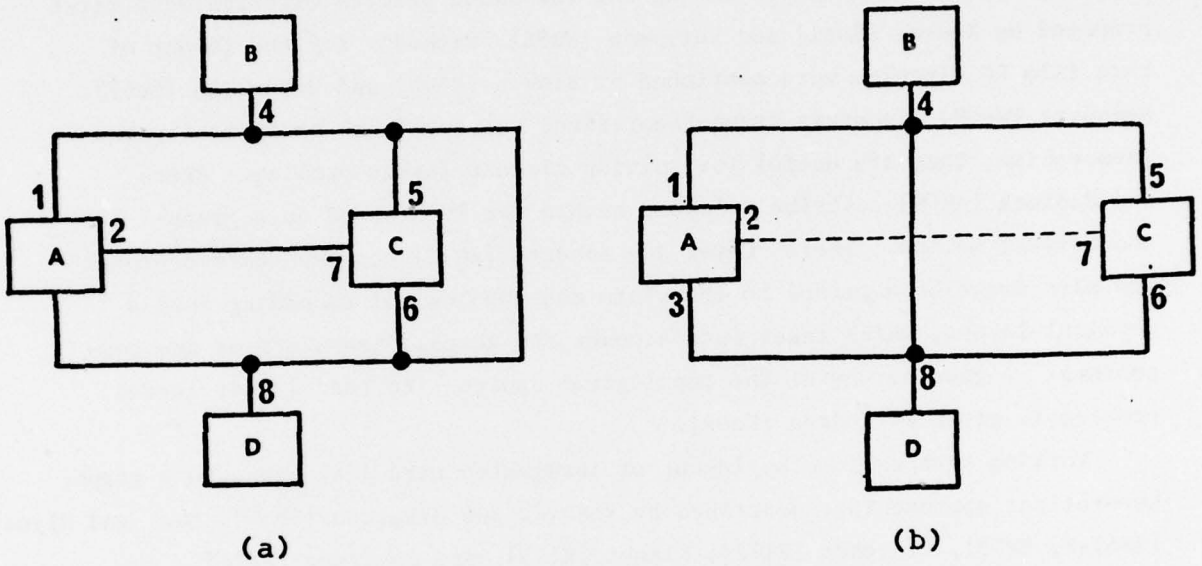

Fig. 1 Influence of Topological Obstruction Caused by Wiring Order.

In this approach, the topological parameters are considered at all stages, while the geometrical information is used only in the last phase of the layout.

Although several attempts were made to solve the circuit layout problem using graph-theoretical methods, working systems have appeared only recently.

Topological methods for laying out one-sided printed circuits were first proposed by Kodres [Ko61] and Weissman [We62]. Methods for the layout of thin film RC circuits were mentioned by Sinden [Si66] and Bedrosian [Be67]. Weinberg [We68] discusses graph-theoretical concepts such as planarity and isomorphism, that are useful for solving circuit layout problem. Akers and Hadlock [AH69] describe a layout method for IC's based on a graph-theoretical method. Akers, Geyer and Roberts [AG70] continue this approach and also describe a method to transform the topological embedding into a physical layout, which takes into account the actual dimensions of the components. A good survey of the topological approach to the circuit layout problem is given by Kodres [Ko69].

Working systems for the layout of integrated circuits, based on a graph-theoretical approach are described by Yoshida and Nakagawa [YN69], Engl and Mlynski [EM69ab, EM73], Fletcher [Fl72], Klamet [Kl73], and Sugiyama [Su74]. An effort to justify theoretically the models used is given by Engl and Mlynski [EM72abc, EM75] and by Vanlier and Otten [VO73].

A serious objection to topological layout methods is that they usually do not take into account any geometrical parameters, such as the number of wires one can route between two adjacent pins of a component or the capacity of a routing channel. As was indicated in [VL74], it is possible to take some finite capacities into account in a graph-theoretical model.

Some interesting results on transforming a topological embedding into a physical layout were reported by Zibert and Saal [Zi74], [ZS74].

Many existing systems for topological IC layout are limited to small-scale circuits. Because of the inadequacy of the models and algorithms employed, they often rely heavily on interaction for obtaining a final layout.

5. Graph Models for the Circuit Layout Problem

In [Va76] elaborate graph models are developed for the problem. These models are based on the concept of partially oriented graph (P. O. graph). In a P. O. graph, certain vertices (called oriented vertices) ahve an associated function that maps the set of neighboring vertices into itself. A P. O. graph is planar when it can be embedded in the plane such that for every oriented vertex the order in which its neighbors appear satisfies the function associated with that oriented vertex.

In the graph model so constructed nets are represented by star subgraphs (with the center being a non-oriented vertex) while components are represented by P.O. subgraphs.

The advantages of this model are:

1) No special constraints have to be imposed on the planarity testing and graph embedding algorithms.
2) Under certain conditions, it is possible to model physical equivalence of terminals as well as logical equivalence of terminals and subcomponents, such that these properties can be used for achieving an optimal layout.

A simple circuit and its P.O. graph model are shown in Fig. 2 and 3.

A disadvantage of this model is that it does not permit connections to be routed under (or over) the area used by a component, during the initial topological layout. However, since routing in this area is severely constrained by geometrical considerations, this disadvantage is not of a serious nature. Moreover, the routing of connections under (or over) the area, used by a component can be done topologically, while respecting finite wiring capacities, once a preliminary topological layout is obtained. A method for doing this was presented in [VL74].

The restriction of not allowing wires to be routed under or over the area occupied by components in the initial P.O. graph model was motivated by the following. Suppose that there were no constraints caused by finite wiring capacities (and that wires can be routed under or over the area occupied by components) then all interconnections can be laid out in a single layer since a collection of trees is always planar. From such a layout one could derive a layout that respects the finite wiring capacities between the terminals

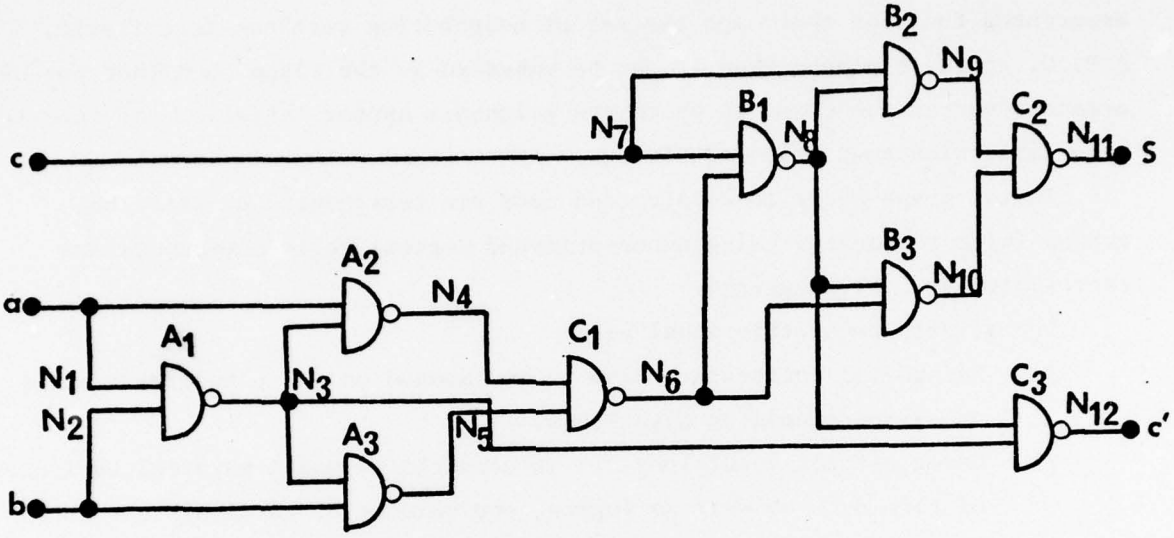

Fig. 2 Full Adder Circuit.

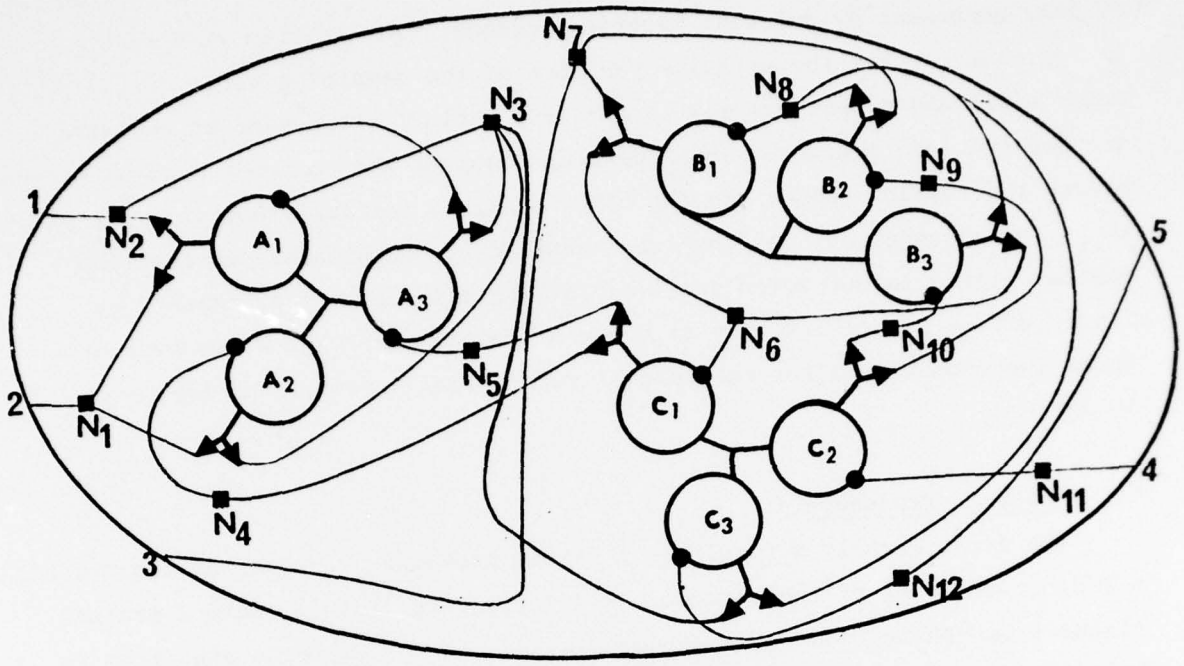

Fig. 3 Graph Model for the Circuit of Fig. 2.

of some component by deleting interconnections. The problem with such an approach is that the relative position of the remaining wires w.r.t other wires and components may be far from optimal after some of the wires are deleted. Furthermore, this approach requires the components to be placed before the routing phase. On the other hand, by initially not allowing wires to be routed under or over the area occupied by components, one can find a maximal planar layout while still satisfying all constraints imposed by finite wiring capacities. By allowing a limited number of wires over or under the component after the initial topological layout, this layout can be improved.

6. A Layout Procedure

The first step in a topological layout procedure consists of constructing a P.O. graph model of the circuit, as described in [Va76]. Next a maximal planar subgraph is found and embedded in the plane. Since no algorithm is known for efficiently finding an optimal solution, a suboptimal solution is obtained in time $O(n^2)$, where n is the number of vertices in the P.O. graph model.

The basis for this procedure is an algorithm for testing the planarity of P.O. graphs in linear time. This algorithm is based on Tarjan's planarity testing algorithm. In order to construct a maximal planar subgraph, one starts with a known planar subgraph. In this case all edges belonging to component models plus a number of edges to make the subgraph connected will always yield a planar subgraph. Starting from this planar subgraph, one can add net edges one at a time if this addition leaves the remaining graph planar.

This results in a list of faces of the embedded P.O. subgraph plus a list of edges that were deleted from the original P.O. graph in order to make it planar. It should be obvious that the only edges that may be deleted from the P.O. graph model are those that represent nets.

The remaining P.O. subgraph, embedded in the plane, provides information on the relative position of components, terminals and interconnections in the first layer.

After a maximal planar subgraph has been embedded in the plane, components are still represented by sometimes complicated graph models, while some net

edges may have been deleted. In the further transformations of the circuit layout graph, these complicated component models are no longer needed. Therefore it is desirable to replace these component models by simple circuits. This results in performing gate and pin assignment.

Because of the restrictions inherent to the graph model (e.g. no connections allowed over the area of a component), some connections that were feasible may not have been embedded. It is possible to embed some of these connections topologically, using a technique proposed in [VL74]. This then yields a new list of faces of the P.O. graph plus a new list of non-embedded edges. From this maximal P.O. subgraph a preliminary physical layout is obtained for the first layer of interconnections. The P.O. subgraph really specifies the relative positions of components and terminals and can be used to place the components and route the interconnections it represents without routing failures. In order to avoid failures due to geometrical obstructions, it is necessary to provide for a large enough area.

In the case of printed circuit boards, where components have to be placed in predetermined fixed locations, this may be difficult. This is due to the fact that the spaces between components have finite wiring capacities. If this is the case, it may be necessary to remove some topologically feasible interconnections in order not to exceed the wiring capacities. In the case of regular printed circuit boards the geometrical obstructions are often the main cause for routing failures. In such cases the topological approach will yield far-from-optimal results. However, when there are no restrictions on where components can be placed, then geometrical obstructions are far less important.

The algorithm for deriving a preliminary physical layout from the topological layout takes into account the following constraints:

- vertices and edges, representing a component are embedded such that the geometrical characteristics of this component are respected.
- the edges representing nets have to be embedded as sequences of vertical and horizontal line segments.
- the external connections have to be placed on the periphery of the circuit in prescribed physical locations.

The basic outline of this algorithm is as follows.

1) Find the inside face of the graph [Start by labeling all faces adjacent to the peripheral circuit with a 1. Then, label with a 2 all faces not yet labeled that are adjacent to those with a label 1. Continue to do this until all faces are labeled. Select one of the faces with the highest label as the inside face.]
2) Embed the peripheral circuit as a rectangle with the external connections placed in the prescribed locations.
3) Break down the face into chains of one of the following types:
   a) already embedded chains.
   b) component periphery chains.
   c) net (interconnection) chains.
4) Let the plane be divided into a number of squares, called "slots", large enough to contain the largest component. Place each of the components, for which there is a type b chain in the current face, into a slot and embed the circuit, representing this component.
5) Consider each of the net chains: if no part of the net has been embedded so far, find an interconnection path that satisfies the prescribed orientation of the face. If a part of the net has been embedded, find an interconnection between the start-vertex of the chain and all vertices and pseudo-vertices* of the net embedded so far. Select the shortest of the paths so obtained.
6) If all faces have been embedded, stop; else, find the face, adjacent to the faces already embedded, that is the closest to the inside face. Go to 2.

While routing the net-chains, it is important that they be embedded in a well specified order, such that the physical embedding corresponds to the topological embedding. The algorithm, used for routing these net-chains, is based on a line-searching algorithm by Hightower [Hi69]. Its advantages

*A pseudo-vertex is a point on the physical embedding of an edge, where two orthogonal line segments join.

are fast execution and minimal storage requirements, while its disadvantage is that it does not always find a path. The reason for the routing algorithm to fail is that the routing is performed on a finite resolution grid. By routing one connection, one might block the only available path for a connection to be routed later. A careful implementation reduces this blocking to a minimum.

Hightower's algorithm is well suited for this problem. In a normal routing problem, the algorithm requires sorting and searching lists of already embedded vertical and horizontal line segments. These lists normally grow with the number of interconnections routed, making the algorithm less efficient while the routing proceeds. In this case, however, the drawing grows from the inside out. At any given stage, there is a periperal circuit of the drawing, corresponding to the sum modulo 2 of all faces embedded at that time. All connections already routed, that are on the inside of the periperal circuit, need not be searched since any new connection being routed can interact only with the current periperal circuit. This property improves the speed of the routing algorithm, especially for large problems.

The steps described so far, allow us to place the components and to route the connections in the first layer. For the second (and subsequent) layer(s) this procedure has to be repeated until all connections are routed. For each layer a new P.O. graph model is constructed. This model represents all the components and all the connections not embedded so far. From this P.O. graph a maximal planar subgraph is then derived.

After the preliminary physical layout of the first layer, the positions of the components are fixed with regard to each other. Therefore, for the second and subsequent layers, an additional step is required to check whether the topological layout, obtained for these layers is compatible with the placement of the components.

This is accomplished as follows. Once the components are placed, all terminals have fixed location. This defines a cellular structure on the board. This cellular structure can be represented by a graph. With each edge of the graph is associated a wire routing capacity between two physically adjacent terminals. The maximal planar P.O. subgraph is then mapped onto this cellular

structure graph and if necessary edges of the P.O. subgraph may be deleted in order to obtain a topological layout satisfying the prior placement of the components.

Fig. 2 shows a circuit consisting of NAND gates, implementing a full-adder circuit. This circuit is to be implemented using 3 components, each containing three identical NAND gates. In this example, the gates have been a priori assigned to one of the components (A, B or C). The 3 gates in each component are logically equivalent (e.g. A_1, A_2, and A_3). The P.O. graph model for this circuit is shown in Fig. 3. The maximal planar subgraph for this circuit is shown in Fig. 4 and the corresponding preliminary physical layout is given in Fig. 5. The P.O. graph model for the rest of the circuit is shown in Fig. 6. Since this graph is planar, 2 layers will be sufficient here. Finally, Fig. 7 shows the mapping of the planar P.O. graph of the second layer onto the cellular structure graph.

From this preliminary physical layout, a final layout has to be derived. Usually, the area allocated for realizing the circuit in this procedure, is far too large and the final step consists of squeezing together the preliminary layout. In its current implementation the algorithm places components with a pre-determined orientation. As can be seen from the example the layout could be improved if component B were rotated. This is necessary for a final layout. Some work on this has been done by Zibert and Saal [Zi74], [ZS74].

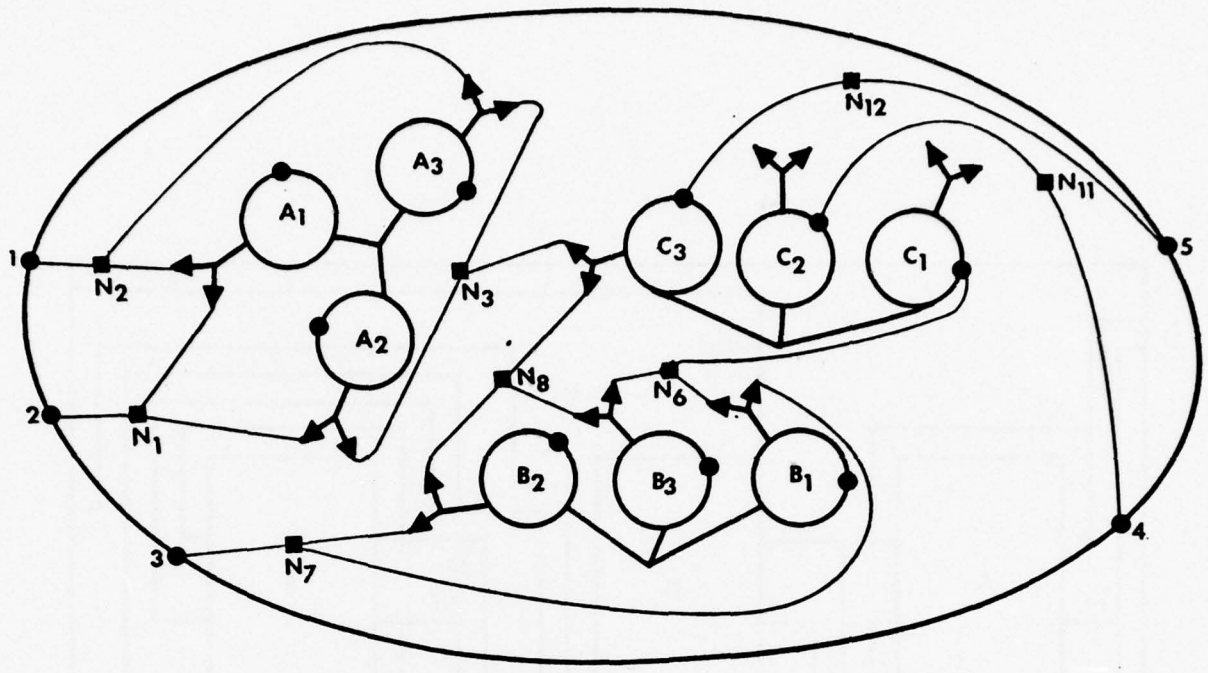

Fig. 4 Planar Subgraph for the First Layer.

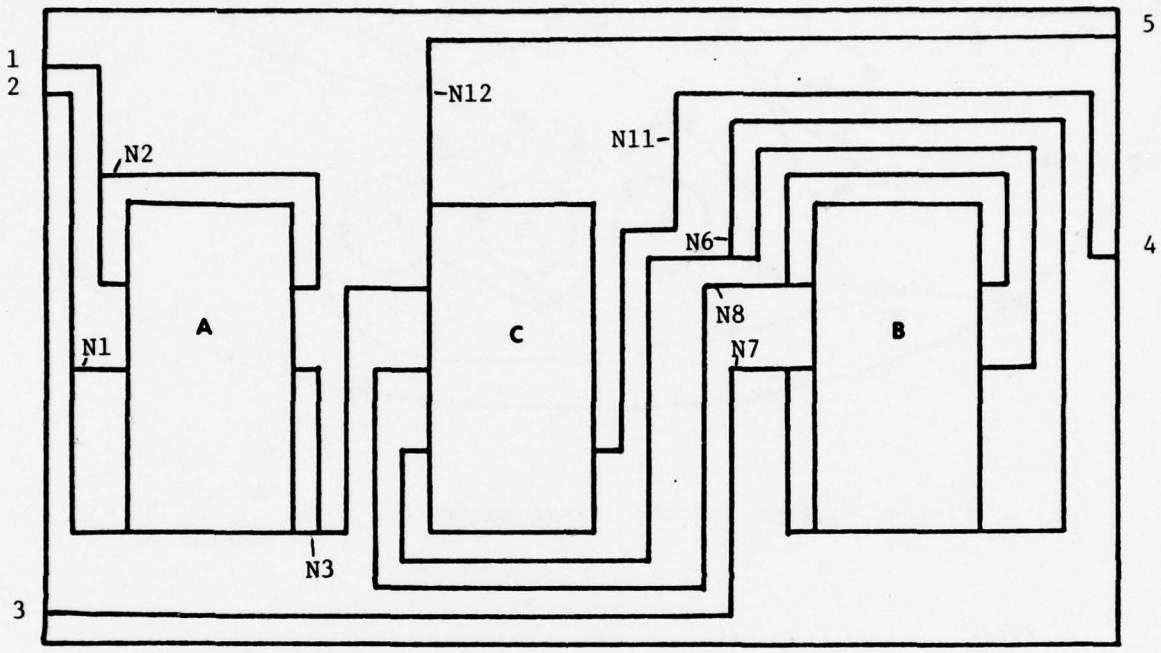

Fig. 5 Preliminary Physical Layout of the First Layer.

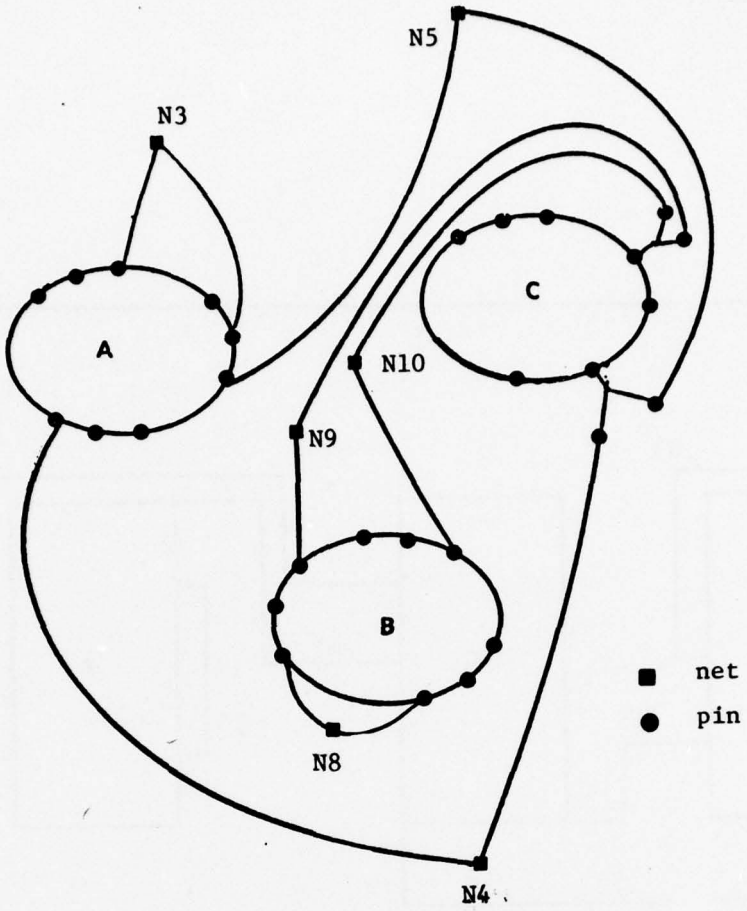

Fig. 6 Graph Model for the second Layer.

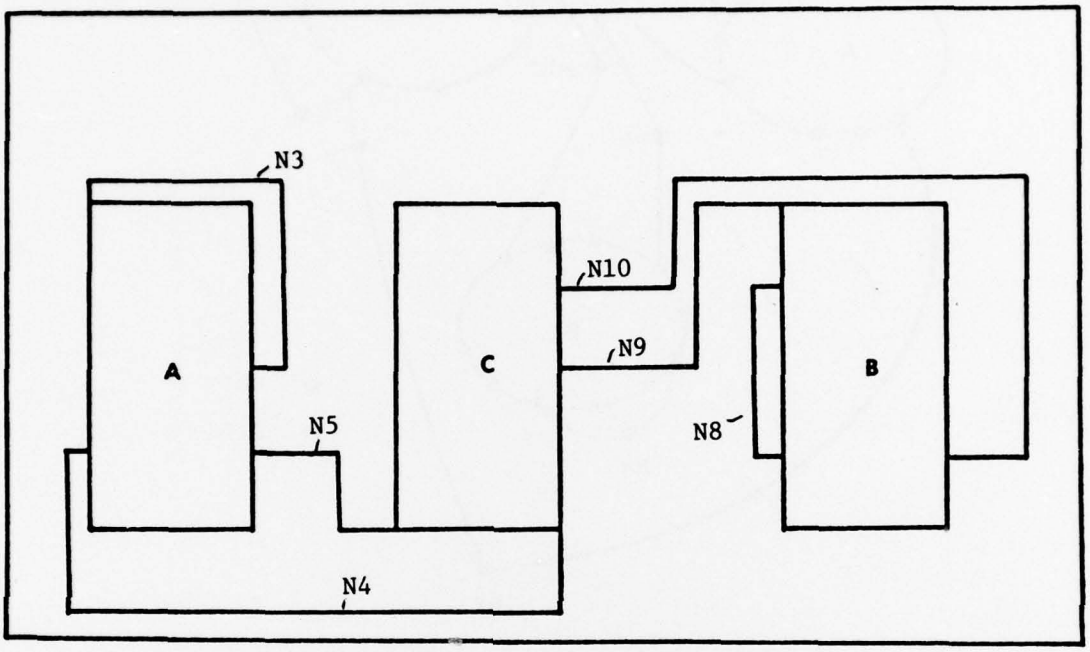

Fig. 7 Preliminary Physical Layout of the Second Layer.

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Circuit topology, computer-aided design, design automation, integrated circuit layout, printed circuit layout, topological layout.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

In this report the topological and geometrical aspects of the circuit layout problem are compared. A circuit layout procedure, based on topological factors, is presented. Whereas most circuit layout procedures are concerned mainly with geometrical aspects, the method described in this report attempts to find a topologically feasible solution to the problem first. From this topological layout, a physical layout is obtained in a second phase. This method can be especially useful for problems where a complete (100%) layout is mandatory.

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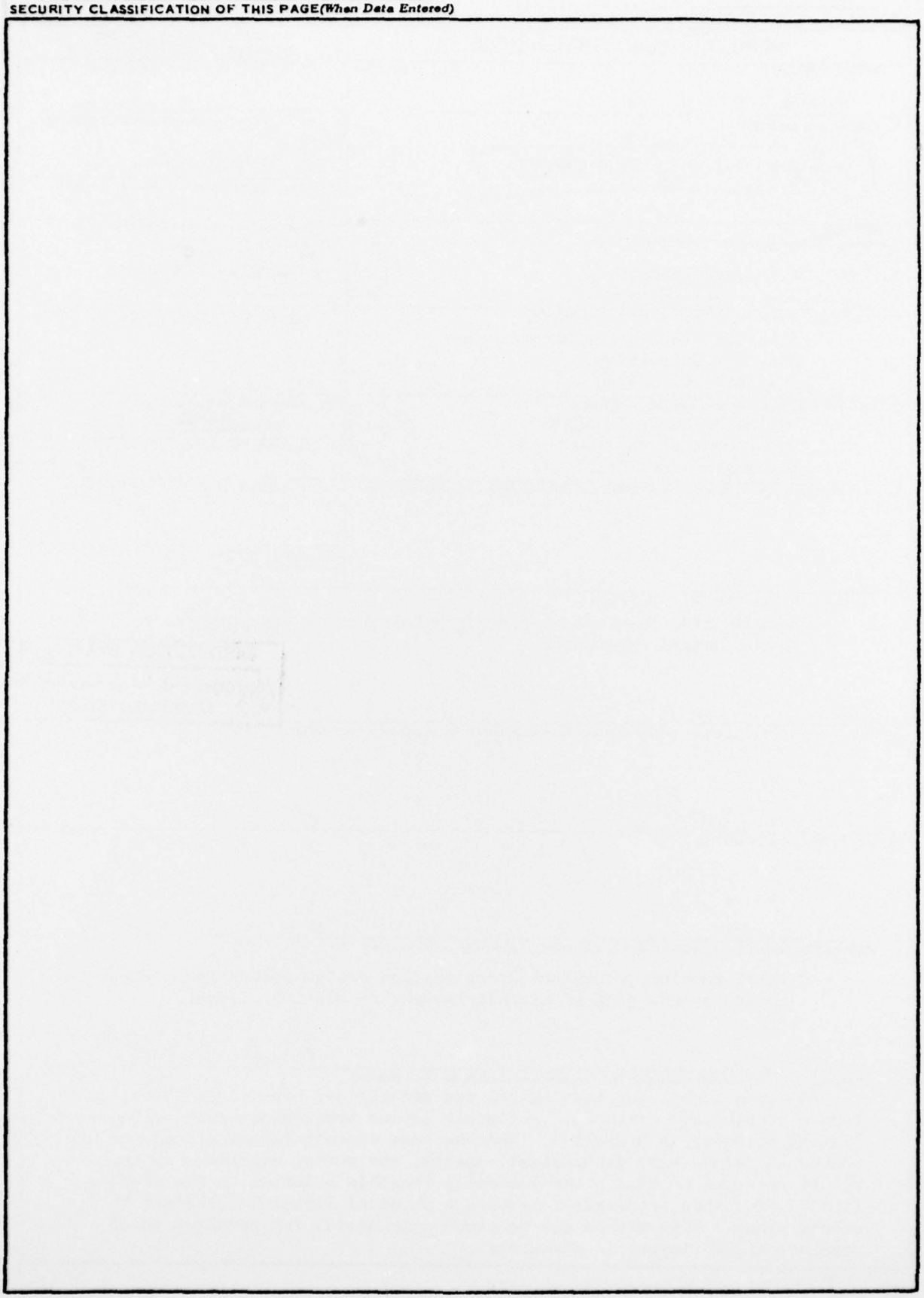

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