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A TELEVISION CAMERA INPUT AND DISPLAY OUTPUT BUFFER SYSTEM.(U)
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A television camera input and display output buffer system has been designed and partially constructed, consisting of a controller for selecting either of two camera inputs, a storage memory, a system controller and a run-length encoder. The memory is easily expandable and currently consists of 4096 8-bit words. The system performs a continuous display from the memory correctly interleaved with the incoming television camera input if desired. This display can take place simultaneously with input to the memory, displaying the old image while the new image is stored.

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SIGNAL PROCESSING LABORATORY

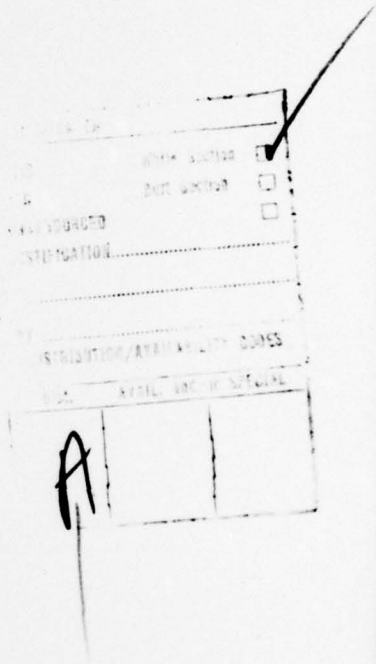
REPORT #16

A Television Camera Input and Display Output Buffer System

by

J.N. England

January 1977



NORTH CAROLINA STATE UNIVERSITY
ELECTRICAL ENGINEERING DEPARTMENT

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ABSTRACT

A television camera input and display output buffer system has been designed and partially constructed as of January 1977. The system consists of a controller for selecting either of two camera inputs, a storage memory, a system controller, and a run-length encoder. The memory is easily expandable and currently consists of 4096 8-bit words. The system controller selects a rectangular section from any portion of a 512 x 512 digitized image. The section may be of any size from 512 x 8 to 1 x 1 to 8 x 512. The system performs a continuous display from the memory correctly interleaved with the incoming television camera input if desired. This display can take place simultaneously with input to the memory, displaying the old image while the new image is stored. The memory system allows maximum DMA rate transfers to and from an Adage AGT/30 host computer.

Introduction

A flexible television camera and display buffer (Fig. 1) was designed so that images from two Fairchild TC-177-RL television cameras could be used as input devices for the Adage AGT/30 computer system. All components for the buffer system are on hand and most of the system has been constructed. The final interfacing to the Adage AGT/30 computer has not been completed, however. This delay is primarily due to the amount of effort needed in recent months to maintain the aging AGT/30 system in running condition. The Signal Processing Laboratory member responsible for the Adage system simply has

not had enough free time to design and construct the interface for the television buffer system. Hopefully this will be accomplished during Spring 1977, so that actual results of implementation of the ideas contained within this report may be published later this year.

1) Television input - Two television cameras have been modified so that they may be externally synchronized and remotely controlled. Referring to Fig. 2, the cameras are connected to a wide-band (10 MHz) video switch which selects, under computer control, one or the other camera for output to a 10 MHz analog-to-digital converter. The television input system generates all system timing - 9.4444 MHz pixel sample clock, 15.75 kHz horizontal sync., and 60 Hz vertical sync. The pixel sample clock is synchronized by the horizontal sync signal so that 512 pixels may be sampled per horizontal line. The digitized video is converted by the analog-to-digital (A/D) converter at this maximum rate or at some computer selected slower rate. The A/D 8-bit output is the input signal for the buffer memory.

2) Buffer memory - In order to make the buffer memory system (Fig. 3) as useful as possible, it was designed to display as well as store television images. Input to the memory may be from the two television cameras (via A/D converter) or from the Adage AGT/30 main memory (via interface controller). The buffer memory output continually refreshes a television display (via a D/A converter) and also is connected to the AGT/30 main memory for image acquisition. In this manner, the

results of CPU image manipulation may be displayed if so desired. The memory is made with bipolar Random Access Memory (RAM) elements so that no memory refresh time is necessary. The memory configuration is flexible and presently consists of 4096 8-bit bytes (TV I/O) or 2048 16-bit words (CPU I/O). It is designed to be easily expandable.

The buffer memory may operate in either a read-only mode (for input to CPU and display) or in a read-then-write mode (for display while inputting an image). The memory operates basically as a 16-bit, 200 ns cycle read-modify-write storage.

3) Image controller - The buffer memory is controlled by a very flexible address sequencer (Fig. 4). The basic pixel sample clock (9.4444 MHz) may be divided by some CPU selected NH so that (512/NH) pixels per horizontal line resolution is available. The CPU may also set NV so that (512/NV) horizontal lines per television frame resolution is selected. In addition, the CPU has control over the number of samples per line and the number of lines per frame as well as location (address) of the block of samples. For example, a 64 x 64 sample block may be obtained either from a small segment ($\frac{1}{64}$) anywhere within a 512 x 512 resolution image or as an entire 64 x 64 resolution image. Sample block size is not constrained to be square nor does it have to fill the buffer memory. Thus any image from 512 x 8 to 1 x 1 to 8 x 512 may be stored within the buffer memory. The buffer controller also allows CPU access to any 16-bit word within the buffer memory.

4) Run-length controller - Since the buffer memory is constructed separately and is connected to the buffer

controller through data and address buses, any auxilliary controller may be added to the system on a plug-in basis. A memory controller for run-length coded input and output has been designed for the system (see Fig. 5). Construction of this controller will be delayed until other operational tests determine the type of run-length input decision to be used. The designed system uses a horizontal thresholded absolute difference decision function. The input television image is coded as 8-bit intensity and 8-bit run length. No special code is used to indicate start of frame or start of line as these functions are taken care of by the output run-length decoder or by the CPU. A special code is used to indicate end-of-field, however, since run-length coded records may be of variable length. The total storage capacity of the run-length coded buffer is dependent, of course, on the image statistics but a worst-case size of 32 x 64 pixels is available. Typically, 4 to 16 times this size could be stored.

The run-length controller is designed to operate in conjunction with the image controller so that window size and resolution are selectable by the CPU for input as well as output.

The run length display decoder is a fairly simple latch and counter circuit for holding the output intensity as long as necessary.

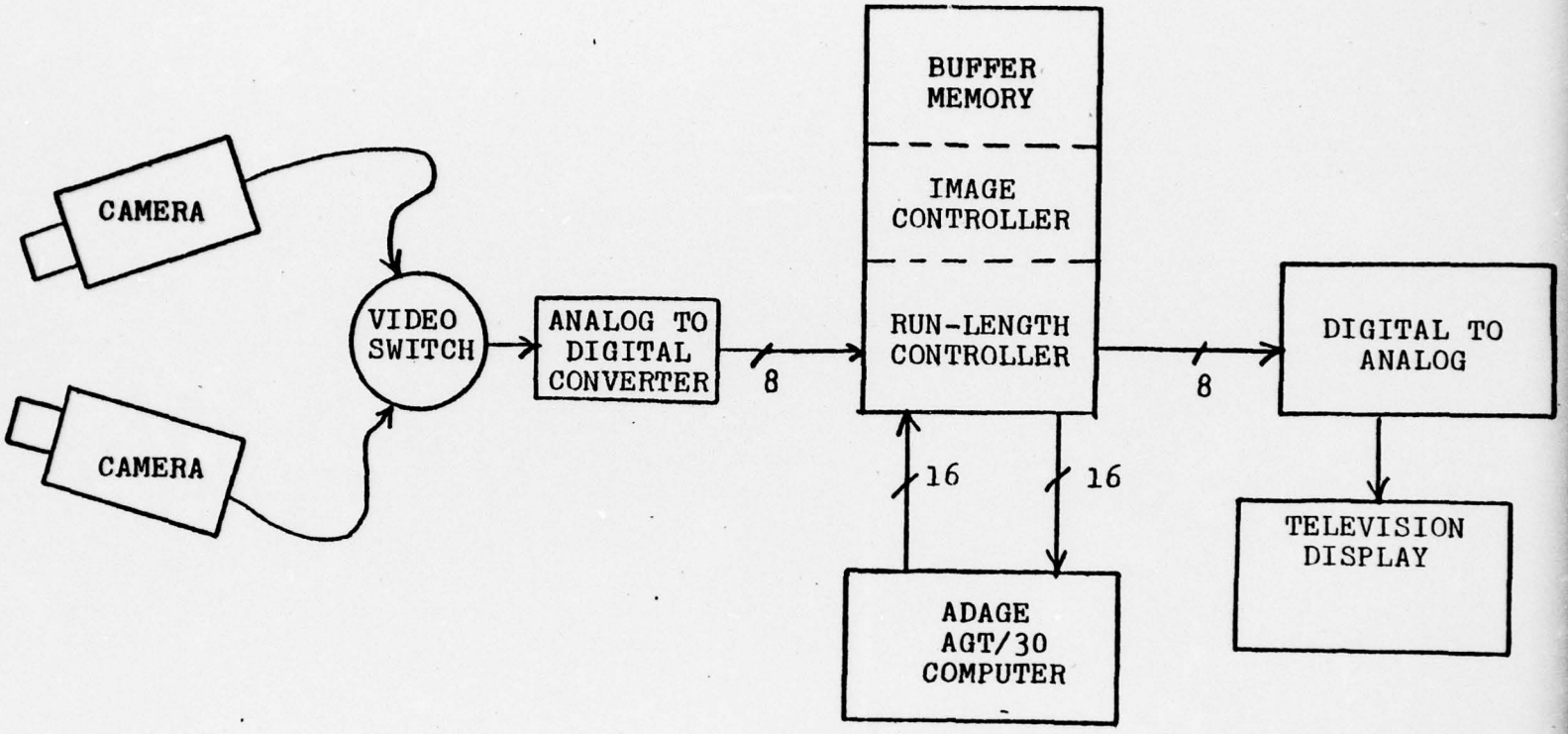

Figure 1 Image input and display system

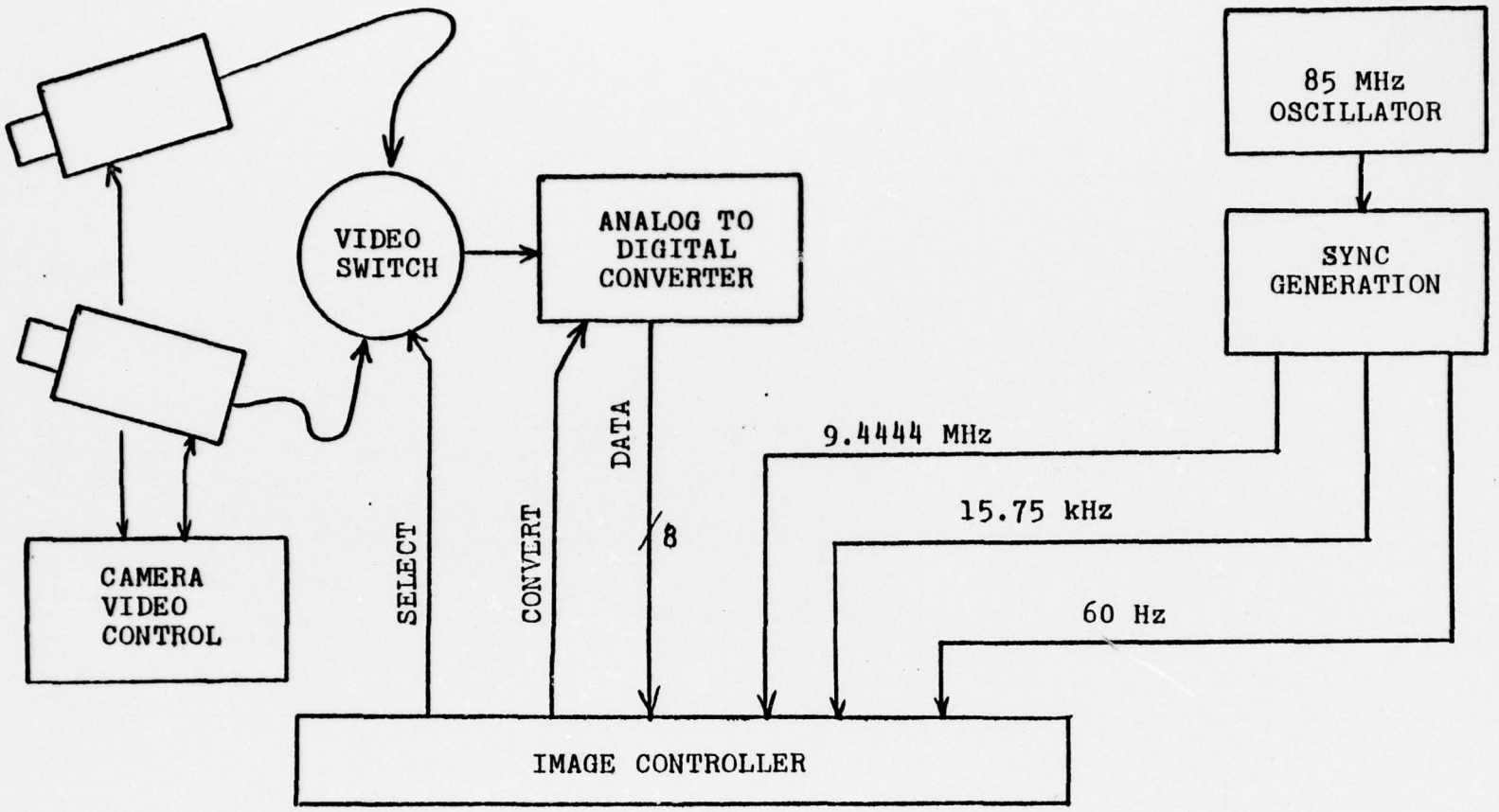

Figure 2 Camera input and control

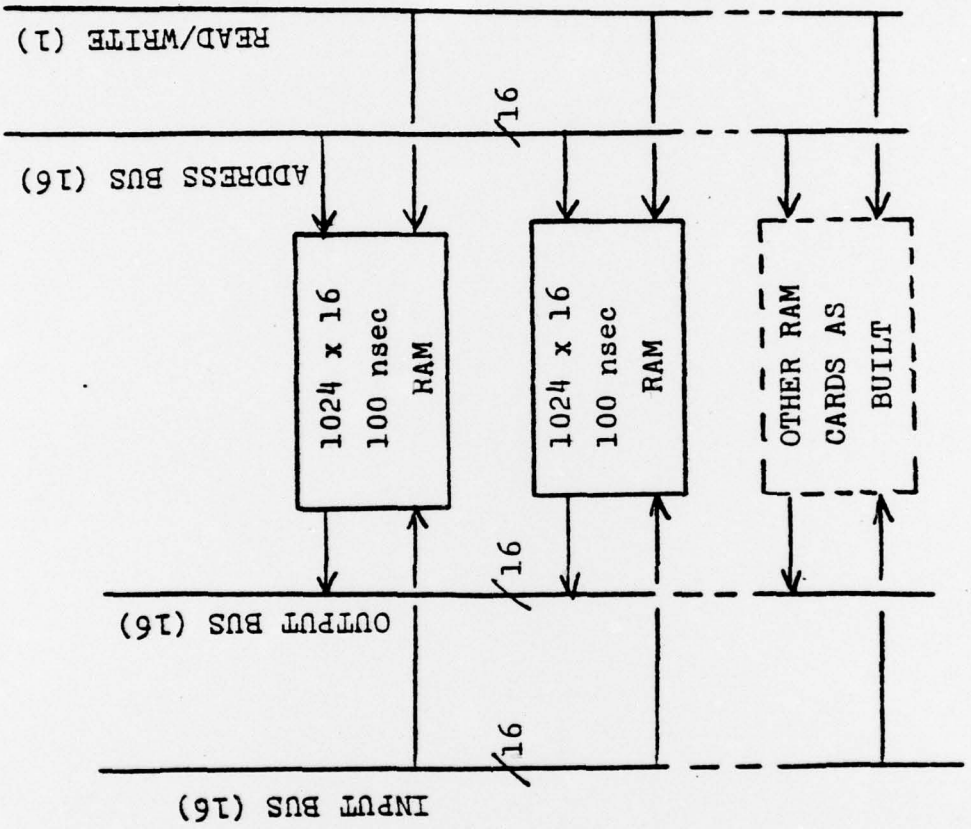

Figure 3 Buffer memory

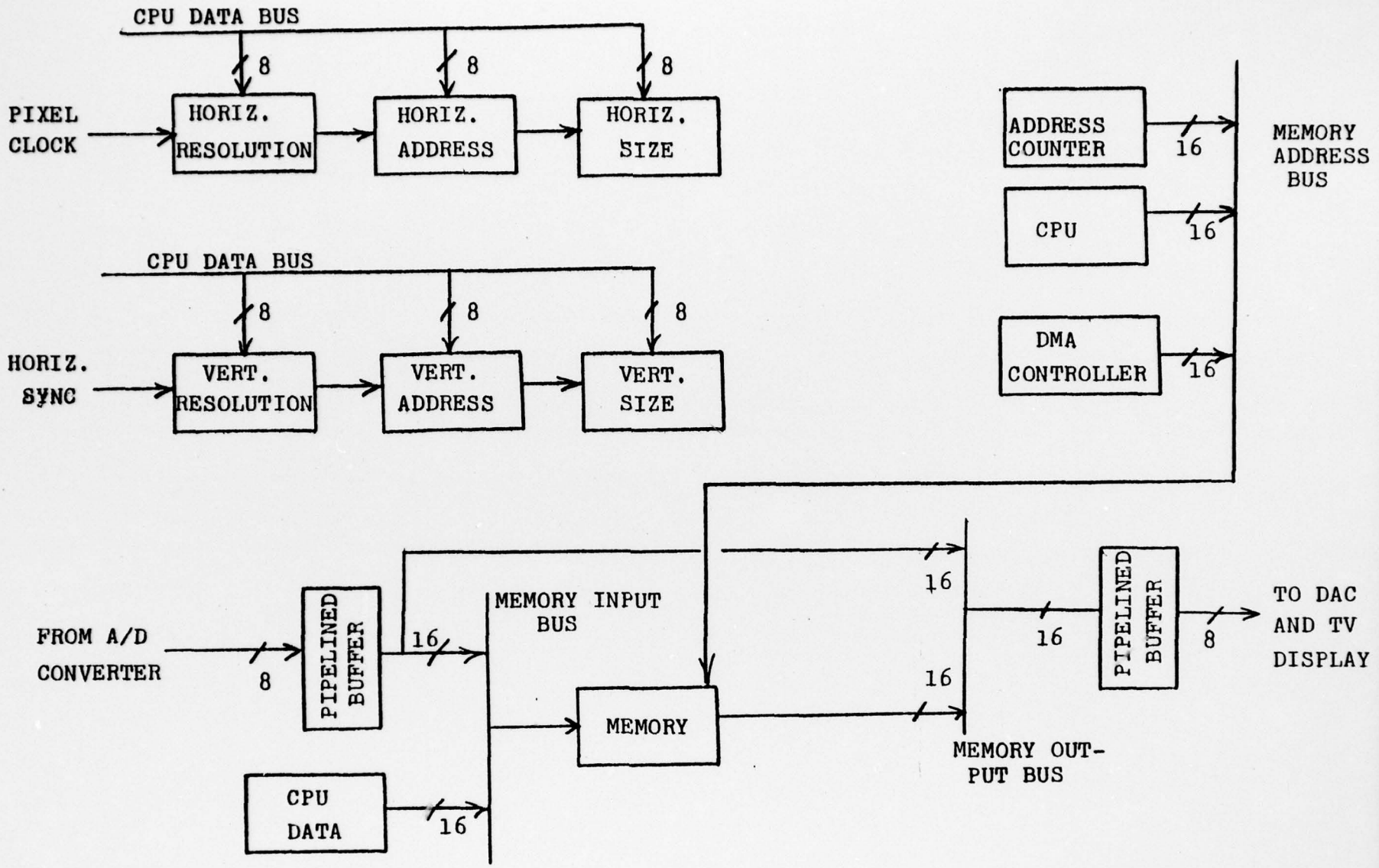

Figure 4 Image controller

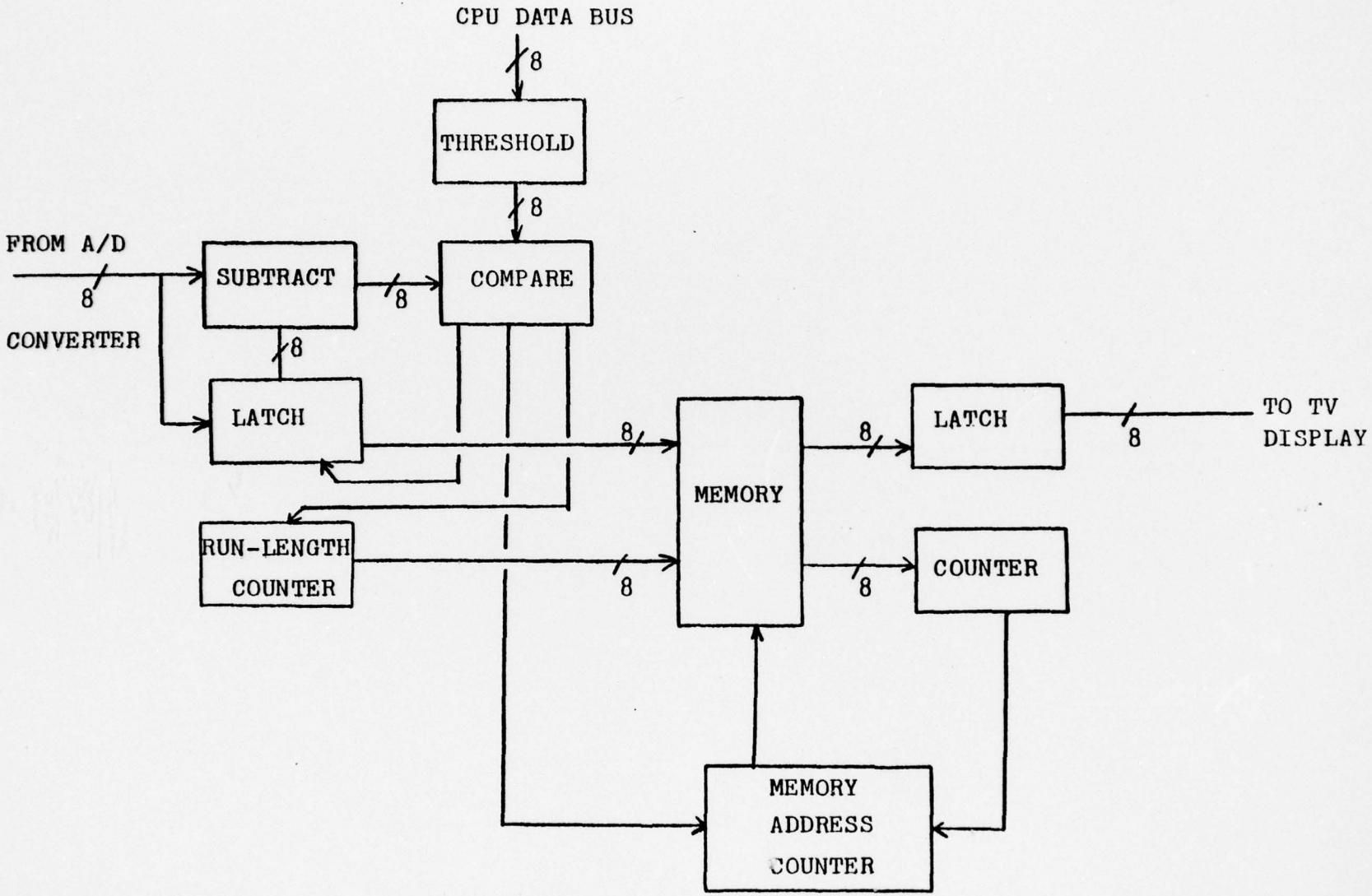

Figure 5 Run length controller