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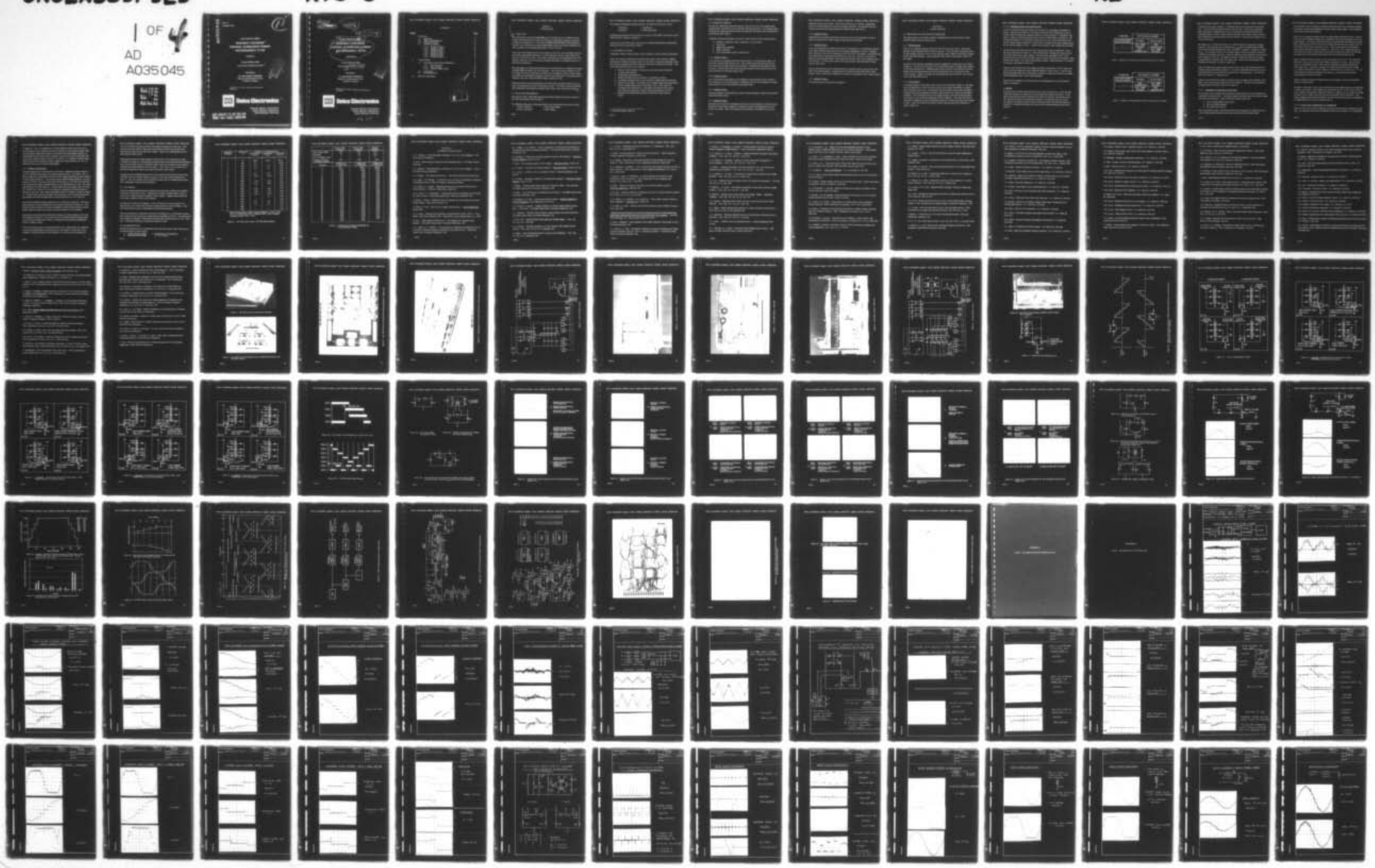

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FINAL TECHNICAL REPORT

FREQUENCY CONVERTER PORTABLE, ALTERNATING CURRENT MULTIFREQUENCY, 10 KW

VOLUME III

Contract CDRL Item A002

Contract No. DAAK02-72-C-0210

Submitted to

U.S. ARMY MOBILITY EQUIPMENT
Research and Development Center
Fort Belvoir, Virginia

Delco Electronics

General Motors Corporation
- Santa Barbara Operations
Santa Barbara, California

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CONTENTS

SECTION I
INTRODUCTION

1.1 OBJECTIVES

The initial phase of the project ~~(Item 0001)~~ was the development of a breadboard circuit capable of performing all the electrical functions of a three-phase frequency converter, as defined in Attachment No. 1 of the contract. After demonstration of three-phase performance, the work scope was extended ~~(Item 0003)~~ to further develop the breadboard circuits to produce 10 kW of single-phase power at 60 Hz or 400 Hz.

Concurrent with development of the 10 kW frequency converter, Delco developed improved step voltage commutation methods for a 100 kW frequency converter under MERDC Contract No. DAAK 02-72-C-0338. Since some circuit advances were applicable to the 10 kW frequency converter, the work scope was enlarged ~~(Item 0004)~~ to incorporate the new circuits into the breadboard.

After three-phase and single-phase performance was demonstrated, an additional investigation ~~(Item 0005)~~ was added to the work statement. This involved demonstration of 15 kVA three-phase and 10 kVA single-phase operation of the breadboard, study of voltage regulation methods for operating the frequency converter from utility power, and performance of regulation tests with a Delco-developed voltage regulation system.

Additional inverter circuit developments (Item 0006) made it possible to replace the transistor step commutation circuits with thyristor circuits. The results of the investigations and developments of Item 0006 are included in this volume of the contract final report.

1.2 MAJOR ACCOMPLISHMENTS

The inverter of Item 0006 weighs approximately twenty pounds less than the inverter of Item 0001 and produces 50% more power.

The following components, costing about $1600, were removed from the inverter circuit:

4 Power Transistors	4 Power Zener Diodes
4 Driver Transistors	2 Power Diodes.

The following components, costing about $250, were added to the inverter circuit:

2 Thyristors	1 Transformer
2 Inductors	4 20mfd Capacitors.

Photographs showing the transition from the inverter of Item 0001 to the inverter of Item 0006 are shown in Figures 1 through 4.*

The inverter of Item 0006 comes much closer to meeting all performance requirements than the inverters of Items 0001 and 0005.

1.3 STATEMENT OF WORK

Modification P00008 amends the basic contract schedule to add Item 0006 as noted below:

"0006 The Contractor shall furnish all engineering, labor, tools, services, supplies, equipment and facilities to design, install, test and deliver improved performance, lower cost circuitry mounted in the 10 kW Frequency Converter furnished as CLIN 0001. This work effort shall include but not be limited to:

a. Memory Circuit Redesign – Widen power center and reduce the number of steps in the waveform.
b. Redesign Step Autotransformer.
c. Design and install Thyristor-Capacitor Commutation Circuitry.
d. Investigate and improve short circuit and 60 Hz, Single-Phase Performance.
e. Reduce Overall Weight – Incorporate circuit design changes where appropriate.
f. Perform Design Demonstration Performance Tests – Tests shall be in accordance with Attachment No. 3 and shall also include maximum power checks and tests necessary to enable a design extrapolation to 100 kW.
g. Document all technical effort and data for inclusion in final technical report."

* Illustrations begin on page 26.

1.4 SUMMARY OF RESULTS

The Item No. 0006 inverter has been tested to a power level of 27 kVA compared with a maximum power of 20 kVA for the circuit that used step transistors. The maximum power of the Item No. 0006 inverter has not been measured thus far because of the limitations of the laboratory power source.

Compared to the previous design, the Item No. 0006 inverter has these characteristics:

- No power transistors, driver transistors, or Zener diodes
- Lower cost
- Higher power capability
- Higher reliability
- More commonality of power switch devices.

1.4.1 Results of Task a

A new waveform was designed with these characteristics: 110° wide power center, 10° wide steps, total harmonic content 5.6%. This waveform permitted the removal of one set of steps from the step forming autotransformer, resulting in the elimination of four thyristors. The new logic circuit uses read-only memories with a total cost of $75 compared with $800 for the previous logic circuit.

1.4.2 Results of Task b

A new step forming autotransformer was designed for the 110° power center waveform. This transformer was assembled with E-I laminations and will be less expensive to manufacture than the C-core type transformer previously used.

1.4.3 Results of Task c

Thyristor-capacitor commutation for the step circuits successfully replaced the transistor commutation step circuits.

1.4.4 Results of Task d

New power center thyristor commutation circuits have been developed in which the energy stored in the commutation capacitor is essentially constant and independent of inverter current and voltage. This circuit improves commutation for all possible short circuit conditions at the inverter output. With the Item 0005 inverter, 60-Hertz, single-phase power was limited primarily by the step switching transistors. The thyristor step commutation circuit permits single-phase power outputs greater than 10 kVA.

1.4.5 Results of Task e

Replacing the step switching transistors with the thyristor step commutation circuit resulted in a total inverter weight reduction of approximately 20 pounds.

1.4.6 Results of Task f

Tests were performed in accordance with contract Attachment No. 3 and included maximum power checks and tests necessary to permit a design extrapolation to 100 kW. Maximum power tests up to 27 kVA were conducted at 60 Hz and 400 Hz, three phase. The performance tests indicate that all performance specifications can be met. However, verification of efficiency measurements should be made because of inherent errors in the method of measurement used. It is felt that the results of the measurements made during the investigation are conservative.

Inverter characteristics such as deviation factor and maximum short circuit current capability can be easily changed. Deviation factor is a function of input-output filter energy storage. Short circuit current capability is a function of commutation circuit energy storage.

1.4.7 Results of Task g

All technical data are documented in Appendix A.

SECTION II
PROJECT DETAILS

2.1 DESCRIPTION OF NEW INVERTER SUBSYSTEMS

The technical effort of Item 0006 resulted in modifications of the inverter power switch assembly and the memory timing circuits.

2.1.1 400 Hz Inverter

Figure 5 is a schematic diagram of the Item 0006 400 Hz inverter circuit. This circuit operates on the principle of "power factor correction." The output filter capacitance value is large enough so that the inverter current leads the output voltage by more than 35 degrees for all rated load conditions. The development of this circuit is described in Volume I of this report.

The power center thyristor commutation energy is supplied by voltage source V_B as shown in Figure 5. In previous circuits part of the commutation energy was supplied by a winding on the step autotransformer. Making the power center thyristor commutation circuit independent of the step autotransformer improves commutation for non-symmetrical short circuit currents. Figures 6 through 8 are photographs that show the bottom, top, and side views of the Item 0006 inverter.

2.1.2 60 Hz Inverter

A schematic diagram of Item 0006 60 Hz inverter circuit is shown in Figure 9. The significant developments for the 60 Hz inverter are the step voltage commutation circuit and the commutation boost circuit. The thyristor step commutation circuit made it possible to eliminate starvation commutation transistors with resultant lower circuit cost and higher reliability. The commutation boost circuit supplies energy to turn off the step thyristors and the power center thyristors during short circuit conditions. This circuit also has the advantages of supplying constant commutation energy for all values of inverter input voltage or load. A side view of the 60 Hz inverter with the required output filter capacitors is shown in Figure 10.

2.1.2.1 Explanation of Step Commutation Circuit

Current is transferred from one voltage level to another by a two-step commutation sequence. Assume that in Figure 11, thyristors SCR2 and SCRa are conducting current to the load, that the transformer polarity is positive, and that capacitor C is charged as indicated. In order to transfer the load current to level 1, SCRb and SCR1 are gated on. The discharge of capacitor C reverse biases SCRa and turns it off. SCR2 is turned off by the reverse voltage ringup of capacitor C, which leaves it charged at the proper voltage polarity for the next step change to level O. Load current continues to flow through SCR1 and SCRb.

The Item 0006 inverter generates two sets of step voltages which are defined as Y and X functions as illustrated in Figure 12. These functions have a fundamental frequency three times that of the inverter output voltages. The step widths and heights of the Y and X functions are derived from the 110^{o} power center waveform described in the Memory Timing Section of this report. The required commutation capacitor voltage polarities to commutate each step are also defined in Figure 12.

Figures 13a and 13d illustrate step voltage circuits that can generate Y and X voltage functions for all load voltage and current conditions defined in Tables I and II. Load currents must flow through either free commutation or auxiliary commutation circuits in accordance with the definitions of the Y and X voltage functions.

Operation of the auxiliary commutation double bus stepchanging circuit is illustrated in Figures 14 through 17.

Y Function

A portion of the Y function step forming circuit is shown in Figure 14a. On the left side of the step transformer is shown the free commutation step selector thyristors. On the right is shown the step selector thyristors that require an auxiliary commutation circuit. The right side thyristors are connected alternately to two separate busses (a) and (b). The auxiliary commutation circuit consists of thyristors SCRa and SCRb and capacitor C. Capacitor C is charged as indicated and load current is flowing through thyristors SCR1 and SCRa.

Y FUNCTION	STEP VOLTAGE & CURRENT	
STEP TRANSFORMER VOLTAGE POLARITY	IN-PHASE	OUT-OF-PHASE
+	AUX. COMM. REQUIRED	FREE COMMUTATION
-	FREE COMMUTATION	AUX. COMM. REQUIRED

Table I. Methods of Commutation for Steps Formed by the Y Function

X FUNCTION	STEP VOLTAGE & CURRENT	
STEP TRANSFORMER VOLTAGE POLARITY	IN-PHASE	OUT-OF-PHASE
+	FREE COMMUTATION	AUX. COMM. REQUIRED
-	AUX. COMM. REQUIRED	FREE COMMUTATION

Table II. Methods of Commutation for Steps Formed by the X Function

Turning on SCRb causes capacitor C to discharge and reverse biases SCRa (see Figure 14b). Load current then transfers from bus (a) to bus (b). The current of capacitor C takes three paths: it supplies load current, it forces current to flow through the non-conducting thyristor of step 1 during resonant discharge, and it forces reverse current to flow through SCRa during the junction recovery interval. At this time the capacitor is in series with the load.

(See Figure 14c.) At this time SCRa is off. SCR0 thyristors are triggered on causing capacitor C to be clamped across voltage source v_{step} and to resonant charge through a current path that flows through SCR1, SCRb, and SCR0. Capacitor C charges to a voltage Kv_{step}. K is a function of the Q of the resonant charge circuit and a function of load current and must be greater than unity. When the capacitor is fully charged it reverse biases SCR1 causing it to turn off. The capacitor now has a sufficient energy with the proper voltage polarity to commutate the next voltage step. Load current now proceeds to flow through SCR0 and SCRb, as shown in Figure 14d.

Figure 18a shows gate trigger timing for SCR1, SCR0, SCRa, and SCRb during the commutation sequence illustrated in Figure 14. The time relationship between the turn-on of SCRb gate and the removal of gate drive from SCR1 is defined as $\Delta\mu$sec. For the Item 0006 60 Hz inverter Δ equals 35 μsec.

Figures 15 and 16 illustrate transfer of current from one voltage level to another for all other Y and X function step voltage and current conditions. The same step commutation principles apply for all these cases as for Figure 14.

2.1.2.2 Explanation of Commutation Boost Circuit

The thyristor reverse voltage step commutation circuit provides the basic mechanism for turning off the step thyristors. Commutation capacitor energy sources are the step voltage taps of the autotransformer. Hence commutation energy varies with

1) The dc voltage applied to the inverter
2) The step voltage magnitude
3) The inverter load current.

When commutation energy is obtained only from the step transformer voltage taps the inverter cannot function with short circuit loads and cannot start with large loads.

A commutation circuit is required in which the energy stored in the commutation capacitor is essentially constant and independent of inverter load or input voltage. The commutation boost circuit performs this function.

Figure 19a is a schematic diagram of the basic step voltage commutation circuit. Required is a source of commutation voltage that is available for each step commutation cycle at the proper polarity. The energy transferred during each commutation cycle should be constant. These requirements are met by the circuit of Figure 19b that shows the energy source circuit connected to the step commutation circuit. These circuits operate as synchronous twin resonant loops with a common inductor L_1. Since the Y and X voltage steps for the 110° wide power center waveform used in the inverter change at the same time, both left and right steps are commutated with energy from the same boost voltage circuit.

Figure 20 shows the double resonant circuits in equivalent circuit form. The instant that thyristors B and R_{S3} are turned on the voltages of capacitors C_B and C_C add to provide a fast rise commutation current. Both capacitors discharge through the step thyristor commutation loop. Capacitor C_C charges to a voltage determined by the boost voltage V_B. Energy contributed by the step voltages or load current that exceeds $1/2\ C_C \cdot K \cdot V_B^2$ *is transferred via voltage developed across inductor* L_1 *and is subtracted from the* energy supplied by the boost circuit.

Figure 21 shows the important voltage and current waveshapes in the step commutation and boost voltage circuits.

Equivalent commutation circuits before and during the commutation sequence are illustrated in Figures 22a and 22b. The complete step commutation circuit for the Y and X step circuits is shown in the schematic diagram of Figure 23. Inductors L_2 are wound on a common permalloy core to couple energy from one step commutation circuit to the other. This energy coupling assures equal commutation currents for both step circuits by compensating for slight differences in circuit resistances and Q.

2.1.2.3 Power Center Commutation C.T. Transformer

Figures 24 and 25 are schematic diagrams of a power center thyristor commutation circuit loop. The difference between the two diagrams is the current transfer (C.T.) transformer

In Figure 24. The C.T. transformer is an autotransformer with a turns ratio of 1:5. The transformer action reduces current flow in the power center thyristor bypass diode and consequently reduces the maximum current flow in the commutation capacitor C_C. Photographs of bypass diode current, capacitor current, and reverse commutation voltages are also shown in Figures 24 and 25. Use of the C.T. transformer reduces bypass diode current from 95 amperes to about 45 amperes at a load of 16 kW, PF = 0.8, as illustrated in the current waveform photographs.

2.1.3 Memory Timing Circuit

The gate trigger time for each thyristor in the inverter schematic circuits of Figures 5 and 9 is controlled by the output of a read-only memory circuit. Five 256 bit (32 x 8) memory chips are programmed on the basis of the computer optimized waveform defined by the drawing of Figure 26. This waveform has the following characteristics: the power center is 110^o wide, each step is equal and 10^{o}wide, there is a 10^o wide zero dwell time. The total harmonic content (excluding triplens) to the 250th harmonic is 5.6%. The center step frequency is the 36th harmonic. The non-triplen harmonics greater than 1% are the 7th, 35th and 37th. Figure 27 is a chart showing the magnitudes of all non-triplen harmonics up to the 41st. Step voltage relationships between two phases are shown in Figure 28. The third step on the left and right sides of the power center are on simultaneously. Step changes on the left and right sides are made synchronously at a 10^o step rate.

The waveform design for the three phase format is illustrated in Figure 29. This three phase waveform is used to design the inverter master timing chart of Figure 30. Each thyristor switch in the inverter circuit is designated on the left and the sequence of gate trigger signals are shown as a function of waveform degrees up to 365 degrees.

Information on the timing chart is utilized to organize the memory timing circuit in the block diagram of Figure 31. Sets of thyristors are assigned to specific programmable read-only memory chips; each memory is controlled and synchronized by appropriate counter and delay circuits.

The memory timing circuit is constructed with five volt, medium power TTL integrated circuits and programmable read-only memories. The output of a 3.456 MHz crystal oscillator is divided to produce a clock frequency of 8.64 kHz for 60 Hz operation or

57.6 kHz for 400 Hz operation as shown in the schematic diagram of Figure 32a. Clock pulses are fed into counters (Figure 32b) which address the read-only memories that synchronously output thyristor gate drive signals. Figure 33 is a photograph of the complete memory timing circuit.

Photographs of unfiltered voltage outputs for the inverter at 60 Hz operation are shown in Figures 34 through 38. Measurements of total harmonic content and individual harmonics of the inverter output voltages are listed in Table III and can be compared to the computer-calculated harmonics tabulated in the last column. Note: there is a very close correspondence between the computer and measured harmonic content values.

Comparisons of the individual harmonics for the waveforms of the inverters of Item 0005, Item 0006, and a new MERDC-designed waveform can be made from the tabulations of Table IV. The new waveform will be considered in future inverter designs because of the lower magnitudes of the 5th and 7th harmonics.

2.2 CONCLUSIONS

It has been demonstrated that power transistor step commutation circuits can be replaced by thyristor commutation circuits. Consequently, the power ratings of power center inverters are no longer limited by transistor current ratings. It appears that practical inverter power ratings of 100 kW can be achieved.

All tasks of Item 0006 were completed. A new 110^{o} wide power center waveform was demonstrated. New power center thyristor commutation circuits were developed. A new step autotransformer using E-I laminations was fabricated and tested.

Tests were performed in accordance with contract Attachment No. 3 and included maximum power checks and tests necessary to enable design extrapolation to 100 kW. The performance tests tabulated in Appendix A indicate that all performance specifications can be met. However, verification of efficiency measurements should be made.

2.3 RECOMMENDATIONS

Additional development work in the following areas will lead to either lower circuit cost or to improved output waveform quality.

- Triplen attenuator design
- Input-output filter design
- Simplification or elimination of T_c^+, T_c^- circuit.

HARMONIC NUMBER	FREQUENCY Hz	PERCENT OF FUNDAMENTAL MEASURED* L-T-N	MEASURED* L-T-L	COMPUTED L-T-N
1	60	100.0	100.0	100.0
3	180	0.1	-	18.03
5	300	0.8	0.8	0.98
7	420	1.5	1.5	1.46
9	540	-	-	3.24
11	660	0.8	0.8	0.96
13	780	0.45	0.44	0.21
15	900	-	-	1.17
17	1020	0.87	0.87	0.65
19	1140	0.58	0.60	0.54
21	1260	-	-	0.86
23	1380	0.40	0.40	0.16
25	1500	0.37	0.36	0.43
29	1740	0.30	0.30	0.15
31	1860	-	0.1	0.12
33	1980	-	-	1.63
35	2100	3.0	3.0	2.88
37	2220	2.5	2.6	2.71
39	2340	-	-	1.37
41	2460	-	-	0.10

* Measurements made at output of triplen attenuator. Load = 11 kW, PF = 1.0. 1 MFD Cap. L-T-N. Measured THD = 5.3%. Computer Designed waveform THD = 5.6%.

Table III. 110^{o} Wide Power Center, 10^{o} Wide Step Waveform

	Item No. 0005 Waveform	Item No. 0006 Waveform	MERDC Waveform
Power Center Width	99^o	110^o	103.7
Step Width	9^o	10^o	10.9
No L-N Voltage Levels	6	5	5
Harmonic Distortion (Excluding Triplens)	4.2%	5.6%	5.0%
Harmonic	Voltage as % of Fundamental	Voltage as % of Fundamental	Voltage as % of Fundamental
1	100.0	100.0	100.00
3	16.2	18.03	16.30
5	0.19	0.98	0.15
7	0.61	1.46	0.87
9	1.06	3.24	1.04
11	0.65	0.96	0.85
13	0.51	0.21	0.51
15	0.40	1.17	0.70
17	0.36	0.65	0.24
19	0.33	0.54	0.61
21	0.27	0.86	0.07
23	0.30	0.16	0.54
25	0.22	0.43	0.07
27	0.27	0.15	0.29
29	0.22	0.35	0.69
31	0.34	0.12	2.49
33	0.11	1.63	3.28
35	0.01	2.88	2.25
37	1.28	2.71	0.58
39	2.59	1.37	0.20
41	2.45	0.10	0.03
43	1.10	0.22	0.29
45	0.02	0.08	0.04
47	0.07	0.22	0.24
49	0.21	0.07	0.04
51	0.12	0.34	0.20
53	0.13	0.19	0.13
55	0.09	0.19	0.16
57	0.12	0.30	0.17
59	0.09	0.05	0.10
61	0.10	0.16	0.00
63	0.09	0.05	

Table IV. Comparison of Harmonic Distribution for Three Waveform Designs

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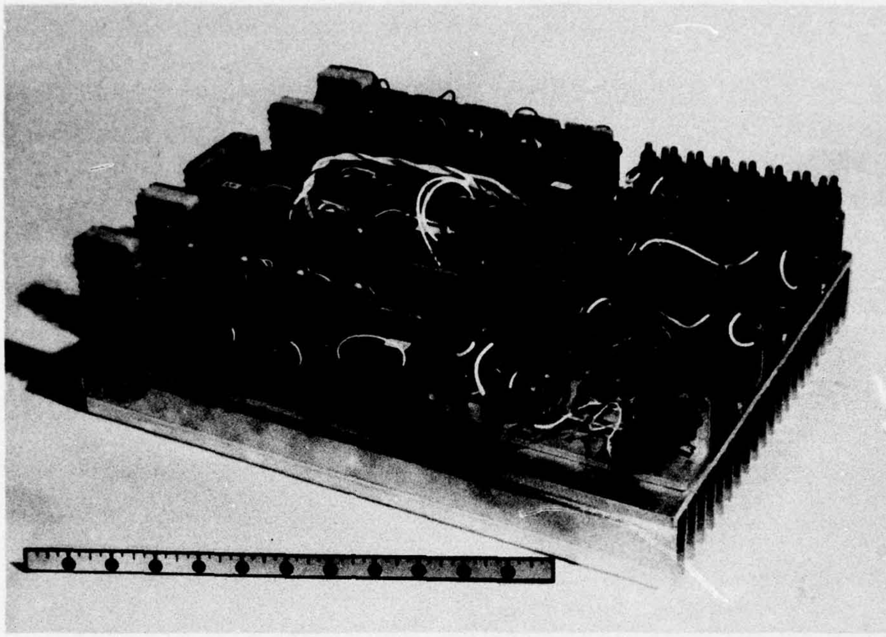


Figure 1. Item 0001 Inverter Power Switch Assembly

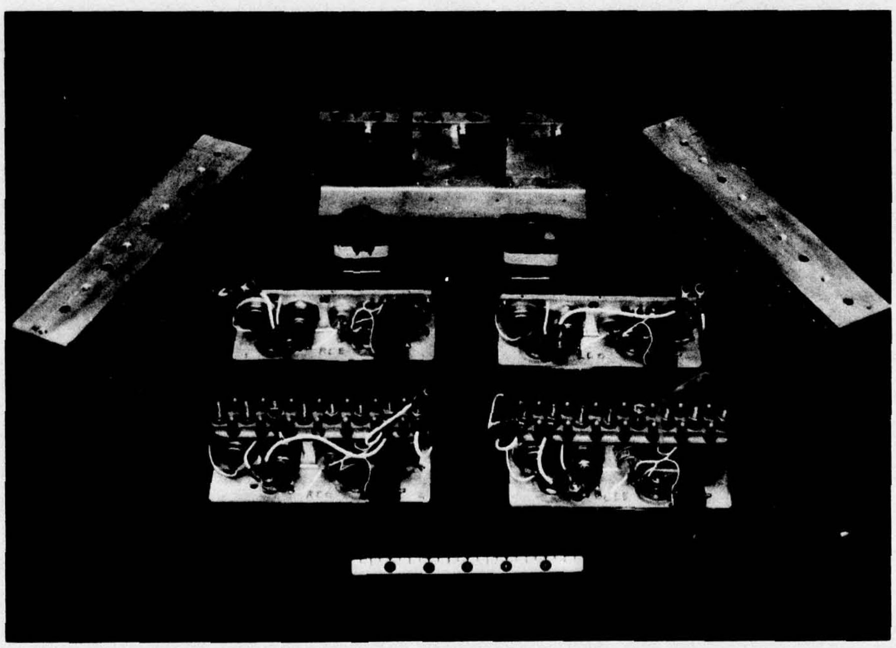


Figure 2. Transistor Step Commutation Circuit Components Removed from Item 0001 Inverter

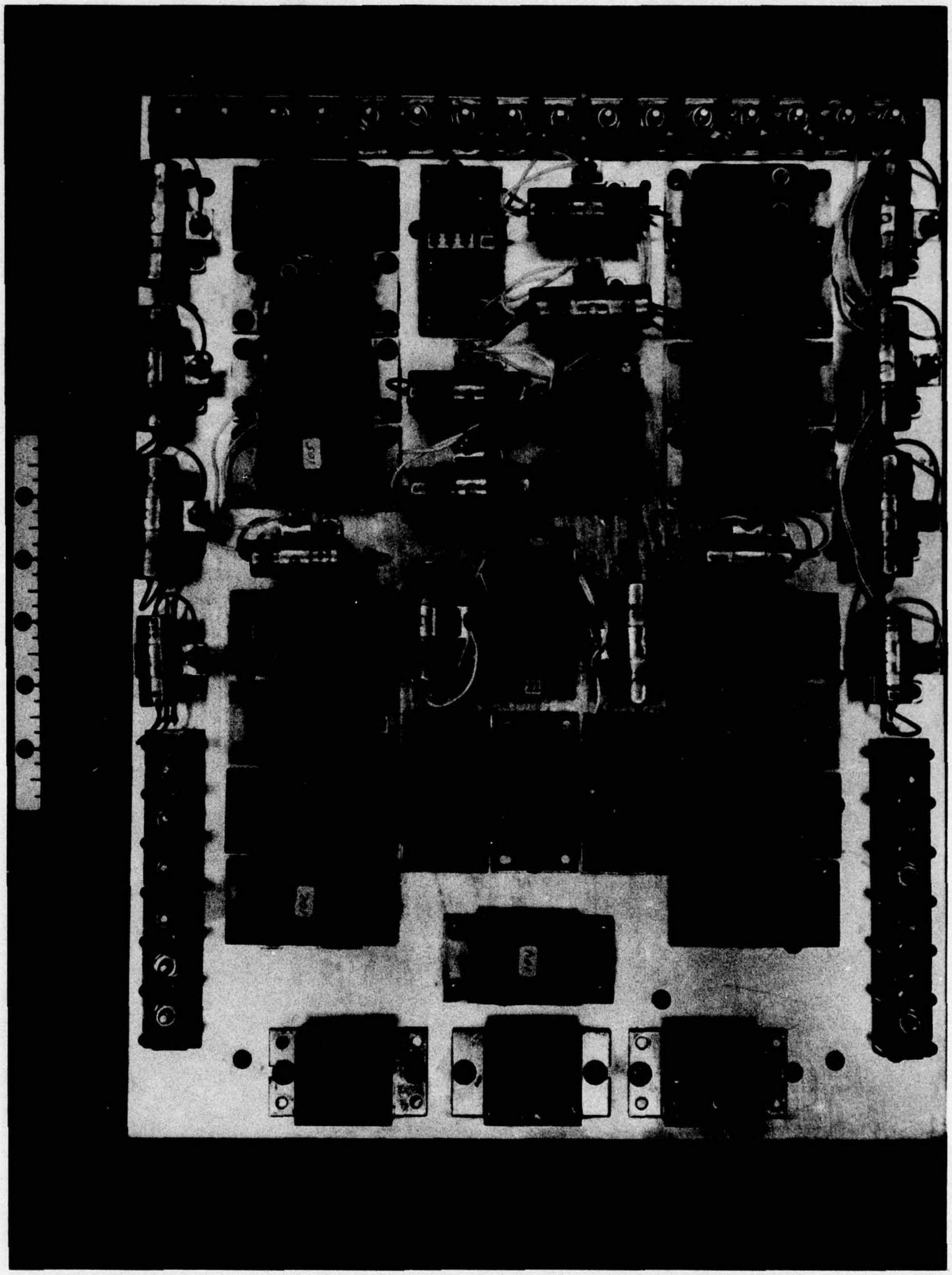


Figure 3. Item 0006 Inverter with Thyristor Step Commutation. Weight 23 lb

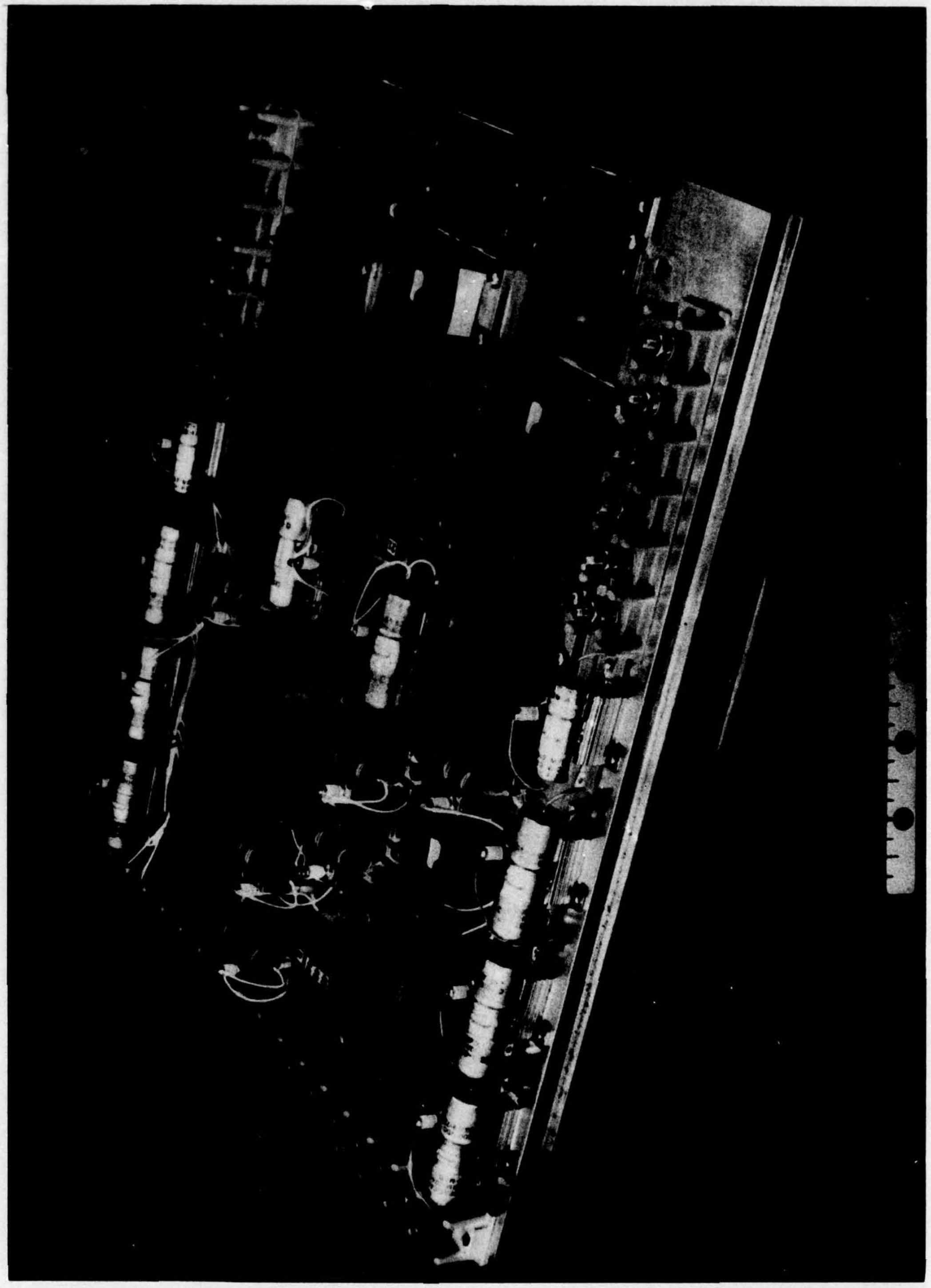


Figure 4. Threequarter View of Item 0006 Inverter Power Switch Assembly

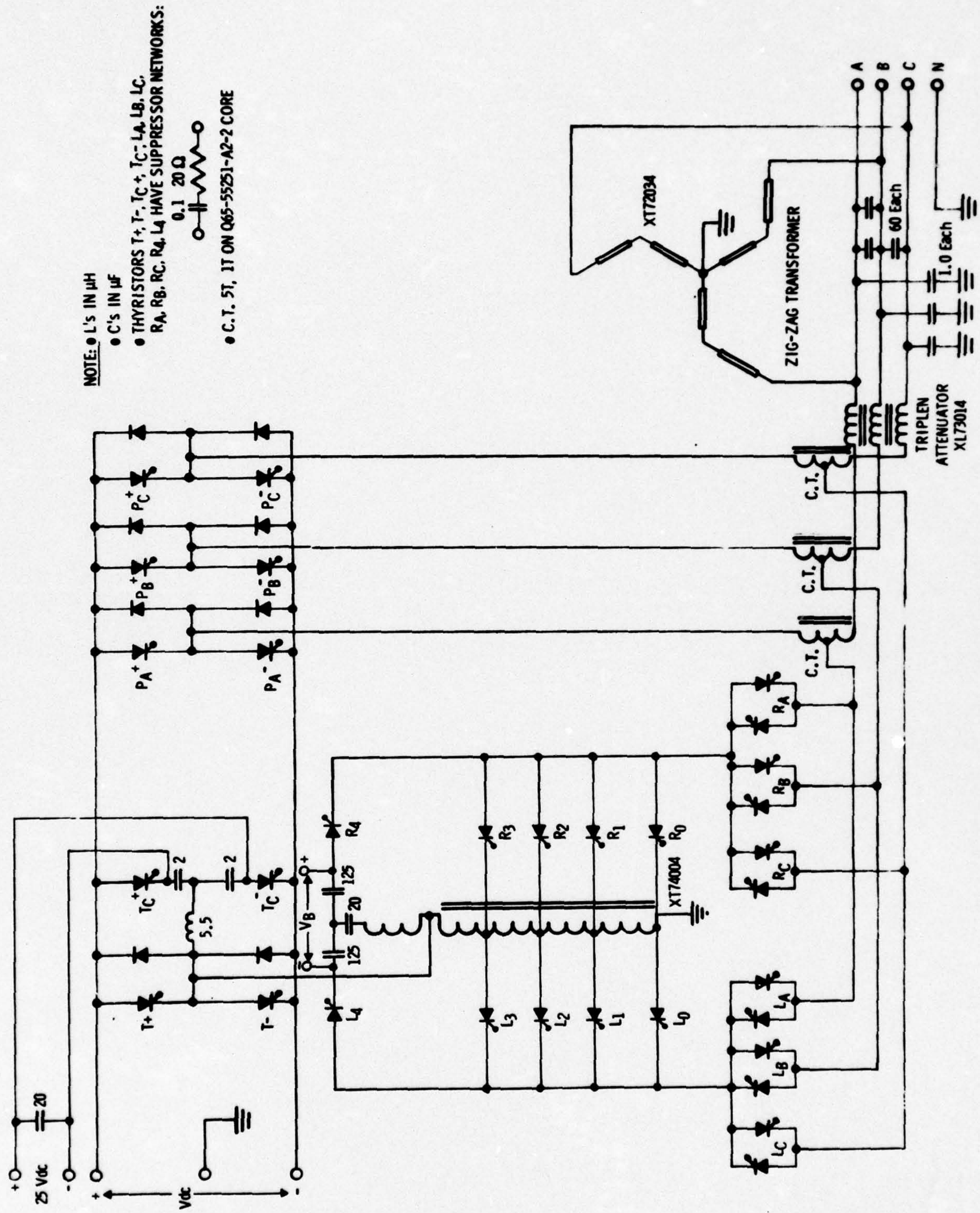


Figure 5. 400 Hz Inverter Circuit

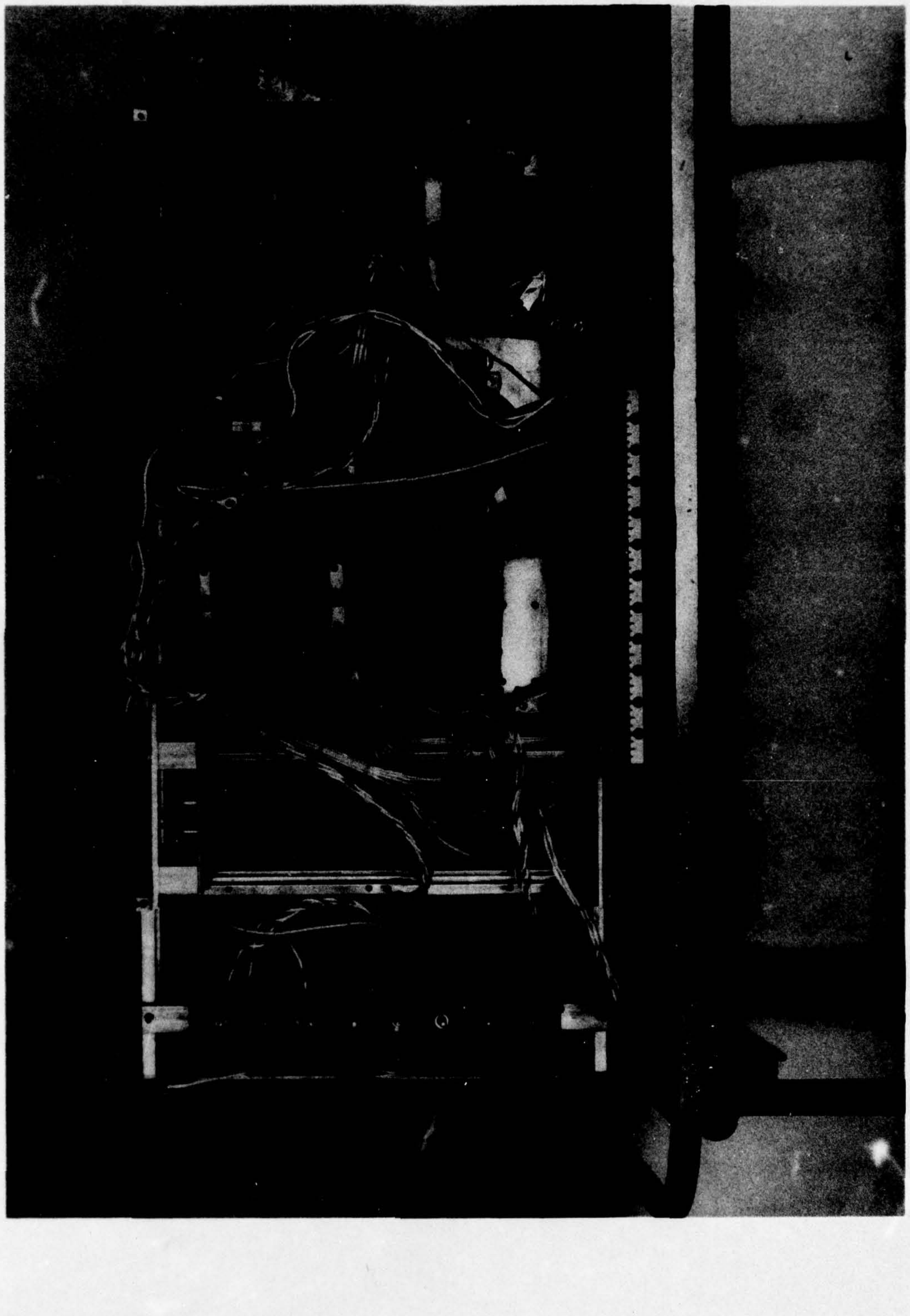


Figure 6. Item 0006 Inverter - Bottom View

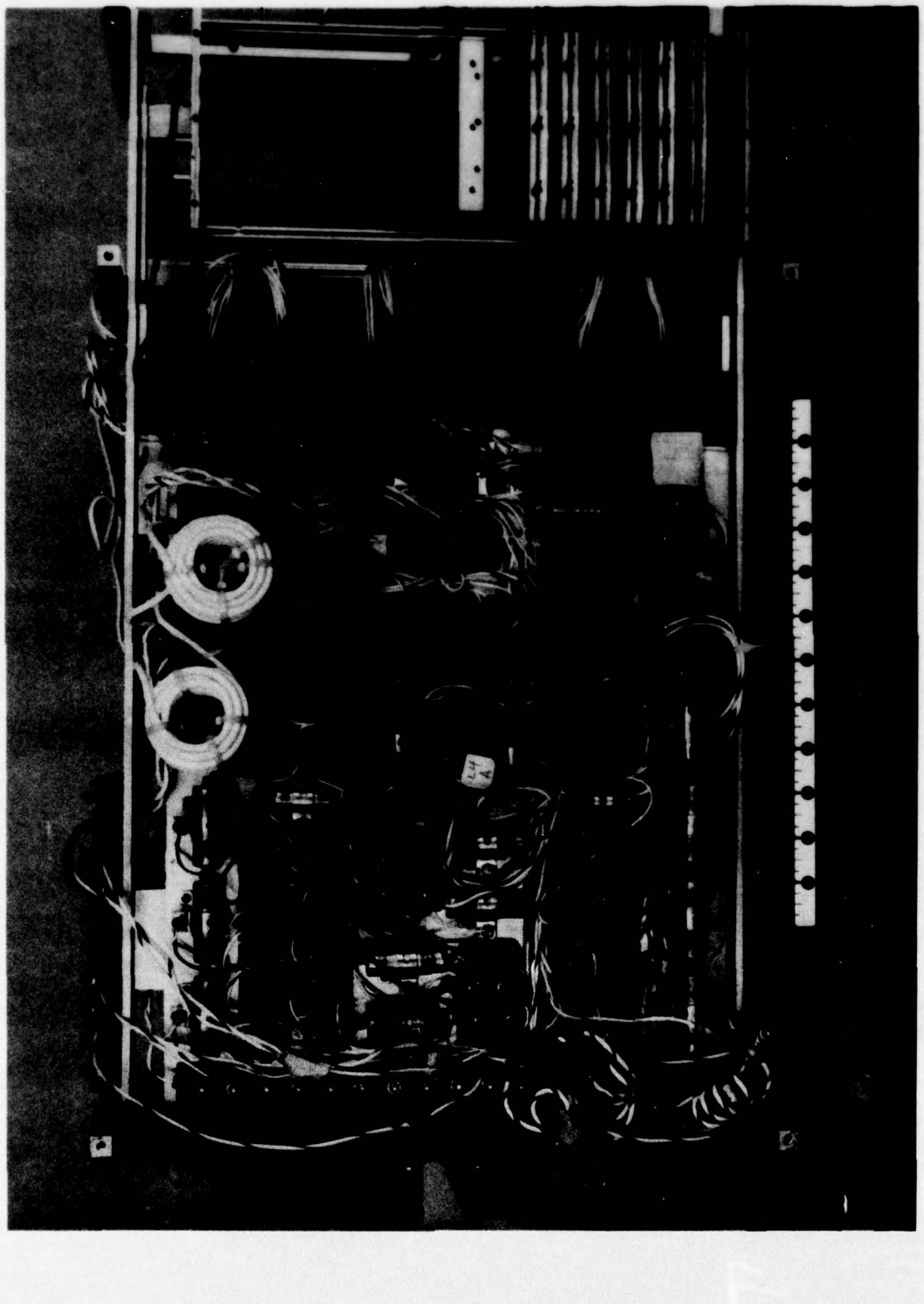


Figure 7. Item 0006 Inverter - Top View

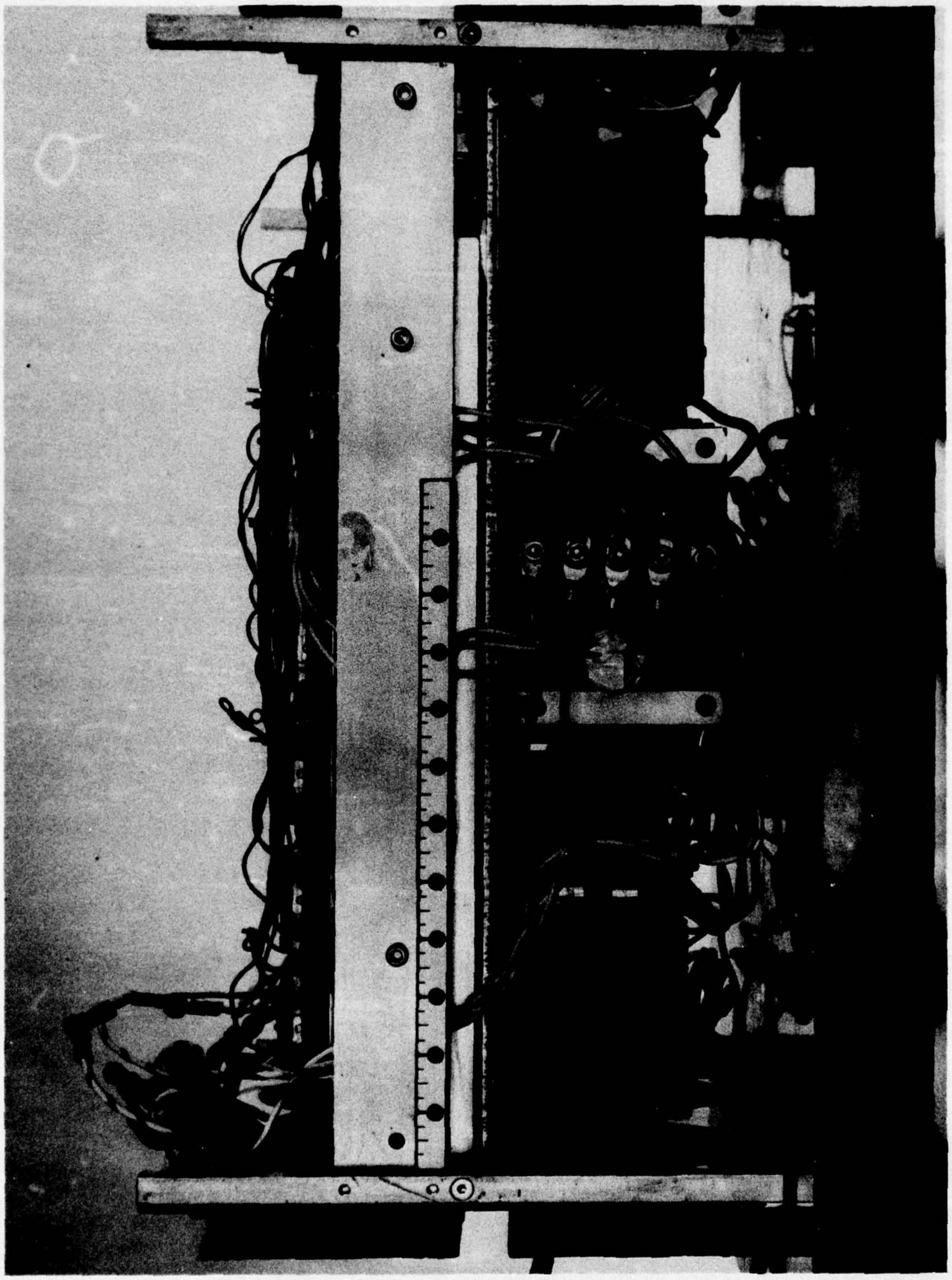


Figure 8. Item 0006 Inverter - Side View

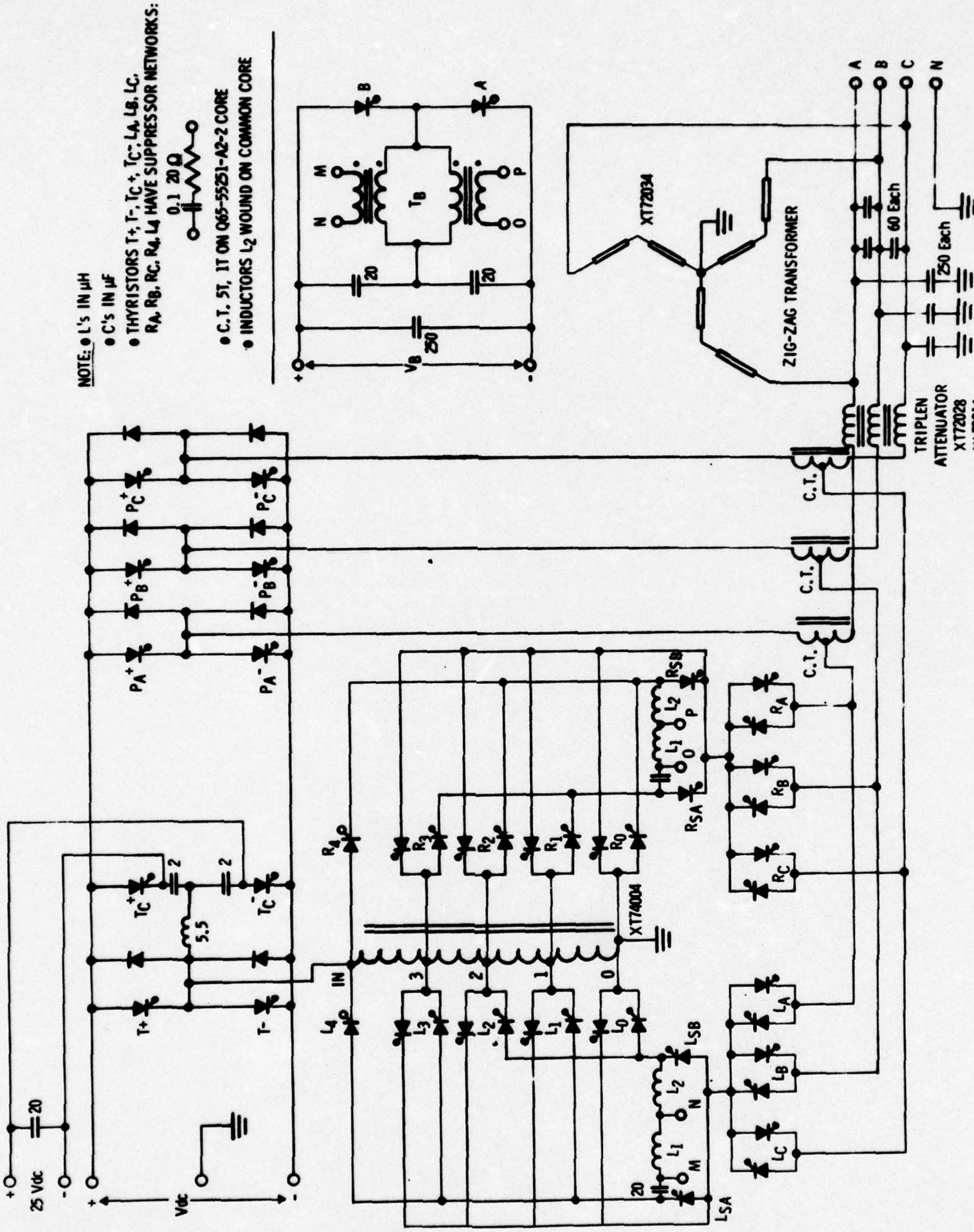


Figure 9. 60 Hz Inverter Circuit

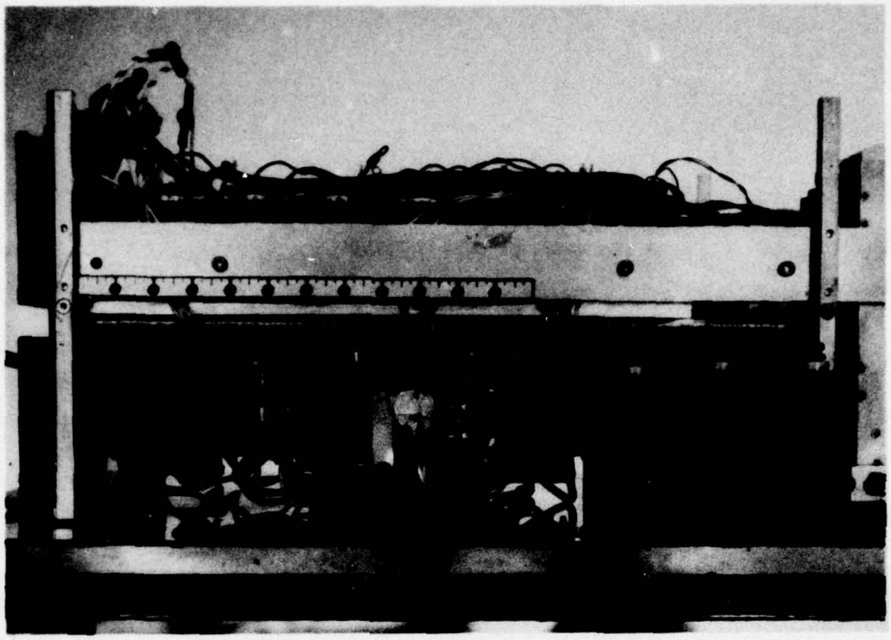


Figure 10. Item 0006 Inverter Showing Addition of 60 Hz Output Filter Capacitors

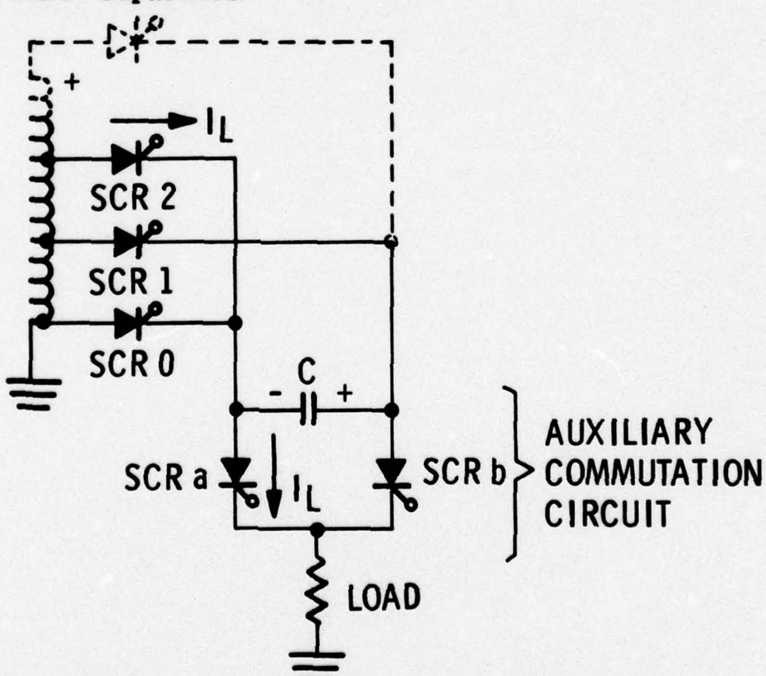


Figure 11. Double Bus Step Changing Circuit

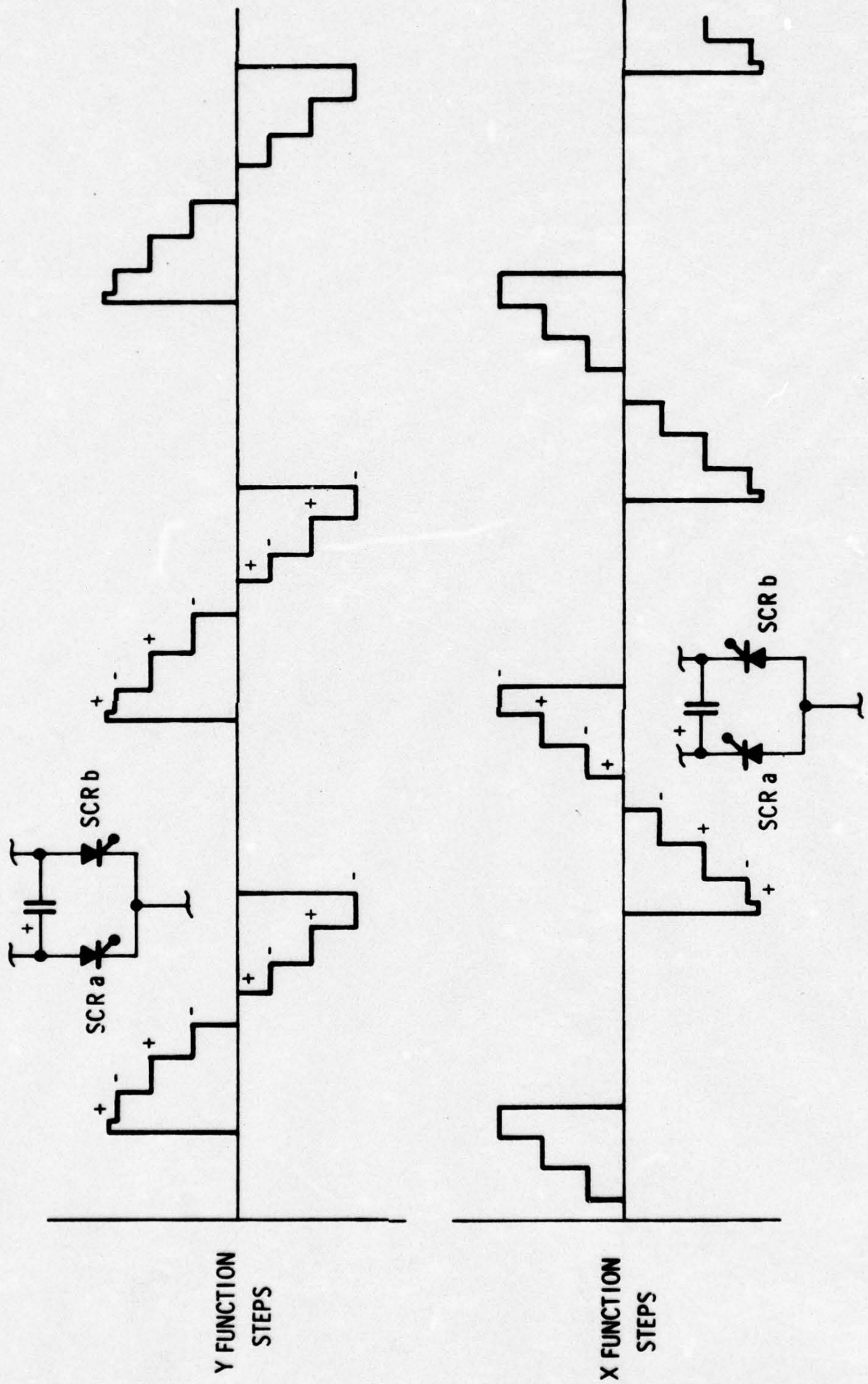


Figure 12. Diagram Showing the Capacitor Voltage Polarities Required to Commutate Each Step for the Y and X Functions

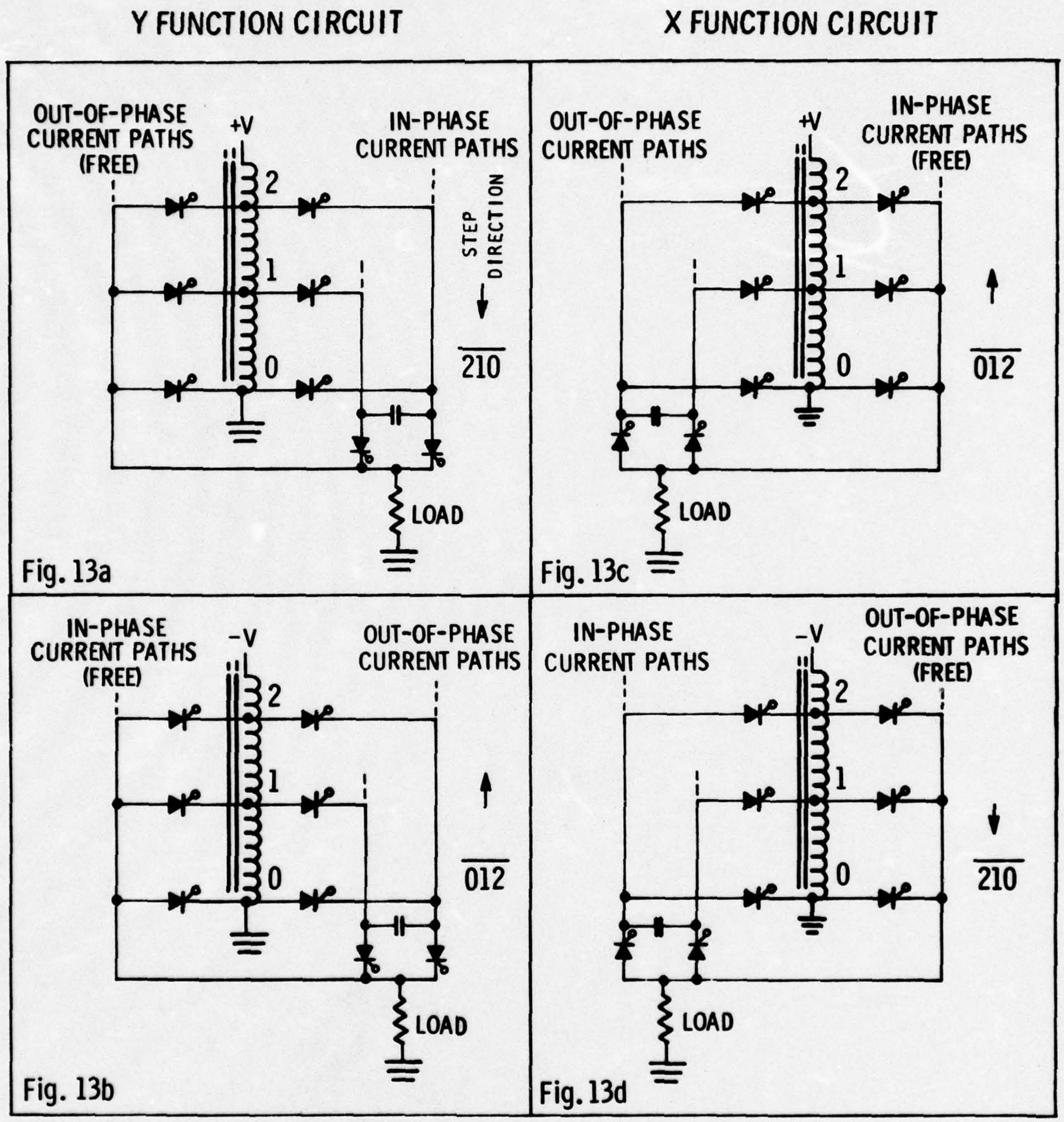


Figure 13. Y and X Step Function Circuits

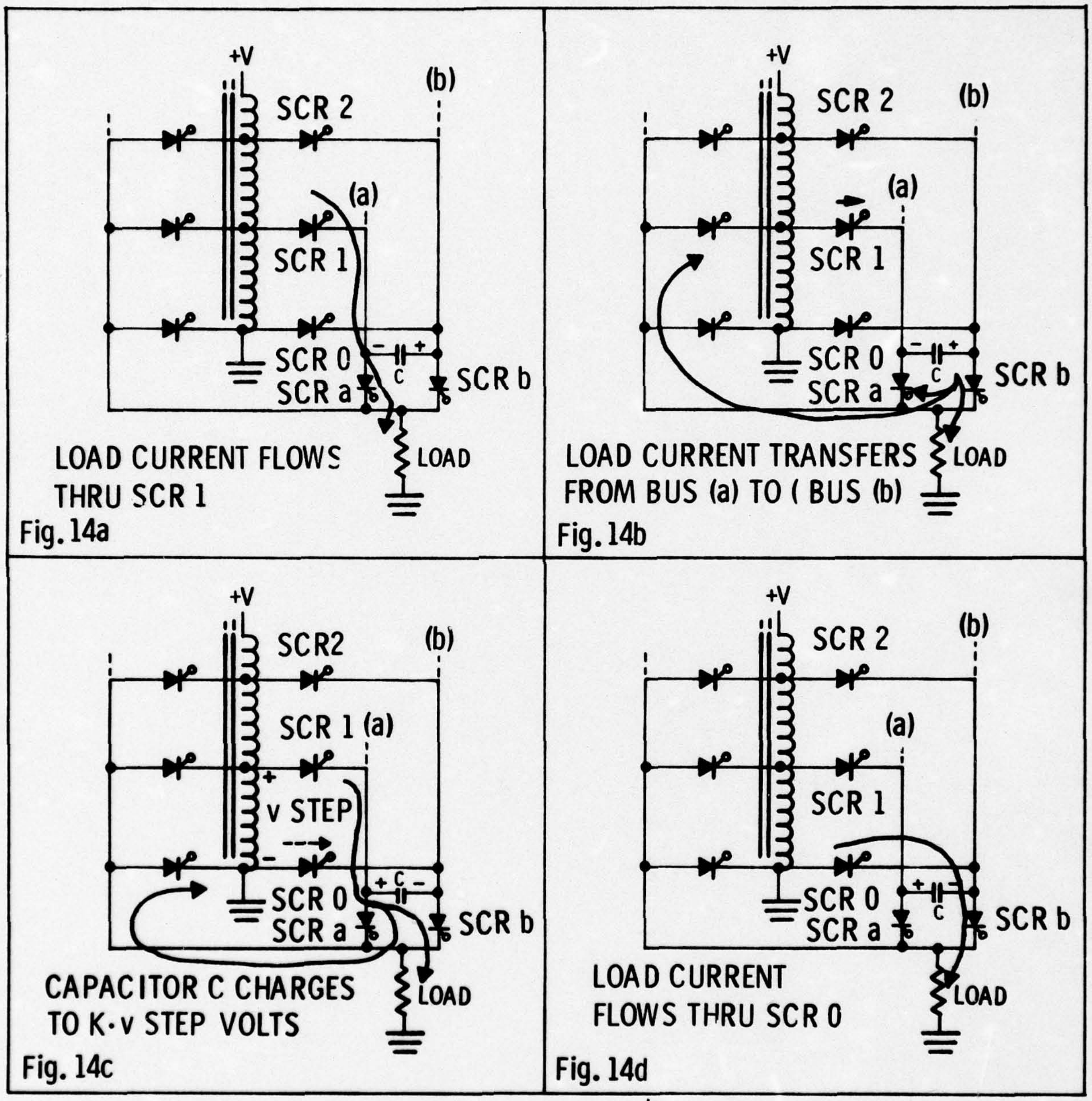


Figure 14. Y Function. Transferring Current from SCR1 to SCR0. Load Voltage and Current Flow Positive

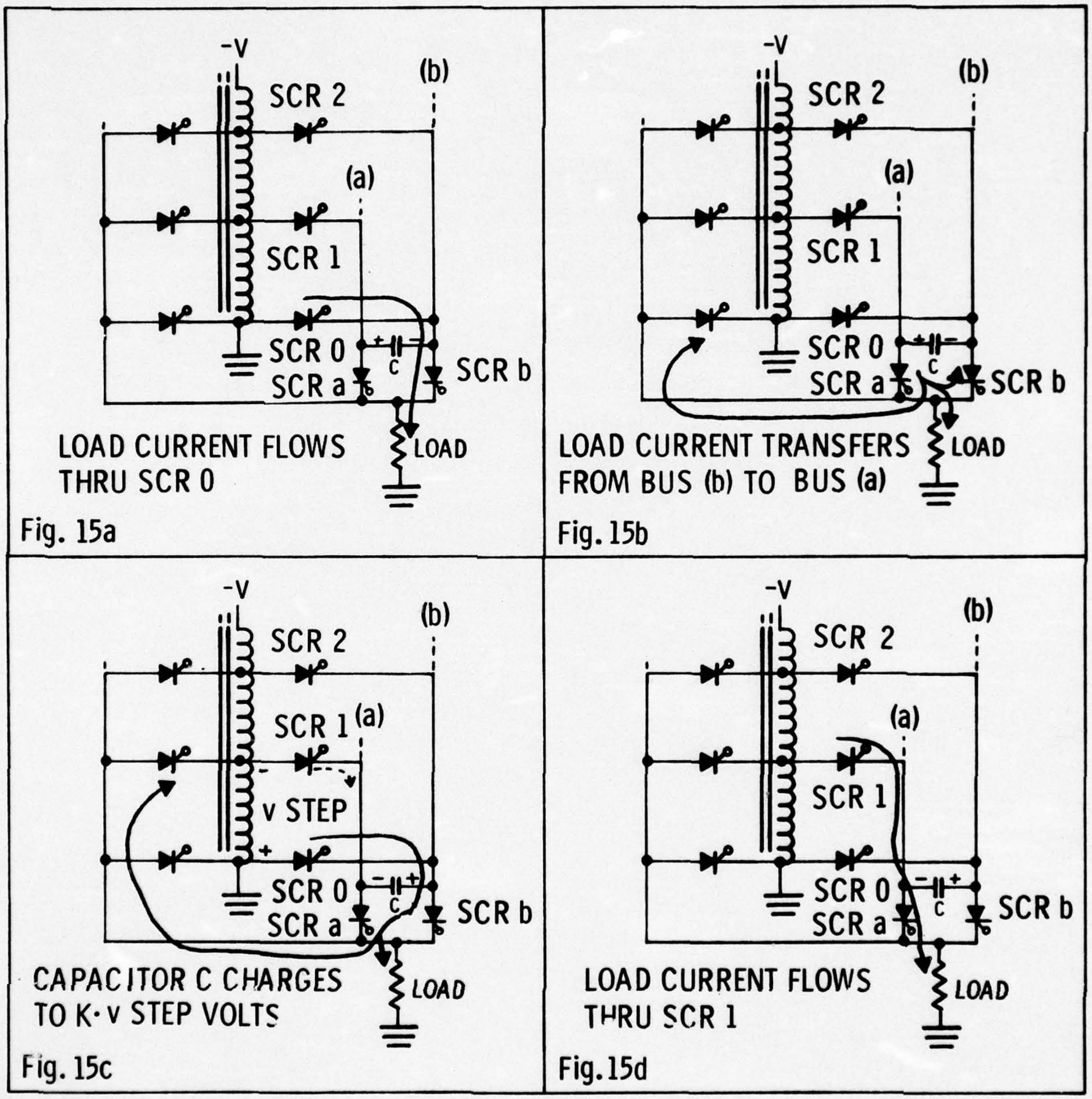


Figure 15. Y Function. Transferring Current from SCR0 to SRC1. Load Voltage Negative; Current Flow Positive

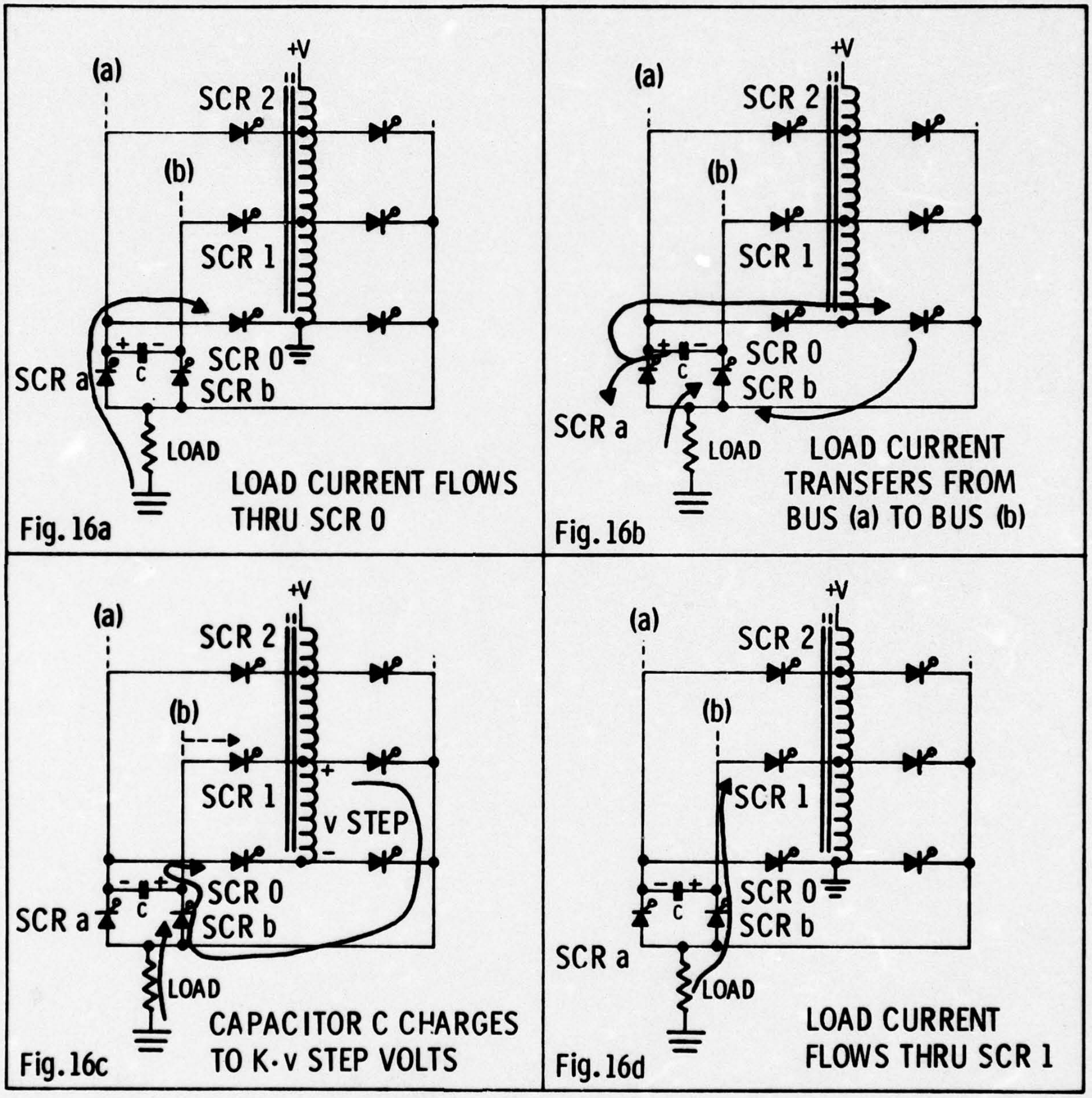


Figure 16. X Function. Transferring Current from SCR0 to SCR1. Load Voltage Positive; Current Flow Negative

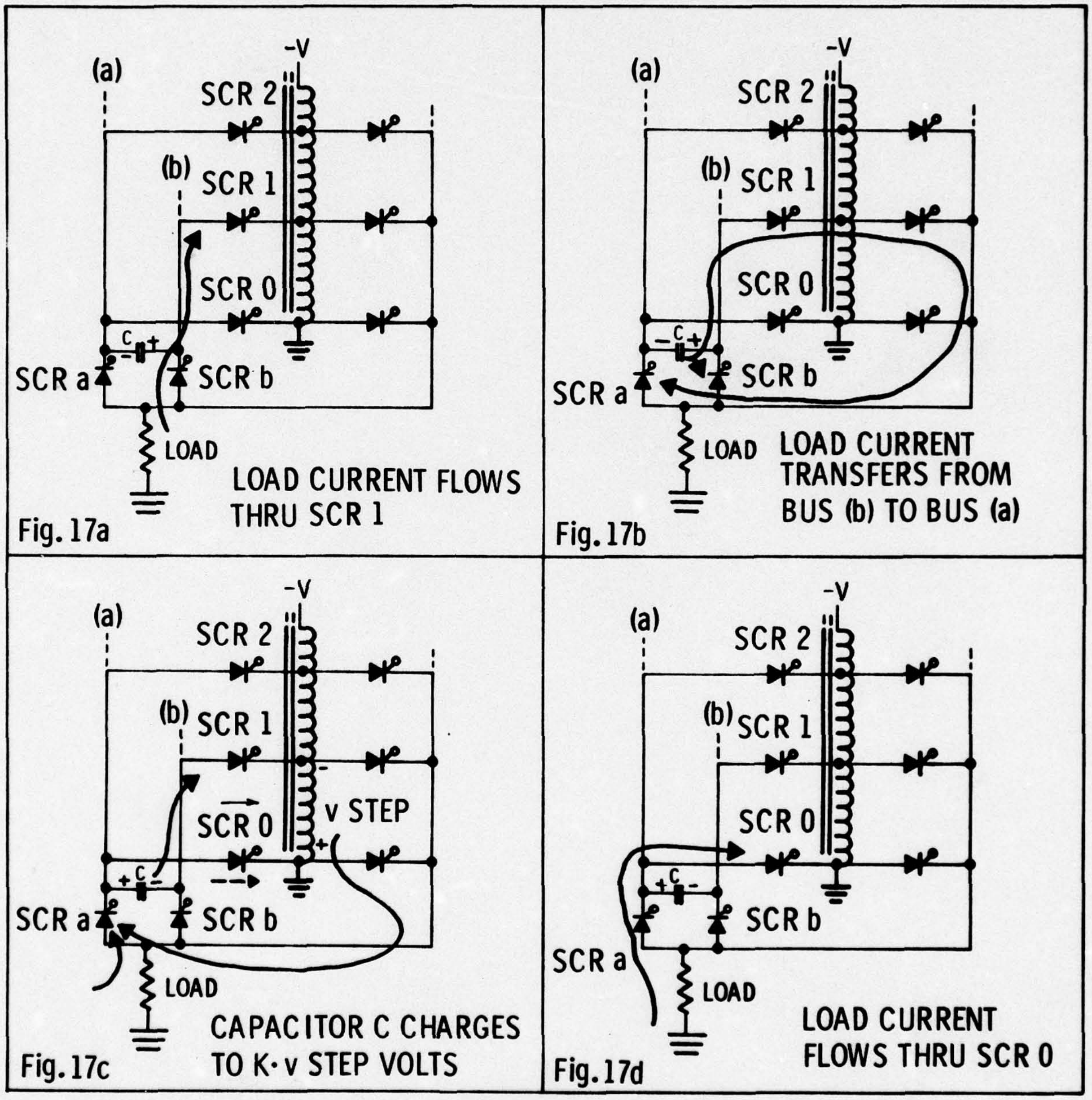


Figure 17. X Function. Transferring Current from SCR1 to SCR0. Load Voltage and Current Flow Negative

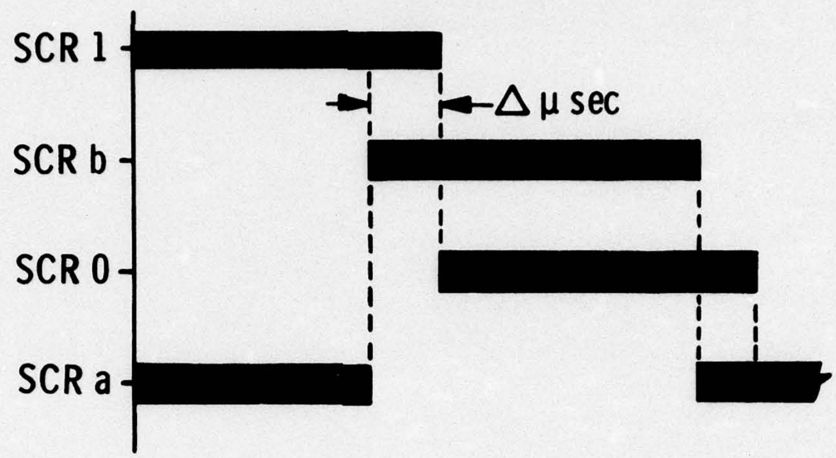


Figure 18a. SCR Trigger Timing Sequence for Figures 14a to 14d

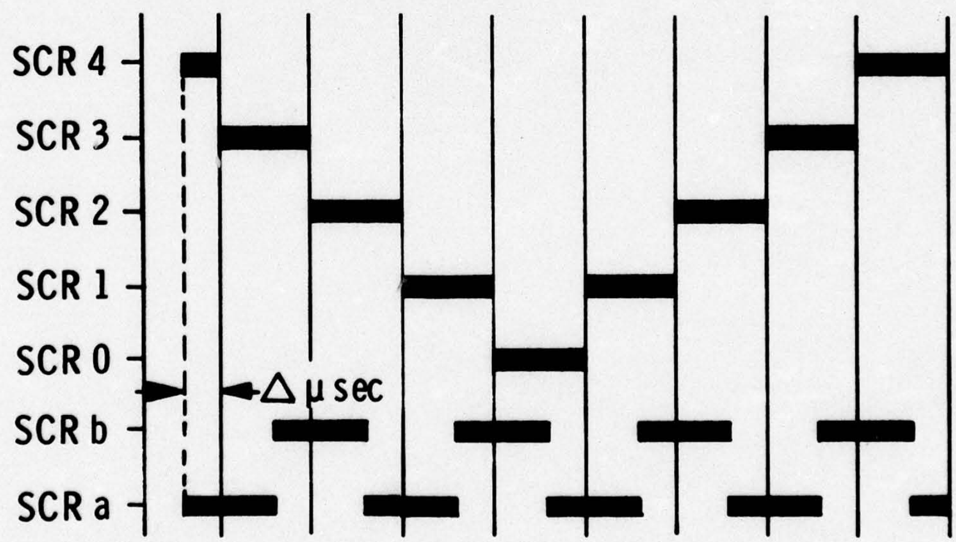


Figure 18b. Y Function Step Timing Diagram

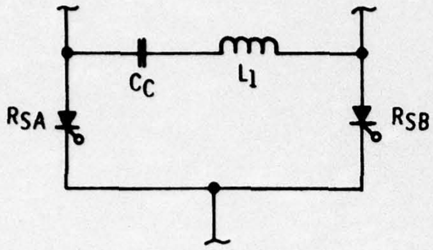


Figure 19a. Basic Step Voltage Commutation Circuit

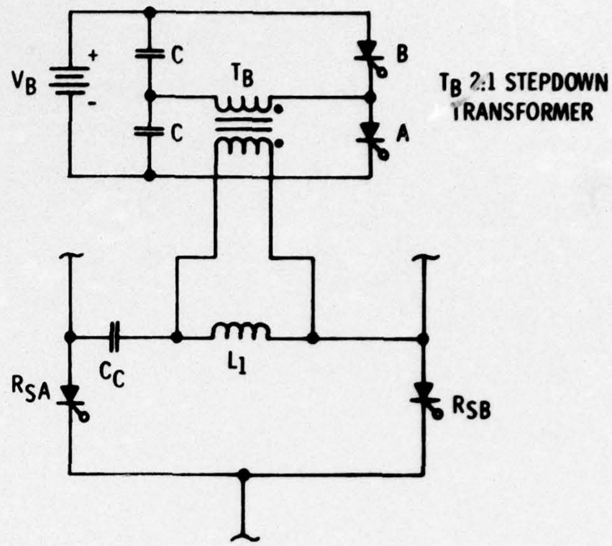


Figure 19b. Method of Obtaining Boost Voltage for Step Commutation

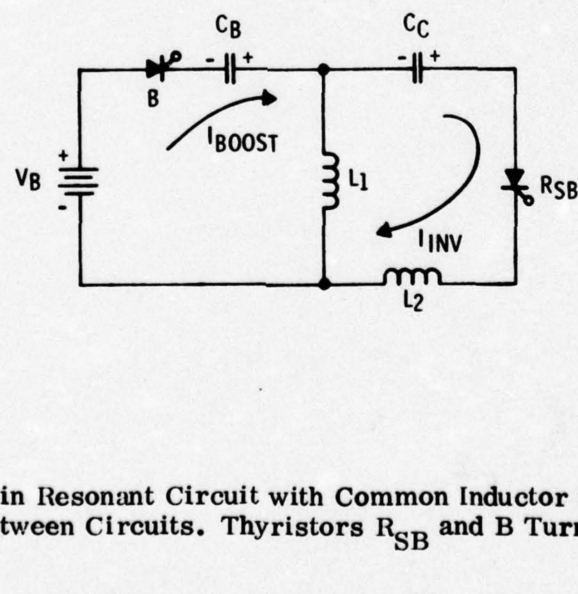
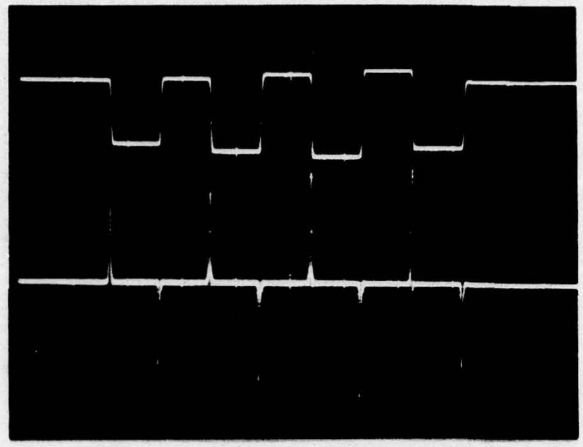


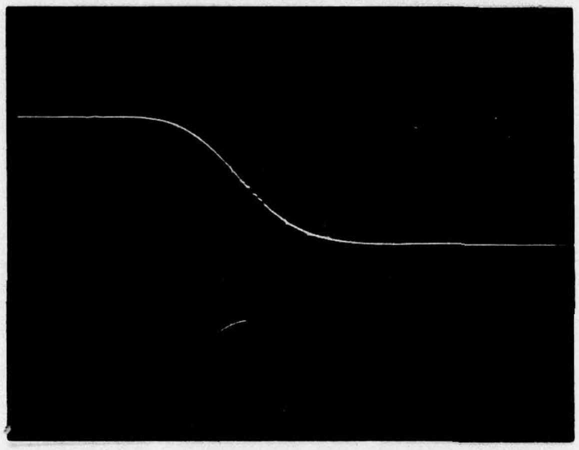
Figure 20. Twin Resonant Circuit with Common Inductor for Energy Transfer Between Circuits. Thyristors R_{SB} and B Turn-on Simultaneously



COMMUTATION CAPACITOR C_C
VOLTAGE 200 V/DIV.

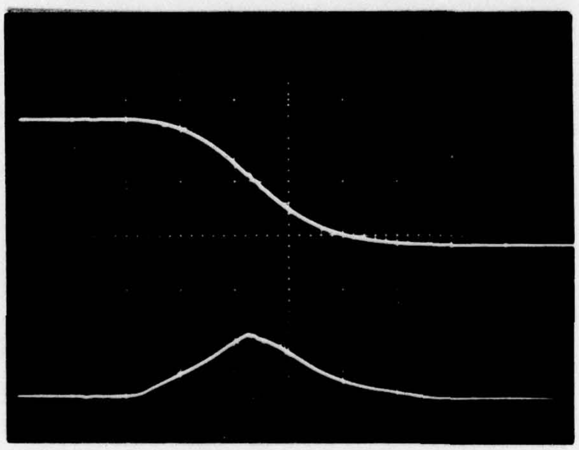
(a) COMMUTATION CAPACITOR C_C
CURRENT 100 A/DIV.

500 μSEC/DIV.; V_B = 66 VDC; I_B = 9 AMPS
0 INPUT VOLTAGE TO 1 INVERTER



COMMUTATION CAPACITOR C_C
VOLTAGE AT POWER CENTER
COMMUTATION TIME, P_C 100 V/DIV.

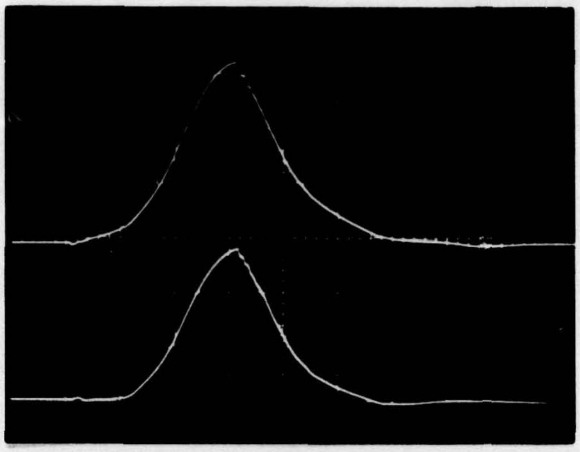
(b) COMMUTATION CAPACITOR C_C
CURRENT 200 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



COMMUTATION CAPACITOR C_C
VOLTAGE 100 V/DIV.

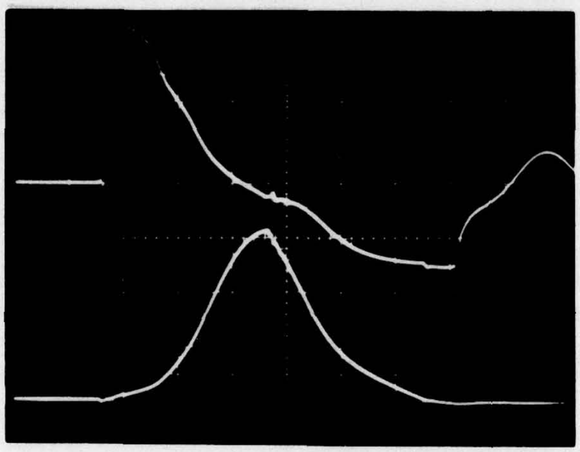
(c) COMMUTATION CAPACITOR C_C
CURRENT 200 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD

Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 1 of 6)



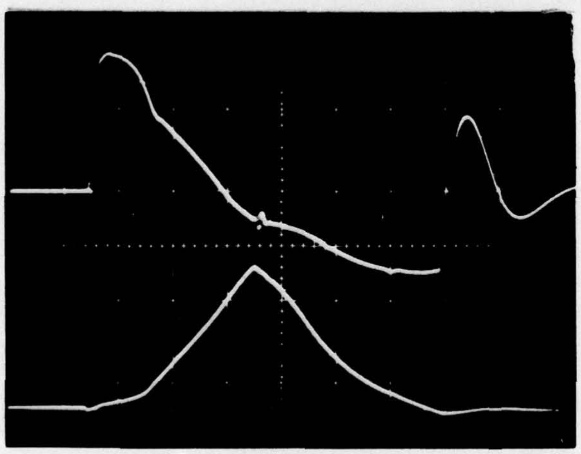
INDUCTOR L_1 CURRENT
100 A/DIV.

(d) COMMUTATION CAPACITOR C_C
CURRENT 100 A/DIV.
10 μSEC/DIV.



INDUCTOR L_1 VOLTAGE
20 V/DIV.

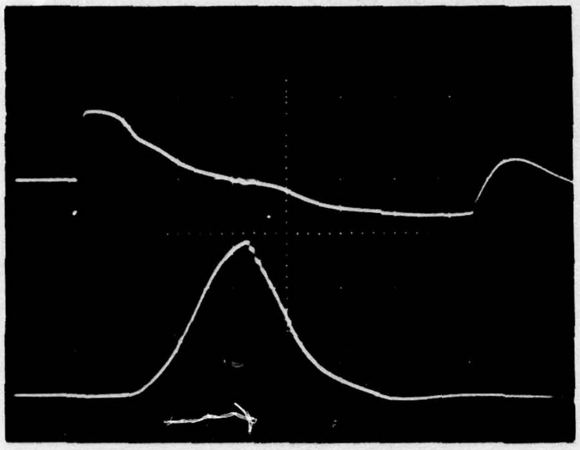
(e) INDUCTOR L_1 CURRENT
100 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



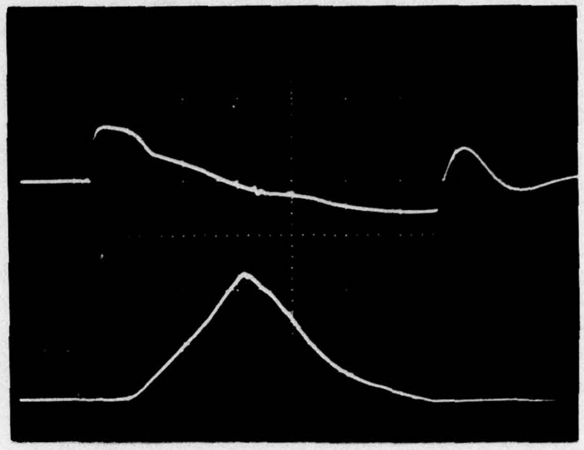
INDUCTOR L_1 VOLTAGE
20 V/DIV.

(f) INDUCTOR L_1 CURRENT
100 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD

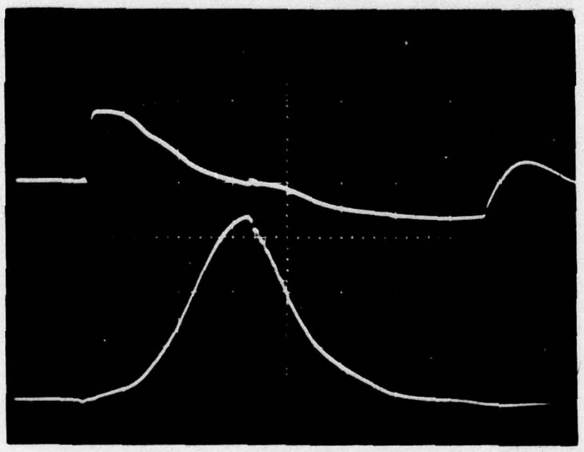
Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 2 of 6)



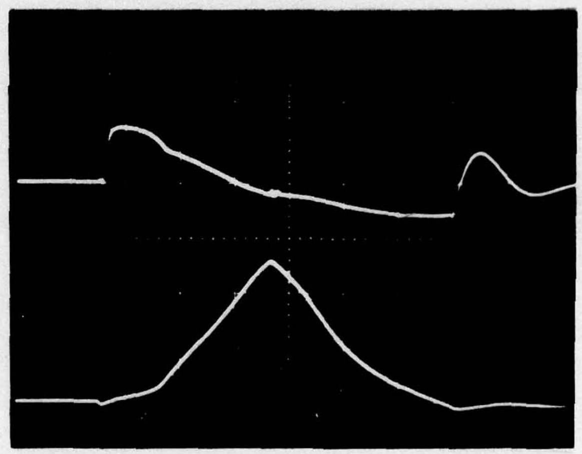
(g) UPPER TRACE INDUCTOR L_1 VOLTAGE 50 V/DIV.
LOWER TRACE COMMUTATION CAPACITOR C_C CURRENT 100 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



(h) UPPER TRACE INDUCTOR L_1 VOLTAGE 50 V/DIV.
LOWER TRACE COMMUTATION CAPACITOR C_C CURRENT 100 A/DIV.
10 μSEC/DIV.
11 kW PF = 0.8 LOAD

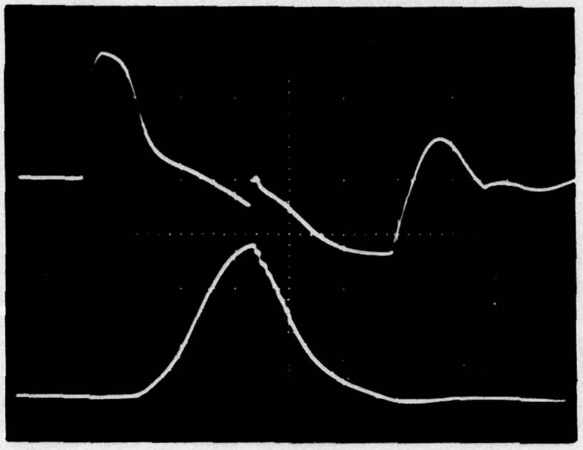


(i) UPPER TRACE TRANSFORMER T_B SECONDARY VOLTAGE 50 V/DIV.
LOWER TRACE TRANSFORMER T_B SECONDARY CURRENT 100 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



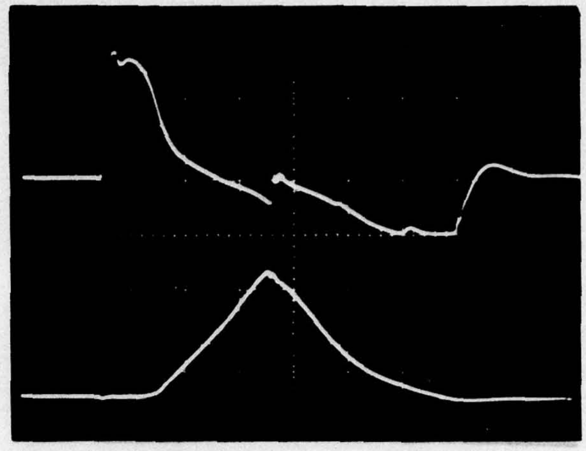
(j) UPPER TRACE TRANSFORMER T_B SECONDARY VOLTAGE 50 V/DIV.
LOWER TRACE TRANSFORMER T_B SECONDARY CURRENT 100 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD

Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 3 of 6)



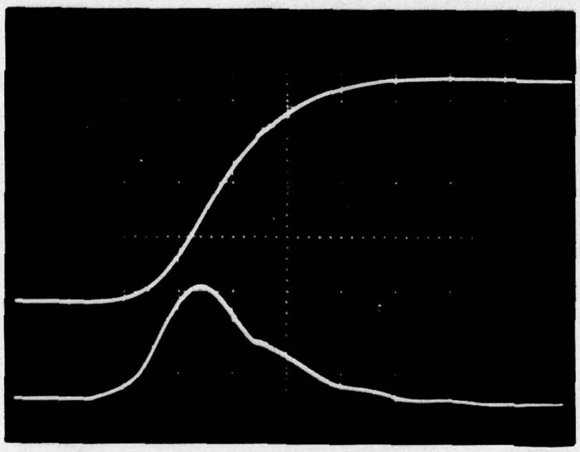
UPPER TRACE INDUCTOR L_2 VOLTAGE 100 V/DIV.

(k) LOWER TRACE COMMUTATION CAPACITOR CURRENT 100 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



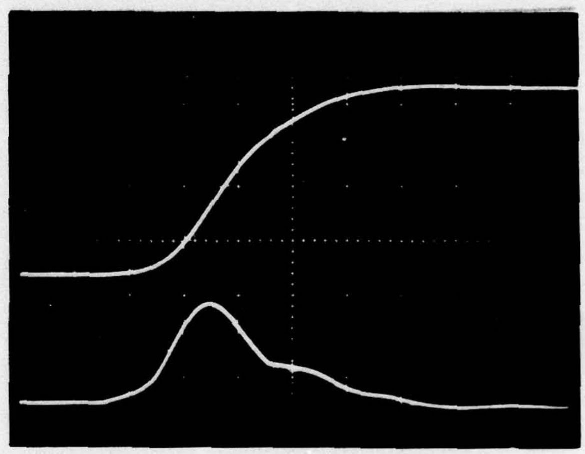
UPPER TRACE INDUCTOR L_2 VOLTAGE 100 V/DIV.

(l) LOWER TRACE COMMUTATION CAPACITOR CURRENT 100 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD



(m) UPPER TRACE BOOST SUPPLY CAPACITOR C VOLTAGE 50 V/DIV.

LOWER TRACE BOOST SUPPLY CAPACITOR C CURRENT 100 A/DIV.
10 μSEC/DIV.
0 INPUT VOLTAGE TO INVERTER



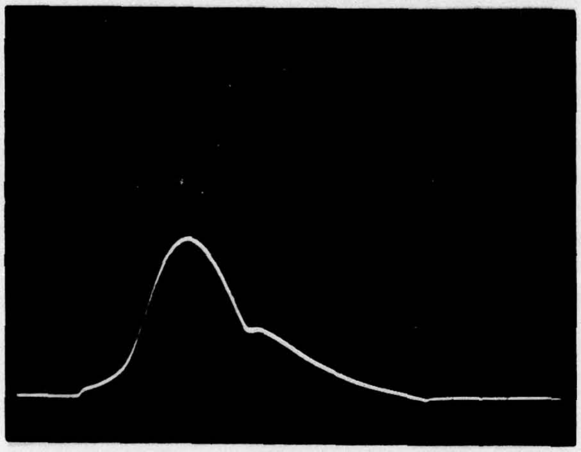
(n) UPPER TRACE BOOST SUPPLY CAPACITOR C VOLTATE 50 V/DIV.

LOWER TRACE BOOST SUPPLY CAPACITOR C CURRENT 100 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD

Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 4 of 6)

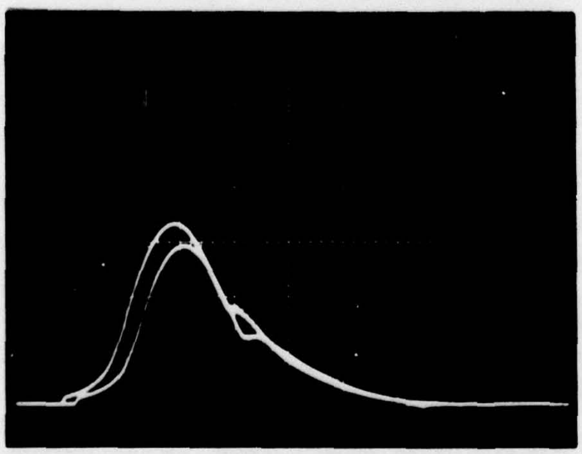
(o) BOOST SUPPLY CURRENT I_B
100 A/DIV.
10 μSEC/DIV.

0 INPUT VOLTAGE TO INVERTER



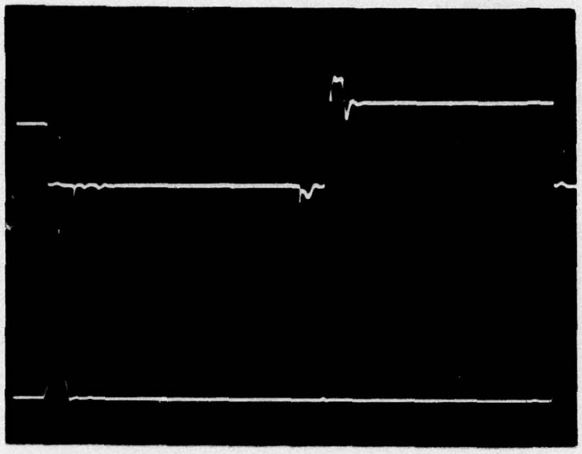
(p) BOOST SUPPLY CURRENT I_B
100 A/DIV.
10 μSEC/DIV.
11 kW, PF = 0.8 LOAD

(AVG INPUT CURRENT DROPS FROM 9 AMPS AT NO LOAD TO 8 AMPS AT 11 kW, 0.8 PF LOAD)

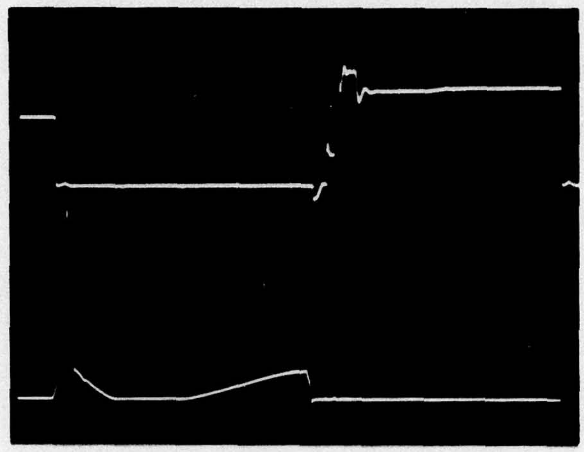


(q) DOUBLE EXPOSURE FOR PICTURES O AND P

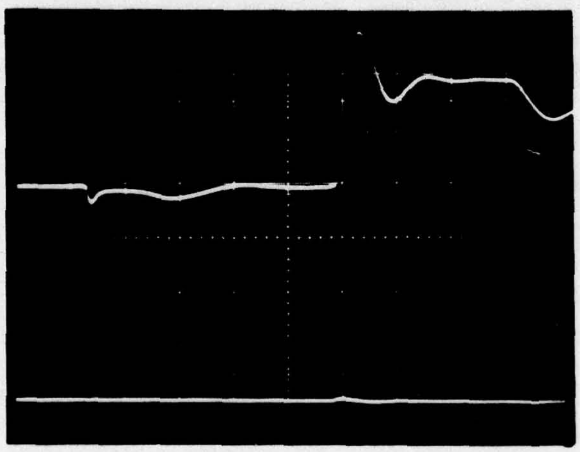
Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 5 of 6)



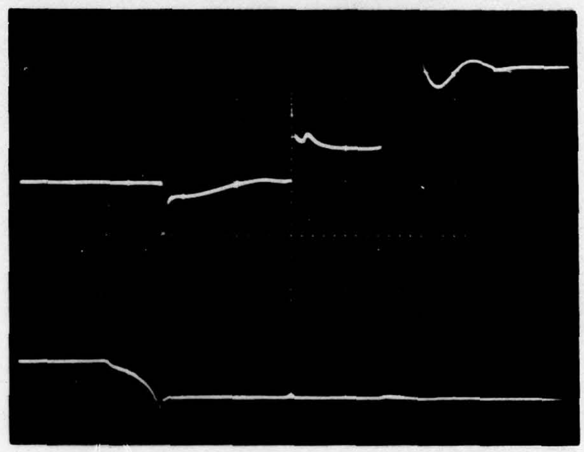
(r)
UPPER TRACE — VOLTAGE ACROSS THYRISTOR R_{SA} FOR THIRD STEP LEVEL 100 V/DIV.
LOWER TRACE — R_{SA} CURRENT 100 A/DIV.
100 μSEC/DIV. NO LOAD



(s)
UPPER TRACE — VOLTAGE ACROSS THYRISTOR R_{SA} FOR THIRD STEP LEVEL 100 V/DIV.
LOWER TRACE — R_{SA} CURRENT 100 A/DIV.
100 μSEC/DIV.
11 kW, PF = 0.8 LOAD



(t) SAME AS (r) BUT TIME = 10 μSEC/DIV.



(u) SAME AS (s) BUT TIME = 10 μSEC/DIV.

Figure 21. Voltage and Current Waveforms for the Commutation Boost Circuit (Sheet 6 of 6)

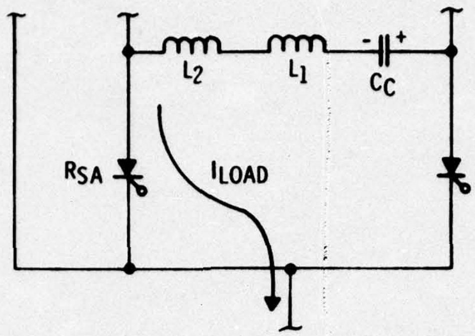


Figure 22a. Equivalent Commutation Circuit When Current Flows through R_{SA}

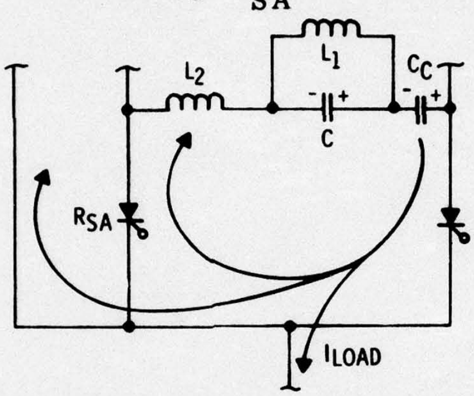


Figure 22b. Equivalent Commutation Circuit When R_{SB} Turns on to Commutate R_{SA} and Transfer Load Current to Another Step Voltage level

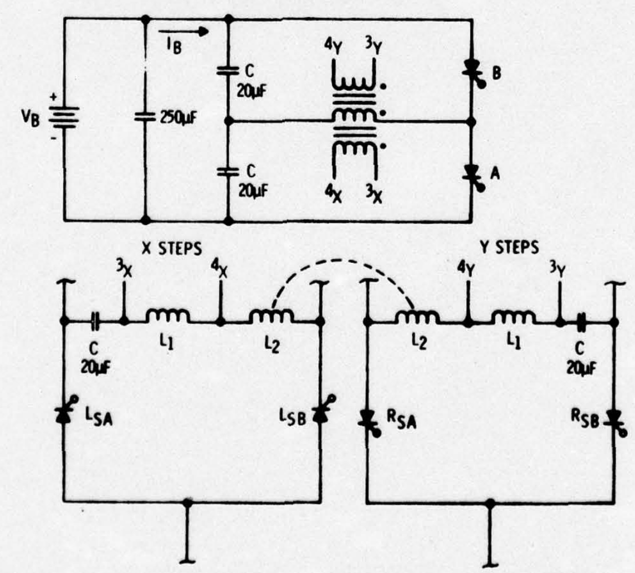


Figure 23. Complete Step Voltage Commutation Circuit

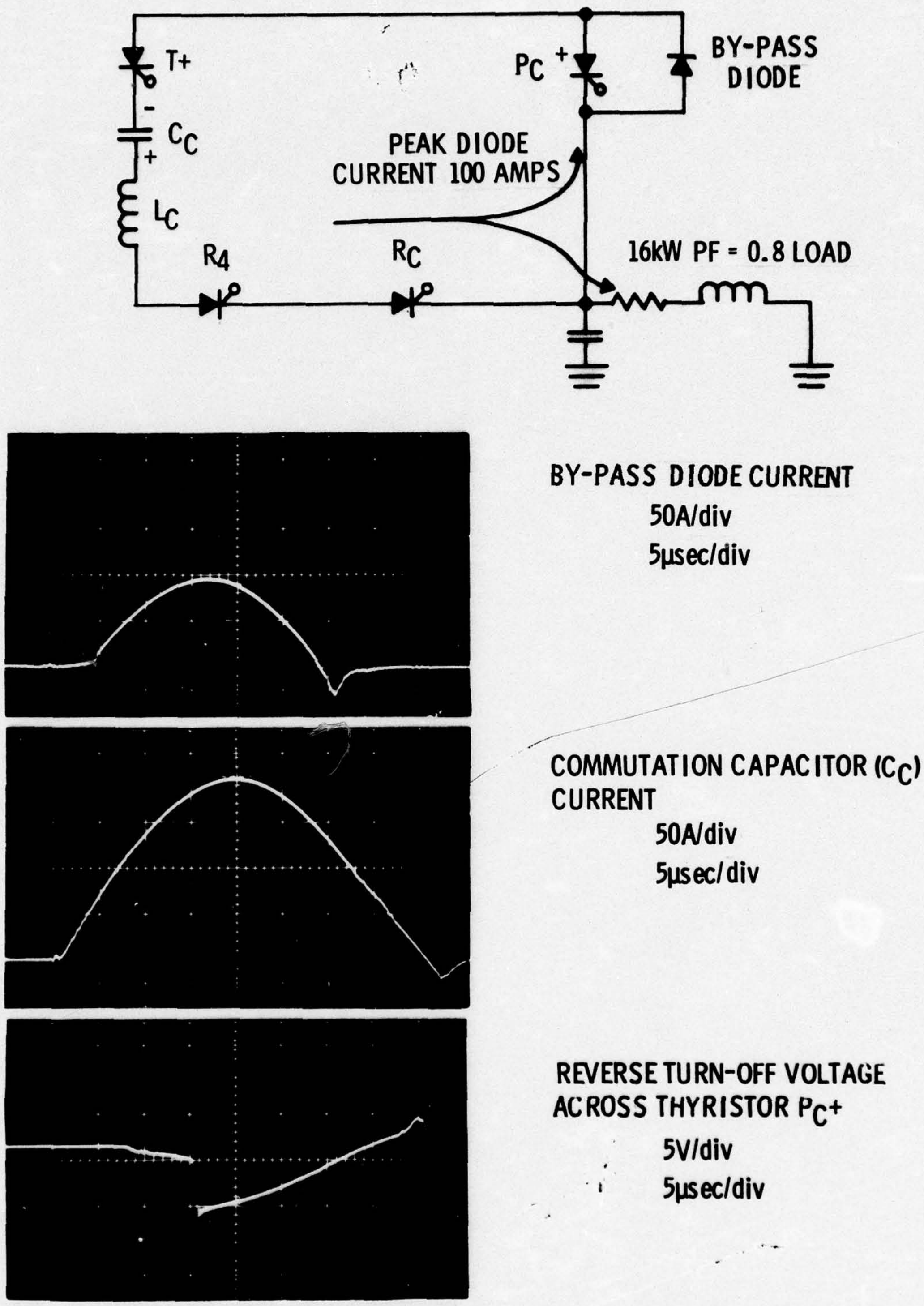


Figure 24. Original Power Center Thyristor Turn-Off Circuit

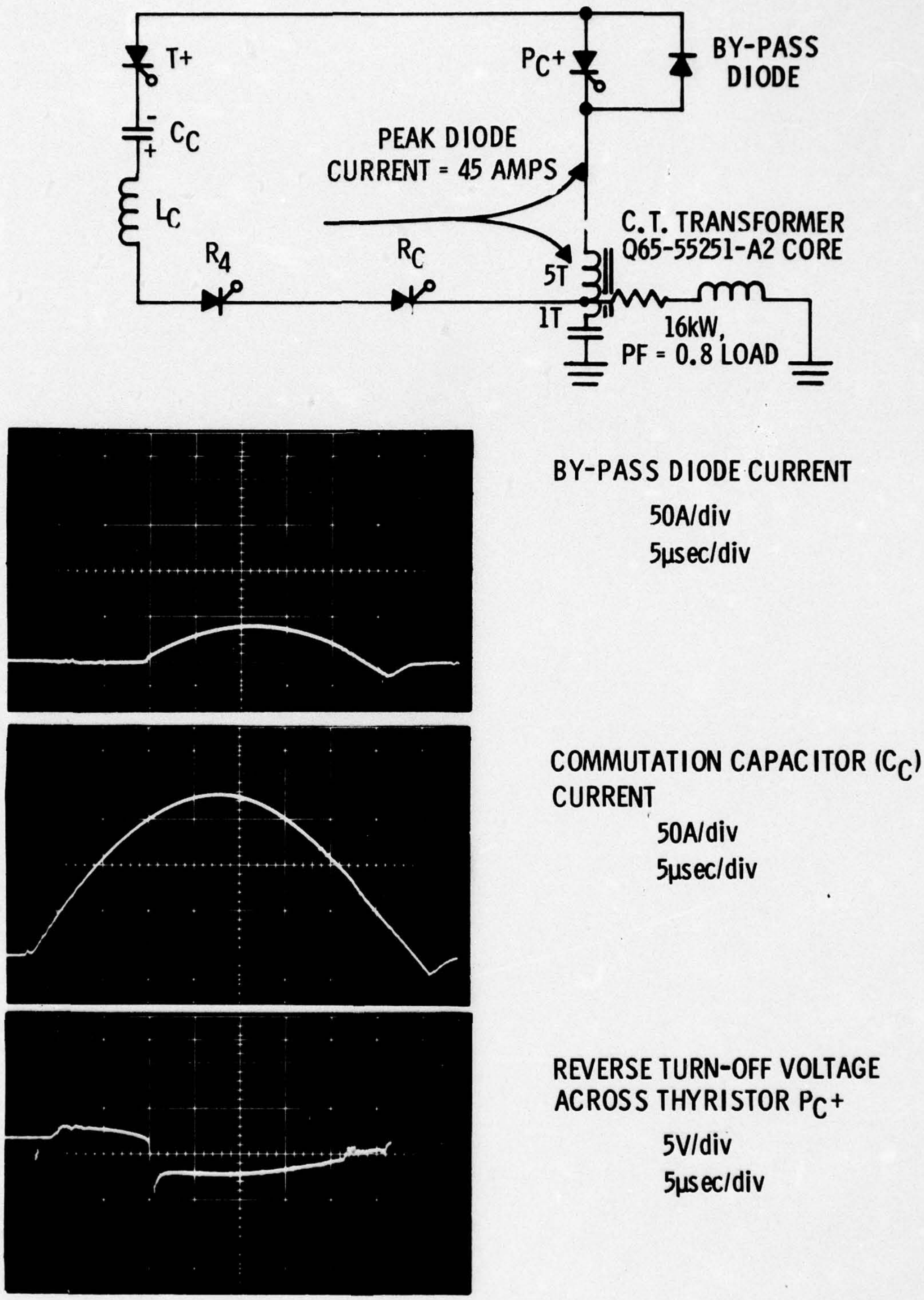
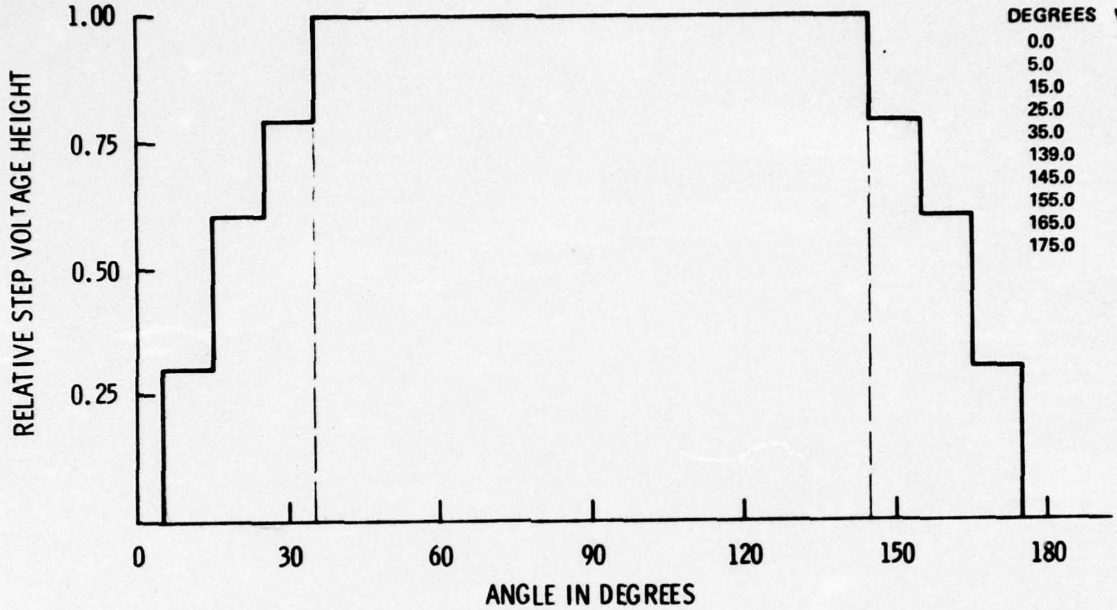


Figure 25. Power Center Thyristor Turn-Off Circuit with C.T. Transformer



DEGREES	VOLTAGE
0.0	0.00
5.0	0.31
15.0	0.61
25.0	0.79
35.0	1.00
139.0	1.00
145.0	0.79
155.0	0.61
165.0	0.31
175.0	0.00

Figure 26. Computer Calculated Waveform Design 110° Wide Power Center, 10° Wide Steps, Zero Dwell Line-to-Neutral THD = 19.14% Line-to-Line THD = 5.6%

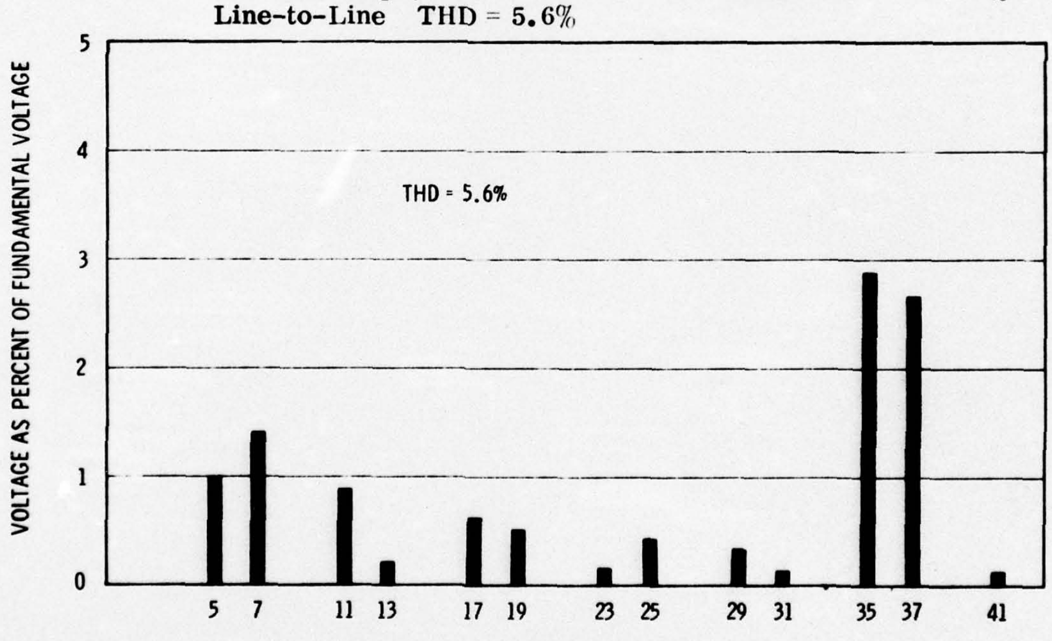


Figure 27. Individual Non-Triplen Harmonics Computed for the 110° Wide Power Center Waveform

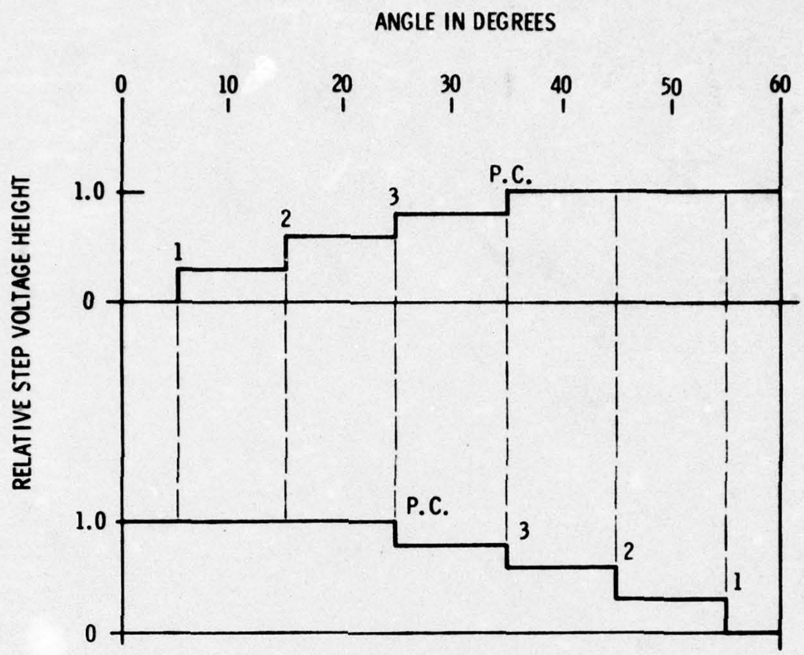


Figure 28. Step Voltage Relationships Between Two Phases for the 110° Wide Power Center Waveform

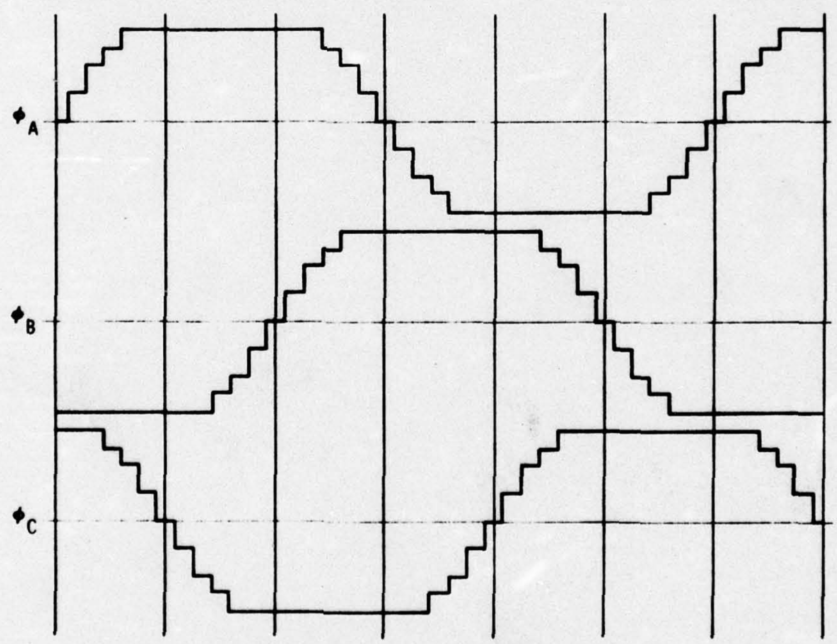


Figure 29. 110° Wide Power Center Wave Three Phase Layout

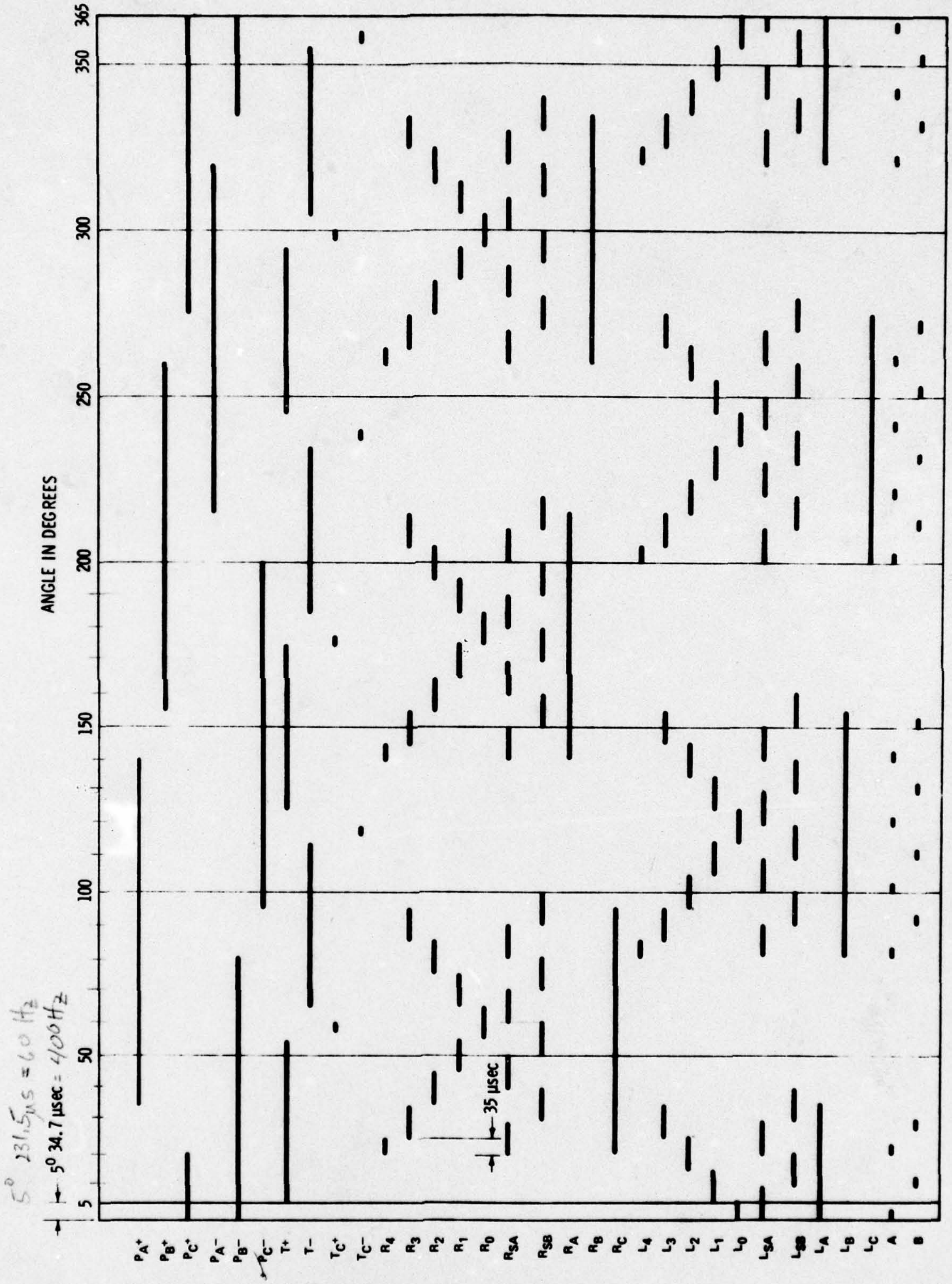


Figure 30. Thyristor Gate Timing Chart for 110° Wide Power Center, 10° Wide Step, Zero Dwell Waveform

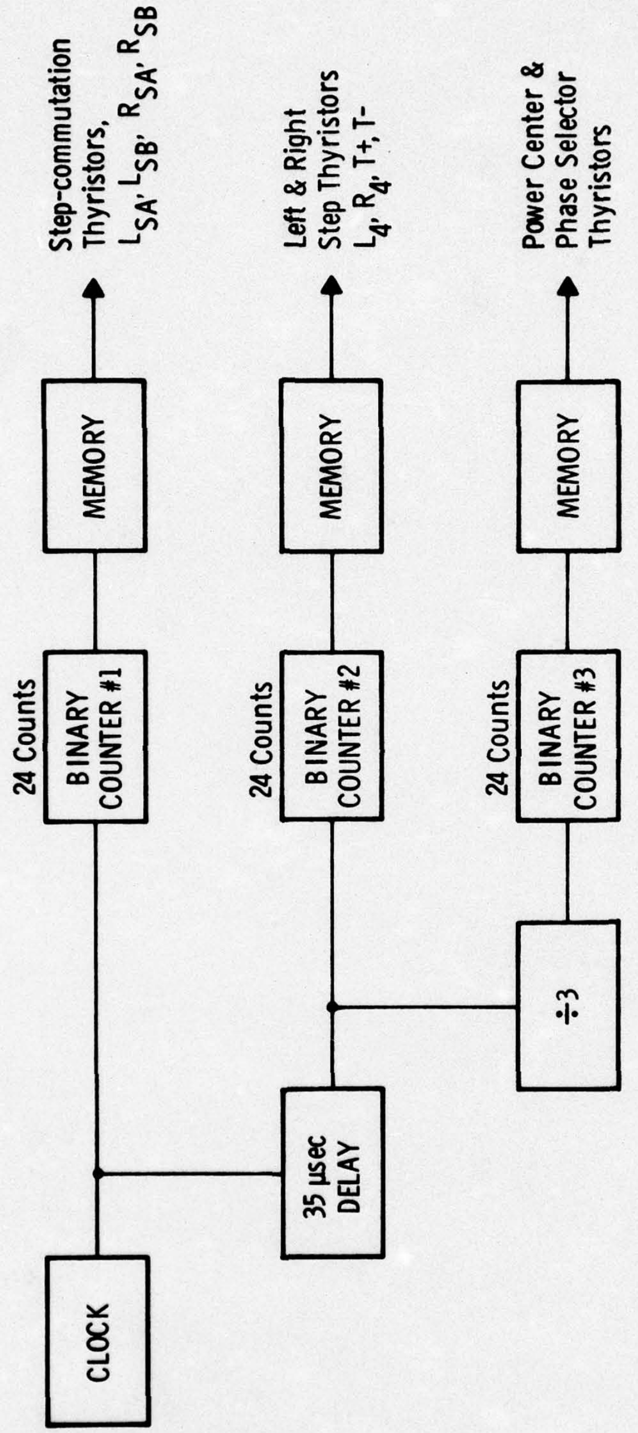


Figure 31. Block Diagram of Memory Timing Circuit

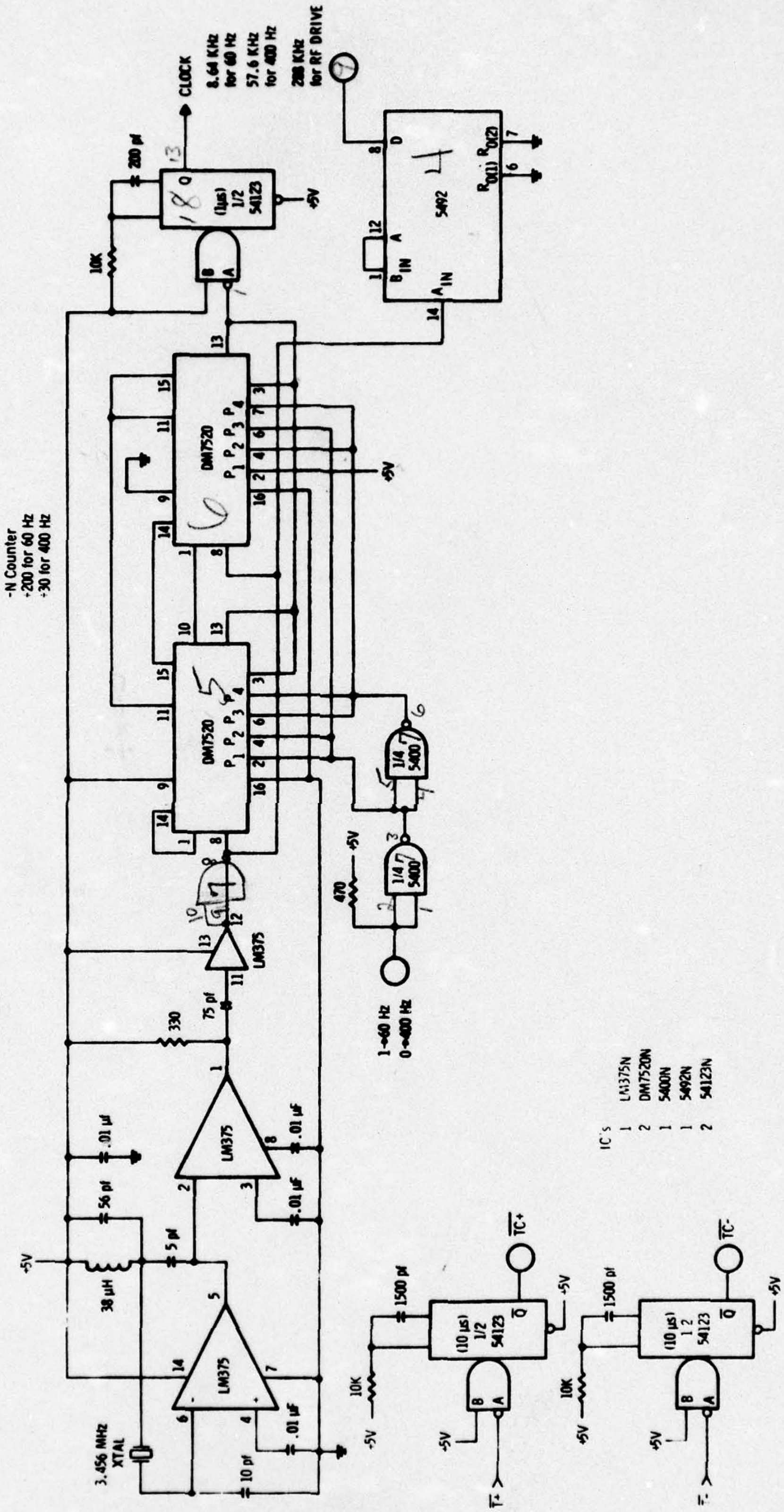


Figure 32a. 110° Wide Power Center Memory Timing Circuit

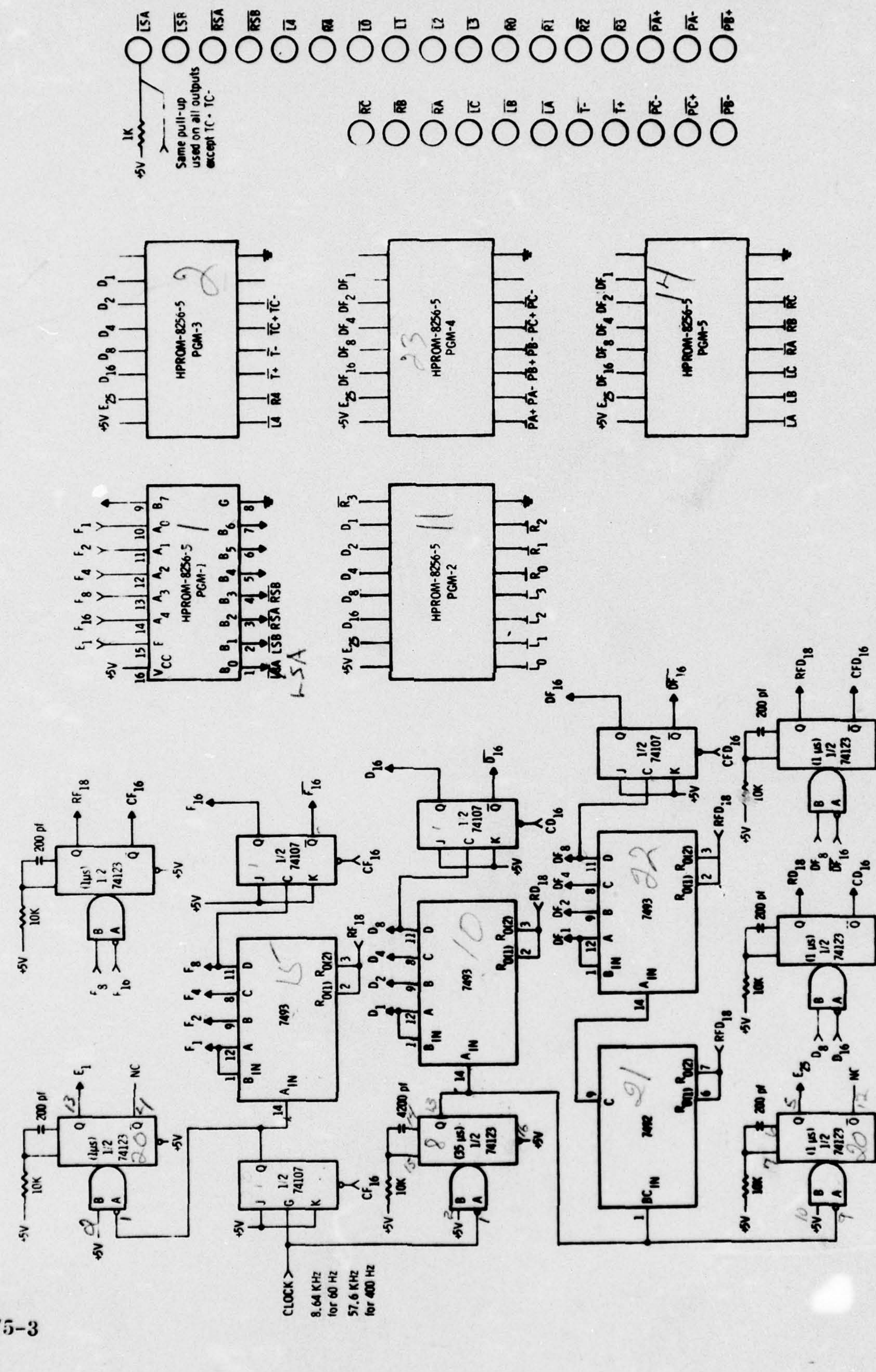


Figure 32b. 110° Wide Power Center Memory Timing Circuit

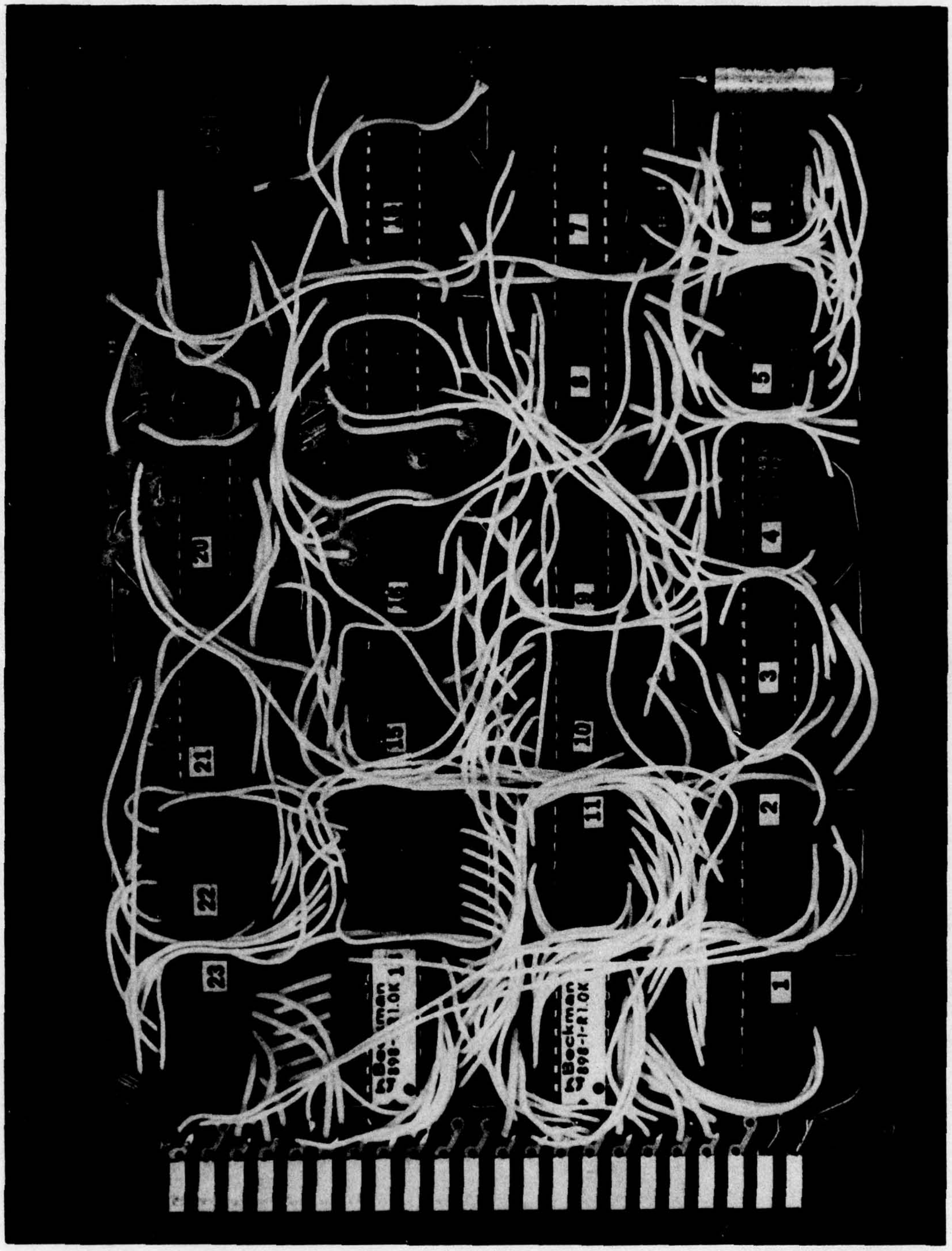


Figure 33. Memory Timing Circuit

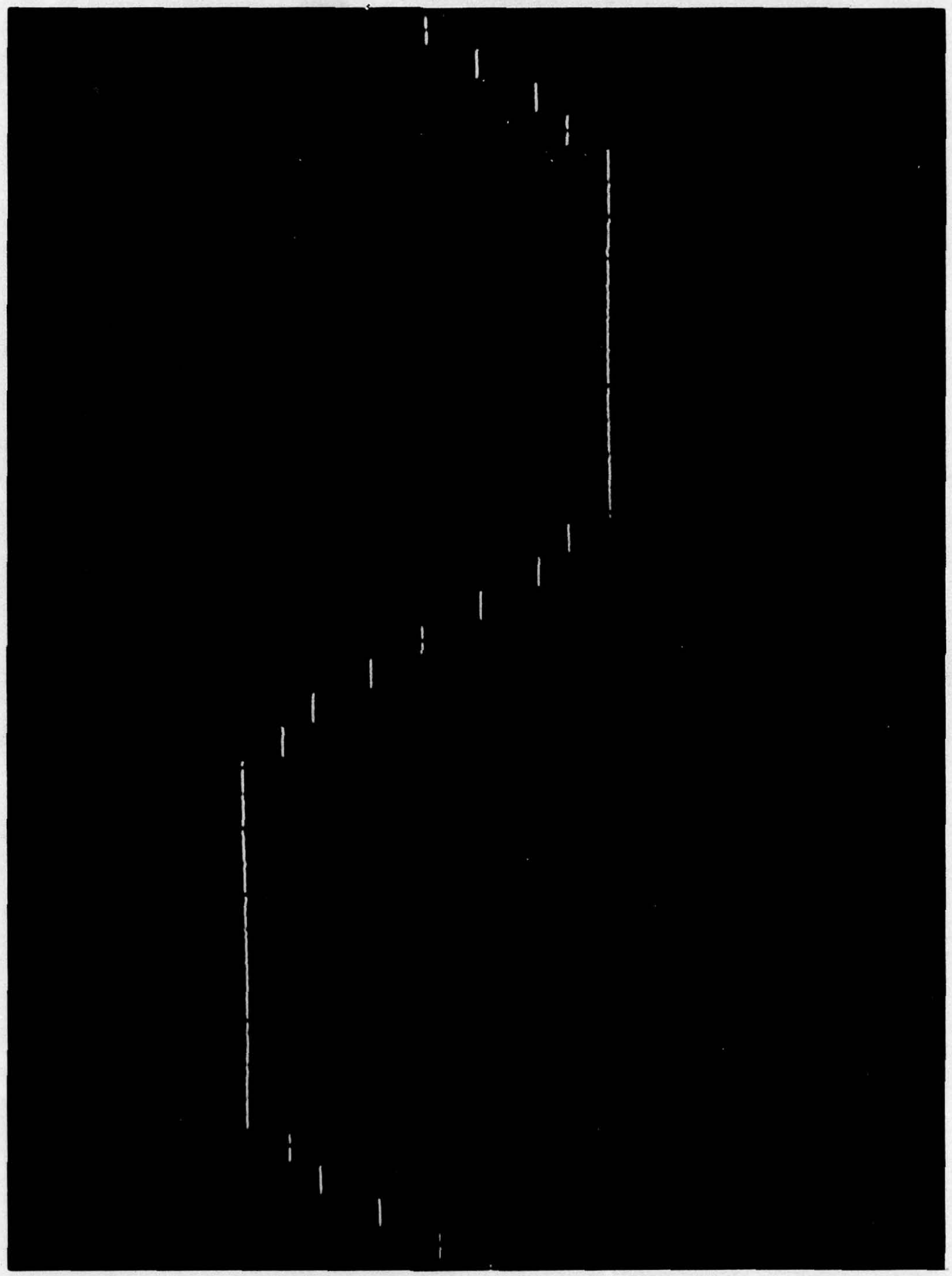


Figure 34. 110^{o} Wide Power Center Line-to-Neutral Voltage Generated by the Item 0006 Inverter

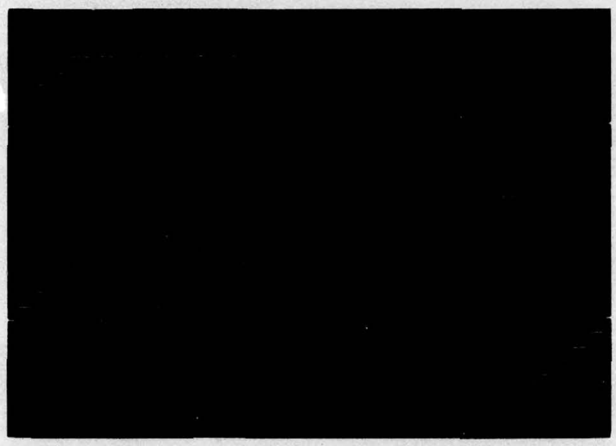


Figure 35. Top Trace: Input to Triplen Attenuator. Bottom Trace: Output of Triplen Attenuator

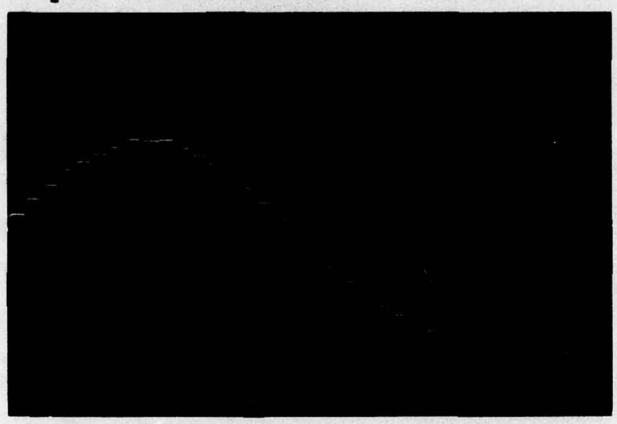


Figure 36. Unfiltered Line-to-Neutral Voltage

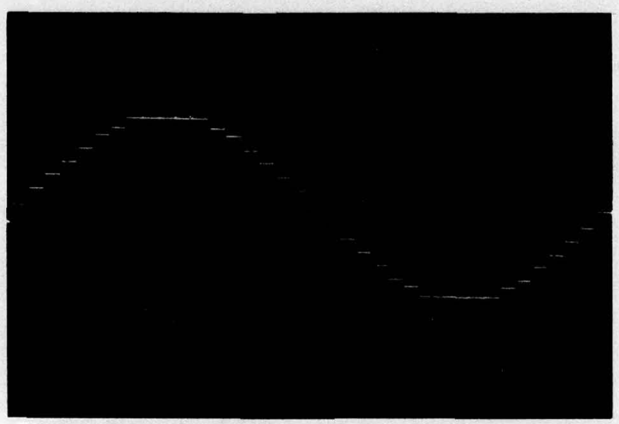


Figure 37. Unfiltered Line-to-Line Voltage

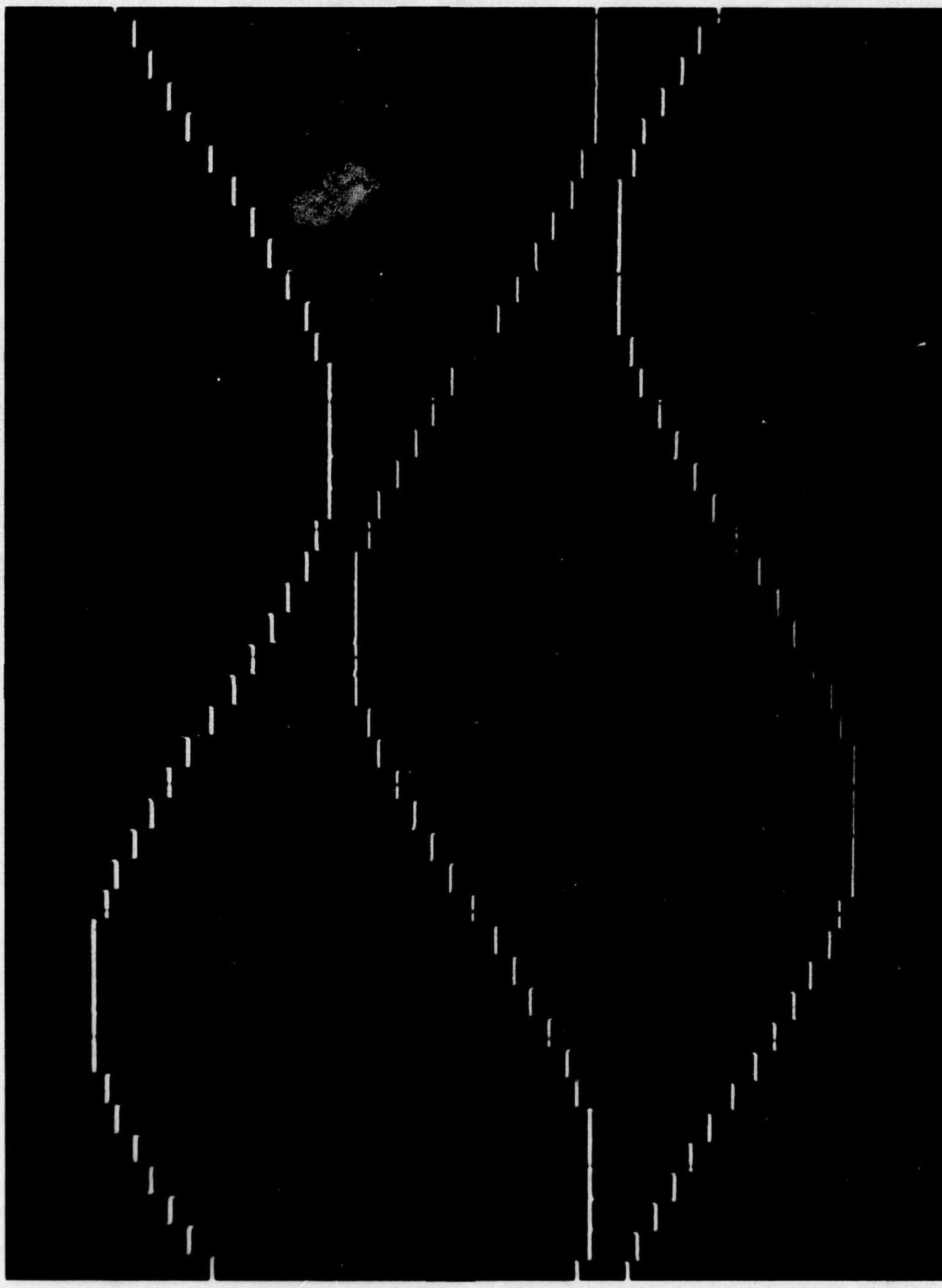


Figure 38. Three Phase Line-to-Line Inverter Output Voltage

APPENDIX A

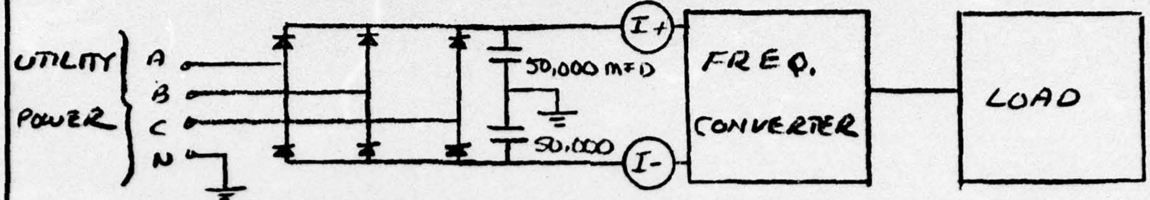
TASK G. DOCUMENTATION OF TECHNICAL DATA

APPENDIX A

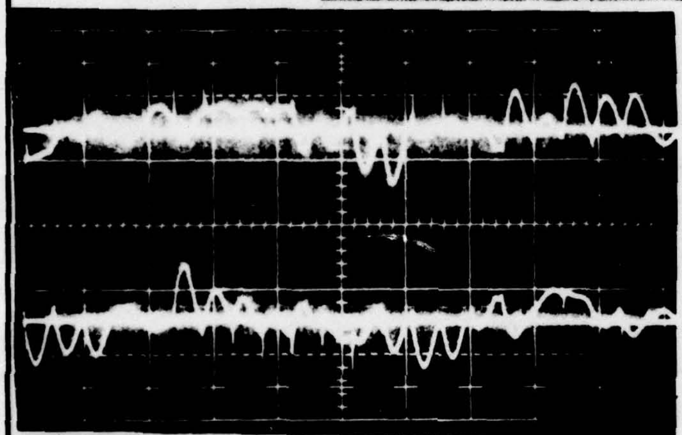
Task g. Documentation of Technical Data

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 1
TITLE CIRCUIT DESIGN DATA 15KVA FREQUENCY CONVERTER ITEM NO. 0006 CONTRACT NO. DAAK02-72-C-0210		PREPARED CORRY		DATE 11/12/7
		CHECKED		
		APPROVED		

CIRCUIT DESIGN TEST DATA 60HZ



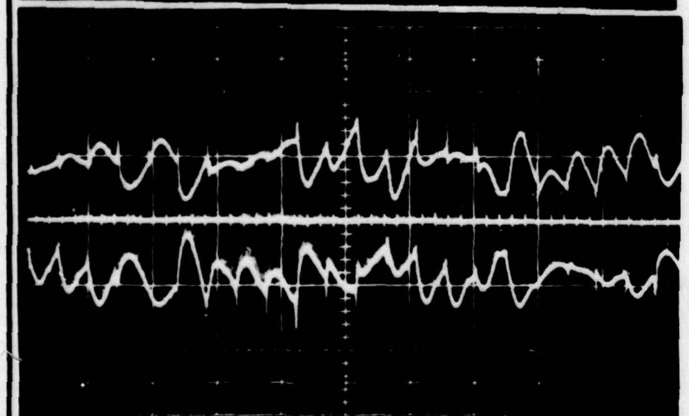
INVERTER INPUT CURRENT - 60HZ 3 PHASE



I+
0
0
I-

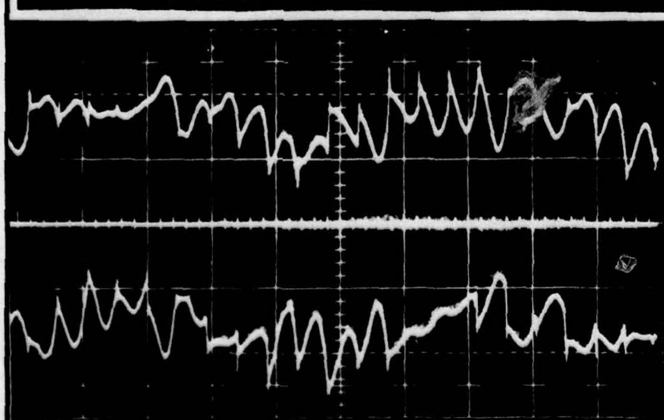
NO LOAD INPUT CURRENT

50A/DIV.
1MS/DIV



I+
0
I-

11KW, PF = 0.8



I+
0
I-

20.6 KW, PF = 0.8

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GENERAL MOTORS CORPORATION

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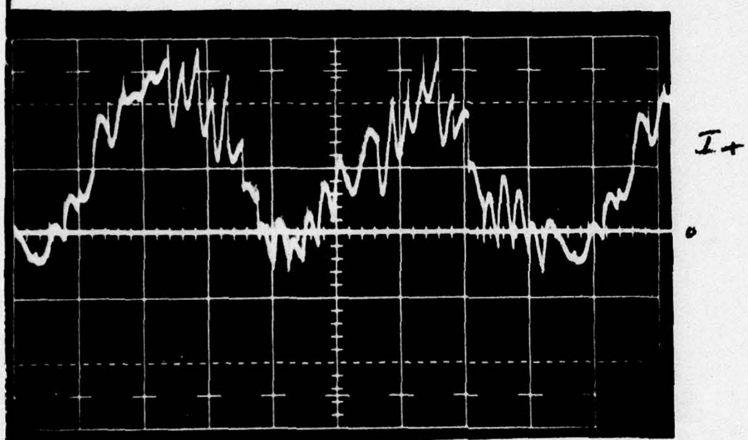
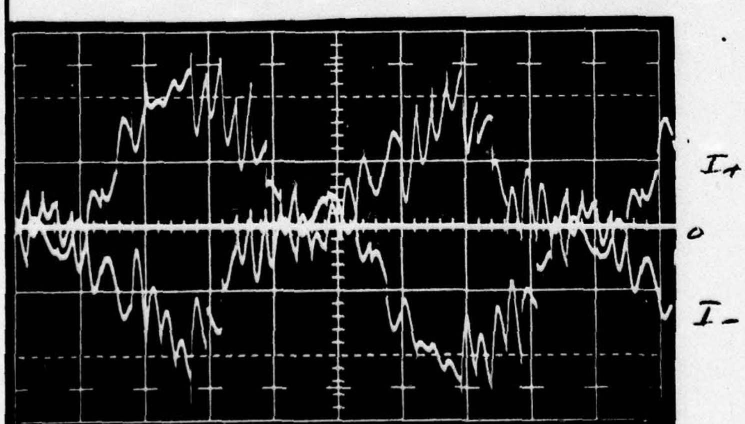
INVERTER DC INPUT CURRENT - 60HZ SINGLE PHASE



10KW, PF= 0.8

50A/DIV.

2ms/DIV.



10KW, PF= 0.8

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TITLE		PREPARED	CORRY	DATE 11/12/7?
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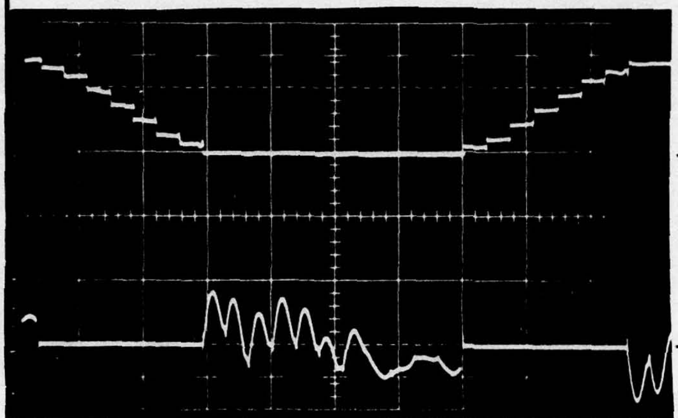
POWER CENTER THYRISTOR VOLTAGES AND CURRENTS 60HZ, THREE PHASE



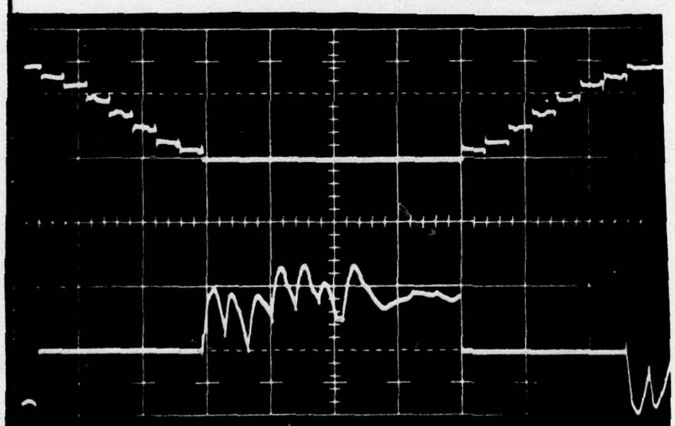
-0

-0

POWER CENTER THYRISTOR VOLTAGE 200 V/DIV.

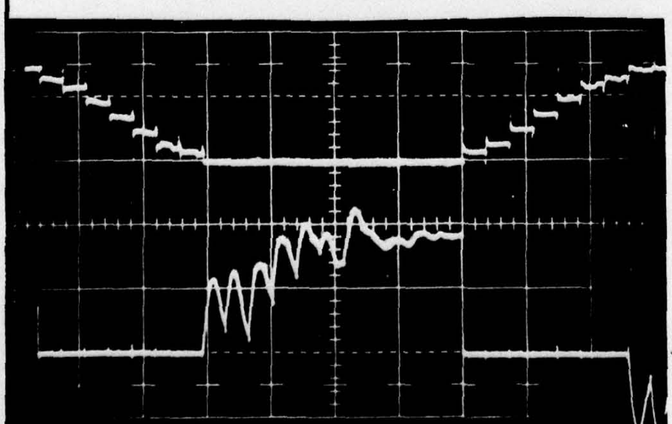
NO LOAD

THYRISTOR & DIODE CURRENT 50A/DIV.



-0

11KW, PF=0.8



-0

20.6 KW, PF=0.8

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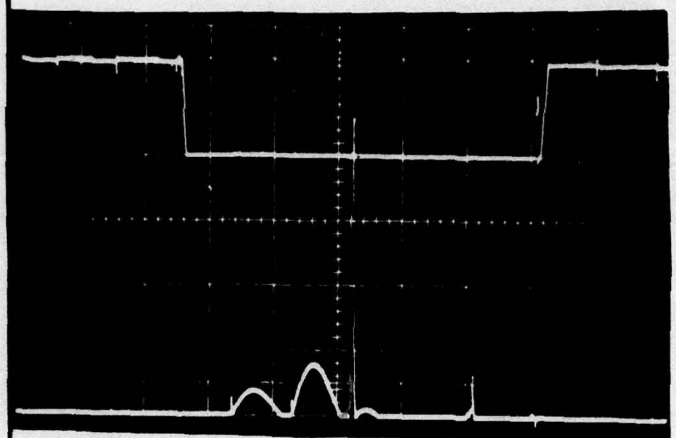


T- THYRISTOR VOLTAGE

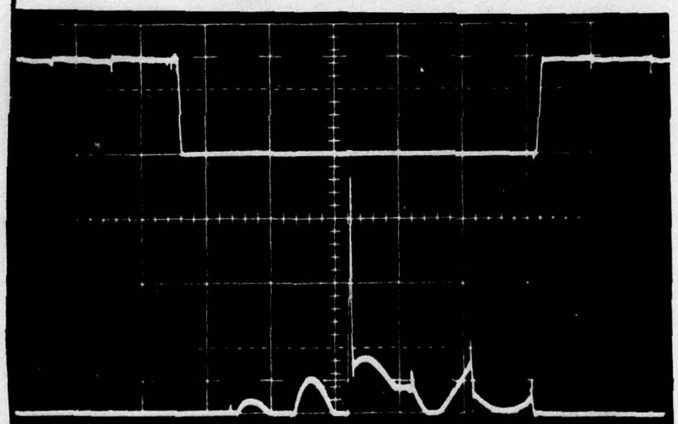
200V / DIV.

NO LOAD

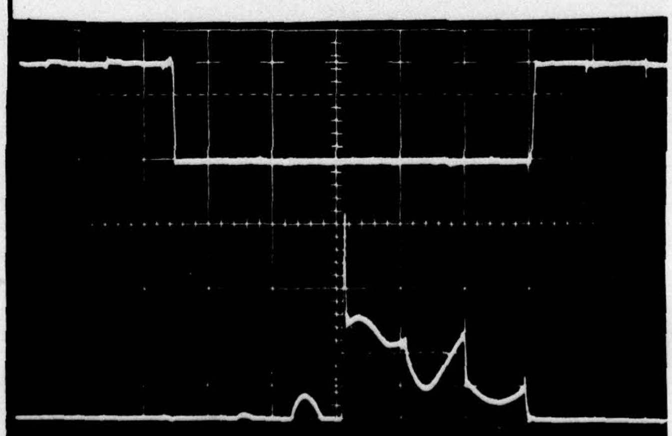
T- CURRENT

50A / DIV.

0.5ms / DIV.



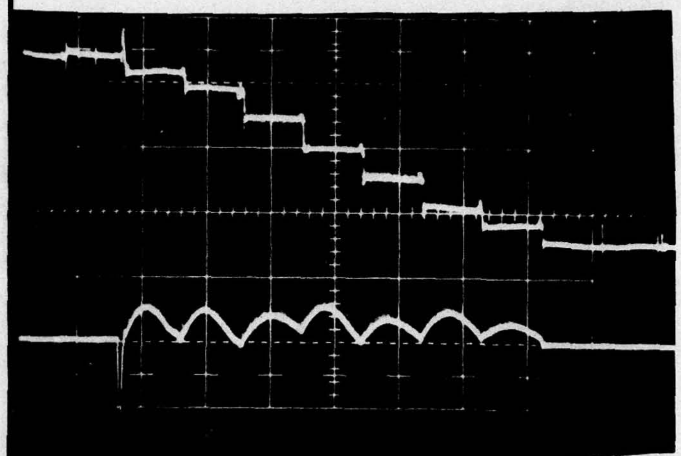
11KW, PF = 0.8



20.6 KW, PF = 0.8

DISTRIBUTION:

STEP VOLTAGES AND CURRENTS - 60HZ, THREE PHASE



0

0

RC. 3 2 1 0 1 2 3

LEFT SIDE STEP VOLTAGE

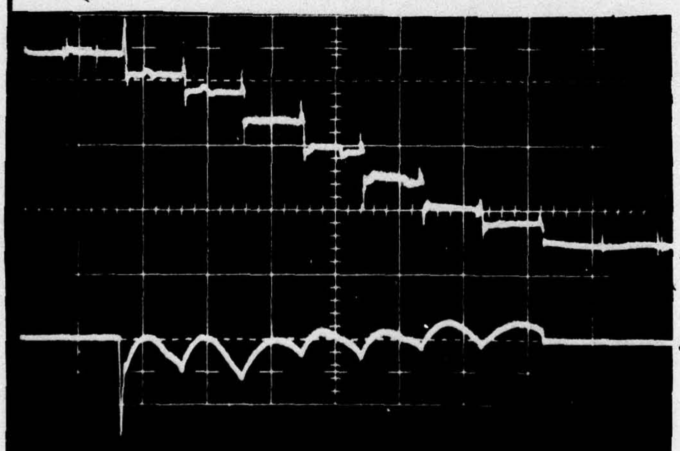
100V/DIV,

NO LOAD

STEP CURRENT

100A/DIV.

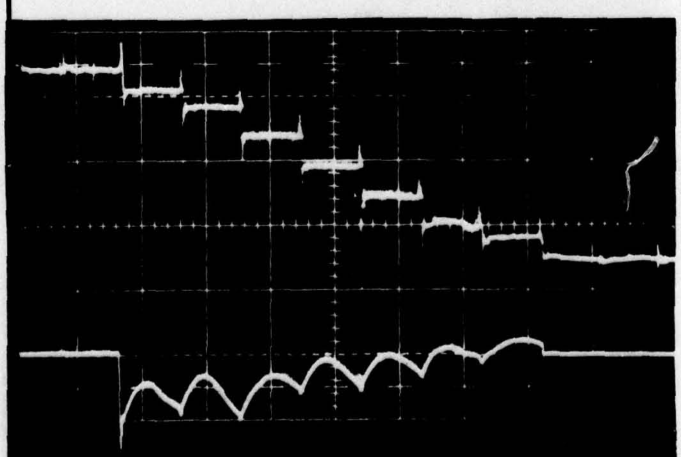
0.5MS/DIV.



0

0

11KW, PF=0.8



-0

0

20.6KW, PF=0.8

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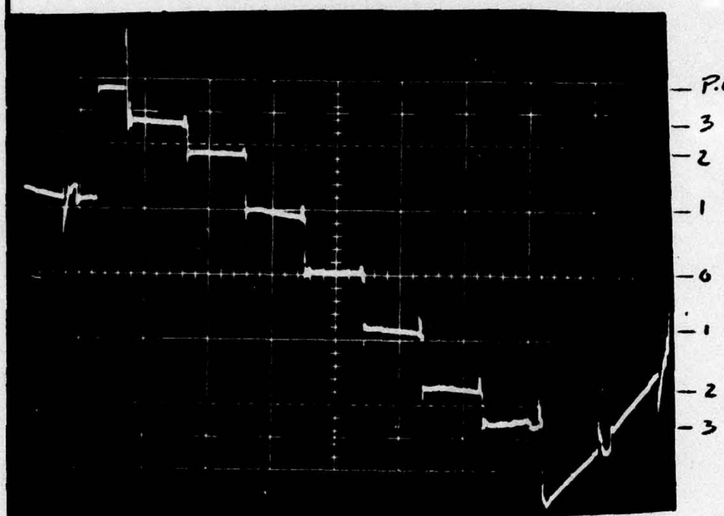
AUTOTRANSFORMER STEP VOLTAGES 60 HZ, 3 PHASE

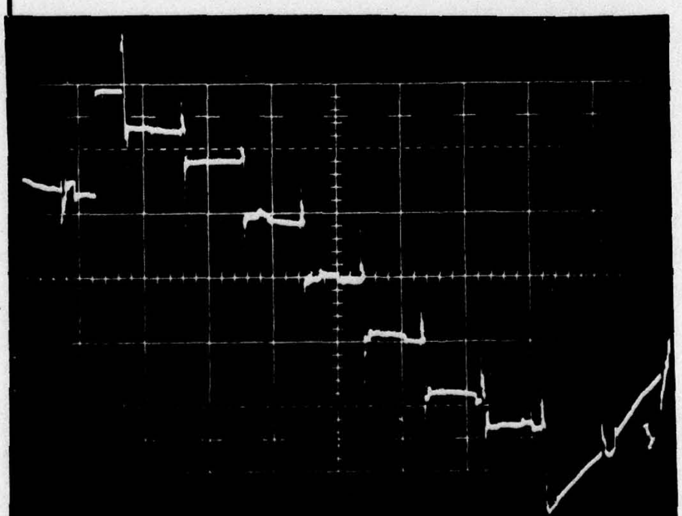


Y STEP FUNCTION

NO LOAD

50V/DIV.

0.5 MS/DIV.



11 KW, PF=0.8

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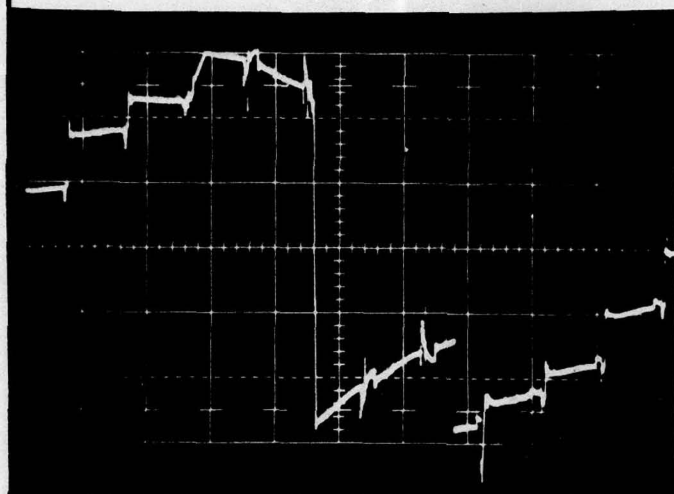
AUTOTRANSFORMER STEP VOLTAGES 60 HZ, 3 PHASE



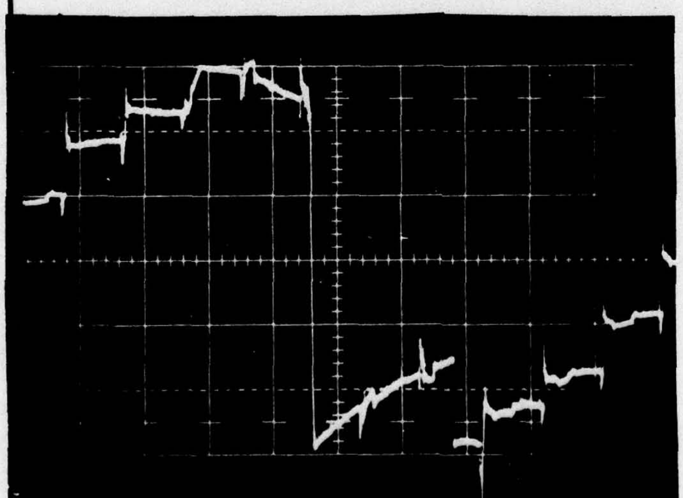
— 3
— 2
— 1
— 0
— 1
— 2
— 3
— P.C.

X STEP FUNCTION

NO LOAD

50V/DIV.

0.5ms/DIV.



11KW, PF=0.8

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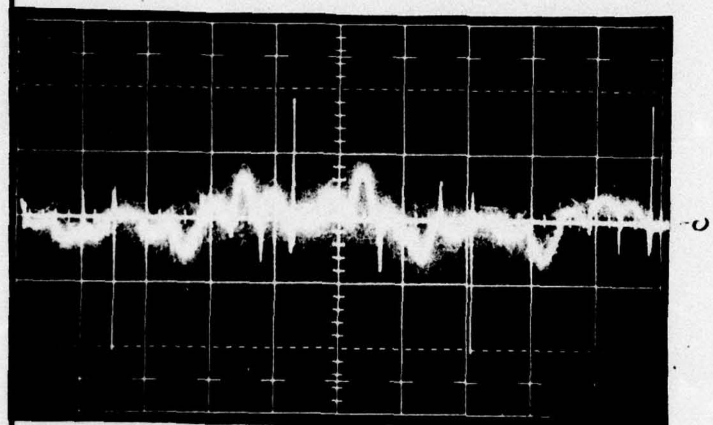
	CHECKED	
	APPROVED	

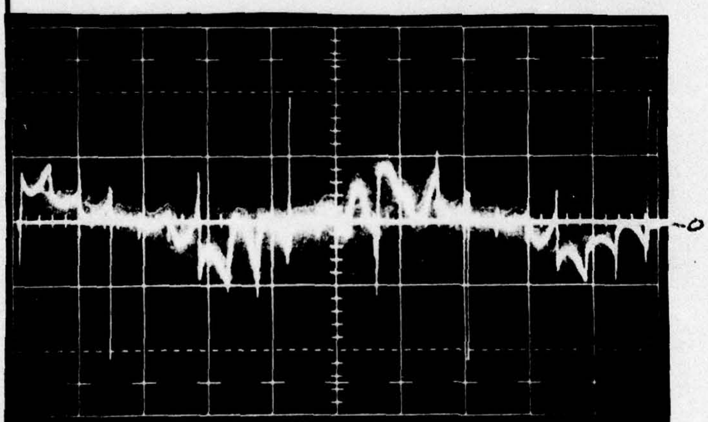
STEP TRANSFORMER CURRENT 60HZ, THREE PHASE



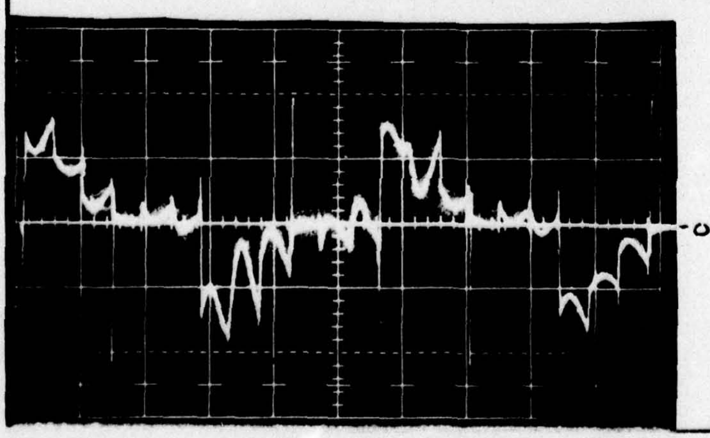
NO LOAD

50 A/DIV.

1ms/DIV.



11KW, PF=0.8



20.6 KW, PF=0.8

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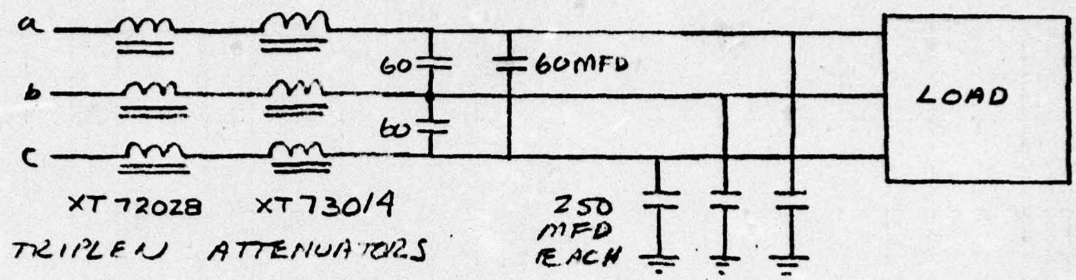
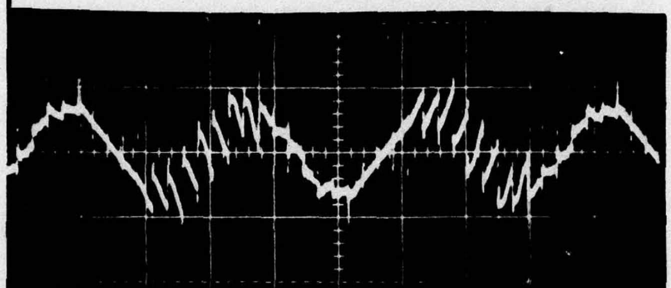
TITLE

PREPARED: CORRY   DATE: 11/12/7[illegible]
CHECKED:
APPROVED:

VOLTAGE DROPS ACROSS TRIPLEN ATTENUATORS - 60HZ, 3 PHASE



OUTPUT FILTER CIRCUIT

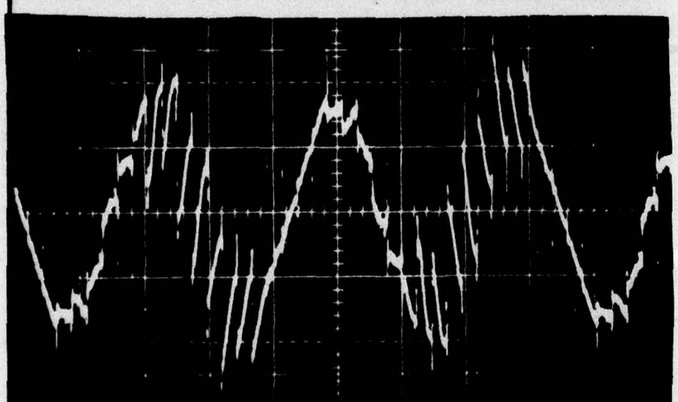


VOLTAGE DROP ACROSS BOTH TRIPLEN ATTENUATORS

NO LOAD

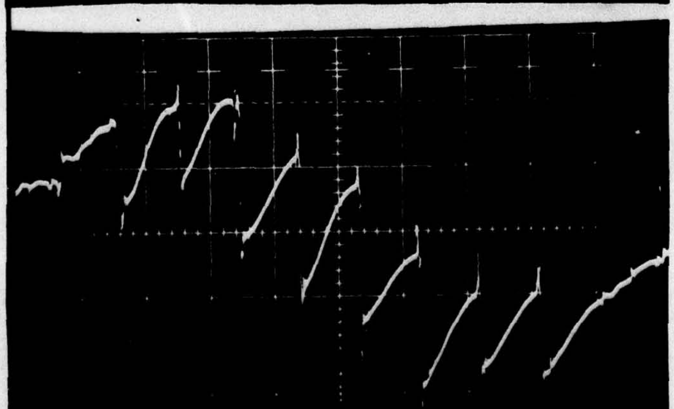
50 V / DIV.

2 ms / DIV.



20V / DIV.

2 ms / DIV.



20V / DIV.

500 μSEC / DIV.

DISTRIBUTION:

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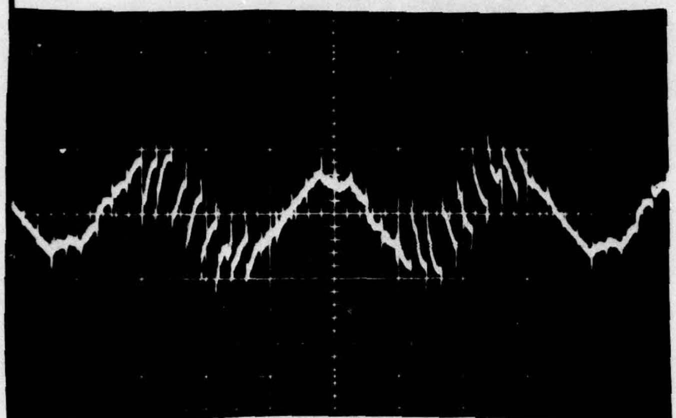
		APPROVED		

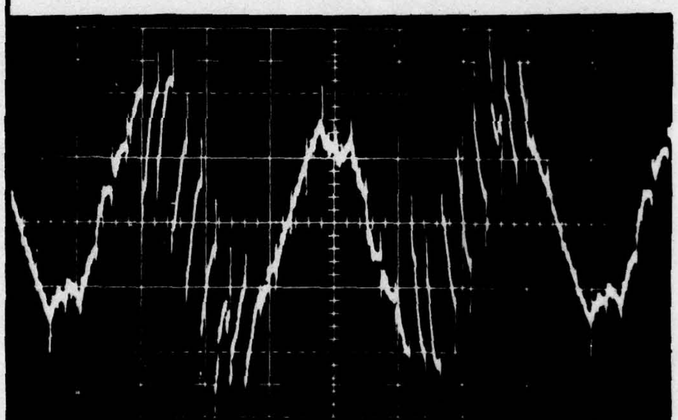


VOLTAGE DROP ACROSS BOTH TRIPLEN ATTENUATORS

20.6 KW, PF=0.8

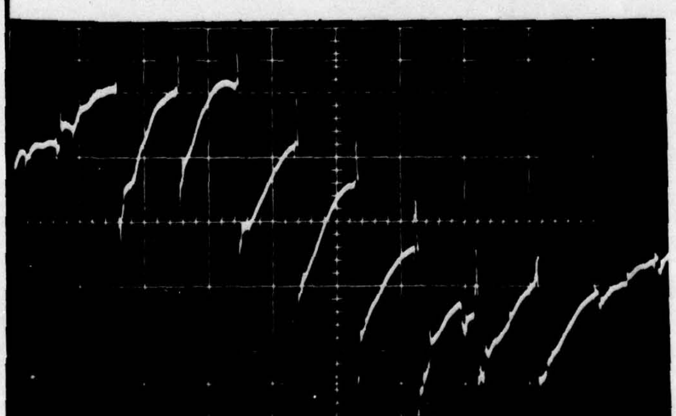
50 V/DIV.

2 ms/DIV.



20 V/DIV.

2 ms/DIV.

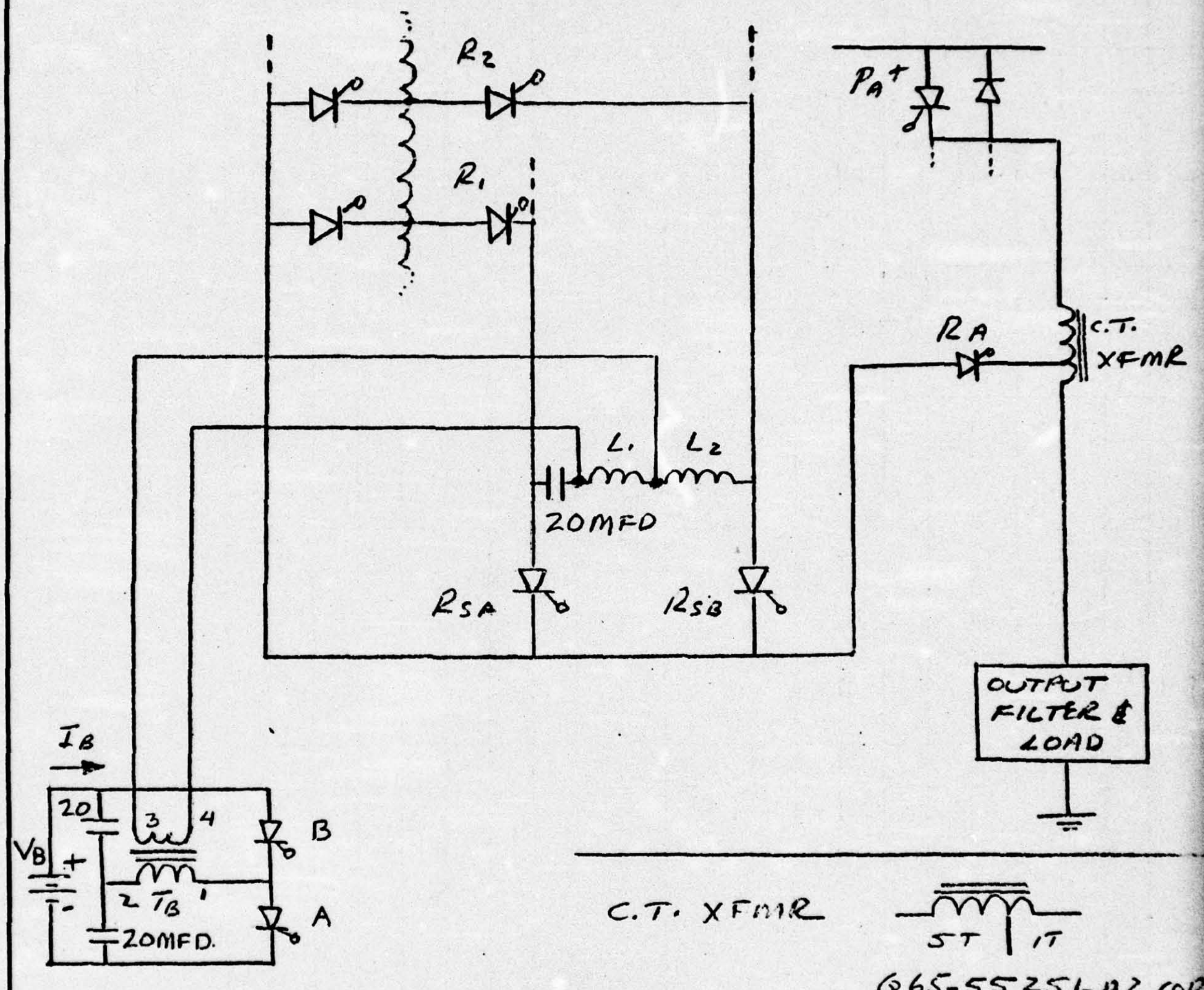


20 V/DIV.

500 μSEC/DIV.

DISTRIBUTION:

MEASUREMENTS OF REVERSE BIAS TURN-OFF VOLTAGES FOR INVERTER THYRISTORS - 60HZ



C.T. XFMR

G65-55251-A2 CORE

FOR TURN-OFF TIME MEASUREMENTS $V_B = 66V$
$I_B = 9$ AMPS

L_1 10 TURNS ON G55-55106-D4 CORE

L_2 8 TURNS ON G-55-55106-D4 CORE
TWO SETS OF TURNS

T_B 20 TURNS PRIMARY
10 TURNS SECONDARY
50001 CORE

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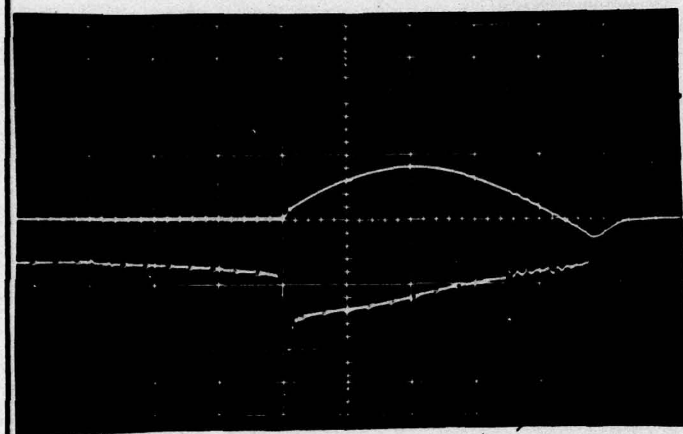
		APPROVED		

REVERSE BIAS TURN-OFF TIMES 60HZ, THREE PHASE

20.6KW PF=0.8 LOADS PAGES 11-17



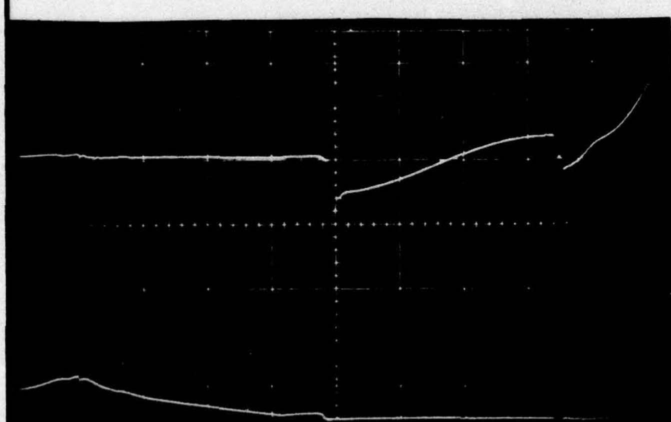
POWER CENTER

Pc TURN OFF

BY-PASS DIODE CURRENT
50A/DIV.

REVERSE BIAS VOLTAGE
5V/DIV.
5μSEC/DIV.

T- TURN-OFF



REVERSE BIAS VOLTAGE
20V/DIV.

5μSEC/DIV.

ANODE CURRENT
50A/DIV.

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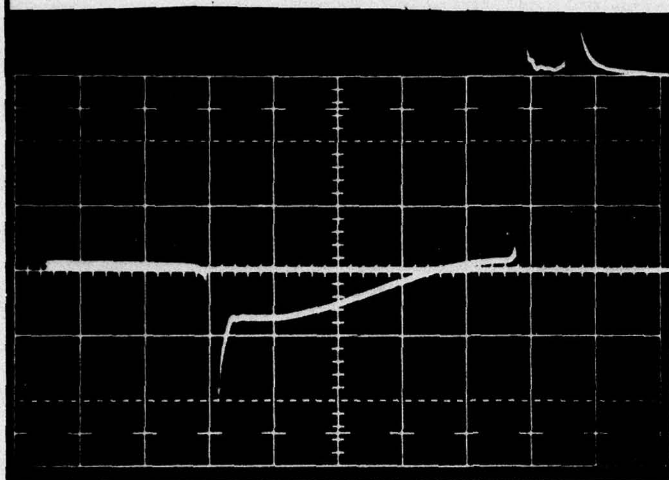


STEP COMMUTATING THYRISTOR LSB TURN-OFF

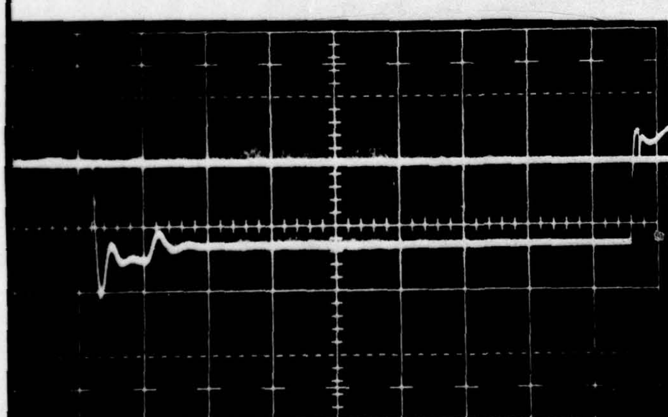
20V/DIV.

5μSEC/DIV.

STEP COMMUTATING THYRISTOR LSA TURN-OFF

20V/DIV.

5μSEC/DIV.



STEP THYRISTOR Lo TURN-OFF

100V/DIV.

50μSEC/DIV.

DISTRIBUTION:

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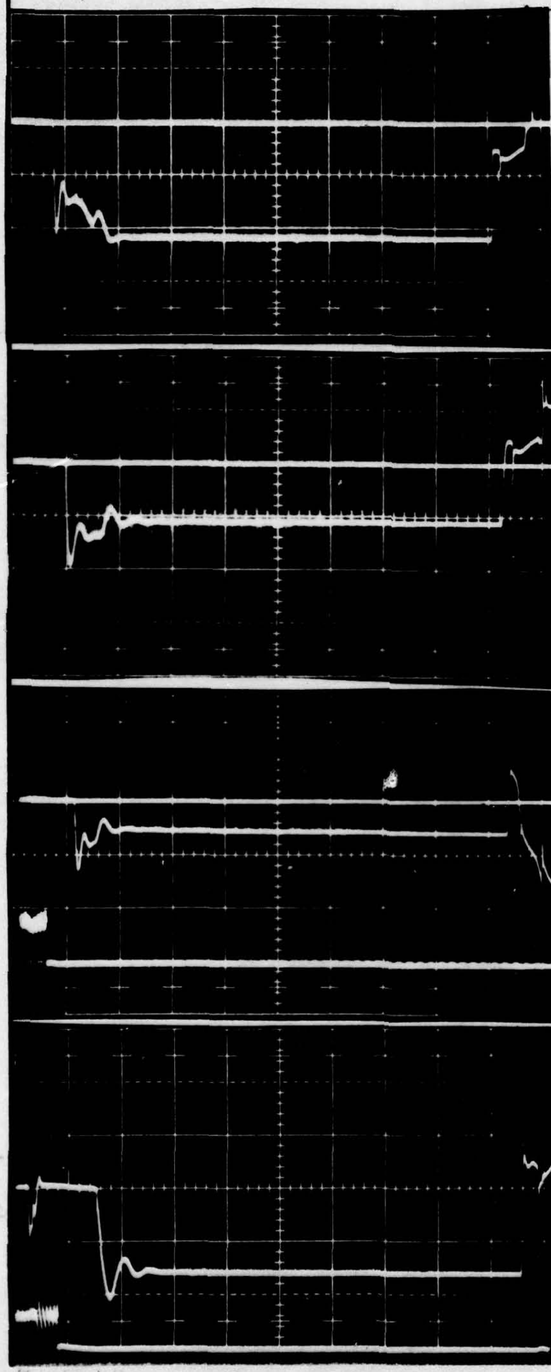

STEP THYRISTOR L_1 TURN-OFF

100V/DIV.

50μSEC/DIV.

STEP THYRISTOR L_2 TURN-OFF

STEP THYRISTOR L_3 TURN-OFF

STEP THYRISTOR L_4 TURN-OFF

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DATE

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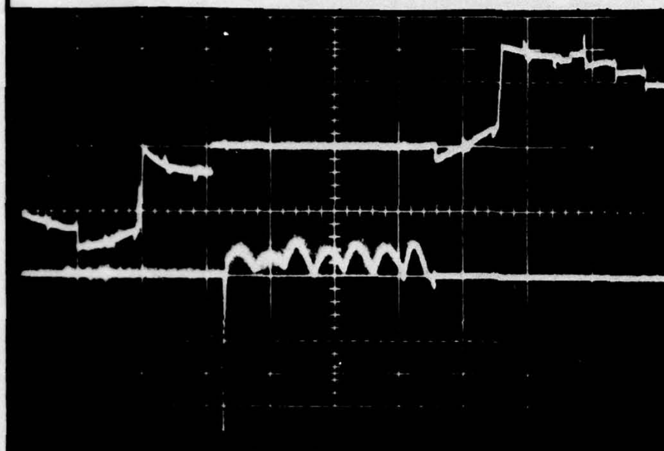
PHASE SELECTOR R_C

TURN-OFF



-0 200V/DIV.

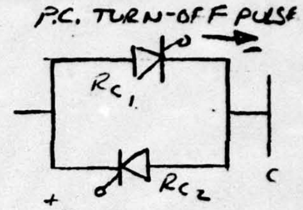
\+

-0 100A/DIV.

\-

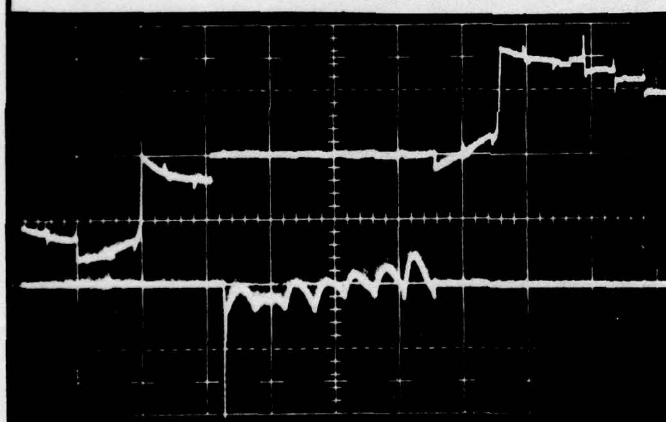
1 MS/DIV.

P.C. TURN-OFF PULSE



NO LOAD CURRENT

P.F. CORRECTED BOTTOM SCR REV. BIASED WHEN P_C TURNS ON



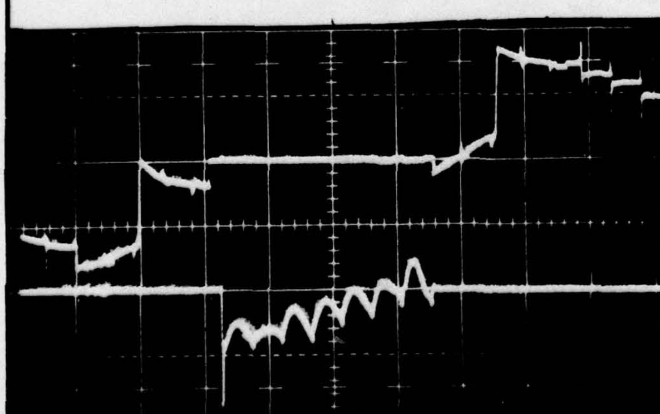
-0

\+

-0

\-

11KW, PF=0.8



-0

\+

-0

\-

20.6 KW, PF=0.8

REVERSED BIASED FOR 400 µSEC. WHEN P_C TURNS-ON

FOR LOW P.F. LAGGING LOADS (NEG. CURRENT) TOP SCR STAEVES OFF.

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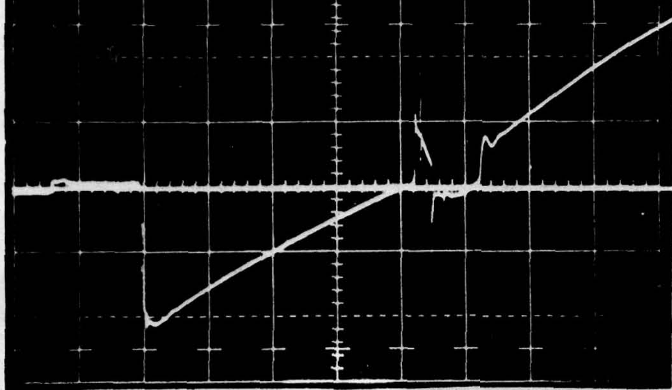
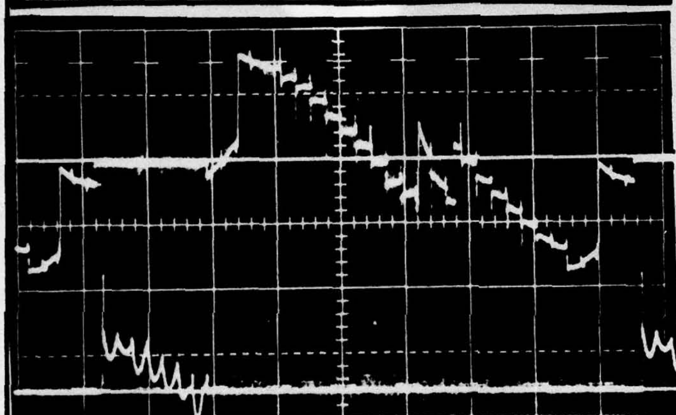
	APPROVED



R_c REVERSE BIASE VOLTAGE

20V/DIV.

100 μSEC/DIV.

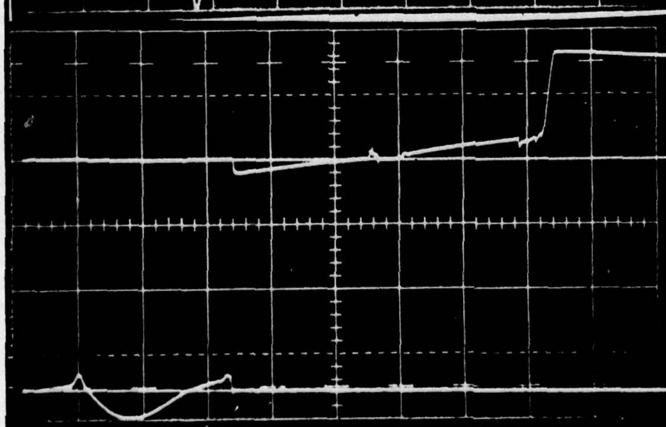


200 V/DIV.

2 mS/DIV.

CURRENT THRU R_{c_2}

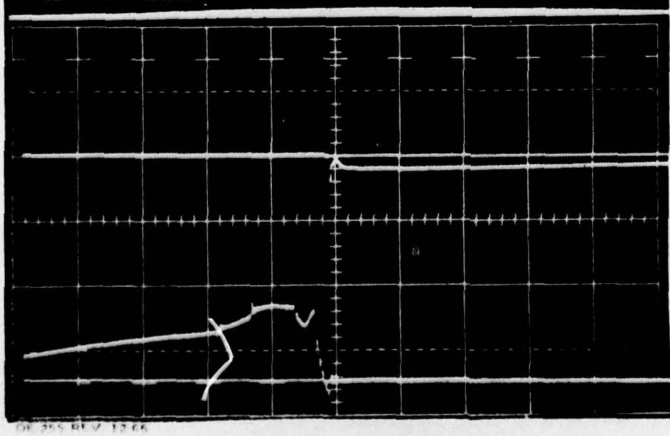
100 A/DIV.



VOLTAGE
200V/DIV.

200 μSEC/DIV.

CURRENT
100A/DIV.



VOLTAGE
200V/DIV.

20 μSEC/DIV

CURRENT
100A/DIV.

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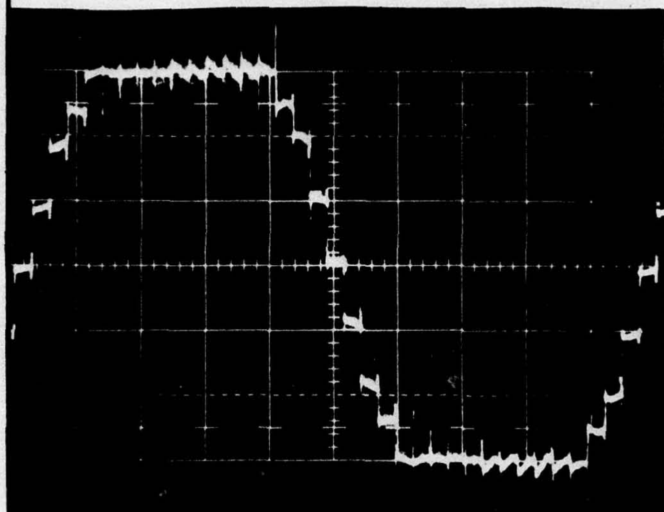
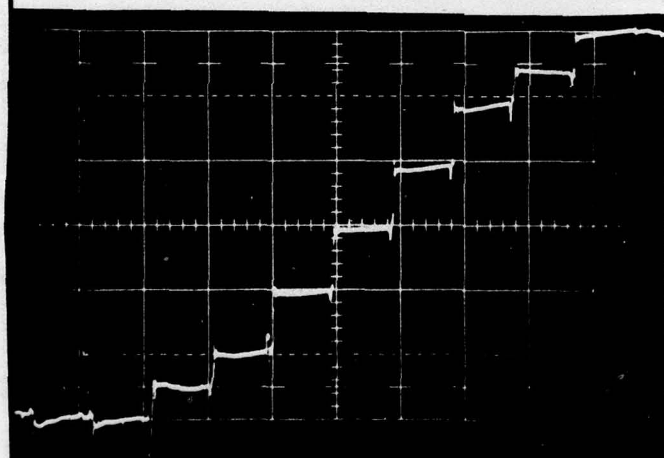
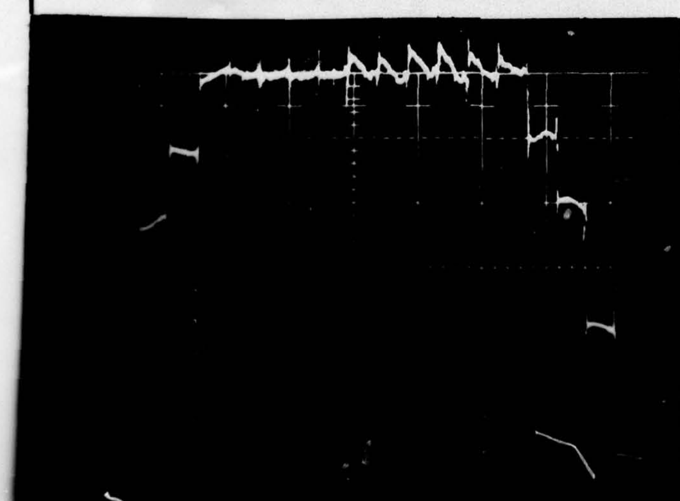
INVERTER BASIC VOLTAGES 60HZ NO LOAD



V_{c-n}



0.5 ms/DIV.



1 ms/DIV.

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 17
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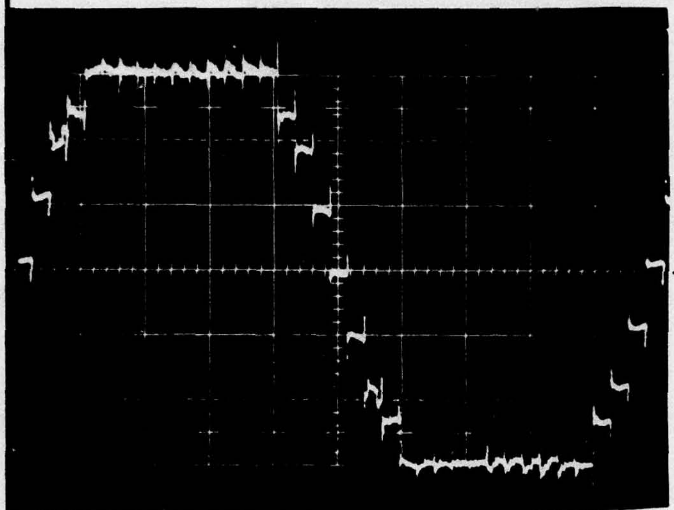
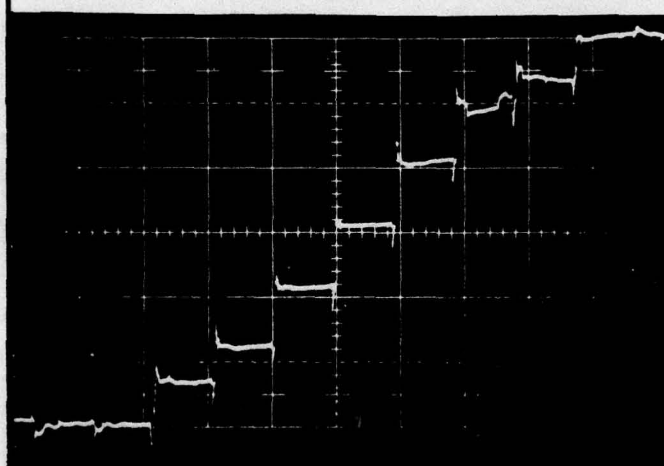
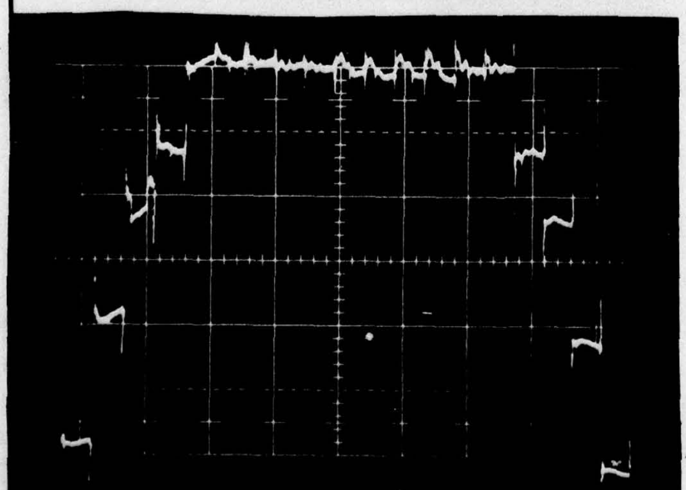
INVERTER BASIC VOLTAGES 60HZ 20.6KW, PF=0.8



Vc-n



0.5 ms/DIV.



1 ms/DIV.

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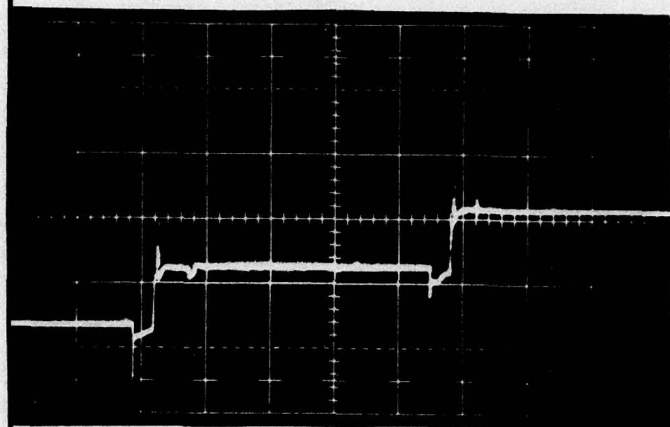
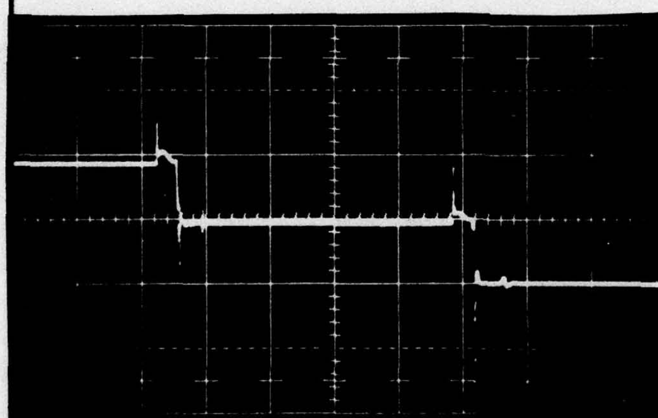
INVERTER BASIC VOLTAGES 60 HZ NO LOAD



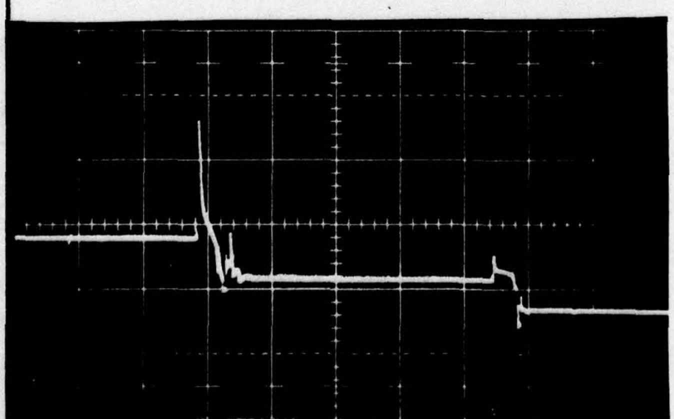
ASCENDING STEPS
2, 1, 0

50V/DIV.

100 μSEC/DIV.



DESCENDING STEPS
1, 0, 1



POWER CENTER AND
STEPS 3, 2

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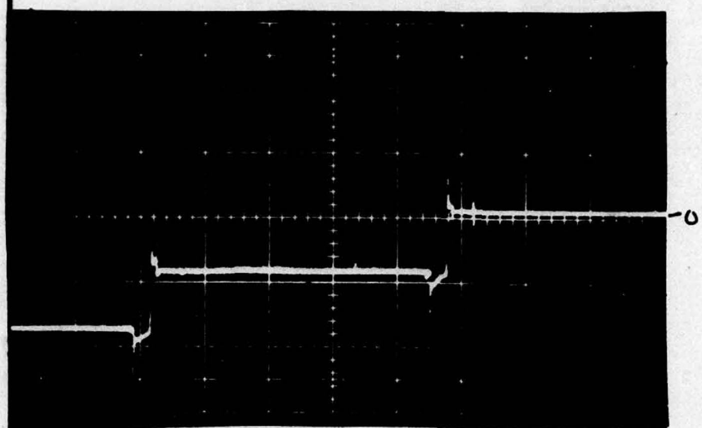
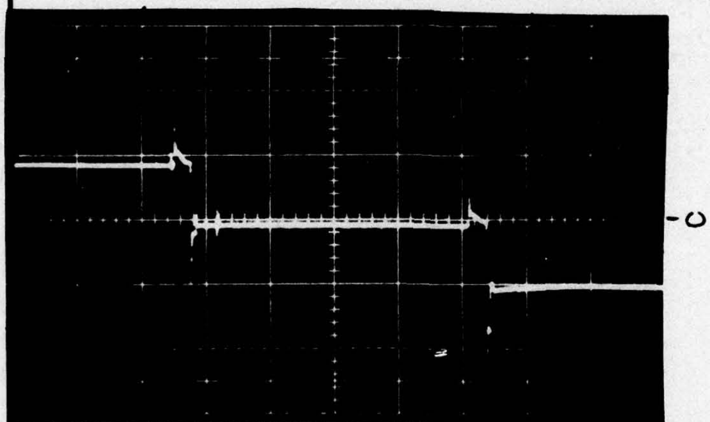
INVERTER BASIC VOLTAGES 60Hz 16KW, PF=0.8

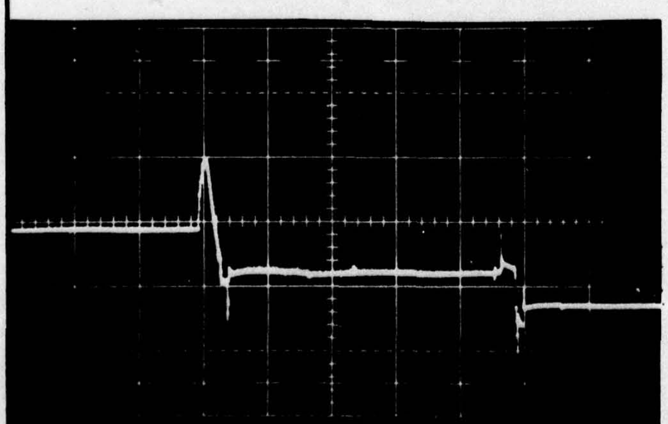


ASCENDING STEPS
2, 1, 0
50 V/DIV.

100 μSEC/DIV.



DESCENDING STEPS
1, 0, 1



POWER CENTER AND
STEPS 3, 2

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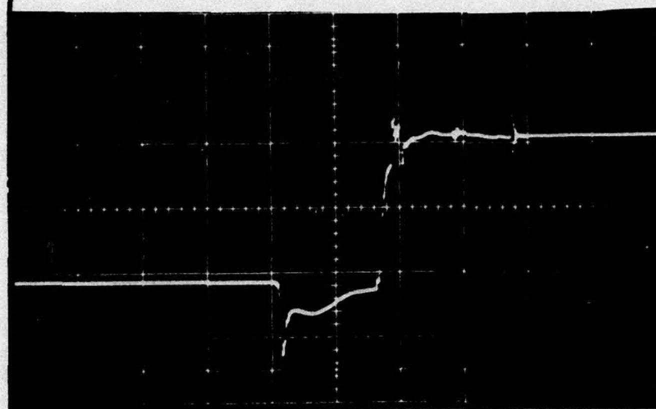
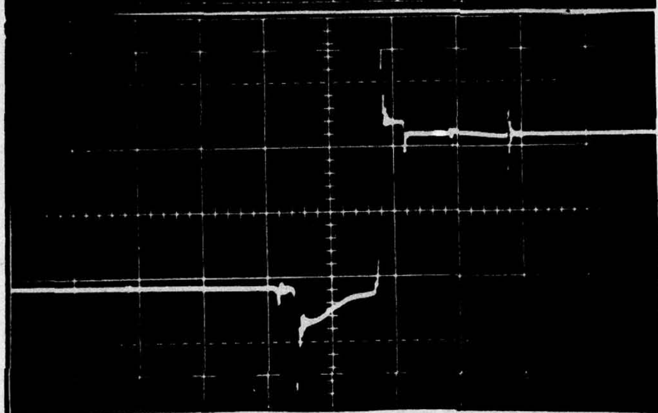


-0

ASCENDING

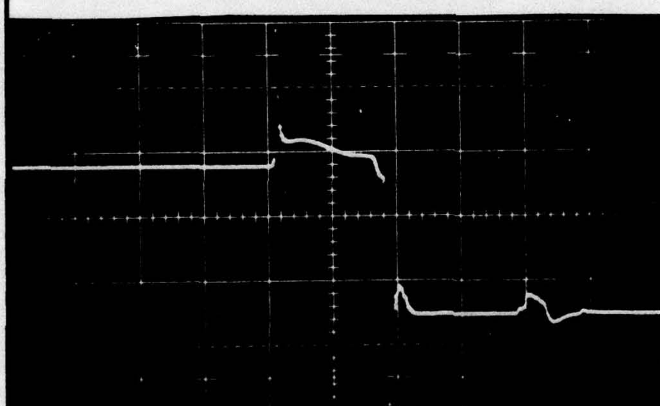
20V/DIV.
20 μSEC/DIV.

NO LOAD



-0

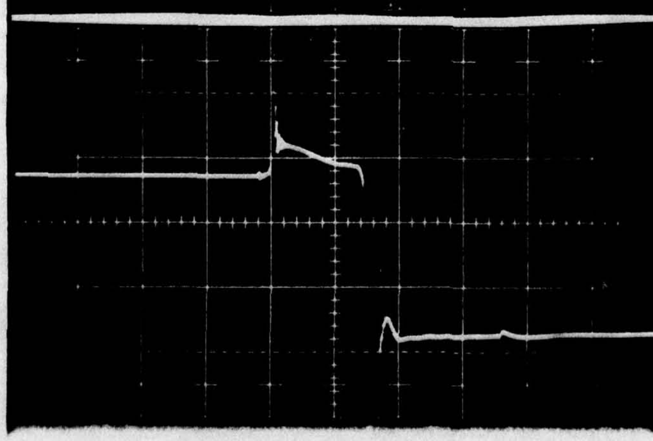
16KW, PF=0.8



-0

DESCENDING

NO LOAD



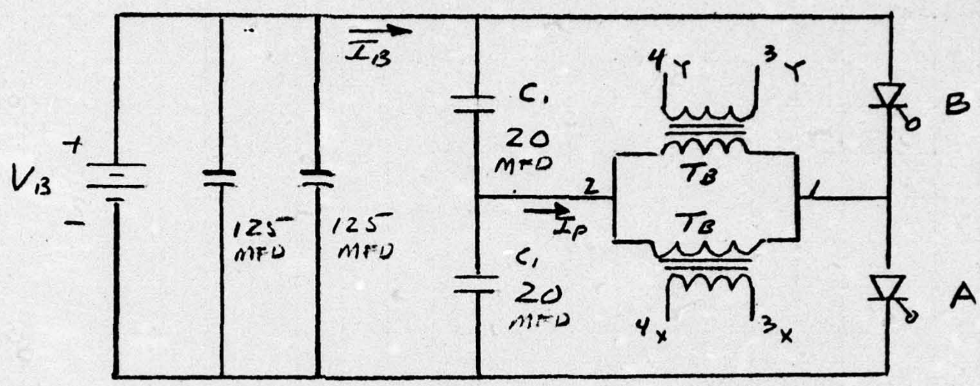
-0

16KW, PF=0.8

DISTRIBUTION:

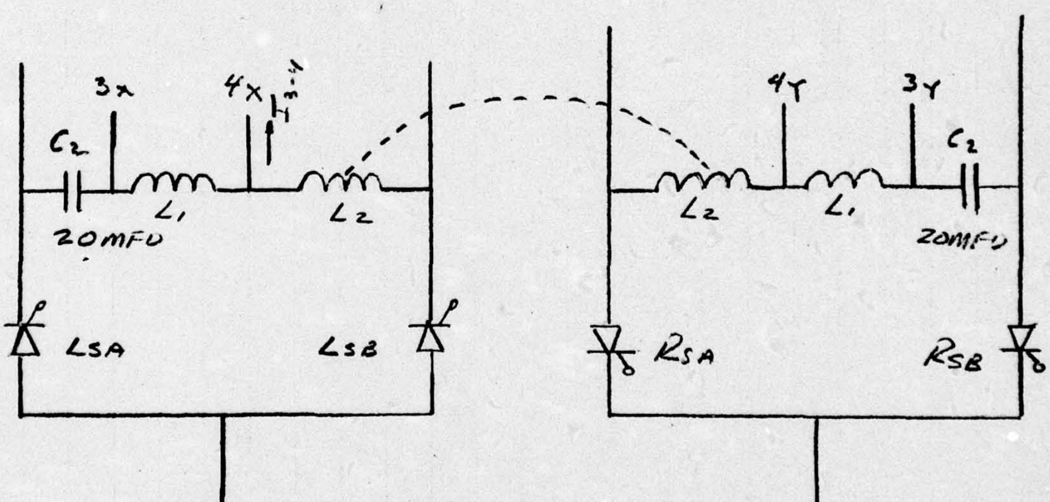
COMMUTATION BOOST CIRCUIT VOLTAGE AND CURRENT WAVEFORMS

(60 HZ OPERATION)



X STEPS

Y STEPS



	V_{RMS}	I_{RMS}
C_1	100	32
C_2	135	50

$V_B = 66$ VDC

$I_B = 9$ AMPS DC

$V_{3-4} = 14.2$ VRMS.

$I_{3-4} = 67$ ARMS

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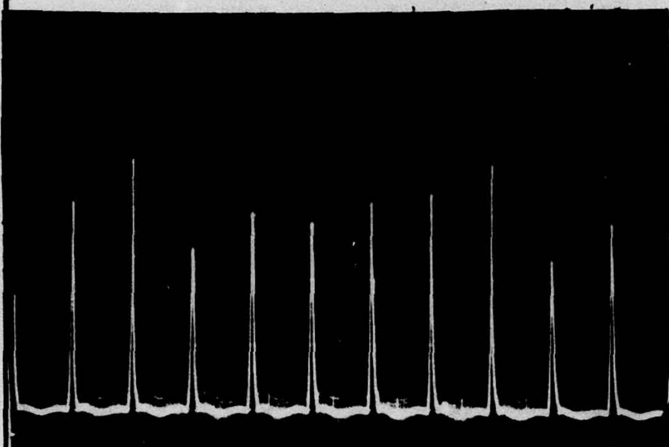
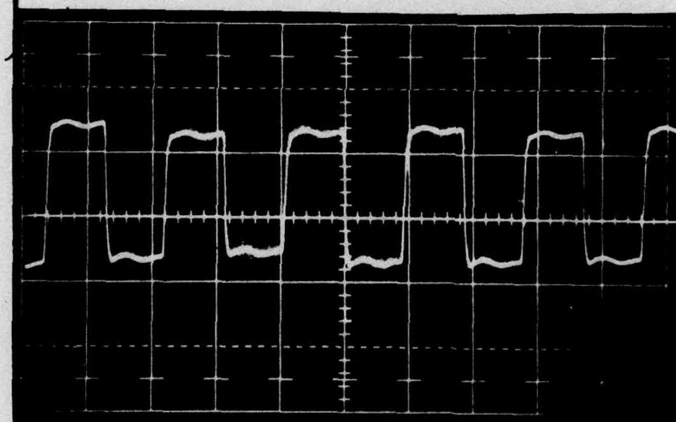
COMMUTATION BOOST CIRCUIT VOLTAGE AND CURRENT WAVEFORMS



I_B

50 A/DIV.

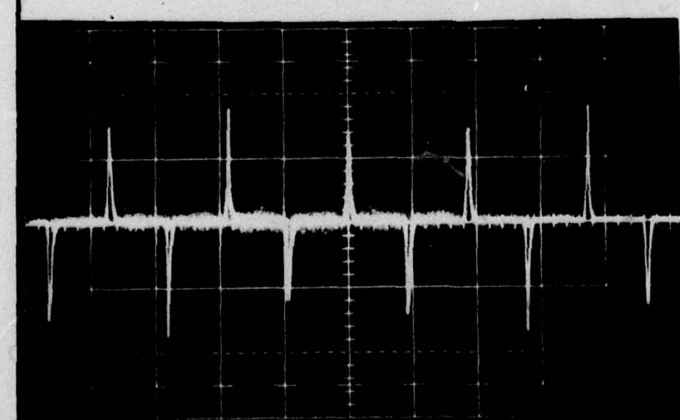
500 μSEC/DIV.



VOLTAGE ACROSS A C_1 CAPACITOR

100V/DIV.

500 μSEC/DIV.



CURRENT INTO PRIMARIES OF TRANSFORMERS T_B

200 A/DIV. 500 μSEC/DIV.

B CURRENTS ↑

A CURRENTS ↓

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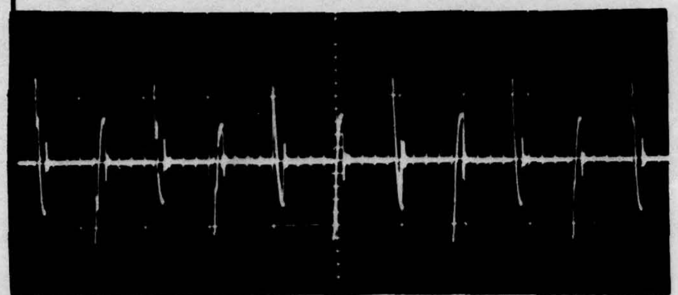
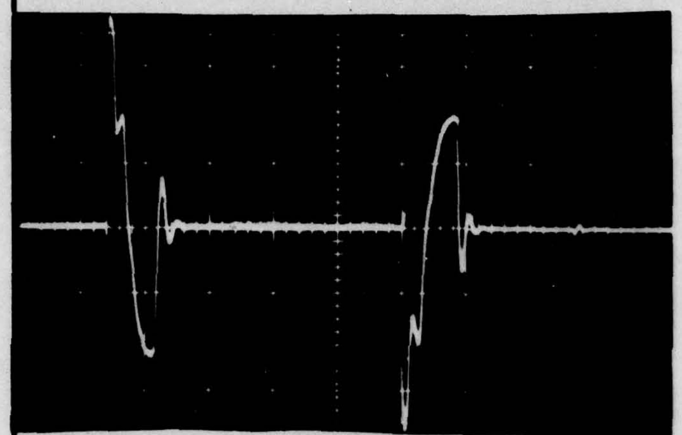
BOOST CIRCUIT WAVEFORMS



VOLTAGE ACROSS L_1

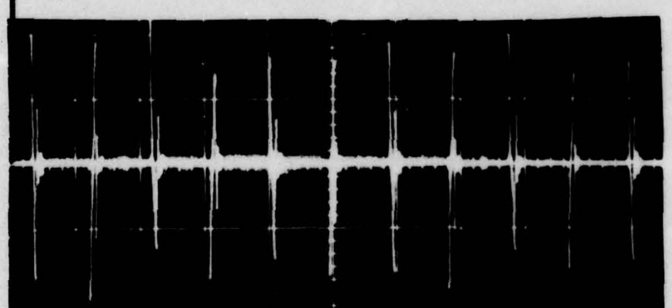
50V / DIV.

500 μSEC / DIV.



20V / DIV.

100 μSEC / DIV.



VOLTAGE ACROSS L_2

50V / DIV.

500 μSEC / DIV.

20 V / DIV.

100 μSEC / DIV.

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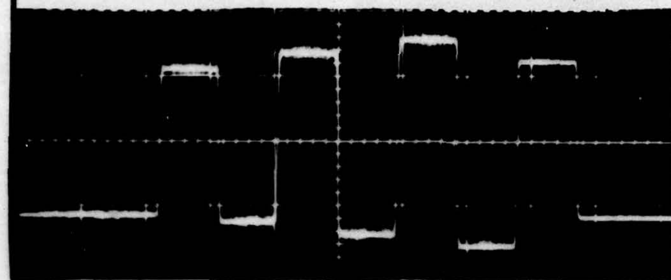
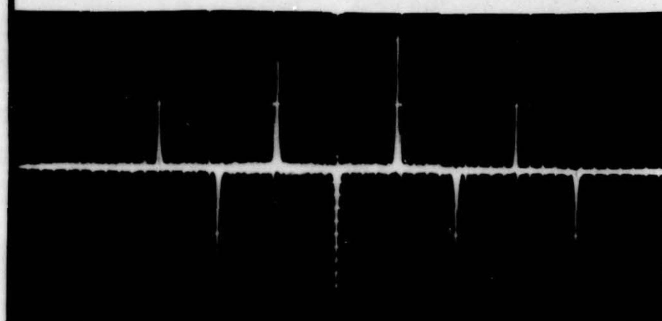
BOOST CIRCUIT WAVEFORMS



VOLTAGE ACROSS C_2

50V/DIV.

500 μSEC/DIV



CURRENT THRU C_2

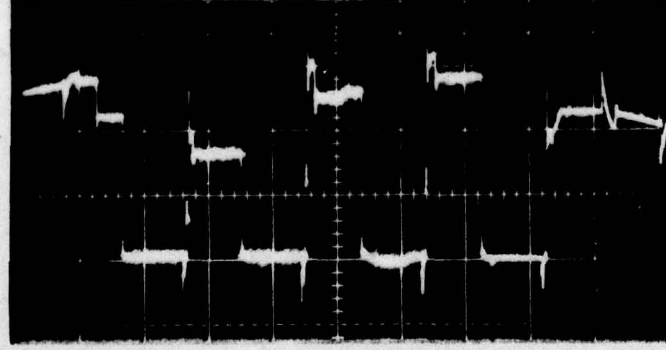
200A/DIV.

500 μSEC/DIV.

CURRENT THRU C_2

50A/DIV

10 μSEC/DIV.



VOLTAGE ACROSS L_{SA}

50V/DIV.

500 μSEC/DIV.

11KW, PF = 0.8

DISTRIBUTION:

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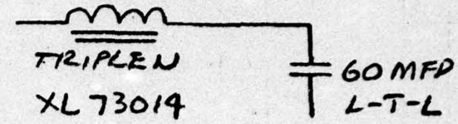
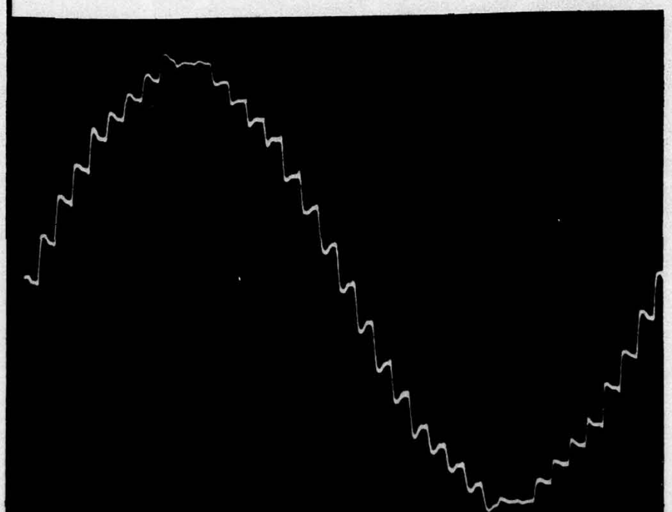
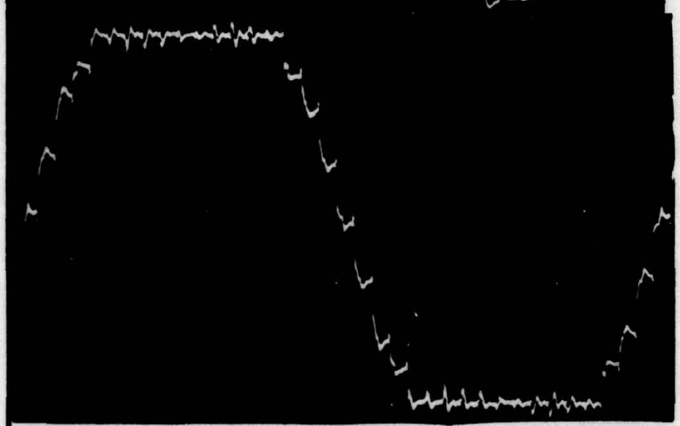
60 HZ OUTPUT FILTER EXPERIMENTS



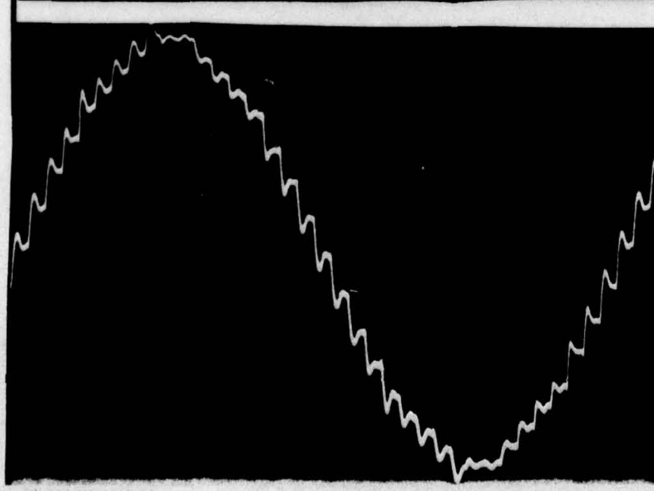
LINE-TO-NEUTRAL VOLTAGE



NO LOAD



NO LOAD

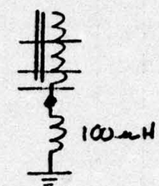


16 KW, PF=0.8

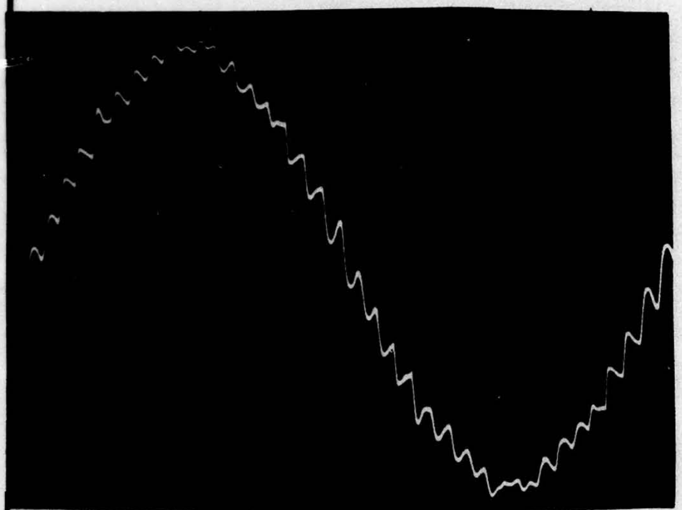
DISTRIBUTION:

60HZ FILTER EXPERIMENTS

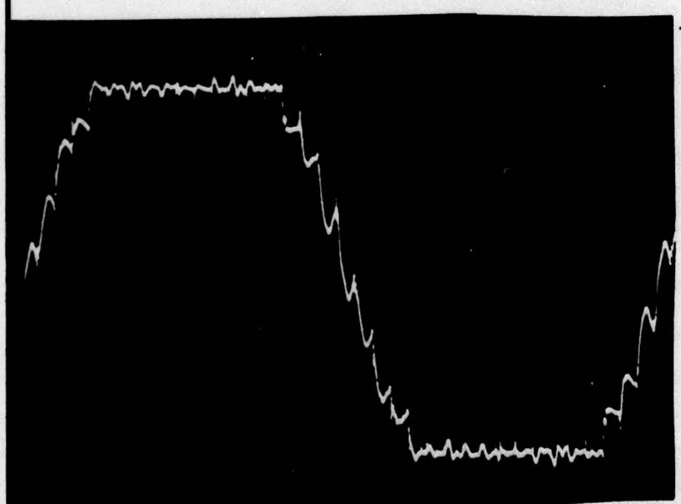
• 100 mH ADDED IN SERIES WITH STEP TRANSFORMER



• OUTPUT FILTER 60 MFD L-T-L
XL 73014 TRIPLEN



L-T-N VOLTAGE
100V/DIV.



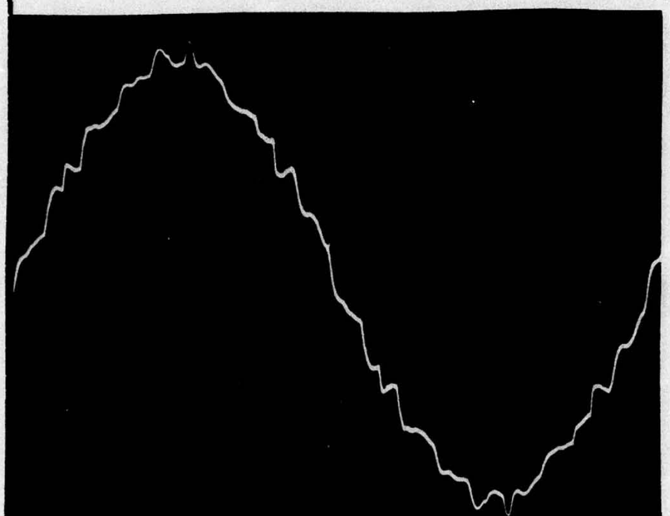
INVERTER BASIC VOLTAGE
100V/DIV.

DISTRIBUTION:

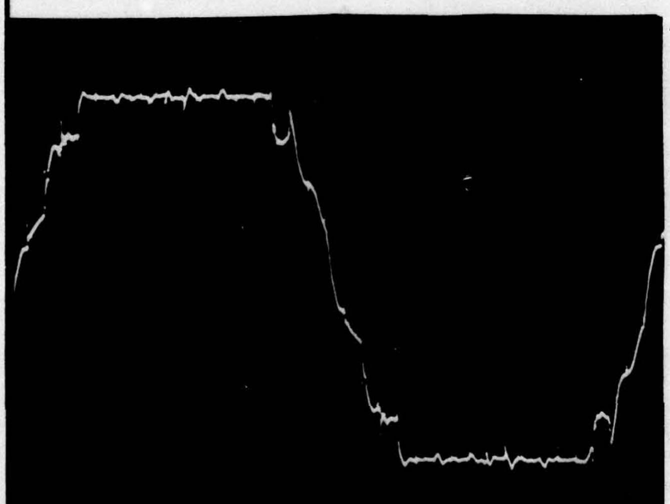
60HZ FILTER EXPERIMENTS

- 1MH ADDED IN SERIES WITH STEP TRANSFORMER

- OUTPUT FILTER 60MFD L-T-L, XL73014 TRIPLEN.



L-T-N VOLTAGE
100V/DIV.



INVERTER BASIC VOLTAGE
100V/DIV.

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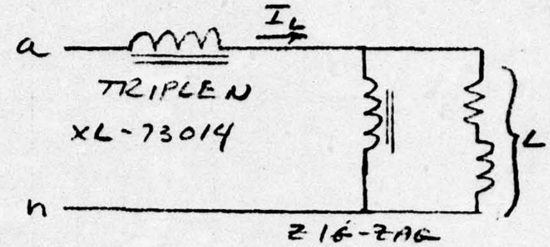
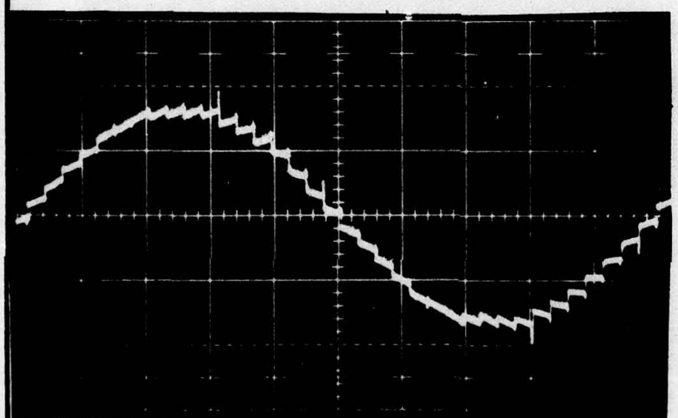
LOAD CURRENT 60HZ, THREE PHASE

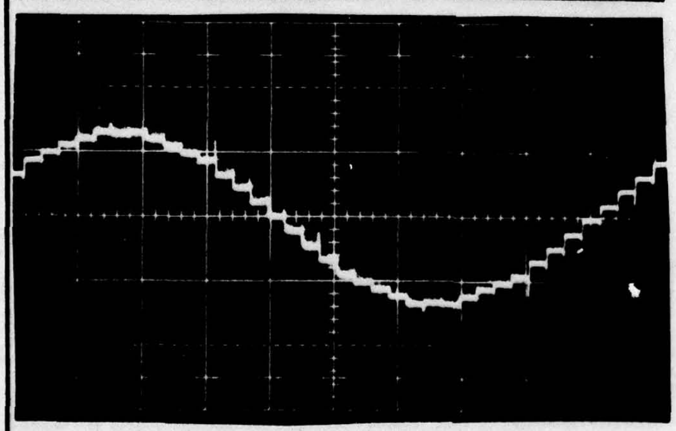




LINE CURRENT

16KW, PF= 0.8 LOAD

50A/DIV.



16KW, PF=1.0 LOAD

50A/DIV.

(NOTE PHASE SHIFT).

DISTRIBUTION:

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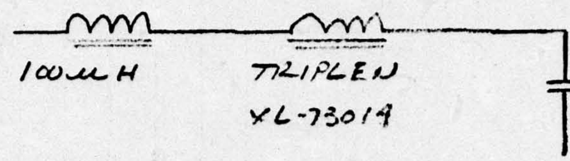
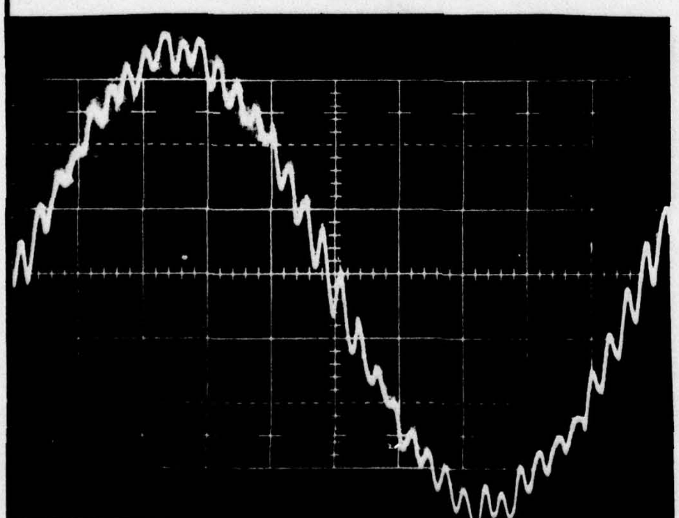
60HZ FILTER EXPERIMENTS



L-T-N VOLTAGE

NO LOAD

THD = 4.6%



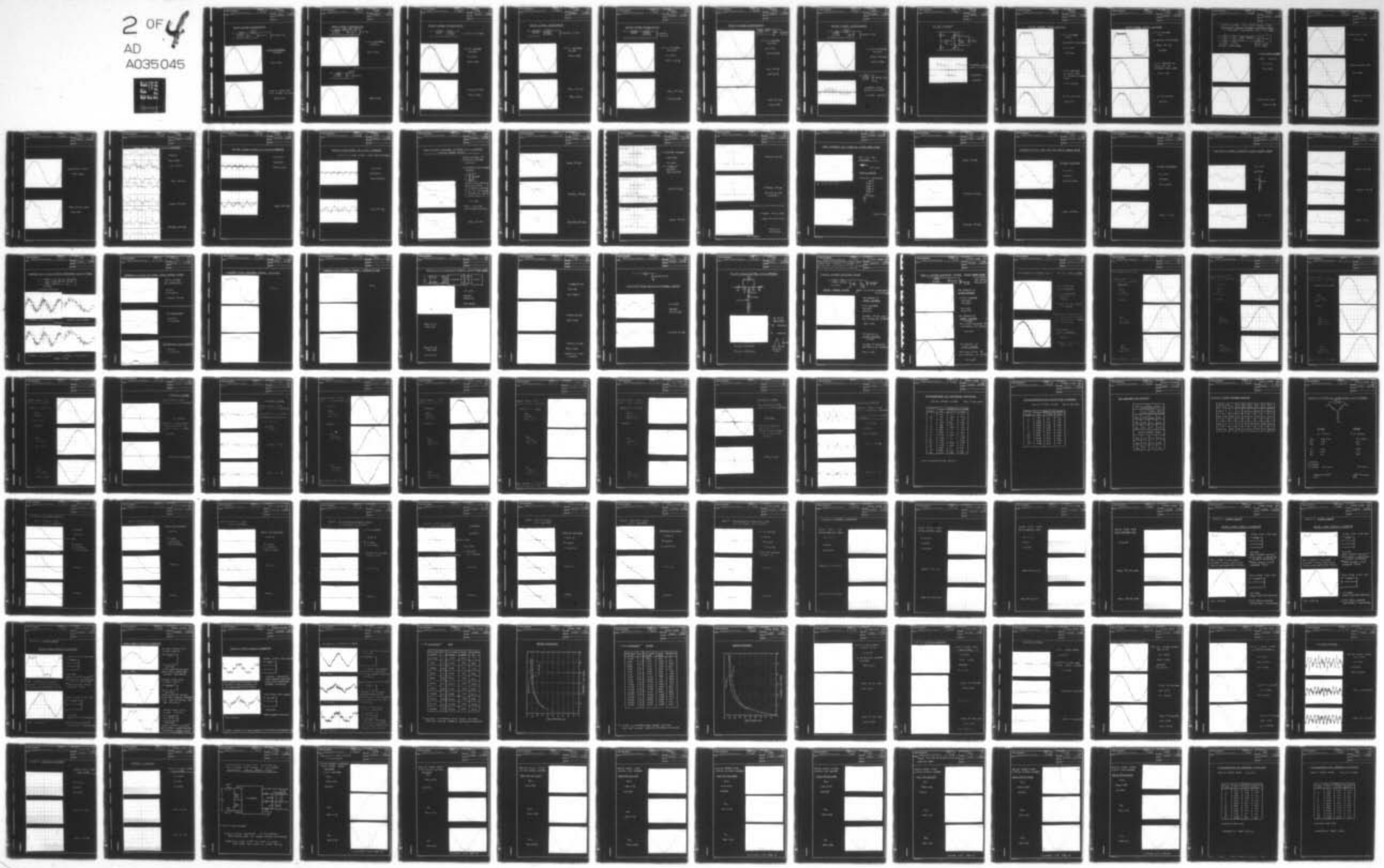
16KW, PF=0.8

THD = 7.68%

DISTRIBUTION:

AD-A035 045 GENERAL MOTORS CORP GOLETA CALIF DELCO ELECTRONICS DIV F/G 9/5
FREQUENCY CONVERTER PORTABLE, ALTERNATING CURRENT MULTIFREQUENC--ETC(U)
JAN 75 T CORRY DAAK02-72-C-0210
UNCLASSIFIED R75-3 NL

2 OF 4
AD
A035045



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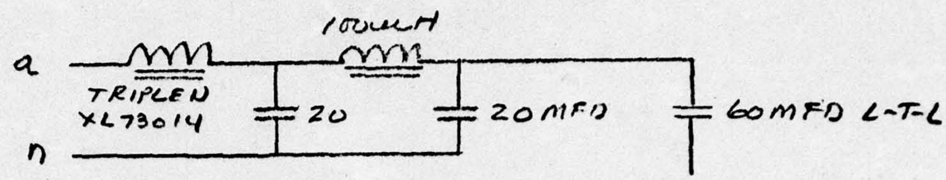
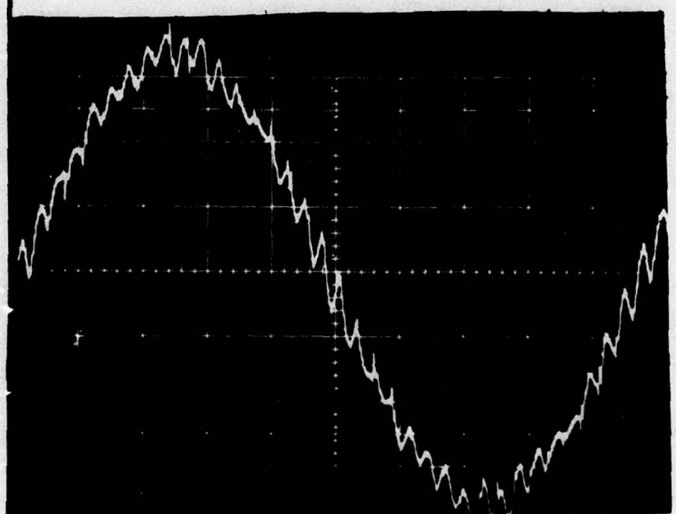
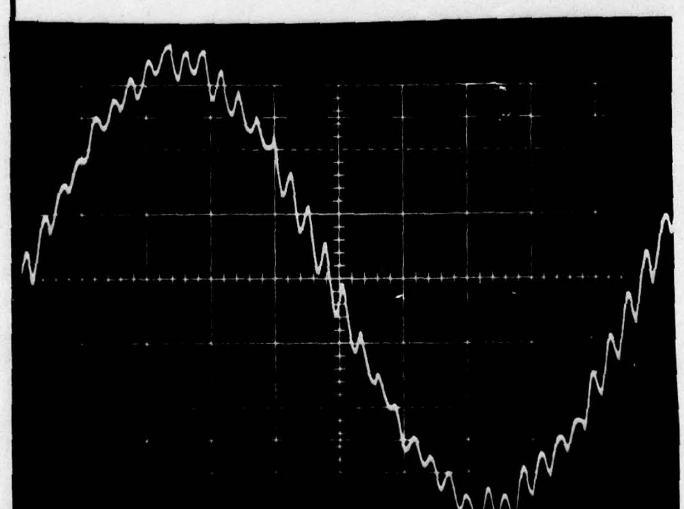
60HZ FILTER EXPERIMENTS





L-T-N VOLTAGE
100V/DIV.

THD = 6.9%



SAME AS ABOVE BUT WITH NEUTRAL REMOVED.

THD = 6.7%

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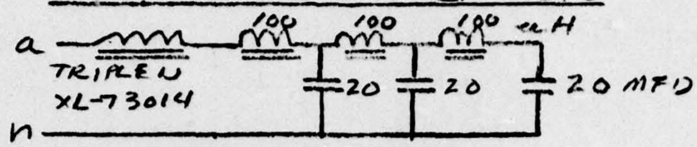
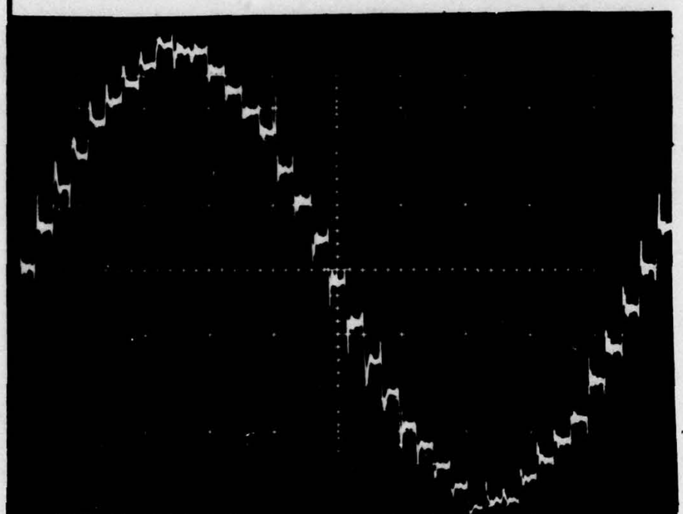
DISTRIBUTION:

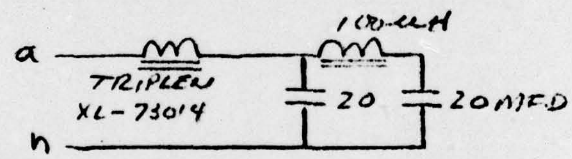
60HZ FILTER EXPERIMENTS

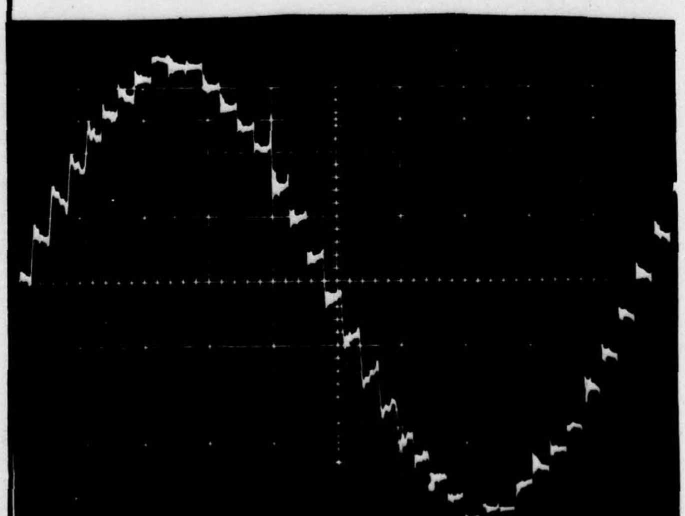




L-T-N VOLTAGE
100V/DIV.

THD= 6.5%





THD= 7.3%

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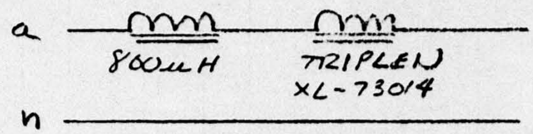
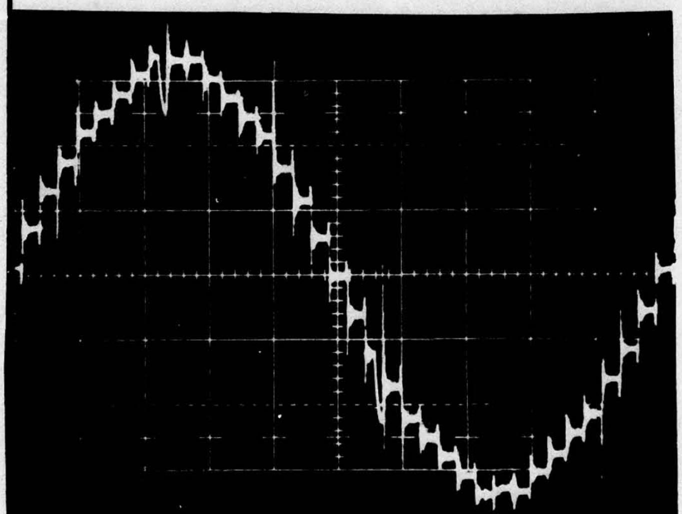
60HZ FILTER EXPERIMENTS



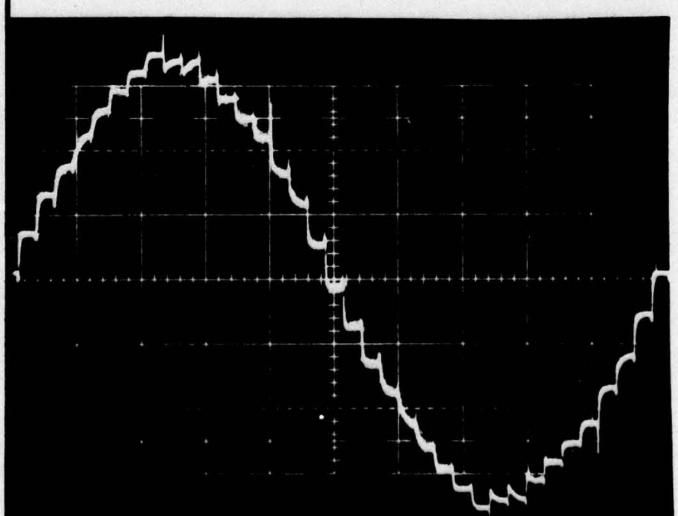
NO OUTPUT CAPACITORS



L-T-N VOLTAGE
100V/DIV.

NO LOAD

THD= 7.6%

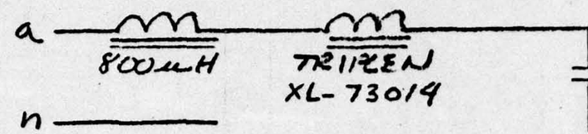


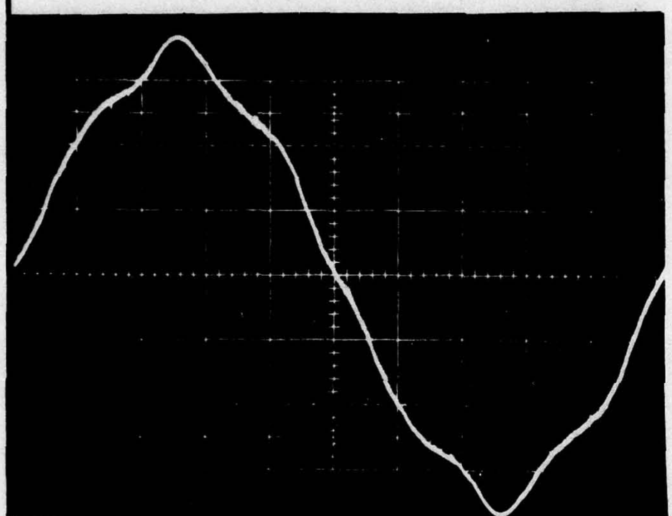
16KW, PF=0.8

THD= 5.8%

DISTRIBUTION:

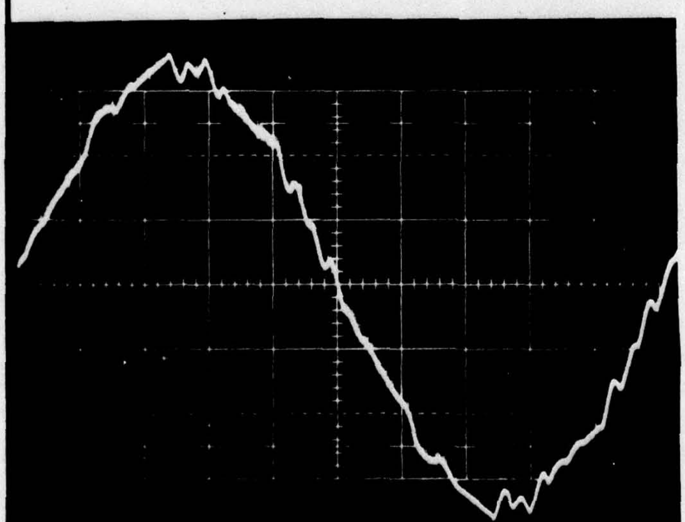
60 HZ FILTER EXPERIMENTS





L-T-N VOLTAGE
100V/DIV.

THD = 5.3%



11KW, PF = 0.8

THD = 4.7%

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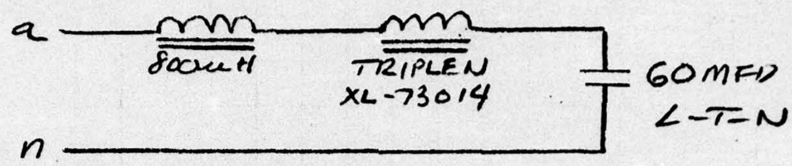
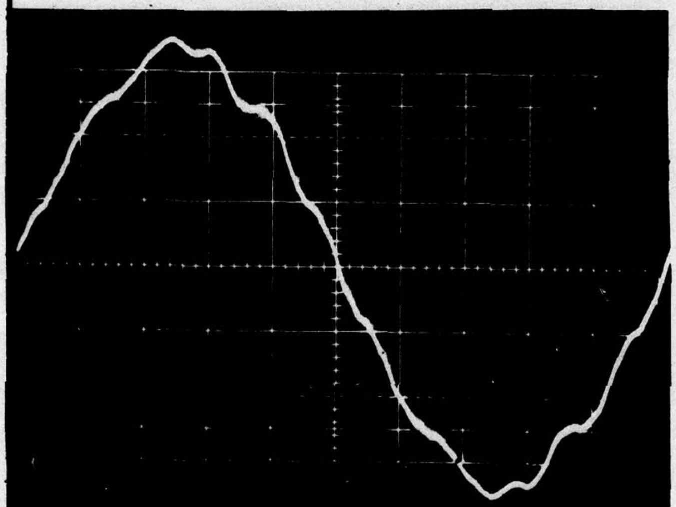
60 HZ. FILTER EXPERIMENTS

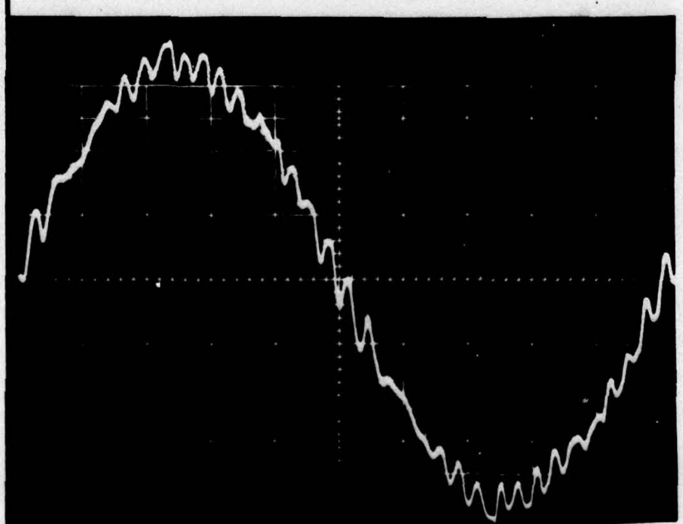




L-T-N VOLTAGE
100V/DIV.

NO LOAD

THD= 4.3%



11KW, PF= 0.8

THD= 6.7%

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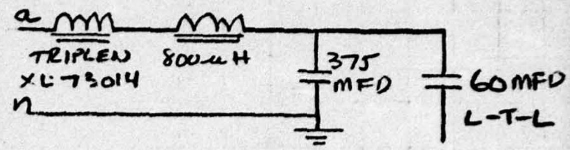
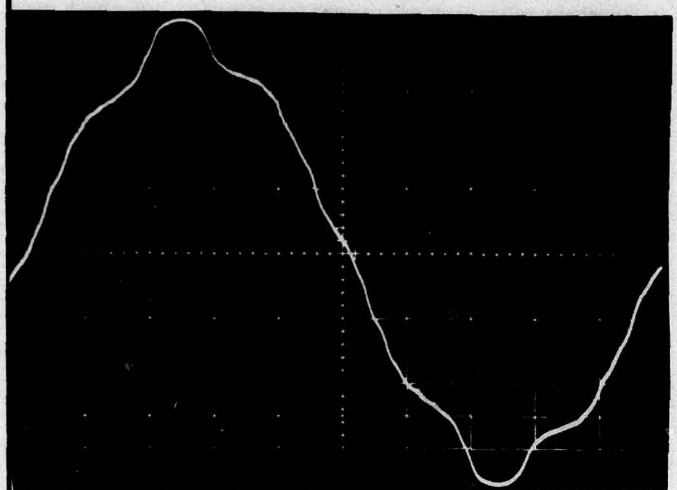
APPROVED	

60 HZ FILTER EXPERIMENTS

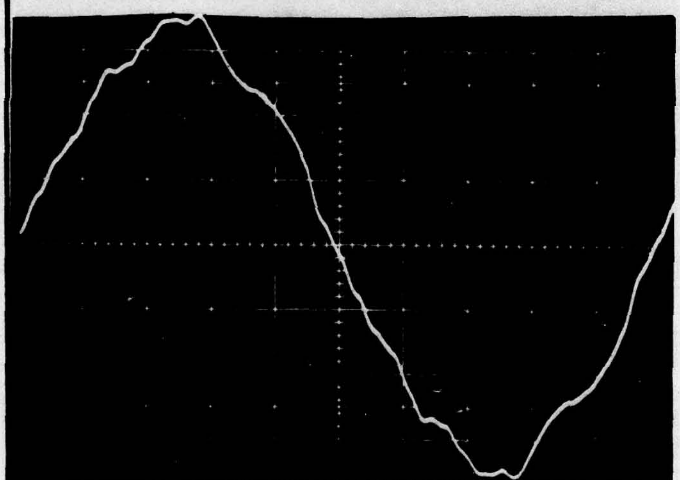




L-T-N VOLTAGE
100V/DIV.

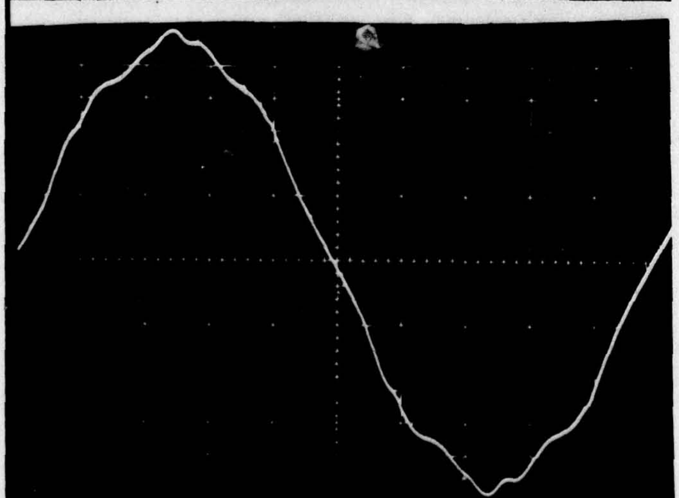
NO LOAD

THD= 6.6%



11KW, PF=1.0

THD= 5.5%

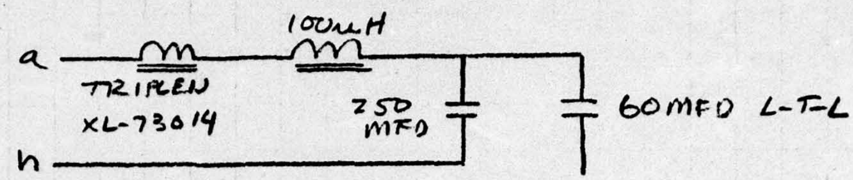


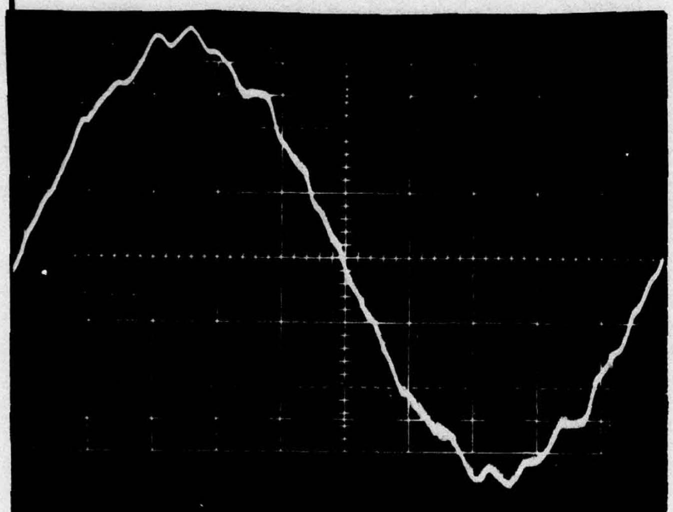
11KW, PF=0.8

THD= 3.9%

DISTRIBUTION:

60 HZ FILTER EXPERIMENTS.

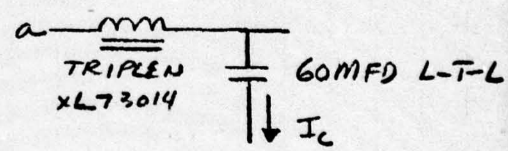


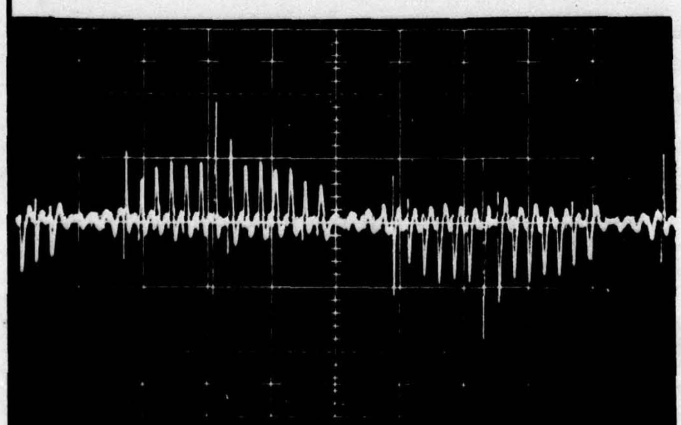


L-T-N VOLTAGE
100V/DIV

6KW, PF=0.8

THD= 3.8%





CURRENT THRU
60 MFD CAPACITOR

10A/DIV. 2ms/DIV.

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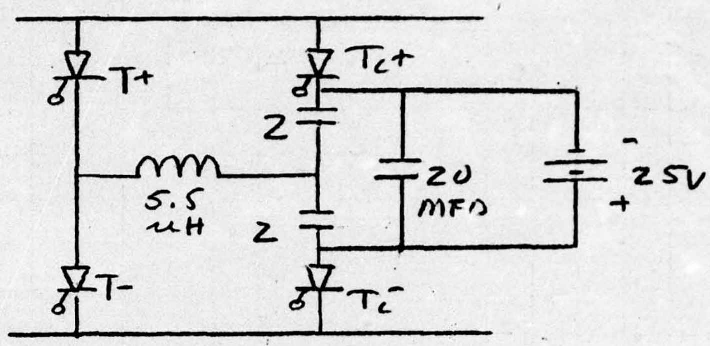
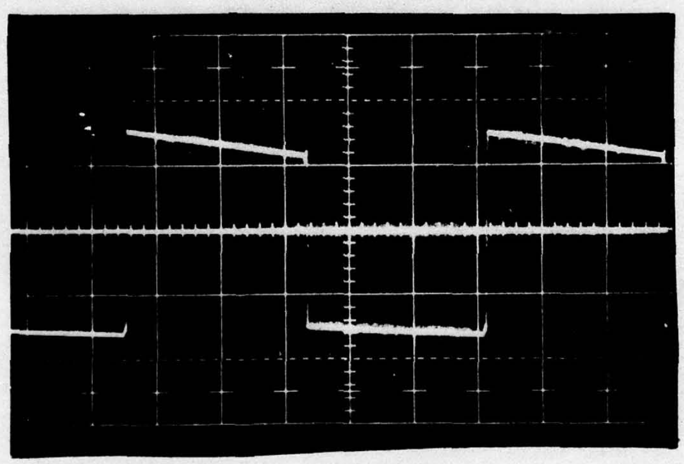
T_c^+, T_c^- CIRCUIT





VOLTAGE ACROSS
2 MFD. CAPACITOR

100V/DIV.

1MS/DIV.

DISTRIBUTION:

DE-255 REV. 12-66

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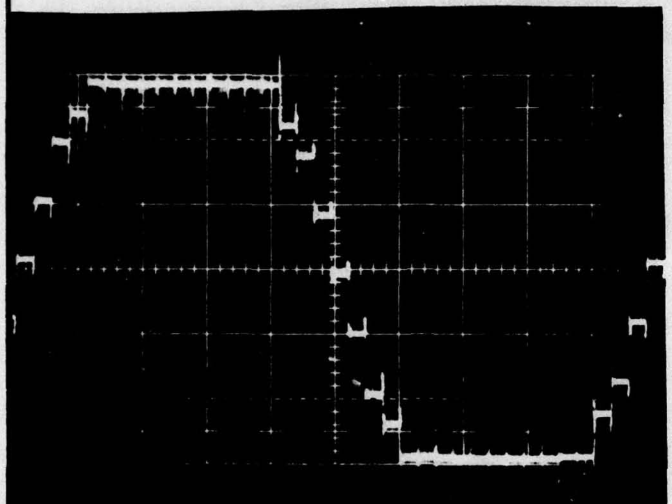
60HZ THREE PHASE VOLTAGES

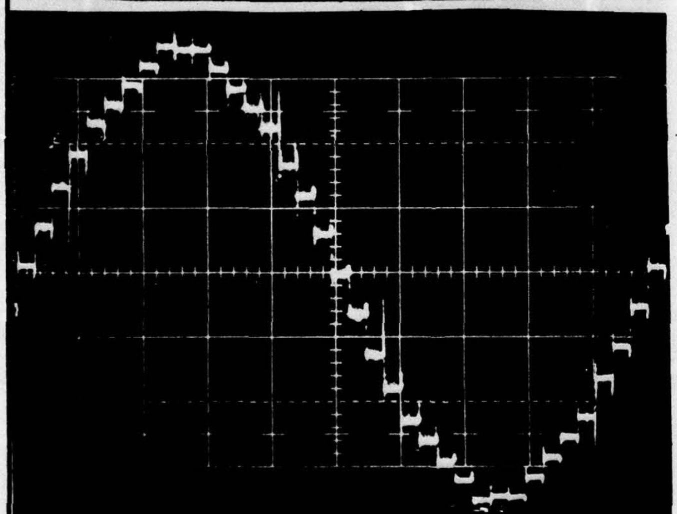


L-T-N VOLTAGE
Va-n

NO OUTPUT CAPACITANCE

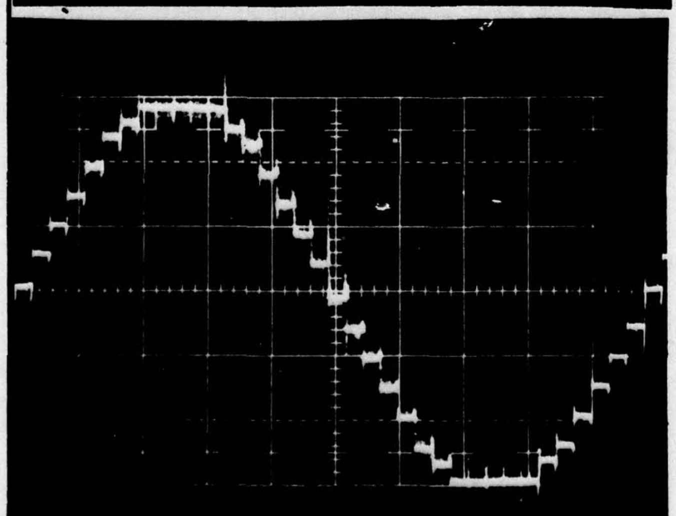
NO LOAD

50V/DIV.



L-T-N VOLTAGE
ON LOAD SIDE
OF TRIPLEN ATTENUATOR

THD = 5.65%



L-T-L VOLTAGE

100V/DIV

DISTRIBUTION:

DE 255 REV. 12-66

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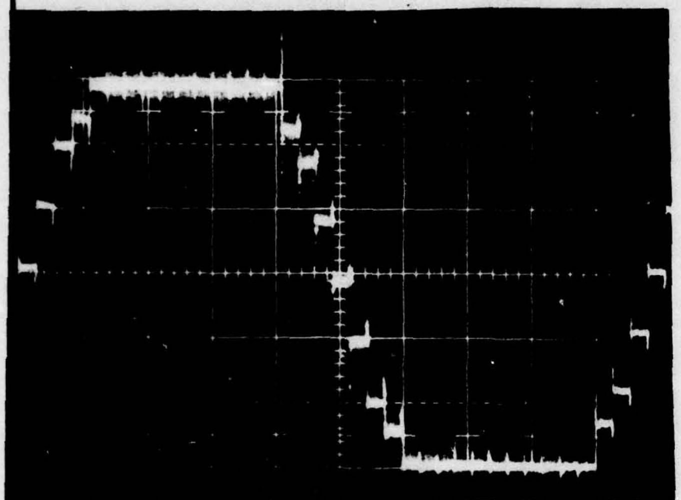
60 HZ THREE PHASE VOLTAGES

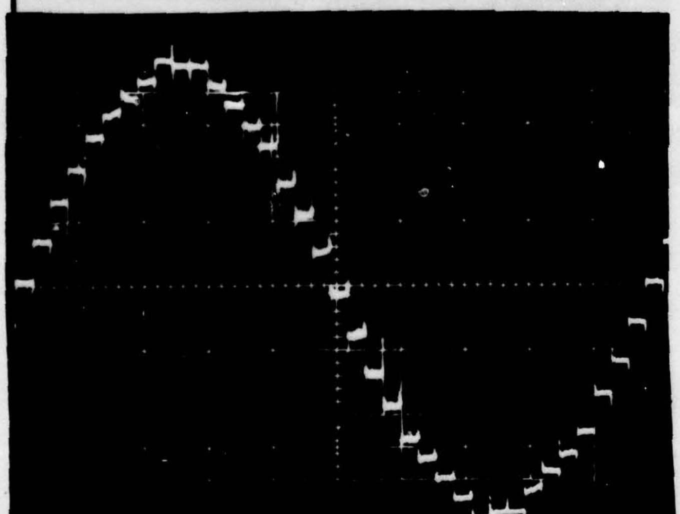


L-T-N VOLTAGE
V_{a-n}

NO OUTPUT CAPACITANCE

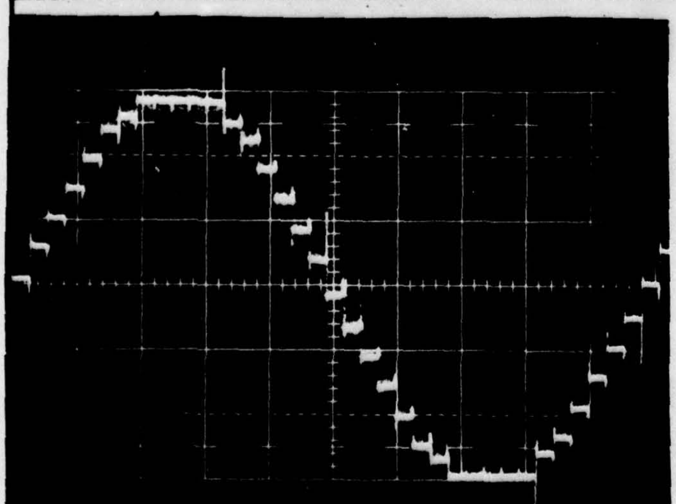
16KW, PF = 0.8

50V/DIV.



L-T-N VOLTAGE ON
LOAD SIDE OF
TRIPLEN ATTENUATOR

THD = 7%

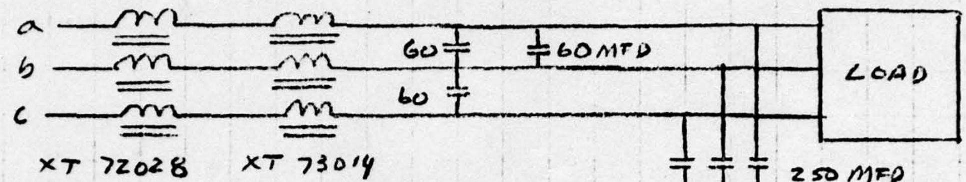


L-T-L VOLTAGE

100V/DIV.

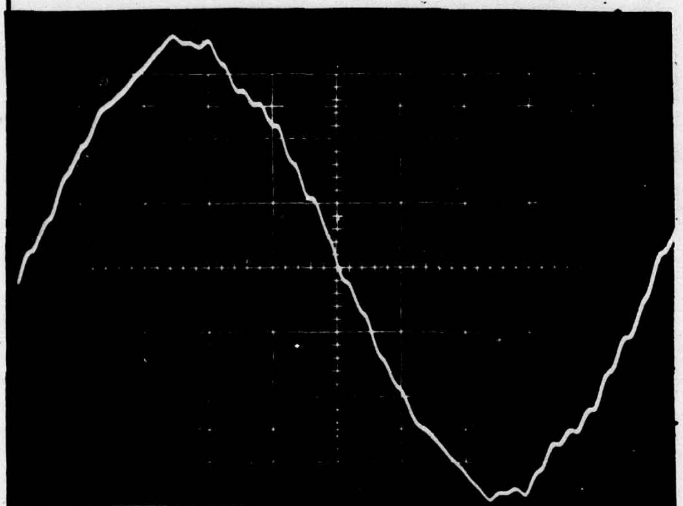
DISTRIBUTION:

OUTPUT VOLTAGES FOR 60HZ, THREE PHASE
OPERATION, POWER FACTOR CORRECTED MODE.
(AUXILIARY COMMUTATION STEPS NOT USED)



TRIPLEN ATTENUATORS

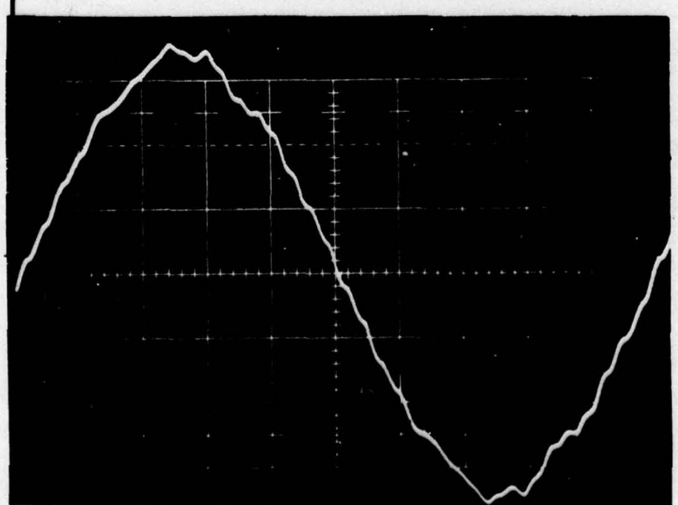
L-T-N OUTPUT VOLTAGES



Van 120Vrms

NO LOAD

THD = 3.5%



2.2KW, 0.8 PF LOAD

THD = 3.14%

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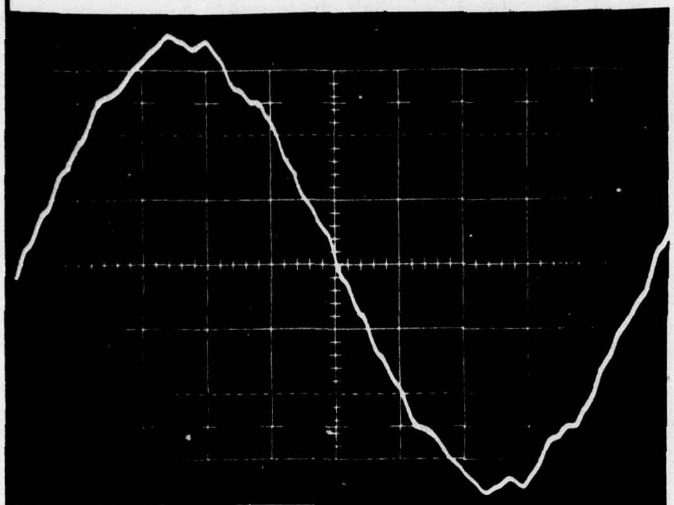
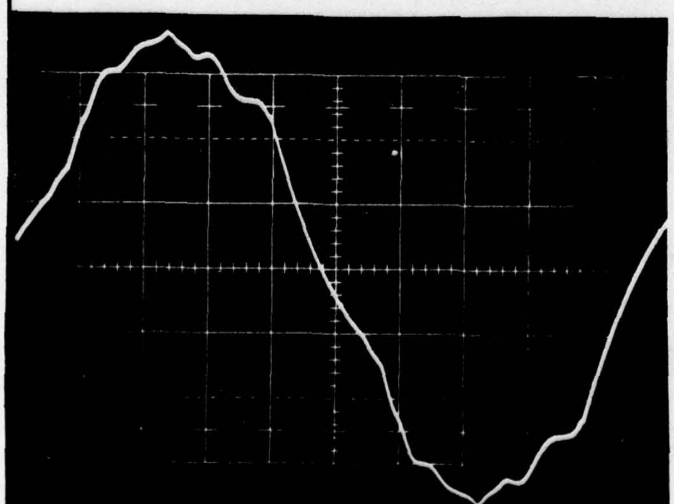


4.4KW, 0.8 PF LOAD

THD = 3.2%

6.6KW, 0.8 PF LOAD

THD = 3.8%



8.8KW, 0.8 PF LOAD

THD = 7%

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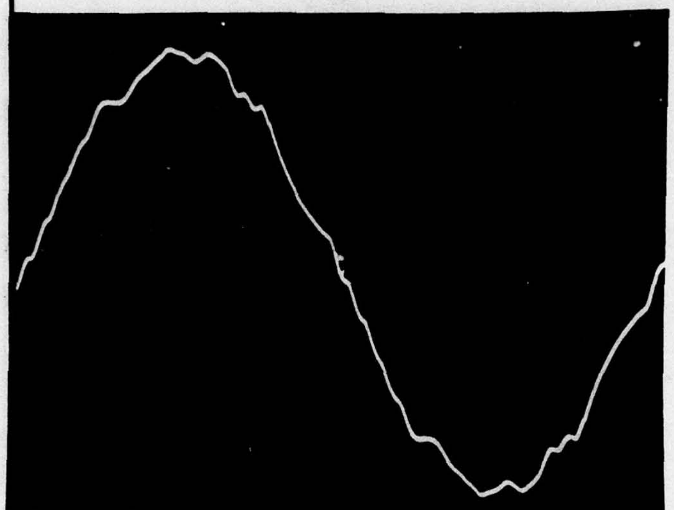
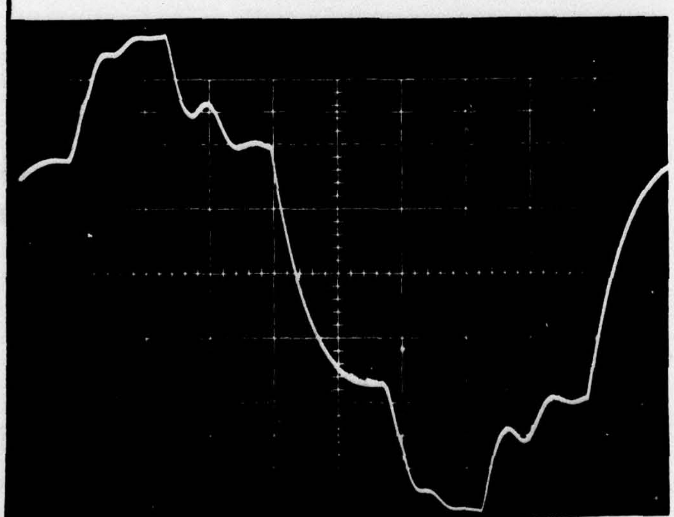


16KW, PF=1.0 LOAD

THD= 4.3%



16KW, PF=0.8 LOAD

THD= 17%

DISTRIBUTION:

DE-255 REV. 12-66

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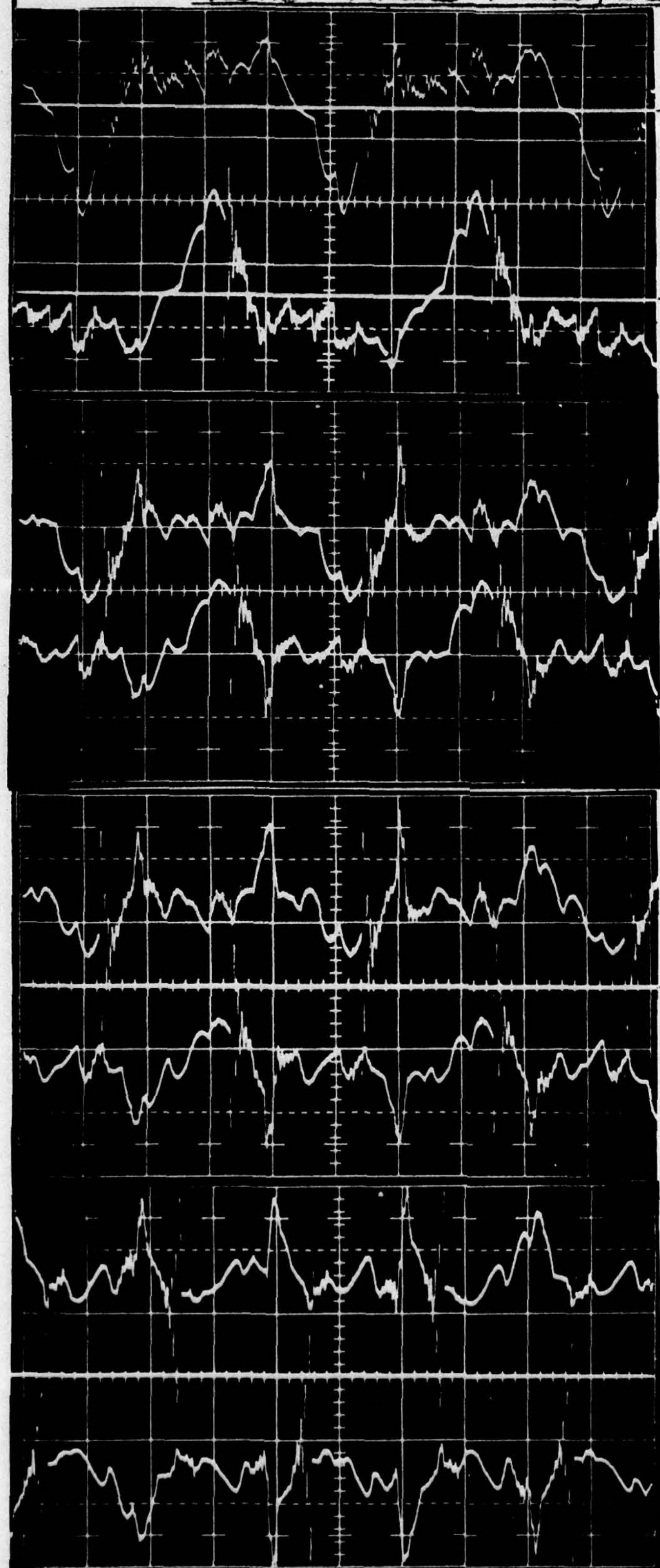
400 HZ THREE PHASE, DC INPUT CURRENTS



50A/DIV.

200 µS/DIV.

NO LOAD

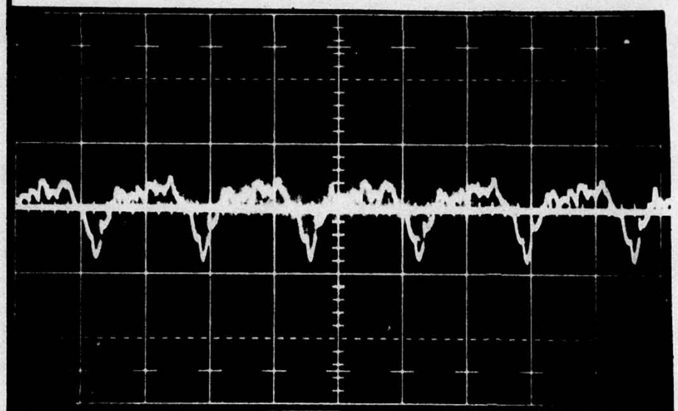
11KW, PF=0.8

16KW, PF=0.8

20.6KW, PF=0.8

DISTRIBUTION:

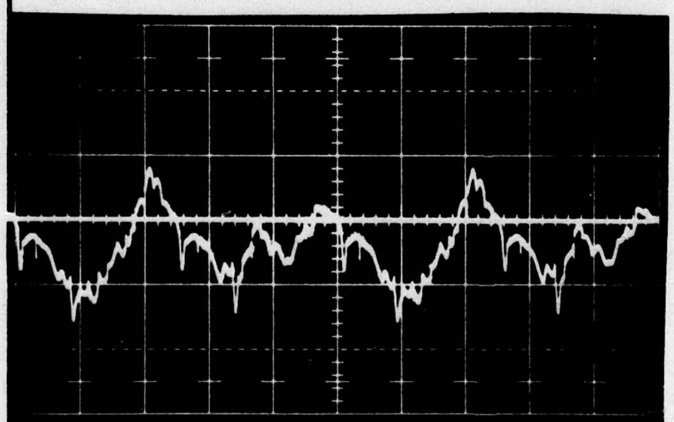
<u>400HZ SINGLE PHASE, DC INPUT CURRENTS</u>



NO LOAD

100A/DIV.

500µsec/DIV.



11KW, PF=0.8

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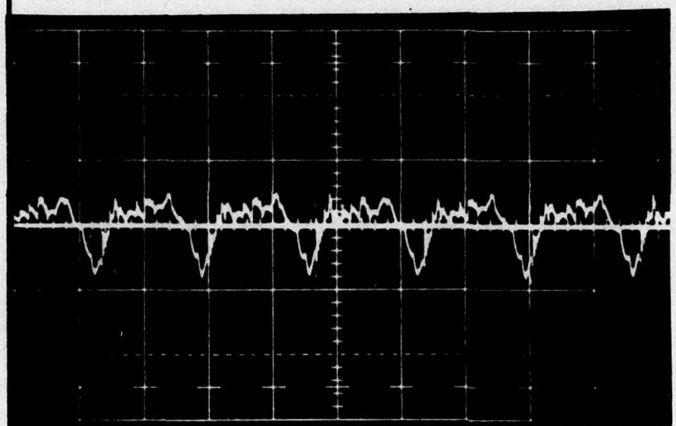
APPROVED

400HZ SINGLE PHASE, DC INPUT CURRENTS

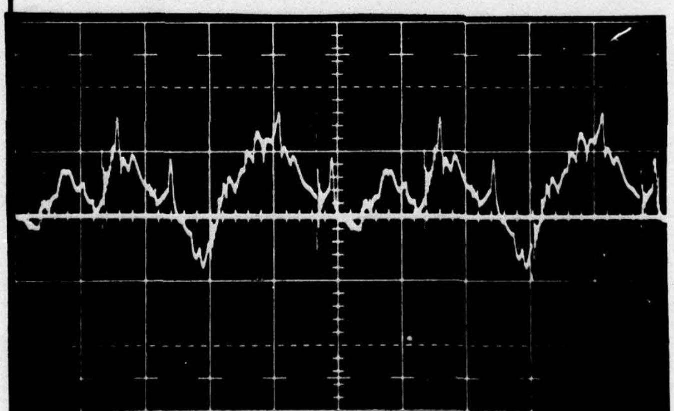
(1 MFD CAPACITOR ACROSS STEP-TRANSFORMER)



NO LOAD

100 A/DIV.

500 μSEC/DIV.



11 KW, PF-0.8

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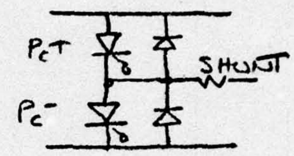
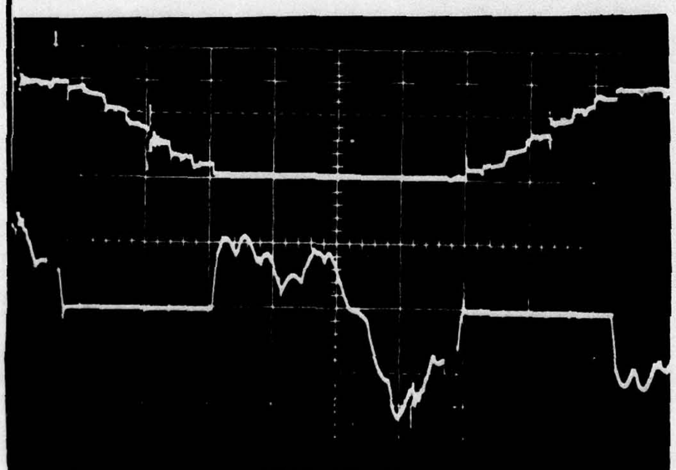
POWER CENTER THYRISTOR VOLTAGES AND CURRENTS.
400HZ, THREE PHASE

POWER CENTER P_C^-
THYRISTOR VOLTAGE
200V/DIV.

THYRISTOR & DIODE CURRENT
50A/DIV.



(BOOST COMMUTATION VOLTAGE = 72VDC
CURRENT = 6AMPS DC
FOR ALL V&I PICTURES
JAPANESE C.T. COMMUTATION XFMR IN.)



NO LOAD

(NOTE: BY PASS DIODE PEAK CURRENT = 210 AMPS)

11KW, PF=0.8

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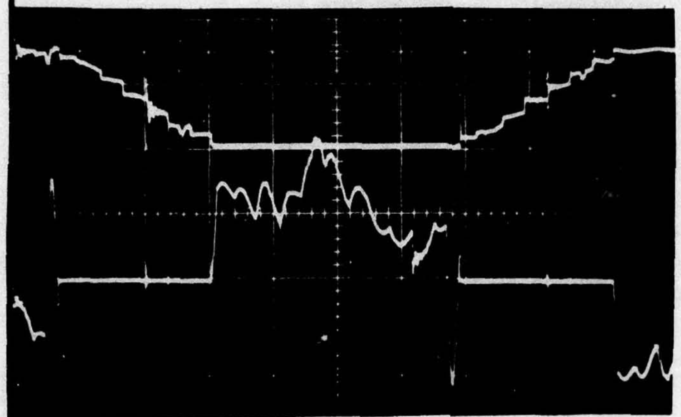
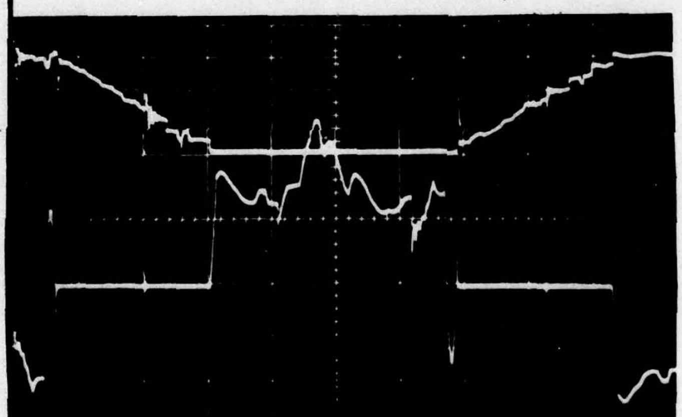
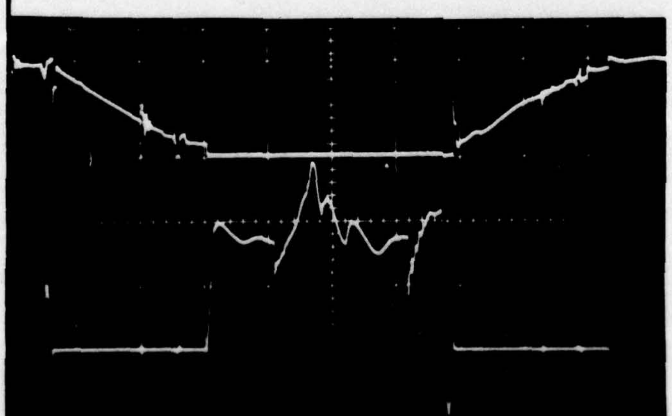


16KW, PF=0.8



20.6KW, PF=0.8



24.8 KW, PF=0.8

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APPROVED

T- THYRISTOR VOLTAGE

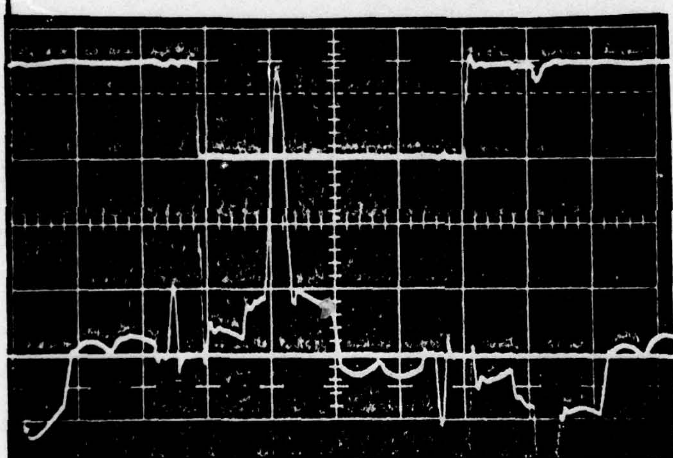
200V/DIV.

NO LOAD

T- CURRENT

50A/DIV.

100μSEC/DIV.



11KW, PF=0.8

16KW, PF=0.8

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20.6 KW, PF= 0.8

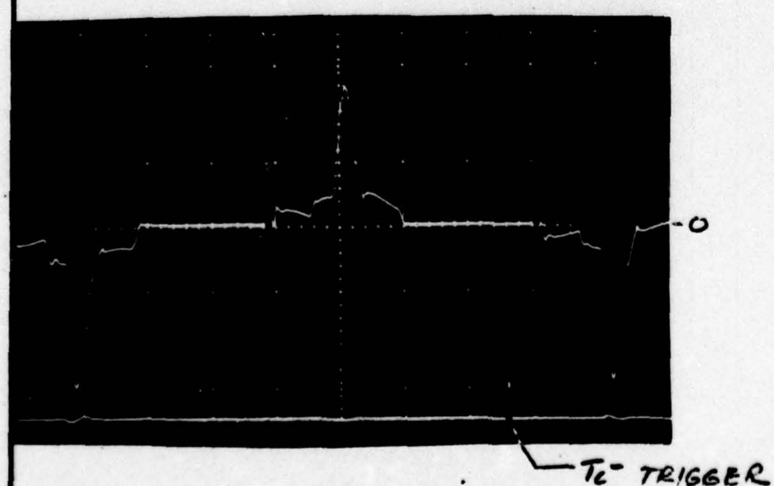
24.8 KW, PF=0.8

(92 AMPS DC INTO INVERTER)

SINGLE PHASE LOAD

5KW, PF= 0.8 L-T-N

100A/DIV.
100µSEC/DIV.



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TITLE

PREPARED CORRY DATE 11/20/79
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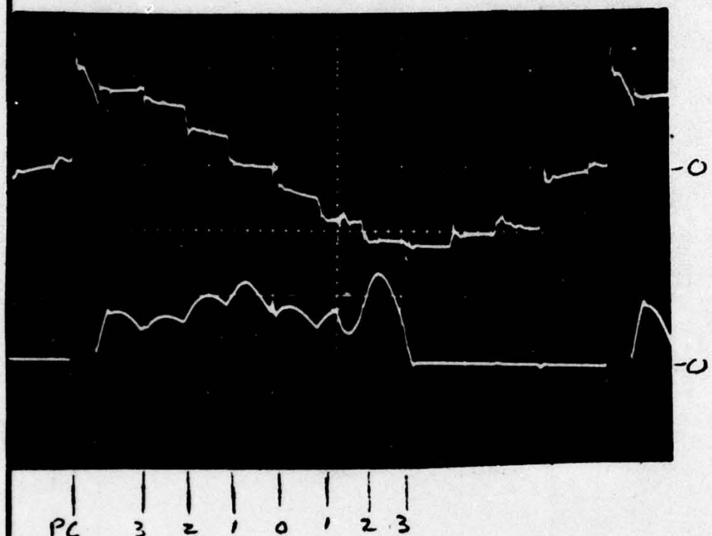
APPROVED

STEP VOLTAGES AND CURRENTS - 400HZ, THREE PHASE



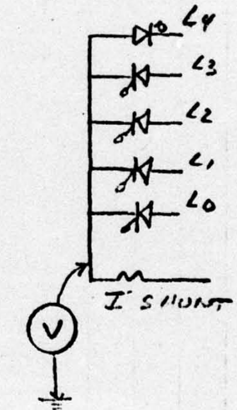
LEFT SIDE STEP VOLTAGE

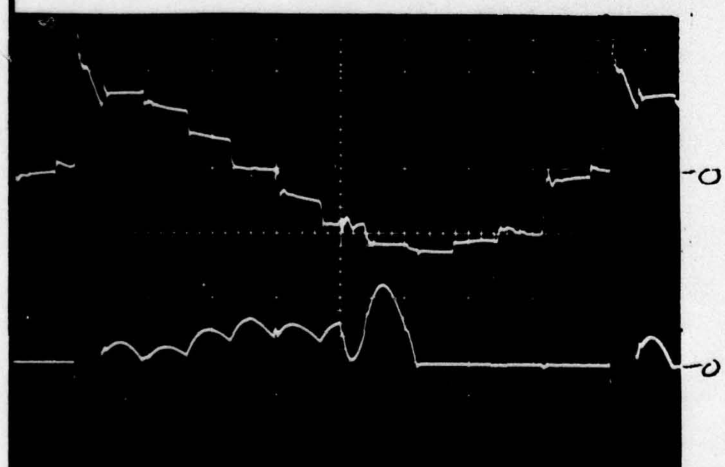
1[redacted]/DIV.

NO LOAD

STEP CURRENT

100A/DIV. 100μSEC/DIV.





11KW, PF=0.8

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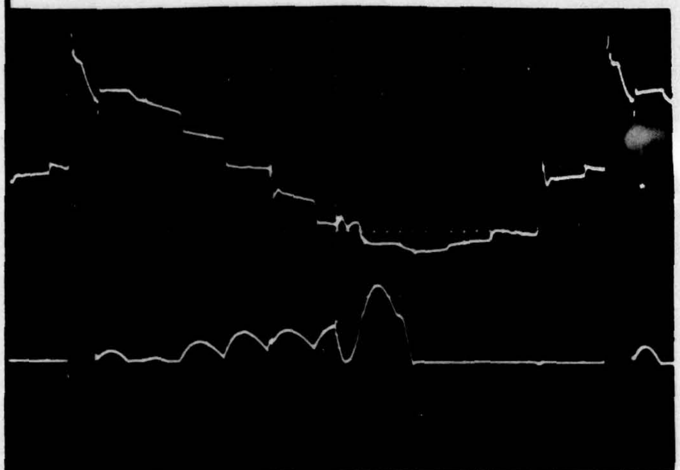
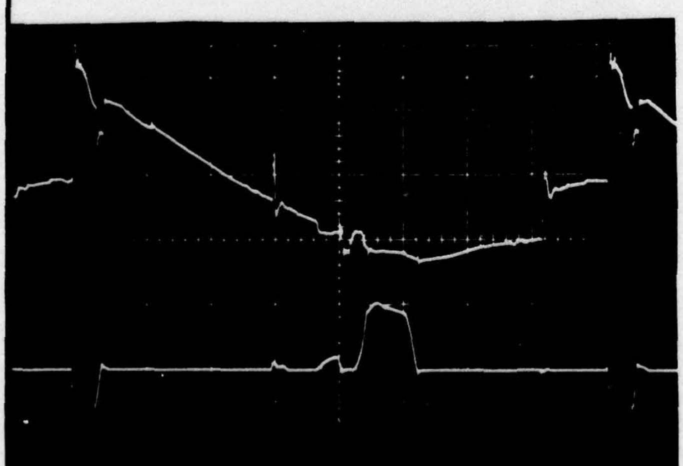
	APPROVED	



16KW, PF=0.8

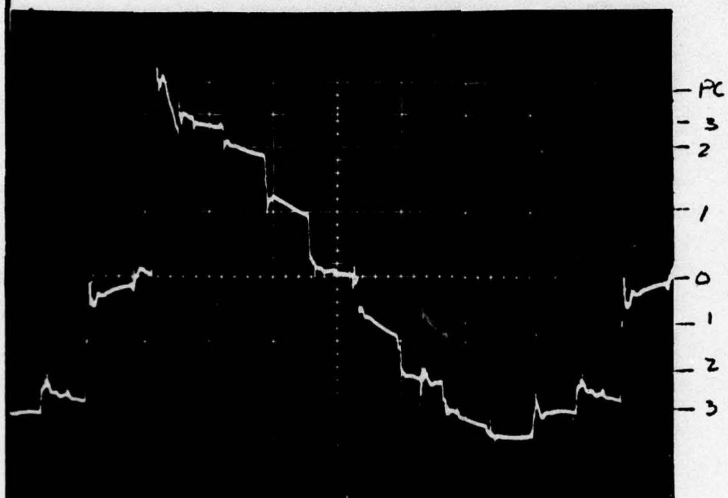
20.6KW, PF=0.8



24.8KW, PF=0.8

DISTRIBUTION:

AUTOTRANSFORMER STEP VOLTAGES 400HZ, THREE PHASE

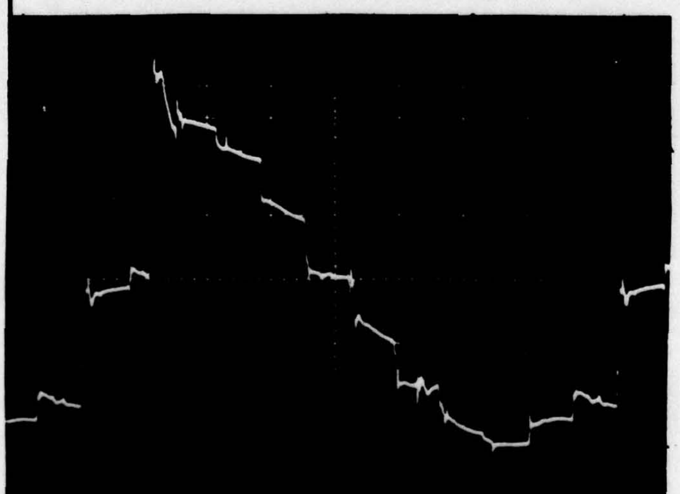


Y STEP FUNCTION

NO LOAD

50V/DIV.

100µSEC /DIV.



11KW, PF= 0.8

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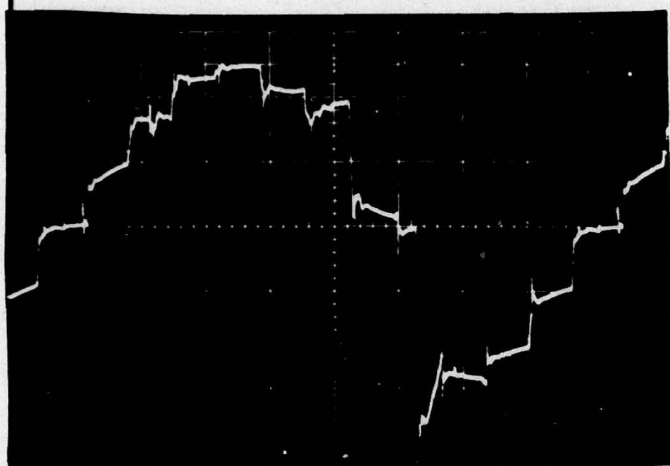


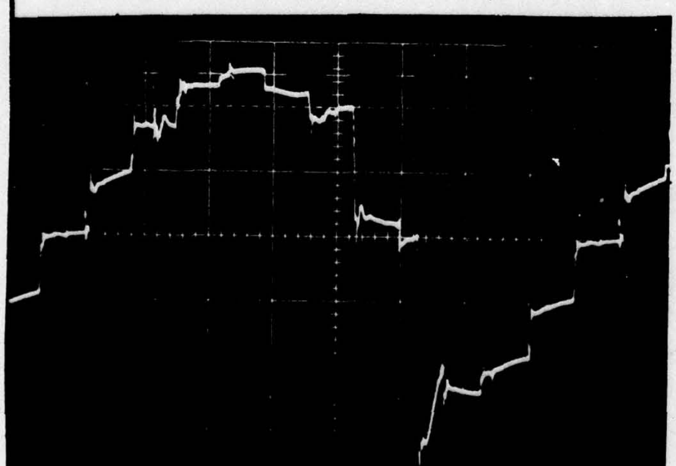
— 3
— 2
— 1
—0
— 1
— 2
— 3

X STEP FUNCTION

NO LOAD

50V/DIV.

100μSEC/DIV.



11KW, PF=0.8

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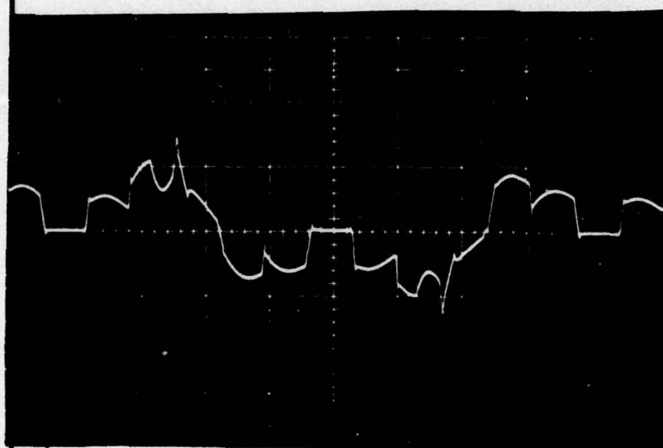
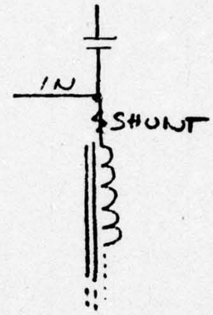
STEP TRANSFORMER CURRENT 400Hz, THREE PHASE

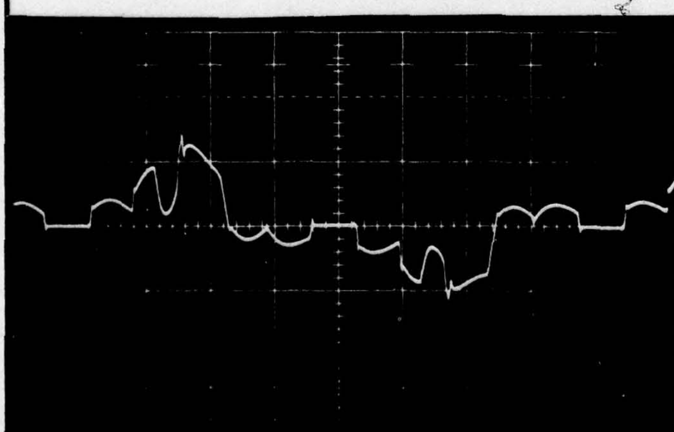


-0

NO LOAD

50A/DIV.





-0

11KW, PF=0.8

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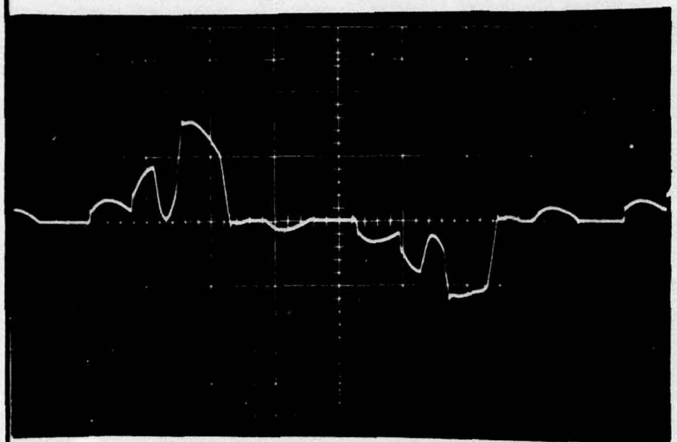
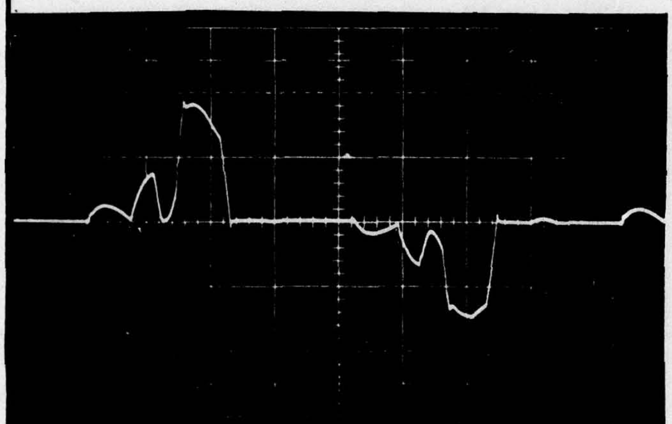
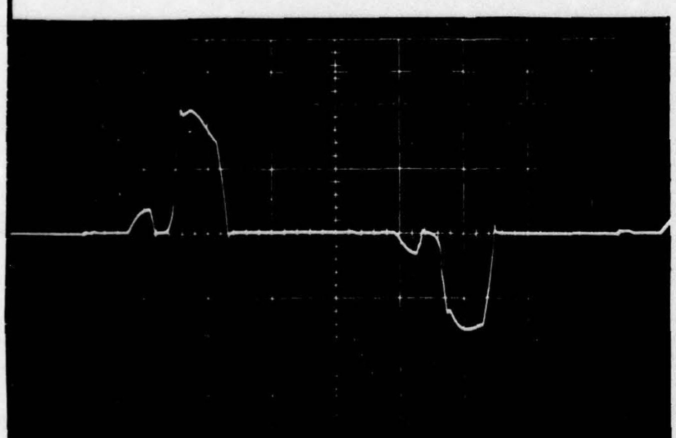


16KW, PF=0.8



20.6KW, PF=0.8



24.8, PF=0.8

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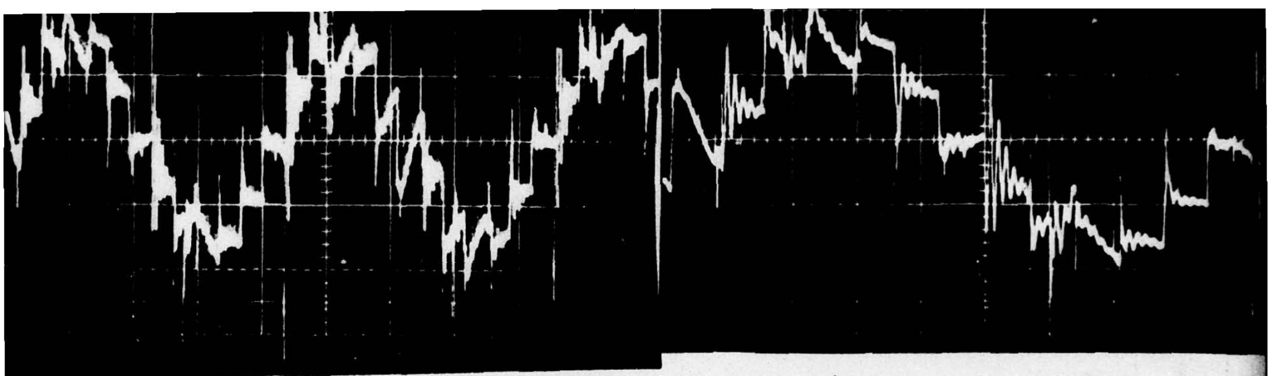

20V/DIV. 2.00 μSEC/DIV. 20V/DIV. 100 μSEC/DIV.

NO LOAD

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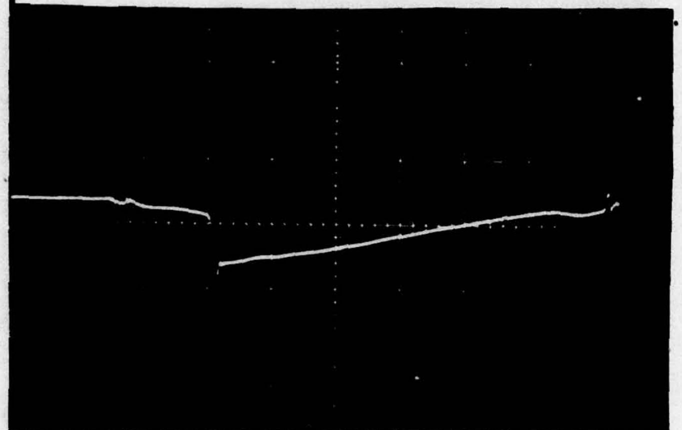
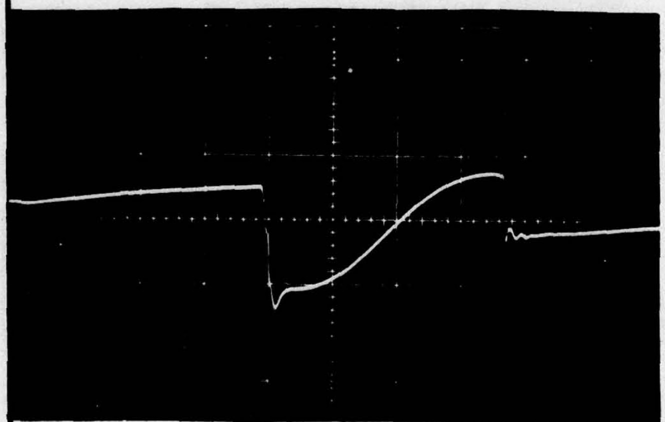
REVERSE BIAS TURN-OFF TIMES 400HZ, THREE PHASE



POWER CENTER
P_C^- TURN-OFF

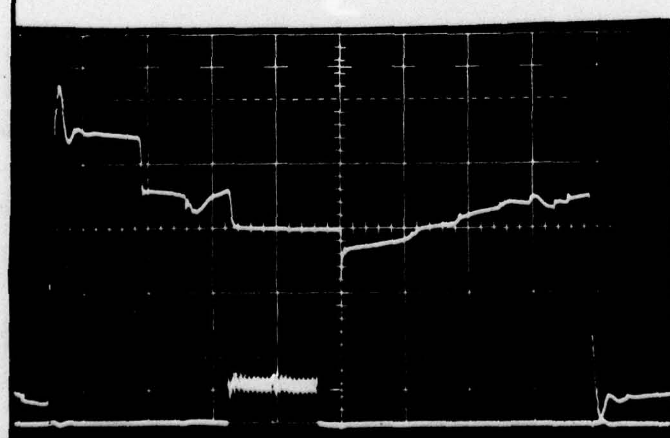
5V/DIV.
5 μSEC/DIV.

20.6KW, PF=0.8



T- TURN-OFF

20V/DIV.
5 μSEC/DIV.



-0

-0 R_3 GATE

R_3 TURN-OFF AS R_2 TURNS-ON

50V/DIV.
50 μSEC/DIV.

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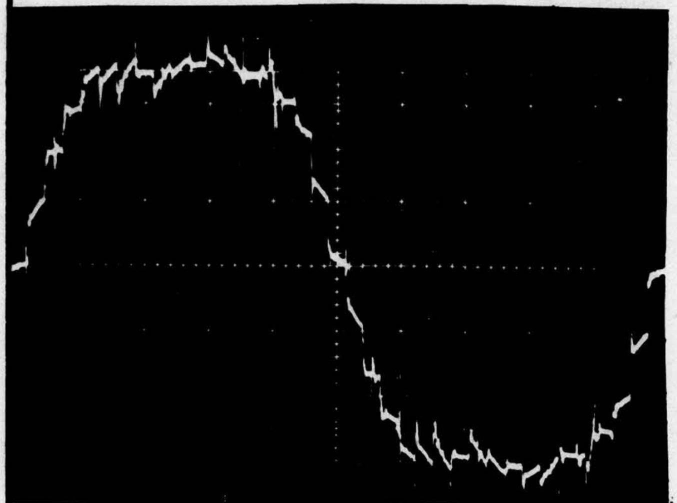
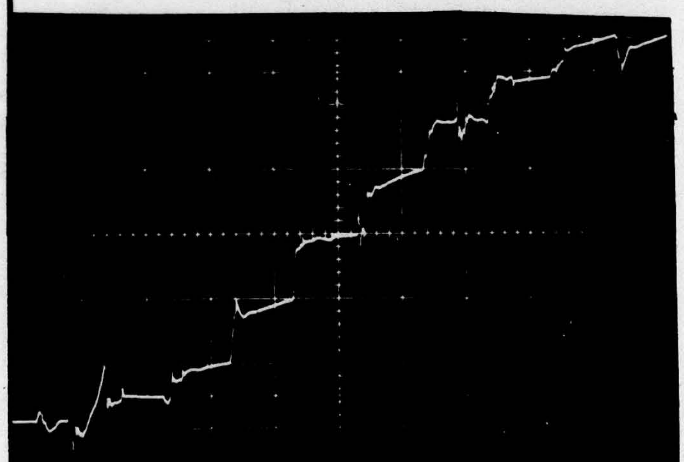
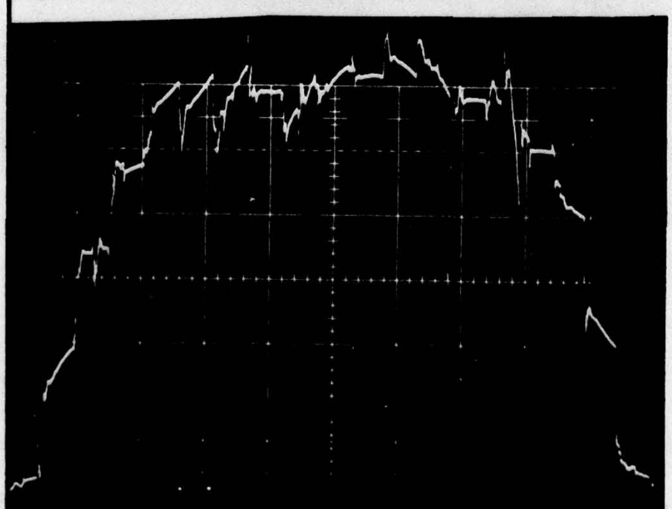
INVERTER BASIC VOLTAGES 400HZ NO LOAD



V_{c-n}





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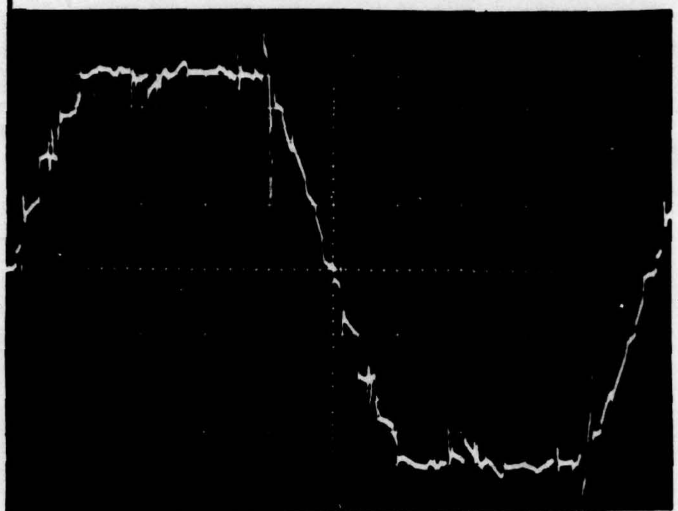
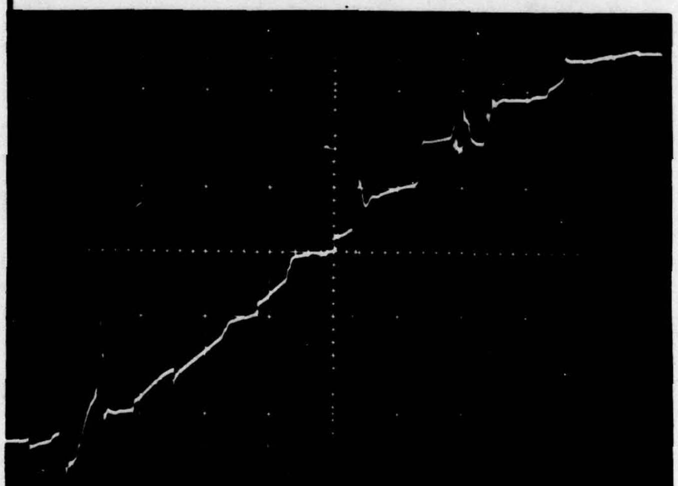
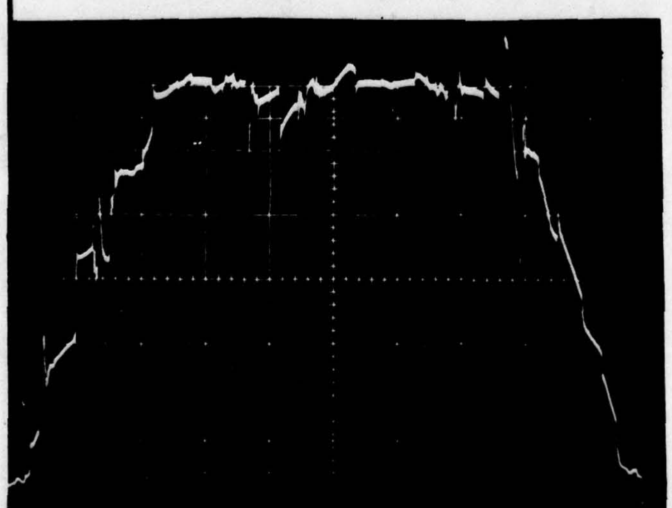
INVERTER BASIC VOLTAGES 400Hz 20.6KW, PF=0.8



V_{c-n}





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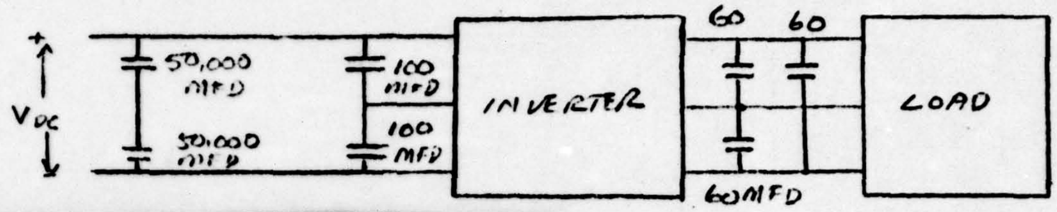
		APPROVED		

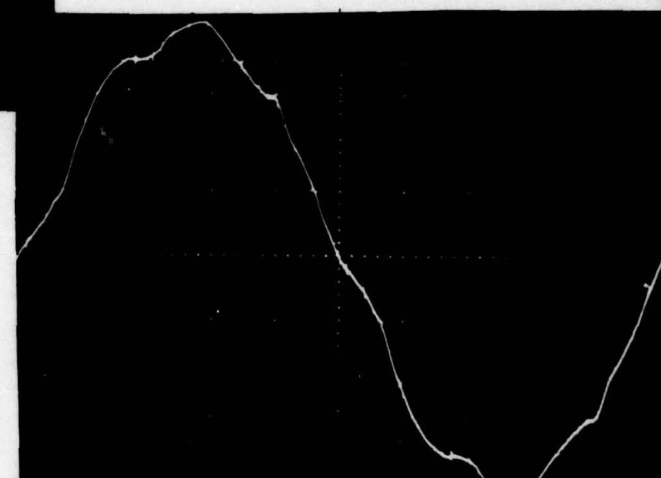
TWO WIRE DC INPUT EXPERIMENT 400HZ, THREE PHASE



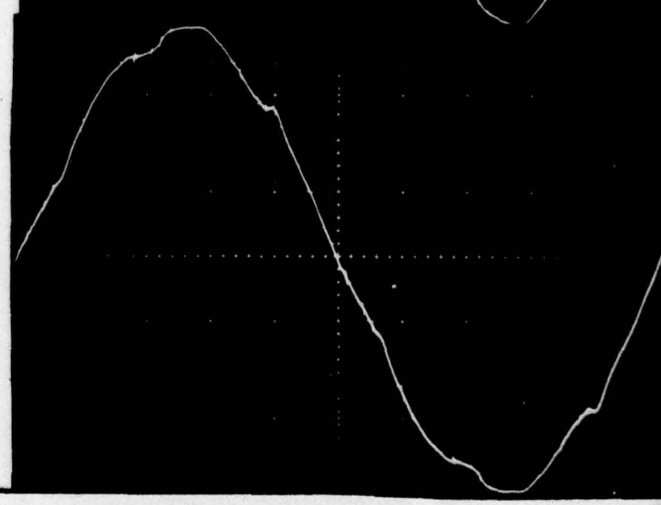
NO LOAD

100V/DIV
THD = 6.4%

V_{DC} = 285VDC



16KW, PF = 1.0
THD = 5.8%



16KW, PF = 0.8
THD = 4.2%

V_{DC} = 295VDC

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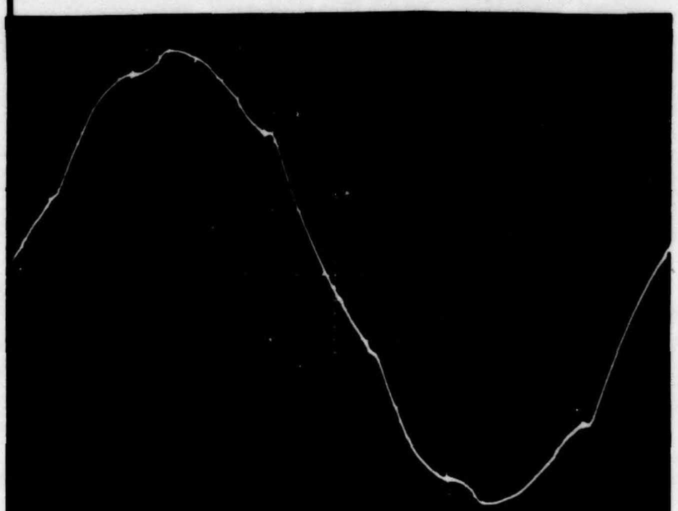
20.6KW, PF=0.8

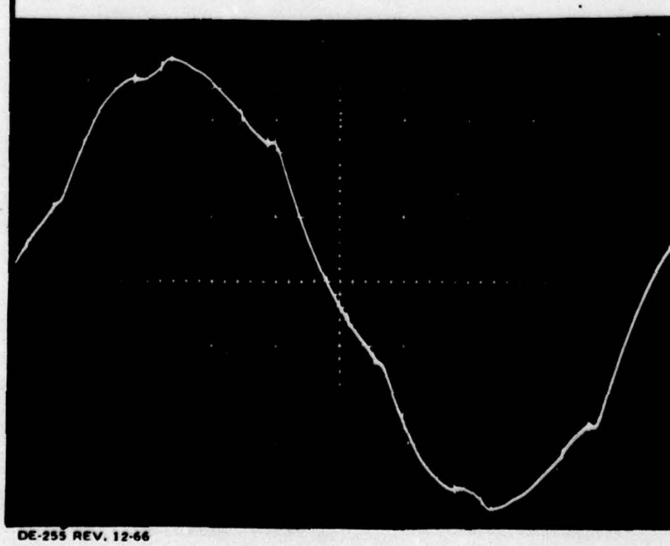
THD= 4%

Vdc=296VDC



22.8KW, PF=0.8

THD=4.4%



24.8KW, PF=0.8

THD =5.2%

92 AMPS DC INPUT CURRENT

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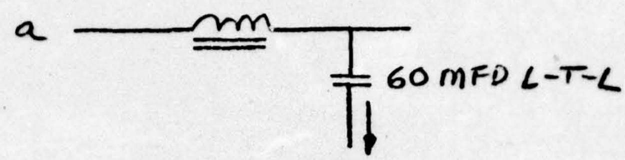
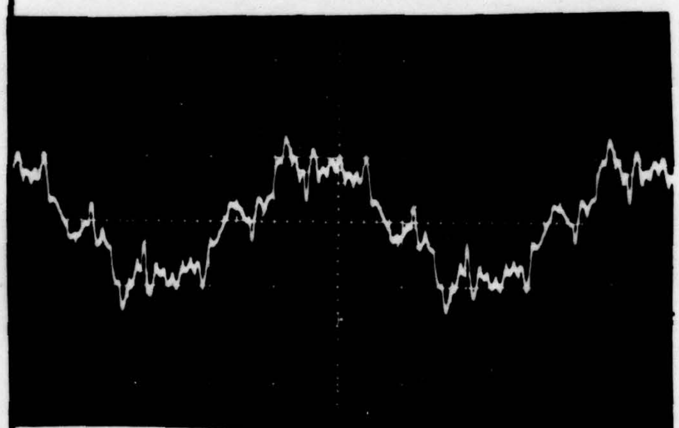
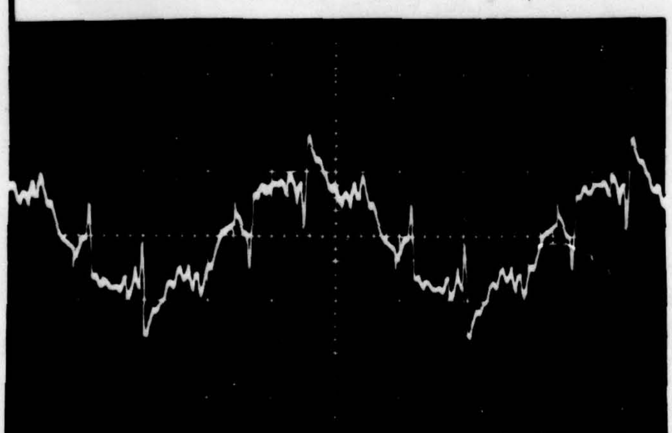


CURRENT THRU 60 MFD. CAPACITOR, 400HZ



NO LOAD

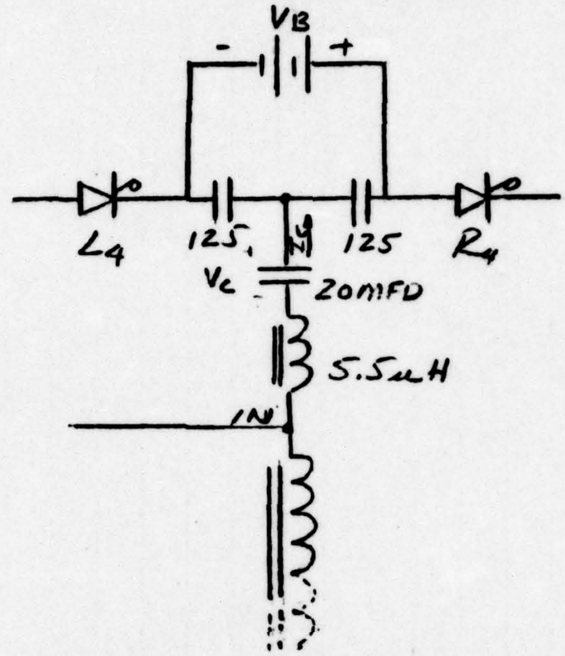
50A/DIV.
500μSEC/DIV.

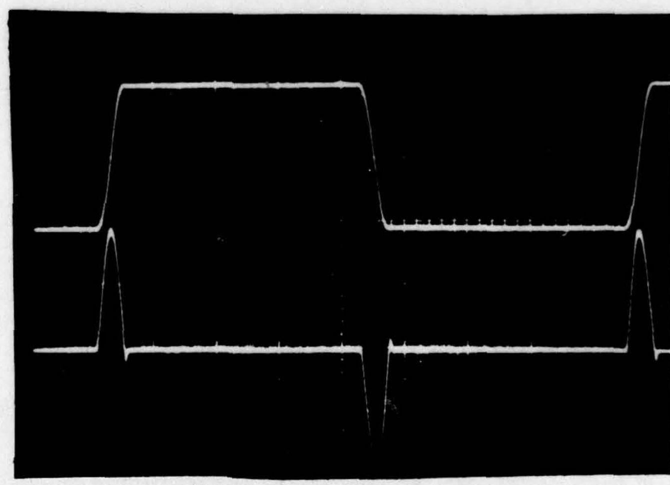


20.6KW, PF=0.8

DISTRIBUTION:

400 Hz POWER CENTER COMMUTATION

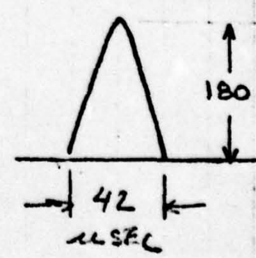




V_B = 70 VDC
I_B = 5 AMPS

V_c 100V/DIV

I_c 100A/DIV.



$V_{c\,RMS}$ = 113.5 Vrms

$I_{c\,RMS}$ = 41.5 Arms.

DISTRIBUTION:

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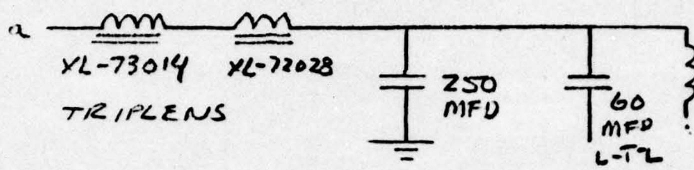
TITLE PERFORMANCE TESTS. ITEM NO. 0006, 15KVA THREE PHASE FREQUENCY CONVERTER, IN ACCORDANCE WITH ATTACHMENT NO. 2 CONTRACT NO. DAAK02-72-3-0210 AND MIL-STD-705B.

PREPARED CORR-1 DATE 11/21/74

CHECKED

APPROVED

3.24.1.1 VOLTAGE OPERATING RANGE



60 HZ THREE PHASE

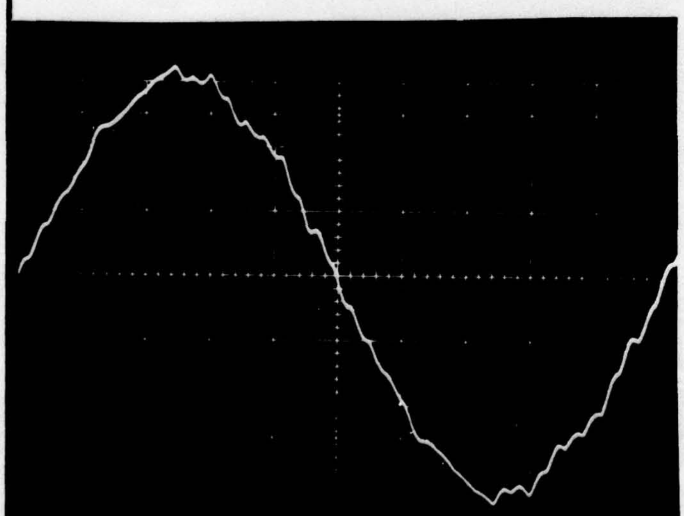
(BOOST COMMUTATION VOLTAGE: 66VDC
I_B = 6.5 AMPS DC)

105 PERCENT OF RATED VOLTAGE

L-T-N VOLTAGE
126V RMS
50V/DIV.

20.6KW, PF=0.8 LOAD
V_{DC} = 315VDC; I_{DC} = 83 AMPS DC

THD = 3.7%



95 PERCENT OF RATED VOLTAGE
114VRMS

20.6KW, PF=0.8 LOAD
V_{DC} = 287VDC; I_{DC} = 76 AMPS DC

THD = 3.5%.

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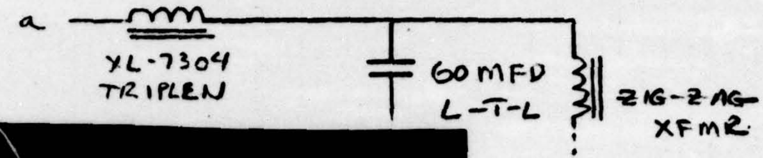
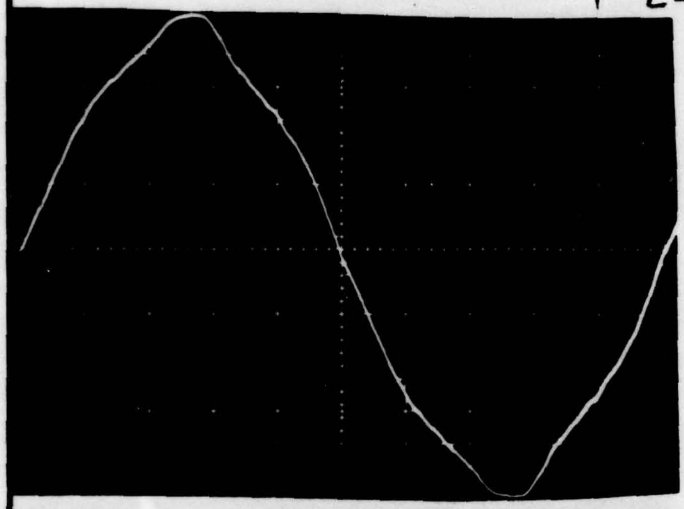
		APPROVED		

3.24.1.1 VOLTAGE OPERATING RANGE 400HZ THREE PHASE



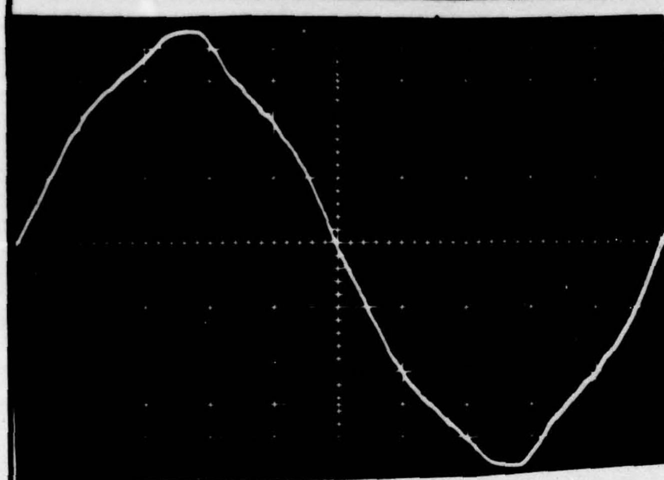
(COMMUTATION BOOST VOLTAGE 30DC; I_B = 2AM



105 PERCENT OF RATED VOLTAGE

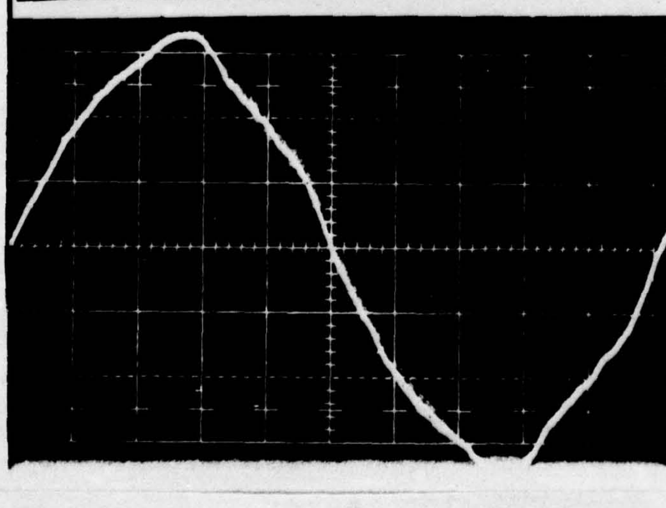
L-T-N VOLTAGE
126 V RMS
50 V/DIV.

NO LOAD
THD = 4%



95 PERCENT OF RATED VOLTAGE
114 V RMS
THD = 3.95% (WITHOUT P.C. COMMUTATION C.T. XFMR)

NO LOAD



95 PERCENT OF RATED VOLTAGE

THD = 4.3% (WITH P.C. COMMUTATION C.T. XFMR)

NO LOAD

DISTRIBUTION:

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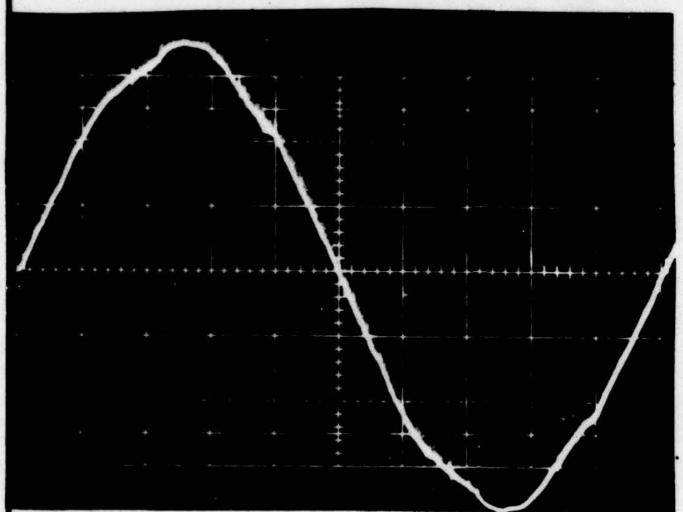
		APPROVED		

3.24.1.1 VOLTAGE OPERATING RANGE — 400 HZ, THREE PHASE

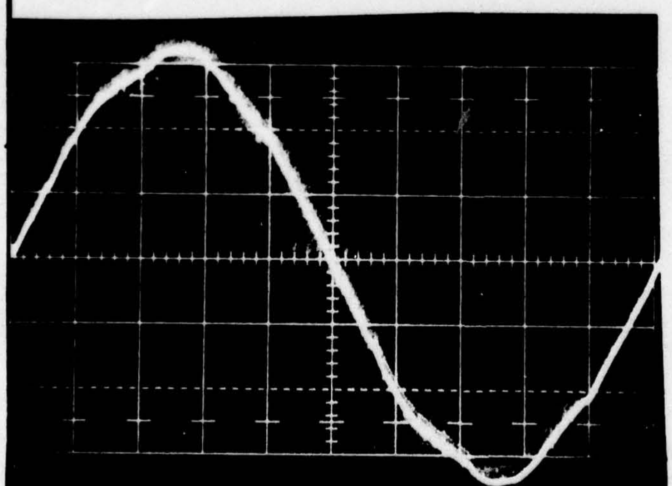


105 PERCENT OF RATED VOLTAGE

L-T-N VOLTAGE
126 VRMS
50V/DIV.

16KW, PF=0.8 LOAD
THD=2.14%

(P.C. REVERSE BIAS TURN-OFF TIME 18 μSEC. WITHOUT COMMUTATION C.T. XFMR. 29 μSEC. WITH C.T. XFMR)



95 PERCENT OF RATED VOLTAGE

114 VRMS

16KW, PF=0.8 LOAD
THD=2.4%

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		APPROVED		

3.24.1.3 VOLTAGE WAVEFORM

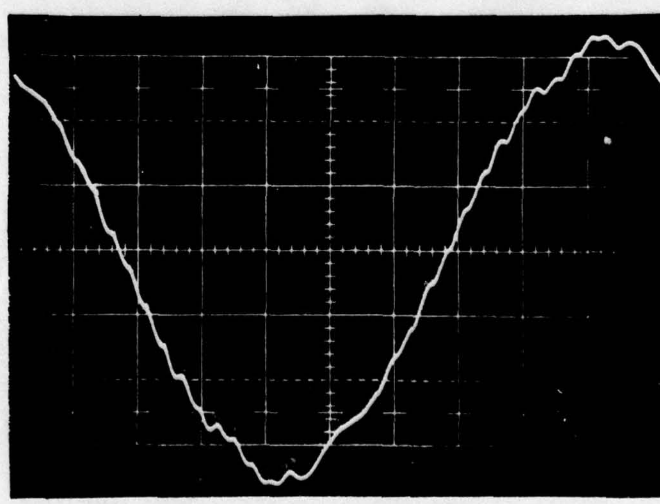
60 HZ THREE PHASE
LINE-TO-NEUTRAL VOLTAGES
NO LOAD

Van
120 Vrms
THD=4%

50V/DIV.

Vbn
119.9 Vrms
THD=4.1%

Vcn
119.9 Vrms
THD=3.75%



(VDC=285.3 VDC ; I_{in} = 2 AMPS)

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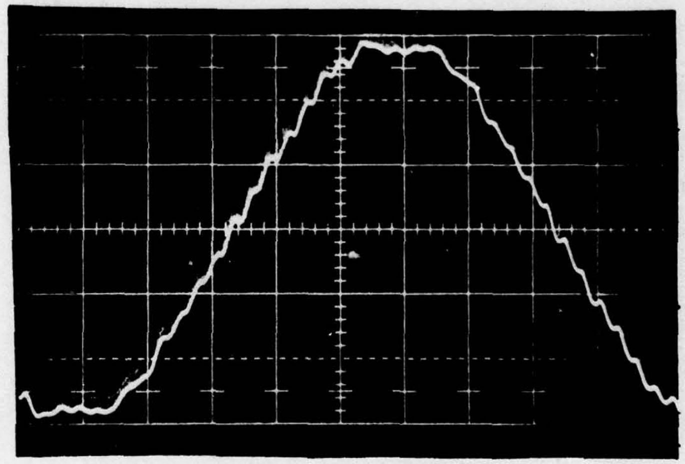
60HZ THREE PHASE
LINE-TO-LINE VOLTAGES

NO LOAD

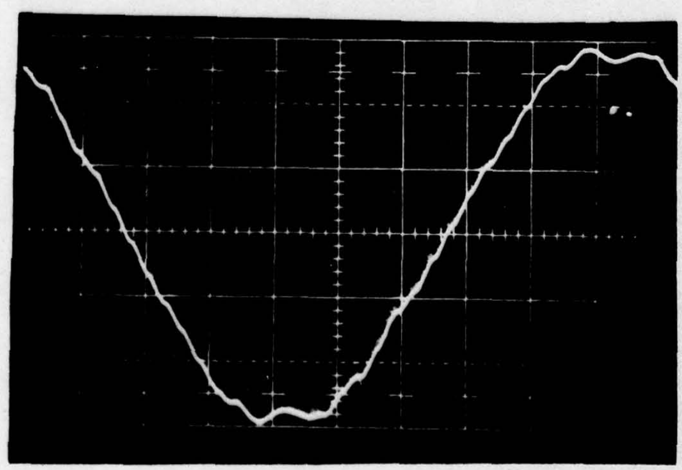
V_{ab}
208 Vrms
THD = 4%

100V/DIV.

V_{bc}
207.9 Vrms
THD = 4.1%



V_{ca}
207.8 Vrms
THD = 3.75%



DISTRIBUTION:

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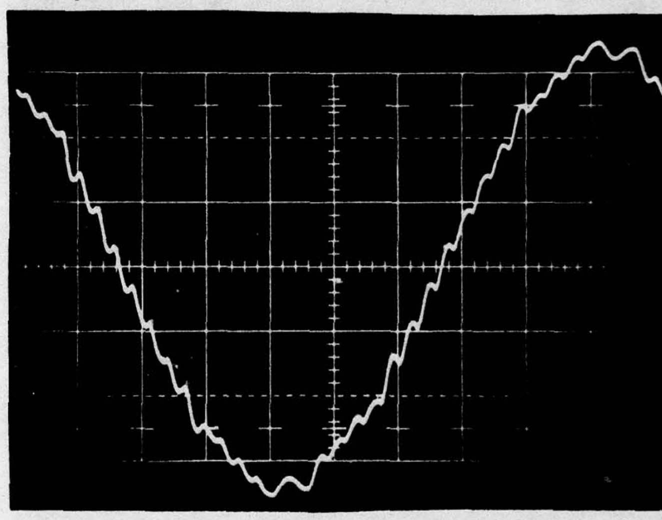
60HZ THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

20.6KW, PF=0.8 LOAD

Van
120.1 Vrms
THD= 3.9%

50V/DIV



Vbn
120.6 Vrms
THD= 4.33%

Vcn
120.5 Vrms
THD= 3.6%

(Vdc=302.5Vdc; Idc=80A)

DISTRIBUTION:

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		APPROVED		

60 HZ THREE PHASE
LINE-TO-LINE VOLTAGES

20.6KW, PF=0.8 LOAD

Vab
207.0 Vrms

THD= 3.9%

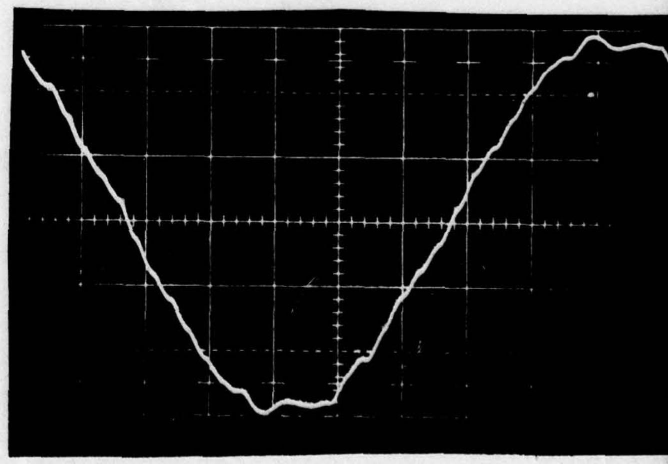
100V/DIV.

Vbc
209 Vrms

THD= 4.33%

Vca
207.2 Vrms

THD = 3.6%



DISTRIBUTION:

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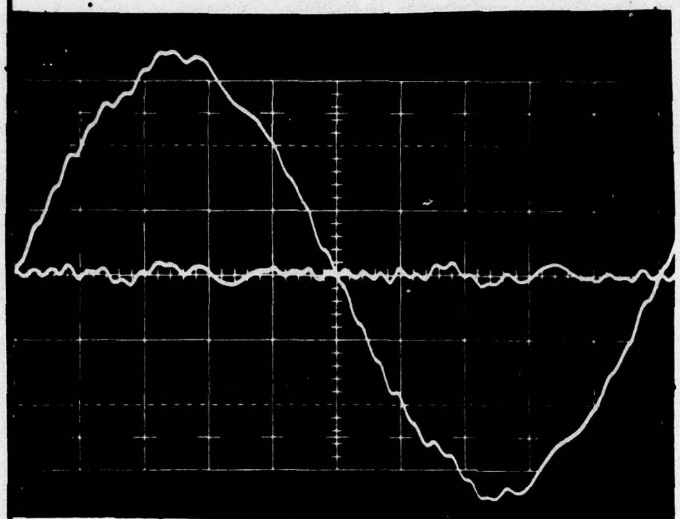
DEVIATION FACTOR

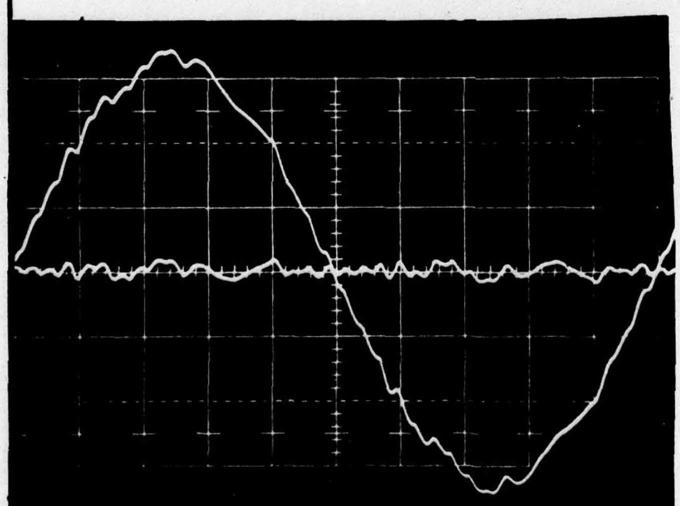
60HZ THREE PHASE
LINE-TO-NEUTRAL VOLTAGES



NO LOAD

VOLTAGE INTO 60HZ NOTCH FILTER COMPARED TO VOLTAGE OUT OF FILTER

50V/DIV.



16KW, PF-0.8 LOAD

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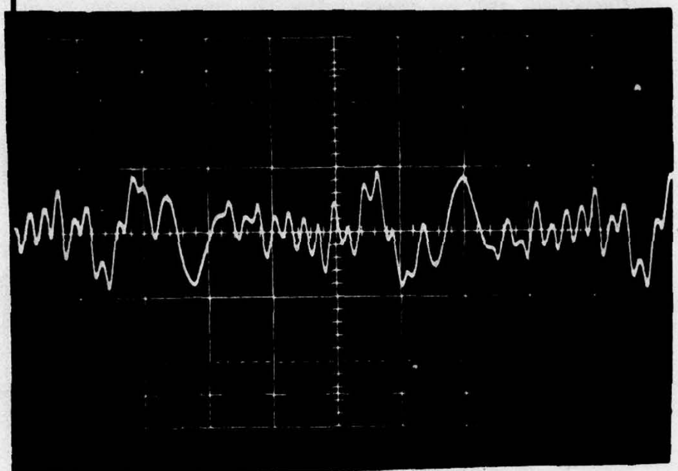
DEVIATION FACTOR

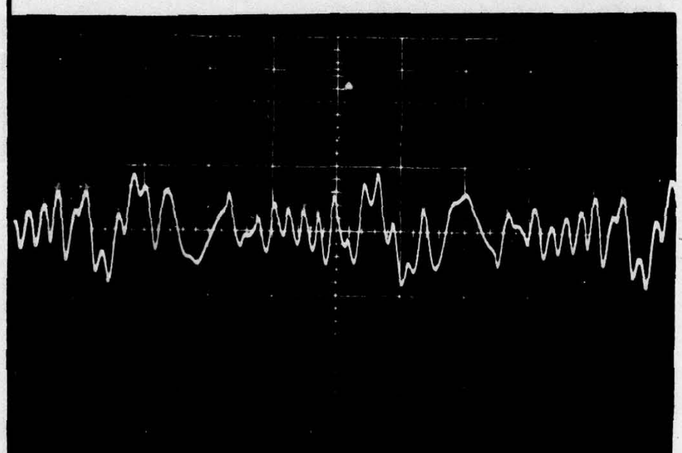
60 HZ THREE PHASE LINE-TO-NEUTRAL VOLTAGES



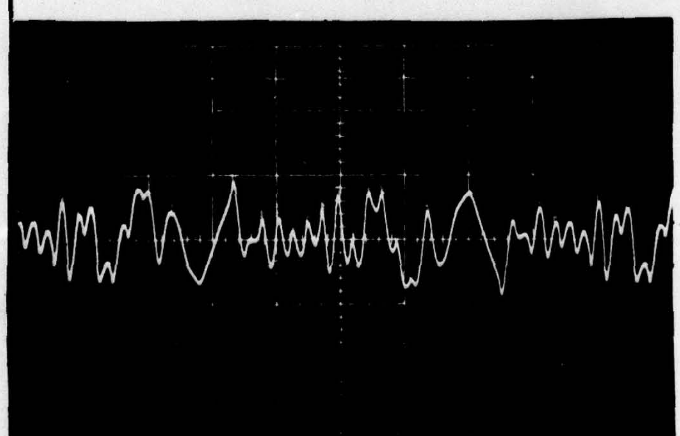
OUTPUT OF 60HZ NOTCH FILTER

NO LOAD

10V / DIV.
2 ms / DIV.



16KW, PF-1.0



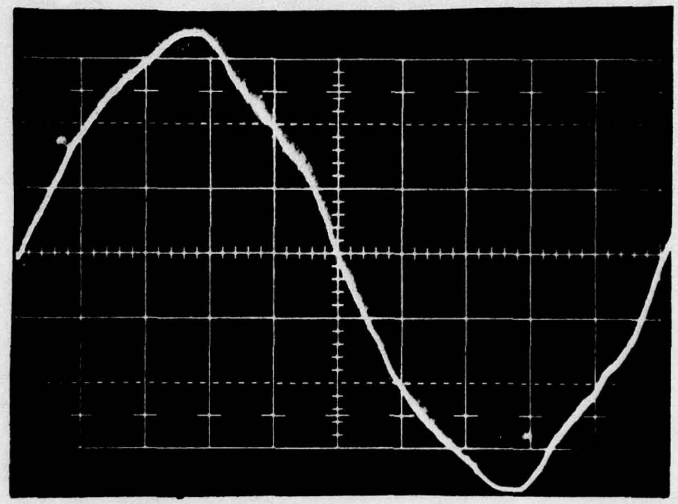
16KW, PF-0.8

DISTRIBUTION:

400 Hz THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

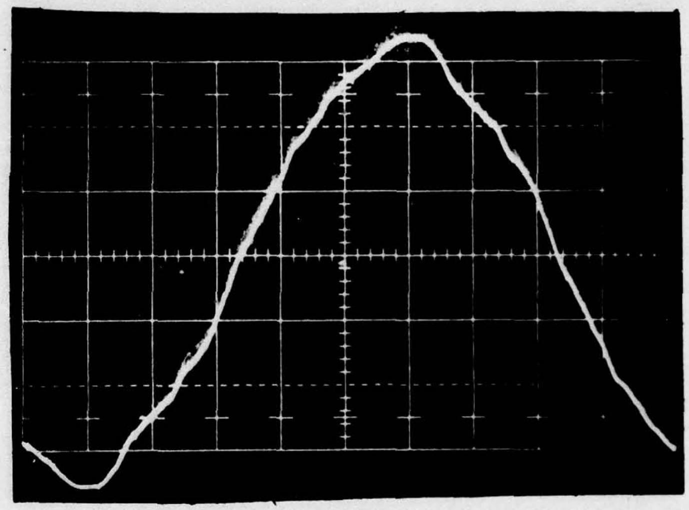
NO LOAD

Van
120 Vrms
THD = 4.2%

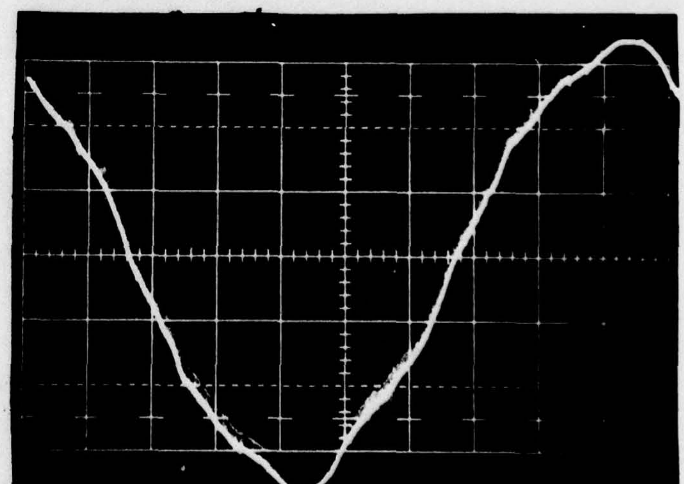


50V/DIV.

Vbn
119.5 Vrms
THD = 3.9%



Vcn
119.9 Vrms
THD = 4.1%



(VDC = 280V DC; IDC = 5 AMPS)
(VBOOST = 80VDC; IBC = 3.0)

DISTRIBUTION:

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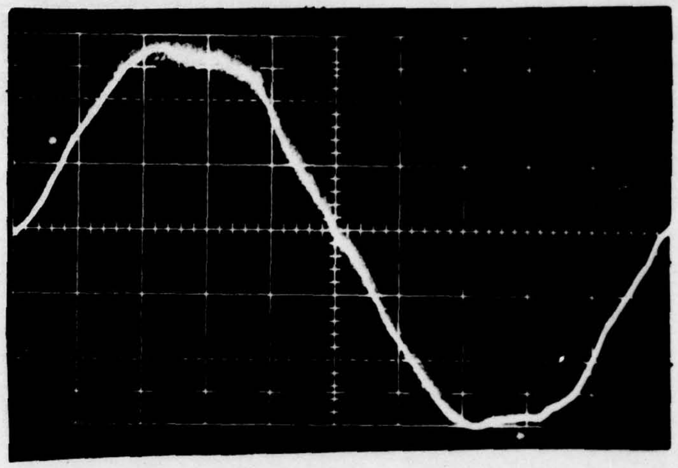
400 HZ THREE PHASE
LINE-TO-LINE VOLTAGES

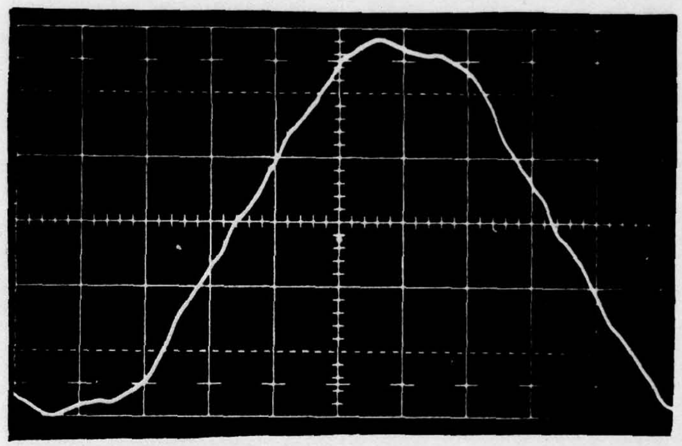
NO LOAD

Vab
207Vrms
THD= 4.2%

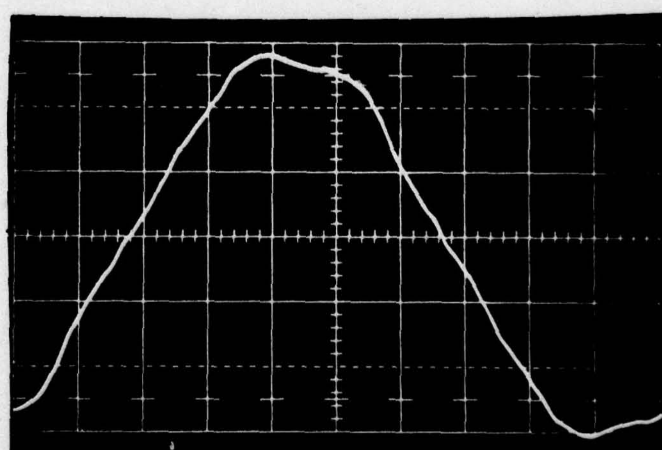
100V/DIV.



Vbc
206.5Vrms
THD= 3.9%



Vca
207.5Vrms
THD= 4.1%



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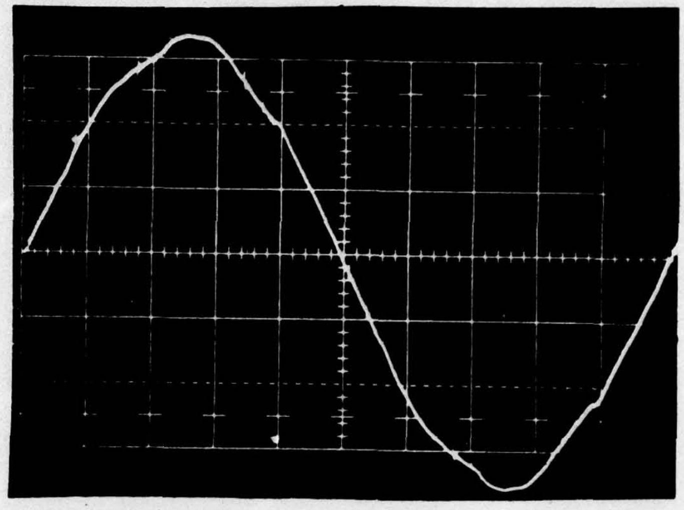
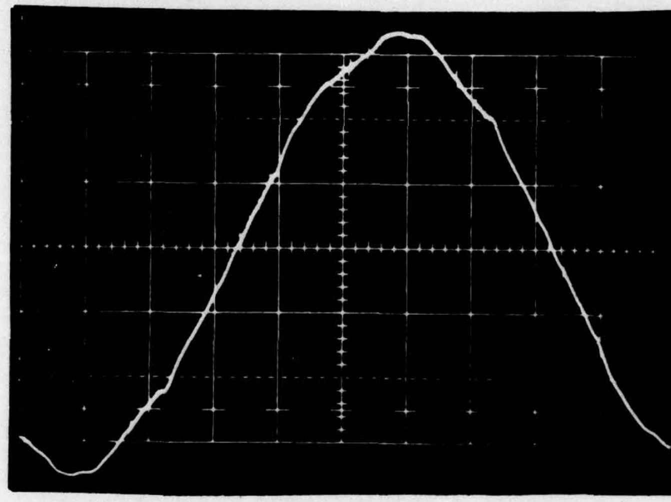
400 HZ THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

16KW, PF=1 LOAD

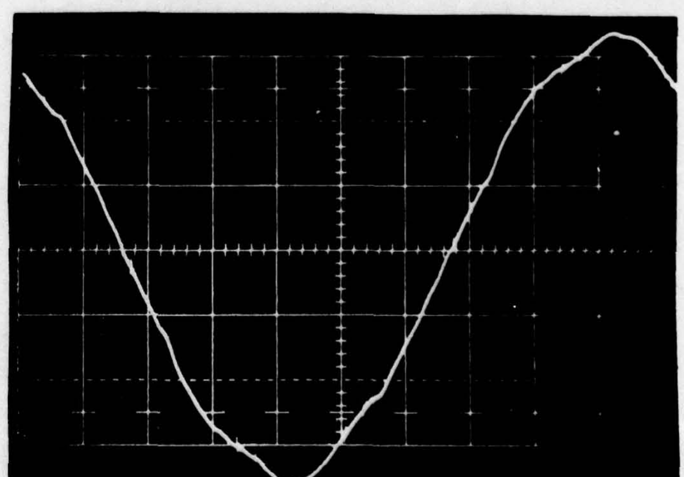
Van
120 Vrms
THD = 2.48%



Vbn
119.3 Vrms
THD = 2.19%



Vcn
120 Vrms
THD = 2.7%



DISTRIBUTION:

(VDC = 295.5 VDC; IDC = 62 A)
(VBOOST = 30V IDC = 3A.)

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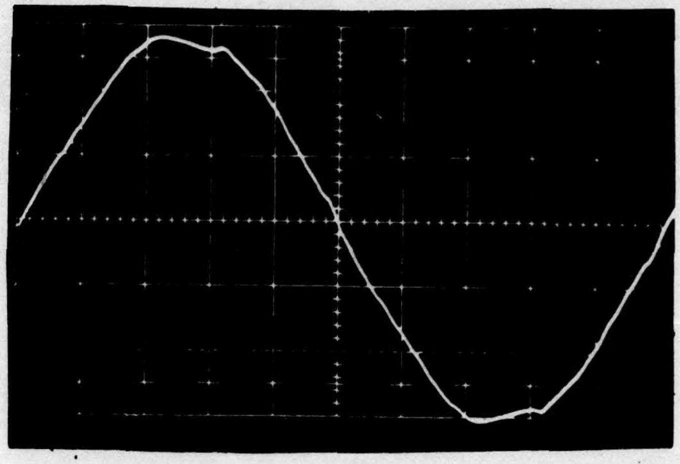
400 Hz THREE PHASE
LINE-TO-LINE VOLTAGES

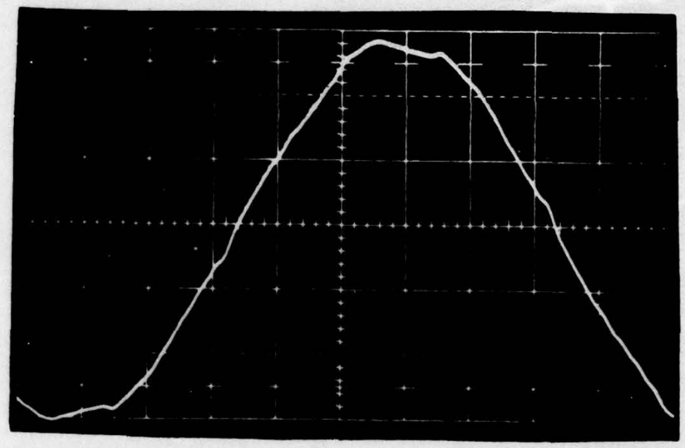
16KW, PF=0.8 LOAD

Vab
206 Vrms
THD= 2.48%

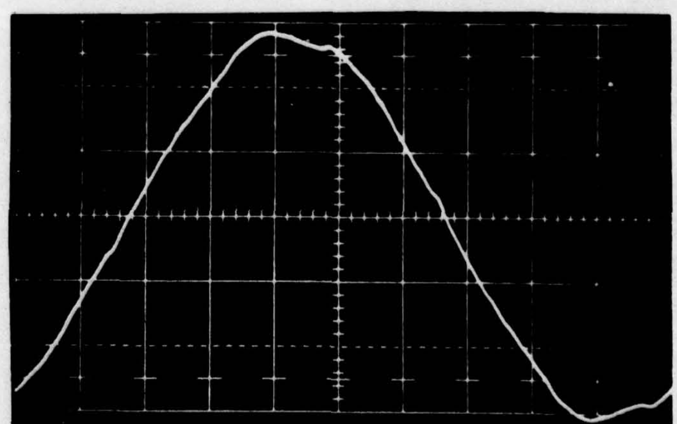
100V/DIV



Vbc
207Vrms
THD= [illegible]



Vca
206.5 Vrms
THD= 2.7%



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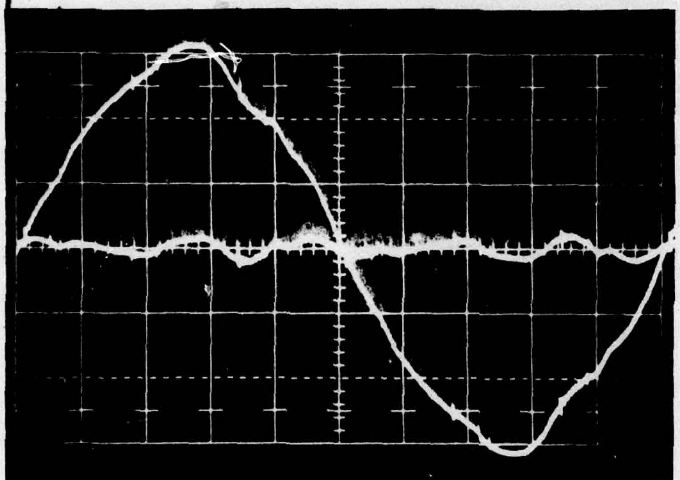
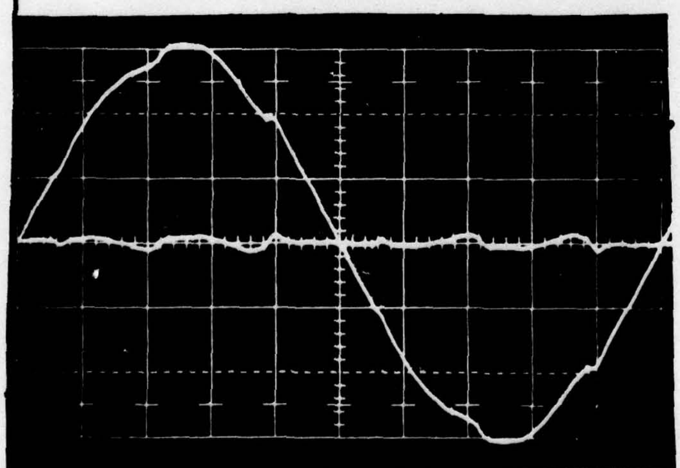
DEVIATION FACTOR

400 HZ THREE. PHASE
LINE-TO-NEUTRAL VOLTAGES



NO LOAD

RELATIVE VOLTAGES
INTO AND OUT OF
400 HZ NOTCH FILTER
10:1 ATTENUATION
5 V/DIV.



16 KW, PF = 0.8

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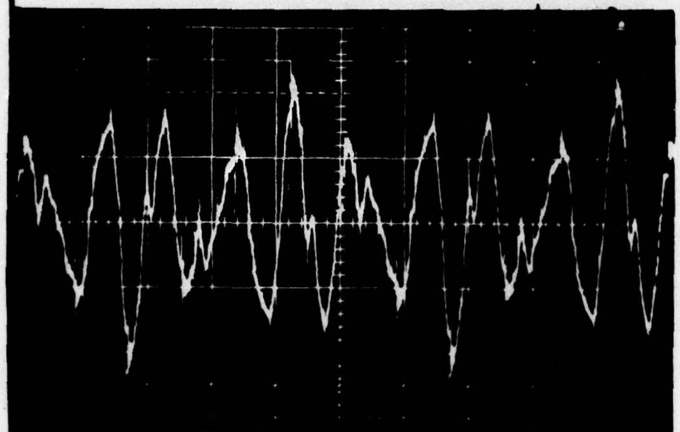
DEVIATION FACTOR

400 HZ THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

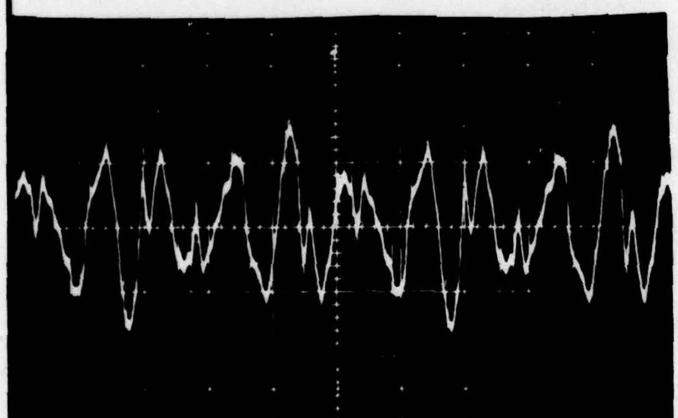
OUTPUT OF 400 HZ NOTCH FILTER



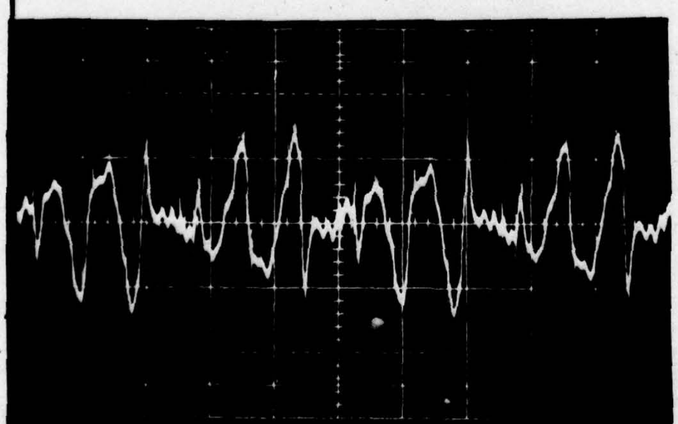
NO LOAD

0.5 V/DIV.

500 μSEC/DIV.



16KW, PF=1.0



16KW, PF 0.8

DISTRIBUTION:

MEASUREMENTS OF INDIVIDUAL HARMONICS

60 HZ THREE PHASE 11KW, PF= 0.8 LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL L-T-N	L-T-L
1	60	100	100
3	180	0.20	0.30
5	300	1.10	1.25
7	420	1.60	1.50
11	660	1.95	1.60
13	780	0.60	0.26
15	900	—	0.26
17	1020	1.60	1.60
19	1140	0.30	0.72
21	1260	—	0.22
23	1380	—	0.28
25	1500	0.20	0.56
29	1740	0.28	1.52
31	1860	—	0.20
35	2100	1.20	1.70
37	2220	0.70	1.20

ONLY HARMONICS ≥ 0.2% RECORDED

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MEASUREMENTS OF INDIVIDUAL HARMONICS

400 HZ THREE PHASE 11KW; PF=0.8 LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL L-T-N	PERCENT OF FUNDAMENTAL L-T-L
1	400	100	100
5	2000	2.4	2.35
7	2800	1.83	1.50
11	4400	0.63	0.80
13	5200	0.78	1.10
17	6800	0.39	0.42
19	7600	0.43	0.60
23	9200	0.31	0.38
25	10,000	0.21	0.33
29	11,600	0.21	0.29
35	14,000	0.22	0.30

DISTRIBUTION:

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DC VOLTAGE COMPONENT

400 HZ, THREE PHASE	MV D.C.		
	NO LOAD	16KW PF=1.0	16KW PF=0.8
Van	23.8	6.8	17.5
Vbn	15.0	0.2	27.9
Vcn	8.3	1.2	12.6
60HZ, THREE PHASE			
Van	3.4	20.0	20.0
Vbn	10.0	24.0	38.0
Vcn	9.5	17.0	37.0

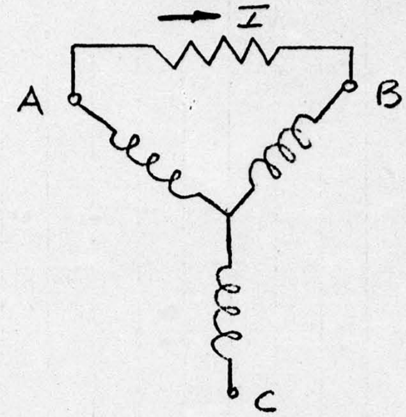
DISTRIBUTION:

3.24.1.4 PHASE VOLTAGE BALANCE

FREQ. HZ	LOAD KW	P.F.	Van Vrms	Vbn Vrms	Vcn Vrms	Vab Vrms	Vbc Vrms	Vca Vrms
60	0	—	120	119.9	119.9	208	207.9	207.8
60	20.6	0.8	120.1	120.6	120.5	207.0	209	207.2
400	0	—	120	119.5	119.9	207	206.5	207.5
400	16	0.8	120	119.3	120	206	207	206.5

DISTRIBUTION:

3.24.1.5 EFFECT OF UNBALANCED LOAD (3 PHASE)



	60 HZ	400 HZ
	I = 12 A.rms	I = 12 A.rms
V_{ab}	206 Vrms	207 Vrms
V_{bc}	206	203
V_{ca}	201	208
V_{an}	117.2	121.2
V_{bn}	117.0	119
V_{cn}	120	118.5
MAXIMUM L-T-L VOLTAGE DIFFERENCE	5.0 Vrms	5.0 Vrms

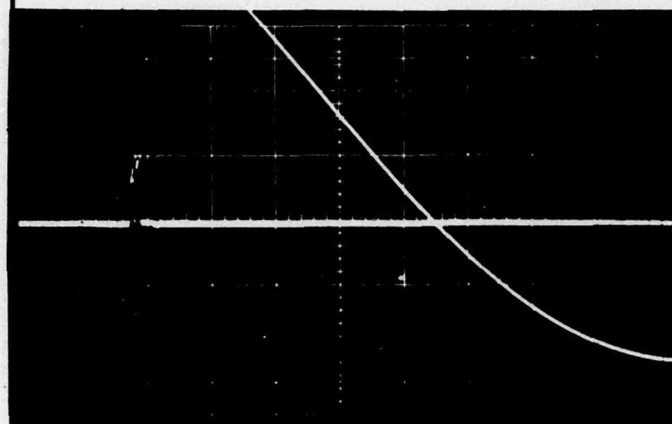
$\frac{5.0}{206} \times 100 = 2.42\%$

$\frac{5.0}{208} \times 100 = 2.4\%$

DISTRIBUTION:

3.24.16 PHASE ANGLE BALANCE

60HZ BALANCED LOAD
L-T-N VOLTAGES



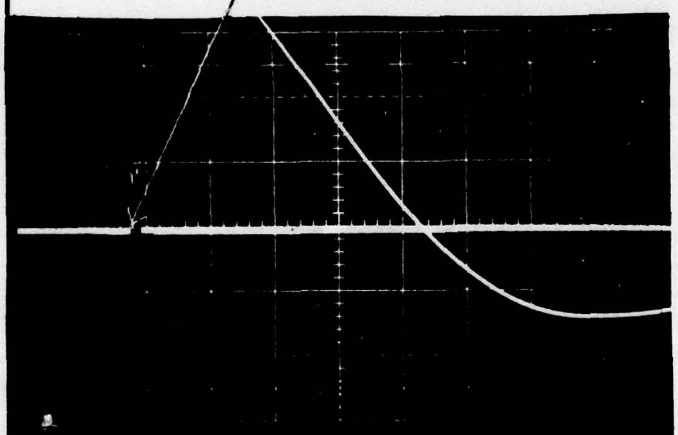
NO LOAD

PHASE A

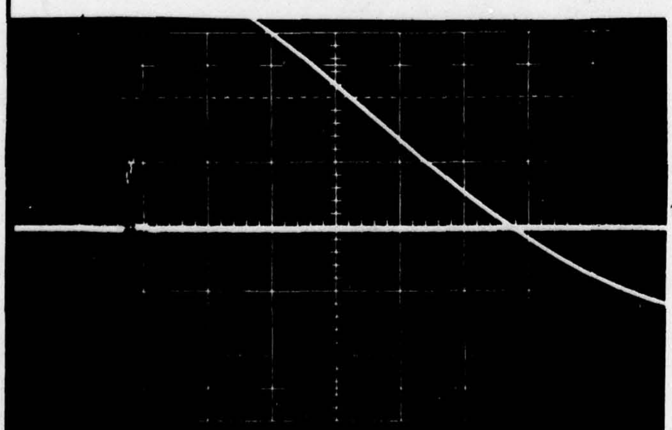
0 CROSS-OVER

↕ 5V/DIV
↔ 1.09°/DIV
(50μsec/DIV)

REFERENCE MARKER



PHASE B



PHASE C

DISTRIBUTION:

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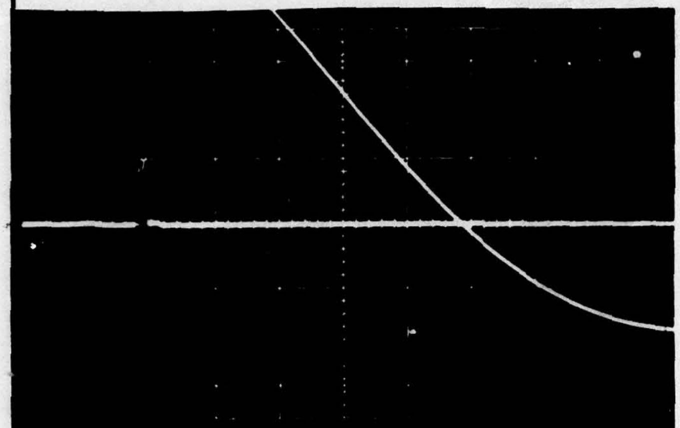
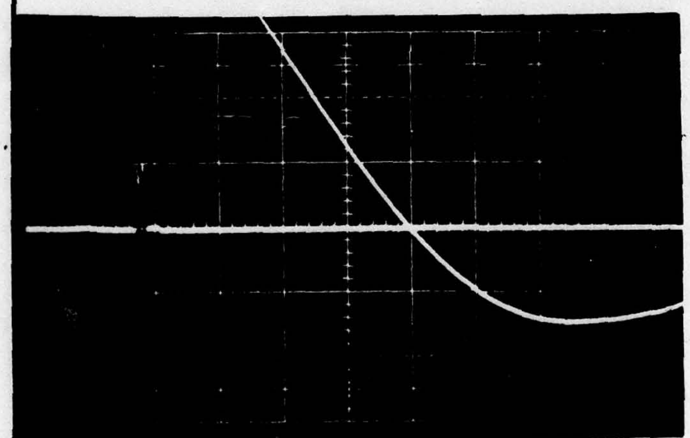
60 HZ BALANCED LOAD
L-T-N VOLTAGES

16KW, PF=1.0 LOAD

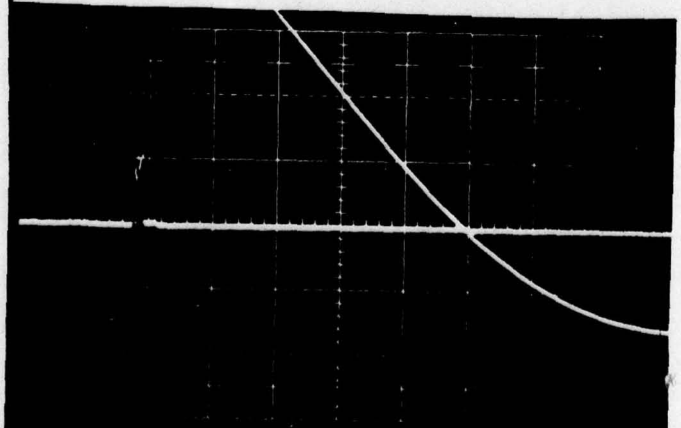


PHASE A

↕ 5V/DIV.
↔ 1.09°/DIV.
(50μSEC/DIV.)



PHASE B



PHASE C

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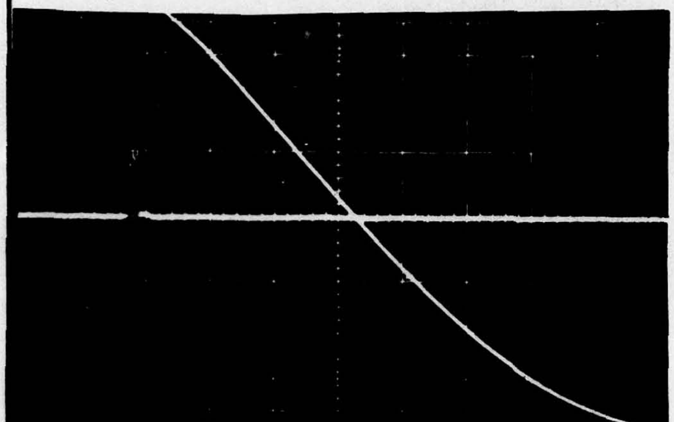
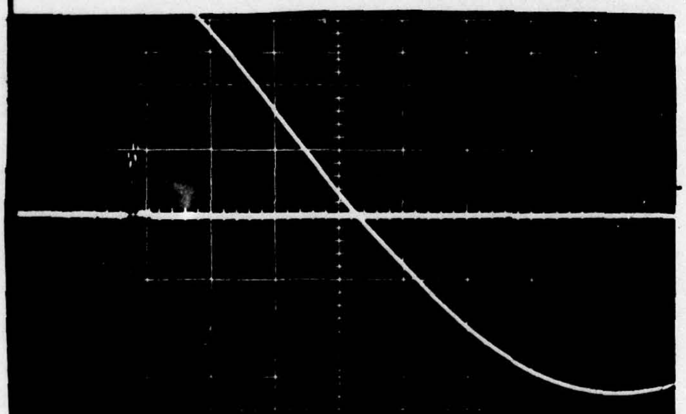
60 Hz BALANCED LOAD
L-T-N VOLTAGES

16KW, PF=0.8 LOAD

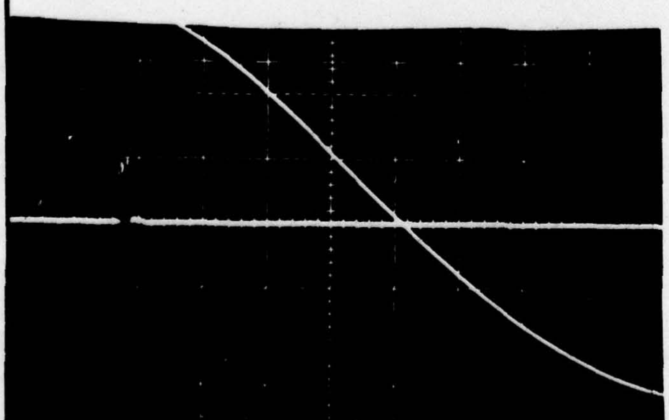


PHASE A

↕ 5V/DIV.
⟷ 1.09°/DIV.
(50μSEC/DIV.)



PHASE B



PHASE C

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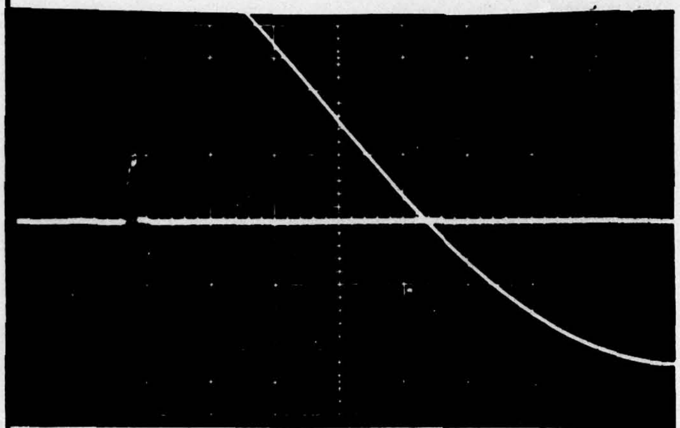
60 HZ <u>25 PERCENT UNBALANCED LOAD</u>
AS DESCRIBED IN 3.24.1.5

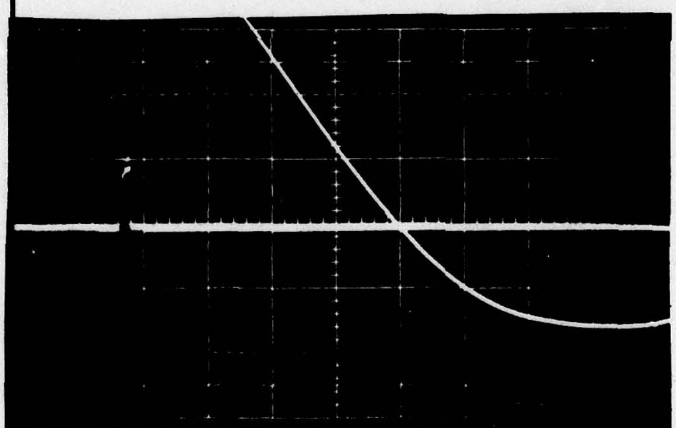
L-T-N VOLTAGES



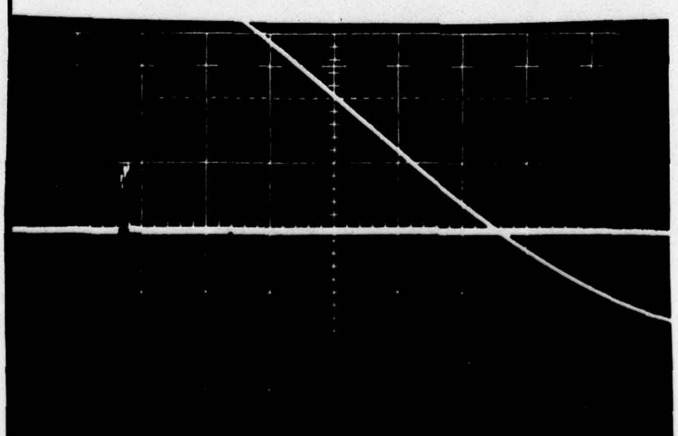
PHASE A

↕ 5V/DIV.
⟷ 1.09°/DIV.

4.4 KW, PF-1.0 LOAD
PHASES A-B



PHASE B



PHASE C

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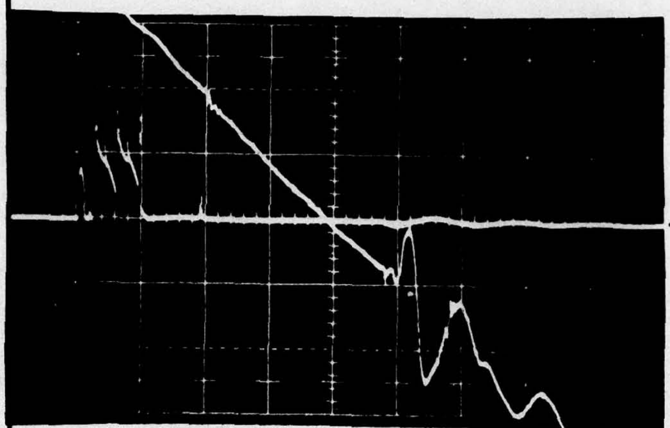
400 HZ BALANCED LOAD
L-T-N VOLTAGES

NO LOAD



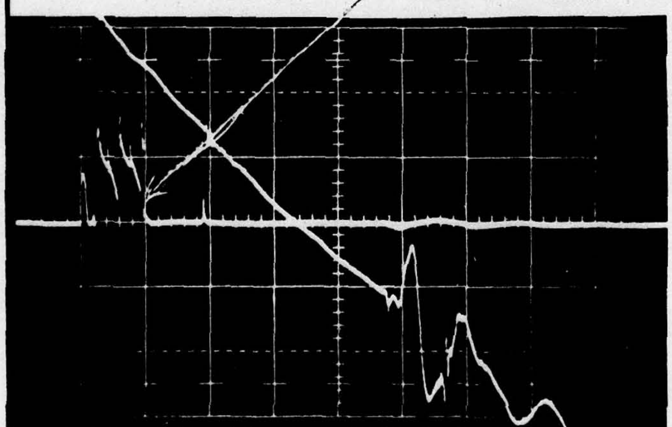
PHASE A

-0 CROSS OVER

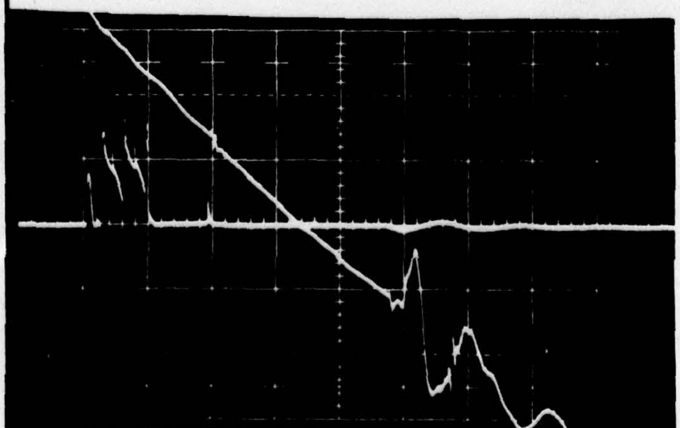
↕ 5V /DIV.

⟷ 1.44°/ DIV.
(10μSEC/DIV.)

-REFERENCE MARKER



PHASE B



PHASE C

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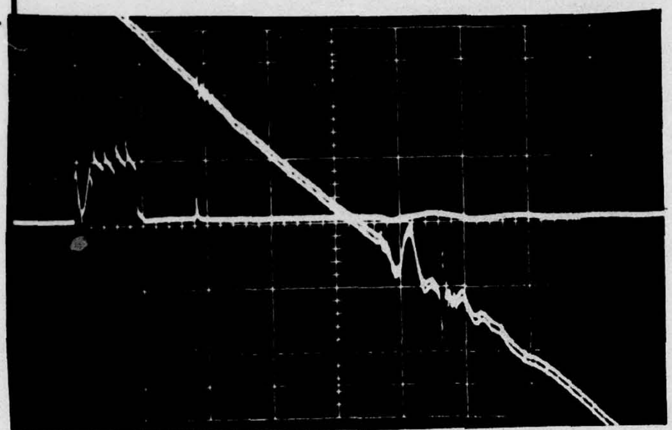
400HZ BALANCED LOAD
L-T-N VOLTAGES

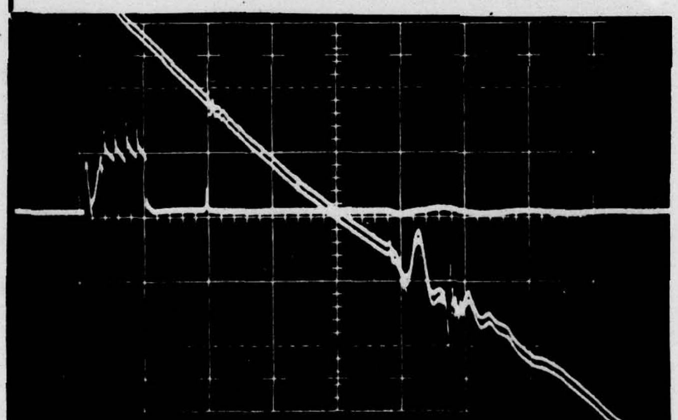
16KW, PF=1.0 LOAD



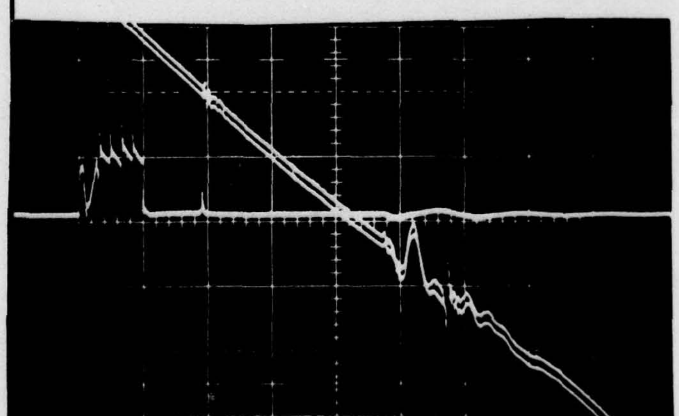
PHASE A

↕ 5V/DIV.

⟷ 1.44°/DIV.



PHASE B



PHASE C

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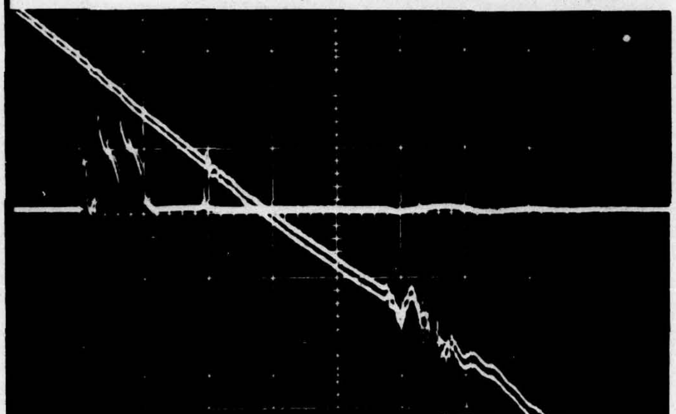
400 HZ BALANCED LOAD
L-T-N VOLTAGES

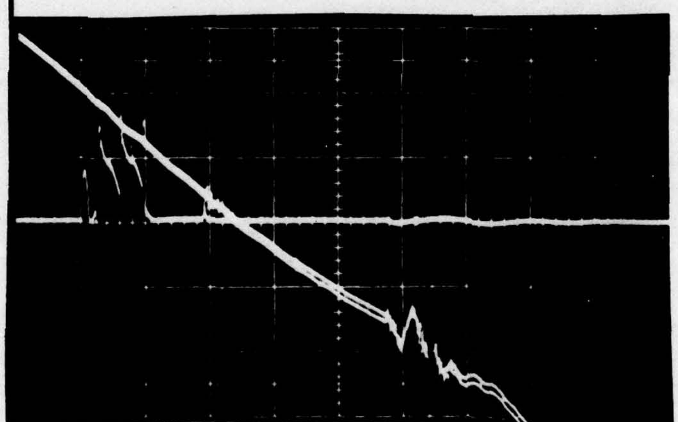


16KW, PF-0.8 LOAD

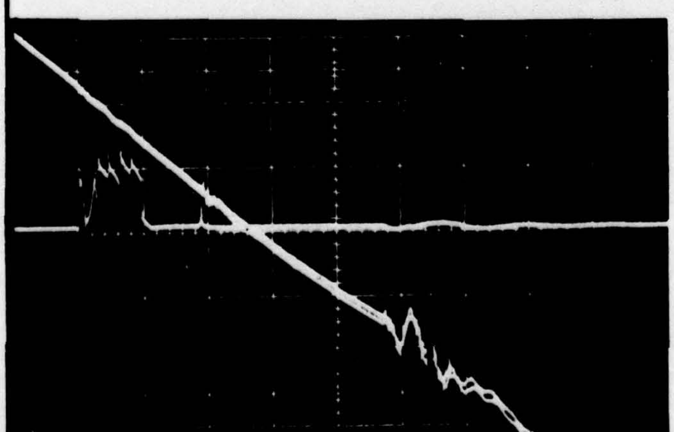
PHASE A

↕ 5V/DIV.

↔ 1.44°/DIV.



PHASE B



PHASE C

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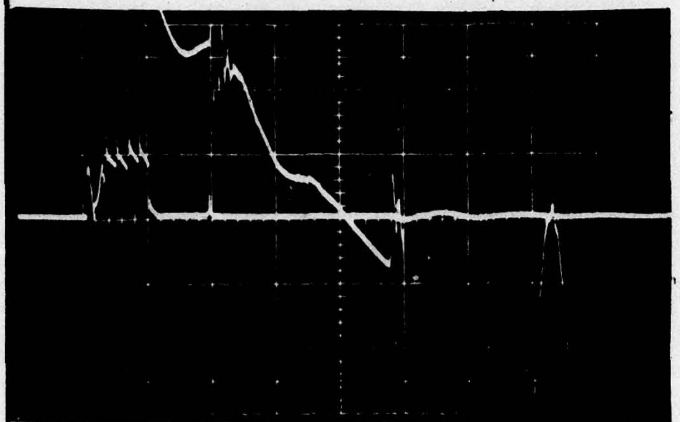
400 Hz 25 PERCENT UNBALANCED LOAD
AS DESCRIBED IN 3.24.1.5



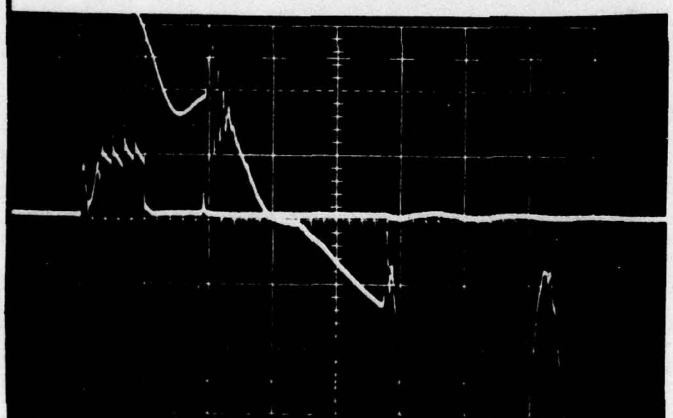
L-T-N VOLTAGE

PHASE A

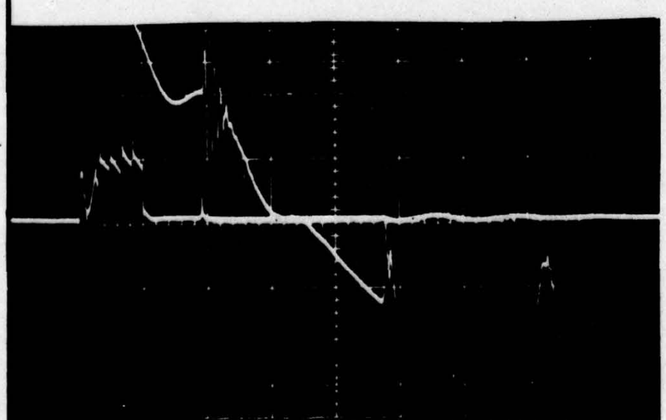
↕ 5V/DIV.

⟷ 1.44°/DIV.

4.4KW, PF = 1.0 LOAD
PHASES A-B



PHASE B



PHASE C

DISTRIBUTION:

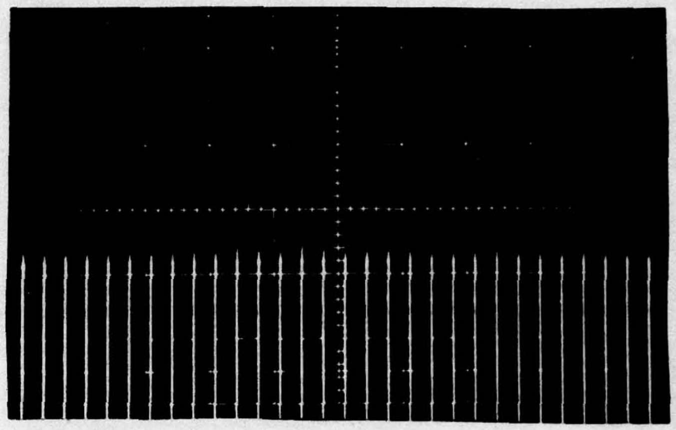
3.24.1.7 VOLTAGE MODULATION

60 HZ THREE PHASE
L-T-N VOLTAGE Van

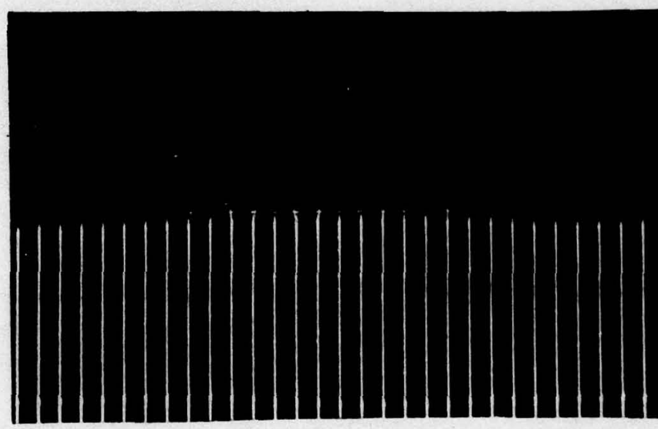
NO LOAD

2V/DIV.

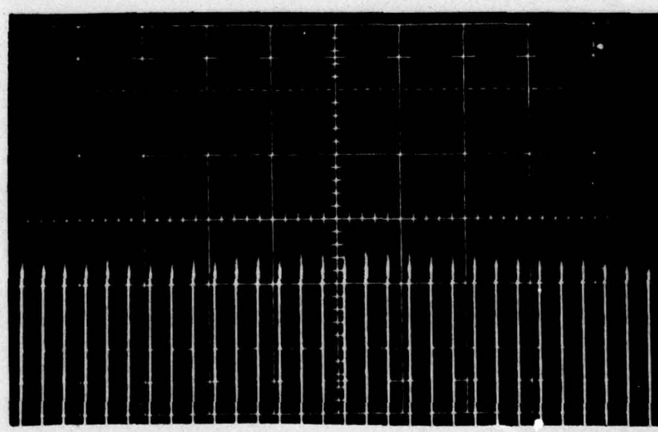
50ms/DIV.



16KW, PF-1.0 LOAD



16KW, PF=0.8 LOAD



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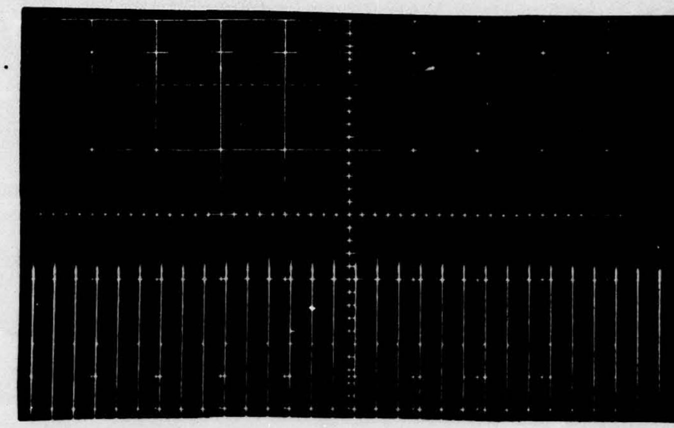
60 HZ THREE PHASE
L-T-L VOLTAGE Vab

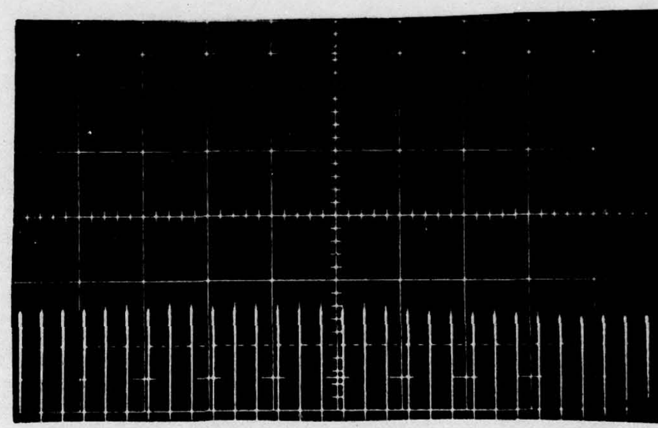
NO LOAD

2V/DIV.

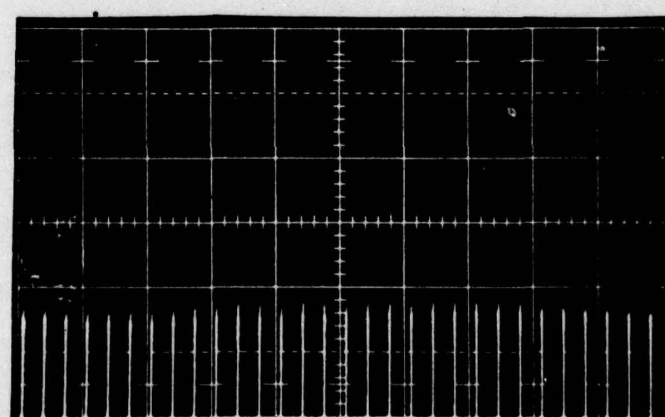
50 ms/DIV.



16KW, PF=1.0 LOAD



16KW, PF=0.8 LOAD



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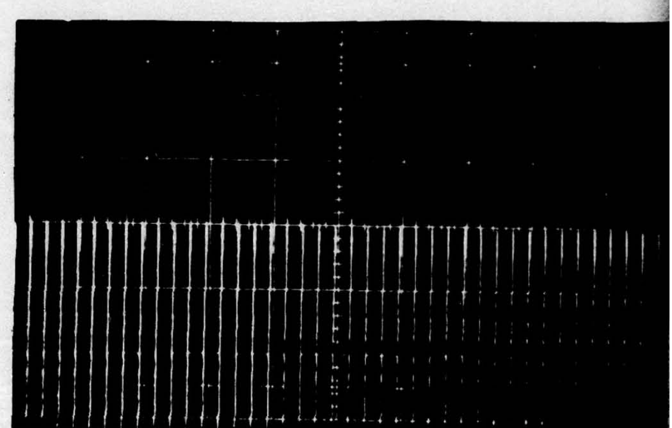
400HZ THREE PHASE
L-T-N VOLTAGE Van

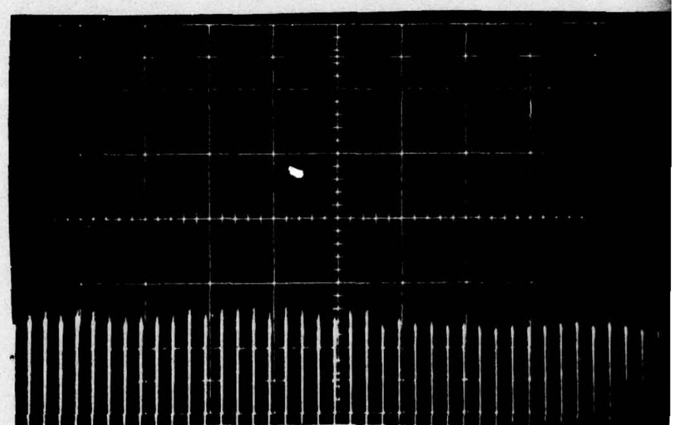
NO LOAD

2V/DIV.

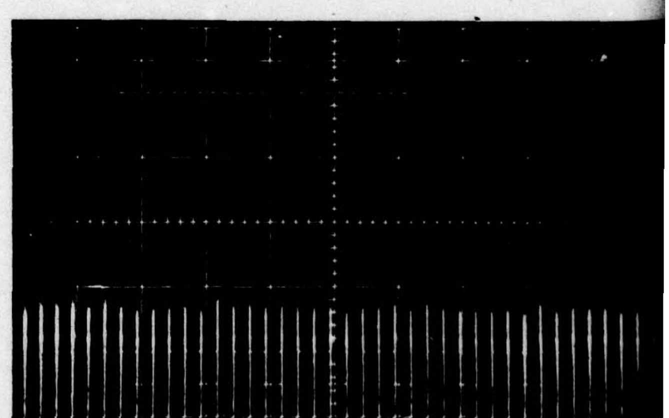
10ms/DIV.



16KW, PF-1.0 LOAD



16KW, PF=0.8 LOAD



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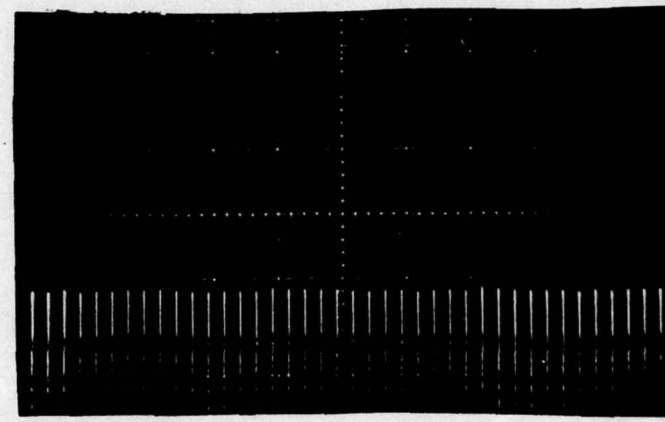
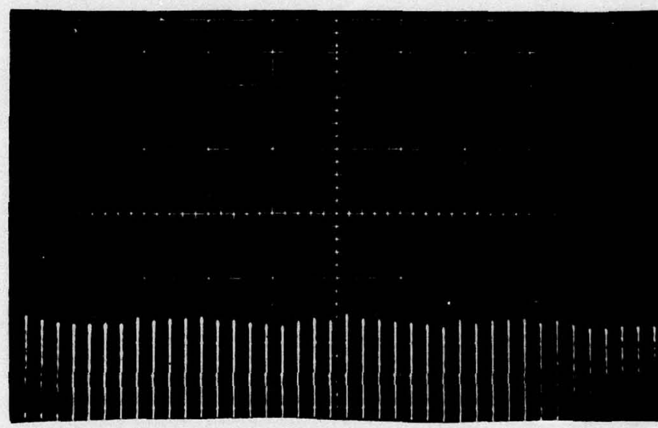
400 HZ, THREE PHASE
L-T-L VOLTAGE Vab

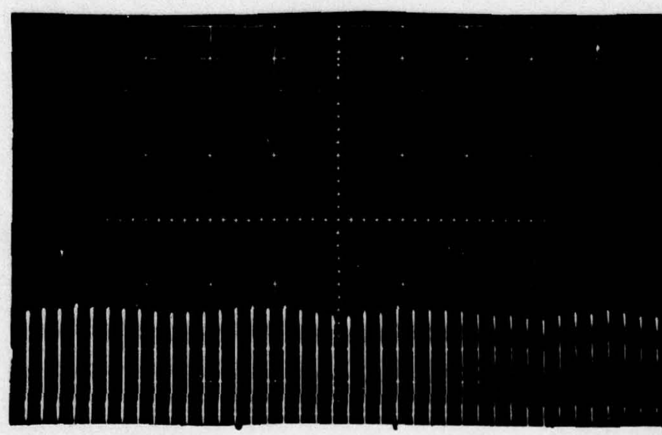
NO LOAD



16KW, PF=1.0 LOAD



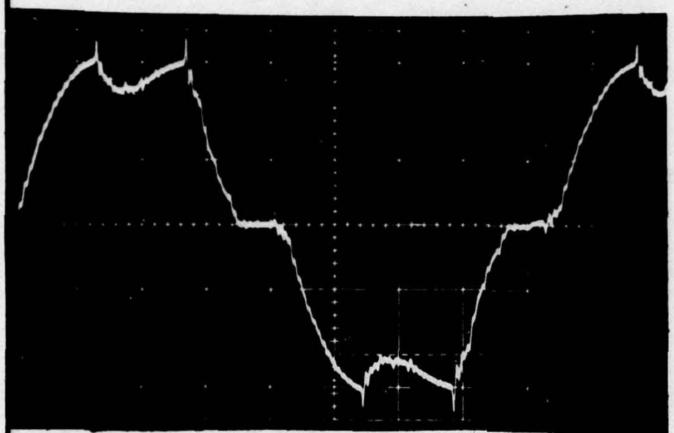
16KW, PF=0.8 LOAD



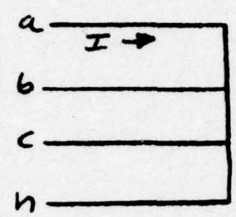
DISTRIBUTION:

3.24.1.13 SHORT CIRCUIT

60 HZ SHORT CIRCUIT CURRENTS

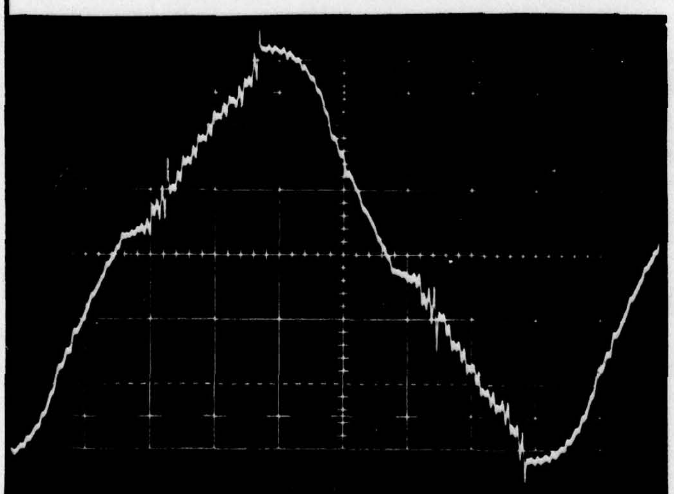


THREE PHASE SHORT CKT

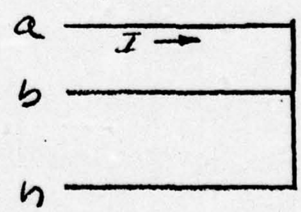


40 A / DIV.
PEAK CURRENT = 100 AMPS*
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)
*POWER SOURCE CIRCUIT BREAKER TRIPS.

V_{DC} = 17.5 VDC (COMM. BOOST VOLTAGE = 66 VDC, I_B = 9 AMPS. FOR ALL 60HZ SHORT CIRCUIT TESTS)



TWO PHASE SHORT CKT.



40 A / DIV.
PEAK CURRENT = 128 AMPS.

(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

V_{DC} = 22.6 VDC

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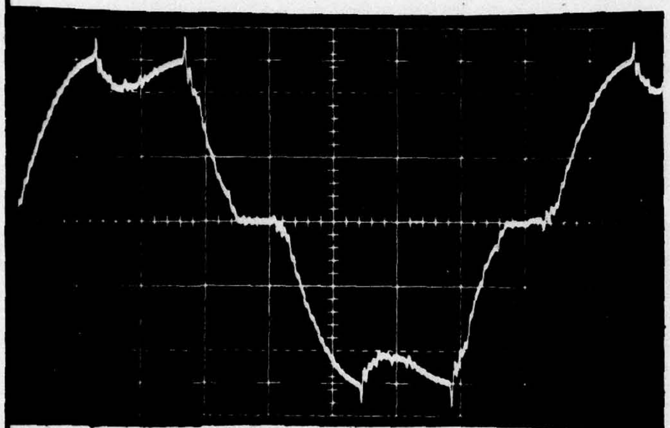
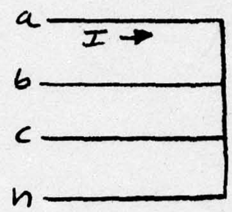
3.29.1.13 SHORT CIRCUIT

60 HZ SHORT CIRCUIT CURRENTS



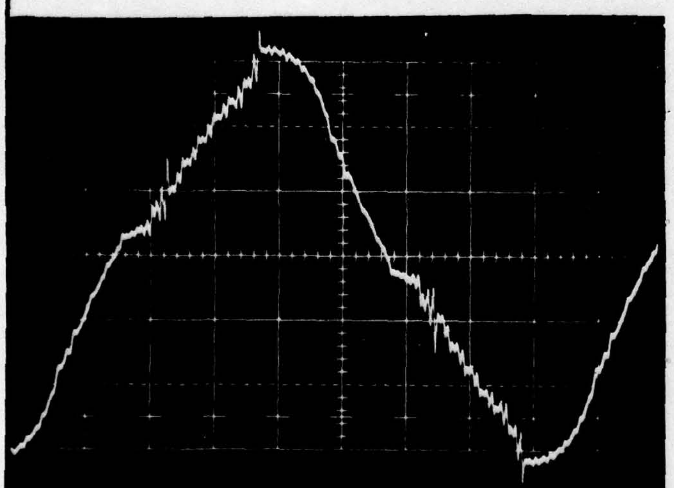
THREE PHASE SHORT CKT



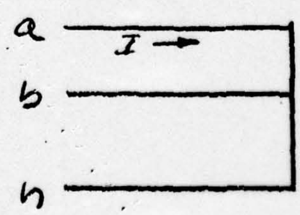
40A / DIV.
PEAK CURRENT = 100 AMPS *
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

V_{DC} = 17.5 VDC (COMM. BOOST VOLTAGE = 66 VDC, I_B = 9 AMPS. FOR ALL 60HZ SHORT CIRCUIT TESTS)

*POWER SOURCE CIRCUIT BREAKER TRIPS.



TWO PHASE SHORT CKT.



40 A / DIV.
PEAK CURRENT = 128 AMPS.

V_{DC} = 22.6 VDC

(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

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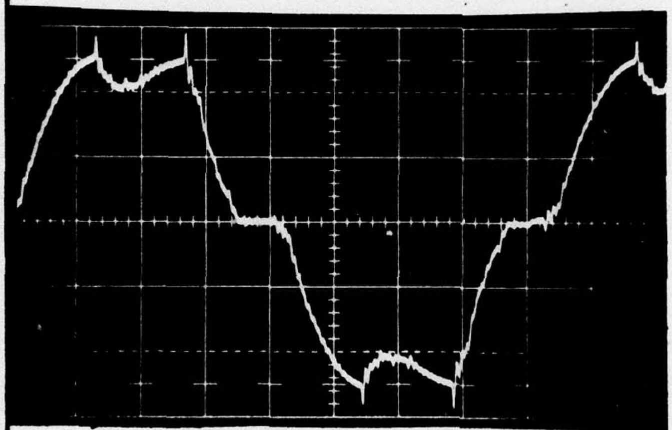
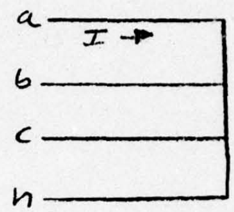
3.29.1.13 SHORT CIRCUIT

60 HZ SHORT CIRCUIT CURRENTS



V_{DC} = 17.5 VDC (COMM. BOOST VOLTAGE = 66 VDC, I_B = 9 AMPS. FOR ALL 60HZ SHORT CIRCUIT TESTS)

THREE PHASE SHORT CKT

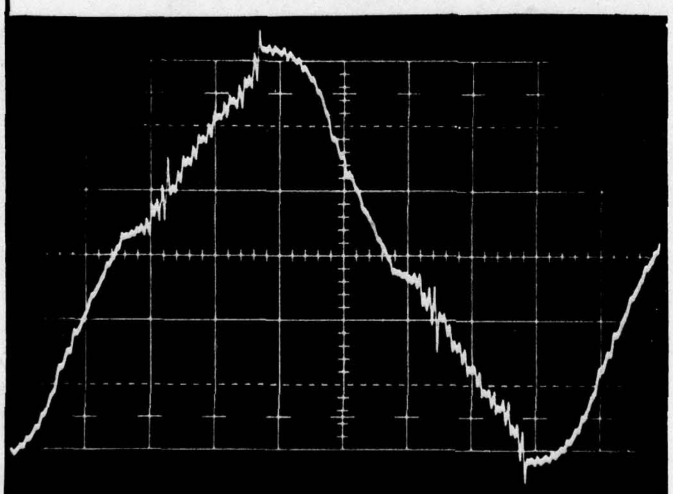


40 A / DIV.

PEAK CURRENT = 100 AMPS*

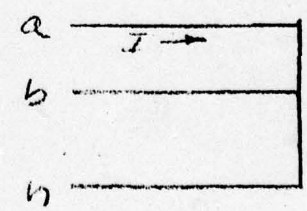
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

*POWER SOURCE CIRCUIT BREAKER TRIPS.



V_{DC} = 22.6 VDC

TWO PHASE SHORT CKT.



40 A / DIV.

PEAK CURRENT = 128 AMPS.

(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

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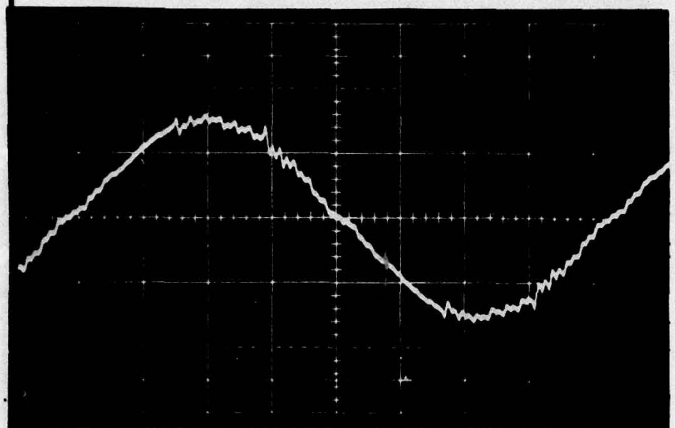
60 HZ SHORT CIRCUIT CURRENTS



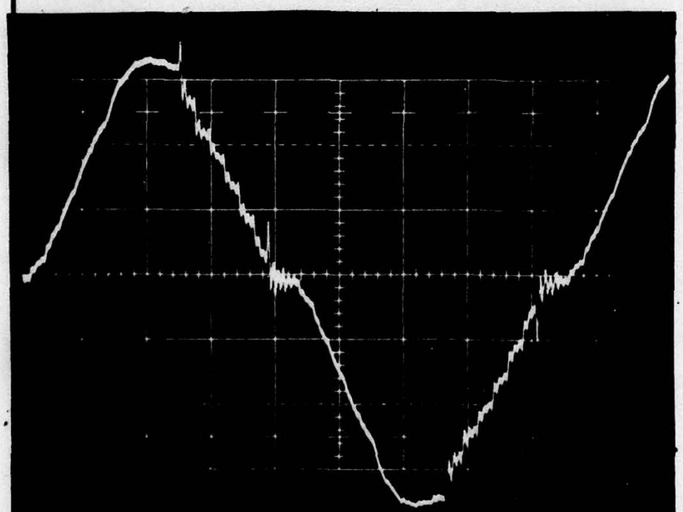
SINGLE PHASE L-T-N
SHORT CIRCUIT

a — I → — n

100 A / DIV.

PEAK CURRENT = 150 AMPS.
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

V_{DC} = 50 VDC



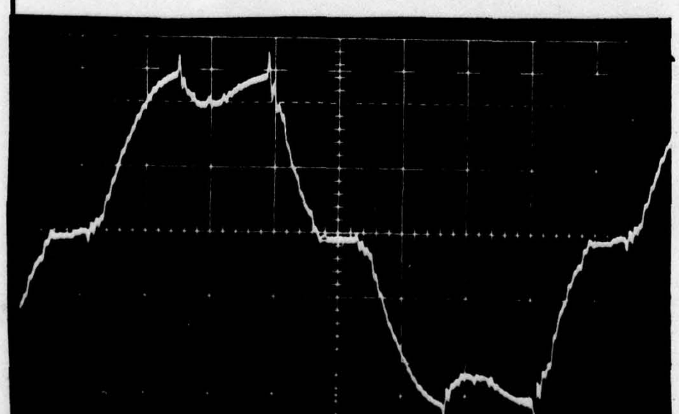
SINGLE PHASE L-T-L
SHORT CIRCUIT

a — I → — b

40 A / DIV.

PEAK CURRENT = 150 AMPS
(2 P.U. PEAK CURRENT REQUIRED FOR 3ϕ = 116.5 AMPS; FOR 1ϕ = 146 AMPS)

V_{DC} = 23.5 VDC



THREE PHASE L-T-L
SHORT CIRCUIT

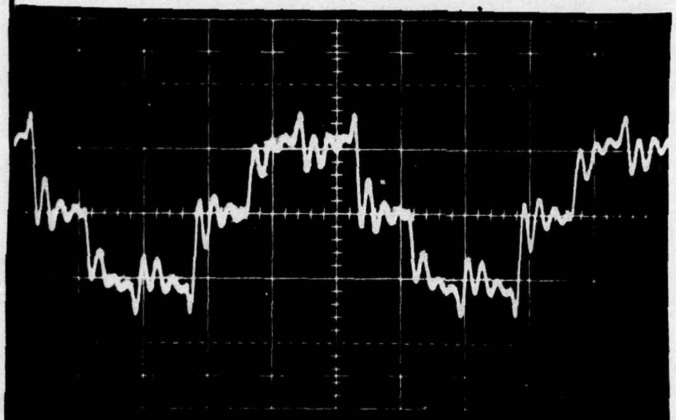
a — I → — b — c

40 A / DIV.

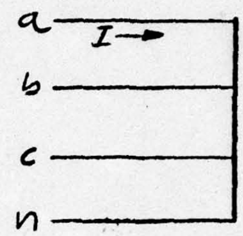
PEAK CURRENT = 100 AMPS*
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS) * POWER SOURCE BREAKER TRIPS.

DISTRIBUTION:

400 HZ SHORT CIRCUIT CURRENTS

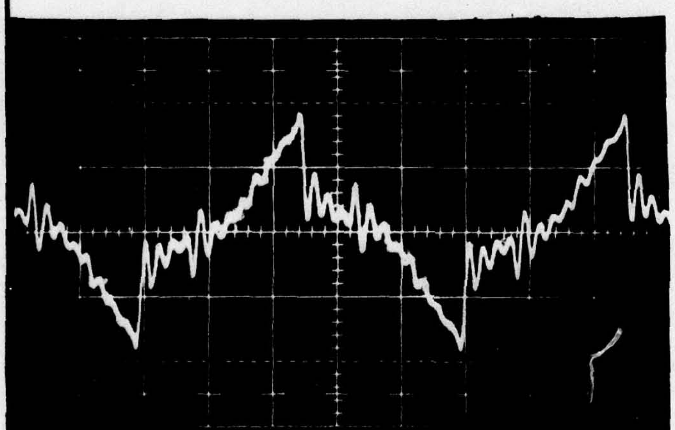


THREE PHASE SHORT CIRCUIT

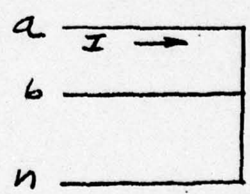


100A/DIV. 500μSEC/DIV.
PEAK CURRENT = 120 AMPS.
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

V_{DC} = 18.5VDC (COMMUTATION BOOST VOLTAGE = 72VDC, I_B = 6AMPS FOR ALL 400HZ SHORT CIRCUIT TESTS)



TWO PHASE SHORT CIRCUIT



100 A / DIV.

PEAK CURRENT = 180 AMPS.

V_{DC} = 30.9VDC

DISTRIBUTION:

(TESTS CONDUCTED WITH POWER CENTER C.T. COMMUTATION TRANSFORMER CKT)

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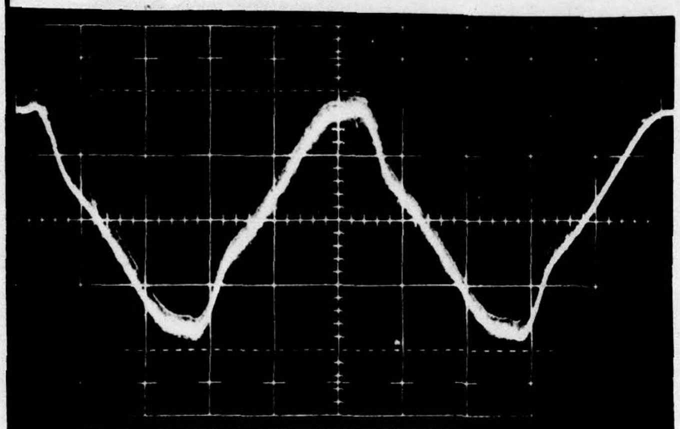
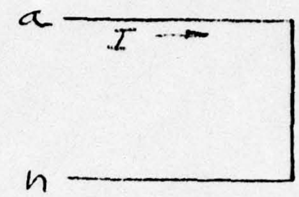
	APPROVED	

400 HZ SHORT CIRCUIT CURRENTS

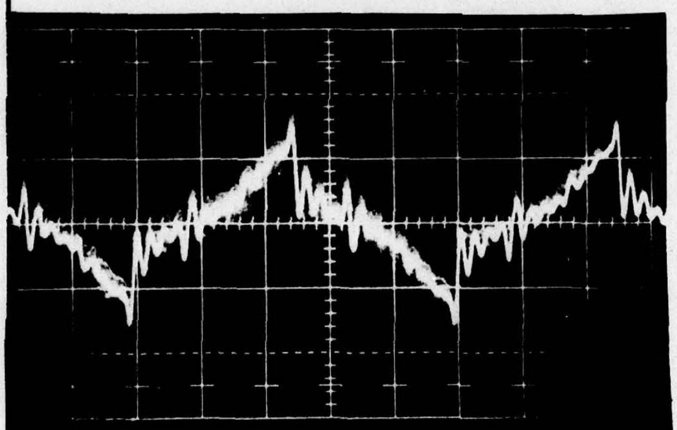


Vdc = 100VDC

SINGLE PHASE L-T-N SHORT CIRCUIT

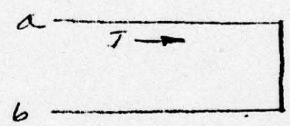


100A/DIV. 500μSEC/DIV.
PEAK CURRENT = 180 AMPS.
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

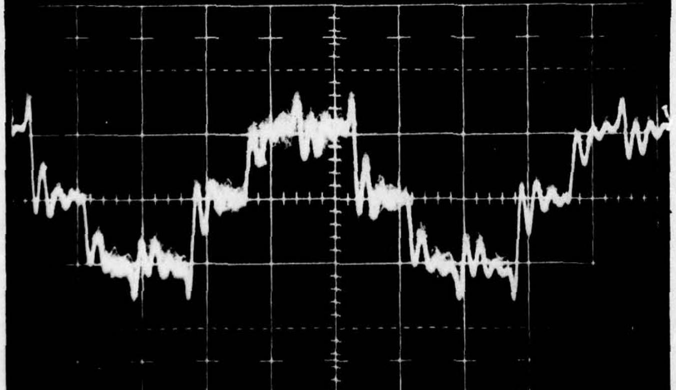


Vdc = 23VDC

SINGLE PHASE L-T-L SHORT CKT.

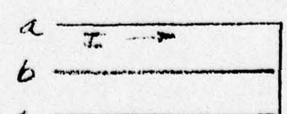


100A/DIV. 500μSEC/DIV.
PEAK CURRENT = 150 AMPS
(2 P.U. PEAK CURRENT REQUIRED FOR 3φ = 116.5 AMPS; FOR 1φ = 146 AMPS)



Vdc = 18.5VDC

THREE PHASE L-T-L SHORT CIRCUIT



100A/DIV. 500μSEC/DIV.
PEAK CURRENT = 120 AMPS.
(2 P.U. PEAK CURRENT REQUIRED = 116.5 AMPS)

DISTRIBUTION:

3.24.3 EFFICIENCY* 60HZ

OUTPUT POWER WATTS	P.F.	INPUT POWER WATTS	LOSSES WATTS	EFFICIENCY %
NO LOAD	—	1445	1445	—
2340	1.0	3435	1095	68.1
2332.8	0.8	3434	1101	67.9
6912	1.0	8047	1135	85.9
6969	0.8	8278	1309	84.2
11,520	1.0	12,725	1205	90.53
11,531	0.8	13,093	1562	88.07
16,628	1.0	18,048	1420	92.13
16,992	0.8	18,916	1924	89.8
21,600	1.0	23,122	1522	93.42
21,888	0.8	24,229	2341	90.33

* INCLUDES COMMUTATION BOOST POWER 720 WATTS
DOES NOT INCLUDE POWER TO ELECTRONICS ≈60 WATTS

DISTRIBUTION:

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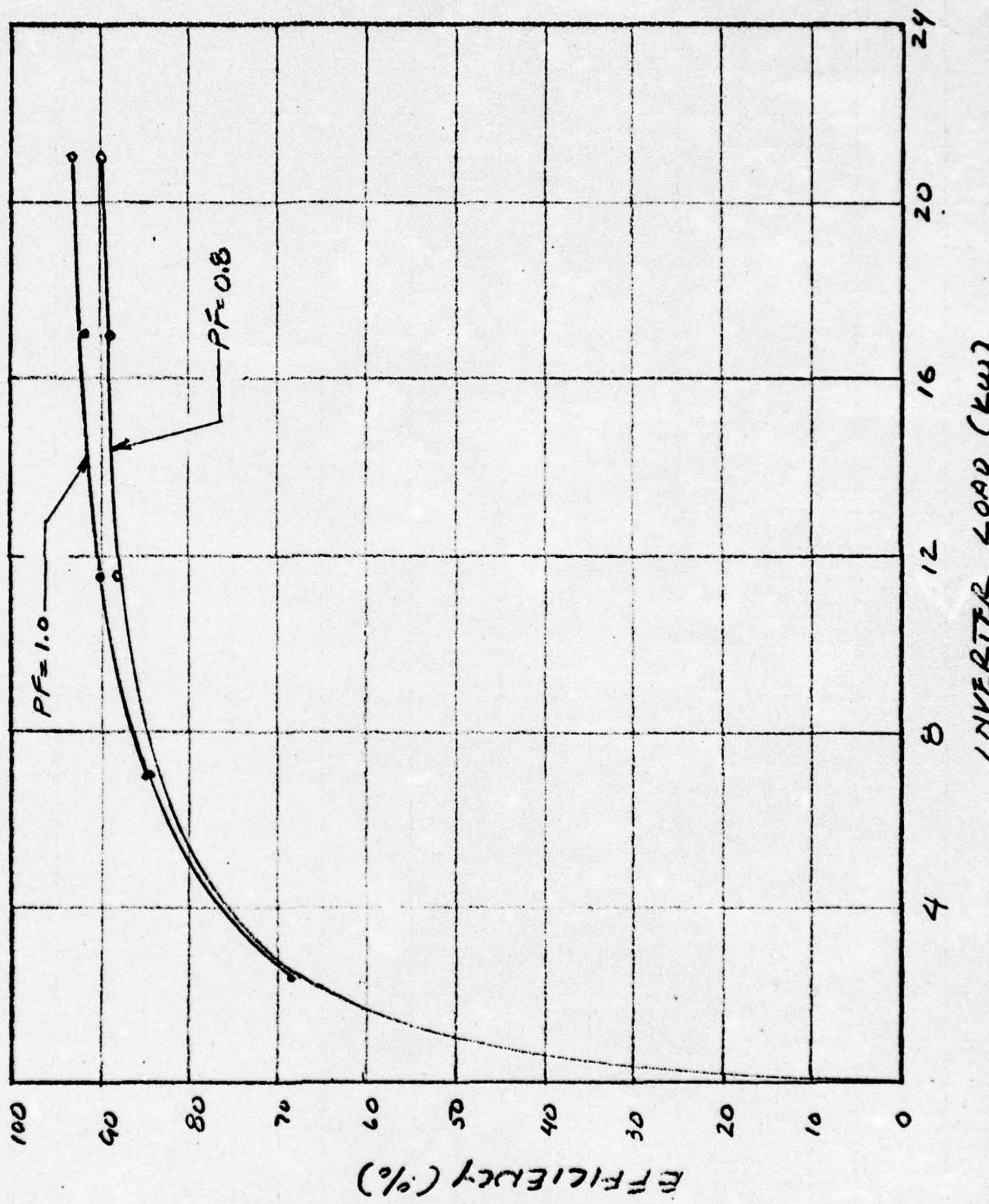
		APPROVED		

60HZ EFFICIENCY



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3.24.3 EFFICIENCY* 400 HZ

OUTPUT POWER WATTS	P.F.	INPUT POWER WATTS	LOSSES WATTS	EFFICIENCY %
NO LOAD	—	1832	1832	—
2268	1.0	4370	2102	51.9
2304	0.8	4239	1935	54.4
4486	1.0	6516	2030	68.8
4608	0.8	6392	1784	72.1
6732	1.0	8982	2250	75.0
6912	0.8	8741	1829	79.0
9720	1.0	11,300	1580	86.0
9216	0.8	10,926	1710	84.4
11,232	1.0	13,470	2238	83.4
11,462	0.8	13,157	1695	87.1
13,464	1.0	15,893	2429	84.7
13,766	0.8	15,709	1943	87.6
16,560	1.0	19,120	2560	86.6
16,876	0.8	18,784	1908	90.0
20,880	1.0	23,805	2925	87.7
21,600	0.8	23,865	2265	90.5
23,400	1.0	26,162	2762	89.4
23,731	0.8	26,236	2505	90.5

* INCLUDES COMMUTATION BOOST POWER 432 WATTS.
DOES NOT INCLUDE POWER TO ELECTRONICS ≈ 60 WATTS.

DISTRIBUTION:

DE-255 REV. 12-66

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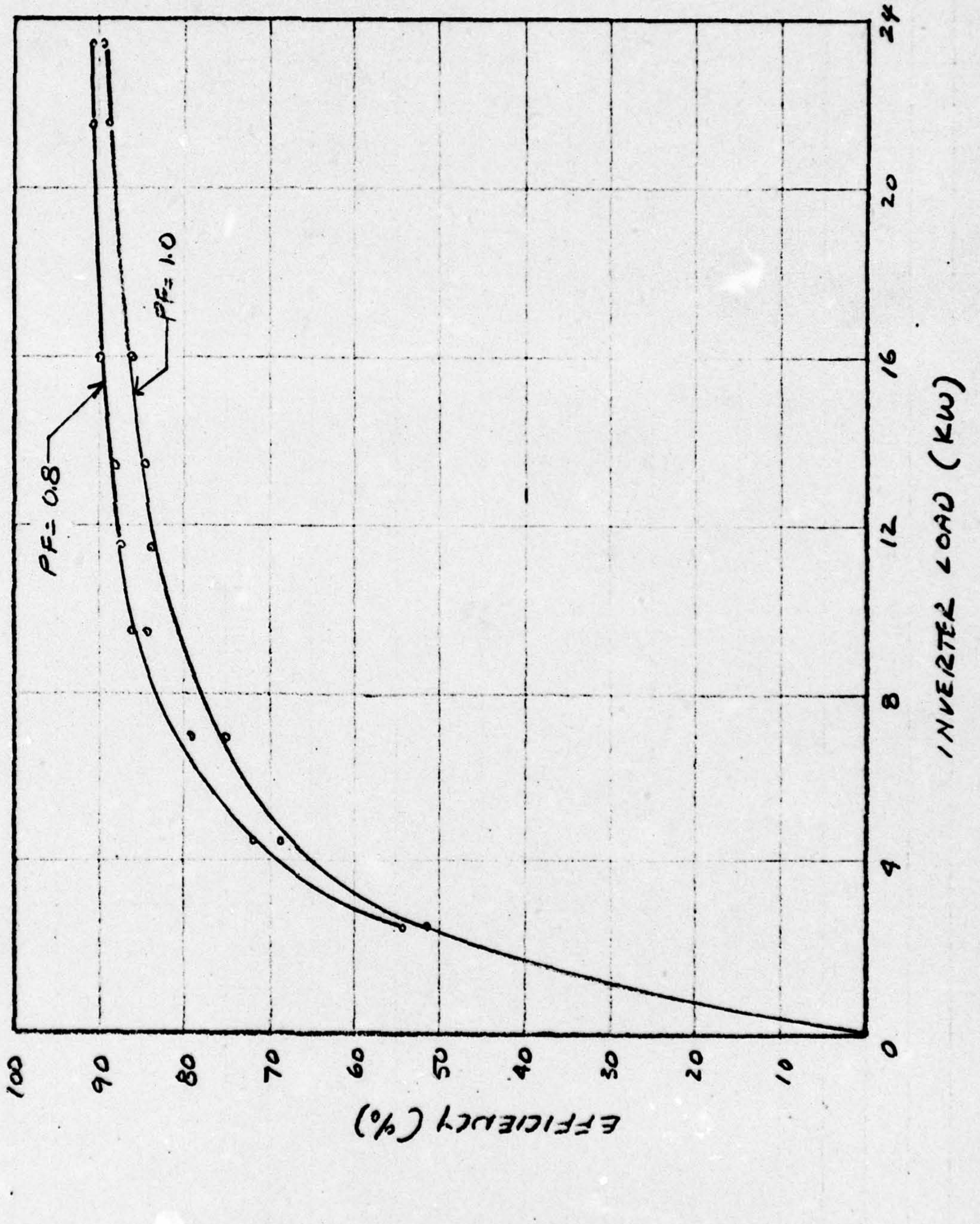
CHECKED

APPROVED

400HZ EFFICIENCY



DISTRIBUTION:

DE-255 REV. 12-65

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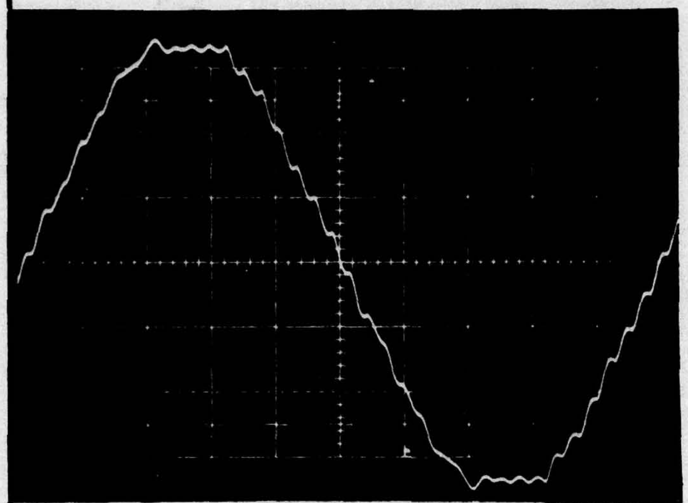
		APPROVED		

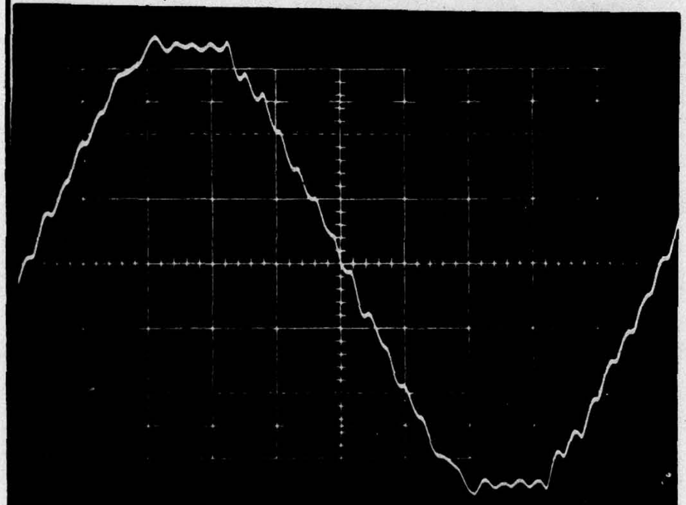


60HZ SINGLE PHASE
THREE WIRE

NO LOAD

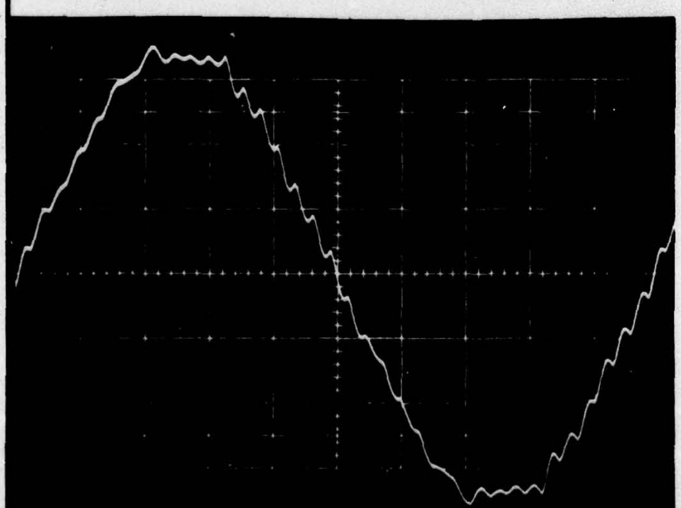
LINE-TO-LINE VOLTAGE
100V/DIV.

THD = 3.68%



10Kw, PF = 1.0 LOAD

THD = 3.75%



10Kw, PF = 0.8 LOAD

THD = 4.1%

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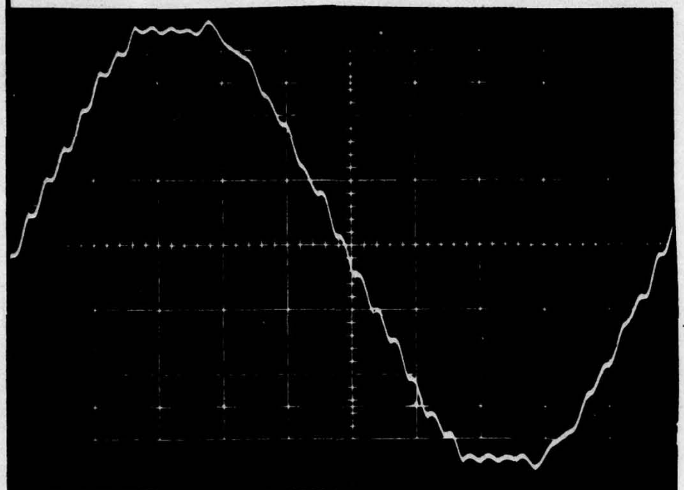
		APPROVED		

3.24.1.3 VOLTAGE WAVEFORM



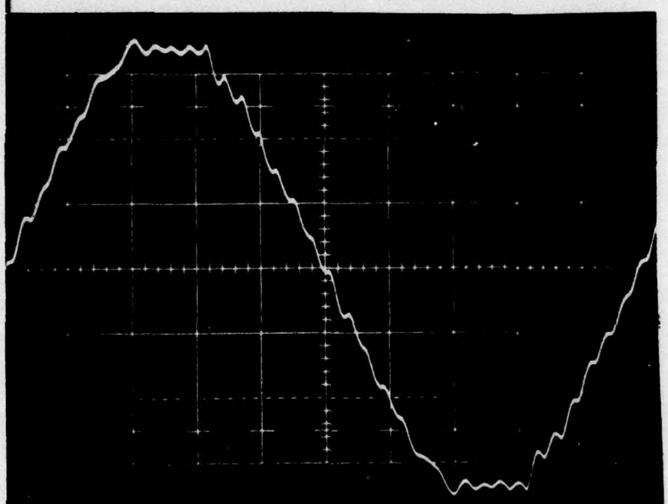
60 HZ SINGLE PHASE
TWO WIRE

NO LOAD

THD = 3.6%

50V/DIV.

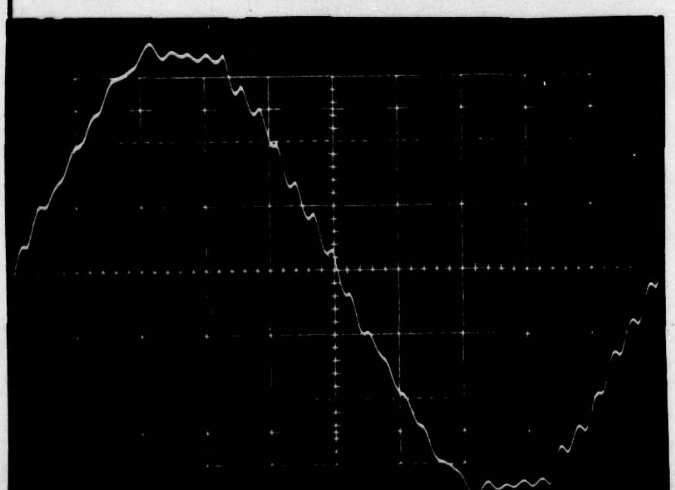
V_{DC} = 270 VDC



10KW, PF = 1.0 LOAD

THD = 3.75%

V_{DC} = 295 VDC



10KW, PF = 0.8 LOAD

THD = 4.0%

V_{DC} = 295 VDC

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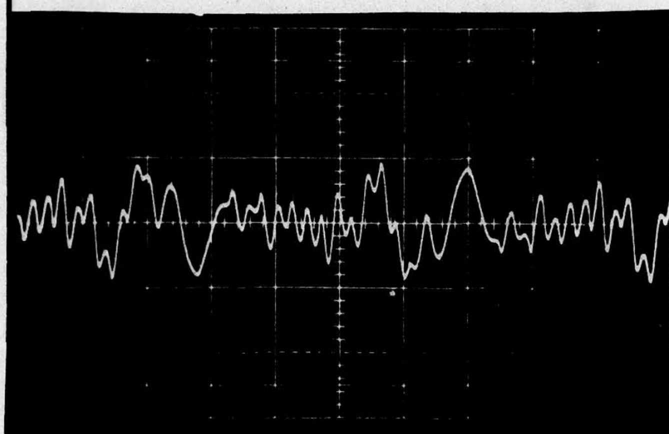
DEVIATION FACTOR

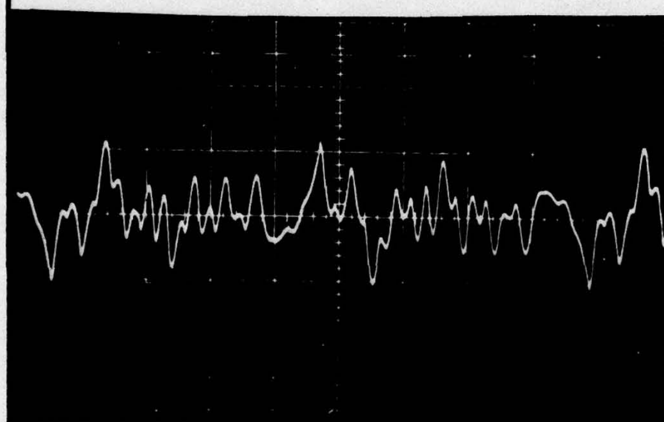
60 HZ SINGLE PHASE

120 V RMS

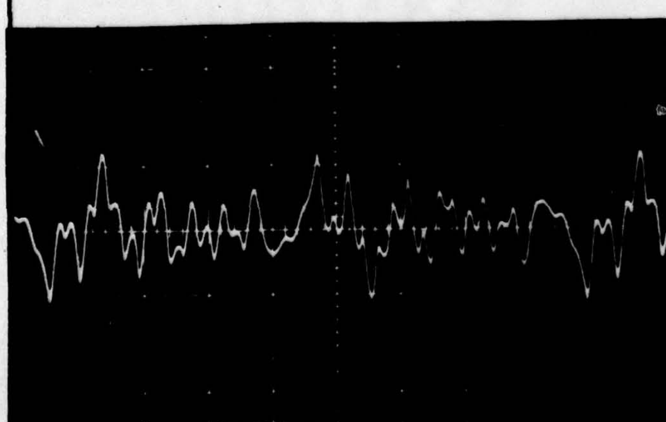


OUTPUT OF 60 HZ NOTCH FILTER 10V/DIV. 2 ms/DIV.

NO LOAD



10 KW, PF = 1.0 LOAD



10 KW, PF = 0.8 LOAD

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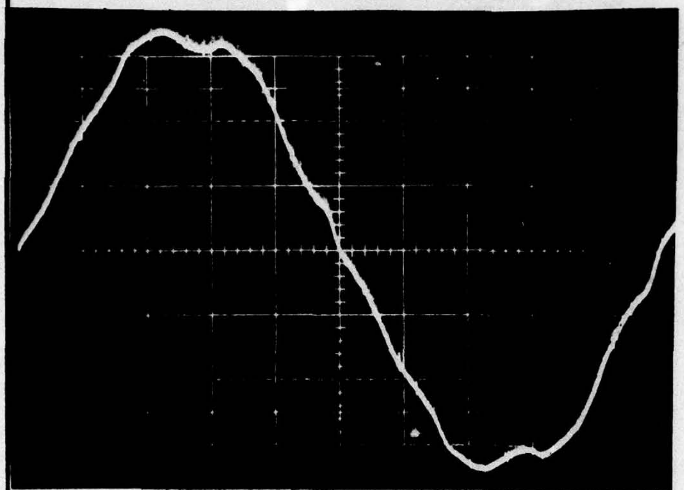
3.24.1.3 VOLTAGE WAVEFORM

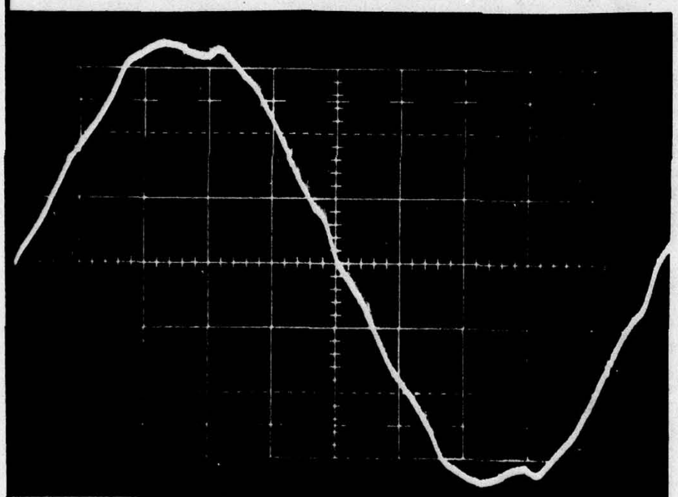


400 HZ SINGLE PHASE
TWO WIRE

NO LOAD

THD= 4.4%

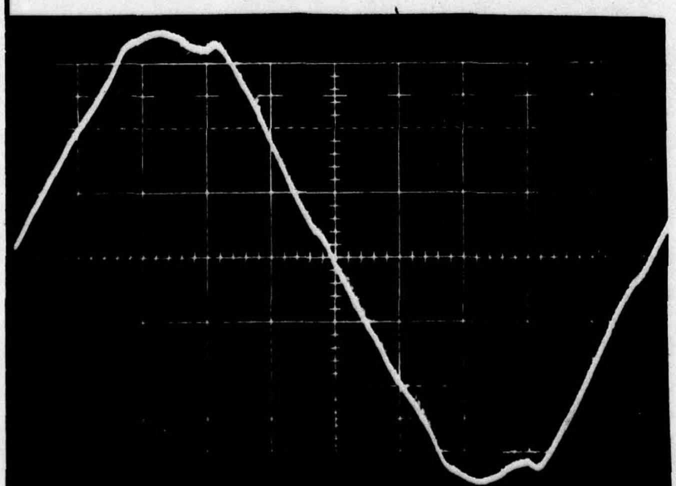
50V/DIV.
VDC= 270 VDC



10 KW, PF= 1.0 LOAD

THD= 3.2%.

VDC= 280 VDC



10 KW, PF= 0.8 LOAD

THD= 4.7%

VDC= 293 VDC.

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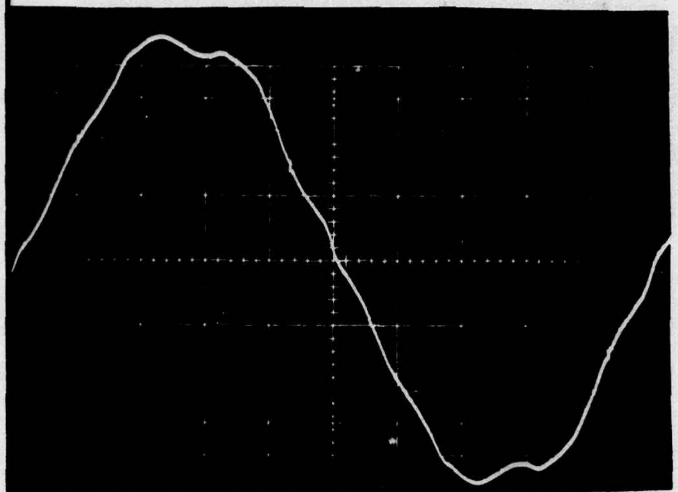
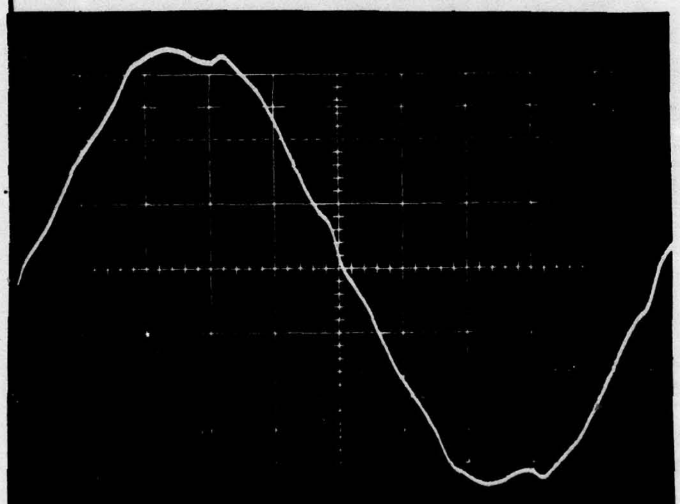


400HZ SINGLE PHASE
THREE WIRE

NO LOAD

THD= 4.4%

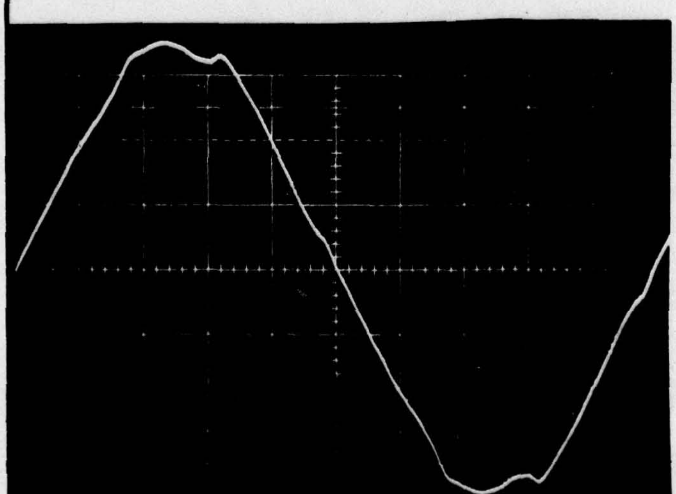
V_{DC}= 273VDC



10KW, PF=1.0 LOAD

THD= 3.4%

V_{DC}= 287VDC



10KW, PF=0.8 LOAD

THD= 3.9%

V_{DC}= 298VDC.

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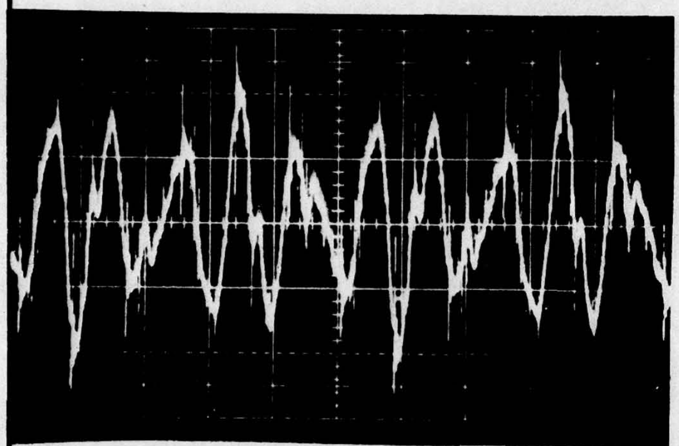
DEVIATION FACTOR

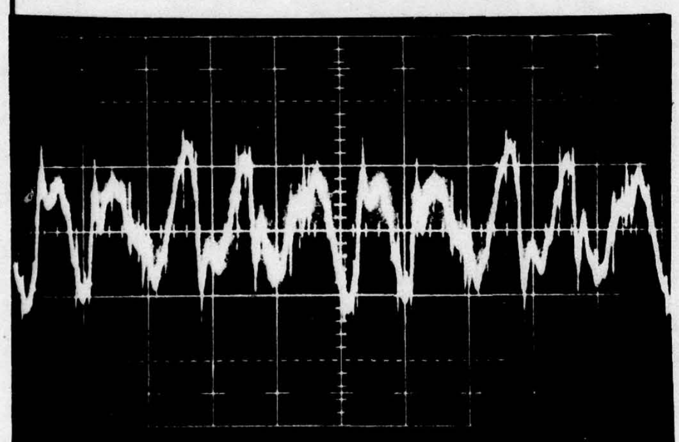


400 HZ SINGLE PHASE
TWO WIRE

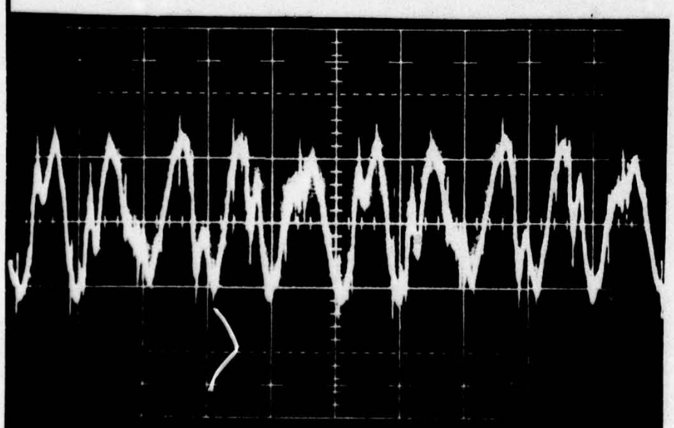
NO LOAD

0.5V/DIV.

500 μSEC/DIV.



10KW, PF= 0.8 LOAD



10KW, PF= 1.0 LOAD

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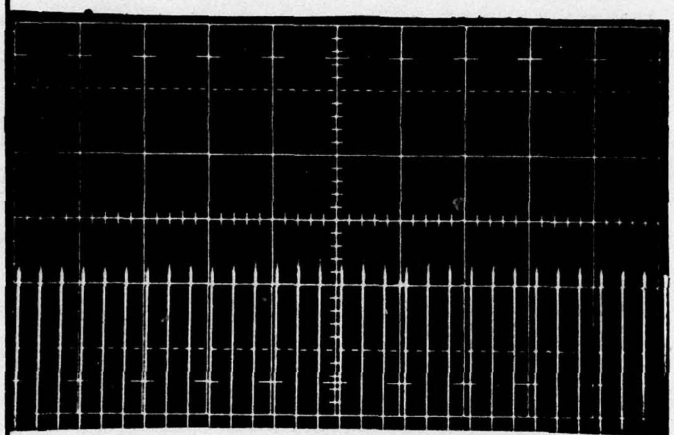
3.24.1.7 VOLTAGE MODULATION

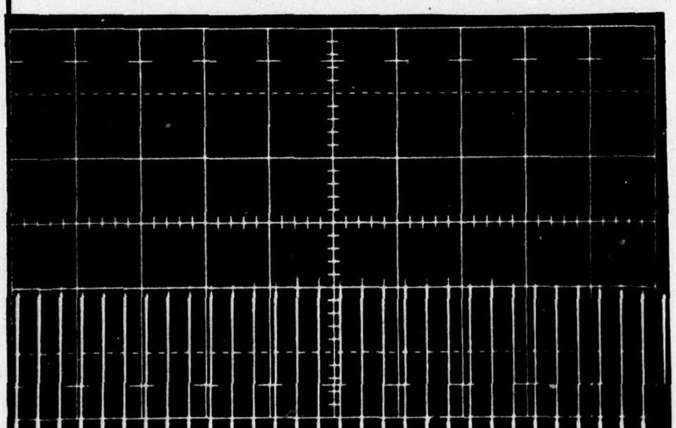
60HZ SINGLE PHASE
TWO WIRE



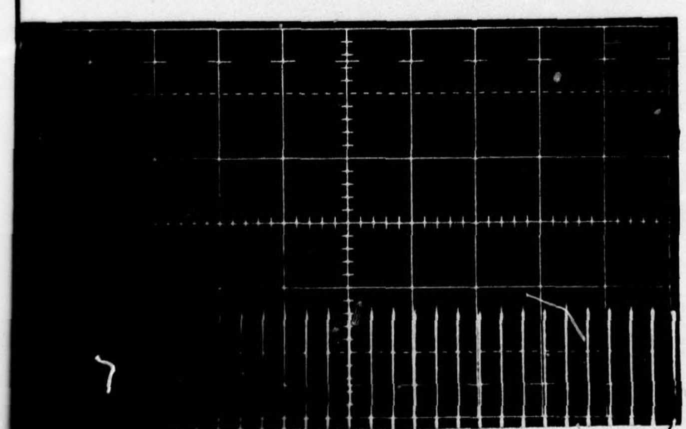
NO LOAD

2V/DIV.

50MS/DIV.



10KW, PF=1.0



10KW, PF=0.8

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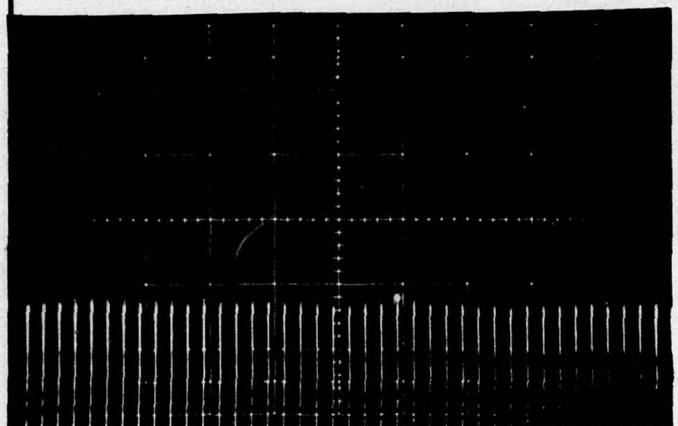
VOLTAGE MODULATION

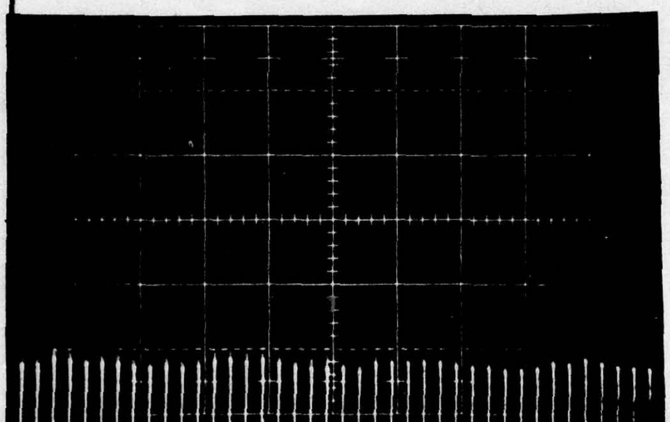
400 HZ SINGLE PHASE
TWO WIRE



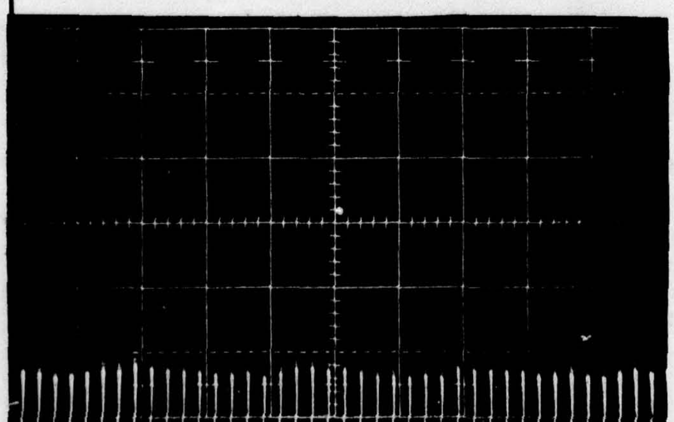
NO LOAD

2V/DIV.

10MS/DIV.



10KW, PF=1.0



10KW, PF=0.8

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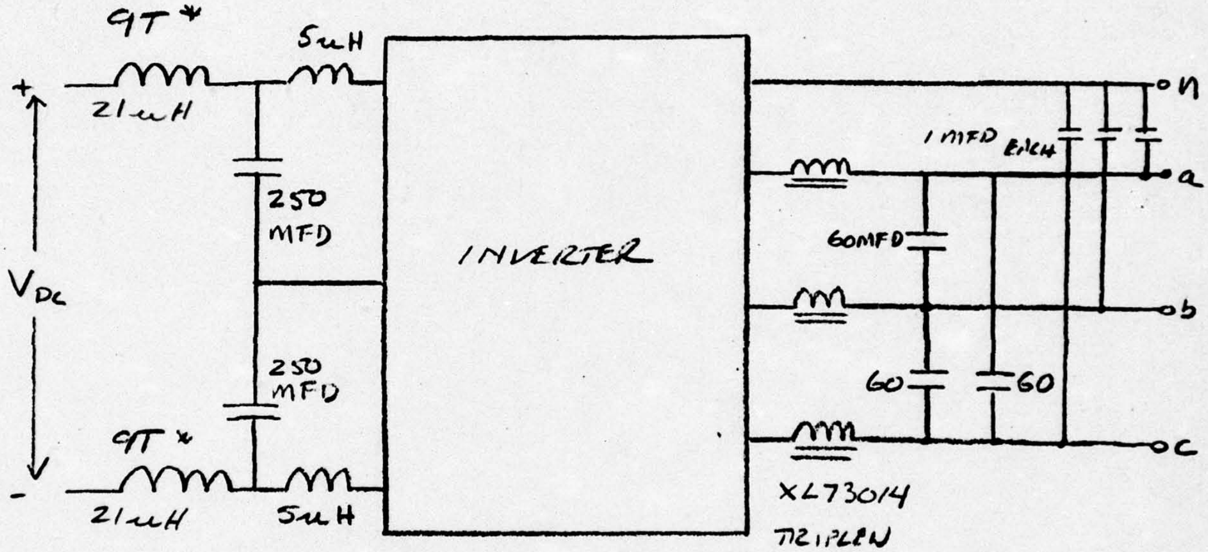
EXPERIMENT TO STUDY THE INFLUENCE OF THE INVERTER INPUT FILTER ON THE OUTPUT WAVEFORM. 400 HZ, THREE PHASE



* E 55-55106-D4 CORE

(V_{BOOST} = 72 VDC ; I_B = 6 AMPS. C.T. COMMUTATION TRANSFORMER USED FOR FULLER CENTER COMMUTATION)

(NOTE: TWO WIRE INPUT COMPARED TO THREE WIRE INPUT FOR DATA ON PAGES 73-76)

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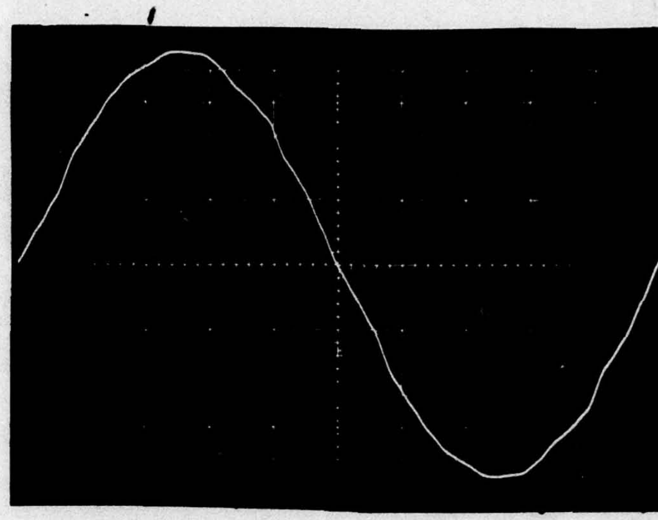
3.24.13 VOLTAGE WAVEFORM
400HZ, THREE PHASE
NO LOAD

L-T-N VOLTAGES

Van

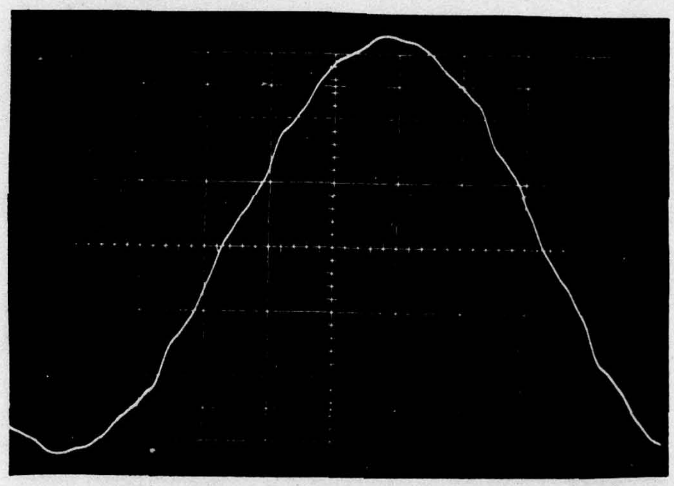
THD= 2.0%

50V/DIV.



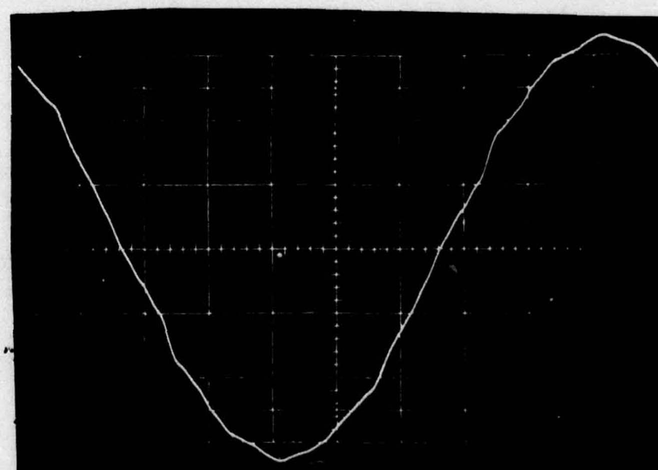
Vbn

THD= 2.5%



Vcn

THD= 2.2%



COMPARE WITH PAGE 73

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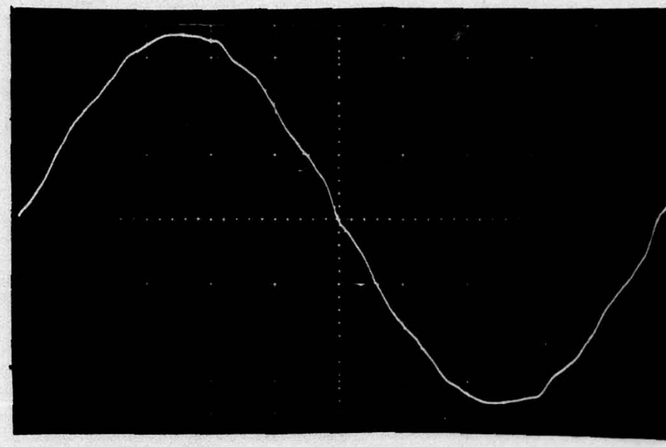
400 HZ, THREE PHASE
LINE-TO-LINE VOLTAGES
<u>NO LOAD</u>

V_{ab}

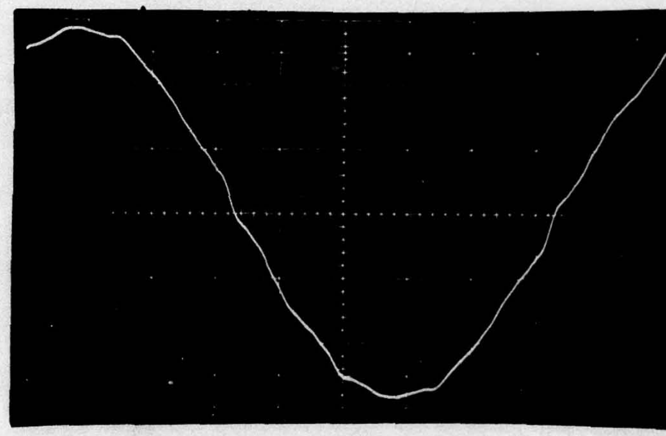
THD= 2.1%

100V/DIV.



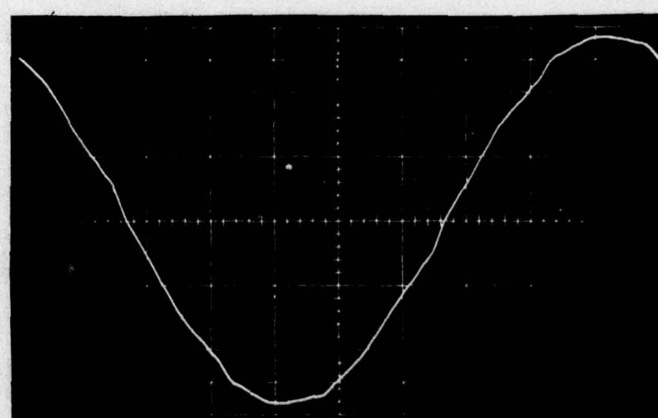
V_{bc}

THD= 2.4%



V_{ca}

THD= 2.1%



COMPARE WITH PAGE 79

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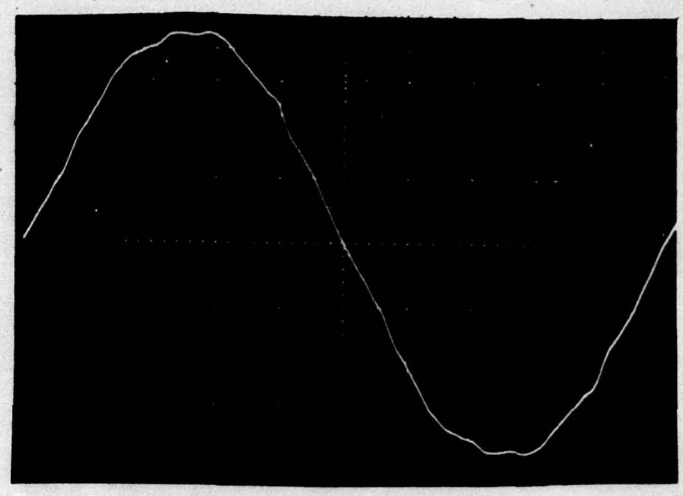
		APPROVED		

400 HZ, THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

11KW, PF = 1.0 LOAD

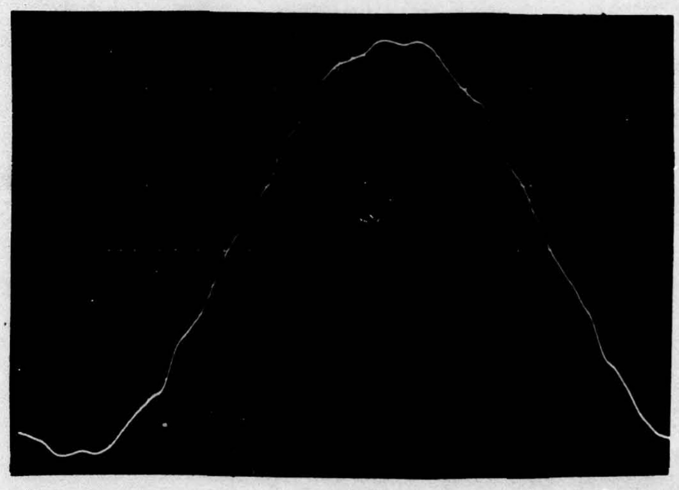
Van

THD = 2.5%



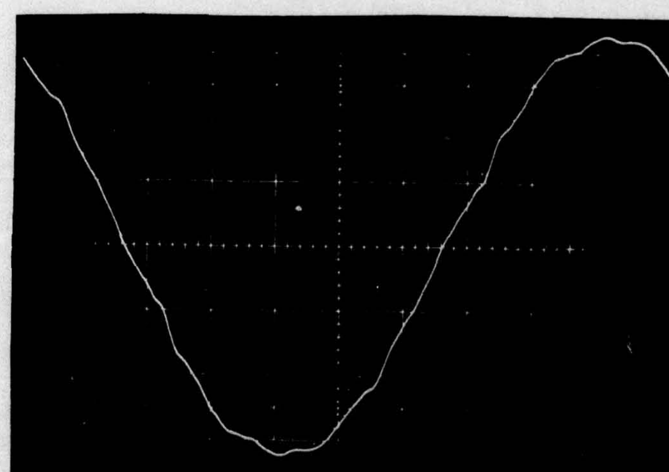
Vbn

THD = 2.95%



Vcn

THD = 2.55%



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		APPROVED		

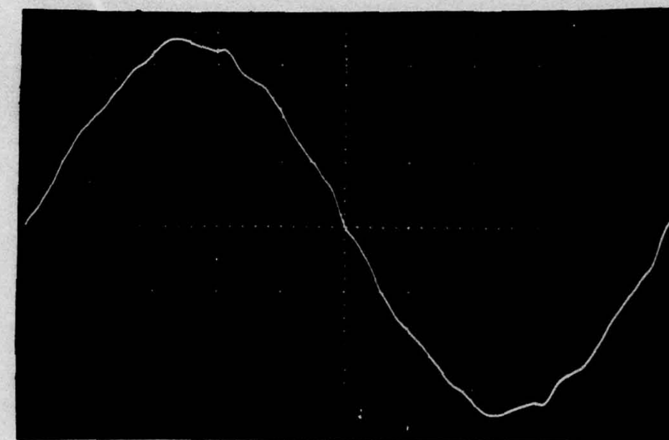
400 HZ, THREE PHASE
LINE-TO-LINE VOLTAGES

11KW, PF=1.0 LOAD

Vab

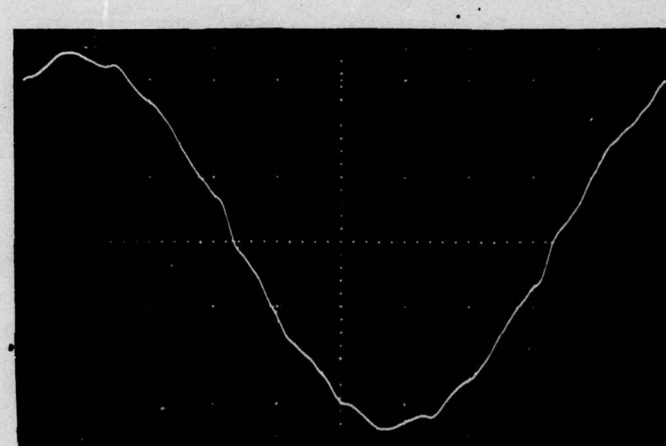
THD= 2.5%

100V/DIV.



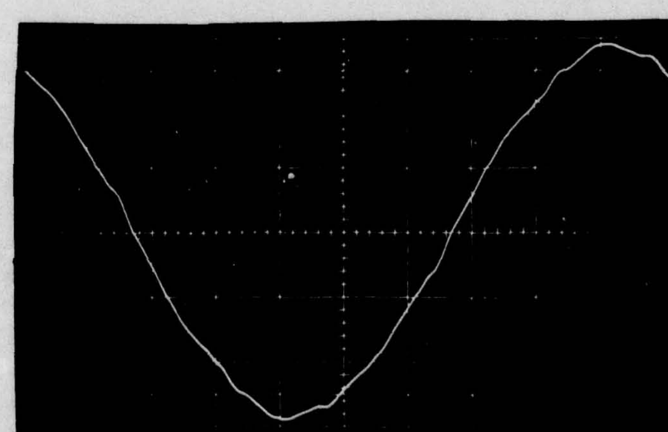
Vbc

THD=2.9%



Vca

THD=2.55%



DISTRIBUTION:

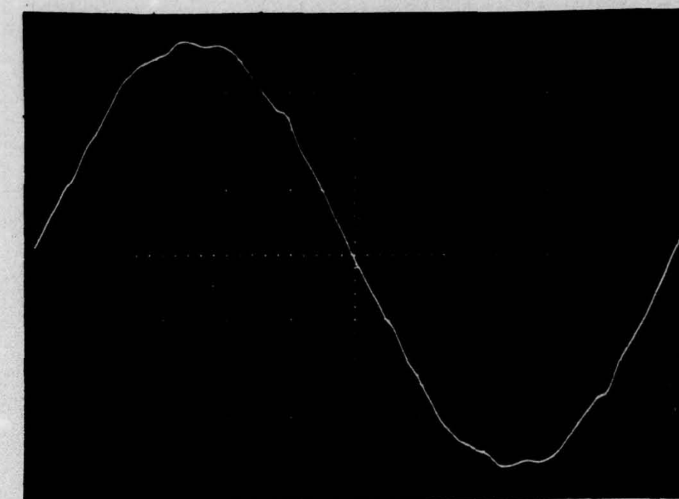
400 HZ, THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

<u>11KW, PF=0.8 LOAD</u>

Van

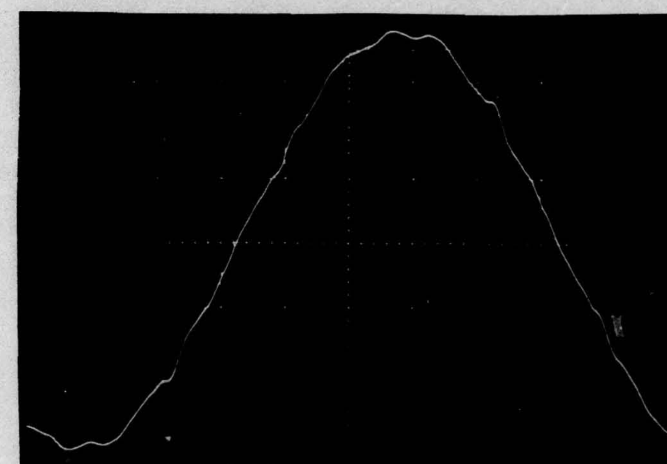
THD= 2.2%

50V/DIV.



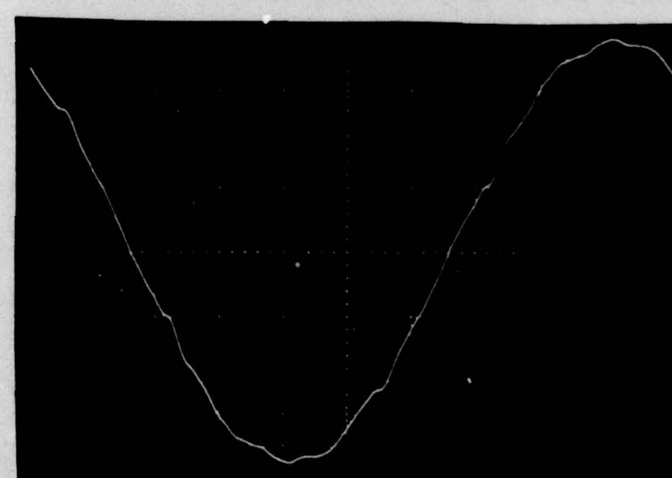
Vbn

THD= 2.6%



Vcn

THD= 2.3%



COMPARE WITH PAGE 119

DISTRIBUTION:

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 118
TITLE			PREPARED CORR-1	DATE 12/9/79
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			APPROVED	

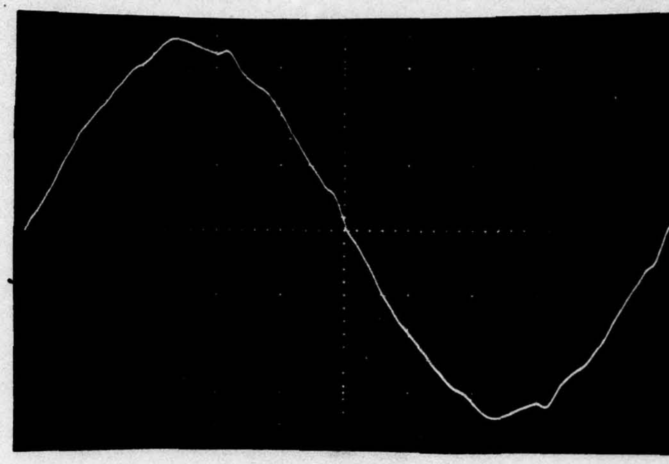
400 HZ, THREE PHASE
LINE-TO-LINE VOLTAGE

11KW, PF=0.8 LOAD

V_{ab}

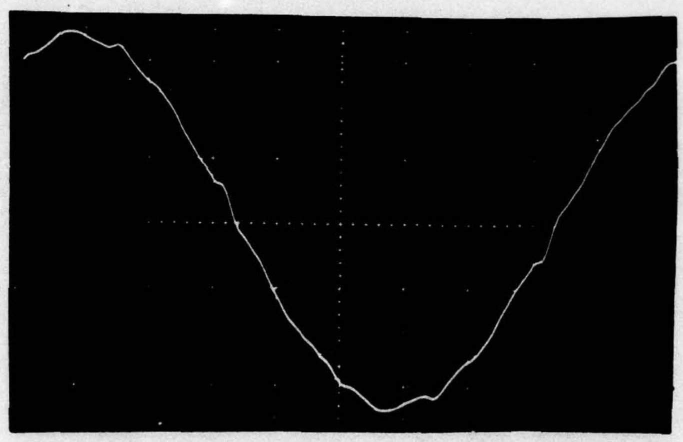
THD=2.2%

100V/DIV.



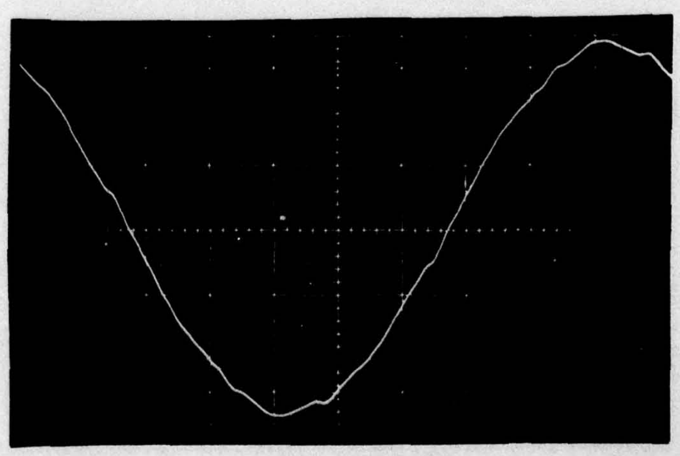
V_{bc}

THD= 2.6%



V_{ca}

THD= 2.3%



DISTRIBUTION:

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 119
TITLE V_{BOOST} REDUCED TO 20 VOLTS; I_B = 2 AMPS FOR THIS TEST.		PREPARED	CORRY	DATE 12/9/74
		CHECKED		
		APPROVED		

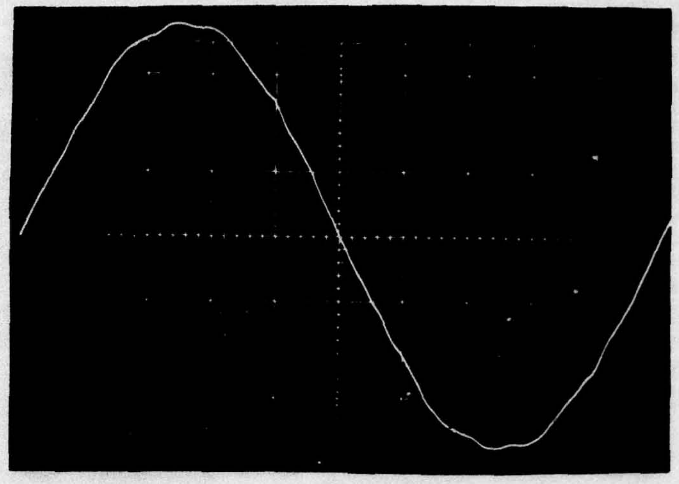
400HZ, THREE PHASE LINE-TO-NEUTRAL VOLTAGES

<u>11KW, PF=0.8 LOAD</u>

Van

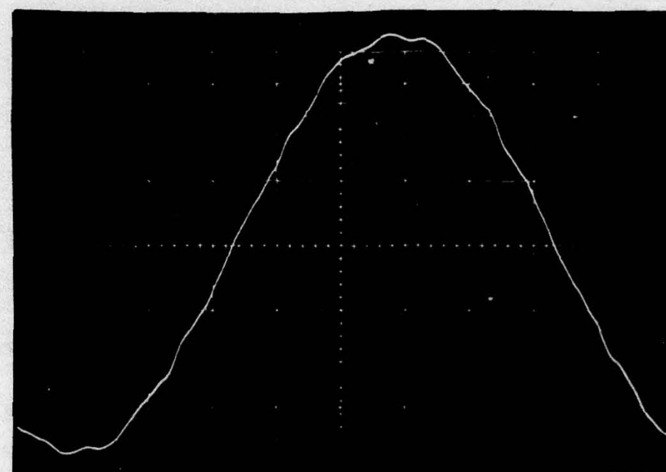
THD= 1.7%

50V/DIV.



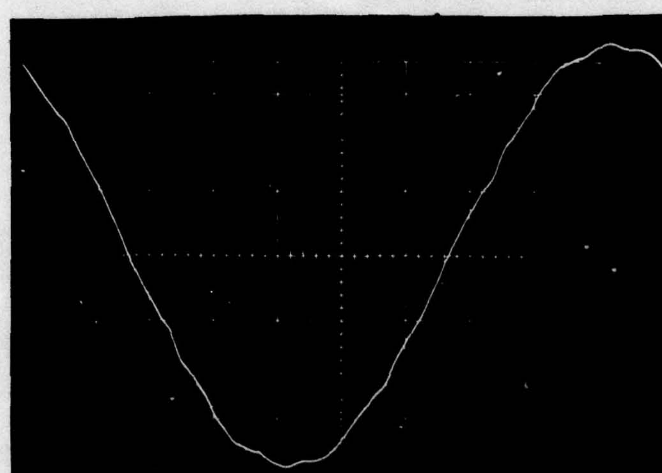
Vbn

THD= 2%



Ven

THD= 1.9%



COMPARE WITH PAGE 117

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DELCO ELECTRONICS
GENERAL MOTORS CORPORATION

REPORT NO.	PAGE	JOB NO.	PAGE
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TITLE

PREPARED: CORRY DATE: 12/9/74
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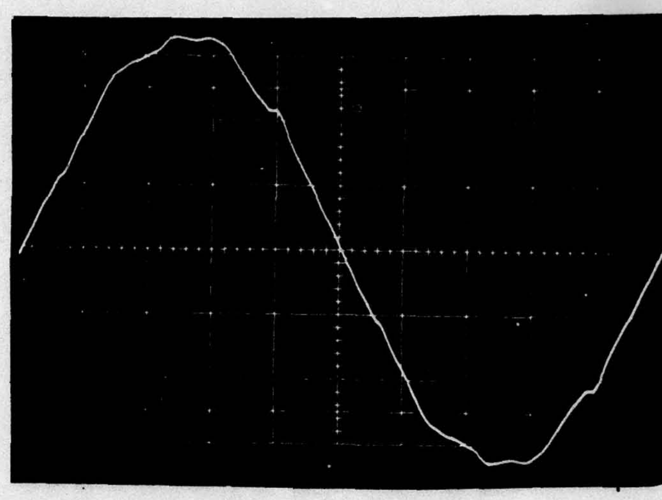
400 HZ, THREE PHASE
LINE-TO-NEUTRAL VOLTAGES

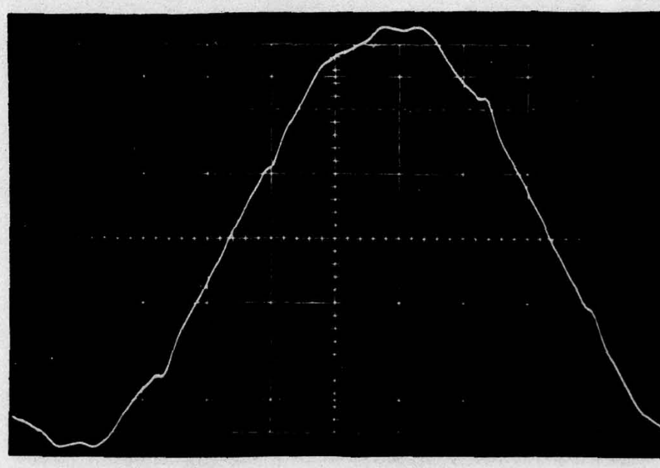
16KW, PF=0.8 LOAD



Van

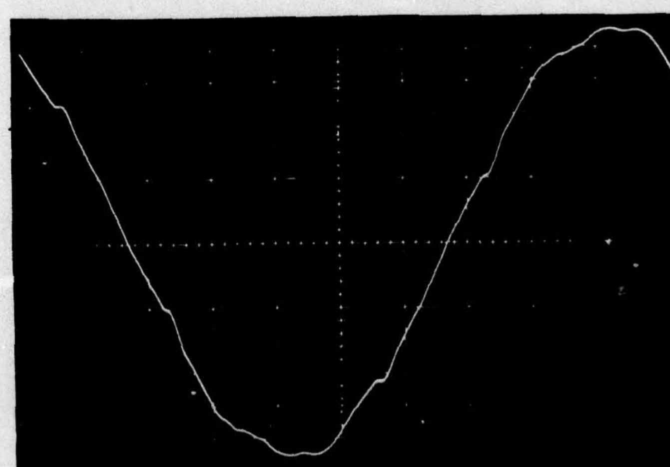
THD= 2.8%

50V/DIV.



Vbn

THD= 3.1%



Vcn

THD= 3.1%

COMPARE WITH PAGE 75

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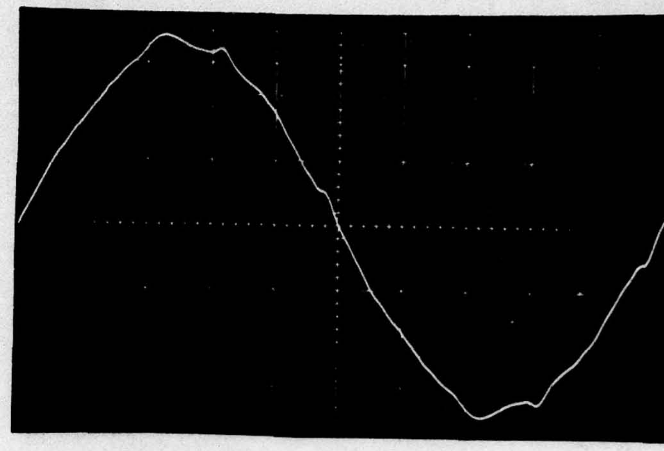
400 HZ, THREE PHASE
LINE-TO-LINE VOLTAGES

<u>16KW, PF=0.8 LOAD</u>

Vab

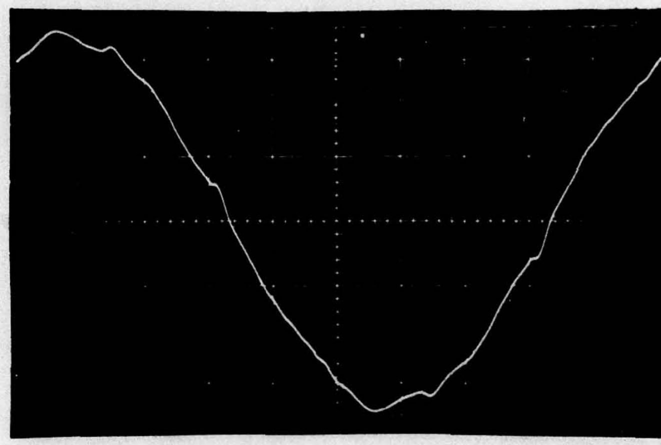
THD= 2.8%

100V/DIV.



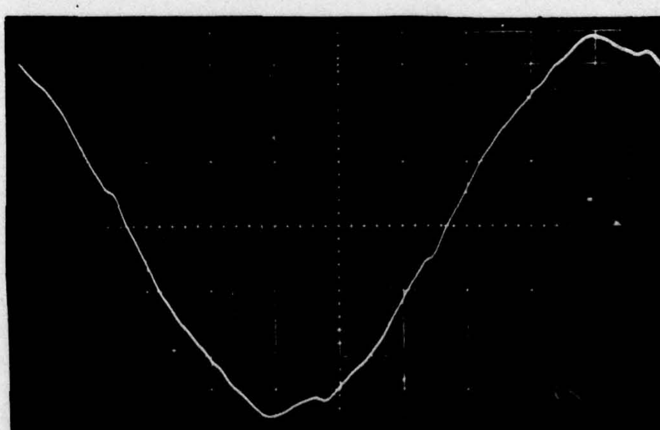
Vbc

THD= 3.1%



Vcn

THD= 3.1%



COMPARE WITH PAGE 76

DISTRIBUTION:

MEASUREMENTS OF INDIVIDUAL HARMONICS

400 HZ THREE PHASE NO LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL L-T-N	PERCENT OF FUNDAMENTAL L-T-L
1	400	100.0	100.0
5	2000	0.48	0.43
7	2800	0.98	0.80
11	4400	0.88	1.10
13	5200	0.93	0.43
17	6800	0.25	0.33
19	7600	0.33	0.44
23	9200	0.27	0.32
25	10,000	0.22	0.27
29	11,600	0.15	0.18
35	14,000	0.23	0.26
37	14,800	0.10	0.10

MEASURED THD = 2.0%

WAVEFORMS ON PAGES 113 & 114

DISTRIBUTION:

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 123
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		APPROVED		

MEASUREMENTS OF INDIVIDUAL HARMONICS

400 HZ THREE PHASE   11KW, PF= 1.0 LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL L-T-N	PERCENT OF FUNDAMENTAL L-T-L
1	400	100.0	100.0
5	2000	1.50	1.45
7	2800	1.20	1.10
11	4400	0.41	1.60
13	5200	1.01	1.60
17	6800	0.24	0.35
19	7600	0.47	0.66
23	9200	0.30	0.40
25	10,000	0.24	0.32
29	11,600	0.16	0.21
35	14,000	0.25	0.24
37	14,800	0.11	0.11

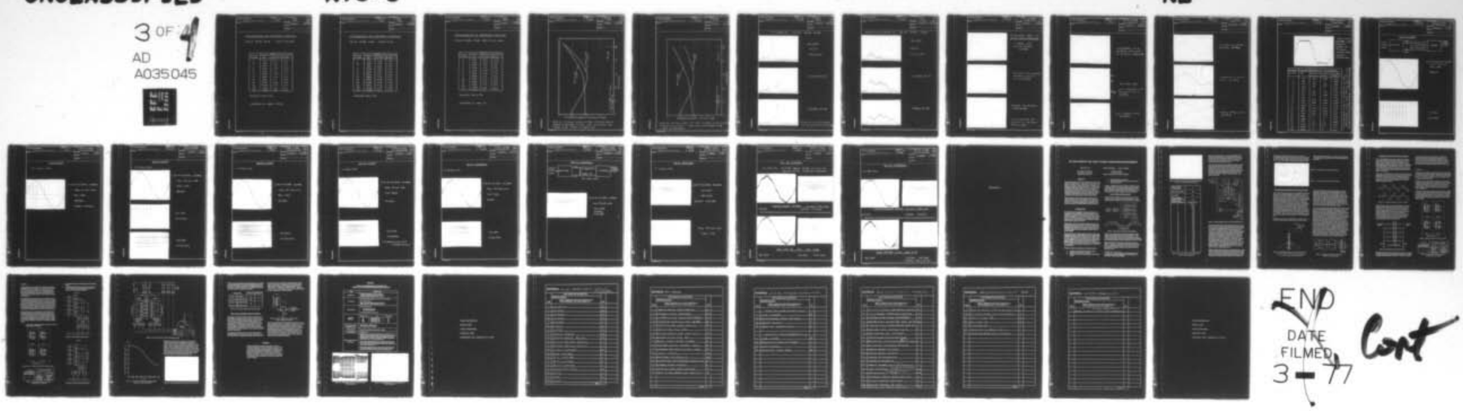
MEASURED THD = 2.5%

WAVEFORMS ON PAGES 115 & 116

DISTRIBUTION:

AD-A035 045 GENERAL MOTORS CORP GOLETA CALIF DELCO ELECTRONICS DIV F/G 9/5
FREQUENCY CONVERTER PORTABLE, ALTERNATING CURRENT MULTIFREQUENC--ETC(U)
JAN 75 T CORRY DAAK02-72-C-0210
UNCLASSIFIED R75-3 NL

3 OF 4
AD
A035045



END
DATE
FILMED
3-77

TITLE

PREPARED CORRY DATE 12/9/74
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MEASUREMENTS OF INDIVIDUAL HARMONICS

400 HZ THREE PHASE 11KW, PF=0.8 LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL	
		L-T-N	L-T-L
1	400	100.0	100.0
5	2000	0.70	0.73
7	2800	1.20	1.10
11	4400	0.80	0.80
13	5200	1.00	1.35
17	6800	0.25	0.31
19	7600	0.52	0.70
23	9200	0.31	0.39
25	10,000	0.26	0.35
29	11,600	0.20	0.23
35	14,000	0.27	0.31
37	14,800	0.12	0.12

MEASURED THD = 2.2%

WAVEFORMS ON PAGES 117 & 118

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DELCO ELECTRONICS
GENERAL MOTORS CORPORATION

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TITLE

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MEASUREMENTS OF INDIVIDUAL HARMONICS

400 HZ THREE PHASE 16 KW, PF=1.0

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL L-T-N	PERCENT OF FUNDAMENTAL L-T-L
1	400	100.0	100.0
5	2000	1.48	1.35
7	2800	2.00	1.95
11	4400	0.89	1.00
13	5200	0.85	1.30
17	6800	0.34	0.46
19	7600	0.46	0.67
23	9200	0.32	0.41
25	10,000	0.26	0.36
29	11,600	0.18	0.23
35	14,000	0.25	0.30
37	14,800	0.13	0.13

MEASURED THD = 3.1%

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 12
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		APPROVED		

MEASUREMENTS OF INDIVIDUAL HARMONICS

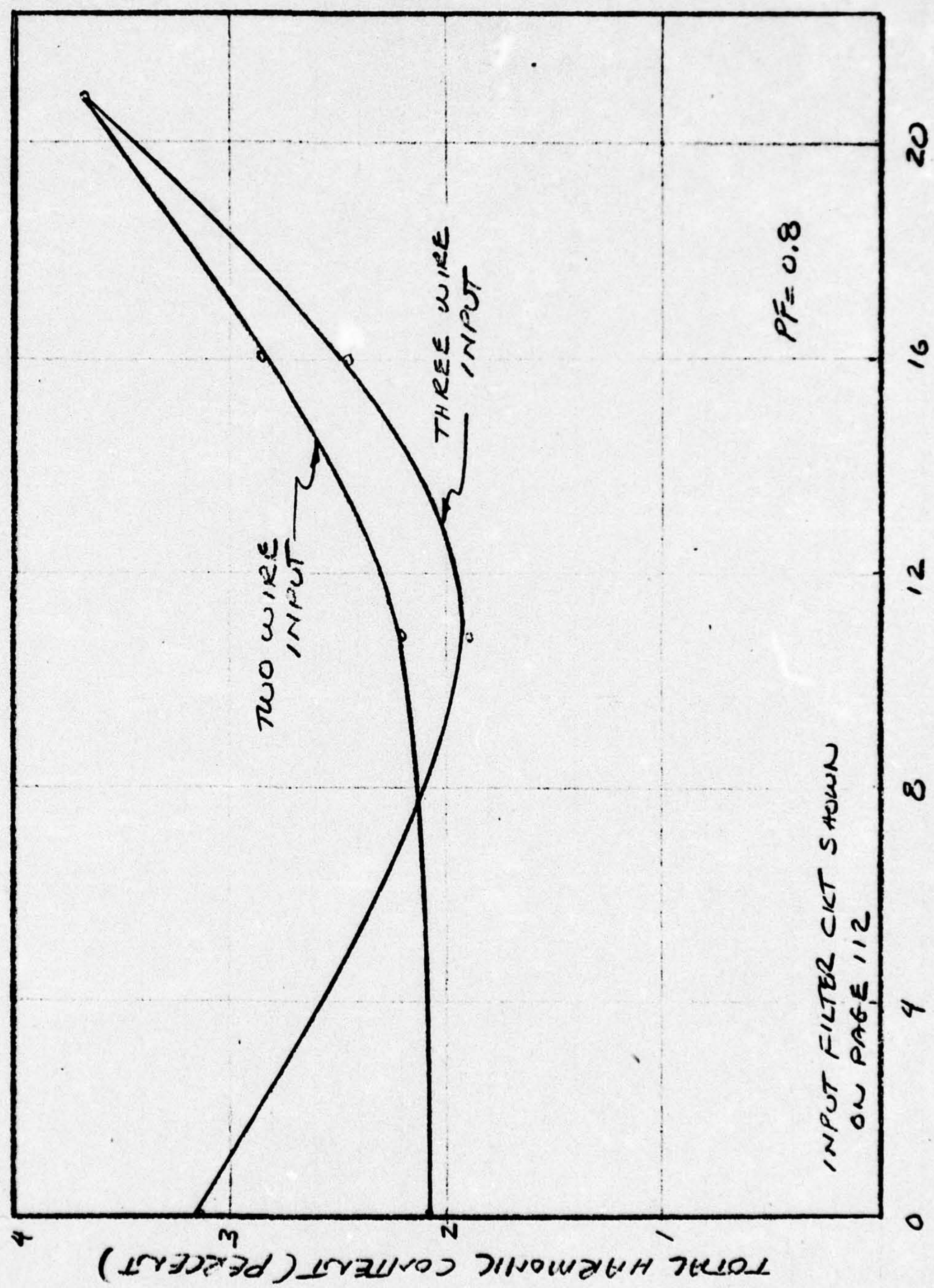
400 HZ THREE PHASE 16KW, PF-0.8 LOAD

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL	
		L-T-N	L-T-L
1	400	100.0	100.0
5	2000	0.93	0.88
7	2800	1.80	1.80
11	4400	1.40	1.50
13	5200	0.63	0.78
17	6800	0.32	0.40
19	7600	0.50	0.60
23	9200	0.32	0.37
25	10,000	0.20	0.20
29	11,600	0.20	0.20
35	14,000	0.28	0.30
37	14,800	0.11	0.11

MEASURED THD= 2.9%

WAVEFORMS ON PAGE 121

DISTRIBUTION:



PLOTS OF HARMONIC CONTENT OF THE INVERTER OUTPUT VOLTAGE WAVEFORMS VS LOAD FOR TWO WIRE AND THREE WIRE INPUT CONNECTIONS

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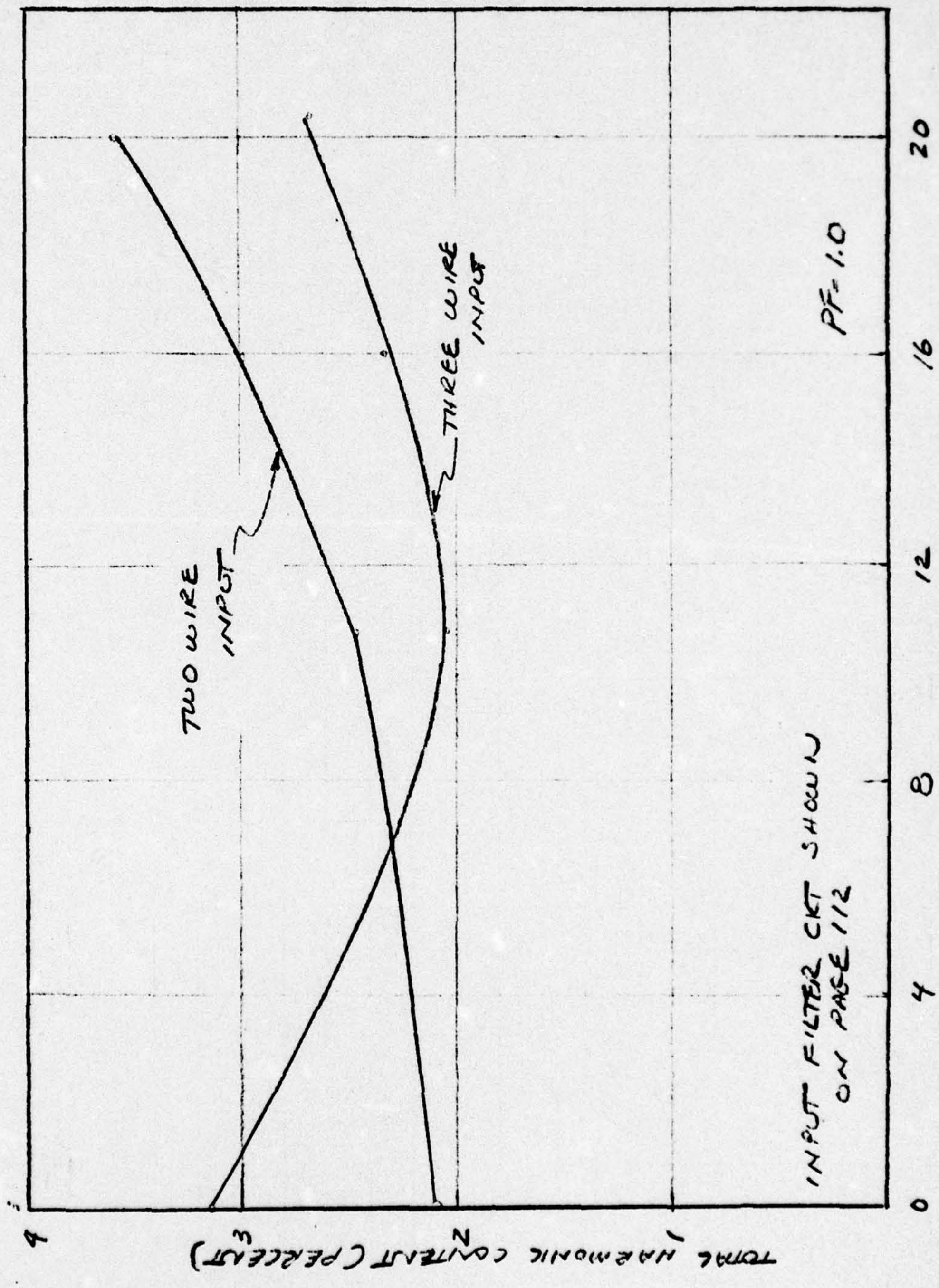

PLOTS OF HARMONIC CONTENT OF THE INVERTER OUTPUT VOLTAGE WAVEFORMS VS LOAD FOR TWO WIRE AND THREE WIRE INPUT CONNECTIONS.

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. DESIGN DATA	PAGE 129
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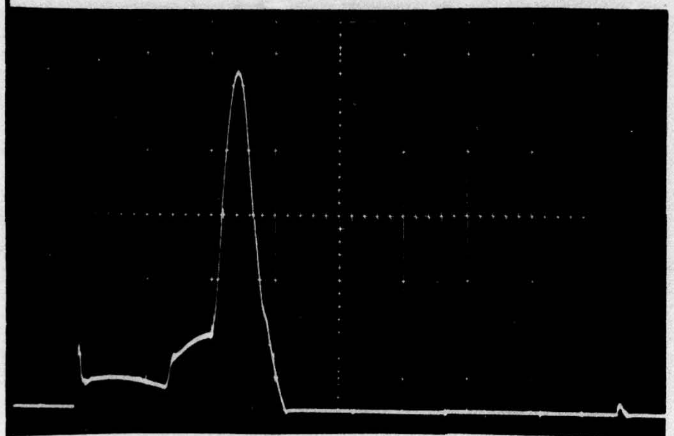
		APPROVED		

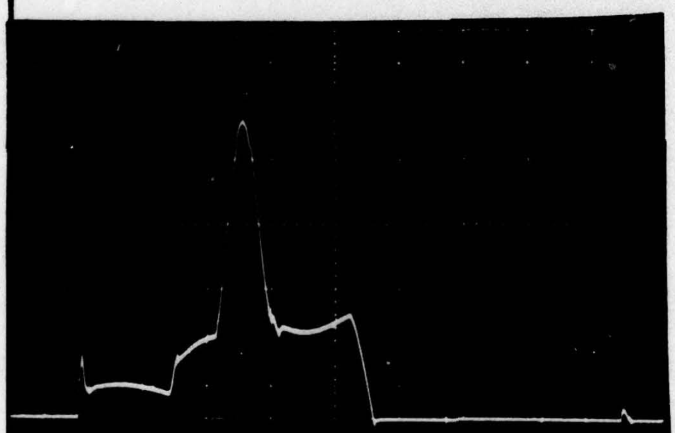
T- CURRENT 400HZ THREE PHASE



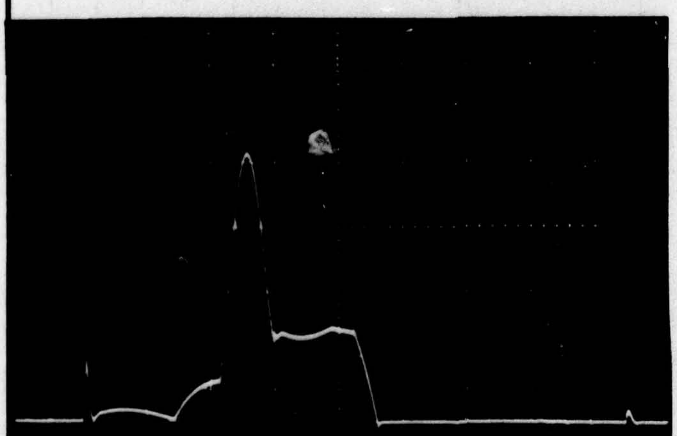
NO LOAD

50A/DIV.

50μSEC/DIV.



20.6KW, PF-1.0



20.6KW, PF=0.8

(2 WIRE INPUT; 60 MFD L-T-L OUTPUT CAPACITANCE)

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DELCO ELECTRONICS
GENERAL MOTORS CORPORATION

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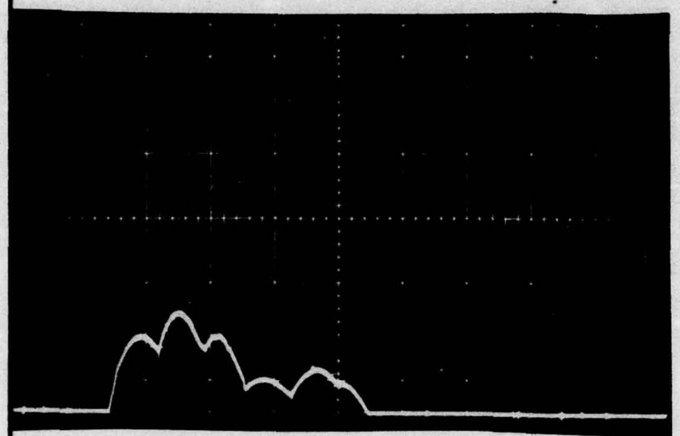
	APPROVED

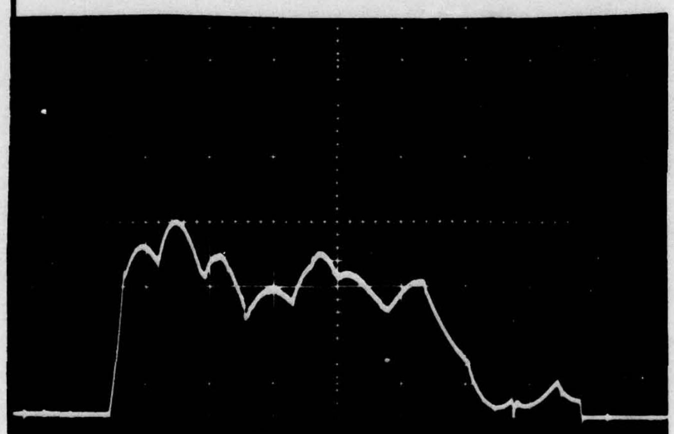
POWER CENTER CURRENT PE 400 HZ THREE PHASE



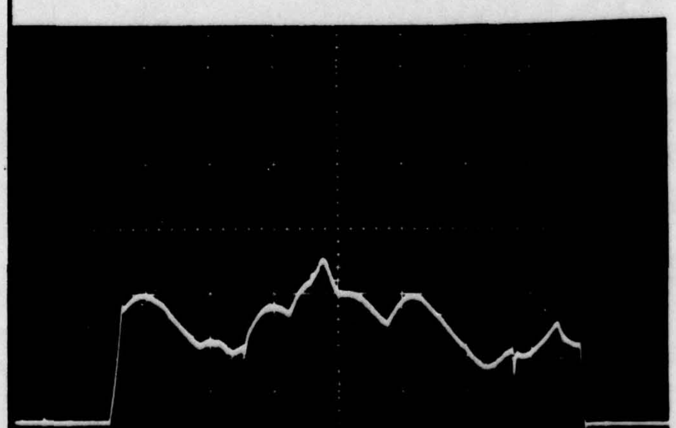
NO LOAD

50A/DIV.

100 μSEC/DIV.



20.6 KW, PF=1.0



20.6 KW, PF=0.8

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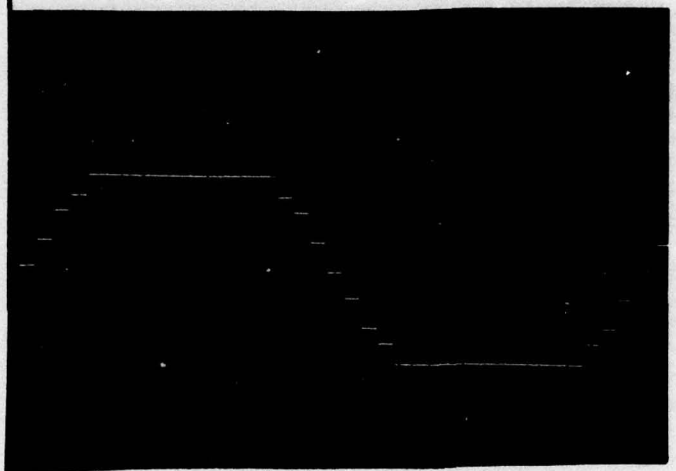
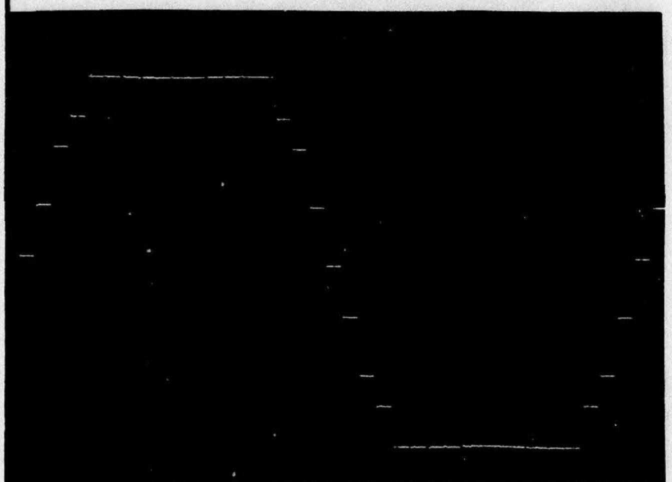
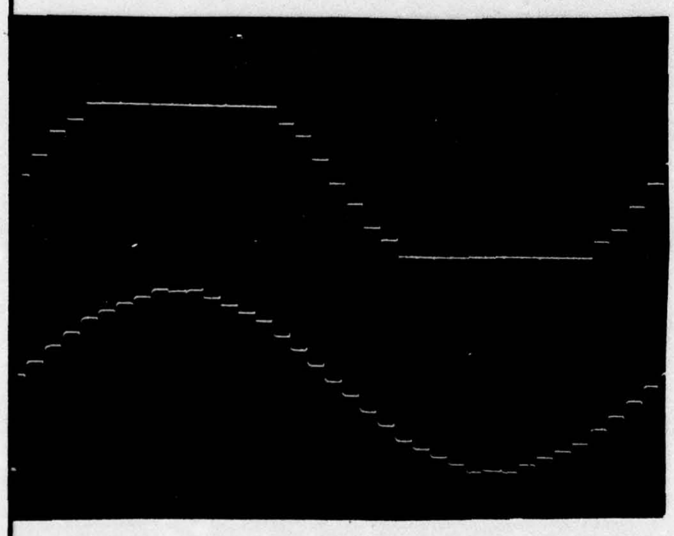
PHOTOGRAPHS TAKEN AT
60HZ, 11KW, PF=1.0 LOAD



INVERTER BASIC
LINE-TO-NEUTRAL
VOLTAGE



BASIC LINE-TO-NEUTRAL
VOLTAGE EXPANDED
IN AMPLITUDE



VOLTAGE INTO TRIPLEN
ATTENUATOR

L-T-N VOLTAGE AT
OUTPUT OF TRIPLEN
ATTENUATOR

DISTRIBUTION:

DE-255 REV. 12-66

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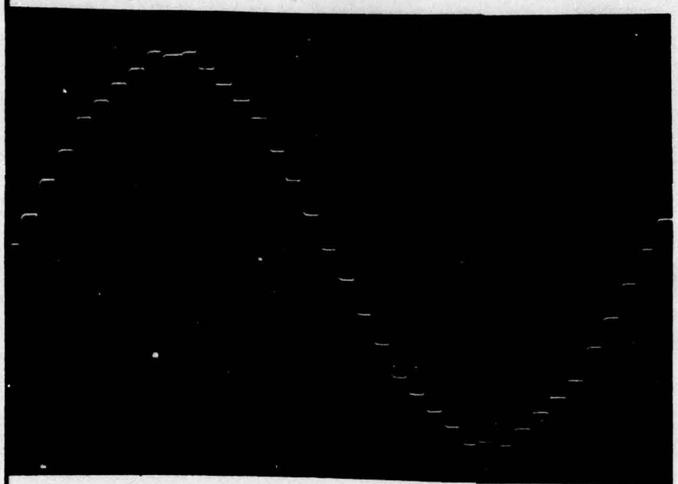
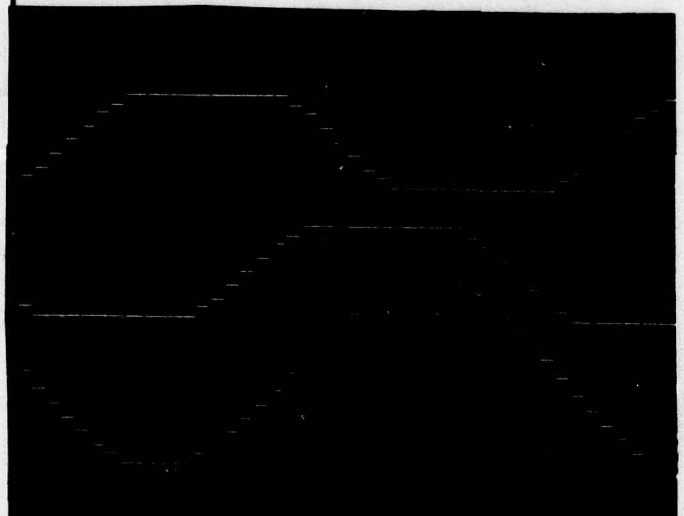
		APPROVED		



UNFILTERED L-T-N VOLTAGE AT OUTPUT OF TRIPLEN ATTENUATOR



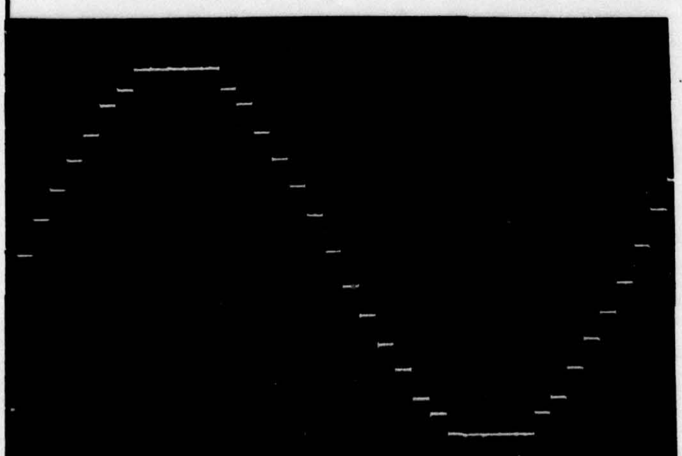
Van

Vbn

Vba

Van + Vbn = Vab

L-T-N VOLTAGES AND RESULTANT L-T-L VOLTAGE



UNFILTERED L-T-L VOLTAGE

DISTRIBUTION:

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0006	PAGE	JOB NO. BASIC VOLTAGE WAVEFORMS	PAGE 133

TITLE	
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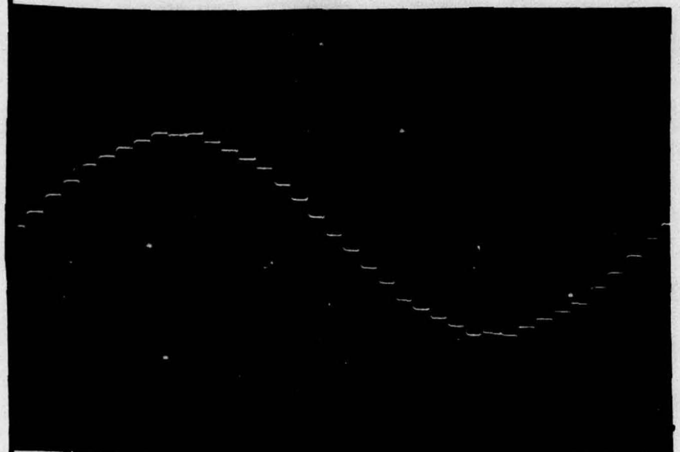
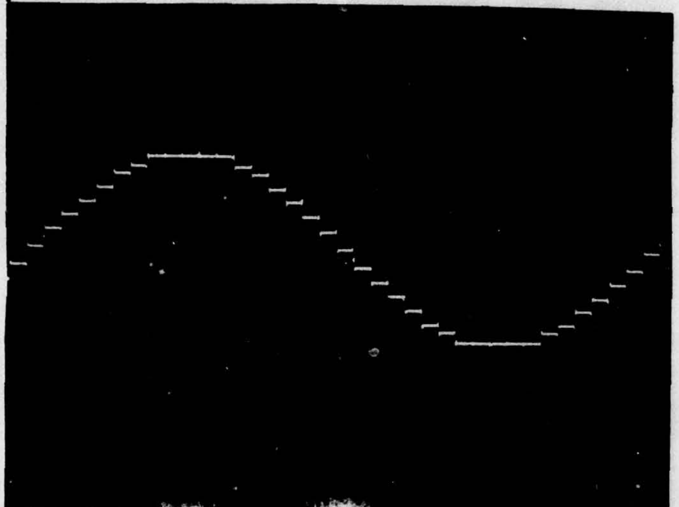
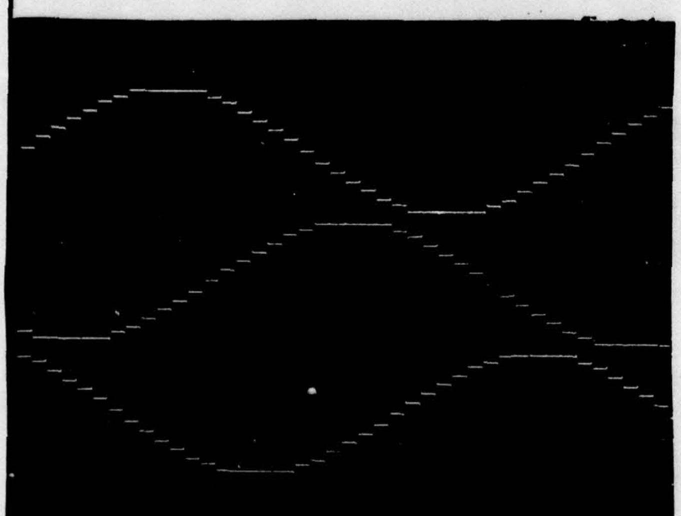


UNFILTERED LINE-TO-NEUTRAL VOLTAGE



UNFILTERED LINE-TO-LINE VOLTAGE



THREE PHASE L-T-L VOLTAGES

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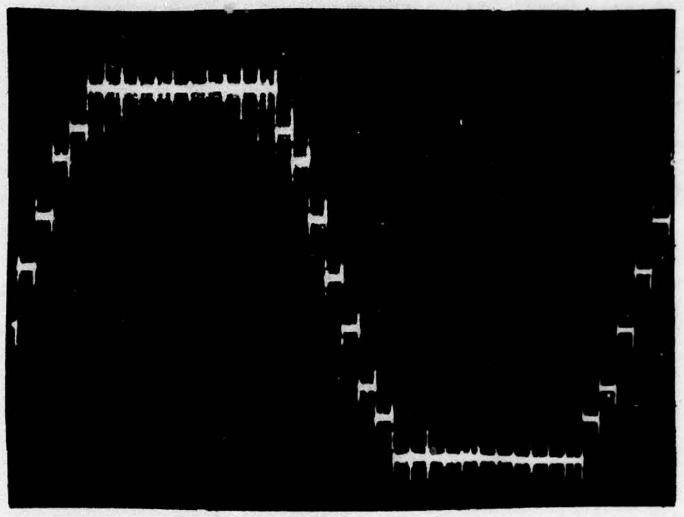
		APPROVED		



BASIC L-T-N VOLTAGE WITH INTENSITY TURNED UP TO SHOW HIGHER FREQUENCY HARMONICS

HARMONIC	FREQUENCY	PERCENT OF FUNDAMENTAL		
NUMBER	HZ	MEASURED* L-T-N	MEASURED* L-TL	COMPUTED L-T-N OR L-T-L
1	60	100.0	100.0	100.0
3	180	0.1	—	18.03
5	300	0.8	0.8	0.98
7	420	1.5	1.5	1.46
9	540	—	—	3.24
11	660	0.8	0.8	0.96
13	780	0.45	0.44	0.21
15	900	—	—	1.17
17	1020	0.87	0.87	0.65
19	1140	0.58	0.60	0.54
21	1260	—	—	0.86
23	1380	0.40	0.40	0.16
25	1500	0.37	0.36	0.43
29	1740	0.30	0.30	0.15
31	1860	—	0.1	0.12
33	1980	—	—	1.63
35	2100	3.0	3.0	2.88
37	2220	2.5	2.6	2.71
39	2340	—	—	1.37
41	2460	—	—	0.10

* MEASUREMENTS MADE AT OUTPUT OF TRIPLEN ATTENUATOR. LOAD = 1KW, PF=1.0. 1MFD CAP. L-T-N MEASURED THD=5.3%. COMPUTER DESIGNED WAVEFORM THD=5.6%

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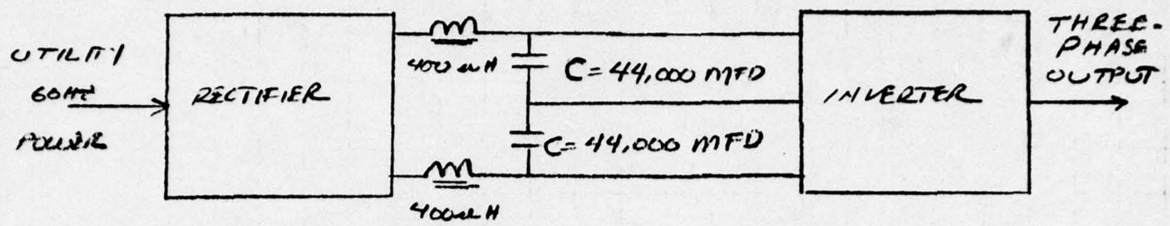
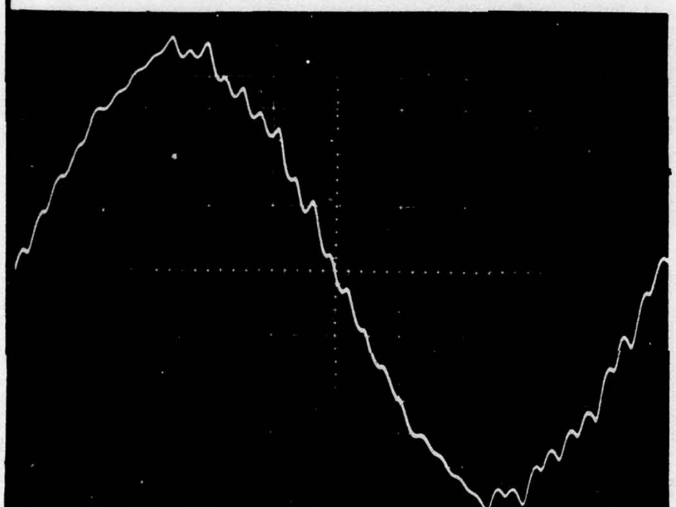
			APPROVED	

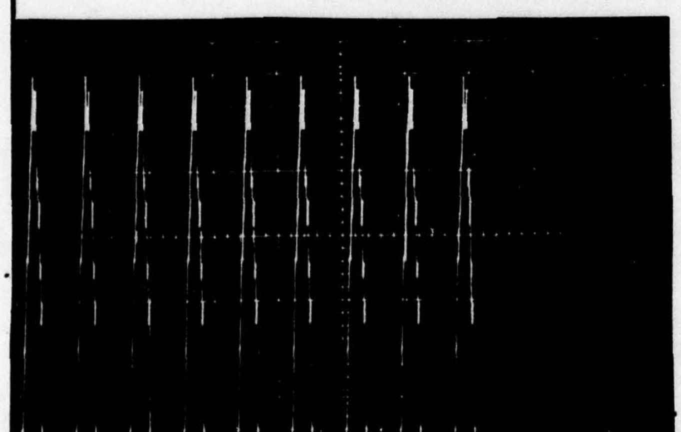
60 HZ OUTPUT





LINE-TO-NEUTRAL VOLTAGE
11KW, PF = 0.8 LOAD
THD = 4.3%

50V / DIV.



20V / DIV.

20ms / DIV.

DISTRIBUTION:

60 Hz OUTPUT

C= 22,000 MFD.

LINE-TO-NEUTRAL VOLTAGE

11kw, PF=0.8 LOAD

THD= 4.3%

50V/DIV.

20V/DIV. 20ms/DIV.

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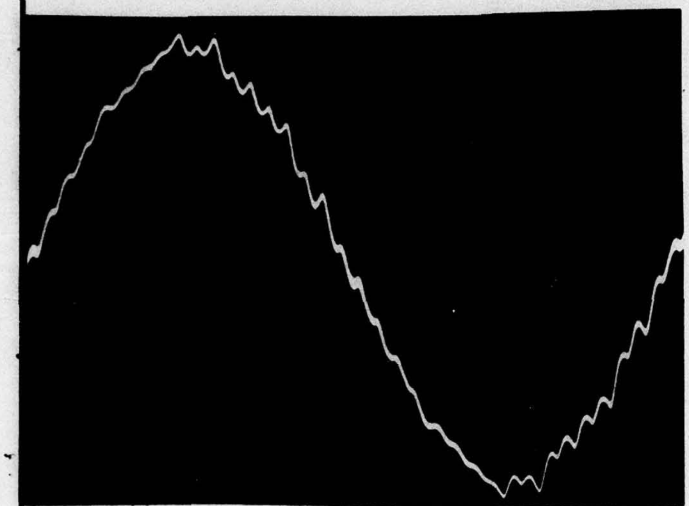
60 HZ OUTPUT

C = 11,000 MFD.

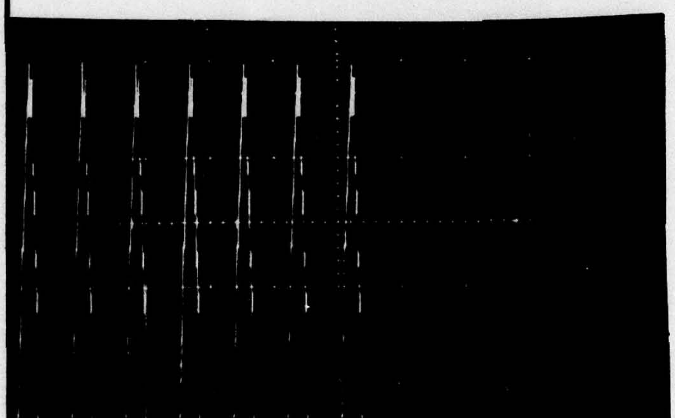


LINE-TO-NEUTRAL VOLTAGE

11KW, PF = 0.8 LOAD

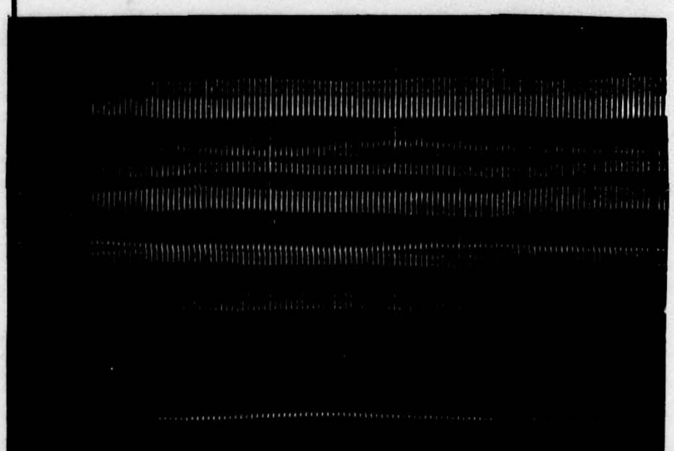
THD = 4.5%

50V/DIV.



20 V/DIV.

20 MS/DIV.



20V/DIV.

0.2 SEC/DIV.

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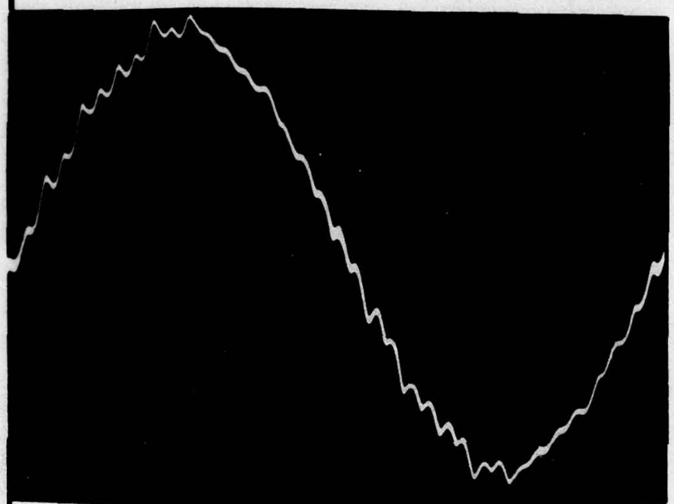
60 HZ OUTPUT

C = 8,800 MFD.

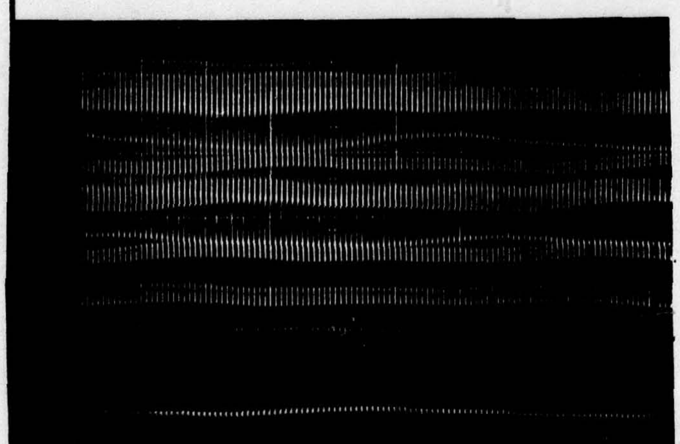


LINE-TO-NEUTRAL VOLTAGE

11KW, PF=0.8 LOAD

THD= 4.4%

50V/DIV.



20V/DIV.

0.2SEC/DIV.

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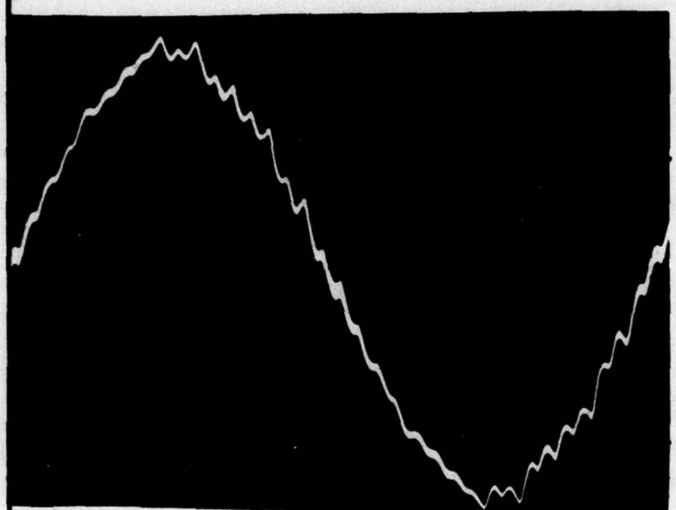
60 HZ OUTPUT

C = 6,600 MFD.

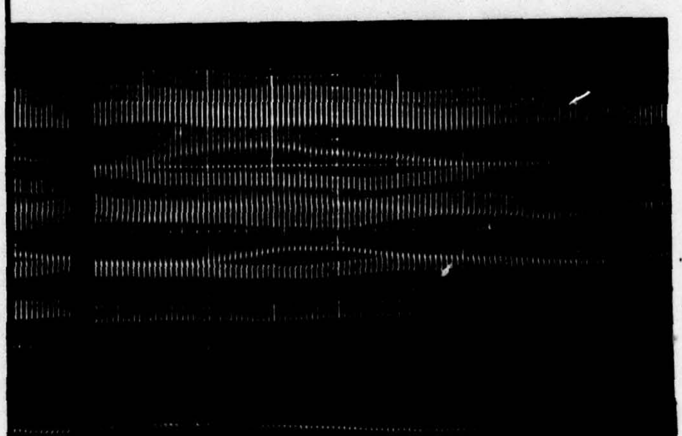


LINE-TO-NEUTRAL VOLTAGE

11KW, PF=0.8 LOAD

THD = 4.6%

50V/DIV.



20 V/DIV.

0.2 SEC/DIV.

(RIPPLE ≈ 4 VOLTS P-TO-P
≈ 0.6 SEC/CYCLE)

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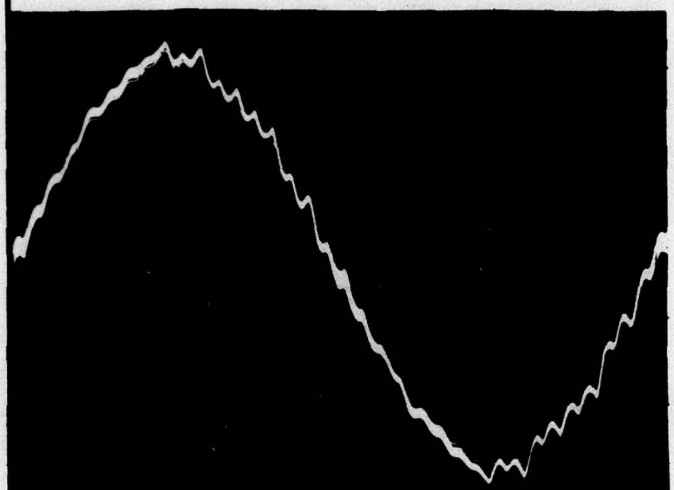
60 Hz OPERATION

C = 4,400 MFD.

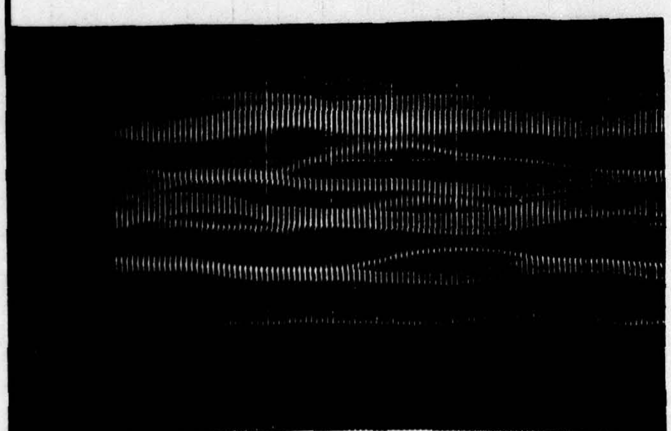


LINE-TO-NEUTRAL VOLTAGE

11KW, PF=0.8 LOAD

THD = 4.6%

50V/DIV.



20V / DIV.

0.2SEC / DIV.

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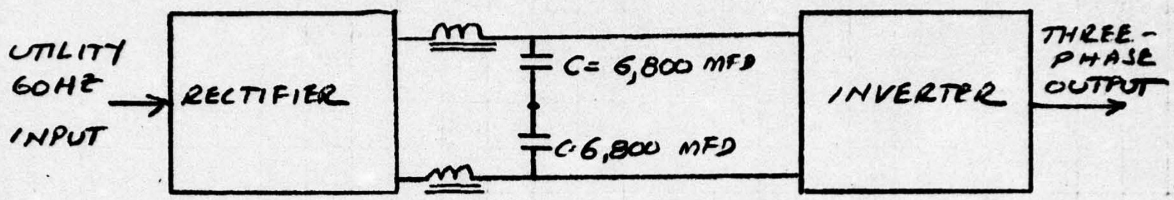
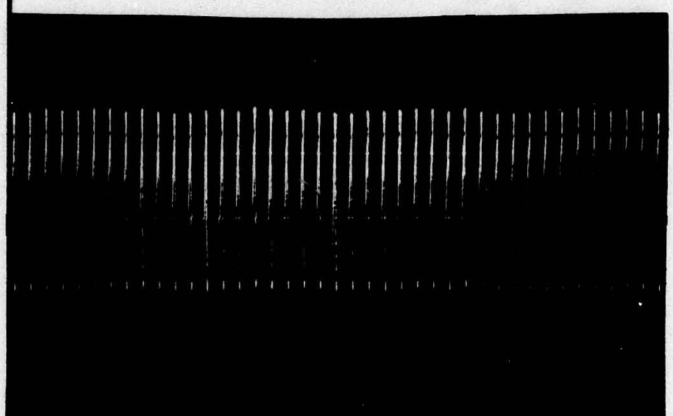
400 HZ OPERATION



TWO WIRE INPUT



LINE-TO-NEUTRAL VOLTAGE

11KW, PF=0.8 LOAD

THD=2.6%

20V/DIV.

10 MS/DIV.

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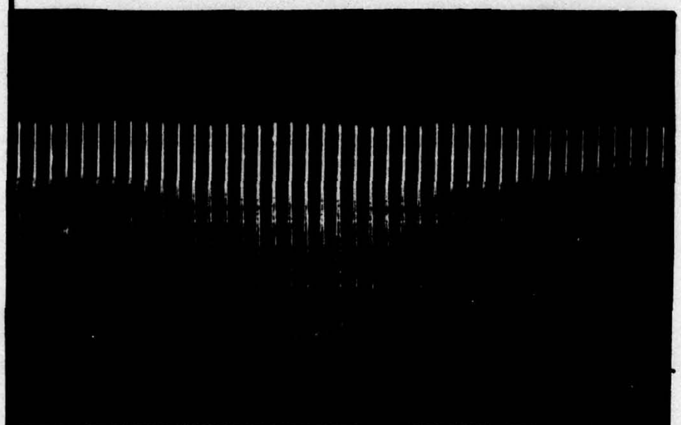
400 HZ OPERATION

C = 4,400 MFD.

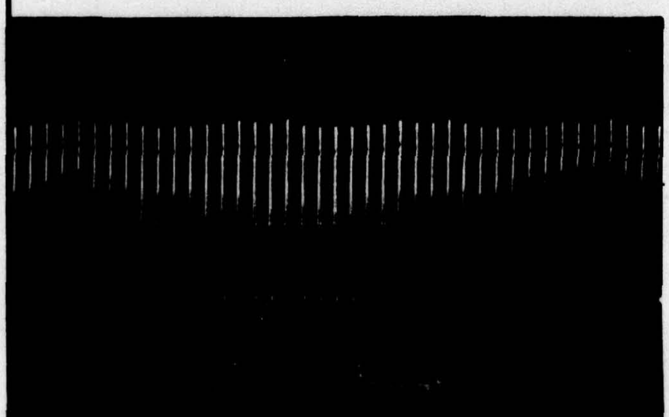


LINE-TO-NEUTRAL VOLTAGE

NO LOAD

THD = 2.2%

20V/DIV. 10MS/DIV.



11KW, PF=0.8 LOAD

THD = 2.7%

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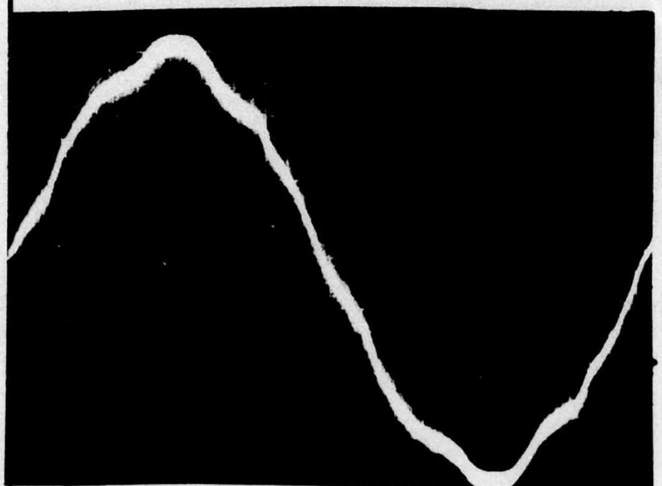
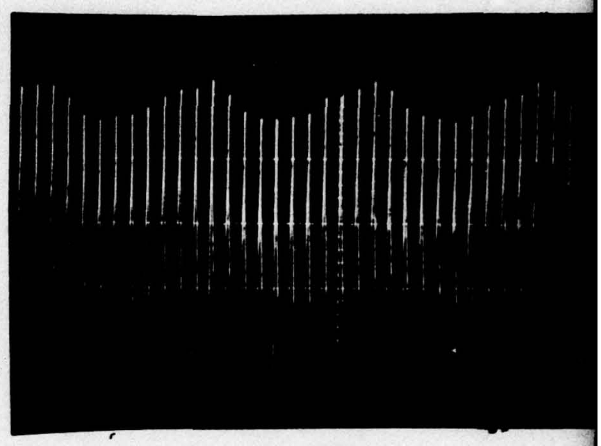
400 HZ OPERATION

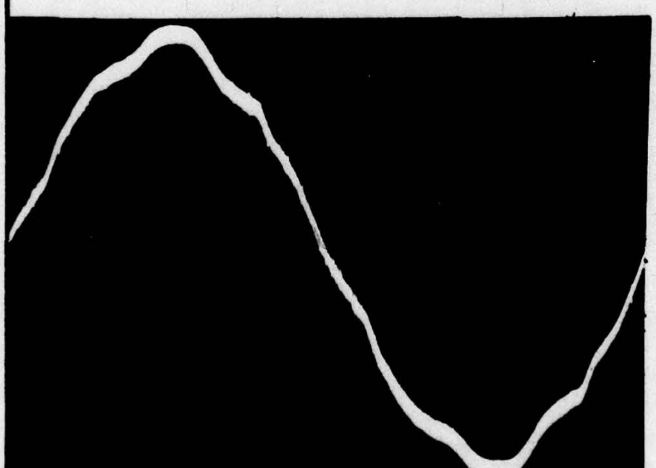
C = 250 MFD. (INVERTER DOESN'T OPERATE WITH C=0 MFD. BECAUSE OF P.F. CORRECTION OPERATION)

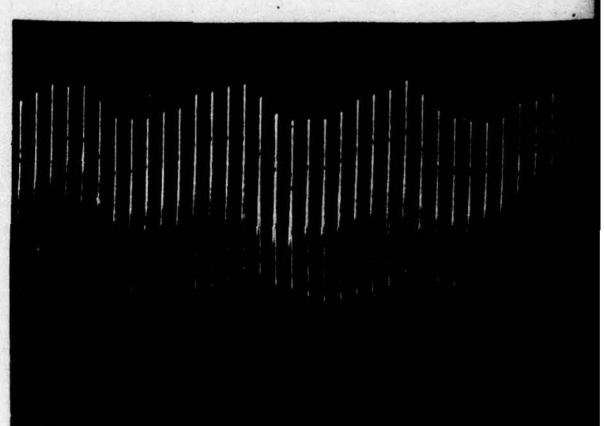




LINE-TO-NEUTRAL VOLTAGE, NO LOAD, THD = 4.6%

50V/DIV. 20V/DIV. 10 MS/DIV.





11KW, PF = 0.8 LOAD THD = 4.6%

50V/DIV. 20V/DIV. 10 MS/DIV.

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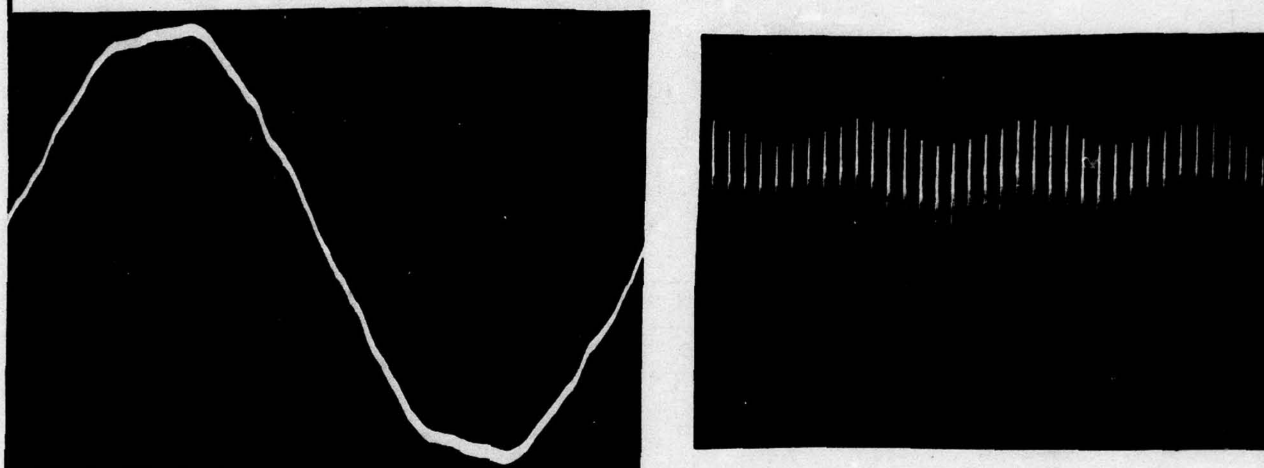
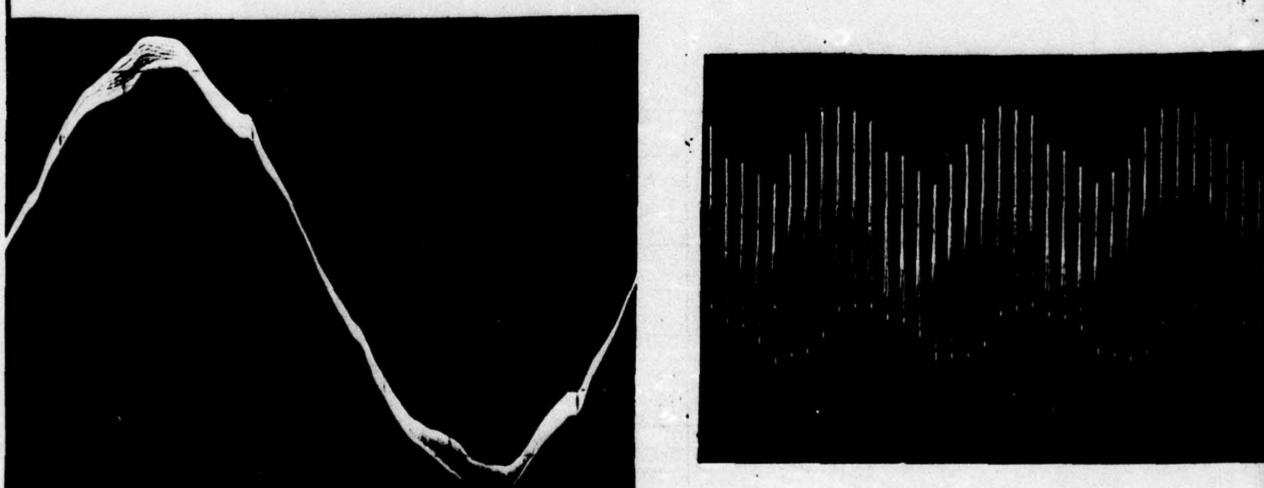
400 HZ OPERATION

C = 500 MFD.



LINE-TO-NEUTRAL VOLTAGE, NO LOAD, THD = 3.4%

50V/DIV. 20V/DIV. 10mS/DIV.



11KW, PF = 0.8 LOAD, THD = 5.7%

50V/DIV. 20V/DIV. 10mS/DIV.
(RIPPLE FREQ ≈ 40 HZ)

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APPENDIX B

DC LINK INVERTER FOR ARMY POWER CONDITIONER REQUIREMENTS

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Delco Electronics Division
General Motors Corporation
Santa Barbara, California

Robert M. McKechnie Robert A. Williams

United States Army
Ft. Belvoir, Virginia
Mobility Equipment R & D Center (MERDC)

ABSTRACT

This paper describes the 12.5 kVA dc link inverter being developed by Delco Electronics – Santa Barbara Operations for USA MERDC, Ft. Belvoir, Virginia. The inverter can produce 120/208 volts three-phase, 120 volts single-phase, or 120/240 volts single-phase power at 60 or 400 Hz. It has an efficiency of 84 to 94% and a breadboard weight of 150 pounds. Based on a patented design concept (No. 3,725,767), the inverter generates stepped wave and square wave voltage segments which are combined as a three-phase composite to produce line-to-line waveforms of 4% total harmonic content before filtering.

Study results show that the basic inverter concept can take several circuit forms, and can be developed with ratings up to 100 kVA. The inverter is being developed as a candidate for the Army 15 kVA general purpose power conditioner, and as such must conform to MIL-STD-1332B and MIL-STD-461A.

INTRODUCTION

The United States Army Mobility Equipment Research and Development Center (MERDC) is sponsoring development of a family of "stand alone" electric power conditioners. Of the approaches available the dc link inverter appears highly feasible in the 3 to 300 kVA power range. Part of this effort is being performed by the Delco Electronics–Santa Barbara Operations under Contract DAAK 02-72-C-0210.

Development of the dc link inverter concept has been concentrated in the medium power range (15 - 30 kVA) wherein most immediate Army requirements lie. Study results clearly show the feasibility and utility of this approach for high power range (100 kVA) applications, and the significant circuit improvements attainable.

The family of power conditioners envisioned by the Army will supply multifrequency (60 Hz/400 Hz) outputs at multivoltages (120/208 volts, three phase for all ratings, and in addition 120/240 volts, single phase for ratings below 15 kVA), and function as uninterruptable power systems (UPS) when a suitable battery supply is added. The output power quality will conform to MIL-STD-1332B even though the input power is of lesser quality, or of a special type (such as the high frequency of the 12.5 kVA turbo-alternator).

Therefore, the power conditioners have potential usage as:

- Line phase converter (1 Ø to 3 Ø or vice versa)
- Frequency converters (60 to 400 Hz)
- Precision power sources, operating from utility grade power
- Uninterruptable power systems
- Special purpose systems (such as a turbo-alternator frequency changer)

A paper * describing the work undertaken to develop a power conditioner for the turbo-alternator application was presented to the 1973 PESC. This work showed the suitability of the Delco approach for general purpose power conditioners. Additional efforts toward this application are described below.

BASIC THREE-PHASE INVERTER

The basic inverter concept is a three-phase, four-wire system consisting of power switching circuits that generate x, y, and center functions, as defined by the voltage waveform in Figure 1.

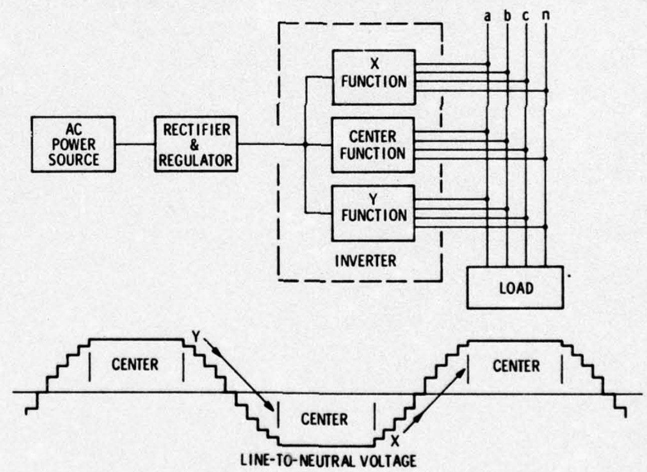

Figure 1. Delco Power Conditioner Block Diagram

Figure 2 is an oscilloscope trace of the flat topped waves generated in a three-phase, line-to-neutral voltage pattern. The waveform has a total harmonic content of 16.9% and consists of only odd harmonics. Removal of the third harmonic (16.02%), and all remaining triplens, reduces total harmonic content to 4.2%.

Individual harmonics of the inverter waveform are shown in Table I. Note the low values of the fifth and seventh harmonics. The only single harmonic of significance is the 41st, which is generated by the stepped character of the output wave and is easily filtered out.

*- T.M. Corry. "A New Concept for Generating Three-Phase Sine Wave Voltages With Semiconductor Power Switches." 1973 PESC. Record pages 230-236.

Figure 2. Three-Phase Line-to-Neutral Voltages Generated by the y, x, and Center Function Circuits

LINE-TO-NEUTRAL VOLTAGE LEVELS	6
POWER CENTER WIDTH	99°
STEP WIDTH	9°
TOTAL HARMONIC CONTENT OF UNFILTERED OUTPUT VOLTAGE	16.9%
INDIVIDUAL HARMONICS	MAGNITUDE (%)
1	100.0
3	16.02
5	0.19
7	0.61
9	1.06
11	0.65
13	0.51
15	0.40
17	0.36
19	0.33
21	0.27
23	0.30
25	0.22
27	0.27
29	0.22
31	0.34
33	0.11
35	0.01
37	1.28
39	2.59
41	2.45
43	1.10
45	0.07
47	0.07
49	0.21
51	0.12
53	0.13
55	0.09
57	0.12
59	0.09
61	0.09

Table I. Harmonic Content of the MERDC 10 kW Inverter Voltage Waveforms

Figure 3 is a schematic diagram of the original MERDC 12.5 kVA inverter showing the y, x, and center function circuits. Three-phase power is rectified and filtered at the input of the inverter. The inverter consists of y, x, and center function circuits, phase selectors and output filter.

The center function generator is a three-phase thyristor bridge circuit through which as much as 80% of the inverter power passes directly from the input to the output. The remaining power passes through the y and x step forming circuits, consisting of a tapped autotransformer, step selector switches and a thyristor circuit that energizes the autotransformer. The phase selectors apply the stepped voltage waveforms to the proper output lines.

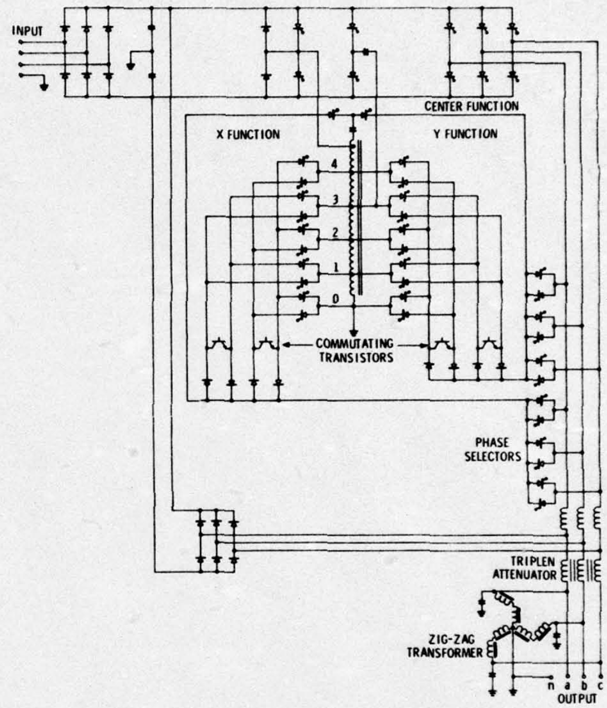

Figure 3. Original MERDC 10 kW Inverter Breadboard Circuit

The triplen attenuator and zig-zag transformer shown in Figure 3 form a circuit of magnetic components that removes the third harmonic and all multiples thereof from the line-to-neutral output voltages. The attenuator is three isolated windings on a common "C" core that function as current limiting impedances to all triplen frequencies in the three-phase output leads. With balanced loads, the harmonic currents in the three windings caused by the fundamental and all odd harmonics other than the triplens are each 120° out of phase. They cancel, and therefore do not induce back-EMFs in the windings. Therefore, the windings appear as air core inductors to the non-triplen frequencies with inductances of a few microhenries. Since the inductance is low to the fundamental, stored energy is low and inverter regulation is not significantly degraded. In contrast, triplen harmonic currents are additive and are limited in magnitude to the core magnetizing current.

While the triplen attenuator serves as a high impedance to triplen currents, the zig-zag autotransformer presents essentially a short circuit to these currents. The relative impedances of the triplen attenuator and the zig-zag transformer are such as to reduce the magnitude of the third harmonic voltage from 16.02% at the

inverter to less than 0.3% at the output. This reduction is accomplished with relatively small investment in size and weight and very low energy storage. The oscilloscope traces in Figures 4a and 4b show the results of eliminating the triplen harmonics from the line-to-neutral voltages, by means of the triplen attenuator and zig-zag transformers, to form a nearly sinusoidal output voltage.

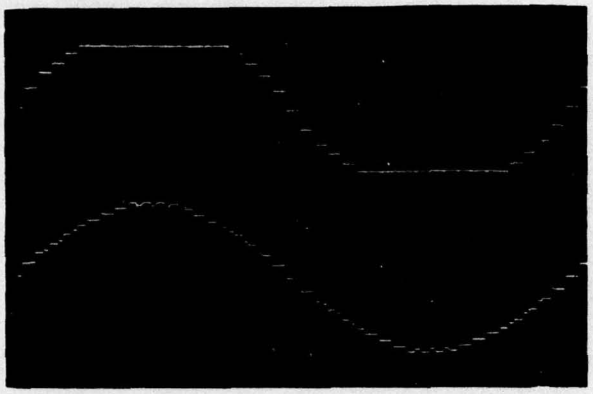

Figure 4a. Voltage at Input of Triplen Attenuator

Figure 4b. Voltage at Output of Triplen Attenuator

THE PROBLEM OF OBTAINING SINGLE-PHASE POWER

As well as producing three-phase power, the MERDC breadboard inverter is now required to produce 10 kW, 0.8 PF, two-wire, 120 volts or three-wire 120/240 volts, at 60 Hz or 400 Hz. The problem was to supply this load unbalance without significantly degrading voltage output quality, efficiency, or transient response. All power handling components in the inverter are sized principally by the magnitude of the load. The size of the zig-zag transformer, however, is determined primarily by the magnitude of load unbalance. For balanced three-phase loads, the zig-zag transformer is essentially unloaded. When a single-phase load is connected line-to-neutral, the transformer maintains currents in the windings equal to one-third the load current. Thus, the rating of the zig-zag transformer is a major factor in determining the magnitude of the 120 volts, two-wire, single-phase loads that are acceptable. Figure 5 depicts the vector relationships between line currents and line-to-neutral voltages for a 120V single-phase load.

Through the action of the zig-zag transformer, current is forced to flow in all three phases of the inverter. This action helps maintain voltage balance across the three phases; but more important, the currents in the unloaded phases are forced in magnitude and phase angle to cancel the ampere turns in the triplen attenuator core due to the fundamental current in the loaded phase. In Figure 5, the current in line A is 2/3 the load current, and is in phase with that line-to-neutral voltage. The current in line B is 1/3 the load current and lags its phase voltage by 60°. Two-thirds of the load power is delivered by line A and 1/6 of the power is delivered by each of lines B and C through action of the zig-zag transformer. Line A carries twice the current compared to rated three-phase loading.

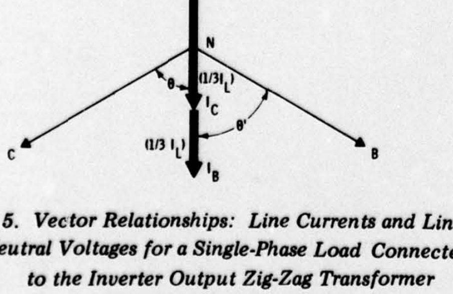

Figure 5. Vector Relationships: Line Currents and Line-to-Neutral Voltages for a Single-Phase Load Connected to the Inverter Output Zig-Zag Transformer

Thus it can be seen that single-phase, 120 volts, two-wire loading of the inverter is achievable without modifying the circuit configuration, but that the magnitude of the unbalanced load is limited primarily by the volt-ampere rating of the zig-zag output transformer. The single-phase 120/240 volts output is not inherently available to the basic inverter design. However, a single-phase autotransformer, connected line-to-line and tapped to produce 120 volts, two-wire or 120/240 volts, three-wire, can be designed to carry rated power and operate efficiently at both 60 and 400 Hz. When single-phase loads are connected line-to-line, the zig-zag transformer does not handle the unbalance and is essentially unloaded. Studies and tests indicate that the most efficient, least costly method of obtaining all single-phase power from the inverter is by means of a single autotransformer, connected line-to-line, with taps at appropriate points on the windings for either two-wire or three-wire output. Figure 6 shows the transformer-to-inverter connection to produce 120/240 volts, 400 Hz, single-phase power. Related test results are briefly summarized in the Appendix. The inner taps are used for 400 Hz operation; the outer taps are used for 60 Hz operation.

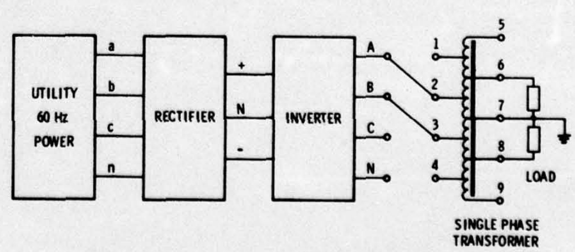

Figure 6. Connections for 400 Hz, Single-Phase, 120/240 V, Three-Wire Power

METHODS OF COMMUTATING STEP CURRENTS

Prior to this investigation the power rating of the original inverter circuit (Figure 3) was limited primarily by the current ratings of the step voltage commutation transistors. Breadboards capable of handling peak powers of 30 kVA have been built using transistor step commutation. However, to extend the inverter performance to the 100 kVA region, step circuits had to be developed in which the transistors were replaced by thyristors. To describe the change in design of step commutation, consider the following:

If the y and x step functions are extracted from the flat-topped, three-phase, line-to-neutral output voltages, they appear as shown in Figure 7a. These functions have a fundamental frequency three times that of the output voltages. The step widths and heights of the y and x functions are derived from computer-optimized, stepped waveforms.

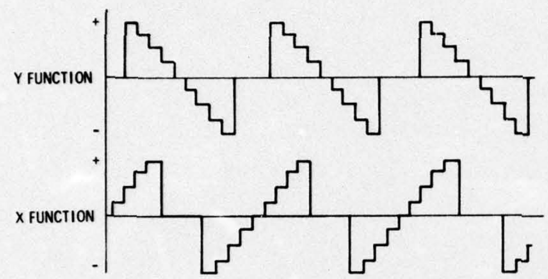

Figure 7a. Graphical Definitions of y and x Functions

Figure 7b shows a basic circuit for generating the y and x step voltage functions. When the transformer voltage polarity is positive, the y function switches start at step 4 and generate voltage steps sequentially down to the zero level and the x function switches start at the zero level and generate voltage steps sequentially up to step 4. When the transformer polarity is negative the y function switches start at the zero level and generate negative voltage steps to step 4 and the x function switches start at step 4 and generate negative voltage steps until the zero level is reached.

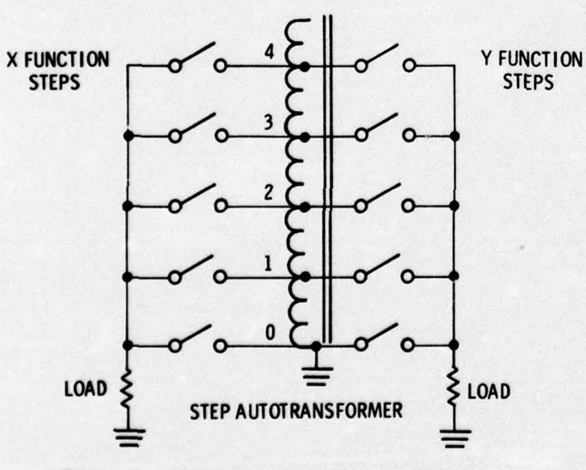

Figure 7b. Elementary Step Forming Circuit

Illustrated in Figure 8 is a step forming circuit that uses thyristors to change voltage levels, plus all possible combinations of voltage polarities and current flows for the y and x functions. Analysis of thyristor commutation requirements for conditions 8a through 8h indicates that all required step changes can be achieved with two basic commutation schemes. Discussed below are methods for determining the appropriate commutation scheme for each y and x voltage step change situation and methods for configuring an improved step forming circuit.

Y Function

In Figure 8a, with voltage and current flow positive, it is desired to transfer current flow from SCR4 to SCR3 in accordance with the y waveform defined in Figure 7a. SCR3 is maintained biased off by the conduction of SCR4; therefore, an auxiliary circuit is required to commutate SCR4.

In Figure 8b, with voltage positive and current flow negative, it is desired to transfer current flow from SCR4 to SCR3. Turning on SCR3 reverse biases and turns off SCR4, causing transfer of current flow to SCR3. Commutation of this type does not require auxiliary turn off circuits and will be referred to as "free commutation."

In Figure 8c, with voltage and current flow negative, it is desired to transfer current flow from SCR3 to SCR4. Turning on SCR4 reverse biases SCR3, resulting in free commutation. In Figure 8d, with voltage negative and current flow positive, an auxiliary commutation circuit is required to transfer current flow from SCR3 to SCR4.

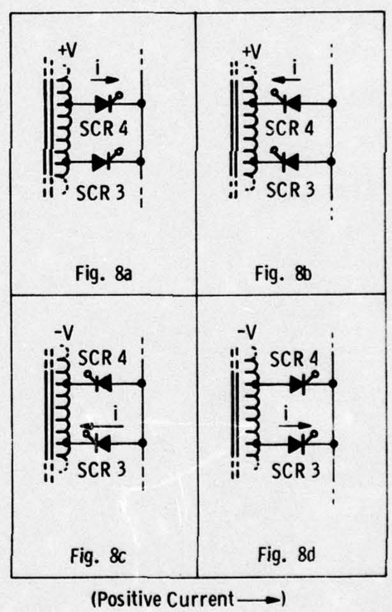

Figure 8. Basic Thyristor Step Forming Circuits

Y FUNCTION	STEP VOLTAGE & CURRENT	
STEP TRANSFORMER VOLTAGE POLARITY	IN-PHASE	OUT-OF-PHASE
+	AUX. COMM. REQUIRED	FREE COMMUTATION
-	FREE COMMUTATION	AUX. COMM. REQUIRED

Table II. Commutation Methods for Steps Formed by the y Function

X Function

A similar approach can be used for the x function, referring to Figures 8e through 8h. Tables II and III summarize commutation methods for all combinations of voltage polarities and current flow directions for the y and x functions, respectively. Through these tabulations, methods can be visualized for reorganizing the y and x step circuits to exploit the free commutation approach.

The original step circuit (Figure 9a) can be modified such that one half of the step thyristors are connected to a free commutation bus and the other half connected to an auxiliary commutation circuit (Figure 9b). The new step circuit improves system efficiency by eliminating four diodes and by setting up current paths that bypass the commutation transistors one-half the time. The schematic diagram in Figure 10 shows the improved step commutation incorporated into the inverter breadboard circuit.

The new step circuit is a continuation of the trend toward reducing the number of power semiconductors required to produce 5% total harmonic content, three-phase voltages. Figure 11, for example, shows that 72 power semiconductors (thyristors, diodes, and transistors) were required in 1969. As studies on the inverter progressed, the requirement steadily decreased to where only 28 will be used in 1974. This reduction is achievable by:

- Using reverse conducting thyristors in place of thyristor-bypass diode combinations.
- Reducing the number of voltage steps on the autotransformer
- Phase shifting the inverter current so that zero current flows in the auxiliary commutation step circuits so that only free commutation is needed.

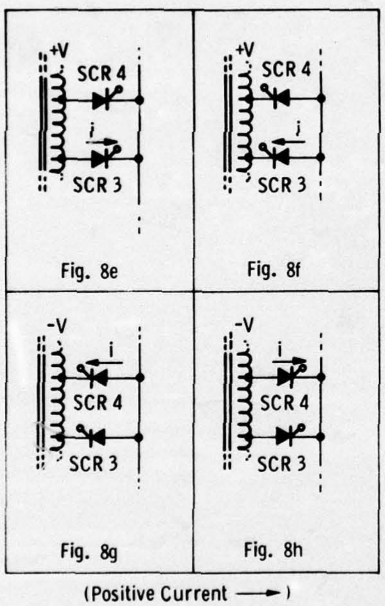

Figure 8 (Cont.). Basic Thyristor Step Forming Circuits

X FUNCTION	STEP VOLTAGE & CURRENT	
STEP TRANSFORMER VOLTAGE POLARITY	IN-PHASE	OUT-OF-PHASE
+	FREE COMMUTATION	AUX. COMM. REQUIRED
-	AUX. COMM. REQUIRED	FREE COMMUTATION

Table III. Commutation Methods for Steps Formed by the x Function

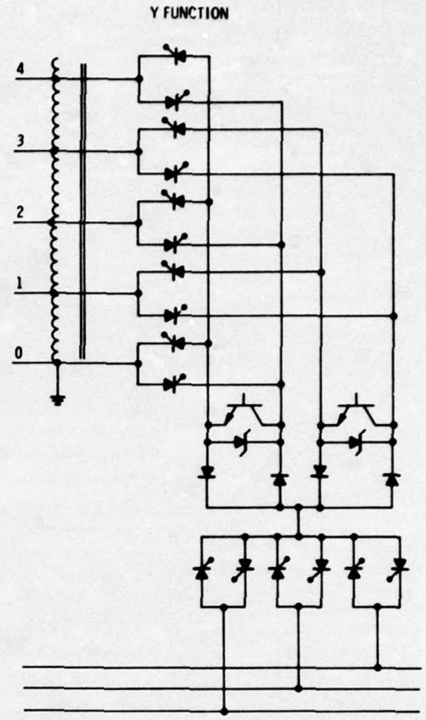

Figure 9a. Original Step Forming Circuit

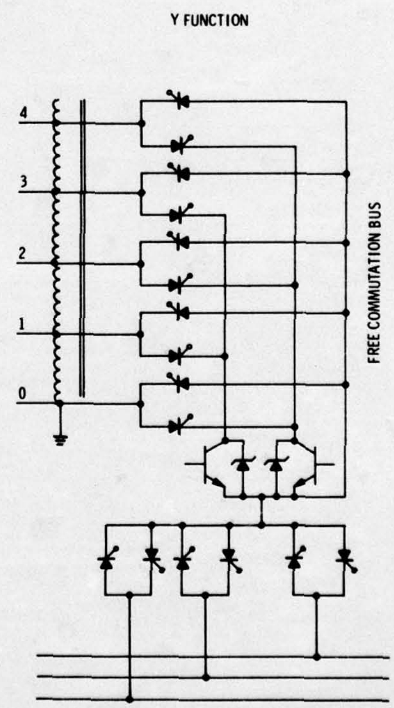

Figure 9b. Improved Step Forming Circuit

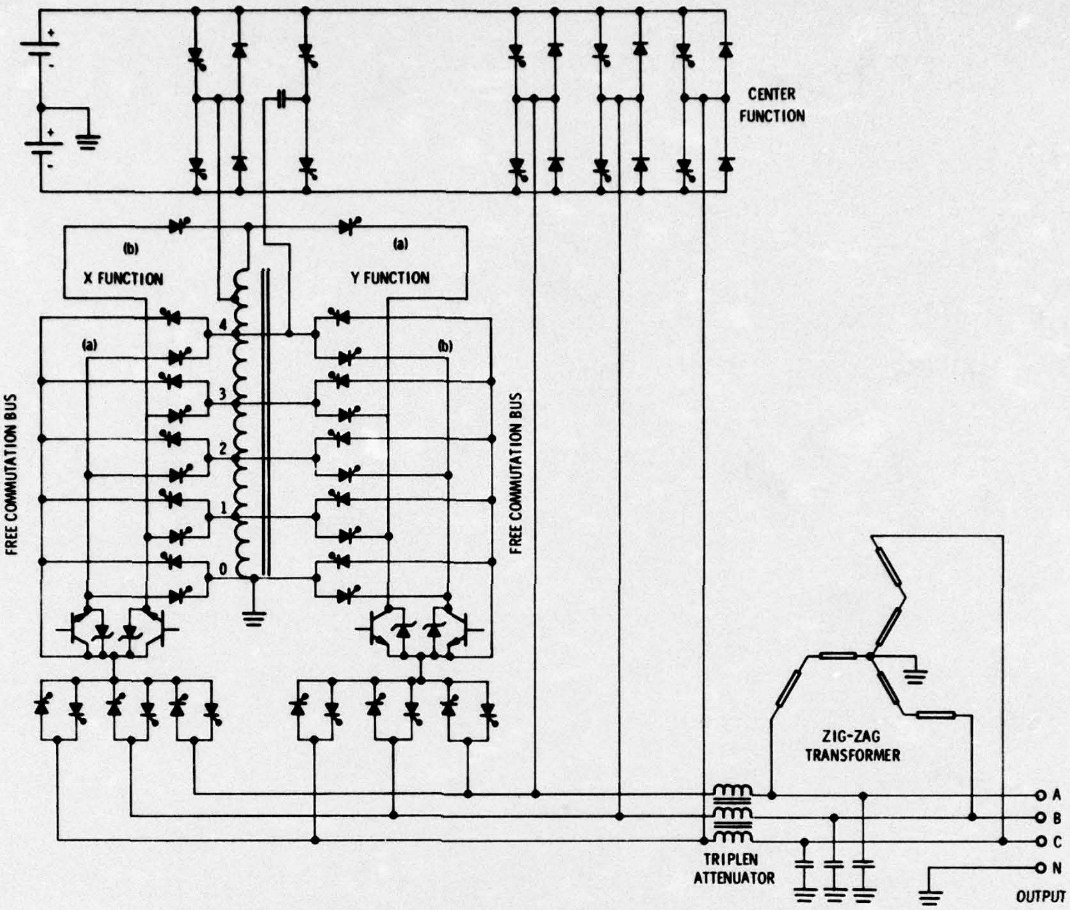

Figure 10. Improved 12.5 kVA Inverter Breadboard Circuit

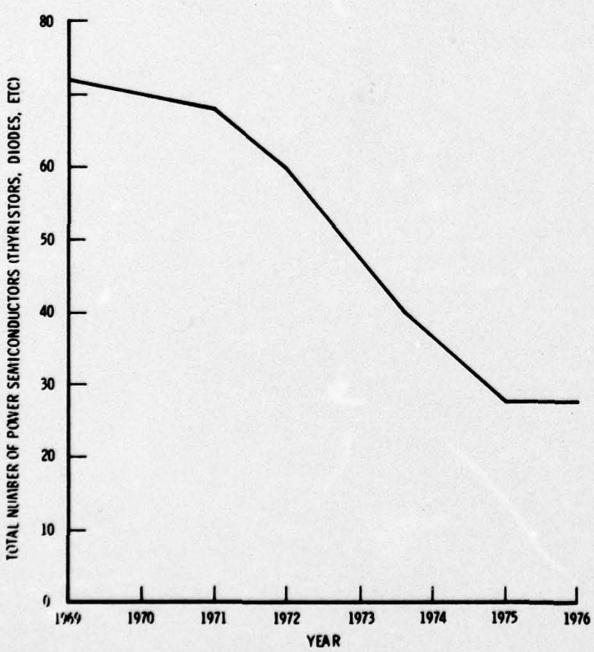

Figure 11. Number of Inverter Power Semiconductors Required to Produce Three-Phase

Elimination of the auxiliary commutation circuits and the associated step thyristors, as suggested in the third point, would account for 12 of the semiconductors eliminated. The penalty, however, is greater capacitance required at the inverter output. That is, at 400 Hz the circuit is cost effective, but at 60 Hz the cost of added capacitors exceeds that of the replaced thyristors. The waveform quality achievable with this circuit at 400 Hz three-phase, full load is shown in Figure 12. Total harmonic content for the illustrated waveform is 0.95%. Total harmonic content at no load is approximately 3%.

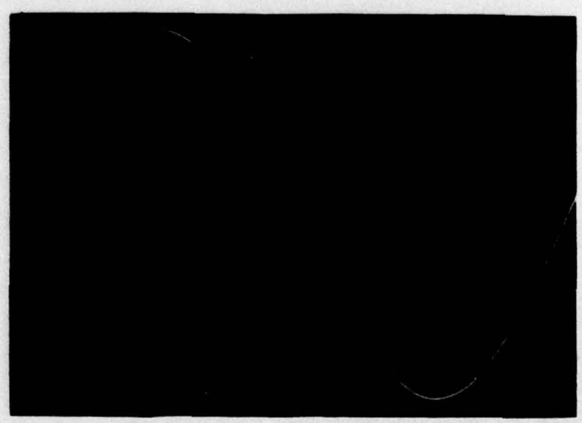

Figure 12. Output Voltage Produced by the Improved Circuit.

Table IV provides preliminary design estimates of size and weight for the inverters rated at 15 kVA for the MERDC-required combinations of frequencies, three-phase and single-phase operation. The efficiency of these inverters will exceed 90% for three-phase operation and 84% for single-phase operation.

POWER RATING	WEIGHT (LB)	VOLUME(FT^3)
15 KVA, 3 PHASE, 400 HZ	65	1
15 KVA, 3 PHASE, 400 or 60 HZ	100	2
15 KVA, 3 PHASE, 400 or 60 HZ OR 10 KVA, 1 PHASE, 400 or 60 HZ	150	3

Table IV. Preliminary Weight and Volume Estimates

REPLACING TRANSISTORS WITH THYRISTORS

Advantages of employing transistor starvation commutation of step thyristors, compared to typical thyristor commutation circuits, are that it requires virtually no energy storage in inductors or commutation capacitors, has low switching losses, and is capable of shorter voltage step widths (because of faster switching capability). Disadvantages are its power limitation (about 30 kVA), higher cost, and need for Zener diodes to provide transistor transient voltage protection. Starvation commutation is also difficult to achieve with high current transistors or parallel transistor combinations.

By reorganizing the step forming circuit it became possible to directly substitute a thyristor reverse voltage commutation circuit (Figure 13) for the transistor starvation commutation circuit.

This was followed by fabrication of experimental step circuits which demonstrated the possibility of achieving considerably higher inverter ratings. For 60 Hz inverters, step currents of 1,000 amperes — sufficient for a 100 kVA system — were commutated. Thus far, commutation of step currents of 300 amperes has been demonstrated for 400 Hz inverters.

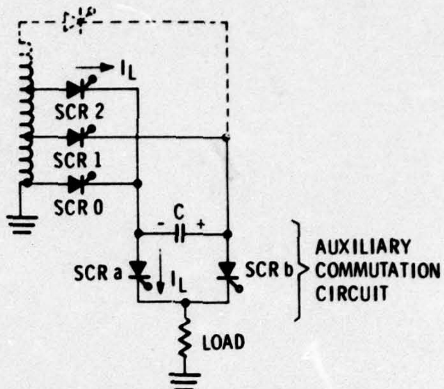

Figure 13. Step Changing Circuit Using Thyristor Reverse Voltage Commutation

Current is transferred from one voltage level to another by a two-step commutation sequence. Assume that in Figure 13 thyristors SCR2 and SCRa are conducting current to the load, that the transformer polarity is positive, and that capacitor C is charged as indicated. In order to transfer the load current to level 1, SCRb and SCR1 are gated on. The discharge of capacitor C reverse biases SCRa and turns it off. SCR 2 is turned off by the reverse voltage ring up of capacitor C which leaves it properly charged for the next step change to level 0. Load current continues to flow through SCR1 and SCRb.

SUMMARY

The Delco breadboard inverter is an example of the Army-sponsored development of dc link technology to obtain a family of compact, lightweight, and efficient power conditioners. Experiments have demonstrated the feasibility of extrapolating the present Delco technology to the 100 kVA level by replacing transistor commutation circuits with thyristors. Through use of innovative switching to obtain desired waveshapes, it is possible to significantly reduce componentry and circuit complexity and improve reliability.

APPENDIX

SINGLE PHASE PERFORMANCE SUMMARY FOR MERDC 12.5 kVA, THREE-PHASE BREADBOARD INVERTER

ITEM	PERFORMANCE
Voltage output	120 Vrms, single-phase, 2-wire, 60 Hz or 400 Hz 120/240 Vrms, single-phase, 3-wire, 60 Hz or 400 Hz Adjustable between 95 and 105% of rated voltage.
Power Output	10 kW, 0.8 PF lagging; 200% rated current for 5 seconds at 400 Hz. 10 kW, 0.8 PF at 60 Hz. (Input - output filter designs limited performance below 200% rated current. Further development required.)
Voltage Waveform	Total harmonic content: 2.1% at 400 Hz, single-phase 4.3% at 60 Hz, single-phase DC voltage component: less than 10 mV.
Single-Phase Efficiency	Frequency (Hz) | Load | Efficiency (%) 60 | 10 kW, 0.8 PF, 2-wire | 89 60 | 10 kW, 0.8 PF, 3-wire | 90 400 | 10 kW, 0.8 PF, 2-wire | 84 400 | 10 kW, 0.8 PF, 3-wire | 85
Effect of Unbalanced Load (Single-Phase, 3-wire)	0.8% at 400 Hz for 5.8 kW unbalance 2.2% at 60 Hz for 5.8 kW unbalance
Voltage Regulation	Less than 1% for all load conditions at 60 Hz or 400 Hz.
Voltage Modulation	Less than 3 volts
Transient Voltage Performance (Single Phase)	With the inverter system initially operating at no load, rated voltage, and at 400 Hz, the rms terminal voltage dropped to 80% of rated voltage when a 0.4 PF lagging load having an impedance of 0.5 per unit was applied to the output terminals of the set. The output voltage jumped to 120% rated voltage when the load was removed. Test not conducted at 60 Hz. With the system operating at 400 Hz and rated voltage, a step change in load from no load to 10 kW, 0.8 PF caused the output voltage to drop to 81% of rated voltage. Removal of the load caused the output voltage to jump to 118% of rated voltage. (See Figure 14a.). Under the same conditions as above but with the inverter operating at 60 Hz, the output voltage dropped to 70% rated value when the load was applied, and increased to 130% when the load was removed. (See Figure 14b.)

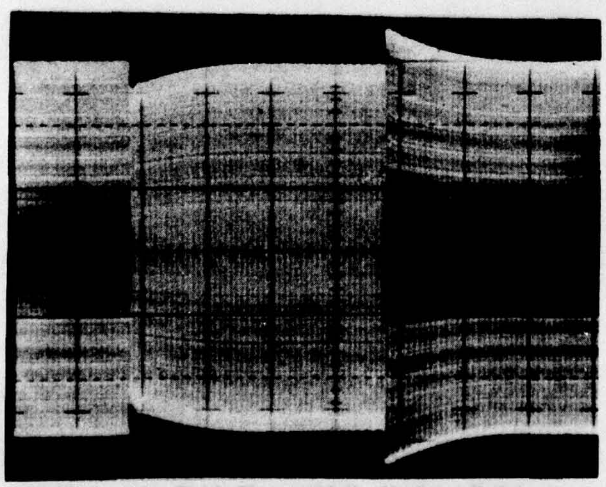

Figure 14a. Single-Phase, 400 Hz, No Load-Full Load Voltage Transients

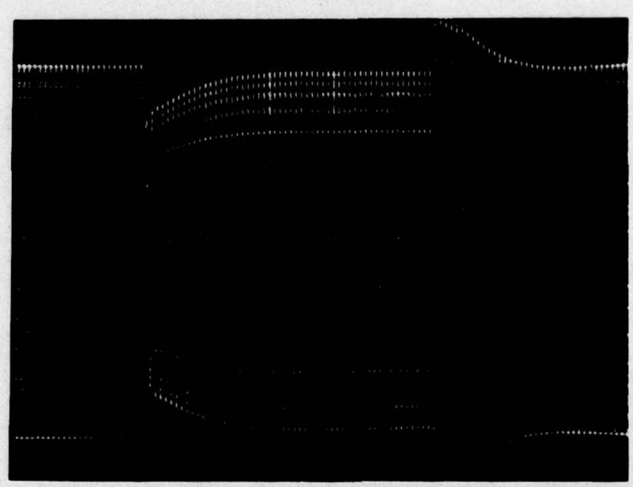

Figure 14b. Single-Phase, 60 Hz, No Load-Full Load Voltage Transients

15KVA INVERTER

PARTS LIST

CDRL ITEM A002

ITEM NO. 0006

CONTRACT NO. DAAK02-72-C-0210

MATERIAL MEMORY TIMING CIRCUIT 110° WIDE POWER CENTER

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
1	LM375N	3	
2	DM8520	2	
3	SN74123	3	
4	SN7492	2	
5	SN7400	1	
6	SN7107	2	
7	SN7493	3	
8	HPROM-8256-5	5	
9	10K OHM RESISTOR 1/4 WATT	7	
10	330 OHM RESISTOR 1/4 WATT	1	
11	470 OHM RESISTOR 1/4 WATT	1	
12	.01 μF CAPACITOR	5	
13	38 μH INDUCTOR	1	
14	5 PF CAPACITOR	1	
15	56 pF CAPACITOR	1	
16	75 pF CAPACITOR	1	
17	220 pF CAPACITOR	6	
18	1000 pF	1	
19	120 pF	2	
20	4200 pF	1	
	TOTAL		

MATERIAL R.F. DRIVERS

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
1	CIRCUIT BOARD RSK 2C296-501	6	
2	SN5402N QUAD NOR GATE	18	
3	SN 5413 N DUAL NAND SCHMITT TRIGGER	6	
4	HTI-6500-5 HARRIS QUAD. CORE DRIVER	6	
5	F625-92-06 CORE, INDIANA GENERAL	36	
6	2N5333 TRANSISTOR PNP	12	
7	RESISTOR, 5 OHM ±3% DALE NH-5	12	
8	RESISTOR, 39 OHM ±5% 1W.	12	
9	ZENER DIODE, UZ740 40 VOLT	6	
10	CAPACITOR, MYLAR 0.015 MFD 100 VDC	6	
11	CAPACITOR, TANTALUM, 100 MFD, 10VDC	6	
12	DIODE, 1N4448	72	
13	HEAT SINK TX 0506-B	12	
14	CONNECTOR, ELCO P/N 00-6007-044-980-002	6	
15	T-STRUT VECTOR TS169N	6	
16	RETAINER KIT, VECTOR BR 19H	4	
17	CASE GUIDE VECTOR BR 19-6-1 3.5"	5	
	TOTAL		

MATERIAL THYRISTOR R.F. DRIVE ISOLATION CIRCUIT

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
	SINGLE SCR DRIVE (18 REQUIRED)		
1	DIODE 1N4448	4	
2	TRANSFORMER, DELCO XT-71036	1	
3	CIRCUIT BOARD	1	
4	TERMINAL, USECO 1281C	4	
	PARALLEL SCR DRIVE (14 REQUIRED)		
1	DIODE 1N4448	8	
2	TRANSFORMER, DELCO XT-72023	1	
3	CIRCUIT BOARD	1	
4	TERMINAL USECO 1281C	6	
	TOTAL		

MATERIAL POWER SWITCH ASSEMBLY ITEM NO. 0006

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
1	THYRISTOR 82-2022 INTERNATIONAL RECTIFIER	20	
2	DIODE 82-0060 INTERNATIONAL RECTIFIER	2	
3	CAPACITOR 0.1 MFD SPRAGUE 196P1049654	18	
4	RESISTOR 20 OHM 25 WATT ±3% DALE NH-25	18	
5	CAPACITOR 20 MFD CORNELL-DUBILIER SCRG-105	1	
6	CAPACITOR 1.0 MFD SPRAGUE 330P31	3	
7	TRANSFORMER, STEP XT74004	1	
8	TRANSFORMER, ZIG-ZAG XT 72034	1	
9	TRANSFORMER, C.T. COMMUTATION 5T, 1T Q65-55151-A2-2	3	
10	TRANSFORMER, SINGLE PHASE XT-73030	1	
11	INDUCTOR TRIPLEN XL 72028	1	
12	INDUCTOR TRIPLEN XL 73014	1	
13	INDUCTOR 515 MICROHENRIES	1	
14	INDUCTOR 5 MICROHENRIES	1	
15	CIRCUIT BREAKER 65 AMP HEINEMAN P3XAM1516	1	
16	WIRE, #12 TEFLON FLEXIBLE MIL-W-16878D TYPE E	100 FT	
17	WIRE, #14 TEFLON FLEXIBLE MIL-W-16878D TYPE E	50 FT	
18	FAN ROTRON MARK 4 GRILL SERIES 747	4	
19	TERMINAL SEASTROM 5903-4-16	3	
20	TERMINAL SEASTROM 5903-6-8	1	
21	TERMINAL AMP CAT. NO. 320574	50	

MATERIAL STEP COMMUTATION CIRCUIT 60 HZ

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
1	THYRISTOR 82-2022 INTERNATIONAL RECTIFIER	3	
2	CAPACITOR 20 MFD SPRAGUE 333P12	4	
3	TRANSFORMER TB	2	
4	INDUCTOR L_1	2	
5	INDUCTOR L_2	1	
6	POWER SUPPLY 66VDC 9 AMPS	1	
7	CAPACITOR 125MFD G.E. 28F1104FC	2	
	TOTAL		

MATERIAL AUXILIARY POWER SUPPLY

ITEM	PART NUMBER AND DESCRIPTION DESCRIBE IN DETAIL PART NO., VENDOR CODE, SPECIFICATION, DIMENSION, UNIT, TRADE OR BRAND NAME, COLOR, TYPE OF MATERIAL, ETC.	QTY	
1	ARNOLD MAGNETICS CORP. POWER SUPPLY ASN-M18/3-A5/2-A2.7/0.3CA	1	
	TOTAL		

15KVA INVERTER

PARTS LIST

CDRL ITEM A002

ITEM NO. 0006

CONTRACT NO. DAAK02-72-C-0210


Cont

AD-A035 045 FREQUENCY CONVERTER PORTABLE ALTERNATING CURRENT MULTIFREQUENCY 10 KW VOL..(U) GENERAL MOTORS CORP GOLETA CALIF DELCO ELECTRONICS DIV I CORRY JAN 75

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