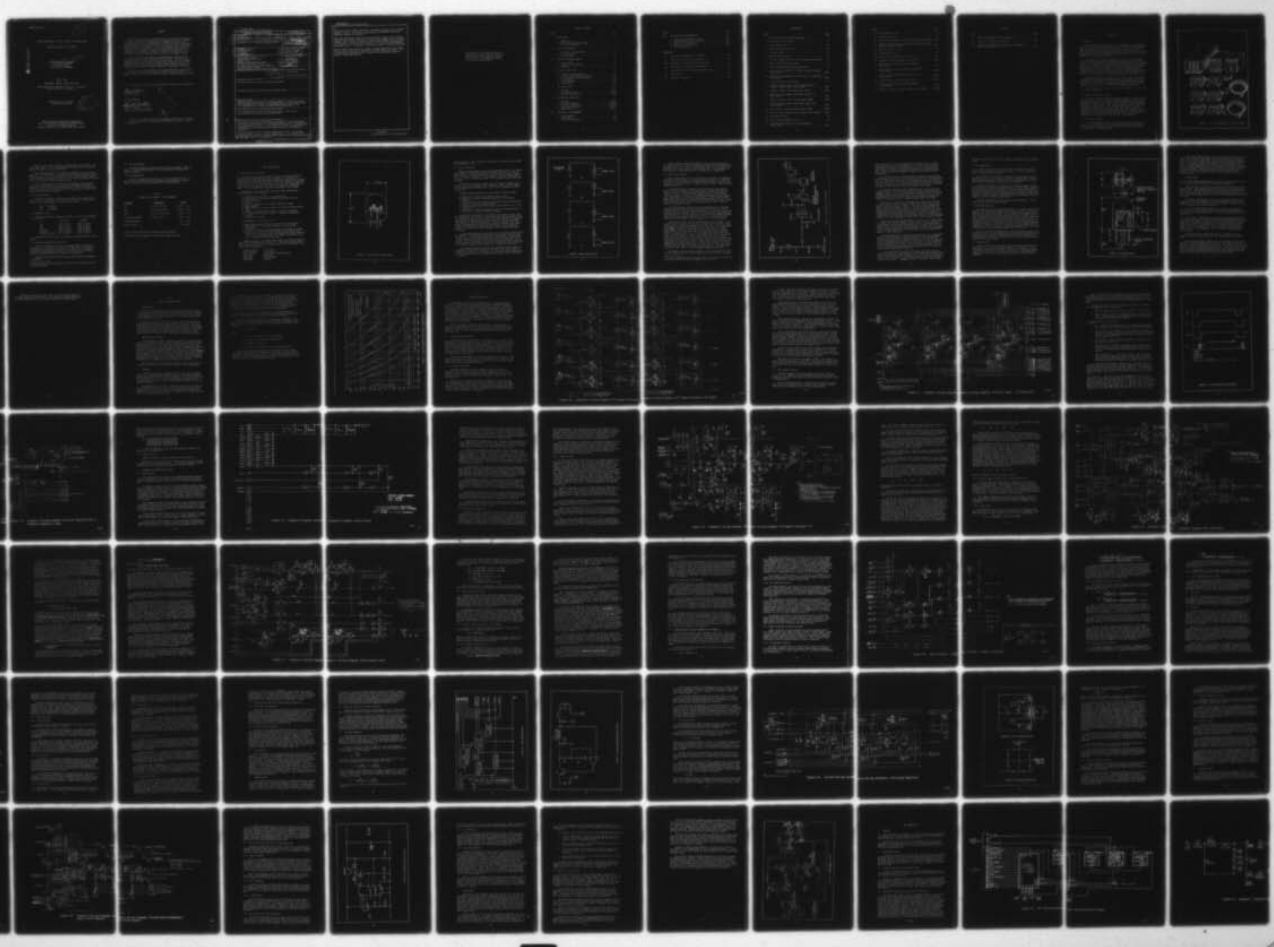
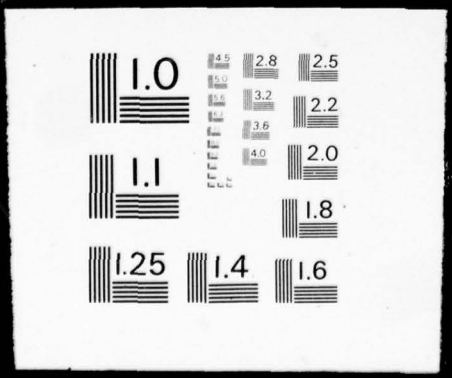
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INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM

AD A032304

New 409933

Edison Electronics Division
McGraw-Edison Company
Grenier Field
Manchester, New Hampshire

JUNE, 1976

TECHNICAL REPORT AFAPL-TR-76-64

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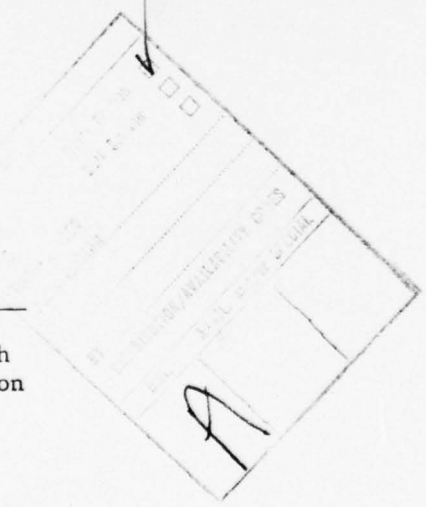
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the background, specifications, design, development, construction and evaluation of an airborne integrated fire and overheat warning system known as the IFOS. It was built to illustrate the possibility of providing fire and overheat detection capability with a high degree of reliability.

The IFOS consists of six ultraviolet flame detector heads, two overheat-sensing thermistor cables, a central computer unit, a crew readout unit to

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indicate fire and overheat conditions, a maintenance warning unit to indicate component failure. The system is self-testing to an important degree and completely automatic in operation.

Three such systems were constructed and extensively tested. Tests included operation under various conditions of input voltage, temperature and altitude. Response times to fire and overheat conditions were measured, and one system was subjected to vibration, shock, humidity, salt spray and electromagnetic interference tests. In addition, a theoretical study of reliability was made.

While the above tests uncovered a number of design weaknesses, all of these defects could be overcome in designing an improved model of the IFOS. It is concluded that a high reliability, automatic fire and overheat detection system is definitely feasible.

The citation of trade names and names of manufacturers in this report is not to be construed as official government endorsement or approval of commercial products or services referenced herein.

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I

INTRODUCTION

1. BACKGROUND

Most operational Air Force aircraft are equipped with overheat sensors for fire and overheat detection. These systems do not offer adequate fire detection capability, as evidenced by their inability to detect a large percentage of the engine nacelle fires in Air Force aircraft. In addition, these systems are highly susceptible to false alarms which result in aborted missions, high operational and maintenance costs and in a few instances, loss of aircraft and lives.

In the 1960's, the AFAPL originated the concept of the Integrated Fire and Overheat Detection System which, because of the system's electronics and the redundant and overlapping coverage provided by the radiation sensors and overheat cables, significantly increased the hazard detection capability and reduced or eliminated the false alarm problem associated with present day detection systems. This system concept consists of radiation sensors for fire and overheat cables for overheat detection, together with a microcircuit for signal processing, thus providing complete hazard detection capability for the engine nacelle of an aircraft.

The objective of this program was to develop a flight qualifiable Integrated Fire and Overheat Detection System with potential application for the engine compartments of an advanced multi-engine bomber/transport aircraft. This system is to distinguish between a fire and an overheat condition and provide highly reliable hazard detection capability.

Three complete systems, with spares, were delivered to the Air Force in 1976 for evaluation.

2. GENERAL DESCRIPTION OF SYSTEM

The system developed under this program consists of six ultraviolet radiation detector heads for detecting engine compartment fires, a dual loop overheat cable for detecting overheat conditions in the engine compartment, a computer control unit, a crew readout unit and a maintenance warning unit. See Figure 1. Each radiation detector head contains two ultraviolet radiation sensors and the dual loop overheat cable were developed for mounting in the engine compartment of an aircraft. The computer control unit and the maintenance warning unit were developed for installation into an aircraft electronic bay. The readout unit was developed for installation into the aircraft crew compartment.

3. SYSTEM SPECIFICATIONS

The exact, detailed specifications for this system are found in Air Force Contract F33615-72-C-1053, and in the Military Specifications to which this contract refers. For the convenience of the reader, these specifications are summarized below.

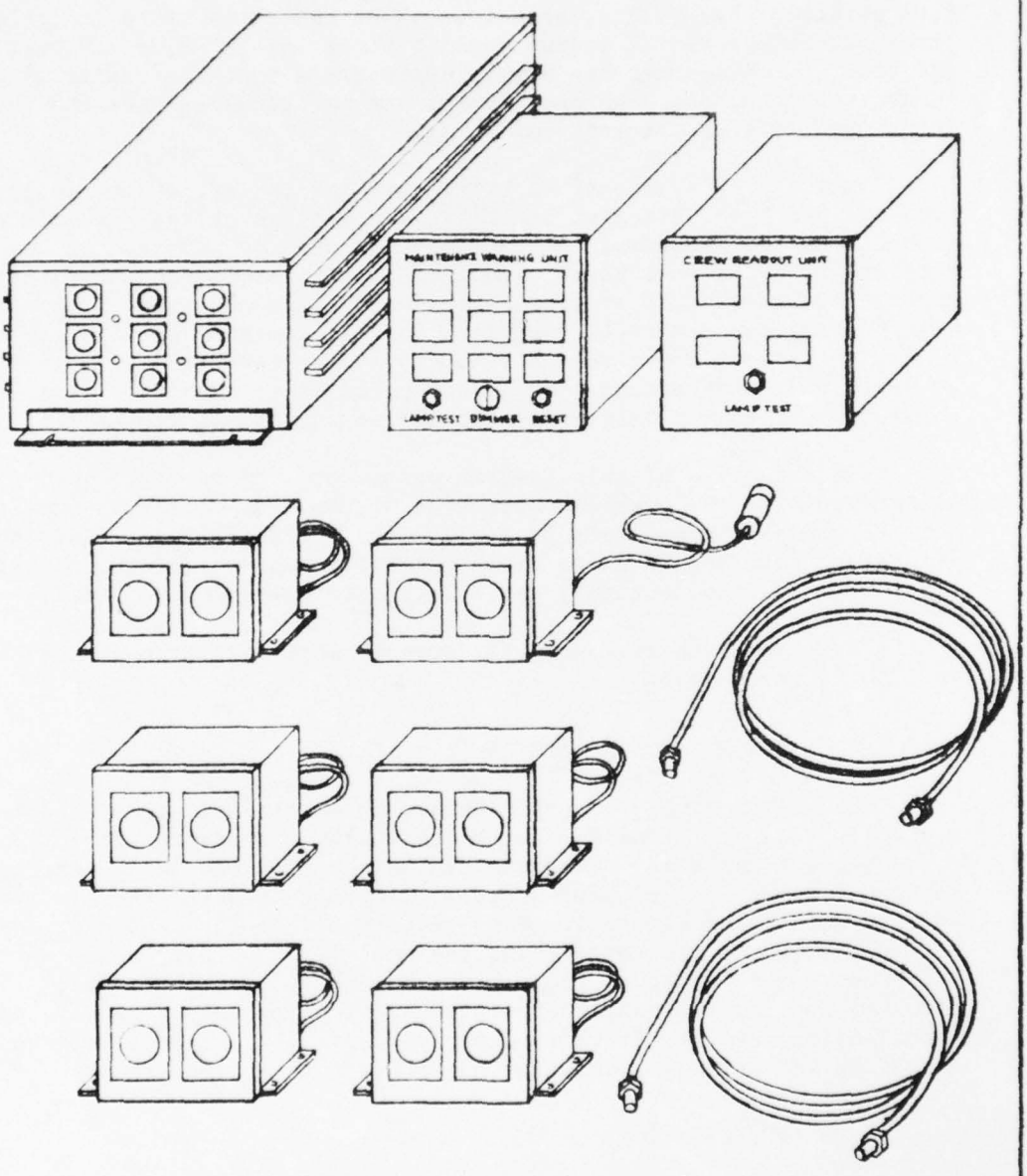


Figure 1. The Integrated Fire and Overheat System

3.1 Response to Flame

Each engine nacelle is monitored by all six flame detector heads of the IFOS. If one or more of these heads detects a flame, the FIRE indicator on the Crew Readout Unit (CRU) is turned on. The sensitivity of each head is such that a burning 5-inch diameter pan of gasoline or JP4 fuel is readily detected at a distance of 4 feet. The FIRE indicator comes on within .5 second of exposure to flame, and goes out within 1.5 seconds of removal of the flame.

3.2 Flame Detector Self-Checking Features

Each detector head is furnished with a small UV source lamp. This lamp is automatically energized for .1 second every 14.4 seconds. If a sensor tube does not respond normally, an indicator, numbered to correspond to the sensor tube, is energized on the Maintenance Warning Unit (MWU).

Normally, both sensor tubes in any one detector head respond to the same flame. If only one tube of the pair generates an output, this is disregarded as being false if the other tube had a normal response to the most recent test. If, on the other hand, the second tube had not responded normally to the most recent test, then the output from the first tube is taken as indicating a fire, and the FIRE indicator is energized.

It is planned that the six flame detector heads will be deployed in such a manner that any fire will cause an output from at least two adjacently-numbered heads. (Numbers considered to be adjacent are 1 and 2, 2 and 3, 3 and 4, 4 and 5, 5 and 6, and 6 and 1.) The system is designed so that if all four sensor tubes in any two adjacent heads fail, the FIRE FAIL indicator of the Crew Readout Unit will be activated by means of a latching relay. This relay can be reset only by pressing the RESET button on the MWU. Also, the relay prevents the FIRE indicator from being activated by any head until the relay is reset.

3.3 Response to Overheat

In addition to the six flame detector heads, each engine nacelle is monitored by a dual-loop overheat cable. This consists of two fifty-foot Edison thermistor cables, installed side-by-side.

If any portion of both cables is heated to a temperature of 398.8°C (750°F ±37.5°F), then the OHEAT (overheat) indicator of the CRU is energized. The alarm is given within 5 seconds of the application of an 815.5°C (1500°F) overheat condition, and is extinguished within 30 seconds of the removal of the overheat condition.

3.4 Overheat Detection Testing

The electrical continuity of each cable is tested once every 14.4 seconds. If a cable is "open," that is, does not exhibit electrical continuity, the appropriate CABLE indicator is energized on the MWU. Also, a very sudden decrease in cable resistance at any time is taken to indicate a defect in the cable of the "short circuit" type, and again the appropriate

CABLE indicator is energized. (An overheat condition is distinguished from a cable short by the fact that the former causes a more gradual decrease in cable resistance.)

Normally, both cables respond in the same way to a given overheat condition by virtue of their side-by-side physical configuration. If only one cable of the pair generates an output, this is disregarded as being false if no defect has been detected in the other cable. If, on the other hand, an open circuit or a short circuit has been detected in the second cable, then the output of the first cable is taken as indicating an overheat condition and the OHEAT indicator is energized.

If both cables are found to be defective, the OHEAT FAIL indicator of the CRU is energized by means of latching relays. These relays can be reset only by pressing the "RESET" button on the MWU. Also, these relays prevent the OHEAT indicator from being activated until the relays are reset.

3.5 Other Self-Checking Features

Part of the electronic circuitry between the sensors and the indicator lamps is automatically tested every 14.4 seconds. If signal continuity is not verified, the CCU (central computer unit) indicator on the MWU is energized.

The output voltages of the various power supplies of the Central Computer Unit are continuously monitored. If the supply voltage for the UV sensor tubes rises above 850V or falls below 750V, then the FIRE FAIL AND OHEAT FAIL indicators of the CRU are energized, as is the CCU indicator of the MWU. A similar response is obtained if a failure occurs in the 300V supply, the +5V supply, or the -5V supply.

Since the IFOS logic circuits are of the synchronous type, an electronic timing clock is employed. The clock oscillator is continuously monitored, and its failure will result in the energization of the FIRE FAIL, OHEAT FAIL and CCU indicators.

If the primary power supply to the entire Central Computer Unit is interrupted, the FIRE FAIL and OHEAT FAIL indicators are activated.

Although the IFOS has a high level of reliability achieved by redundancy and self-checking circuitry, it is not completely protected against all types of failures such as an indicator lamp failure or a relay contact failure.

3.6 The Maintenance Warning Unit

The MWU is designed to indicate to service personnel when maintenance work on the IFOS is needed, and to provide some diagnosis of the trouble.

There are twelve UV indicators, one for each of the twelve sensor tubes. Each indicator is activated if its sensor tube does not respond to the test signal described under 3.2, above.

There are two "Cable" indicators, labeled CABLE A and CABLE B. If a cable tests "open," or if a shorted cable is inferred (see 3.4), then the appropriate cable indicator is activated.

The remaining indicator on the MWU is labeled CCU for Central Computer Unit. This indicator is activated when the 800V power supply voltage rises too high or falls too low, when the -5V or the +300V power supply fails, when the clock oscillator stops, or when various automatic electrical tests of the signal circuitry indicate a fault.

All of the indicators on the MWU are activated by latching relays. Once closed, these relays remain closed until intentionally opened by pressing the RESET button on the MWU front panel. Thus, fault indication is retained even when the electrical power is turned off, and even if the fault is intermitent in appearance.

3.7 Power Requirements

The IFOS is designed to operate from a direct current power source with a potential difference of from 18 volts to 30 volts. Approximate standby current requirements for a 28 volt source are:

CCU:	1.2 ampere
MWU:	.120 ampere
CRU:	.035 ampere

3.8 Temperature Range

Operating and storage temperature ranges for the various components of the IFOS are:

	Operating	Storage
CCU	-40°C to 85°C	-65°C to 150°C
MWU	-40°C to 71°C	-65°C to 150°C
CRU	-40°C to 71°C	-65°C to 150°C
UV Heads	-54°C to 260°C	-65°C to 260°C
OH Cables	-54°C to 815.5°C	-65°C to 815.5°C
Connection Cables	-54°C to 110°C	-65°C to 110°C

Additionally, the UV heads are designed to withstand 1093°C for one minute.

3.9 Other Environmental Specifications

The CCU, the UV heads, and the connecting cables are designed to operate at all altitudes from sea level to 70,000 feet. These units are also designed to withstand salt water spray, 20g of shock, and high humidity, as specified in MIL-STD-810A. All sections of the IFOS are designed to perform satisfactorily under 15g of vibration.

Compliance with MIL-STD-461A* insures freedom from electromagnetic interference.

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*Certain sections of this Standard were waived by the Air Force for the delivered equipment.

3.10 Size and Weight

Approximate dimensions and weight of each IFOS component is shown in Table 1. These dimensions neglect the protruding cable connectors and mounting brackets.

3.11 Maintenance Aids

The MWU, discussed in 3.6 above, is the primary diagnostic aid. A test jack is provided on the CCU to enable service personnel to quickly measure twenty-one critical voltages without opening the case.

Table I

Dimensions and Weights of IFOS Components

Component	Dimensions	Weight
CCU	7-1/2" x 12" x 19"	30 lbs., 13 oz.
MWU*	6" x 6-1/4" x 9-1/2"	6 lbs., 11 oz.
CRU*	5-1/2" x 5-1/2" x 8"	4 lbs., 4 oz.
Flame Detector Head	4-1/4" x 3" x 3"	2 lbs., 2 oz.
Overheat Cables**	---	1 lb., 7 oz.
Detector Cable	---	3/4 oz/ft

*Not including shock mounts, mounting plates and straps

**Two cables, each composed of three 16-foot cables in series.

II

FLAME DETECTOR HEAD

1. THE EDISON U/V SENSOR TUBE

1.1 The heart of the IFOS flame detector head is the patented Edison ultraviolet radiation detector, shown in Figure 2. This device is essentially an ultraviolet-sensitive Geiger-Mueller counter tube, responding to radiation from 1900 Å to 2900 Å. While such radiation is emitted by flames and arcs, it is seldom found within the Earth's atmosphere from other sources, including the Sun, fluorescent lamps and incandescent lamps. Thus the Edison tube is unlikely to generate a false alarm.

Advantages of the Edison sensor tube over other flame detector devices are many. They include:

a) Freedom from false alarms, as discussed above
b) High sensitivity, due to gas amplification within the tube
c) Proven reliability
d) Low cost
e) Ability to operate over an extreme temperature range
f) Rapid response
g) Repeat capability, which is ability to operate during successive fires
h) Mechanical ruggedness (with regard to shock and vibration)
i) No sensitivity to humidity, wind, or changes in atmospheric pressure
j) A large output signal

Disadvantages of these sensors are:

a) High-voltage power supplies are necessary for tube biasing
b) The sensitivity of the sensor decreases with increasing temperature
c) The tube characteristics change somewhat with aging and storage
d) A thin film of oil or gasoline between the tube and a flame absorbs much ultraviolet light and thus greatly reduces sensitivity. (Such a film might occur, for example, when engine oil or fuel is sprayed onto a tube envelope.)

Edison Electronics, at present, manufactures two different types of sensor tubes, the Mark I and the Mark II. A specially-screened Mark II tube is used for the IFOS. The following are some of the details of the sensor tube's construction:

Outside Diameter:	1.125 inches
Overall Length:	1.625 inches
Glass Envelope:	Ultraviolet transmitting glass
Glass Stem:	7720 Nonex
Stem Leads:	Nickel-tungsten
Electrodes:	Tungsten

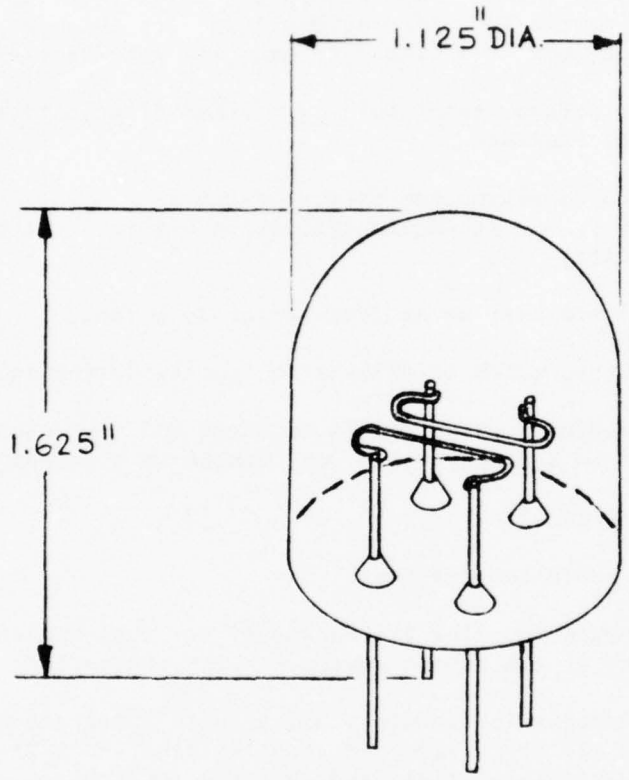


Figure 2. The Edison U/V Sensor Tube

Further details of tube construction and theory of operation can be found in references (1) - (3).

1.2 Circuit Properties

Figure 3a shows a basic circuit for Geiger-Mueller tubes. The signal output consists of random electrical pulses when the tube is struck by weak radiation. Intense radiation may cause the tube to conduct continuously. The series resistor is always necessary to permit "quenching" of the tube--that is, restoring the tube to its original condition after each discharge.

Three simple variations of this circuit are shown in Figures 3b, 3c and 3d. Also, small capacitors can be added in various places to modify such characteristics as pulse width. The circuit of Figure 3d is used for the IFOS.

Important dynamic properties for this sensor circuitry include:

a) Sensitivity to ultraviolet radiation from a flame.
b) Response to sunlight, hereafter referred to as "long-wave response."
c) Output resulting from cosmic rays and environmental radioactivity, referred to as the "background count."
d) Output resulting from no discernible cause, referred to as "self-excitation."
e) Occurrence of "multiple counting," where one discharge leads to a chain of one or more following discharges.

These dynamic properties are a function of the supply voltage, the tube temperature, the values of circuit resistance and capacitance (stray or intentional), the past history of the tube with respect to storage and usage, and the individual tube--different tubes of the same lot number vary somewhat in their characteristics. The basic design problem was to devise an arrangement which, under all operating conditions, has satisfactory sensitivity and freedom from false alarms. This problem was solved by a combination of tube screening, circuit design, and signal processing.

It was found that adequate sensitivity to ultraviolet radiation could be obtained by screening the sensor tubes at worst-case conditions (see section 1.3). Self-excitation problems were eliminated by using an 800-volt square wave to bias the sensor tube, rather than the usual direct current. The "multiple count" problem was greatly alleviated by use of a nonretriggerable monostable circuit which is triggered by the first pulse of a train of pulses, and which blanks out closely-following pulses.

The longwave response problem and the background-count problem were eliminated by additional screening of the sensor tubes and by use of a digital pulse counter. This counter circuit gives an output signal only if eight or more counts are received from the sensor tube in a period of 2.4 seconds.

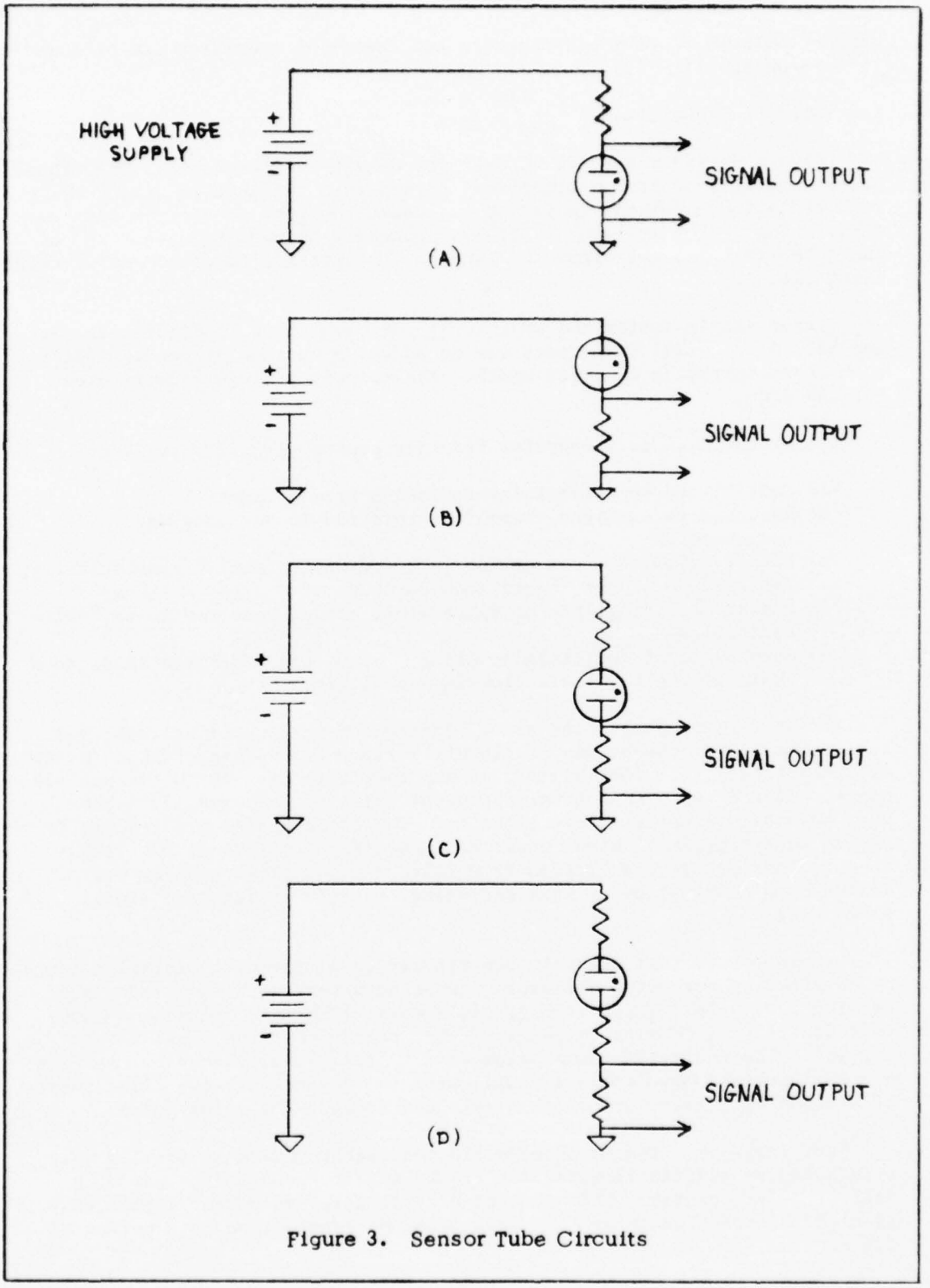


Figure 3. Sensor Tube Circuits

Figure 4 shows a simplified schematic of the circuitry associated with each sensor tube. The two comparators amplify the pulse outputs from the sensor tube to a standard five-volt level, while the functions of the monostable and counter circuits were described above. The operation of the circuitry is described more fully in section 1.2 of Chapter IV.

1.3 Sensor Tube Screening

Edison sensor tubes for use in the IFOS are screened by two separate procedures. One procedure is to insure adequate sensitivity to flame and the other is to insure adequate freedom from false alarms. For both procedures the circuit of Figure 4 is used, with an electronic digital counter attached to point X.

To screen the tubes for adequate flame sensitivity, each tube is placed with its electrodes twelve inches from a standard propane flame. (This is a flame of pure propane gas burning in air, the gas emitted through a .02 inch orifice, and with pressure adjusted to give a flame 1-3/4 inches high.) The tube is operated under the highest design temperature 260°C (500°F) and the lowest design supply voltage (750V), since these represent worst-case conditions for sensitivity to U/V light. Tubes are accepted for service only if they supply at least fifty counts per second to the digital counter.

IFOS specifications require that the system respond to a five-inch diameter gasoline flame four feet away within one-half second. Now it has been found that a sensor tube which gives fifty counts per second from a standard propane flame will give 31.25 counts per second from the above gasoline flame. In one-half second, which is the desired maximum response time, about sixteen counts would result. Thus, a fire alarm would be generated,* as only eight counts are needed in a 2.4 second interval.

Unfortunately, there are some complications to this argument. First, the count rate is subject to statistical fluctuation, due in part to the random nature of photon bombardment of the sensor tube. Thus, even though the <u>average</u> sensitivity of the sensor tube is 16 counts per .5 second, during <u>some</u> .5 second intervals less than 16 counts will be received. Second, there is the fact that every 2.4 seconds the digital counter of Figure 4 is reset to zero. Now if a fire starts just before the reset pulse, the counter might be reset to zero before eight counts are accumulated, and thus perhaps 15 counts would be required in the .5 second period to give a fire alarm. Third, there is the fact that the clock rate of the IFOS might possibly differ by as much as 20% from the design value, changing the 2.4 second reset time to 1.92 seconds, leading to a further lengthening of average response time. Fourth, one must take into account the fact that the system is disabled (for testing) for .12 seconds every sixth reset time. This, too, will lengthen average response time.

By assuming that the counts obtained in a given time interval follow the well-known Poisson distribution function, it is possible to calculate

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*It is here assumed that the other sensor tube in the head has failed, and thus only one tube is needed to generate the fire alarm.

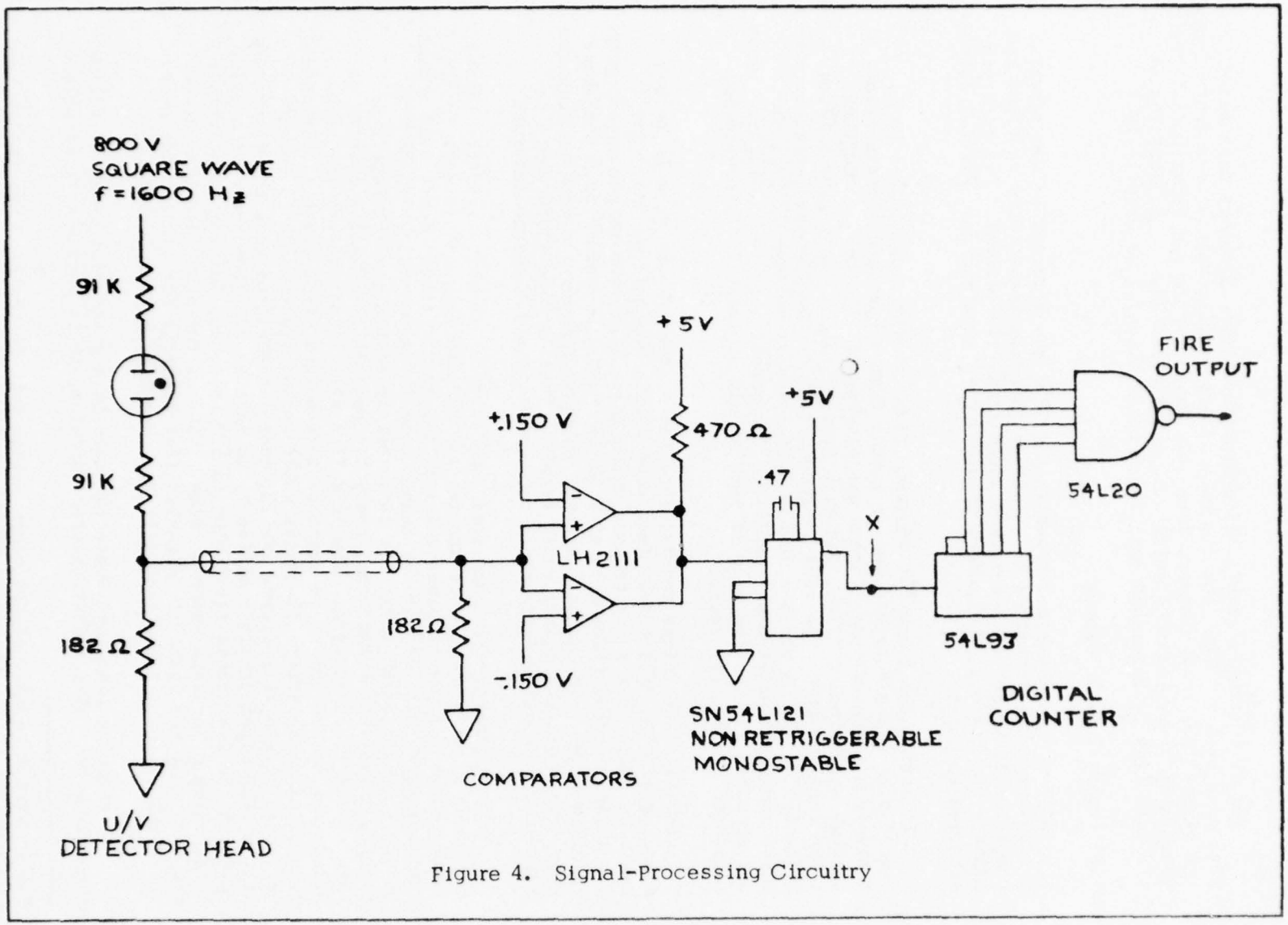


Figure 4. Signal-Processing Circuitry

the probability that a fire warning will be obtained within .5 second. These calculations are given in Appendix I, and indicate that the fire alarm will be given in .5 second 94.3% of the time. To confirm these calculations, a number of experimental response time measurements were made. There was excellent agreement between the calculations and the measurements.

Now with both tubes in one head required to generate an output for the fire signal to be given, the probability of rapid (.5 second) response will be a few percent less, since a fire signal must await the slower of the two sensor tubes. But with two separate heads responding to the same fire (the normal case), the probability of rapid response will be greater than 99%, as here the faster head will generate a fire signal.

It should be noted that these calculations are for worst-case conditions, where the sensor tube is operated at maximum temperature and minimum voltage. It is also assumed that the sensor tube has the minimum acceptable sensitivity, and that the fire is of minimum intensity and maximum distance from the head. Under average conditions, response to a fire will be obtained within .5 second virtually 100% of the time.

To screen the sensor tubes for freedom from false alarm, each tube is placed with its electrodes twelve inches from a light source which simulates intense sunlight. (This is a 200 watt tungsten-halogen lamp with a 2 mm thick Corning 054 filter.) The tube is operated with the highest design supply voltage (850V), since this represents worst-case conditions for the generation of pulses from the longwave response, from background counting and from self-excitation. Tubes are accepted for service only if they register not more than 5 counts in a ten-second test interval, the tests being made at both -53.8°C (-65°F) and 260°C (500°F).

Now 5 counts in ten seconds implies 1.2 counts in 2.4 seconds, whereas 8 counts are needed to generate a fire signal. However, again there is statistical fluctuation of the number of counts, and during many 2.4 seconds, three or more counts will be received. Further, the clock rate of the IFOS might possibly differ by 20% from the design value, changing the 2.4 second receptive time to 2.88 seconds, and thus increasing the number of counts registered.

By assuming that the 5 counts per ten seconds follows a Poisson distribution, the probability of a false alarm can readily be determined. This calculation is made in Appendix II, where it is found that the average time between false alarms is 6.04 hours if one tube can generate a fire alarm and 46,000 hours if both sensor tubes in a given head are needed to generate a fire signal, as is the normal condition. With six fully functioning flame detector heads in one system, the average time between false alarms becomes 7,666 hours.

It should be noted that these false alarms calculations are for worst-case conditions. Specifically, it was assumed that the sensor tube barely passed the screening procedure, that it was operated at maximum supply voltage, and that it was pointed directly at the sun when the sun was directly overhead. Average conditions of sunlight, tube voltage,

and tube screening would lead to far larger time figures than those given above.

2. U/V SOURCE LAMP

2.1 In order to periodically test the Edison U/V sensor tubes, a U/V source lamp is included in each detector head. This lamp is activated for a .1 second every 14.4 seconds.

At the start of this program, a satisfactory source lamp could not be found, and so it was necessary to develop a suitable lamp. A special, high-filament-temperature incandescent lamp was considered, but it was felt that a gas-discharge lamp would be more reliable.

Problems encountered in the design of this discharge lamp included wandering of glow spot and unstable operation at 260°C (500°F). Wandering of the glow spot results in variation of the U/V output and changes in the starting voltage. This problem was overcome by adding a nickel cross-bar to the cathode rod and by covering most of the cathode rod with glass beading. Unstable operation at high temperature was eliminated by use of a getter to absorb certain gas impurities.

The final design of the source lamp is shown in Figure 5. A neon-argon mixture is used as the fill gas.

2.2 Developmental Tests

Two lamps were put on continuous operation at 5 ma life test at 260°C (500°F). One lamp gave approximately the same U/V output at 214 hours operation as it did at the start. The U/V output of the second life test lamp was down 25% after 266 hours continuous operation at 260°C (500°F). This is considered more than adequate as one hour of continuous lamp operation is equivalent to 150 hours of system operation where the lamp is energized for 0.1 second four times a minute. Other lamps which were run on pulsed operation at 260°C (500°F) for up to 64 hours showed negligible change in U/V output. A sample of the lamps was also evaluated for performance at cold temperature and no appreciable change in U/V output being noted after one hour continuous operation at -54°C (-65°F).

Two U/V source lamps together with a sensor tube were vibrated up to 500 CPS at 15 g's input for three hours in each of three orthogonal planes. During vibration scanning no resonances were found; and there were no visible mechanical defects or degradation of the lamp or sensor tube performance after the vibration.

2.3 Lamp Selection

As part of the screening process, each source tube is pulsed with a 300V pulse, .1 second wide, connected through a 37KΩ resistor. It is placed six inches away from a Mark II sensor tube of minimum acceptable sensitivity, connected into the circuit of Figure 4. Acceptable source tubes must give at least fifty counts at both -54°C (65°F) and 260°C (+500°F).

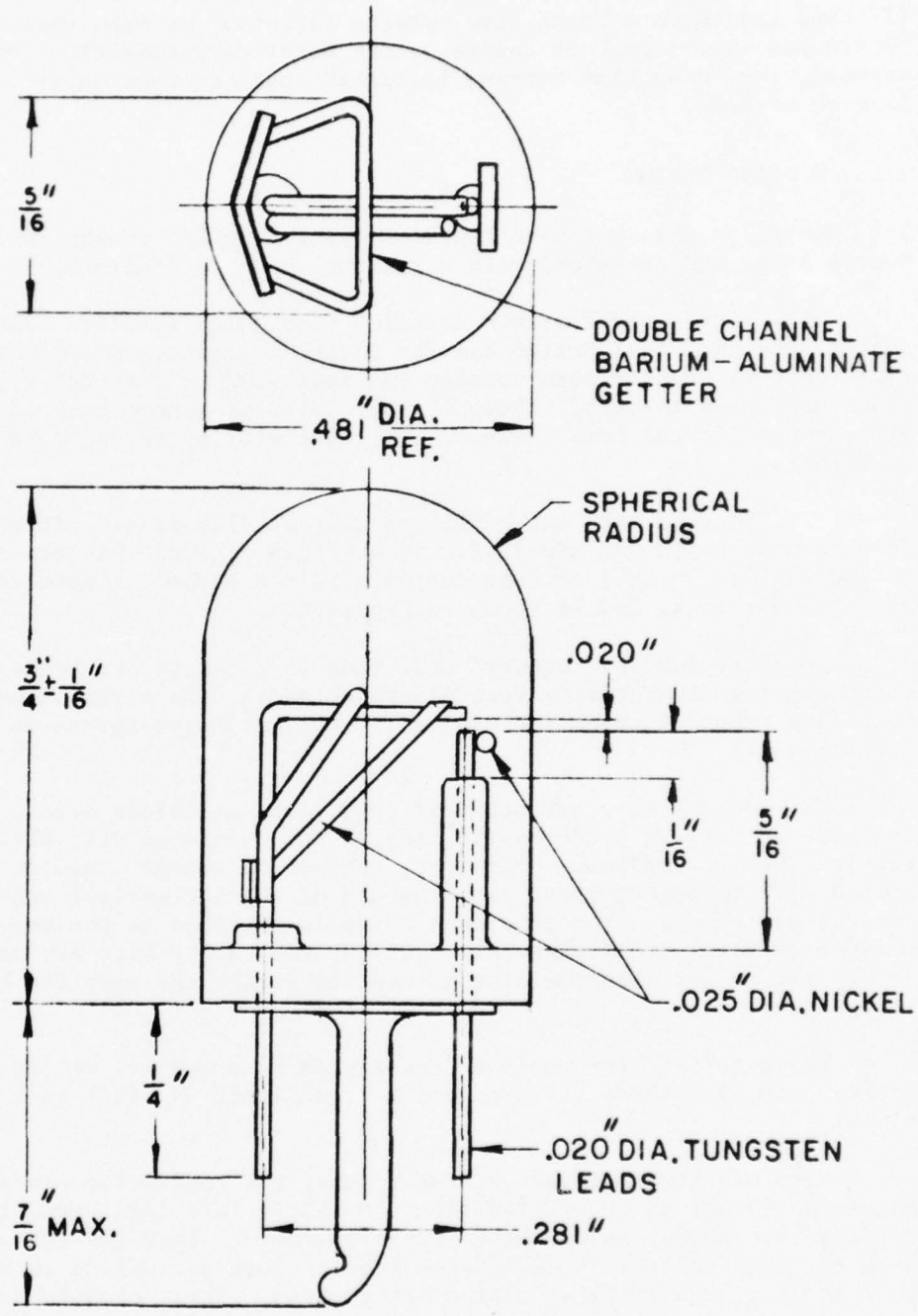


Figure 5. U/V Source Lamp

During actual IFOS operation, the pulsed source tube must cause each sensor tube to give at least eight counts for that tube to "test good." Because of statistical variations, a source tube, which causes an average count of fifty per .1 second, will sometimes give considerably fewer counts. By assuming a Poisson distribution, one can calculate how often fewer than eight counts will occur. This calculation is made in Appendix III, and indicates a "mean time between failures" of more than 133 days of continuous operation. Of course, since worst-case conditions were assumed, the "mean time between failures" under average conditions would be much greater.

3. HOUSING DESIGN

3.1 The flame detector head contains two Edison U/V sensor tubes, one U/V source lamp, and the electronic circuitry shown in Figure 6.

Shown in Figure 7 is the detector head which resulted from the first design attempt. This design has the desirable feature of requiring light from the test lamp to pass through the same windows that U/V light from a flame must pass through. Thus, if these windows become covered with oil or dirt, rendering the head useless, this fact will be detected by the periodical tests.

The Figure 7 head was built and successfully passed vibration tests in accordance with MIL-STD-810B. It was then decided that the size and weight (3 lbs. 10 oz.) of this design were too large. A reduced size head was then designed, and is shown in Figure 8.

To carry out the required reduction in size, it was necessary to eliminate the desirable feature discussed above, where the light from the test lamp passes through the windows. (The Air Force agreed to waive this requirement.)

The housing is constructed of passivated stainless steel. Windows are made of optical grade quartz, sealed and cushioned with RTV8262 silicon rubber adhesive/sealant. Electronic components are attached to a glass-bonded mica component board with the aid of the RTV sealant and a high-temperature solder. The component board is attached to the housing by means of screws with lockwashers. Screws and safety wire are used to attach the cover. Spot welding is used to attach the mounting brackets to the housing.

The detector head would be redesigned as a sealed, welded unit, thereby removing the potting material from direct exposure to the 2000°C flame.

When U/V light strikes a sensor tube, the ionization process within causes U/V light to be emitted from the tube. This light can, in turn, be detected by another sensor tube in the vicinity. Thus the two tubes in the detector housing could trigger each other. Such a coupling is very undesirable and can lead to false alarms being given. Thus, each tube is coated with RTV adhesive in such a way that only U/V light entering through the windows or from the test lamp will also enter a sensor tube.

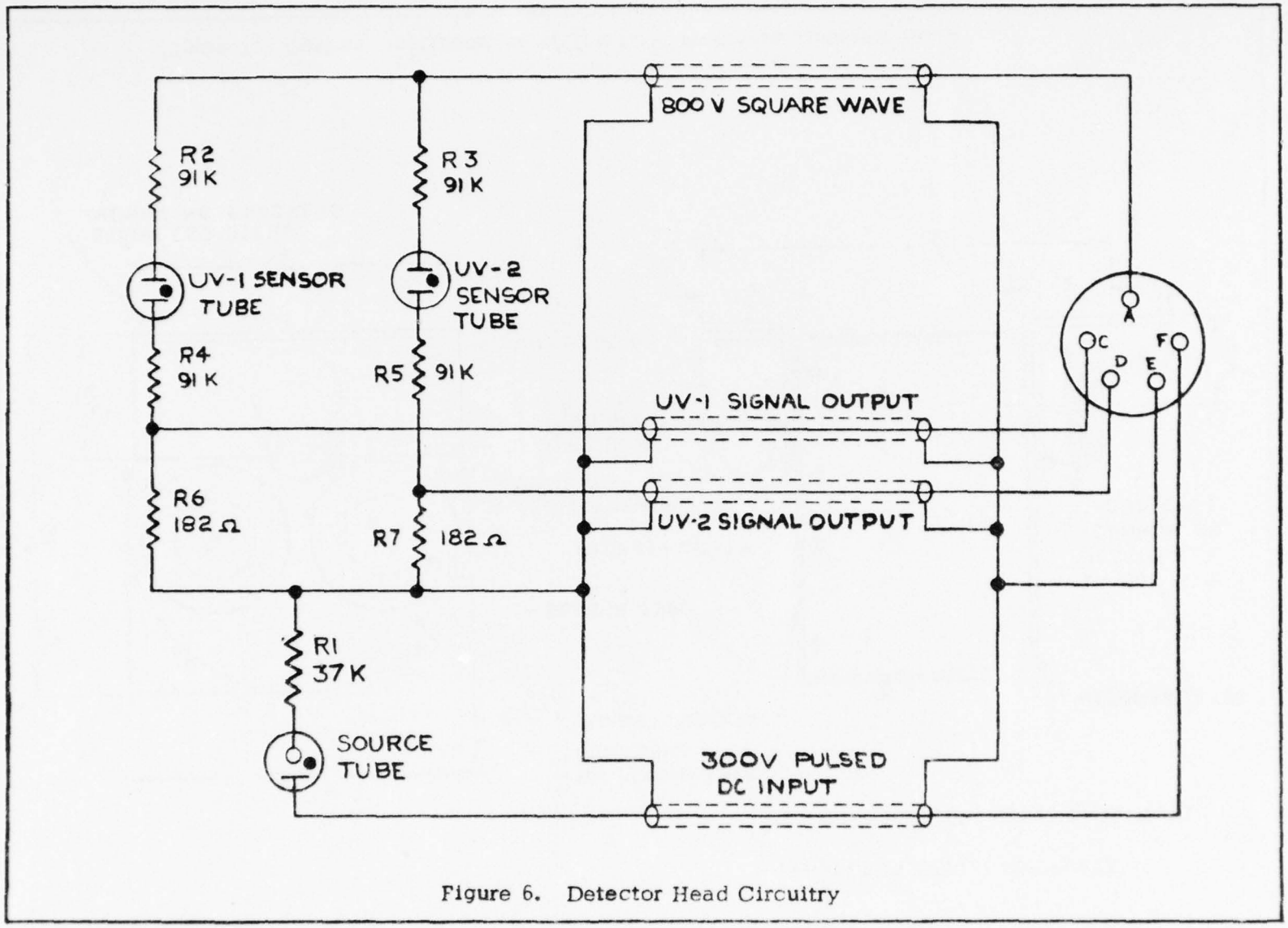


Figure 6. Detector Head Circuitry

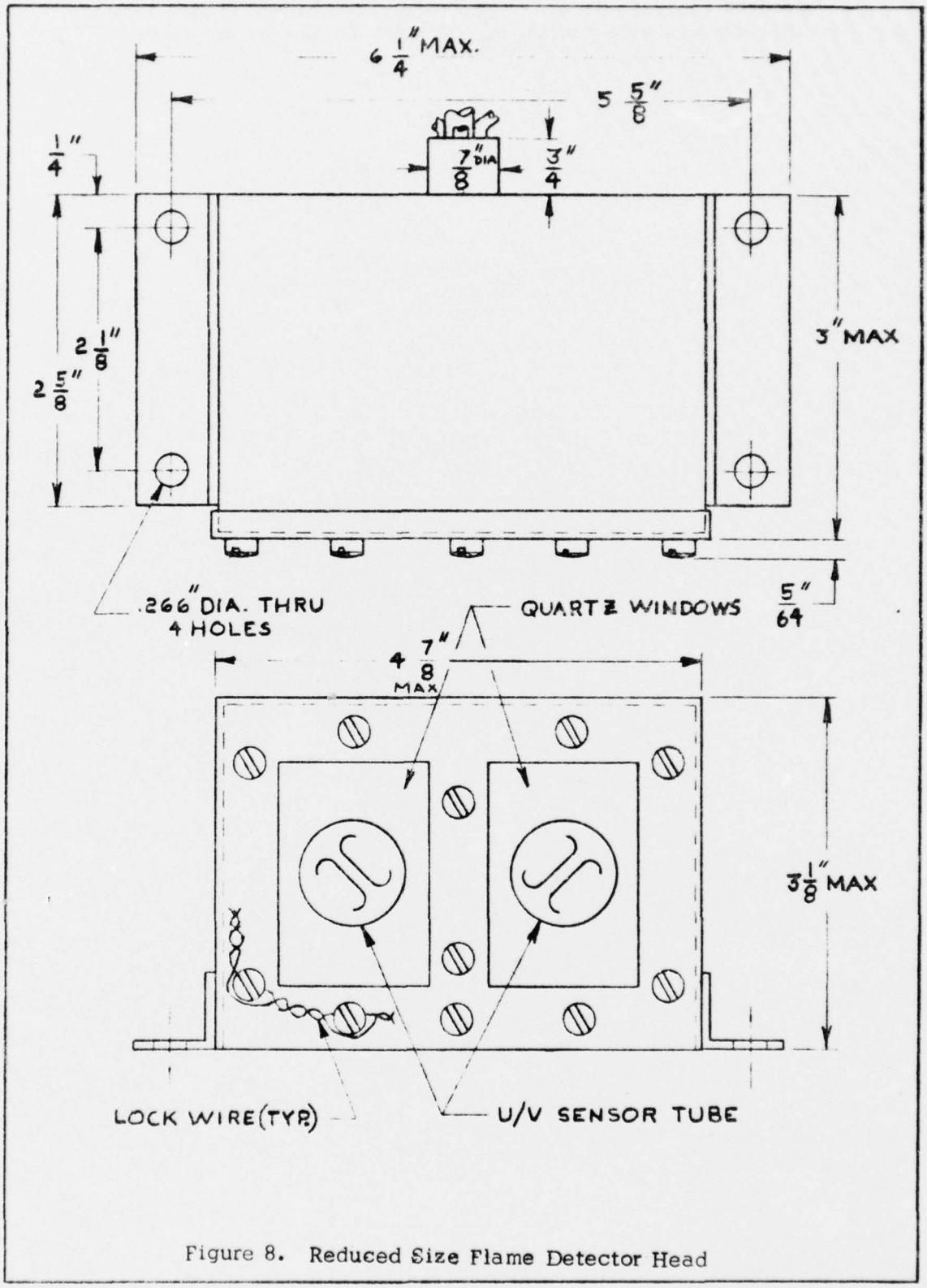


Figure 8. Reduced Size Flame Detector Head

Cathode sputtering in the test lamp can cause an opaque deposit on the glass opposite the cathode area. The test lamp is positioned in such a way that this deposit will not block U/V light to the sensor tubes.

III

THERMISTOR OVERHEAT SENSOR

1. SENSOR DESIGN

Aircraft overheat detection system requires sensors which provide safe and reliable overheat detection with a minimum of shorts or opens. The sensor used in this contract was the Edison Model 244 which, because of its ruggedness and operational stability, has produced an excellent service record in the field.

The Edison Model 244 sensor is of coaxial cable construction and consists of a tubular dual-wall outer sheath, a center wire and a compacted temperature-sensitive semiconductor filler material. Operating on the electronic conduction principle, the Edison cable does not depend on any physical change of the temperature-sensitive material within the cable, ensuring therefore excellent operational reversability which enables the cable to present normal and overheat conditions repeatedly.

2. DESCRIPTION OF OPERATION

The semiconductor material contained in the Edison thermistor-type cable is a proprietary blend of oxides of manganese and yields a temperature resistance curve with a large slope which enables the sensor to detect hot spots while at the same time permitting temperature averaging to evaluate normal high ambient temperature areas. In principle, the filler or core material being essentially an insulator at room temperature, becomes a good conductor when heated to some predetermined higher temperature. Conduction is by electrons and thus the sensor resistance can be measured by application of a D.C. voltage. This is a distinct advantage over sensors which depend upon ionic conduction and, therefore, must be operated from AC voltages and are more sensitive to moisture.

For the purpose of system design the sensor cable is considered as a resistive element which is an inverse function of cable temperature.

3. IMPEDANCE

A common way of testing continuous cables is to expose the entire length to a predetermined oven temperature and measure cable impedance between center wire and sheath with an ohmmeter. This technique suffices as an acceptance test of a finished cable because any abnormally low resistance section along the cable length registers markedly on the total parallel impedance.

By performing this procedure on one small section of the cable at a time, along the entire cable length, data from excessively high or low resistance sections will not conceal or overshadow normal temperature characteristics, or variations in these characteristics arising from variations in fabrication or processing.

Standard practice at Edison is to test a six-inch section every two feet along the length of the cable. This technique yields an accurate profile of cable resistance and reveals all but the most localized resistive extremes. Normal variations in resistance are generally due to non-uniformity of the cable cross-section along its cable length causing variations in filler thickness. Localized variations in cable resistance may be due to moisture ingress at a leaky end seal, inhomogeneities in the oxide mix or loss of a chip of oxide from the extrusion.

Plots of cable resistivity (ohm-feet) versus temperature for a family of cables with various characteristic temperatures (the temperature at which the resistivity is 5000 ohm-ft.) are shown in Figure 9.

The relation between resistance and temperature is similar to the resistance of many thermistor-type semiconductors over considerable ranges. The resistance at a given temperature can be determined accurately by the equation:

$$R = R_o \exp(B/T)$$

where

T = absolute temperature in Degrees Rankine

R = resistance in ohm-feet at temperature T

R_o = constant in ohm-feet

B = slope of the temperature resistance characteristic

Here cable resistance increases to a very high level but, being limited by the electrophysical properties of this cable, does not become infinite as the equation would imply. As temperature approaches infinity, the minimum value of cable resistance is limited by the resistance of the center wire and sheath and does not become zero.

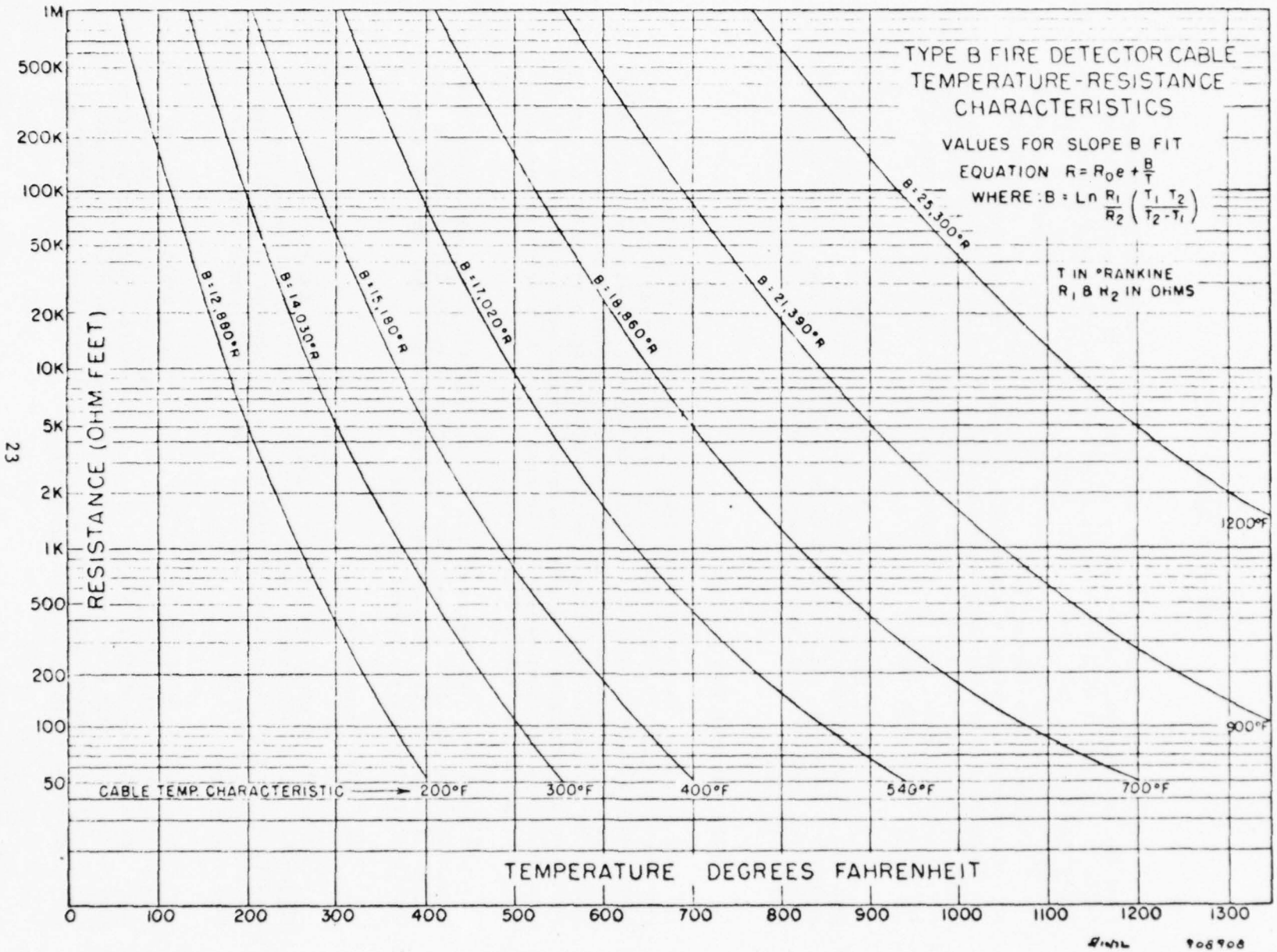


Figure 9. Cable Temperature-Resistance Characteristics

IV

COMPUTER CONTROL UNIT

The computer control unit has the function of correlating signals from the dual overheat sensor cables and from the six radiation detector heads in accordance with predetermined operational constraints and providing signals to the crew readout unit and to the maintenance warning unit. The computer control unit contains a transient suppressor network, a power supply regulator, voltage monitors, a clock as well as signal processing and correlating circuitry for both the overheat and radiation sensors. The computer control unit was designed to operate in an ambient temperature range of -40°C (-40°F) to 85°C (185°F) in a military environment. The detailed specific requirements of the computer control unit are delineated in Section I of this report.

Much of the signal processing circuitry is of the digital type, based on TTL integrated circuits. Positive logic is used to describe the operations involved, and so a Boolean ONE indicates voltage levels in the range from 2.0V to 5.5V, while a Boolean ZERO indicates voltage levels from OV to .8V.

1. FIRE AND FIRE-FAIL SECTION

1.1 As discussed in the Introduction, fire detection is achieved by the employment of six flame detector heads. Each head contains two U/V sensor tubes and a U/V source lamp for testing the sensors. A fire warning should be generated when both sensors in any head have tested good and when both give an output signal resulting from fire U/V radiation striking the sensors. An output signal from only one sensor should not result in a fire warning unless the other sensor in the head failed to respond to the test lamp during the most recent test.

To provide a high degree of reliability against false alarms and fire detection failures, fire signal flow is carried from the U/V sensors to the signal processors, fire warning logic, fire-fail logic, and computer diagnostic logic in twelve parallel channels.

1.2 U/V Signal Processors

Schematic diagrams for the U/V signal processors are found in Figure 10. These processors consist of twelve identical circuits, six located on each of two printed-circuit boards, designated A3 and A4. The operation of the circuit for signal UV11 (from head 1, sensor tube 1) is described below.

When tube 11 is struck by U/V light, it develops positive and negative pulses across its 182Ω load resistor (see Figure 6), located in head one. The amplitude of these pulses is about 250mv with random pulse widths varying up to a maximum of one-half of the period of the 800V square wave used to bias the sensor tube. These pulse signals are transmitted through a coaxial cable to terminal 12 of board A3.

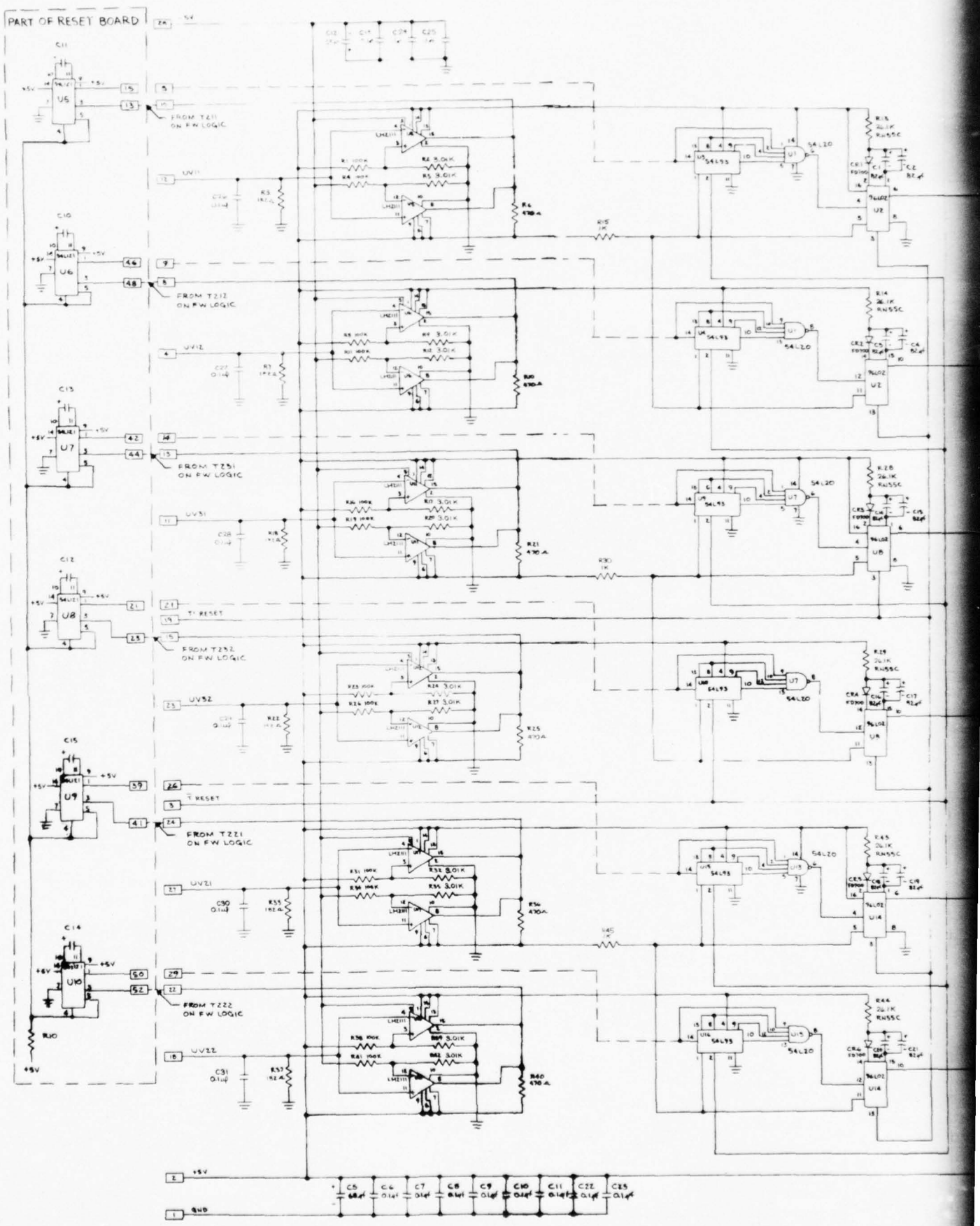
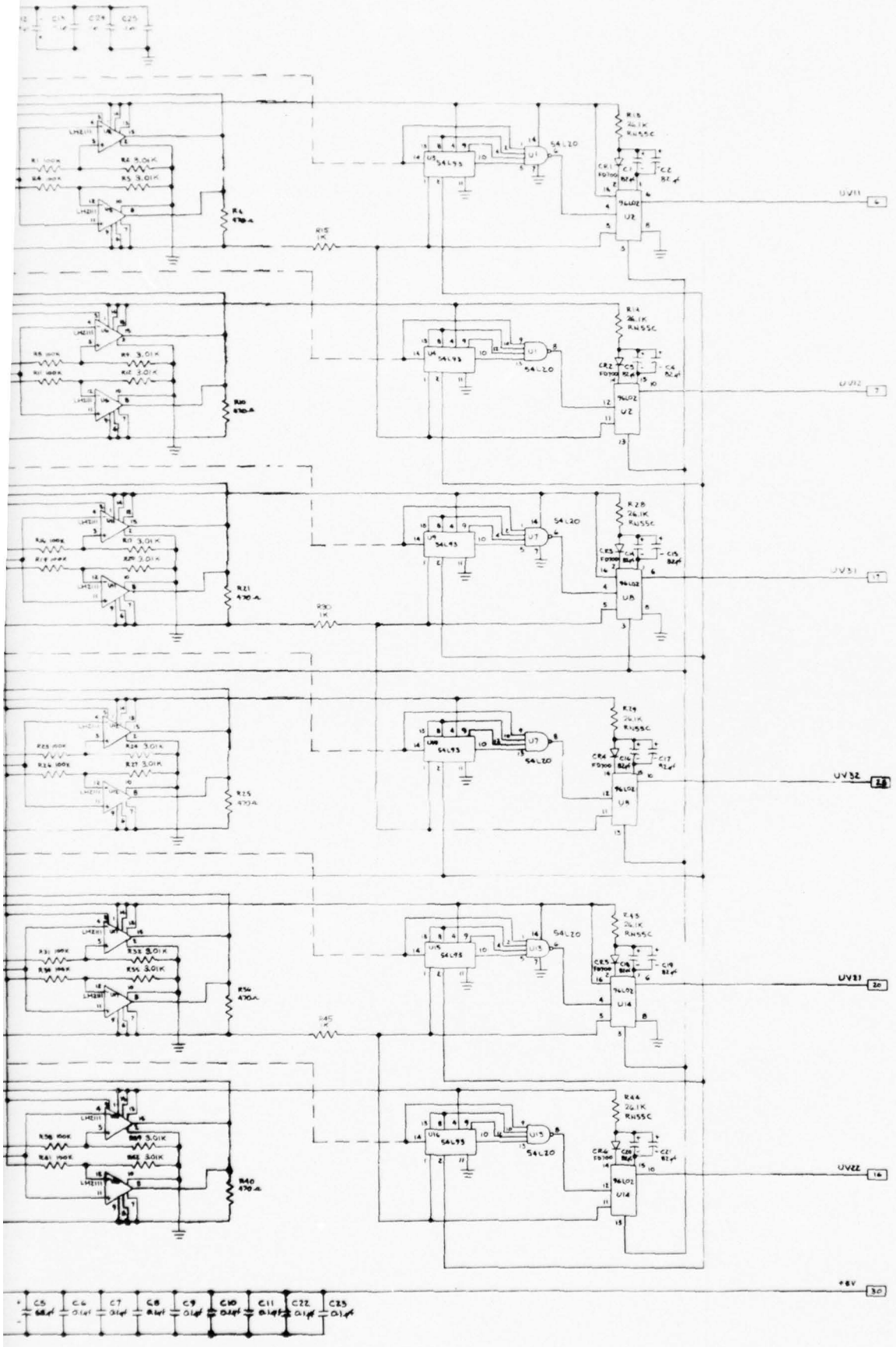


Figure 10. Schematic Wiring Diagram, U/V Signal Processor



atic Wiring Diagram, U/V Signal Processor (A) Board

The dual comparators labeled U5 both amplify and rectify the signal pulses. Their outputs are "wired-ORed" together, and consist of five-volt negative-going pulses based at +5V. Resistors R1, R2, R4 and R5 back-bias the comparator inputs to eliminate signals of magnitude 150mv or less. (Such signals, not originating in the sensor tube, might result from undesired coupling to other circuits.)

Output pulses from the comparators are applied to the input of a nonretriggerable monostable, U5. (U5 is physically located on A5, the "Reset" board.) This monostable converts all input pulses to output pulses of a uniform width, namely 1/3 msec. The nonretriggerable feature alleviates much of the "multiple-count" problem (see section 1.2 of Chapter II). Here, the first pulse of a train of pulses triggers the monostable, which then has no response to the following pulses for at least 1.3 msec.

Under certain conditions, the input to the monostable consists of a group of fifteen pulses originating from the Fire Warning circuits. These pulses, labeled T211, are coupled into the signal processor circuit by means of a "wired-OR" connection. Since the time between each two pulses is one m sec. and the period of the monostable is 1.3 msec., these fifteen input pulses result in only eight output pulses.

The next components in the signal path are a ripple binary counter (U3) and an associated NAND gate, U1. An output pulse results from the NAND gate only after eight input pulses to the ripple counter. A reset signal, labeled $\overline{T}$ RESET, is applied to the counter every 2.4 seconds, and so the NAND will have an output signal only if the eight input pulses are received in the period between the reset pulses. It is this circuitry which prevents a false fire signal resulting from long-wave response, background count and self-excitation of the sensor tube.

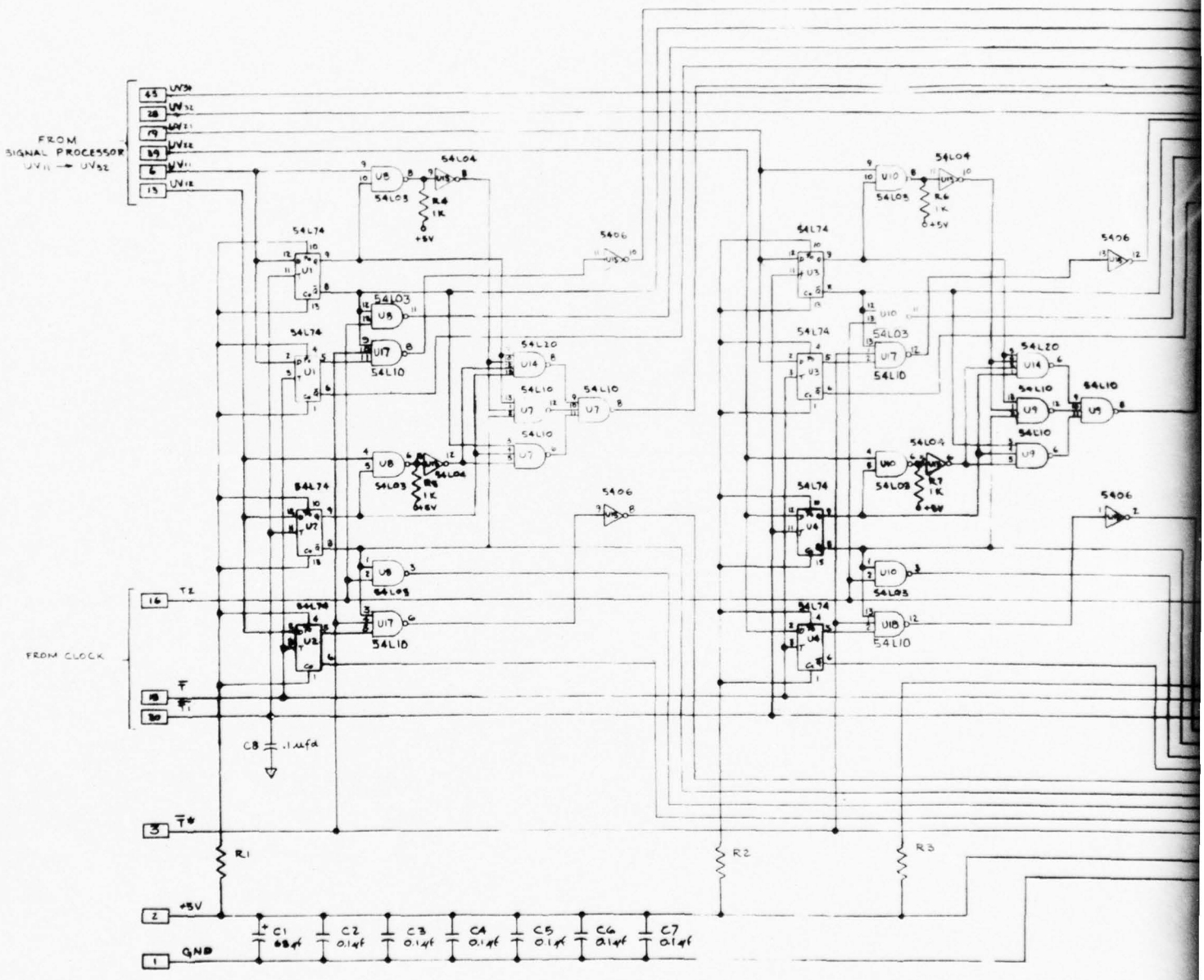
Pulses from the U1 NAND gate are used to trigger the retriggerable monostable U2. Components C1, C2 and R13 set the period of U2 to 1.3 seconds. If U2 receives input pulses not more than 1.3 seconds apart, it will provide a constant, steady output which is insensitive to the random variations in the times between individual input pulses.

Monostable U2 is reset by the signal T' RESET. This signal is a double pulse occuring every 14.4 seconds. The first pulse resets U2 just before the test source lamp is pulsed, and the second pulse resets U2 .12 seconds later, so that no fire indication is given as a result of the test.

1.3 Fire Warning Circuits

Schematic diagrams for the fire warning circuits are found in Figure 11. (This drawing strictly describes the circuitry on the A6 printed-circuit board. The circuitry on the A7 board is identical except for nomenclature.)

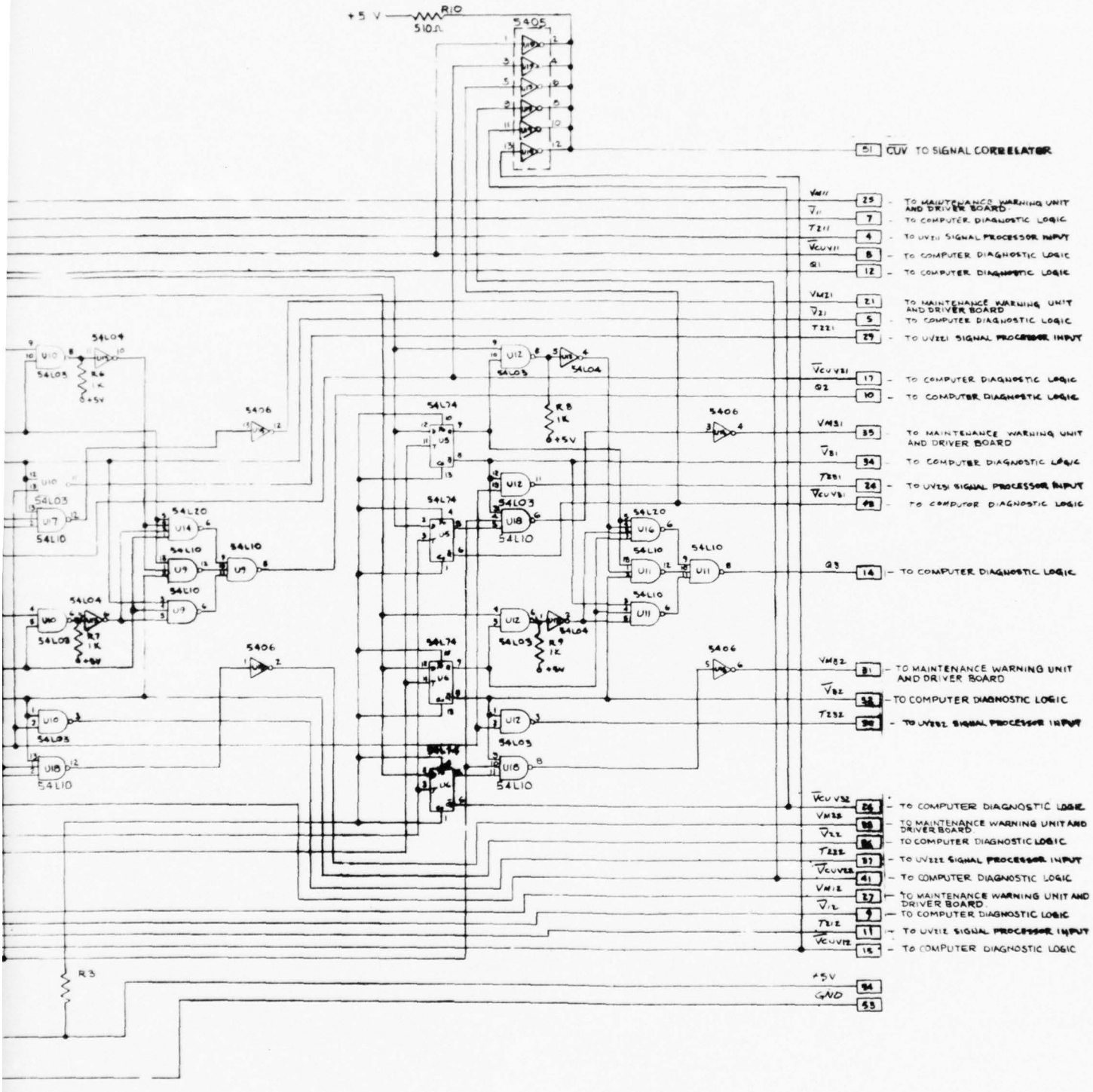
The fire warning circuitry is divided into six identical blocks--one block for each detector head. Further, each block has a symmetry where each half corresponds to one U/V fire signal channel.



NOTE:

1. UNLESS OTHERWISE SPECIFIED, +5V CONNECTS TO PIN 14 AND GND TO PIN 7 OF ALL LOGIC.
2. PIN "1" IS LOCATED ON THE SILVER END OF THE CONNECTOR.

Figure 11. Schematic Wiring Diagram,



matic Wiring Diagram, Fire Fail Logic - U/V Detectors

Each of the six blocks of circuitry uses four timing signals, which are shown in Figure 12 for easy reference. Note that the four flip-flops in each block are of the "D" type, the preset and clear inputs are not used, and date transfer takes place on a low-to-high transition of a clock pulse.

Consider the block of circuitry dealing with detector head number one. The inputs to this circuitry are:

1. The four timing signals of Figure 12, namely $\overline{T}1$, $\overline{T}$, $\overline{T}*$, and T2.

2. Boolean signals from the U/V signal processors, namely UV11 and UV12. A boolean value of ONE indicates that the corresponding sensor tube has responded to U/V light.

The outputs from this circuitry are:

1. Q1: A value of ONE indicates that at least one of the two signal channels has tested good and that a fire has been detected.

2. T211 and T212: If a response to the test lamp in the detector head is not obtained, these pulses are sent back to the U/V signal processors to determine whether the fault is a defective sensor tube or defective circuitry.

3. $\overline{V}11$ and $\overline{V}12$: A value of ONE indicates that no response was obtained from the test lamp.

4. VM11 and VM12: A value of ONE indicates that a response was obtained from T211 and T212 test pulses, but not from the test lamp. It is these signals which activate the UV indicators of the MWU.

5. $\overline{V}$CUV11 and $\overline{V}$CUV12: A value of ONE indicates that no response was obtained from the test pulses. Any VCUV signal becoming a ONE will make the $\overline{CUV}$ signal a ZERO, to indicate a failure in the electronic circuitry (CUV stands for "computer, ultraviolet").

To explain the functioning of this circuitry, operation under four different conditions is described in detail. Again, the description is given for the circuitry associated with head number one. The integrated-circuit packages U1 and U2 each contain two flip-flops, and so the expressions "upper half" and "low half" will be used to refer to specific flip-flops.

1.3.1 Condition: There are no defective components and no fire is detected. At t = 0, the test lamp comes on for 105 msec. This causes UV11 and UV12 to become ONE for about 120 msec. At the end of $\overline{T}1$ (t = 105 msec.), the upper halves of U1 and U2 are set (Q = 1), and at the end of $\overline{T}$ (t = 120 msec.) the lower halves of U1 and U2 are set. Then UV11 and UV12 become ZERO, but all four flip-flops remain set. Q1, $\overline{V}11$, $\overline{V}12$, VM11, VM12, $\overline{V}$CUV11, and $\overline{V}$CUV12 are all ZERO, $\overline{CUV}$ is ONE, and no T211 or T212 pulses are gated.

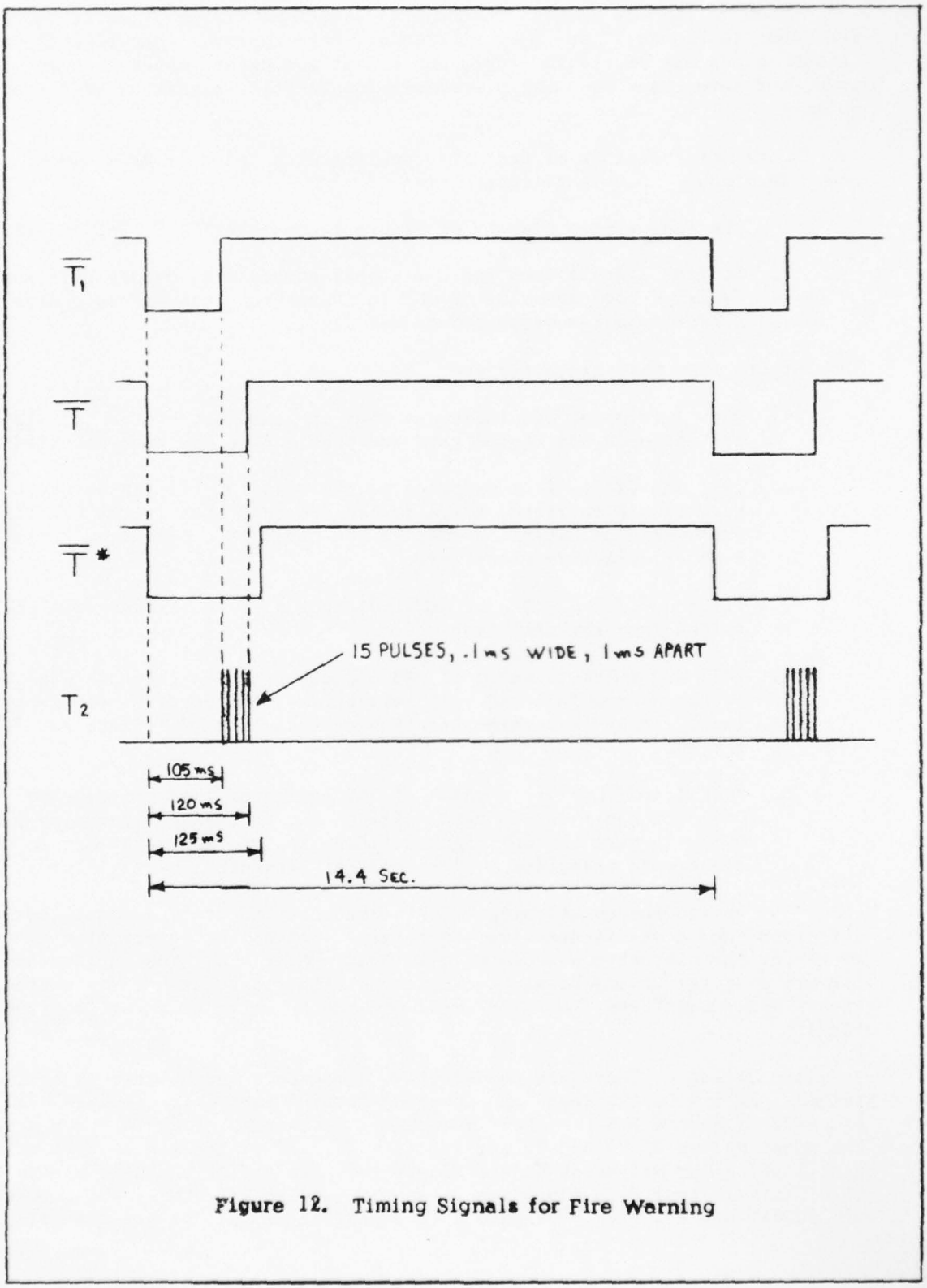


Figure 12. Timing Signals for Fire Warning

1.3.2 Condition: There are no defective components and a fire is detected. UV11 and UV12 become ONE. All four flip-flops have been previously set, as described in 1.3.1. This causes ZEROs to appear on pins 6 and 8 of U8, ONEs to appear on pins 8 and 12 of U13, and ZERO to appear at pin 8 of U14 and hence a ONE to appear at pin 8 of U7. This is the Q1 = ONE signal.

1.3.3 Condition: Sensor tube number two in head number one is defective, and does not generate an output when illuminated by the test lamp. At the end of 105 msec., with UV12 = 0, the upper half of U2 is cleared. T2 pulses are then gated through U8, coming out on pin 3 as T212 pulses, which go back to channel two on the U/V signal processor board. These pulses in turn make UV12 = ONE, so that at the end of $\overline{T}$ (t = 120 msec.) the lower half of U2 is not cleared. With the upper half of U2 not set, $\overline{V}12$ is a ONE, and after $\overline{T}$* again becomes ONE, pin 6 of U17 becomes ZERO, resulting in VM12 = ONE. If a fire were to occur now, the Q1 output would be obtained via pin 12 of U7.

1.3.4 Condition: There is a defect in the electronics in channel number one in the U/V signal processor, such that UV11 is always ZERO. Here, by t = 120 msec., both halves of U1 have been cleared, as UV11 remained zero in spite of the injection of T211 pulses. With both halves of U1 at the Q = 0 state, $\overline{V}11$ = ONE, $\overline{V}$CUV11 = ONE, and, through the action of the U19 inverters, $\overline{CUV}$ = ZERO. If a fire were to occur now, the Q1 output would be obtained via pin 6 of U7.

1.4 Fire Fail Warning Logic

The schematic diagram for the fire fail warning logic is found in Figure 13.

This circuitry performs three functions: It develops a fire warning signal, a fire fail warning signal, and inhibits the T' RESET signal to the U/V signal processors during fire conditions.

Consider first the fire warning circuitry. The six fire signals, Q1 ... Q6, from the fire warning logic are combined in an OR relationship by the circuits of U13 and U7. Thus the signal on pin 8 of U7 is a ONE if any of the flame dectector heads senses a fire. Pin 5 of U18 follows pin 8 of U7, except that a ONE cannot be "passed through" during test time. This inhibition is due to applying the signal $\overline{T}$* (see Figure 10) to pin 4 of U9, and is needed because the signals Q1 ... Q6 normally become ONE during test time. The fire signal is then passed through a gate and an inverter and appears on pin 5 of the printed-circuit board connector. The gate just mentioned inhibits this signal if a "fire fail warning" signal is present. The net effect of this circuitry is to implement the Boolean expression.

$$FW = \overline{\overline{FFW}\ \overline{T}^*}\ (Q1 + Q2 + Q3 + Q4 + Q5 + Q6).$$

Consider now the fire fail warning circuitry. IFOS specifications require that the CCU generate a fire fail warning signal when any two adjacent heads fail (see section 3.2 of Chapter I). This is accomplished by first combining the twelve signals $\overline{V}11$, $\overline{V}12$ . . . $\overline{V}62$ from the fire warning circuits with six 4-input NAND circuits. Thus if detector heads one and two failed, signals $\overline{V}11$, $\overline{V}12$, $\overline{V}21$ and $\overline{V}22$ would all be ONE, and

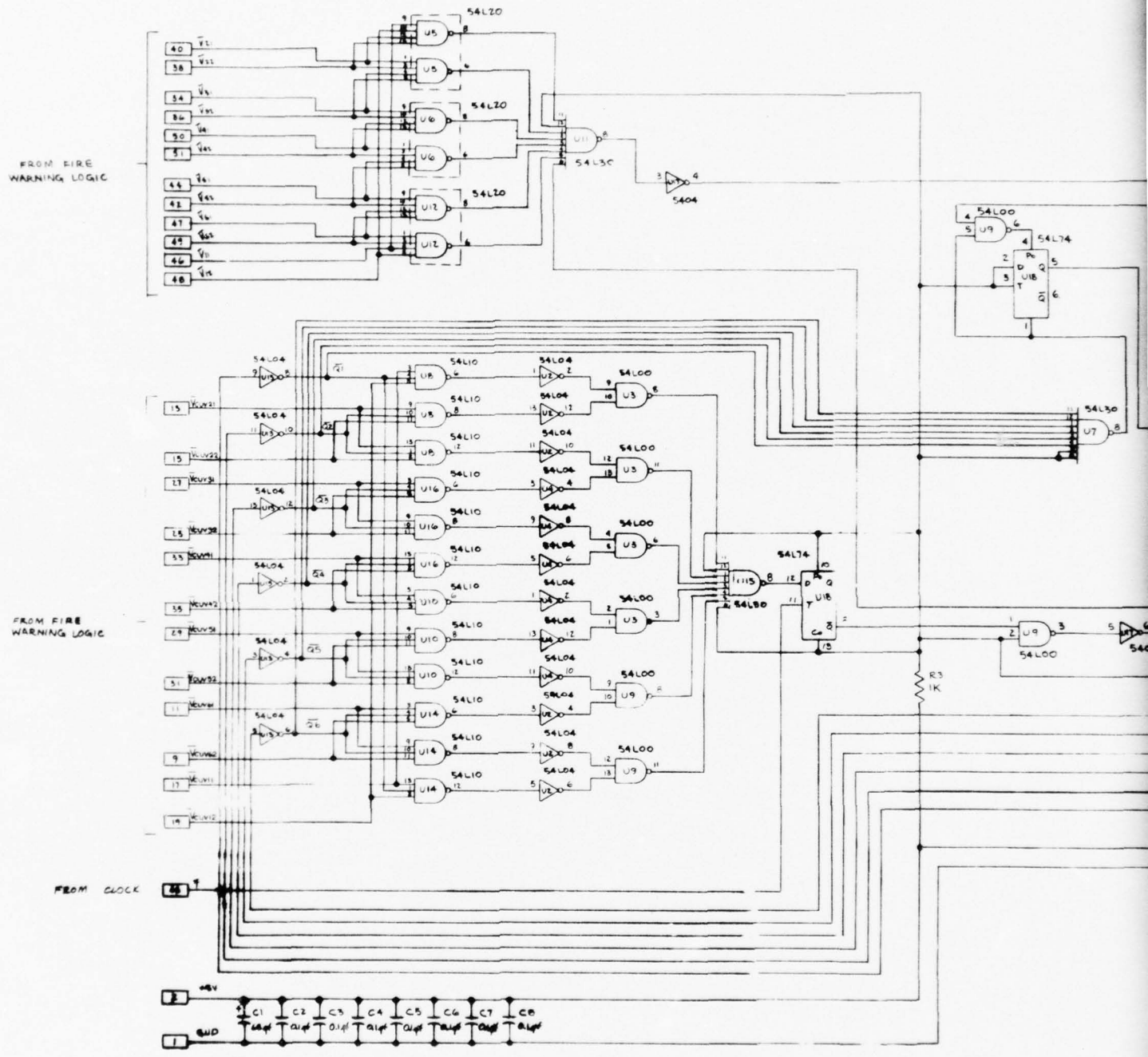


Figure 13. Schematic Wi
Computer Diag

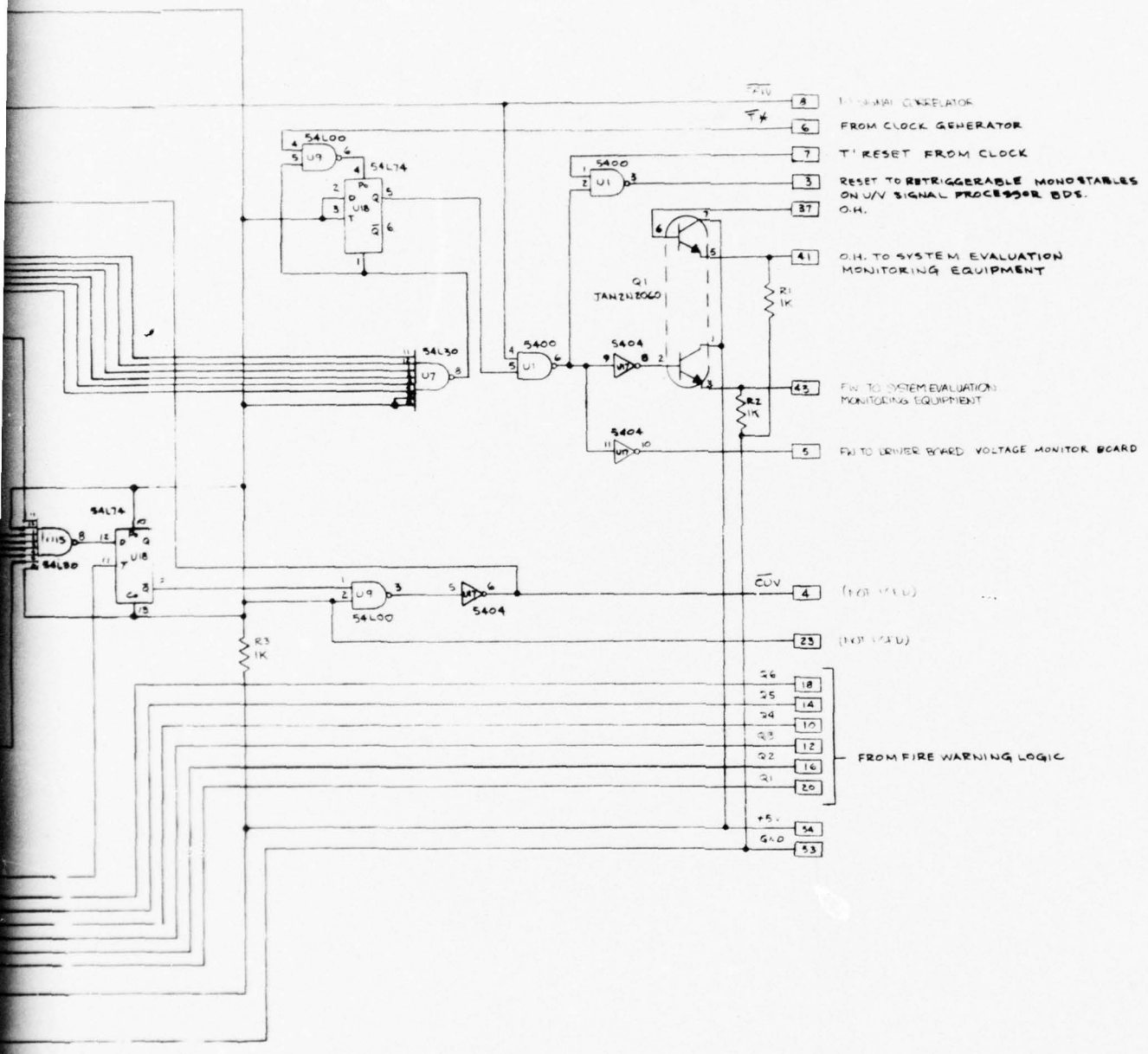


Figure 13. Schematic Wiring Diagram, Fire Fail Warning Logic & Computer Diagnostic Logic

and an output ZERO would appear on pin 8 of U5. The circuits U11 and U17 combine the outputs of the six NAND gates to give an OR function. (The signal on pin 6 of U11 presently performs no useful function.) The overall function of the fire fail warning circuitry is to implement this expression:

$$FFW = \overline{\bar{V}11\ \bar{V}12\ \bar{V}21\ \bar{V}22} + \overline{\bar{V}21\ \bar{V}22\ \bar{V}31\ \bar{V}32}$$
$$+ \overline{\bar{V}31\ \bar{V}32\ \bar{V}41\ \bar{V}42} + \overline{\bar{V}41\ \bar{V}42\ \bar{V}51\ \bar{V}52}$$
$$+ \overline{\bar{V}51\ \bar{V}52\ \bar{V}61\ \bar{V}62} \quad \overline{\bar{V}61\ \bar{V}62\ \bar{V}11\ \bar{V}12}$$

T' RESET is inhibited by the fire warning signal by means of the upper half of the NAND gate U1.

1.5 Driver Circuitry

Figure 14 shows the schematic diagram for this circuitry.

Resistors R1 to R12 are "pull up" resistors for the open-collector inverters of the fire warning circuits. The cascaded inverters are used to amplify the fire warning signal before it is sent to the CRU.

2. OVERHEAT AND OVERHEAT-FAIL SECTION

2.1 Basic Approach

To provide reliability against false alarms and overheat detection failures, redundancy is used for both the sensors and the electronics. Also, the electronics is periodically tested for both false ON and false OFF.

The overheat system consists of two sensor-computer channels (sensor loop A - Channel A and sensor loop B - Channel B) whose outputs are directed to the display units. Each alarm channel consists of a sensor cable loop, both ends of which are connected to a corresponding signal processor in the computer control unit. Signal processor output is in turn applied to a fault evaluation circuit, an output circuit and a signal correlator circuit which is common to both overheat alarm channels and the U/V portion of the system.

Even though the range of sensing element circuit resistance in which an overheat alarm may be signalled includes resistance values that could be produced by partial shorts in the sensor cable, connectors, or wiring, the computer control unit is capable of discriminating between an overheat or a partial short condition.

Sensor cables, having thermal mass, do not react instantly to variations in temperature while a large majority of shorts, absolute or partial, take on the character of a step input change in cable resistance.

In the course of this program, it was decided that the technique of examining and comparing the outputs of a group of signal processor amplifiers, connected by way of a bridge network to each sensor cable, in the

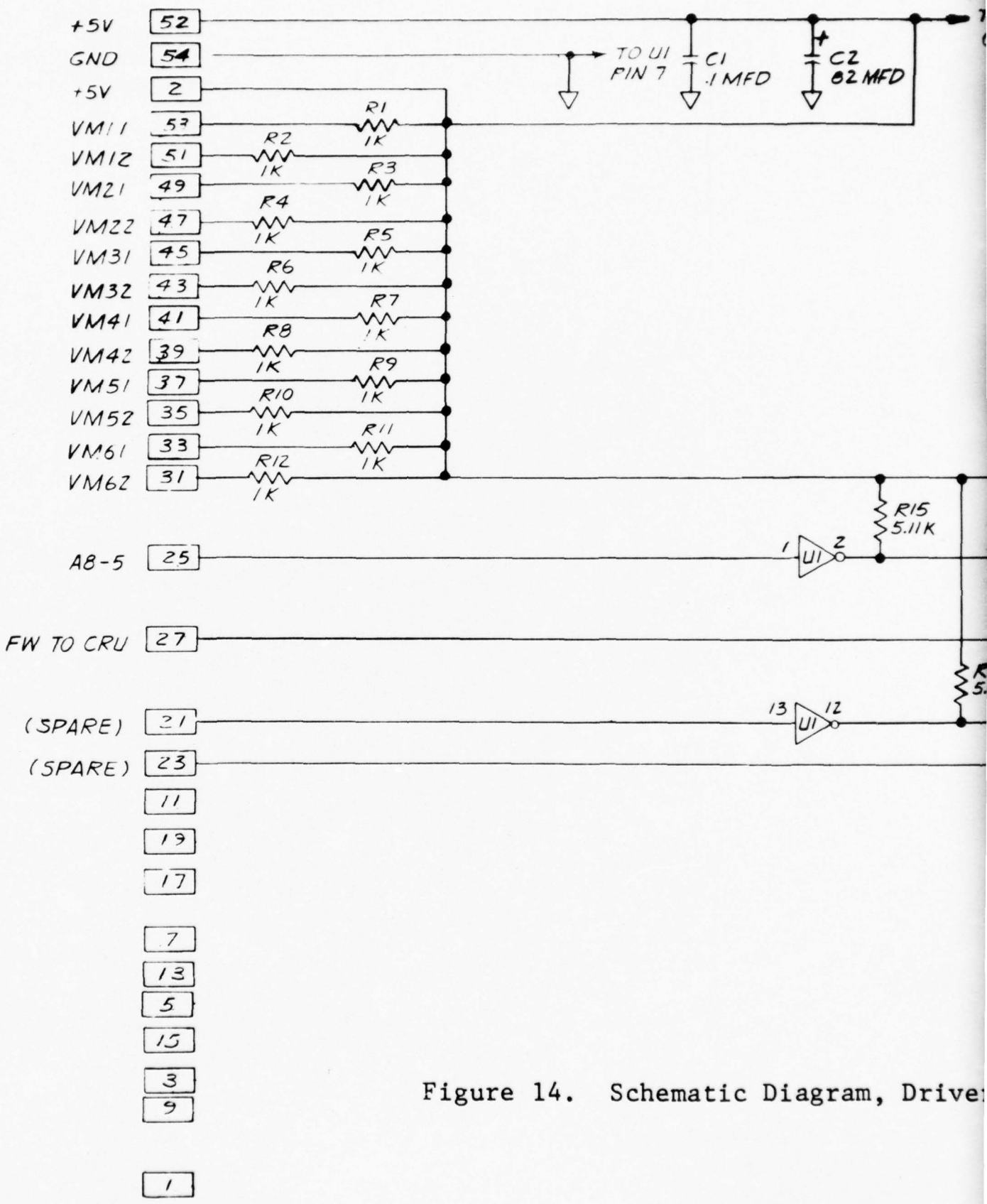
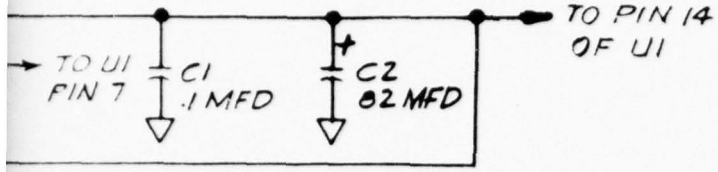
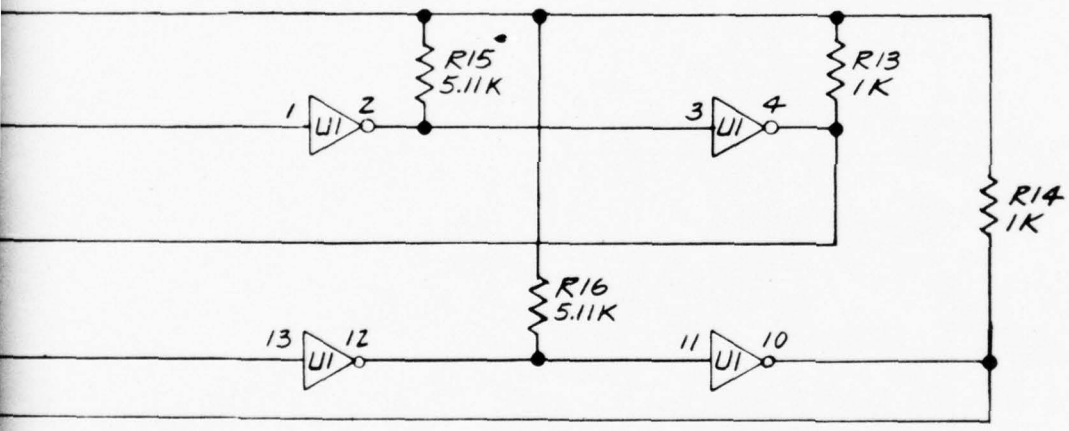


Figure 14. Schematic Diagram, Drive





PRINTED WIRING BOARD —
ASSY 44283
AW 61694

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS
2. U1 = SN5406J
3. PIN "1" IS LOCATED ON THE SILVER END OF THE CONNECTOR.

Schematic Diagram, Driver Board

time domain was an effective means by which sensor short discrimination could be accomplished. In addition, the periodic application of test pulses to both sensor cable and signal processor circuitry was found to be an effective means for monitoring the status of sensor cable continuity against opens and shorts and the status of amplifier operation against electronic faults appearing as false ON's and false OFF's.

Three amplifier channels are by way of bridge circuit detection networks linked to each sensor to obtain the signals for sensor cable and signal processor status. These are designed as A1, A2 and A3 for sensor loop A and, in like manner, B1, B2 and B3 for sensor loop B.

Amplifier A2, containing an input delay network, operates in conjunction with A1 to determine the existence of either an overheat condition or a cable short. Here, on a steady state basis, A2 is so set as to become activated at a slightly lower sensor temperature than A1. Thus for overheat conditions A2 would be actuated before A1. This condition is symbolized by the term A21 which is monitored during normal, no-test, time. Amplifier A3 is used with A1 and A2 to aid in determining the status of cable circuit continuity.

In the course of this work, it was found necessary to periodically apply two test pulses (TC12 and TC22) to provide a continuous and automatic check of both sensor cable and signal processor status. Here overheat detection occurs during the 14.86 second (nominal) no-test interval. Once detected, the condition of overheat is memorized and cuts out overheat fail and cable fail circuitry, preventing their display.

The operational continuity of sensor cable A and alarm amplifiers A1 and A2 is checked by applying a turn-on pulse TC12 to the input circuitry of A1 and A2 by way of cable A. The operational continuity of amplifier A3 is checked by the direct application of TC12 to the input circuit of A3. The pulse width of TC12 is approximately 45 milliseconds long.

Pulse TC22 is a turn-off pulse which starts approximately 60 milliseconds after the end of TC12, and is approximately 35 milliseconds wide. It is applied directly to the inputs of A1, A2 and A3, and is used to detect cable shorts and amplifier faults appearing as a false ON.

A shorted cable occurring any time actuates A1 and A2. This condition is detected at the conclusion of turn-off pulse TC22, and during the beginning of the normal no-test period.

2.2 Description and Operation

From input to output each alarm channel contains a Wheatstone bridge type detection network operating in conjunction with a three amplifier channel signal processor, a cable and signal processor fault differentiating board, and an output board. The per-channel output boards operate in conjunction with a signal correlator board which is common to both overheat channels to provide signals to the Crew Readout Unit for the generation of OVERHEAT FAIL warnings and signals to the Maintenance Warning Unit

for the generation of cable and signal processor fail warnings. Here, the signal correlator also combines sensor cable fault signals and signal processor fault signals with fail terms from clock monitor and voltage monitor circuitry, used by the entire computer control unit, for the production of overheat fail warning signals. In an analogous manner, the signal correlator also provides fire-fail warning signals.

The overheat portion of the computer control unit obtains its power from aircraft-type unregulated 28VDC, and is transient protected by a choke-zener diode transient suppressor network. Plus five volts from a switching regulator and minus five volts from a DC/DC converter and linear regulator circuit provide logic power to both channels from input to output. The computer control unit signal correlator obtains its power from the five volt reference supply.

2.2.1 Signal Processor

As can be seen in Figure 15, both ends of the sensor cable are connected to the input circuit. Here, one end of the center conductor is connected to bridge resistor R1 and the three amplifier channels A1, A2, and A3. The other end of the center conductor is connected to an open collector inverter U2-1 which, when activated by turn-on pulse TC12, connects the center conductor to ground potential by way of test resistor R5. Both ends of the outer sheath of the sensor cable are connected to the bottom of the detector bridge. A return wire connected to the sensor cable sheath is brought back to power common by way of terminal 1. This configuration represents the detector portion of this bridge where R1 is the upper leg and sensor cable center wire-to-sheath resistance is the lower leg. Resistors R2 and R6, R3 and R7, and R4 and R8 are the upper and lower bridge set point legs for amplifier channels A1, A2, and A3, respectively.

Channel A, consists of one-half of dual comparator integrated circuit chip U1. Channel A2 consists of an input stage (the other half of dual comparator U1), a delay network consisting of resistor R21 and capacitance C26 and C27 and an output stage consisting of one-half of dual comparator U3. Channel A3 consists of one-half of dual comparator U4.

All of the amplifiers connected to the bridge circuit contain positive hysteresis networks and R-C filters for protection against spurious noise voltages existing on the sensor cable.

Since upper bridge resistors R1, R2, R3 and R4 have the same resistance, lower set point resistors R6, R7, and R8 will represent the center wire-to-sheath resistance at which inputs to amplifier channels A1, A2, and A3 will be zero excluding the effect of positive hysteresis circuitry.

Thus as sensor cable temperature increases, cable resistance decreases and as it passes through 270 ohms, for example, signal voltage across terminals of U1-2 increases from a negative value through zero to a positive value causing in turn a positive going output from terminal 8

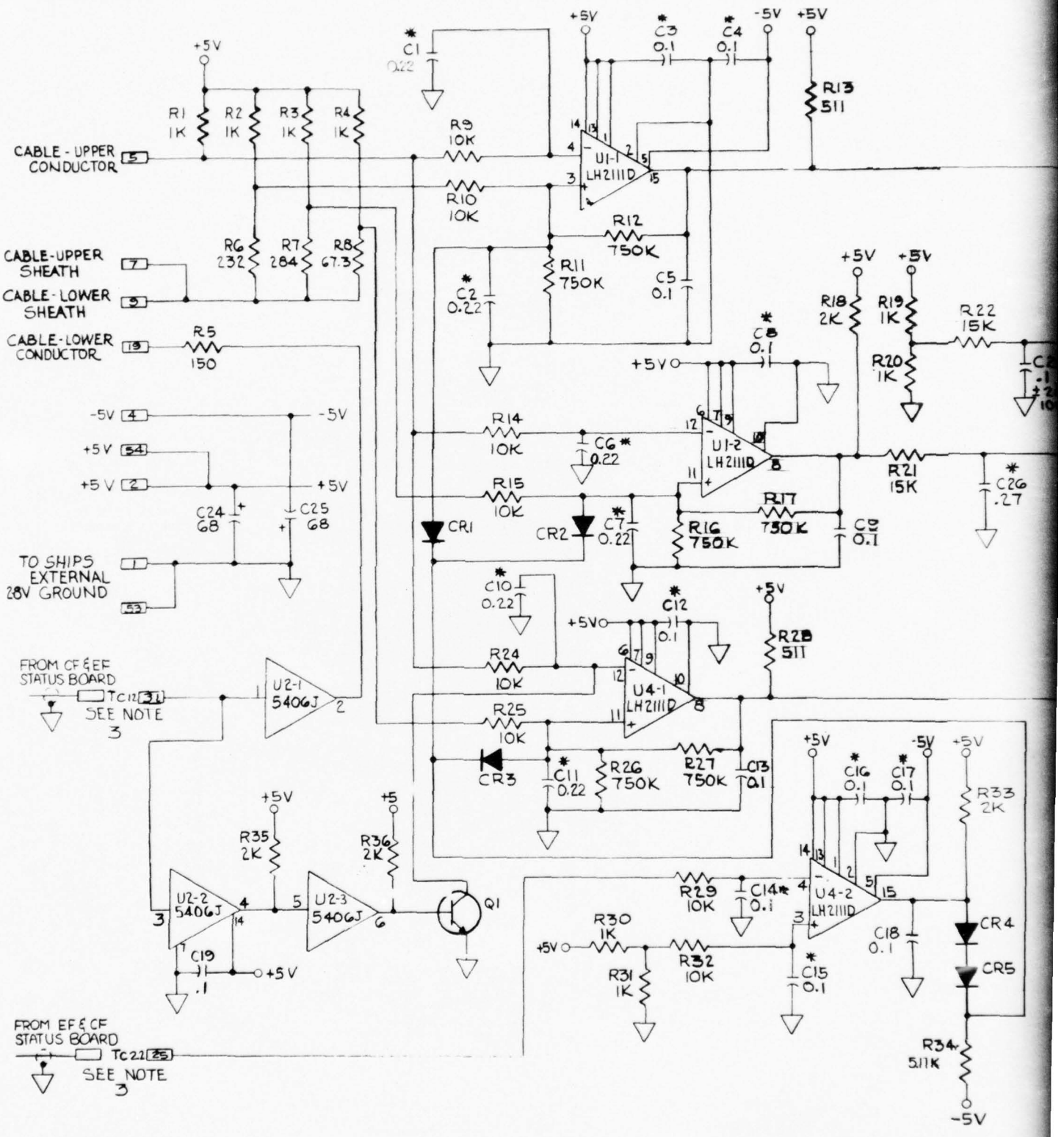
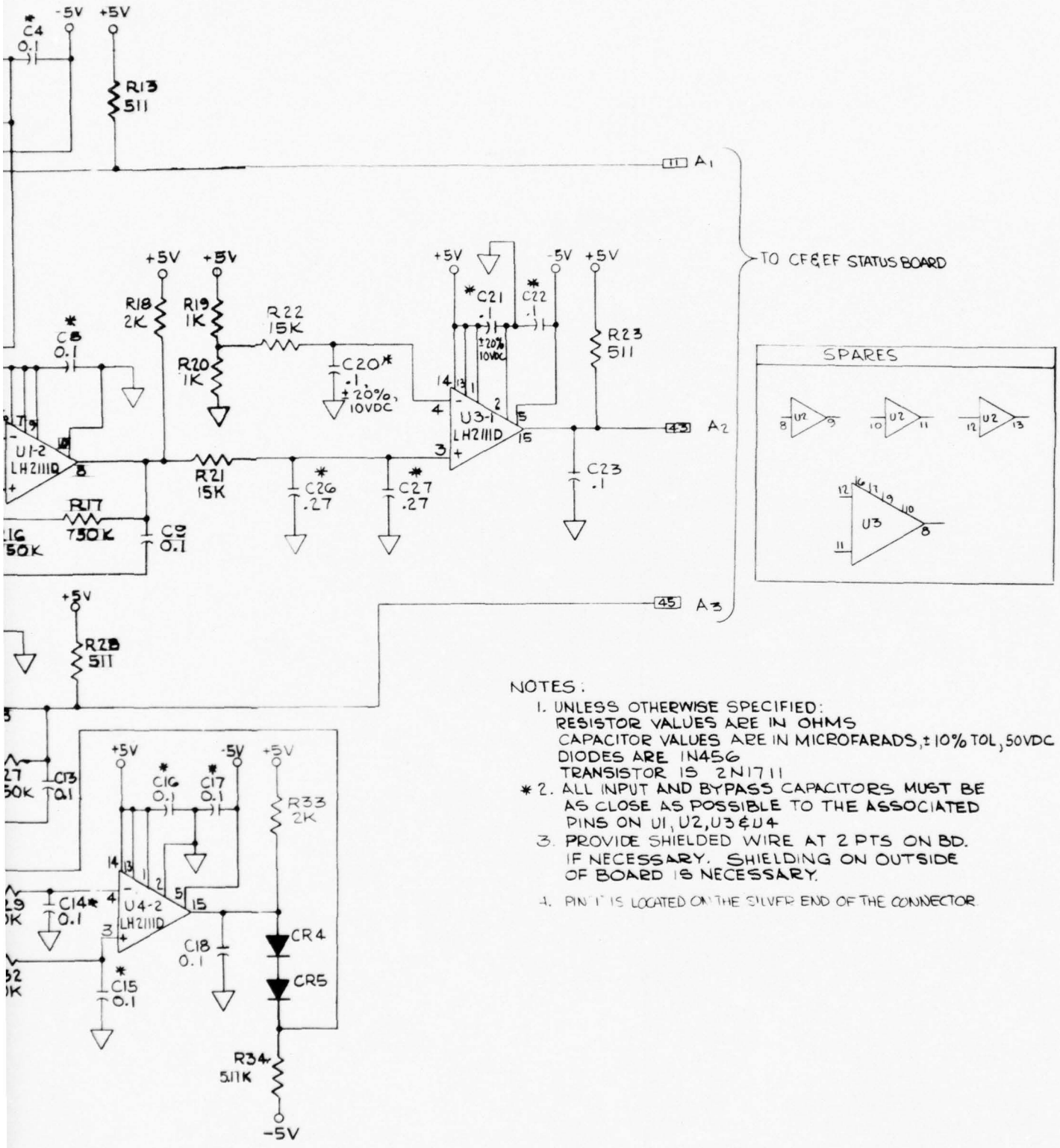


Figure 15. Schematic Wiring Diagram, O/



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS
   CAPACITOR VALUES ARE IN MICROFARADS, ± 10% TOL, 50VDC
   DIODES ARE 1N456
   TRANSISTOR IS 2N1711
2. * ALL INPUT AND BYPASS CAPACITORS MUST BE AS CLOSE AS POSSIBLE TO THE ASSOCIATED PINS ON U1, U2, U3 & U4
3. PROVIDE SHIELDED WIRE AT 2 PTS ON BD. IF NECESSARY. SHIELDING ON OUTSIDE OF BOARD IS NECESSARY.
4. PIN 1 IS LOCATED ON THE SILVER END OF THE CONNECTOR

:ic Wiring Diagram, O/H Signal Processor "A"

of U1. This output voltage is applied, by way of the delay network, to comparator U3-1 which supplies signal processor output A2.

As cable resistance decreases further and passes through 220 ohms, signal voltage across dual comparator U1-1 becomes positive and supplies signal processor output A1 without the time delay experienced by A2.

For center conductor to outer sheath partial shorts of less than 220 ohms, A1 will be activated before A2 (A12) at the end of turn off pulse TC22 and the beginning of the normal no-test period whereas for gradual changes in cable resistance due to an overheat condition, A2 will be activated before A1 (A21). This is the manner in which cable shorts are differentiated from true overheat conditions.

In a manner similar to A1, channel A3 output is present when center wire to cable resistance reaches a value lower than 63 ohms which is viewed as a direct short.

By way of inverters U2-2 and U2-3 and transister Q1, turn on pulse TC12 is also applied directly to comparator U4-1, which presents amplifier channel A3 output.

Turn-on pulse TC12 is applied to inverter U2-1 which then connects the open side of the sensor cable center wire to ground potential. The result of this test is that both amplifier channels A1 and A2 are now activated by way of the cable. Should an open circuit exist in center wire circuitry, these amplifiers would not be activated. Thus, for an open in sensor cable A, the single fault logic displayed by A1, A2, and A3 during TC12 would be

A1	A2	A3	TC12	TC22
0	0	1	1	0

The comprehensive truth table for the overheat system is included as Appendix IV.

Turn-off pulse TC22 starts approximately 60 milliseconds after the end of TC12 and is used to detect cable shorts and amplifier faults appearing as a false ON.

As seen in Figure 15, non-inverting inputs U1-1, U1-2 and U4-1 are joined by the way of isolation diodes CR1, CR2, and CR3, respectively, to a voltage divider network consisting of resistor R33, diodes CR4 and CR5, and resistor R34. Here comparator U4-2 is connected to the junction of R33 and CR4 and is used as a voltage level shifter which during the no-test state provides a positive bias to the divider network keeping isolation diodes CR1, CR2, and CR3, in an off-biased, non-conducting state. In this no-test state all channels are thus permitted to operate in a standard monitoring mode. When turn-off test pulse TC22 is applied to U4-2, the amplifier shifts the bias voltage on the voltage divider from plus to minus, diodes CR1, CR2, and CR3 conduct current, and the input amplifiers of channels A1, A2, and A3 are turned off. Should any amplifier channel remain in an on state, this condition will be diagnosed by

fault circuitry as a signal processor fault. If A1, for example, remained ON the logic pattern presented would be as follows:

A1	A2	A3	TC12	TC22
1	0	0	0	1

This condition would then be evaluated as an electronic fault in signal processor A. Information of this condition would be applied both to the Maintenance Warning Unit where the CCU light would be turned on, and to the Crew Readout Unit where it would be stored as an overheat fail in channel A (OHFA) for future operation with other signals.

Should amplifiers A1 and A2 be in an ON state because of either an overheat condition or a cable short, they would be turned off periodically by the application of TC22. Since A2 has an input delay, the end of TC22 and beginning of the no-test period would cause first A1 and then A2 to be reactivated into an on-state (A12). However, if A1 and A2 were turned on by an overheat condition (A21), occurring during the preceding no-test period, the existing overheat signal and display would be maintained. If, on the other hand, no overheat condition exists, then the signal caused by A12 would be allowed to generate both a CFA display in the Maintenance Warning Unit, and store an overheat fail signal for channel A (OHFA) in the Crew Readout Unit where it would block a corresponding overheat signal. The logical presentation of a cable short at the end of TC22 and the beginning of no test is presented as follows:

A1	A2	A3	T12	T22
1	1	0	0	0

where the sequence of A1 and A2 (A12) is sensed.

2.2.2 Cable and Signal Processor Fault Diagnostic Circuitry

The truth table shown in Appendix IV represents all the possible states of signal processor output and test modes, any one of which can exist at a particular time. It is important to note that further logic considerations have to be made to accommodate the existence of a more than one event, that is, a chain of events each of which is represented by its particular line. As will be discussed later, one solution that is employed is the concept of first-come first-serve priority logic.

This concept is employed in both the cable and signal processor fault board and the output board to enable decision making, and in the Crew Readout Unit to memorize warnings of OVERHEAT or OVERHEAT FAIL with certainty.

2.2.2.1 Cable Fault

A study of the truth table in Section IV for the logic expression denoting a fault in cable A, results in the analysis of a number of lines. When simplified, the logic equation for cable fault A (CFA) becomes

$$CFA = A12\ \overline{TC12}\ \overline{TC22} + \overline{A1}\ \overline{A2}\ A3\ TC12\ \overline{TC22}$$

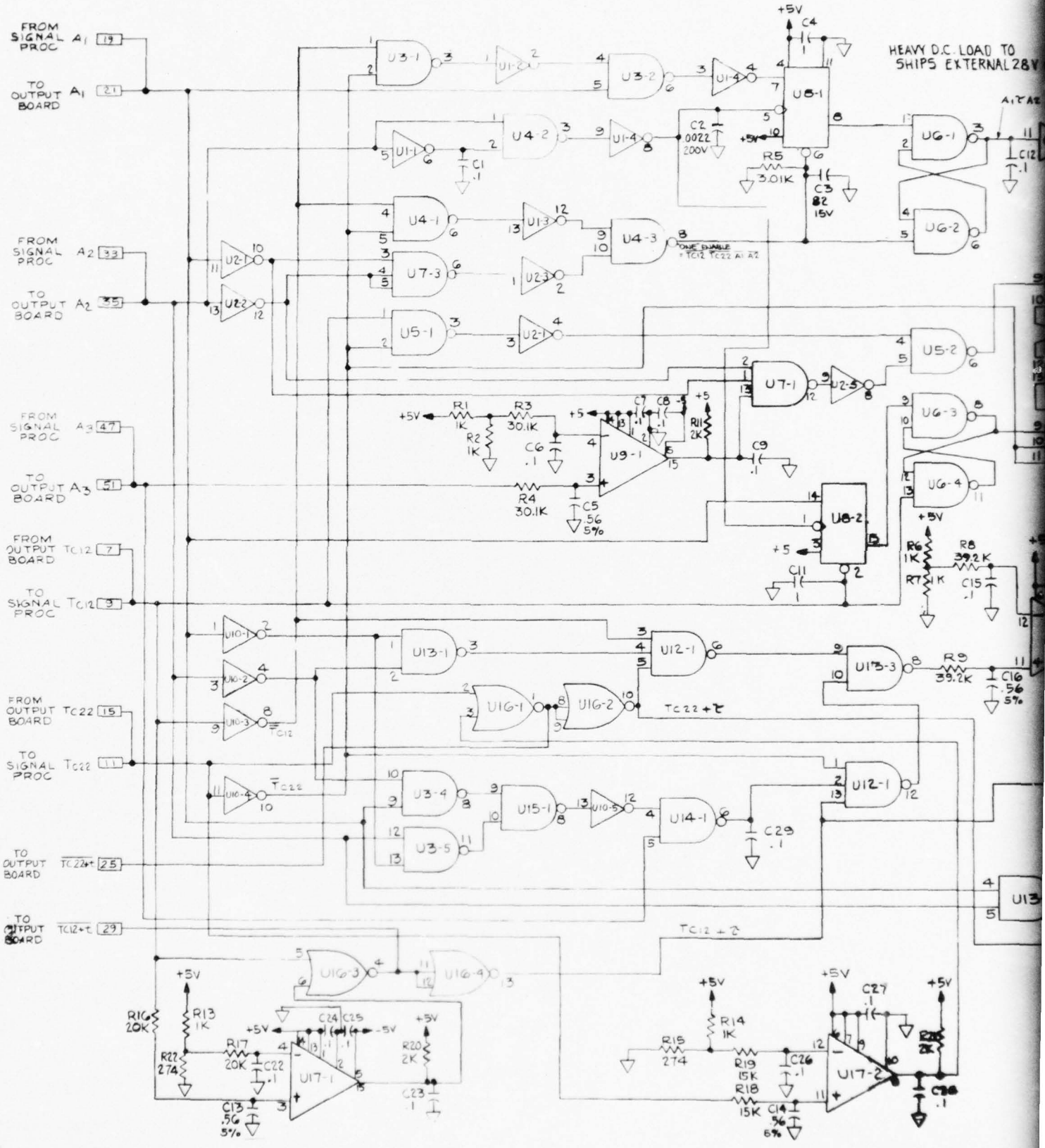
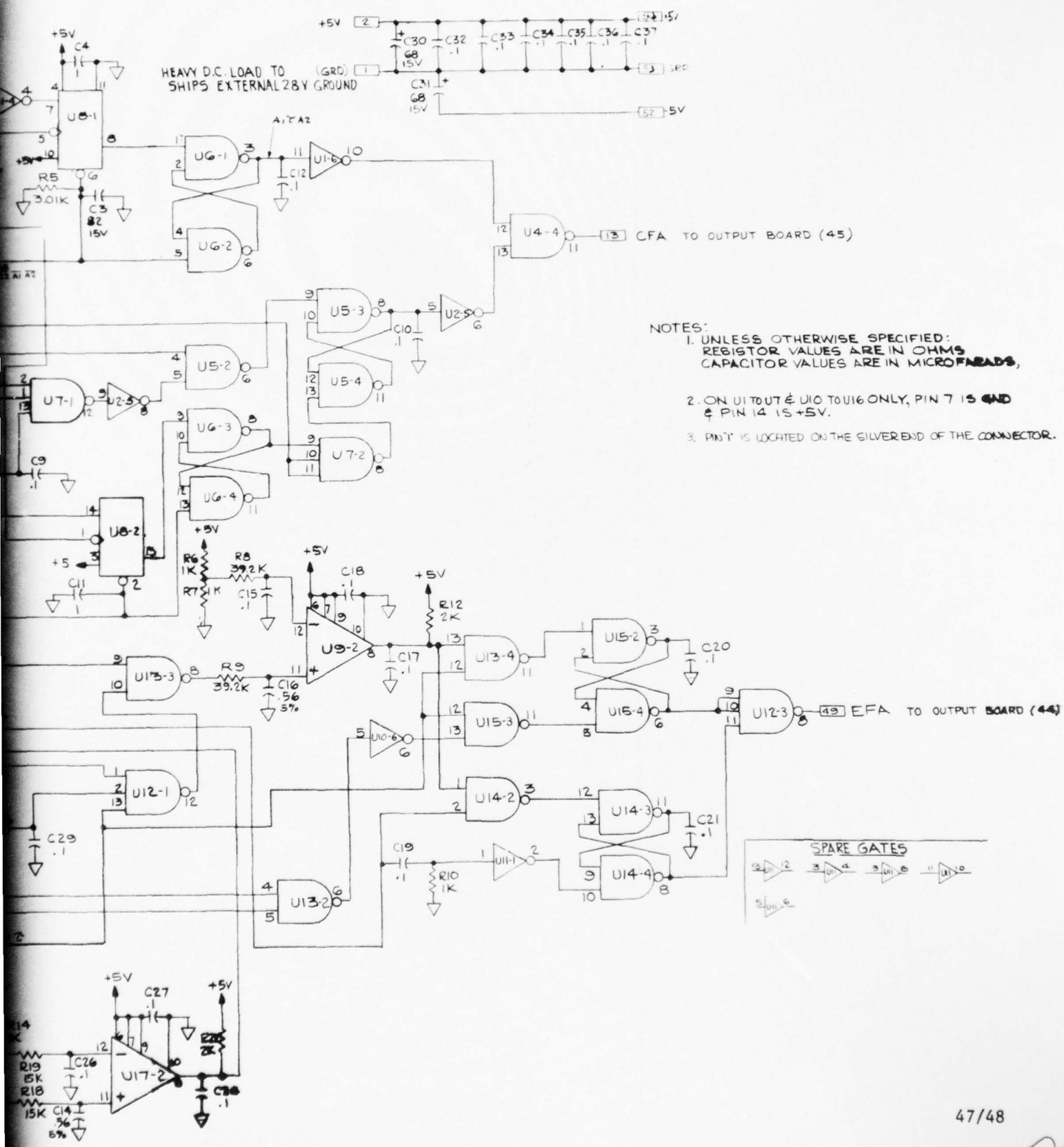


Figure 16. Schematic Diag



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS CAPACITOR VALUES ARE IN MICROFARADS,
2. ON U1 TO U7 & U10 TO U16 ONLY, PIN 7 IS GND & PIN 14 IS +5V.
3. PIN "1" IS LOCATED ON THE SILVER END OF THE CONNECTOR.

16. Schematic Diagram, CFA & EFA Logic

where the first term denotes a cable short (A1 occurring before A2) found during no-test, and the second term denotes an open cable found during TC12. (Refer to Figure 16.)

Cable short status and cable open circuit status are applied to NAND gate U4-4. This element is a NAND gate for logical ONE inputs but can be used as a NOR gate for logical ZERO inputs. Normal no-fault states are presented as logical ONE's to the input of this gate and result in a normal no-fault logical ZERO at output. The occurrence of either cable fault, however, will cause either logical ONE input to be changed to a logical ZERO and result in a CFA logical ONE at the output terminal.

The sensor cable short condition A12 $\overline{TC12}$ $\overline{TC22}$ is detected by J-K flip-flop U8-1 and is applied in the form $\overline{\overline{TC12}\ \overline{TC22}}$ A12 to set terminal 1 of the latch consisting of NAND gates U6-1 and U6-2. By way of inverter U1-6, the inverse is applied to input terminal of U4-4. For the normal no-fault state, both flip-flop and latch are maintained in a reset condition by a reset signal applied to terminal 6 of U8-1 and terminal 5 of U6-2. Here, reset (a ZERO) is applied as long as both A1 and A2 are not activated during the no-test interval. This condition is logically expressed as $\overline{\overline{TC12}\ \overline{TC22}\ A1\ A2}$, where the overall conversion denotes that the reset condition is represented by a logical ZERO.

Under cable short conditions reset is removed. Then at the termination of TC22 and the beginning of no-test ($\overline{TC12}$ $\overline{TC22}$) A1, which is reactivated before A2, is applied directly to U3-2 where it is combined with the no-test term.

The no-test term is obtained by inverting the states presented by TC12 and TC22, by way of inverters U10-3 and U10-4 and then ANDing the resulting signal with NAND gate U3-1 and inverter of U1-2 which generates a logical ONE for the no-test condition of $\overline{TC12}$ $\overline{TC22}$ at the input of U3-2. The output of U3-2 is now $\overline{TC12}$ $\overline{TC22}$ A1, which by way of inverter U1-4 is fed to J-K flip-flop U8-1.

As with all J-K flip-flops, input to output operation is actuated by a clock pulse. In the circuit described, A2 when reactivated after A1, generates by way of U1-1, capacitor C1, NAND gate of U4-2 and inverter of U1-4, a one-shot pulse to terminal 5. Should A2 occur before A1, no information would be transferred. In this manner, the sequence of A1 operating before A2 is detected and is latched by U6-1 and U6-2. Only when cable status returns to normal will this information be erased.

The sensor cable open fault condition $\overline{A1}$ $\overline{A2}$ A3 TC12 $\overline{TC22}$ is detected and retained by the latch consisting of NAND gates U5-3 and U5-4 during test time TC12. By way of inverter U2-5 its inverse is applied to U4.

After a careful study of the possible sensor loop status modes, it was concluded that the reset logic term which most properly represents a return to normal condition would be TC12 $\overline{TC22}$ A12. This term signifies that A1 and A2 are being properly sequenced into an ON state during TC12, an operation which could only be performed by way of a continuous cable in the normal no-fault, no-alarm state. The actual term for reset is implemented by a logical ZERO. It is applied by way of NAND gate U7-2 to terminal 13 of the latch.

When an open cable exists, the break in continuity prevents signal processor amplifier channels A1 and A2 from being activated during TC1. At this time, reset term TC12 $\overline{TC22}$ A12 is removed from the latch permitting open cable information to be reused and retained.

In open cable term TC12 $\overline{TC22}$ $\overline{A1}$ $\overline{A2}$ A3, test pulse TC12 is ANDed with $\overline{TC22}$ by way of NAND gate U5-1 and inverter U2-4.

The amplifier states of A1 and A2 are ANDed with a delayed presentation of A3 by NAND gate U7-1 and of inverter U2-5. Here A3 is delayed by resistor R4, capacitor C5, and biased comparator U9-1 to permit A1 and A2 to stabilize before being examined during TC12. Otherwise, a false open cable fault warning signal would be generated.

The time states of TC12 and $\overline{TC22}$ and states of amplifier outputs A1, A2, and A3 are now combined in NAND gate U5-2. The combined result is now applied to the SET terminal 9 of U5-3 and U5-4 latch in the form TC12 $\overline{TC22}$ $\overline{A1}$ $\overline{A2}$ A3. If an open cable exists, this term is a ZERO while a continuous cable will give a ONE. For an open cable, a logical ONE results from the latch network which by way of inverter U2-5 is presented as a ZERO to the general CFA NAND U4-4. Should an open cable be replaced and the computer control unit be re-energized, reset action will change this cable fault ZERO to a ONE as discussed below.

In the open cable reset term $\overline{TC12\ \overline{TC22}\ A12}$, A12 is obtained in a manner similar to that discussed previously. The circuitry used to detect and retain A12 consists of J-K flip-flop U8-2 and a latch consisting of NAND gates U6-3 and U6-4. Here, a logical ZERO reset signal is continuously applied during the absence of TC12. TC12 is applied in logical ONE form as an enabling signal to both J-K flip-flop and latch. Should cable continuity be restored, A1 and the following pulsed one-shot form of A2 (A12 generated during TC12) are detected by the J-K flip-flop and retained by the latch. This action provides a signal at terminal 9 of U7-2 in the form of TC12 A12 which is then combined with no-turn-off test term $\overline{TC22}$. The result appears as a logical ZERO reset pulse to terminal 13 of the open cable latch U5-4 in the form TC12 $\overline{TC22}$ A12. This action restores the no fault logical ONE at terminal 13 of U4-4.

2.2.2.2 Signal Processor Fault (Channel A, for example)

A collection and simplification of the terms defining an electronic fault in signal processor A results in the following equation:

$$\begin{aligned} EFA = {} & \overline{TC12}\ \overline{TC22}\ (A1\ \overline{A2}) \\ & + \overline{TC12}\ TC22\ (A1 + A2) \\ & + TC12\ \overline{TC22}\ (A1\ \overline{A2} + \overline{A1}\ A2 + \overline{A1}\ \overline{A3} + A21) \end{aligned}$$

Here the terms shown present those signal processor failures which, on a one-fault basis, make it impossible to establish either a cable fault or an overheat condition in sensor cable-channel A.

After careful investigation it was found that further simplification of this equation was warranted.

The first term, $\overline{TC12}\ \overline{TC22}$ A1 $\overline{A2}$, could indicate that A1 had become shorted, or that a cable overheat condition had occurred but that A2 was in an OFF-fault state, or that A1 $\overline{A2}$ was the early stage of a cable short fault occurrence where A2 was soon to follow. The condition could be ascertained with certainty during the off-test period depicted in the second expression $\overline{TC12}$ TC22 (A1 + A2), the second condition could be established during the on-test period shown in the third expression TC12 $\overline{TC22}$ (A1 $\overline{A2}$ -------), and the third condition would be discovered by the cable fault circuitry described previously in section 2.2.1. As a result, the term $\overline{TC12}\ \overline{TC22}$ A1 $\overline{A2}$ was removed.

The third term, TC12 $\overline{TC22}$ (A1$\overline{A2}$ + $\overline{A1}$A2 + $\overline{A1A3}$ + A21) denotes that a signal processor fault exists during the turn-on test period. Here, the absence of A3 with or without the absence of A1 ($\overline{A3}$ vs $\overline{A1A3}$) would constitute a failure in open cable circuit detection. So A3 would suffice. A21, during turn-off pulse TC12, was also removed because of an important aspect in single fault logistics. It was found that the condition of cable A being near but not in an overheat state could cause only A2 to be activated which during turn on test pulse TC12, would cause A21 to be presented. The result would be the false display of an electronic fault displacing a pending valid overheat condition.

The final equation for signal processor electronic faults becomes, therefore,

$$EFA = \overline{TC12}\ TC22\ (A1 + A2) + TC12\ \overline{TC22}\ (A1\overline{A2} + \overline{A1}A2 + \overline{A3})$$

where, $\overline{TC12}$ TC22 (A1 + A2) reveals that a signal processor fault exists if A1 or A2 remain in a false ON state during turn-off test pulse TC22. In Figure 16, the terms are presented in inverted form as $\overline{\overline{TC12}\ TC22\ (A1 + A2)}$ and $\overline{TC12\ \overline{TC22}\ (A1\overline{A2} + \overline{A1}A2 + \overline{A3})}$ to terminals 9 and 10, respectively of NAND gate U13-3. Here normal no-fault states appear as ONE's and a fault, at either input, is presented as a ZERO.

In the first term, $\overline{TC12}$ TC22 (A1 + A2), inverter U10-3 provides $\overline{TC12}$ to terminal 3 of NAND gate 3-4-5-6 of U12. By way of inverters U10-1 and U10-2 and dual input NAND gate 1-2-3 of U12, the term $\overline{A1A2}$ is obtained and applied to terminal 4 of U12. In combination with 12-11-8 of dual comparator U17, and NOR gates 2-3-1 and 8-9-10 of U16, a slightly stretched form of TC22 is applied to terminal 5 of U12. As will be explained later, the stretching of TC22 permits greater discrimination between nonsense pulses generated during normal no-fault conditions and true fault pulses. The result at terminal 6 of U12 is an output in the form of $\overline{\overline{TC12}\ (TC22 + t)\ \overline{A1\ A2}}$ which is rewritten as $\overline{TC12}$ (TC22 + t) (A1 + A2).

To obtain the second term, TC12 $\overline{TC22}$ (A1$\overline{A2}$ + $\overline{A1}$A2 + $\overline{A3}$), the term

$$\overline{\overline{A1A2}\ \overline{A1A2}\ A3}$$

is first developed by way of inverters 1-2 and 3-4 of U10, dual NAND gates 10-9-8 and 12-13-11 of U3, NAND gate 10-9-8 of U15, inverter 13-12 of U10, and dual NAND gate 4-5-6 of U14. It is then combined with a slightly stretched form of TC12 (TC12 + t) and $\overline{TC22}$ to become

$$\overline{(TC12 + t)\ TC22\ (A1\overline{A2}\ \overline{A1}A2\ A3)},$$

which in effect is

$$\overline{(TC12 + t)\ \overline{TC22}\ (A1\overline{A2} + \overline{A1}A2 + \overline{A3})},$$

the fault term in ZERO form. This term is applied to terminal 10 of U13.

For false-ON or false-OFF signal processor faults, the ZERO pulse applied to terminals 9 or 10, respectively, of U13 causes on output fault pulse EFA in logical ONE form, to be applied to a delay network. The delay network acts as a well defined low pass filter which blocks nonsense pulses of short pulse width formed during the normal no-fault gating operations associated with each of the two terms described above, but allows the broader pulses generated by true signal processor fault conditions during TC12 + t and TC22 + t to be detected. The delay network consists of resistor R9, capacitor C16 and biased comparator 11-12-8 of U9.

Signal processor fault information is thus obtained in pulse form at output terminal 8 of U9. Here a logical ONE pulse occurs from a false-OFF fault presented during TC12 + t or a false-ON presented during TC22 + t.

The latching network which retains false-OFF fault information consists of NAND gates 1-2-3 and 4-5-6 of U15. Should a false-OFF fault pulse (the second term in the equation) occur during TC12, it and a keying pulse representing TC12 + t are then combined to provide an actuating pulse at SET terminal 1 of the latch. This results in an inverted EFA signal in logical ZERO form being applied to terminal 9-10 of triple NAND output gate U12. When proper operation of the amplifier channels has been restored, a reset pulse generated by the combination of TC12 + t and the amplifier outputs at NAND gate 12-13-11 of U15 is applied to RESET terminal 5 of the latch. This action changes the logical ZERO fault presentation at terminals 9-10 of U12 to a ONE.

In like fashion, the latching network which retains false-ON fault information consists of NAND gates 12-13-11 and 9-10-8 of U14. Here, a false-ON fault pulse occurring during TC22 is combined with a keying pulse representing TC22 + t at NAND gate 1-2-3 of U14 to provide an actuating pulse to SET terminal 12 of the latch.

The repair of signal processor false-ON faults will now eliminate output fault pulse EFA from terminal 8 of U9 and cause a logical ZERO to exist at terminal 1 of U14 during turn-off pulse TC22. This condition will allow a differentiated TC22 + t pulse to reset the U14 latch. (The differentiation is performed by C19 and R10.) The result is that the false-ON fault ZERO presentation at terminal 11 of triple NAND gate 9-10-11-8 of U12 is replaced by a no-fault logical ONE.

In a manner similar to the operation of the CFA output gate 12-13-11 of U4, a fault ZERO at either input terminal 9-10 or 11 of NAND gate 9-10-11-8 of U12 causes a logical ONE EFA fault output signal at terminal 8 of U12. Here, restoration of proper operation will change the logical ONE to a normal no-fault ZERO.

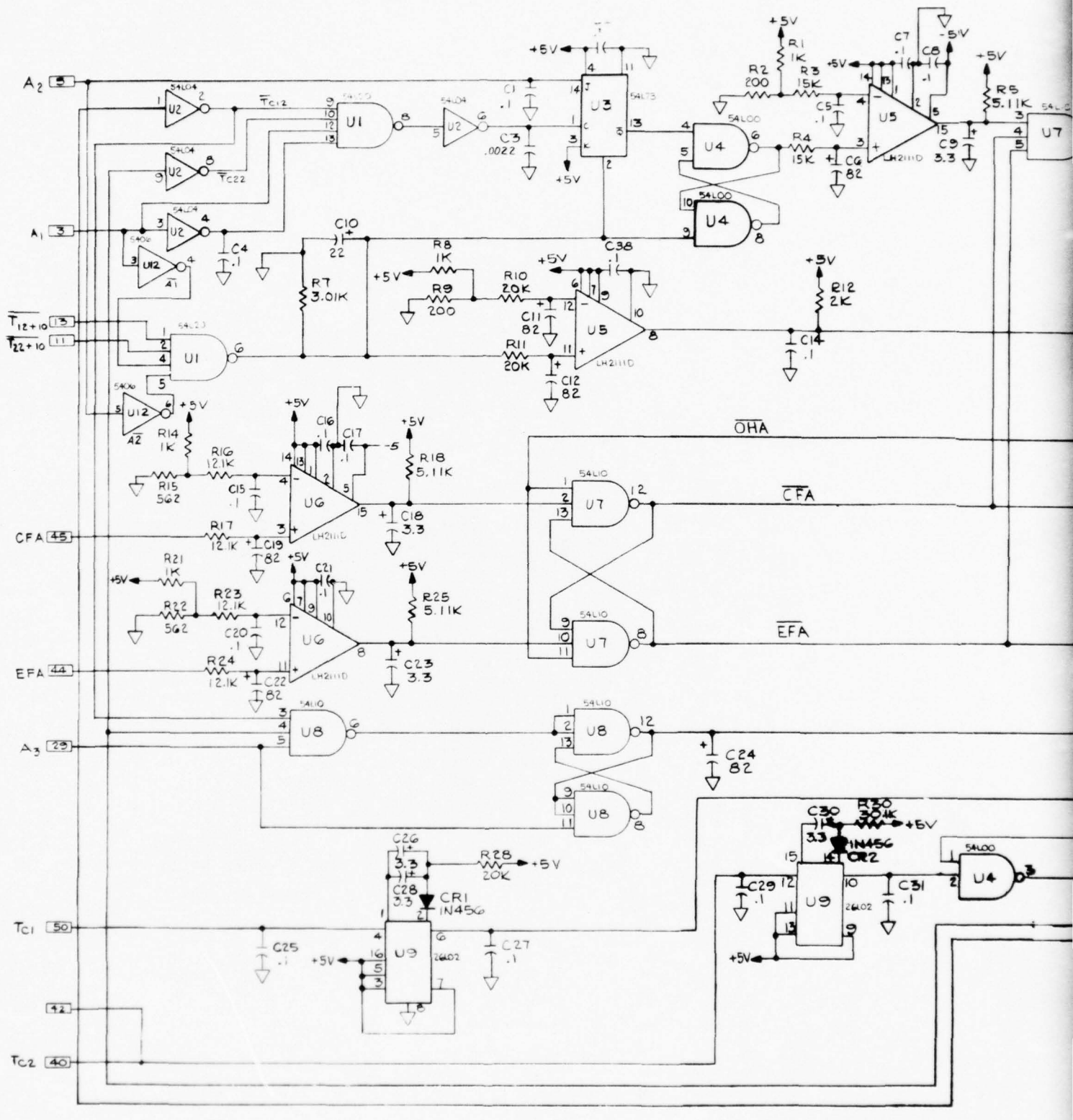
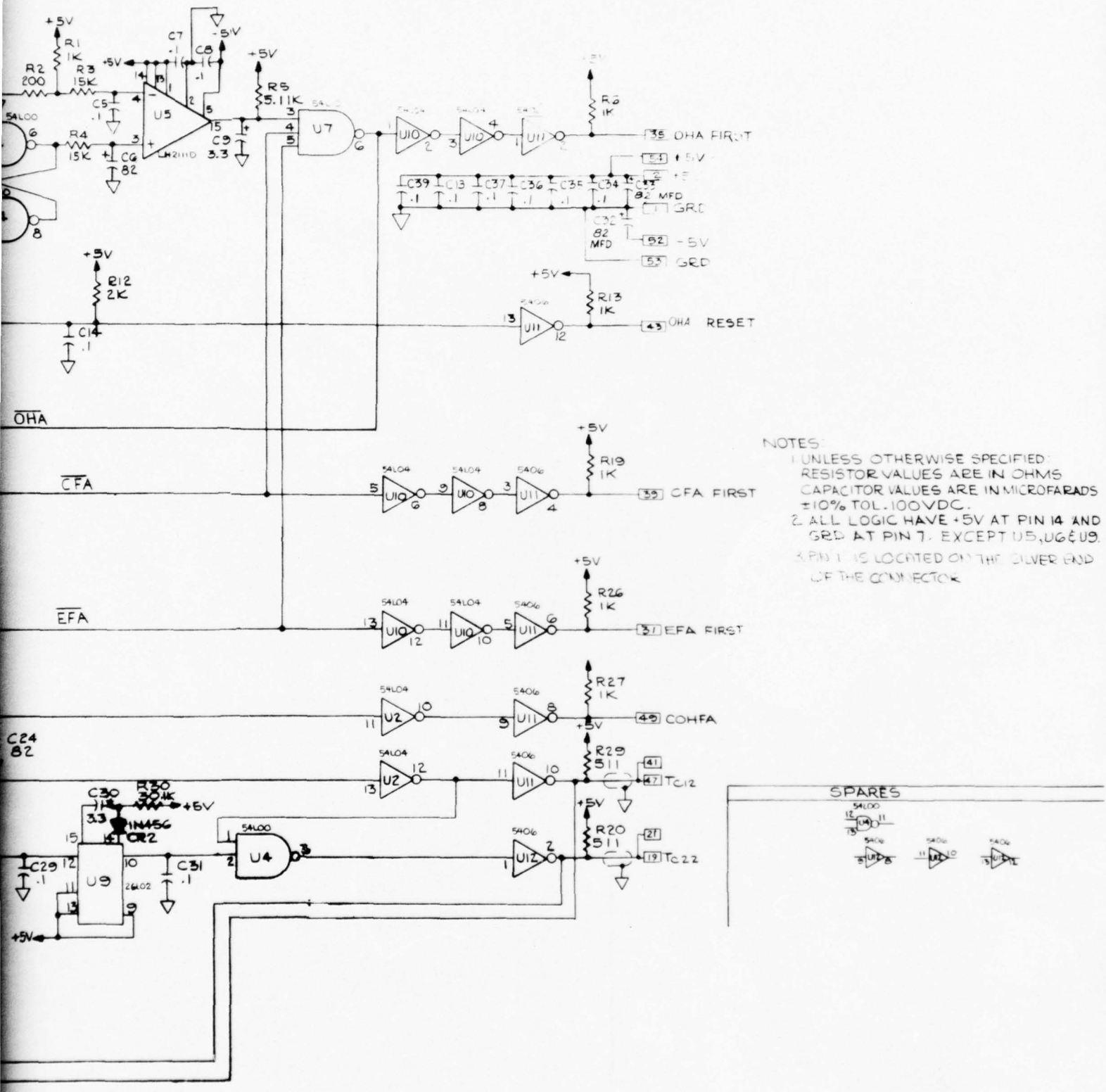


Figure 17. Schematic Wiring Diagram



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTOR VALUES ARE IN OHMS
CAPACITOR VALUES ARE IN MICROFARADS
±10% TOL. 100VDC.
2. ALL LOGIC HAVE +5V AT PIN 14 AND GRD AT PIN 7. EXCEPT U5, U6 & U9.
3. PIN 1 IS LOCATED ON THE SILVER END OF THE CONNECTOR

chematic Wiring Diagram, Multi-Output Logic

Sensor cable and signal processor faults for loop B are obtained in identical fashion with alarm channel amplifiers B1, B2 and B3. A grouping of the fault equations for both sensor cable-alarm channel systems is presented below:

$$CFA = A12\ \overline{TC12}\ \overline{TC22} + \overline{A1}\ \overline{A2}\ A3\ TC12\ \overline{TC22}$$

$$CFB = B12\ \overline{TC12}\ \overline{TC22} + \overline{B1}\ \overline{B2}\ B3\ TC12\ \overline{TC22}$$

$$EFA = \overline{TC12}\ TC22\ (A1 + A2) + TC12\ \overline{TC22}\ (A1\ \overline{A2} + \overline{A1}\ A2 + \overline{A3})$$

$$EFB = \overline{TC12}\ TC22\ (B1 + B2) + TC12\ \overline{TC22}\ (B1\ \overline{B2} + \overline{B1}\ B2 + \overline{B3})$$

Here, the terms TC12 + t and TC22 + t have not been shown because they are not used in fault pulse generation, but in pulse detection only.

2.3 Multiple Output Circuitry

The multiple output board, board A for example, provides in the main, overheat detection and signal presentation (OHA) for its associated sensor cable-signal processor channel, a bidirectional solid state interlock between OHA and correspondingly, cable fault signal CFA and signal processor fault signal EFA, a simple electronic fault term COHFA, and stretched pulses TC12 and TC22 which are expansions of clock pulses TC1 and TC2, respectively. Refer to Figure 17.

One generated through first-come first-serve logic, OHA is applied to the Crew Read-out Unit for storage to be combined with other signals, should they occur. Signals CFA and EFA are by way of first-come first-serve logic, applied to the signal correlator board to be combined with those fail terms, which heretofore, have not been considered (fail terms for the clock and power supplies) to derive OHFA. The CFA signal is also applied to the Maintenance Warning Unit for presentation of a cable fault.

2.3.1 Overheat Detection (Channel A for example)

A study of the truth table shown in Appendix IV results in the following equation of overheat signal OHA:

$$OHA = \overline{TC12}\ \overline{TC22}\ A21$$

Here, A21 indicates the sequence of actuation of processor amplifier A2 before A1 which occurs when a non-instantaneous overheat condition is sensed by Cable A during the no-test period.

2.3.1.1 Overheat and Reset Logic

An overheat condition, A2 before A1, is detected by J-K flip-flop 14-1-13, of U3, and retained by a latch circuit consisting of NAND gates 4-5-6 and 10-9-8 of U4. Both flip-flop and latch circuit are maintained in a normally reset state by the condition represented by the equation:

$$RESET = \overline{\overline{(TC12 + t)(TC22 + t)}\ \overline{A1\ A2}}$$

Here the overall inversion signifies that the reset signal is a logical ZERO which exists when A1 and A2 are normal (each zero) during the no-test period. $\overline{TC12}$ + t and $\overline{TC22}$ + t are used to ensure that A1 and A2 have been attained in the region beyond test.

The reset term is obtained with 4 input NAND gate 1-2-4-5 of U1. Here, $\overline{TC12 + t}$, $\overline{TC22 + t}$, $\overline{A1}$ and $\overline{A2}$ (by way of inverter 3-4 of U12) are normally applied as logical ONE's to input terminals 1,2,4 and 5 respectively of NAND gate U1. This results in the reset function described above being provided at output terminal 6 of U1. By way of the delay network consisting of resistor R11, capacitor C12, and biased comparator 11-12-8 of U5, and inverter 13-12 of U11, reset is also transmitted to output terminal 43 where it is applied to the Crew Readout Unit as OHA RESET.

To present the no-test interval, TC12 and TC22 are NANDed at input terminals 9 and 10, respectively of NAND gate U1.

When activated by an overheat condition, A2 appears first and is applied to J terminal 14 of J-K flip-flop U3. In addition, reset is removed. A1, in following A2, provides, by way of input terminal 12 of U1 and the circuit consisting of inverter 3-4 of U2, capacitor C4, and input terminal 13 of input NAND gate U1, a signal which when combined with $\overline{TC12}$ and $\overline{TC22}$ at terminals 9 and 10 respectively, generates a one-shot pulse representing $\overline{TC12}$ $\overline{TC22}$ A1.

This pulse, when applied to clock terminal 1 of U3 permits A2 information existing at J terminal 4 to be transmitted in inverted form to inverted output terminal 13. The resulting logic is $\overline{TC12}$ $\overline{TC22}$ A21 where the overall inversion symbol denotes that an overheat condition is detected and presented as a logical ZERO. This signal is applied to latch SET terminal 4 of U4. Latch output at terminal 6 of U4 is now $\overline{TC12}$ $\overline{TC22}$ A21 (actually OHA) which by way of the low pass filter consisting of resistor R4, capacitor C6, and biased comparator U5, is applied as a logical ONE to NAND gate 3-4-5-6 of U7. This NAND gate forms part of the solid state interlock circuitry between OHA and CFA or EFA. If, at this time, there is no cable fault or signal processor electronic fault, CFA and EFA appear as logical ONE's at terminals 4 and 5, respectively, of NAND gate 3-4-5-6 of U7, thereby permitting OHA input at terminal 3 to generate a logical ZERO at output terminal 6 of U7.

This ZERO output, after being inverted, appears as a logical ONE (OHA FIRST) at output terminal 35. In addition, this ZERO output is also applied to terminals 1 and 11 of NAND gate 1-2-13-12 and 9-10-11-8 of U7. This action forces CFA and EFA to stay at locigal ONE levels, thereby retaining OHA at NAND gate 3-4-5-6 of U7 and also preventing the presentation of a CFA or EFA output.

When an overheat condition has passed and sensor cable A is once again at a normal no-alarm resistance level, A2 and A1 become deactivated. In turn, logical ONE signals again appear at terminals 1, 2, 4 and 5 of NAND gate U1; the reset term $(\overline{TC12 + t})$ $(\overline{TC22 + t})$ $\overline{A1}$ $\overline{A2}$ is again generated, J-K flip-flop 14-1-13 of U3 and the overheat latch discussed above, are reset and an OHA RESET signal in logical ONE form again appears at

terminal 43 for reset operation of the OHA alarm circuitry located in the Crew Readout Unit.

The overheat pulse from terminal 8 of U1 will be lost if A1 becomes ONE during test time, when TC12 or TC22 are ONE. Then no OVERHEAT indication will be given. Since TC12 and TC22 occupy about 80 milliseconds of the 14.4 second test cycle, one would expect this condition to occur about .080/14.4 = .0055% of the time. This would mean that about one out of every 180 overheat conditions (resulting from one cable) would not give an OVERHEAT indication. Experiments, however, show that only about one out of every 2900 overheat conditions is missed. The reason for this discrepancy is unknown.

2.3.2 CFA and EFA Logic and Interlock.

Since cable fault (CFA) and signal processor fault (EFA) information is derived from the same set of signal processor amplifier channels A1, A2 and A3, the occurrence of both events, if not differentiated, could lead to unintelligible information (two lines in the truth table at one time). For this reason, CFA and EFA are retained on a first-come first-serve priority basis by way of interlock circuitry. This circuitry consists of NAND gates 1-2-13-12 and 9-10-11-8 of U7.

By way of the delay network consisting of resistor R17, capacitor C19, and biased comparator 3-4-15 of U6, a CFA signal, generated by the circuitry described in Section 2.2 is applied as a logical ONE to input terminal 2 of U7. In analogous fashion, an EFA signal, obtained by way of the delay network consisting of resistor R24, capacitor C22, and biased comparator 11-12-8 is applied as a logical ONE to input terminal 10 of U7.

It should be observed that the normal no-fault no-alarm state of $\overline{\text{CFA}}$, $\overline{\text{EFA}}$, and $\overline{\text{OHA}}$ are applied as logical ONE's to their corresponding interlock opposites. That is, $\overline{\text{CFA}}$ and $\overline{\text{EFA}}$ are applied to terminals 4 and 5, respectively, of OHA gate 3-4-5 of U7, CFA is applied to terminal 9 of EFA gate 9-10-11-8 of U7, EFA is applied to terminal 13 of CFA gate 1-2-13 of U7, and $\overline{\text{OHA}}$ is applied to both CFA and EFA gates as described previously. Thus an alarm state for any one of these variables will result in its inverted form locking out the other two.

2.3.3 COHF Circuitry and Logic (Channel A, for example)

As discussed previously, signal processor faults which cause a loss in detection of either cable faults or overheat conditions are designated as EF (EFA for loop A, for example). Even though faults of lesser severity would not necessarily affect normal operation, they would constitute an impending danger in being the cause of future faults of greater severity. The term for these faults, in signal processor A, for example, is COHFA.

An examination of the faults in the truth table lead to a selection of this equation for COHFA:

$$\text{COHFA} = \overline{\text{TC12}}\ \text{TC22}\ \text{A3}$$

This term is obtained by use of NAND gate 3-4-5-6 of U8 and retained by a latch consisting of NAND gates 1-2-13-12 and 9-10 11-8 of U8. Here states $\overline{TC12}$, TC22 and A3 are applied to terminals 3, 4 and 5 respectively. If during $\overline{TC12}$ TC22, A3 is in a false-ON state, all inputs then appear as logical ONE's. This condition results in a logical ZERO output at terminal 6 of U8 which, when applied to terminal 1-2, sets the latch. The resulting output of the latch, at terminal 12 of U8 is, by way of inverters 11-10 of U2 and 9-8 of U11, presented as a logical ONE COHFA signal at output terminal 49 for transmission to the following signal correlator circuit.

After repair, A3 then appears as a logical ZERO during $\overline{TC12}$ TC22 and resets the latch described above, causing the COHFA signal at output terminal 49 to be restored to a normal no-fault ZERO.

2.3.4 TC12 and TC22 Circuitry

As stated previously, test pulses TC1 and TC2 are generated by clock circuitry. Their pulse widths, normally 25 and 15 milliseconds, respectively, are quite adequate for implementing the diagnostics of U/V fire and fire fault detection, but because of the timing relations between overheat amplifier channels A1 and A2, are too small for overheat and overheat fault detection.

TC12, nominally 45 milliseconds, is obtained by applying TC1 to a pulse stretching network consisting of one-shot multivibrator 4-6 of U9 located on the A board. The resulting output is by way of inverters 13-12 of U2 and 11-10 of U11 applied to output terminals 41 and 47 for use at all overheat signal processor circuits and fault circuits (A and B). In like fashion TC22, nominally 35 milliseconds, is obtained by way of one-shot multivibrator 12-10 of U9 and applied by way of NAND gate 1-2-3 of U4 and inverter 1-2 of U12 to output terminals 19 and 21.

On occasion, when power is first applied to the CCU, a false TC22 pulse is generated by U9, at the same time that TC12 is generated. This false pulse is believed to be caused by turn-on transients, and can seriously disrupt the system operation. For this reason, a connection is made from U2-12 to U4-4 to gate out this undesired pulse.

2.4 Signal Correlator Circuitry and Logic

Signal correlator circuitry combines the secular warning terms of fire sensor failure, fire signal processor failure, overheat sensor failure (A or B), overheat signal processor failure (A or B), clock failure, and voltage failure, to provide the final signals for overheat fail (OHFA and OHFB), fire fail (FFW), and computer failure (C). This circuitry, which is powered by the +5V reference supply, is shown in Figure 18.

2.4.1 C Correlator Circuitry

The term C represents any electronic failure, simple or serious, in U/V fire signal processor circuitry, overheat signal processor circuitry, in clock circuitry, or in power supply circuitry. The equation representing this correlation is:

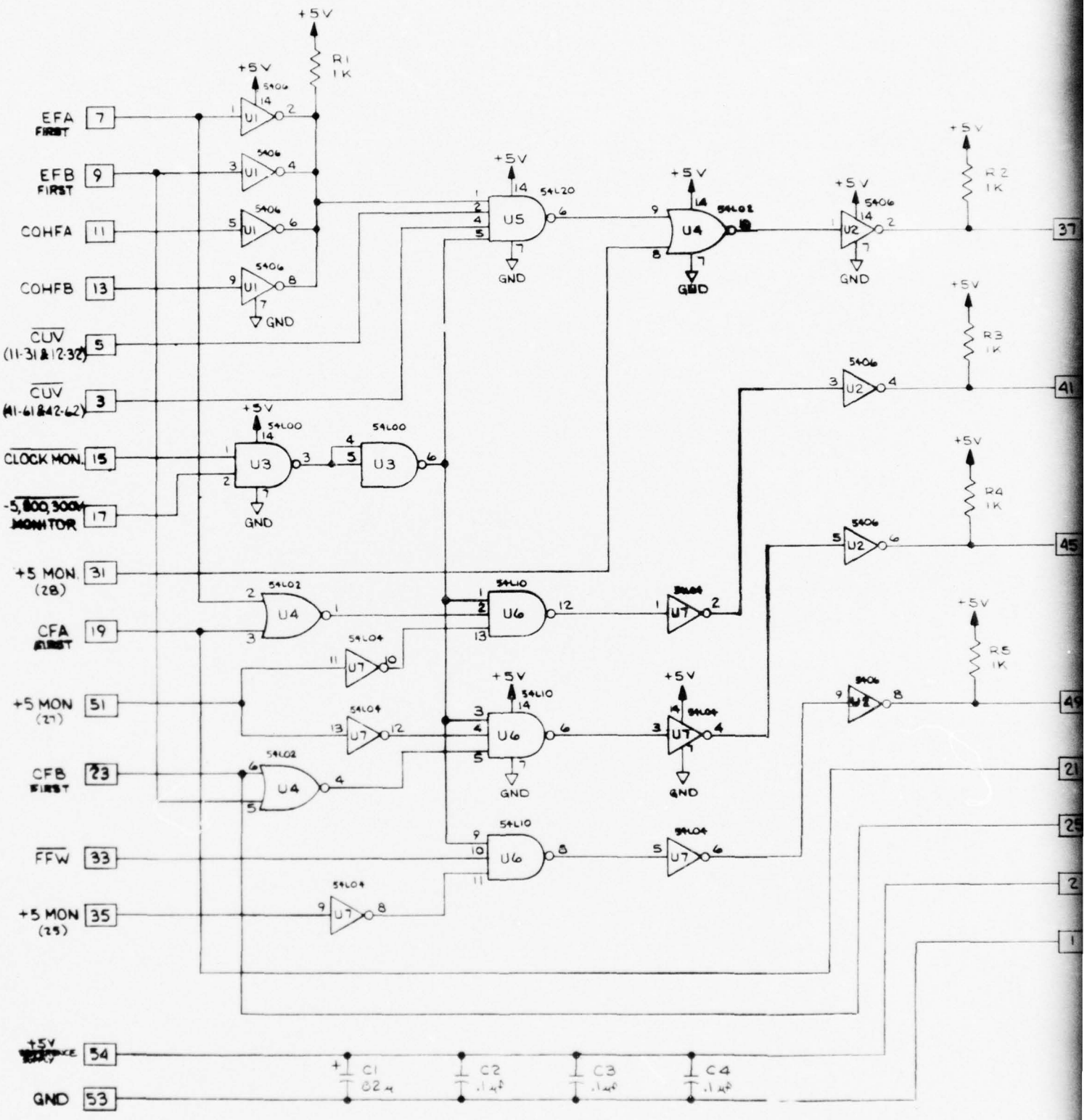
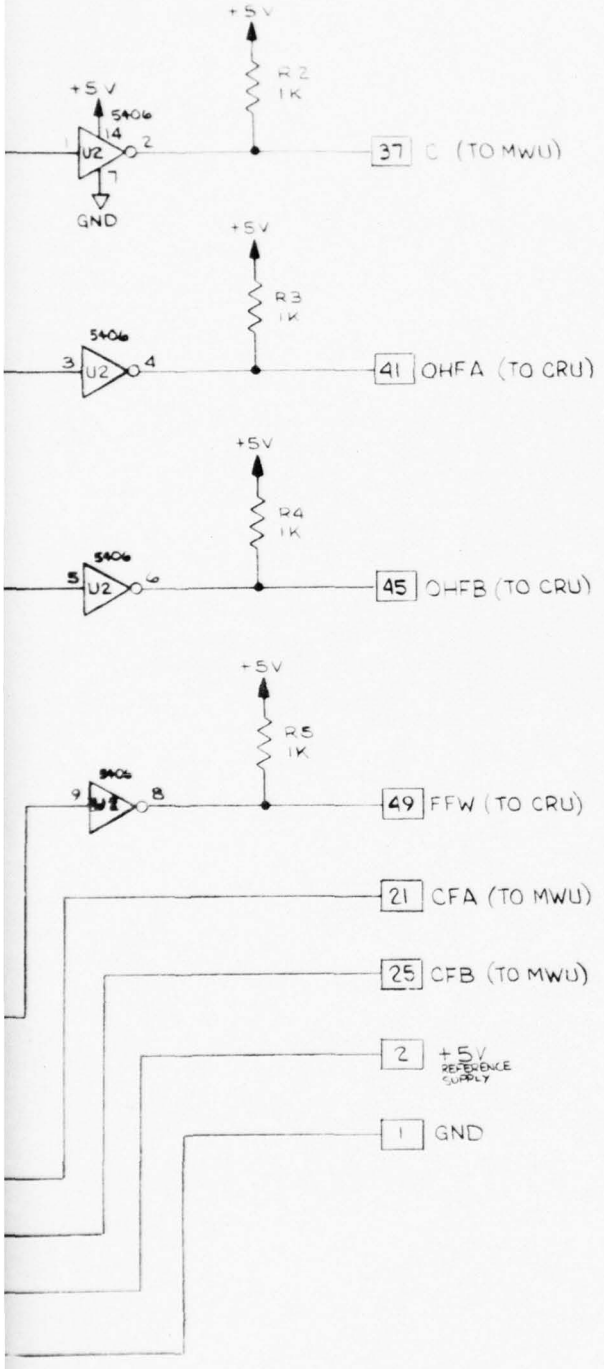


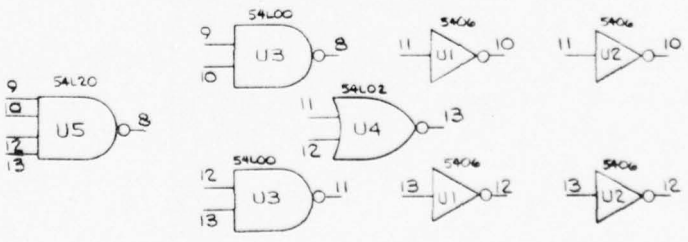
Figure 18. Logic Diagram - Signal



NOTE

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS ± 10% TOL. 100 VDC.
2. ALL LOGIC HAVE +5V AT PIN 14 AND GRD AT PIN 7.
3. PIN "1" IS LOCATED ON THE SILVER END OF THE CONNECTOR.

SPARES



ic Diagram - Signal Correlator

$$C = EFA + EFB + COHFA + COHFB + \overline{\overline{CUV\ (11\text{-}31\ \text{and}\ 12\text{-}32)}} + \overline{\overline{CUV\ (41\text{-}61\ \text{and}\ 42\text{-}62)}} + \overline{\overline{\text{Clock Monitor}}} + \overline{\overline{-5,800,300V\ \text{Monitor}}} + 5V\ \text{Monitor}$$

The right side of the above expression are inputs which are applied to the signal correlator. By way of inverter 1-2, 3-4, 5-6, 9-8 of U1, dual NAND gates 1-2-3 and 4-5-6 of U3, NAND gate U5 and NOR gate 9-8-10 of U4, all of the terms are ORed. The resulting output is then inverted by inverter 1-2 of U2 and presented at output terminal C for transmission to the Maintenance Warning Unit. For normal no-fault conditions C is a logical ZERO. When, however, any input presents an electronic fault alarm, C is transferred to a logical ONE state.

2.4.2 OHFA and OHFB Correlator Circuitry

To be complete, overheat failure statements must also include the failures in clock circuitry and power supply circuitry. The equations for OHFA and OHFB now become:

$$OHFA = CFA + EFA + \overline{\overline{\text{Clock Monitor}}} + \overline{\overline{-5,800,300V\ \text{Monitor}}} + 5V\ \text{Monitor}$$

$$OHFB = CFB + EFB + \overline{\overline{\text{Clock Monitor}}} + \overline{\overline{-5,800,300V\ \text{Monitor}}} + 5V\ \text{Monitor}$$

Here, the terms for OHFA, for example, are ORed by way of NAND gates 1-2-3 and 4-5-6 of U3, NOR gate 2-3-1 of U4, inverter 11-10 of U7, and NAND gate 1-2-13-12 of U6. The resulting output from terminal 12 of U6 is, by way of inverters 1-2 of U7 and 3-4 of U2, presented at output terminal 41 for transmission to the Crew Readout Unit.

In like fashion, the terms for OHFB are ORed by way of NAND gates 1-2-3 and 4-5-6 of U3, NOR gate 6-5-4 of U4, inverter 13-12 of U7, and NAND gate 3-4-5-6 of U6. The resulting output from terminal 6 of U6 is by way of inverters 3-4 of U7 and 5-6 of U2 presented at output terminal 45.

For normal no-fault conditions OHFA and OHFB are logical ZERO's. Should a cable or signal processor fault appear at the input, OHFA or OHFB (or both if a fault occurs in each channel) will change from logical ZERO to logical ONE. When a clock or power failure appears, both OHFA and OHFB will change from ZERO to ONE. The individual presentation of OHFA or OHFB to the Crew Readout Unit will result simply in their storage for future use. The presentation of both OHFA and OHFB, however, will result in the display of OHEAT FAIL in the Crew Readout Unit.

2.4.3 FFW Correlation Circuitry

In a manner analogous to the final generation of OHFA and OHFB, FFW is obtained by combining the fire fail warning signal $\overline{FFW}$ with both clock and power failure warning. The equation showing this relation is:

$$FFW = \overline{\overline{FFW}} + \overline{\text{Clock Monitor}} + \overline{5,800,800V\ \text{Monitor}} + 5V\ \text{Monitor}$$

Here the terms for FFW are ORed by way of NAND gates 1-2-3 and 4-5-6 of U3, inverter 9-8 of U7, and NAND gate 9-10-11-8 of U6. The output at terminal 8 of U6 is applied by way of inverter 5-6 of U7 and 9-8 of U2 to output terminal 49.

A presentation of a fault signal at any input will cause the output, FFW, to change from a normal no-fault logical ZERO to a logical ONE.

3. CLOCK GENERATOR AND PULSE TIMING

All of the timing signals necessary to operate the fire detection system and the overheat detection system emanate from this circuit (refer to Figure 19.) The circuit consists of a clock pulse generator whose output is applied to four cascaded counter circuits to obtain pulse edges at certain intervals of time. These timed pulse edges are then decoded and summed to yield the test pulses employed in this system.

3.1 The Clock

The clock pulse generator consists of an integrating circuit timing oscillator U2. Resistors R1 and R2 and capacitor C1 are employed with U2 to generate the basic clock pulse at output terminal 3 of U2. This pulse is a periodic square wave voltage whose width and period of repetition are nominally 100 microseconds and one millisecond, respectively.

3.2 Counting

By way of inverter 9-8 of U13, the clock pulse is applied to a cascaded counter circuit consisting, in the main, of integrated circuit counters U4, U3, U5 and U6. Here, U3, U4 and U6 are 4-BIT ripple binary counters, while U5 is a decade counter wired to provide divide-by-ten counting. By way of NAND gate 9-10-12-13-8 of U12 and NAND gate 1-2-3 of U10, U4 counts and resets with every 15 pulses applied from the clock so as to provide a single 100 microsecond pulse about every 15 milliseconds, a divide by 15 operation.

The output of U4 is now applied to U3, which in turn, provides periodic half-period square wave pulses every 30, 60, 120 and 240 milliseconds (pulse widths of 15, 30, 60 and 120 milliseconds respectively) at terminals 13, 9, 10, and 12 respectively. Here, the 60 millisecond pulse (with a period of 120 milliseconds) at terminal 10 represents a divide-by-8 output which is now applied to divide-by-10 counter U5 to obtain 600 millisecond pulses every 1200 milliseconds. This periodic voltage is applied to input terminal 14 of U6.

Output terminal 12 of U6 provides an unsymmetrical square wave 9.6 seconds long, which is repeated every 14.4 seconds. Repetition is accomplished by employing the coded outputs of terminals 12, 10, 9 and 13 when they render the logic presentation 1, 1, 0, 0 respectively. (This is the standard binary presentation for an input count of 12.) By way of inverters

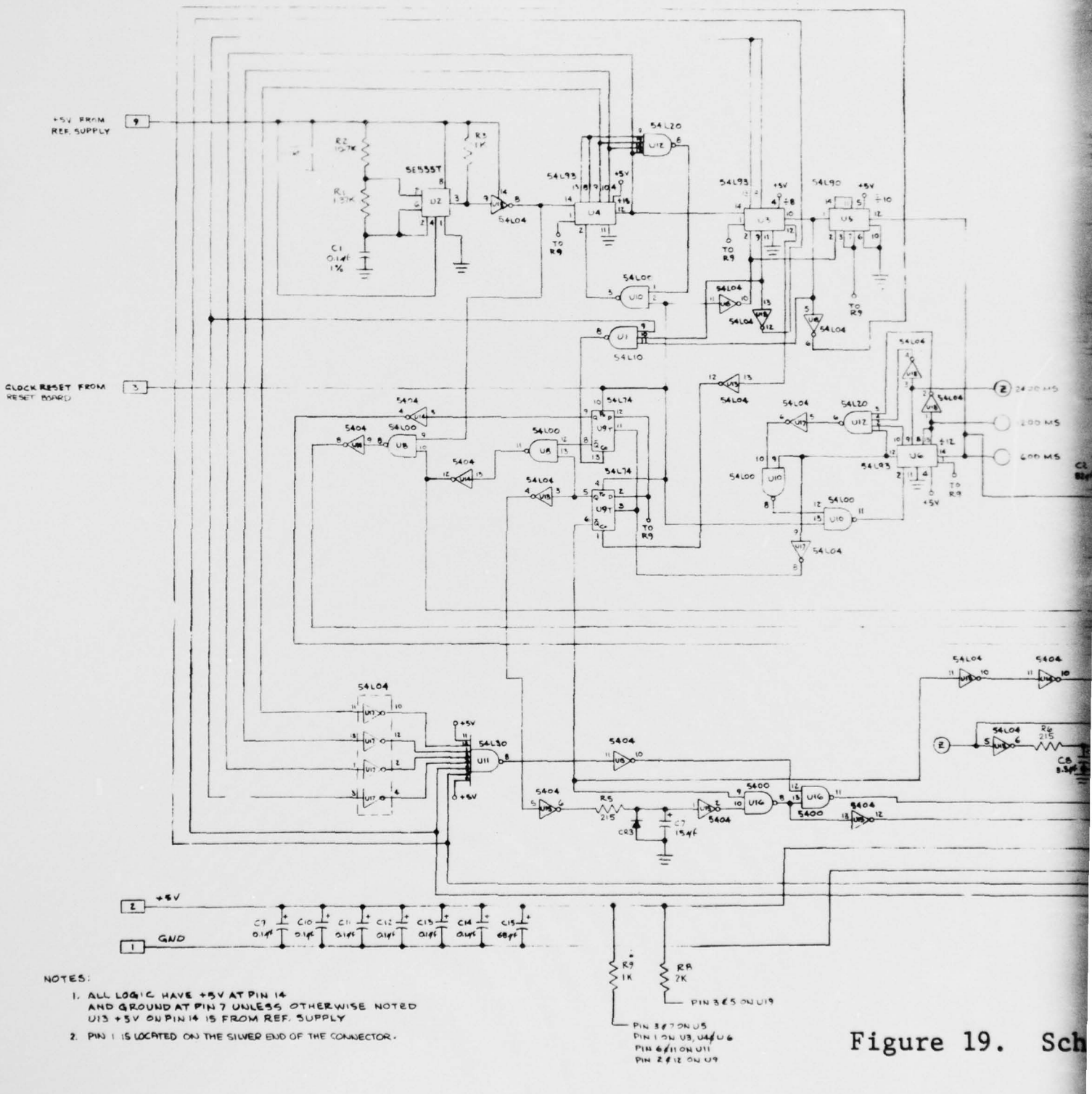


Figure 19. Sch

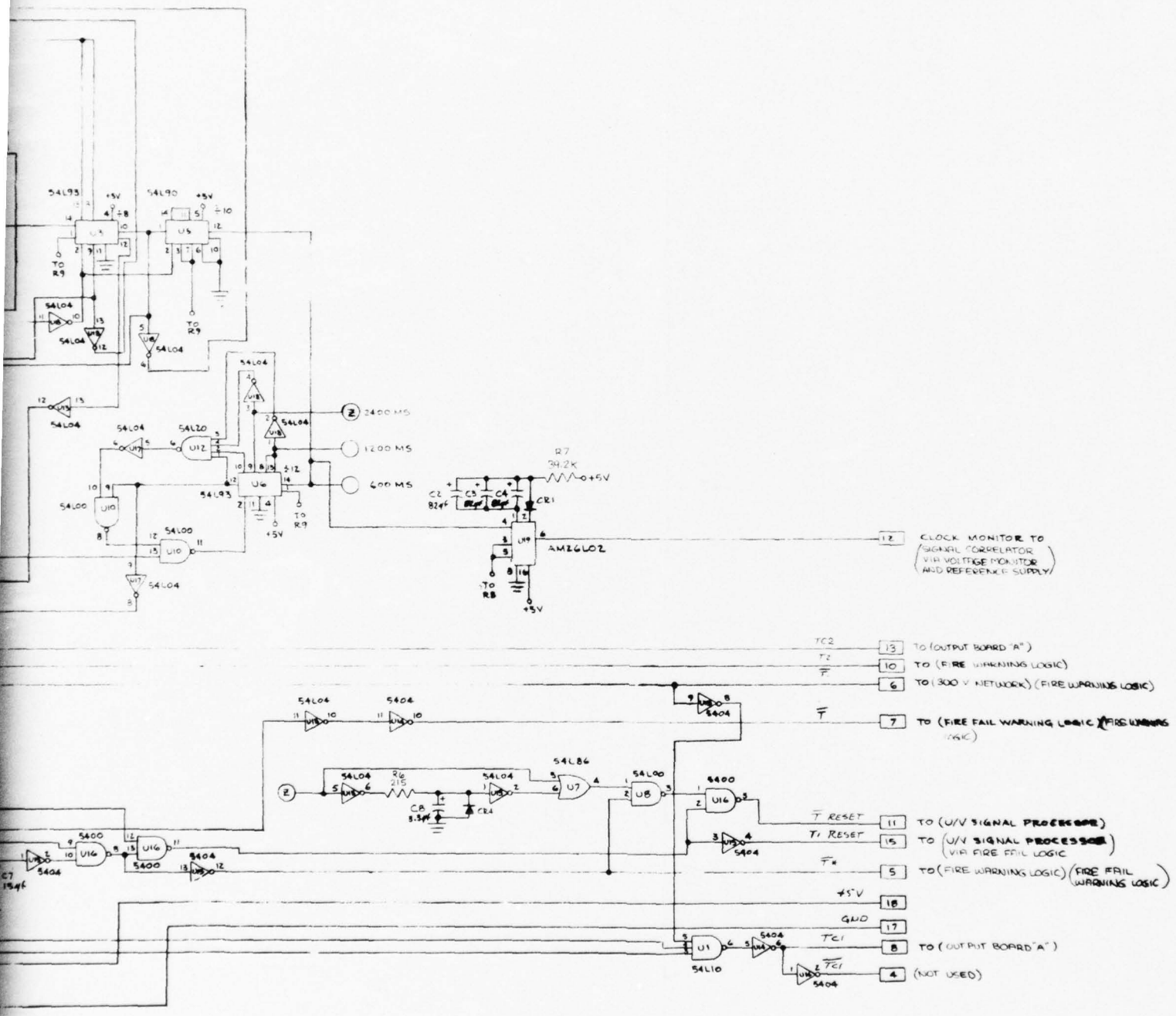


Figure 19. Schematic Wiring Diagram, Clock Generator

1-2 and 3-4 of U18, NAND gate 1-2-4-5-6 of U12, inverter 5-6 of U17 and NAND gates 10-9-8 and 12-13-11 of U10, this divide-by-12 output array generates a reset pulse into terminal 2 of U6, and the process is then repeated 14.4 seconds later (12 counts X 1200 milliseconds per count).

The positive-going front edge of the 9.6 second output pulse is applied every 14.4 seconds to clock terminals 11 and 3 of D-type flip-flops 12-9 and 2-5 of U9, respectively, yielding a logical ONE output at Q terminals 9 and 5 and a logical ZERO at $\overline{Q}$ terminals 8 and 6 every 14.4 seconds. The flip-flops provide a start time reference at which some of the pulses previously mentioned are keyed to generate the test pulses employed in the overheat and fire signal processor and logic circuitry.

3.3 Fire Test Pulses

3.3.1 Test Pulse $\overline{T1}$

Test pulse $\overline{T1}$ is applied to both the U/V glow lamp switch and fire warning logic circuitry every 14.4 seconds.

The pulse width of $\overline{T1}$ is established by first NANDing the binary outputs at terminals 13, 9 and 10 of counter U3 at NAND gate 9-10-11-8 of U1. The resulting output at terminal 8 of U1 appears as a periodic ONE voltage pulse which is 105 milliseconds wide and is repeated every 120 milliseconds.

Since counter U3 is linked by counters U5 and U6 to the basic 14.4 second timing period (about 4 times a minute), the front edge of the first 105 millisecond pulse will coincide with the beginning of the 14.4 second period. The two signals are combined at D-type flip-flop U9 and, by way of inverter 3-4 of U14, are presented as a ZERO level pulse (ONE going to ZERO) which is nominally 105 milliseconds wide and repeated every 14.4 seconds. This pulse, $\overline{T1}$ is presented at circuit output terminal 6.

3.3.2 Test Pulse T2

Test pulse T2 is employed to implement the testing of the U/V signal processor operating in conjunction with Fire Warning circuitry. This test is applied to each U/V alarm channel (Signal Processor and Fire Warning). The pulse is essentially a group of 15 logical ONE pulses grouped in a 15 millisecond time envelope. This group is applied approximately 105 milliseconds after the initiation of the system (14.4 second period) reset pulse and reapplied every 14.4 seconds.

T2 is obtained by NANDing the one kilohertz output clock U2 with a 15 millisecond time envelope which is repeated every test time (14.4 seconds). The envelope is obtained by NANDing the 105 millisecond $\overline{Q}$ output and the 120 millisecond Q output at output terminals 8 and 5, respectively, of D-type flip-flop U9 which is clocked every 14.4 seconds.

3.3.3 Test Pulse $\overline{T}$

Test pulse $\overline{T}$ is used in conjunction with test pulse $\overline{T1}$ to test Fire Fail warning logic. It is obtained from $\overline{Q}$ output terminal 6 of D-type

flip-flop U-9 and, by inverters 11-10 of U13 and 11-10 of U14, applied to output terminal 7. Output $\overline{T}$ is normally at a ONE logic level but is transferred to a ZERO level for 120 milliseconds at the beginning of every system reset period of 14.4 seconds (about 4 times a minute).

3.3.4 Test Pulse $\overline{T*}$

Output $\overline{T*}$ is used to test Fire Warning logic circuitry. It has a normal logic ONE value which is changed to ZERO for 125 milliseconds at the beginning of every system reset time occurring every 14.4 seconds (about 4 times a minute).

The source of $\overline{T*}$ is Q output terminal 5 and $\overline{Q}$ output terminal 6 of D-type flip-flop U-9. $\overline{Q}$ is a 120 millisecond wide logic ZERO pulse occurring every 14.4 seconds. Here, Q is applied by way of inverters 3-4 of U13 and 5-6 of U15, to a delay-shift network consisting of resistor R5, capacitor C7 and inverter 1-2 of U15. The output of the shift network is now NANDed with $\overline{Q}$ to generate a logic ONE pulse at terminal 8 of NAND gate U16 which is 125 milliseconds wide. By way of inverter 13-12 of U15 this pulse is now inverted into output signal $\overline{T*}$ and applied to output terminal 5.

3.3.5 Test Pulse T1 Reset

T1 Reset is a logical ONE double pulse which is used to implement a reset operation on the retriggerable monostable multivibrators in the U/V signal processor. The first pulse is generated at the beginning of system reset and the second pulse occurs 120 milliseconds later. This process is repeated at the beginning of each system reset period of 14.4 seconds (about four per minute).

A periodic pulse is first generated by NANDing the inverted outputs at terminals 9, 10 and 12 of counter U4 with the inverted outputs of 9 and 10 of counter U3. The result at output terminal 8 of NAND gate U11 is now inverted and applied to input terminal 12 of NAND gate U16 where it appears as a periodic logical ONE pulse about 100 microseconds wide which is repeated every 120 milliseconds.

The other input to terminal 13 of NAND gate U16 receives the inverse of $\overline{T*}$ (refer to 3.3.4), namely $\overline{T*}$, which is a logical ONE pulse 125 milliseconds wide occurring at the beginning of each system reset period of 14.4 seconds. The output at terminal 11 of NAND gate U16 is inverted by inverter 3-4 of U15 and appears as the logical ONE double pulse, T1 Reset.

3.3.6 Test Pulse $\overline{T}$ Reset

$\overline{T}$ Reset is a reset pulse which is applied to the U/V signal processor every 2.4 seconds. The 2.4 second repetition time is obtained from output terminal 9 of counter U6 which presents a half-wave pulse 2.4 seconds wide every 4.8 seconds. This output is applied to terminal Z to provide a positive logical ONE keying pulse every 2.4 seconds to input terminal 1 of NAND gate U8 which combines the keying pulse with $\overline{T*}$, a logical ZERO pulse 125 milliseconds wide which is generated every 14.4 seconds (refer to paragraph 3.3.4). The output of U8-3 is now NANDed with

the inverse of T1 reset, namely $\overline{\text{T1 Reset}}$, a logical ZERO double pulse occurring every 14.4 seconds (refer to paragraph 3.3.5). The resulting output, $\overline{\text{T}}$ Reset, is a logical ONE pulse about 100 microseconds wide which is repeated every 2.4 seconds and is synchronized with the 14.4 second system test cycle. Every sixth pulse, at test time, is double.

3.4 Overheat Test Pulses TC1 (Turn-on) and TC2 (Turn-Off)

3.4.1 Test Pulse TC1 (Turn-On)

Output TC1 is a normal logic ZERO level voltage that is transferred to a logical ONE level for 29 milliseconds every system test time (4 times a minute). It is applied to the overheat detection system. It is obtained by combining T1 (obtained by inverting $\overline{\text{T1}}$ with inverter 9-8 of U15) with the inverted forms of outputs 9 and 10 of counter U3 (by way of inverters 13-12 of U18 and 5-6 of U18) at NAND gate 5-4-3-6 of U1. The result is a logic ZERO pulse lasting about 29 milliseconds which, by way of inverter 5-6 of U14, is formed into TC1.

3.4.2 Test Pulse TC2 (Turn-Off)

Output TC2 is a normal logic ZERO voltage which is transferred to a logic ONE state 105 milliseconds after the start of each system test. The logic ONE state exists for about 15 milliseconds. It is applied to the overheat detection system. It is derived by NANDing the 105 millisecond $\overline{\text{Q}}$ output and 120 millisecond Q output at terminals 8 and 5, respectively, of D-type flip-flop U9 at NAND gate 12-13-11 of U8. This results in a normally ONE state signal which is transferred to ZERO 105 milliseconds after the start of each system test (every 14.4 seconds) and restored to logic level ONE 15 milliseconds later. This output is inverted by inverter 13-12 of U14 into output signal TC2.

3.5 Clock Monitor

The clock monitor is a checking circuit that determines proper clock operation. It consists of retriggerable monostable multivibrator U19 which with resistor R7 and capacitors C2, C3 and C4 has a time constant of 2.9 seconds. That is, for a given input pulse, the multivibrator output pulse lasts 2.9 seconds. If input pulses are repeated within 2.9 seconds, the output is maintained at a logical ONE level. The actual input is a logical ONE periodic voltage obtained from the output 13 of counter U6. It is 600 milliseconds wide and is repeated every 1200 milliseconds. If this input is interrupted for more than 2.9 seconds, the multivibrator output will go to logical ZERO. This signal is sent to the Signal Correlator to generate FAIL signals for the Crew Readout Unit and the Maintenance Warning Unit.

4. POWER SUPPLIES

The Computer Control Unit contains a transient and reverse voltage protected power supply system which operates on 28 DC V aircraft power (refer to Figure 11). This system consists of two main switching regulators, a DC to AC inverter, and two linear regulators. One switching regulator supplies, by way of a load filter, 8.5 DC V power to the DC to

AC inverter. The other switching regulator provides an 800 AC V square wave for ultraviolet sensor tube circuitry, and by way of simple rectifier circuitry, 300 DC V for ultraviolet test lamp circuitry and negative voltage for one linear regulator which supplies -5 DC V to logic circuitry. The other linear regulator, in conjunction with a storage capacitor, is used as a reference supply providing prolonged storage type +5 DC V to both signal correlator circuitry and voltage monitoring circuitry.

4.1 Transient and Reverse Voltage Protection

Reverse voltage protection is accomplished by way of a fast recovery power rectifier connected in series with the 28 DC V input power line.

As shown in Figure 20, DC power is applied by way of the rectifier to the transient suppression network which consists of an inductor-resistor circuit connected in series with the power supply system and a voltage-clamping zener diode network connected across the power supply system. Here, the inductor is used to block high-voltage, high-frequency (microseconds to milliseconds) transients and to provide sufficient time for the zener diodes to become effective. The resistor is used to provide current-limiting protection to the zener diodes for relatively long-term transients.

4.2 Switching Regulator

Switching regulators provide at least three major advantages over linear regulators. These are: (1) higher efficiency, seventy-five to eighty-five percent being typical; (2) the use of fewer components and (3) smaller size for a given output power. The switching regulators used in the IFOS are of the self-oscillating type.

The basic circuit is shown in Figure 21. Here, the comparator-driver senses the voltage across the inductor, this voltage being related to the current i_L by the equation:

$$E_L = L \frac{di_L}{dt}.$$

Initially, the load voltage Vo will be zero, and Q1 will be ON. The voltage at the noninverting input will approach this value:

$$V_1 = V_{in} \frac{R_b}{R_a + R_b} + V_{ref} \frac{R_a}{R_a + R_b}$$

When Vo reaches V_1, the comparator will switch, turning Q1 off. The diode, CR1, now becomes forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until Vo reaches this value:

$$V_2 = 0 \frac{R_b}{R_a + R_b} + V_{ref} \frac{R_a}{R_a + R_b}$$

The comparator will switch, Q1 will be turned back on, and the cycle will repeat.

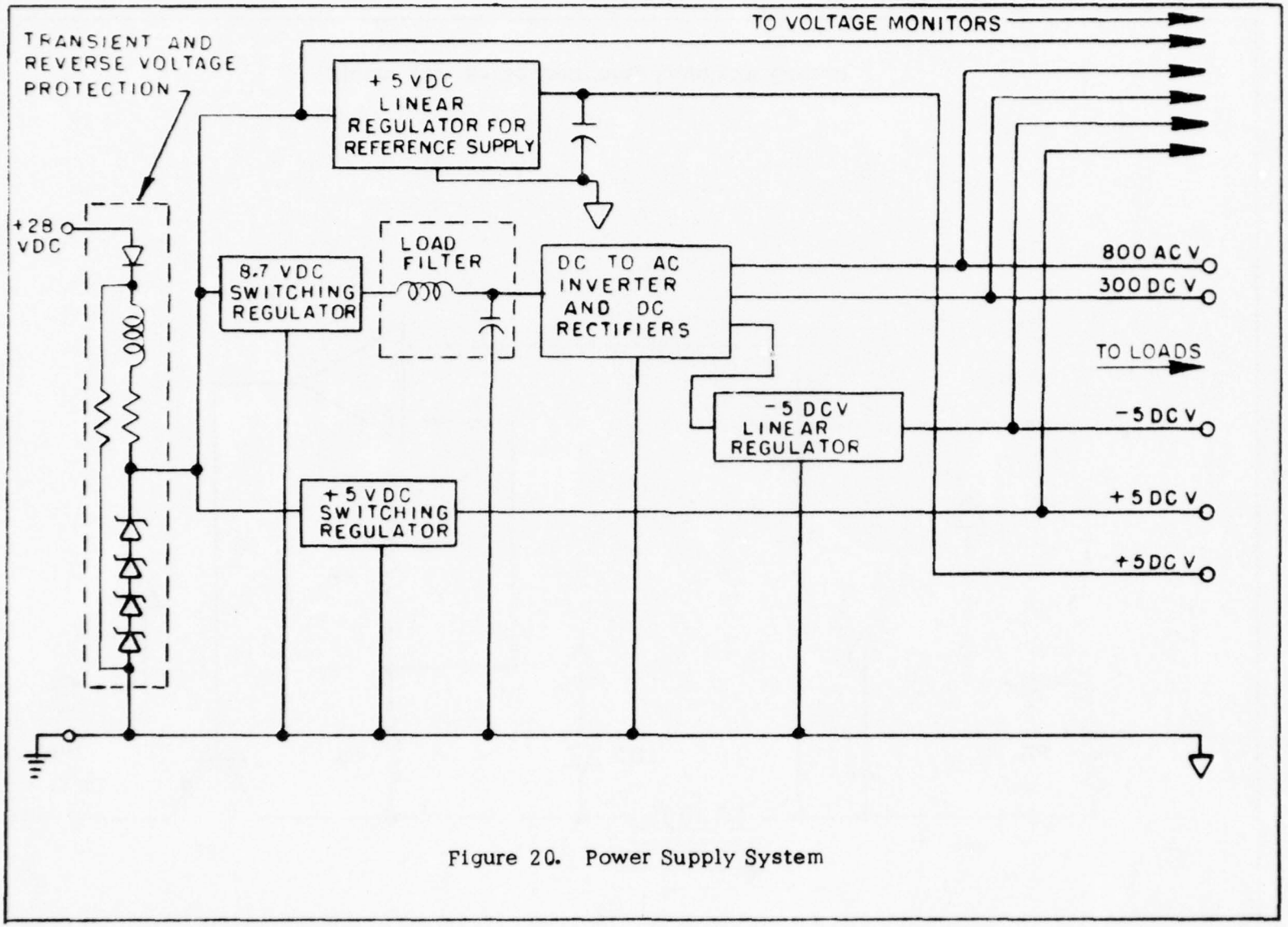


Figure 20. Power Supply System

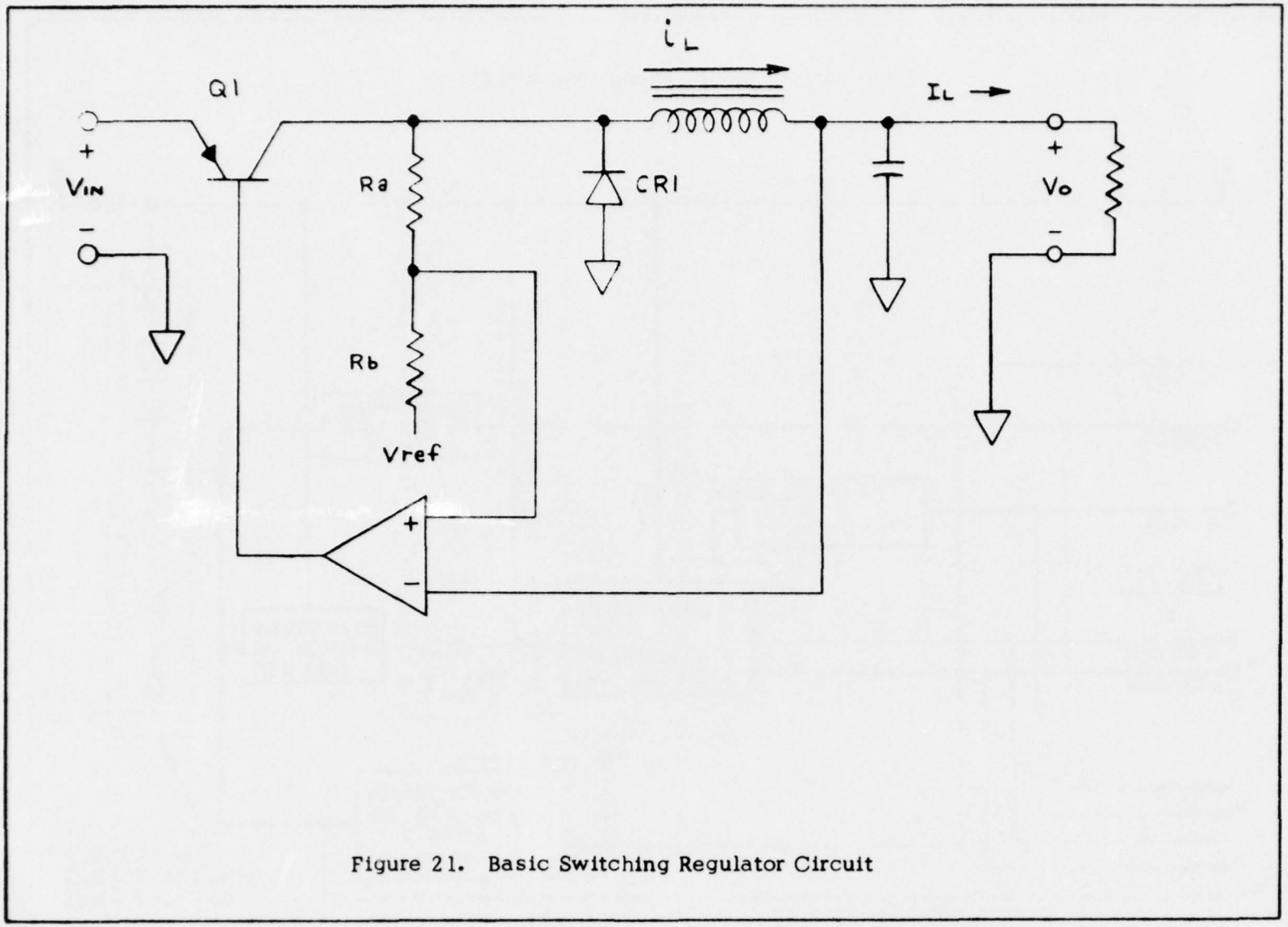


Figure 21. Basic Switching Regulator Circuit

Vo, the output voltage, will necessarily contain a ripple voltage. By properly selecting the values of Ra and Rb, the ripple voltage magnitude can be kept small. The d.c. component of the output voltage will then be approximately V_{ref}.

The switching frequency depends on component values, the input voltage V_{in}, and the average load current I_L. By making this frequency high, inductor size can be minimized, but then the selection of a suitable pass-transistor and diode becomes more critical.

Figure 22 shows the schematic of the switching regulator circuits used in the IFOS. The MC1569R integrated circuit performs the comparator function. The two 2N1711 transistors are used to provide current-limiting. Potentiometers R17 and R20 are used to adjust the two output voltages to the exact values required. Diodes CR2, CR3, CR4 and CR5 are used to prevent the comparator from being driven into saturation, which would cause a decrease in efficiency.

4.3 DC to AC Converter

Operational theory common to most transistor inverters is illustrated by considering the basic push-pull saturable-transformer - coupled two-transistor oscillator circuit of Figure 23.

Here, transformer flux oscillates between the two states of flux density saturation, M and K, shown in Figure 24. The frequency of oscillation can be described by the following equation:

$$f = V \times 10^8/4N1AB$$

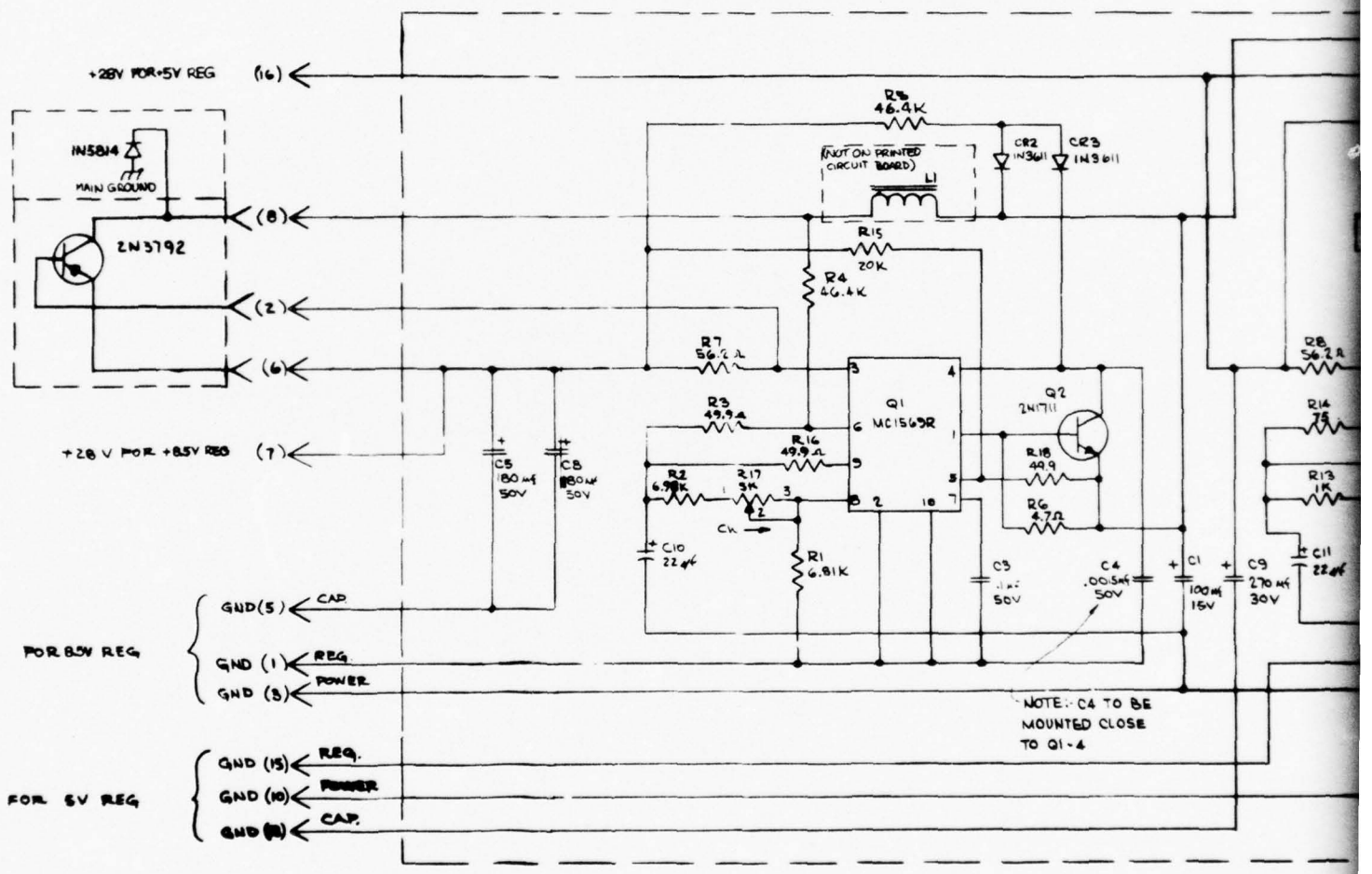
where f is the operating frequency in hertz, V is the peak voltage across the primary winding of N1 turns, A is the cross-sectional area of the core in square centimeters, and B is the saturation flux density in gauss. Here, transformer flux is equal to the product of flux density and core area ($\phi = BA$).

Resistors RB1 and RB2 are employed to equalize the base drive of NPN switching transistors Q1 and Q2, respectively. Resistor R_S assures start-up current to transistor Q1 to ensure the start of proper oscillation.

When voltage V_{cc} is applied and Q1 is turned on, the entire voltage less transistor saturation voltage, is applied across upper primary winding N1 (V = VCC -VceSAT). Current (magnetizing and load) starts to flow into the no-dot end of upper winding N1, and flux and flux density change as a function of time (from saturation level M through J toward saturation level K) at a constant rate to satisfy the equation:

$$V = L \frac{di}{dt}$$

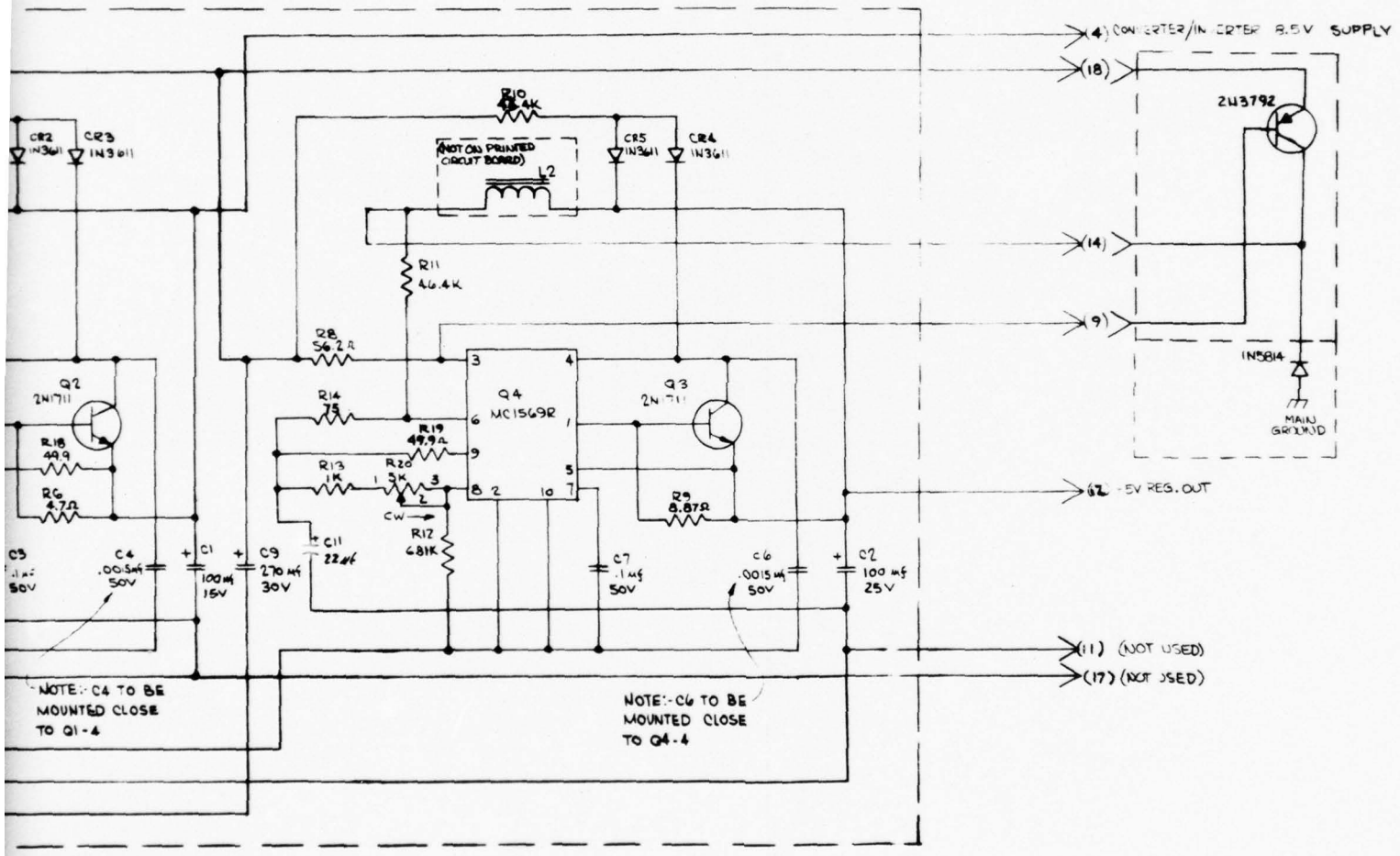
This action causes voltages to be induced which are positive at the no-dot ends of the windings, providing, thereby, a sustaining base drive to transistor Q1, an "off" base voltage to transistor Q2, and a constant output



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PRINTED WIRING BOARD ASSY — 44012

NOTES:
1. PIN "1" IS LOCATED ON THE SILVER END OF THE CONNECTOR.

Figure 22. Printed Wiring Schem



nted Wiring Schematic, Switching Regulator

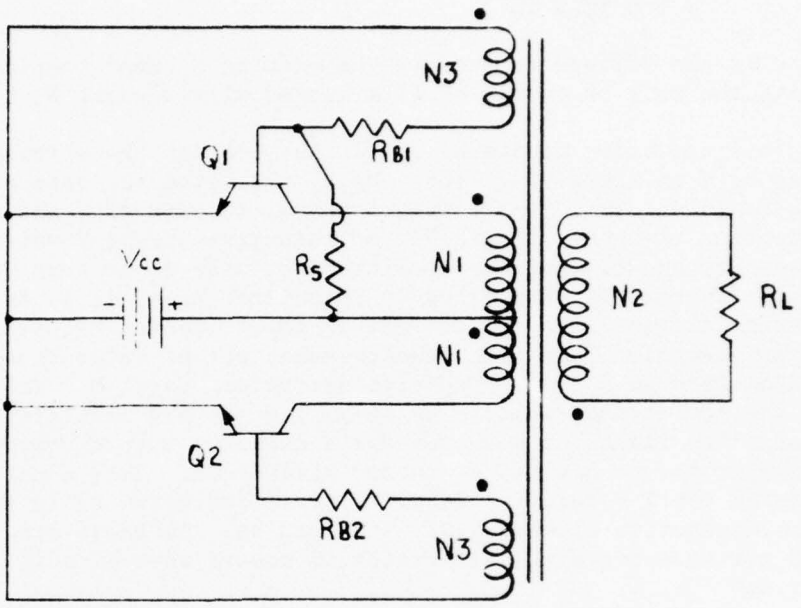


Figure 23. Basic Converter Circuit

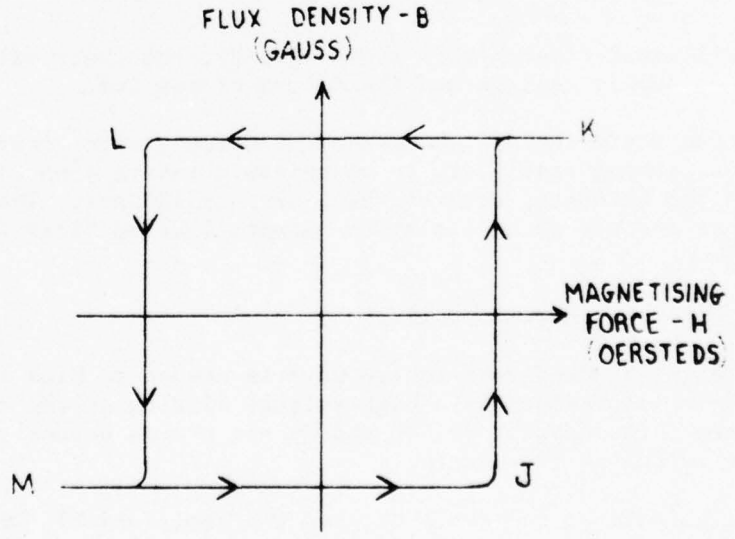


Figure 24. Transformer B-H Curve

voltage which is positive at the no-dot end of output winding N2. All voltages are induced according to the equation:

$$e = N \frac{D\phi}{dt} \times 10^{-8}$$

where e is the voltage induced in the winding N under consideration, and $d\phi/dt$ is the rate of change of flux linked with winding N.

This condition continues until flux reaches the saturation level denoted by K on Figure 24. Then, $D\phi/dt$ and hence the base voltages, decrease rapidly. This causes transistor Q1 to turn off, and, by circuit interruption of upper winding N1, an inductive kickback which reverses the polarity on all windings causing transistor Q2 to turn on. (The time for this reversal is determined by transistor response.) As Q2 starts conducting current into the dot-end of lower winding N1, transformer flux reverses direction, and flux density comes out of saturation level K, traveling through L toward opposite saturation level M. This action sustains the new voltage polarities keeping Q2 on and maintaining Q1 off. The resulting induction now provides a constant output voltage which is negative at the no-dot end of output winding N2. This constant voltage is induced until saturation level M is reached where Q2 is turned off and, again by inductive kickback, Q1 is turned on. As these processes are repeated during succeeding half-cycles, a square wave AC output voltage is produced.

The converter circuit used in the IFOS is shown in Figure 25. It is identical to the circuit just described, except that R_S is made variable. This resistor is carefully adjusted for each individual circuit board to insure oscillator starting under all conditions of load and temperature.

Oscillation frequency is about 1400 Hz, the exact value being a function of supply voltage and the nature of the load.

It was found that if the converter circuit were powered directly from the switching regulator, an undesirable interaction would occur between the two circuits, both of which are oscillators. This problem was overcome by the use of an isolation network labeled "load filter" on Figure 20.

4.4 High-Voltage Power Supplies

An eight-hundred-volt square wave is needed to bias the U/V sensor tubes. This is obtained by a high-voltage winding on the converter transformer. Two capacitors, C6 and C9 are placed across this winding to eliminate switching transients.

The purpose of the diode CR1 and the resistors R7, R8, R9, R11, R12 and R14 is to provide a low d.c. voltage proportional to the high a.c. voltage. This low voltage is called "Attenuated 800V" and is used for monitoring purposes--see reference (5). During initial equipment adjustment, the high voltage is set to exactly 800V by means of the adjustment on the switching regulator. Then, "Attenuated 800V" is set to exactly 1.000V by means of R12.

A three-hundred volt direct current supply is needed to operate the test sources in the U/V detector heads. This is obtained by use of a second high-voltage winding on the converter transformer, a rectifier diode (CR2), and a filter capacitor (C8).

4.5 Negative Voltage Power Supply

A negative five volts is required for operation of the CCU circuitry. This power supply is physically located on the Converter-Inverter board and the schematic appears in Figure 25.

A ten-volt square wave is taken from a winding on the converter transformer. This is changed to d.c. by diode bridge CR3, and filtered by C5. The potential difference is then reduced to five volts by an integrated-circuit linear voltage regulator, Q2. The output voltage is set by resistors R3 and R4, and is typically -5.3V. Resistors R5 and R13 limit the output current to about 140mA. Further details of operation can be found in reference (5).

4.6 Reference Supply

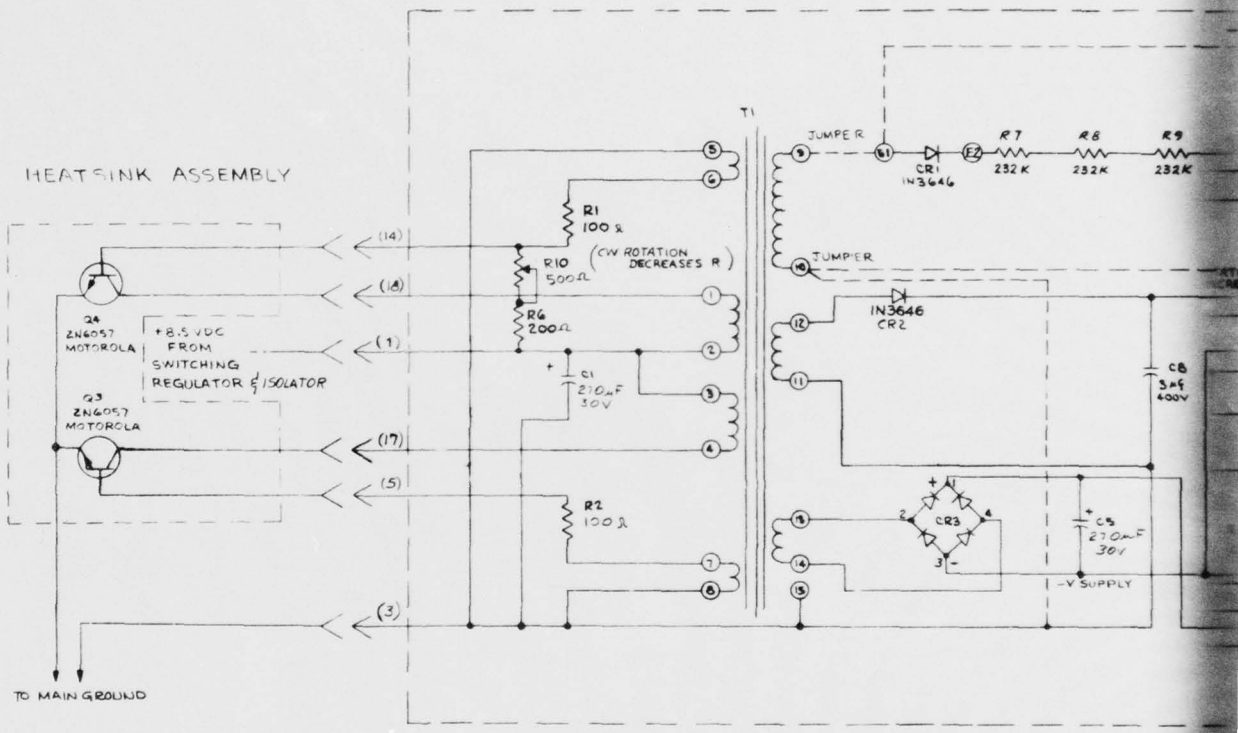
In order to detect and register certain types of system defects, and to simplify the "reset" circuitry described in reference (6), it is desirable to have available an auxiliary five-volt supply. This "reference supply" should come on before the regular five-volt supply when the main power is supplied, and should maintain an output voltage longer than the regular supply when power is turned off.

A linear series-type regulator, operated from the main +28 DCV (after the transient-suppressor), meets the above requirements. Physically, this circuit is located on the A10 printed-circuit board, with the pass-transistor mounted on the CCU sidewall, and the output storage capacitor mounted outside of the card rack. Most of the circuitry is shown in Figure 26, while the complete circuit is shown in Figure 27.

In this circuit, the integrated circuit MC1569R supplies a voltage reference and an error amplifier. The 2N6057 transistor is of course the series control transistor, while the 2N1711 transistor and the 20 ohm resistor are part of the current-limiting circuit. The output voltage is determined by the 1.91 Kohm and 6.81 Kohm resistors together with the 2 Kohm potentiometer which is used for exact adjustment. It is the purpose of the 2700 ufd capacitor to maintain the output voltage for a number of milliseconds after power is turned off. Further details can be found in reference (6).

5. VOLTAGE MONITORS

Voltage monitors are employed in the Computer Control Unit to detect failures in power supply circuitry and excessive drift in supply voltages. These malfunctions, in effect, constitute a major electronic fault because they can cause improper circuit behavior leading to failures in fire and overheat detection.

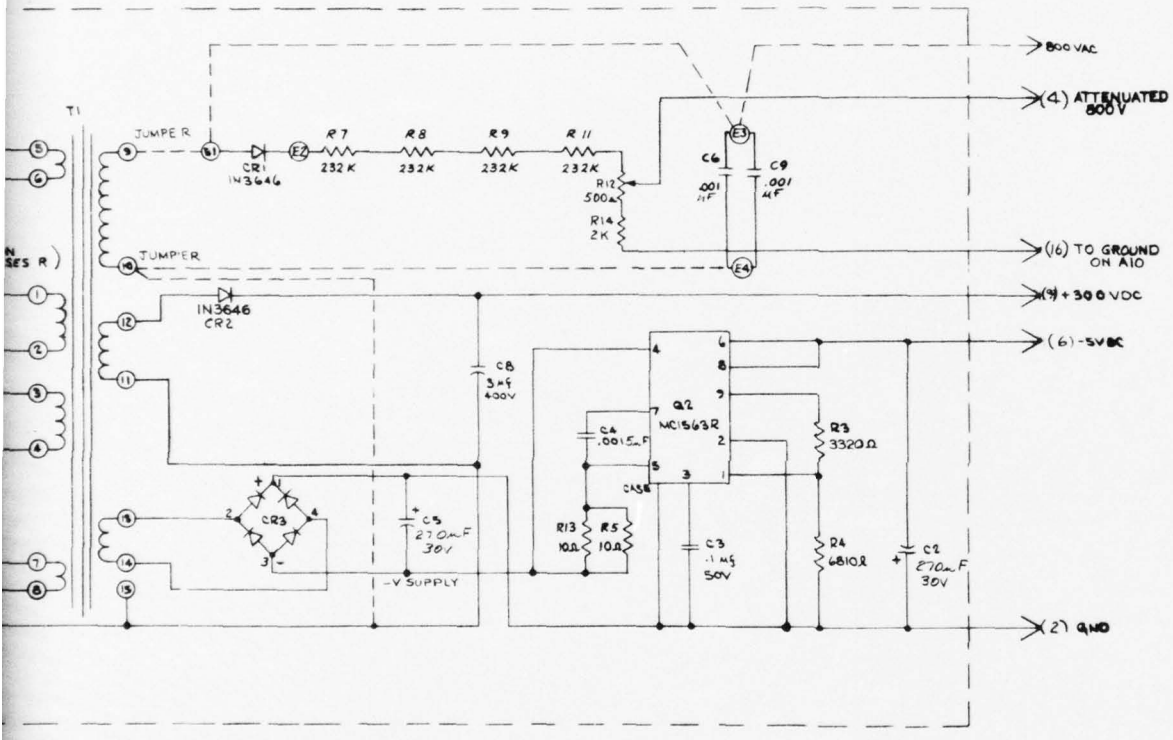


PRINTED WIRING BOARD ART WORK - 6372
PRINTED WIRING BOARD ASSY — 44010

NOTES:

1. PIN 1 IS LOCATED ON THE OUTER END OF THE CONNECTOR.

Figure 25. Printed Wiring Schematic - C



nted Wiring Schematic - Converter/Inverter

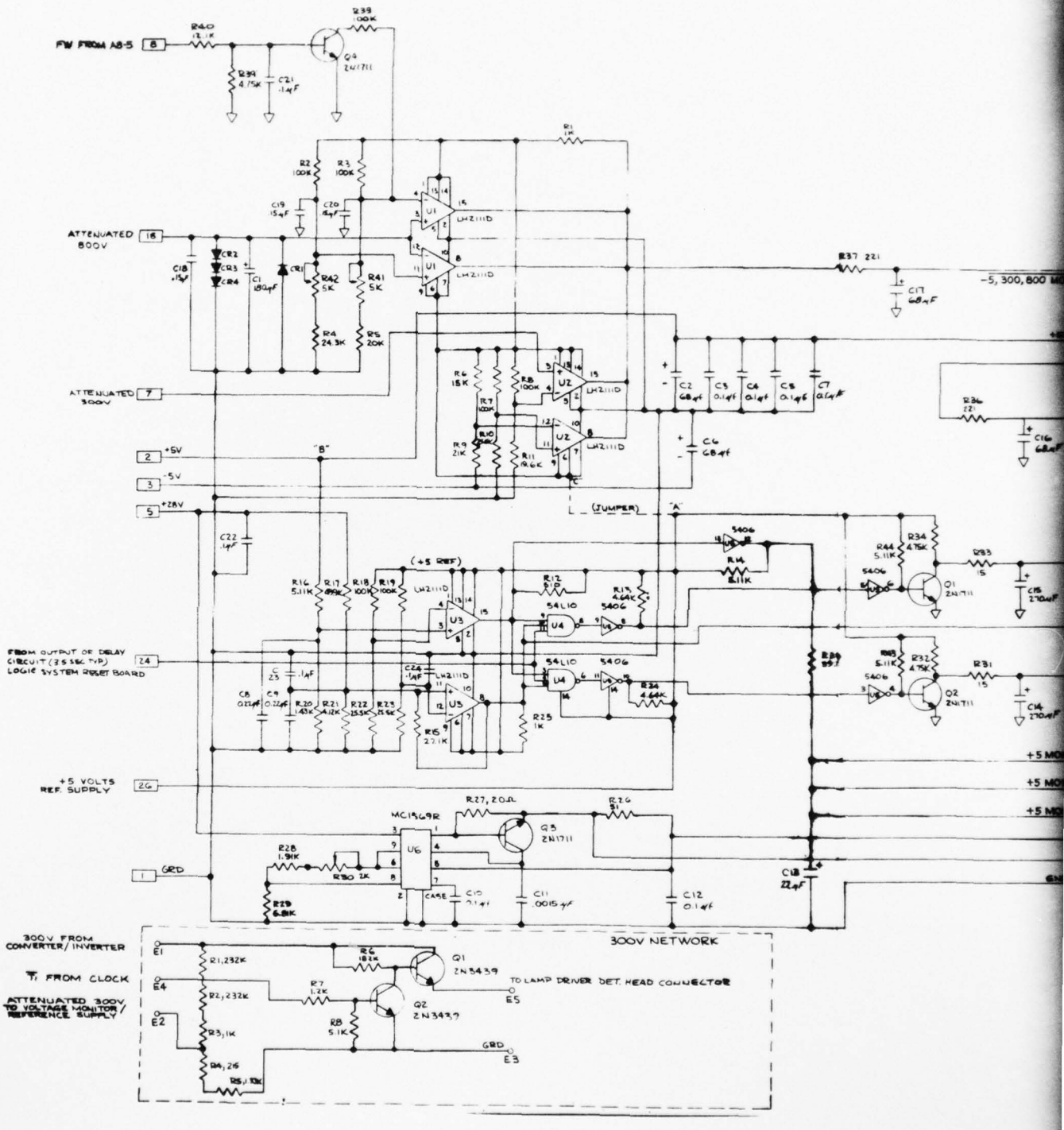
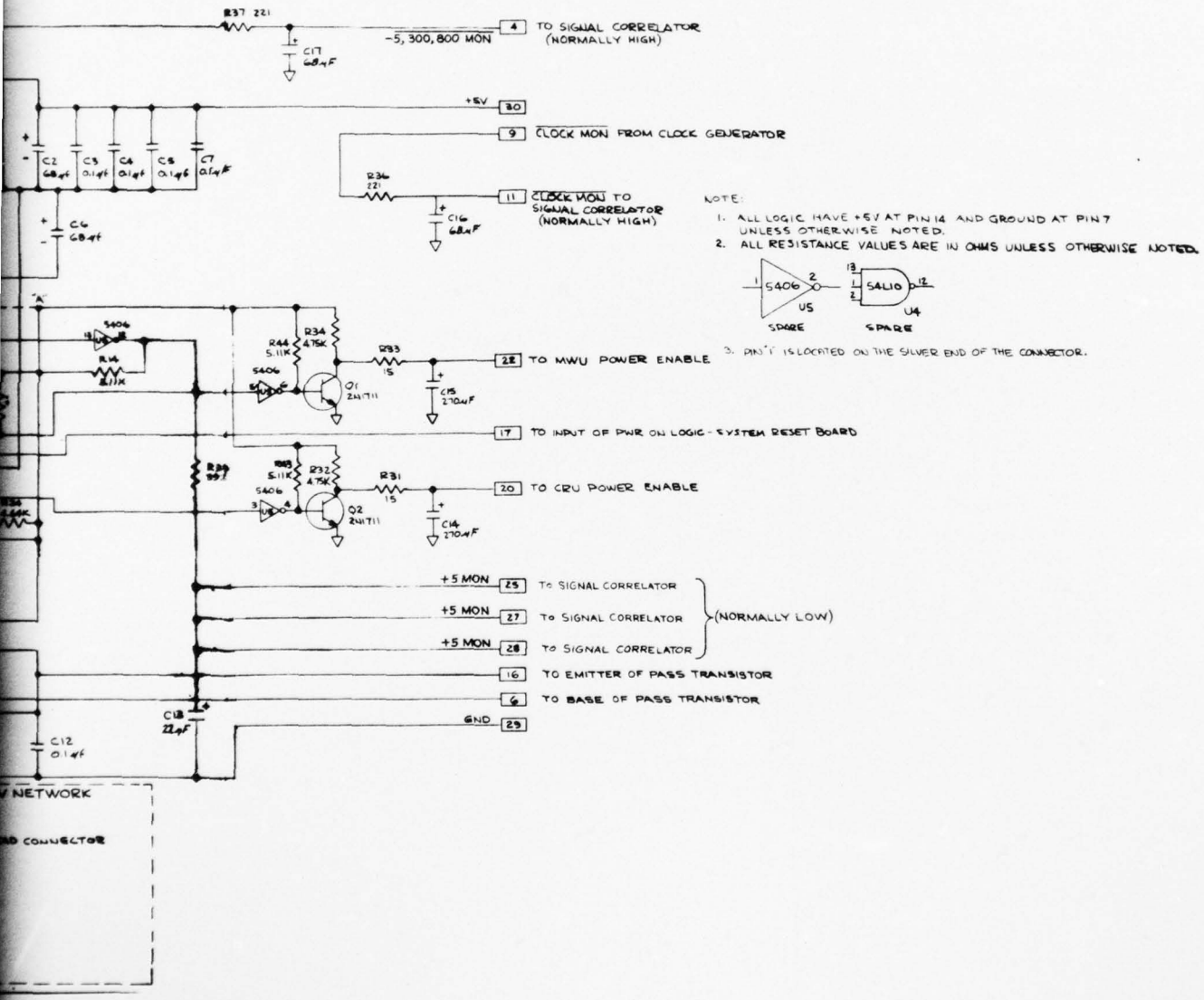


Figure 26. Schematic Wiring Diagram, Vo
Supply +300V Network



matic Wiring Diagram, Voltage Monitor/Reference
ly +300V Network

81/82

All voltage monitoring is done by way of bridge detection networks (refer to Figure 26). Here, signals obtained by sampling the supply voltages under consideration are applied to biased integrated circuit comparators which perform the function of voltage-level detection. A loss or a prohibitive change in a particular supply voltage beyond a predetermined level causes the corresponding comparator to provide a fail signal to the signal correlator which then generates fail signals for use in the Crew Readout Unit and/or the Maintenance Warning Unit.

5.1 800 ACV, 300 DCV, and -5 DCV Voltage Monitoring

Comparator outputs for 800 ACV, 300 DCV and -5 DCV voltage monitoring are "wire ORed" to pull-up resistor R1. Here, the signals for normal no-fault conditions, and a power supply failure, are presented as logical ONE and a logical ZERO, respectively.

5.1.1 800 ACV Monitor

By way of a rectifier and voltage divider sampling network located near the DC to AC inverter, and C1, a filtered DC analog signal of the 800 ACV supply is applied to a dual-level detection network. This network consists of set-point resistors R2, R4 and R42, and comparator 12-11-8 of U1 for high-voltage-level detection, and resistors R3, R5 and R41 and comparator 3-4-15 of U1 for low-voltage-level detection. Here, the high and low AC voltage boundary levels are set at 850 ACV and 750 ACV, respectively.

When a fire condition occurs, transistor Q4 is turned on to lower the low AC voltage boundary to about 630 volts. Thus loading effects on the AC supply by the U/V sensor tubes will not disrupt operation.

5.1.2 300 DCV Monitor

By way of a resistive voltage-divider network connected to the 300 VDC output, an analog signal of the 300 VDC supply is applied to terminal 3 of comparator U2. Here, the level below which the 300 VCD supply must not drop is 247 volts which is established by set point resistors R8 and R11.

5.1.3 -5 DCV Monitor

The -5 DCV supply voltage and the +5 DCV reference supply voltage are summed by way of resistors R9 and R6, respectively, at inverting terminal 12 of comparator U2. If the magnitude of the -5 DCV supply voltage decreases beyond a certain level (becomes less negative, increasing toward zero) the net voltage summed at terminal 11 (established by R7 and R10), and comparator 11-12-8 of U2 then generates ZERO fault signal at terminal 8.

5.2 Line Voltage and +5 DCV Monitoring

The loss or interruption of line voltage and/or +5 DCV power to all logic circuitry could, during transition time, be the source of spurious signals which, in reaching the Crew Readout Unit and Maintenance Warning Unit, could give rise to false warnings. Comparators 3-4-15 and 11-12-8

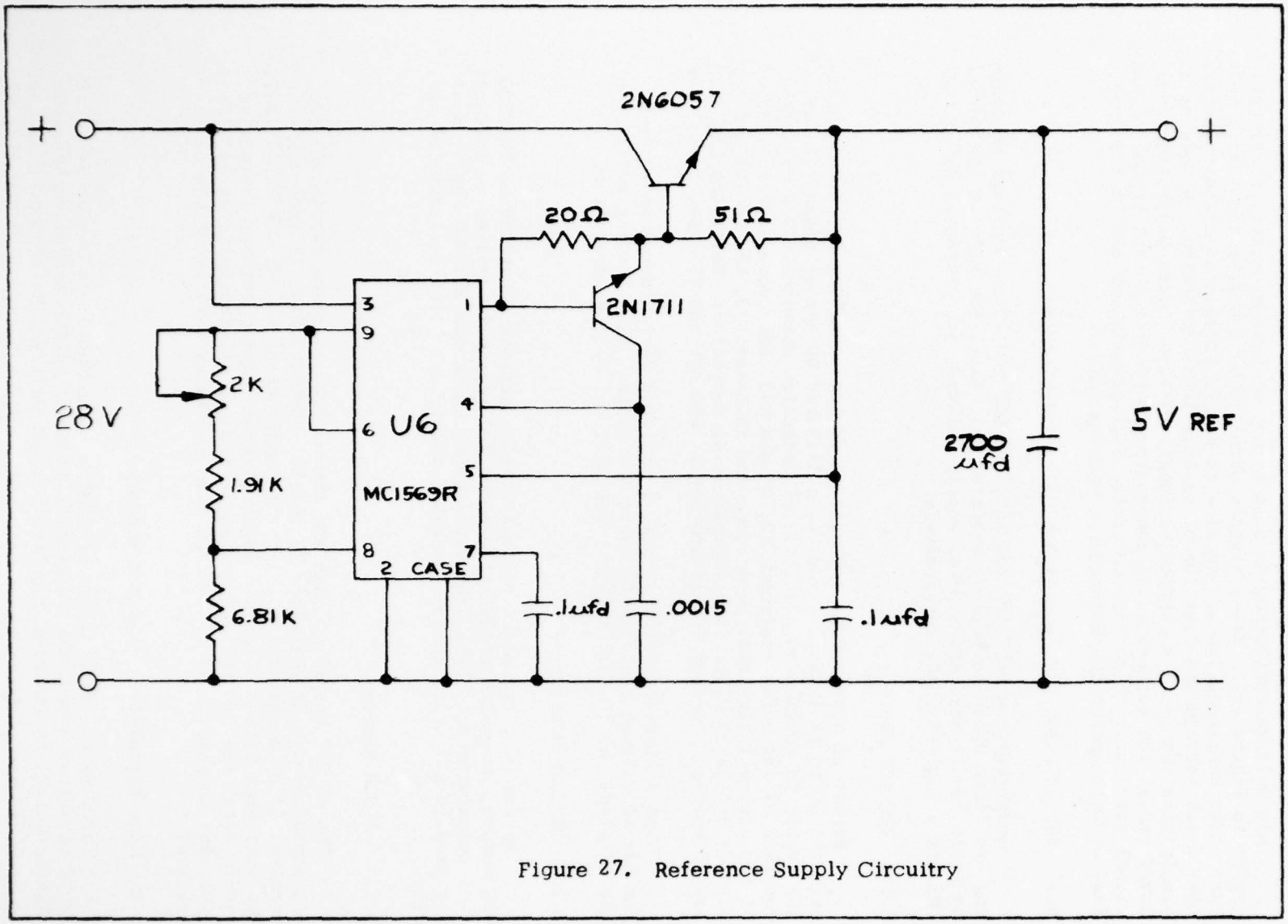


Figure 27. Reference Supply Circuitry

of U3 are the monitors for the +5 DCV supply and line voltage, respectively, and are powered by the +5 DCV reference supply discussed in Section 4.6.

5.2.1 +5 VDC Monitor

By way of voltage divider resistors R16 and R20, a signal voltage analog of the +5 DCV supply voltage is compared to the set voltage established by resistors R18 and R22 and applied to terminal 3 of U3. When the +5 DCV supply voltage fails, comparator 3-4-15 of U3 provides a ZERO signal to inverter 13-12 of U5. In turn, this inverter then provides a logical ONE fault signal to the signal correlator which then sends fail signals to the Crew Readout Unit and Maintenance Warning Unit.

5.2.2 Line Voltage Monitor

A signal-voltage analog of line voltage is applied by way of resistors R17 and R21 to comparator 11-12-8 of U3. Resistors R19 and R23 set the bias level of this comparator. Positive feedback resistor R15 is used to eliminate undesirable oscillation which would otherwise occur when the comparator happened to be biased into the linear region of operation. As will be discussed later in the section on Reset System operation, this comparator operates in conjunction with NAND gates 9-10-11-8 and 3-4-5-6 of U4, inverters 9-8 and 11-10 of U5, and the Reset System to maintain logical ONE enabling signals to enable circuitry in the Maintenance Warning Unit and Crew Readout Unit. Under normal no-fail conditions, the logical ONE signals maintain the enabling networks in a conductive state and, thereby, maintain power to the display and relay circuitry in the Maintenance Warning Unit and Crew Readout Unit.

Should a loss or interruption of line power occur, comparator 11-12-8 provides a logical ZERO to NAND gates 9-10-11-8 and 3-4-5-6 of U4 which change the outputs of inverters 9-8 and 11-10 respectively, from a logical ONE to a logical ZERO. As a result, the enable circuits in the Maintenance Warning Unit and Crew Readout Unit are deactivated, and power to all relay circuitry is removed.

6. SYSTEM RESET

When power is first applied to the IFOS, the various flip-flops and monostables in the system assume unpredictable states. These states are a function of many unknown factors, including manufacturing tolerances. At this time, improper signals are sent to the Crew Readout Unit and to the Maintenance Warning Unit, which could cause the latching relays of those units to latch in improper positions, and thus present a false and misleading display. Therefore, when power is applied to the system, the relay-driver power supply must not be energized until a "reset" signal has been applied to various circuits in the Central Computer Unit to place them in their proper states.

Further, when power is removed from the system, improper relay latching is again possible. As the supply voltages fall toward zero, the various circuits will begin to malfunction, and again improper signals are sent to the CRU and the MWU. Hence, the relay-driver power supply must be rapidly turned off before any of the other circuits begin to malfunction.

It is also necessary to have a means for manual resetting of the various latching relays of the system, after mainenance work has been done, for example.

To summarize, the system reset circuitry must perform these functions:

1. Issue a "reset pulse" to all CCU circuits (but not CRU or MWU circuits) when power has been applied and when the input voltage has risen to a satisfactory level.

2. Turn on the power supply to the CRU and MWU relay drivers after the reset pulse has been issued.

3. Turn off the power to the relay drivers rapidly whenever the main input voltage falls to levels too low for satisfactory operation.

4. Reset the latching relays of the CRU and the MWU when the manual RESET button is pressed.

The circuitry to accomplish the above is physically located on the Reset printed-circuit board (A5) and on the Voltage Monitor Board (A10). Schematic diagrams are found in Figure 26. For the convenience of the reader, part of this circuitry is also shown in Figure 28.

6.1 Description of Operation

First, consider the first three functions above. When power is applied to the CCU and reaches a voltage of about 14V, the output from the 11-12-8 section of comparator U3 (on A10) becomes a ONE. This is sent to the Reset board as the "28V MONITOR" signal. This comparator is of straight-forward design, except that feedback resistor R15 has been added. This resistor prevents oscillation which would otherwise occur when the comparator was biased in the linear region.

On the Reset board, the 28 V MONITOR signal releases the two U1 monostable circuits from the direct clear condition, gates on the +5 V power to the rest of the circuitry, and provides one input to U3 NAND gate. When capacitor C2 charges up to a few volts, the monostable 4-5-6 of U1 is triggered by the negative-going signal on pin 8 of U3.

The positive-going signal on pin 6 of U1 in turn triggers monostable 11-12-10 of U1. Thus, both monostables are triggered at about the same time. Monostable 4-5-6 has a period of about 2.0 seconds, while 11-12-10 has a period of about 3.2 seconds.

When the monostable 4-5-6 triggers, a reset pulse is generated and sent to the Clock Generator by circuits not shown in Figure 28. About 2.0 seconds later, when the 4-5-6 monostable returns to its normal state, a second reset pulse is generated.

At the end of 3.2 seconds, the other monostable returns to its normal state. Pin 10 of U1 becomes a ZERO which results in a ONE on board-connector pin 10, which is labeled "Reset Delay," and which is sent to a printed-circuit board A10.

On A10, the Reset Delay signal is applied to NAND gates 9-10-11 and 3-4-5 of U4. By this time, the +5V power supply will be in normal operation and there will be a ONE on pin 15 of U3. Of course, pins 5 and 10 of U4 are ONE as these pins are connected to the 28V MONITOR line. Thus all inputs to both NAND gates are ONE, and the MWU and CRU relay enable signals become ONE. These enables then cause power to be applied to the MWU and CRU relay-drivers, and normal system operation begins.

When the input voltage falls down to a value where the various power supplies begin to malfunction, the 28 V MONITOR signal goes to ZERO which makes the relay enable signals quickly go to ZERO and hence quickly removes power from the relay-drivers. Also, the two monostables on A5 are forced to the CLEAR state (if they are not already in that state) in preparation for a new power-on sequence.

Because of various timing problems, on occasion pulses appear on the outputs of the U4 NAND gates of A10, at inappropriate times. Components C14, C15, R31, R32, R33 and R34 form low-pass filters to remove these unwanted pulses.

The latching relays of the MWU AND THE CRU can be reset by pushing the RESET button on the MWU. Signals from the switch are "debounced" by two U4 NAND gates on board A5. The output from the debouncing circuit triggers the monostable 11-12-10 of U2, which has a period of 1.0 second. The output from the monostable is inverted and sent to the MWU to activate the reset relay. This reset action is inhibited during the normal 3.2 second turn-on delay by the connection to pin 13 of U2 on board A5.

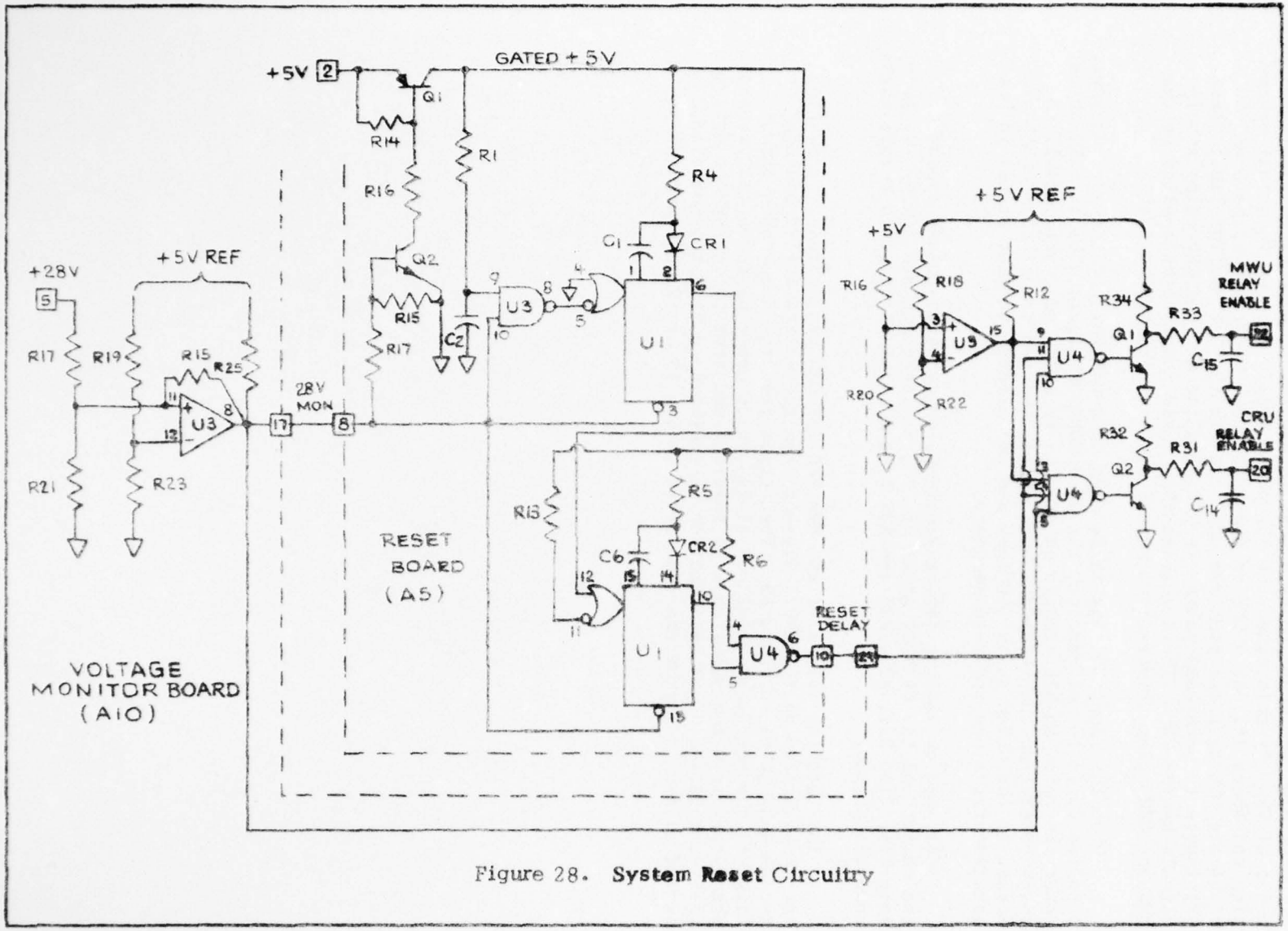


Figure 28. **System Reset** Circuitry

V.

CREW READOUT UNIT

I. APPROACH

The Crew Readout Unit contains a red FIRE warning lamp, a white FIRE FAIL warning lamp, an amber OVERHEAT warning lamp, a white OVERHEAT FAIL warning lamp, and an indicator lamp test switch.

The approach which was selected for handling this display was the employment of transistor-amplifier-driven relays sensing logic network signals from the Computer Control Unit and providing contact actuation of the visible warning displays.

2. CREW READOUT POWER

As shown in Figure 29, the 28 DCV input power first passes through a transient and reverse voltage protection network and then goes to two 12 DCV power supplies. One supply is for powering the indicator lamps, while the other supplies power to the relay coils and the transistor drivers. The output from the "Relay Regulator" power supply is gated by the "Relay-Enable" network.

2.1 Transient and Reverse Voltage Protection

As with the Computer Control Unit, reverse voltage protection is accomplished by way of a fast-recovery power rectifier connected in series with the 28 DCV input power line.

DC power is applied by way of the rectifier to the transient suppression network which consists of an inductor-resistor circuit connected in series with both the relay power supply and the lamp power supply, a clamping zener diode network and a capacitor. See Figure 30. The capacitor is necessary to prevent the relay and lamp power supplies from developing oscillations.

2.2 Relay Power Disable Circuitry (Refer to Figure 30.)

The relay power disable circuit is employed to provide power to the relay circuits during normal operation conditions. Here, a continuous logic ONE signal, provided by the voltage monitor and reference supply circuitry in the Computer Control Unit, is applied to transistor Q2, which maintains series transistor Q1 in a conducting state, providing, thereby, power to relay circuitry. Should a power failure or power interruption occur in the Computer Control Unit, this continuous signal is immediately removed and relay power is disabled. By way of the voltage monitoring circuitry, the reference supply, and a system reset circuit (refer to Figure 28) the continuous logical ONE signal is reapplied a few seconds after the resumption of Computer Control Unit power, enabling power to be reapplied to the relays. This delay is used to allow all logic circuitry in the Computer Control Unit to be stabilized prior to the reapplication

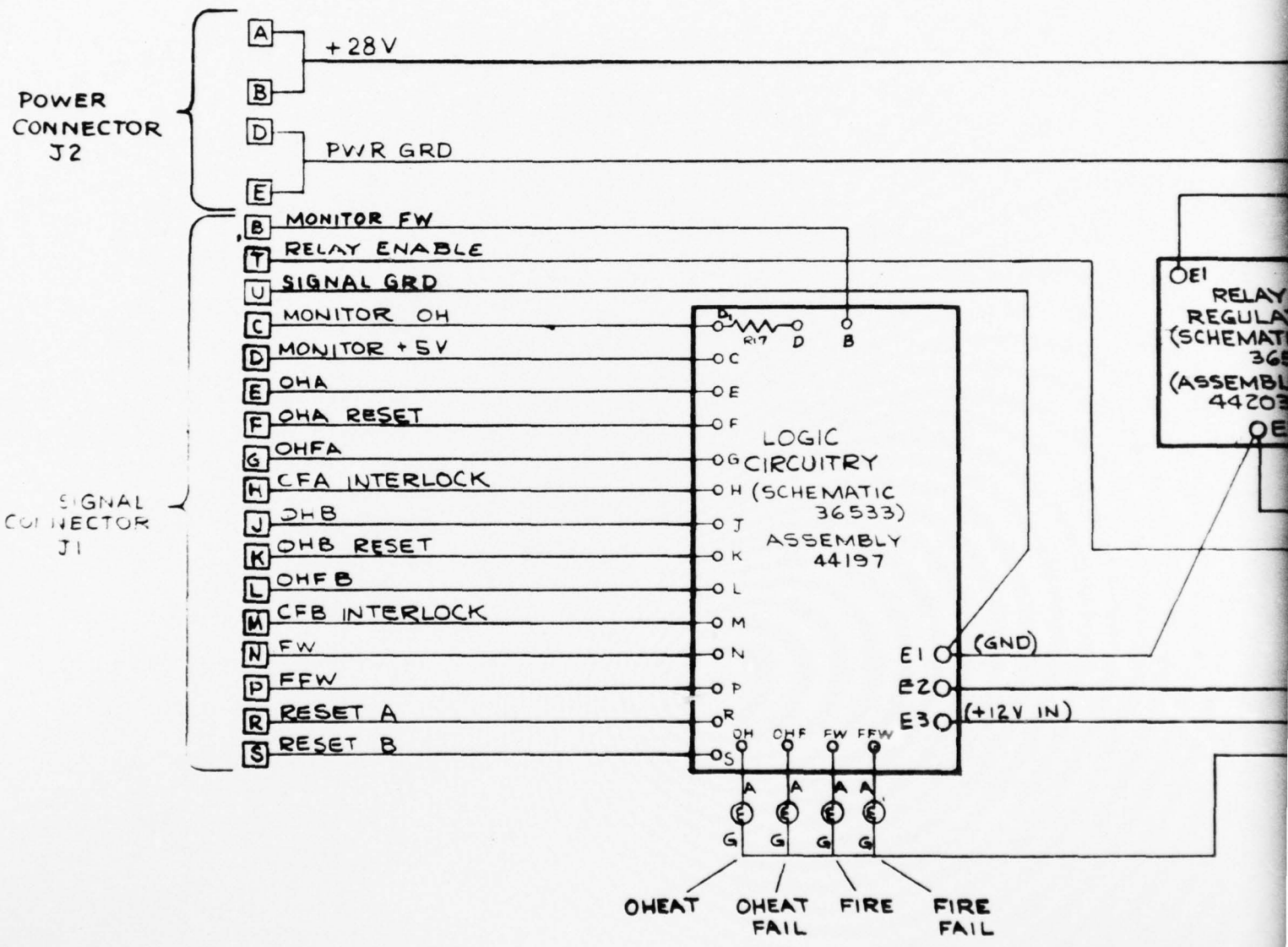
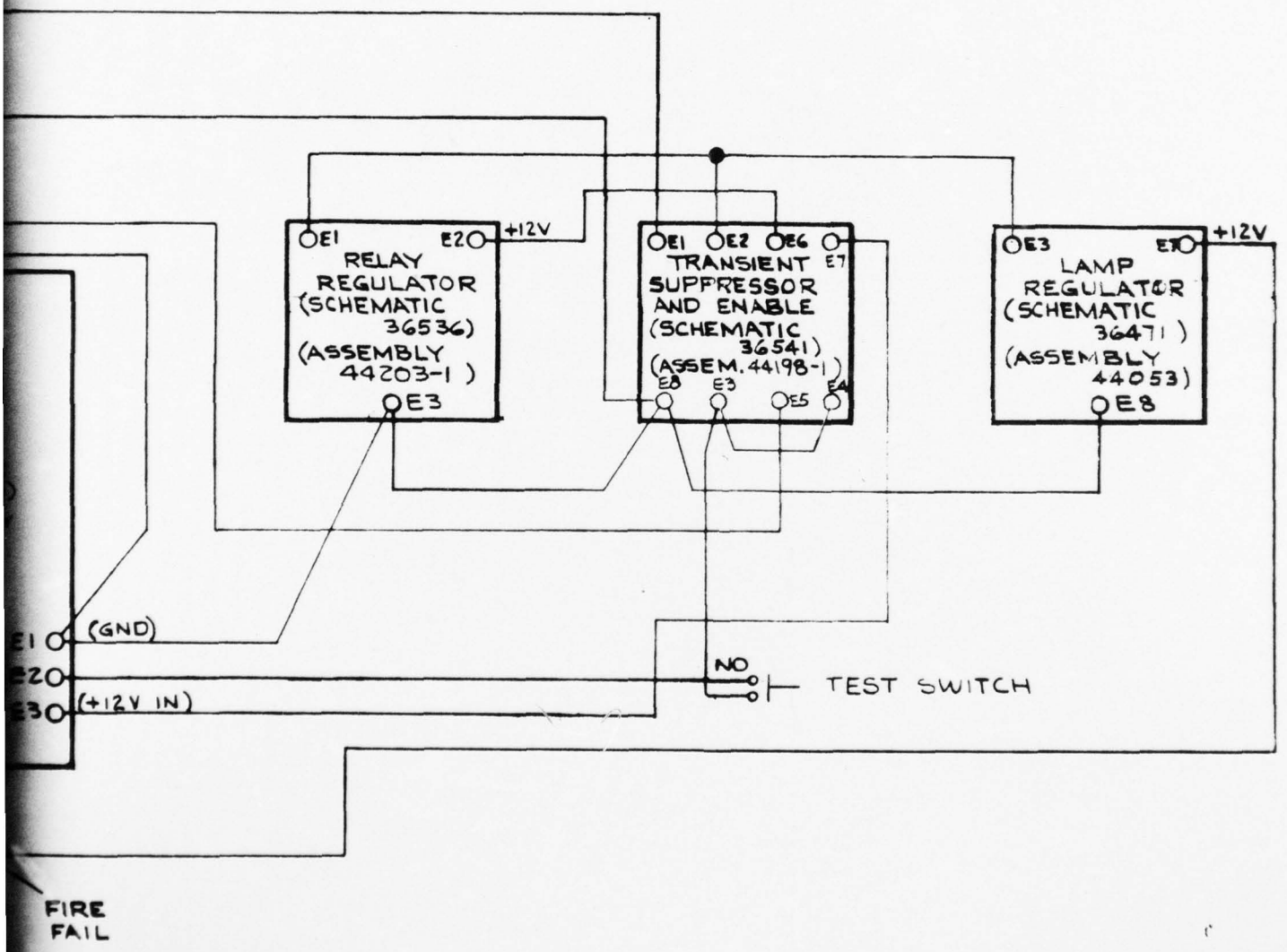


Figure 29. CRU Interconnectio



CRU Interconnection Diagram

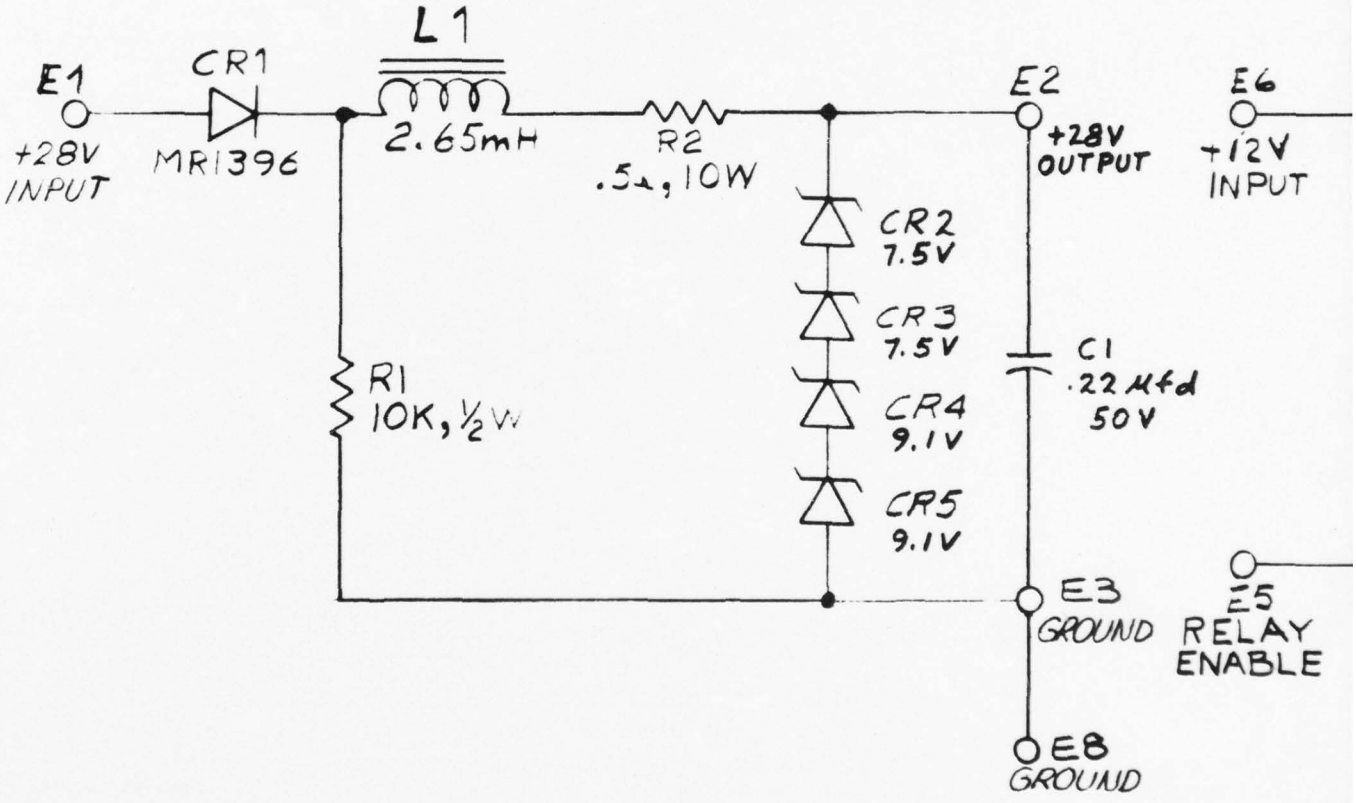
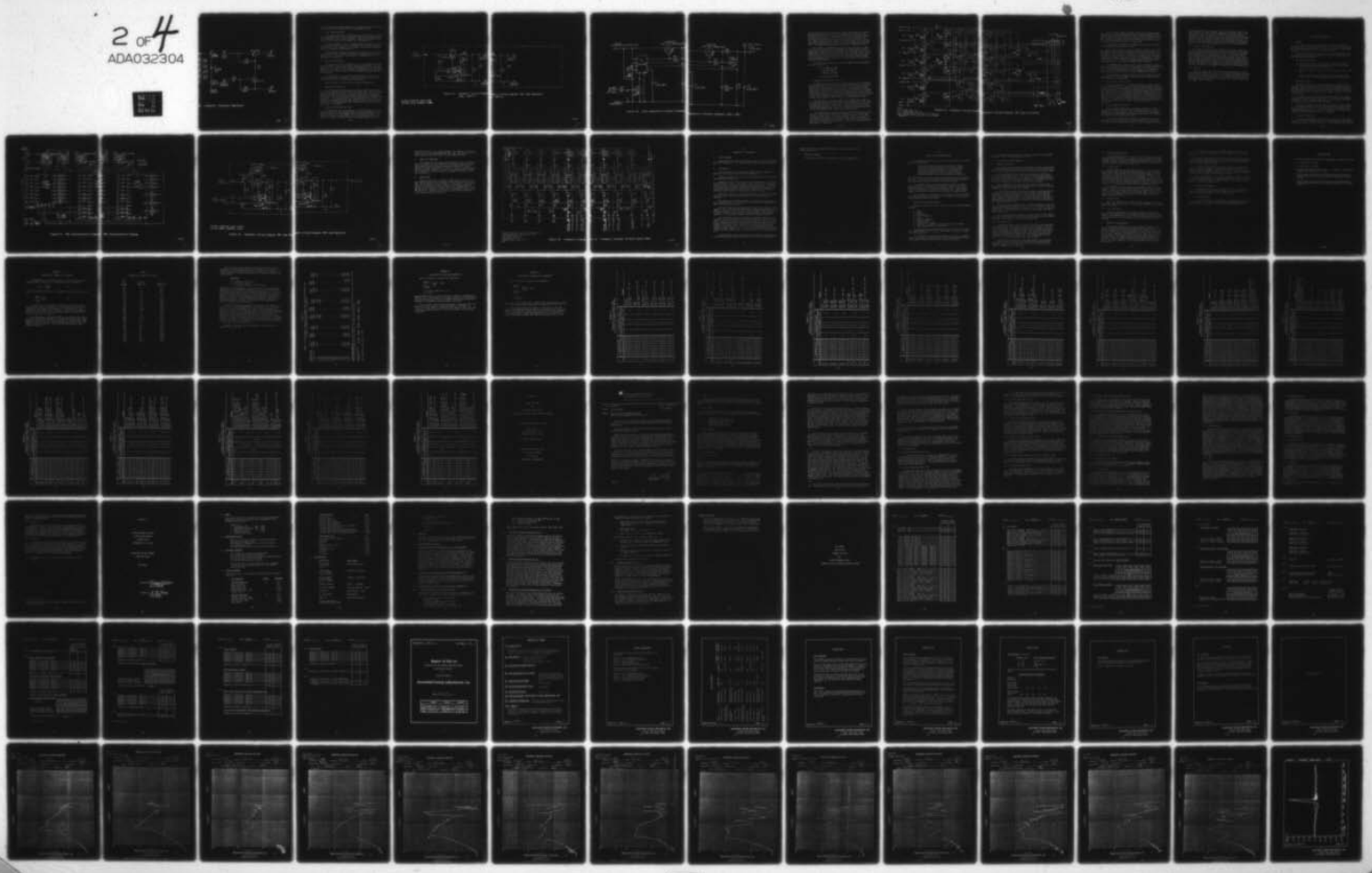


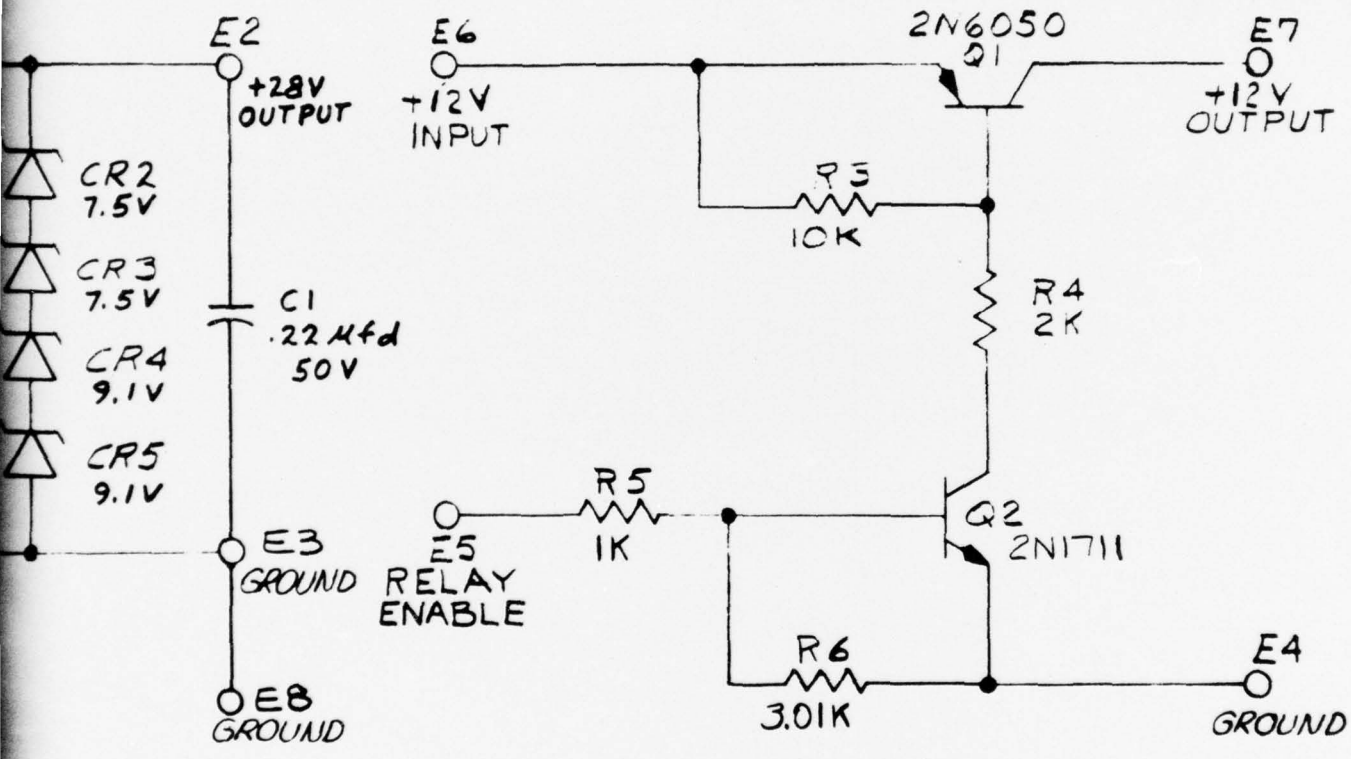
Figure 30. Schematic, Transient

AD-A032 304 MCGRAW-EDISON CO MANCHESTER N H EDISON ELECTRONICS DIV F/G 1/4
INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM.(U)
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UNCLASSIFIED AFAPL-TR-76-64 NL

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30. Schematic, Transient Suppressor

of relay power so that random signals in the computer due to power start-up, are prevented from generating false warnings in the CRU.

2.3 Lamp Voltage Regulator

This regulator, powered by transient and reverse voltage protected 28 DCV provides 12 DCV to the crew readout lamps. The regulator consists of an integrated circuit linear regulator, a current-limit-sensing transistor Q2, and a series load transistor Q1. (See Figure 31.)

The load voltage of 12 DCV is established by the junction of reference resistors R1 and R2 which are connected across reference terminal 9 of integrated circuit regulator U1 and common. The set point voltage is applied to reference sense terminal 8.

Output voltage is sensed at terminal 5 of U1 which in turn controls the conduction of Q1. Resistor R4 provides a voltage analog of load current which is monitored by transistor Q2. See reference (6) for further details of operation.

2.5 Relay Voltage Regulator

This circuitry is shown in Figure 32. It is a standard, well-known linear regulator circuit, using an NPN series pass-transistor. The integrated circuit U1 provides the voltage reference and the error amplifier necessary for operation. Output voltage is determined in part by resistors R4 and R5, and R4 can be adjusted to set the output voltage to the exact value required.

The transistor Q2, in conjunction with R2 and U1 sets a current limit of very roughly 1.5 amperes. Transistor Q1 is the result of an earlier design and is no longer used in this circuit.

Further details of operation can be found in reference (6).

3. READOUT LOGIC CIRCUITRY

All visible warning displays are actuated by transistor-amplifier-driven relay contacts (refer to Figure 33). Here, use is made of latching and non-latching relays in order to provide proper control of warning readout by signals provided by the Computer Control Unit and Maintenance Warning Unit. The use of transistor buffer-type amplifiers minimizes the constraints to be encountered in logic network signal circuit design. In addition, the attenuating effects that long runs (100 feet between Computer Control Unit and Crew Readout Unit) might have on directly operated lamp relays is eliminated.

3.1 Overheat and Overheat Fail Logic

As discussed in the work statement, the overheat signals from the Computer Control Unit when properly combined in the Crew Readout Unit will cause the operation of the OVERHEAT lamp in the Crew Readout Unit. An additional overheat warning, initiated by the Crew Readout Unit, is provided at an electrical connector pin at the Computer Control Unit for

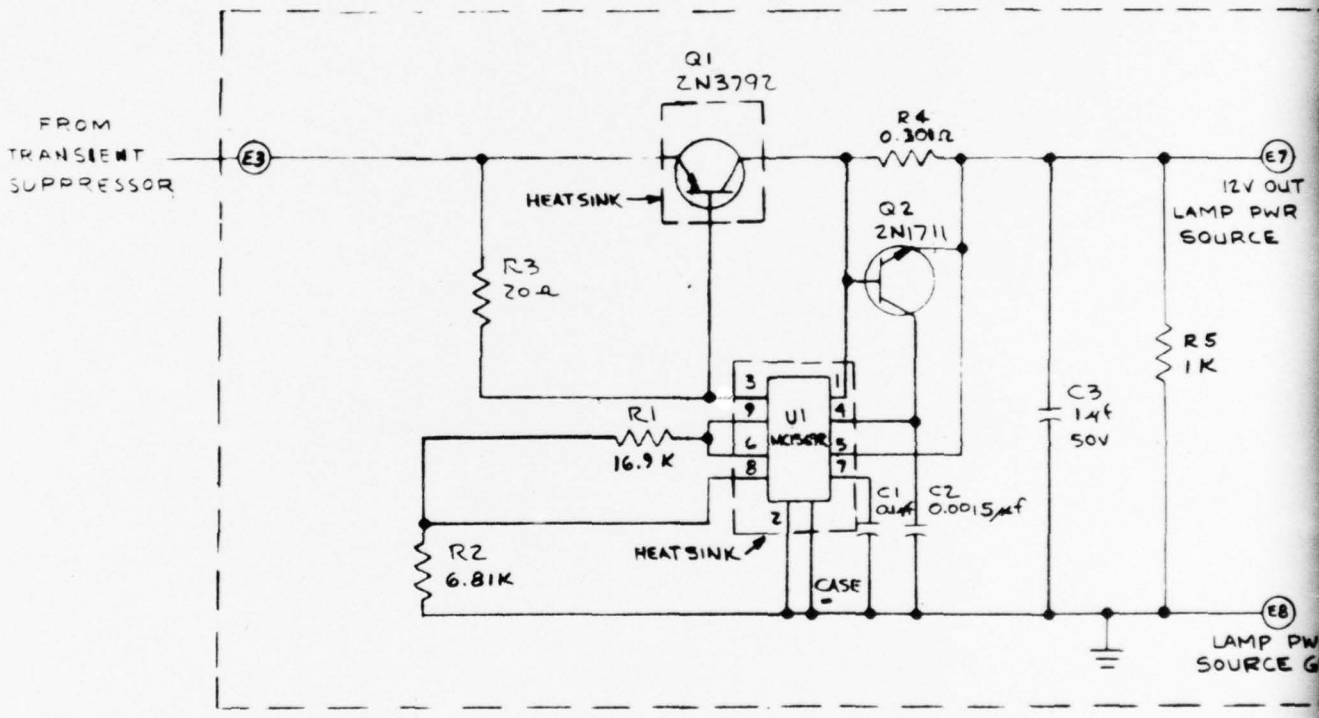
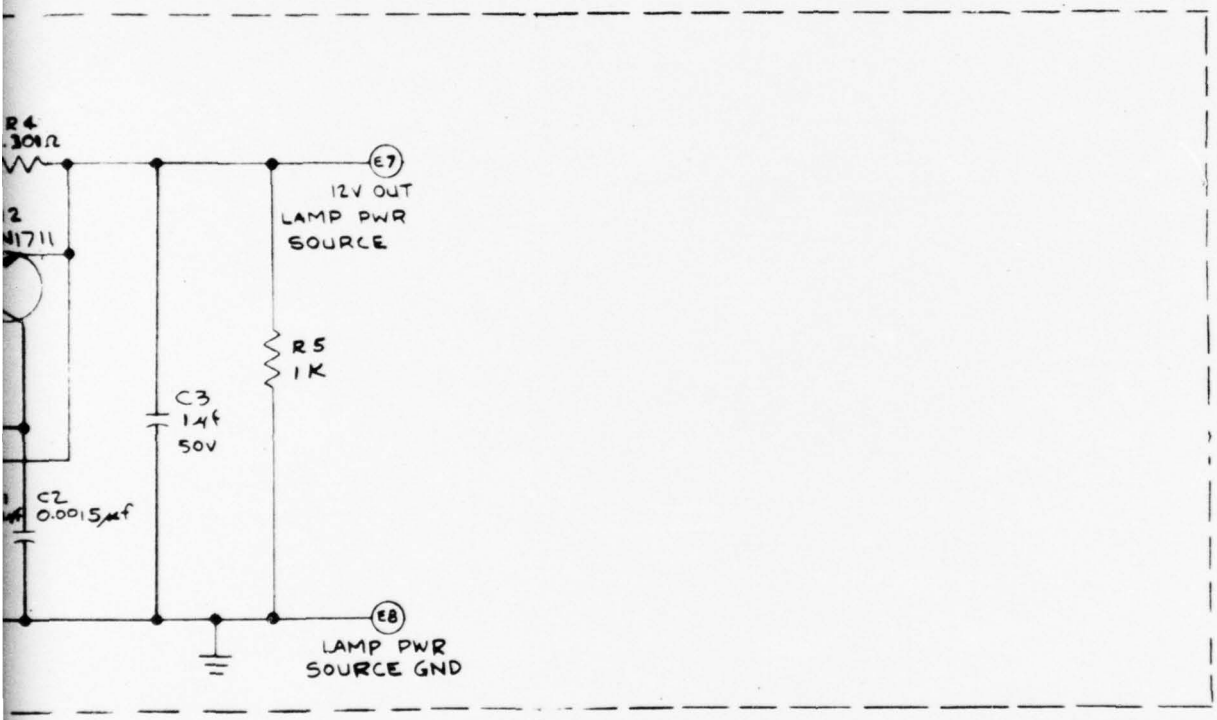


Figure 31. Schematic Wiring Diagra
(Dwg. #36471)

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matic Wiring Diagram, CRU Lamp Regulator
. #36471)

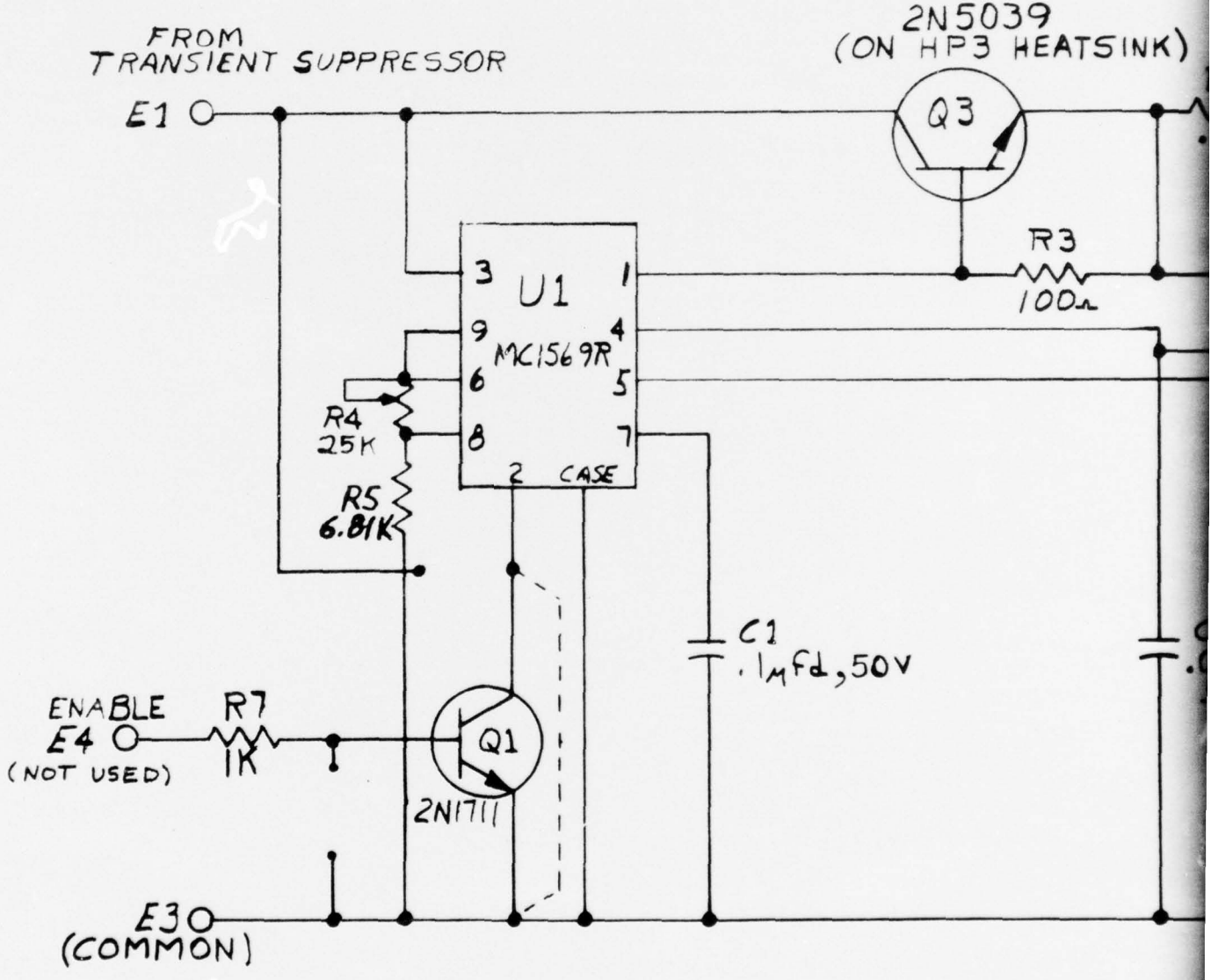
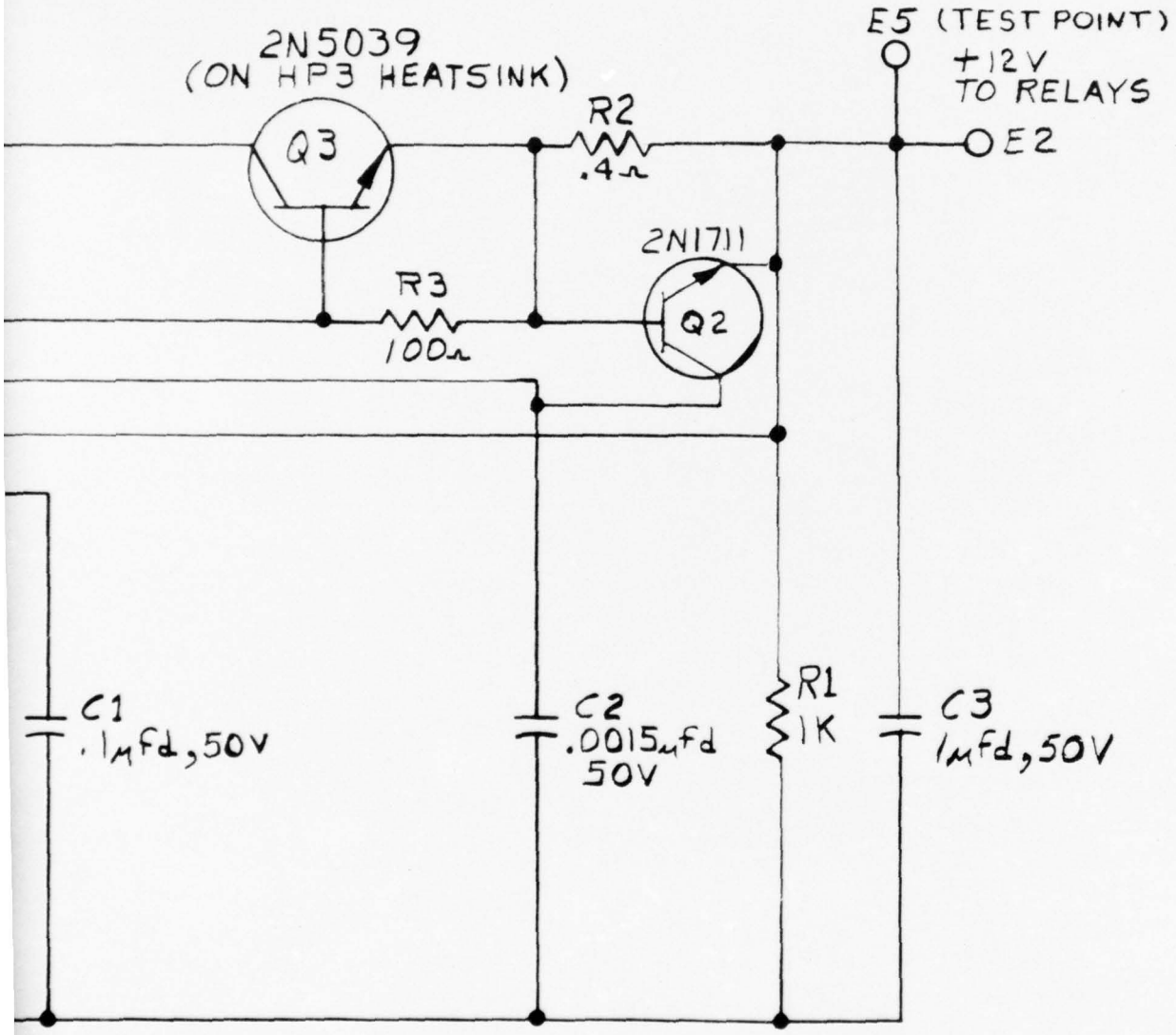


Figure 32. Relay Regulator & Disable Schemati



egulator & Disable Schematic (CRU & MWU)

possible system evaluation monitoring. Once initiated and until cleared, the OVERHEAT warning will lock out the OVERHEAT FAIL warning, and the CABLE FAIL warning of the corresponding cables which are sensing overheat. In addition, the Computer Control Unit shall give fail signals to the Crew Readout Unit when cables and/or their associated electronics test fail. These signals will be combined in the Crew Readout Unit to provide an OVERHEAT FAIL warning shall remain on until the system is checked and reset. The OVERHEAT FAIL warning shall override the OVERHEAT warning.

The OVERHEAT and OVERHEAT FAIL functions described above are implemented by the employment of four latching-relay memory channels and two output relays. Here, OVERHEAT and OVERHEAT FAIL conditions are initially diagnosed and memorized on a per-loop basis (four latching relays, two for OHA and OHFA and two for OHB and OHFB) and then, when appropriate conditions in both loop-channel sections occur, displayed as system OVERHEAT and system OVERHEAT FAIL conditions (OH, or OHF, respectively provided by the non-latching relays).

The final logical equations for system OVERHEAT and system OVERHEAT FAIL are as follows:

$$OH = OHA\ \overline{OHFA}\ OHB\ \overline{OHFB}$$
$$+\ OHA\ \overline{OHFA}\ \overline{OHB}\ OHFB$$
$$+\ \overline{OHA}\ OHFA\ OHB\ \overline{OHFB}$$

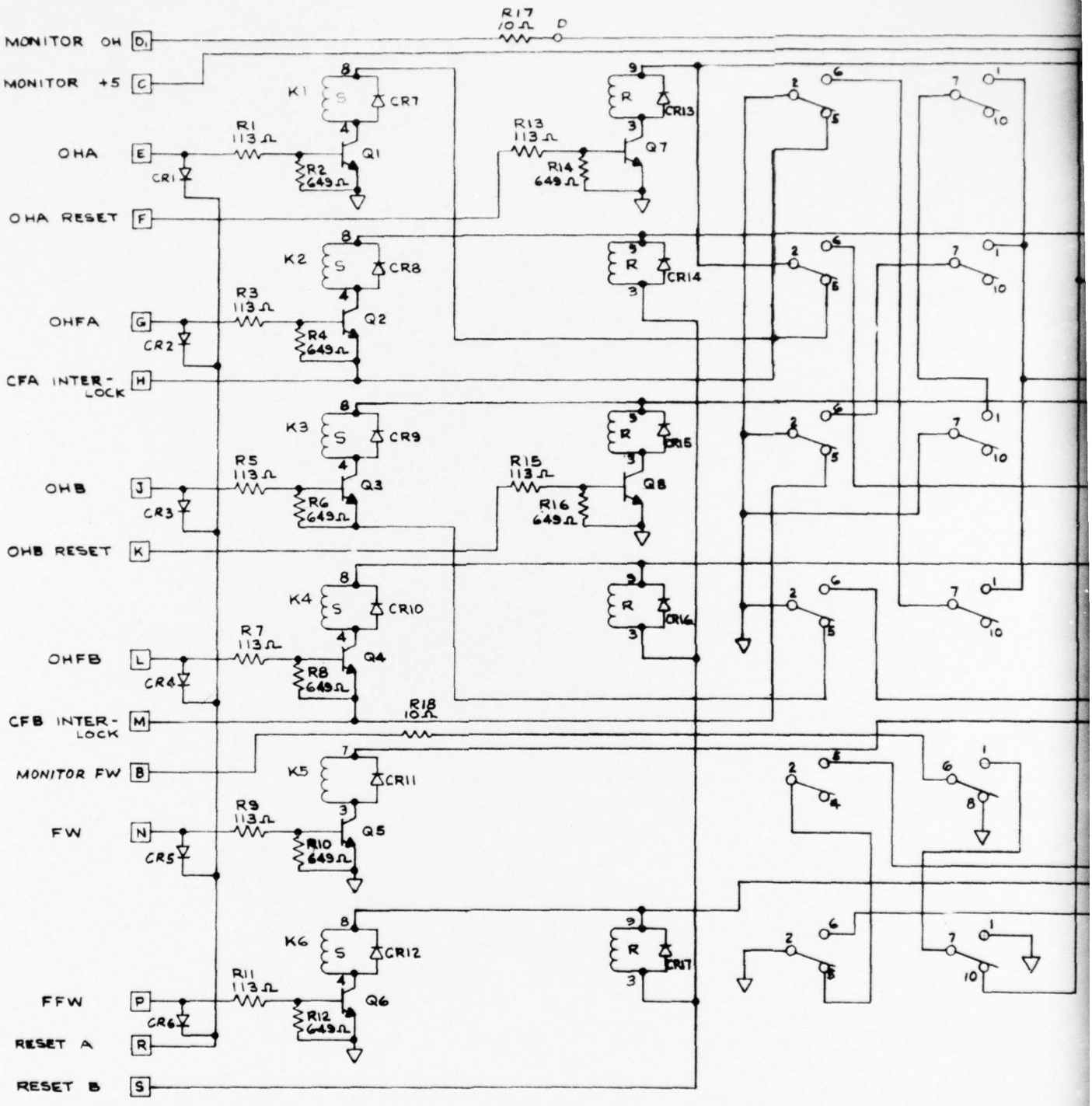
$$OHF = OHFA\ \overline{OHA}\ OHFB\ \overline{OHB}$$

3.2 Overheat and Overheat Fail Circuitry

In Figure 33, it can be seen that per-channel signals for OVERHEAT, OHA and OHB, derived from the per-loop output circuits A and B in the Computer Control Unit, are applied to the inputs of transistor Q1 and Q3, respectively, which activate the set coils of latching relays K1 and K3, respectively. For return to normal conditions per channel, reset signals from output circuit A and B are applied to transistors Q7 and Q8, respectively, which activate the reset-coils of latching relays K1 and K3, respectively. Here, warning and reset signals for this operation are so controlled by the Computer Control Unit as to be nonconcurrent in time.

In like fashion, per-channel signals for OVERHEAT FAIL, OHFA and OHFB, derived from the signal correlator circuit are applied to the inputs of transistors Q2 and Q4, respectively, which activate the set coils of latching relays K2 and K4, respectively. Here, the relays can be reset only by pressing the common reset button located in the Maintenance Warning Unit when OVERHEAT FAIL signals are no longer present.

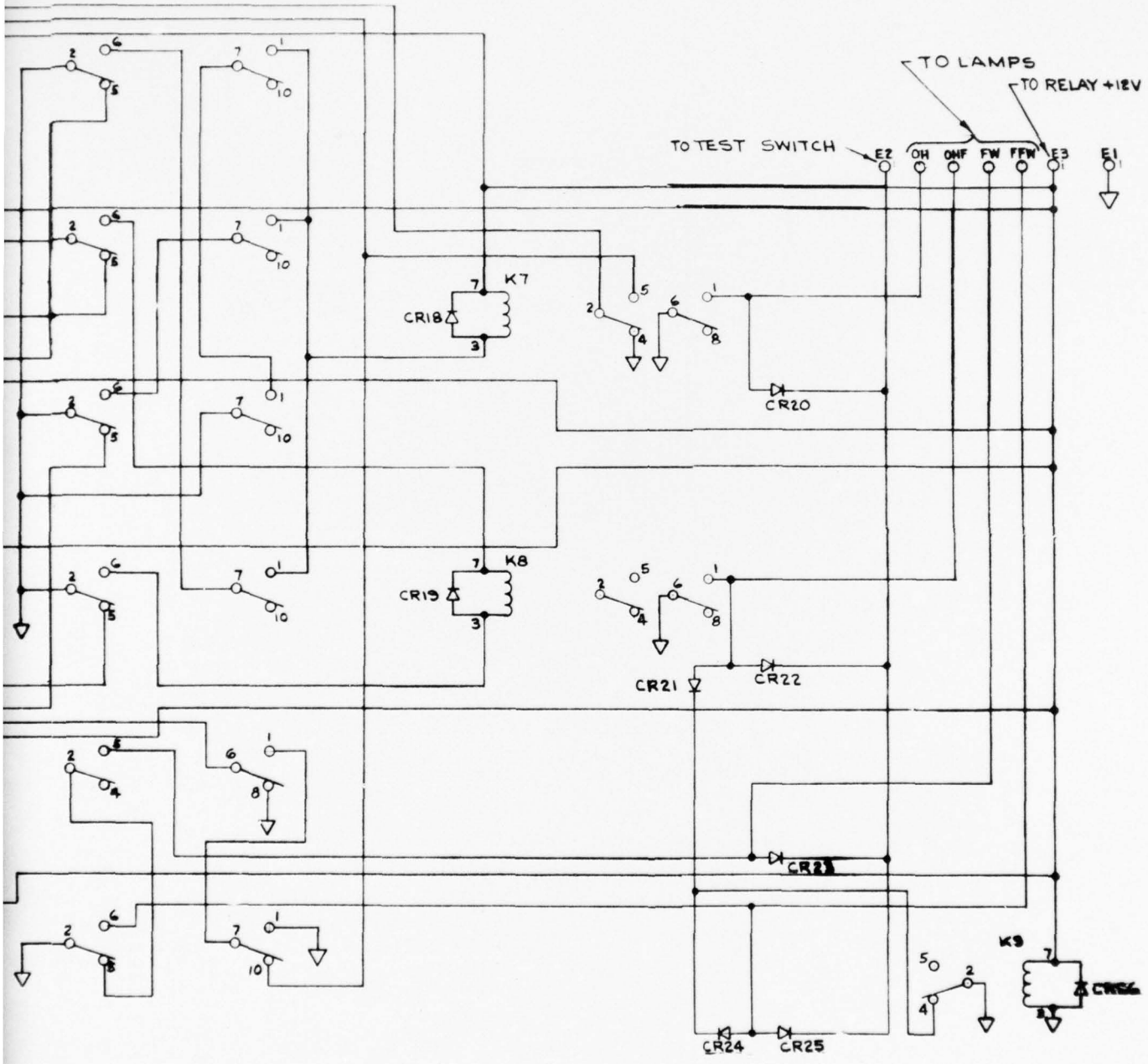
The occurrence of an overheat condition in channel A results in the removal of reset signal voltage and the application of overheat signal voltage to transistor Q1. This causes latching relay K1 to be set and relay contacts K1-2 and K1-7 to be transferred. Here, the transfer of K1-2 locks out both OHFA set transistor Q2 and the CFA set transistor located in the Maintenance Warning Unit. Contacts K1-7 provide the OVERHEAT channel A closure OHA.



NOTES:

1. ALL DIODES ARE IN3611
2. ALL TRANSISTORS ARE 2N1711
3. ALL LATCHING RELAYS ARE SHOWN IN RESET POSITION.
4. NON-LATCHING RELAYS ARE SHOWN IN NON-ENERGIZED POSITION.

Figure 33. Schematic Wiring Diagra



chematic Wiring Diagram, CRU Logic Circuitry

If an A channel OVERHEAT FAIL (HFA) should have occurred instead, however, the fail signal OHFA provided by the signal correlator would have activated transistor Q2 which, in turn, would have energized the set coil of OHFA relay K2 and caused the transfer of relay contact K2-2 and K2-7. Here, the transfer of K2-2 locks out OHA set transistor Q1, and provides the OVERHEAT FAIL channel A closure OHFA.

The generation of OVERHEAT or OVERHEAT FAIL latchings for channel B are accomplished in identical fashion.

Should conditions occur in both loop-channel systems A and B as to generate any of the optional combinations shown in the equation for system OVERHEAT (OH) discussed in paragraph 3.1, output relay K7 will be actuated. In turn, contact K7-2 transfers and provides the 5 DCV signal for the system evaluation monitoring circuit. Relay contact K7-6 also transfers and provides energizing voltage to the OVERHEAT lamp, causing a visible OH display. Termination of the OVERHEAT condition in either loop-channel A or B will cause the OVERHEAT lamp to turn off.

When OVERHEAT FAIL conditions occur in both loop-channel systems A and B so as to generate the terms in the equation for system OVERHEAT FAIL (OH) as discussed in paragraph 3.1, output relay K8 will be actuated. Here, contact K8-6 transfers and provides voltage to the OVERHEAT FAIL lamp, causing a visible display of a system OVERHEAT FAIL condition.

As with OVERHEAT, a return to normal in either channel loop system will eventually allow the OVERHEAT FAIL light to go off when the reset button in the MWU is depressed.

3.3 FIRE and FIRE FAIL Output Logic

As discussed previously, the FIRE and FIRE FAIL signals produced by the Computer Control Unit operate red and white warning lights, respectively. Once activated, the FIRE FAIL warning remains on until the system is checked and reset. The FIRE FAIL warning shall override the FIRE warning. These functions are implemented in the Crew Readout Unit by the employment of a non-latching relay for FIRE and a latching relay for FIRE FAIL. The signal for a system FIRE condition, FW, is obtained from the FIRE FAIL and U/V computer diagnostic circuitry (refer to Figure 13 and Section 1.4 of Chapter IV). The FIRE FAIL warning signal is obtained from the signal correlator circuit (refer to Figure 18 and Section 2.4 of Chapter IV).

3.4 FIRE and FIRE FAIL Circuitry

The FIRE signal generated in the computer diagnostic circuitry is applied to the input circuit of buffer-transistor Q5 which, in turn, actuates non-latching relay K5. Here, the contacts on K5 now transfer and energize the FIRE WARNING light and also provide the 5 DCV signal for the system evaluation monitoring circuit.

Should, on the other hand, a FIRE FAIL condition occur, the Computer Control Unit applies FIRE FAIL warning signal FFW to the input circuitry of buffer transistor Q6, which, in turn, actuates the set coil

of latching relay K6. As a result, contact K6-2 transfers and cuts out power access to the FIRE light and energizes the FIRE FAIL light. Also, contact K6-7 transfers and removes 5 DCV from the system evaluation monitoring circuit. A return to normal (no faults) condition will cause the removal of the FIRE FAIL warning signal and permits turn-off of the FIRE FAIL light when the reset button in the Maintenance Warning Unit is pressed. Here, the pressing of the reset button results in a momentary closure of the circuit which energizes reset coil of latching relay K6.

3.5 CCU Power Fail Indication

In order to provide a positive indication of failure of power to the CCU, a relay K9 was added to the CRU logic circuitry. During normal standby operation, K9 is energized by the 12 DCV relay power, and there is no electrical path between contacts 2 and 4. If CCU power should fail, the Relay Enable signal will become ZERO, and the circuitry discussed in Section 2.2 will remove the 12 DCV relay power. Relay K9 will then no longer be energized, contacts 2 and 4 will be connected, and the FIRE FAIL and OVERHEAT FAIL lamps will be energized through diodes CR21 and CR24. Relay K9 is not a latching relay, and so when power returns to the CCU, the FIRE FAIL and OVERHEAT FAIL lamps will go off automatically.

3.6 Lamp Test

Isolation diodes CR20, CR22, CR23 and CR25 are employed to allow testing of crew readout lamps. Here, in the forward direction, the diodes provide a path for lamp current flow to the common test switch which bypasses the associated relay contacts. The reverse blocking character of the diodes, however, prevents the inadvertent turn-on of all lights when any single relay is activated.

VI.

MAINTENANCE WARNING UNIT

1. APPROACH

It is the purpose of the MWU to provide a positive indication of defective sensors or electronic components. To this end, the front panel has fifteen illuminated indicators. A lamp test switch and a lamp dimmer control are also provided, as is a system reset switch.

All indications are of the "latching" type--once they appear, they will remain until intentionally removed. In this way, intermittent defects can be readily signaled.

The fifteen indicators are:

a. UV11, UV12 ... UV62. These indicate a defective U/V sensor tube, the first number indicating the head, the second number indicating which tube within the head.

b. CCU--This indicates a failure in the electronic circuitry of the CCU.

c. Cable A, Cable B--These indicate either an open circuit or a short circuit in the corresponding thermistor overheat cable.

2. MWU POWER SUPPLIES

As shown in Figure 34, 28 DCV input power first passes through a transient and reverse-voltage protection network and then goes to two 12 DCV power supplies. One supply is for powering the indicator lamps, while the other supplies power to the relay coils and the transistor drivers. The output from the "Relay Regulator" power supply is gated by the "Relay Enable" network.

The transient and reverse-voltage protection circuitry, the relay enable circuitry, and the relay power supply of the MWU are all identical to those of the CRU. Schematic diagrams are found in Figures 30 and 32. Descriptions of operation are found in Section V.

A schematic diagram of the MWU lamp power supply is found in Figure 35. This unit is very similar to the CRU lamp power supply whose operation is described in 2.3 of V. In the MWU supply, two transistors are used in parallel for the pass transistor, and one of the voltage-setting resistors is made variable to serve as a lamp dimmer.

3. UV AND CCU INDICATORS

Circuitry for these indicators is shown in Figure 36. This circuitry consists of thirteen identical channels. In each channel, a ONE signal from the CCU turns on a 2N1711 transistor. Current through this transistor

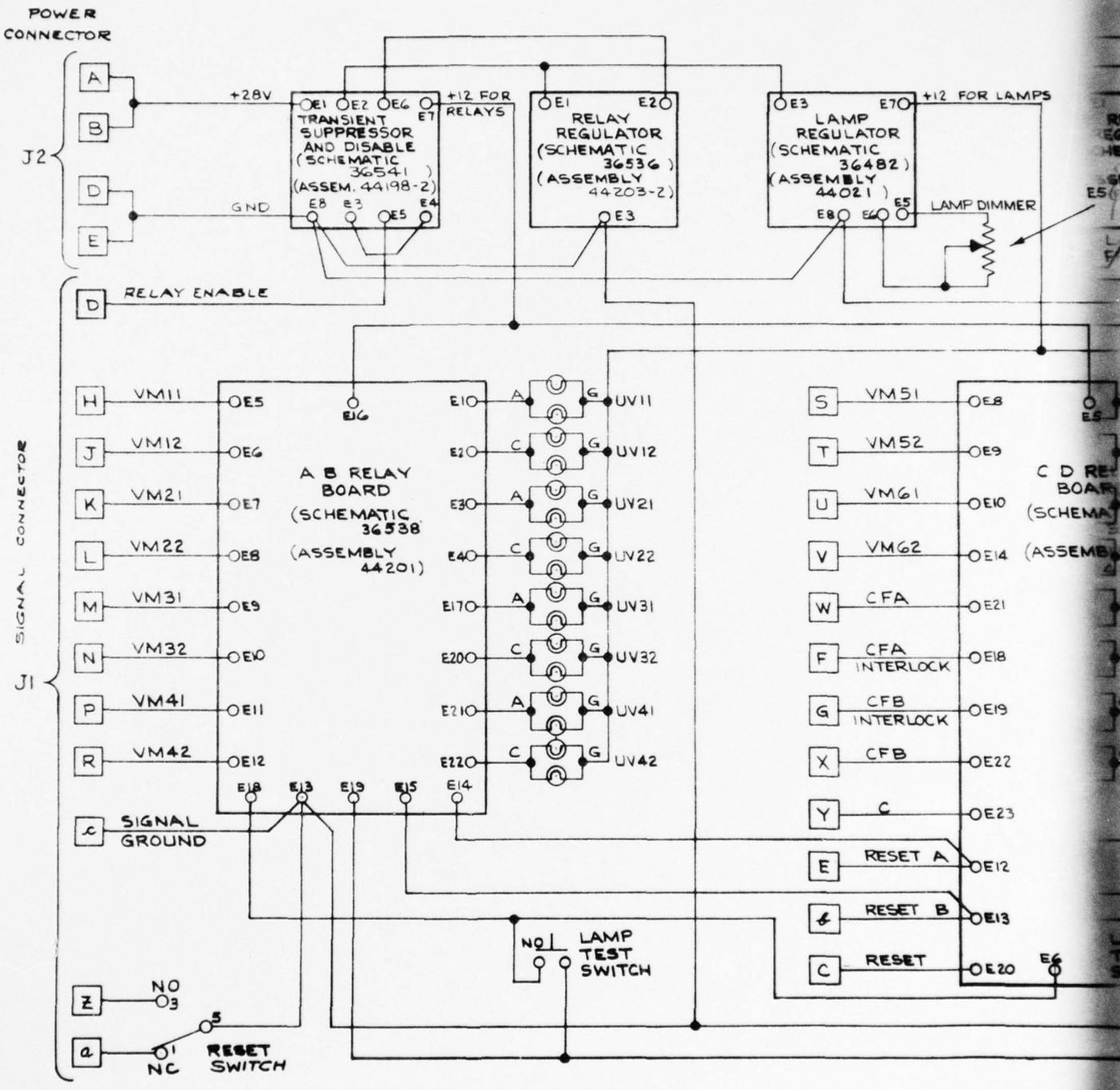
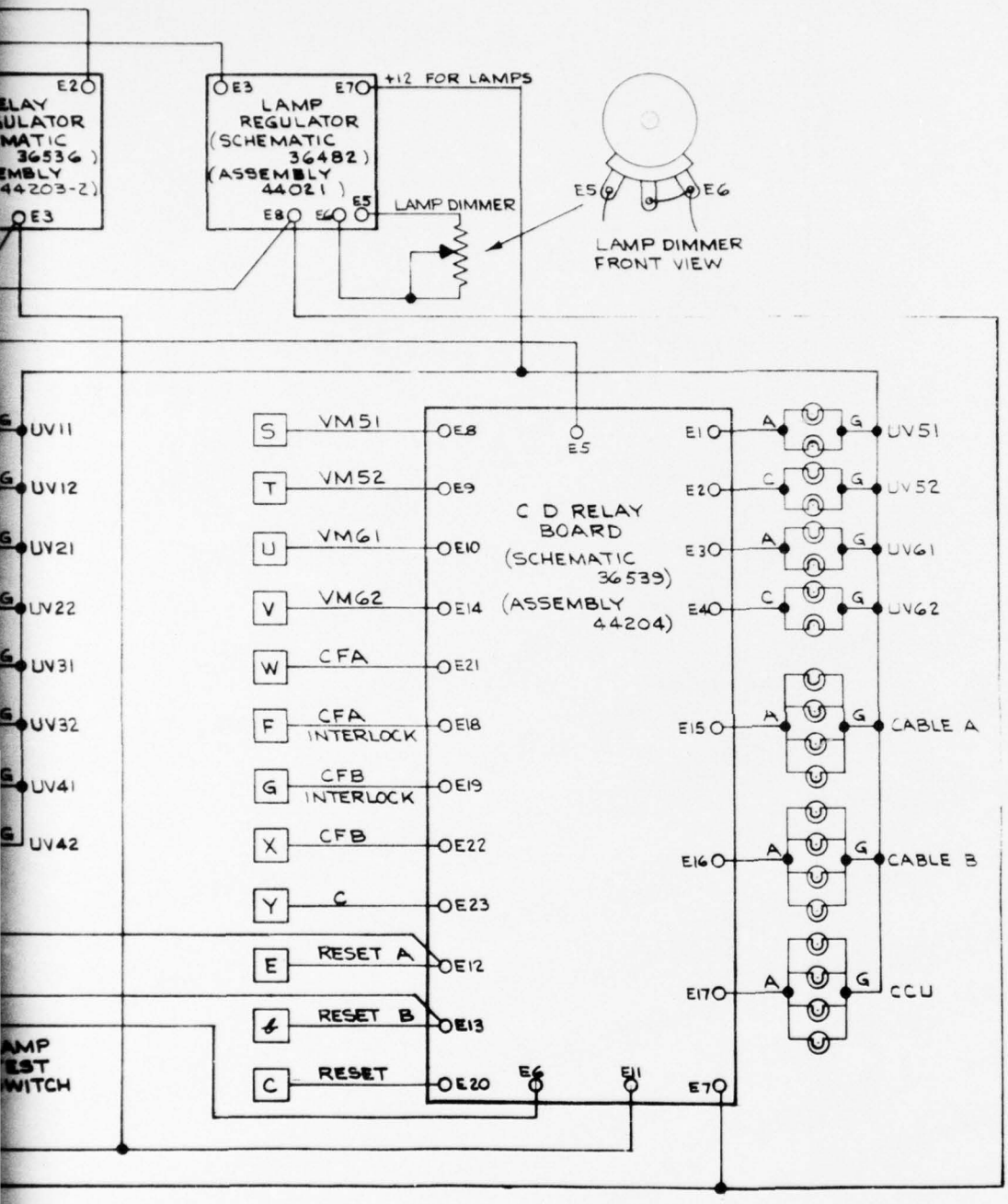
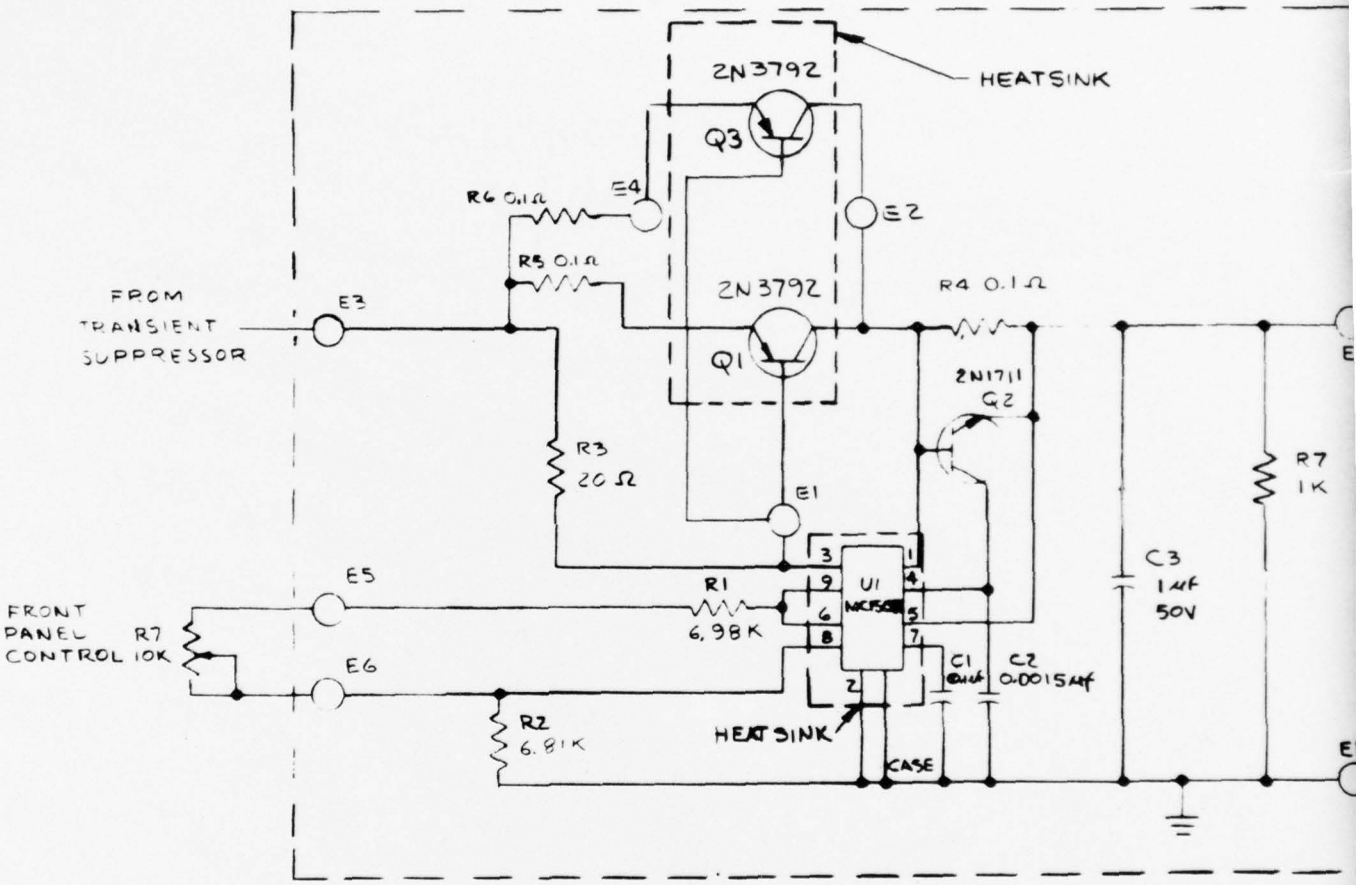


Figure 34. MWU Interconnection Diagram

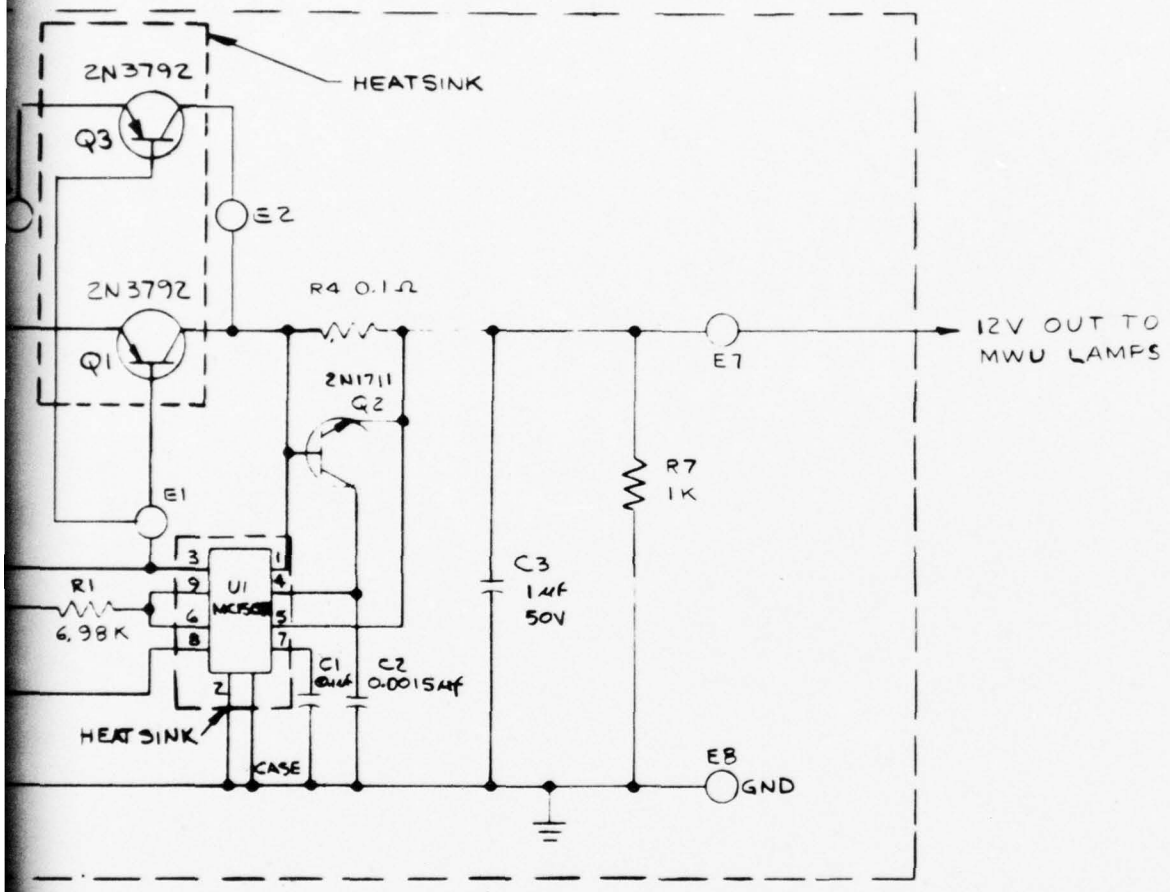


MWU Interconnection Diagram



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Figure 35. Schematic Wiring Diagram, MWU Lamp R



matic Wiring Diagram, MWU Lamp Regulator

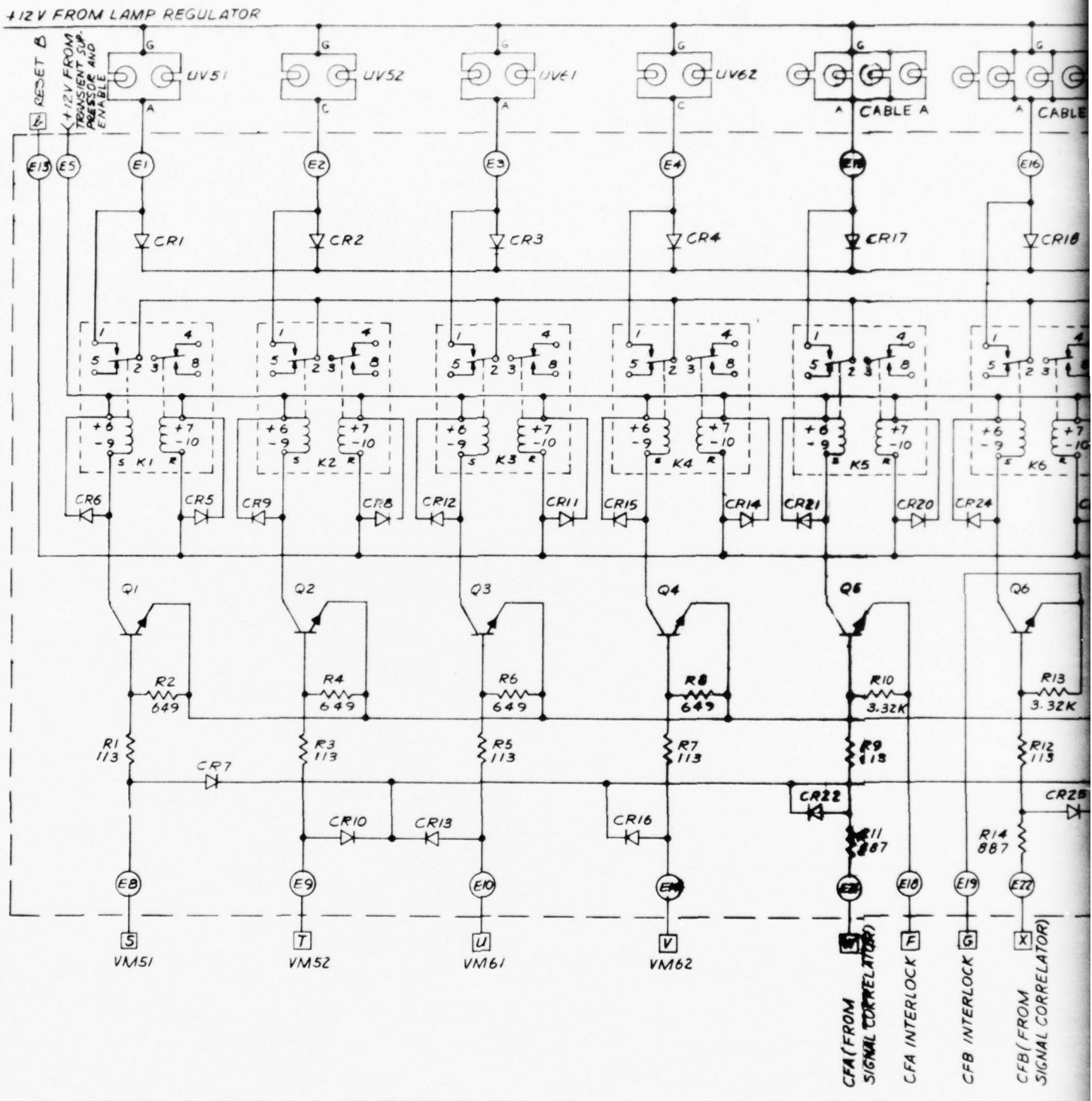
activates the set coil of a latching relay. The contacts of the relay supply power to the corresponding indicator lamp. The relay can be reset only by pressing the reset button, by action described below.

4. CABLE FAIL INDICATORS

The circuitry for the cable fail indicators is shown in Figure 36. These two channels are very similar to the thirteen channels described above, except that the transistor emitters are returned to common ("ground") through relay contacts in the CRU. Thus, if an overheat condition is present on channel A, cable fail A indicator cannot be turned on. Similarly, an overheat condition on channel B inhibits the cable fail B indicator.

5. MANUAL RESET

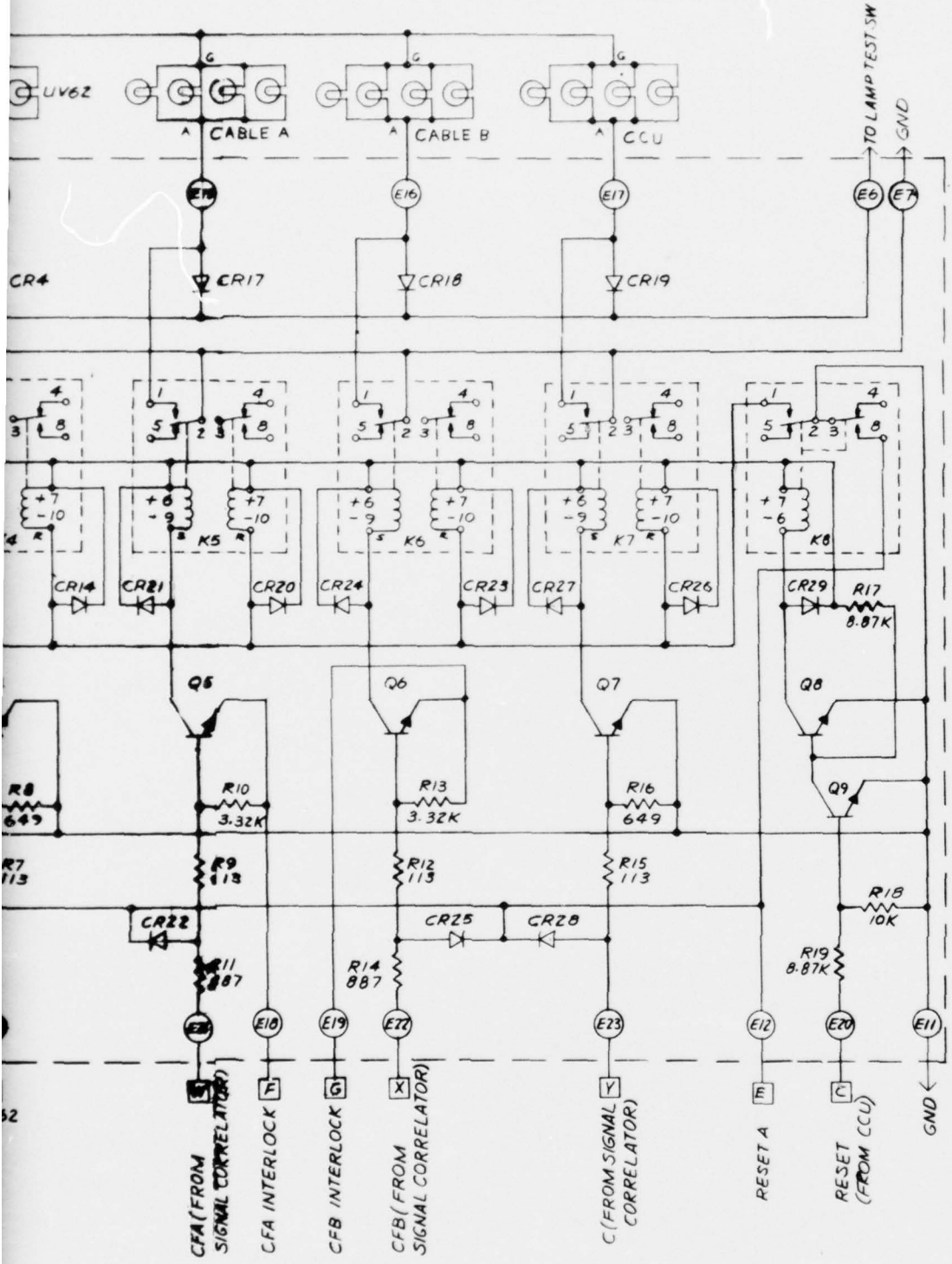
When the reset button is pressed, a ONE is sent back to the CCU. After debouncing and other processing, a ONE signal is sent back to the MWU. This is applied to E20 in Figure 36. This signal is amplified by transistors Q8 and Q9, and then activates a non-latching relay, K8. Contact 1 of K8 energizes all reset coils of the latching relays of the MWU and the CRU. Contact 8 of K8 shorts all transistor inputs (of both MWU and CRU) to common to present the set coils from being energized at the same time the reset coils are.



5. NON-LATCHING RELAY IS SHOWN IN UNENERGIZED POSITION.
4. LATCHING RELAYS ARE SHOWN IN RESET POSITION.
3. ALL TRANSISTORS ARE 2N[illegible]
2. ALL DIODES ARE IN3611.
1. ALL RESISTOR VALUES ARE IN OHMS UNLESS OTHERWISE SPECIFIED:

NOTES

Figure 36. Schematic Diagram



re 36. Schematic Diagram, CD Relay Board (MWU)

VII.

EXAMINATION OF PERFORMANCE

1. TESTS PERFORMED

In accordance with contract requirements, the first IFOS constructed was tested extensively. The complete test procedure is given in Appendix V.

2. TEST RESULTS

The test report of the McGraw-Edison Quality Control engineer, together with test data sheets, is given in Appendix VI.

Generally speaking, all of the tests were passed by the IFOS, excepting vibrational and EMI tests.

Mechanical failures under vibration necessitated the use of external shock absorbers in order to continue the tests. This was not a very satisfactory solution as it makes front-panel mounting impossible. According to a McGraw-Edison mechanical engineer who examined the test results, the vibrational failure problems could easily be overcome in the design of a production model, without the use of external shock absorbers.

During EMI testing, no conducted or radiated susceptibility problems were encountered, but excessive conducted and radiated emission was observed.

This undesired interference appears to originate in these places: the "lamp regulators" of the MWU and CRU, and the switching regulators and power inverter circuit of the CCU.

The lamp regulators cause interference because they oscillate. These regulators are of the negative-feedback linear type, and oscillations are readily eliminated by minor circuit changes. (Possible changes include different component values, different component lay-out, and additional capacitors.) All remaining problems would then originate in the CCU.

Now oscillations cannot be eliminated in switching regulators or in inverters, since these circuits work only because they do oscillate. However, by better filtering of the power leads to the CCU, the a.c. energy causing interference could be prevented from leaving the metal box by conduction. (The present filters are of the "L" type, oriented to prevent energy from entering the box. Further, the power "return" lead is unfiltered. Large filters of the "π" type on all power leads would prevent energy from being conducted out of the metal box as well as from entering it.)

Suppressing the energy leaving the box by conduction, together with an improved grounding system, would probably also eliminate interference

leaving the system by radiation, although one cannot be certain of this without actual trials.

3. RELIABILITY ANALYSIS

A theoretical study of IFOS reliability is given in Appendix VII.

VIII.

CONCLUSIONS AND RECOMMENDATIONS

The Statement of Work, which is a part of the contract for the IFOS project, indicates that:

> The objective of this program is to develop a flight qualifiable Integrated System with a potential application for the engine compartments of an advanced multi-engine bomber/transport aircraft. This system will distinguish between a fire and an overheat condition and provide highly reliable hazard detection capability.

This objective was met by the three systems delivered to the Air Force in June, 1976. These systems demonstrate that high reliability, automatic fire and overheat detection systems are definitely feasible.

It is evident from the test results given in Chapter VII that a number of defects are present in the mechanical design. These defects necessitated the use of external shock absorbers, which in turn, made front-panel mounting of the MWU and the CRU impossible. These defects, however, could easily be overcome in the design of a production model.

In the course of carrying out the IFOS project, several other areas of possible improvement became apparent. The remainder of this chapter lists and details such possibilities.

I. IMPORTANT SYSTEM CHARACTERISTICS

Important characteristics for a system for fire and overheat warning include:

A. Size
B. Weight
C. Reliability
D. Power consumption
E. Cost
F. Physical ruggedness
G. Response speed
H. Sensitivity (to flame)
I. Stability of parameters (alarm temperature for overheat)
J. Ease, speed and cost of maintenance

Various degrees of improvement seem readily possible for the first five characteristics and for the last one listed. More specific suggestions are given below.

It is assumed that the complete system will consist of a Computer Control Unit (CCU), a Crew Readout Unit (CRU), a Maintenance Warning Unit (MWU), Detector Heads, Overheat Cables and connecting cables.

The contract goals referred to in the discussion are "System Weight and Volume Goals" of Contract F33615-72-C-1053.

2. SIZE, WEIGHT & POWER CONSUMPTION

2.1 Computer Control Unit

Most of the volume and weight of the present CCU stems from the logic cards, their sockets, housing and associated wiring, and from the various circuits used to supply power to the logic circuits and the detector heads.

The size and weight of the logic circuitry could be reduced by a factor of at least two or three by the use of a different logic design or by the use of a microprocessor. With the aid of a custom-made LSI chip, all of the logic could be placed on a single 4" x 5" printed-circuit card, but such a chip would be very expensive to design and produce.

Power consumption of the logic circuitry could be reduced by the same measures that reduce size and weight and also by the use of CMOS logic elements to replace the present TTL elements.

At least half of the input power to the present system goes into the operation of the sensor tubes in the detector heads. By placing small transformers in the detector heads, it should be possible to make the stand-by power consumption smaller. With a current-limiting circuit, the power consumption could be kept low even under intense fire conditions. Reduced power consumption would lead to smaller and lighter power supplies with reduced heat dissipation.

With the changes suggested above, the overall dimensions of the CCU might be reduced from the present 7-1/2" x 12" x 19" to about 5" x 6" x 12". Stand-by power consumption might be reduced to 5 or 10 watts from the present 28 watts. It is difficult to see how the contract goal of 24 cubic inches could be met.

It is anticipated that the weight reduction would be in the range of 50 to 75% of the present CCU weight of 30#, 13 oz. and a follow-on program CCU weight design objective of 8# could be established.

2.2 Crew Readout Unit

Presently, the CRU is about 5-1/2" x 5-1/2" x 8" in size and weighs about 4-1/4 pounds. There are four internal circuit boards. By the use of 24V relays, the "Relay Regulator" board could be eliminated. An improved "Lamp Regulator" would be somewhat smaller and would eliminate the need for the "Transient Suppressor" board. The circuitry of the "Logic" board could be simplified somewhat and could be placed among the four indicators, just behind the front panel. The resulting unit would be about 4" x 4" x 4" and would weight less than 2 pounds.

Because of the current and voltage requirements of the presently-used indicator lamps, it would not be possible to eliminate the "lamp regulator" board. The contract goal of 12 cubic inches would seem to require a different type of indicator.

2.3 Maintenance Warning Unit

The present MWU is about 6" x 6-1/4" x 9-1/2" in size, and weighs approximately 6-3/4 pounds. If a different type of indicator were used, a dramatic reduction in size and weight would be possible. By the use of latching flag-type indicators, it should be possible to easily meet the contract goals of 12 cubic inches and .8 lb.

2.4 Detector Heads

Present flame detector heads measure about 4" x 3" x 3" and weigh about 2 pounds each. By the use of miniature sensor tubes (now under development at McGraw-Edison) and a few minor design changes, it would be possible to reduce the size of the head somewhat. Of course, if a transformer were included in the head, as discussed in 2.1, above, this saving would be used up. Inclusion of a high-voltage transformer for the U/V sensor and a lower-voltage pulse transformer for the U/V source would allow the use of MIL-Spec qualified electrical connectors since the input voltage to the detector head could be reduced to approximately 50V.

Miniaturization of the detector head components volume and weight reductions would be offset by the inclusion of the connector and transformers. However, the combined cable and detector head weight of 10 lbs, 7 oz. would be reduced by the use of low voltage cable. It is anticipated that this weight reduction would be in the order of 50% with a design objective of 5 lbs.

2.5 Overheat Cables

There is no apparent way to reduce the size and weight of the overheat cables. They weigh a total of 1-1/2 pounds, compared to the contract goal of 1/2 pound.

2.6 Connecting Cables

By use of a transformer in the detector heads, the thick, heavy expensive high-voltage cable used at present could be replaced with much smaller, less expensive wire. Low voltage fire zone wire would result in a weight reduction of 67% resulting in a 40 foot cable length weight of 3 pounds.

3. RELIABILITY CONSIDERATIONS

In the present system, there are many individual components whose failure would lead to failure of the entire system. By the use of greater redundancy and a revised logic design, it appears to be possible to build a system which would work normally in spite of the failure of any one single component. Even indicators can be made with this feature --by having two lamps illuminating the same jewel and energized from separate circuits, a burned-out bulb will not prevent an alarm from being given. With the addition of monitoring photocells and SCR "crowbars," a defective lamp-driver circuit can be prevented from giving a false alarm.

The occasional failure of the OVERHEAT indicator to come on (see 2.3.1.1 of Section IV) could readily be overcome with a different logic design.

Reliability can further be improved by the use of more reliable components and fewer interconnections. Thus, the use of a microprocessor to replace the many separate integrated circuits of the present IFOS should lower the failure rate considerably.

To obtain the full reliability permitted by a given design would require a carefully designed and implemented reliability program, with attention to the care taken in production and quality control, the conditions and time of storage, shipment conditions, care taken in installation and human factors of users and maintenance personnel.

Careful examination of the meaning of reliability reveals that there are several possible definitions, not equivalent to each other. To proceed with a detailed design of an improved IFOS, it would be necessary to define the reliability goals exactly.

4. MAINTENANCE CONSIDERATIONS

Some improvement in the speed and ease of repair could probably be made by providing for additional fault diagnosis on the MWU, and by providing convenient test points in the CCU, MWU and CRU.

5. COST CONSIDERATIONS

At the present stage, it is impossible to estimate the cost of an improved IFOS. The use of a microprocessor to replace many digital integrated circuits would hopefully reduce both labor and material costs.

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3. U.S. Patent No. 3,213,312.

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5. Specifications and Applications Information for MC1563R Negative Voltage Regulators, Motorola Semiconductor Products, Inc., Phoenix, Arizona.

6. Specifications and Applications Information for MC1569R Positive Voltage Regulators, Motorola Semiconductors Products, Inc., Phoenix, Arizona.

APPENDIX I

CALCULATION OF PROBABILITY OF RESPONSE

The probability of obtaining N counts in a time interval where the expected number of counts is A, is given by this Poisson formula:

$$P\ (N,A) = \frac{A^N\ e^{-A}}{N!} \qquad (1)$$

It follows that the probability of obtaining N or more counts in this time is:

$$\sum_{X=N}^{X=\infty} \frac{A^X\ e^{-A}}{X!} \qquad (2)$$

For later use it is convenient to prepare a table of the values of (2) for various values time intervals. In this table, we assume a tube sensitivity of 15 counts in .480 seconds. (A time interval of .480 seconds was chosen rather than .500 seconds to simplify the calculations and to allow .02 seconds for the fire warning relay to close and the indicator to respond.) See Table II.

From this table, an approximate answer to the response time calculation can be immediately determined. It is seen that eight or more counts, and hence a fire warning, will be obtained 98.2% of the time within .480 seconds. Since this does not take into account the effects of the "reset" signals and the test periods, a more accurate answer requires a more complex calculation.

TABLE II

PROBABILITY OF EIGHT OR MORE COUNTS

TIME (T) SECONDS	EXPECTED COUNTS (A)	PROBABILITY
.032	1	.0000
.064	2	.0011
.072	2.25	.0022
.096	3	.0119
.104	3.25	.0183
.120	3.75	.0377
.128	4	.0511
.144	4.50	.0865
.160	5	.1334
.168	5.25	.1607
.192	6	.2560
.200	6.25	.2862
.208	6.50	.3272
.224	7	.4013
.240	7.5	.4753
.256	8	.5470
.264	8.25	.5880
.288	9	.6761
.296	9.25	.7040
.320	10	.7798
.352	11	.8568
.360	11.25	.8770
.384	12	.9105
.416	13	.9460
.448	14	.9684
.480	15	.9820
.512	16	.9900
.544	17	.9946
.576	18	.9971
.600	18.75	.9980

The calculation of the average alarm probabilities was done by dividing the counting window into twenty intervals and individually calculating the alarm probability for a fire starting at each interval. A sample calculation to obtain the probability of a specific response time is given below:

Conditions:

S = 15 counts in .480 seconds
N = 8 counts for alarm
M = 1.92 seconds (minimum counting window)

Calculation of the probability of alarm for a .480 second response time assuming that the fire starts .192 seconds before the end of the reset time cycle is as follows. At 0.192 seconds before the end of the cycle, the expected count from Table II is 6, which corresponds to a 0.2560 probability of alarm at N = 8 counts. As the probability is being determined for a total 0.480 second response time, during the next reset cycle there remains 0.480 - .192 or 0.288 seconds during which there is an additional probability of alarm. Therefore, the total probability is $0.256 + (1-0.2560) \times 0.6761 = 0.7620$.

Similar calculations were made for twenty equal time intervals within the 1.92 second counting window, and averaged to get the probability for a 0.480 second response time. Table III shows a summary of probability calculation for various response times, including probability calculations with a 0.120 second test time. All time intervals are equal except the second which was made .060 seconds or half the test time. This gives a better average for the start of fire during the test time interval than would be obtained with the 0.096 second interval. Although the test time adds to the insensitive time, and decreases the probability of alarm, its effect is only slight (1% or less) in view of the fact that it occurs only once in six reset cycles.

Finally, it is seen that a fire warning will be given within .5 second 94.34% of the time.

TABLE III

SUMMARY OF CALCULATIONS OF PROBABILITY OF RESPONSE FOR 0.480 SECOND RESPONSE TIME
ALARM = 8 COUNTS; RESET TIME = 1.92 SECONDS

START OF FIRE SECONDS AFTER t = 0	2-3-4-5 RESET CYCLES	NEXT RESET CYCLE	TOTAL PROB.	1ST RESET CYCLE	NEXT RESET CYCLE	TOTAL PROB.	6TH RESET CYCLE	NEXT RESET CYCLE	TOTAL PROB.
0	.9820	-	.9820	.8720	-	.8720	.9820	-	.9820
0.060	"	-	"	.9487	-	.9717	"	-	"
0.192	"	-	"	.9820	-	.9820	"	-	"
0.288	"	-	"	"	-	"	"	-	"
0.384	"	-	"	"	-	"	"	-	"
0.480	"	-	"	"	-	"	"	-	"
0.516	"	-	"	"	-	"	"	-	"
0.672	"	-	"	"	-	"	"	-	"
0.768	"	-	"	"	-	"	"	-	"
0.864	"	-	"	"	-	"	"	-	"
0.960	"	-	"	"	-	"	"	-	"
1.056	"	-	"	"	-	"	"	-	"
1.152	"	-	"	"	-	"	"	-	"
1.245	"	-	"	"	-	"	"	-	"
1.344	"	-	"	"	-	"	"	-	"
1.440	.9820	-	.9820	.9820	-	.9820	.9820	-	.9820
1.536	.9105	.0010	.9115	.9105	.0010	.9115	.9105	-	.9105
1.632	.6761	.0820	.7581	.6761	.0820	.7581	.6761	.0007	.6768
1.728	.2560	.5060	.7620	.2560	.5060	.7620	.2560	.1206	.3766
1.824	.0119	.9014	.9133	.0119	.9014	.9133	.0199	.5870	.5989

DESIGN CONSIDERATION: One test interval (0.120 sec.) is included in each period of six reset time cycles. The test interval appears at the start of the first reset time cycle.

Reset Time Cycle:	1	2	3	4	5	6
Probability:	0.9432	0.9528	0.9528	0.9528	0.9528	0.9061

Ave. probability per period - 0.9434

APPENDIX II

CALCULATION OF FALSE ALARM PROBABILITY

Here it is desired to evaluate this expression:

$$\sum_{X=8}^{X=\infty} \frac{A^X e^{-A}}{X!} \text{ , where}$$

$A = (.5^c/s)\ (2.88\ \text{sec}) = 1.44$
$3 = 2.718 \ldots$

Using published tables (4) with interpolation, leads to a probability of .000132. This is the probability of a false alarm per 2.88 second period. The probability per second is then .0000458, and the "mean time between failures" is 1/.0000458 or 21,800 seconds or 6.04 hours.

With two sensor tubes required to generate a fire alarm, the probability of a false alarm per 2.88 second period is $(.000132)^2$, or 1.74×10^{-8}. This leads to a probability per second of $.605 \times 10^{-8}$, and a "mean time between failures" of 1.655×10^8 seconds, or 46,000 hours or 960 days.

APPENDIX III

CALCULATION OF FAILURE-TO-TEST PROBABILITY

Here it is desired to evaluate this expression:

$$\sum_{X=0}^{X=7} \frac{A^X e^{-A}}{X!}$$, where

$A = 40$
$e = 2.718...$

Forty counts, rather than fifty, is taken as the expected number to allow for the fact that component variations could make the clock run 20% fast.

Using published tables (4) leads to a probability of less than .000001. Since the test period could occur as often as once every 11.52 seconds, the probability of failure per second is less than .0000000867. This is equivalent to a "mean time between failures" of greater than 11,520,000 seconds or greater than 3200 hours or greater than 133 days.

APPENDIX IV

INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
0	0	0	0	0	0	0	0	0						Normal
1	0	0	0	0	0	0	0	1						No Faults
2	0	0	0	0	0	0	1	0			X		X	No A and B Test = OHF, COHF
3	0	0	0	0	0	0	1	1			X		X	COHF, OHF
4	0	0	0	0	0	1	0	0			X			COHF
5	0	0	0	0	0	1	0	1			X			COHF
6	0	0	0	0	0	1	1	0		X	X		X	No A Test and CFB = OHF, COHF
7	0	0	0	0	0	1	1	1			X		X	COHF, OHF
8	0	0	0	0	1	0	0	0						No Conclusion (See 9)
9	0	0	0	0	1	0	0	1			X			EFB, COHF
10	0	0	0	0	1	0	1	0			X		X	No A Test and EFB - OHF, COHF
11	0	0	0	0	1	0	1	1			X		X	COHF, OHF
12	0	0	0	0	1	1	0	0			X			COHF
13	0	0	0	0	1	1	0	1			X			EFB, COHF
14	0	0	0	0	1	1	1	0			X		X	No A Test and EFB = OHF, COHF
15	0	0	0	0	1	1	1	1			X		X	COHF, OHF
16	0	0	0	1	0	0	0	0			X			EFB, COHF
17	0	0	0	1	0	0	0	1			X			EFB, COHF
18	0	0	0	1	0	0	1	0			X		X	No A Test and EFB = OHF, COHF
19	0	0	0	1	0	0	1	1			X		X	COHF, OHF
20	0	0	0	1	0	1	0	0			X			EFB, COHF
21	0	0	0	1	0	1	0	1			X			EFB, COHF
22	0	0	0	1	0	1	1	0			X		X	No A Test and EFB = OHF, COHF
23	0	0	0	1	0	1	1	1			X		X	COHF, OHF

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TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
24-1	0	0	0	1	1	0	0	0						B_{21} = OHB
-2										X				B_{12} = CFB
25	0	0	0	1	1	0	0	1			X			EFB, COHF
26-1	0	0	0	1	1	0	1	0			X		X	B_{21} = EFB, No A Test and EFB = OHF, COHF
-2											X			B_{12}, No A Test, COHF
27	0	0	0	1	1	0	1	1			X		X	COHF, OHF
28-1	0	0	0	1	1	1	0	0			X			B_{21} = OHB, COHF
-2										X				B_{12} = CFB
29	0	0	0	1	1	1	0	1			X			EFB, COHF
30-1	0	0	0	1	1	1	1	0			X		X	B_{21} = EFB, No A Test and EFB = OHF, COHF
-2											X			B_{12}, No A Test, COHF
31	0	0	0	1	1	1	1	1			X		X	COHF, OHF
32	0	0	1	0	0	0	0	0			X			COHF
33	0	0	1	0	0	0	0	1			X			COHF
34	0	0	1	0	0	0	1	0	X		X		X	COHF, CFA and No B Test = OHF, COHF
35	0	0	1	0	0	0	1	1			X		X	COHF, OHF
36	0	0	1	0	0	1	0	0			X			COHF
37	0	0	1	0	0	1	0	1			X			COHF
38	0	0	1	0	0	1	1	0	X	X			X	CFA and CFB = OHF
39	0	0	1	0	0	1	1	1			X		X	COHF, OHF
40	0	0	1	0	1	0	0	0			X			COHF
41	0	0	1	0	1	0	0	1			X			EFB, COHF
42	0	0	1	0	1	0	1	0	X		X		X	CFA and EFB = OHF, COHF
43	0	0	1	0	1	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
44	0	0	1	0	1	1	0	0			X			COHF
45	0	0	1	0	1	1	0	1			X			EFB, COHF
46	0	0	1	0	1	1	1	0	X		X		X	CFA and EFB = OHF, COHF
47	0	0	1	0	1	1	1	1			X		X	COHF, OHF
48	0	0	1	1	0	0	0	0			X			EFB, COHF
49	0	0	1	1	0	0	0	1			X			EFB, COHF
50	0	0	1	1	0	0	1	0	X		X		X	CFA and EFB = OHF, COHF
51	0	0	1	1	0	0	1	1			X		X	COHF, OHF
52	0	0	1	1	0	1	0	0			X			EFB, COHF
53	0	0	1	1	0	1	0	1			X			EFB, COHF
54	0	0	1	1	0	1	1	0	X		X		X	CFA and EFB = OHF, COHF
55	0	0	1	1	0	1	1	1			X		X	COHF, OHF
56-1	0	0	1	1	1	0	0	0			X			B(21) = OHB, COHF
-2										X	X			B(12) = CFB, COHF
57	0	0	1	1	1	0	0	1			X			EFB, COHF
58-1	0	0	1	1	1	0	1	0	X		X		X	B(21) = EFB, CFA and EFB - OHF, COHF
-2									X		X			B(12), CFA, COHF
59	0	0	1	1	1	0	1	1			X		X	COHF, OHF
60-1	0	0	1	1	1	1	0	0			X			B(21) = OHB, COHF
-2										X	X			B(12) = CFB, COHF
61	0	0	1	1	1	1	0	1			X			EFB, COHF
62-1	0	0	1	1	1	1	1	0	X		X		X	B(21) = EFB, CFA and EFB = OHF, COHF
-2									X					B(12), CFA
63	0	0	1	1	1	1	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
64	0	1	0	0	0	0	0	0						No Conclusion (see 65)
65	0	1	0	0	0	0	0	1			X			EFA, COHF
66	0	1	0	0	0	0	1	0			X		X	EFA and No B Test = OHF, COHF
67	0	1	0	0	0	0	1	1			X		X	COHF, OHF
68	0	1	0	0	0	1	0	0			X			COHF
69	0	1	0	0	0	1	0	1			X			EFA, COHF
70	0	1	0	0	0	1	1	0		X	X		X	EFA and CFB = OHF, COHF
71	0	1	0	0	0	1	1	1			X		X	COHF, OHF
72	0	1	0	0	1	0	0	0						No Conclusion (See 73)
73	0	1	0	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
74	0	1	0	0	1	0	1	0			X		X	EFA and EFB = OHF, COHF
75	0	1	0	0	1	0	1	1			X		X	COHF, OHF
76	0	1	0	0	1	1	0	0			X			COHF
77	0	1	0	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
78	0	1	0	0	1	1	1	0			X		X	EFA and EFB = OHF, COHF
79	0	1	0	0	1	1	1	1			X		X	COHF, OHF
80	0	1	0	1	0	0	0	0			X			EFB, COHF
81	0	1	0	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
82	0	1	0	1	0	0	1	0			X		X	EFA and EFB = OHF, COHF
83	0	1	0	1	0	0	1	1			X		X	COHF, OHF
84	0	1	0	1	0	1	0	0			X			EFB, COHF
85	0	1	0	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
86	0	1	0	1	0	1	1	0			X		X	EFA and EFB = OHF, COHF
87	0	1	0	1	0	1	1	1			X		X	COHF, OHF

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TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
88-1	0	1	0	1	1	0	0	0						B(21) = OHB
-2										X				B(12) = CFB
89	0	1	0	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
90-1	0	1	0	1	1	0	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
91	0	1	0	1	1	0	1	1			X		X	COHF, OHF
92-1	0	1	0	1	1	1	0	0			X			B(21) = OHB, COHF
-2										X				B(12) = CFB
93	0	1	0	1	1	1	0	1			X		X	EFA and EFB = OHF, COHF
94-1	0	1	0	1	1	1	1	0			X		X	B(21) = EFB, and EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
95	0	1	0	1	1	1	1	1			X		X	COHF, OHF
96	0	1	1	0	0	0	0	0			X			COHF
97	0	1	1	0	0	0	0	1			X			EFA, COHF
98	0	1	1	0	0	0	1	0			X		X	EFA and No B Test = OHF, COHF
99	0	1	1	0	0	0	1	1			X		X	COHF, OHF
100	0	1	1	0	0	1	0	0			X			COHF
101	0	1	1	0	0	1	0	1			X			EFA, COHF
102	0	1	1	0	0	1	1	0		X	X		X	EFA and CFB = OHF, COHF
103	0	1	1	0	0	1	1	1			X		X	COHF, OHF
104	0	1	1	0	1	0	0	0			X			COHF
105	0	1	1	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
106	0	1	1	0	1	0	1	0			X		X	EFA and EFB = OHF, COHF
107	0	1	1	0	1	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
108	0	1	1	0	1	1	0	0			X			COHF
109	0	1	1	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
110	0	1	1	0	1	1	1	0			X		X	EFA and EFB = OHF, COHF
111	0	1	1	0	1	1	1	1			X		X	COHF, OHF
112	0	1	1	1	0	0	0	0			X			EFB, COHF
113	0	1	1	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
114	0	1	1	1	0	0	1	0			X		X	EFA and EFB = OHF, COHF
115	0	1	1	1	0	0	1	1			X		X	COHF, OHF
116	0	1	1	1	0	1	0	0			X			EFB, COHF
117	0	1	1	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
118	0	1	1	1	0	1	1	0			X		X	EFA and EFB = OHF, COHF
119	0	1	1	1	0	1	1	1			X		X	COHF, OHF
120-1	0	1	1	1	1	0	0	0			X			B(21) = OHB, COHF
-2										X	X			B(12) = CFB, COHF
121	0	1	1	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
122-1	0	1	1	1	1	0	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
123	0	1	1	1	1	0	1	1			X		X	COHF, OHF
124-1	0	1	1	1	1	1	0	0			X			B(21) = OHB, COHF
-2										X	X			B(12) = CFB, COHF
125	0	1	1	1	1	1	0	1			X		X	EFA and EFB = OHF, COHF
126-1	0	1	1	1	1	1	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
127	0	1	1	1	1	1	1	1			X		X	COHF, OHF
128	1	0	0	0	0	0	0	0			X			EFA, COHF
129	1	0	0	0	0	0	0	1			X			EFA, COHF
130	1	0	0	0	0	0	1	0			X		X	EFA and No B Test = OHF, COHF
131	1	0	0	0	0	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
132	1	0	0	0	0	1	0	0			X			EFA, COHF
133	1	0	0	0	0	1	0	1			X			EFA, COHF
134	1	0	0	0	0	1	1	0		X	X		X	EFA and CFB = OHF, COHF
135	1	0	0	0	0	1	1	1			X		X	COHF, OHF
136	1	0	0	0	1	0	0	0			X			EFA, COHF
137	1	0	0	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
138	1	0	0	0	1	0	1	0			X		X	EFA and EFB = OHF, COHF
139	1	0	0	0	1	0	1	1			X		X	COHF, OHF
140	1	0	0	0	1	1	0	0			X			EFA, COHF
141	1	0	0	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
142	1	0	0	0	1	1	1	0			X		X	EFA and EFB = OHF, COHF
143	1	0	0	0	1	1	1	1			X		X	COHF, OHF
144	1	0	0	1	0	0	0	0			X		X	EFA and EFB = OHF, COHF
145	1	0	0	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
146	1	0	0	1	0	0	1	0			X		X	EFA and EFB = OHF, COHF
147	1	0	0	1	0	0	1	1			X		X	COHF, OHF
148	1	0	0	1	0	1	0	0			X		X	EFA and EFB = OHF, COHF
149	1	0	0	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
150	1	0	0	1	0	1	1	0			X		X	EFA and EFB = OHF, COHF
151	1	0	0	1	0	1	1	1			X		X	COHF, OHF
152-1	1	0	0	1	1	0	0	0			X	X		B(21) = OHB, EFA and OHB = OH, COHF
-2										X	X		X	B(12) = CFB, EFA and CFB = OHF, COHF
153	1	0	0	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
154-1	1	0	0	1	1	0	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
155	1	0	0	1	1	0	1	1			X		X	COHF, OHF

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	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
156-1	1	0	0	1	1	1	0	0			X	X		B(21) = OHB, EFA and OHB = OH, COHF
-2										X	X		X	B(12) = CFB, EFA and CFB = OHF, COHF
157	1	0	0	1	1	1	0	1			X		X	EFA and EFB = OHF, COHF
158-1	1	0	0	1	1	1	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
159	1	0	0	1	1	1	1	1			X		X	COHF, OHF
160	1	0	1	0	0	0	0	0			X			EFA, COHF
161	1	0	1	0	0	0	0	1			X			EFA, COHF
162	1	0	1	0	0	0	1	0			X		X	EFA and No B Test = OHF, COHF
163	1	0	1	0	0	0	1	1			X		X	COHF, OHF
164	1	0	1	0	0	1	0	0			X			EFA, COHF
165	1	0	1	0	0	1	0	1			X			EFA, COHF
166	1	0	1	0	0	1	1	0		X	X		X	EFA and CFB = OHF, COHF
167	1	0	1	0	0	1	1	1			X		X	COHF, OHF
168	1	0	1	0	1	0	0	0			X			EFA, COHF
169	1	0	1	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
170	1	0	1	0	1	0	1	0			X		X	EFA and EFB = OHF, COHF
171	1	0	1	0	1	0	1	1			X		X	COHF, OHF
172	1	0	1	0	1	1	0	0			X			EFA, COHF, NEED TC22 for B2
173	1	0	1	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
174	1	0	1	0	1	1	1	0			X		X	EFA and EFB = OHF, COHF
175	1	0	1	0	1	1	1	1			X		X	COHF, OHF
176	1	0	1	1	0	0	0	0			X		X	EFA and EFB = OHF, COHF
177	1	0	1	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
178	1	0	1	1	0	0	1	0			X		X	EFA and EFB = OHF, COHF
179	1	0	1	1	0	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
180	1	0	1	1	0	1	0	0			X		X	EFA and EFB = OHF, COHF
181	1	0	1	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
182	1	0	1	1	0	1	1	0			X		X	EFA and EFB = OHF, COHF
183	1	0	1	1	0	1	1	1			X		X	COHF, OHF
184-1	1	0	1	1	1	0	0	0			X	X		B(21) = OHB, EFA and OHB = OH, COHF
-2										X	X		X	B(12) = CFB, EFA and CFB = OHF, COHF
185	1	0	1	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
186-1	1	0	1	1	1	0	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
187	1	0	1	1	1	0	1	1			X		X	COHF, OHF
188-1	1	0	1	1	1	1	0	0			X	X		B(21) = OHB, EFA and OHB = OH, COHF
-2										X	X		X	B(12) = CFB, EFA and CFB = OHF, COHF
189	1	0	1	1	1	1	0	1			X		X	EFA and EFB = OHF, COHF
190-1	1	0	1	1	1	1	1	0			X		X	B(21) = EFB, EFA and EFB = OHF, COHF
-2											X			B(12), EFA, COHF
191	1	0	1	1	1	1	1	1			X		X	COHF, OHF
192-1	1	1	0	0	0	0	0	0						A(21) = OHA
-2									X					A(12) = CFA
193	1	1	0	0	0	0	0	1			X			EFA, COHF
194-1	1	1	0	0	0	0	1	0			X		X	A(21) = EFA, EFA and No Test B = OHF, COHF
-2											X			A(12), No Test B, COHF
195	1	1	0	0	0	0	1	1			X		X	COHF, OHF
196-1	1	1	0	0	0	1	0	0			X			A(21) = OHA, COHF
-2									X		X			A(12) = CFA, COHF
197	1	1	0	0	0	1	0	1			X			EFA, COHF
198-1	1	1	0	0	0	1	1	0		X	X		X	A(21) = EFA, EFA and CFB = OHF, COHF
-2										X	X			A(12), CFB, COHF
199	1	1	0	0	0	1	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
200-1	1	1	0	0	1	0	0	0						A(21) = OHA
-2									X					A(12) = CFA
201	1	1	0	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
202-1	1	1	0	0	1	0	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
203	1	1	0	0	1	0	1	1			X		X	COHF, OHF
204-1	1	1	0	0	1	1	0	0			X			A(21) = OHA, COHF
-2									X		X			A(12) = CFA, COHF
205	1	1	0	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
206-1	1	1	0	0	1	1	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
207	1	1	0	0	1	1	1	1			X		X	COHF, OHF
208-1	1	1	0	1	0	0	0	0			X	X		A(21) = OHA, OHA and EFB = OH, COHF
-2									X		X		X	A(12) = CFA and EFB = OHF, COHF
209	1	1	0	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
210-1	1	1	0	1	0	0	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
211	1	1	0	1	0	0	1	1			X		X	COHF, OHF
212-1	1	1	0	1	0	1	0	0			X	X		A(21) = OHA, OHA and EFB = OH, COHF
-2									X		X		X	A(12) = CFA, CFA and EFB = OHF, COHF
213	1	1	0	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
214-1	1	1	0	1	0	1	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
215	1	1	0	1	0	1	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
216-1	1	1	0	1	1	0	0	0	X	X			X	A(12) and B(12) = CFA and EFB = OHF
-2										X		X		A(21) and B(12) = OHA and CFB = OH
-3									X			X		A(12) and B(21) = CFA and OHB = OH
-4												X		A(21) and B(21) = OHA and OHB = OH
217	1	1	0	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
218-1	1	1	0	1	1	0	1	0			X			A(12), B(12), COHF
-2											X			A(21) = EFA, B(12), COHF
-3											X			A(12), B(21) = EFB, COHF
-4											X		X	A(21) and B(21) = EFA and EFB = OHF, COHF
219	1	1	0	1	1	0	1	1			X		X	COHF, OHF
220-1	1	1	0	1	1	1	0	0	X	X			X	A(12) and B(12) = CFA and CFB = OHF
-2										X		X		A(21) and B(12) = OHA and EFB = OH
-3									X		X	X		A(12) and B(21) = CFA and OHB = OH, COHF
-4											X	X		A(21) and B(21) = OHA and OHB = OH, COHF
221	1	1	0	1	1	1	0	1			X		X	EFA and EFB = OHF, COHF
222-1	1	1	0	1	1	1	1	0			X			A(12), B(12), COHF
-2											X			A(21) = EFA, B(12), COHF
-3											X			A(12), B(21) = EFB, COHF
-4											X		X	A(21) and B(21) = EFA and EFB = OHF, COHF
223	1	1	0	1	1	1	1	1			X		X	COHF, OHF
224-1	1	1	1	0	0	0	0	0			X			A(21) = OHA, COHF
-2									X					A(12) = CFA
225	1	1	1	0	0	0	0	1			X			EFA, COHF
226-1	1	1	1	0	0	0	1	0			X		X	A(21) = EFA, EFA and No B Test = OHF, COHF
-2											X			A(12), No Test B, COHF
227	1	1	1	0	0	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
228-1	1	1	1	0	0	1	0	0			X			A(21) = OHA, COHF
-2									X		X			A(12) = CFA, COHF
229	1	1	1	0	0	1	0	1			X			EFA, COHF
230-1	1	1	1	0	0	1	1	0		X	X		X	A(21) = EFA, EFA and CFB = OHF, COHF
-2										X				A(12), CFB
231	1	1	1	0	0	1	1	1			X		X	COHF, OHF
232-1	1	1	1	0	1	0	0	0			X			A(21) = OHA, COHF
-2									X					A(12) = CFA
233	1	1	1	0	1	0	0	1			X		X	EFA and EFB = OHF, COHF
234-1	1	1	1	0	1	0	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
235	1	1	1	0	1	0	1	1			X		X	COHF, OHF
236-1	1	1	1	0	1	1	0	0			X			A(21) = OHA, COHF
-2									X		X			A(12) = CFA, COHF
237	1	1	1	0	1	1	0	1			X		X	EFA and EFB = OHF, COHF
238-1	1	1	1	0	1	1	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
239	1	1	1	0	1	1	1	1			X		X	COHF, OHF
240-1	1	1	1	1	0	0	0	0			X	X		A(21) = OHA, OHA and EFB = OH, COHF
-2									X		X		X	A(12) = CFA, CFA and EFB = OHF, COHF
241	1	1	1	1	0	0	0	1			X		X	EFA and EFB = OHF, COHF
242-1	1	1	1	1	0	0	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
243	1	1	1	1	0	0	1	1			X		X	COHF, OHF

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INTEGRATED FIRE AND OVERHEAT SYSTEM
TRUTH TABLE FOR OVERHEAT SIGNAL PROCESSOR

	PROCESSOR OUTPUT								SYSTEM STATUS LIGHTS					
LINE	A1	A2	A3	B1	B2	B3	TC 12	TC 22	CABLE A	CABLE B	COM-PUTER	OVER-HEAT	OVERHEAT FAIL	REMARKS
244-1	1	1	1	1	0	1	0	0			X	X		A(21) = OHA, OHA and EFB = OH, COHF
-2									X		X		X	A(12) = CFA, CFA and EFB = OHF, COHF
245	1	1	1	1	0	1	0	1			X		X	EFA and EFB = OHF, COHF
246-1	1	1	1	1	0	1	1	0			X		X	A(21) = EFA, EFA and EFB = OHF, COHF
-2											X			A(12), EFB, COHF
247	1	1	1	1	0	1	1	1			X		X	COHF, OHF
248-1	1	1	1	1	1	0	0	0	X	X			X	A(12) and B(12) = CFA and CFB = OHF
-2										X	X	X		A(21) and B(12) = OHA and CFB = OH, COHF
-3									X			X		A(12) and B(21) = CFA and OHB = OH
-4											X	X		A(21) and B(21) = OHA and OHB = OH, COHF
249	1	1	1	1	1	0	0	1			X		X	EFA and EFB = OHF, COHF
250-1	1	1	1	1	1	0	1	0			X			A(12), B(12), COHF
-2											X			A(21) = EFA, B(12), COHF
-3											X			A(12), B(21) = EFB, COHF
-4											X		X	A(21) and B(21) = EFA and EFB = OHF, COHF
251	1	1	1	1	1	0	1	1			X		X	COHF, OHF
252-1	1	1	1	1	1	1	0	0	X	X			X	A(12) and B(12) = CFA and CFB = OHF
-2										X	X	X		A(21) and B(12) = OHA and CFB = OH, COHF
-3									X		X	X		A(12) and B(21) = CFA and OHB = OH, COHF
-4											X	X		A(21) and B(21) = OHA and OHB = OH, COHF
253	1	1	1	1	1	1	0	1			X		X	EFA and EFB = OHB, COHF
254-1	1	1	1	1	1	1	1	0						A(12), B(12), No Faults
-2											X			A(21) = EFA, B(12), COHF
-3											X			A(12), B(21) = EFB, COHF
-4											X		X	A(21) and B(21) = EFA and EFB = OHF, COHF
255	1	1	1	1	1	1	1	1			X		X	COHF, OHF

APPENDIX V

GENERAL TEST PLAN

FOR

SYSTEM PERFORMANCE TESTS

INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM

AIR FORCE CONTRACT F33615-72-C-1053

MAY 15, 1972

(REVISED JUNE 10, 1975)

(REVISED DECEMBER 11, 1975)

REPORT NUMBER 59377-1

EDISON ELECTRONICS DIVISION

MCGRAW-EDISON COMPANY

GRENIER FIELD

MANCHESTER, NEW HAMPSHIRE

McGRAW-EDISON COMPANY
Edison Electronics Division

Grenier Field Municipal Airport, Manchester, N.H. 03103

TO: Mat Reiser

DATE: 11 June 1976

FROM: Dick Jurentkuff

cc: M. Bober

Subject: CORROSION OF SHIELDING BOX ON THE COMPUTER CONTROL UNIT (I.F.O.S.)

As you know, the shielding box (Dwg. No. B-61725) when mounted in the CCU showed signs of severe corrosion after the CCU went thru the humidity test.

The print called for the finish to be cadmium plate yellow chromate per QQ-P-416, Type II, Class 3.

After reading the spec thru, I found that cadmium plate is not recommended for usage as we did for the shielding box. For instance: Cadmium plated parts should not be used in a nonventilated container with/or in contact with electrical equipment. Cadmium plated parts should not be in an area where there is the presence of organic electrical insulation, phenolic resinous substances and others containing unsaturated carbon to carbon linkages such as oil paints, potting compounds, RTV, etc.

Just to verify these facts, I sent a shielding box to Plant #2 to check if indeed it was cadmium plated. Results were that it was cadmium plated but wasn't able to verify thickness of plating. I then took the same box, submitted it for 48 hours of salt spray which showed no signs of corrosion.

Summary: Cadmium plate is not a suitable plating to be used in applications such as Edison Electronics is doing now. It would be my opinion not to use Cadmium plating on any electronic equipment. I would also suggest that this part should have a finish of tin plating per MIL-T-10727, Type II. Type II is hot dipped.

R. Jurentkuff

RJ/meg

1.0 SCOPE

This specification defines the performance tests which will be run on the Integrated Fire and Overheat Detection System for aircraft to fulfill the requirements of Contract F33615-72-C-1053, Attachment 1, paragraph IVB.

2.0 TEST SYSTEM

The test system will consist of the following parts with the associated interconnecting cable assemblies except as noted in section 4.3 and 4.4.

1 Computer Control Unit (CCU)
1 Maintenance Warning Unit (MWU)
1 Crew Readout Unit (CRU)
6 Ultraviolet Detector Heads
1 Dual Overheat Cable Loop

3.0 TEST CONDITIONS

Unless otherwise specified, all tests will be performed at nominal input voltage and at room temperature, humidity and barometric pressure. Also, unless otherwise specified, the test system shall not be operated during the environmental tests of 4.3 and 4.4 Also, the tests of paragraph 4.2 shall be performed with cables one hundred feet in length between the Computer Control Unit and the readout units. All other tests will either be 25 or 100 feet. Cable length between Computer Control Unit and Detector Heads shall be 40 feet. Paragraph 4.2.2 thru 4.2.9 will be accomplished outdoors on Edison grounds. All other tests will take place under standard Laboratory conditions.

4.0 TEST PROCEDURE

4.1 Initial System Test

4.1.1

The system shall be energized and observed for proper operation. All lights on the Maintenance Warning Unit and Crew Readout Unit shall be out. The lamp switch on each readout unit shall be pushed to verify that all lamps are operational.

4.1.2

Each Ultraviolet Detector Head shall, in turn, be exposed to a saturating source of ultraviolet radiation. The FIRE warning light of the Crew Readout Unit shall come on during exposure with all other lights remaining unchanged. The source shall then be removed and the FIRE warning shall go out. One Sensor in the Detector Head shall be shielded both from the saturating source and also from the test source and the other sensor shall be exposed to the saturating source. The FIRE warning light and the appropriate sensor light on the Maintenance Warning Unit shall come on. The

shield shall be removed from the first sensor, placed over the second and the RESET switch on the Maintenance Warning Unit shall be pushed. The FIRE warning light shall again be on, the first sensor light on the Maintenance Warning Unit shall be out, and the second sensor light on the Maintenance Warning Unit shall come on. This test shall be repeated for each Detector Head.

4.1.3

The test source in each Detector Head shall be, in turn, shielded from the sensors. The Maintenance Warning Unit lights for the two sensors in that Detector Head shall come on. With the source still shielded, the two sensors in the Detector Head shall be exposed to a saturating source of ultraviolet radiation. The FIRE warning light on the Crew Readout shall not come on until the next time the (shielded) test source is activated. An adjacent Detector Head shall be exposed to the saturating source and the FIRE warning light shall come on. The test source shield and the saturating source shall then be removed and the RESET switch depressed. The associated lights on the Maintenance Warning Unit and the Crew Readout Unit shall go out. This test shall be repeated for each Detector Head.

4.1.4

The test sources in two adjacent Detector Heads shall be shielded. The lights on the Maintenance Warning Unit for the sensors in these Detector Heads, shall come on. The FIRE FAIL light shall also come on. The shields shall then be removed from the two sources and no change in the condition of the lights shall occur. The remaining four Detector Heads shall then be exposed to a saturating source of ultraviolet radiation. The FIRE warning light shall not come on. This test shall be repeated for all adjacent Detector Heads.

4.1.5

Both dual Overheat Cables shall be heated with a localized heating or in an oven. The OVERHEAT light on the Crew Readout Unit shall come on during the exposure with all other lights remaining unchanged. The heat source shall then be removed and the OVERHEAT light shall go out. One cable shall then be disconnected at one end from the circuit. The heat shall then be applied to both cables and the appropriate cable light on the Maintenance Warning Unit and the OVERHEAT light shall come on. The heat shall be removed and the overheat light shall go out. The first cable shall be reconnected to the circuit, the second cable disconnected and the reset button pushed. The appropriate change shall occur on the Maintenance Warning Lights. Heat shall then be applied to both cables and the OVERHEAT light shall come on. The heat shall be removed and the OVERHEAT light shall go out. The second cable shall be reconnected and the Reset button pushed. The appropriate change shall occur on the Maintenance Warning Lights. Heat shall then be applied to both cables and the OVERHEAT light shall come on. The heat shall be removed and the OVERHEAT light shall go out.

4.1.6

The "lower" ends of both cables shall be disconnected from the circuit. The appropriate cable lights on the Maintenance Warning Unit and

the OVERHEAT FAIL light on the Crew Readout Unit shall come on. The cables shall then be heated with localized heating or in an oven. The OVERHEAT light shall not come on. Heat shall be removed and the cables shall then be reconnected and the Reset button pushed. The cable lights on the Maintenance Warning Unit and the OVERHEAT FAIL light shall go out.

4.1.7

One of the dual Overheat Cables shall be disconnected at the "lower" end from the Computer Control Unit and shorted from center wire to sheath. The appropriate light on the Maintenance Warning Unit shall come on. The second cable shall similarly be disconnected and shorted. The OVERHEAT FAIL light shall come on in addition to the appropriate Maintenance Warning Unit light. Both cables shall be reconnected to the Computer Control Unit with the shorts removed and the Reset button pushed. The Maintenance Warning Unit lights and OVERHEAT FAIL light shall go out.

4.1.8

The power input to the Computer Control Unit shall be interrupted. Both the FIRE FAIL and the OVERHEAT FAIL lights on the Crew Readout Unit shall come on.

4.1.9

One ultraviolet Detector Head and one Overheat Cable shall be disconnected from the Computer Control Unit. The appropriate lights on the Maintenance Warning Unit shall come on. Power to the system shall be removed for a period of three hours and then reapplied. When power is reapplied, the Maintenance Warning Unit lights shall return to their status before power was removed.

4.2 Performance Test

4.2.1 Overheat Cable Calibration Test

The overheat cables shall be placed in a calibrated oven or bath with the balance of the system at room ambient conditions. The oven or bath temperature shall be raised to within 100°F of the cable alarm temperature and then increased at a rate not exceeding 4°F per minute until the OVERHEAT light comes on. The control shall alarm within ±5% of its normal alarm temperature.

4.2.2 Detector Head Calibration Test

Each Detector Head shall in turn be exposed to the fire of paragraph 4.5 of MIL-D-27729A. The FIRE light shall come on within 500 milliseconds, at least 90% of the time, when the Detector Head is 4 feet away from the flame along its center line. Following alarm, approximately one-half (design goal 1/2), the flame front of the test fire shall be physically blocked from the Detector Head view and the alarm indication shall continue to hold. Following this, the flame shall be completely blocked from the Detector Head view and the FIRE light shall go out within 0.2 to 1.5 seconds. These tests shall be performed under various steady state power inputs of MIL-STD-704 except the low voltage limit should not be less than 18 VDC. This test sequence shall be repeated for each Detector Head.

At the completion of this test utilizing fire of MIL-D-27729A, paragraph 4.5, qualify and calibrate substitute propane flame source for equivalent response and profile characteristics for inside laboratory use.

4.2.3 Detector Head Cone of Vision

Each Detector Head shall be tested for cone of vision in the horizontal and vertical planes at 40° off the center line using the test fire paragraph 4.5 of MIL-D-27729A. The FIRE warning light shall come on within 500 milliseconds, at least 90% of the time, when the Detector Head is 4 feet away from the flame. Following alarm, one-half the flame front of the test fire shall be physically blocked from the Detector Head view and the alarm indication shall continue to hold. This test sequence shall be repeated for each Detector Head.

4.2.4 Detector Head Attenuation Test

Each Detector Head shall continue to function and cause an alarm when exposed to a rapidly burning 5-inch diameter pan of gasoline (100 octane) or JP4 fuel with and without the addition of 30 percent by volume of hydraulic fluid when the window in the Detector Head is coated with JP4 fuel. There shall be a minimum air flow of 100 CFM across this window. The FIRE light shall come on when the Detector Head to test-flame distance is no less than 2 feet along its center line. This test sequence shall be repeated for each Detector Head.

4.2.5 Overheat Cable Power Variation Tests

Flame tests in accordance with paragraph 4.5.4 of MIL-F-7872C shall be performed on the Overheat Cables under the various steady state input power conditions specified in MIL-STD-704 except the low voltage limit should not be less than 18 VDC. This limit applies to all overheat cable tests, in particular, General Test Plan paragraphs 4.2.6, 4.2.7, 4.2.8 and 4.2.9. In each case, an alarm shall occur in not more than 5 seconds after exposure to flame and shall clear in not more than 30 seconds after removal of the flame.

4.2.6 Overheat Cable Response Time with 815°C (1500°F) Flame

Flame tests shall be conducted on the Overheat Cables in accordance with 4.5.4 of MIL-F-7872C using a flame temperature of 815°C (1500°F). An alarm shall occur in not more than 10 seconds after flame application.

4.2.7 Overheat Cable Reset Time

The flame test of paragraph 4.5.4 of MIL-F-7872C shall be applied to the Overheat Cables for a period of at least one minute. The flame shall then be removed. Within 5 seconds after the alarm has cleared, the flame shall be reapplied and an alarm shall occur in not more than 5 seconds.

4.2.8 Overheat Cable Partial Extinguishment Test

The flame tests of paragraph 4.5.4 of MIL-F-7872C shall be applied to the Overheat Cables for a period of 30 seconds. The test flame shall then be masked so as to reduce its effective area of contact by approximately 50 percent. The alarm signal shall not clear. After an additional 30 seconds, the flame shall be removed entirely and the alarm signal shall then clear in not more than 30 seconds.

4.2.9 Overheat Cable Repeated Response and Clearance Time Test

The flame test of paragraph 4.5.4 of MIL-F-7872C shall be applied for two periods of at least one minute each. The cables shall be cooled to room temperature or to the alternate temperature permitted by paragraph 4.5.1.1 of MIL-F-7872C after each exposure to flame. The flame shall then be applied a third time to the same portion previously heated. An alarm signal shall occur in not more than 5 seconds after each exposure to flame, the alarm shall clear in not more than 30 seconds after the flame has been removed. Artificial means of cooling the cables shall not be used. During these tests, the cable elements subjected to the flame shall be vibrated at an acceleration of 10 g at a frequency of 30 cycles per second. This vibration may be produced by a mechanical means such as an 1800 rpm motor driving an eccentric arm or cam.

4.2.10 Overheat Cable Salt Water Immersion Test

With the system operating at standby, the Overheat Cables shall be disconnected at a convenient point. The OVERHEAT FAIL light shall come on. The open end fittings shall be completely immersed in a 5 percent solution (by weight) of salt water for not less than 10 seconds and an alarm shall not occur. The end fitting shall be removed from the salt solution and excess solution may be shaken off. Within one minute after removal from the salt solution, the cables shall be reconnected and the Reset button pushed. The OVERHEAT FAIL light shall go out.

4.3 Environmental Tests

4.3.1 Electromagnetic Interference

The complete system shall be subjected to the electromagnetic interference tests of MIL-STD-461A of Category I-C equipment. System performance shall be as required by that specification.

4.3.2 High Temperature

The complete system shall be subjected to a forty-eight hour 71.1°C (160°F) storage test. At the conclusion of this test and while still at temperature, the system shall be checked for normal operation by exposing the Detector Head to a saturating source of ultraviolet radiation and by exposing the Overheat Cables to localized heating. Lights on the two readout units shall be observed for proper operation. Following this, the Maintenance Warning Unit and Crew Readout Unit shall be removed from the test chamber to room ambient and the chamber temperature brought to 82.2°C

(180°F) and held for a period of four hours. At the conclusion of this test and while still at temperature, the system shall be checked for normal operation by exposing each Detector Head to a saturating source of ultraviolet radiation simultaneously for 5 minutes and by exposing the Overheat Cables to localized heating. Lights on the Readout Units shall be monitored for proper operation. Following this and with the Computer Control Unit still at 82.2°C (180°F), the Overheat Cables shall be removed from the oven and the calibration test of paragraph 4.2.1 repeated. The system alarm point shall not vary more than 6 percent from the reference alarm temperature of 4.2.1. Following this, the Detector Heads shall be placed in a separate oven for four hours at 260°C (500°F) while the Computer Control Unit is held at 82.2°C (180°F) for the same period and the calibration test, using the qualified propane flame of 4.2.2, shall be repeated for each Detector Head. Also, the Detector Head shall be checked against the equivalent of 5000 foot candles of unfiltered sunlight originating at an angle of 45° or less from the zenith and shall not cause a false alarm.

4.3.3 Low Temperature

The complete system shall be subjected to a four-hour -40°C (-40°F) storage test. At the conclusion of this test and while still at temperature, the system shall be checked for normal operation by exposing each Detector Head to a saturating source of ultraviolet radiation and by exposing the cables to localized heating. Lights on the Maintenance Warning Unit and the Crew Readout Unit shall be observed for proper operation. Following this, the Overhead Cables shall be removed from the chamber and shall undergo the calibration test of paragraph 4.2.1 with the Computer Control Unit still at -40°C. The system alarm point shall not vary more than 6 percent from the reference alarm temperature of 4.2.1 Following this, with the Computer Control Unit and Detector Heads still at -40°C, the calibration test using the qualified calibrated propane flame of 4.2.2, shall be repeated for each Detector Head. Also, the Detector Head shall be checked against equivalent of 5000 foot candles of unfiltered sunlight originating at an angle of 45° or less from zenith and shall not cause a false alarm.

4.3.4 Shock

Shock tests shall be performed on the system in accordance with Procedure I of method 516 of MIL-STD-810B using a sawtooth waveform at a level of 20 g's and a duration of 11 milliseconds. The test shall be performed on Overheat Cables sixty inches long. Also, the shock test may be performed on the complete test system at one time or potions of the system may be tested individually to accommodate fixturing. During this test, the Overheat Cables shall be supported by mounting clamps spaced approximately 8 inches apart. Following this test, the system shall be checked for normal operation by exposing the Detector Heads to a saturating source of ultraviolet radiation and by exposing the cables to localized heating.

4.3.5 Extreme Exposure

One Detector Head shall be subjected to two repeated exposures at a temperature of 1093.3°C (2000°F) in an oven for a period of 1 minute each. Following this, the Detector Head shall be checked in the system for normal operation by means of a saturating source of ultraviolet radiation. Also, the Detector Head shall be checked against the equivalent of 5000 foot candles of unfiltered sunlight originating at an angle of 45° or less from the zenith and shall not cause a false alarm.

4.3.6 Altitude

The complete system* shall be installed in an altitude chamber and operated at a standby. The chamber temperature shall then be reduced to -40°C (-40°F) and the pressure reduced to the equivalent of 70,000 feet above sea level. These conditions shall be maintained for one hour. At the conclusion of this time and while still at temperature and pressure, the system shall be checked for normal operation by means of a saturating source of ultraviolet radiation and by localized heating or resistance in parallel with the Overheat Cables. The chamber shall then be returned to room ambient conditions and the system again checked for normal operation by means of the saturating source of ultraviolet radiation and by localized heating of the cables.

4.4 Environmental Tests

4.4.1 Temperature Shock

The complete system* shall be subjected to a temperature shock test in accordance with Method 503, Procedure I of MIL-STD-810B. The temperature extremes shall be 71.1°C (160°F) and -40°C (-40°F). At the conclusion of this test, the system shall be checked for normal operation by means of ultraviolet radiation for the Detector Heads and by means of localized heating of the Overheat Cables. Following this, one Detector Head shall be subjected to a temperature shock test from -53.8°C (-65°F) to 300°C (572°F) in accordance with paragraph 4.3.4 of MIL-D-27729A. The Detector Head shall be checked for normal operation following this test, by means of a saturating source of ultraviolet radiation.

4.4.2 Vibration

Vibration tests shall be performed on the system in accordance with Procedure I, Curve E, Parts 1, 2 and 3; Time schedule I of Method 514 of MIL-STD-810B. The test shall be performed on one Detector Head rather than six and shall be performed on Overheat Cables sixty inches long. Also, the vibration may be performed on the complete test system at one time or portions of the system may be vibrated individually to accommodate fixturing. During this test, the Overheat Cables shall be supported by mounting clamps spaced approximately 8 inches apart. Following the test,

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*The Crew Readout Unit and the Maintenance Warning Unit need not be subjected to these tests.

the system shall be checked for normal operation by exposing the Detector Heads to a saturating source of ultraviolet radiation and by exposing the cables to localized heating.

4.4.3 Humidity

The complete system* with one Detector Head instead of six, shall be subjected to a humidity test in accordance with Method 507, Procedure I of MIL-STD-810B. The Crew Readout Unit and Maintenance Warning Unit will be subjected to a reduced humidity test for information and evaluation. Immediately after completion of testing, the system shall be checked for normal operation by means of a saturating source of ultraviolet radiation for the Detector Head and localized heating for the Overheat Cables.

4.4.4 Salt/Fog

The system* with one Detector Head instead of six, shall be subjected to a salt/fog test in accordance with Method 509, Procedure I of MIL-STD-810B. Immediately following this test, the system shall be checked for normal operation by means of a saturating source of ultraviolet radiation for the Detector Head and localized heating for the Overheat Cables. The system shall then be inspected for corrosion, stored for 48 hours and retested in accordance with the Method 509 requirements.

Note: Paragraphs 4.3.1, 4.3.4 and 4.3.6 are to be done by an outside vendor.

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*The Crew Readout Unit and the Maintenance Warning Unit need not be subjected to these tests.

APPENDIX VI

EDISON ELECTRONIC DIVISION

McGRAW-EDISON COMPANY

GRENIER FIELD

MANCHESTER, N. H. 03103

INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM

TEST REPORT

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CHIEF ENGINEER

1.0 OBJECT

This report documents the qualification test program performed by McGraw-Edison Electronics Division on one Integrated Fire and Overheat Detection System.

SYSTEM SN 1

1	Crew Readout Unit	CRU	44222
1	Maintenance Warning Unit	MWU	44221
1	Computer Control Unit	CCU	44238
6	Flame Sensor Heads		44227
2	Overheat Sensor Cables		

2.0 ADMINISTRATIVE DATA

Shock & vibration test performed by Associated Testing Laboratory, Burlington, Mass.
Electromagnetic interface test: performed by Sanders Associates, Nashua, N.H.
All remaining tests were performed at Edison facilities.

3.0 APPLICABLE DOCUMENTS

Mil-F-7872C Fire & Overheat Warning Systems
Mil-Std 810B Environmental Test Methods
Mil-D-27729A Smoke and Fire Detection for Aerospace Vehicles
Mil-Std-704 Electrical Aircraft Power
Mil-Std-461A Electromagnetic Interface

General Test Plan for System Performance Test, Integrated Fire and Overheat Detection System, Air Force contract F33615-72-C-1053.

4.0 TESTING PERFORMED

The following tests were performed in accordance with the general test plan:

TEST PERFORMED	SYSTEM	PARAGRAPH
Initial System Test	1	4.1
Lamp Indications		4.1.1
Flame Sensor logic		4.1.2
Sensor Fault logic		4.1.3
Adjacent Head Fault logic		4.1.4
Overheat Sensor		4.1.5
Initial System Test	1	4.1
Overheat Open Fault logic		4.1.6
Overheat Short Fault logic		4.1.7
Power interupt logic		4.1.8
Fault memory		4.1.9

Performance Test	1	4.2
Overheat Cal		4.2.1
Detector head cal		4.2.2
Detector head vision		4.2.3
Detector head attenuation		4.2.4
Overheat Power variation		4.2.5
Overheat Cable response time 815°C (1500°F)		4.2.6
Overheat Cable reset time		4.2.7
Overheat Cable partial extinguishment test		4.2.8
Overheat Cable repeated response and clearance		4.2.9
Overheat Cable salt water immersion test		4.2.10

Environmental Test	1	4.3
Electromagnetic Environmental		4.3.1
High Temp		4.3.2
Low Temp		4.3.3
Shock		4.3.4
Extreme Exposure Sensor		4.3.5
Altitude		4.3.6
Temperature Shock		4.4.1
Vibration		4.4.2
Humidity		4.4.3
Salt Spray		4.4.4

4.1 Test Equipment

Description	Make & Model
Power supply 0-30 volt DC 5 amp	Harrison Model 622A
Temp Chamber 37.7°C (-100°F) 176.6°C (+350°F)	Thermotron F-11-CH-22
Hi Temp Chamber 23.8°C (+75°F) 1204.9°C (2200°F)	Lindberg Type 51442
Humidity Chamber	Blue M FR-256PC
Salt Spray Chamber	Associated Testing SA.80
Decade Box	Leed Northrup 4776
Hi Temp Chamber	GECO-Type HCO
Flame Pot	Edison per MIL-F-7872
Turner Propane Torch (Calibrated propane flame)	

Edison Quartz 10 Dine tube
(Sunlight source)

5" diameter stainless steel
gasoline container (open flame)

Stop Watch

Shutter

5.0 CONCLUSION

One system performed within the specification tolerances during and after each test of this program except where as noted in the results section. See appendixes A test plan, B data sheets.

6.0 TEST PROCEDURE AND RESULTS

6.1 Initial Test, Reference Paragraph 4.1.2 of Test Procedure

The initial test plan is a confidence check of system logic and sensor operation. A failure was discovered during test of paragraph 4.1.2 when it was observed that the maintenance warning unit, MWU, did not exhibit the correct indicator response. This discrepancy was related to an electrical failure of electronic circuit card within the computer control assembly. Integrated circuit component *UI3 failed due to a solder wisker shorting* the device. This condition was caused by a workmanship problem. Test was successfully passed after replacement of circuit card assembly. To implement the test procedure it was necessary to remove the quartz lens assembly from the sensor case to be able to cover the sensor with a Dixie cup.

6.2 Performance Test, Reference Test Procedure Paragraph 4.2

Overheat cable response times were measured using a flame pot configured to Mil-F-7872C. Flame sensor response times were measured using a flame source defined by Mil-D-27729A in conjunction with a shutter arrangement to supply a sync pulse to an oscilloscope for measuring response time.

6.3 Environmental Test Reference Test Procedure Paragraph 4.3

6.3.1 Electromagnetic Environment Ref TP 4.3.1

This test was conducted by Sanders Associates; see Appendixes C for test report. Maximum limits were exceeded in the following test:

CEO-3 Broadband, 28 volt return lead
280 KHZ to 1.5 MHZ
CEO-3 Narrow band, 28 volt return lead
260 KHZ, 560 KHZ, 850 KHZ
CEO-3 Transient 28 volt return 800 KHZ
CEO-3 Transient 28 volt positive lead 25 MHZ

REO-2 Broadband radiation .014 MHZ .020 MHZ and .031 MHZ
REO-2 Narrow band radiation 25 MHZ
125 MHZ 254 MHZ 284 MHZ
REO-2 Transient 25 MHZ

The following tests were satisfactorily passed: RS03, RS02, CS06, CS02, CS01.

6.3.2 High Temp Storage, Reference TP 4.3.2

High temp storage was successfully completed after an initial problem was encountered with four flame sensor heads as the sensor tubes became fogged due to residue deposit formed from outgassing of the potting compound. This residue attenuated the UV Signal from the source lamps to the sensor tube resulting in self-test failure. A fifth flame sensor failed due to an element within the UV tube that separated due to probable temperature stress on an imperfection of the element itself. The weld of the element itself remained secure and was not at fault. Probable cause of element imperfection may have been related to stress during welding operation. All of the flame sensors were reworked and properly cured, the unit with the defective tube was replaced and all of the flame sensors were re-tested and passed.

6.3.3 Extreme Exposure Reference TP 4.3.5

Flame sensor #5 was placed in 1093.3°C (2000°F) oven for 60 seconds; after approximately 35 seconds the potting around the quartz glass lens ignited. At the end of the period the unit was removed and fire extinguished by smothering the flame. The flame sensor was connected to the CCU for the functional test. The Quartz lens was observed to have a slight residue coating. The flame sensor was de-energized and placed again in the oven for the second one-minute exposure. After 20 seconds the potting compound re-ignited and at 30 seconds the flame sensor cable ignited. After removal from the oven the flames were smothered and the unit tested. The flame sensor failed the first self test but upon reseting system reset normal operation was obtained. Although this time the quartz lens was heavily coated, it would still respond to open flame. Examination also showed that sensor tubes and source lamp were coated heavily from residue.

6.3.4 Vibration Test Reference Paragraph 4.4.2 of the TP

The test was conducted by Associated Testing Laboratory of Burlington, Mass. The vibration test was performed in accordance with paragraph 4.4.2 of the procedure. No problems were encountered with the sensor head or overheat cable. Initial problems were encountered with the CCU, MWU and CRU assemblies. Vibration and shock were successfully passed after incorporating external Barry shock isolators to all three units. The C.R.U. and C.C.U. also had several mechanical changes as a result of initial surveys which indicated

that mechanical strengthening would be necessary. The following is a summary of modifications made on the CRU:

1. Lamp regulator printed board open PC run--replaced with jumper wire--probable cause: defective etch covered by solder bridge.

2. Relay logic Board
   Wire jumper open, secured with RTV

3. Harness Cable, broken wires resoldered and secured.

The following modifications were made on the C.C.U.:

1. Capacitor on C/I board broke off--used Augot clamps instead of cable ties. Added buss jumpers to strengthen PC etch.

2. Transient suppressor--strengthen mounting by using heavier hardware.

3. Reconfigure mounting on filter choke. Add ribs to side wall to dampen resonances.

4. Add additional tie-downs to resistors on transient suppressor.

No modifications were made on the M.W.U.

6.3.5 Humidity Test Ref. TP 4.4.3

After removal of the system from the chamber the unit was turned on and was not functional due to a failure of the transient suppressor assembly in the CCU. The failure was electrical and not directly related to the humidity test. Cause of the failure was related to insufficient thickness of insulator bushings under zener diodes and tendency for diodes to creep causing them to short. One of the diodes had a cracked seal at the time of replacement.

There also appeared to be corrosion on the shield box for the R.F.I. filters which is cadmium plated. The "hair" observed is due probably to the fact that the choice of cadmium in a non-ventilated box was in the presence of RTV and other organic electrical substances. Cadmium is not recommended in QQ-P-416 this application and should be changed to tin plate per Mil-T-10727.

6.3.6 Salt Spray Test Ref. TP 4.4.4

Upon removal of Flame Sensor Head 44227 from the chamber the unit was tested and found to be non-operational. The fault was traced to a cracked UV tube and not related to salt spray. The tube failure was probably related to handling of the Flame Sensor assembly unit but cannot be confirmed. Examination of the Flame Sensor did not reveal any signs of salt water corrosion.

A Note on System #2

During a reliability test on System #2, the FIRE warning light came on for one second when no fire was present. Various considerations suggested this false alarm originated in U/V Detector Head 011. This head was changed to another input channel and testing resumed.

About 30 hours later, a second false FIRE warning occurred, this one apparently due to a power-line abnormality. In over 200 hours of further testing, no further false FIRE warnings have occurred.

DATA SHEETS

FOR USE WITH

"GENERAL TEST PLAN

FOR

SYSTEM PERFORMANCE TESTS

INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM"

System # 1 Date 2/23/76 Initials

		Test Satisfactory Yes	No
4.1.1			
	All lights out	✓	
	Lamp test - CRU	✓	
	Lamp test - MWU	✓	
4.1.2			
	"Fire" warning from head #1	✓	
	"Fire" warning from head #2	✓	
	"Fire" warning from head #3	✓	
	"Fire" warning from head #4	✓	
	"Fire" warning from head #5	✓	
	"Fire" warning from head #6	✓	
	Sensor 1 shielded, Sensor 2 exposed - head #1	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #1	✓	
	Sensor 1 shielded, Sensor 2 exposed - head #2	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #2	✓	
	Sensor 1 shielded, Sensor 2 exposed - head #3	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #3	✓	
	Sensor 1sshielded, Sensor 2 exposed - head #4	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #4	✓	
	Sensor 1 shielded, Sensor 2 exposed - head #5	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #5	✓	
	Sensor 1 shielded, Sensor 2 exposed - head #6	✓	
	Sensor 2 shielded, Sensor 1 exposed - head #6	✓	
4.1.3	Test source shielded - head #1	✓	
	Test source shielded, Tubes exposed - head #1	✓	
	Head #1 source shielded, head #2 exposed	✓	
	Head #1 source shielded, head #6 exposed	✓	
	Reset Button Pressed	✓	
	Test source shielded - head #2	✓	
	Test source shielded, tubes exposed - head #2	✓	
	Head #2 source shielded, head #3 exposed	✓	
	Head #2 source shielded, head #1 exposed	✓	
	Reset Button Pressed	✓	
	Test source shielded - head #3	✓	
	Test source shielded, tubes exposed - head #3	✓	
	Head #3 source shielded, head #4 exposed	✓	
	Head #3 source shielded, head #2 exposed	✓	
	Reset Button Pressed	✓	
	Test source shielded - head #4	✓	
	Test source shielded, tubes exposed - head #4	✓	
	Head #4 source shielded, head #5 exposed	✓	
	Head #4 source shielded, head #3 exposed	✓	
	Reset Button Pressed	✓	

System # 1 Date 2/23/76 Initials _____

4.1.3 (Continued)	Test Satisfactory Yes	No
Test source shielded - head #5	✓	
Test source shielded, tubes exposed - head #5	✓	
Head #5 source shielded, head #6 exposed	✓	
Head #5 source shielded, head #4 exposed	✓	
Reset Button Pressed	✓	
Test source shielded - head #6	✓	
Test source shielded, tubes exposed - head #6	✓	
Head #6 source shielded, head #1 exposed	✓	
Head #6 source shielded, head #5 exposed	✓	
Reset Button Pressed	✓	
4.1.4		
Source shielded in heads #1 & #2	✓	
Shields removed	✓	
Heads #3, #4, #5 & #6 exposed	✓	
Sources shielded on eads #2 & #3	✓	
Shields removed	✓	
Heads #1, #4, #5 & #6 exposed	✓	
Sources shielded in heads #3 & #4	✓	
Shields removed	✓	
Heads #1, #2, #5, & #6 exposed	✓	
Sources shielded in heads #4 & #5	✓	
Shields removed	✓	
Heads #1, #2, #3 & #6 exposed	✓	
Sources shielded in heads #5 & #6	✓	
Shields removed	✓	
Heads #1, #2, #3, & #4 exposed	✓	
Sources shielded in heads #6 & #1	✓	
Shields removed	✓	
Heads #2, #3, #4, & #5 exposed	✓	
4.1.5		
Cables A and B heated	✓	
Cable A disconnected, both cables heated	✓	
Cable A reconnected, Cable B disconnected, Reset	✓	
Cables A and B heated	✓	
Cable B reconnected, reset button pushed	✓	
Cables A and B heated	✓	

System # 1 Date 2/23/76, 3/9/76 Initials _____

	Test Satisfactory Yes	No
4.1.6		
Cables A and B disconnected at J12, J14	✓	
Cables A and B heated	✓	
Cables A and B reconnected, reset button pushed	✓	
4.1.7		
Cable A disconnected at J12 and shorted	✓	
Cable B disconnected at J14 and shorted	✓	
Cables A and B reconnected, reset button pushed	✓	
4.1.8		
Power to Computer Control Unit turned off	✓	
4.1.9		
Head #1, Cable A disconnected	✓	
Power reapplied after three (3) hours	✓	

4.2.1

Measured alarm temperature 406.1°C (763°F)

4.2.2

Input Power = 24 volts

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		140 ms		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	
"Fire" on within 1.5 seconds	✓		✓		✓		✓		✓		✓	

Input Power = 30 volts

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		40 ms		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	
"Fire" out within 1.5 seconds	✓		✓		✓		✓		✓		✓	

* Y = Yes, N = No

System # 1 Date 3/10/76 Initials _____

4.2.2 (Continued)

Input Power = 18 volts

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		✓		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	
"Fire" out within 1.5 seconds	✓		✓		✓		✓		✓		✓	

4.2.3

Horizontal planes - 40° off center

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		✓		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	

Vertical planes - 40° off center

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		✓		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	

4.2.4

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
*	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
Burning fuel (pure)	✓		✓		✓		✓		✓		✓	
Burning fuel & hydraulic fluid	✓		✓		✓		✓		✓		✓	

* Y = Yes, N = No

System # 1 Date 3/11/76 Initials _____

4.2.5

Input Power = 24 volts

Alarm time: 6 (3)
Clear time: 7

Input Power = 30 volts

Alarm time: 6 (3)
Clear time: 7

Input Power = 18 volts

Alarm time: 6 (3)
Clear time: 7

4.2.6

Alarm time: 8 Sec.

4.2.7

Alarm time after reapplied flame: 3 Sec.

4.2.8

Is 50% masking test satisfactory? Yes
Clear time after flame removal 4 Sec.

4.2.9

Alarm times: 7 (4) 4 4 sec.
Clear times: 7 7 7 sec.

4.2.10

	Test Satisfactory? Yes	No
Cables disconnected	✓	
End fittings immersed	✓	
Cables reconnected, reset button pushed	✓	

System # 1 Date 3/17/76 Initials _____

	Tests Satisfactory? Yes	No
4.3.1 Electromagnetic interference tests	See Report	
4.3.2 Entire system at 71.1°C (160°F)		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	
CCU, heads and cables at 82.2°C (180°F)		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	

Measured alarm temperature 392.2°C (738°F)

Detector Heads at 260°C (500°F)

3/22/76

*	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		✓		✓		✓		✓	
One-half of flame blocked	✓		✓		✓		✓		✓		✓	
"Fire" out within 1.5 seconds	✓		✓		✓		✓		✓		✓	

Is false alarm test satisfactory? Yes

* Y = Yes, N = No

System # 1 Date 3/23/76 Initials _____

4.3.3

	Test Satisfactory? Yes	No
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	

Measured alarm temperature 404.4°C (760°F)

	Head #1		Head #2		Head #3		Head #4		Head #5		Head #6	
	Test Satisfactory?											
	Y	N	Y	N	Y	N	Y	N	Y	N	Y	N
"Fire" on within .5 second	✓		✓		✓		✓		✓			
One-half of flame blocked	✓		✓		✓		✓		✓			
"Fire" out within 1.5 seconds	✓		✓		✓		✓		✓			

Is false alarm test satisfactory? Yes

4.3.4

	Test Satisfactory? Yes	No
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	OK	

4.3.5

Response to ultraviolet radiation	✓	
False alarm test	OK	

* Y = Yes, N = No

System # 1 Date 4/29/76 Initials _____

	Test Satisfactory? Yes	No
4.3.6		
-40°C, 70000 ft.		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	
Room temperature, pressure		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	OK	
4.4.1		
After -40°C (-40°F)/71.1°C (160°F) Temperature shock		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	
After -53.8°C (-65°F)/300°C (572°F) detector head shock		
Response to ultraviolet exposure	✓	

System # 1 Date 4/29/76 Initials _____

	Test Satisfactory? Yes	No
4.4.2 Post Vibration		
Response to ultraviolet - Head #1	✓	
Response to ultraviolet - Head #2	✓	
Response to ultraviolet - Head #3	✓	
Response to ultraviolet - Head #4	✓	
Response to ultraviolet - Head #5	✓	
Response to ultraviolet - Head #6	✓	
Response to overheat condition	✓	
4.4.3		
Response to ultraviolet, overheat conditions	✓	
4.4.4		
Response to ultraviolet, overheat immediately after	✓	
Response to ultraviolet, overheat after 48 hours storage	✓	

Test Report No. T-3884-11 No. of Pages 31

Report of Test on

INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM

ENVIRONMENTAL TESTING

for

EDISON ELECTRONICS

Associated Testing Laboratories, Inc.

Date May 24, 1976

	Prepared	Checked	Approved
By	R. Goddard	E. Mencow	E. Kulcsar
Signed	R Goddard	Ed Mencow	E. Kulcsar
Date	5/25/76	5/25/76	5-26 76

Administrative Data

1.0 Purpose of Test:

To determine the ability of the submitted Integrated Fire and Overheat Protection System to comply with the requirements of the test specified in the Procedures of this report.

2.0 Manufacturer: Edison Electronics Division
McGraw Edison Company
Grenier Field
Manchester, New Hampshire 03103

3.0 Manufacturer's Type or Model No.:

4.0 Drawing, Specification or Exhibit: Edison Electronics General Test Plan, Dated May 15, 1972, revised Report Number 59377-1, June 10, 1975 and December 11, 1975.

5.0 Quantity of Items Tested: One (1) System

6.0 Security Classification of Items: Unclassified

7.0 Date Test Completed: May 11, 1976

8.0 Test Conducted By: **Associated Testing Laboratories, Inc.**

9.0 Disposition of Specimens: Returned to Edison Electronics Division Of McGraw-Edison Company.

10.0 Abstract:

The submitted Integrated Fire and Overheat Protection System was subjected to Environmental Testing in accordance with the above procedures. The System successfully completed the Environmental Test specified.

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Clifton, New Jersey 07012
Burlington, Massachusetts 01803

GENERAL INFORMATION

The Vibration and Shock Tests were performed on the following:

One (1) - C R U (Crew Readout Unit).
One (1) - C C U (Computer Control Unit).
One (1) - Detector Head.
One (1) - Heat Detector Cable.
One (1) - M W U (Maintenance Warning Unit).

The Altitude Test was performed on the entire system consisting of the following:

One (1) - C R U (Crew Readout Unit).
One (1) - C C U (Computer Control Unit).
One (1) - M W U (Maintenance Warning Unit).
Six (6) - Ultraviolet Detector Heads
One (1) - Dual Overheat Cable Loop

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Burlington, Massachusetts 01803

LIST OF APPARATUS

ITEM	MANUFACTURER	MODEL NO.	ACCURACY	CALIBRATION DATE	CALIBRATION DUE DATE
Vibration System	Ling Electronics	335	N/A	3/17/76	6/17/76
Sinusoidal Vibration Control System	Spectral Dynamics	----	F±2% A±5%	3/6/76	6/6/76
High Frequency Equalizer	Associated Testing Laboratories, Inc.	ATL2-4/c	±5%	1/12/76	4/12/76
Vibration Meter	MB Electronics	M3	N/A	N/A	N/A
Vibration Pickup	MB Manufacturing	115	±10%	1/23/75	Before Use
Sinusoidal Vibration Control System	Spectral Dynamics	----	F±2% A±5%	3/9/76	6/9/76
Accelerometer	Endevco Corp.	2271A	±5%	1/12/76	4/12/76
Charge Amplifier	Unholtz-Dickie	11MS	±1% output	3/17/76	6/17/76
Accelerometer	Endevco Corp.	2215E	±5%	2/23/76	5/23/76
Temperature Altitude Chamber	Associated Testing Laboratories, Inc.	LHA-27-CR-LC	±2°F	3/30/76	5/30/76
Vibration Control System	Hewlett-Packard	5425	F±2% A±5%	Before Use	

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ALTITUDE TEST

TEST PROCEDURE

The Complete System was subjected to an Altitude Test in accordance with Edison Electronics General Test Plan as follows:

The System was placed within an Altitude Chamber which was then sealed. A functional check was then performed at a standby. The Chamber temperature was decreased to -40°F and stabilized for one hour. The internal pressure was simultaneously reduced to simulate an altitude of 70,000 feet (33.59mm).

Following one hour of stabilization, and while still at the required test parameters, an operational check was performed. The pressure and temperature were then reduced gradually to room ambient and the system was again checked for normal operation.

TEST RESULTS

There was no evidence of any physical damage following the test. The System functioned satisfactorily during and following the exposure as reported by a representative of Edison Electronics.

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VIBRATION TEST

TEST PROCEDURE

The individual system components as listed in the Abstract were subjected to a Sinusoidal Vibration Test in accordance with MIL-STD-810B, Procedure I, Curve Z, Parts 1, 2, and 3 and Time Schedule I. The following is a description of the test as it was performed.

The System Components were individually mounted to vibration test fixtures. The test fixture was then securely attached to the table of a vibration exciter. A control accelerometer for monitoring and controlling the input vibration amplitude was mounted on the test fixture near the specimen mounting points. A monitor accelerometer was utilized in conjunction with an "X-Y" plotter to determine the presence of resonant frequencies.

The System Components were then subjected to a Vibration Test. The Vibration Test was performed at room ambient temperature.

A resonance survey of the Components along each orthogonal axis was made. The frequency range from 5 to 500 Hz was performed at reduced levels.

During the frequency sweep from 5 to 500 Hz, the output of the monitor accelerometer probe was monitored in order to determine the presence of resonant frequencies. A resonant frequency was defined as a frequency at which the ratio of the output of the monitor accelerometer to the input vibration amplitude was 2 or greater. Each resonance was recorded.

Each component was then subjected to Sinusoidal Vibration along the same orthogonal axis over the frequency range of 5 to 500 Hz. The range from 5 to 500 Hz and back to 5 Hz was traversed at a logarithmic rate in approximately 15 minutes (0.26 decades/minute). The input vibration amplitudes are given below:

VIBRATION TEST

TEST PROCEDURE (continued)

Frequency (Hz)	Input Vibration Amplitude
5 - 14	0.1 inch d.a.
14 - 23	±1g
23 - 90	0.036 inch d.a.
90 - 500	±15g's

The total cycling time was determined from the table given below:

CYCLING AND DWELL APPORTIONMENT

Number of Resonances	0	1	2	3	4
Total Dwell Time in Minutes at Resonant Points	0	30	60	90	120
Total Cycling Time in Minutes	180	150	120	90	60

The Components were vibrated along the same orthogonal axis at the resonant frequencies which were determined during the resonance survey. Vibration was for 30 minutes at each resonant point. If more than four resonant points were noted from the resonant survey, only the four most severe were used for resonance vibration.

The above procedure was performed in each of the Components three orthogonal axes. At the conclusion of vibration in each axis, each unit was examined for any signs of damage.

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VIBRATION TEST

TEST RESULTS

Each individual System Component tested successfully completed 3 hours of vibration per axis with no physical damage.

Refer to Appendix for resonant search data.

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SHOCK TEST

TEST PROCEDURE

The Individual System Components were subjected to a shock test in accordance with Edison Electronics General Test Plan, as follows:

The units were individually mounted to the shock machine. The shock machine was previously calibrated to produce a shock pulse of 20g peak amplitude and 11 milliseconds time duration. The shock pulse wave form approximated that of a sawtooth. Each component was subjected to a total of 18 blows, three in each direction of three mutually perpendicular axes.

Following the test, the units were removed from the fixture and examined for damage. The System was then checked for normal operation.

TEST RESULTS

The System Components all satisfactorily completed the shock test with no physical damage noted. The System operated satisfactorily following the test as reported by the Edison Electronics representative.

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A P P E N D I X

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10g input
shock mounted

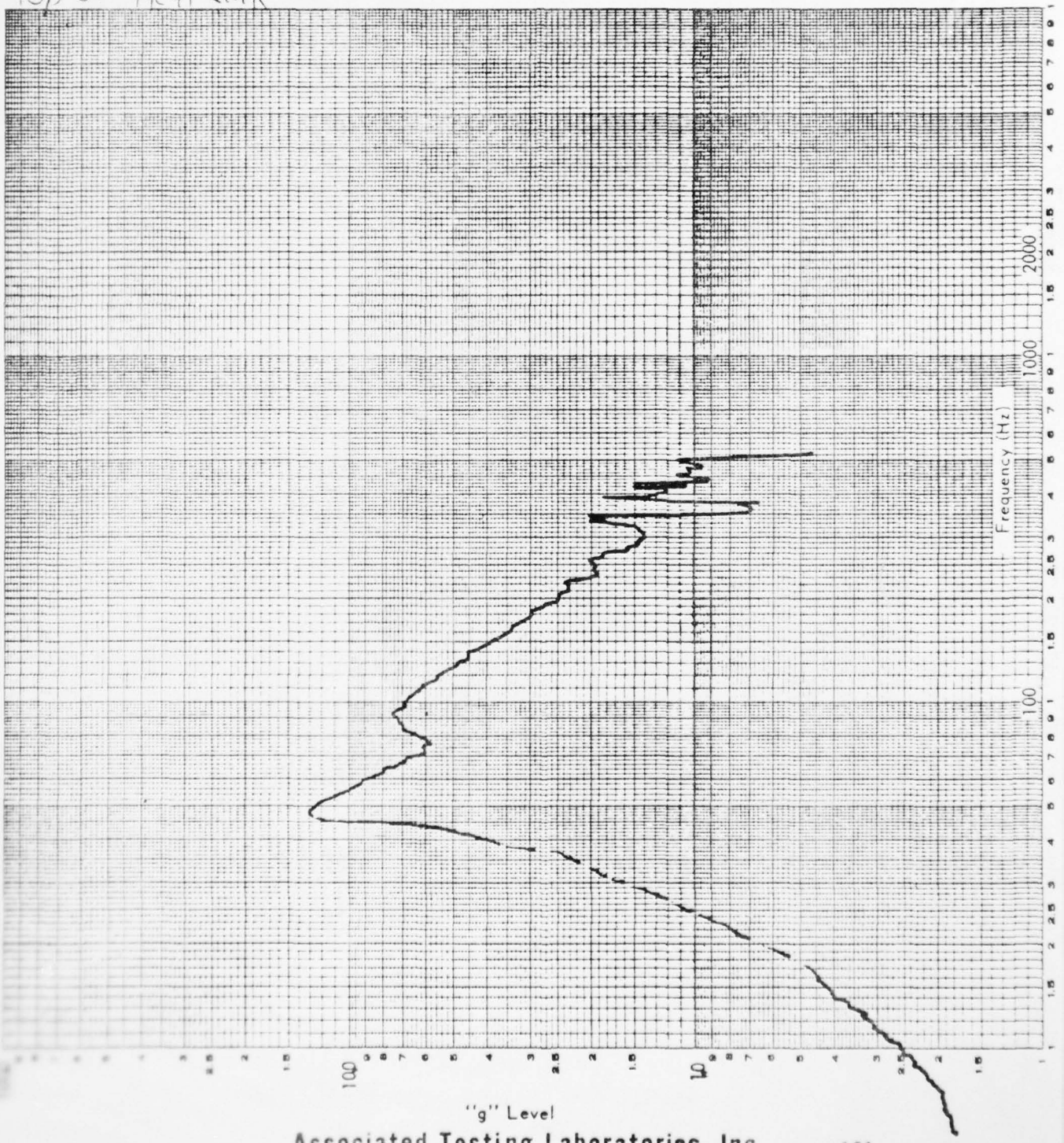
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-388f Customer EDISON Date 4/15/26

Specimen P/N CRU Specimen S/N _____ Test Temp. RM

Axis Vertical Technician RG

Top of Heatsink



VIBIGRAPH MADE IN U.S.A.

NO. 187 L33 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

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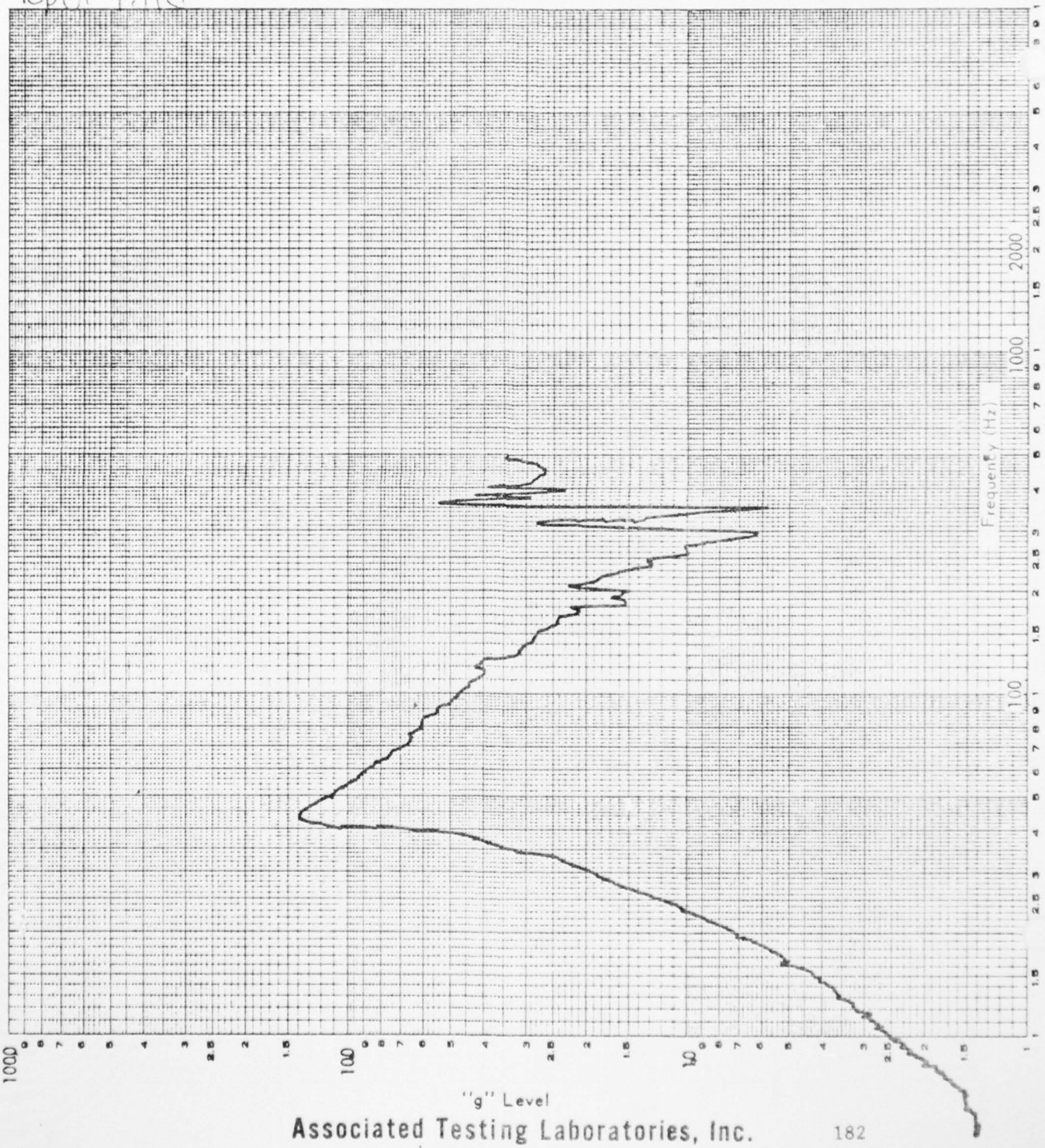
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edson Date 4/9/16

Specimen P/N CRU Specimen S/N _____ Test Temp. RM

Axis vert. (Z) Technician RG

Top of filter



VISIGRAPH MADE IN U.S.A.

NO 197 L33 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

Associated Testing Laboratories, Inc. 182

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Burlington, Massachusetts 01803

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shock mounted

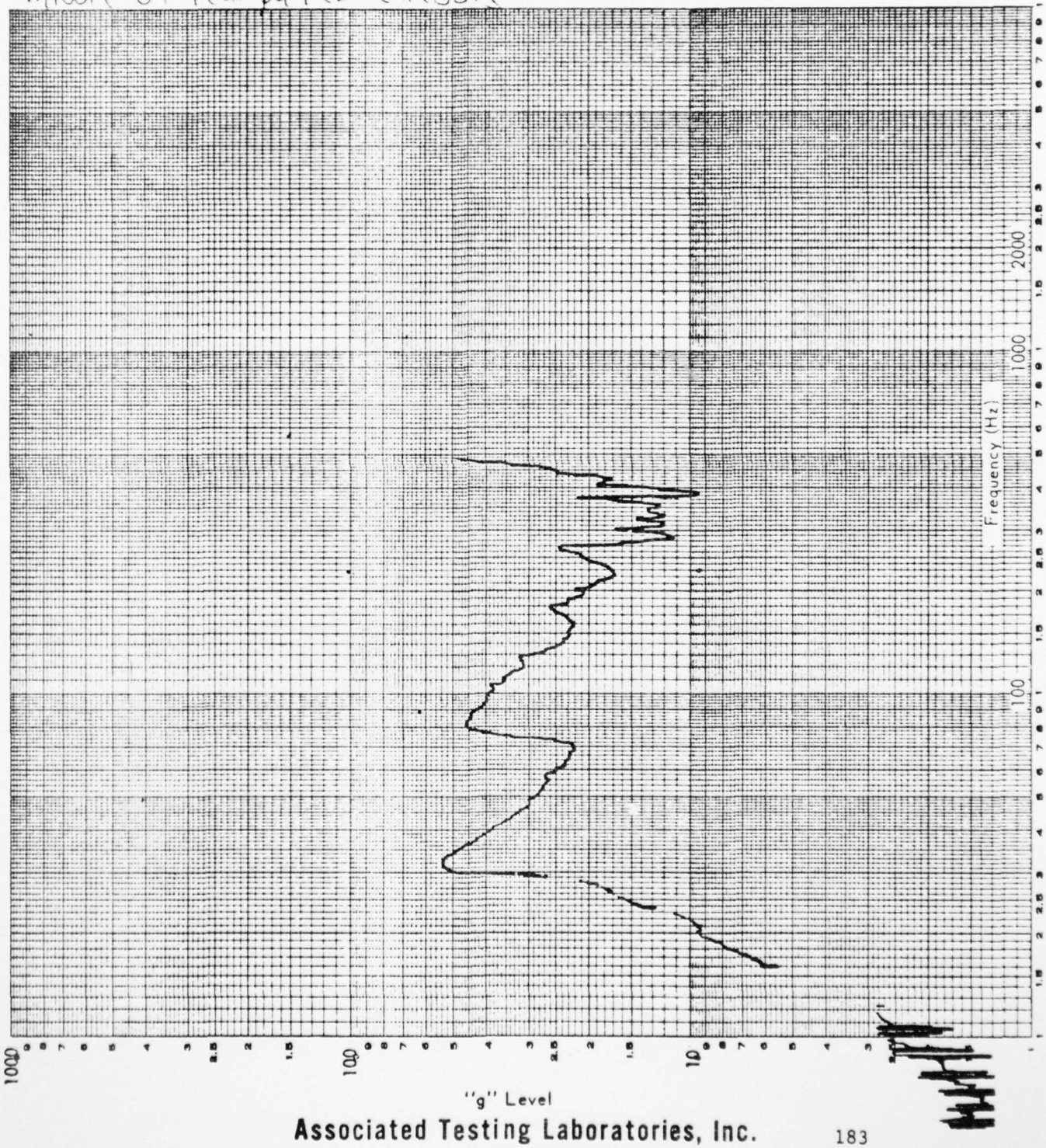
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/9/76

Specimen P/N CRU Specimen S/N _____ Test Temp. RM

Axis major thr zontal Technician RG

middle of rear panel chassis



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NO 15T L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

Associated Testing Laboratories, Inc.

Clifton, New Jersey 07012

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shock mounted
new fixture

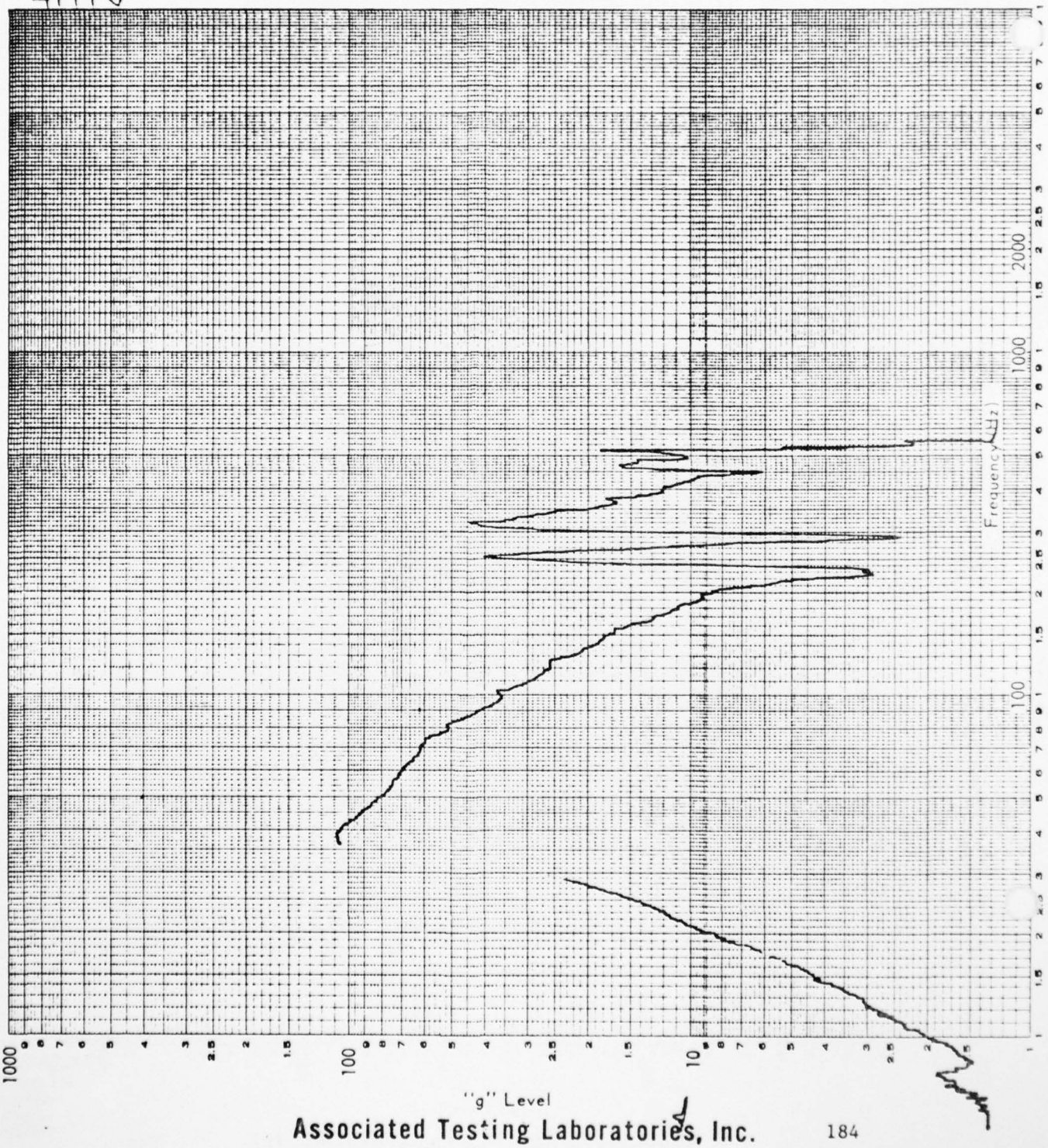
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-388C Customer Edison Date 4/7/86

Specimen P/N MWU Specimen S/N _____ Test Temp. RM

Axis vertical Technician RG

filter



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NO 197 L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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10g input
shock mounted
new fixture

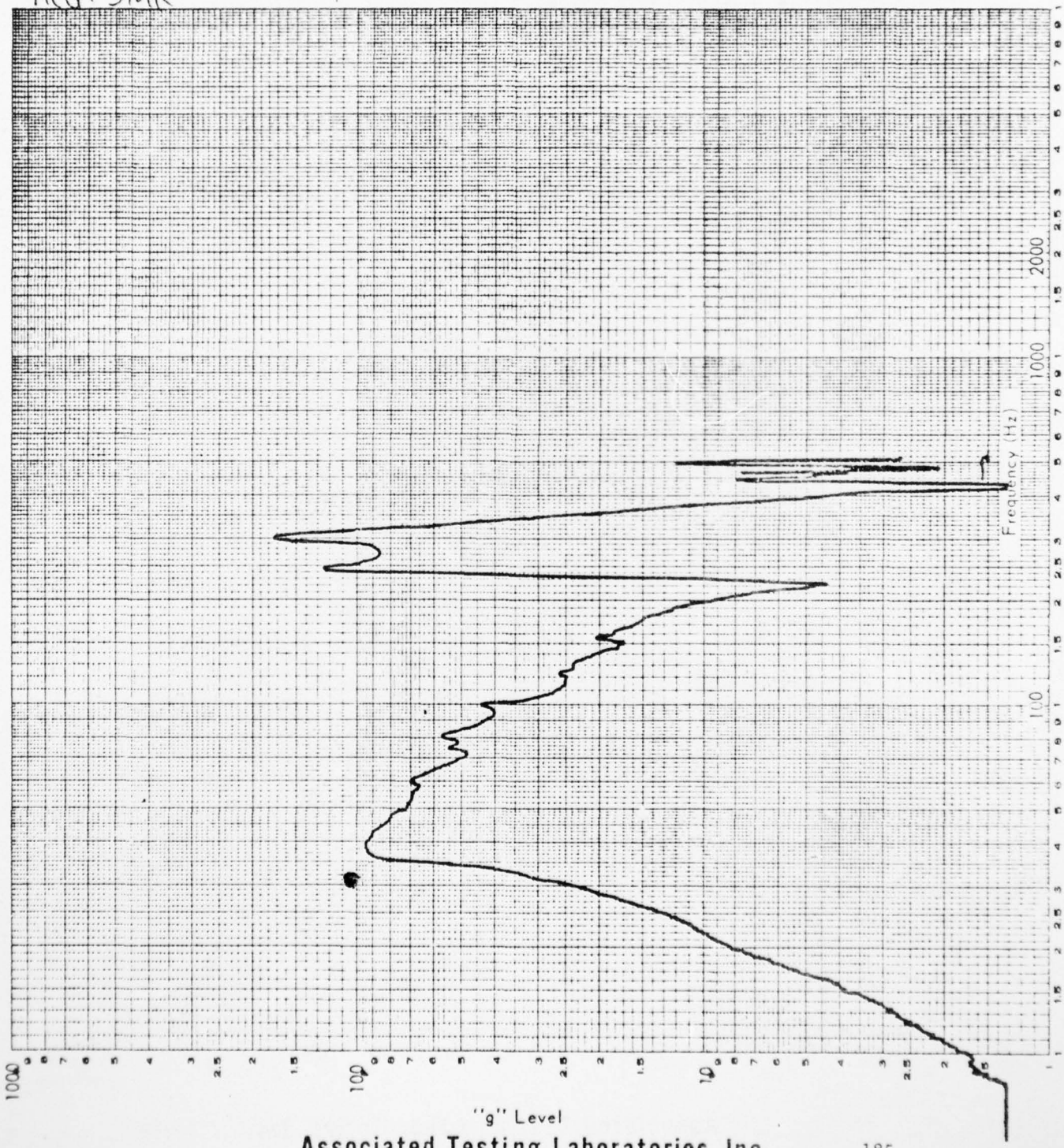
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3854 Customer EDISON Date 4/7/76

Specimen P/N MW4 Specimen S/N _____ Test Temp. RM

Axis Vertical Technician RG

heat sink



VISIGRAPH® MADE IN U.S.A.

NO 1ST 333 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

0 g input
shock mounted
new fixture

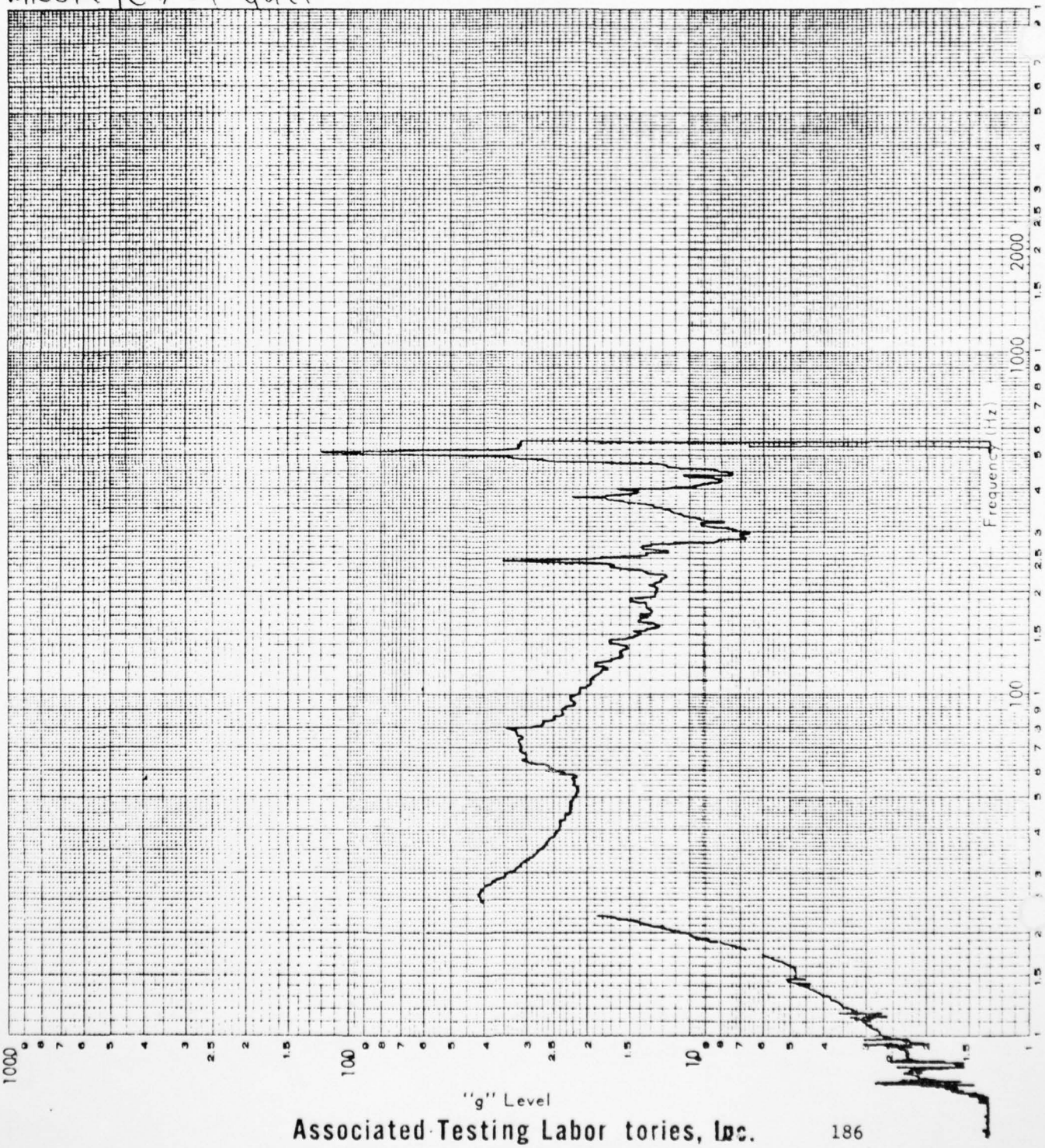
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/7/76

Specimen P/N MWU Specimen S/N _____ Test Temp. RM

Axis Major horizontal Technician RG

middle rear of unit



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NO 1ST L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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T-3884-11

shock mounted
New fixture

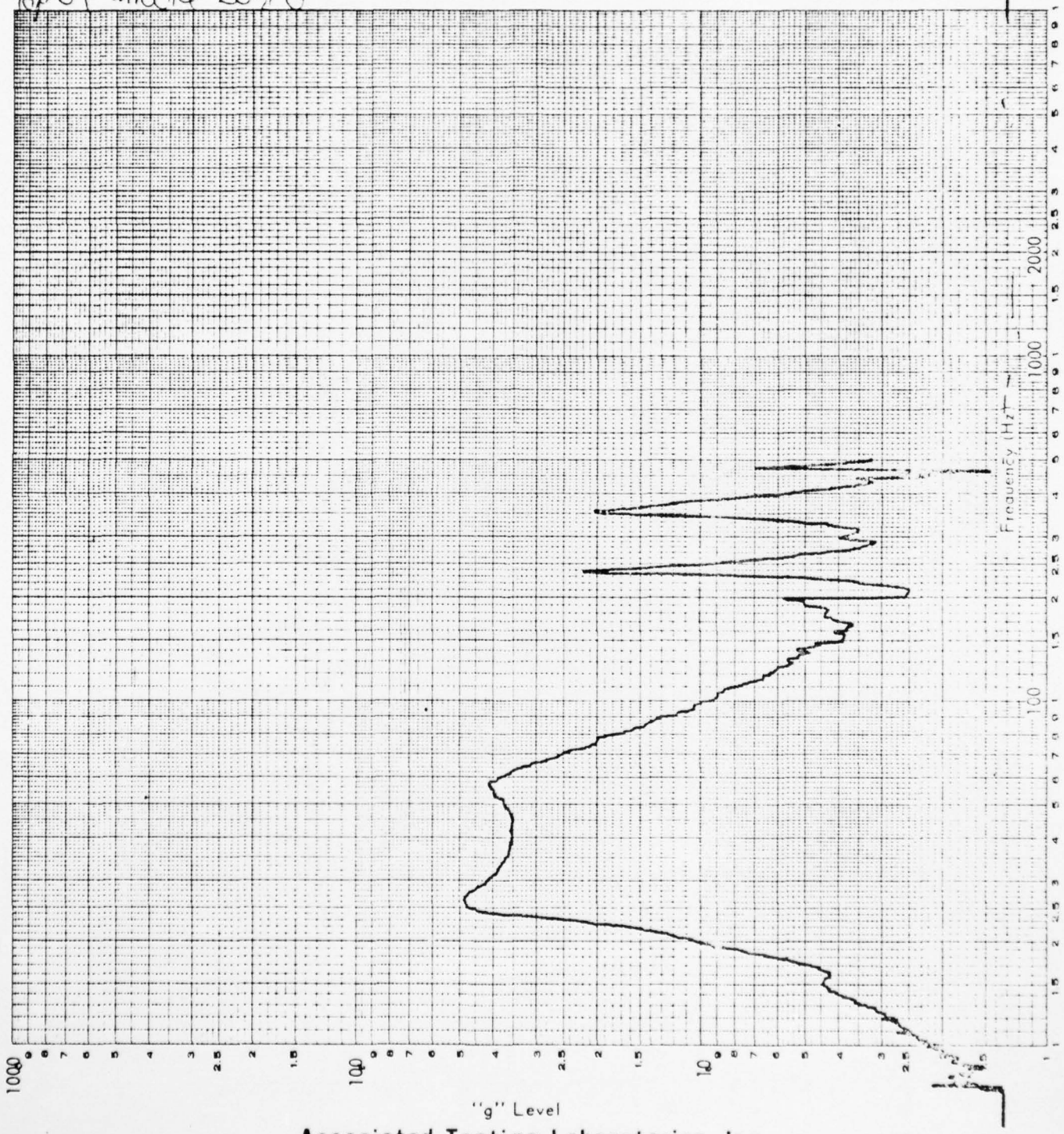
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/1/86

Specimen P/N MW4 Specimen S/N _____ Test Temp. RM

Axis Major Horizontal Technician QC

Top of middle board



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NO 15T L33 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

10g input
shock isolator mounted

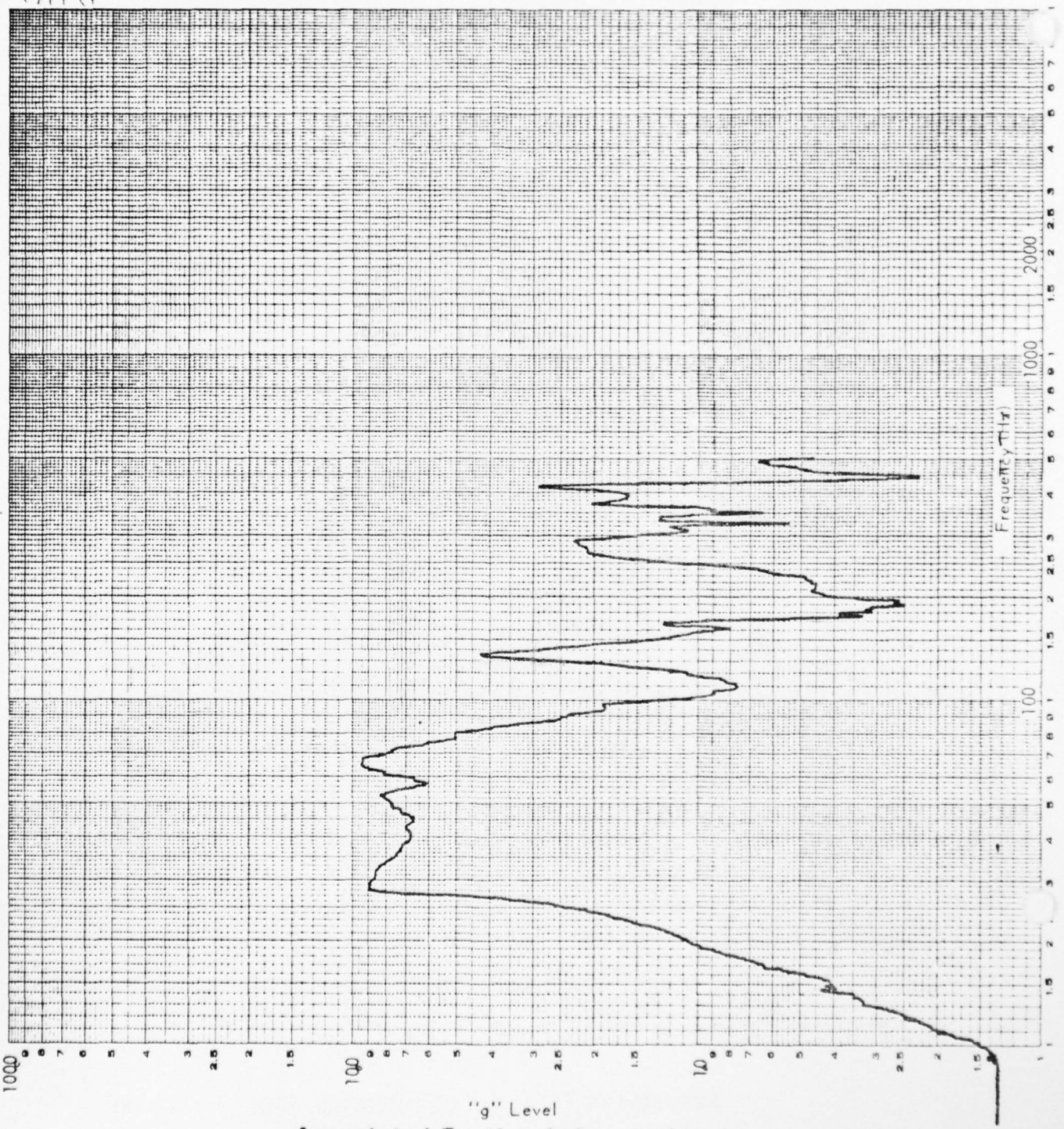
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/5/76

Specimen P/N CCU Specimen S/N _____ Test Temp. RM

Axis vertical Technician RG

filter



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NO 15T L33 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

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10g input
Shock Isolator mounted

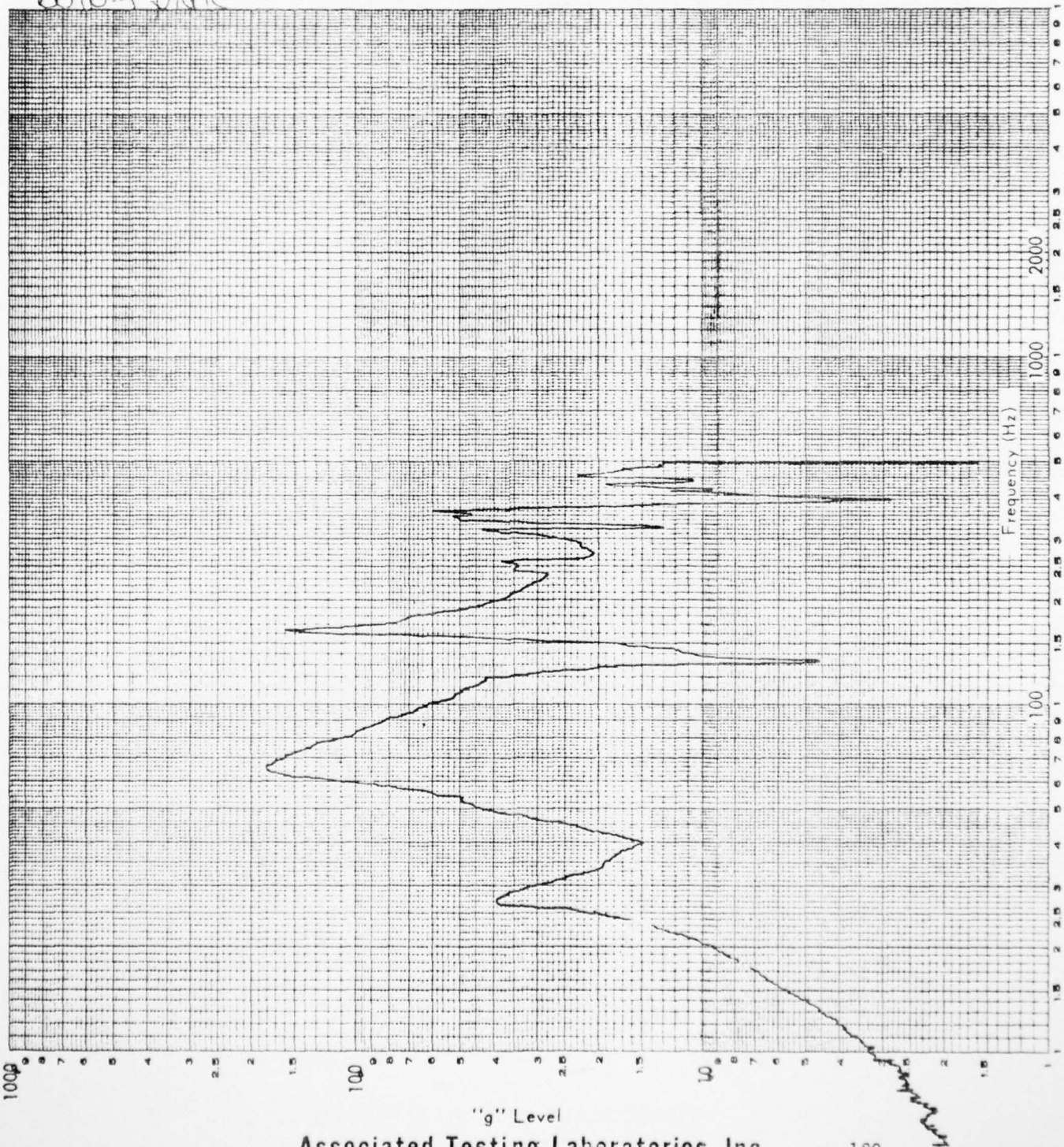
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/5/16

Specimen P/N CCU Specimen S/N _____ Test Temp. RM

Axis Vertical Technician RG

bottom plate



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NO 157 L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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10g sprial
shock mounted

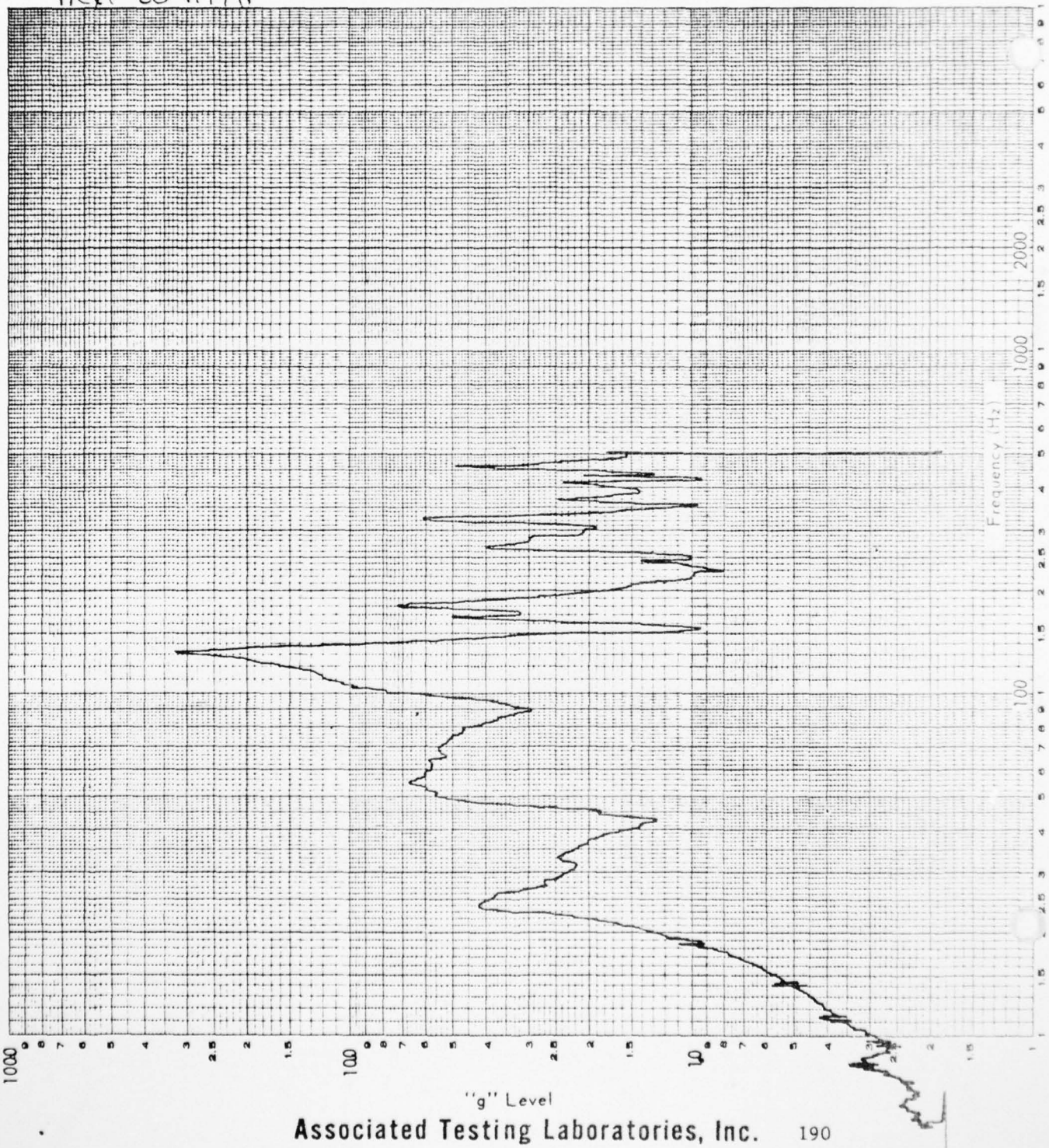
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-7884 Customer Edson Date 4/5/16

Specimen P/N CCU Specimen S/N _____ Test Temp. RM

Axis minor Horizontal Technician RG

next to filter



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NO 15T L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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10g input
Shock Mounted

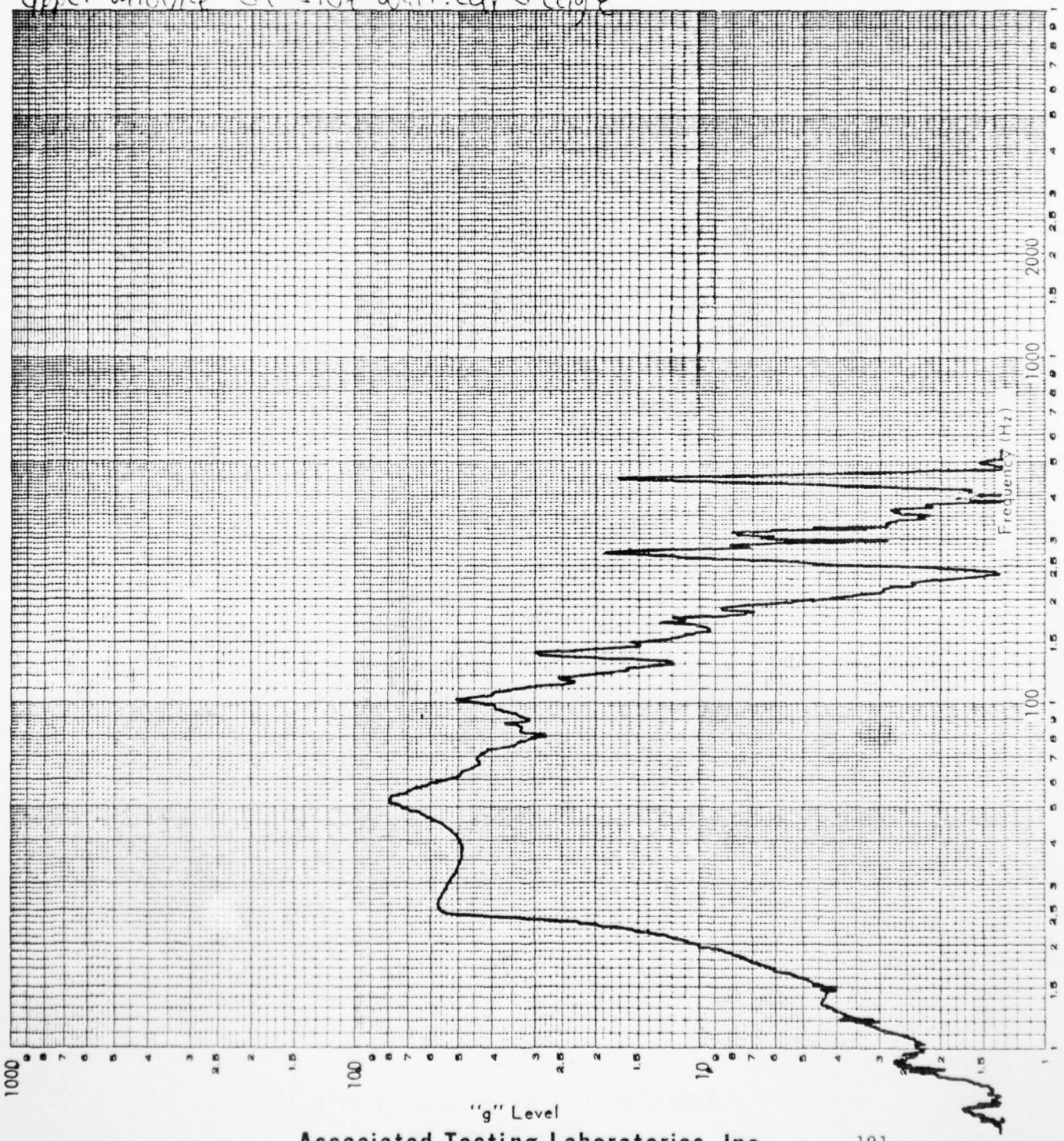
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/5/26

Specimen P/N CCU Specimen S/N _____ Test Temp. RM

Axis Minor Horizontal Technician RG

Upper middle of side wall Card cage



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NO 15T - L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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Burlington, Massachusetts 01803

1g input
rock mounted

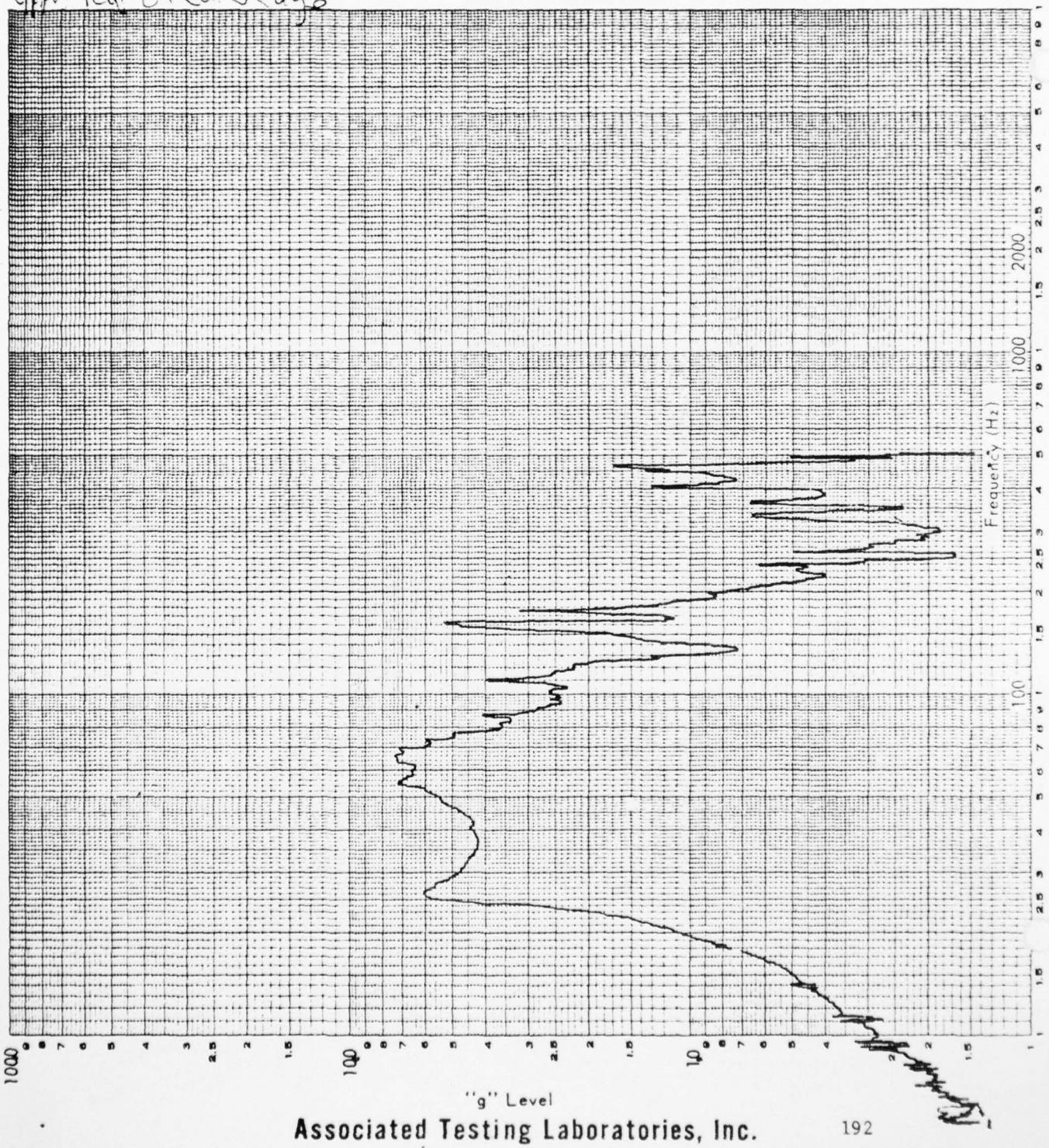
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-5884 Customer EDISON Date 4/6/16

Specimen P/N CCG Specimen S/N _____ Test Temp. RM

Axis Major Horizontal Technician QC

upper rear of card cage



VISIGRAPH MADE IN U.S.A.

NO 15T L33 GRAPH PAPER LOGARITHMIC 3 CYCLES X 3 CYCLES

10g input
shock mounted

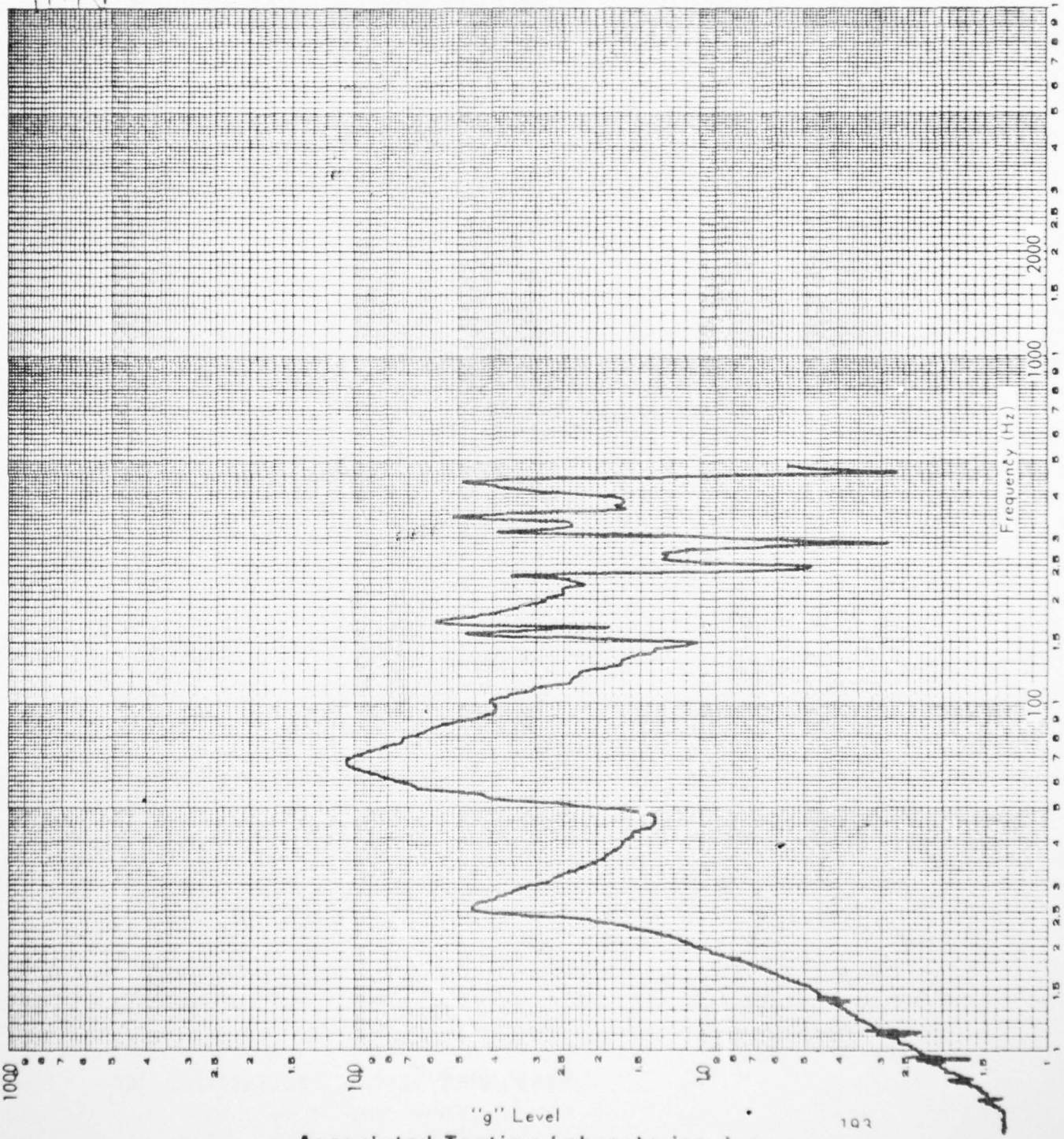
SINUSOIDAL VIBRATION ANALYSIS

Job Number T-3884 Customer Edison Date 4/6/16

Specimen P/N CCU Specimen S/N _____ Test Temp. Rm

Axis Major Axis Technician RG

filter



VIBROGRAPH MADE IN U.S.A.

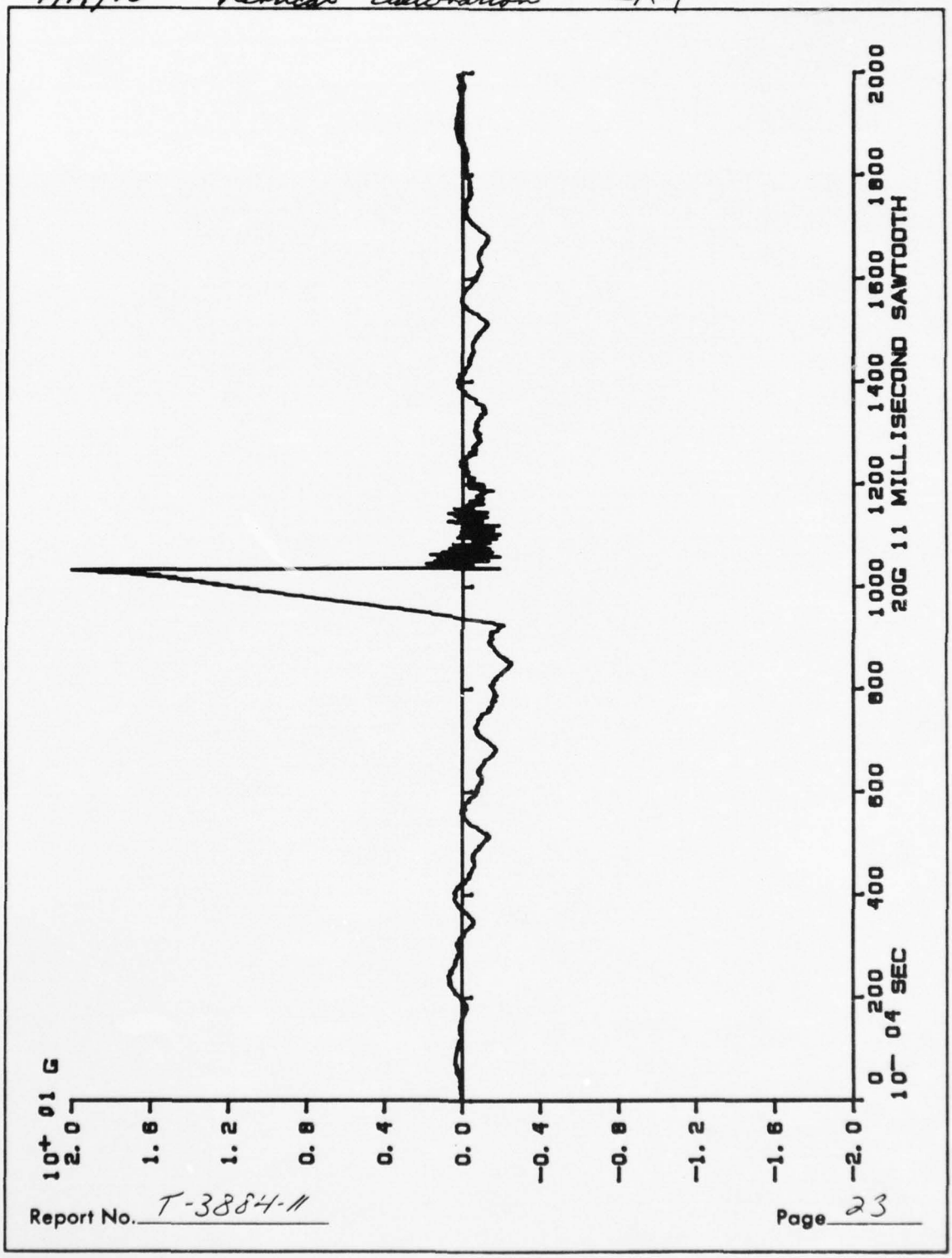
NO 197 - L33 GRAPH PAPER
LOGARITHMIC
3 CYCLES X 3 CYCLES

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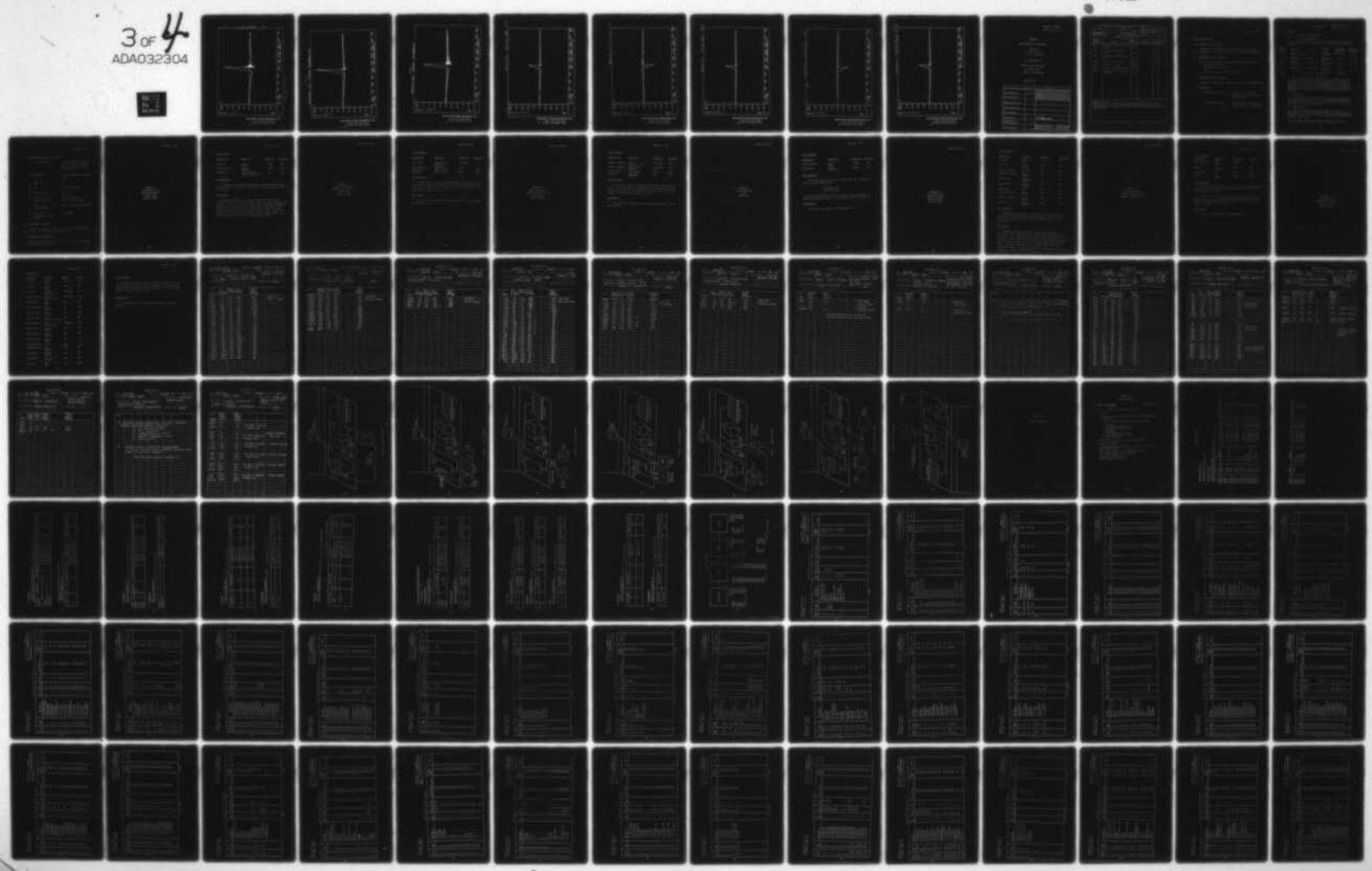
4/19/76 Vertical Calibration CRY



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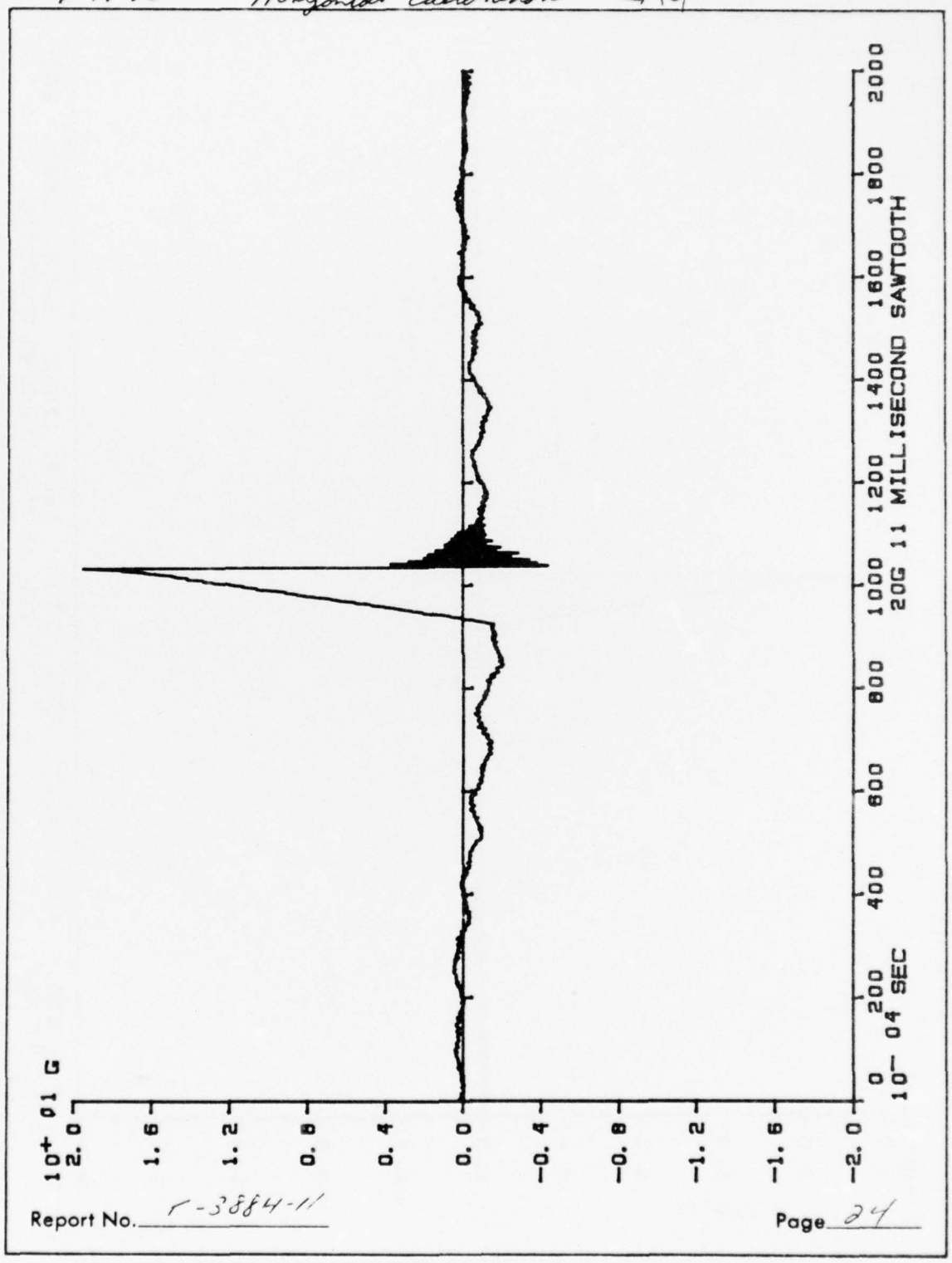
AD-A032 304 MCGRAW-EDISON CO MANCHESTER N H EDISON ELECTRONICS DIV F/G 1/4
INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM.(U)
JUN 76 G SUMINSKI, O RIEMER, F HANKEY F33615-72-C-1053
UNCLASSIFIED AFAPL-TR-76-64 NL

3 OF 4
ADA032304




OF
323O4

4-19-76 Horizontal Calibration CRU



Report No. F-3884-11

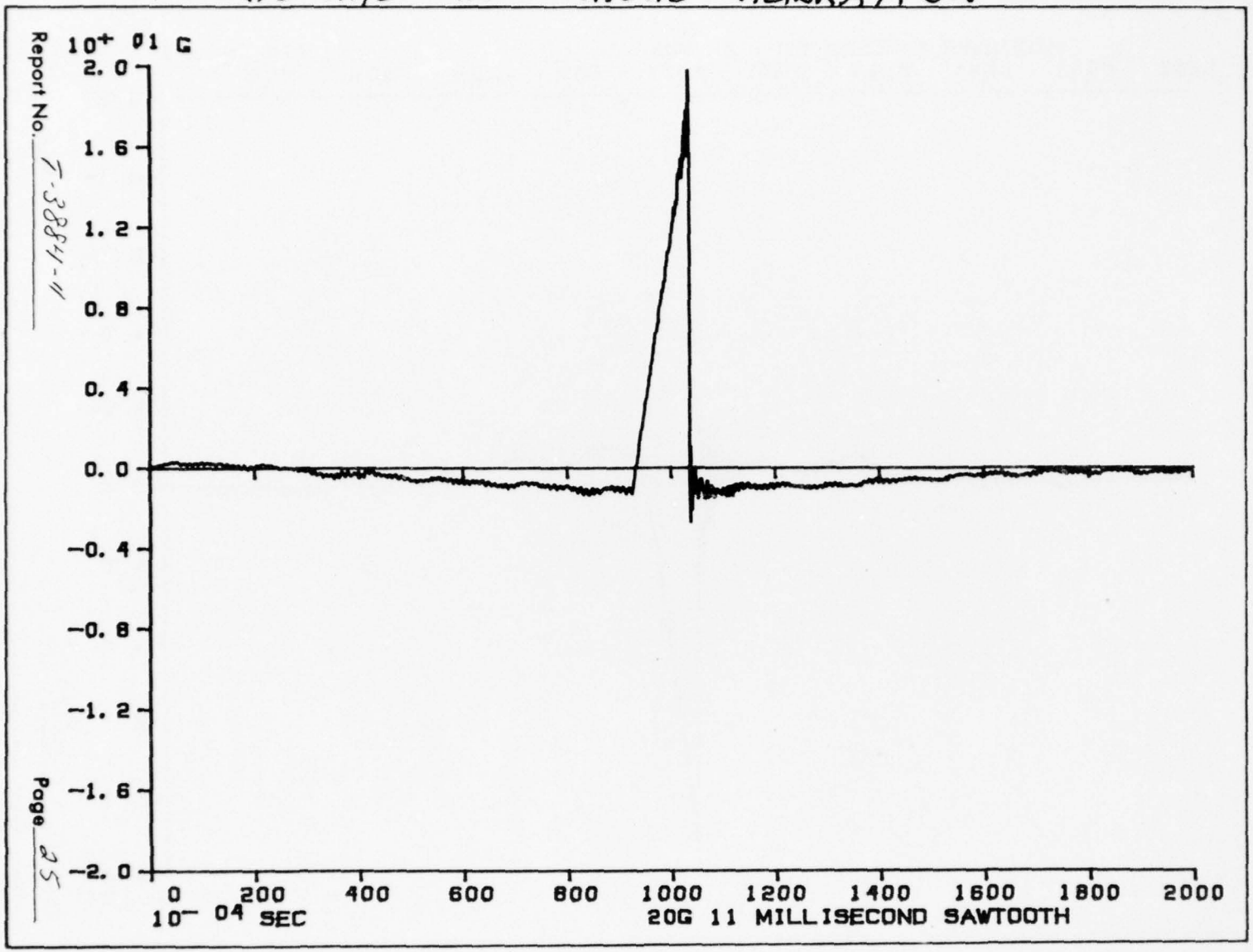
Page 24

Horizontal Axes

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CCU

HORIZONTAL AXIS FIXTURE CALIBRATION



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CCU

VERTICAL AXIS FIXTURE CALIBRATION

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horizontal Detector Cable 4/1/76

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198 Burlington, Massachusetts 01803

Vertical Detector cable 4/1/76

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Clifton, New Jersey 07012
Burlington, Massachusetts 01803

Pos. Vertical Detector Head 2/1/26
10+ 01 G
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
0
200
400
600
800
1000
1200
1400
1600
1800
2000
10-- 04 SEC
20G 11 MILLISECOND SAWTOOTH
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Page 29

neg. vertical detector head 4/1/76

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Associated Testing Laboratories, Inc.
Clifton, New Jersey 07012
201 Burlington, Massachusetts 01803

Associated Testing Laboratories, Inc.

Clifton, New Jersey 07012
Burlington, Massachusetts 01803

Report No. 2439

Revision _____

REPORT OF

ELECTROMAGNETIC INTERFERENCE

TEST ON

MC GRAW EDISON CO.

I. F. O. EQUIPMENT

TEST PERFORMED BY

SANDERS ASSOCIATES, INC.

95 CANAL STREET

NASHUA, NEW HAMPSHIRE

CONTRACT NO.

	DATE	SIGNATURE
TEST INITIATED	5/5/76	
TEST COMPLETED		
REPORT WRITTEN BY		
TEST TECHNICIAN		
TEST ENGINEER		
SUPERVISOR		R. Lawson
GOVERNMENT REP. (If Applicable)		
FINAL RELEASE		

ELECTROMAGNETIC INTERFERENCE REPORT TEST SUMMARY SHEET

TEST ITEM: ONE I.F.O. SN 1	REPORT NO. 2439	DATE TEST COMPL. 5/7/76
		DATE REPT. COMPL.
MANUFACTURER: MC GRAW EDISON	SPECIFICATION MIL-STD-461A Notice 3	

SUMMARY OF TEST RESULTS

TEST METHOD	TITLE	SPEC. PARA.	REMARKS	PASS	FAIL
CE03	20 KHz to 50 MHz, Power Leads	6.2			X
CS01	30Hz to 50KHz, Power Leads	6.4		X	
CS02	50KHz to 400MHz, Power Leads	6.5		X	
CS06	Spike, Power Leads	6.9		X	
RE02	9.5KHz to 10GHz	6.12			X
RS02	Magnetic Induction Field	6.18		X	
RS03	14KHz to 10GHz Electric Field	6.19			

SUMMARY OF REPORT: CE03: Worst case BB emission exceeds limit by 32dB. Worst case NB emission exceeds limit by 26dB. RE02: Worst case BB emission exceeds limit by 12dB. Worst case NB emission exceeds limit by 21dB.

1.0 ADMINISTRATIVE DATA

1.1 Purpose/Reason for Test

To determine if McGraw-Edison, IFO Equipment complies with the requirements of MIL-STD-461A, Notice 3, for Class 1A equipment.

1.2 Description of Test Sample

The IFO equipment tested consisted of the following units:

Crew Read-out Unit
Maintenance Warning Unit
C.C.U.
6 ea U.V. Detectors (Flame Sensors)

1.3 Disposition of Test Sample

Equipment was returned by McGraw Edison by their representative.

1.4 References

MIL-STD-461A, Notice 3	Electronics Interference Characteristics Requirements for Equipment.
MIL-STD-462, Notice 2	Electromagnetic Interference Characteristics, Measurement of

2.0 GENERAL

2.1 1. Accuracy of Measurements

2.1.1 Field Intensity Meters

The principle means of determining frequency and amplitude during the test was one or more of the following field intensity meters:

Check If Used	Model No.	Mfr.	Frequency Range	Frequency Accuracy	Amplitude Accuracy
☐	EMC-10 Calibrated every	Fairchild	20Hz-50kHz months	±(1/2% + 5Hz)	±1/2 dB
☐	EMC-25 Calibrated every	Fairchild	14kHz-1GHz 12 months	±2%	±1.5 dB
☐	EMA-910 Calibrated every	Singer/Empire	1GHz-26.5GHz 12 months	±1/2%	±2 dB
☐	NF-105 Basic Unit	Singer/Empire	14kHz-1GHz 12 months	±2%	±1 dB
☐	TX - 12 Months ☐ TA - 12 Months ☐ T1 - 12 Months				
☐	T2 - 12 Months ☐ T3 - 12 Months				

These instruments were calibrated by the Sanders Associates Instrumentation Calibration/Standards Laboratory, which operates a government approved calibration program in accordance with MIL-C-45662A, "Calibration System Requirements". The calibrating equipment accuracy required by MIL-C-45662A is several orders of magnitude greater than that of the EMC instrumentation listed above. This ensures the greatest possible frequency and amplitude data accuracy.

2.2 Transducers

All antennas--(with one exception)--and current probes use the correction factors supplied by their respective manufacturers. The single exception is the Empire VA-105 41-inch vertical rod antenna (150kHz to 30MHz) which is calibrated every six months by the Sanders' Calibration Laboratory.

2.3 Signal Sources

A variety of signal sources were used to develop the r.f. environment for system susceptibility tests. The field intensity was monitored by the field intensity meters described above, and so the signal source was not a primary consideration in determing the accuracy of measurement.

The signal sources are calibrated by the S/A Instrument Calibration/Standards Laboratory on a 12 month cycle.

2.4 Description of Shielded Enclosure

a)	Type Construction:	Per MIL-E-8881; Type 11B per Table I; Double shield cell type, solid metal, Class C per Table II.
b)	Manufacturer:	RayProof Corporation, Norwalk, Conn.
c)	Model No:	81
d)	Size:	6.1M x 3M x 2.4M
e)	Door Clerance:	2M x 1.8M
f)	Filter Current & Voltage Rating:	RayProof 1B41-60 60 amp, 115V AC, 400 Hz
g)	Ground Plane Size & Material:	Copper .92M x 3.4M x 79MM thick
h)	DC Bonding Resistance of Ground Plane:	.2 milliohms

2.5 Test Sample Operation

For all EMI tests the IFO was placed into normal operation. None of the test light indicators were lit.

2.6 Susceptibility Monitoring

During susceptibility testing, the test lights were monitored to check for any malfunction.

APPENDIX A
TEST METHOD CE03
CONDUCTED EMISSION
POWER LEADS
20KHz to 50MHz

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG.	SERIAL NO.	CAL.DATE
EMI METER	NF-105 EMPIRE	3348	7/75
CURRENT PROBE	91550-1 STODDART	BF496	N/A
CAPACITORS	10μfd FEEDTHRU SANDERS ASSOCIATES	N/A	N/A

TEST PROCEDURE

Broadband and narrowband conducted emissions were measured from 20KHz to 50MHz, on the 28VDC power leads. The test setup is shown in Figure I.

TEST RESULTS

Broadband conducted emissions exceeding CE03 limits were measured on +28 volt and return leads. Worst case conducted emission exceeds the limit by 32dB on 28V return lead. Narrowband conducted emission exceeding CE03 limits were measured on 28V return lead. Worst case conducted emission exceeds limits by 26dB. Transients exceeding CE03 limits were measured on +28V and return leads. Worst case exceeds limits by 25dB. See data sheets 1 thru 6.

APPENDIX B
TEST METHOD CS01
CONDUCTED SUSCEPTIBILITY
POWER LEADS
30Hz to 50KHz

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG	SERIAL NO.	CAL.DATE
OSCILLATOR	200CD HEWLETT-PACKARD	333-54618	N/A
POWER AMPLIFIER	M0100 BOGEN	J-52	N/A
TRANSFORMER	6220-1 SOLAR	N/A	N/A
VOLTMETER	630PL TRIPLETT	4593	10/75

TEST PROCEDURE

A 3V RMS signal was injected on the 28VDC high and return leads of the power supply from 30Hz to 50KHz. The IFO operation was monitored for susceptibility by a visual check of the test lamps. The test setup is shown in Figure 2.

TEST RESULTS

No lights came on to indicate any malfunction during this test. See data sheet 7.

APPENDIX C
TEST METHOD CS02
CONDUCTED SUSCEPTIBILITY
POWER LEADS
50KHz to 400MHz

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG	SERIAL NO.	CAL.DATE
SIGNAL GENERATOR	60618 Hewlett-Packard	434-08498	8/75
SIGNAL GENERATOR	608 Hewlett-Packard	202-04499	8/75
RF VOLTMETER	91CA BOONTON	1122	3/76
CAPACITOR	EMI-F-0059 SANDERS	N/A	N/A

TEST PROCEDURE

A 1 volt RMS signal was injected on the 28VDC high and return leads of the power supply. During testing IFO operation was monitored for susceptibility indications by a visual check of the test lights. The test setup is shown in Figure 3.

TEST RESULTS

No lights came on during test to indicate malfunction. See data sheet 8.

APPENDIX D
TEST METHOD CS06
SPIKE
POWER LEADS

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG	SERIAL NO.	CAL.DATE
SPIKE GENERATOR	6471-F SOLAR	17536	7/75
OSCILLOSCOPE	541A TEKTRONIX	022490	10/75

TEST PROCEDURE

Positive and negative 56 volt 10 μsec spikes were injected on the plus 28 volt power leads.

(a) Single shots
(b) 6 to 10 PPS

The IFO operation was monitored for susceptibility indications by monitoring indicator lamps. The test setup is shown in Figure 4.

TEST RESULTS

No failure lamps came on. See data sheet 9.

APPENDIX E
TEST METHOD RE02
RADIATED EMISSION
14KHz to 10GHz
ELECTRIC FIELD

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG	SERIAL NO.	CAL. DATE
EMI METER	EMA 910 EMC	121-121	4/76
EMI METER	NF-105 EMPIRE	3348	7/75
VERTICAL ANTENNA	ODC-100BT	137	6/75
BICONICAL ANTENNA	7825 HONEYWELL	N/A	N/A
CONE ANTENNA	93490-1 STODDART	N/A	N/A
CONE ANTENNA	93491-1 STODDART	N/A	N/A
HAND PROBE	MP-105	N/A	N/A
VERTICAL ANTENNA	VR-105 EMPIRE	181	5/76
VERTICAL ANTENNA	VA-105 EMPIRE	796	8/75
EMI METER	EMA-10 FAIRCHILD	10342	12/75

TEST PROCEDURE

Broadband and narrowband radiated emission measurements were performed from 14KHz to 10GHz. The measurement antenna was positioned 1.0 meter from the test sample. The test setup is shown in Figure 5.

TEST RESULTS

Broadband radiated emissions exceeding RE02 limits were detected at 14KHz, 20KHz and 31KHz. Worst case emission at 31KHz is 12dB above limit. Narrowband radiated emissions exceeding RE02 limits were detected at various frequencies between 25MHz and 284MHz. The worst case narrowband emission at 25MHz exceeds RE02 limits by 21dB. Transient radiated emissions exceeding RE02 limits were detected at 25MHz. The emission level was 12dB above limits at this frequency. See data sheets 10 thru 13.

APPENDIX F.
TEST METHOD RS02
RADIATED SUSCEPTIBILITY
MAGNETIC INDUCTION FIELD

TEST EQUIPMENT

DESCRIPTION	MODEL/MFG	SERIAL NO.	CAL.DATE
SPIKE GENERATOR	6471-5 SOLAR	17536	7/75
VARIAC	116 SUPERIOR	N/A	N/A
TRANSFORMER	N/A	N/A	N/A
METER	25A WESTON	CC673	2/76

TEST PROCEDURE

A test wire carrying 100 volt 10μsec spikes was wrapped around the case of IFO maintenance warning unit crew read out unit, all cables and DC power leads.

A test wire carrying 20 amperes of 400 Hz current was wrapped around same units. The one operation was monitored for susceptibility by a visual check of the test lamps. The test setup is shown in Figure 6.

TEST RESULTS

No failure lamps came on. See data sheet 14.

APPENDIX G
TEST METHOD RS03
RADIATED SUSCEPTIBILITY
ELECTRIC FIELD
14KHz to 10GHz

TEST EQUIPMENT

	Description	Model/Mfg.	Serial No.	Cal Date
—	EMI Meter	EMA-910 Singer	121-121	4/76
—	EMI Meter	NF-105 Empire	3348	7/75
—	Oscillator	HP200 CD Hewlett Packard	333-54618	N/A
—	Signal Generator	HP606 A Hewlett Packard	434-08498	8/75
—	Power Amplifier	MO100 Bogen	J52	N/A
	Power Oscillator	404A Microdot	32	12/75
	Power Oscillator	406A Microdot	87	12/75
	Power Oscillator	125 Airborne Instru. Lab.	12510	N/A
	Signal Generator	616B Hewlett Packard	259-00099	10/75
	Signal Generator	C772A Microlab	519	2/76
	Signal Generator	X772A Microlab	324	2/76
—	Vertical Antenna	VR105 Empire	181	5/76
—	Vertical Antenna	VA-105	796	8/75
—	Biconical Antenna	7825 Honeywell	N/A	N/A
—	Cone Antenna	93490-1 Stoddart	N/A	N/A
	Horn Antenna	CA-L, S, M, X Polarad	N/A	N/A
	EMI Meter	EFS-1 26 IFI	317	9/75

TEST PROCEDURE

The one system was immersed in an electric field 10V/M from 14KHz to 35MHz and 5V/M from 35MHz to 10GHz. IFO operation was monitored for susceptibility by a visual check of the test lamps. The test setup is shown in Figure 7.

TEST RESULTS

No susceptibility indications were observed. See data sheet 15.

DATE: 5/5/76 REPORT NO: 2439 DATA SHEET 1 OF 1

ITEM TESTED: IFO SN 1

TEST EQUIPMENT: NF-105
91550-1 PROBE

TEST PERFORMED: CEO-3 20KHZ TO 50 MHZ POWER LEADS BB

TEST CONDITIONS:

PERFORMED BY: K.U.

FREQ. MHZ	IG LEVEL dBμV/MHz	PROBE FACTOR	COND LEVEL dBμV/MHz		CEO3 LIMIT dBμV/MHz		
.020	70	+12	82		134		28VDC
.030	67	+8	75		126		HIGH LEAD
.040	66	+6	72		120		
.060	86	+2	88		114		
.080	68	0	68		108		
.100	58	-2	56		104		
.142	62	-4	58		98		
.180	49	-5	44		94		
.300	85	-9	76		84		
.400	37	-10	27		81		
.580	78	-11	67		73		
.800	38	-12	26		66		
1.0	31	-13	18		62		
2.0	44	-13	31		50		
2.95	55	-13	42		50		
3.8	64	-14	50		50		
6.0	67	-14	53		50		
7.9	48	-14	34		50		
10.0	52	-15	37		50		
15.0	37	-15	22		50		
19.5	38	-15	23		50		
30.0	34*	-15	19		50		
40.0	28*	-15	13		50		
50.0	52	-14	38		50		

DATE: 5/7/76 REPORT NO: 4437 DATA SHEET 6 OF 15

ITEM TESTED: EFO SN1

TEST EQUIPMENT: EMC-25
91550-1 PROBE

TEST PERFORMED: CE03 20KHZ TO 50MHZ POWER LEADS N.B

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RH

FREQ. MHZ	Meter Reading dBuV	PROBE FACTOR dB	COND LEVEL dBuA			CE03 LIMIT dBuA	
.025	22	+10	32			76	28VDC
.035	26	+8	34			72	HIGH LEAD
.050	31	+4	35			68	
.058	37	+3	40			66	
.075	28	+1	29			62	
.116	10	-3	7			58	
.150	44	-5	39			54	
.280	48	-8	40			46	
.435	24	-10	14			40	
.560	43	-11	32			37	
.850	36	-12	24			32	
1.1	16	-13	3			30	
2.3	26	-14	12			20	

EMC DATA SHEET

DATE: 5/5/76 REPORT NO: 2439 DATA SHEET 3 OF 15

ITEM TESTED: IEO SN1

TEST EQUIPMENT: NF-105
91550-1 PROBE

TEST PERFORMED: CEO-3 .020MHz, 80 MHz
8MHz & 25MHz TRANSIENTS

TEST CONDITIONS:

PERFORMED BY:

FREQ. MHZ	IG LEVEL dBμV/MHz	PROBE FACTOR dBμV/MHz	COND. LEVEL dBμV/MHz		CEO 3 LIMIT dBμV/MHz		
.020	72	+12	84		134		28 VDC
.800	35	-12	23		66		HIGH LEAD
8.0	45	-14	31		50		
25.0	90	-15	75	/	50		

EMC DATA SHEET

DATE: 5/5/76 REPORT NO: 2439 DATA SHEET 4 OF

ITEM TESTED: IFO SN1 TEST EQUIPMENT: NF-10 91550-1 Rec

TEST PERFORMED: CEO-3 20 KHZ TO 50 MHZ POWER LEADS B.B.

TEST CONDITIONS: PERFORMED BY:

FREQ. MHZ	IG LEVEL dBμV/MHZ	PROBE FACTOR	COND. LEVEL dBμV/MHz			CE03 LIMIT dBμV/MHz	
.020	76	+12	88			134	28 VDC
.030	78	+8	86			126	RETURN LEA
.040	87	+6	93			120	
.060	80	+2	82			114	
.080	74	0	74			108	
.100	69	-2	67			104	
.140	90	-4	86			98	
.200	66	-7	59			92	
.280	>120	-9	111	✓		86	
.400	105	-10	95	✓		81	
.580	105	-11	94	✓		72	
.800	100	-12	88	✓		66	
1.0	107	-13	94	✓		62	
1.5	84	-13	71	✓		55	
1.95	59	-13	46			51	
2.9	54	-14	40			50	
4.0	58	-14	44			50	
6.0	63	-14	49			50	
8.0	46	-14	32			50	
10.0	51	-15	36			50	
15.0	36	-15	21			50	
20.0	30*	-15	15			50	
30.0	34*	-15	19			50	
40.0	32*	-15	17			50	
50.0	52	-14	38			50	

EMC DATA SHEET

DATE: 5/7/76 REPORT NO: 2439 DATA SHEET 5 OF 15

ITEM TESTED: IFO SN1

TEST EQUIPMENT: EMC-25
91550-1 PROBE

TEST PERFORMED: CE03 20KHZ TO 50MHZ POWER LEADS W. B

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RLS

FREQ. MHZ	Meter Reading dBuV	PROBE FACTOR dB	COND LEVEL dBuA			CE03 LIMIT dBuA	
.026	36	+10	46			76	28 VDC
.035	40	+8	48			72	RETURN
.050	36	+4	40			68	
.058	34	+3	37			66	
.116	10	-3	7			58	
.150	50	-5	45			54	
.260	76	-8	68	↙		46	
.440	52	-10	42			40	
.560	74	-11	63	↙		37	
.850	60	-12	48	↙		32	
2.3	33	-14	19			20	

EMC DATA SHEET

DATE: 5/5/76 REPORT NO: 2439 DATA SHEET 6 OF 15

ITEM TESTED: IFO SN 1 TEST EQUIPMENT: NF-105
91550-1 PROBE

TEST PERFORMED: CEO-3 .02 MHz .80 MHz
8 MHz & 25 MHz TRANSIENTS

TEST CONDITIONS: NORMAL OPERATION PERFORMED BY:

FREQ. MHz	IG LEVEL dBuV/MHz	PROBE FACTOR dB	COND. LEVEL dBuV/MHz		CEO3 LIMIT dBuV/MHz		
.020	79	+12	91		134		28 VDC
.800	100	-12	88	✓	66		RETURN LEAD
8.0	46	-14	32		50		
25.0	61	-15	46		50		

EMC DATA SHEET

DATE: 5/6/76 REPORT NO: 2439 DATA SHEET 7 OF 15

ITEM TESTED: IFO S/N1

TEST EQUIPMENT: TRIPLET 630PL
ISOLATION XFORMER 4952
HP 200CD
BOGEN AMP. M0100

TEST PERFORMED: CS01 30 Hz TO 50KHz

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: K.U.

FREQ. Hz	INJECTED LEVEL V/RMS		REQ LEVEL V/RMS				
30	3.0		3.0				+28 VDC
↓	3.0		TO				HIGH LEAD
↓	3.0						& 28VDC
50KHz	3.0		1.0				RETURN LEAD
			NO MALFUNCTION WAS DETECTED				
			ON EATHER +28VDC OR RETURN LEADS.				

EMC DATA SHEET

DATE: 5/6/76 REPORT NO: 2439 DATA SHEET 8 OF 15

ITEM TESTED: IFO S/N 1

TEST EQUIPMENT: RF VOLT METER
POWER AMP, BOONTON 230A
SIG. GENERATOR 606A H.P.
SIG GENERATOR 608A H.P.

TEST PERFORMED: CS02 50KHZ TO 400MHZ
POWER LEADS

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: K.U.

FREQ. MHZ	INJECTED LEVEL V/RMS		REQ. LEVEL V/RMS				
.050	1.0		1.0				+28VDC
|	|		|				HIGH LEAD
400	1.0		1.0				28VDC
							RETURN LEAD

EMC DATA SHEET

DATE: 5/7/76 REPORT NO: 2439 DATA SHEET 9 OF 15

ITEM TESTED: IFO SN 1

TEST EQUIPMENT: 6471-5 SPIKE GEN 541A SCOPE

TEST PERFORMED: CSO6 SPIKE SUSCEPTIBILITY

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RC

FREQ.							
1.	POSITIVE AND NEGATIVE 56 VOLT 10 USEC SPIKES WERE APPLIED TO THE PLUS 28 VDC POWER LEADS AS FOLLOWS						
	a.) SINGLE SHOT						
	b.) 6 to 10 PPS FOR 5 MINUTES EACH						
	NO FAILURE LAMPS CAME ON.						

EMC DATA SHEET

DATE: 5/6/76 REPORT NO: 2439 DATA SHEET 10 OF 15

ITEM TESTED: IFO SN 1

TEST EQUIPMENT: NF 105
ANT. VA 105 SN. 181
VA 105 SN 796

TEST PERFORMED: REO-2 14KHZ TO 16HZ
ELECTRIC FIELD B-B.

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY:

FREQ. MHZ	dBuv/MHZ	ANTENNA FACTOR dB/M	FIELD dB uV M/MHZ		REO 2 LIMIT dB uv/MHZ		
.014	55	60	115	✓	110		
.020	56	58	114	✓	108		
.031	62	56	118	✓	106		
.040	49	55	104		105		
.060	38	55	93		103		
.080	40	54	94		101		
.100	38	54	92		100		
.150	39	44	83		98		
.200	32	44	76		97		
.300	33*	44	77		95		
.400	32*	37	69		94		
.600	31*	39	70		92		
.800	32*	40	72		91		
1.0	33*	34	67		90		
1.5	30	35	65		88		
2.0	34	36	70		86		
3.0	31	29	60		85		
4.0	32	29	61		83		
6.0	32*	26	58		81		
8.0	34	24	58		80		
9.0	41	24	65		79		
10.	32	24	56		79		
15	31*	21	52		77		
21	43	21	64		75		
35	31*	21	52		73		

EMC DATA SHEET

DATE: 5/6/76 REPORT NO: 2439 DATA SHEET 11 OF 15

ITEM TESTED: IFO S/N1 TEST EQUIPMENT: 7825, 93490-1

TEST PERFORMED: REO-2 BB CONTINUED

TEST CONDITIONS: NORMAL OPERATION PERFORMED BY:

FREQ. MHZ	IG LEVEL dBuV/MHz	ANT FACTOR dB	FIELD dB uV M/MHz			REO 2 LIMIT dBuV M/MHz	
30	30*	12	42			74	
40	30*	13	43			72	HORIZONTAL
60	31*	8	39			71	BICONICAL
80	31*	8	39			69	
100	32	14	46			68	
130	48	15	63			67	
200	29*	18	47			65	
30	30*	12	42			74	
40	31*	13	44			72	VERTICAL
60	26*	8	34			71	BICONICAL
80	30*	8	38			69	
100	32*	14	46			68	
125	57	15	72			68	
200	30	18	48			65	
254	63	17	80			68	
300	30*	17	47			69	CONE ANTENNA
400	30*	18	48			72	S/N 93490-1
600	30*	21	51			76	
800	30*	24	54			79	
1.0	30*	26	56			80	

EMC DATA SHEET

DATE: 5/7/76 REPORT NO: 2439 DATA SHEET 12 OF 1?

ITEM TESTED: EFO SN1

TEST EQUIPMENT: EMC-23 VR-1-105 VA-105 7825, 93490-1 93491-1

TEST PERFORMED: RE02 NB 14KHZ TO 10GHZ

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RH

FREQ. MHZ	Meter Reading dBuV	ANT. FACTOR dB	FIELD INT dBuV/m			REQ LIMIT dBuV/m	
8.0	-6	24	18			32	
25.0	30	21	51	V		30	
125	32	16	48	V		40	VERT BICON
125	42	16	58	V		40	HORIZ BICON
254.0	36	17	53	V		45	CONICAL LOG
284.0	41	17	58	V		45	SPIRAL
							SCAN TO 10GHZ NO OTHER N.B SIGNALS.

EMC DATA SHEET

DATE: 5/6/76 REPORT NO: 2439 DATA SHEET 13 OF 15

ITEM TESTED: IFO S/N 1

TEST EQUIPMENT: NF 105
VR3-105 S/N 151
VA-105 S/N 796

TEST PERFORMED: REO-2 TRANSIENT

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY:

FREQ. MHZ	IC LEVEL dBMV @1HZ	ANT FACTOR dB	FIELD INT dBMV @1MHZ			REO2 LIMIT dBMV @1MHZ	
.020	—						
.800	—						
8.0	39	24	63			80	
25.0	66	21	87	✓		75	
400.0	—						

EMC DATA SHEET

DATE: 5/7/76 REPORT NO: 2439 DATA SHEET 14 OF 15

ITEM TESTED: IFO SN1

TEST EQUIPMENT: 6471-5 SPIKE GEN

TEST PERFORMED: RS02 MAGNETIC INDUCTION FIELD

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RJ

FREQ.							
1. A TEST WIRE CARRYING 100 VOLT 10USEC SPIKES WAS WRAPPED AROUND a. DC POWER LEADS b. ALL CABLES c. CREW READ OUT UNIT d. MAINT WARNING UNIT e. IFO UNIT							
2. A TEST WIRE CARRYING 20 AMPERES OF 400HZ CURRENT WAS WRAPPED AROUND SAME UNITS IN ITEM 1 ABOVE. NO FAILURE LAMPS CAME ON.							

EMC DATA SHEET

DATE: 5/7/76 REPORT NO: 2439 DATA SHEET 15 OF ___

ITEM TESTED: IFO SN/1

TEST EQUIPMENT: SEE TEST EQUIP. LIST FOR RS03.

TEST PERFORMED: RS03 14 KHZ TO 10 GHZ E FIELD

TEST CONDITIONS: NORMAL OPERATION

PERFORMED BY: RU

FREQ. MHZ	RAD. FIELD V/M		REQ. FIELD V/M				
.014	10		10				
TO	10		10	NO FAIL LIGHTS			
25.0	10		10	CAME ON			
25	10		10				VERT + HORIZ
TO	10		10	NO FAIL LIGHTS			BICON
35	10		10	CAME ON			
35	5.0		5.0	NO FAIL LIGHTS			VERT BICON
TO	5.0		5.0	CAME ON			
200	5.0		5.0				
35	5.0		5.0	NO FAIL LIGHTS			HORIZ BICON
TO	5.0		5.0	CAME ON			
200	5.0		5.0				
200	5.0		5.0	NO FAIL LIGHTS			CONE ANT.
TO	5.0		5.0	CAME ON			
1000	5.0		5.0				
1000	5.0		5.0	NO FAIL LIGHTS			HORN ANT.
TO	5.0		5.0	CAME ON			
10,000	5.0		5.0				

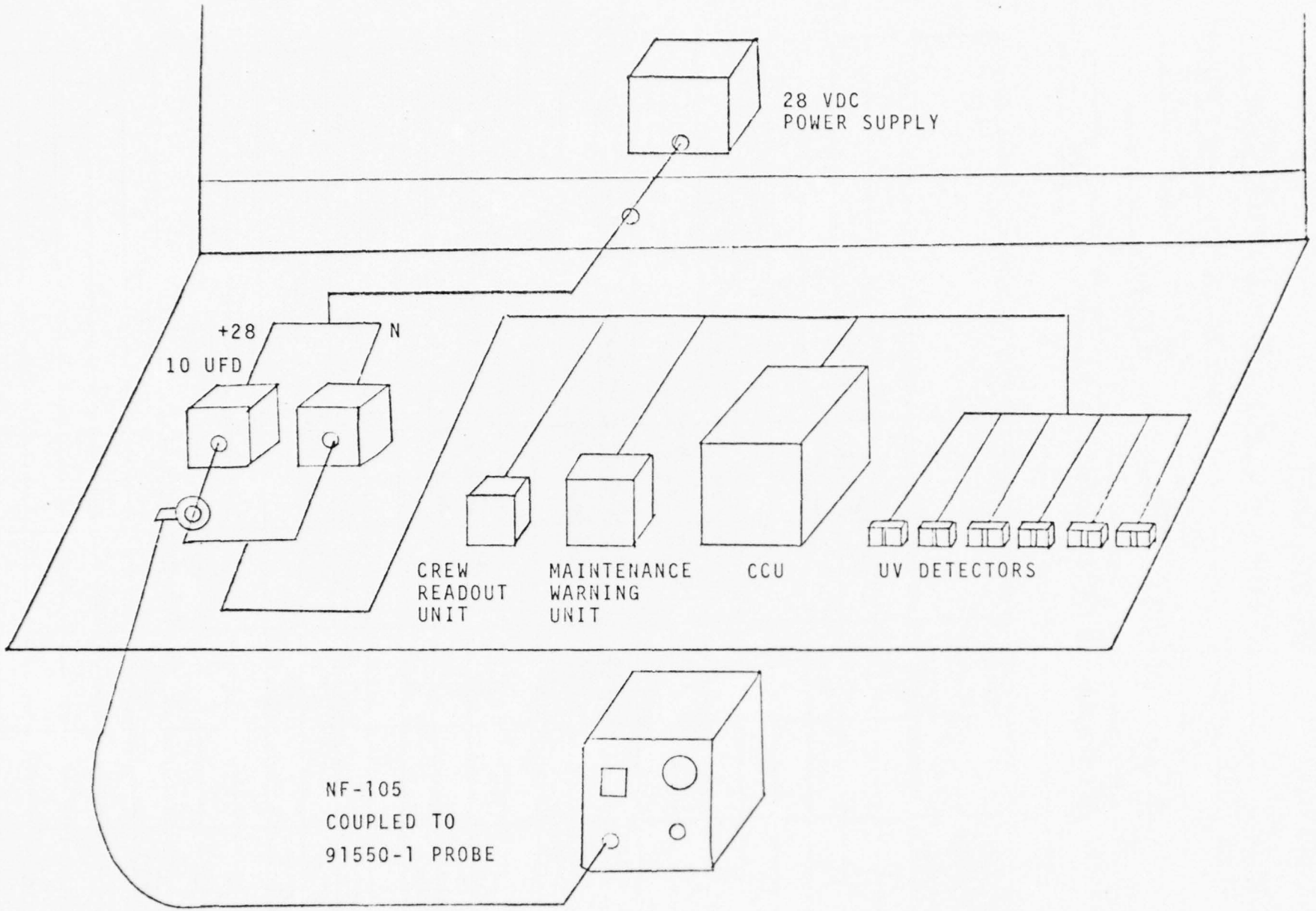


FIGURE 1. CE03 TEST SETUP

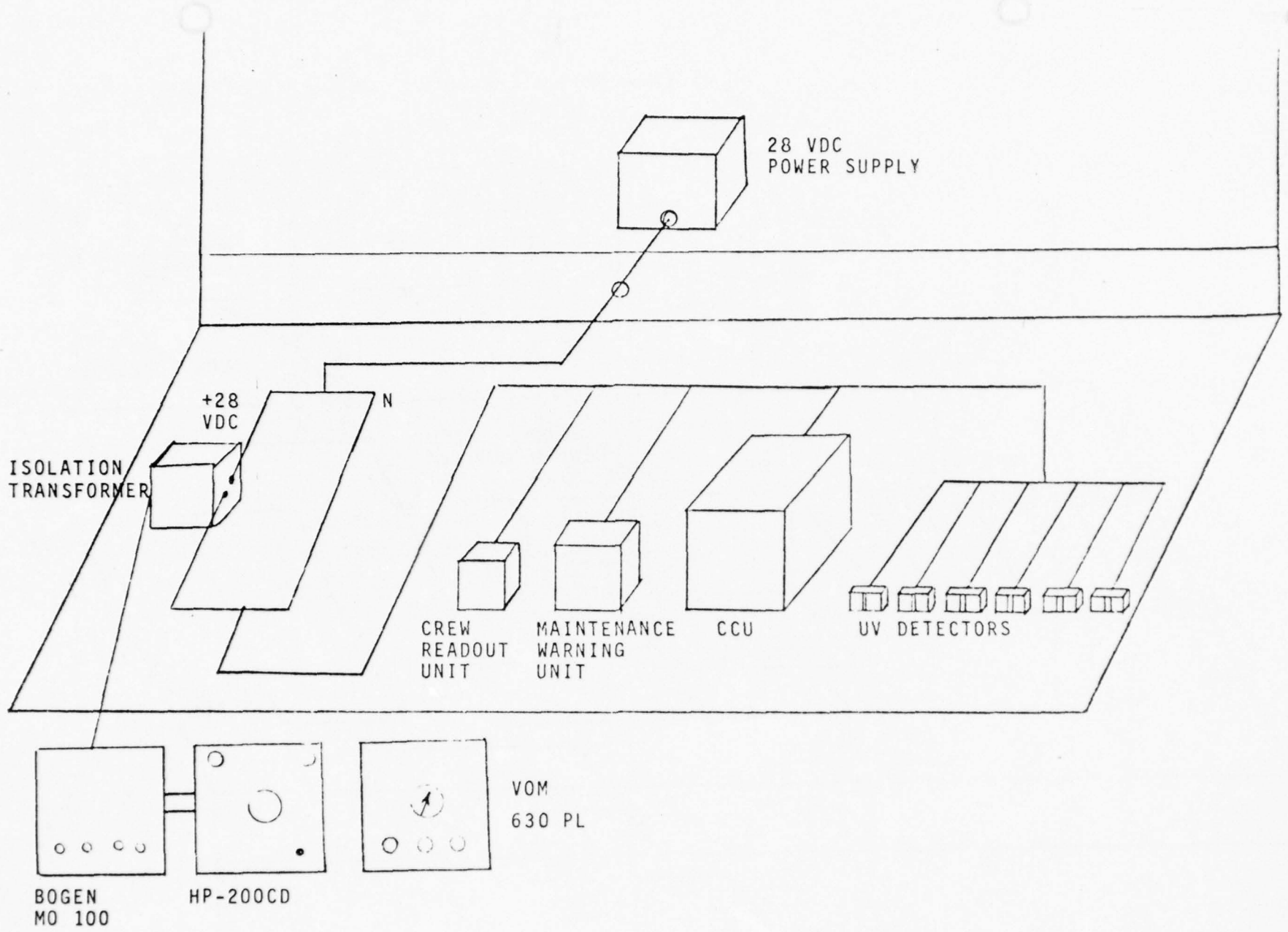


FIGURE 2. CS01 TEST SETUP

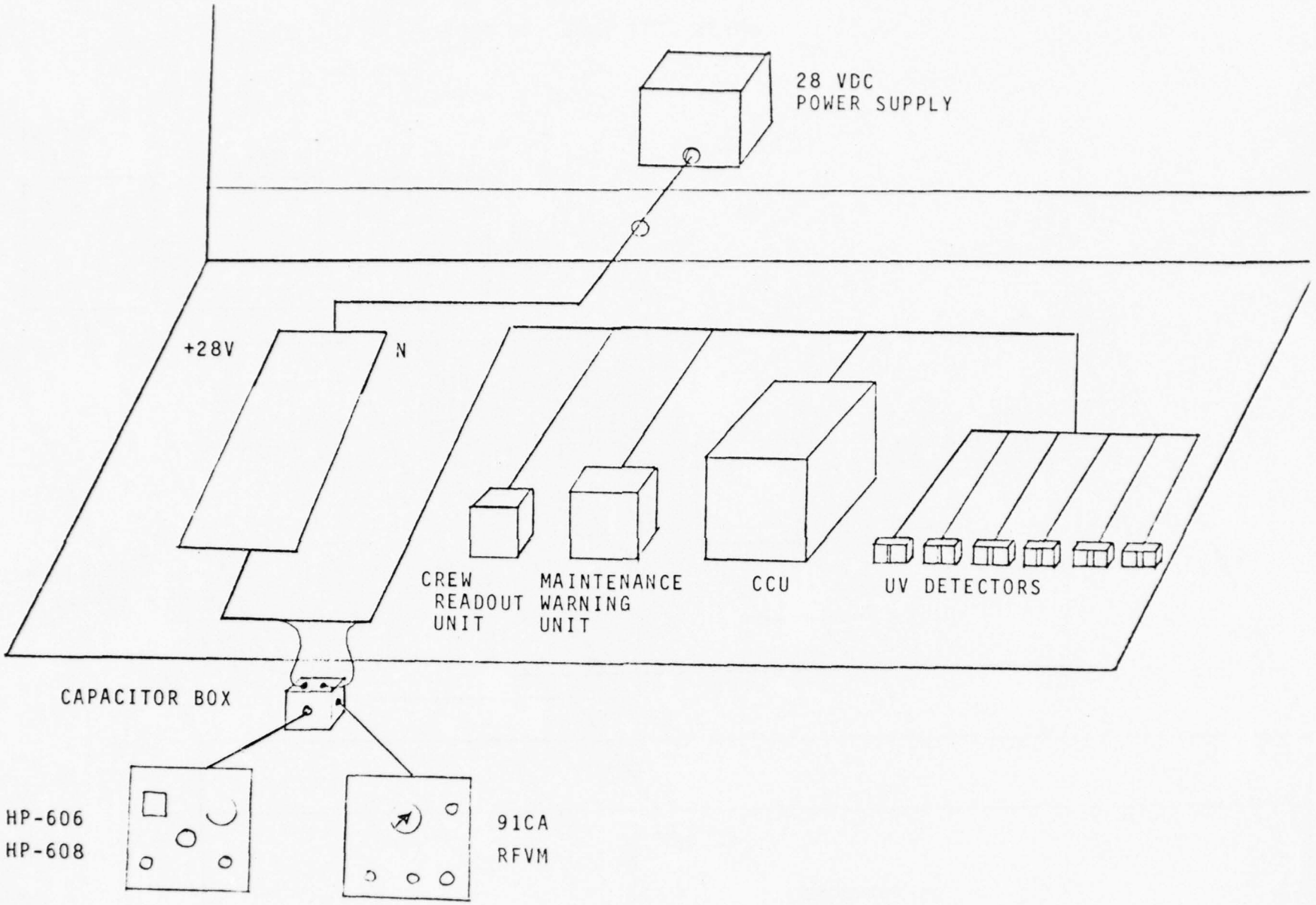


FIGURE 3. CSO2 TEST SETUP

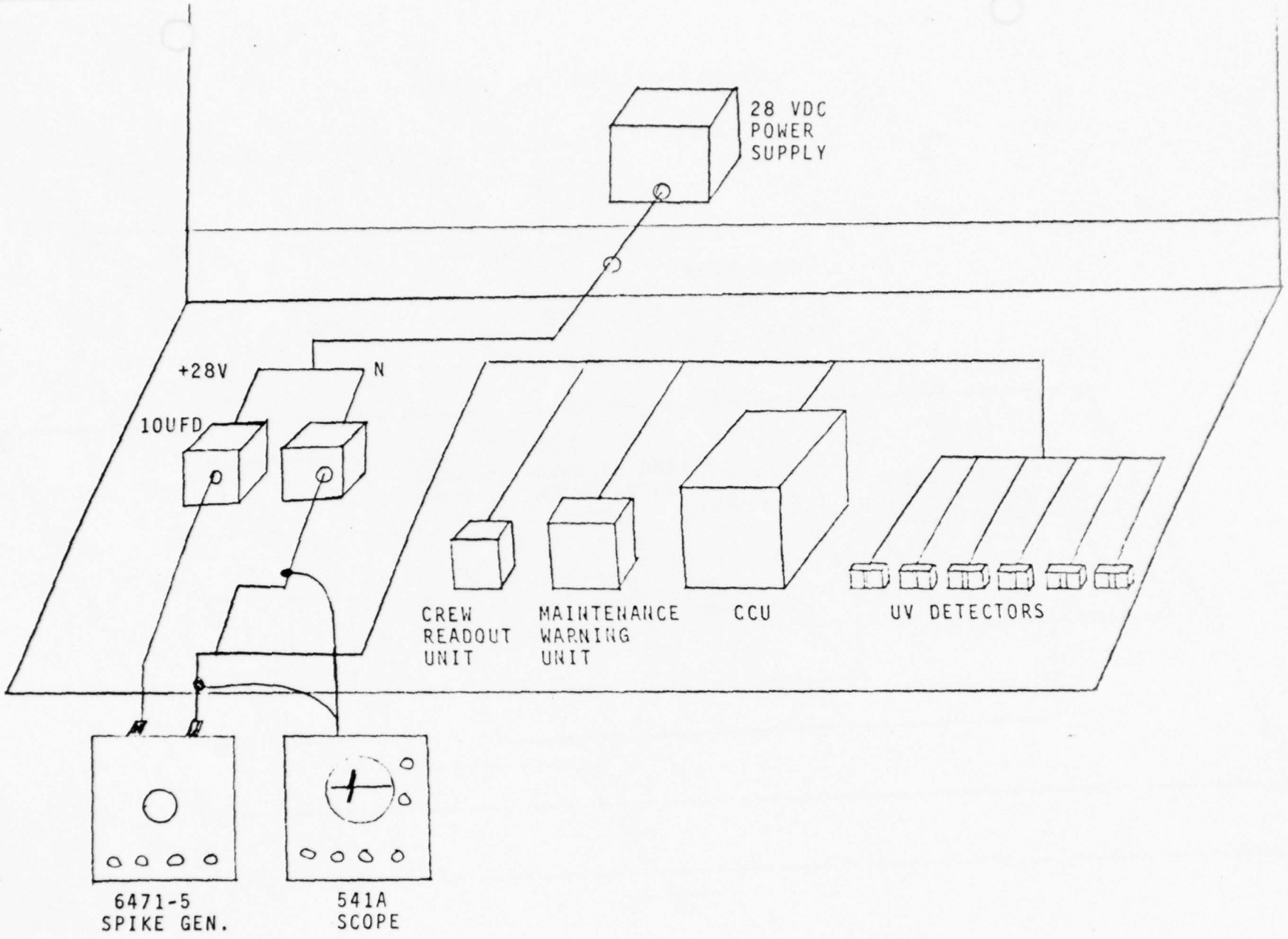


FIGURE 4. CS06 TEST SETUP

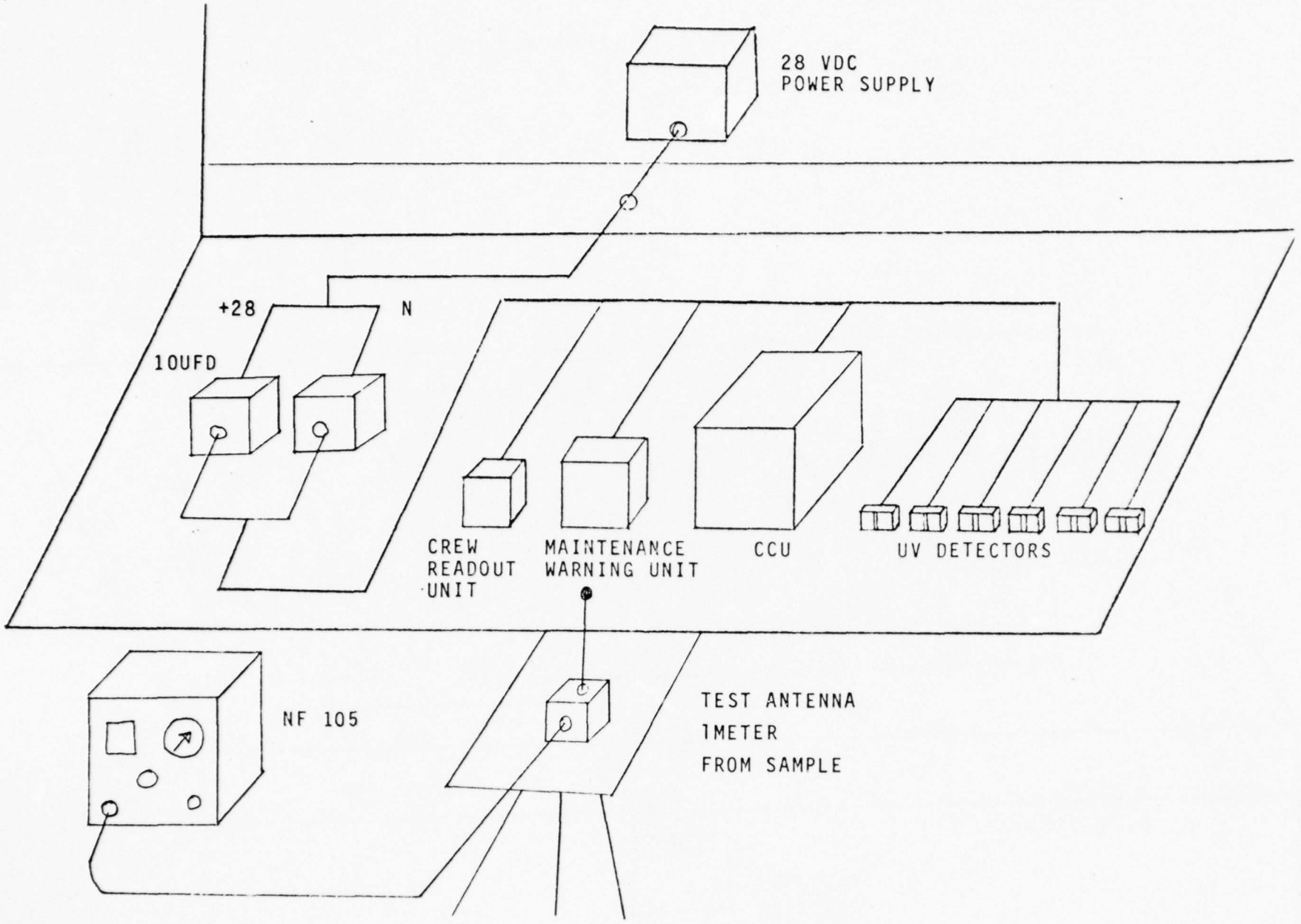


FIGURE 5. RE02 TEST SETUP

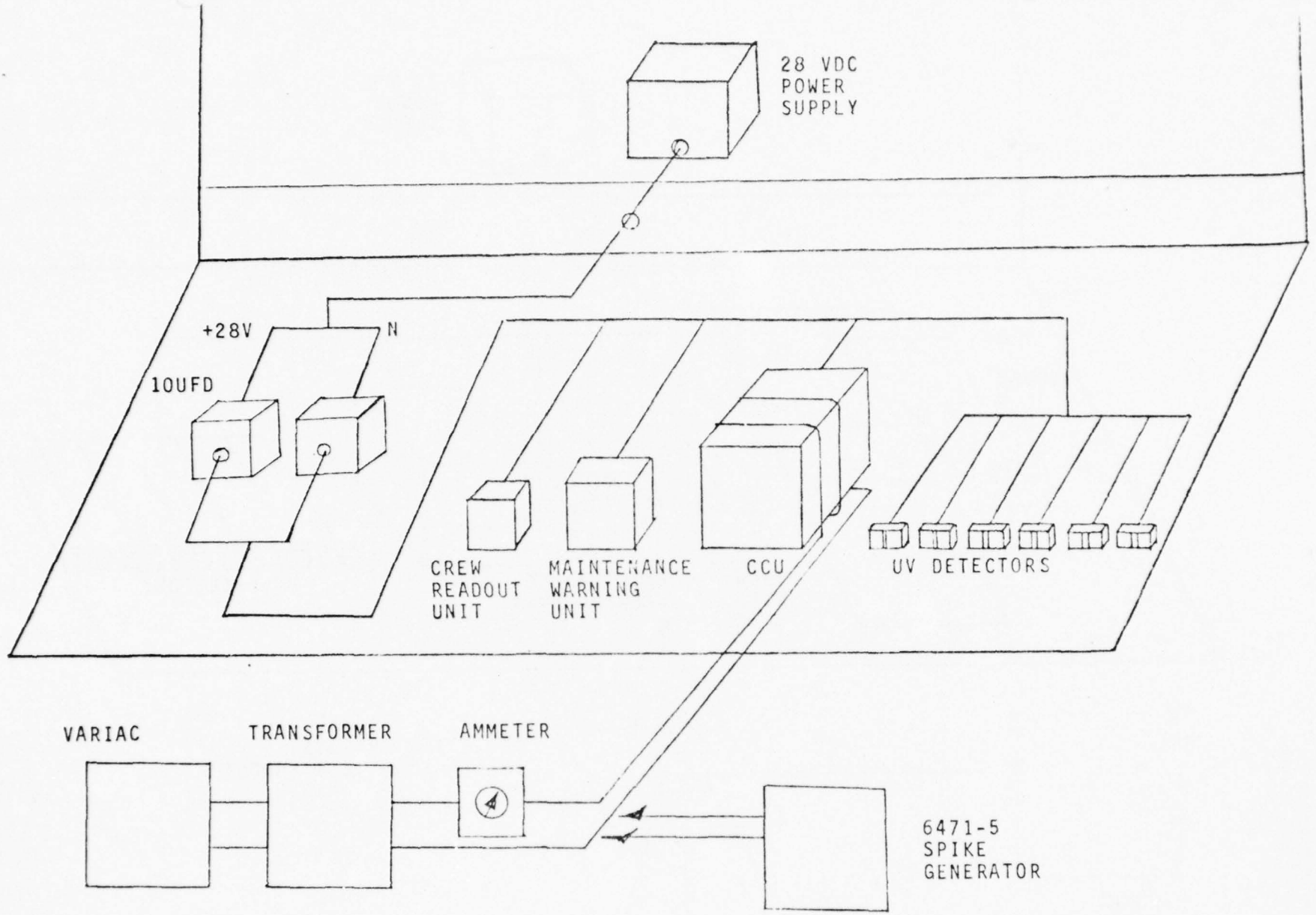


FIGURE 6. RS02 TEST SETUP

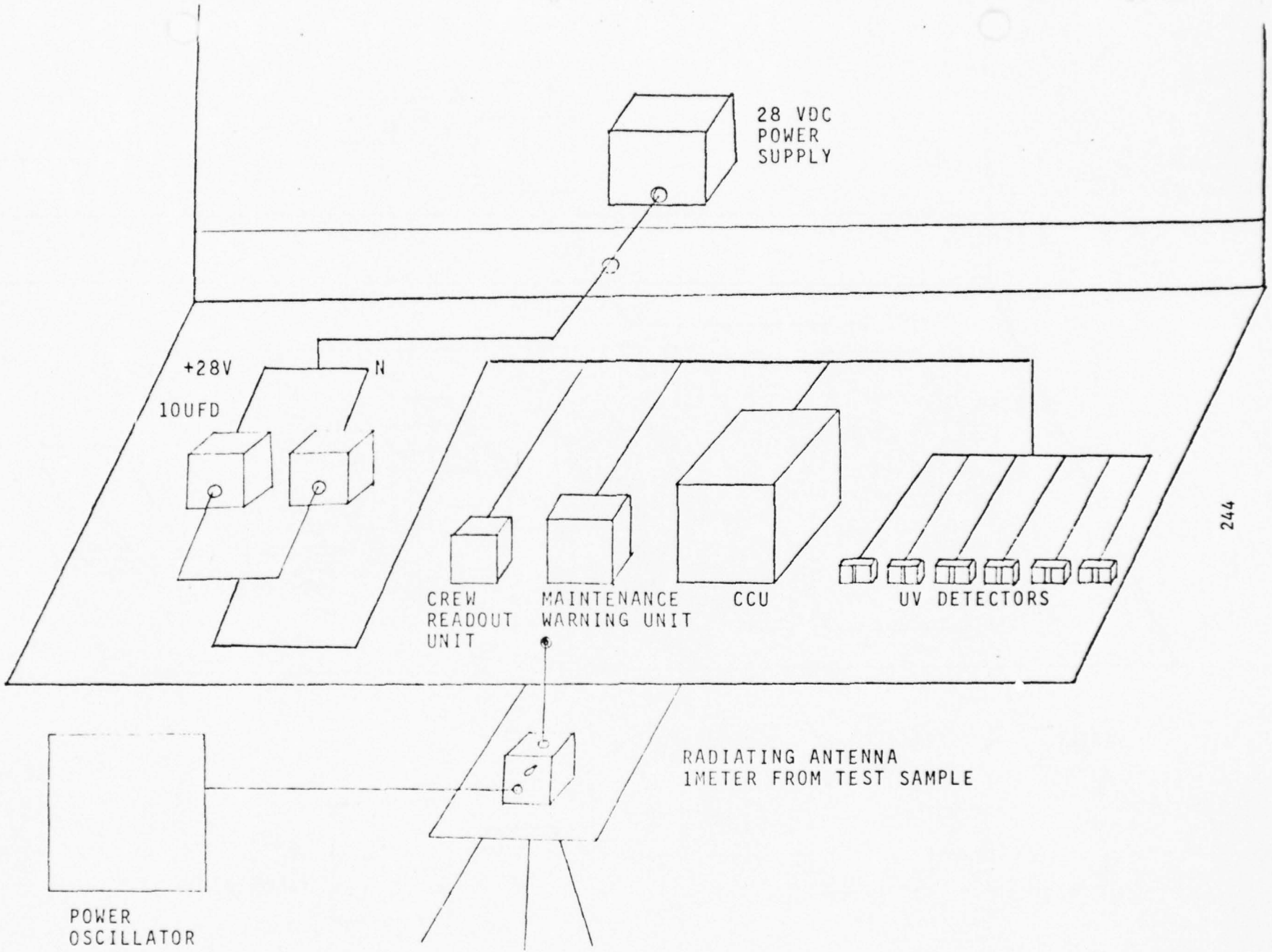


FIGURE 7. TS03 TEST SETUP

APPENDIX VII

RELIABILITY ANALYSIS

APPENDIX VII

RELIABILITY ANALYSIS

Reference: MIL-HDBK-217B 20 September 1974
MIL-STD-756A

Prediction: 355 Hours, mean time between failures

1. Enclosures

   A. Mathematical model as described in MIL-STD-756A and mathematical description.

   B. Failure rate schedules for each drawing number and listing

      a. Item Number
      b. Part type or part drawing number
      c. Quantity of each part required
      d. Part rating
      e. Part stress
      f. Part failure rate per 10^6 hours
      g. Total failure rate for each item
      h. Sample computations

2. Design Prediction Procedure: MIL-STD-756A, Paragraph 5.2

3. Computation Explanation:

   Failures are considered to be serial. If one part should fail, the whole equipment fails.

   MTBF = $\frac{1}{\Sigma \lambda}$, where λ is the failure rate of each part.

   CCU Ambient temperature is taken to be 95°C

   CRU and MWU are taken to be 71.1°C.

   Sensors are taken to be 205°C.

SAMPLE CALCULATIONS

1. Computer Control Unit

Unit Temperature = 95°C
References - MIL - Handbook 217B

1.1 Integrated Circuits

Junction Temperature = 105°C
References: Texas Instruments TTL 1973 Data Book
Formula (MIL-HDBK 217B, Page No. 2.1.1-1 $\lambda_P = \pi_L \pi_Q (C\pi_T + C_2 \pi_E)$

Part Number	Ref. Pg. No.	Active Components	$\lambda_P = \pi_L \pi_Q (C\pi_T + C_2 \pi_E)$		Failure Rate x 10^{-6}
SN54L20	86-66	4 x 2	1 x 150 (.0021 x 3 + .0050 x 4)	=	3.95
SN54L04 SN5404	86-63	4 x 6	150 (.0043 x 3 + .0074 x 4)	=	6.38
SN54L73	128-76	8 x 2 = 16 gates	150 (.0084 x 3 + .011 x 4)	=	10.38
SN5400 SN54L00	86-62	4 x 4	150 (.0033 x 3 + .0064 x 4)	=	5.28
SN54L10	86-64	4 x 3	150 (.0027 x 3 + .0056 x 4)	=	4.58
SN5406	106-63	5 x 6	150 (.0050 x 3 + .0080 x 4)	=	7.05
SN4L02	92-62	4 x 6			6.38
SN54L30	86-68	1 x 4	150 (.0013 x 3 + .0039 x 4)	=	2.93
SN54L93	224	33 gates	150 (.014 x 3 + .014 x 4)	=	14.70
SN54L121	134-82	10 gates	150 (.0062 x 3 + .0089 x 4)	=	8.175
SN54L74	120-76	2 x 6 = 12 gates	150 (.0069 x 3 + .0095 x 4)	=	8.85
SN54L90	224	37 gates	150 (.015 x 3 + .014 x 4)	=	15.15
SN54L86	209	4 x 1 gates	150 (.0013 x 3 + .0039 x 4)	=	2.93
SN54L03	88-63	4 x 3	150 (.0027 x 3 + .0058 x 4)	=	4.69

Part Number	Ref. Pg. No.	Active Components	$\lambda_p = \pi_L \pi_Q (C\pi_T + C_2 \pi_E)$		Failure Rate X 10^{-6}
SN5405	88-63	6 x 3	150 (.0035 x 3 + .0067 x 4)	=	5.59
MC1569R		21 Linear	150 (.0057 x 32 + .013 x 4)	=	35.10
MC1563R		30 Linear	150 (.0075 x 32 + .0165 x 4)	=	45.09
LH2111		2 x 6 gates	150 (.0069 x 3 + .0095 x 4)	=	8.85
AM26L02		9 x 2 gates	150 (.0091 x 3 + .011 x 4)	=	10.69

1.2 Rectifiers

References Unitrode & MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.2.4.1): $\lambda_p = \lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C$

P/N	Description	Stress Factor	$\lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$	Failure Rate x 10^{-6}
1N456		S = .1	.0036 (25 x 25 x .6 x .7 x 1)	.94
	Bridge Rectifier Unitrode	S = .5	4 x .016 (25 x 5 x 1.5 x .7 x 1)	8.20
FD700			.0036 (25 x 25 x .6 x .7 x 1)	.94
IN3611	200V, 2A Unitrode	S = .1	.0036 (25 x 5 x 1.5 x .7 x 1)	.472
IN483B	60V		.0036 (25 x 5 x .6 x .7 x 1)	.19

1.3 Connectors (MIL Spec 55302 Diallyl Phthalate)

Reference MIL Handbook 217B
Formula MIL Handbook 217B, pg. 2.11.1: p = b (E x P) + cyc

P/N	No. of Contacts	b (E x P) + cyc	Failure Rate x 10^{-6}
J	54	.042 (4 x 10.42) + 54 x .011	2.34
J	18	.042 (4 x 3.71) + 18 x .011	.86
J	30	.042 (4 x 560) + 30 x .011	1.27

1.4 Transistors

Reference MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.2.1.1): $\lambda_p = \lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$

P/N	Description	Stress Factor	$\lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$	Failure Rate x 10^{-6}
2N2060	NPN Dual		2 x .013 (25 x 3 x 10 x .3 x 1)	1.365
2N1711	NPN		.010 (25 x .7 x 10 x .3 x 1)	.525
2N2439	NPN	.4	.020 (25 x .7 x 10 x .3 x 1)	1.05
2N2905	PNP		.015 (25 x .7 x 10 x .3 x 1)	.79

1.5 Transformers

Reference MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.7.1): $\lambda_p = \lambda_b (\pi_E \times \pi_F)$

P/N	$\lambda_b (\pi_E \times \pi_F)$	Failure Rate x 10^{-6}
Edison 15997	.0040 (5 x 20)	.40

1.6 Resistors

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.5.2-1): $\lambda_p = \lambda_b (\pi_E \times \pi_R \times \pi_Q)$

Description	Stress Factor	$\lambda_b (\pi_E \times \pi_R \times \pi_Q)$	Failure Rate x 10^{-6}
Resistor	.1	.0025 (5 x 1 x 1)	.013
	.2	.0029 (5 x 1 x 1)	.015
	.5	.0043 (5 x 1 x 1)	.022
RC	.5	.0054 (4 x 1 x 5)	.108
	.1	.0021 (4 x 1 x 5)	.042
RB	.1	.0051 (15 x 1 x 5)	.3825
	.5	.0085 (15 x 1 x 5)	.6375

1.7 Potentiometers

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.5.6-1): $\lambda_p = \lambda_b \pi_{TAPS} (\pi_R \times \pi_V \times \pi_Q \times \pi_E)$

Description	$\lambda_b \pi_{TAPS} (\pi_R \times \pi_V \times \pi_Q \times \pi_E)$	Failure Rate x 10^{-6}
Trimpot	.796 x 1 (1 x 1 x 6 x 4)	19.10

1.8 Capacitors

Reference: MIL Handbook 217B

Formula (MIL Handbook 217B, pg. 2.6.4-1 & 2.6.5-1): $\lambda_p = \lambda_b (\pi_E \times \pi_Q)$ CK06 Capacitors

$\lambda_p = \lambda_b (\pi_E \times \pi_{SR} \times \pi_Q)$ Tantalum Capacitors

Capacitor Type	Stress Factor	$\lambda_b (\pi_E \times \pi_Q)$	Failure Rate x 10^{-6}
CK06	.1	.0023 x (4 x 10)	.092
		$\lambda_b (\pi_C \times \pi_{SR} \times \pi_Q)$	
Tantalum	.1	.011 (4 x .07 x 1.5)	.004
	.17	.012 (4 x .07 x 1.5)	.006
	.22	.013 (4 x .07 x 1.5)	.007
	.33	.016 (4 x .07 x 1.5)	.013

2. Maintenance Warning Unit and Crew Readout Unit

Unit Temperature 71.1°C

2.1 Integrated Circuits

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.1.1-1): $\lambda_p = \pi_L \times \pi_Q \times (C\pi_T + C_2 \pi_E)$

P/N	Active Components	$\pi_L \times \pi_Q \times (C\pi_T + C_2 \pi_E)$	Failure Rate x 10^{-6}
SN5406J		1 x 150 (.0051 x 1.3 + .0080 x 4)	5.85
MC1569R	21 Linear	1 x 150 (.0057 x 7.5 + .014 x 4)	14.85
SN5406	30	1 x 150 (.0051 x 1.3 + .0080 x 4)	5.79

2.2 Rectifier Diodes

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.2.4-1): $\lambda_p = \lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$

P/N	Description	$\lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$	Failure Rate x 10^{-6}
MR1396	Rectifier	.0073 (25 x 25 x 1.5 x .7 x 1)	4.85
IN3611	Rectifier	.0024 (25 x 25 x .6 x .7 x 1)	.63

2.3 Zener Diodes

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.2.5-1): $\lambda_p = \lambda_b (\pi_E \times \pi_A \times \pi_Q)$

P/N	Description	$\lambda_b (\pi_E \times \pi_A \times \pi_Q)$	Failure Rate x 10^{-6}
	Zener Diode	.0044 (25 x 1.5 x 25)	2.75

2.4 Transistors

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.2.1-1): $\lambda_p = \lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$

Type	Stress Factor	$\lambda_b (\pi_E \times \pi_Q \times \pi_A \times \pi_{S2} \times \pi_C)$	Failure Rate x 10^{-6}
PNP	.1	.011 (25 x .7 x 10)	.578
NPN	.1	.0076 (25 x .7 x 10)	.394

2.5 Relay

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.9-1): $\lambda_p = \lambda_b (\pi_E \times \pi_C \times \pi_{cyc} \times \pi_F)$

	Description	$\lambda_b (\pi_E \times \pi_C \times \pi_{cyc} \times \pi_F)$	Failure Rate x 10^{-6}
	Relay	.0079 (16 x 1.5 x .1 x 6)	.1137

2.6 Resistors

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.5.2-1): $\lambda_p = \lambda_b (\pi_E \times \pi_R \times \pi_Q)$

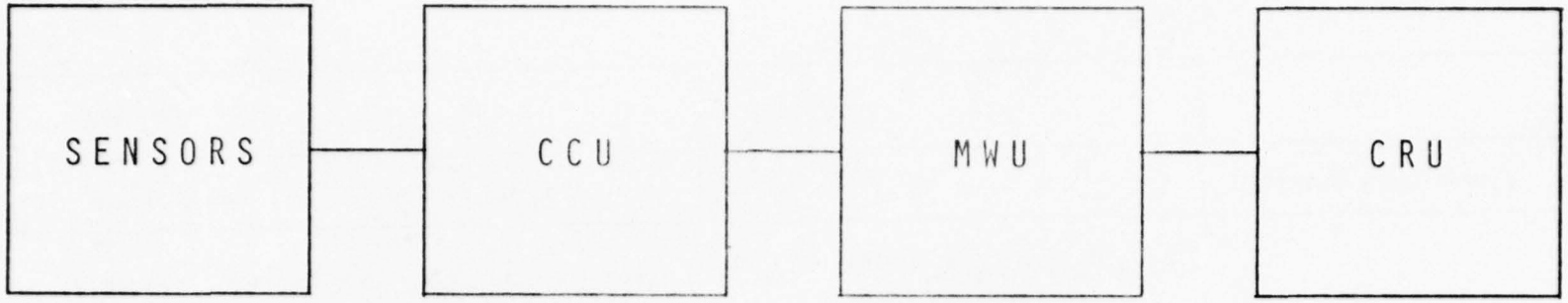
Description	Stress Factor	$\lambda_b (\pi_E \times \pi_R \times \pi_Q)$	Failure Rate x 10^{-6}
RN	.17 .5	.0022 (5 x 1)	.011 .017
RW	.33 .5	.0064 (15 x 1 x 5)	.375 .48

2.7 Potentiometer

Reference: MIL Handbook 217B
Formula (MIL Handbook 217B, pg. 2.5.6-1): $\lambda_p = \lambda_b \pi_{taps} (\pi_R \times \pi_V \times \pi_Q \times \pi_E)$

Description	Stress Factor	$\lambda_b \pi_{taps} (\pi_R \times \pi_V \times \pi_Q \times \pi_E)$	Failure Rate x 10^{-6}
Potentiometer	.1		15.14

RELIABILITY MODEL



Drawing	Failures (10^6 Hrs.)
44195	151.11
44195	151.11
44195	151.11
44195	151.11
44195	151.11
44195	151.11
Σλ for Sensors	906.66

Drawing	Failures (10^6 Hrs.)
44014	121.80
44014	121.80
44023	147.24
44068	81.30
44215B	.56
44205	9.96
44132	112.16
44135	92.90
44139	43.38
44192	90.87
44126	37.13
44061	195.12
44061	195.12
44073	135.51
44012	96.80
44010	83.59
44015	95.36
44198-3	19.18
Σλ for CCU	1679.78

Drawing	Failures (10^6 Hrs.)
44204	33.68
44203-2	37.83
44021C	18.79
44198-2	14.91
44201	36.25
Σλ for MWU	141.46

Drawing	Failures (10^6 Hrs.)
44053	17.27
44197	20.72
44198-1	14.91
44203-1	37.83
Σλ for CRU	90.73

SENSORS	909.66
CCU	1679.78
CRU	141.46
MWU	90.73

$\Sigma\lambda = 2818.63 \times 10^{-6}$

$$MTBF = \frac{1}{\Sigma\lambda} = 355 \text{ HRS}$$

Sheet No 1 of 1

SUB SYSTEM: _____

ASS'Y DWG. NO. C44195

ASS'Y TITLE Component Board Assembly

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1		B-42743 Sensor Tube	2			46.45	92.90	
2		A-1599 U/V Glow Tube	1			46.45	46.45	
3	R1	37K, WW	1	7.5W		1.06	1.06	
4	R2-R5	91K, WW	4	7.5W		1.06	4.24	
5	R6, R7	182Ω, WW	2	1W		.69	1.38	
6		Wire, Bare, Nickel Ribbon	AR			.30	.30	
7		Cable, Stranded	15 ft			2.40	2.40	
8		Cable, Single Cond.	45 ft			2.00	2.00	
9	J1	Connector	1			.38	.38	
		TOTAL					151.11	

Sheet No. 1 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44014

ASS'Y TITLE Fire Warning Logic

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1		Printed Ckt. Conn. 00-8219-054-00-002	1			2.34	2.34	
2-7	U1-U6	SN54L74J (TI or Equiv.)	6			8.85	53.10	
8	U7	SN54L10J (TI or Equiv)	1			4.58	4.58	
9	U8	SN54L03J "	1			4.69	4.69	
10	U9	SN54L10J "	1			4.58	4.58	
11	U10	SN54L03J "	1			4.69	4.69	
12	U11	SN54L10J "	1			4.58	4.58	
13	U12	SN54L03J °	1			4.69	4.69	
14	U13	SN54L04J "	1			6.38	6.38	
15	U14	SN54L20J "	1			3.95	3.95	
16	U15	SN54L06J '	1			7.05	7.05	
17	U16	SN54L20J "	1			3.95	3.95	
18	U17	SN54L10J "	1			5.28	5.28	
19	U18	SN54L10J "	1			5.28	5.28	
20	U19	SN54L05J "	1			5.59	5.59	
21	C1	68 mF 15V (Mallory) TAS686M015P1F	1	15V	5V	.007	.007	
22	C2	0.1 mF (Erie) 8131-M050-W5R-104M	1	50V	5V	.092	.092	

Sheet No. 2 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44014

ASS'Y TITLE Fire Warning Logic

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate per 10^6 Hrs/Part	Total Failure Rate	Notes
23	C3	0.1 mF (Erie) 8131-M050-W5R-104M	1	50V	5V	.092	.092	
24-28	C4-C8	0.1 mF (Erie) 8131-M050-W5R-104M	5	50V	5V	.092	.46	
29-37	R1-R9	1.0K ohm 1/2W RC20GF102J	9	1/2W		.042	.378	
38	R10	510 ohm 1/2W	1	1/2W		.042	.042	
						TOTAL (2 pages)	121.80	

Sheet No. 1 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44023

ASS' TITLE Clock Generator

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	U1	SN54L10J	1			4.58	4.58	
2	U2	SN54L10J	1			4.58	4.58	
3	U3	SN54L93J	1			14.70	14.70	
4	U4	SN54L93J	1			14.70	14.70	
5	U5	SN54L90J	1			15.15	15.15	
6	U6	SN54L93J	1			14.70	14.70	
7	U7	SN54L86J	1			2.93	2.93	
8	U8	SN54L00J	1			5.28	5.28	
9	U9	SN54L86J	1			2.93	2.93	
10	U10	SN54L00J	1			5.28	5.28	
11	U11	SN54L30J	1			2.93	2.93	
12	U12	SN54L20J	1			3.95	3.95	
13	U13	SN54L04J	1			6.38	6.38	
14	U14	SN5405J	1			6.38	6.38	
15	U15	SN5404J	1			6.38	6.38	
16	U16	SN5400J	1			5.28	5.28	
17	U17	SN54L04J	1			6.38	6.38	
18	U18	SN54L04J	1			6.38	6.38	
19	U19	AM26L0251E	1			14.70	14.70	

Sheet No. 2 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44023

ASS'Y TITLE Clock Generator

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
20	C1	.01 mF (TRW) X440UW0.10mF50V	1	50V	5V	.004	.004	
21	C2	82 mF (Kemet) T330D826K015AS	1	15V	5V	.007	.007	
22-24	C3-5	82 mF (Kemet) T330D826K015AS	3	15V	5V	.007	.021	
25	C6	-						
26	C7	18 mF (Kemet) T330C186K015AS	1	15V	5V	.007	.007	
27	C8	3.3 mF (Kemet) T330B335K025AS	1	25V	5V	.006	.006	
28	C9	.01 mF (Erie) 8131-M050-W5R-104M or 8131-M050-XTR-104M	1	50V	5V	.092	.092	
29-34	C10-14	0.1 mF (Erie)	5	50V	5V	.092	.46	
35	C15	68 mF (Mallory)	1	15V	5V	.007	.007	
36	C16	0.1mF (Erie)	1	50V	5V	.092	.092	
37	R1	1.37K Ohms RN60C1371F	1	1/8W		.015	.015	
38	R2	10.7K Ohms RN60C1072F	1	1/8W		.013	.013	

Sheet No. 3 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44023

ASS'Y TITLE Clock Generator

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
39	R3	1.0K RC20GF102J	1	1/2W		.042	.042	
40	R4							
41	R5	215 ohms RN55C2150F	1	1/10W		.022	.022	
42	R6	215 ohms RN55C2150F	1	1/10W		.022	.022	
43	R7	39.2K RN55C3922F	1	1/10W		.013	.013	
44	R8	2.0K RC20GF202J	1	1/2W		.042	.042	
45	R9	1.0K RC20GF102J	1	1/2W		.042	.042	
46	CR3	1N3611 (Unitrode)	1			.472	.472	
47	CR4	1N3611 (Unitrode)	1			.472	.472	
48	CR1	FD700 (Fairchild)	1			.94	.94	
49		PC Connector (Elco) 00-8219-018-00-002	1			.86	.86	

TOTAL (3 pages) 147.241

Sheet No. 1 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44068

ASS'Y TITLE Voltage Monitor/ Reference Supply

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
		P.C. Conn. (Elco) 00-8219-030-600-002				1.27	1.27	
1	C1	180MF (Sprague) 130D187X0050T2	1	50V	5V	.004	.004	
2	C2	68 mF (Mallory) TA5686M015PIF	1	15V	5V	.007	.007	
3	C3	0.1 mF (Erie) B131-M050-W5R-104M	1	50V	5V	.092	.092	
4	C4	0.1 mF (Erie)	1	50V	5V	.092	.092	
5	C5	0.1 mF (Erie)	1	50V	5V	.092	.092	
6	C6	68 mF (Mallory)	1	15V	5V	.007	.007	
7	C7	0.1 mF (Erie)	1	50V	5V	.092	.092	
8	C8	0.22 mF (Erie) B131-M050-W5R-224K	1	50V	5V	.092	.092	
9	C9	0.22 mF (Erie)	1	50V	5V	.092	.092	
10	C10	0.1 mF (Erie)	1	50V	5V	.092	.092	
11	C11	0.0015 mF (Erie)	1	50V	5V	.092	.092	
12	C12	0.1 mF (Erie)	1	50V	5V	.092	.092	
13	C13	22 mF (Kemet)	1	10V	5V	.013	.013	
14	C14	270 mF (Sprague) 130D277X003T2	1	30V	5V	.006	.006	

Sheet No. 2 of 5

ASS'Y DWG. NO. D-44068

SUB SYSTEM: CCU

ASS'Y TITLE Voltage Monitor/ Reference Supply

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate per 10^6 Hrs/Part	Total Failure Rate	Notes
15	C15	270 mF (Sprague)	1	30V		.006	.006	
16	C16	68 mF (Kemet) T330D686M015AS	1	15V		.007	.007	
17	C17	68 mF (Kemet)	1	15V		.007	.007	
18	C18	0.15 mF (Erie) 8131-M050-W5R-154K	1	50V		.092	.092	
19 & 20	C19,20	0.15 mF (Erie)	2	50V		.092	.184	
21	C21	0.10 mF (Erie) 8131-M050-W5R-104K	1	50V		.092	.092	
22-24	C22-24	0.1 mF (Erie)	3	50V	5V	.092	.276	
25	CR1	1N3611 (Unitrode)	1	200V		.47	.47	
26-28	CR2-4	1N483B	3	60V		.19	.57	
29-31	U1-3	LH2111D (Nat.)	3	60V		8.81	26.43	
32	U4	SN54L10J (TI)	1			4.58	4.58	
33	U5	SN5406J (TI)	1			7.05	7.05	
34	U6	Pos. voltage Reg. (Mot) MC1569R	1			35.10	35.10	
35-39	Q1-4	2N1711 (Mot)	4			.525	2.10	
40	R1	1K RC20GF102J	1	1/2W		.108	.108	
41	R2	100K RN55E1003B	1	1/10W		.013	.013	

Sheet No. 3 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44068

ASS'Y TITLE Voltage Monitor/ Reference Supply

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
42	R3	100K RN55E1003B	1	1/10W		.013	.013	
43	R4	24.3K RN55E2432B	1	"		.013	.013	
44	R5	20.0K RN55E2002B	1	"		.013	.013	
45	R6	15.0K RN55E1502B	1	"		.013	.013	
46	R7	100K RN55E1003B	1	"		.013	.013	
47	R8	100K RN55E1003B	1	"		.013	.013	
48	R9	21.0K RN55E2102B	1	"		.013	.013	
49	R10	25.2K RN55E2552B	1	"		.013	.013	
50	R11	19.6K RN55E1962B	1	"		.013	.013	
51	R12	510 ohm RC20GF511J	1	1/2W		.108	.108	
52	R13	4.64K RN55C4641F	1	1/10W		.013	.013	
53	R14	RN55C5111F	1	1/10W		.013	.013	
54	R15	221K RN55C2213F	1	"		.013	.013	
55	R16	5.11K RN55E5111B	1	"		.013	.013	
56	R17	49.9K RN55E4992K	1	"		.013	.013	
57	R18	100K RN55E1003B	1	"		.013	.013	
58	R19	100K RN55E1003B	1	"		.013	.013	
59	R20	1.43K RN55E1431B	1	"		.013	.013	

Sheet No. 4 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44068

ASS'Y TITLE Voltage Monitor/ Reference Supply

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
60	R21	4.12K RN55E4121B	1	1/10W		.013	.013	
61	R22	25.5K RN55E2552B	1	"		.013	.013	
62	R23	25.5K RN55E2552B	1	"		.013	.013	
63	R24	4.64K RN55C4641F	1	"		.013	.013	
64	R25	1K RC20GF102J	1	1/2W		.108	.108	
65	R26	51 ohm RC20GF510J	1	1/2W		.108	.108	
66	R27	20 ohm RN55C20R0F	1	1/10W		.022	.022	
67	R28	1.91K RN55E1911B	1	"		.013	.013	
68	R29	6.81K RN55E6811B	1	"		.013	.013	
69	R30	-						
70	R31	15 ohm RS-2B (Dale)	1	3W		.638	.638	
71	R32	4.75K RN55C4751F	1	1/10W		.013	.013	
72	R33	15 ohm RS-2B (Dale)	1	3W		.638	.638	
73	R34	4.75K RN55C4751F	1	1/10W		.013	.013	
74	R35	392 ohm RN55C3920F	1	"		.022	.022	
75 & 76	R36,37	221 ohm RN60C2210F	2	"		.022	.044	
77	R38	100K RN55C1003F	1	1/10W		.013	.013	
78	R39	4.75K RN55C4751F	1	"		.013	.013	

Sheet No. 5 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44068

ASS'Y TITLE Voltage Monitor/ Reference Supply

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
79	R40	12.1K RN55C1212F	1	1/10W		.013	.013	
80	R41	-						
81	R42	-						
82	R43	5.11K RN55C5111F	1	1/10W		.013	.013	
83	R44	5.11K RN55C5111F	1	1/10W		.013	.013	

Sheet No. 1 of 1

SUB SYSTEM: CCU

ASS'Y DWG. NO. B-44215B

ASS'Y TITLE 30V Network

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	R1	RN65C232F	1	1/4W		.022	.022	
2	R2	RN65C2323F	1	1/4W		.022	.022	
3	R3	RN60C1001F	1	1/8W		.022	.022	
4	R4	RN55D2150F	1	1/10W		.022	.022	
5	R5	RN60D1331F	1	1/8W		.022	.022	
6	R6	RN75C1823F	1	1W		.022	.022	
7	R7	RC20GF122J	1	1/2W		.108	.108	
8	R8	RC20GF512J	1	"		.108	.108	
9	Q1	2N3439 (Mot)	1			.105	.105	
10	Q2	2N3439 (Mot)	1			.105	.105	
					TOTAL		.558	

Sheet No. 1 of 1

SUB SYSTEM: CCU

ASS'Y DWG. NO. C-44205

ASS'Y TITLE Driver Board

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1-14	R1-14	1K, RN55	14	1/10W	.05W	.022	.308	
15	R15	5.11K RN55	1	"	.05W	.022	.022	
16	R16	5.11K, RN55	1	"	.05W	.022	.022	
17	C1	0.1 mF 8131 (Erie)	1	50V	5V	.092	.092	
18	C2	82 mF (Kemet) T330D826K015AS	1	15V	5V	.079	.079	
19	U1	SN5406J	1			7.10	7.10	
20	J1	PC Conn. (Elco) 00-8219-054-000-002	1			2.34	2.34	
						TOTAL	9.963	

Sheet No. 1 of 4

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44132

ASS'Y TITLE CFA & EFA Logic

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
		PC Connector 00-8219-054-000-002	1			2.34	2.34	
1 & 2	U1&U2	SN54L04J (T.I. or Eq.)	2			6.38	12.76	
3-6	U3-6	SN54L00J	4			5.28	21.12	
7	U7	SN54L10J	1			4.58	4.58	
8	U8	SN54L73J	1			10.56	10.56	
9	U9	LH2111D (Nat.)	1			8.81	8.81	
10&11	U10&11	SN54L04J (T.I. or Eq.)	2			6.38	12.76	
12	U12	SN54L10J	1			4.58	4.58	
13-15	U13-15	SN54L00J	3			5.28	15.84	
16	U16	SN54L02J	1			6.38	6.38	
17	U17	LH2111D (Nat.)	1			8.81	8.81	
18	R1	1K 1/10W RN55D1001F	1	1/10W	.01W	.013	.013	
19	R2	1K 1/10W	1	1/10W	.01W	.013	.013	
20	R3	30.1K 1/10W RN55D3012F	1	1/10W	.01	.013	.013	
21	R4	30.1K 1/10W	1	1/10W	.01	.013	.013	
22	R5	30.1K RN55R3011F	1	1/10W	.01	.013	.013	
23	R6	1K 1/10W RN55D1001F	1	1/10W	.01	.013	.013	

Sheet No. 2 of 4

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44132

ASS'Y TITLE *CFA & EFA Logic*

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
24	R7	1K 1/10W	1	1/10W	.01W	.013	.013	
25	R8	39.2K 1/10W RN55D3922F	1	1/10W	.01W	.013	.013	
26	R9	39.2K 1/10W	1	1/10W	.01W	.013	.013	
27	R10	1K 1/10W RN55D1001F	1	"	"	.016	.016	
28	R11	2K 1/10W RN55D2001F	1	"	"	.013	.013	
29	R12	2K 1/10W	1	1/10W	.01W	.013	.013	
30	R13	1K, 1/10W RN55D1001F	1	1/10W	.02W	.016	.016	
31	R14	1K, 1/10W	1	"	.02W	.016	.016	
32	R15	274 ohms, 1/10W RN60C2740D	1	1/10W		.013	.013	
33	R16	20K 1/10W RN55D2002F	1	1/10W		.013	.013	
34	R17	20K 1/10W	1	"		.013	.013	
35	R18	15.0K 1/10W RN55D1502F	1	"		.013	.013	
36	R19	15.0, 1/10W	1	"		.013	.013	
37	R20	2K, 1/10W RN55D2001F	1	"		.013	.013	

Sheet No. 3 of 4

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44132

ASS'Y TITLE CFA & EFA Logic

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
38	R21	2K 1/10W	1	1/10W		.013	.013	
39	R22	2K 1/10W RN55D2001F	1	1/10W		.013	.013	
40	C1	0.1 mF (Erie) CK06BX104K	1	100V	5V	.092	.092	
41	C2	.0022 mF CK05BX222K	1	200V	5V	.092	.092	
42	C3	82 mF (Kemet) T330D826K-015AS	1	15V	5V	.01	.01	
43	C4	0.1 mF (Erie) CK06BX104K	1	100V	"	.092	.092	
44	C5	.56 mF (Gudeman) F410A564S-5	1	50V	"	.092	.092	
45	C6	0.1 mF (Erie) CK06BX104K	1	100V	"	.092	.092	
46-50	C7-11	0.1 mF (Erie)	5	100V	"	.092	.46	
50	C12	0.1 mF (Erie)	1	100V	"	.092	.092	
52	C13	.56 mF (Gudeman) F410A564S-5	1	50V	"	.092	.092	

Sheet No. 4 of 4

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44132

ASS'Y TITLE CFA & EFA Logic

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
53	C14	.56 mF (Gudeman) F410A564S-5	1	50V	5V	.092	.092	
54	C15	0.1 mF (Erie)	1	100V	"	.092	.092	
55	C16	.56 mF (Gudeman) F410A564S-5	1	50V	"	.092	.092	
56	C17	0.1 mF (Erie) CK06BX104K	1	100V	"	.092	.092	
57	C18	0.1 mF (Erie)	1	100V	"	.092	.092	
58-69	C19-29	0.1 mF (Erie)	11	100V	"	.092	1.012	
70	C30	.56 mF (Gudeman) F410A564S-5	1	50V	"	.092	.092	
71	C31	.56 (Gudeman)	1	50V	"	.092	.092	
72-78	C32-37	0.1 mF (Erie)	6	100V	"	.092	.552	
						TOTAL (4 Pages)	112.16	

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SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44135

ASS'Y TITLE Multi Output (A13)

"A" Board

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	U1	SN54L20J (T.I. or Eq.)	1			3.95	3.95	
2	U2	SN54L04J "	1			6.38	6.38	
3	U3	SN54L73J "	1			10.38	10.38	
4	U4	SN54L00J "	1			5.28	5.28	
5	U5	LH2111D (Nat. or Eq.)	1			9.81	9.81	
6	U6	LH2111D "	1			9.81	9.81	
7	U7	SN54L10J (T.I. or Eq.)	1			4.58	4.58	
8	U8	SN54L10J "	1			4.58	4.58	
9	U9	AM261L0251E	1			10.69	10.69	
10	U10	SN54L04J (T.I. or Eq.)	1			6.38	6.38	
11	J1	00-8219-054-000-002	1			2.34	2.34	
12	U11	SN5406J (T.I. or Eq.)	1			7.05	7.05	
13	U12	SN5406J "	1			7.05	7.05	
14	CR1	1N456	1			.945	.945	
15	CR2	1N456	1			.945	.945	
16	R1	1KRN55D1001F	1	1/10W	.02	.015	.015	
17	R2	200 ohms RN55D2000F	1	"		.013	.013	

Sheet No. 2 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44135

ASS'Y TITLE Multi Output (A13)
"(A)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
18	R3	15K RN55D1502F	1	1/10W		.013	.013	
19	R4	15K RN55D1502F	1	"		.013	.013	
20	R5	5.11K RN55D5111F	1	"		.013	.013	
21	R6	1K RN55D1001F	1	"		.015	.015	
22	R7	3.01K RN55D3011F	1	"		.013	.013	
23	R8	1K RN55D1001F	1	"		.015	.015	
24	R9	200 ohms RN55D2000F	1	"		.013	.013	
25	R10	20K RN55D2002F	1	"		.013	.013	
26	R11	20K RN55D2002F	1	"		.013	.013	
27	R12	2K RN55D2001F	1	"		.013	.013	
28	R13	1K RN55D1001F	1	"		.015	.015	
29	R14	1K RN55D1001F	1	"		.015	.015	
30	R15	562 ohms RN55D5620F	1	"		.013	.013	
31	R16	12.1K RN55D1212F	1	"		.013	.013	
32	R17	12.1K RN55D1212F	1	"		.013	.013	
33	R18	5.11 RN55D5111F	1	"		.013	.013	
34	R19	1K RN55D1001F	1	"		.015	.015	

Sheet No. 3 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44135

ASS'Y TITLE Multi Output (A13) "(A)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
35	R20	511 ohms RN55D5110F	1	1/10W	.05W	.022	.022	
36	R21	1K RN55D1001F	1	1/10W	.02W	.015	.015	
37	R22	562 ohms RN55D5620F	1	"		.013	.013	
38	R23	12.1K RN55D1212F	1	"		.013	.013	
39	R24	12.1K RN55D1212F	1	"		.013	.013	
40	R25	5.11K RN55D5111F	1	"		.013	.013	
41	R26	1K RN55D1001F	1	"	.02W	.015	.015	
42	R27	1K RN55D1001F	1	"	.02W	.015	.015	
43	R28	20K RN55D2002F	1	"		.015	.015	
44	R29	511 ohms RN55D5110F	1	"	.05	.022	.022	
45	R30	30.1K RN55D3012F	1	"		.013	.013	
46	C1	.1 mF CK06BX104K	1	100V	5V	.092	.092	
47	C2	.1 mF CK06BX104K	1	"	5V	.092	.092	
48	C3	.0022 mF CK05BX222K	1	200V	5V	.092	.092	
49	C4	.1 mF CK06BX104K	1	100V	5V	.092	.092	
50	C5	.1 mF CK06BX104K	1	"	5V	.092	.092	
51	C6	82 mF (Kemet) T330D826K015AS	1	15V	"	.007	.007	

Sheet No. 4 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44135

ASS'Y TITLE Multi Output (A13)

"(A)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
52	C7	.1 mF CK06BX104K	1	100V	5V	.092	.092	
53	C8	.1 mF CK06BX104K	1	"	"	.092	.092	
54	C9	3.3 mF (Kemet) T330B335K035AS	1	23V	"	.006	.006	
55	C10	22 mF (Kemet) T330C226K015AS	1	10V	"	.013	.013	
56	C11	82 mF (Kemet)	1	15V	"	.007	.007	
57	C12	82 mF (Kemet)	1	"	"	.007	.007	
58	C13	.1 mF CK06BX104K	1	100V	"	.092	.092	
59	C14	.1 mF CK06BX104K	1	"	"	.092	.092	
60	C15	.1 mF CK06BX104K	1	"	"	.092	.092	
61	C16	.1 mF CK06BX104K	1	"	"	.092	.092	
62	C17	.1 mF CK06BX104K	1	100V	"	.092	.092	
63	C18	3.3 mF (Kemet)	1	23V	"	.006	.006	
64	C19	82 mF (Kemet)	1	15V	"	.007	.007	
65	C20	.1 mF CK06BX104K	1	100V	"	.092	.092	
66	C21	.1 mF CK06BX104K	1	"	"	.092	.092	
67	C22	82 mF (Kemet)	1	15V	"	.007	.007	

Sheet No. 5 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44135

ASS'Y TITLE Multi Output (A13)

"(A)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
68	C23	3.3 mF (Kemet)	1	23V	5V	.006	.006	
69	C24	82 mF (Kemet)	1	15V	"	.007	.007	
70	C25	.1 mF CK06BX104K	1	100V	"	.092	.092	
71	C26	3.3 mF (Kemet)	1	23V	"	.006	.006	
72	C27	.1 mF CK06BX104K	1	100V	"	.092	.092	
73	C28	3.3 mF (Kemet)	1	23V	"	.006	.006	
74	C29	.1 mF CK06BX104K	1	100V	"	.092	.092	
75	C30	3.3 mF (Kemet)	1	23V	"	.006	.006	
76	C31	.1 mF CK06BX104K	1	100V	"	.092	.092	
77	C32	82 mF (Kemet)	1	15V	"	.007	.007	
78	C33	82 mF (Kemet)	1	"	"	.007	.007	
79	C34	.1 mF CK06BX104K	1	100V	"	.092	.092	
80	C35	.1 mF CK06BX104K	1	"	"	.092	.092	
81	C36	.1 mF CK06BX104K	1	"	"	.092	.092	
82	C37	.1 mF CK06BX104K	1	"	"	.092	.092	
83	C38	.1 mF CK06BX104K	1	"	"	.092	.092	
84	C39	.1 mF CK06BX104K	1	"	"	.092	.092	
						TOTAL (5 pages)	92.90	

Sheet 1 of 1

ASS'Y DWG. NO. D-44139

SUB SYSTEM: CCU

ASS'Y TITLE Signal Correlator

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	U1	SN5406J (T.I. or Eq.)	1			7.05	7.05	
2	U2	SN5406J "	1			7.05	7.05	
3	U3	SN54L00J	1			5.28	5.28	
4	U4	SN54L02J	1			6.38	6.38	
5	U5	SN54L20J	1			3.95	3.95	
6	U6	SN54L10J	1			4.58	4.58	
7	U7	SN54L04J	1			6.38	6.38	
8	R1	1K RN55D1001F	1	1/10W	.025	.016	.016	
9-12	R2-4	1K RN55D1001F	3	"	"	.016	.048	
13	R5	1K RN55D1001F	1	"	"	.015	.015	
14	C1	82 mF (Kemet)	1	15V	5V	.01	.01	
15-17	C2-4	0.1 mF CK06BX104K	3	100V	5V	.092		
18	J3	PC Connector 00-8219-054-000-002	1	100V	5V	2.34	2.34	
						TOTAL	43.38	

Sheet 1 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44192

ASS'Y TITLE Multi Output "(B)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	
1	J1	PC Connector 00-8219-054-000-002	1			2.34	2.34	
2	U1	SN54L20 (T.I. or Eq.)	1			3.95	3.95	
3	U2	SN54L04J	1			6.38	6.38	
4	U3	SN54L73J	1			10.38	10.38	
5	U4	SN54L00J	1			5.28	5.28	
6	U5	LH2111D (Nat. or Eq.)	1			8.81	8.81	
7	U6	LH2111D "	1			8.81	8.81	
8	U7	SN54L10J (T.I. or Eq.)	1			4.58	4.58	
9	U8	SN54L10J "	1			4.58	4.58	
10	U9	AM26L0251E	1			10.69	10.69	
11	U10	SN54L04J (T.I. or Eq.)	1			6.38	6.38	
12	U11	SN5406	1			7.05	7.05	
13	U12	SN5406J	1			7.05	7.05	
14	CR1	1N456	1			.945	.945	
15	CR2	1N456	1			.945	.945	
16	R1	1K RN55D	1	1/10W	.01W	.013	.013	
17	R2	200 RN55D	1	"	"	.013	.013	
18	R3	15K RN55D	1	"	"	.013	.013	

Sheet 2 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44192

ASS'Y TITLE Multi Output "(B)" Board

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
19	R4	15K RN55D	1	1/10W	.01W	.013	.013	
20	R5	5.11K RN55D	1	"	"	.013	.013	
21	R6	1K RN55D	1	"	"	.013	.013	
22	R7	3.01K RN55D	1	"	"	.013	.013	
23	R8	1K "	1	"	"	.013	.013	
24	R9	55D	1	"	"	.013	.013	
25	R10	20K "	.	"	"	.013	.013	
26	R11	20K "	1	"	"	.013	.013	
27	R12	2K "	1	"	"	.013	.013	
28	R13	1K "	1	"	"	.013	.013	
29	R14	1K "	1	"	"	.013	.013	
30	R15	562 "	1	"	"	.013	.013	
31	R16	12.1K "	1	"	"	.013	.013	
32	R17	12.1K "	1	"	"	.013	.013	
33	R18	5.11K "	1	"	"	.013	.013	
34	R19	1K "	1	"	"	.013	.013	
35	R20	-						

Sheet No. 3 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44192

ASS'Y TITLE Multi-Output "(B)" Board

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
36	R21	1K RN55D	1	1/10W	.01W	.013	.013	
37	R22	562 RN55D	1	"	"	.013	.013	
38	R23	12.1K "	1	"	"	.013	.013	
39	R24	12.1K "	1	"	"	.013	.013	
40	R25	5.11K "	1	"	"	.013	.013	
41	R26	1K "	1	"	"	.013	.013	
42	R27	1K "	1	"	"	.013	.013	
43	R28	20K "	1	"	"	.013	.013	
44	R29	200 "	1	"	"	.013	.013	
45	R30	30.1K "	1	"	"	.013	.013	
46	C1	.1 mF CK06	1	100V	5V	.092	.092	
47	C2	.1 mF "	1	"	"	.092	.092	
48	C3	.0022 mF CK06	1	"	"	.092	.092	
49	C4	.1 mF "	1	"	"	.092	.092	
50	C5	.1 mF "	1	"	"	.092	.092	
51	C6	82 mF (Kemet) T330D	1	15V	"	.007	.007	
52	C7	.1 mF CK06	1	100V	"	.092	.092	
53	C8	.1 mF CK06	1	100V	"	.092	.092	

Sheet No. 4 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44192

ASS'Y TITLE Multi Output "(B)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
54	C9	3.3 mF T330 (Kemet)	1	23V	5V	.006	.006	
55	C10	22 mF T330 (Kemet)	1	10V	"	.008	.008	
56	C11	82 mF (Kemet) T330	1	15V	"	.007	.007	
57	C12	82 mF (Kemet) T330	1	15V	"	.007	.007	
58	C13	.1 mF CK06	1	100V	"	.092	.092	
59	C14	.1 mF CK06	1	"	"	.092	.092	
60	C15	.1 mF CK06	1	"	"	.092	.092	
61	C16	.1 mF CK06	1	"	"	.092	.092	
62	C17	.1 mF CK06	1	"	"	.092	.092	
63	C18	3.3 mF T330	1	23V	"	.006	.006	
64	C19	82 mF (Kemet) T330	1	15V	"	.007	.007	
65	C20	.1 mF CK06	1	100V	"	.092	.092	
66	C21	.1 mF CK06	1	"	"	.092	.092	
67	C22	82 mF (Kemet) T330	1	15V	"	.007	.007	
68	C23	3.3 mF T330	1	23V	"	.006	.006	
69	C24	82 mF (Kemet) T330	1	15V	"	.007	.007	
70	C25	.1 mF CK06	1	100V	"	.092	.092	
71	C26	3.3 mF T330 (Kemet)	1	23V	"	.006	.006	

Sheet No. 5 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44192

ASS'Y TITLE Multi Output "(B)" Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
72	C27	.1 mF CK06	1	100V	5V	.092	.092	
73	C28	3.3 mF T330	1	23V	"	.006	.006	
74	C29	.1 mF CK06	1	100V	"	.092	.092	
75	C30	3.3 mF T330	1	23V	"	.006	.006	
76	C31	.1 mF CK06	1	100V	"	.092	.092	
77	C32	82 mF (Kemet) T330	1	15V	"	.007	.007	
78	C33	82 mF (Kemet) T330	1	15V	"	.007	.007	
79-84	C34-39	.1 mF CK06	6	100V	"	.092	.552	

TOTAL (5 pages) 90.87

Sheet No. 1 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44126

ASS'Y TITLE O/H Signal Processor "A"

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	R1	1K RN60C1001D	1	1/8W	.2W	.015	.015	
2-4	R2-4	1K RN60C1001D	3	1/8W	.2W	.015	.045	
5	R5	150 RN55C1500F	1	1/10W	.05W	.022	.022	
6	R6	232 RN60C2320D	1	1/8W		.013	.013	
7	R7	284 RN60C2840D	1	1/8W		.013	.013	
8	R8	67.3 RN55C67R3F	1	1/10W		.013	.013	
9	R9	10K RN55C1002F	1	"		.013	.013	
10	R10	10K RN55C1002F	1	"		.013	.013	
11	R11	750K RN60D7503F	1	1/8W		.013	.013	
12	R12	750K RN60D7503F	1	"		.013	.013	
13	R13	511 RN55C5110F	1	1/10W	.05W	.022	.022	
14&15	R14-15	10K RN55C1002F	2	1/10W		.013	.026	
16&17	R16-17	750K RN60D7503F	2	1/8W		.013	.026	
18	R18	2K RN55D2001F	1	1/10W		.013	.013	
19&20	R19&20	1K RN55D1001F	2	"		.013	.026	
21&22	R21&22	15K RN55D1502F	2	"		.013	.026	
23	R23	511 RN55C5110F	1	"	.05W	.022	.022	
24&25	R24&25	10K RN55C1002F	2	"		.013	.026	

Sheet No. 2 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44126

ASS'Y TITLE O/H Signal Processor "A"

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
26&27	R26&27	750K RN60D7503F	2	1/8W		.013	.026	
28	R28	511 RN55C5110F	1	1/10W	.05W	.013	.013	
29	R29	10K RN55C1002F	1	1/10W		.013	.013	
30-31	R30&31	1K RN55D1001F	1	1/10W	.1W	.013	.026	
32	R32	10K RN55C1002F	1	1/10W		.013	.013	
33	R33	2K RN55D2001F	1	1/10W		.013	.013	
34	R34	5.11K RN55D5111F	1	"		.013	.013	
35&36	R35-36	2K RN55D2001F	2	"		.013	.026	
37&38	C1-2	.22 mF CK06BX224K	2	50V	5V	.092	.184	
39-41	C3-5	0.1 mF (Erie) 8131-M050-WSR-104M	3	"	"	.092	.276	
42&43	C6&7	.22 mF CK06BX224K	2	50V	5V	.092	.184	
44&45	C8&9	0.1 mF (Erie)	2	"	"	.092	.184	
46&47	C10&11	.22 mF CK06BX224K	2	"	"	.092	.184	
48-59	C12-23	0.1 mF (Erie)	12	"	"	.092	1.104	
60&61	C24&25	68 mF (Mallory) TAS686M015P1F	2	15V	"	.007	.014	
62&63	C26&27	.27 mF (Gudeman) F410A2745-5	2	50V	"	.092	.184	
64-69	CR1-5	1N456 (T.1.)	5			.945	4.725	

Sheet No. 3 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44126

ASS'Y TITLE O/H Signal Processor "A"

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
70	Q1	2N1711 (T.I. or Eq.)	1			.53	.53	
71	U1	LH2111D (Nat. or Eq.)	1			6.54	6.54	
72	U2	SN5406J (T.I. or Eq.)	1			7.10	7.10	
73	U3	LH2111D (Nat. or Eq.)	1			6.54	6.54	
74	U4	LH2111D "	1			6.54	6.54	
75	J1	PC Connector 00-8219-054	1			2.34	2.34	
						TOTAL (3 pages)	37.13	

Sheet No. 1 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44061

ASS'Y TITLE U/V Signal Processor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	U1	SN54L20J (T.I. or Eq.)	1			3.95	3.95	
2	U2	26 L0251E (Fairchild or Eq.	1			10.69	10.69	
3	U3	SN54L93J (T.I. or Eq.)	1			14.70	14.70	
4	U4	SN54L93J "	1			14.70	14.70	
5	U5	LH2111D (Nat. or Eq.)	1			8.81	8.81	
6	U6	LH2111D "	1			8.81	8.81	
7	U7	SN54L20J	1			3.95	3.95	
8	U8	26L0251E (Fairchild or Eq.)	1			10.69	10.69	
9	U9	SN54L93J	1			14.70	14.70	
10	U10	SN54L93J	1			14.70	14.70	
11	J1	00-8219-030-000-002 P.C. Connector	1			1.27	1.27	
12	U11	LH2111D	1			8.81	8.81	
13	U12	LH2111D	1			8.81	8.81	
14	U13	SN54L20J	1			3.95	3.95	
15	U14	26L0251E (Fairchild or Eq.)	1			10.69	10.69	
16	U15	SN54L93J	1			14.70	14.70	

Sheet No. 2 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44061

ASS'Y TITLE U/V Signal Processor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
17	U16	SN54L93J	1			14.70	14.70	
18	U17	LH2111D	1			8.81	8.81	
19	U18	LH2111D	1			8.81	8.81	
20	C1	82 mF (Kemet or Eq.) T330D826K015AS	1	15V	5V	.007	.007	
21	C2	82 mF (Kemet or Eq.)	1	"	"	.007	.007	
22	C3	82 mF "	1	"	"	.007	.007	
23	C4	82 mF "	1	"	"	.007	.007	
24	C5	68 mF (Mallory or Eq.) TAS686M015Pie	1	15V	5V	.007	.007	
25	C6	0.1 mF (Erie or Eq.) 8131-M050-X7R-104K	1	50V	"	.092	.092	
26	C7	0.1 mF (Erie or Eq.)	1	50V	"	.092	.092	
27-30	C8-11	0.1 mF "	4	"	"	.092	.368	
31	C12	68 mF (Mallory or Eq.)	1	15V	"	.007	.007	
32	C13	0.1 mF (Erie or Eq.)	1	50V	"	.092	.092	
33	C14	82 mF (Kemet or Eq.)	1	15V	"	.007	.007	
34	C15	82 mF "	1	15V	"	.007	.007	
35	C16	82 mF "	1	"	"	.007	.007	
36	C17	82 mF "	1	"	"	.007	.007	

Sheet No. 3 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44061

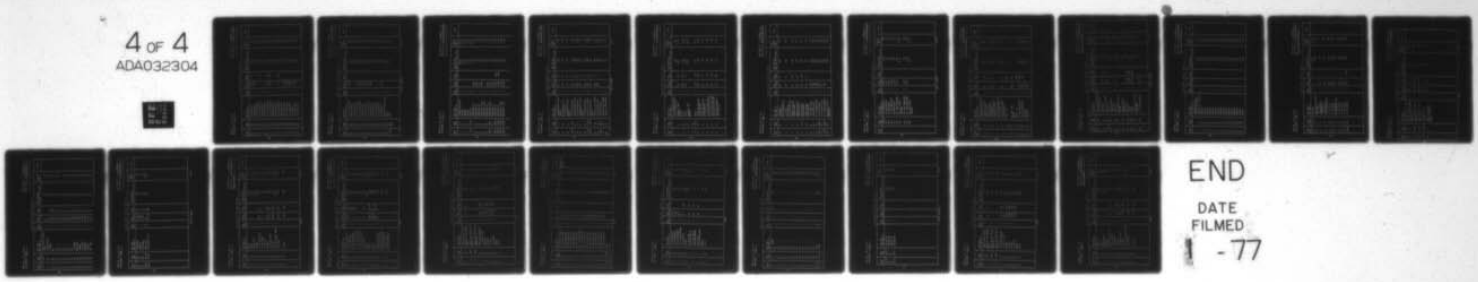
ASS'Y TITLE U/V Signal Processor

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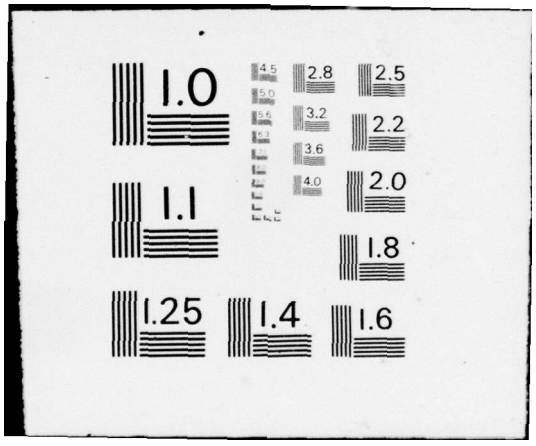
Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
37	C18	82 mF (Kemet or Eq.)	1	15V	5V	.007	.007	
38	C19	82 mF "	1	"	"	.007	.007	
39	C20	82 mF "	1	"	"	.007	.007	
40	C21	82 mF "	1	"	"	.007	.007	
41-50	C22-31	0.1 mF (Erie or Eq.)	10	50V	"	.092	.920	
51	R1	100K RN55C1003F	1	1/10W	"	.013	.013	
52	R2	3.01K RN55C3011F	1	1/10W	"	.013	.013	
53	R3	182 ohm RN55C1820F	1	"	"	.013	.013	
54	R4	100K RN55C1003F	1	"	"	.013	.013	
55	R5	3.01K RN55C3011F	1	"	"	.013	.013	
56	R6	470 ohm RC20GF471J	1	1/2W	.25W	.108	.108	
57	R7	182 ohm RN55C1820F	1	1/10W	.05W	.022	.022	
58	R8	100K RN55C1003F	1	"		.013	.013	
59	R9	3.01K RN55C3011F	1	"		.013	.013	
60	R10	470 ohm RC20GF471F	1	1/2W	.25W	.108	.108	
61	R11	100K RN55C1003F	1	1/10W		.013	.013	
62	R12	3.01K RN55C3011F	1	"		.013	.013	
63	R13	26.1K RN55C2612F	1	"		.013	.013	
64	R14	26.1K RN55C2612F	1	"		.013	.013	

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INTEGRATED FIRE AND OVERHEAT DETECTION SYSTEM.(U)
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Sheet No. 4 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44061

ASS'Y TITLE U/V Signal Processor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
65	R15	1K RC20GF102J	1	1/2W	.25	.108	.108	
66	R16	100K RN551003F	1	1/10W		.013	.013	
67	R17	3.01K RN55C3011F	1	"		.013	.013	
68	R18	182 ohm RN55C1820F	1	"	.05W	.108	.108	
69	R19	100K RN55C1003F	1	"		.013	.013	
70	R20	3.01K RN55C3011F	1	"		.013	.013	
71	R21	470 ohm RC20GF471J	1	1/2W	.25W	.108	.108	
72	R22	182 ohm RN55C1820F	1	1/10W	.05W	.108	.108	
73	R23	100K RN55C1003F	1	"		.013	.013	
74	R24	3.01K RN55C3011F	1	"		.013	.013	
75	R25	470 ohm RC20GF471J	1	1/2W	.25W	.108	.108	
76	R26	100K RN55C1003F	1			.013	.013	
77	R27	3.01K RN55C3011F	1	1/10W		.013	.013	
78	R28	26.1K RN55C2612F	1	1/10W		.013	.013	
79	R29	26.1K RN55C2612F	1	1/10W		.013	.013	
80	R30	1K RC20GF102J	1	1/2W		.108	.108	
81	R31	100K RN55C1003F	1	1/10W		.013	.013	
82	R32	3.01K RN55C3011F	1	"		.013	.013	

Sheet No. 5 of 5

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44061

ASS'Y TITLE U/V Signal Processor

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
83	R33	182 ohm RN55C1820F	1	1/10W		.022	.022	
84	R34	100K RN55C1003F	1	"		.013	.013	
85	R35	3.01K RN55C3011F	1	"		.013	.013	
86	R36	470 ohm RN55C471J	1	1/2W		.022	.022	
87	R37	182 ohm RN55C1820F	1	1/10W		.022	.022	
88	R38	100K RN55C1003F	1	1/10W		.013	.013	
89	R39	3.01K RN55C3011F	1	1/10W		.013	.013	
90	R40	470 ohm RC20GF471J	1	1/2W		.108	.108	
91	R41	100K RN55C1003F	1	1/10W		.013	.013	
92	R42	3.01K RN55C3011F	1	"		.013	.013	
93	R43	26.1K RN55C2612F	1	"		.013	.013	
94	R44	26.1K RN55C2612F	1	"		.013	.013	
95	R45	1K RC20GF102J	1	1/2W		.108	.108	
96	CR1	FD700 (Fairchild or Eq.)	1			.94	.94	
97	CR2	FD700	1			.94	.94	
98-101	CR3-CR6	FD700	4			.94	3.76	
						TOTAL (5 pages)	195.12	

Sheet No. 1 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44073

ASS'Y TITLE System Reset Assembly

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	U1	26L02DM (Multivib)	1			10.69	10.69	
2	U2	26L02DM	1			10.69	10.69	
3	U3	DM54L00J	1			5.28	5.28	
4	U4	DM5400J	1			5.28	5.28	
5-16	U5-16	SN54L121J	12			8.175	98.10	
17	R1	RN55C1002F 10K	1	1/10W		.013	.013	
18	R2	RN60C1001F 1K	1	1/8W		.013	.013	
19	R3	RN60C1001F 1K	1	1/8W		.013	.013	
20	R4	RN55C2432F 24.3K	1	1/10W		.013	.013	
21	R5	RN55C3922F 39.2K	1			.013	.013	
22	R6	RN60C1001F 1K	1	1/8W		.013	.013	
23&24	R7&8	RN55C3922F 39.2K	2	1/8W		.013	.026	
25	R9	RN60C1001F 1K	1	1/8W		.013	.013	
26&27	R10&11	RN55C110F 511	2	1/10W	.05W	.022	.044	
28&29	R12&13	RN55C1001F 1K	2	1/10W	.025W	.013	.026	
30&31	R14&15	RN55C2211F 2.21K	2	1/10W		.013	.026	
32&33	R16&17	RN55C5111F 5.11K	2	1/10W		.013	.026	

Sheet No. 2 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44073

ASS'Y TITLE System Reset Assembly

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
34	C1	130D277X0030T2 270 mF Sprague	1	30V	5V	.006	.006	
35	C2	8131-M050-W5R-104K 0.1 mF (Erie)	1	50V	5V	.092	.092	
36	C3	TAS686M015PIF 68 mF Mallory	1	15V	5V	.007	.007	
37&38	C4&5	8131-M050-W5R-104K	2	50V	5V	.092	.184	
39	C6	130D277X0030T2 270 mF	1	30V	5V	.006	.006	
40	C7	8121-M050-W5R-472K	1	50V	5V	.092	.092	
41	C8	T330D826K015AS 82 mF (Kemet)	1	15V	5V	.007	.007	
42	C9	8131-M050-W5R-104K	1	50V	5V	.092	.092	
43-55	C11-21	X463 UW 047 mF (TRW)	12	50V	5V	.004	.048	
56-59	C22-25	8131-M050-W5R-104K (Erie)	4	50V	5V	.092	.368	
60	C26	X483 W2 0.56 mF (TRW)	1	50V	5V	.092	.092	
61	C27	8131-M050-W5R-104K	1	50V	5	.092	.092	
62-64	CR1-3	FD700 Fairchild	3			.94	2.82	
65	Q1	Transistor PNP 2N2905	1			.53	.53	
66	Q2	Transistor NPN 2N1711	1			.79	.79	
						TOTAL (2 pages)	135.51	

Sheet No. 1 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44012

ASS'Y TITLE Switching Regulator

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
		P.C. Connector (Elco) 00-8219-018-000-002				.86	.86	
1	Q1	Regulator (MOT) MC1569R	1	50V	10V	23.90	23.90	
2	Q2	2N1711	1	50V	8.5V	1.125	1.125	
3	Q3	2N1711	1	50V	5V	1.125	1.125	
4	Q4	Regulator (MOT) MC1569R	1			23.90	23.90	
5	CR1	-						
6-9	CR2-5	1N3611	4	1.0A	1 mA	1.56	6.24	
10	C1	100 MF 25V (Sprague) 137D107X0025F2	1	25V	8.5V	.108	.108	
11	C2	100 MF 25V (Sprague) 137D107X0025F2	1	25V	5V	.072	.072	
12	C3	0.1 mF 50V (Erie Red Cap) 8131-M050-W5R-104K	1	50V	8.5V	.108	.108	
13	C4	.0015 mF 50V (Erie Red Cap) 8121A040-W5R-152M	1	50V	8.5V	.108	.108	
14	C5	180 mF 50V (Sprague) 130D187X0050T2	1	50V	28V	.025	.025	

Sheet No. 2 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44012

ASS'Y TITLE Switching Regulator

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
15	C6	.0015MF50V (Erie Red Cap) 8121-A050-W5R-152M	1	50V	5V	.092	.092	
16	C7	0.1 mF 50V (Erie Red Cap) 8131-M050-W5R-104K	1	50V	5V	.092	.092	
17	C8	180MF50v (Sprague) 130D187X0050T2	1	50V	28V	.025	.025	
18	C9	270MF30V (Sprague) 130D277X0030T2	1	30V	5V	.007	.007	
19	C10	22mF15V (Kemet) T330C226K015AS	1	15V	8.5V	.025	.025	
20	C11	22mF15V (Kemet) T330C226K015AS	1	15V	5V	.010	.010	
21	R1	6.81K RN60C 6811F	1	1/8W		.013	.013	
22	R2	6.98K RN60C 6981F	1	1/8W		.013	.013	
23	R3	49.9 ohm RN60C49R9F	1	1/8W		.022	.022	
24-25	R4&R5	46.4K RN60C4642F	2	1/8W		.013	.026	
26	R6	4.71W (Dale) NS-1A	1	1W		.48	.48	
27-28	R7&R8	56.2 ohms RN70C56R2F	2	1/2W		.022	.044	
29	R9	8.87 ohms (Vishay) VKRKR027349	1			.022	.022	

Sheet No. 3 of 3

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44012

ASS'Y TITLE Switching Regulator

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
	R10&11	46.4K RN60C4642F	2	1/8W		.013	.026	
	R12	6.81K RN60C6811F	1	1/8W		.013	.013	
	R13	1K RN60C10001F	1	1/8W		.013	.013	
	R14	75 ohms RN60C75R0F	1	1/8W		.022	.022	
	R15	20K RN55C2002F	1	1/10W		.013	.013	
	R16	49.9 ohms RN60C49R9F	1	1/8W		.022	.022	
	R17	Pot. 5K (Vishay) 1203AY5K				19.10	19.10	
	R18	49.9 ohms RN60C49R9F	1	1/8W		.022	.022	
	R19	49.9 ohms RN60C49R9F	1	1/8W		.022	.022	
	R20	Pot. 5K (Vishay) 1203AY5K				19.10	19.10	
						TOTAL (3 Pages)	96.795	

Sheet No. 1 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. C-44010

ASS'Y TITLE Converter/Inverter
Printed Circuit Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	2	Printed Circuit Connec. 00-8219-018-000-002				.86	.86	
2	C1	270mF30V (Sprague) 130D277X0030T2	1	30V	8.5V	.007	.007	
3	C2	270mF30V (Sprague) 130D277X0030T2	1	30V	5V	.006	.006	
3	C3	0.1 mF (Erie Red Cap) 8131MD50-W5R-104M	1	50V	5V	.013	.013	
4	C4	0.0015 mF (Erie Red Cap) 8121-A050-W5R-152K	1			.013	.013	
5	C5	270 mF 30V (Sprague) 130D277X0030T2	1	30V	5V	.007	.007	
6	C6	43990 . 001	1		800V	.1	.1	
7	C7	-						
8	C8	3mF 400V (TRW) X463UW	1	400V	300V	.1	.1	
9	C9	43990 . 001			800V			
10	R1	100 ohms RN65C1000F	1	1/4W	.125W	.022	.022	
11	R2	100 ohms RN65C1000F	1	1/4W	.125W	.022	.022	
12	R3	RN55C3321F	1	1/10W		.013	.013	
13	R4	RN60C6811F	1	1/8W		.013	.013	

Sheet No. 2 of 2

SUB SYSTEM: CCU

ASS'Y DWG. No. C-44010

ASS'Y TITLE Converter/Inverter
Printed Circuit Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
14	CR3	Diode Bridge (Unitrode) 673-1S or 673-4S	1			8.20	8.20	
15	R5	RN55C10R0F	1	1/10W	.05	.022	.022	
16	R6	200 ohms RW70V2000F	1	1W	.5W	.72	.72	
17-19	R7-9	RN65C2323F	3	1/4W		.013	.013	
20	R10	Trimpot (Bourns) 3250W-1-501	1			19.10	19.10	
21	R11	RN65C2323F	1	1/4W		.013	.013	
22	Q2	Neg Regulator (MOT) MC1563R	1			30.00	30.00	
23	R12	Trimpot (Bourns) 3250W-1-501	1			19.10	19.10	
24	R13	RN55C10R0F	1	1/10W	.05	.022	.022	
25	CR1	1N3646	1	2500V	800V	2.34	2.34	
26	CR2	1N3646	1	2500V	800V	2.34	2.34	
27	T1	Transformer (Torelco) TAE #15997	1			.40	.40	
28	R14	2K 1/10W RN55C2001F	1	1/10W		.013	.013	

TOTAL (2 pages) 83.59

Sheet No. 1 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44015

ASS'Y TITLE Fire Fail Warning Logic & Computer Diagnostic

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
		Printed Ckt Conn. 00-8219-054-000-002				2.34	2.34	
1	U1	SN5400J (TI or Equiv.)	1			5.28	5.28	
2	U2	SN54L04J	1			6.38	6.38	
3	U3	SN54L00J	1			5.28	5.28	
4	U4	SN54L04J	1			6.38	6.38	
5	U5	SN54L20J	1			3.95	3.95	
6	U6	SN54L20J	1			3.95	3.95	
7	U7	SN54L30J	1			2.93	2.93	
8	U8	SN54L10J	1			4.58	4.58	
9	U9	SN54L00J	1			5.28	5.28	
10	U10	SN54L10J	1			4.58	4.58	
11	U11	SN54L30J	1			2.93	2.93	
12	U12	SN54L20J	1			3.95	3.95	
13	U13	SN54L04J	1			6.38	6.38	
14	U14	SN54L10J	1			4.58	4.58	
15	U15	SN54L30J	1			2.93	2.93	
16	U16	SN54L10J	1			4.58	4.58	
17	U17	SN5404J	1			6.38	6.38	

Sheet No. 2 of 2

SUB SYSTEM: CCU

ASS'Y DWG. NO. D-44015

ASS'Y TITLE Fire Fail Warning Logic & Computer Diagnostic

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
18	U18	SN54L74J	1			10.56	10.56	
19	Q1	Dual Transistor (MOT) JAN 2N2060	1			1.365	1.365	
20	C1	68 mF (Mallory) TAS686M015P1F	1	15V	5	.007	.007	
21	C2	0.1 mF (Erie) 8131-M050-W5R-104M	1	50V	5	.092	.092	
22	C3	0.1 mF (Erie)	1	50V	5	.092	.092	
23	C4	0.1 mF (Erie)	1	50V	5	.092	.092	
24	C5	0.1 mF (Erie) 8131-M050-W5R-104M	1	50V	5	.092	.092	
25	C6	0.1 mF (Erie)	1	50V	5	.092	.092	
26	C7	0.1 mF (Erie)	1	50V	5	.092	.092	
27	C8	0.1 mF (Erie)	1	50V	5	.092	.092	
28-30	R1-3	2.0K RC20GF202J	3	1/2W	.013W	.042	.126	

Sheet No. 1 of 1

SUB SYSTEM: CCU

ASS'Y DWG. NO. C-44198-3B

ASS'Y TITLE Transient Suppressor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	L1	Inductor Ass'y 44211	1	10A	1.0A	0.43	0.43	
2	L2	CR1, Pwr Rectifier (MOT) MR1396 Si	1	12A	1A	3.37	3.37	
3-4	CR2&3	Zener, Pwr (MCG Elect) TSD-3C-7-5	2	100W/ms	100W/ms	3.42	6.84	
5-6	CR4&5	Zener, Pwr (MCG Elect) TSD-3C-9-1	2	100W/ms	100W/ms	3.42	6.84	
7-8	R2&R3	.5 ohm 10W (RCL) T-D-78	2	10W	5W	.64	1.28	
9	R1	10K, 1/2W (Allen-Bradley) WWRC2DGF-103K	1	1/2W	.10W	.42	.42	
					TOTAL		19.18	

Sheet No. 1 of 2

SUB SYSTEM: MWU

ASS'Y DWG. NO. D-44204

ASS'Y TITLE CD Relay Board

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Failure Rate	Notes
1-7	K1-K7	FL11D (Potter & Brumfield)	7	12V		.111	.777	
8	K8	Latching FC11D	1	12V		.111	.111	
9	R1	113 RN60	1	1/8W	.01W	.01	.01	
10	R2	649 "	1	1/8W	.01W	.01	.01	
11	R3	113 "	1	1/8W	.01	.01	.01	
12	R4	649 "	1	1/8W	.01	.01	.01	
13	R5	113 "	1	1/8W	.01	.01		
14	R6	649 "	1	1/8W	.01	.01	.01	
15	R7	113 "	1	1/8W	.01	.01	.01	
16	R8	649 "	1	1/8W	.01	.01	.01	
17	R9	113 "	1	1/8W	.01	.01	.01	
18	R10	3.32K RN55	1	1/10W	.01	.01	.01	
19	R11	887K RN55	1	1/10W	.01	.01	.01	
20	R12	113RN60	1	1/8W	.01	.01	.01	
21	R13	3.32K RN55	1	1/10W	.01	.01	.01	
22	R14	887K RN55	1	1/10W	.01	.01	.01	
23	R15	113RN60	1	1/8W	.01	.01	.01	
24	R16	649 RN60	1	1/8W	.01	.01	.01	

Sheet No. 2 of 2

SUB SYSTEM: MWU

ASS'Y DWG. NO. D-44204

ASS'Y TITLE CD Relay Board

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
25	R17	8.87K RN55	1	1/10W	.01	.01	.01	
26	R18	10K RN55	1	1/10W	.01	.01	.01	
27	R19	8.87K RN55	1	1/10W	.01	.01	.01	
28-57	CR1-29	1N3611 (Si)	29	4W	.4W	1.00	29.00	
58-67	Q1-Q9	2N1711-NPN 134-14	9	800 mW	80mW	.40	3.6	

TOTAL (2 pages) 33.678

Sheet No. 1 of 1

SUB SYSTEM: MWU

ASS'Y DWG. NO. C-44203-2

ASS'Y TITLE Relay Regulator & Disable Assembly

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	Q1	2N1711	1			2.23	2.23	
2	Q2	2N1711	1			2.23	2.23	
3	Q3	2N5039 (Mot)	1			2.23	2.23	
4	U1	MC1569R	1			14.85	14.85	
5	C1	.1 mF (Erie) 8131	1	50V	12V	.24	.24	
6	C2	.0015 mF 8121	1	"	"	.24	.24	
7	C3	1.0 mF 8151	1	"	"	.24	.24	
8	R1	1K RN60	1	1/8W	.06W	.017	.017	
9	R2	0.4 (Dale) RS-2B	1	3W	1W	.375	.375	
10	R3	100 RN55	1	1/10W	.06W	.017	.017	
11	R4	25K Pot (Bourns) 3290W	1			15.14	15.14	
12	R5	6.81K RN55	1	1/10W	.01W	.010	.010	
13	R6	-						
14	R7	1K RN55	1	1/10W	.01W	.010	.010	
					TOTAL		37.83	

Sheet No. 1 of 1

SUB SYSTEM: MWU

ASS'Y DWG. NO. D-44021C

ASS'Y TITLE Lamp Regulator

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	R1	6.98K RN60C6981F	1	1/8W	.20W	.011	.011	
2	R2	6.81K RN60C6811F	1	"	.20W	.011	.011	
3	R3	20 ohms RN60C20R0F	1	"	.06W	.017	.017	
4	R4	0.1 ohm (Dale RS-23)	1	3W	1.5W	.48	.48	
5	R5	0.1 ohm (Dale RS-23)	1	"	"	.48	.48	
6	R6	0.1 ohm (Dale RS-23)	1	"	"	.48	.48	
7	R7	1K RN75C1001F	1	1W	.14W	.011	.011	
8	V1	MC1569R	1			14.85	14.85	
9	Q1	2N3792	1	150W	5W, 12V	.578	.578	
10	Q2	2N1711	1	800 mW	12V	.893	.893	
11	Q3	2N3792	1	150W	5W, 12V	.578	.578	
12	C1	0.1 mF 50V (Erie) 8131-M050-W5R-104M	1	50V	12V	.132	.132	
13	C2	0.0015 mF (Erie) 50V 8121-A050-W5R-152K	1	"	"	.132	.132	
14	C3	1 mF 50V (Erie) 8151-M050-W5R-105K	1	"	"	.132	.132	
						TOTAL	18.79	

Sheet No. 1 of 1

SUB SYSTEM: MWU

ASS'Y DWG. NO. C-44198-2

ASS'Y TITLE Transient Suppressor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	L7	Inductor Ass'y 44211	1			.43	.43	
2	CR1	Rectifier, Pwr MR1396 (MOT)	1	12A	1A	2.15	2.15	
3-4	CR2&3	Zener, Pwr (MCG Elect) TSD-3C-7-5	2			2.75	5.50	
5-6	CR4&5	Zener, Pwr (MCG Elect) TSD-3C-9-1	2			2.75	5.50	
7	R1	10K (Allen-Bradley)	1	1/2W	.08W	.02	.02	
8	R2	.5 (RCL) T-D-78	1	10W	5W	.30	.30	
9	R3	10K RN55	1	1/10W	.01W	.01	.01	
10	R4	2K RN55	1	1/10W	.01W	.01	.01	
11	R5	1K RN55	1	1/10W	.01W	.01	.01	
12	R6	3.01K RN55	1	1/10W	.01W	.01	.01	
13	Q1	2N6050				.578	.578	
14	Q2	2N1711				.394	.394	
						TOTAL	14.91	

Sheet No. 1 of 1

SUB SYSTEM: MWU

ASS'Y DWG. NO. D-44201

ASS'Y TITLE AB Relay Board

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1-8	K1-K8	FL11D Relay, Latching	8	12V		.111	.888	Similar to D-44204
9	R1	113 ohm RN60C1130F	1	1/8W		.01	.01	
10	R2	649 ohm RN60C6490F	1	1/8W		.01	.01	
11	R3	649 ohm RN60C6490F	1	1/8W		.01	.01	
12	R4	113 ohm RN60C1130F	1	1/8W		.01	.01	
13	R5	113 ohm RN60C1130F	1	1/8W		.01	.01	
14	R6	649 ohm RN60C6490F	1	1/8W		.01	.01	
15	R7	649 ohm RN60C6490F	1	1/8W		.01	.01	
16	R8	113 ohm RN60C1130F	1	1/8W		.01	.01	
17	R9	113 ohm RN60C1130F	1	1/8W		.01	.01	
18	R10	649 ohm RN60C6490F	1	1/8W		.01	.01	
19	R11	649 ohm RN60C6490F	1	1/8W		.01	.01	
20	R12	113 ohm RN60C1130F	1	1/8W		.01	.01	
21	R13	113 ohm RN60C1130F	1	1/8W		.01	.01	
22	R14	649 ohm RN60C6490F	1	1/8W		.01	.01	
23	R15	649 ohm RN60C6490F	1	1/8W		.01	.01	
24	R16	113 ohm RN60C1130F	1	1/8W		.01	.01	
25-56	CR1-CR32	1N3611	32			1.00	32.00	
57-65	Q1-Q8	2N1711	8			.40	3.20	
						TOTAL	36.25	

Sheet No. 1 of 1

SUB SYSTEM: CRU

ASS'Y DWG. NO. D-44052A

ASS'Y TITLE Lamp Regulator

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	R1	16.9K RN60C1692F	1	1/8W		.01	.01	
2	R2	6.81K RN60C6811F	1	1/8W		.01	.01	
3	R3	20 Ohm RN60C20R0F	1	1/8W		.02	.02	
4	R4	0.301 Ohm RW79UR301F	1	3W		.48	.48	
5	R5	1K RN75C1001F	1	1W	.15W	.01	.01	
6	U1	MC1569R	1			14.85	14.85	
7	C1	0.1 mF (Erie) 8131-M050-W5R-104	1	50V	12V	.14	.14	
8	C2	0.0015 mF (Erie) 8121-A050-W5R152K	1	50V	12V	.14	.14	
9	C3	1 mF (Erie) 8151-M050-W5R-105K	1	50V	12V	.14	.14	
10	Q1	2N3792				.58	.58	
11	Q2	2N1711	1			.89	.89	
					TOTAL		17.27	

Sheet No. 1 of 2

SUB SYSTEM: CRU

ASS'Y DWG. NO. D-44197

ASS'Y TITLE CRU Logic Circuitry

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	R1	113 RN60C	1	1/5W	.01W	.010	.010	
2	R2	649 "	1	"	"	"	.010	
3	R3	113 "	1	"	"	"	.010	
4	R4	649 "	1	"	"	"	.010	
5	R5	113 "	1	"	"	"	.010	
6	R6	649 "	1	"	"	"	.010	
7	R7	113 "	1	"	"	"	.010	
8	R8	649 "	1	"	"	"	.010	
9	R9	113 "	1	"	"	"	.010	
10	R10	649 "	1	"	"	"	.010	
11	R11	113 "	1	"	"	"	.010	
12	R12	649 "	1	"	"	"	.010	
13	R13	113 "	1	"	"	"	.010	
14	R14	649 "	1	"	"	"	.010	
15	R15	113 "	1	"	"	"	.010	
16	R16	649 "	1	"	"	"	.010	
17-24	Q1-8	2N1711	8			.394	3.152	
25-50	CR1-26	1N3611	26			.63	16.38	

Sheet No. 2 of 2

SUB SYSTEM: CRU

ASS'Y DWG. NO. D-44197

ASS'Y TITLE CRU Logic Circuitry

FAILURE RATE DATA

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rating Per 10^6 Hrs/Part	Total Failure	Notes
51-54	K1-K4	L5A-2C-12B	4			.114	.456	
55	K5	JRA-M2C-12B	1			.114	.114	
56	K6	LJA-2C-12B	1			.114	.114	
57-60	K7-9	JRA-M2C-12B	3			.114	.342	
						TOTAL (2 Pages)	20.718	

Sheet No. 1 of 1

SUB SYSTEM: CRU

ASS'Y DWG. NO. C-44198-1

ASS'Y TITLE Transient Suppressor

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	L7	Inductor Ass'y 44211	1			.43	.43	
2	CR1	Rectifier, Pwr MR1396 (MOT)	1	12A	1A	2.15	2.15	
3-4	CR2&3	Zener, Pwr (MCG Elect) TSD-3C-7-5	2			2.75	5.50	
5-6	CR4&5	Zener, Pwr (MCG Elect) TSD-3C-9-1	2			2.75	5.50	
7	R1	10K (Allen-Bradley)	1	1/2W	.08W	.02	.02	
8	R2	.5 (RCL) T-D-78	1	10W	5W	.30	.30	
9	R3	10K RN55	1	1/10W	.01W	.01	.01	
10	R4	2K RN55	1	1/10W	.01W	.01	.01	
11	R5	1K RN55	1	1/10W	.01W	.01	.01	
12	R6	3.01K RN55	1	1/10W	.01W	.01	.01	
13	Q1	2N6050				.578	.578	
14	Q2	2N1711				.394	.394	
						TOTAL	14.91	

Sheet No. 1 of 1

SUB SYSTEM: CRU

ASS'Y DWG. NO. C-44203-1

ASS'Y TITLE Relay Regulator & Disable Assembly

F A I L U R E R A T E D A T A

Item No.	Part Code	Part Type Part Dwg. No.	Qty Req'd	Part Rating	Part Stress	Part Failure Rate Per 10^6 Hrs/Part	Total Failure Rate	Notes
1	Q1	2N1711	1			2.23	2.23	
2	Q2	2N1711	1			2.23	2.23	
3	Q3	2N5039 (Mot)	1			2.23	2.23	
4	U1	MC1569R	1			14.85	14.85	
5	C1	.1 mF (Erie) 8131	1	50V	12V	.24	..24	
6	C2	.0015 mF 8121	1	"	"	.24	.24	
7	C3	1.0 mF 8151	1	"	"	.24	.24	
8	R1	1K RN60	1	1/8W	.06W	.017	.017	
9	R2	0.4 (Dale) RS-2B	1	3W	1W	.375	.375	
10	R3	100 RN55	1	1/10W	.06W	.017	.017	
11	R4	25K Pot (Bourns) 3290W	1			15.14	15.14	
12	R5	6.81K RN55	1	1/10W	.01W	.010	.010	
13	R6	-						
14	R7	1K RN55	1	1/10W	.01W	.010	.010	
						TOTAL	37.83	