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MICROPROCESSOR PRINTED CIRCUIT BOARDS FOR DIGITAL PROTOTYPE SYS--ETC(U)
JUN 76 D K FRONEK, R A LANE

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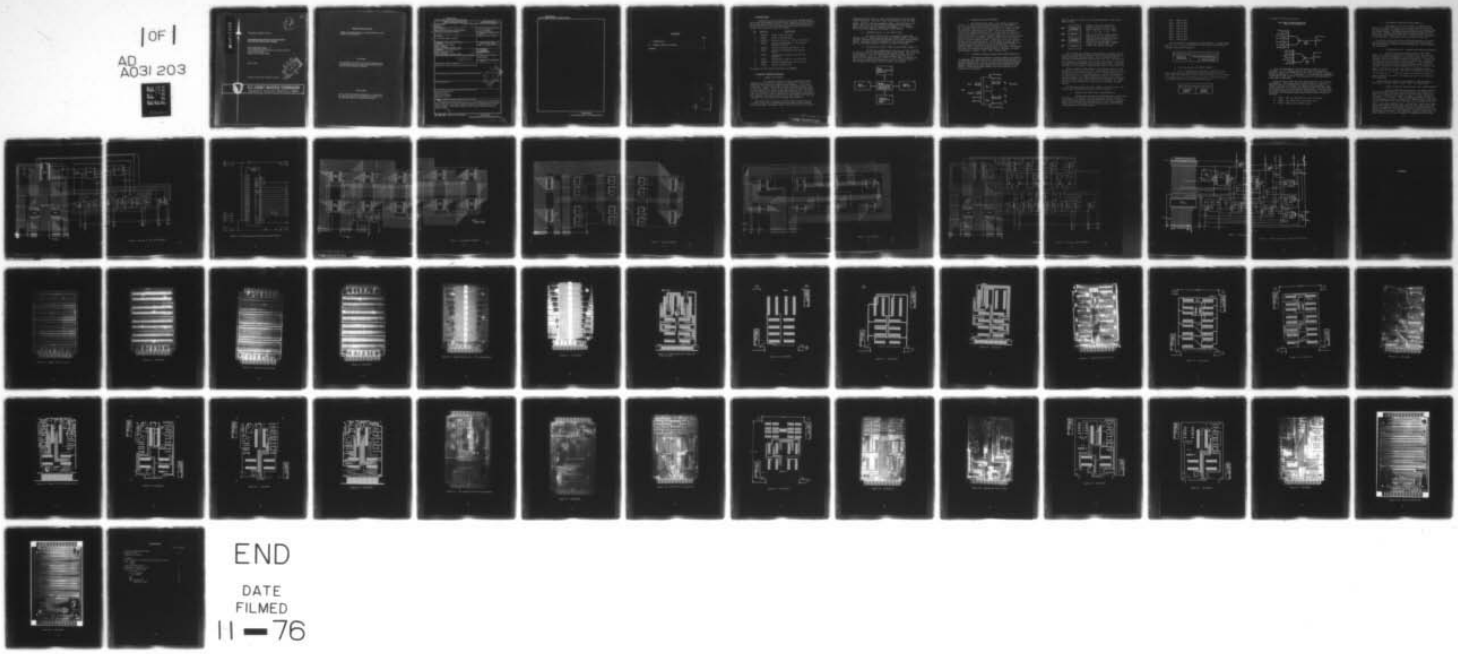

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TECHNICAL REPORT RC-76-3

MICROPROCESSOR PRINTED CIRCUIT BOARDS FOR DIGITAL PROTOTYPE SYSTEMS

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Redstone Arsenal, Alabama 35809

29 June 1976

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

During the last year, several 4.5 in. × 6 in. printed circuit boards have been designed and fabricated for general and special purpose use in prototyping digital circuits. Since these designs represent a considerable effort, this report presents a descriptive overview of the various circuits and printed circuit boards.

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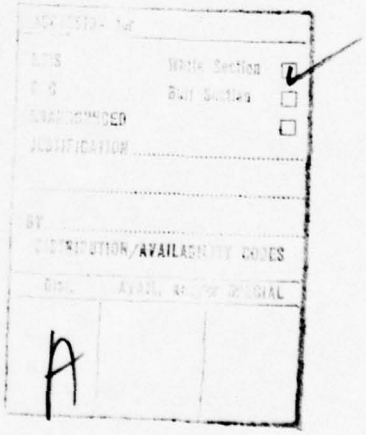


I. INTRODUCTION

During the last year, several 4.5 in. × 6 in. printed circuit boards have been designed and fabricated for general and special purpose use in prototyping digital circuits. Since these designs represent a considerable effort, this report presents a descriptive overview of the various circuits and printed circuit boards.

No.	Board No.	Board Title
1	N06990-A	Single 44-pin DIP board
2	200039	Double 44-pin DIP board
3	N07202-A	Single 44 pin 20 in. × 16 in. matrix board
4	200014	Motorola microprocessor - less control and clock circuits
5	200016B	Motorola microprocessor RAM (1K × 8)
6	200025	Motorola microprocessor with discrete clock
7	200030	Microprocessor interface PlA with rate generator
8	200031	Microprocessor ROM (1K × 8) Intel 1702
9	200035A	Motorola microprocessor with IC clock
10	200036	General interface PlA

The layouts for each board are found in the Appendix.

II. GENERAL PURPOSE DIP BOARDS

A. (N06990-A and 200039)

The increased usage of the dual inline package (DIP) integrated circuit (IC) has required the design of a 4.5 in. × 6 in. printed circuit board with standard 44-pin connector. This format allows both a single board design and more complicated designs using a "card rack" module. There are two versions of the DIP board format. The most common is the single 44-pin edge connector board. Occasionally, circuit signals will be generated that require more than 44 pin-outs on the board. A double connector DIP board format is provided for this function. Peripheral signals such as TTY, RS-232, etc., are conveniently fed to the outside on the second edge connector.

Both circuit board formats can easily accept sixteen 16-pin DIP or twenty 14-pin DIP. The predrilled hole pattern allows resistors (up to half-watt), capacitors, diodes, and active devices to be easily

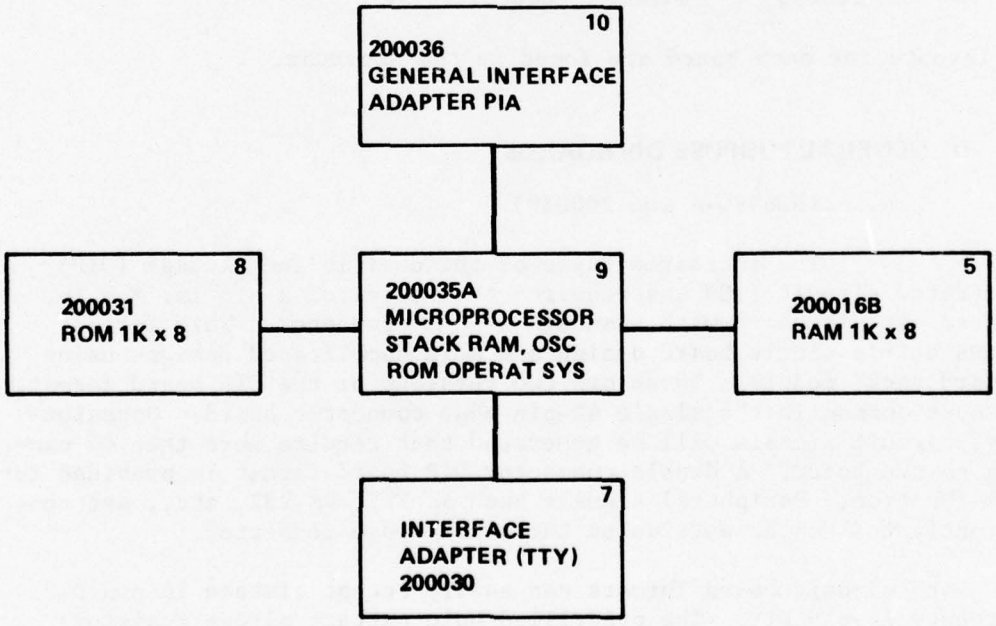
integrated with the DIP IC's. Each circuit pin hole allows two additional connections. Four power buses are provided for V_{cc} and signal ground. Usually, these are assigned in pairs — front and back of the board. Pins 1, 22, A, and Z have been assigned for this purpose. More often 1 and A are tied together and assigned "+5 V." Likewise 22 and Z are tied together and assigned "signal ground."

B. (N07202-A) 20 in. × 16 in. Matrix Board

The matrix board is used as a general purpose diode transfer circuit. Special purpose read only memories (ROM's), decoding, and logic functions are easily implemented on this printed circuit board format. Although the board is designed to house passive components, both V_{cc} and signal ground are bused to one side of the board.

C. Microprocessor Boards (200014 through 200036) (Figure 1)

The Motorola microprocessor "chip set" has been configured on four 4.5 in. × 6 in. multilayer printed circuit boards. The system has been designed to allow easy expansion of additional memory and peripheral interface circuits. This modular concept makes this set of printed circuit boards extremely flexible. This series of boards makes easy use of the Motorola microprocessor family in a general system. The following block diagram shows the overall configuration.

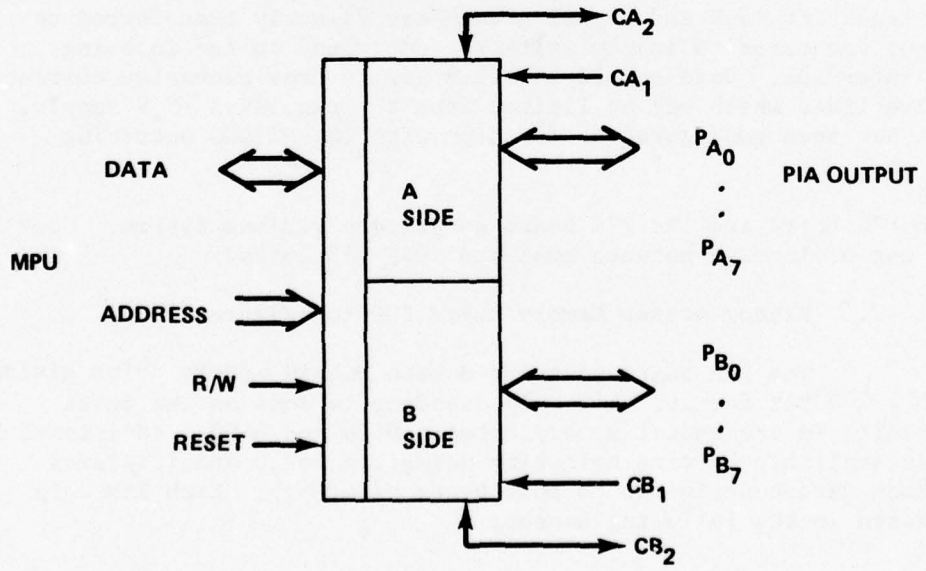


D. Microprocessor Board (200035A)

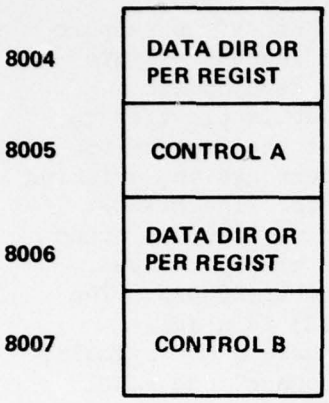
The microprocessor board is the center of processing activity. In addition to the microprocessing unit (MPU) M6800, a 128 × 8 random access memory (RAM) is provided as a "stack" to support the interrupt activities of the microprocessor. The address of this stack memory is A000 through A07F (Hex). For design development requiring the MIKBUG operating system, a 24-pin socket is prewired to accept the MC6830 ROM. This ROM has been prepared at the factory to give the user several routines — loading, memory interrogation, printing a specified array, user program execution address, etc. The MIKBUG ROM has a prewired address at E000. Should the user wish to use other software for the operating system, the ROM (6830) is simply removed. The overall schematic diagram is shown in drawing number 200035. The Motorola MC6870A 2 phase clock chip (also the MC6871B) is a self-contained crystal oscillator providing phase 1 and phase 2 MPU signals. This board also contains the necessary logic to "debounce" the panel input switches — "Reset," "NMI," "HALT," "Single Step."

E. Peripheral Interface Adapter Board (200030)(Figure 2)

The Motorola peripheral interface adapter (PIA) MC6820 is responsible for taking data from a user system and presenting it to the 8-bit MPU data bus. The PIA is a bidirectional device capable of inputing/outputing two 8-bit data registors and corresponding strobe signals. Because of the large number of pin-outs required for this device, a second 44-pin edge connector has been fabricated at the output side of the board.



The MPU treats this device as four memory locations at 8004, 8005, 8006, and 8007.



During a "reset all internal PIA registers are set to zero. This coding configures the PIA as inputs ($P_{A_0} \ldots P_{A_7}$; $P_{B_0} \ldots P_{B_7}$). However, bit 2 in each control register must be set to a "1" to allow the selection of the peripheral register (otherwise the data direction register will be selected). Loading an "04" into 8005 and 8007 accomplishes this control function.

The PIA board also contains a rate generator, MC-14536, and the necessary line driver/line receiver chips to allow a teletype current loop or the RS-232 interface format. The rate generator must be adjusted to synchronize with the band rate. Pot, R_1, is provided for this function. When properly set, the TTY should produce an asterisk (*) when "Reset" is selected from the front panel switch. (110 band represents a timing signal of approximately 9 msec at test point E-5).

Optical isolators (4N33) provide a DC isolation between the MOS PIA and the current loop of the TTY. Jumper options allow the PIA to be selected as a TTY current loop device or a RS-232 format with ±12 V. The bus lines for +5 V and signal ground are directly transferred to the output connector to supply voltages and ground to the incoming circuit interface. Care should be taken not to draw excessive current from these lines which may be limited from the regulated +5 V supply. This PIA has been configured to function with the MIKBUG operating system.

The MPU board and the PIA board comprise a minimum system. User program can be located between A04A and A07F (53 bytes).

F. Random Access Memory Board 200016B(Figure 3)

The RAM board contains 8 each MC6810 memory chips giving a 1K (1024) × 8 bit format. All chip decoding is done on the board which results in sequential memory between 0000 and 0400. Additional memory is available by card selecting using a 4 to 16 demultiplexer chip. Each card contains up to 1024 bytes of memory. Each RAM chip is addressed in the following manner:

RAM 1 0000 to 007F

RAM 2 0080 to 00FF

RAM 3 0100 to 017F

RAM 4 0180 to 01FF

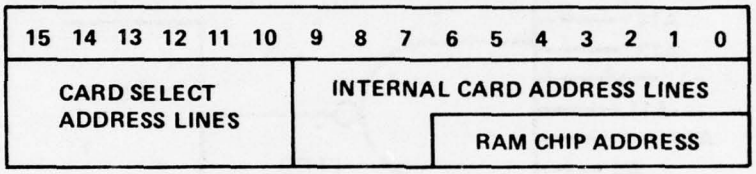
RAM 5 0200 to 027F

RAM 6 0280 to 037F

RAM 7 0300 to 037F

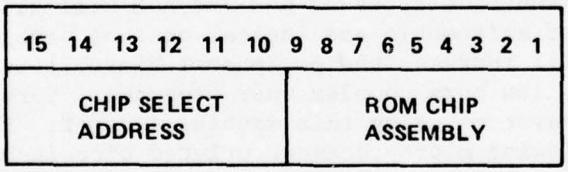
RAM 8 0380 to 03FF .

The RAM locations are hardwired at these addresses. Address lines, A_{10}, A_{11}, A_{12}, A_{13}, A_{14}, although not actively used, are provided for additional chip select capability.



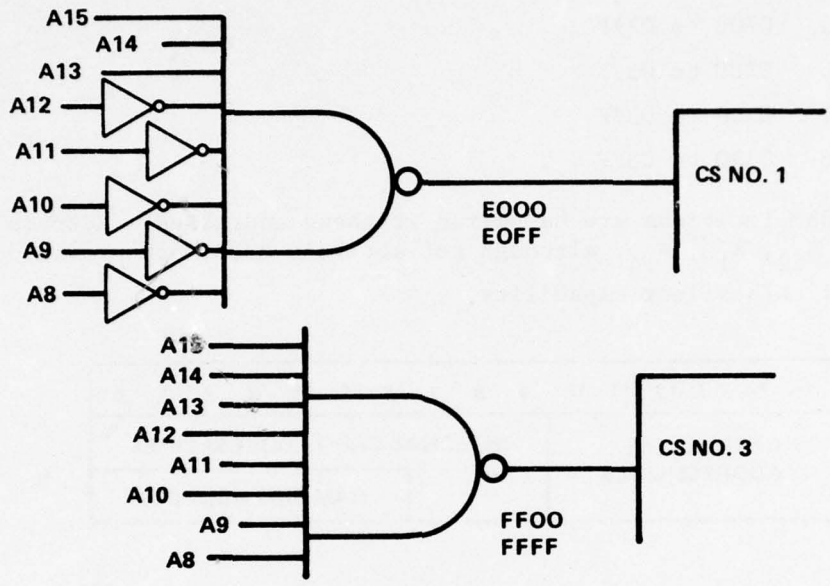
G. Read Only Memory Board 200031 (Figure 4)

A 1K × 8 ROM array (UV erasable) is provided on this card. Decode logic is provided with one 74C04 inverter chip and a 74C30 eight input NAND gate. Address lines A_8 through A_{15} are available on the board and are to be selected by the user. Absolute addressing is available with the limit of six inverting inputs.



An example of a ROM array follows:

SELECT ROM 1 AT EOOO THROUGH EOFF
ROM 3 AT FFOO THROUGH FFFF.



Intel 1702 programmable read only memories (PROM) are used on this board. A -9 V supply is required for normal read operation. Currently, there is no UV-PROM device that does not require a negative voltage in addition to +5 V (typically). It is assumed that programming of the PROM is done elsewhere — the program line is hardwired in the "read" mode of operation.

These four boards (MPU, PIA, RAM, ROM) constitute a small working microcomputer. One thousand bytes of RAM and ROM will allow many adequate solutions of arithmetic and logical control problems. Additional PIA boards will increase the peripheral flexibility while additional memory will allow more complex user programs. Currently there are several working systems using this machine concept. For additional flexibility the following microprocessor printed circuit boards are available:

1) 200014 - MPU, PIA, RAM, ROM less clock and control
2) 200025 - MPU, Stack, ROM with discrete clock
3) 200036 - General PIA interface board.

H. Microcomputer Subsystem 200014 (Figure 5)

This single 4.5 in. × 6 in. board is intended to be used with a "piggy back" printed circuit board having the additional pin outs necessary to interface the PIA teletype and the external clock and control signals. The MIKBUG resident operating system is assumed to be used. Additional ROM (6830) space has been provided with the chip selects at the option of the user. A RAM stack and a program RAM is also available - chip selects are at the option of the user.

This board was an early version of the microprocessor system and does not have the flexibility of easy expansion. The entire system can be constructed on this board and the "piggy back" card attached to the system board.

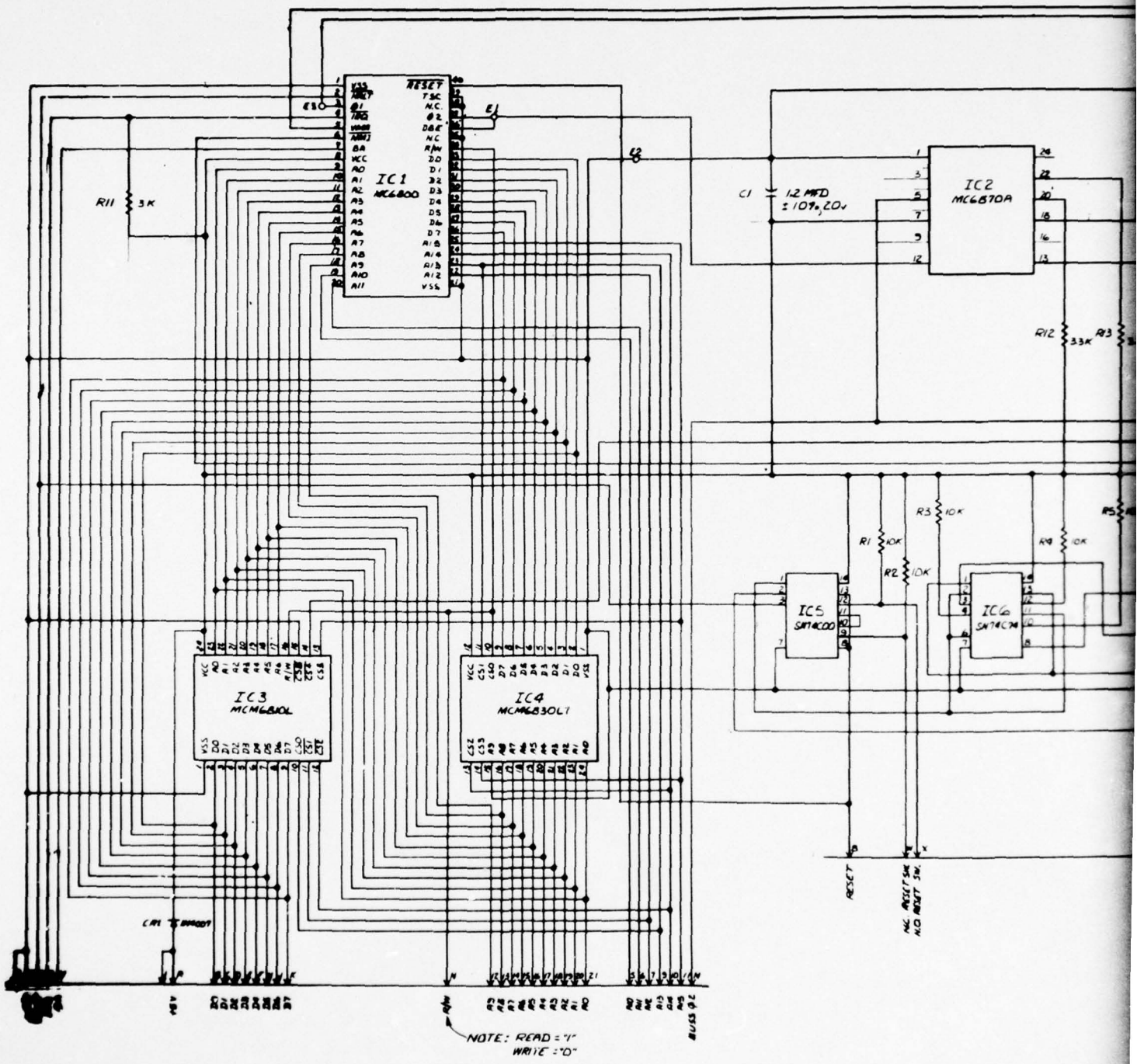
I. Microprocessing Unit - Discrete Clock Board 20025 (Figure 6)

This MPU board closely approximates the MPU 200035A board. The exception being that of a discrete clock. There may be a reason to run the microcomputer at clock speeds slower than the fixed frequency offered by the MC6871B crystal oscillator IC. A slower clock frequency can allow more memory (increased capacitance) to respond to the bus system without data and address buffers. A dual monostable multivibrator (9602) generates the nonoverlapping clock signals at a frequency determined by timing components R_1, R_2, C_1, C_2. Phase 1 and phase 2 clock signals are processed through the NPN-PNP transistor driver stage (Q_1, Q_2, Q_3, Q_4). The levels at the output of this stage are very near V_{cc}, 5 V. The high voltage is required by the MPU for proper clocking. Bus phase 2 is buffered and sent to the control bus for distribution.

Control logic to "debounce" switch inputs is also contained on this board to perform "Reset," "Halt," "NMI," and "Single Step."

J. General Peripheral Interface Board, PIA - 200036 (Figure 7)

The PIA MC6820 interface adapter is the primary parallel device that communicates with the external world. The user has the option of two 8-bit data ports that can be configured as inputs or outputs in any combination (16 inputs, 15 inputs - 1 output, 14 inputs - 2 outputs, ... 16 outputs). There are additional control signals that may be configured as inputs or outputs from program control. This board contains the address bus; control functions, V_{cc} and signal ground in a double 44-pin edge connector format. The user must choose chip selects, and provide external conductor paths from the PIA to the external circuits. The remainder of the general PIA board is configured as a DIP prototype format. Up to twelve 16-pin DIP's or fifteen 14-pin DIP IC's may be used on this board. Rate generators, buffers, decode logic, and other interface circuits may be especially implemented on this board.



Fi

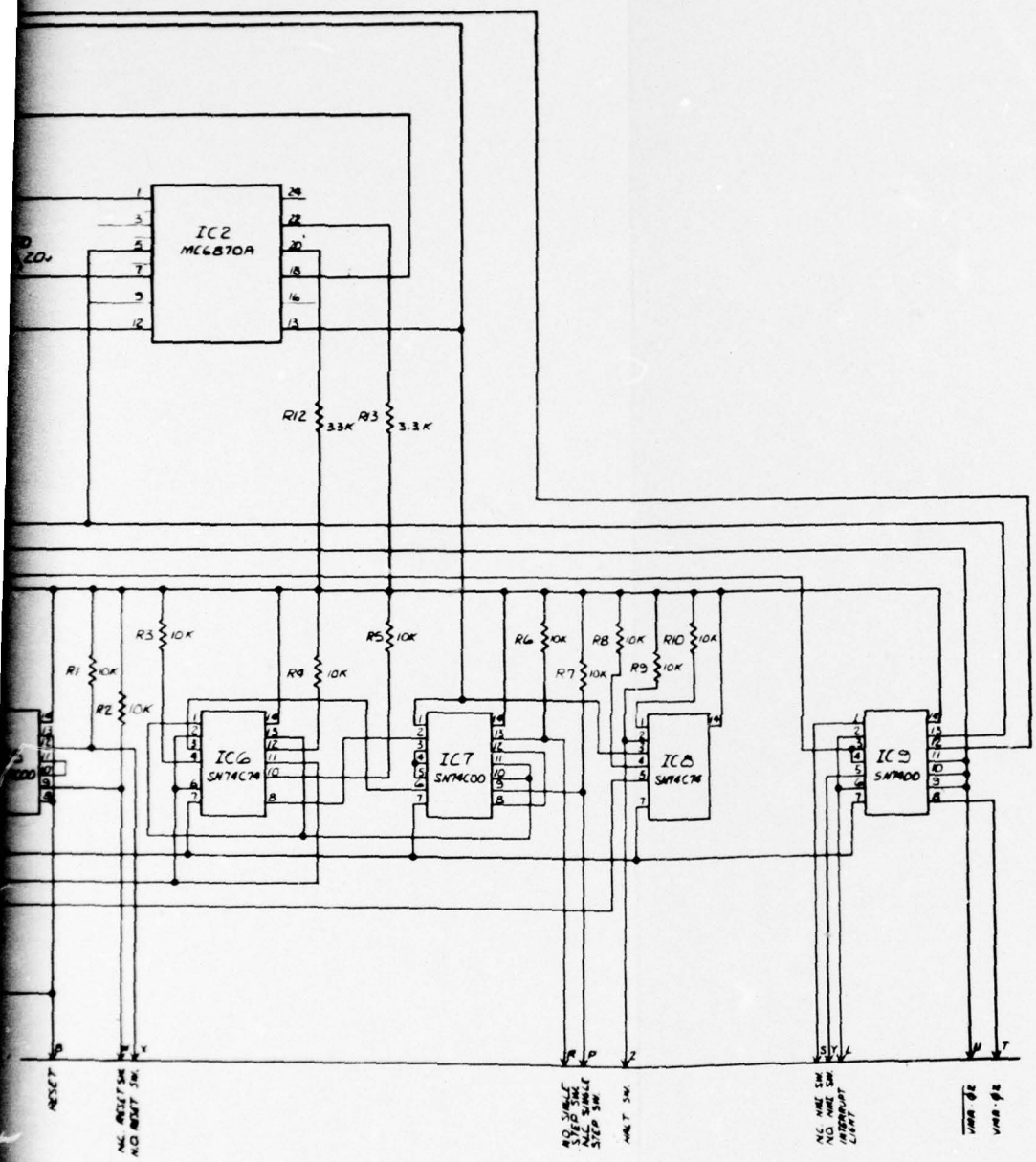


Figure 1. MPU and 24 clock chip schematic.

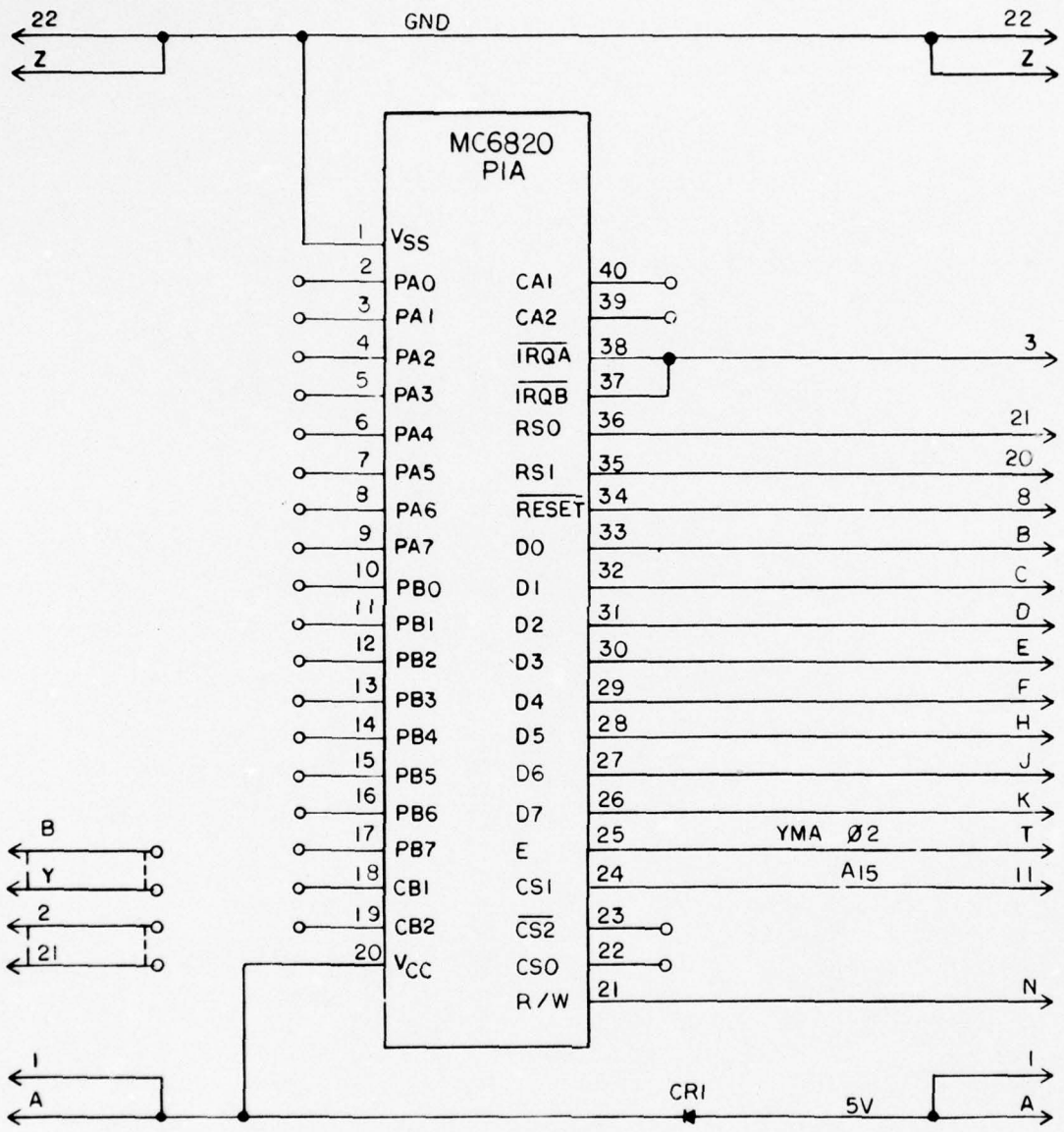
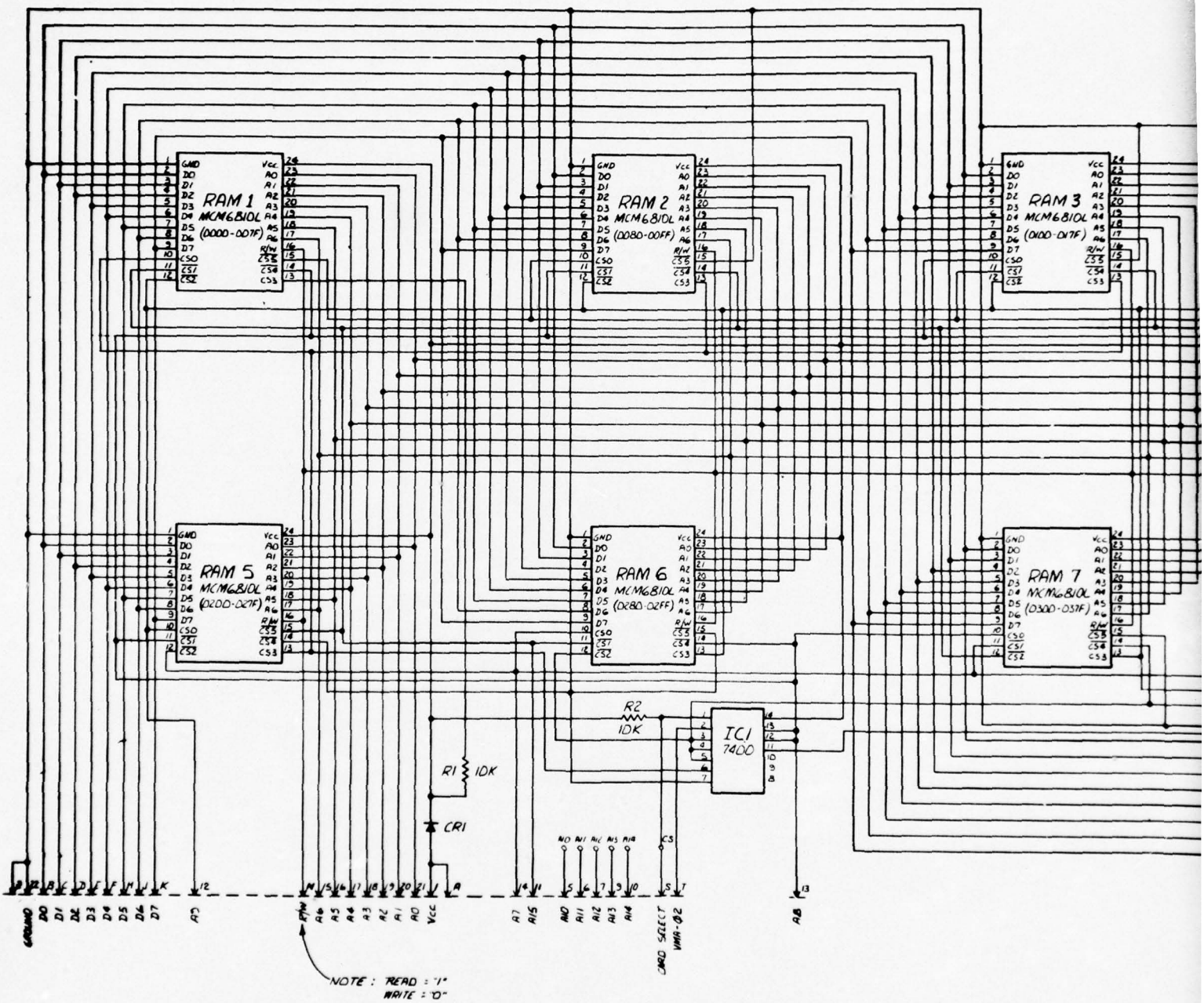


Figure 2. Peripheral interface adapter universal board.



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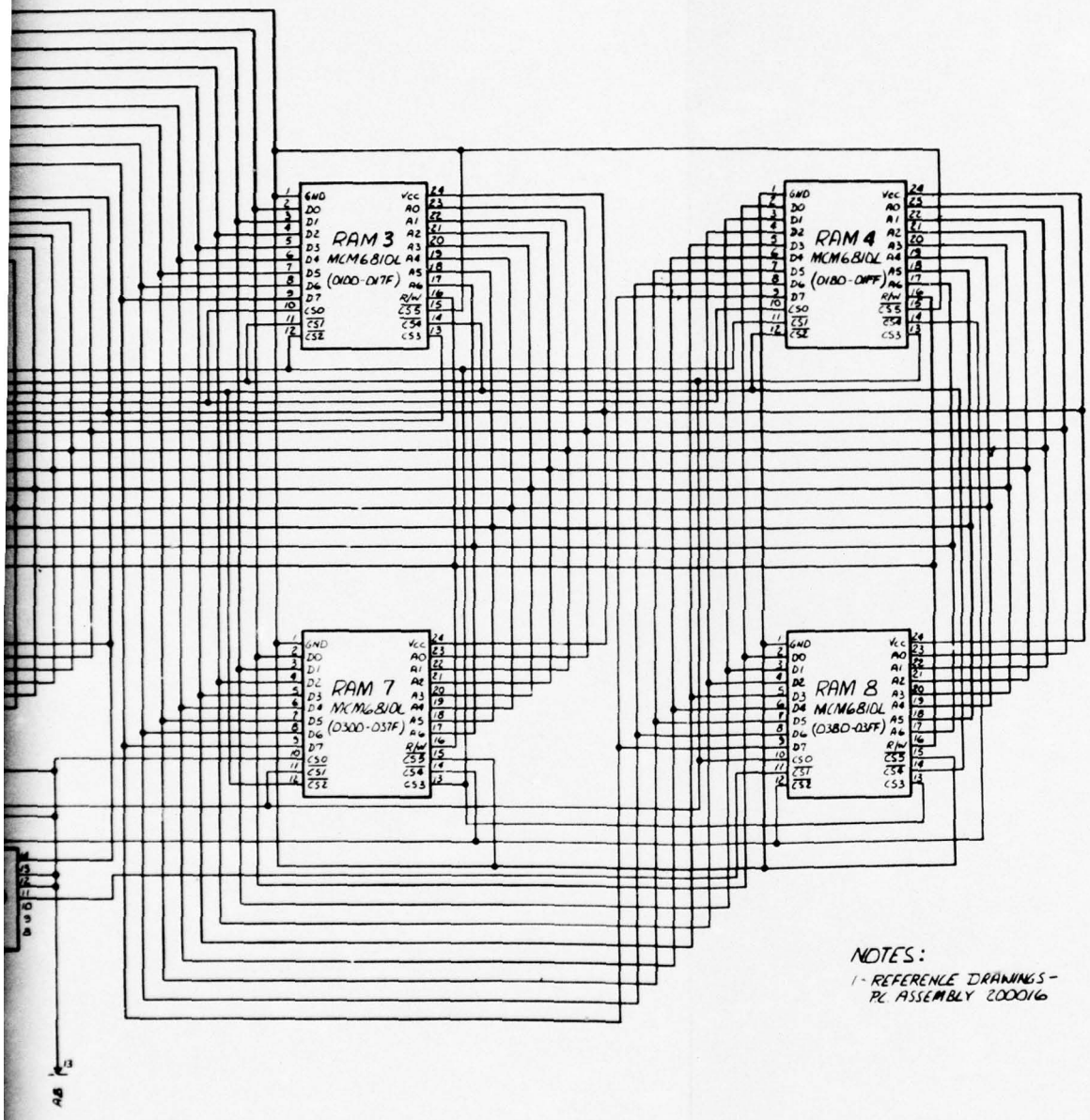
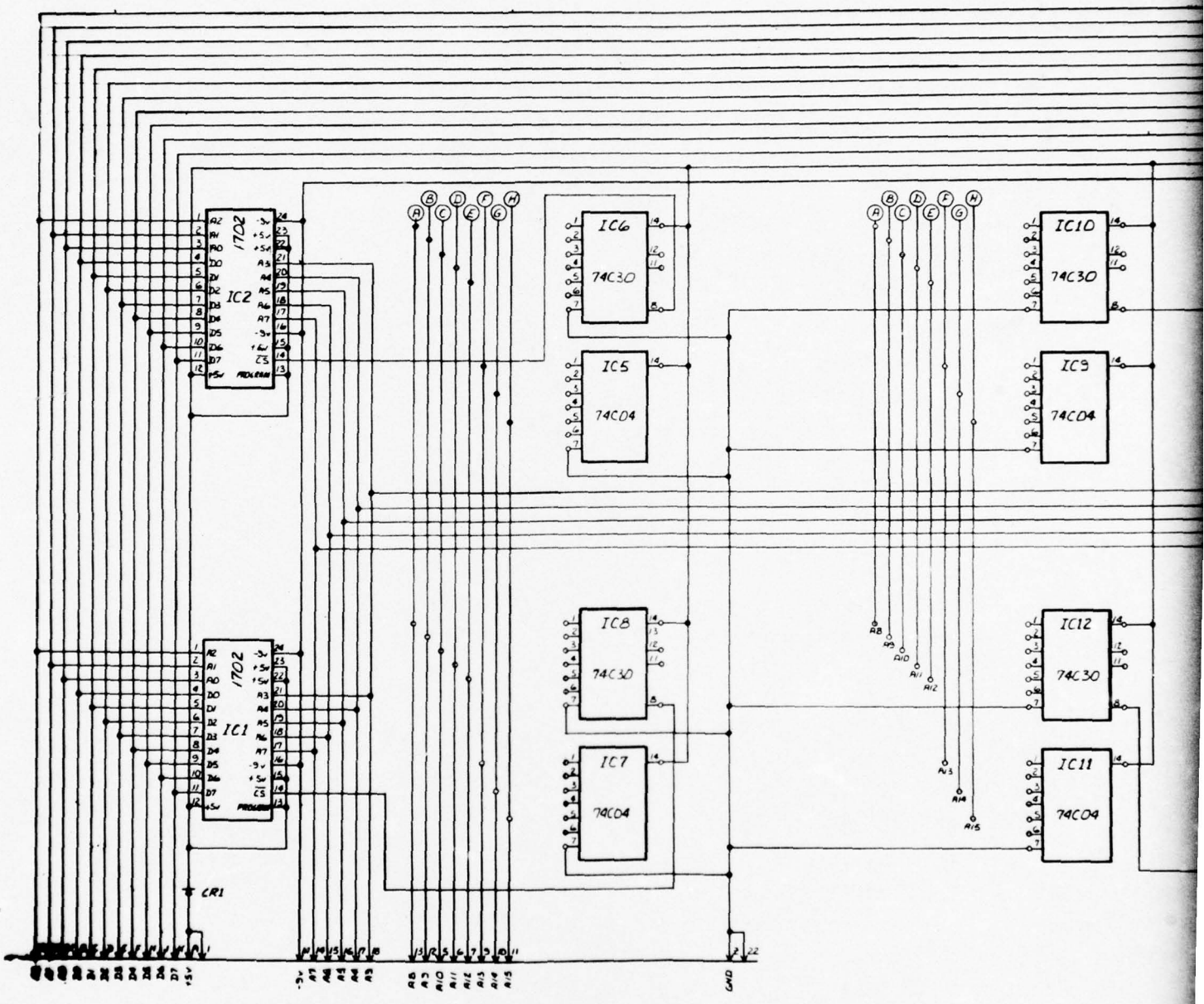


Figure 3. MPU 6800 RAM schematic.


IC1
1702
IC2
1702
IC5
74C04
IC6
74C30
IC7
74C04
IC8
74C30
IC9
74C04
IC10
74C30
IC11
74C04
IC12
74C30
CR1
PROGRAM
+5V
-5V
GND

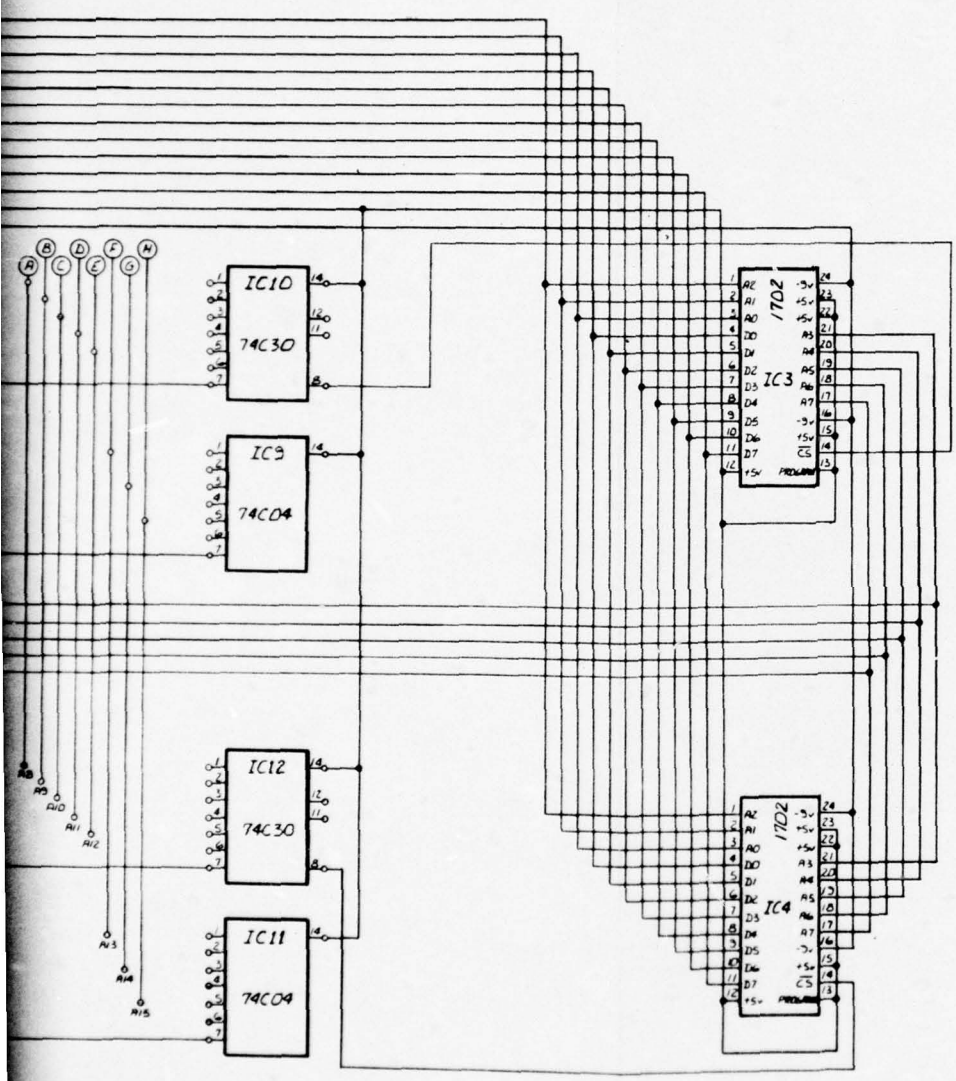
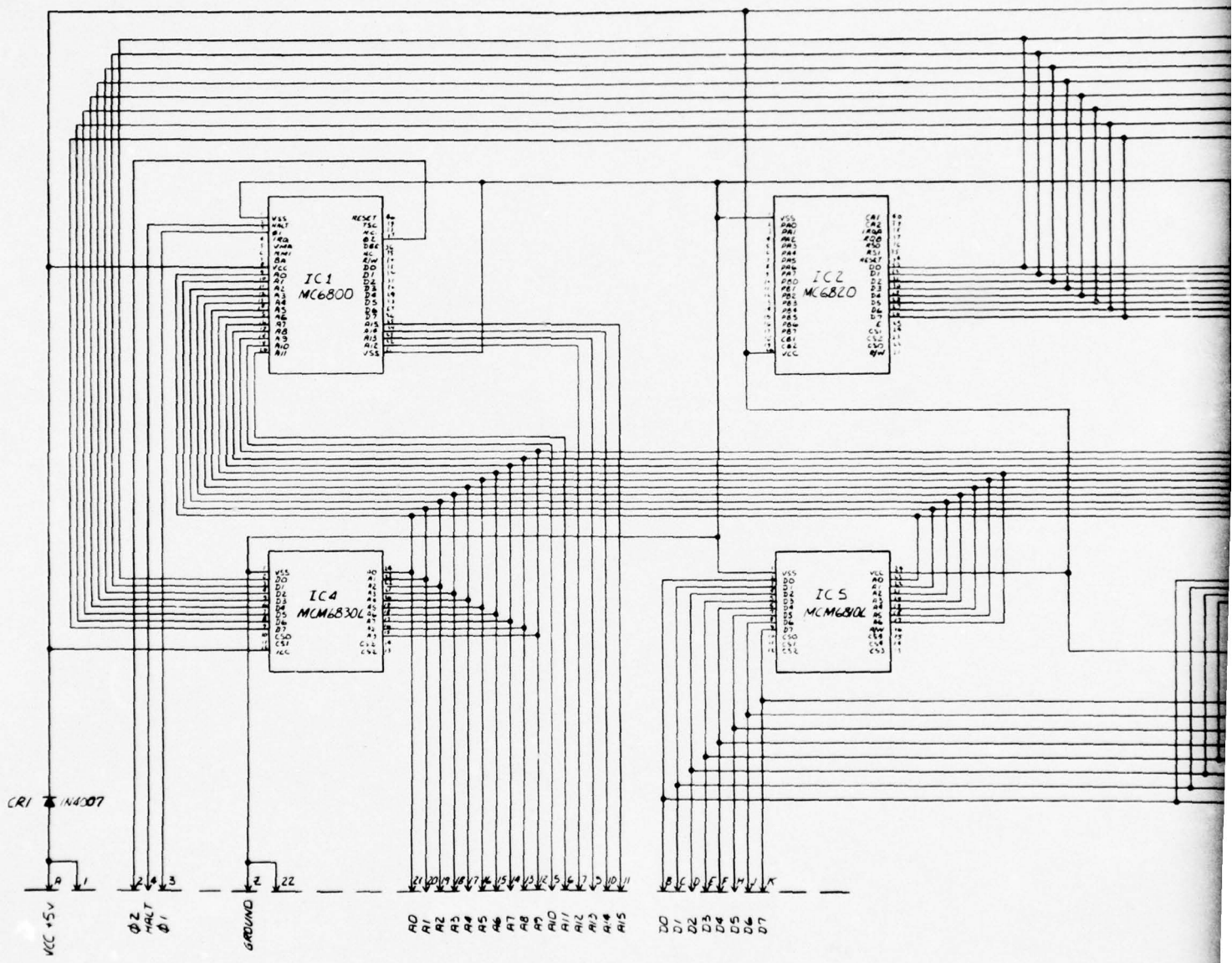


Figure 4. MPU ROM schematic.


IC1
MC6800
IC2
MC6820
IC4
MCM6830L
IC5
MCM6830L
CR1 IN4007
VCC +5V
Ø2
HALT
Ø1
GROUND
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7

Figure

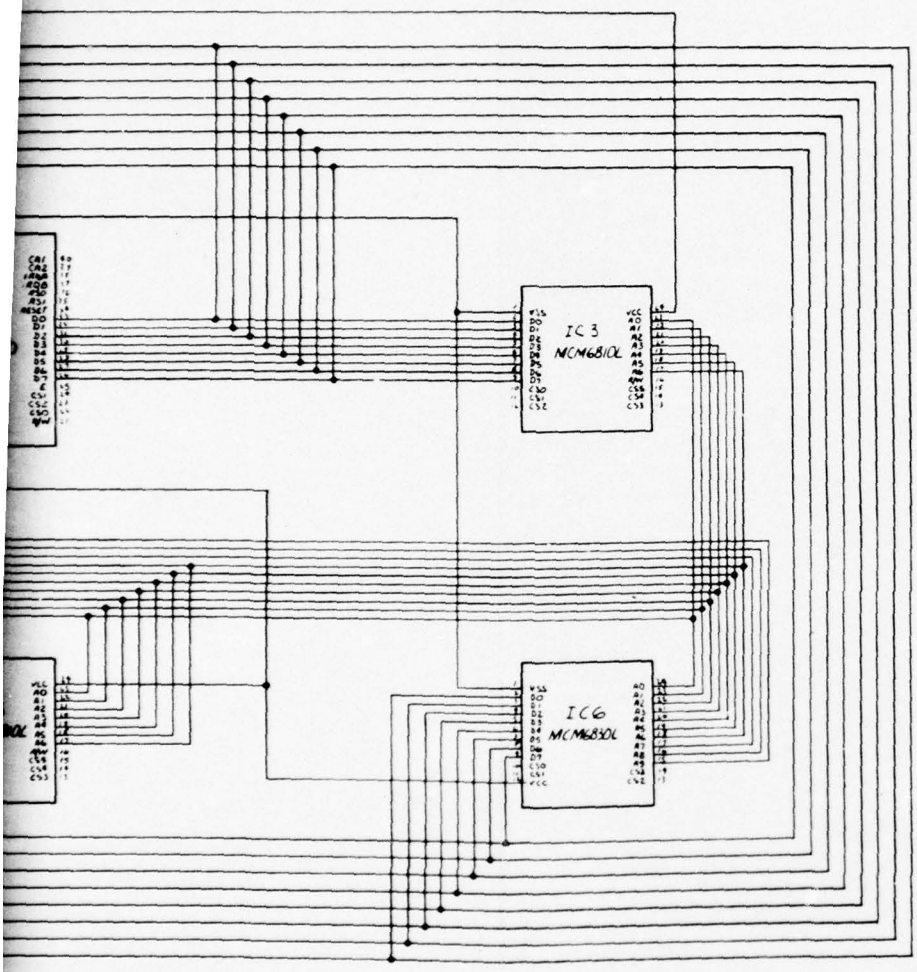


Figure 5. MPU schematic.

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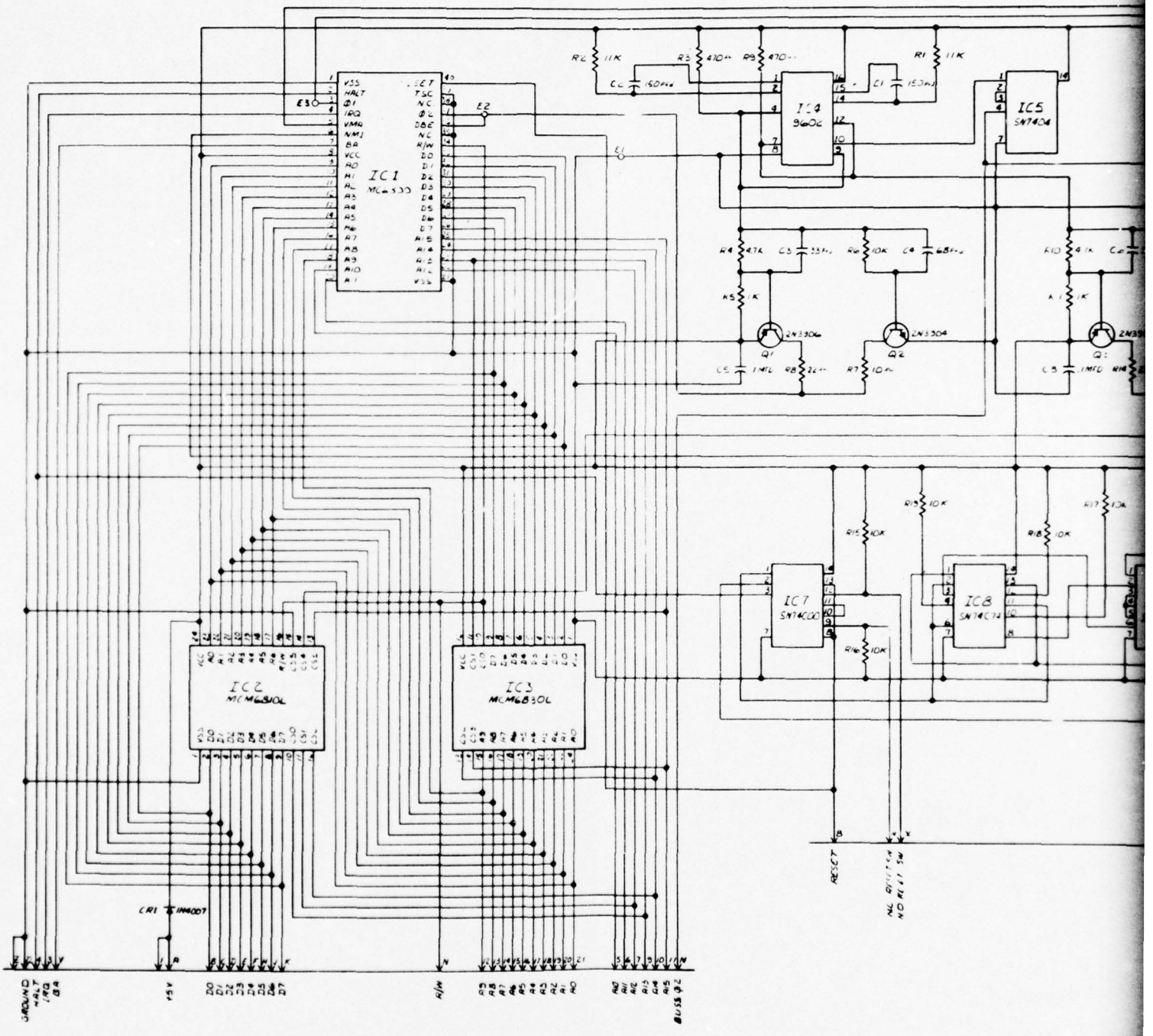
IC1
IC2
MCM6830L
IC3
MCM6830L
IC4
9602
IC5
SN7404
IC7
SN74C00
IC8
SN74C14
R2 11K
R3 470Ω
R9 470Ω
R1 11K
C2 150PFD
C1 150PFD
R4 47K
C3 33PFD
R6 10K
C4 68PFD
R5 K
Q1 2N3906
Q2 2N3904
C5 1MFD
R8 22K
R7 10K
R15 10K
R16 10K
R18 10K
R19 10K
R17 13K
CR1 1N4007
E1
E2
E3
RESET
NO MI / SW
GROUND
HALT
IRQ
Ø4
15V
D0
D1
D2
D3
D4
D5
D6
D7
R/W
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
BUSS Ø2

Figure 6

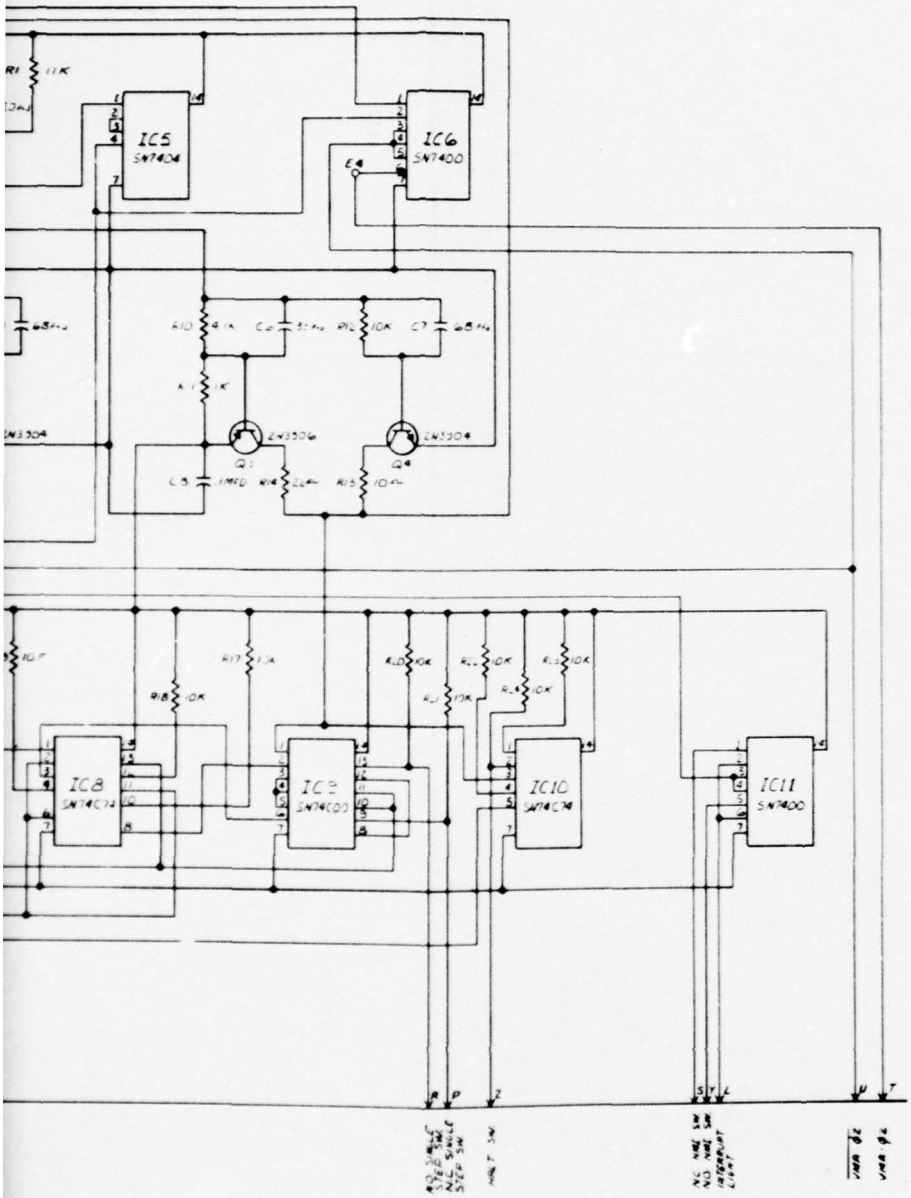

Figure 6. MPU and 2φ clock schematic.

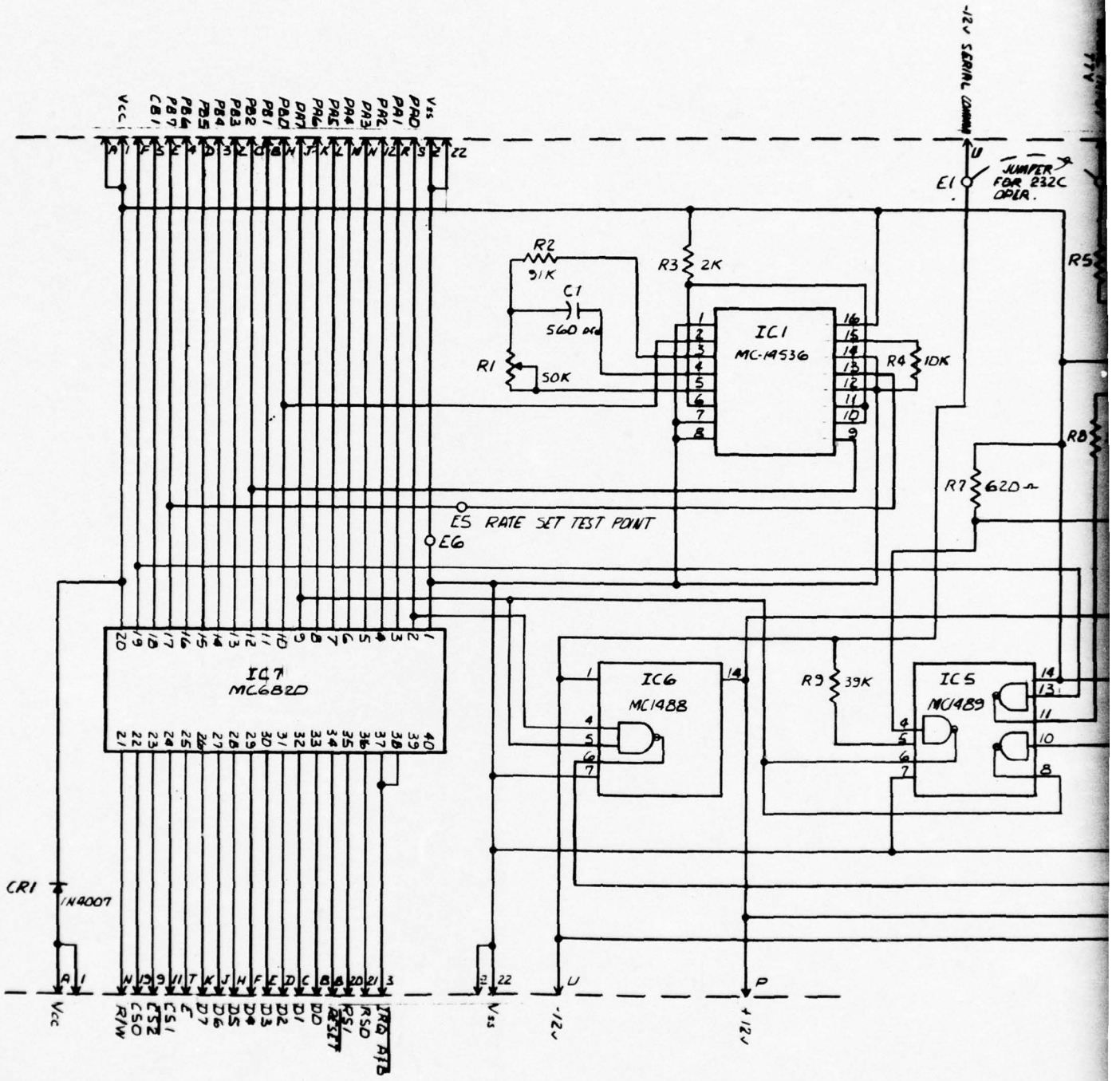

Figure 7. Teletype

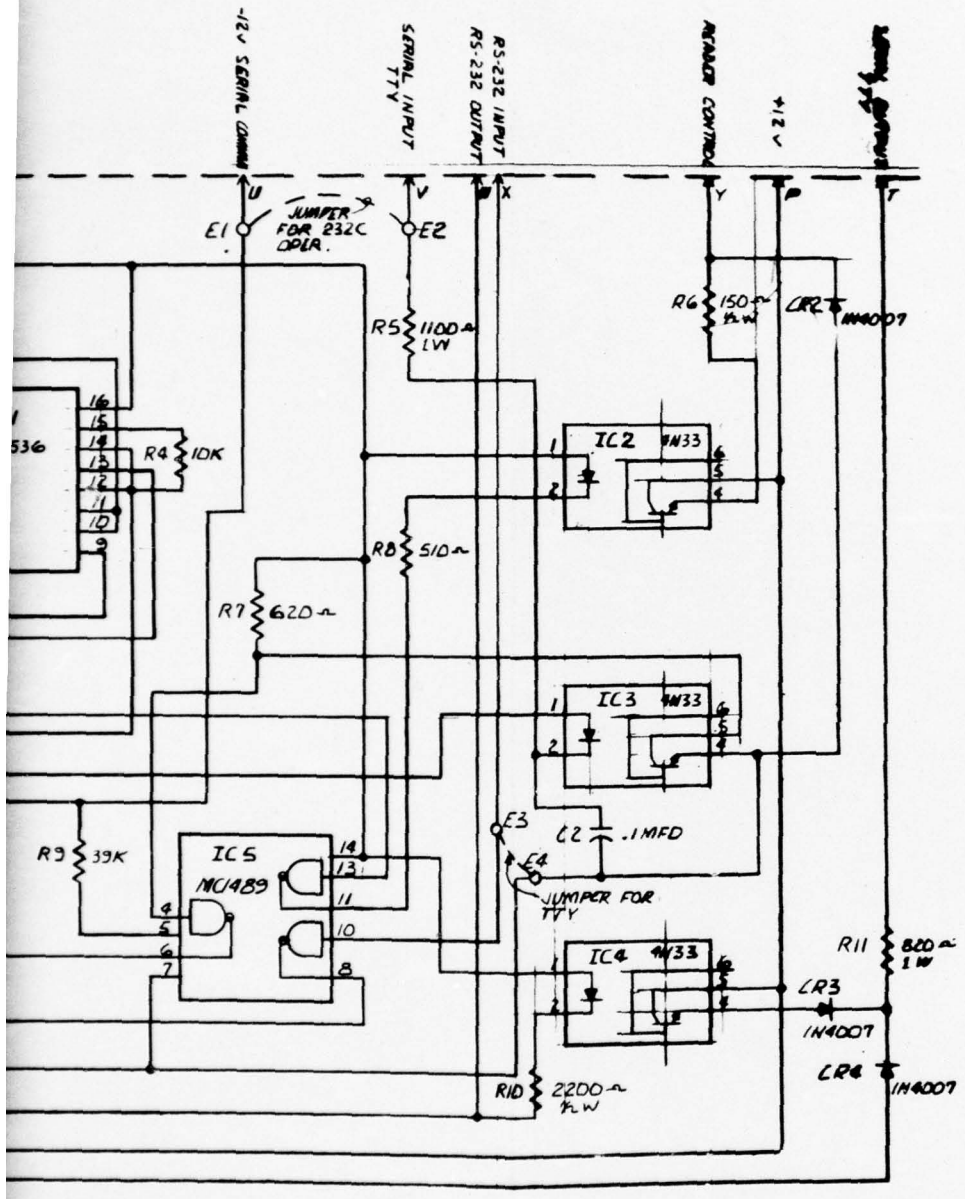

Figure 7. Teletype peripheral interface adapter board.

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APPENDIX

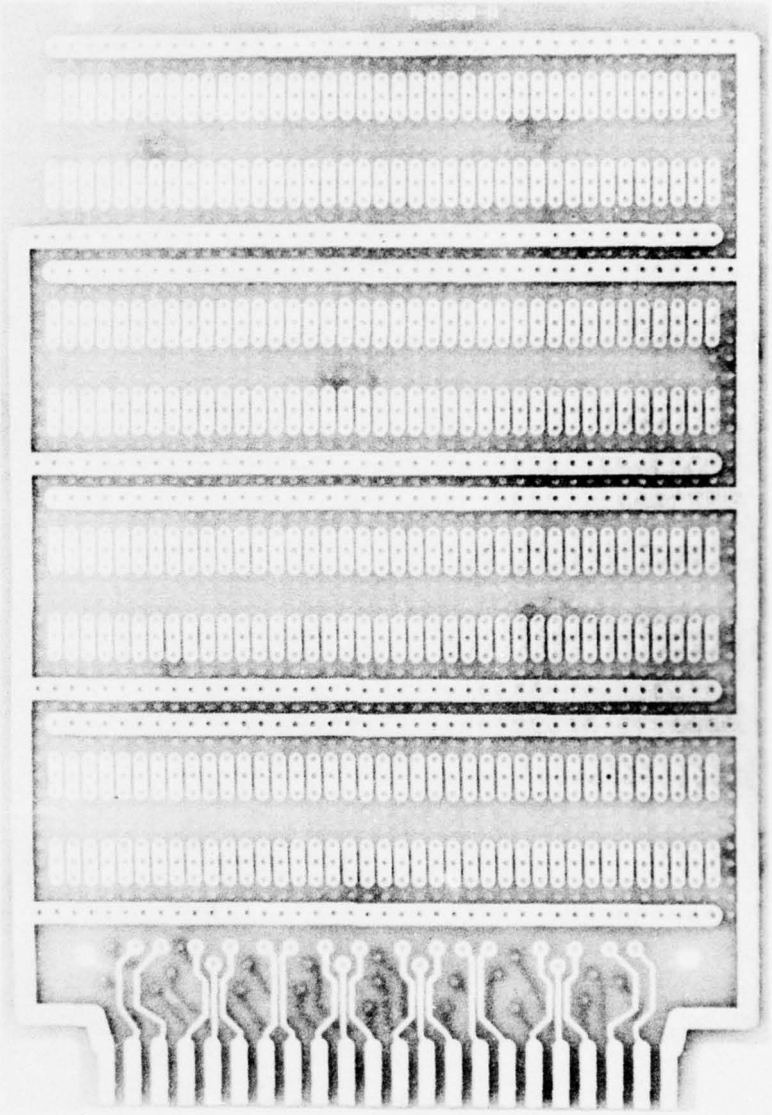

Figure A-1. Single 44-pin DIP board.

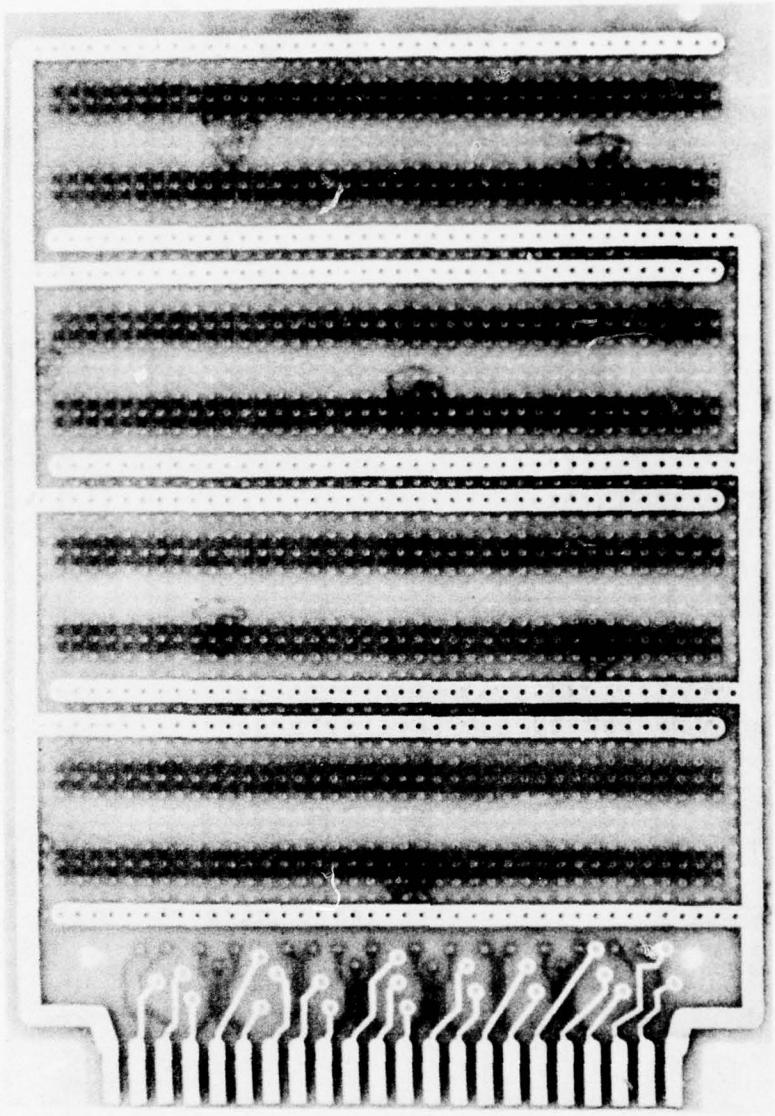

Figure A-1. (Concluded).

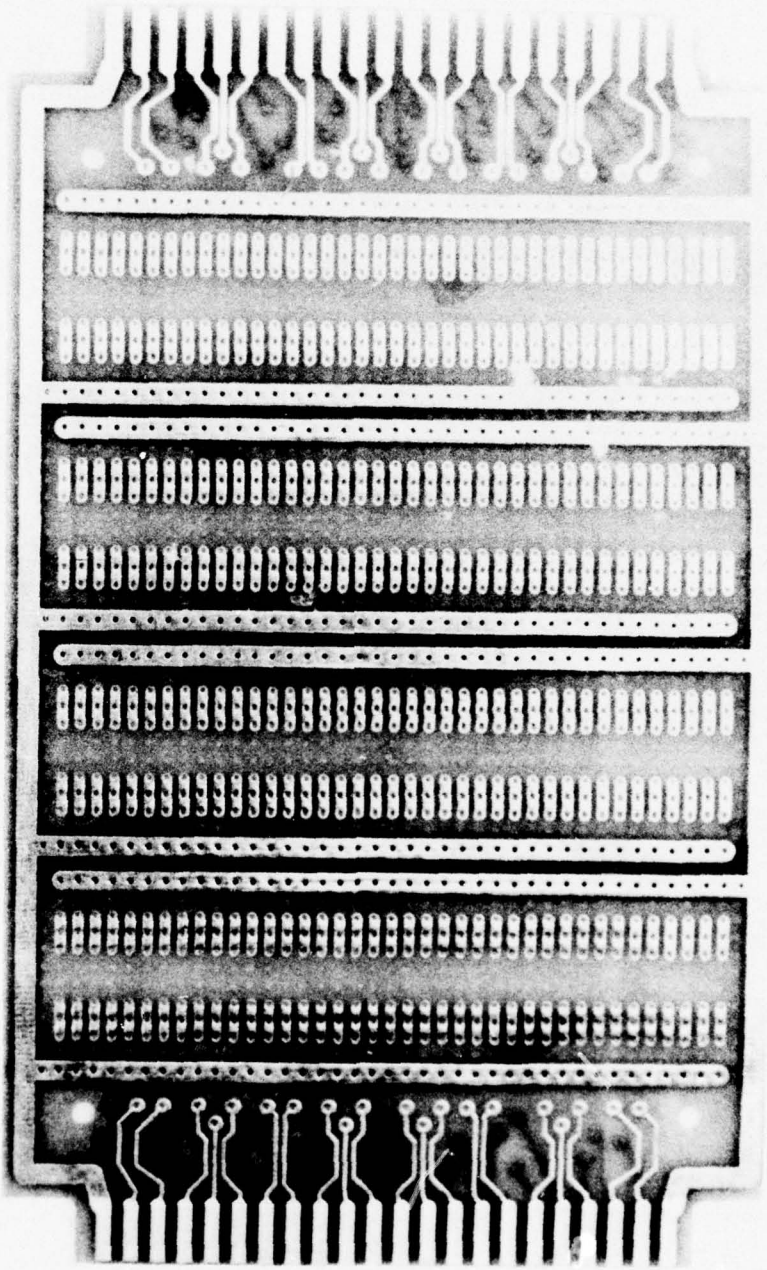

Figure A-2. Double 44-pin DIP board.

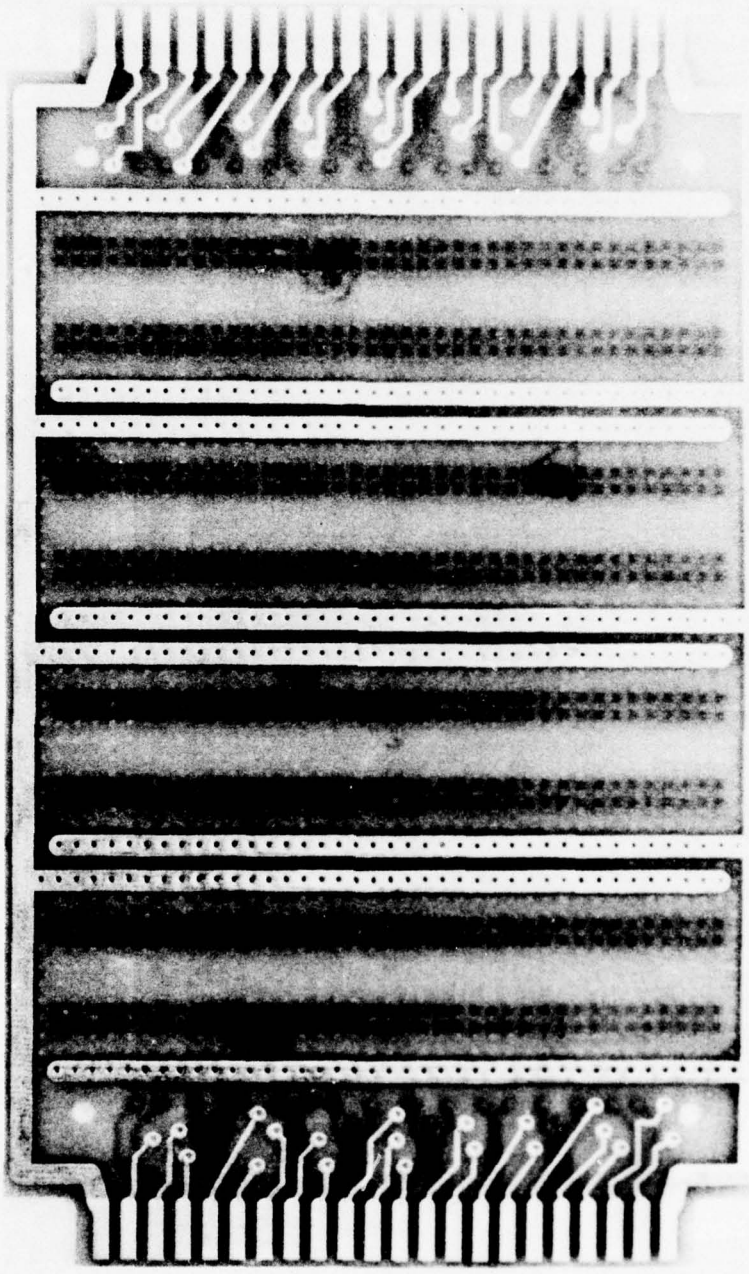

Figure A-2 (Concluded).

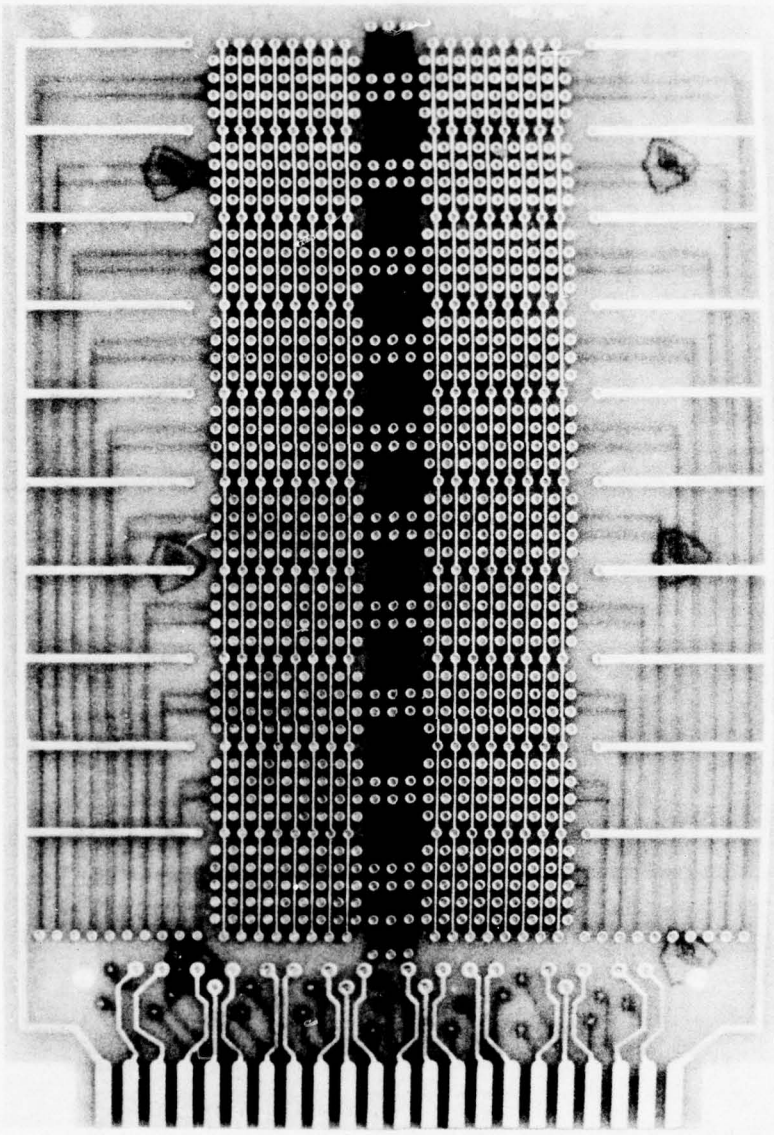

Figure A-3. Single 44-pin 20 in. × 16 in. matrix board.

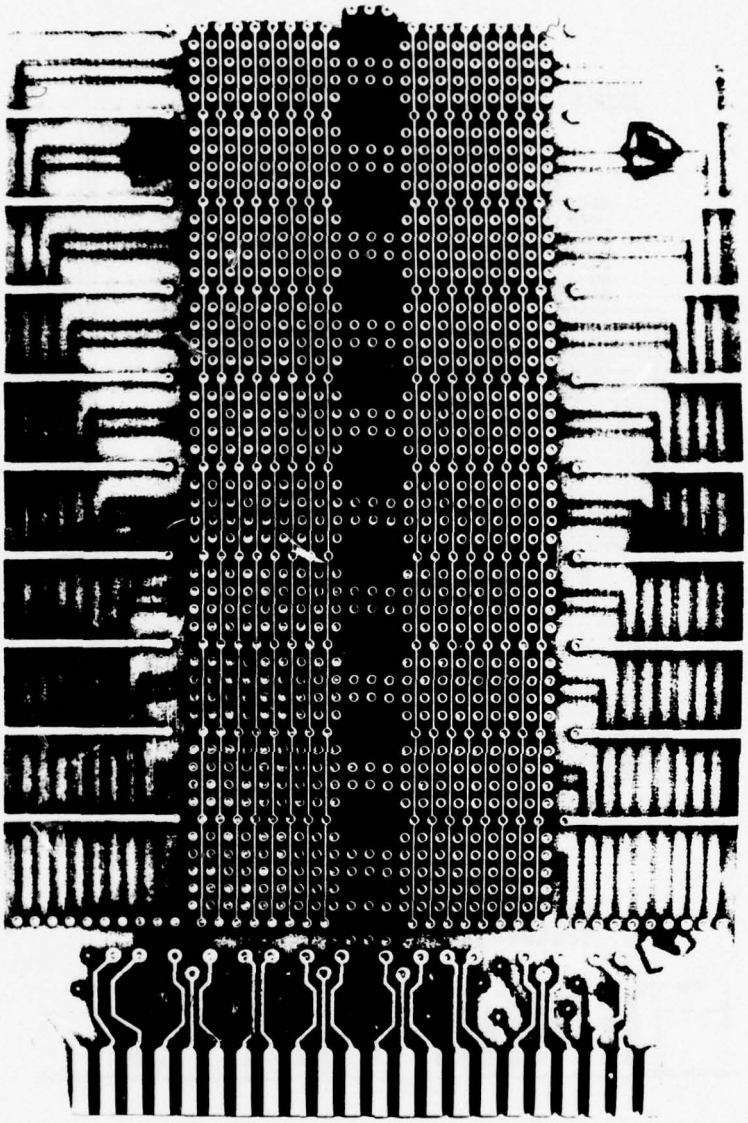

Figure A-3. (Concluded).

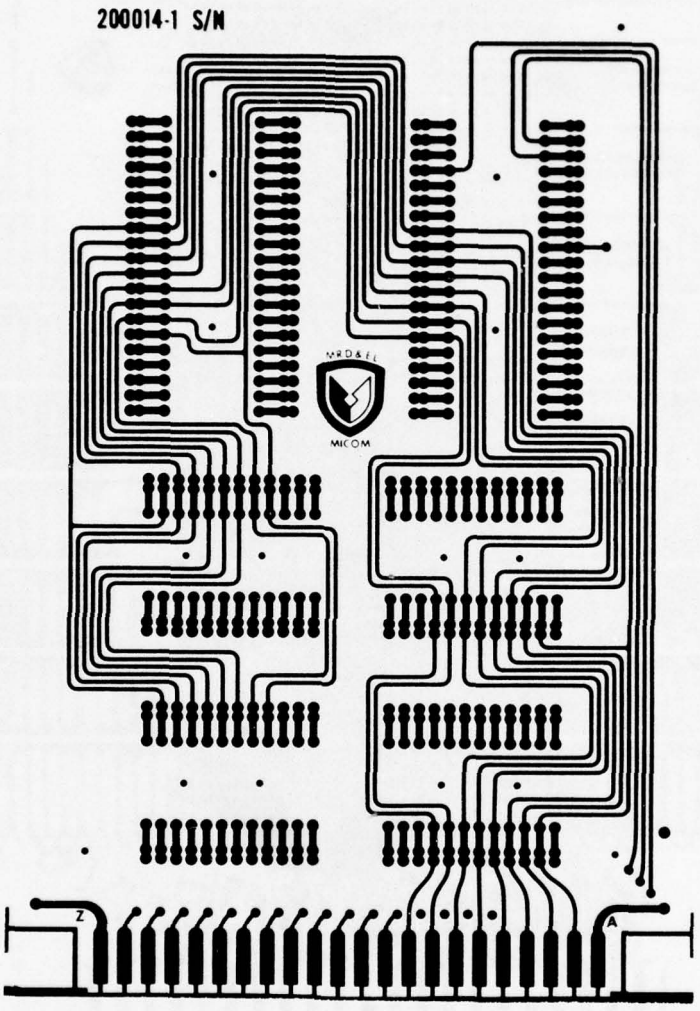

Figure A-4. Motorola MPU-less control and clock circuits.

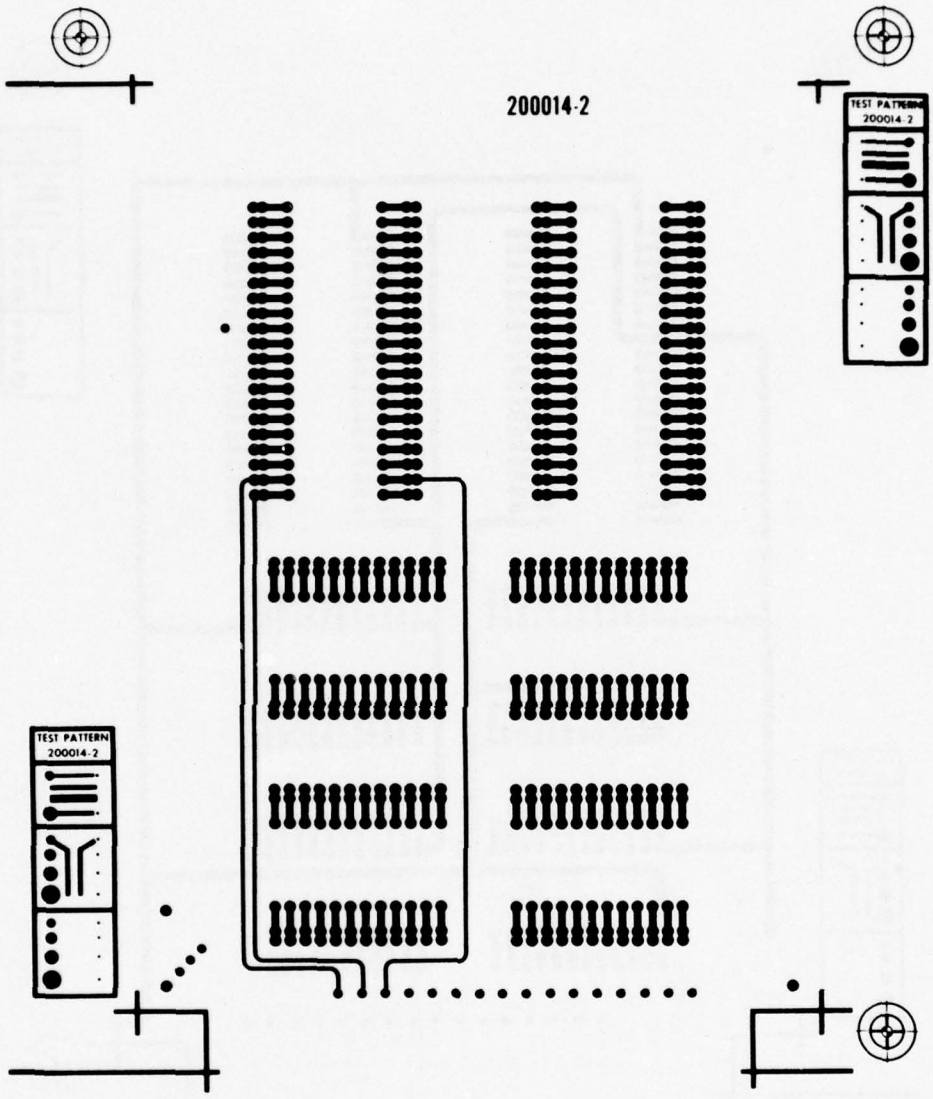

Figure A-4. (Continued).

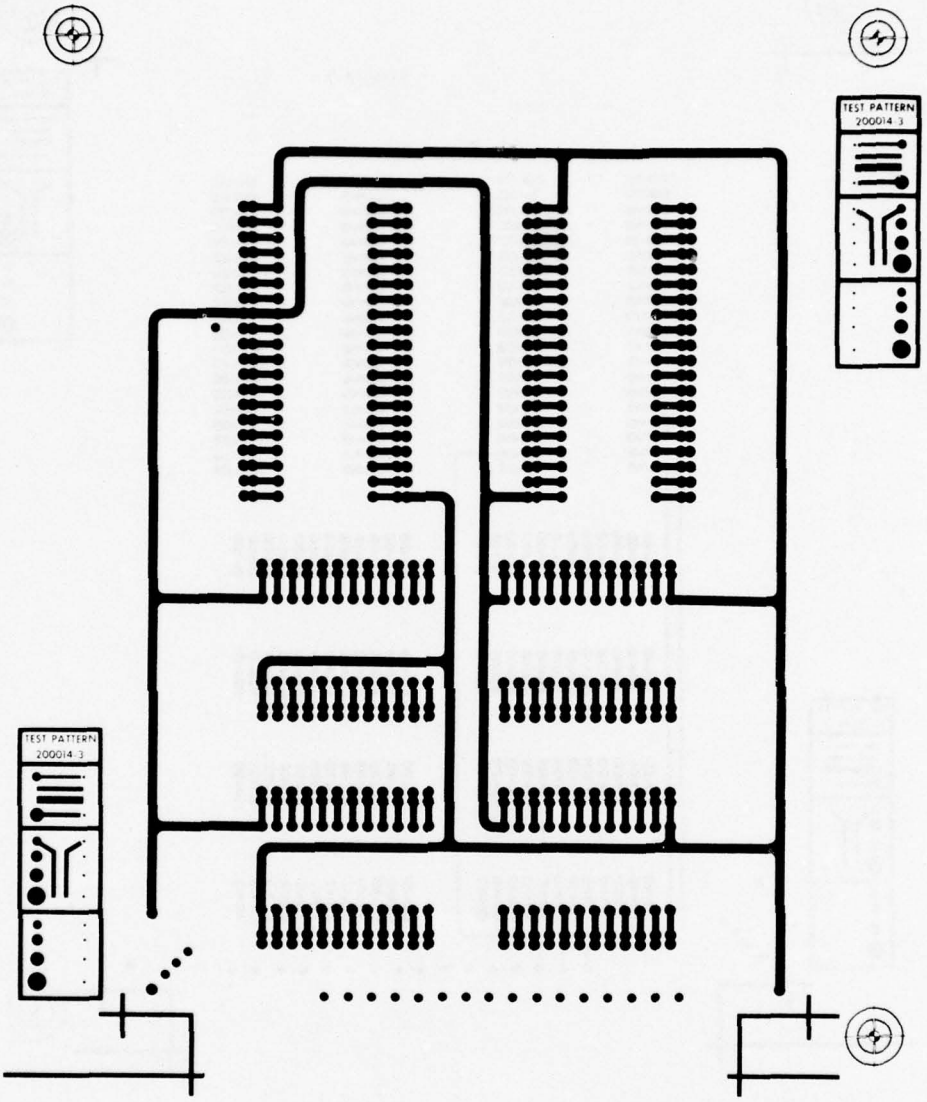

Figure A-4. (Continued).

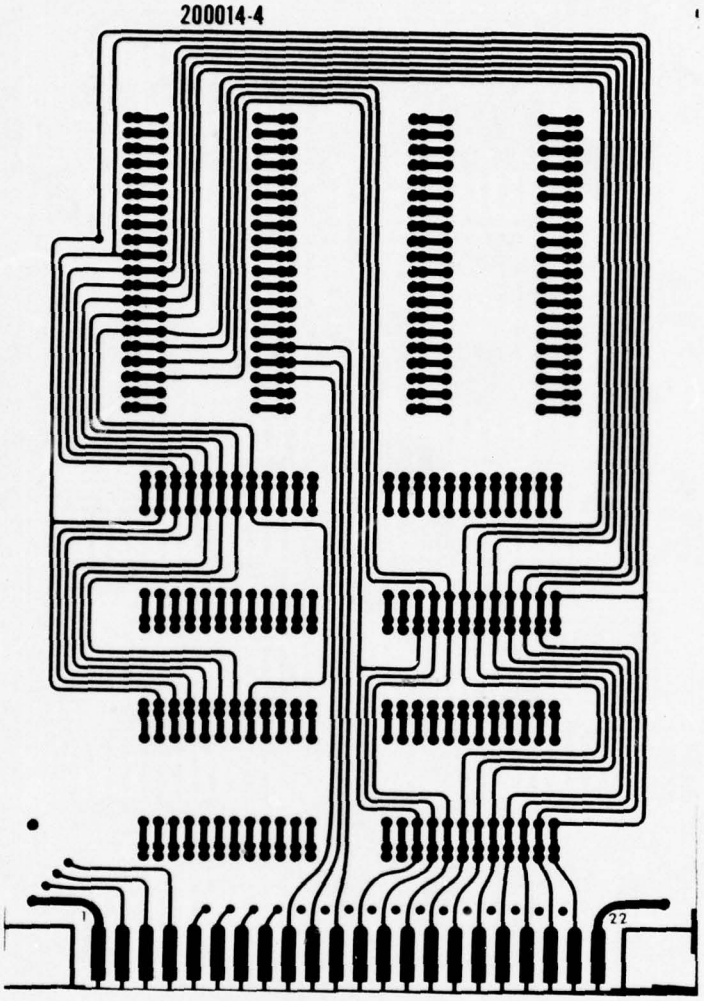

Figure A-4. (Concluded).

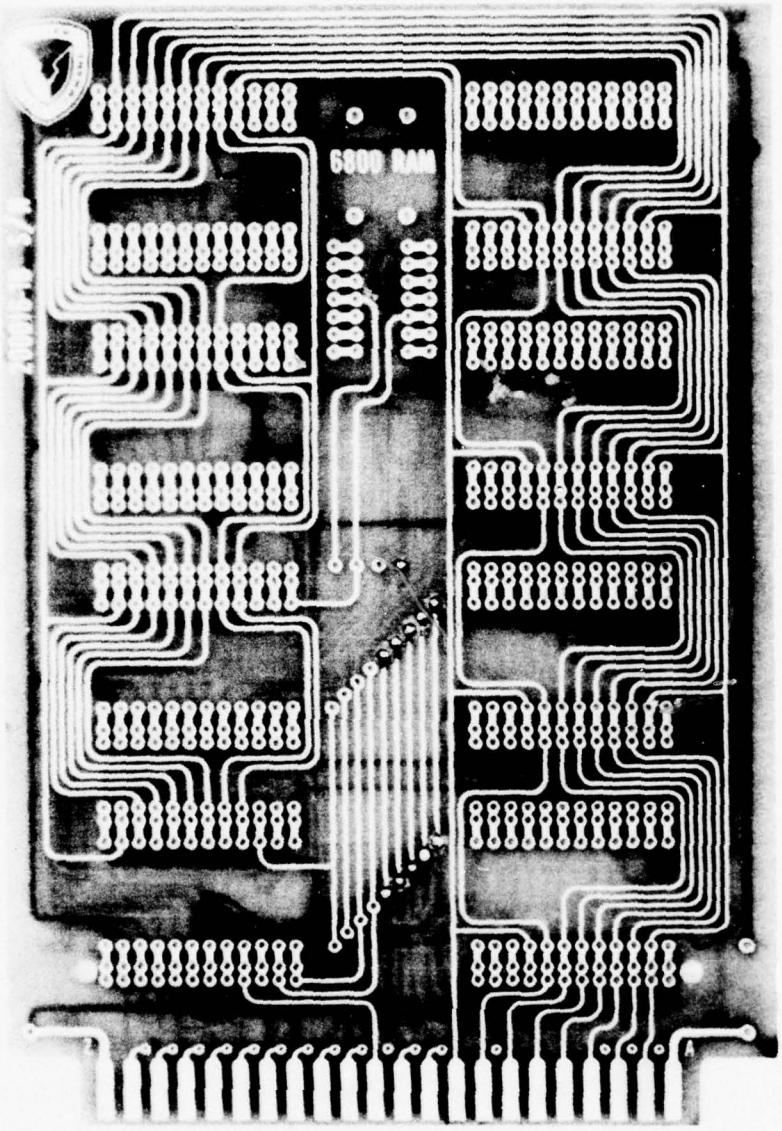

Figure A-5. Motorola MPU RAM (1K × 8).

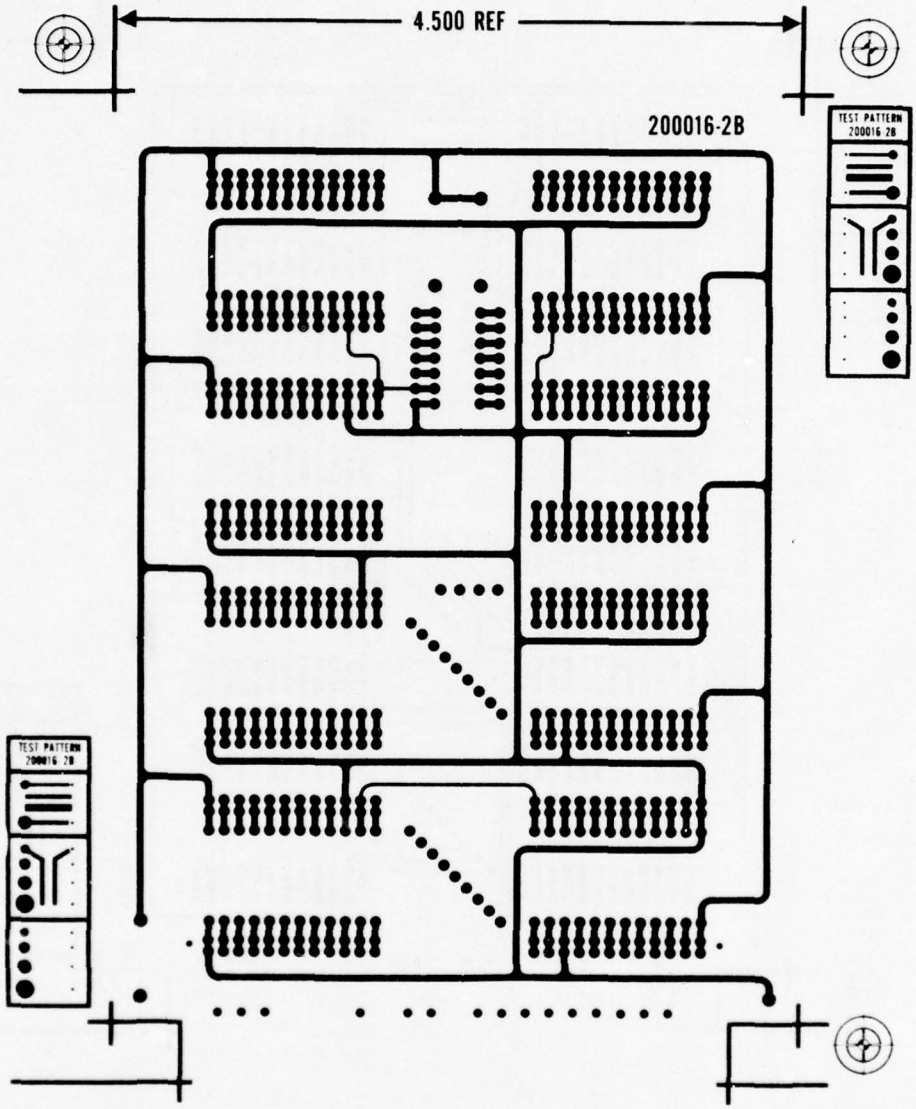

Figure A-5. (Continued).

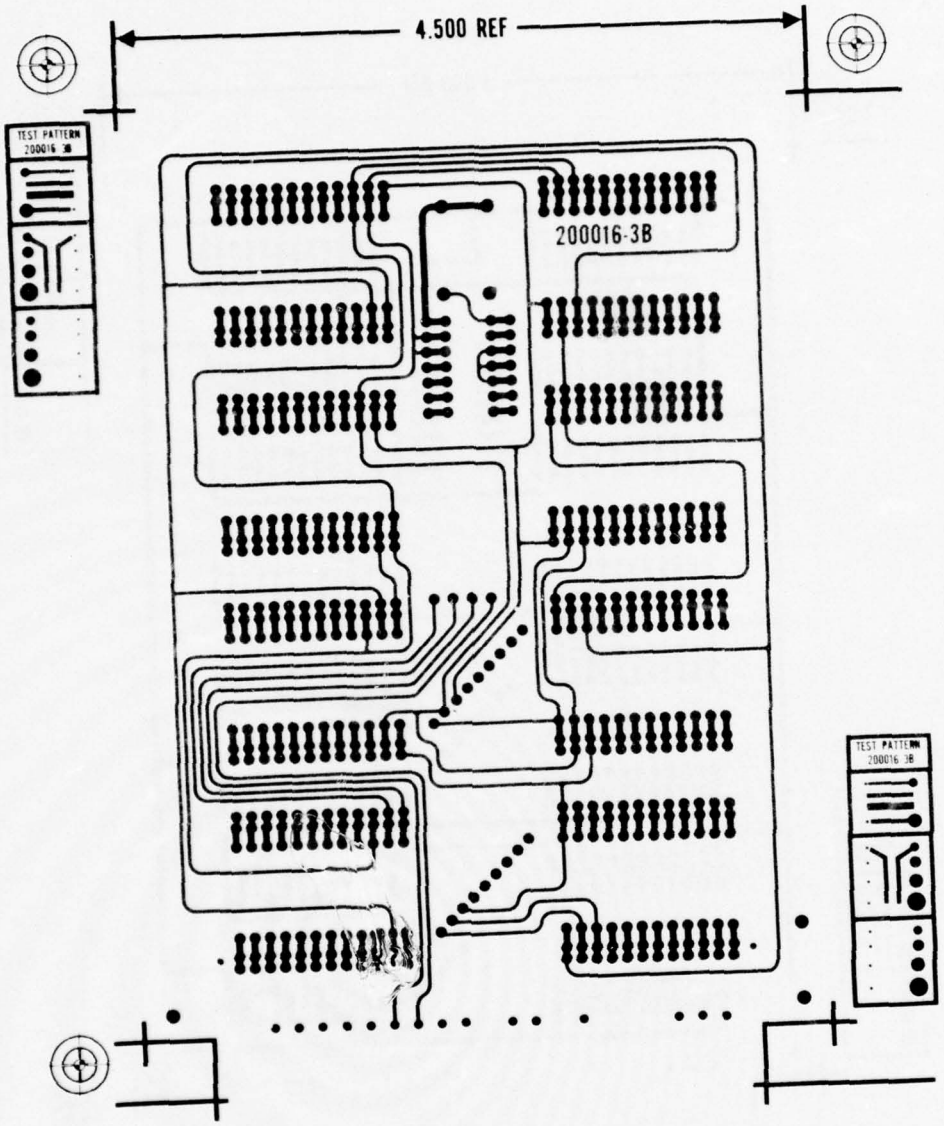

Figure A-5. (Continued).

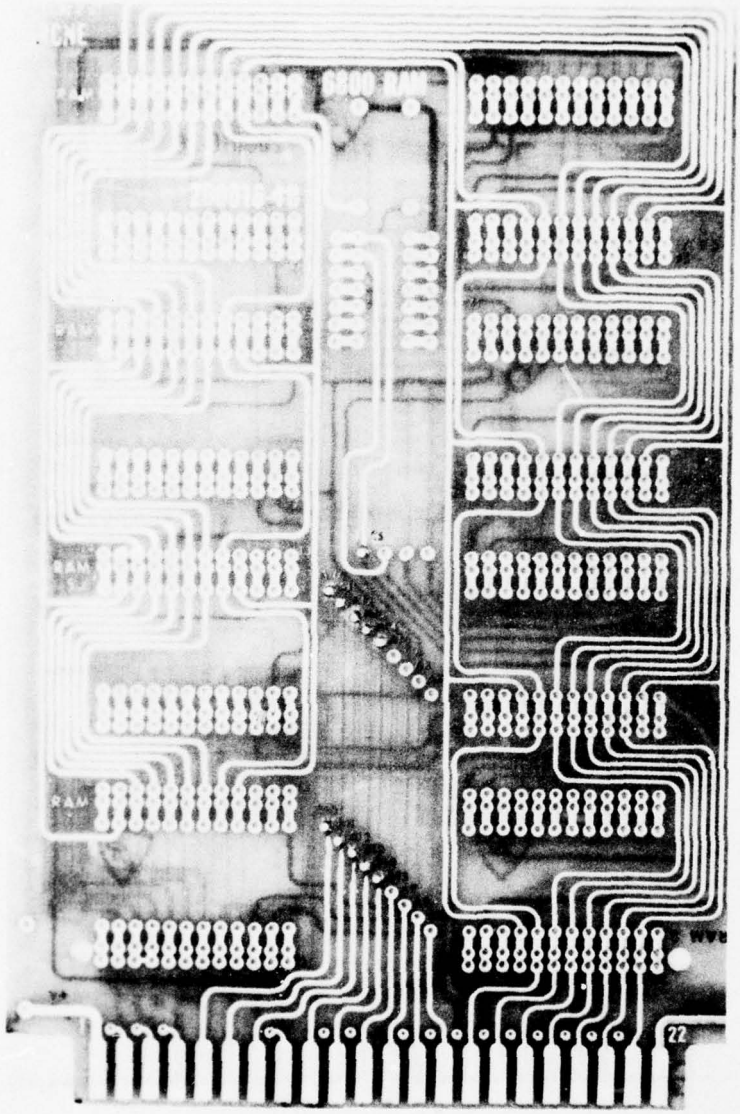

Figure A-5. (Concluded).

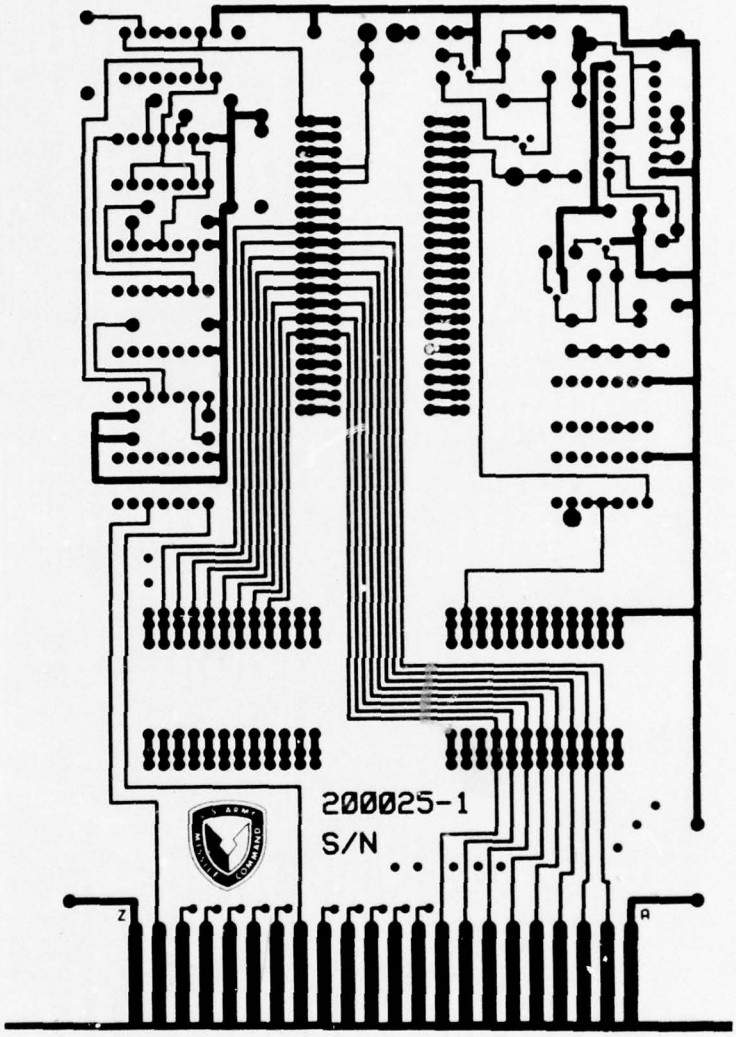

Figure A-6. Motorola MPU with discrete clock.

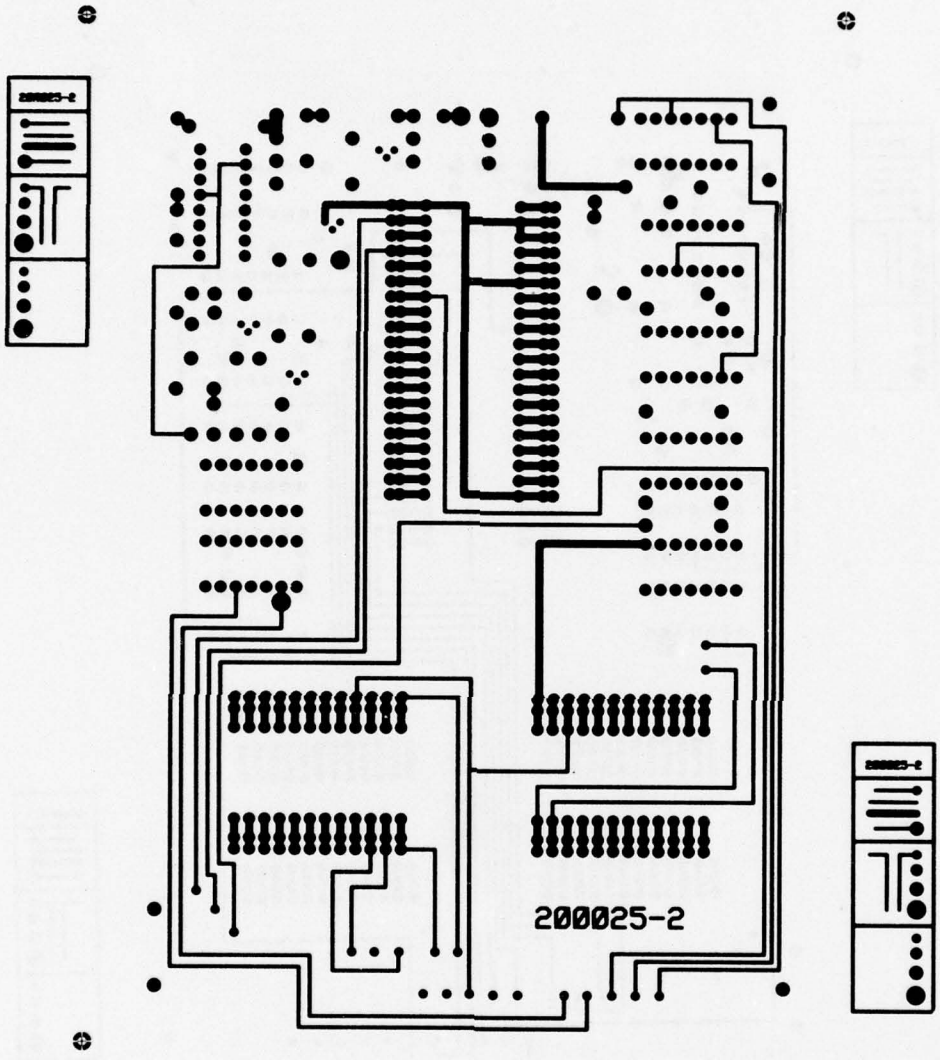

Figure A-6 (Continued).

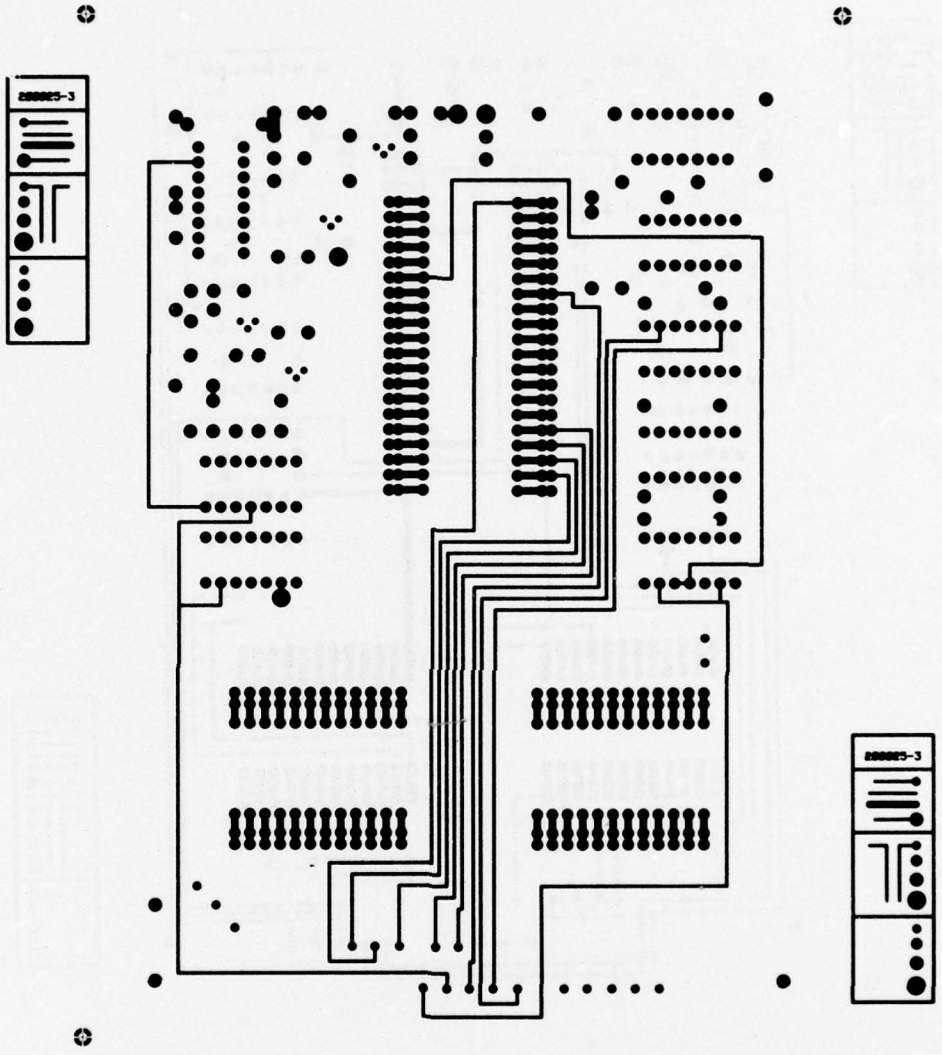

Figure A-6. (Continued).

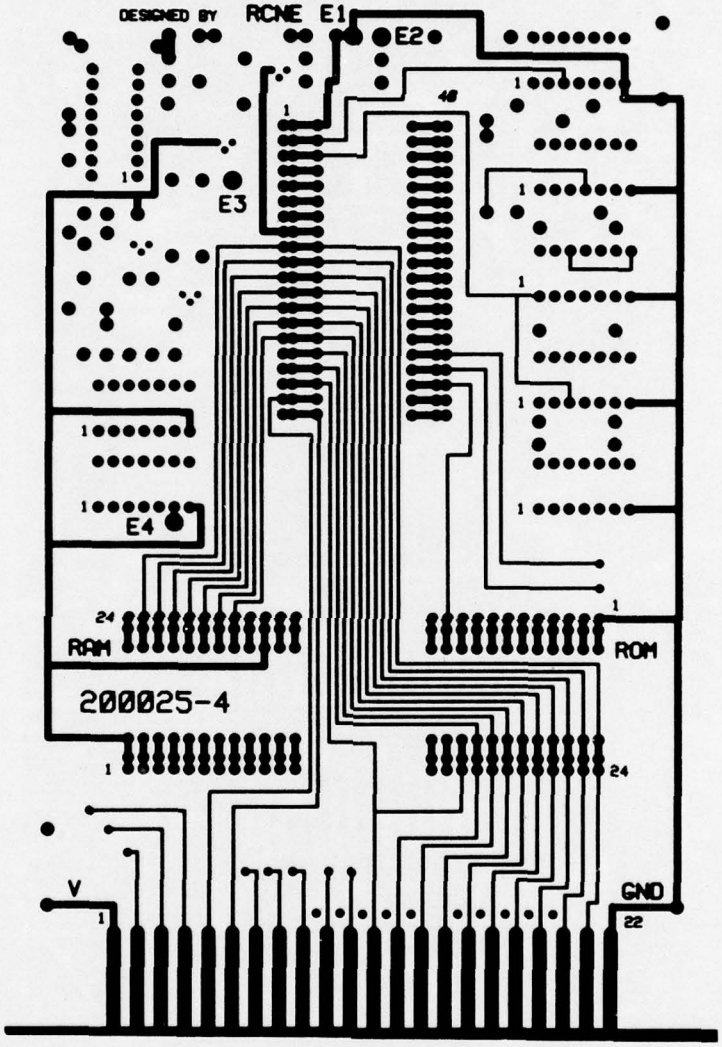

Figure A-6. (Concluded).

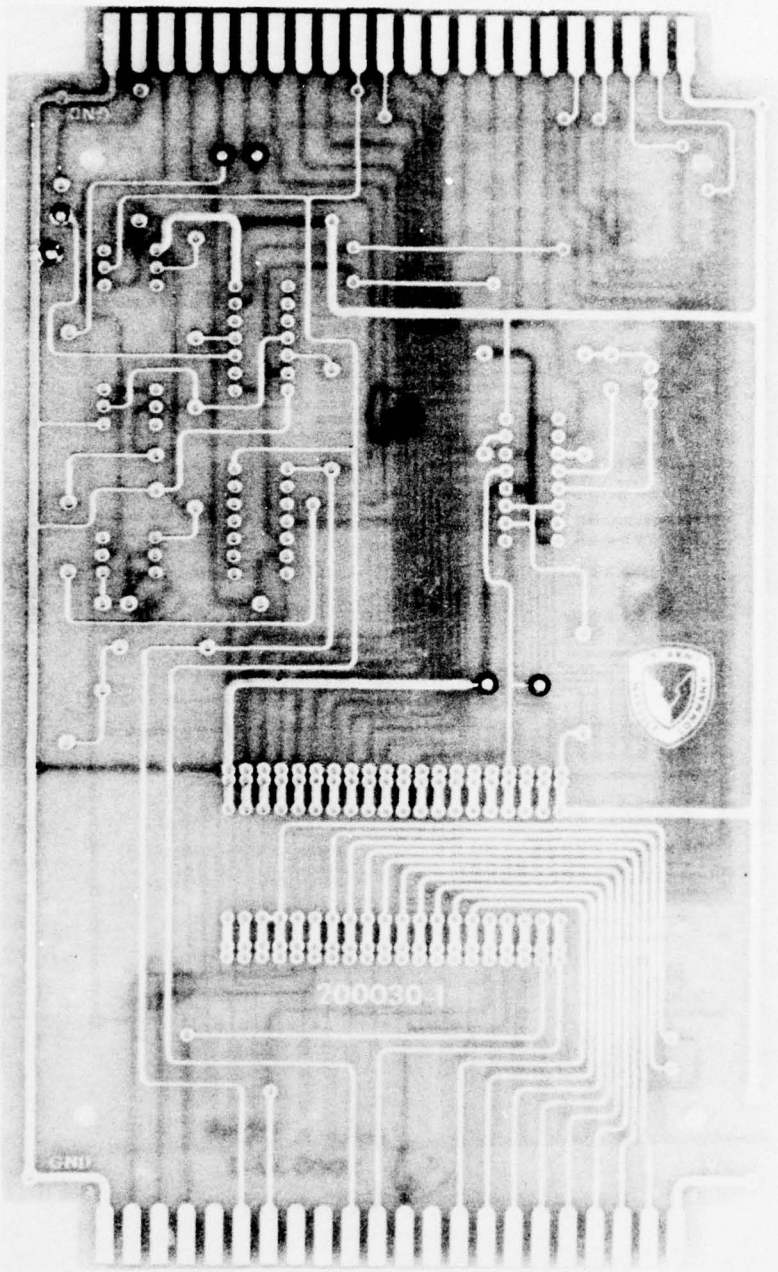

Figure A-7. MPU interface PIA with rate generator.

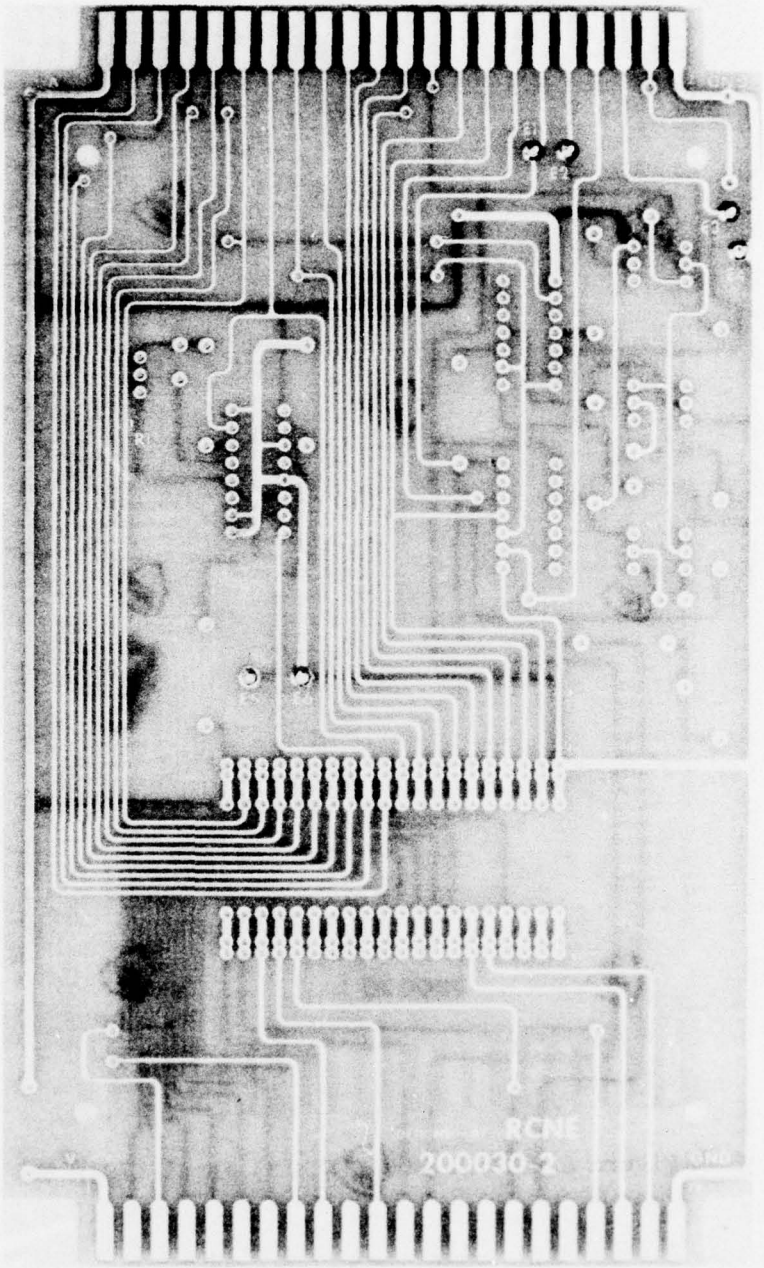

Figure A-7 (Concluded).

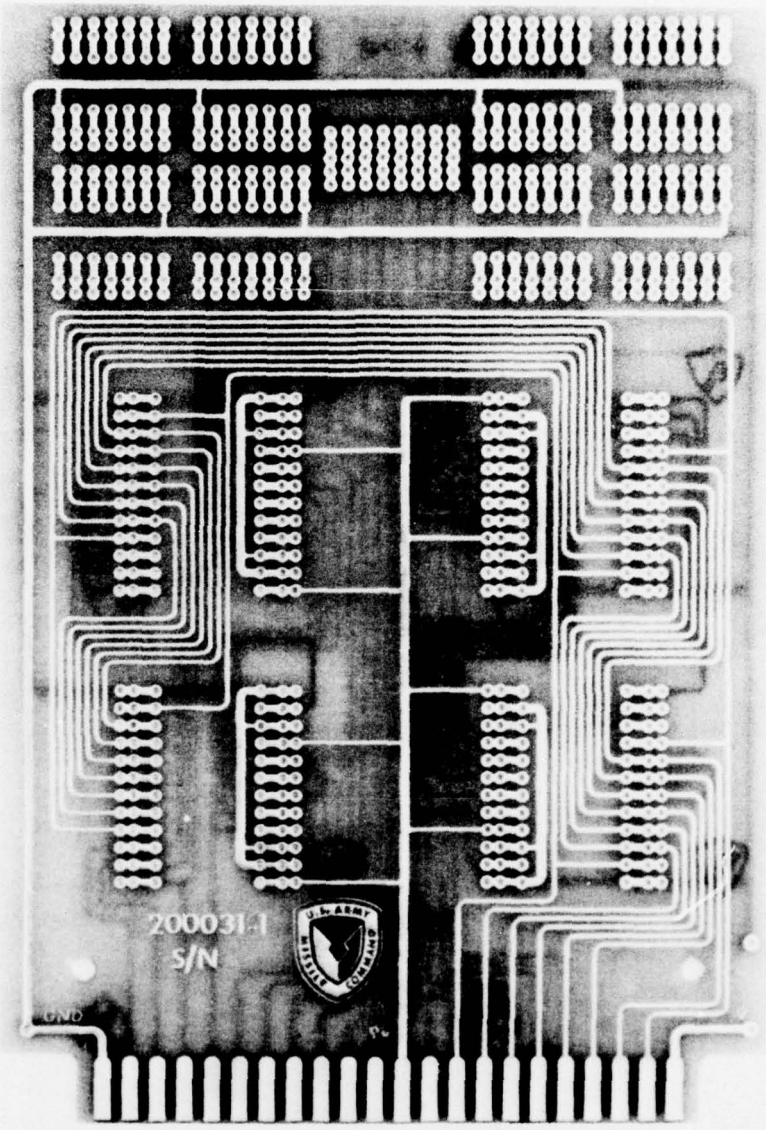

Figure A-8. MPU ROM (1K × 8) intel 1702.

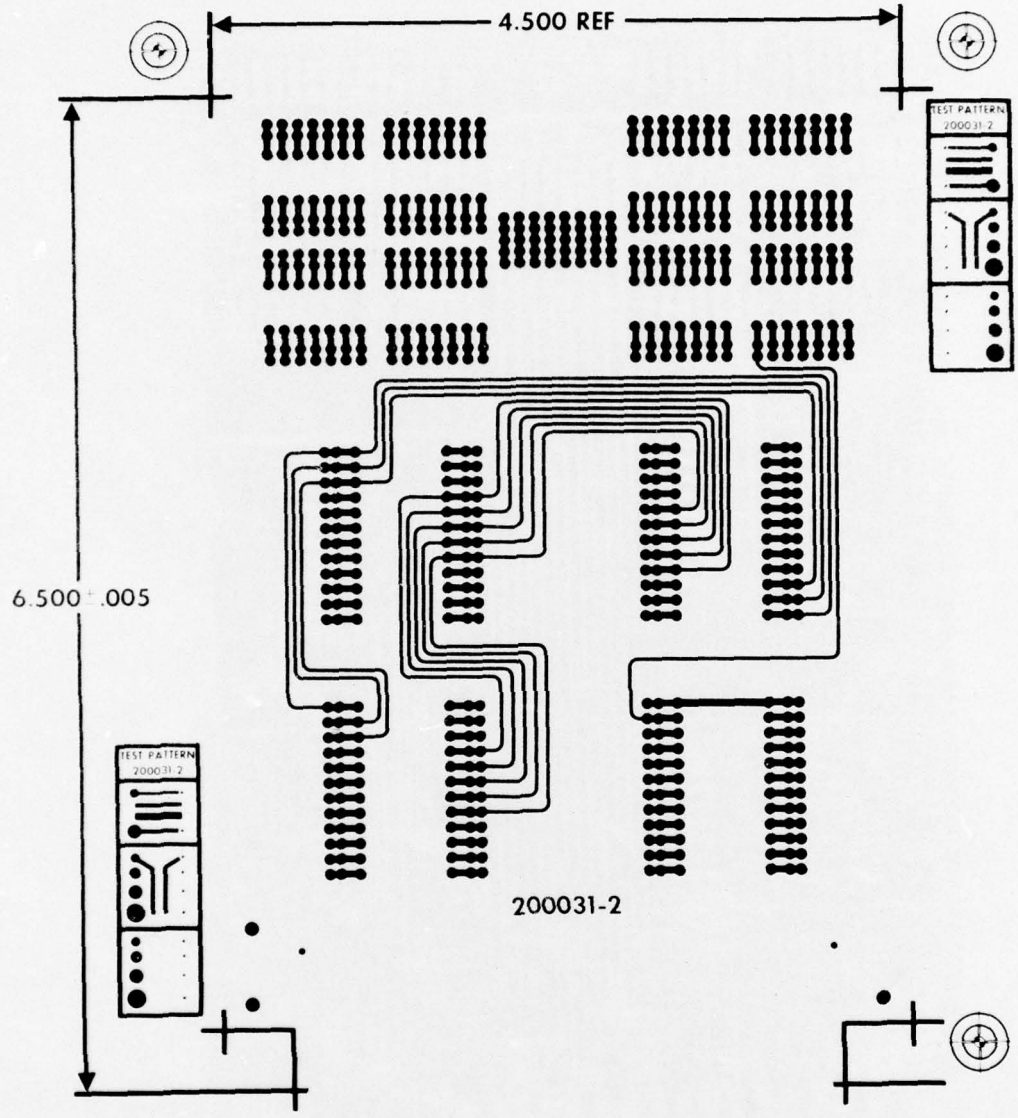

Figure A-8. (Continued).

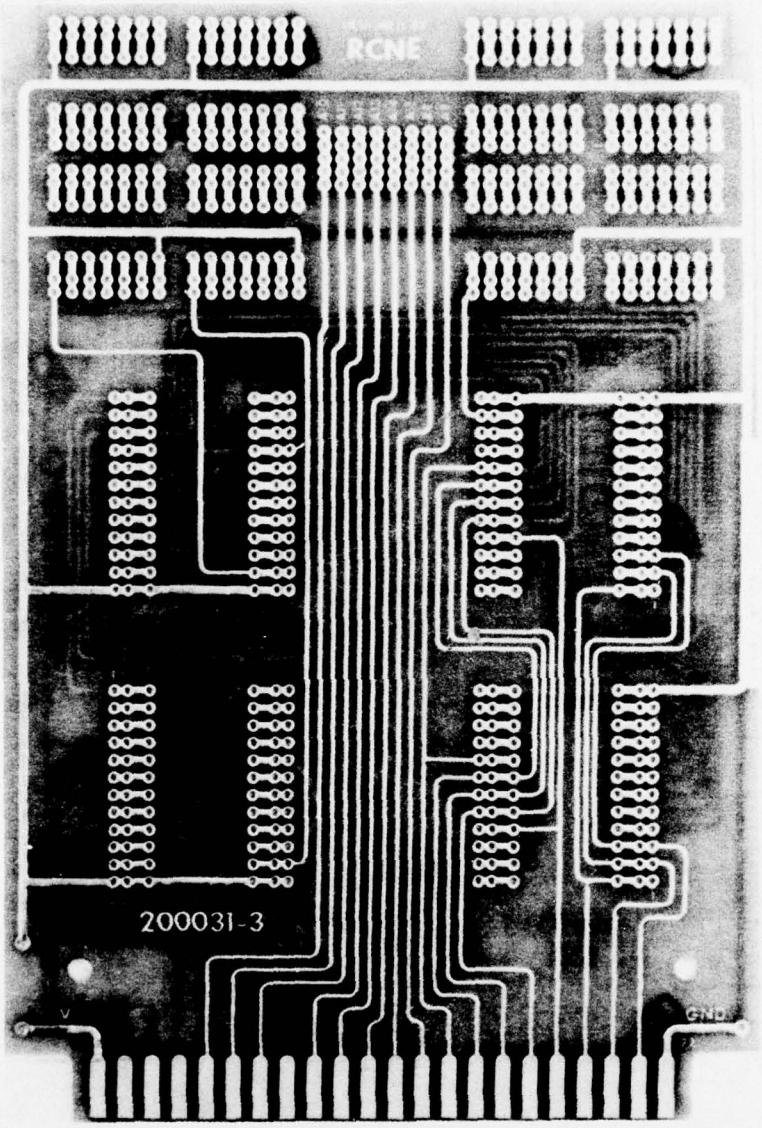

Figure A-8. (Concluded).

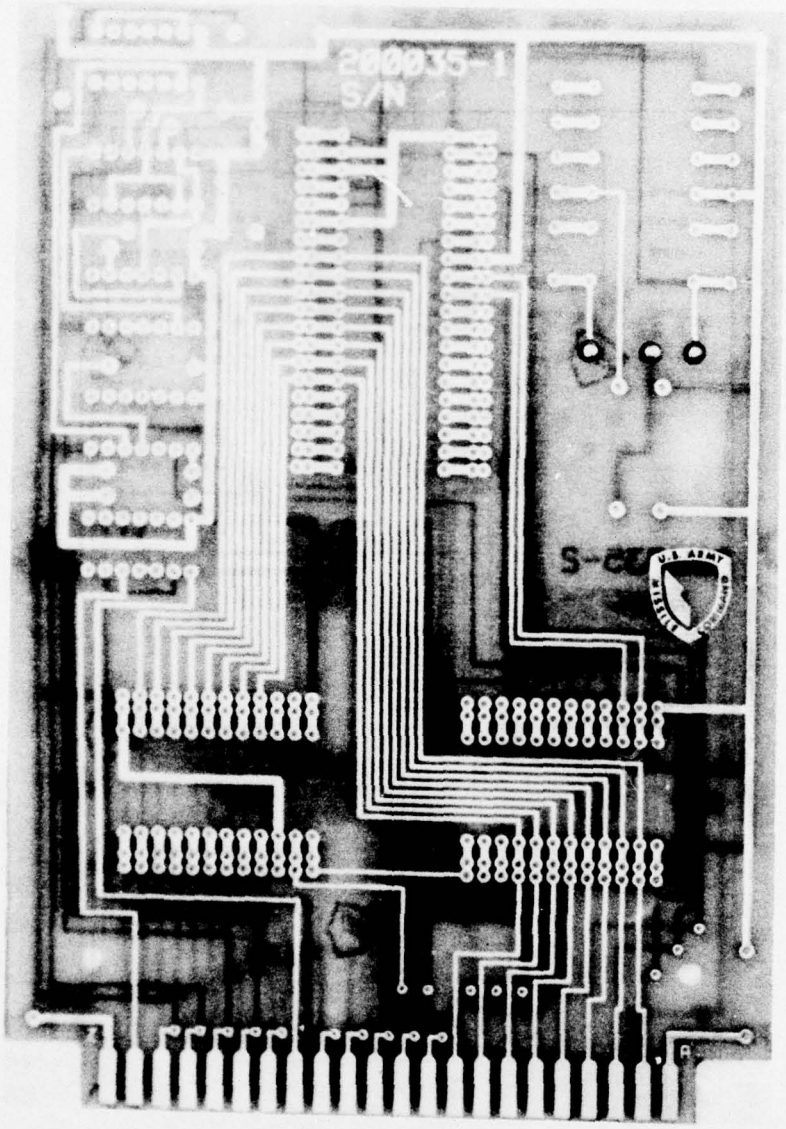

Figure A-9. Motorola MPU with IC clock.

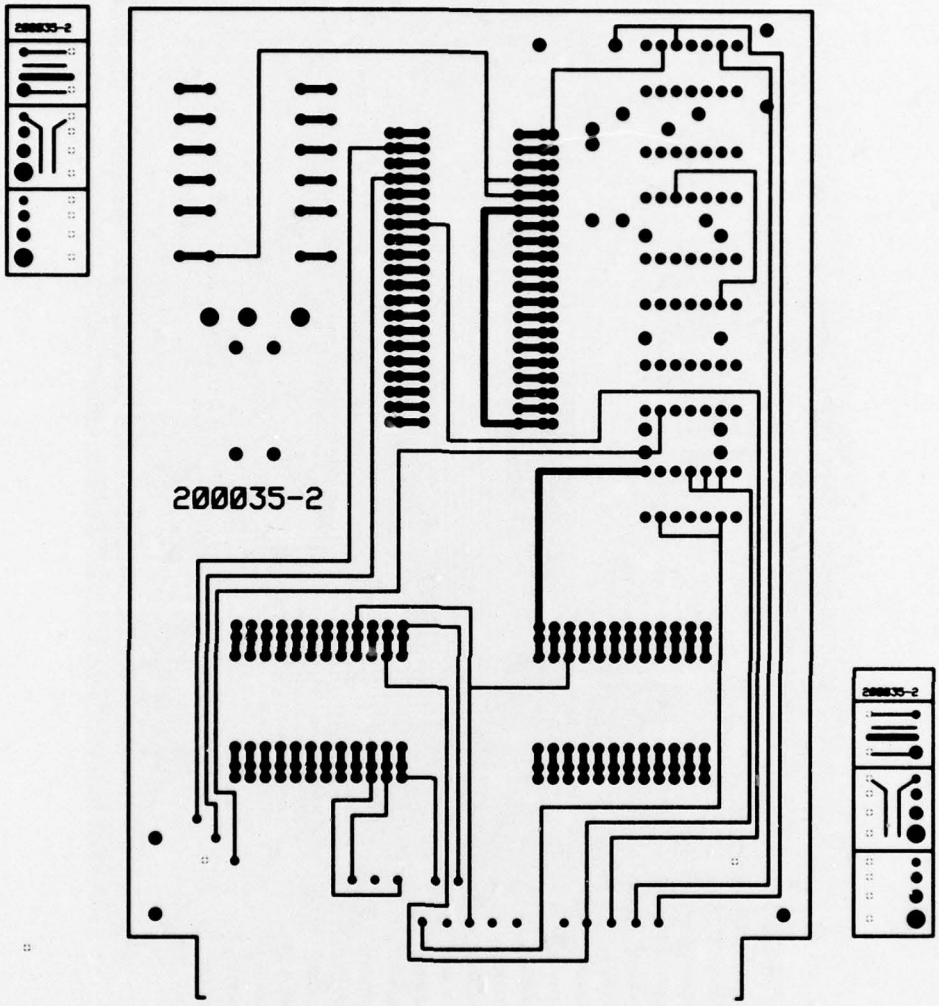

Figure A-9. (Continued).

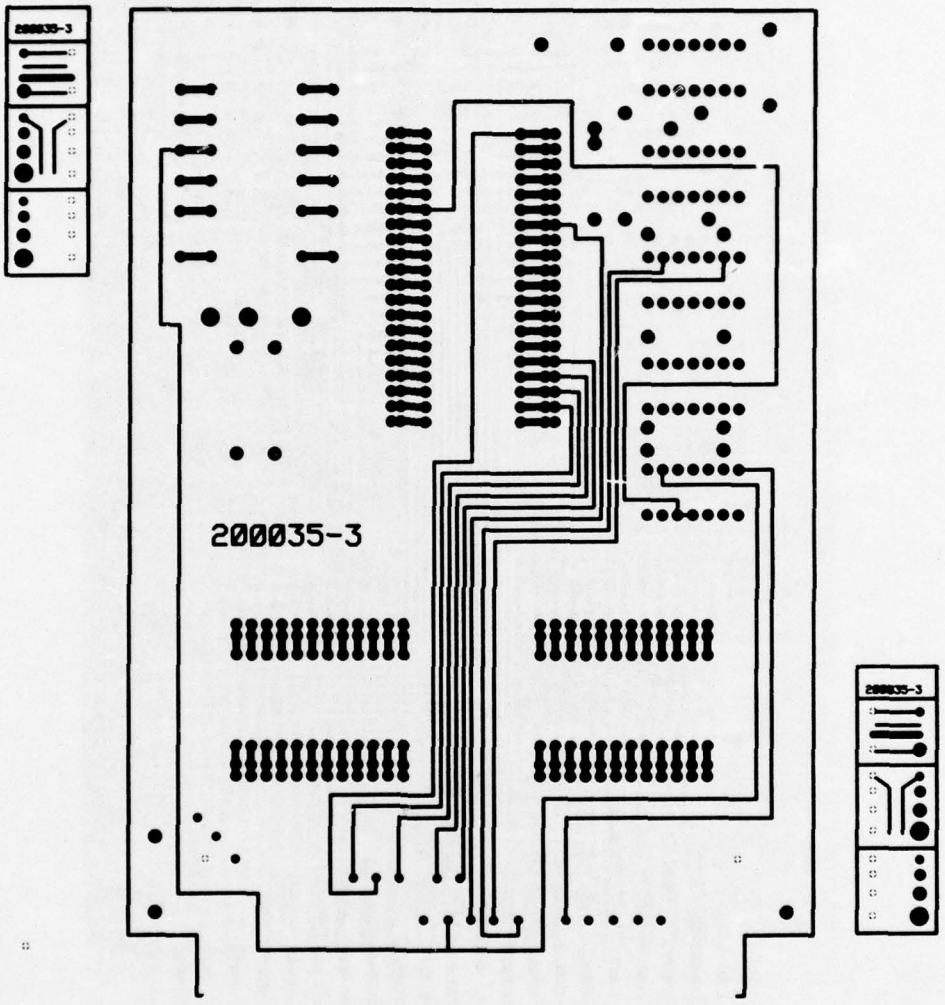

Figure A-9. (Continued).

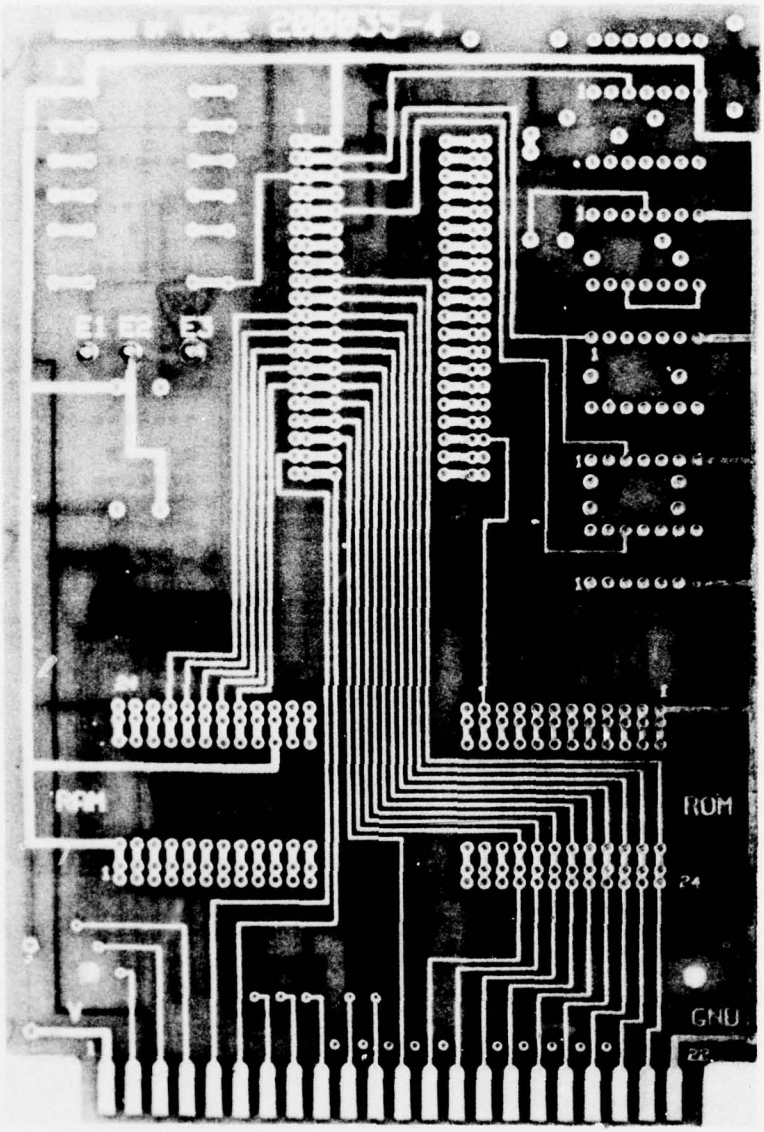

Figure A-9. (Concluded).

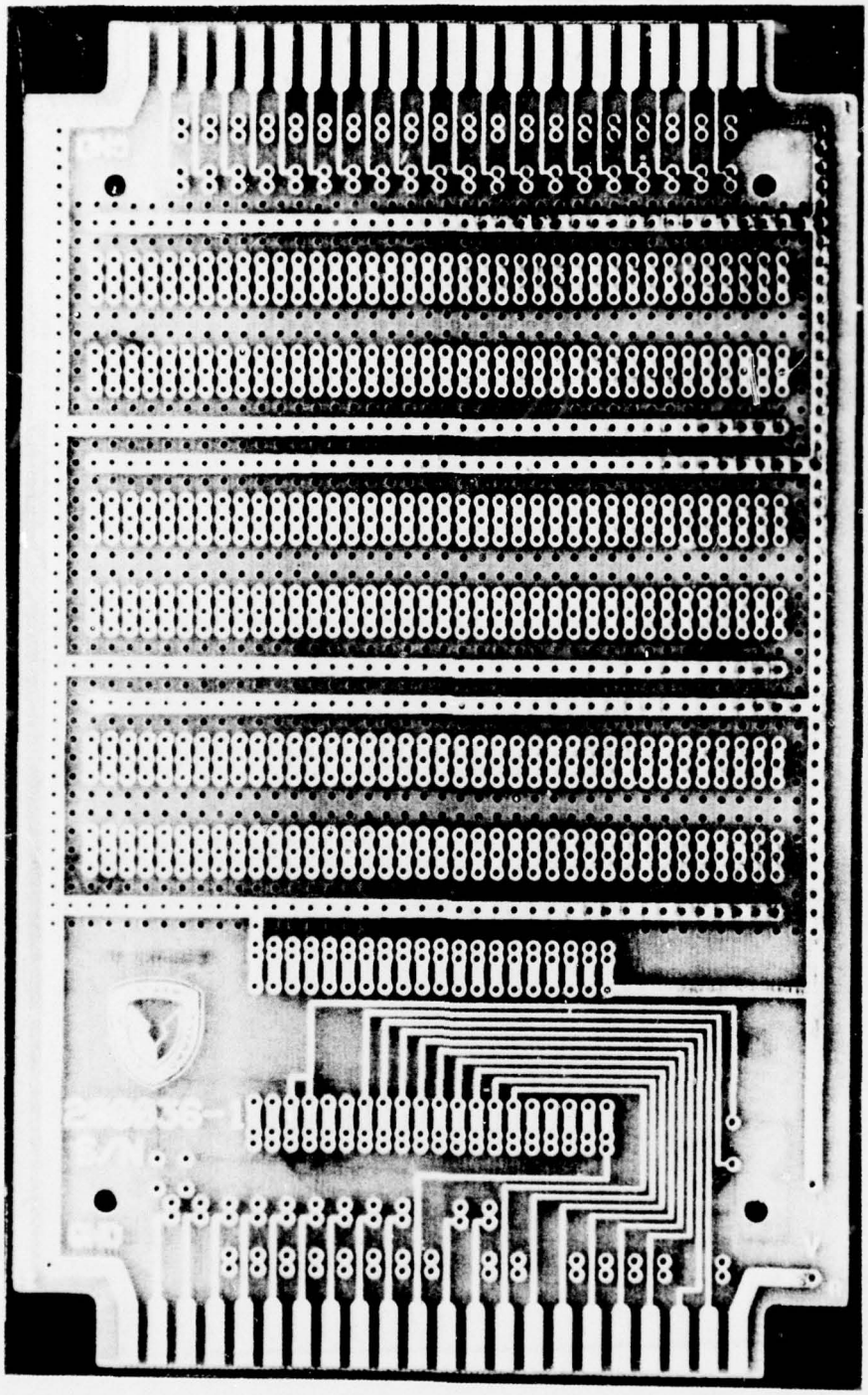

Figure A-10. General interface PIA.

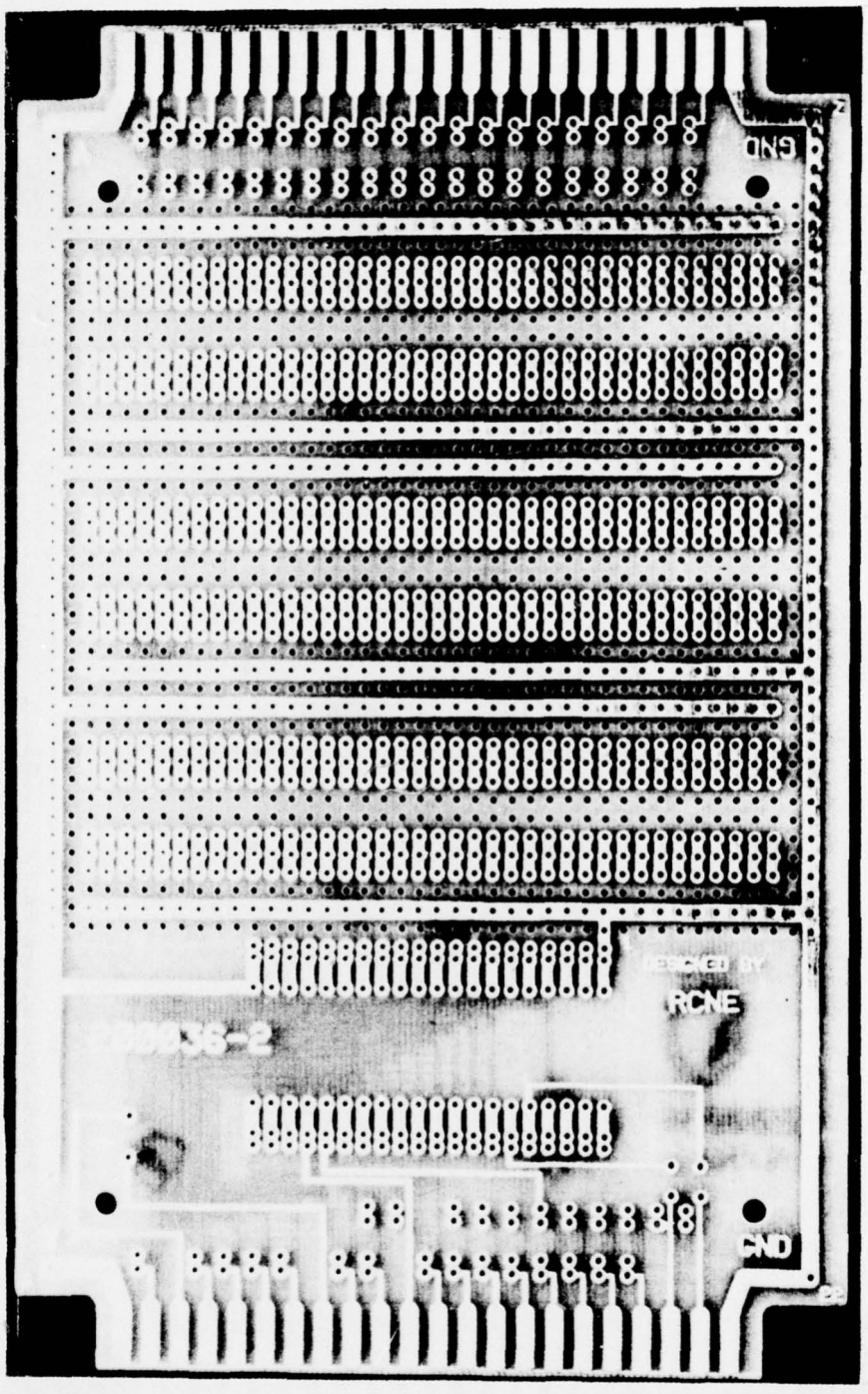

Figure 10. (Concluded).

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