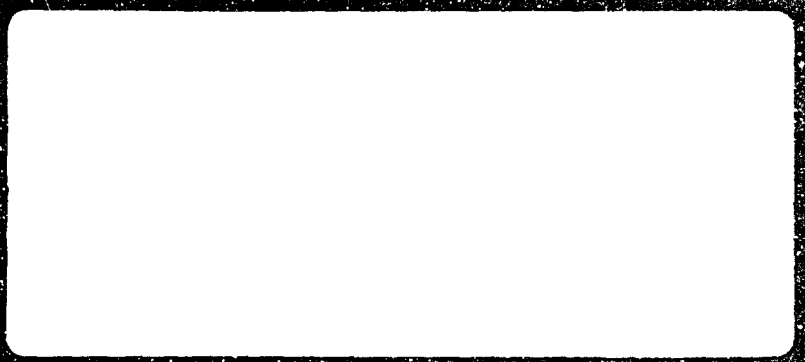
CCD PHOTOSENSOR ARRAY DEVELOPMENT PROGRAM (PHASE II), AND APPENDIX A: DISTRIBUTED FLOATING-GATE AMPLIFIER (DFGA)

Fairchild Space and Defense Systems

Prepared for:

Naval Electronic Systems Command

April 1975



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FAIRCHILD SPACE AND DEFENSE SYSTEMS
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Report No. ED-AX-61

CCD Photosensor Array Development Program (Phase II)

FINAL REPORT

April 1975

for

Naval Electronics Systems Command

Contract No. N00039-73-C-0015

Prepared by the Scientific and Engineering Staff of
Fairchild Camera and Instrument Corporation

FOREWORD

This report was prepared by the Scientific and Engineering Staff of Fairchild Camera and Instrument Corporation for the Naval Electronics Systems Command under Navy Contract No. N00039-73-C-0015. The work was performed in Fairchild's Research and Development Division, Palo Alto, California, and Space and Defense Systems Division, Syosset, New York.

The work, performed between 2 April 1973 and 30 August 1974, was directed for the Navy by Mr. L. Sumney (NESC). He was assisted by the following members of the tri-service review team: Dr. D.F. Barbe (NRL), Dr. R.A. Belt (AFAL), Mr. S.B. Campana (NADC), Dr. I. Lagnado (NELC), Mr. J.F. Martino (NVL), and Mr. H.J. Ubele (NADC).

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Mr. I. Hirschberg, Director of Electro-Optical Systems, Space and Defense Systems Division, was Program Manager for the Phase II program.

ABSTRACT

This report describes the performance achieved during Phase II of a three-phase program for the development of charge-coupled device (CCD) low-light-level image sensors.

The Phase I program results demonstrated the potential advantages of CCD techniques for low-light-level image sensing. New concepts in CCD design and processing techniques, i.e., the buried channel and sealed-channel silicon gate, were used to produce 1 x 500 element linear arrays and 100 x 100 element area arrays with dynamic range characteristics in excess of 1000/1. These arrays demonstrated the effectiveness of the buried channel; low-light imaging thresholds were limited only by dark-current and amplifier noise effects equivalent to 200 electrons/element; adequate charge-transfer efficiency was achieved over the full range of useful operation.

The Phase II program results demonstrated that very low level CCD signal packets can be transferred and detected at the element readout rates required for a 500 TV line image sensor. It was demonstrated, by both theory and experiment, that sufficiently high charge-transfer efficiency is retained for 10 electron level signals; comparable noise-equivalent signal levels are achieved with a twelve-stage distributed floating-gate amplifier (DFGA) structure. A 190 x 244 element area image sensor, which incorporated the DFGA, demonstrated the detection of a bar pattern image with less than 40 photoelectrons/element in the image highlights.

This report contains detailed information on the design, related process techniques, and performance data, for the linear and area array sensors generated during Phase II. Design and performance data dealing with the 1 x 1000 linear array and a family of area arrays with 100 x 100, 190 x 244 and 380 x 488 elements are also described. The report also contains information on key investigations, namely, a theoretical analysis of the influence of bulk traps on charge-transfer efficiency for small numbers of photoelectrons, the experimental investigation of the transfer of small charge packets, analyses of process techniques for the reduction of dark current non-uniformities, and TV camera system developments.

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SECTION 1

INTRODUCTION

The objective of this program for the Naval Electronics Systems Command is to develop charge-coupled device (CCD), low-light-level,image sensors. This report describes Fairchild Camera and Instrument's accomplishments in Phase II of this program, namely, the demonstration of the scientific validity of the Fairchild design and techniques approach toward achieving this objective.

Phase I was concluded with the development of a 500-photoelement linear image sensor and a 100 x 100 photoelement area sensor which exhibited a dynamic range in excess of 1000:1. The linear sensor was sensitive to as few as 200 photoelectrons at room temperature; greater than 0.9999 charge-transfer efficiency was obtained at 1 MHz. These low-noise high-transfer efficiency properties were achieved mainly by the incorporation of a buried channel in the silicon substrate, which prevents photoelectrons from being trapped by surface states at the silicon/silicon dioxide interface. The limiting factors for obtaining a lower noise level and an accompanying increase in sensitivity were reset noise in the gated-charge-integrator on-chip amplifier and shot noise in the dark current at room temperature. To progress to an order of magnitude higher in sensitivity, Fairchild proposed an innovation, based on the development of a floating-gate amplifier, the distributed floating-gate amplifier (DFGA).

From the beginning of Phase II, a number of questions were raised that concerned the validity of Fairchild's approach for achieving significantly improved low-light-level CCD image sensors:

1) Would there be sufficient charge-transfer efficiency to detect photosignals of the order of 10 electrons?

2) Would there be adequate charge transfer efficiency at standard TV video bit rates?

3) Would the DFGA fulfill its promise for responsivity at the low-light-level of tens of photoelectrons at TV bit rates?

4) Would the DFGA be compatible in operation with a large area image sensor of the interline transfer design?

Fairchild's achievement in Phase II was the demonstration by experimental results that the answer to each of these key questions was positive:

1) It was demonstrated by both theory and experiment that high-transfer efficiency is retained for 10 electron photosignals.

2) A 190 x 244 photoelement produced a high quality image at a 10-MHz output bit frequency.

3) The first distributed floating-gate amplifier was produced. A noise equivalent signal of 20 electrons was measured at a TV-comparable sampling time of 50 nanoseconds.

4) A 40-electron bar-pattern image was detected by a 190 x 244 interline transfer image sensor by its on-chip DFGA.

In addition to these major achievements, there were a number of device development and technological accomplishments which are described in Section 2 of this report.

SECTION 2

PROGRAM SUMMARY

The Phase II program began with the design, fabrication and functional testing of two devices that were initiated during Phase I. These devices were a 1000-photoelement linear image sensor, the CCLID-1000B, and a redesigned 100 x 100 photoelement sensor, the CCAID-100BD.

The CCLID-1000B fulfilled its design expectations. Greater than 30% modulation was obtained at the Nyquist limit. By virtue of a reduction in CCD cell length from the 1.2 mils of the CCLID-500A to 0.77 mil, the transfer efficiency was sufficiently high to obtain a 10-MHz output bit rate in comparison to a maximum bit rate of 2 MHz for the CCLID-500A. Improved light shielding was achieved by the use of a second metal layer. A compensation gated-charge integrator amplifier was incorporated on the chip. Finally, a gate protection diode was employed.

The CCAID-100BD redesign of the CCAID-100A resulted in a number of improvements. Simplified clocking was obtained by use of a comb-shaped channel stop rather than a serpentine configuration. More reliable charge transfer from the vertical CCD register in the photoarray to the horizontal CCD output register was obtained by redesigning the channel stop at the interface between the two registers. Reduced leakage between vertical transfer gates resulted from the use of wider polysilicon gaps. Sharper images were achieved by employing an n^+ diffusion in the gated-charge integrator reset circuit, which increased the speed of amplifier response. These improvements were incorporated in the design of the larger CCAID-244A array.

The CCAID-244A is a 244-row, 190-column photoarray. Like the CCAID-100BD, it is an interline-transfer organized device with the same type of doped-undoped polysilicon gate electrode structure. Different from earlier devices, two floating-gate amplifiers (FGA's) and a distributed floating-gate amplifier (DFGA) are incorporated in addition to the conventional dual-gate differential gated-charge-integrator amplifier (DDA). High quality images were obtained at moderate illumination levels from both the FGA and the DDA at a 10-MHz output bit rate. Images as low as 40 photoelectrons/pixel were detected with the DFGA operated at a sampling rate equivalent to a 7-MHz video pixel rate.

At a later stage of the program, the CCAID-244B was designed with the more advanced self-aligned barrier, oxide-gap, 2-phase CCD register electrode structure instead of the doped-undoped polysilicon structure.

The final major device-development accomplishment of the program was the design of the CCAID-488A, a 488-row, 380-column area image sensor with DDA, FGA and DFGA on-chip amplifiers. Like the CCAID-244B, the interline CCD registers employed the self-aligned barrier, oxide-gap, 2-phase electrode structure. It was designed for less critical mask alignment in wafer fabrication than for the CCAID-244A because of its larger size. A single level of polysilicon was employed over a significant portion of the photoelements for higher light transmission. Although the chip measures 427 mils x 472 mils, photomasks were produced without photocomposition by use of a 5X reduction lens. At the end of Phase II, the first wafer-fabrication runs were completed.

Throughout the program, a series of technological studies were performed with the objective of extending basic CCD technology to predict the performance of low-light-level image sensors and to establish design requirements for optimal performance. These studies included a theoretical treatment of the influence of bulk traps on charge-transfer efficiency for small numbers of photoelectrons and the validation of these predictions by light spot measurements on oxide-gap, 2-phase CCD registers. It was found that with a dark charge of less than 4 electrons/pixel, 15 ± 3 photoelectrons were carried through 238 transfers with a loss of 1 ± 5 photoelectrons.

As part of these investigations, low-temperature imaging tests were performed with the CCAID-100BD. Spectral response measurements were made and compared to theoretical models. Finally, non-imaging CCD applications were investigated. This study resulted in the design of an electronic input register that was incorporated into the CCAID-244A, 244B and 488A.

SECTION 3

CONTENTS OF REPORT

The extensive material in this report has been organized in four major sections, Device Development, CCD Technology Studies, Technology Parameter Studies, and Test Instrumentation and TV Camera Systems.

Section 4, Device Development, treats the five image sensors involved in the Phase II program in approximate chronological order of development. Information for each device is presented in two major subsections. The first is a device description which includes functional elements, structural details, design features and clocking; the second subsection deals with device performance, including the results of image-sensing characterization experiments performed with these devices.

Section 4.1, for example, is devoted to the CCLID-1000B. The device-description subsection 4.1.1 first presents a schematic diagram of the device, a photograph of the chip, and a general description of device operation. Second, device structures and dimensions are given. Third, there is a description of design features unique to the device such as the use of a second metal layer for improved light shielding, the on-chip compensation amplifier, and the gate protection. Fourth, the timing diagram for clocking is given. The device performance subsection, 4.1.2, presents experimental evidence for high charge-transfer efficiency at a 10-MHz output bit rate. This is followed by an evaluation of square-wave response, transfer characteristics, uniformity of photoresponse, and dynamic range. Finally, the results of imaging tests with this device in a slow-scan camera are described.

Section 4.2 presents the CCAID-100BD. Following the sequence of the previous section, an organized description of this device is given in subsection 4.2.1. Subsection 4.2.2 contains an extensive discussion of device performance, beginning with image sensing test results at room temperature and at reduced temperatures. This is followed by a description of charge-transfer efficiency tests from near-saturation illumination down to the level of noise equivalent signal, which is approximately three orders of magnitude lower in illumination level. The final subsection describes dark-current measurements performed with the device.

Section 4.3 contains a complete description of the CCAID-244A. Of special significance are subsection 4.3.2.1, which presents imaging results at high output bit rates, and subsection 4.3.2.2 which describes DFGA image responsivity experiments at less than 40 photoelectrons/pixel.

Sections 4.4 and 4.5 are devoted to a description of the design of the two related devices, the CCAID-488A and the CCAID-244B.

The most extensively treated subject in Section 5, CCD Technology Studies, is the investigation of charge-transfer efficiency at low signal levels, Section 5.1. The investigation is first introduced by a discussion of the objective of this investigation. This is followed by an estimate of the influence of bulk traps on charge-transfer efficiency from calculations based on a theoretical model. The final subsection describes experimental measurements that verify these estimates.

Section 5.2 is essentially a reference to the DFGA Program. Although this effort was not funded by this NESC program, it provided a key element of support, the development of the DFGA. In its own right, the result of this effort was a verification of the predicted high responsivity of this amplifier, 10^2 μV/electron, and the noise equivalent signal of 20 electrons at a sampling time of 50 nanoseconds, which is equivalent to standard TV bit rates. The Final Report of the DFGA Program is included as an appendix to this report.

Section 5.3 describes, briefly, a set of spectral response measurements, which are compared to calculations from theoretical models.

Section 6, Technology Parameter Studies, deals with a long-term investigation of dark-current nonuniformities caused by dark-current spikes. The investigation includes analytical techniques for the identification of the source of these spikes and process techniques for the elimination of these sources.

Section 7, Test Instrumentation and TV Camera Systems, contains information on systems development activities in support of the device development program. Section 7.1, for example, describes test set modifications implemented for CCLID-1000B and CCAID-244/488 image sensor evaluation. Section 7.2 is concerned with CCAID TV camera development, with emphasis on design concepts uniquely applicable to systems using Fairchild interline-transfer area arrays. Of particular significance is subsection 7.2.4 which includes preliminary study results and performance projections for a CCAID-488 low-light-level TV camera. The final section 7.3 briefly describes features of the CCAID-100BD Television Camera delivered during Phase II.

SECTION 4

DEVICE DEVELOPMENT

4.1 CHARGE-COUPLED LINEAR IMAGING DEVICE, 1000 x 1, MODEL B (CCLID-1000B)

One of the initial objectives of the Phase II program was to complete the development of an advanced linear image sensor which had begun in Phase I. The more significant objective characteristics of this sensor were to increase the number of photoelements by a factor of two and to increase the maximum output bit rate by at least the same factor without a sacrifice of response at high spatial frequency. This advanced charge-coupled linear imaging device was the CCLID-1000B.

4.1.1 Device Description

The CCLID-1000B is a charge-coupled linear image sensor device with 1000 photoelements. Compared to the CCLID-500A, which was developed under the first phase of this contract, the CCLID-1000B has smaller cell spacing and several design improvements.

4.1.1.1 Functional Elements

The chip organization of the CCLID-1000B is essentially the same as the CCLID-500A. It employs two opaque CCD registers in a parallel-transfer readout configuration. The 1000 photoelements are formed by one polysilicon photogate electrode and a serpentine channel-stop pattern. The two 502-bit CCD shift registers are located on the two sides of the photogate. Each register is separated from the photogate by a transfer gate that controls charge transfer from the photogate to the shift registers. At the end of the two 502-bit shift registers is a 2-bit shift register that accepts charge packets from the two long shift registers and provides a sequential output signal to a gated-charge integrator. A block diagram, a pin layout diagram and a photomicrograph of the device are shown in Figures 4-1, 4-2, and 4-3, respectively.

4.1.1.2 Structural Details

The structural details of CCLID-1000B are essentially the same as the CCLID-500A, but with reduced dimensions. The photosensors have a 19.5 μm element pitch; the shift registers have 8-μm gate lengths and 5-μm gaps between gates. Since the shift registers are three-phase CCD, each bit is 39 μm long. The overall chip size is 795 mils x 60 mils.

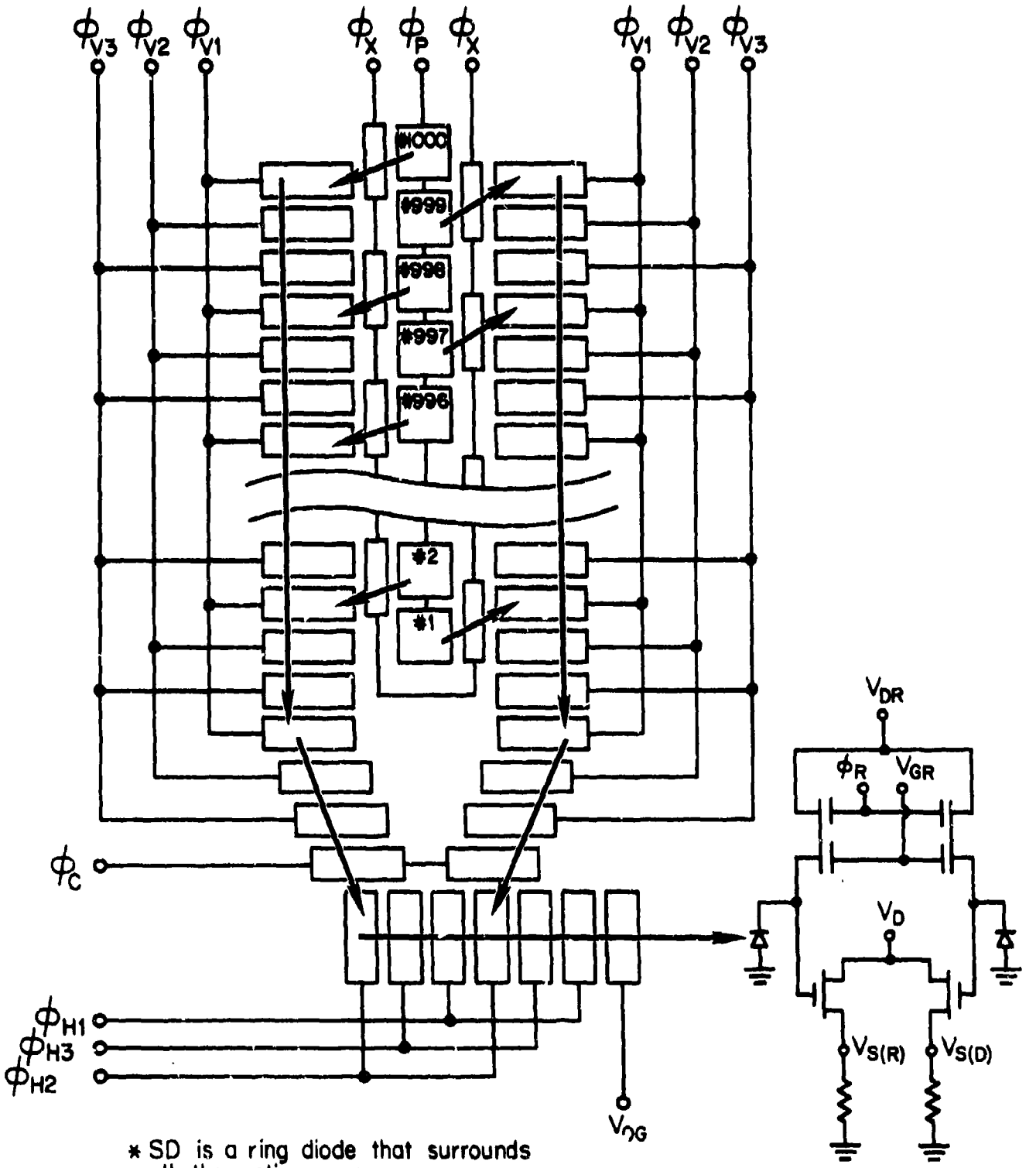

FIGURE 4-1. BLOCK DIAGRAM OF CCLID-1000B

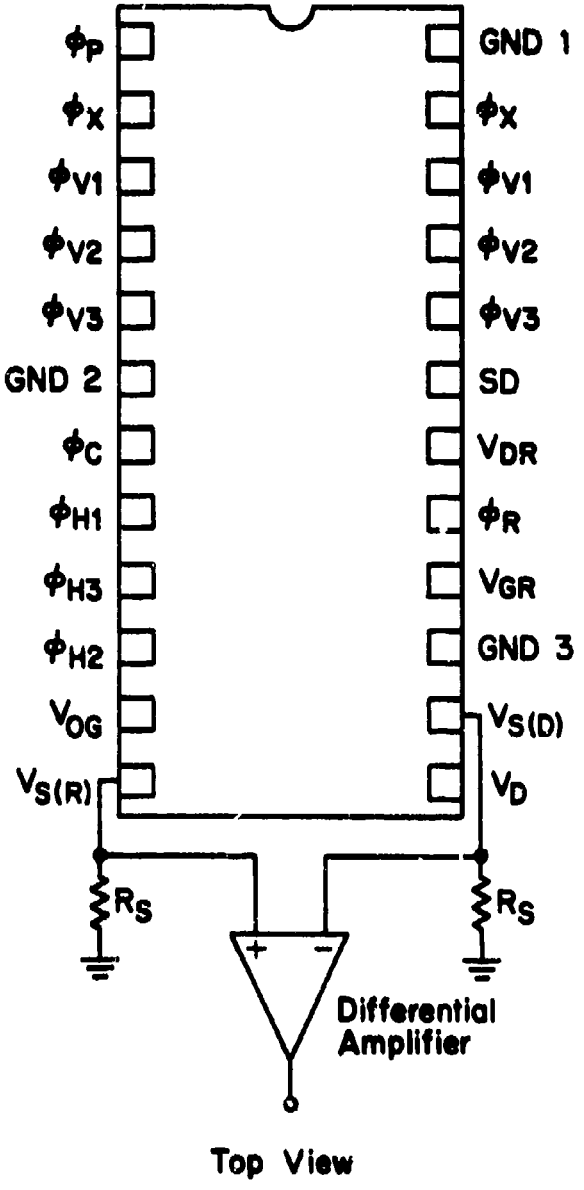

FIGURE 4-2. PIN LAYOUT OF CCLID-1000B

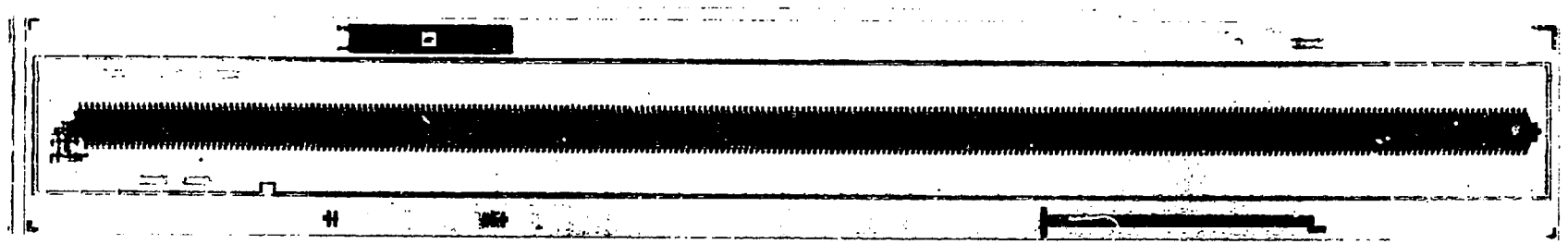

FIGURE 4-3. PHOTOMICROGRAPH OF CCLID-1000B

4.1.1.3 Design Features

The CCLID-1000B possesses several design improvements over the CCLID-500A:

- A second layer of metalization and a ring diode are employed to reduce peripheral photoresponse.
- A compensated output is provided to generate the same coherent noise as that contained in the uncompensated output signal.
- Gate protection diodes on small gates are employed.
- A dual gate reset transistor is used to reduce reset noise.

4.1.1.3.1 Second Layer of Metalization and Ring Diode

If light is absorbed in the silicon-substrate other than under the photogate, photoelectrons are generated, which can diffuse into either the analog CCD shift registers or into the photoelements, producing an erroneous output signal. The CCLID-1000B utilizes a second layer of opaque metalization and a ring diode to minimize this peripheral response. The ring diode surrounds the active area and the second metalization covers all the area inside the ring diode except for the photogate. Light that enters silicon outside the metalization creates photoelectrons. However, these electrons are collected at the ring diode, which is reversed biased. The optical window and the cover of the package are also designed to shield light from the periphery of the device. A combination of the proper cover design and metalization has resulted in a negligible peripheral response.

4.1.1.3.2 Compensation Output

The output signal of CCLID-1000B possesses coherent reset noise caused by capacitive coupling of the reset clock (ϕ_R) to the output node. This coherent noise can easily be cancelled using a differential amplifier if a signal similar to the noise is available. The compensation output provides this signal. It is produced on the chip by a dummy output stage which does not receive the signal charge. Since the signal is generated on the same chip, a good match is obtained between the noise in the real output and the dummy output.

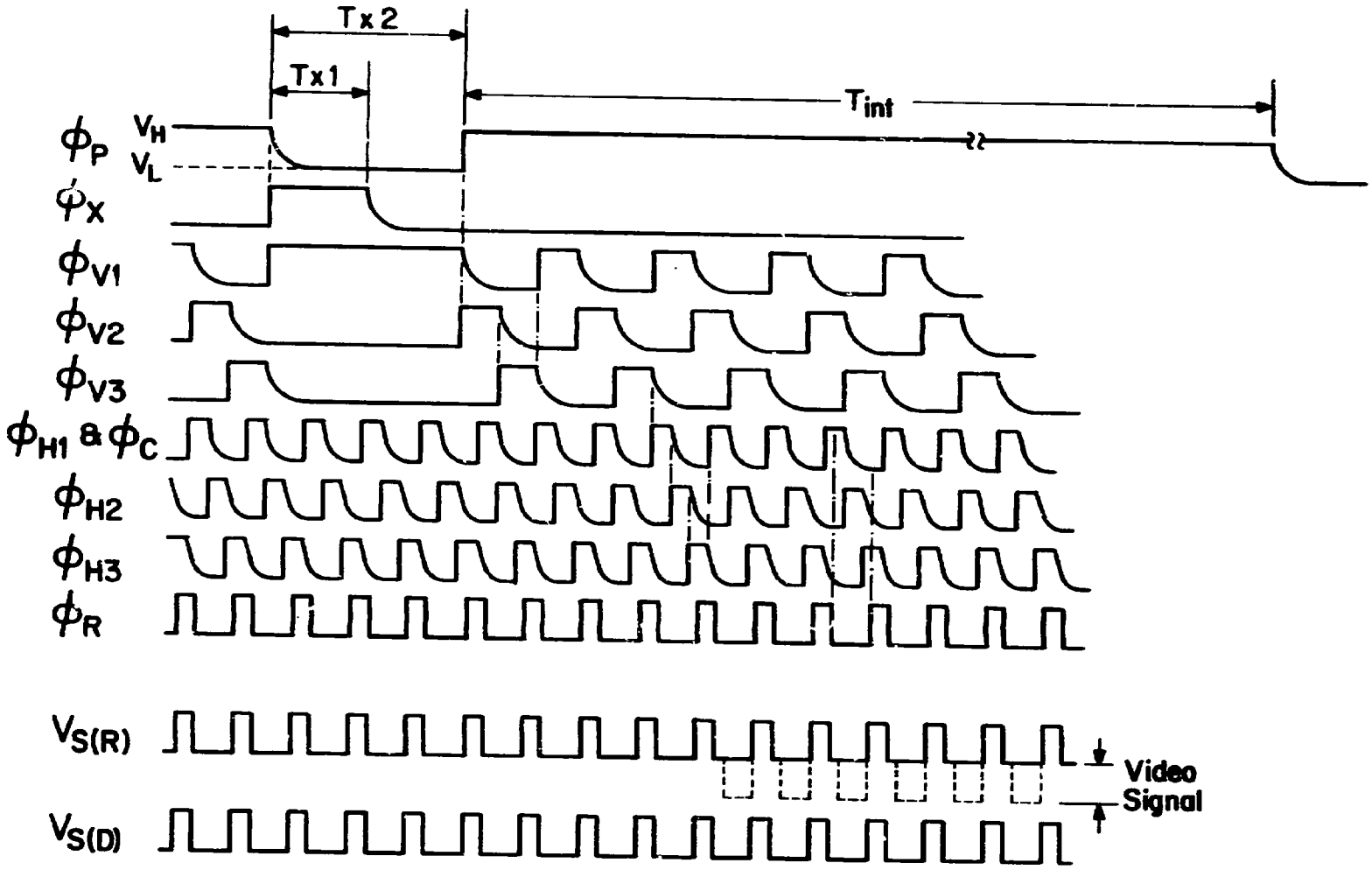

FIGURE 4-4. CLOCKING SEQUENCE FOR CCLID-1000B

4.1.1.3.3 Gate Protection Diodes

The small gates of CCLID-1000B are protected by back-to-back diodes connected in parallel to the gates. These protection diodes have breakdown voltages higher than the clock voltages and lower than the oxide breakdown voltage. Therefore, should a static charge be introduced, it breaks down the diodes before it can damage the oxide. The inclusion of the protection diodes made the CCLID-1000B much less sensitive to handling than the CCLID-500A.

4.1.1.3.4 Dual Gate Reset Transistor

In addition to the compensation output, the reset noise itself has been reduced by employing a reset transistor with two separate gates. In operation, the gate closer to the output node is dc biased while the other gates are pulsed. The dc-biased gate shields the reset pulse from coupling to the output node. Although the reset noise is reduced, the dual gate reset transistor increases the capacitance of the output node and thereby decreases the output voltage swing.

4.1.1.4 Clocking

The clocking requirement is similar to that of the CCLID-500A. A timing diagram of the drive pulses is shown in Figure 4-4.

4.1.2 Device Performance

4.1.2.1 Transfer Efficiency

The charge-transfer efficiency of the CCLID-1000B has been found to be approximately the same as the CCLID-500A. However, because of smaller geometries, higher frequency operation can be achieved with the CCLID-1000B. Figure 4-5 shows scope traces of the output signal at 10 MHz when a light spot illuminates the 3rd, 4th, 997th and 998th element. By comparing the signal magnitudes of the 3rd and 997th output, a transfer efficiency of approximately 99.97% per transfer is found.

4.1.2.2 Square-Wave Response, Transfer Characteristic, Unformity and Dynamic Range

The following paragraphs describe the test instrumentation, test conditions and test results for an output clock frequency of 1.2 MHz (or an integration time of 870 μsec).

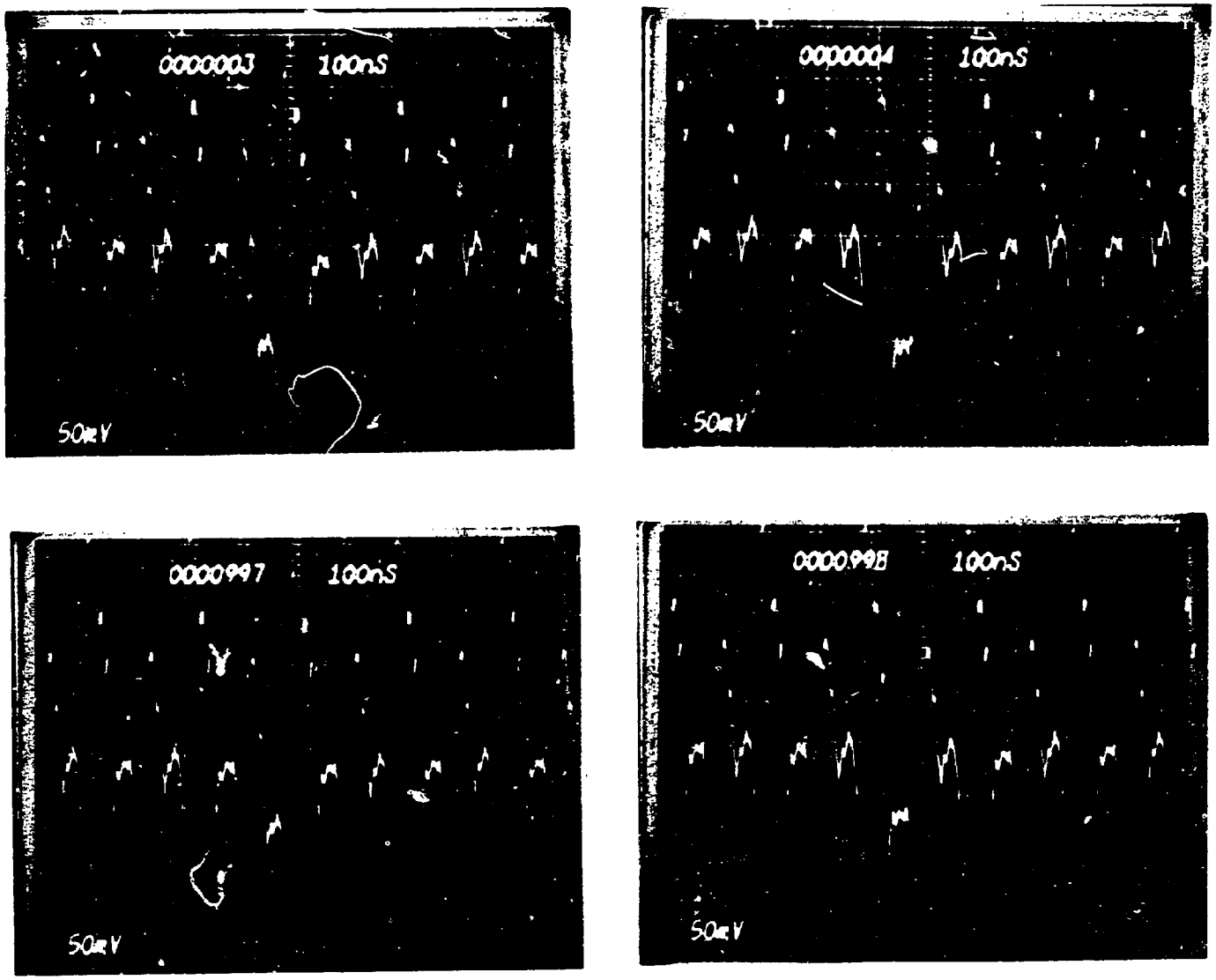

FIGURE 4-5. 10-MHz OPERATION OF THE CCLID-1000B

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4.1.2.2.1 Test Instrumentation

The test instrumentation used is shown in Figure 4-6. As shown, a resolution target is imaged on the array. The array's video output is displayed on an oscilloscope and is simultaneously sampled by a sample-and-hold amplifier. The output of the sample-and-hold (S/H) amplifier is displayed on a display monitor.

The resolution target is a standard high contrast Westinghouse target, which consists of a black-white reference and ten resolution groups where each group consists of four cycles. The target is imaged on the array with a Bausch and Lomb 3" Super Baltar lens. The magnification was chosen so that the highest resolution group at the array under test is 25 line pairs per mm. The target is illuminated by a 1000-watt tungsten halogen lamp, regulated to match closely a 2854°K black body radiator in the silicon band. Table 4-1 lists the target resolution groups at the image plane.

4.1.2.2.2 Square-Wave Response

For this test, a square-wave target was imaged on the CCLID array. The target consisted of 10 resolution groups, 3.5 cycles each, plus a one-cycle black-white reference. The target was imaged on the array so that the highest resolution of the array surface was 25 line pairs/mm; each resolution group was 2.5 line pairs/mm coarser than the previous one. The lowest spatial frequency imaged on the array was 2.5 line pairs/mm. The black-white reference was at 0.7 line pairs/mm. The nominal spatial frequency of the CCLID-1000B array elements is 25.6 line pairs/mm, which corresponds to its 0.77 mil pitch.

The array output was amplified by an external amplifier with a gain of 20 and displayed on an oscilloscope. The amplifier output was sampled by a sample-and-hold amplifier, and the output of the S/H was displayed on a second trace of the oscilloscope. Figure 4-7 is a photograph of both traces showing the array's response to spatial frequencies between 12.5 and 25 line pairs/mm.

Figure 4-8 shows the square-wave response vs. spatial frequency for the array. At each spatial frequency, the voltage difference between the white and black bars is measured. This measurement is made when the bars are in phase with the array elements, and also at other random phasing relationships. Both mean and peak modulations are plotted as a percentage of the modulation of the black-white reference target.

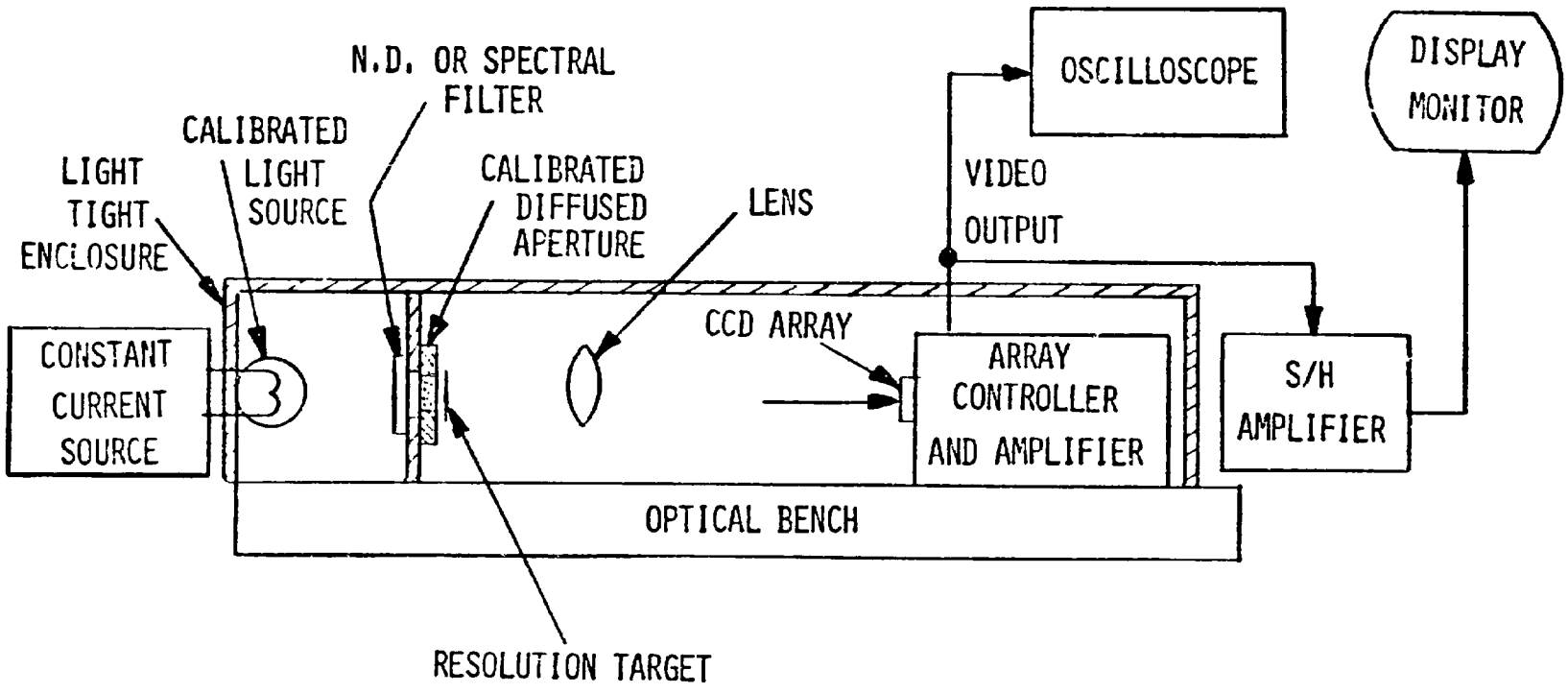
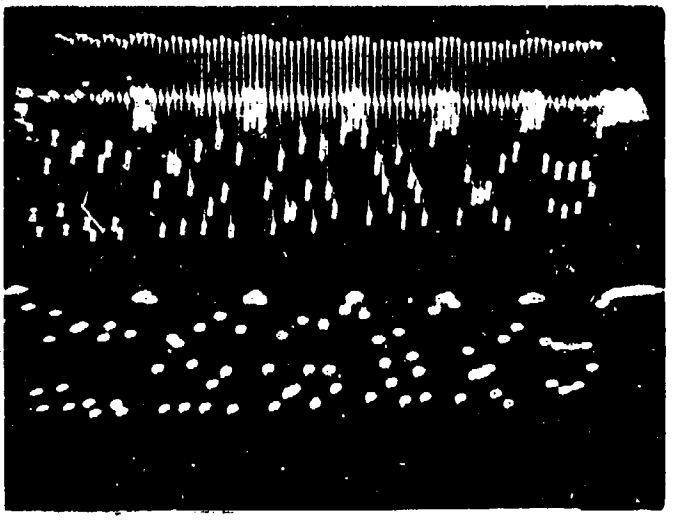


FIGURE 4-6. CCLID-1000B TEST INSTRUMENTATION

TABLE 4-1

RESOLUTION TARGET GROUPS
(AT THE CCLID-1000B)

GROUP	NO. OF CYCLES	MEASURED RESOLUTION LP/MM	NOMINAL RESOLUTION LP/MM
Black-white Reference	1	.695	.7
1	4	2.507	2.5
2	4	4.825	5.0
3	4	7.325	7.5
4	4	9.583	10.0
5	4	12.545	12.5
6	4	14.999	15.0
7	4	16.324	17.5
8	4	20.059	20.0
9	4	22.258	22.5
10	4	25.000	25.0



AMPLIFIER

SAMPLE
& HOLD

12.5 15 17.5 20 22.5 25 ►L.P/MM

ARRAY OUTPUT AT 1.2MHz
3" SUPER BALTAR AT F/8 (1/2 SAT)
AMPLIFIER GAIN = 20
Y=.5V/CM

FIGURE 4-7. SQUARE WAVE RESPONSE OF CCLID-1000B

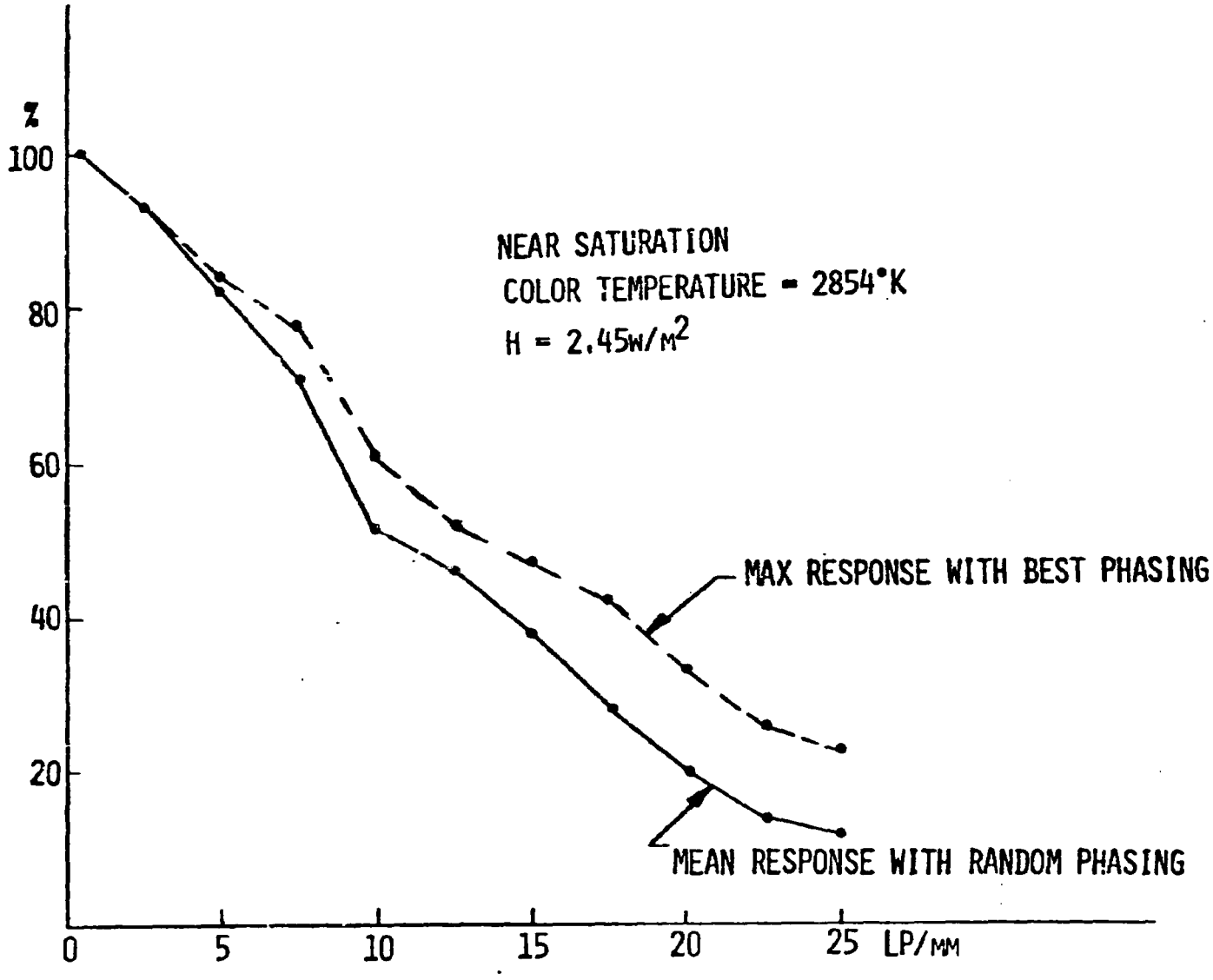


FIGURE 4-8. SQUARE WAVE RESPONSE, 1.2 MHz

4.1.2.2.3 Transfer Characteristics

The irradiance falling on the array was reduced in steps from saturation. The array's average signal output at each irradiance level was measured.

Figure 4-9 is a plot of the transfer characteristics of the array. The abscissa shows the energy falling on the array in $\mu W/cm^2$. The ordinate shows the signal amplitude at the output of an external amplifier with a gain of 10.

4.1.2.2.4 Uniformity

The array was evenly illuminated with diffused light, without a lens, to measure the uniformity of the array itself rather than that of the complete optical system.

Figure 4-10 is an oscilloscope photograph that shows the array uniformity near saturation. The photograph shows a little more than one line scan. The horizontal scale is 100μs/cm and the vertical scale is 0.5 volt/cm. The non-uniformity shown is $\pm$ 2.5% of the signal level.

Figure 4-11 shows the array's uniformity at dark. The horizontal scale is 100 μs/cm and the vertical scale is 0.1 volt/cm.

Both photographs show the output of the external amplifier with a gain of 10. A sample-and-hold amplifier was not used in this test.

4.1.2.2.5 Dynamic Range

To obtain the dynamic range of the array, the resolution target was imaged on the array; the output of the S/H amplifier was used as a video input to a video monitor. The maximum resolution was observed on the monitor for light levels varying from above saturation until only the lowest resolution could be resolved on the monitor. Figure 4-12 shows the plots of irradiance vs. observed maximum resolution at the beginning, center and end of the array. For this case, saturation was at 245 $\mu w/cm^2$. The lowest discernable signal was at 0.151 $\mu w/cm^2$. The dynamic range of the array is the ratio between these two irradiance levels, namely, 1600:1.

4.1.2.3 Imaging with a Slow-Scan Camera

The CCLID-1000B has been employed in a slow-scan prototype camera that employs a rotating mirror to implement vertical sweep. As the image is generated line-by-line, it is stored in a PIP silicon-target storage tube.

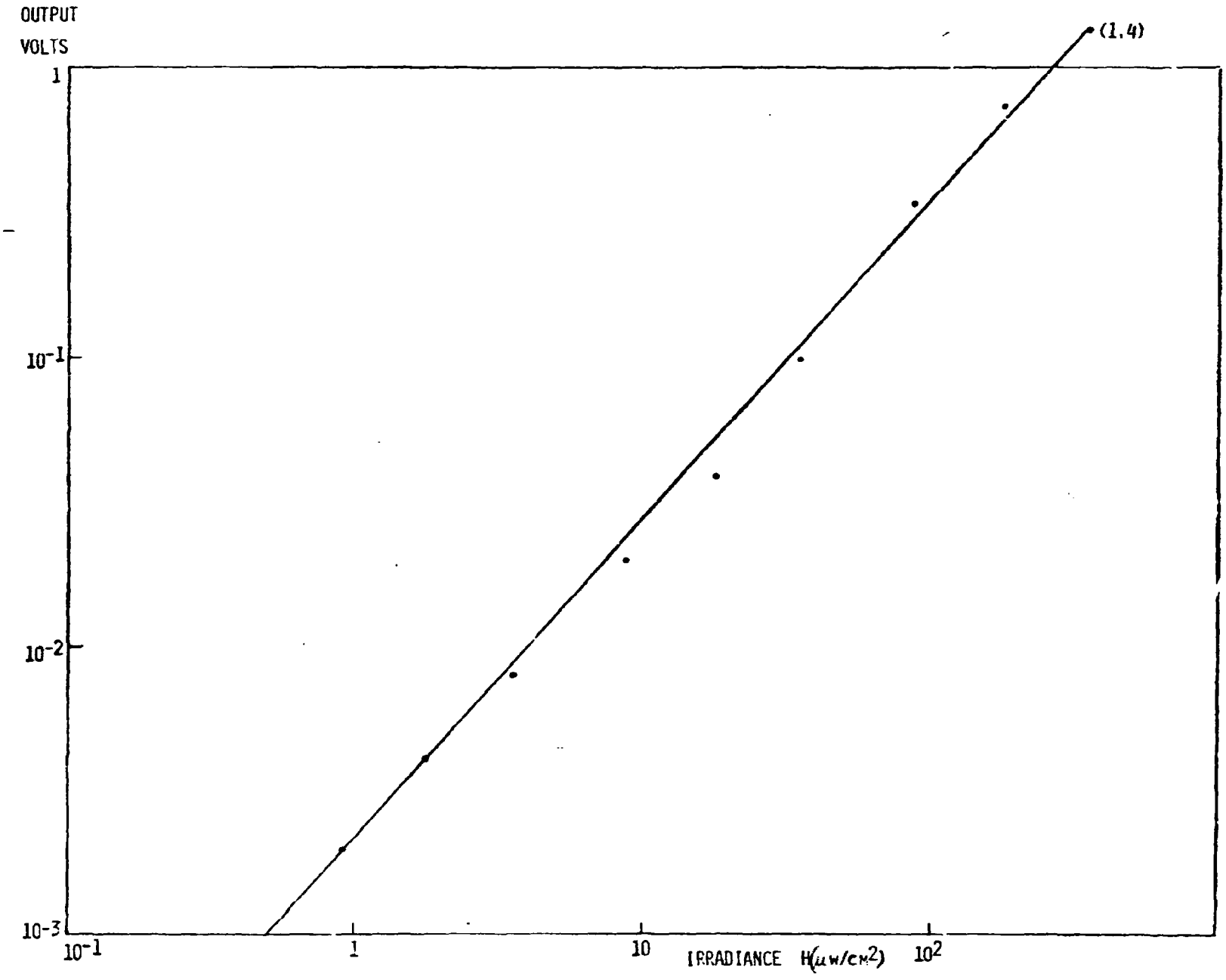


FIGURE 4-9. TRANSFER CHARACTERISTICS FOR CGLID-1000B

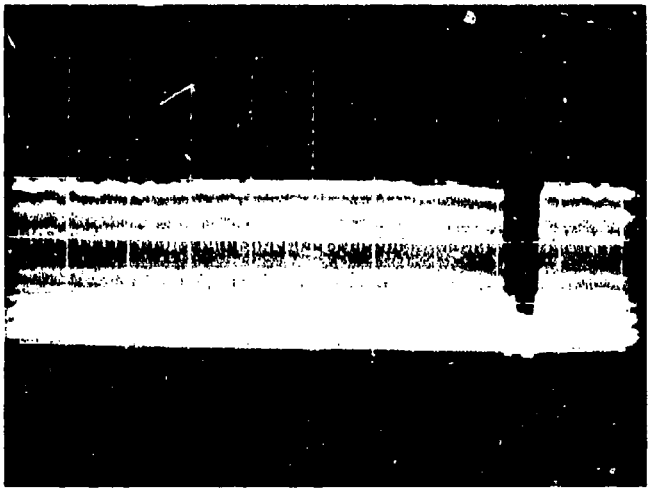


FIGURE 4-10. UNIFORMITY NEAR SATURATION

FIGURE 4-11. UNIFORMITY AT DARK

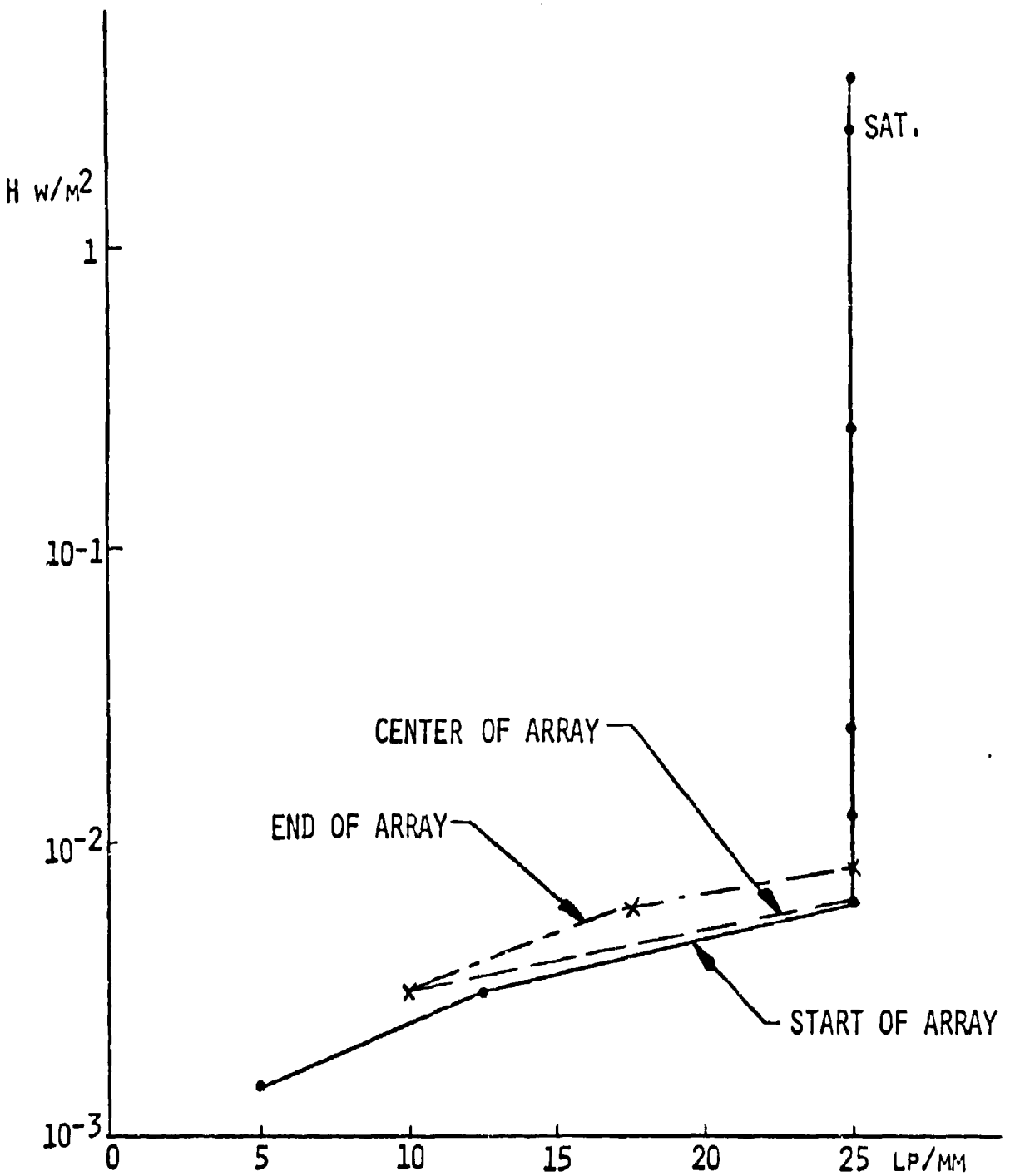


FIGURE 4-12. 100% CONTRAST RESOLUTION, 1.2 MHz

Figures 4-13 and 4-14 are photographs of a stored frame of information displayed on a HP 1310A CRT display under the conditions listed in Table 4-2.

Since the limit of resolution of the HP 1310A is approximately 750 lines, the test-pattern image shown in Figure 4-13 is electronically expanded in Figure 4-14 to demonstrate the limiting resolution of the CCLID-1000B. The nonlinearity of the lines, which may be observed in the diagonal lines of the test pattern, are the result of small perturbations in the angular velocity of the rotating mirror. It should also be mentioned that the video signal has no gamma correction.

4.2 CHARGE-COUPLED AREA IMAGING DEVICE, 100 x 100, MODEL BD (CCAID-100BD)

Like the CCLID-1000B, development of the CCAID-100BD was initiated during Phase I of the program when it became apparent that a number of improvements of the original model could be made. These improvements included simplified clocking, more reliable charge transfer from the interline registers to the output register, reduced leakage betwen doped-undoped polysilicon gate electrodes, and an on-chip preamplifier with a higher speed of response.

The device also served to confirm the high charge-transfer efficiency, low noise, and large dynamic range characteristics of charge-coupled area array designs employing buried-channel principles; characteristics which are essential for the detection of low-light-level images. Both imaging performance at low light level and the measurement of charge-transfer efficiency are described in this section.

4.2.1 Device Description (CCAID-100B and CCAID-100BD)

The CCAID-100B is a 100 x 100 element buried channel, two-phase implanted barrier CCD area imaging device. It is a derivative of the CCAID-100A, Fairchild's first CCD area imaging device. During the course of the program, the 100B was revised slightly; this modified version is referred to as the CCAID-100BD. In the following subsections no distinction is made between the B and BD versions, except where such a discussion touches on significant differences between the two.

4.2.1.1 Functional Elements

The 100B consists of 10,000 photosensitive elements arranged in 100 columns each containing 100 elements. Interdigitated with these columns, are vertical two-phase CCD analog shift registers which move the charge informa-

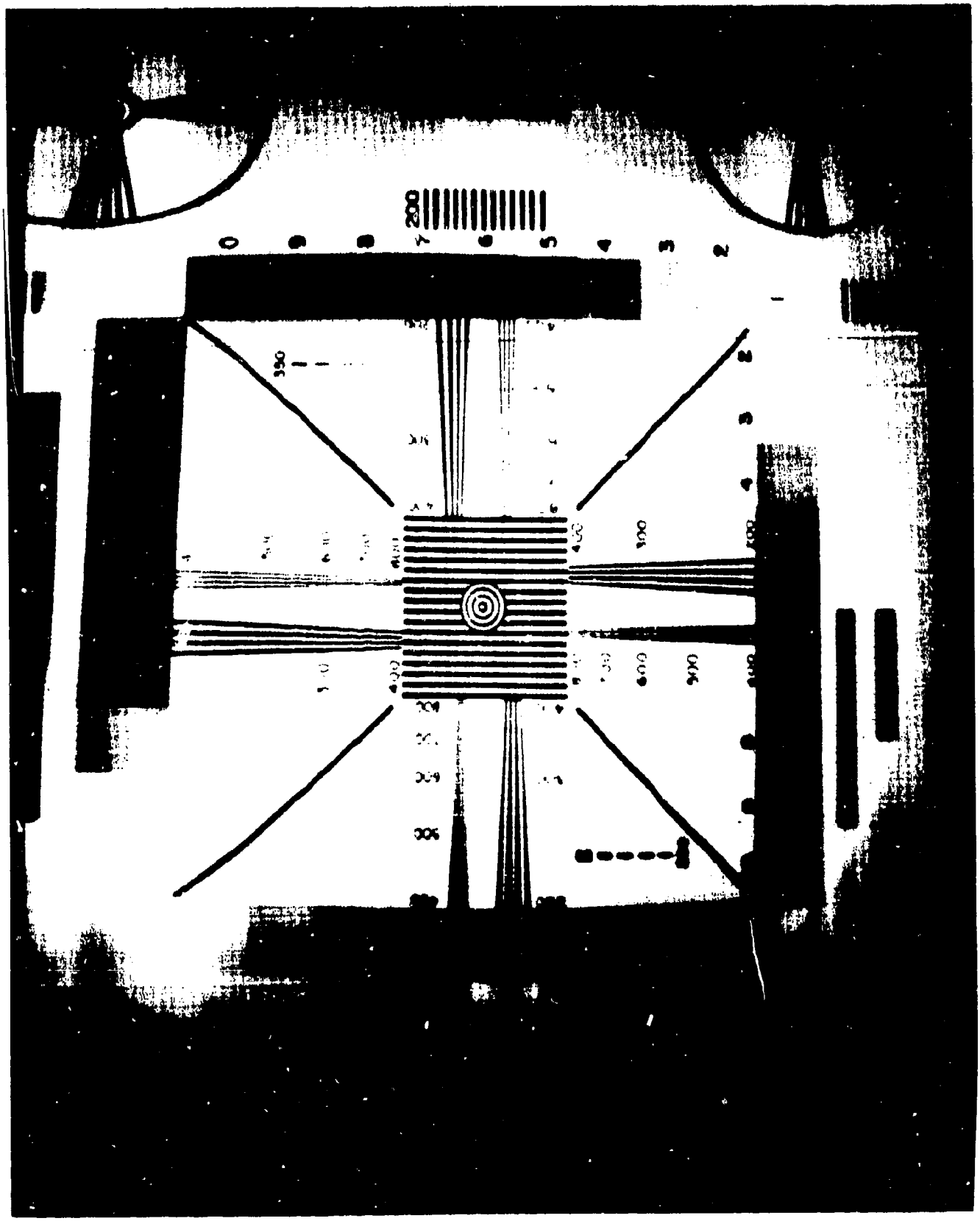


FIGURE 4-13. SLOW-SCAN CAMERA IMAGE

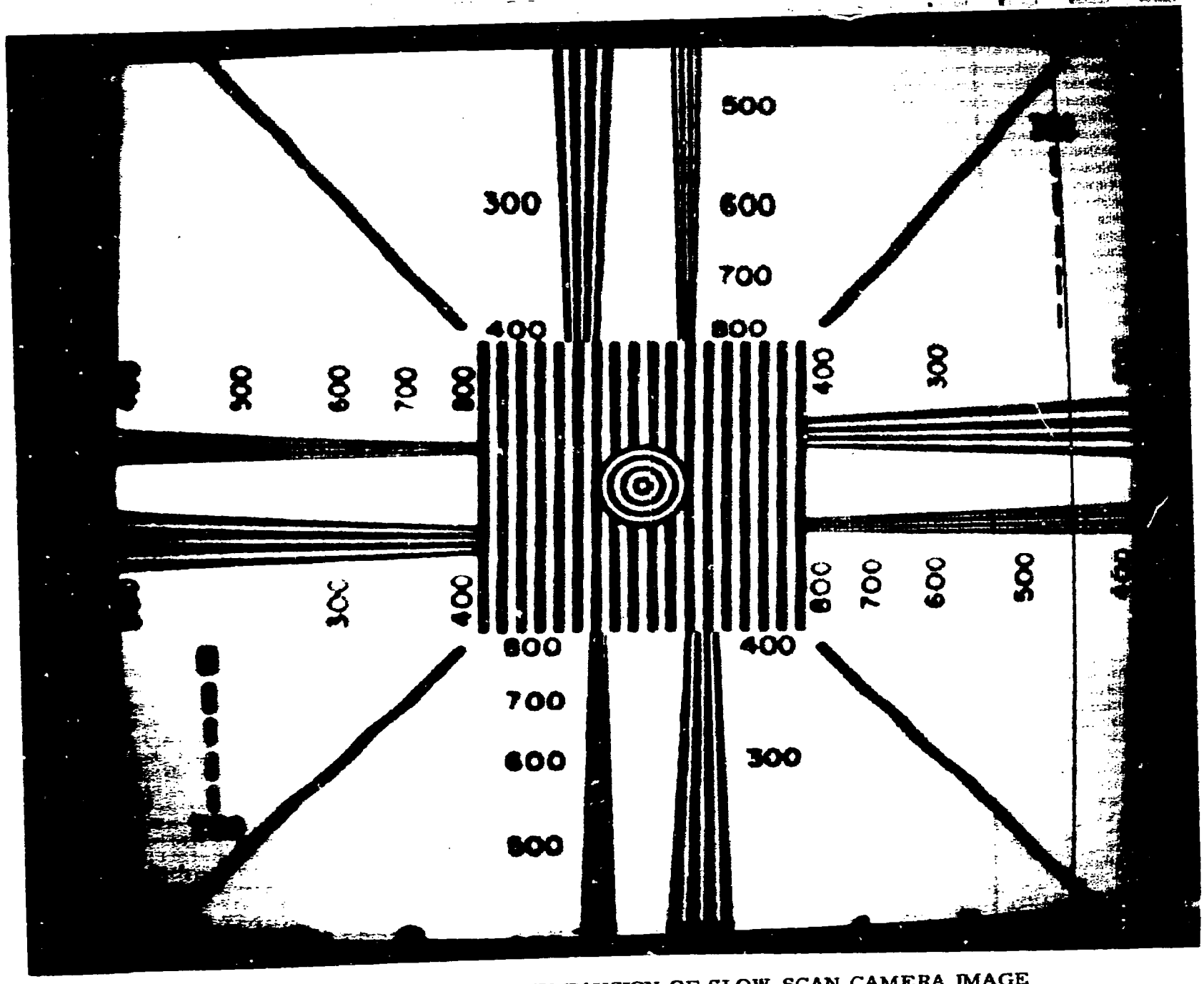


FIGURE 4-14. ELECTRONIC EXPANSION OF SLOW-SCAN CAMERA IMAGE

75P-392

TABLE 4-2

CONDITIONS FOR DISPLAY OF SLOW-SCAN-CAMERA IMAGE OF FIGURES 4-13 AND 4-14

Integration Time:	2 msec/line
Frame Time:	2 sec (photo shows single sweep)
Target Illumination:	≈ 30 ft. candles tungsten
Lens:	f 2.8, 25 mm (Kodak)
Scan Mode:	Mirror (in front of lens) scans from top to bottom (defining top as the normal view of a 4 x 3 TV format)
Resolution:	1000 picture elements across 400 dimension; 750 lines across 300 dimension

tion from the sensing columns to an output register. There are, therefore, 100 vertical shift registers and information is fed to the output register on a parallel shifting basis. Each row of stored charge thus corresponds to one line of video information.

Figure 4-15 is a photograph of the die. The die size is 151 x 191 mils. The center-to-center spacing of the photoelements is 1.6 mils horizontally and 1.2 mils vertically for a 4 x 3 aspect ratio. Along the top of the die is the output register which is coupled to a gated-charge-detector MOS amplifier. Around the periphery are a number of test structures, which include lightly and heavily implanted capacitors, polysilicon test resistors and facsimiles of the output circuitry.

The mechanics of charge shifting can be explained by considering Figure 4-16, which shows the upper right corner of the array including the output circuits. Light incident on photosites A and B, generate charge carriers that are integrated under the frame gate, designated ϕ_F. At the end of one field, charges in A sites are transferrred to the vertical shift registers where they are shifted in parallel into the horizontal register one line at a time. At the end of the next field, charges from B sites are transferred out. This shifting system has several novel features. First, it is a transfer-gateless technique. Since ϕ_{V1}, and ϕ_{V2}, are complementary, clocking can be arranged so that when ϕ_F is lowered, ϕ_{V1} is high during one field transfer and ϕ_{V2} is high during alternate transfers. Signal charges for both fields are integrated for one frame time, similar to conventional TV image sensor operation.

4.2.1.2 Structural Details

Figure 4-17 shows a cross-sectional view of the device through the area array in a direction parallel to a row. It shows two photosites and a portion of the vertical register associated with the site on the left. The top view shows the hook-shaped channel stop region, which defines the boundaries of the photosite completely, except for a small region occupied by a controllable barrier (cross-hatched). Running vertically over the photosite is a polysilicon frame gate. A second polysilicon gate lies over the frame gate stripes; between photosites it is in contact with the thin gate dielectric that covers the vertical register. The two-phase drive for the vertical register is supplied by pulses applied to rows of this second polysilicon layer.

The bottom view of Figure 4-17 illustrates, in cross-section, the multiple layers that make up the device. The doped regions in the p-type substrate consist of the p+ channel stop, the n-type ion-implanted buried channel layer,

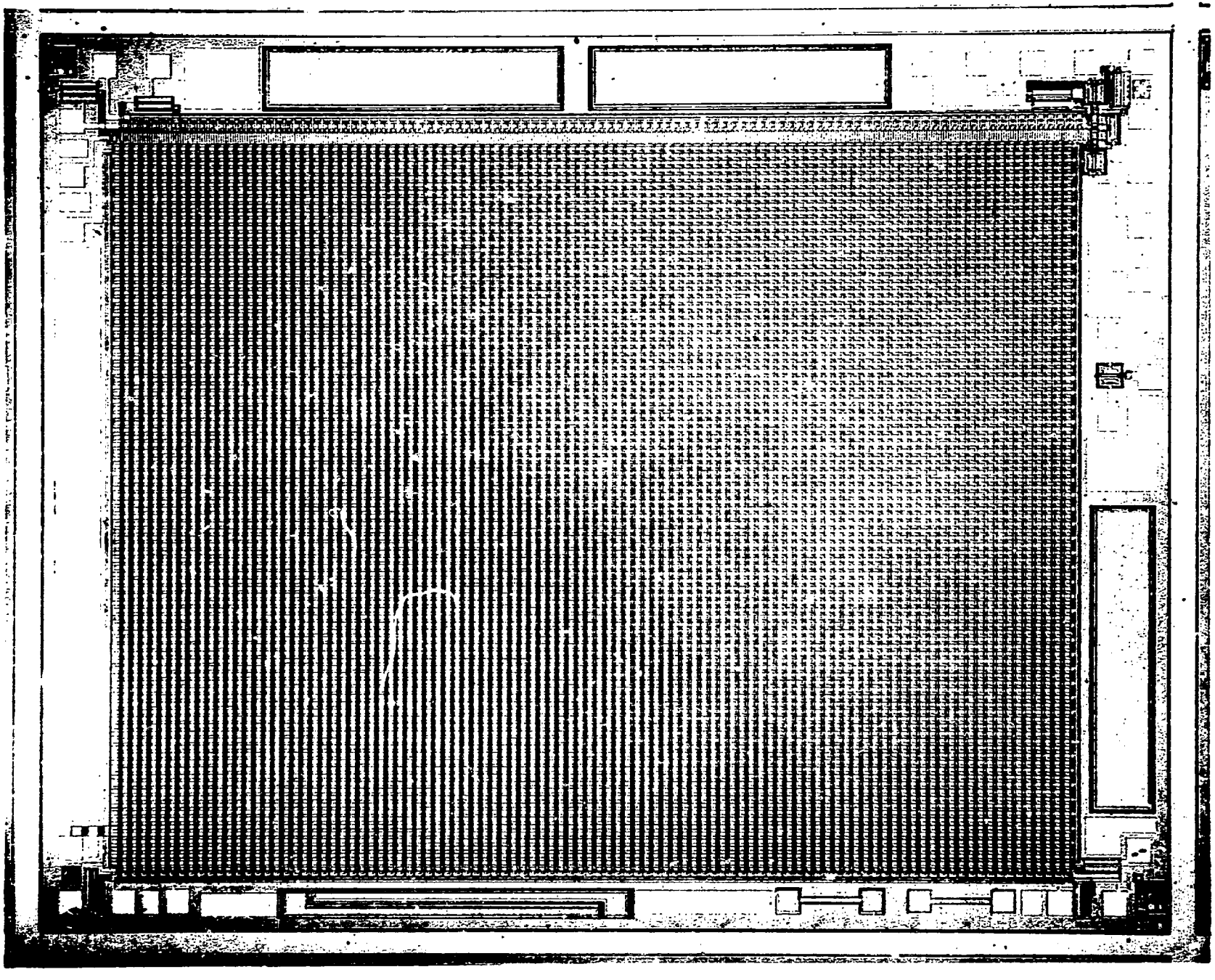


FIGURE 4-15. FAIRCHILD CCAID-100B DIE

75P-383

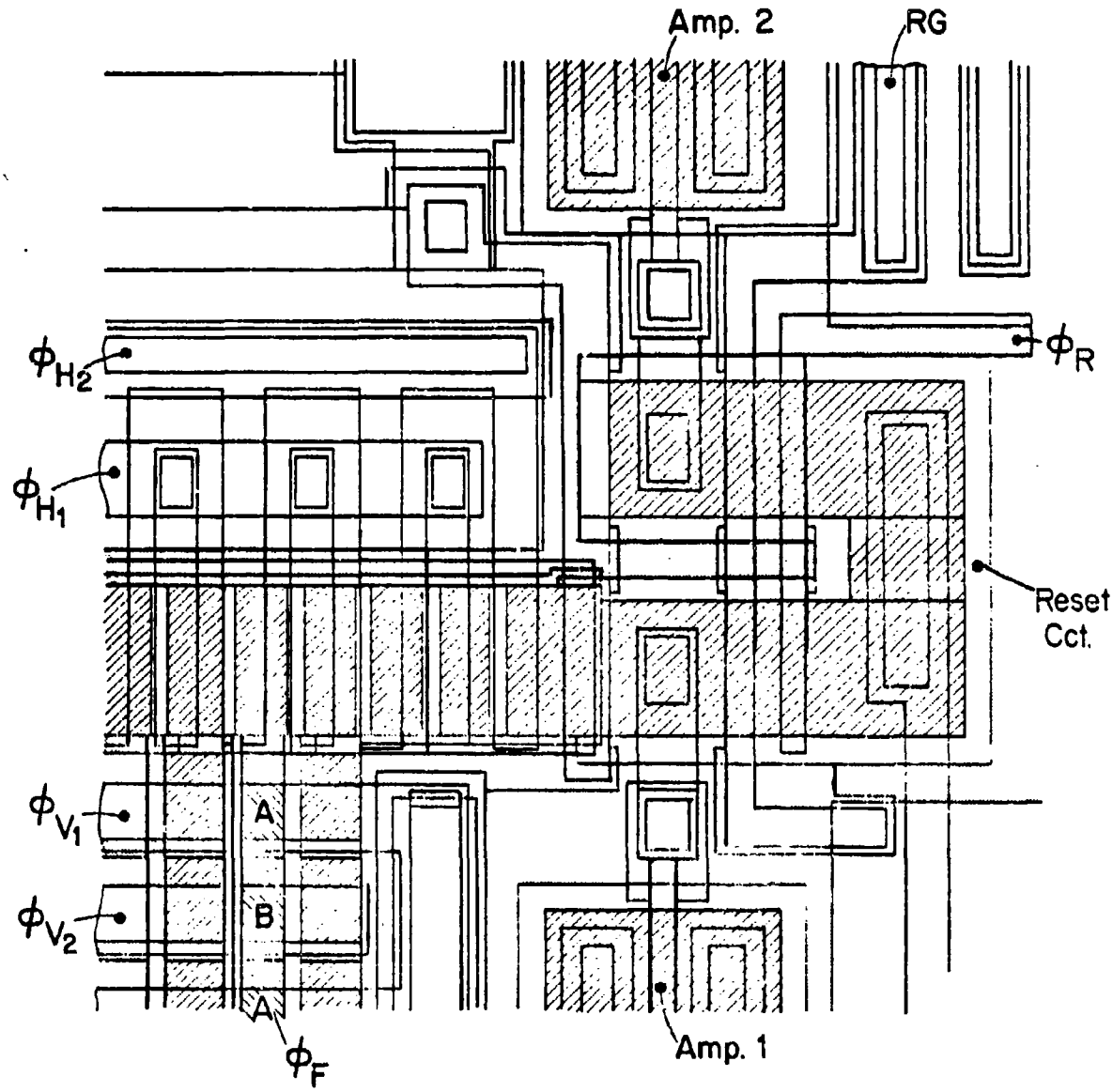


FIGURE 4-16. OUTPUT CIRCUITRY SHOWING DIFFERENTIAL AMPLIFIER AND DUAL GATE RESET CIRCUIT

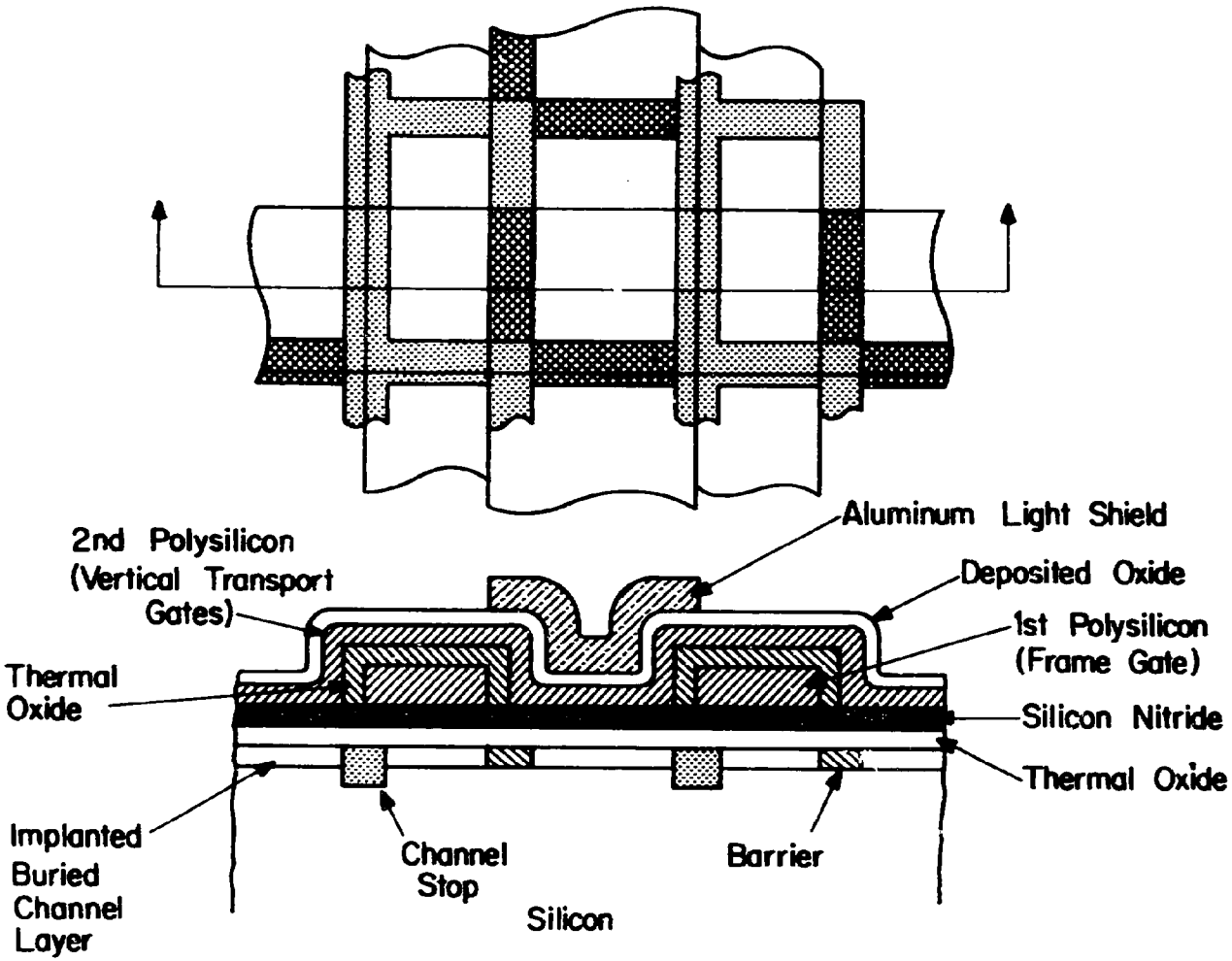


FIGURE 4-17. CROSS-SECTIONAL VIEW OF PART OF THE AREA ARRAY

and the n^- ion-implanted barrier regions. The n^+ regions that define the amplifier sources and drains are not shown. The gate dielectric is a composite layer of silicon dioxide and silicon nitride. Above this are the two polysilicon layers, where the second is insulated from the first by the thermal oxidation of the first layer. Above the second polysilicon layer there is contact vapox that is used as a base for the aluminum conductors that connect electrodes to off-chip circuits. The aluminum also serves as an opaque layer over those parts of the device which must be shielded from light.

Table 4-3 shows the essential features of the process sequence. Though devices fabricated to date were built in a research environment, it is believed that the process is capable of high yield. The smallest cut is 0.2 mil; this is the cut that defines the channel stop. No contact cut is smaller than 0.4 mil. The silicon nitride layer serves not only as a redundant dielectric for pinhole protection, but is also used to preserve the gate oxide thickness during subsequent oxidation.

It is possible to make the process self-aligned by performing the barrier implant after the gate-doping mask has been formed. In this case, the barrier is confined to openings common to both masks. Figure 4-18 illustrates the general nature of the alignment problem where misalignment is shown to result in either an unwanted barrier or unwanted well. Self-aligned processing eliminates the barrier in (b). In (c), however, an unwanted well would still result. By suitable mask design this is avoided and in practice occurs only as the result of gross misalignment.

4.2.1.3 Design Features

Many of the design features of the 100B existed on the 100A, however, the 100B incorporates a number of improvements. A list of these changes relative to the 100A is as follows:

1) A left-right reversal of the image format to correct for the reversal that occurs in the optics.

2) The use of a comb-type channel stop structure instead of the serpentine design used on the 100A. This change simplifies clocking, since column signal information for both fields enters the output register via the same horizontal gates. With the serpentine structure, information in a column for field 1 was inserted into the output register at a point closer to the amplifier than the information for field 2.

TABLE 4-3. CCAID-100 PROCESS SEQUENCE

1. Grow thick oxide.
2. Define channel stop; predep and diffuse boron; regrow C.S. oxide.
3. Define thin oxide regions; grow thin thermox layer; add thin layer of silicon nitride.
4. Implant donors to form buried channel.
5. Deposit first polysilicon layer; dope and etch to form frame gate; oxidize afterwards.
6. Define barrier locations and implant boron to produce barriers.
7. Deposit second polysilicon layer; remove it everywhere except in the active regions; oxidize to provide masking oxide for the next step.
8. Etch oxide to form vertical and horizontal gate pattern; dope with phosphorus to form diffused gates in second polysilicon layer and S-D regions.
9. Add contact vapox; define and etch contacts. Evaporate aluminum; etch to define bonding pads, etc., alloy.
10. Deposit thick vapox, evaporate second layer aluminum and etch to form light shield; etch holes in vapox to expose bonding pads.

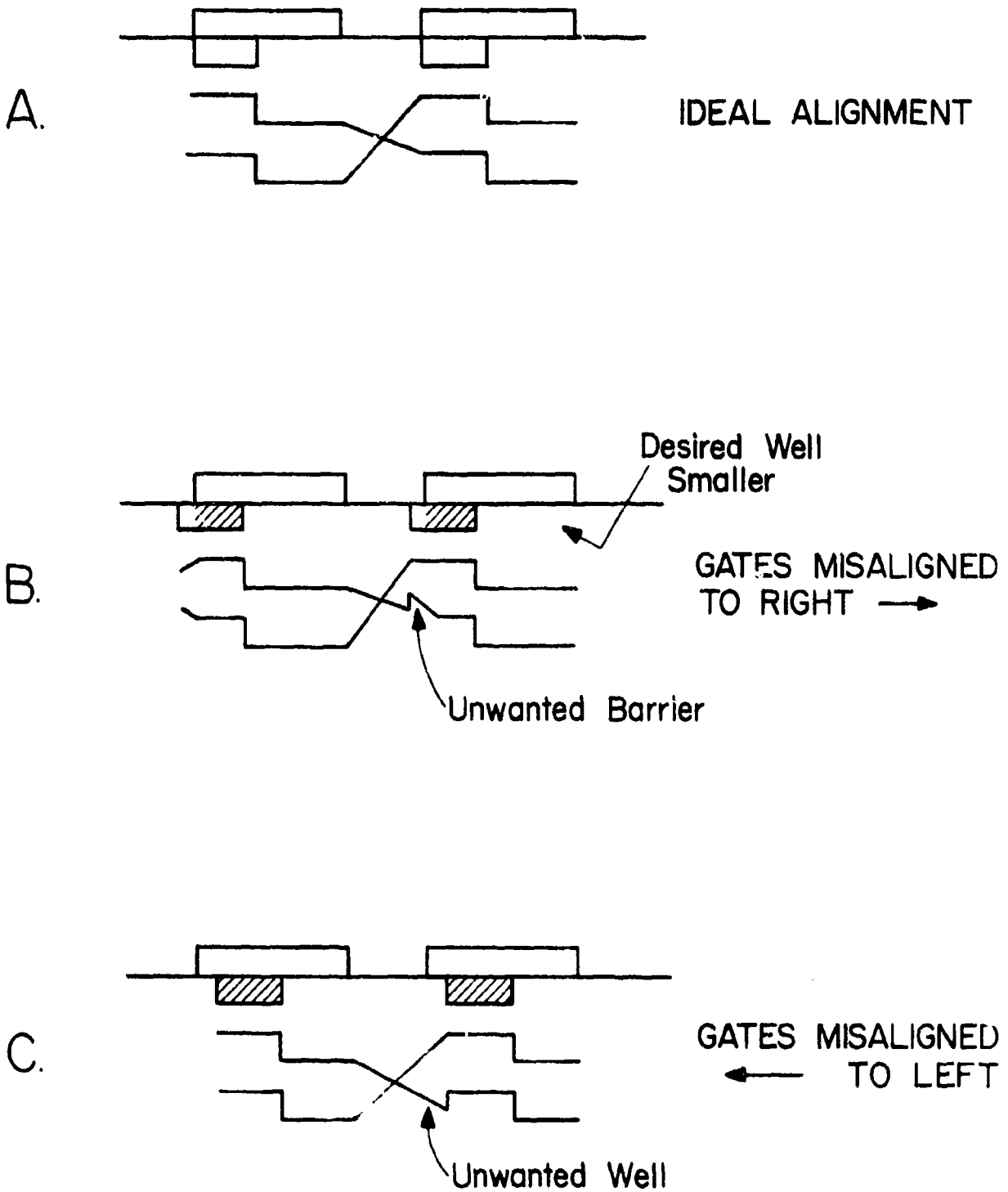


FIGURE 4-18. QUALITATIVE EFFECT OF GATE MISALIGNMENT ON POTENTIAL PROFILE

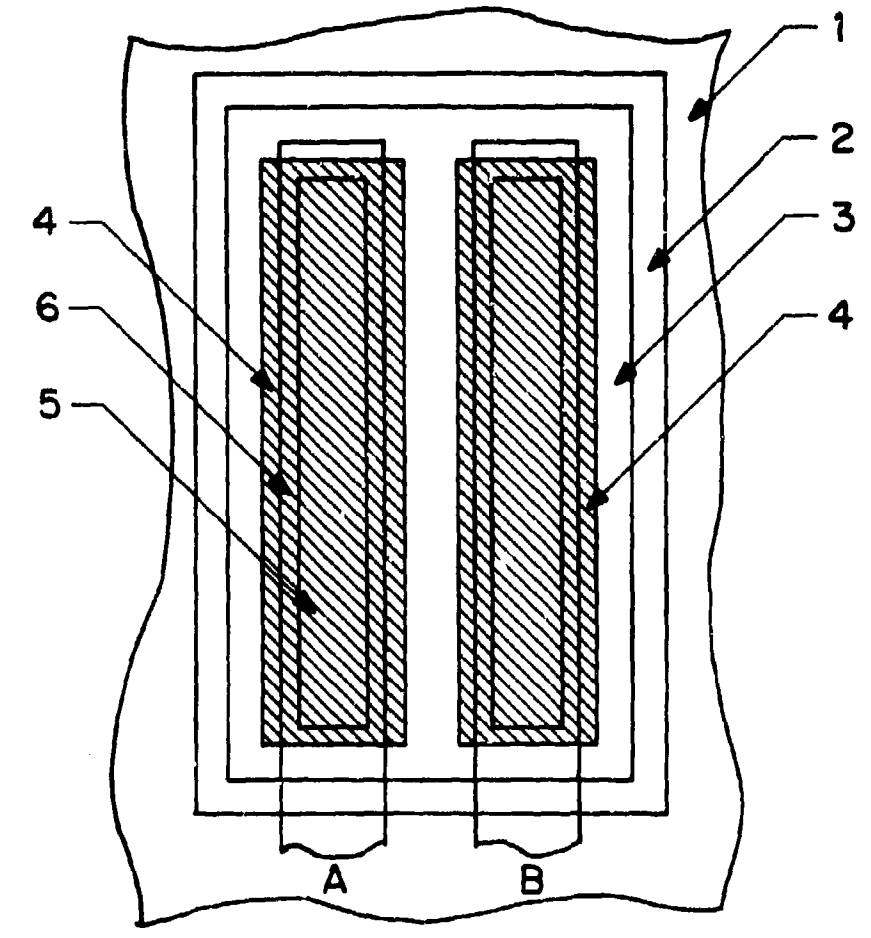
The displacement had to be corrected by delaying field 1 for two horizontal clock pulses in order to reconstruct properly the image on the monitor.

3) The vertical and horizontal gate structures are formed by selectively doping the second polysilicon layer. On the 100A device the undoped regions between the gates was 0.3 mil. On the 100B the gaps between the vertical gates were widened to 0.4 mil. This helped reduce the incidence of shorts between vertical gates.

4) The location of the two-phase barriers relative to the polysilicon gates was changed in order to give better insurance against the occurrence of unwanted potential wells.

5) A novel polysilicon gate protection structure was incorporated. Its main advantage is that it is simpler than the bilateral gate protection systems commonly used. Existing gate protection systems either are unidirectional, i.e., they protect only against transients of one polarity, or they protect against both polarities by employing processing additional to that required to make the device. In the system employed here, no additional processing is required and it is bilateral.

Figure 4-19 illustrates a typical 100B gate protection structure. Layers A and B are aluminum metal lines which contact two islands of doped polysilicon (4), which are diffused into a block of undoped polysilicon (3). Metal line A connects to the gate to be protected; metal line B connects to the system ground, i.e., the semiconductor substrate. In operation, static charges of either polarity which attempt to build up on line A are limited to the breakdown voltage determined by the separation between the polysilicon regions (4). The separation between the doped polysilicon regions is set to obtain a breakdown voltage less than that which would break down the gate dielectric, which is part of dielectric (7) in Figure 4-19. The separation is also chosen to prevent breakdown below the gate operating voltages. In a CCD application, there is a window between approximately 20 volts and 80 volts where the gate protection system can operate. In one easily implemented embodiment, the gate protection system is designed to break down at approximately 40V.



1-Silicon Substrate
2-Contact Vapox
3-Undoped Polysilicon
4-Doped Polysilicon
5-Contact Cuts
6-Aluminum
7-Thin Dielectric

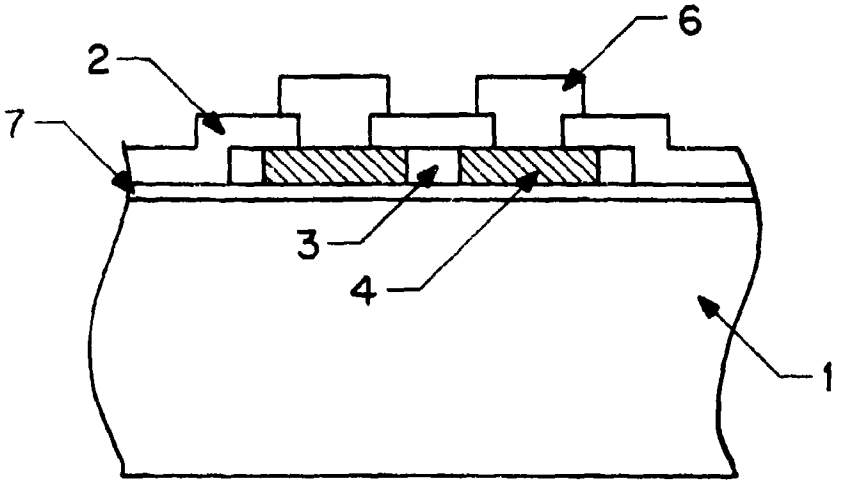


FIGURE 4-19. THERMAL POLYSILICON GATE PROTECTION STRUCTURE

6) An electrical input capability was added to the output register. The purpose of this feature was to facilitate analysis of the high speed circuitry, i.e., the output amplifier reset circuit as well as the output register.

7) An anti-blooming structure was added to the area array. This consisted of an overflow sink for each vertical register, located at the end remote from the output register.

8) A mask was designed to pattern a second layer of aluminum which serves as a light shield. This was intended to augment the shielding provided by the first aluminum layer and in particular to provide more complete shielding of the amplifier.

9) Several other minor changes were made primarily for the purpose of improving fabrication margins during processing.

The subsequent modifications to the 100B which were reflected on the 100BD are illustrated in Figure 4-20. The anti-blooming structure was eliminated to make room for the addition of an input register. Since the electrical input on the output registers was then considered to be redundant, it was also eliminated. The gated-charge-integrator circuit was modified to improve reset action.

4.2.1.4 Clocking

Wave forms suitable for clocking the CCAID-100 series of devices are shown in Figure 4-21. All registers are operated in a two-phase mode. Sharp images can be obtained with horizontal clock frequencies (F_H) up to 5 MHz. One hundred and two (102) horizontal clock pulses are needed to empty the output register. In terms of F_H, the vertical clock frequency F_V is

$$F_V = \frac{1}{\frac{102}{F_H} + H_I}$$

where:

H_I is the horizontal inhibit period.

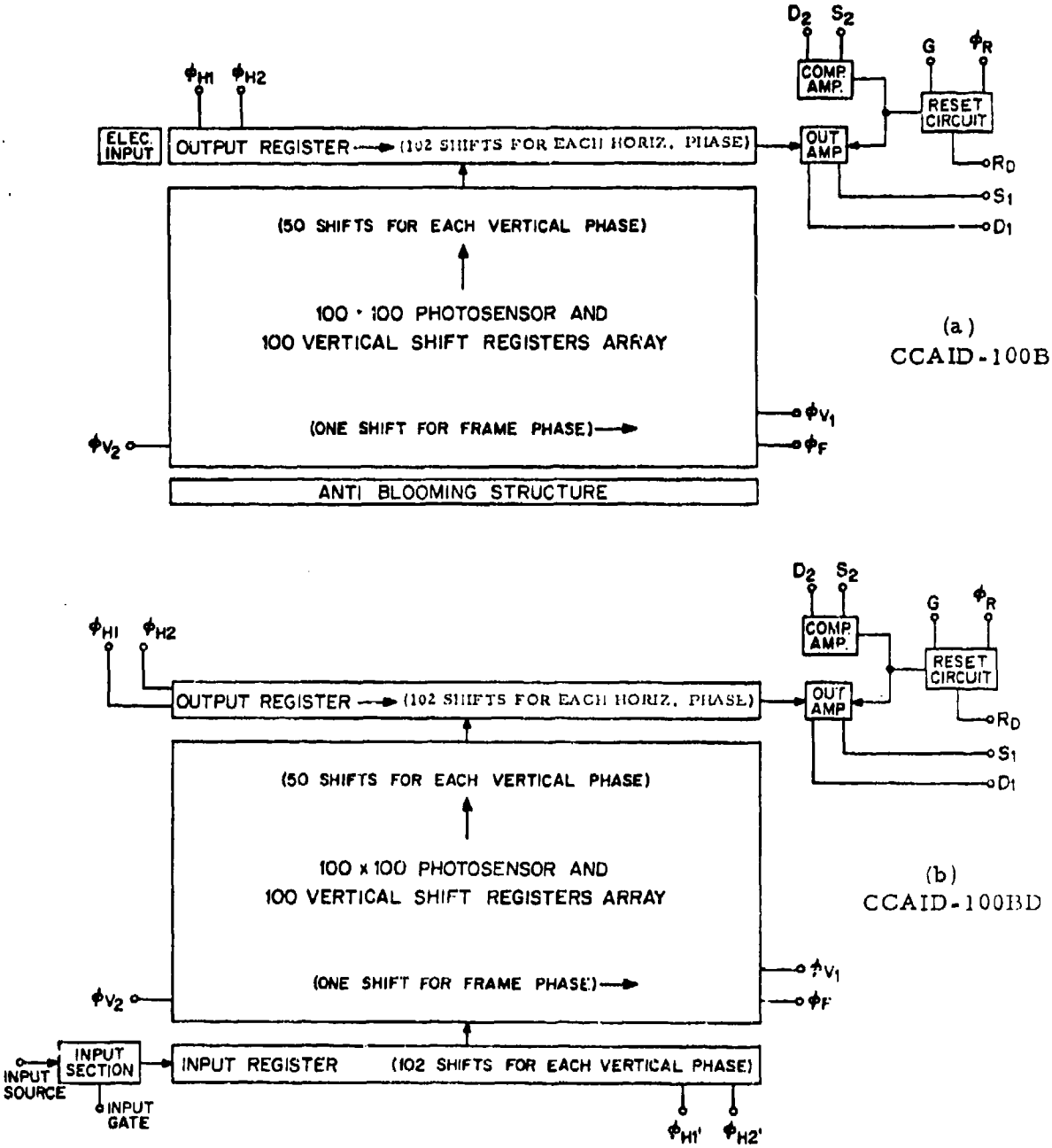


FIGURE 4-20. CCAID-100B and 100BD FUNCTIONAL LAYOUT

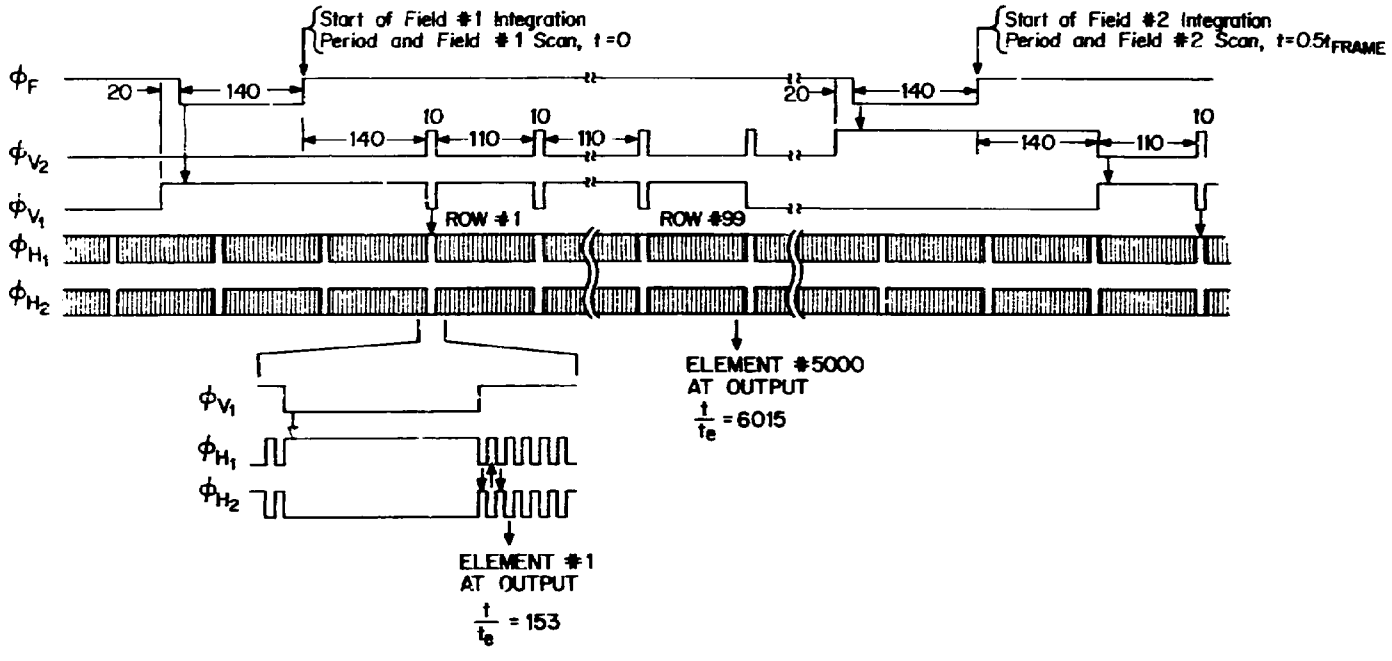


FIGURE 4-21. CLOCK TIMING DIAGRAM FOR CCAID-100B

In terms of F_V, the frame rate F_F is

$$F_F = \frac{F_f}{2} = \frac{1}{100/F_V + 2\,V_I}$$

where:

F_f is the field rate and V_I is the vertical inhibit period.

The inhibit periods H_I and V_I are, respectively, intervals when the next line is transferred into the output register and the next field is transferred into the vertical registers. As the equations indicate, the vertical clock rate is slightly less than 1/100th of the horizontal rate. Also, the frame rate is slightly less than 1/100th of the vertical rate.

Φ_{H1} and Φ_{H2} are complementary square waves. Φ_{V1} and Φ_{V2} are also complementary but with an assymetrical period to optimize the ratio of line scanning time to blanking time.

Each vertical burst consists of at least 50 pulses, the number required to shift out one field of information. At the end of each field, the frame gate is lowered and video information is transferred to whichever vertical gates are high. As can be seen, a special transfer pulse is inserted in the blanking interval of each vertical phase during alternate fields to accomplish the desired transfer. The reset clock Φ_R operates at the same rate as the horizontal clocks. It is used to reset the amplifier gate after each bit has been sampled.

Figure 4-22 shows the circuits used to generate the required wave forms. The master oscillator, in the upper left, operates at twice the horizontal bit rate. For the values shown, the master oscillator operates at 1 MHz. The frame rate is approximately 30/second. Also included are the horizontal sweep circuits used to drive a display monitor.

4.2.2 Device Performance

4.2.2.1 Imaging Tests

Imaging tests were performed with the objective of determining image quality at low-light-levels and reduced temperatures. The dynamic range, that is, the ratio of saturation signal to RMS noise level in the dark, is approximately 1000:1 for this device and is virtually independent of temperature. However, near room temperature dark-signal non-uniformities

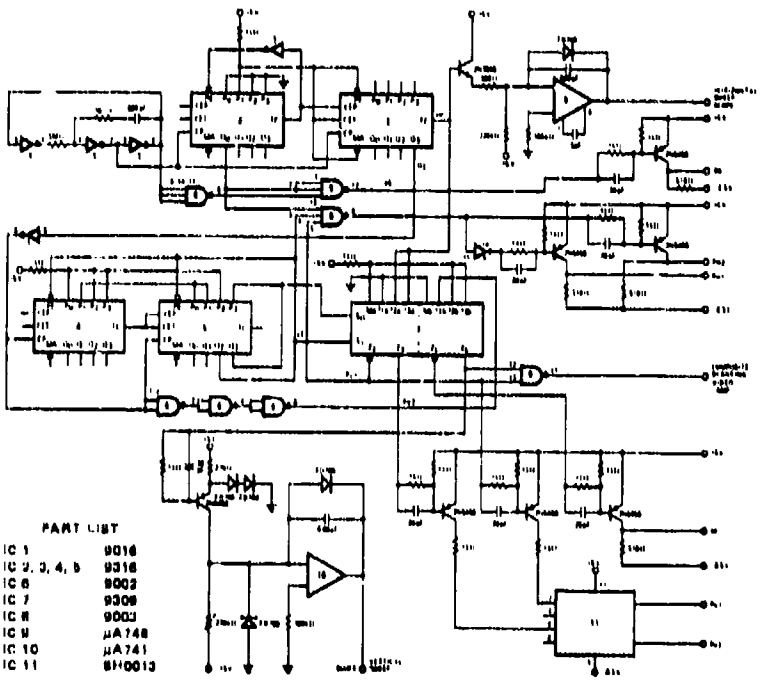


FIGURE 4-22. FREQUENCY AND PULSE GENERATING CIRCUITS

result in fixed pattern noise at low-light-level. Therefore, imaging tests were performed at lower temperatures where dark-current non-uniformities are substantially reduced. Detailed data pertaining to dark signal and charge-transfer efficiency are given in subsequent sections.

At room temperature, high quality imaging has been demonstrated at 30 frames per second. The video image shown in Figure 4-23 had a dynamic range at the display output estimated to be approximately 20:1 with highlights in the picture close to the saturation level of the device. (In this figure and in the following set of figures, the first picture element that is read out is in the lower left-hand corner.) At reduced light intensities and with readjustment of the video gain, the image quality remains high with the exception that dark signal non-uniformities appear. Figure 4-24 shows a video image for a highlight signal level equal to 10 percent of saturation. In this picture, the small white spots are dark signal non-uniformities of the type referred to as dark-current spikes. For the conditions of this imaging test, the tested unit had approximately 40 dark-current spikes with amplitudes in the approximate range of 0.5 to 5% of saturation. From an estimated saturation charge level of 4×10^5 electrons, a frame time of 1/30th second, and a photoelement area of 6.0×10^{-6} cm^2, these 40 spikes correspond to dark-current density variations in the range of 1.6 to 16 nA/cm^2.

In addition to dark-current spikes, Figure 4-24 shows vertical streaks that are both brighter and darker than the surrounding image. Those that are brighter are considered to be caused by the same type of defect which causes the spikes. Here, the defects are in the vertical registers rather than in the photoelements. The darker vertical streaks appear to be caused by signal annihilation mechanism occurring at the point where the vertical registers join the horizontal register. This can result from a structural defect that in turn causes part of the signal charge to be injected into the substrate. It has been observed on devices that exhibit this phenomenon that the horizontal clock voltages influence the magnitude of the dark streaks, while the vertical clock voltages do not. Further investigation is required to eliminate this effect if it persists in the newer area image sensors.

On cooling, the dark signal magnitudes decrease. For temperatures below approximately -20°C, the dark signal effects are small compared to amplifier noise. At -40°C, the same unit that produced the room temperature images shown in the two previous figures was tested over a wide range of light levels. These images are shown in Figure 4-25. No change is apparent in the near-saturation light level (Picture a) on cooling. At the first reduced light level (Picture b), a highlight signal level ≈10% of saturation, the image quality appears as good as at the near-saturation level.

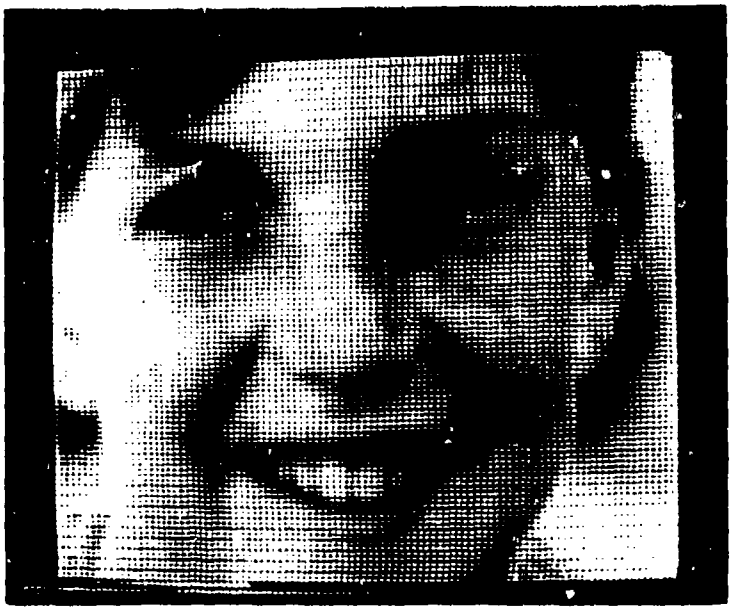
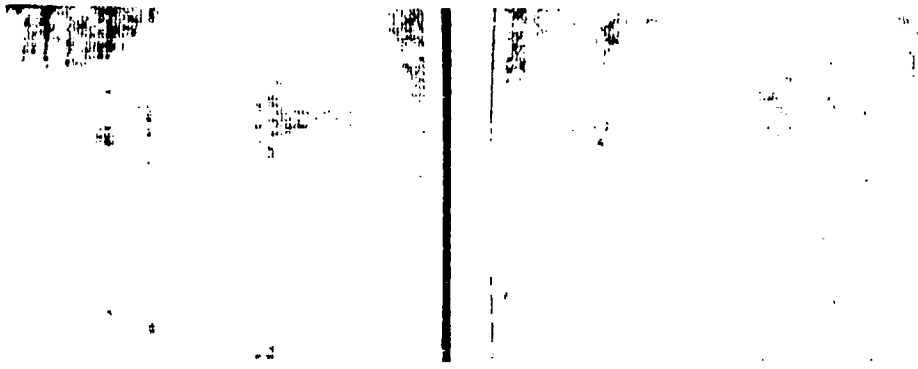


FIGURE 4-23. IMAGING AT 27°C NEAR SATURATION ILLUMINATION LEVEL

FIGURE 4-24. IMAGING AT 27°C AT 10% OF SATURATION ILLUMINATION LEVEL

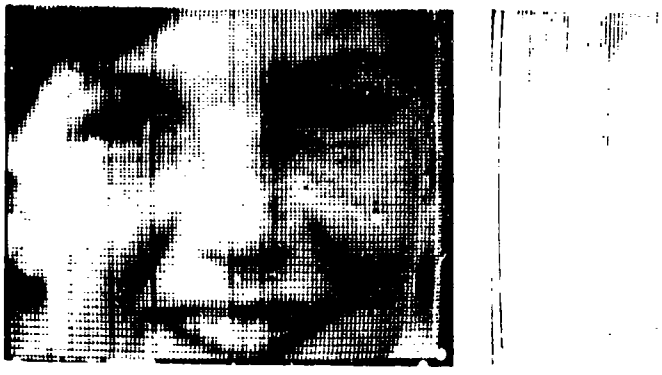
(a) Highlight Signal Level
≃360,000 Electrons/Pixel
1/30 sec. Exposure

(b) Highlight Signal Level
≃36,000 Electrons/Pixel
1/30 sec. Exposure



(c) Highlight Signal Level
≃3600 Electrons/Pixel
1/30 sec. Exposure

(d) Highlight Signal Level
≃360 Electrons/Pixel
1/30 sec. Exposure



(e) Highlight Signal Level
≃3600 Electrons/Pixel
5 sec. Exposure

(f) Highlight Signal Level
≃360 Electrons/Pixel
10 sec. Exposure

FIGURE 4-25. IMAGING AT -40°C. ILLUMINATION LEVEL WAS SUCCESSIVELY ATTENUATED BY A FACTOR OF TEN IN FIGURES (a) TO (d). FIGURES (e) AND (f) WERE MADE AT THE SAME ILLUMINATION LEVELS AS FIGURES (c) AND (d), RESPECTIVELY.

Not only have the dark-current spikes disappeared, but also the dark streaks. With the highlights at one percent of saturation (Picture c), the dark streaks reappear and resolution is limited by random noise. Picture e shows this same illumination condition photographed with a five-second exposure. Because random noise is averaged out, a few more dark streaks become apparent. Again, these dark streaks are seen to be uniform from top to bottom and do not have any cumulating degrading effect on the image toward the right-hand side of the picture. Hence, it is concluded that the signal annihilation mechanism discussed above takes place only during the horizontal blanking time. In pictures d and f, it can be seen that at the lowest signal levels there is some loss of horizontal transfer efficiency but no apparent loss of vertical transfer efficiency.

In conclusion, high quality imaging has been reported on one device over a substantial dynamic range. However, at low light levels, the image quality was degraded primarily by a vertical dark-streak effect.

4.2.2.2 Characterization of Charge-Transfer Efficiency

4.2.2.2.1 Test Facility

In order to investigate the charge-transfer efficiency (CTE) characteristics of CCAID-100BD arrays at low temperature, the low temperature test facility, shown schematically in Figure 4-26, was constructed.

The device, housed in a small dry box, is cooled by a stream of dry nitrogen gas, which passes through a liquid nitrogen bath at 77°K. The temperature is regulated in part by manually controlling the gas flow. Fine temperature adjustments are made using resistive heaters mounted on either side of the device. Two thermocouples attached to the top and bottom of the device, as shown, monitor the temperature. After steady state conditions have been reached, the device temperature is stable to within a few degrees for periods of an hour or more. The two temperature readings agree within a few degrees.

The optical response of the array to a light spot is measured by mounting the dry box on the X-Y stage of a trinocular microscope. This microscope is equipped with a light spot lamp mounted on the third ocular. The image of the point source lamp is focused through a 10X objective to produce a light spot that can lie entirely within a 0.8-mil x 1.2 mil photoelement.

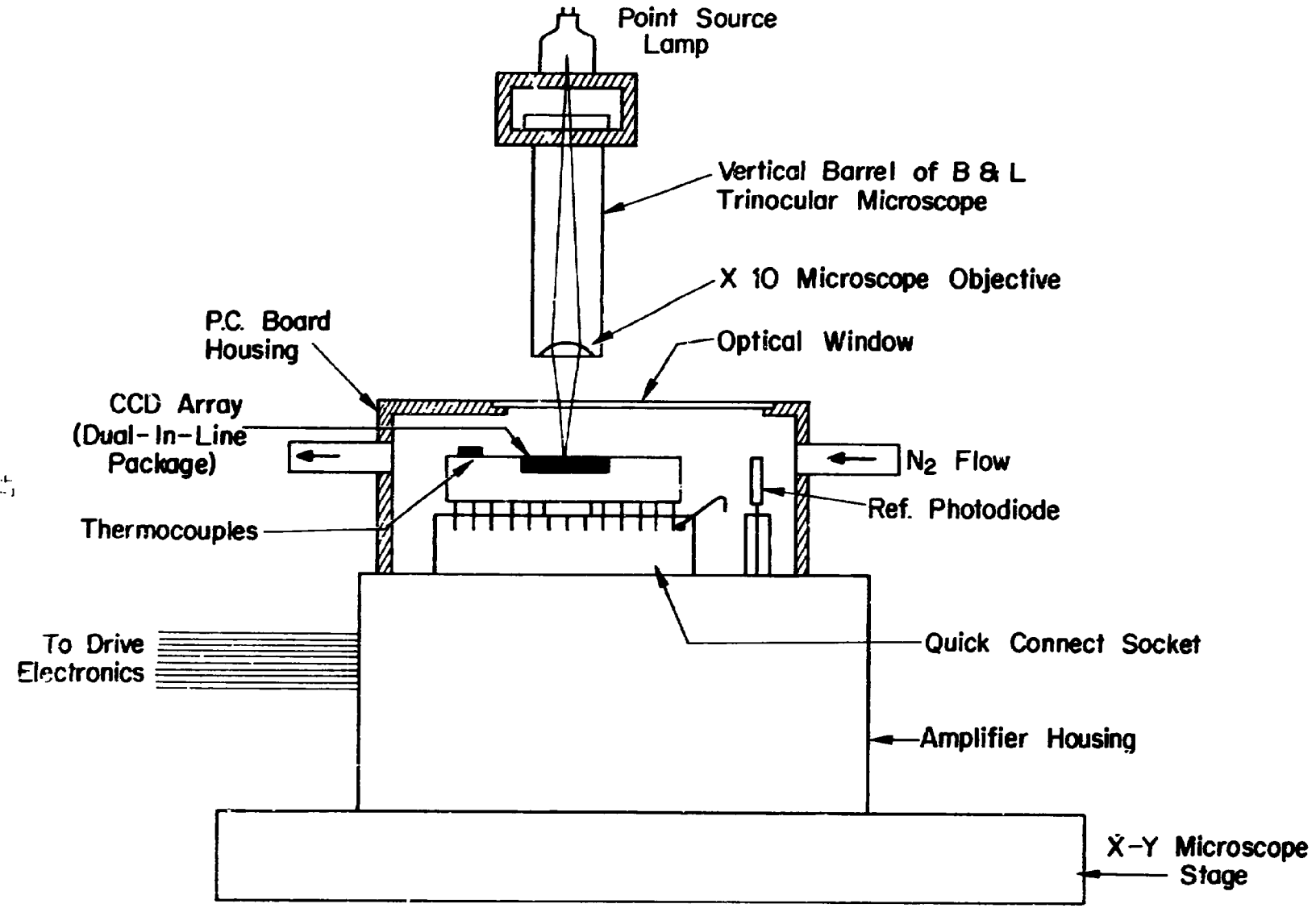


FIGURE 4-26. LOW TEMPERATURE LIGHT SPOT FACILITY

4.2.2.2.2 Methods of Measuring Transfer Efficiency

The light spot is centered on a photoelement located at coordinates (X, Y) of the array; the output amplifier is chosen as the origin. The video outputs from this element, $V_p(X,Y)$, from the trailing horizontal element, $V_{TH}(X+1,Y)$, and from the trailing vertical element in the same field, $V_{TV}(X,Y+2)$, are measured by chopping the light-spot intensity and determining the change in signal amplitude with an oscilloscope.

The conventional calculation of charge-transfer inefficiency in the vertical registers and in the horizontal register is made using the expressions:

$$\epsilon_V = \frac{V_{TV}(X,Y+2)}{\frac{Y}{2} \cdot V_p(X,Y)}$$

$$\epsilon_H = \frac{V_{TH}(X+1,Y)}{X \cdot V_p(X,Y)}$$

where X and $\frac{Y}{2}$ are the number of horizontal and vertical transfers, respectively. Values of ϵ_V and ϵ_H thus obtained were typically $\sim 10^{-4}$ at high light levels. At light-spot intensities below 10% of saturation illumination, trailing-pulse amplitudes were generally too small to be measurable by direct viewing of the video signal on an oscilloscope. The smallest detectable trailing-pulse signal was approximately 0.1% of saturation.

A second method for determining charge-transfer efficiency is to measure the linearity of response to a light spot of decreasing intensity for a photoelement remote from the amplifier. A linear variation in output pulse amplitude with light intensity can only be obtained when the total effect of all charge loss and all transfer inefficiency mechanisms is small. The linearity of the amplifier is established by measuring the response to a light spot for a photoelement close to the amplifier. This method is then limited only by the accuracy of calibration of the neutral density filters used to reduce the light intensity. The calibration is typically ±20%. An interference filter peaked at approximately 0.55 μm was used in all measurements; it served as an attenuator and provided a very low level of optical crosstalk.

4.2.2.2.3 Experimental Results

Linearity and trailing pulse data for the temperature range 25°C to -80°C are summarized in Table 4-4. The device used was a blemish-free CCAD 100BD. As the temperature was lowered, the operating voltages were

TABLE 4-4

RESPONSE CHARACTERISTICS OF A CCAID-100BD DEVICE TO A LIGHT SPOT OF VARIED INTENSITY OVER THE TEMPERATURE RANGE 30°C TO -80°C

V_{SAT} = 70 mV f_o = 500 KHz Device No. 99-W5-8 t_j = 25.5 ms

T (°C)	X, Y	Light Spot * Intensity Relative $\lambda \simeq$ 0.5 µm	V_p ** (mV)	V_{TH} (mV)	V_{TV} (mV)	Operating Voltages (V) $V_{\phi RH}$, $V_{\phi RL}$, $V_{\phi HH}$, $V_{\phi HL}$, $V_{\phi VH}$, $V_{\phi VL}$, $V_{\phi PH}$, $V_{\phi PL}$
30°	50,96	1	29.0	0.4	0.2	6, 2, 14.5, -5
		0.1	3.6	0.2	0.2	3.5, -4.5, 13 , 2.5
		0.01	0.4	0.2	0.2	
	97,98	1	40.0	0.5	0.5	5.2, 2.8, 5, -5, 3, -7, 12.5, 2
-18°	97,2	0.5	17.0	<0.2		
	97,2		17.0***	<0.2		
	97,50		14.0	<0.2		
	97,50		19.0***	<0.2		
	97,98		10.0	<0.2		
	97,98		17.0***	<0.2		
	97,50		19.0	<0.2		5.2, 2.8, 5, -5,
			19.0***	<0.2		3.5, -10 , 12.5, -2,
-50	97,96	1.0	62.0	0.5	0.5	
		0.5	25.5	0.5	0.2	
		0.1	5.0	0.2	0.2	
		0.01	0.7	0.2	0.2	
		0.005	0.25			5.2, 2.8, 5, -5,
		0.002	0.08			3.5, -12.5, 12.5, 2
-80°	99,96	1	50	0.8	0.2	
		0.5	20	0.4	0.2	
		0.01	0.6	0.1	0.1	
		0.002	0.15			
		0.001	0.08			

* - A relative spot intensity of "1" is 50% to 75% of the device saturation intensity.
** - Accuracies range from ± 0.05 mV to ± 0.2 mV.
*** - Incremental response to the light spot in the presence of uniform background illumination.

changed to optimize transfer efficiency. The operating voltages given in the last column of the table are presented in chronological order as the voltages were tuned first to optimize horizontal-transfer efficiency at 30°C and then to optimize vertical-transfer efficiency at lower temperatures. The definitions of these operating-voltage symbols are given in Table 4-5.

At -18°C the vertical-transfer efficiency was low for a set of operating voltages that gave high CTE at room temperature. Under these conditions neither the horizontal or the vertical trailing pulses were larger than 2% of the principal pulse amplitude, despite the charge loss in the vertical register, which was evident from the reduction in the principal pulse amplitude as the light spot was moved along the vertical register from element (97,2) to element (97,98). This apparent charge loss, not detectable in the trailing pulses, may be caused by a decrease in CTE at low signal levels which smears the trailing pulse train uniformly along the vertical register. This loss of signal is reduced by providing a uniform background illumination. More satisfactory performance was obtained after retuning of the vertical clock voltages, namely, increasing the negative swing from -7 to -10 volts. As can be seen from the last entry at T = -18°C, this eliminates any dependence on background-charge level and increases the amplitude of the principal pulse.

At -50°C it was necessary to increase the negative swing even further to obtain good CTE at the lowest signal level. It was found that this set of voltages was optimum not only at -50°C and -80°C but also at room temperature when the device was subsequently warmed up. Extensive data, however, was taken only at the lower temperatures where the absence of dark current allowed more accurate signal amplitude determinations at low signal levels. The low temperature data indicate that near the saturation level the trailing pulse amplitudes V_{TH} and V_{TV} were typically 1% or less of the main signal pulse, V_p, throughout the array. The corresponding transfer efficiencies calculated from the above expression were, consequently, 0.9999 or higher.

Good linearity of response is indicated in Figure 4-27 for operation at -50°C, a frame rate of 40 Hz, and a bit rate of 500 KHz. The data points follow a straight line within experimental error for illumination levels ranging from 50% of saturation down to the lowest measurable point at 0.2% of saturation. This indicates that no measurable reduction in transfer efficiency occurs at signal levels down to the noise level of the amplifier.

TABLE 4-5

DEFINITIONS OF CCAID-100BD OPERATING VOLTAGE SYMBOLS

SYMBOL	PARAMETER
$V_{\phi HL}$	Horizontal Register Clock Voltage LOW
$V_{\phi HH}$	Horizontal Register Clock Voltage HIGH
$V_{\phi VL}$	Vertical Register Clock Voltage LOW
$V_{\phi VH}$	Vertical Register Clock Voltage HIGH
$V_{\phi RL}$	Reset Clock Voltage LOW
$V_{\phi RH}$	Reset Clock Voltage HIGH
$V_{\phi PL}$	Photogate Clock Voltage LOW
$V_{\phi PH}$	Photogate Clock Voltage HIGH

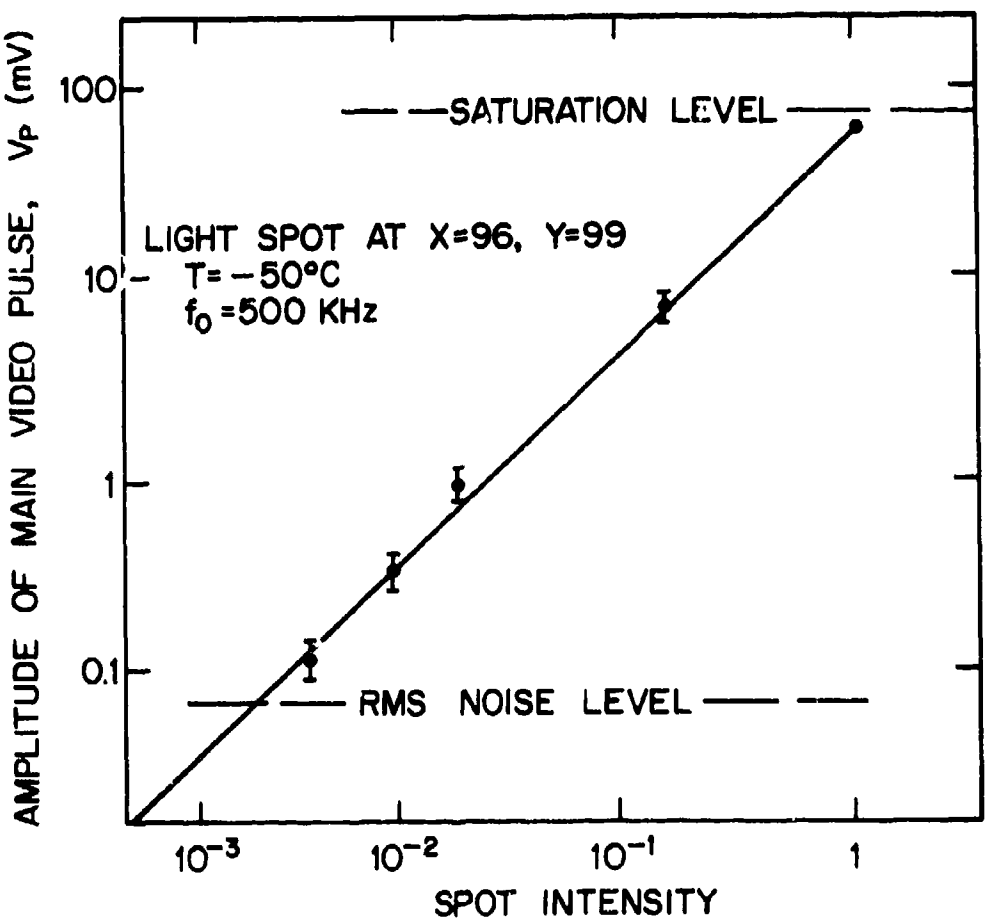


FIGURE 4-27. LIGHT SPOT RESPONSE VS. LIGHT SPOT INTENSITY FOR CCAID-100BD UNIT NO. 99-W5-8

4.2.2.3 Characterization of Dark Current

It has been observed in a variety of buried-channel charge-coupled devices that both the average dark signal and the dark-signal non-uniformities have a temperature dependence that is approximately the same as that of the intrinsic carrier concentration parameter, n_i, for silicon for a limited temperature range extending downward from 25°C. Assuming this temperature dependence from 25°C to -60°C, the dark signal effects would vary as shown in Figure 4-28. This figure shows both the calculated dark signal effects and the amplifier noise as a function of temperature. An average dark-current density of 3 nA/cm^2 at 25°C is assumed; this was typical of the units studied. This current density generates a dark charge of approximately 3% of saturation for a 33-msec integration period. At room temperature the typical peak-to-peak dark signal or dark-current spike is approximately 10% of saturation. This limits the dynamic range for only a small number of picture elements. Dark-current shot noise is negligible over the full temperature range shown in the figure. Below -25°C all dark signals are below the rms amplifier noise.

Figure 4-29 shows the temperature dependence of the average dark signal for a representative CCAID-100BD device. This figure also shows a calculated curve based on the measured room temperature dark-current density of 4 nA/cm^2 and the temperature dependence of the n_i parameter. The two curves track down to -10°C. In order to explain the deviation at lower temperature, it is necessary to explore the dependence of this effect on the type of impurity in the silicon and on gettering processes.

4.3 CHARGE-COUPLED AREA IMAGING DEVICE, 190 x 244 MODEL A (CCAID-244A)

The design of the CCAID-244A incorporates three significant advances over the CCAID-100BD. First, the number of photoelements is increased by a factor greater than four. Second, it has an output bit rate in excess of the 7-MHz value required for NTSC standards-compatible operation of sensors with double the number of photoelements per row. Third and most significant, it is the first device to incorporate a distributed floating-gate amplifier (DFGA). Furthermore, this was the first DFGA made in the form of an integrated circuit. The demonstration of the low noise properties and the resulting low-light-level imaging properties of this device, which are described in Section 4.3.2.4, may be considered to be the major achievement of this second phase of the program.

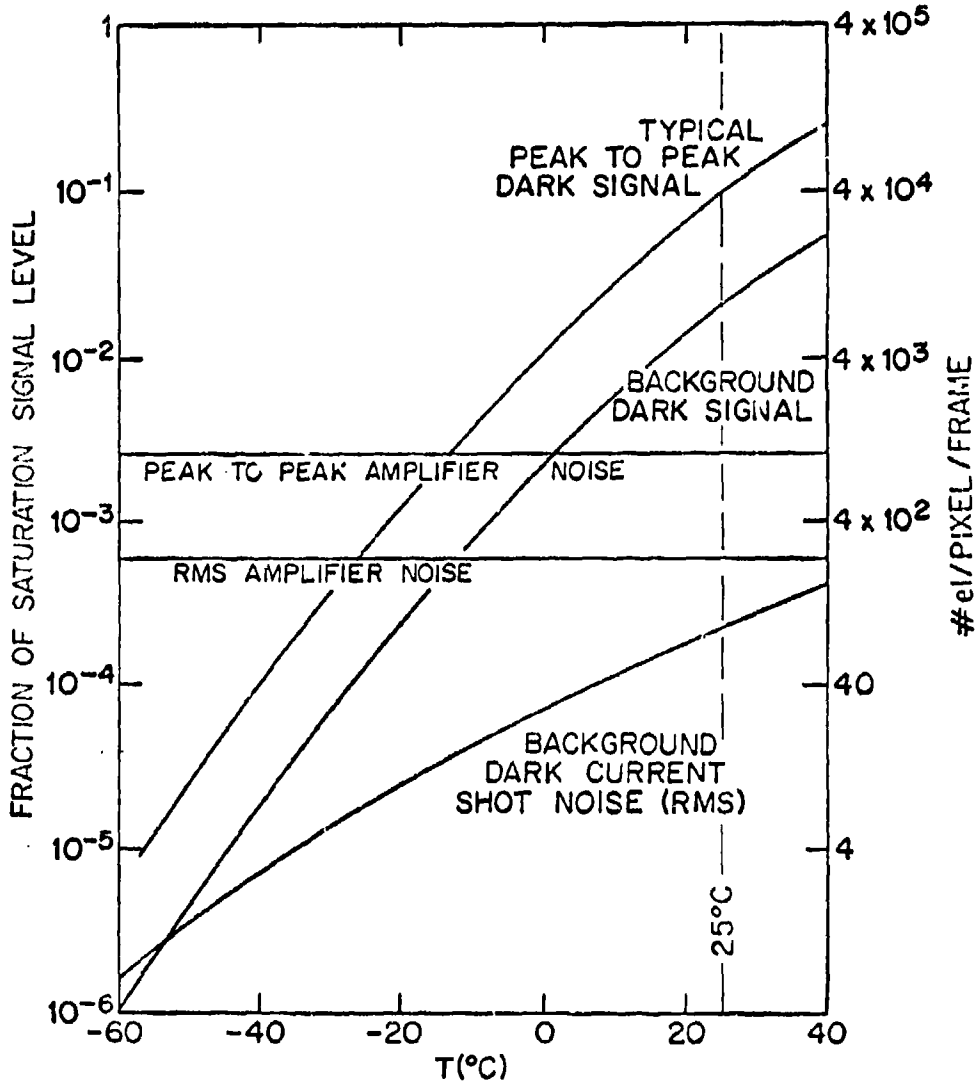


FIGURE 4-28. DARK SIGNAL EFFECTS. Peak-to-peak, average and RMS dark signal plotted against temperature, expressed as a fraction of saturation. All curves are calculated for $J_D \simeq 3nA/cm^2$ for room temperature.

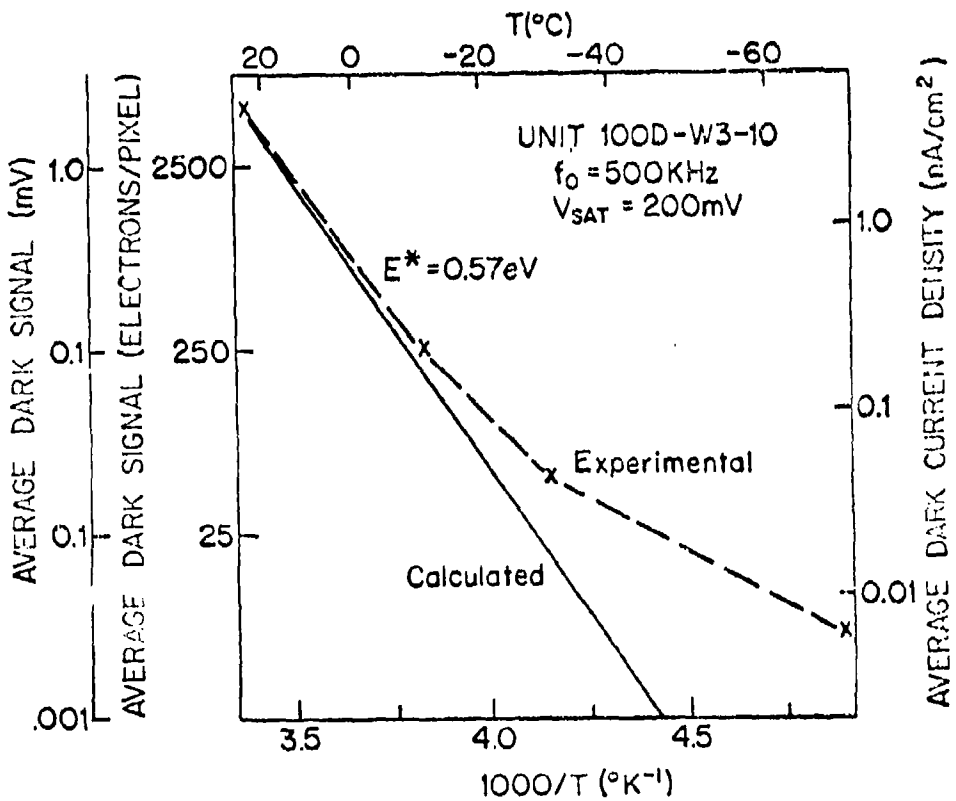


FIGURE 4-29. EXPERIMENTAL AND CALCULATED CURVES OF DARK CURRENT VS. TEMPERATURE. The experimental data were taken with a unit exhibiting an average dark current of 4 nA/cm^2 at room temperature. The two ordinates on the left give the dark output and the corresponding dark charge per pixel. The ordinate on the right gives the calculated dark current density.

4.3.1 Device Description

4.3.1.1 Functional Elements

The CCAID-244A is a 190 x 244 photoelement charge-coupled area imaging device. Since it follows the development of the CCAID-100B, many of its structural features are similar to those of the smaller device. The 244A is considered to be a stepping stone to a larger device, the CCAID-488A, which has four times the number of sensing elements, i.e., 380 x 488; as required for resolution comparable to the effective resolution of commercial television. The rationale behind choosing 190 x 244 elements for the 244A is that it is a half-size 380 x 488; much of the experience gained with it can, therefore, be readily extrapolated to the larger device.

Figure 4-30 shows a functional layout of the 244A. As with the CCAID-100 series devices, it employs interleaved sensor and storage arrays. The area array portion of the device is similar in construction to the 100BD except for the number of elements involved and their dimensions. An input register is included to facilitate electrical testing and also to increase the utility of the array. The area array portion is of the 2-phase implanted-barrier type; the input and output registers are 4-phase structures. The 4-phase structure is employed, since it offers a more flexible clocking configuration for the high speed registers and the floating-gate amplifiers. The amplifier section is unique in that it contains four separate output amplifier systems arranged to facilitate performance comparison measurements. These amplifiers are (1) a gated-charge integrator (DDA), (2) a distributed floating-gate amplifier (DFGA), (3) an input floating-gate amplifier (FGA1) located at the input to the DFGA and (4) an output floating-gate amplifier (FGA2) located at the end of the input channel of the DFGA. There are two charge-steering gates, one located at the input to the gated-charge integrator; the other to the floating gate devices. Because the charges in the CCD channel are sensed non-destructively by the individual floating-gate amplifiers, no steering is required within that system.

A view of the 244A die is shown in Figure 4-31. It contains 33 bonding pads. Although the pad count is not minimal, it reflects the desire to have maximum operating flexibility for the first implementation of the DFGA. In a minimum pad system, the pad count could be reduced to 28 without sacrificing any operational features. Descriptions of the pad functions are given in Table 4-6. Other structures visible in Figure 4-31 are test devices used to facilitate evaluation. These are polysilicon test resistors, implanted test capacitors for determining the barrier height, facsimiles of the output circuitry, and gate-protection test structures.

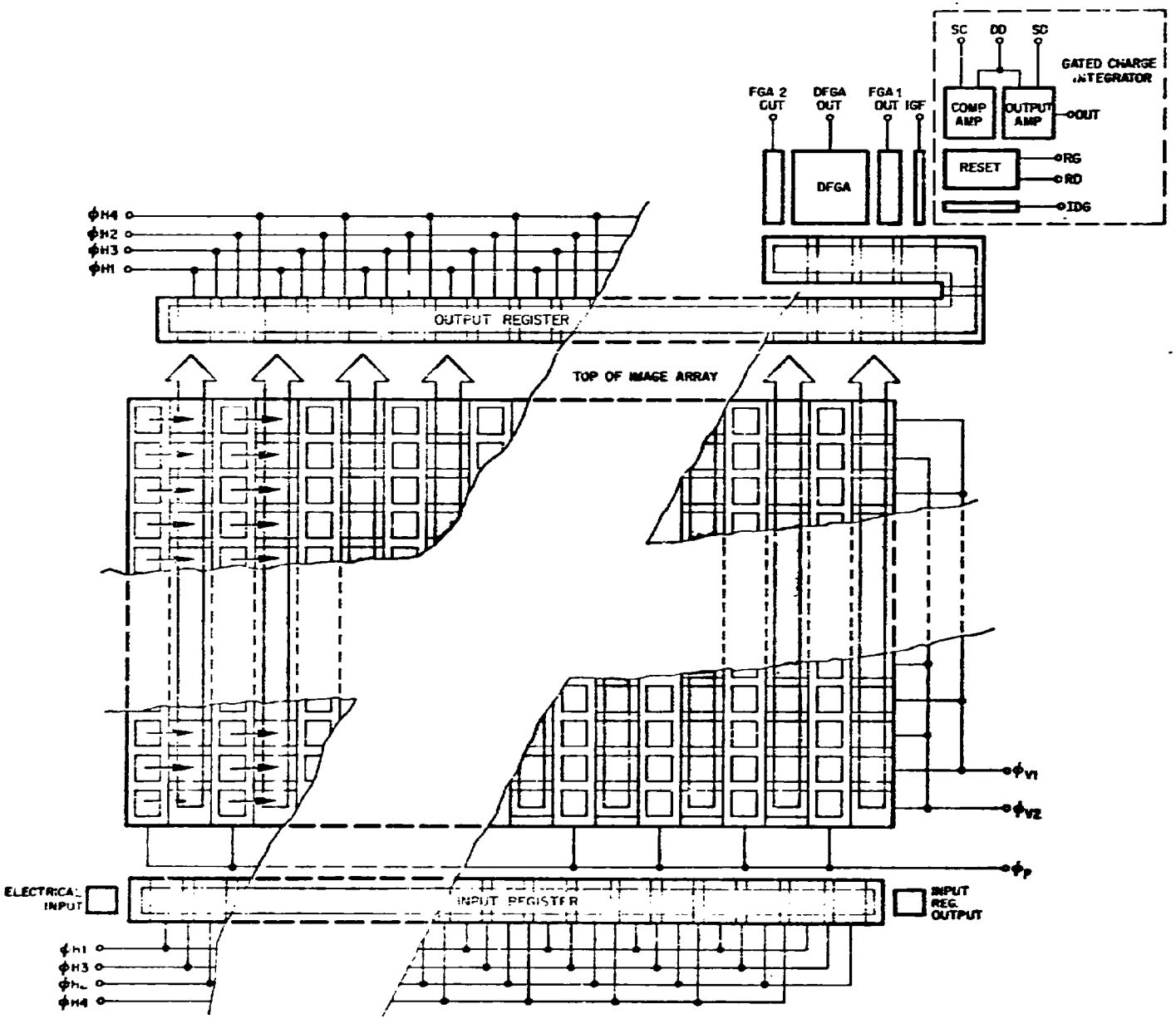


FIGURE 4-30. FUNCTIONAL LAYOUT OF CCAID-244A

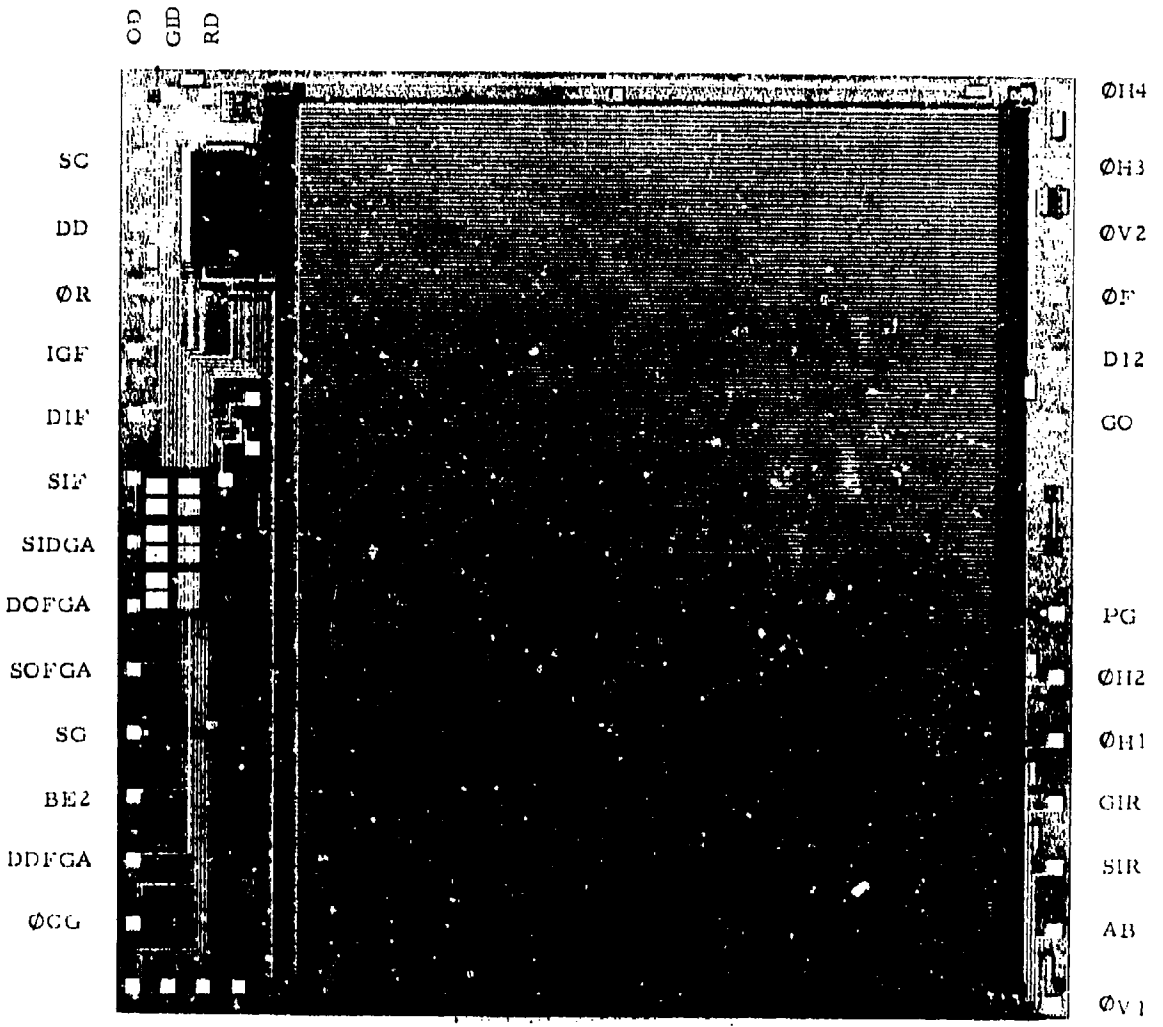


FIGURE 4-31. CCAID-244A DIE

TABLE 4-6. CCAID-244A PIN DESIGNATIONS

PIN NO.	SYMBOL	PURPOSE
1	GRDC	DC Control Gate between DFGA Input and Output Registers. Used for Transient Reduction.
2	ϕ_{CG}	Clocked Control Gate between Input and Output DFGA Registers; in Phase with ϕ_{H2}.
3	DDFGA	Sink for Input and Output DFGA Registers.
4	BE_2	Bias Electrode for Floating Gate of Output Register.
5	SG	Signal Ground.
6	SOFGA	Source of Distributed Floating-Gate Output Amplifier.
7	DOFGA	Drain of Distributed Floating-Gate Output Amplifier.
8	SIDGA	Source of Inter-Register Floating-Gate Amplifiers.
9	SIF	Source of Input Floating-Gate Amplifier.
10	DIF	Drain of Input Floating-Gate Amplifier.
11	IGF	Input Gate to Floating-Gate Amplifier System.
12	ϕ_R	Reset Gate.
13	DD	Drains of Differential Amplifier.
14	SC	Source of Compensation Amplifier.
15	OD	Signal Output of Differential Amplifier.
16	GID	Input Gate to Differential Amplifier.
17	RD	Reset Drain.
18	ϕ_{H4}	Horizontal Register, Minor Phase 4.
19	ϕ_{H3}	Horizontal Register, Minor Phase 3.
20	ϕ_{V2}	Vertical Register, Phase 2.
21	ϕ_F	Frame Gate Clock Input.
22	DIR	Drain of Input Register.
23	GO	Output Gate of Input Register.
24	PG	Power Ground.
25	ϕ_{H2}	Horizontal Register Major Phase 2.
26	ϕ_{H1}	Horizontal Register Major Phase 1.
27	GIR	Input Gate to Input Register.
28	SIR	Input Source to Input Register.
29	AB	Anti-Blooming Bias.
30	ϕ_{V1}	Vertical Register, Phase 1.
31	BE_1	Inter-Register Bias Electrode.
32	SOF	Source of Output Floating-Gate Amplifier.
33	DOF	Drain of Output Floating-Gate Amplifier.

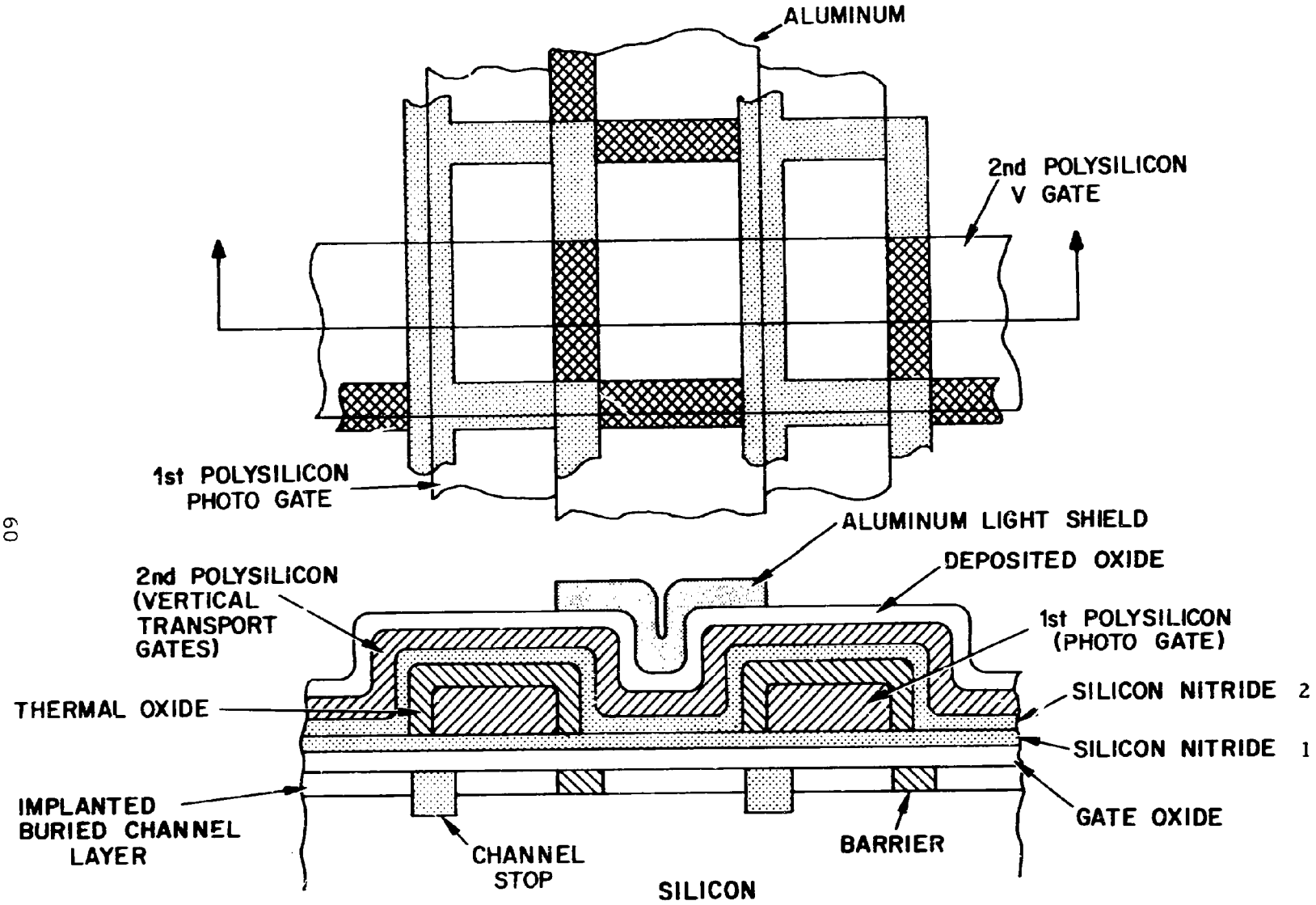


FIGURE 4-32. CROSS-SECTION OF CCAID-244A AREA ARRAY

4.3.1.2 Structural Details

The die size for the 244A is 248 mils by 242 mils. One of the design objectives was to constrain both the X and Y dimensions to ≤ 250 mils, to avoid photocomposition of the photolithographic masks. The output register, for example, was folded in the X direction to employ space in the more available Y direction.

The cell size in the area array section is 30 μm horizontally x 18 μm vertically to make the dimensions of the active area 5700 μm (224 mils) x 4392 μm (173 mils) and to result in a 4:3 aspect ratio. This choice of cell size results in a format close to that of the super-8 camera (5.3 x 4.0 mm). Relative to the CCAID-100B device, the 244A has 46,360 photosensing elements versus 10,000 for the 100B, and has a chip area of 57,600 mil^2 versus 29,987 mil^2 for the latter.

A cross-section through the area array in a direction parallel to the photoelement rows is shown in Figure 4-32. It may be noted that this part of the structure is very similar to that of the 100B device. A second layer of silicon nitride has been added to reduce the incident of shorts between the two polysilicon layers. In addition, the packing density of the 244A is much higher; cells are on 30 μm x 18 μm centers versus 40.6 μm x 30.5 μm centers for the 100B. The photosensitive area for a cell is 216 μm^2. The charge storage area for a photosite is 76 μm^2 and the storage area for a vertical register is 84 μm^2. The area utilization factor for photosensitivity is 40%.

Some of the operational characteristics projected from the structural layout are:

Signal saturation charge	0.06 pC (based on 2.5V barriers)
Maximum signal	3.7×10^5 electrons
Dark current	2.5×10^{-9}A (assuming 10 nA/cm^2 at T = 25°C)
Dark charge	1.8×10^{-15} coulombs (integration time = 33 μsec and T=25°C)

Experience with prior linear array designs indicates that the present structure should operate well at an output clock frequency of 7.16 MHz, the proposed upper frequency limit. The horizontal gate lengths are sufficiently short that there is no time constant problem introduced by the resistance of the polysilicon which forms the gates. Although the vertical register gates and photogate are long narrow strips of polysilicon with substantial

resistance (20 Ω/□), the operating frequencies are much lower (15.7 KHz and 60 Hz, respectively) and again the time constants are adequately low. The vertical gate time constant is 230 nsec; the photogate time constant is 120 nsec. The total input capacitance at the terminals of each vertical gate is approximately 1500 pF; the total capacitance at the photogate terminal is approximately 2250 pF.

4.3.1.3 Design Features

4.3.1.3.1 Output Register and Amplifier Interface

Most of the design innovations on the 244A relative to the 100B are incorporated in the output section of the device. Figure 4-33 (a) shows the portion of the output register which interfaces with the amplifier structure. As was indicated previously, the horizontal arrays are 4-phase structures, though they can also be operated in a 2-phase mode. The major phases, designated ϕH_1 and ϕH_2, are formed from the first polysilicon layer; the minor phases, ϕH_3 and ϕH_4, are made from the second polysilicon layer and are separated from the major phases by thermal oxide formed on the lower gates plus a thin layer of silicon nitride. The overlap between the two sets of gates is 2 μm which is in compliance with the 2 μm design rule objectives for all layers. Since the area array cells are on 30 μm centers, the output register gate lengths are constrained by these considerations and the desire to avoid polysilicon etching problems by keeping gaps reasonably wide. The choices resulted in 10 μm major gate lengths, 9 μm minor gate, and 5 μm major gaps and 6 μm minor gaps, as depicted in the cross-sectional drawing in Figure 4-33 (b).

As Figure 4-33 (a) indicates, there are two 90° turns required in order to satisfy the chip format objectives discussed earlier. Tests performed on completed devices indicate that performance is not impaired by these charge-steering techniques. Two separate control gates are shown (shaded) which enable one to direct charges either to the DDA or to the DFGA channel. The DFGA channel directs charge to FGA1 and FGA2 as well as the DFGA. This channel was made approximately half the width of that of the output channel to minimize noise. Since the DFGA is primarily designed for low-light-level operation, the reduced saturation charge was considered a worthwhile tradeoff.

Another useful feature of this design is that overload DFGA charge can be drained to the DDA. The DDA then serves as a DFGA saturation control. It should also be noted that the DFGA can be separately evaluated by injecting signals electrically into the DFGA through the DDA reset circuit.

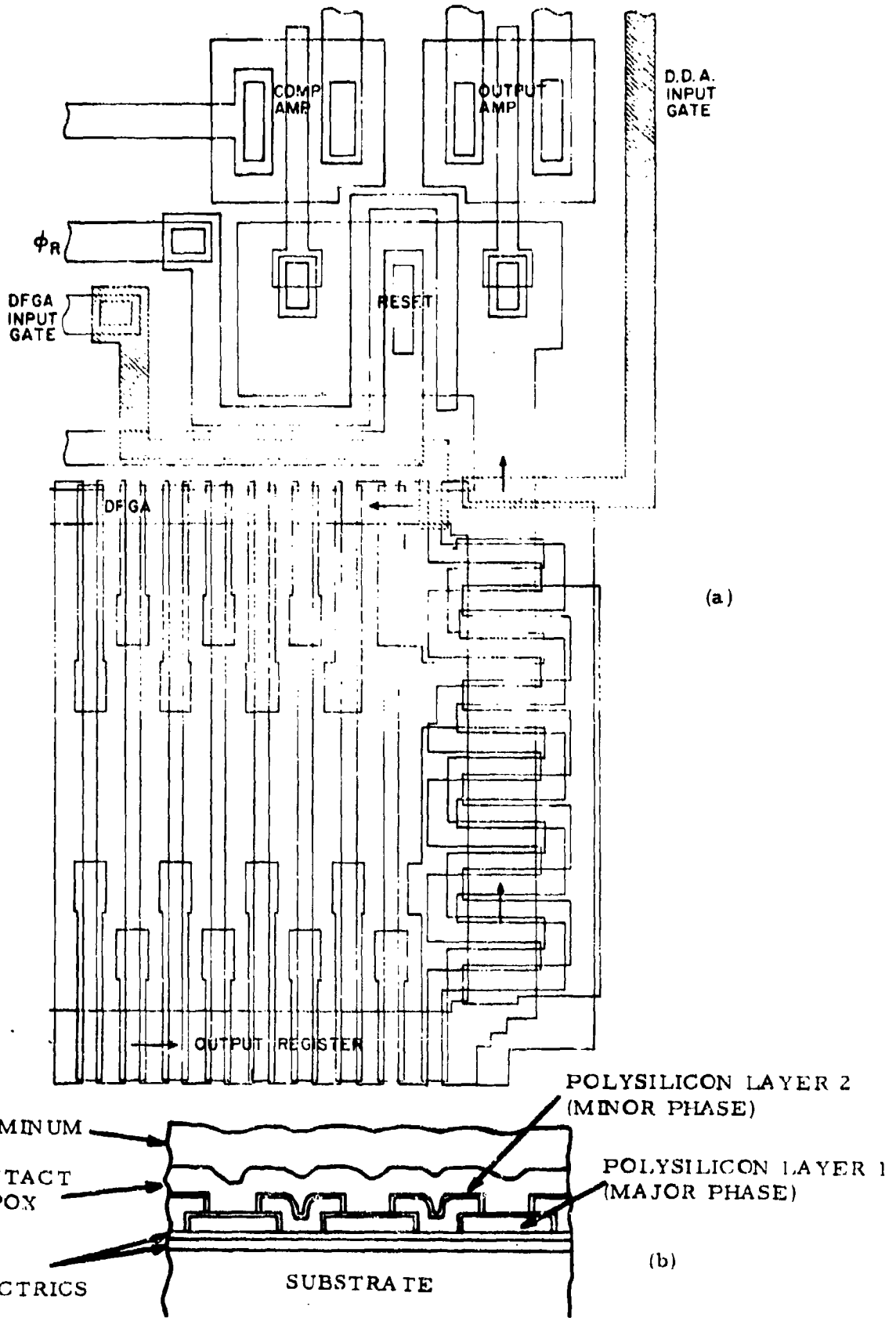


FIGURE 4-33. (a) OUTPUT SECTION OF CCAID-244A AND (b) CROSS-SECTION THROUGH HORIZONTAL GATE STRUCTURE

4.3.1.3.2 Amplifiers

As in the case of the CCAID-100 series, the DDA consists of a MOS transistor signal amplifier and a reset circuit for resetting the amplifier gate after each charge packet has been sampled. In addition, there is a compensation amplifier that does not receive the signal, but is subjected to the same reset transients as the signal amplifier. By taking the difference between the two outputs in an external amplifier, the reset transients can be suppressed.

Figure 4-34 shows a view of the floating-gate amplifier system. Signal packets from the output register are transferred into the floating-gate input channel from the lower right where they are first sensed by FGA1. As they are clocked on down the input channel, they are subsequently sensed by the twelve floating-gate structures associated with the DFGA. Finally, they are detected by another single-stage floating-gate amplifier (FGA2) and then terminated in a sink diode at the end of the channel.

Each of the twelve DFGA floating gates modulates its source-drain MOS transistor region, which injects charge under the large gates shown above the floating gates. This large gate structure is referred to as the DFGA output channel. Here, the amplified charges for each stage are added as they pass through the channel. Charges clocked through the output channel pass a large floating gate,which detects the final signal level and couples it to an output single-stage floating-gate amplifier, designated FGA3. The charge is then terminated in a sink diode. The DFGA MOS transistors are activated by a long gate designated as ϕ_{CG}. Running in parallel to and adjacent with ϕ_{CG} is a second gate (G_{RDC}), which is dc biased to reduce transient coupling from the ϕ_{CG} clock to the output channel.

4.3.1.3.3 Column Anti-Blooming

The CCAID-244A employs an anti-blooming structure at the interface between the area array and the output register. This is a column anti-blooming system, i.e., it permits blooming along a vertical register but is designed to prevent overloading of the output register. As initially designed, the original structure did not function properly; and in all operating 244A devices produced to date the anti-blooming circuit has been inhibited(devices so modified have been designated 244A'). Figure 4-35 (a) shows a typical anti-blooming cell. There are 189 such structures on a device, i.e., one per vertical register. As designed, the cell consists of an n^+ diffusion in the substrate immediately above the last photosite. Between this diffusion and the vertical registers on either side of it are implanted barriers that have the same barrier height as those in the registers. Thus, the threshold for

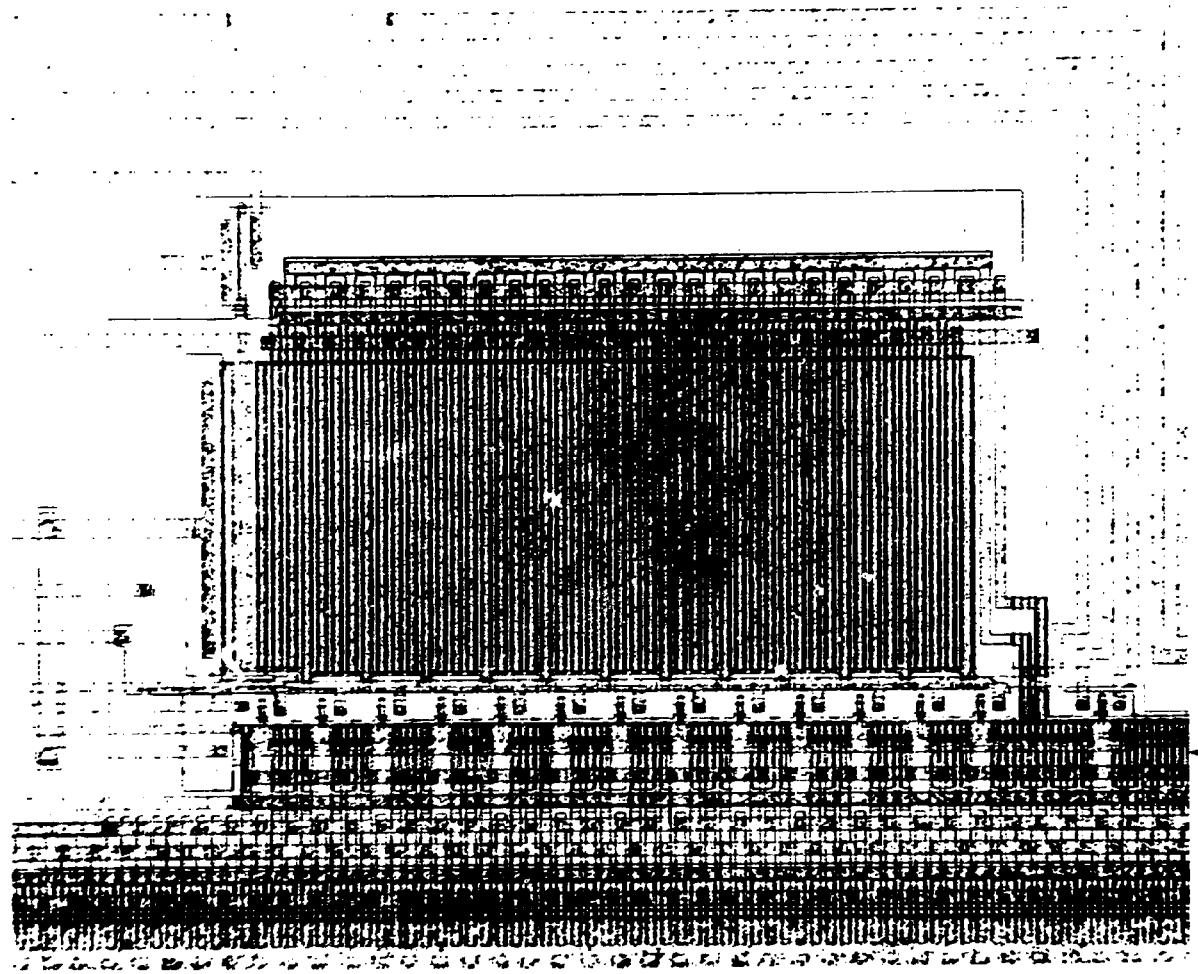


FIGURE 4-34. FLOATING-GATE AMPLIFIER SYSTEM - SHOWING THE THREE SINGLE FLOATING-GATE AMPLIFIERS AND THE TWELVE-STAGE DISTRIBUTED FLOATING-GATE STRUCTURE

75P-381

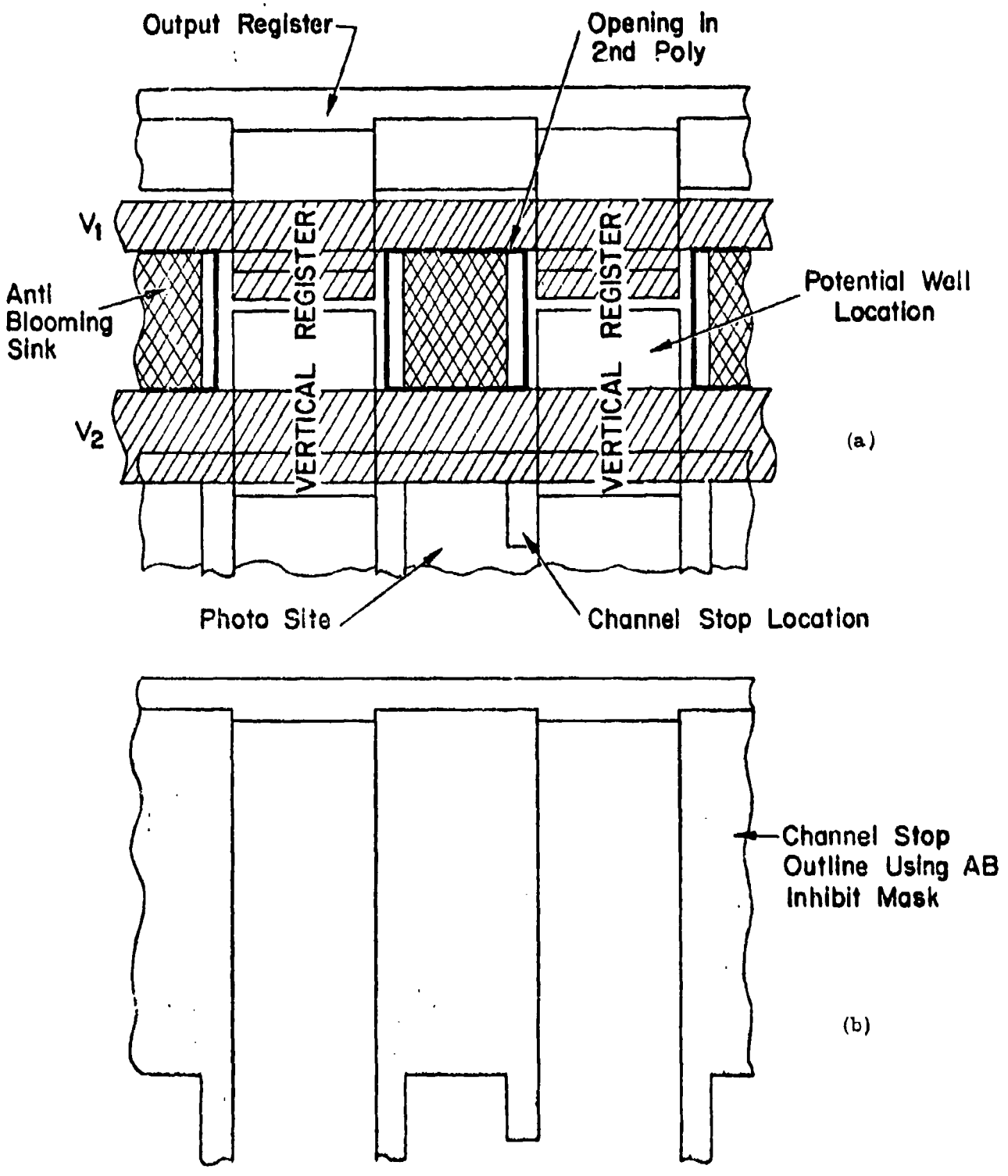


FIGURE 4-35. ANTI-BLOOMING STRUCTURE MODIFICATION (a) Anti-blooming on 244A. (b) Modified channel stop outline when AB inhibit mask is used. The effect of the inhibit mask is to dope the entire anti-blooming structure heavily p-type.

anti-blooming operation is fixed and operates at the point where the vertical register starts to bloom. The problem with the original structure is that a slight misalignment during masking caused the anti-blooming barriers to short out. This structure has been redesigned so that a 2 μm misalignment tolerance exists for all levels. Figure 4-35 (b) shows a channel stop mask option used to permit fabrication of the device without the anti-blooming circuit. Anti-blooming action is inhibited by doping the entire substrate part of the structure with boron.

4.3.1.3.4 Registers

Figure 4-36 shows a view at the opposite end of the array from the output register. The input register is identical to the output register. It contains an output gate and drain, in addition to an input gate and source. The output structure not only serves as an evaluation vehicle for the register but also functions as an overflow sink for excess charge. The horizontal drive lines for the input register are connected to the same bonding pads as are those of the output register, i.e., both registers are constrained to clock at the same rate. Information can be read in at one rate and read out at another only if these are sequential operations.

4.3.1.3.5 Gate Protection

Polysilicon gate protection is employed on most of the 244A gates. This protection system is similar to that used on the CCAID-100 series devices but is designed to operate over a more optimum voltage range. The n^+ mask of the 244A contains a series of gate protection test structures with different gap lengths, to permit a more complete characterization of this system than was previously possible. Figure 4-37 shows the dependence of breakdown voltage on gap length. The gap length used on the 244A is 6 μm, which for the process used yields breakdowns of approximately 40 volts.

4.3.1.4 Clocking

Although the 244A was designed to operate at standard TV rates, a more general clocking system has been employed to evaluate the device. This system provides the needed flexibility of operating over a wide frequency range and under variable drive conditions. Both systems are presented in this section.

The four-phase clocking circuit used for the high speed horizontal registers must drive four sets of gates separately. This circuit is designed to store charge under two sets of gates (major phases), while the other

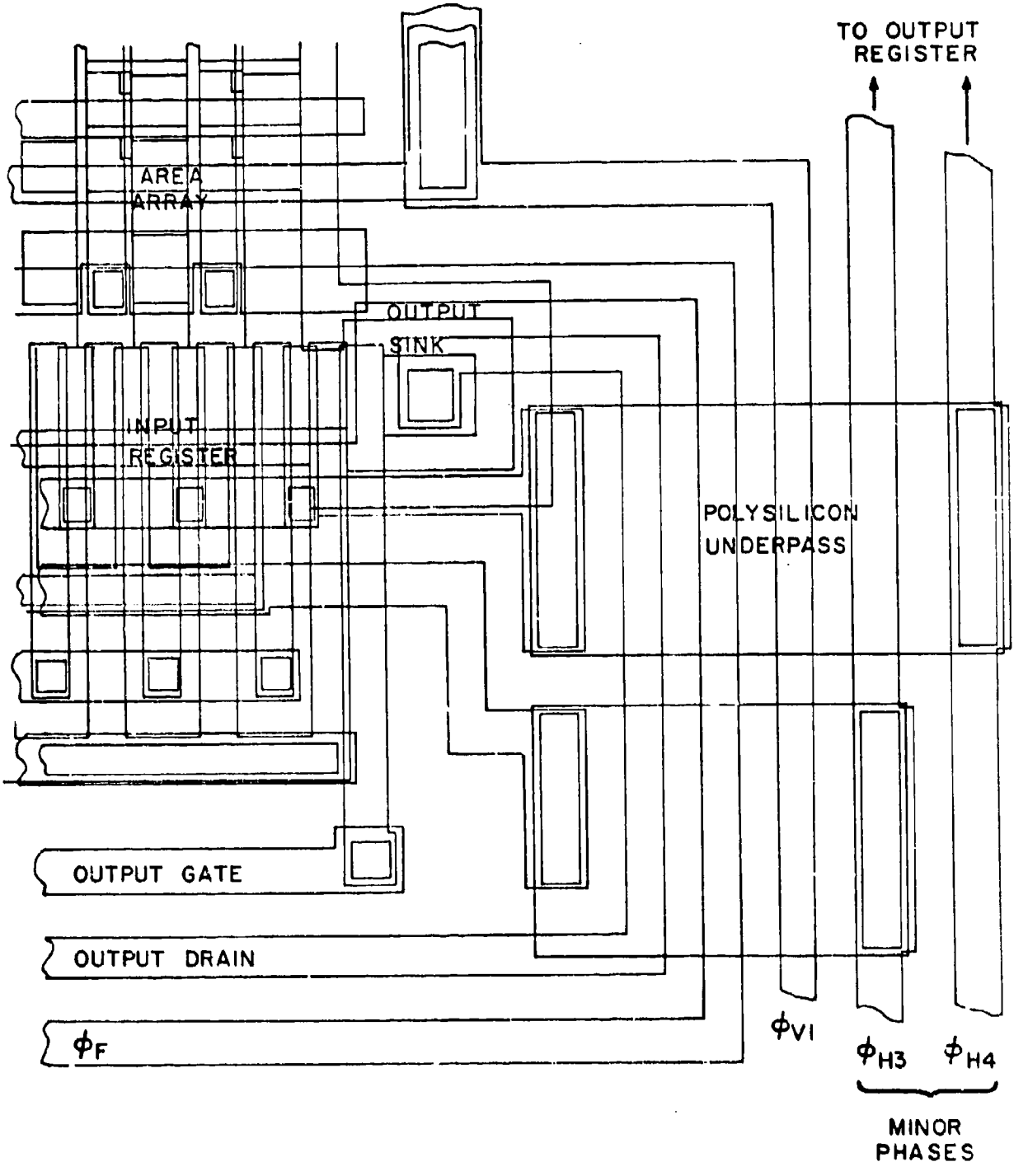


FIGURE 4-36. OUTPUT END OF THE INPUT REGISTER

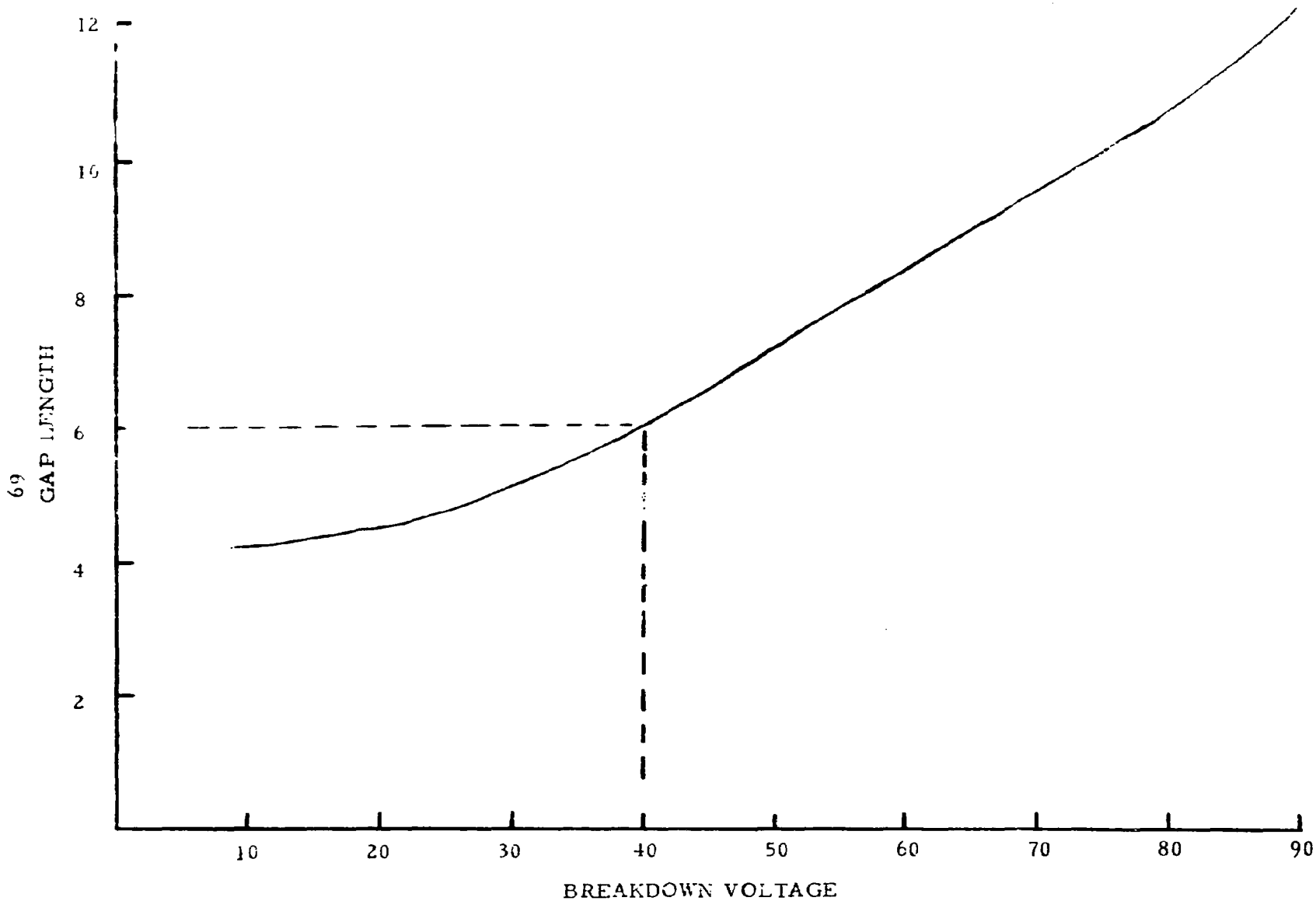


FIGURE 4-37. GATE PROTECTION CHARACTERIZATION CURVE OBTAINED FROM EVALUATION OF 244A TEST STRUCTURES

two sets (minor phases), are used to control charge transfer. The minor-phase gates serve the same purpose as the implanted barrier in the CCAID-100. This structure can then be considered to be a two-phase system where the barrier height is controllable. The bit rate is the same as that of a two-phase system. The gate structure is designed to maximize storage capacity under the two major phases.

In its simplest form, clocking is straightforward. Exisiting two-phase drive systems were readily adapted by adding a driver to each of the two phases as shown in Figure 4-38.

Here, ϕ_{H1} and ϕ_{H2} are the major phases; ϕ_{H3} is the minor phase for ϕ_{H1}, in phase with ϕ_{H1} but at a different voltage level; ϕ_{H4} is the minor phase for ϕ_{H2}, in phase with ϕ_{H2} but also at a different voltage level. Additionally, ϕ_{H2} and ϕ_{H4} are in anti-phase to ϕ_{H1} and ϕ_{H3}.

The input register, output register and DFGA are driven from the same four-phase clocking circuit. While a line of information is clocked out of the array, another line can be clocked in. Since the area array is directional, there is no possibility for undesirable transfer from the area array into the input register.

There are 190 information bits in each horizontal line. The horizontal output register receives 190 pulses for each clock phase plus an additional number to process the information through the output section. The longest path is that through the amplifier connecting channel and the DFGA input channel. There are 24 transfers for each phase in the DFGA channel and 19 in the connecting channel. The total number of high speed transfers for each phase is, therefore, 190 + 43 = 233.

For a horizontal clock rate of 7.16 MHz, the element time is 140 nsec; thus the high speed sections are emptied in $140 \times 10^{-9} \times 233 = 32.6$ μsec. Since the horizontal interval is 63.5 μsec, the inactive time is 30.9 μsec.

When the same horizontal clock is used for the input register, 233 transfer pulses must be employed although only 190 gates are involved. Therefore, information is inserted after 43 clock pulses have occurred.

In the vertical register, there are two extra vertical gates at the output register to allow incorporation of the anti-blooming circuit; at the other end, there is one additional vertical gate necessitated by the presence of the input register. To do this, 246 pulses are required to empty the vertical register. The vertical clock rate is 15.75 KHz for a scan time of 15.6 msec/field and a vertical inhibit time of 1.07 msec (60 Hz field rate).

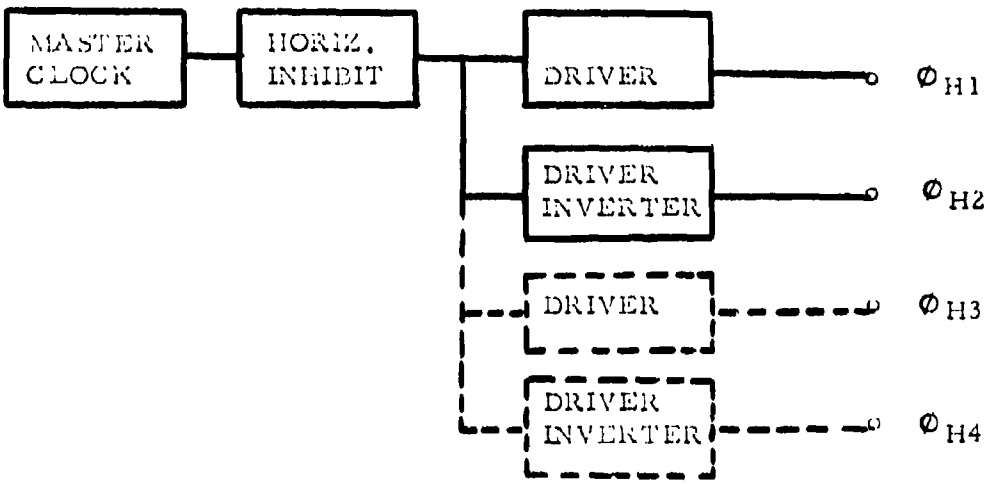


FIGURE 4-38. ADAPTATION OF TWO-PHASE CLOCK SYSTEM TO FOUR-PHASE. Phases 3 and 4 are of equal phasing and width as phases 1 and 2 but of higher voltage amplitude.

Figure 4-39 shows the circuit for a variable frequency clocking system. The master clock is an external generator that operates at 4 times the CCD bit rate. Its output goes to a frequency divider T_1, which produces outputs at 1/2 and 1/4 the master clock rate. The CCD bit generator contains the logic necessary to generate the minor phases of the input and output registers, and ϕ_{CG} for the DFGA. The logic for the vertical registers and photogates are derived in the vertical interval generator and frame interval generator, respectively. The vertical pulse train is fed to T22, a multiplexer, which is activated by the output of T21 to inhibit the vertical pulses and insert transfer pulses as required. Figure 4-40 shows a timing diagram for the circuit. Two hundred and sixty CCD bit pulses are generated, 40 more than the minimum needed to empty the output register. During the horizontal inhibit period, all horizontal phases except ϕ_{H1} are kept low until the next line of video has been transferred in from V_1, which is also low at this time. One hundred and twenty-eight vertical pulses are generated per field; one hundred and twenty-four are needed as a minimum.

The horizontal clocking shown in Figure 4-40 is a variation of the modified two-phase system discussed previously. Here, all four phases are of the same voltage amplitude; the phase relationships are adjusted to produce the required potential profiles in the device, as shown in Figure 4-41. This method, in principle, provides more optimum operating conditions for the DFGA because both phase gates on either side of the floating gates can be kept low while the floating-gate charge is being detected. However, this clocking method at very high frequencies places more stringent rise-time requirements on the minor phases than does the conventional system. For example, at 7.16 MHz the pulse width of a minor phase of a 4-phase system is 35 nsec, which dictates rise and fall times of 10 nsec. It is difficult to find low dissipation drivers with 15 to 20 volt swings for this kind of transient response.

Charges are transferred from the area array to the output register during the horizontal inhibit interval. Two methods for accomplishing the transfer were evaluated initially. These are shown in Figure 4-42. The method selected depends on the implant mask option used in building the device under test. Devices made with a No. I mask do not have a barrier between the area array and output register. In order to prevent charges in the output register from spilling back into the area array, the vertical clocking used must differ somewhat from that employed on the CCAID-100 series devices. Although runs made with a No.II mask may be clocked similar to the CCAID-100 series devices, these devices do not have a self-aligned barrier between the photogates and the vertical registers. Since successful operating units were made using the No. I mask and since this is the preferred one, the No.II option has been abandoned.

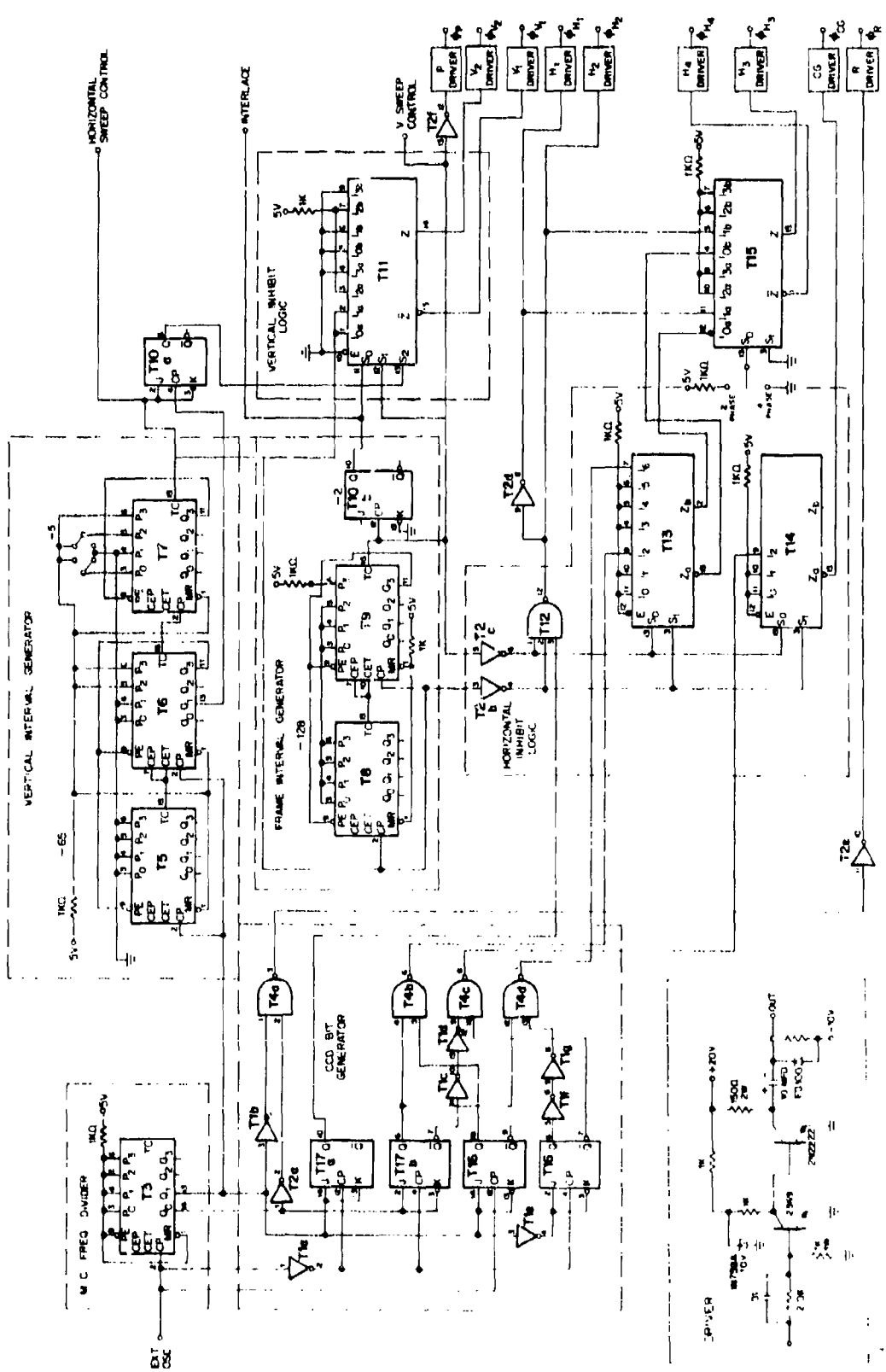
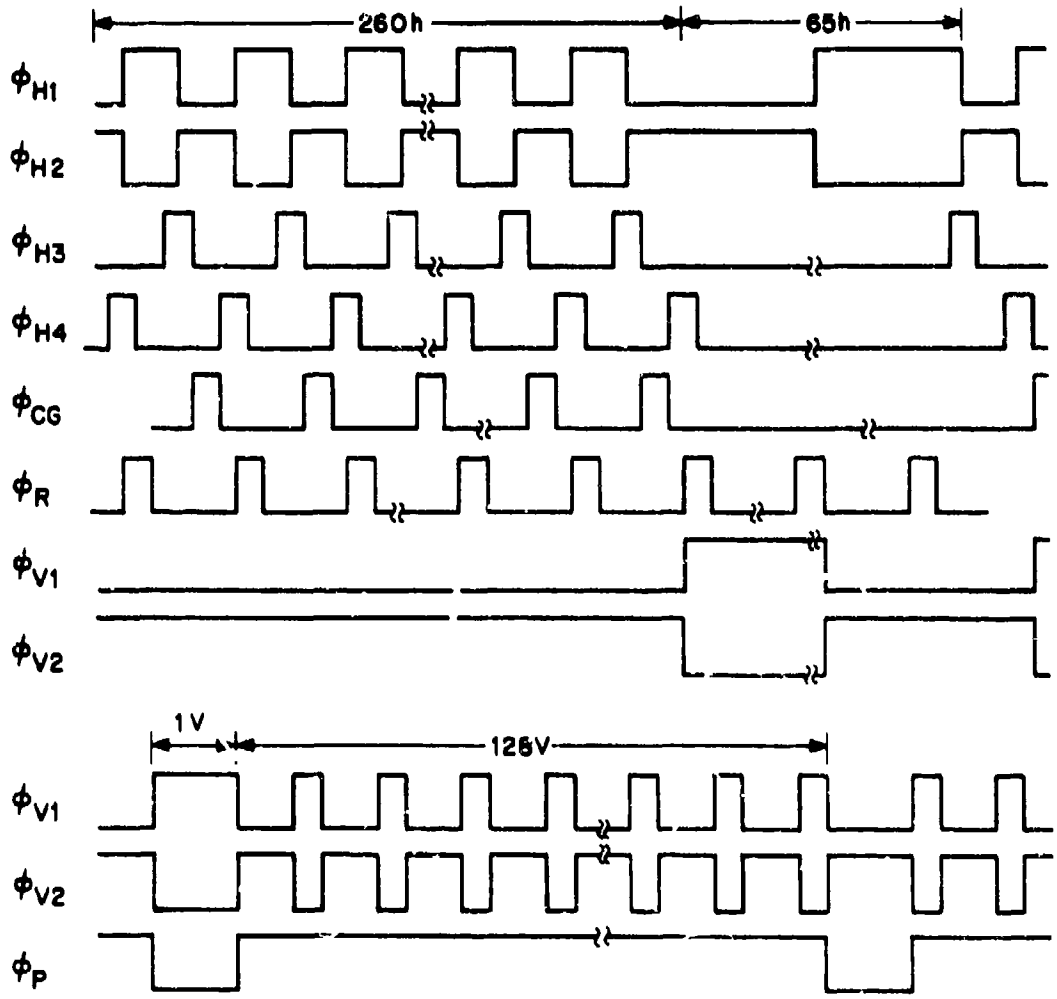


FIGURE 4-39. VARIABLE FREQUENCY DRIVE CIRCUITS FOR CCAID-244



For 2ϕ Operation, ϕ_{H1} and ϕ_{H3} are in Phase; also ϕ_{H2} is in Phase with ϕ_{H4}

FIGURE 4-40. VARIABLE FREQUENCY CLOCKING FOR 244A (4 Ø)

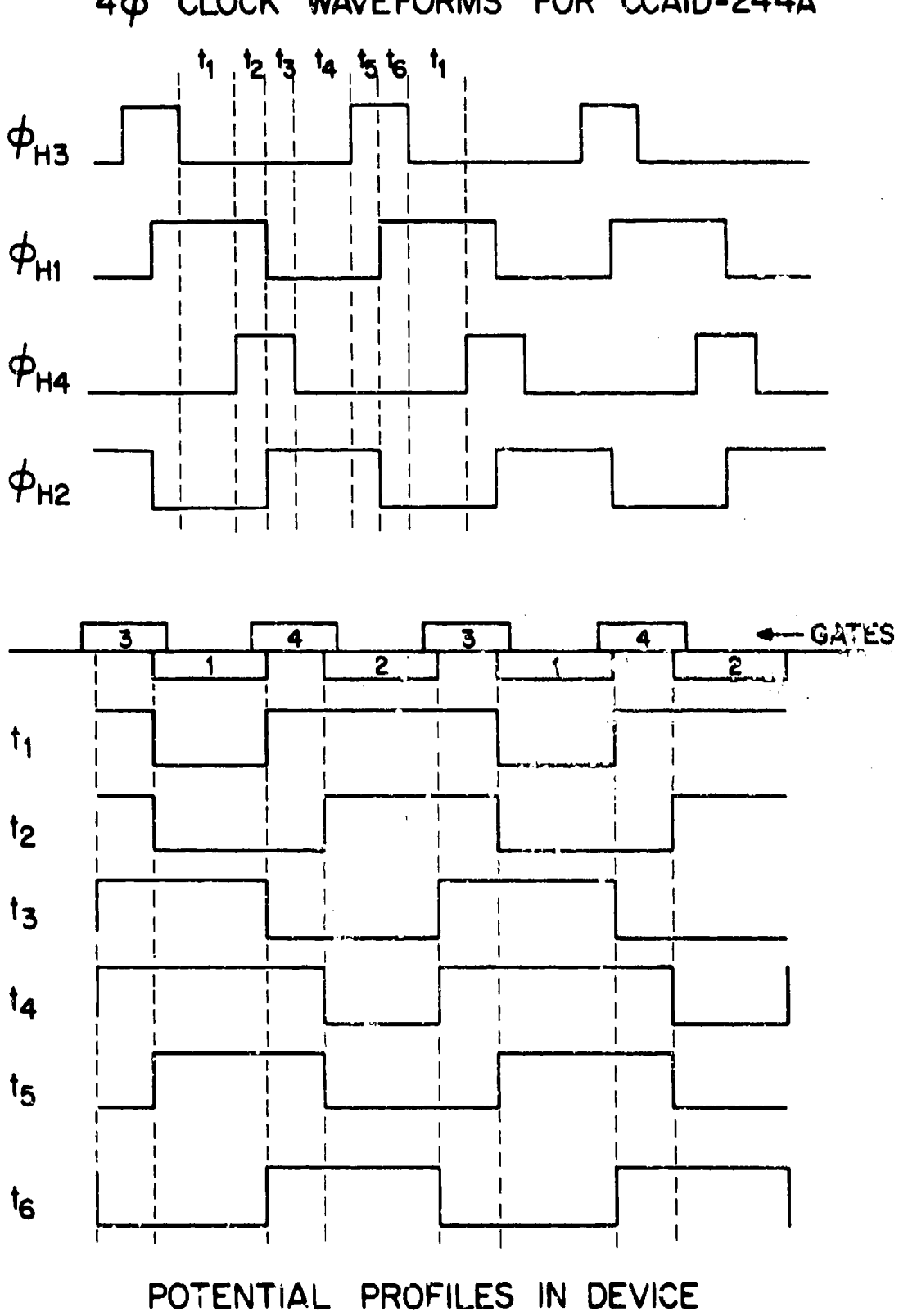


FIGURE 4-41. CLOCK WAVEFORMS AND POTENTIAL PROFILES FOR CCAID-244A

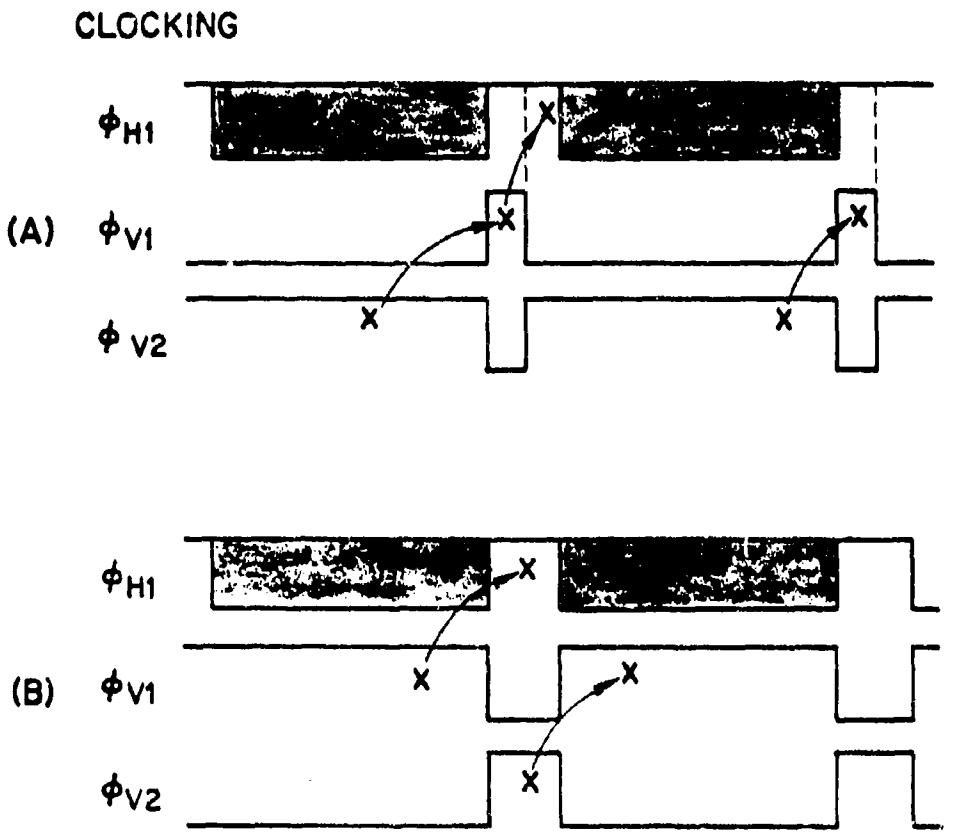


FIGURE 4-42. CLOCKING METHODS CORRESPONDING TO BARRIER IMPLANT MASK OPTIONS. (A) for "I" mask; (B) for "II" mask.

Figure 4-43 shows a fixed frequency timing diagram compatible with the Fairchild 3261 sync generator and capable of operating with a standard TV receiver. Wave form (1) is the vertical drive output from the sync generator used to generate the vertical sweep. Wave forms (2) and (3) are sync generator outputs used to identify the start of odd and even fields. These are added in external circuitry to generate ϕ_p, the CCD photogate pulse, wave form (5). Composite blanking, wave forms (4) and (9), is also available from the sync generator. The CCD horizontal pulses, (10) and (11), are started at some time after each horizontal blanking pulse ends to center the image on the monitor. The CCD vertical pulses (6) and (7), are similarly delayed in order to center the picture vertically.

A circuit implementation of this timing sequence is shown in Figure 4-44. The master clock (MC) frequency divider is driven by a 28.636-MHz crystal oscillator for NTSC clocking. The CCD bit generator generates the high speed CCD pulses at 7.16 MHz. The line start and stop timer circuits, and the field start and stop timer circuits are responsible for the picture centering mentioned above.

The inhibit circuits are used to control the start and stop time of the horizontal and vertical pulses and also to insert transfer pulses where necessary. The drivers provide the positive and negative swings necessary to drive the 244A. They are capable of operating to 10 MHz.

4.3.2 Device Performance

4.3.2.1 Performance Objectives

The following specifications were established as initial objectives:

Type of Readout	2/1 interlace
Readout Rate	3.58 x 2 = 7.16 M bits/sec
Format Aspect Ratio	4 (w) x 3 (h)
Number of Photoelement Rows/Frame	244 (Note 1)
Number of Photoelements/Row	190 (Note 1)
Saturation Charge Level	5×10^5 electrons/cell
Cell Size	18 um x 30 um
Format Size	0.202" (w) x 0.154" (h) (Note 1)
Frame Rate	1/2 Field Rate
Field Rate	59.95 Hz
Line Rate	2/455 x chroma subcarrier 15,734 Hz

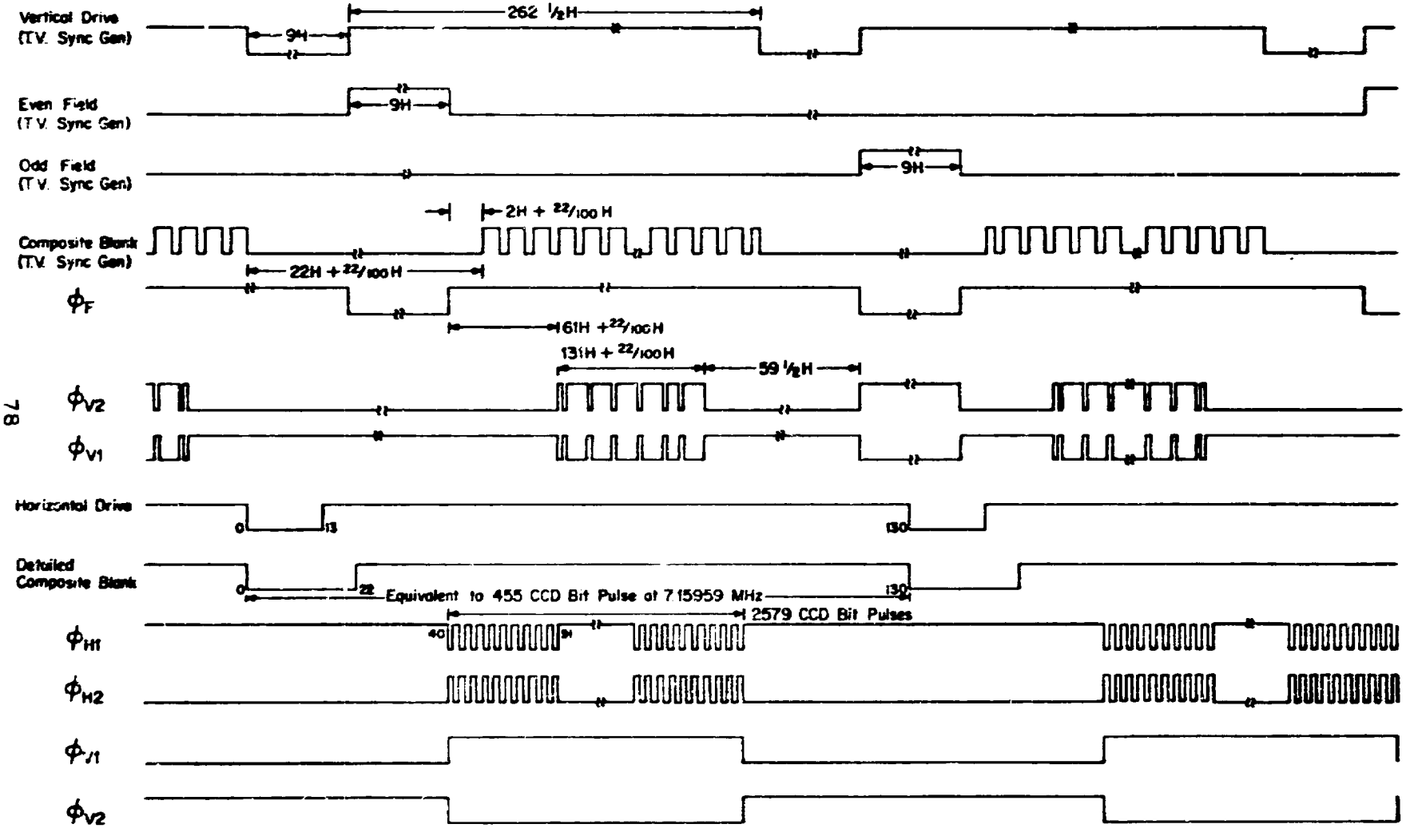


FIGURE 4-43. TIMING DIAGRAM FOR FIXED FREQUENCY CLOCK SYSTEM

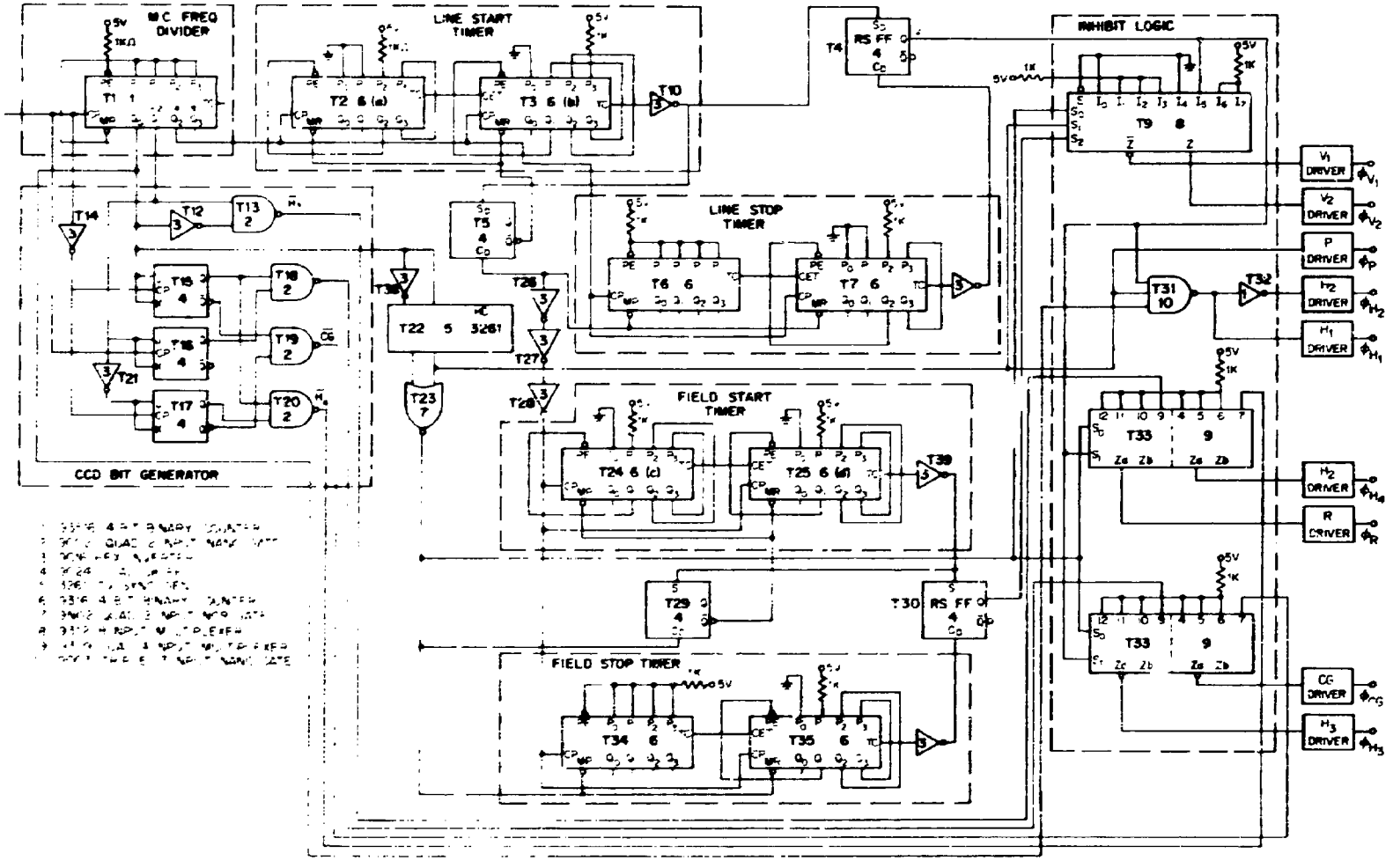


FIGURE 4-44. FIXED FREQUENCY DRIVE CIRCUITS FOR CCAID-244

On-Chip Amplifiers	Dual-gate Differential (DDA) and DFGA
Dark Current	4 nA/cm^2; 0.026 pA/sq. mil at 25°C
Sensitivity (NES)	10 to 40 electrons with DFGA and device cooling

Note 1: Characteristic based on scale factor of 1/2 applied to a full-frame NTSC compatible CCAID design. Future full-frame chip to have 486 element rows/frame, with 378 elements/row, with 0.306" x 0.402" format size.

Beyond this initial definition, other mutually agreed upon requirements were incorporated during the initial device design phase. Floating-gate amplifiers were added at each end of the DFGA input channel primarily for the purpose of facilitating DFGA evaluation. An electrical input register was added to increase device utility and to facilitate electrical testing. A column anti-blooming structure was also incorporated.

In the latter stages of the program, minimum standards were established for cosmetic quality, and a slightly revised minimum criterion for low-light-level sensitivity was defined. The cosmetic standard was proposed after it became obvious that defects were a major problem on a device this large. The low-light-level requirement was that low-light-level images down to 40 electrons be detected. Implicit in such a requirement was that the DFGA output be used and the device be cooled.

4.3.2.2 High-Light-Level Imaging Results

The major performance objectives have been met. A number of runs have yielded devices with good low-light-level area imaging capability at clock rates in excess of the 7.16 MHz design rate. Figure 4-45 shows images from the DDA output of an array clocked at 7, 10 and 20 MHz. These are high-light-level room-temperature images. Even at the highest frequency, horizontal drifting that is characteristic of poor transfer efficiency is not present as the light level is lowered.

Typical DDA saturation output voltage (V_o) on units fabricated to date is 10 mV across a 1 K source resistor (Rs). Assuming gm = 0.6 mmho, the voltage at the amplifier gate (Vg) is:

$$V_g = V_o \left(\frac{1 + gm\ Rs}{gm\ Rs} \right) = 27\ mV$$

CLOCK RATE

7 MHz

15 MHz

20 MHz

FIGURE [illegible] CAID-244A DDA IMAGES

The total capacitance at this node is approximately 1 pF; then

$$q_{SAT} = 1 \times 10^{-12} \times 27 \times 10^{-3} = 0.027 \text{ pC}$$
$$\approx 1.7 \times 10^{5} \text{ electrons}$$

Based on the potential-well area in the CCD registers and photosites, the projected saturation level for 2.5-volt barriers is 3.28×10^5 electrons. The difference between the actual and projected values is apparently caused by a slightly lower barrier height than designed. On a few devices, however, output signals of 30 mV were found, which is slightly in excess of the design value.

Figure 4-46 shows images from a device illustrating outputs obtained from the DDA, FGA1 and the DFGA. The clocking rate for this series of pictures was 10 MHz; the ambient temperature was +25°C. At high light levels, characterization has centered around image-defect evaluation. Both material and process factors were major contributors to defects. Material-oriented problems manifest themselves as dark-current spikes. Each spike is usually confined to a single photosite. Such spikes are frequently so numerous that they become a major limitation to imaging at very low light levels. Figure 4-47 illustrates some of the dark-current patterns observed. These types of defects are commonly associated with stacking faults in the silicon wafers. The faults become locations for precipitated contaminants that can act as dark-current generators. The faults need not be caused by surface damage; they can also occur during crystal growing. In particular, they have been noted during the growth of float-zone material and tend to form swirls not unlike that shown in Figure 4-47. Whatever their origin, the effect of the stacking faults can be minimized by gettering the contaminants. The 244A process employed phosphorus bulk gettering. It was, however, introduced at an early stage in the process sequence because the high temperature cycle involved required that it be performed before the transport gate structure was formed in the undoped polysilicon. There is also strong evidence that no significantly high temperature process should be performed after the gettering operation. A successful low temperature bulk gettering process has been developed more recently and is being employed as the last process before metalization.

In addition to dark-current spikes, many devices had a lower dynamic range at 25°C than was expected. This was caused by a high, uniform, dark-current level, which resulted in room temperature dynamic ranges of approximately 100:1. When the devices were cooled to below -10°C, values of 1000:1 or more were measured.

DDA

FCA

DFCA

FIGURE 4-46. CCAID-244A DDA, FCA AND DFCA IMAGES

75P-390

FIGURE 4-47. DARK-CURRENT PATTERNS ON 244A DEVICES

75P-380

The dark-current collection area in a photosite is 234 μm^2. Assuming a dark current density of 10 nA/cm^2, each photosite generates 2.34×10^{-14}A of dark current at room temperature. The integration time used for the measurements was 33 msec (30 frames/sec). The average photosite dark charge is then:

$$q_{DARK} = 2.34 \times 10^{-14} \times 33 \times 10^{-3} = 7.7 \times 10^{-16}C$$
$$= 4.8 \times 10^{3} \text{ electrons}$$

This yields a photosite dark-charge noise limited dynamic range of

$$\frac{q_{SAT}}{\sqrt{q_{DARK}}} \qquad \frac{1.7 \times 10^{5}}{69} = 2460:1$$

Extrapolation of the observed dark-current values from 25°C to lower temperatures indicates that such devices would have to be cooled to approximately -20°C to obtain a dynamic range of 1000:1. This was verified by cooling experiments. Recent experimental work indicates that this uniform dark current is caused by fast surface states that are normally eliminated by a hydrogen anneal. It is not effective on the 244A because of the large silicon nitride area that acts as a barrier to the hydrogen. Longer annealing cycles are being evaluated.

Another major source of image defect is physical defects in the structure created during fabrication. These may be divided into two categories, those caused by defects in the photomasks and those caused by imperfect processing. A correlation can readily be established between the defects in photomasks and the corresponding defects on wafers. The incidence of such defects is high. Figure 4-48 shows images from devices in wafer form where the image was a light spot incident on each die. In each case, a selected image defect is traceable to physical defects on the corresponding die. For the examples shown, the physical defect gave rise to open gates that drive the vertical shift registers. Either to the right or left of the open gate, all shift register sites in the row affected become inoperative. Vertical line defects are also common and are normally caused by open gates in the output register.

Though defects at any mask level can cause image defects, defects in some layers are more detrimental than others. Mask No. 3, for example, is critical because it defines the polysilicon photogates; the structures that integrate carriers for the longest period. Protrusions from the polysilicon photogate into the adjacent vertical register are especially detrimental. Mask No. 6 defines the transport gates for the registers. There are 244 such gates in the area array; each is 225 mils long and 0.4 mil wide.

As indicated in Figure 4-48, such defects usually produce image defects beyond the locale of the device defect and often affect entire lines or picture segments. Strong emphasis is being placed on upgrading current photomask quality and the photomasking techniques that ultimately degrade them.

4.3.2.3 Performance of the Input Register

A limited characterization was performed on the input-register structure. The primary objective was to confirm that it functioned and to evaluate its linearity. A view of this structure is shown in Figure 4-49.

Best results were obtained by biasing the input source with dc while the input gate was clocked. The input gate transfers minority carriers from the source to a region under the first horizontal phase electrode, in this case a Φ_{H2} gate. The best way to accomplish this is to keep Φ_{H2} continuously in a high state during the input gate excursion. The input gate pulse should, therefore, start high after Φ_{H2} is made high, and drop low before Φ_{H2} goes low. In this way, the charge transferred in is solely a function of the input gate voltage and is not influenced by transient conditions. In addition, the possibility of reverse transfer when Φ_{H2} goes low, is avoided.

In order to operate the input and output registers simultaneously, the usual imaging mode clocking must be slightly modified. The wave forms shown in Figure 4-50 enable simultaneous transfer to be made from the input register to the area array and from the area array to the output register. Imaging can also be performed with this clocking by adding a small amount of external circuitry.

Figure 4-51 shows the relationship between input gate voltage and output voltage from the DDA. Beyond the 50% point in the DDA output, linearity becomes poor. Input structures with improved linearity exist and are being incorporated on more recent Fairchild devices.

4.3.2.4 DFGA Image Sensing at Low-Light Level

The low-light-level image-sensing performance of the CCAID-244A, with the DFGA structure described in Appendix A, was the central issue in determining the technological validity of this second phase effort of the program. This section contains a complete description of the experimental determination of this low-light-level imaging capability. The results of these experiments showed that a bar-pattern image could be sensed with this device at a signal level of 33 electrons per CCD pixel. The noise equivalent signal (NES) was determined to be 23 electrons per pixel.

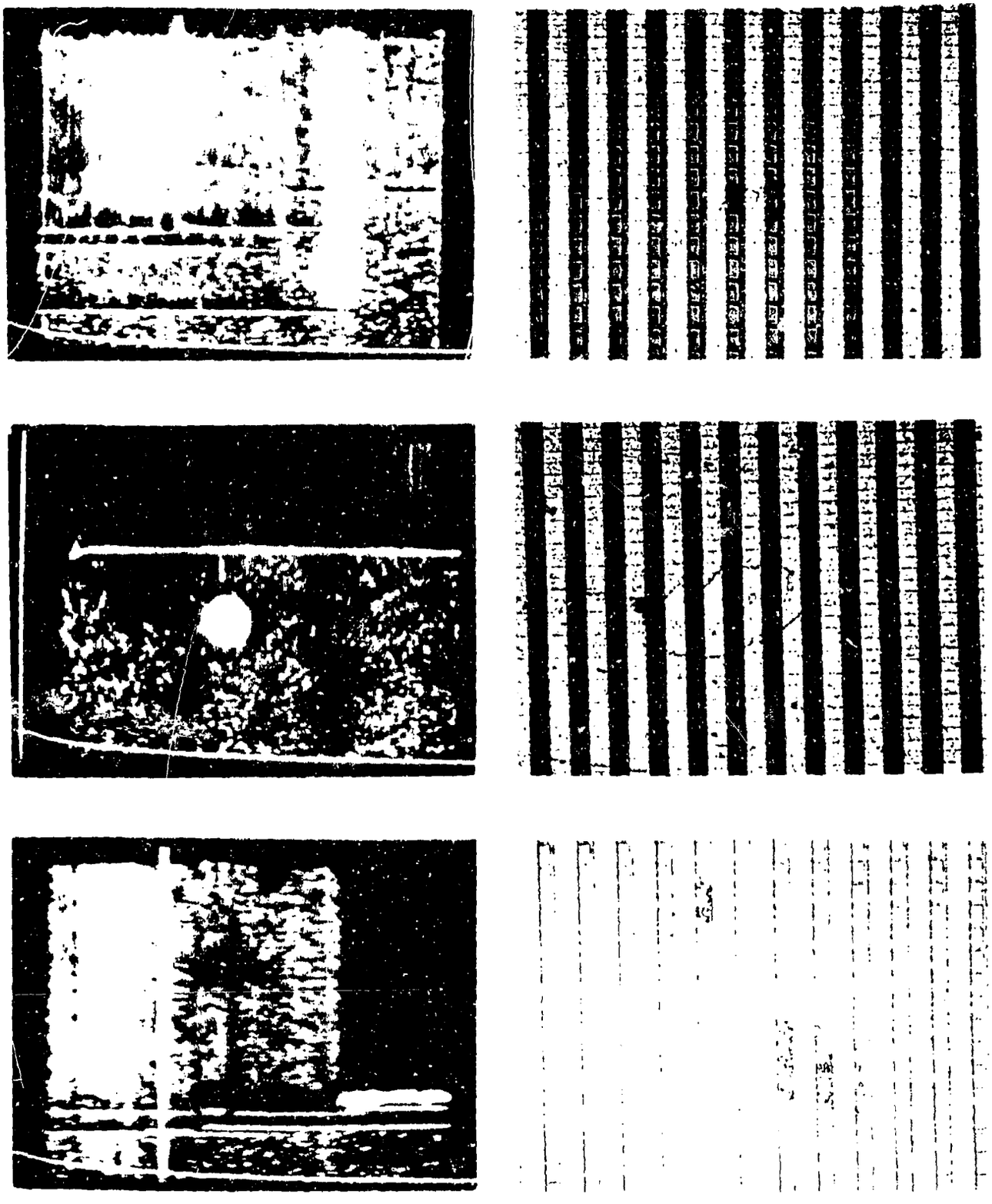


FIGURE [illegible]. IMAGE DEFECTS (LEFT) CAUSED BY PHYSICAL DEFECTS (RIGHT)

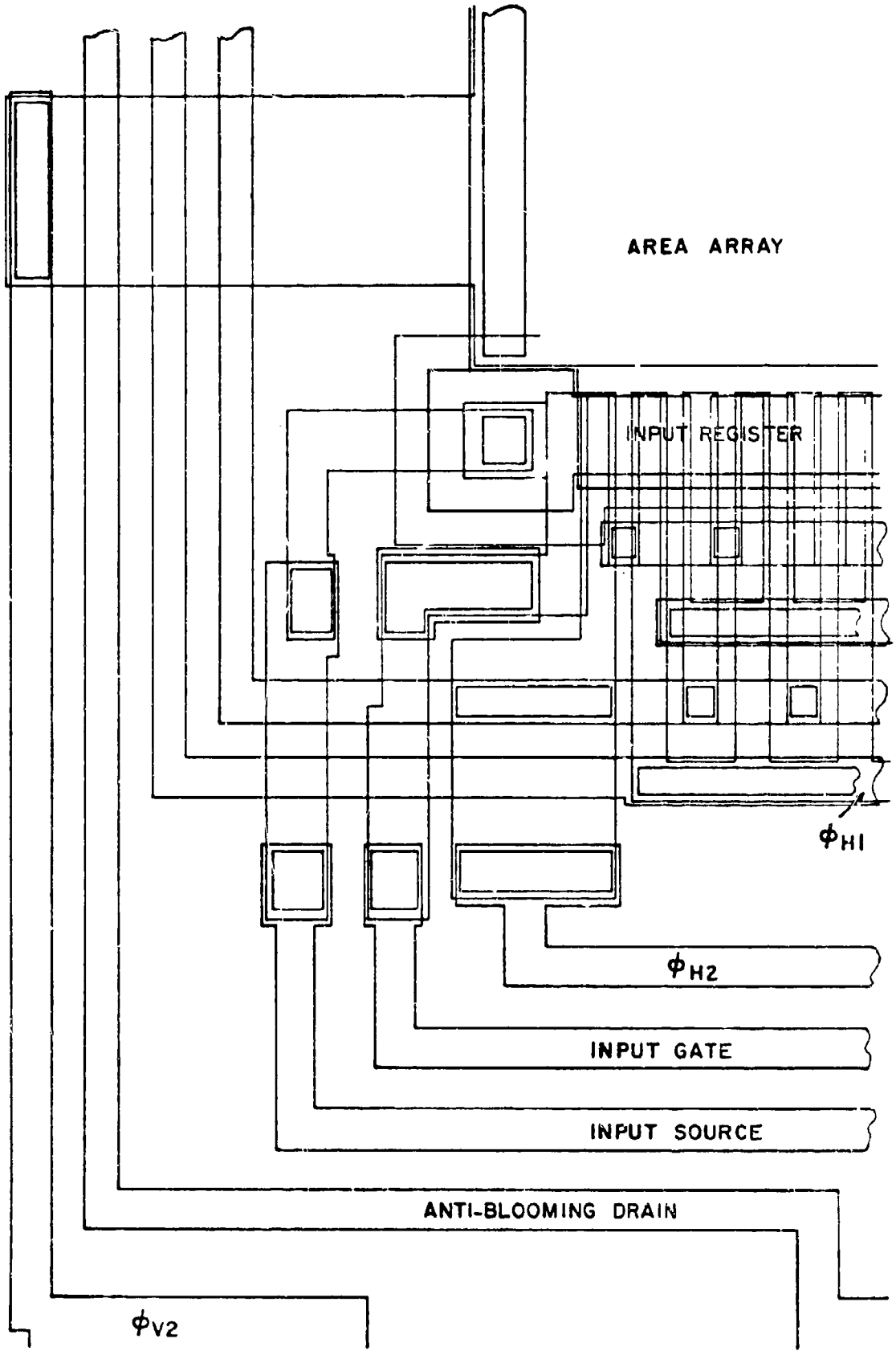


FIGURE 4-49. ELECTRONIC INPUT STRUCTURE

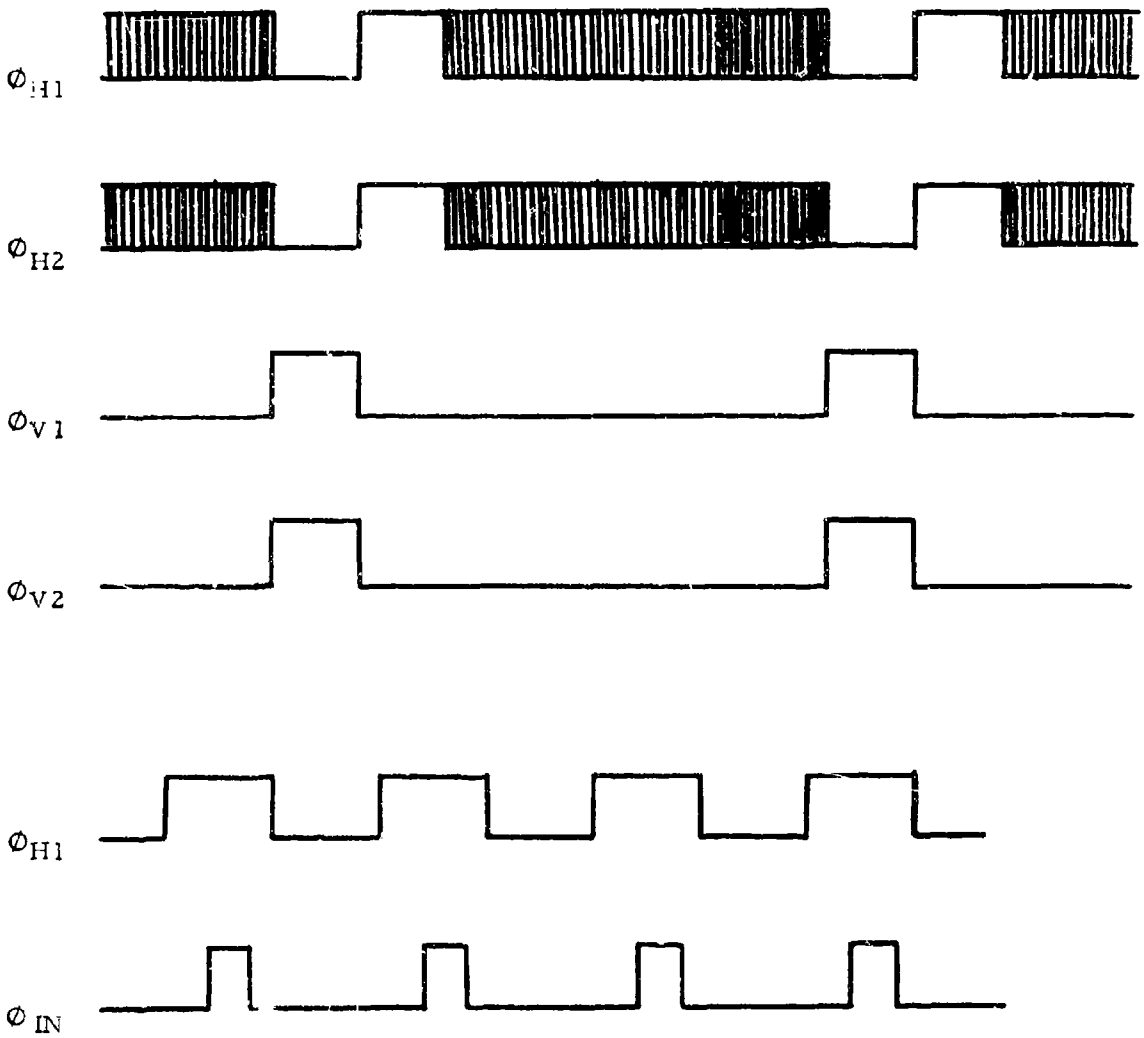


FIGURE 4-50. MODIFIED CLOCKING FOR SIMULTANEOUS TRANSFER FROM INPUT REGISTER TO OUTPUT REGISTER

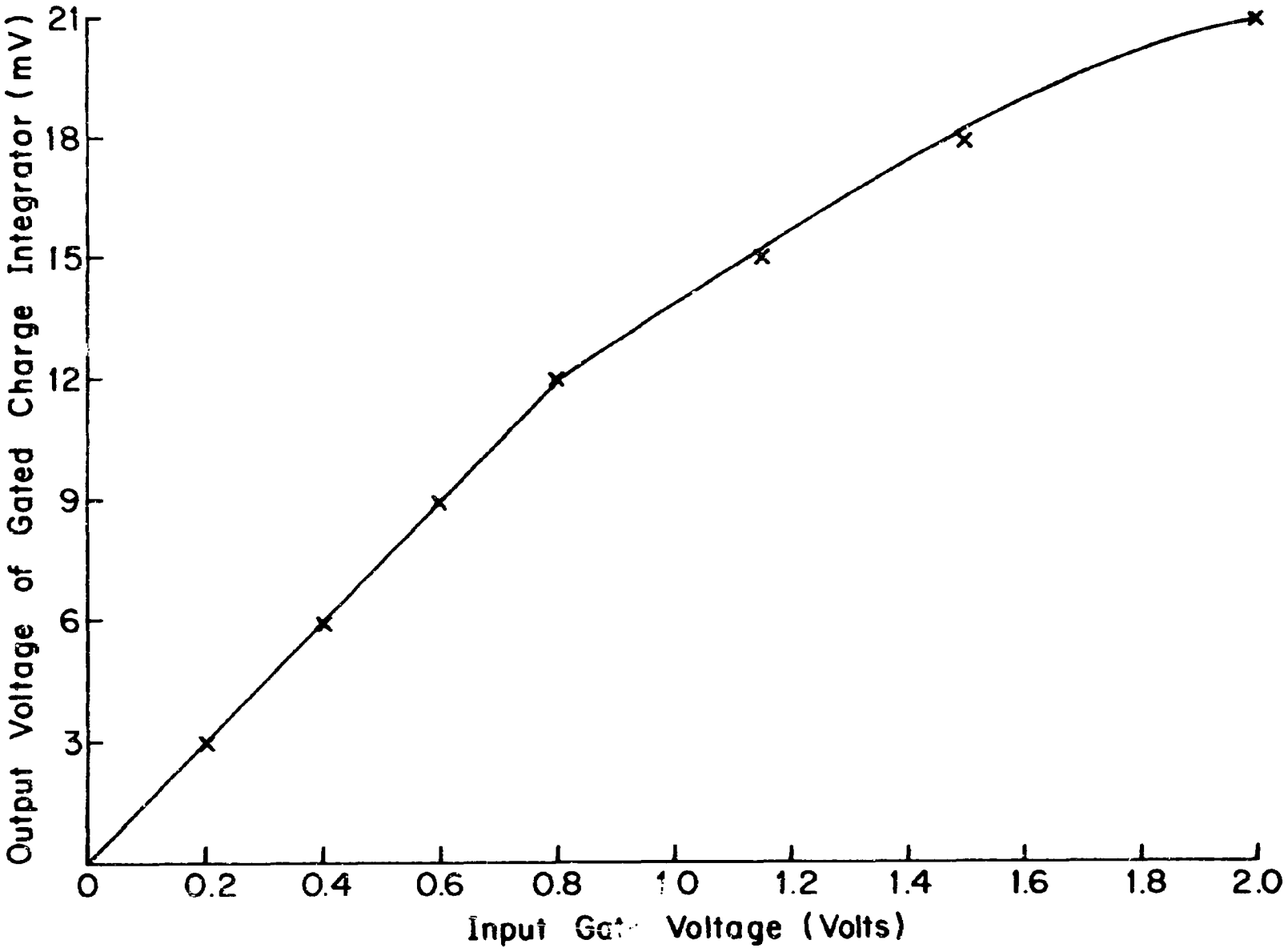


FIGURE 4-51. INPUT GATE VOLTAGE VS. DDA OUTPUT VOLTAGE

In these experiments, considerable attention was given to the determination of the 33-electron minimum detectable signal, the 23-electron NES from noise data, and the uniquely non-linear transfer characteristic of the DFGA, which extends to low signal levels. The latter characteristic was found to be consistent with independent measurements for another DFGA of the same gain at low signal level.

The following paragraphs describe (1) the characterization of parameters related to the interpretation of experimental results, (2) the test equipment and test procedures utilized, (3) the experimental results, and (4) comparisons of predicted and measured results.

4.3.2.4.1 Characterization of Related Parameters

1) Saturation Phenomena

In the process of calibrating the low-light-level (L^3) imaging system, it is essential to be able to detect any of several saturation processes in the device. These processes are: photoelement saturation, vertical register saturation, input register saturation at the DFGA, and DFGA output-register saturation. Table 4-7 presents measured and calculated parameters related to these saturation processes. With increasing light level, photoelement saturation occurred first in most units; in some, vertical register saturation. Photoelement saturation was typically 1 to 1.5×10^5 electrons; for some units is was as low as 7×10^4 electrons.

2) Blemish Level at High Gain

At the high system gain levels required for L^3 imaging, only a small number of units were available with uniform imaging performance over even a limited area. Units were selected with an area of approximately 25 percent of the raster area which was free of large blemishes. These units also had to be sufficiently uniform in photoresponse over the full raster to perform a meaningful photocurrent calibration.

3) Dark Current Density at 25°C

The total dark-current density for the selected units, averaged over the full array, ranged from 15 to 40 nA/cm^2.

TABLE 4-7

SATURATION LEVELS AND RELATED PARAMETERS OF THE CCAID-244A

Parameters	Value	Notes
Photosensor Parameters		
Saturation charge density	~ 6000 el/μm^2	1
Well area after diffusion	60 μm^2	2
Saturation level, calculated	3.6×10^5 el	
Saturation level, measured	0.7 to 1.5×10^5 el	3, 7
Vertical Register Parameters		
Implanted barrier potential	2.8V	4
Saturation charge density	3250 el/μm^2	5
Well area after diffusion	82 μm^2	2
Saturation level, calculated	2.7×10^5 el	
Saturation level, measured	~ 1.5×10^5 el	6, 7
DFCA Input Register		
Saturation level, measured	~ 3×10^5 el	

Notes:

1. Calculated from the active buried-channel n-implant dose with the assumption that the n-type layer is 90% neutral at saturation.
2. Measured on a few typical samples.
3. Photosensor saturation is observed when a small light spot blooms as a vertical line of full picture height.
4. Measured.
5. Calculated from the barrier potential and the capacitance per unit area.
6. Vertical register saturation is observed when a small light spot blooms as a vertical line a few picture elements in length.
7. The differences between calculated and measured saturation level is primarily due to larger than anticipated lateral diffusion of channel stops.

The average dark-current density in the selected areas used for L^3 imaging was estimated to be in the range 5 to 15 nA/cm^2.

4) Floating-Gate Responsivities

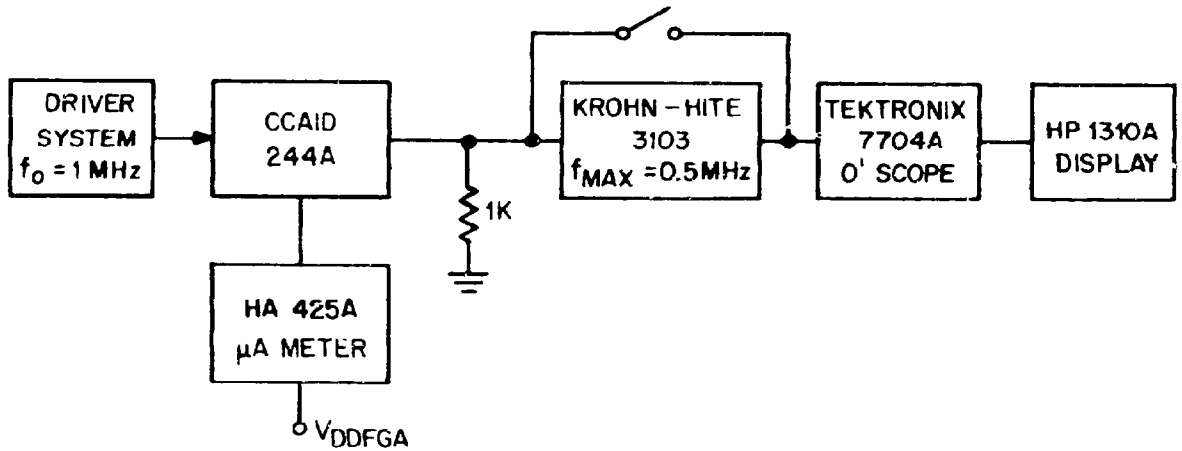
The floating-gate responsivities of the two FGA's and of the individual input amplifiers of the DFGA were designed to be equal. Estimates of this responsivity were obtained for several of the units used in the L^3 imaging tests. The FGA1 and FGA2 amplifier output responsivities for these units were found to be in the range of 0.2 to 0.35 μV/electron. The higher values were obtained where it was possible to apply the full 15-volt drain bias specified by the design, and where a relatively large source resistor was used, namely 4.7KΩ. The lower values were obtained where it was necessary to limit the drain bias because of low breakdown voltage or excess noise. In all cases, the estimated responsivities at the floating-gate electrode were in the range of 2 to 3 μV/electron.

4.3.2.4.2 Test Equipment and Procedures

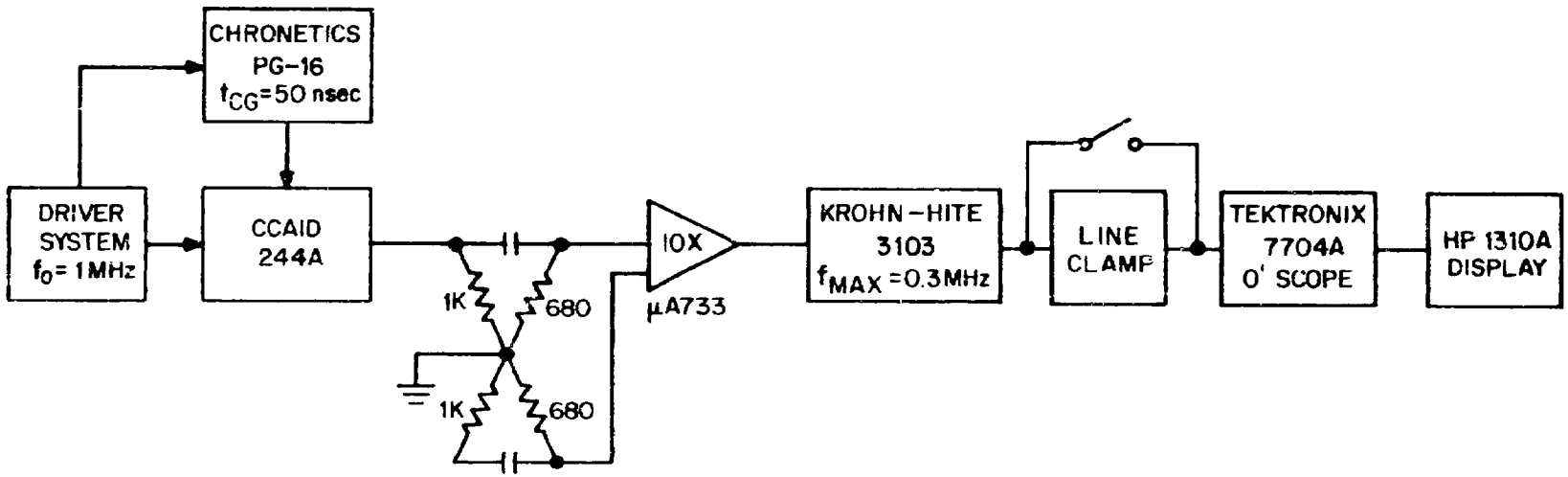
1) Test Equipment

Figure 4-52 shows two block diagrams of the video output circuitry used in the L^3 imaging experiments; the first was used for FGA imaging and the second for DFGA imaging. FGA imaging was performed initially to tune the units for all drive voltages except those needed to operate the DFGA. Later, the FGA was used to calibrate the signal level of the test pattern.

The driver system was designed for general-purpose testing of the CCAID-244A, as described in Section 4.3.1.4. The Krohn-Hite Model 3103 bandpass filter was set for a maximum frequency equal to the Nyquist frequency in the FGA imaging tests. For the DFGA imaging tests, the maximum frequency was set at 60% of the Nyquist frequency. This was done, in lieu of a properly functioning sample-and-hold circuit, to reduce the very large amplitude of the f_o frequency component in the unprocessed DFGA output. The line clamp was necessary in all of the L^3 imaging experiments in order to remove 60 cycle modulation and associ-



(a) FGA TUNING AND CALIBRATION SYSTEM



(b) DFGA L^3 IMAGING SYSTEM

FIGURE 4-52. BLOCK DIAGRAMS OF THE ELECTRONIC SYSTEM AS USED FOR (a) INITIAL TUNING OF THE 244A AND FINAL CALIBRATION USING THE FGA OUTPUT, AND (b) FOR DFGA IMAGING

ated low frequency noise. However, for measurements at higher light levels the line clamp was removed or bypassed because of an undesirable frequency-response function in the line clamp circuit. The polarity of the X-Y display was selected for each experiment to provide the best contrast.

The unit to be tested was mounted on a custom-made socket board and the alumina header was heat-sunk with "L-grease" to a copper block on which a chromel-alumel thermocouple was mounted. Provisions were made so that a portion of the socket board surrounding the device could be housed in an air-tight Delrin cold chamber with a 0.06-inch thick glass window. This assembly is shown in Figure 4-53. The μA733 10X low-noise amplifier that was used in all DFGA tests is located at the bottom right of the socket board.

The trinocular light spot arrangement shown in Figure 4-54 is similar to that described in Section 4.2.2.1, except that the trinocular stage is mounted on a more rugged precision base. For test pattern imaging, the light spot was replaced by a transparency and a diffused light source. The test pattern was a bar pattern of approximately 5 white bars in a square format, and was of such size that the spatial frequency on the device was approximately 20 percent of the Nyquist frequency ($0.2f_N$).

2) Device Tuning Procedure Using the FGA's

A unit was initially tuned by adjusting the drive system to obtain the optimum test-pattern image from the FGA1 preamplifier at a light level of approximately 50% saturation. The device was then tuned for maximum signal modulation at FGA2 to obtain optimum charge transfer through the DFGA input channel.

3) Bar Pattern Input Signal Level Calibration Using FGA1

The procedure for calibrating the input signal is given in Table 4-8. The uniform illumination source was the field illuminator of the trinocular microscope. This provided a signal uniformity across the array of approximately ± 10%.

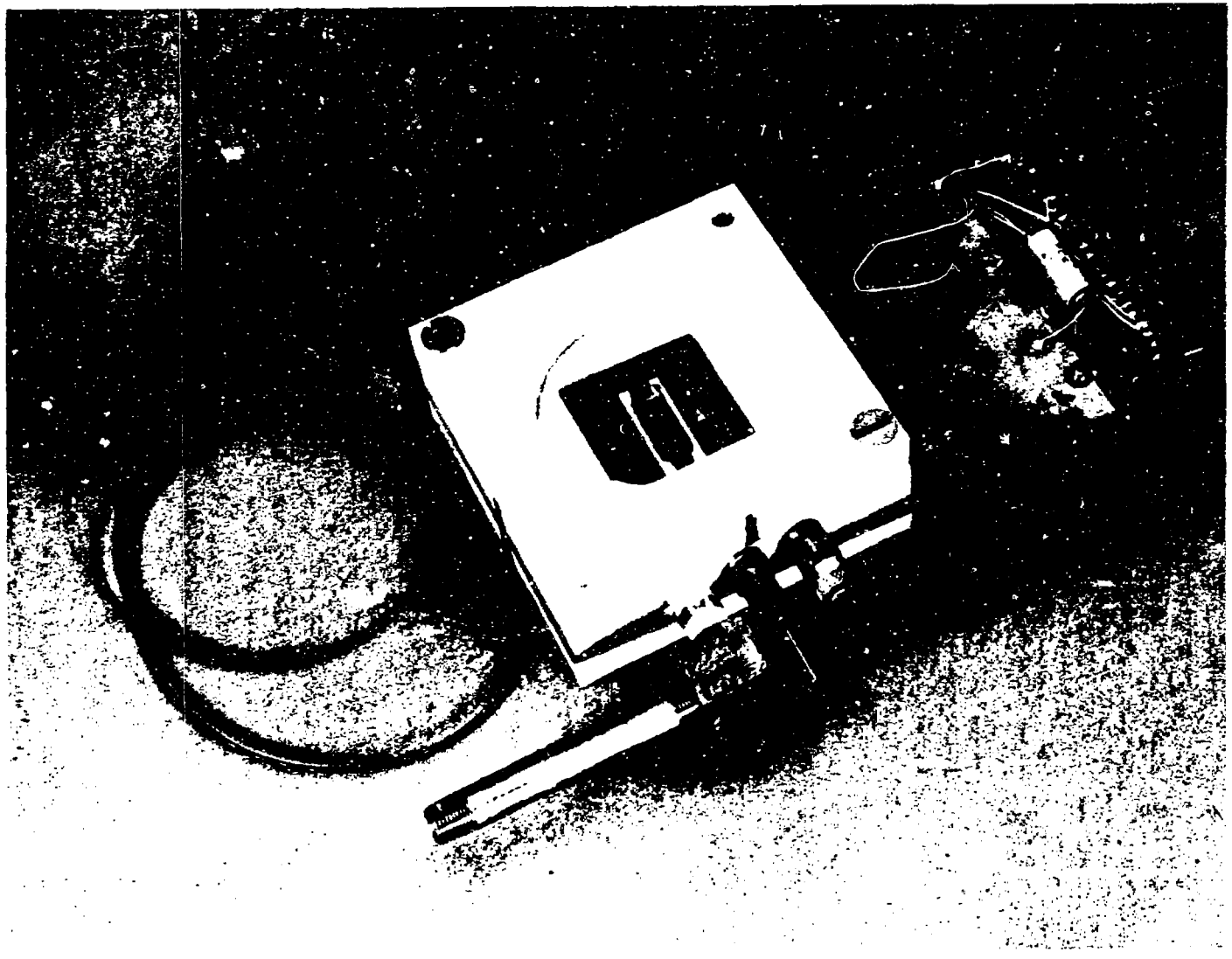


FIGURE 4-53. LOW TEMPERATURE CELL FOR CHARACTERIZATION OF CHARGE-COUPLED IMAGING DEVICES FROM ROOM TEMPERATURE DOWN TO APPROXIMATELY -100°C

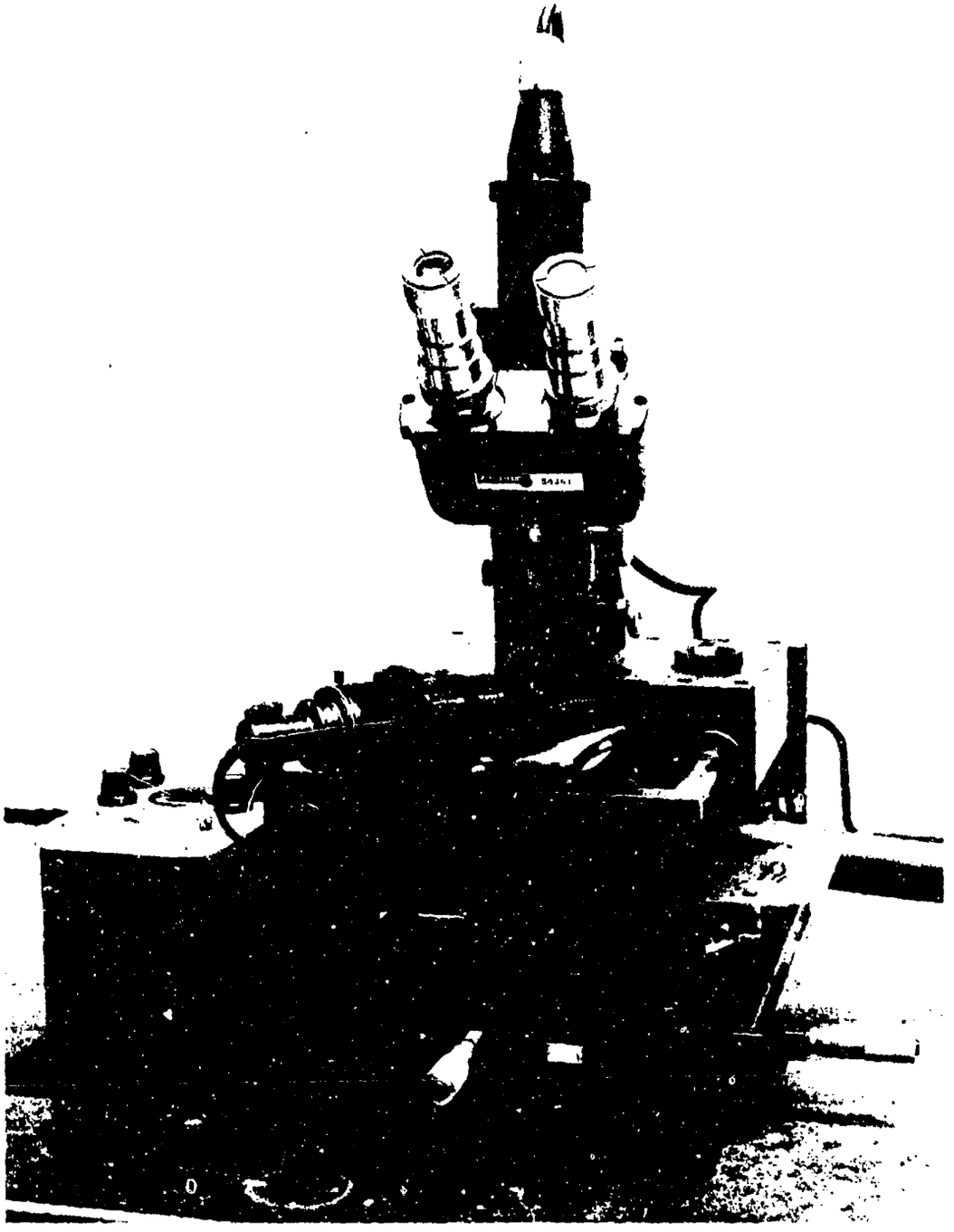


FIGURE 4-54. THE LIGHT SPOT PROBE STATION SHOWING THE TRINOCULAR MICROSCOPE WITH THE CONCENTRATED ARC LAMP HOUSING. A PORTION OF THE LOW TEMPERATURE CELL CAN BE SEEN IN THE LOWER RIGHT PORTION OF THE PICTURE

TABLE 4-8

PROCEDURE FOR CALIBRATING THE TEST PATTERN INPUT SIGNAL LEVEL

1) Turn off the DFGA by setting V_{SIDGA} several volts more positive than when the DFGA is on. This is done to facilitate photocurrent measurements in the sink diode (DDFGA) after FGA2.

2) Using FGA1 and the bar pattern source, adjust the light output to just below the level where the first saturation phenomenon is observed. This output is defined as the reference output signal.

3) Shut off the test pattern source; turn on the flood illumination source, which provides a uniform circular illuminated area with a diameter equal to the height of the 244A photoelement array.

4) Read the photocurrent from the sink diode (DDFGA) as the difference between total current and dark current. An HP 425A microammeter may be employed.

5) Calculate the reference signal level in electrons/pixel from the photocurrent, the frame rate, and the number of photoelements illuminated by the uniform circular image.

6) Obtain the levels of the smaller signals with the aid of calibrated neutral density filters.

4) Final Device Tuning Procedure Using the DFGA

After cooling the device to the desired temperature, the intensity of the test pattern was set at a level close to the minimum level for observing the DFGA output signal on the oscilloscope. The DFGA gain was then optimized at that signal level. This was done by adjustment of all DFGA drive voltages as well as the voltages of the horizontal clocks. Since this procedure resulted in a significant increase in gain, it was repeated at each lower input signal level. In this way, the gain was maximized at the lowest signal levels.

5) Procedure for Determining the Minimum Detectable Signal (MDS)

After the gain had been maximized, the intensity of the test pattern image was decreased further by steps of 20 to 30 percent each until the image could just barely be seen on the X-Y display. The viewing conditions of the X-Y display were optimized. The image could be moved slowly or be turned on and off. The most favorable area of the device was used. The temperature of the device was adjusted until the lowest MDS was achieved.

6) Procedure for Determining the Noise Equivalent Signal (NES)

There are four parts to this procedure: (1) determination of the transfer characteristic or "gain curve" of the DFGA after the device has been tuned for the best MDS, (2) measurement of the peak-to-peak input noise, (3) extrapolation of the transfer characteristic to the peak-to-peak noise level, and (4) division of the peak-to-peak input noise value by five to give the RMS input noise. The RMS input noise level is by definition the NES.

The transfer characteristic was obtained using the calibrated test pattern signal and calibrated neutral density filters. Because it had been found that the shape of the transfer characteristic (on a log-log plot) differs from device to device and with tuning adjustment, it was necessary to take sufficient data for a given device for a reliable extrapolation at the lower signal levels. For the noise measurement, the electronic system shown in Figure 4-52 (b) was used; the bandwidth was set at 0.3 MHz for a device output frequency of 1.0 MHz. Ideally, the bandwidth would be set at 0.5 MHz,

which corresponds to the Nyquist frequency for the device; the lower bandwidth was required here to prevent saturation of the oscilloscope preamplifier by the 1.0-MHz main frequency component from the DFGA. The line clamp was in the circuit for the noise measurement. The peak-to-peak noise was measured both by direct viewing of the oscilloscope display and from photographs of the display where approximately 100 traces were recorded per photograph.

4.3.2.4.3 Test Results

1) Minimum Detectable Signal (MDS)

Table 4-9 summarizes the three best MDS determinations for the two best units. The three minimum detectable signal levels are 45, 35, and 33 el/pixel, respectively. The output frequencies 1.0 and 2.5 MHz were used interchangeably; no consistent effect on MDS was found. For a given device, the temperature where the best L^3 imaging was obtained was most often in the range of -10°C to 0°C. Although additional cooling was expected to improve imaging quality by reducing dark-signal effects, there invariably appeared one or another kind of extraneous effect which limited performance. One persistent limitation in these experiments was the occurrence of a large excess noise whenever the device was cooled to -20°C or lower for any length of time; this was apparently caused by moisture condensation on circuitry adjacent to the cold cell that housed the device.

2) Noise Equivalent Signal (NES)

Table 4-9 also gives the NES for one device determined at the time of the best MDS determination, Test No. 3, with the corresponding gain and noise determinations. The NES value of 23 el/pixel was the best NES value obtained from reproducible data at the time of the MDS determination of < 40 el/pixel. In other cases, either the NES value was > 40 el/pixel or the NES result could not be reproduced.

The NES in Test No. 3 was determined from the transfer characteristic shown in Figure 4-55 and a peak-to-peak noise determination as shown in Figure 4-56. The four data points of the transfer characteristic indicate a slope of 0.50 over the range of signal levels 800 to 25,000 el/pixel. The peak-

TABLE 4-9

SUMMARY OF DFGA L^3 IMAGING EXPERIMENTS

Test No.	Unit No.	fo (MHz)	T(°C)	Minimum Detectable Signal (el/pixel)	DFGA Gain at 800 el/pixel (μV/el)	Peak-to-Peak Noise (mV)	NES (el/pixel)
1	29-W4-3	2.5	-4	45	-	0.2	-
2	34-W6-33	1.0	-20	35	-	-	-
3	34-W6-33	1.0	0	33	2	1	23*

* The NES for this unit was estimated by: (1) extrapolation of the DFGA response curve (Figure 4-55) to the point where the output is half the peak-to-peak noise, (2) reading the corresponding input signal value, and (3) dividing that value by 2.5.

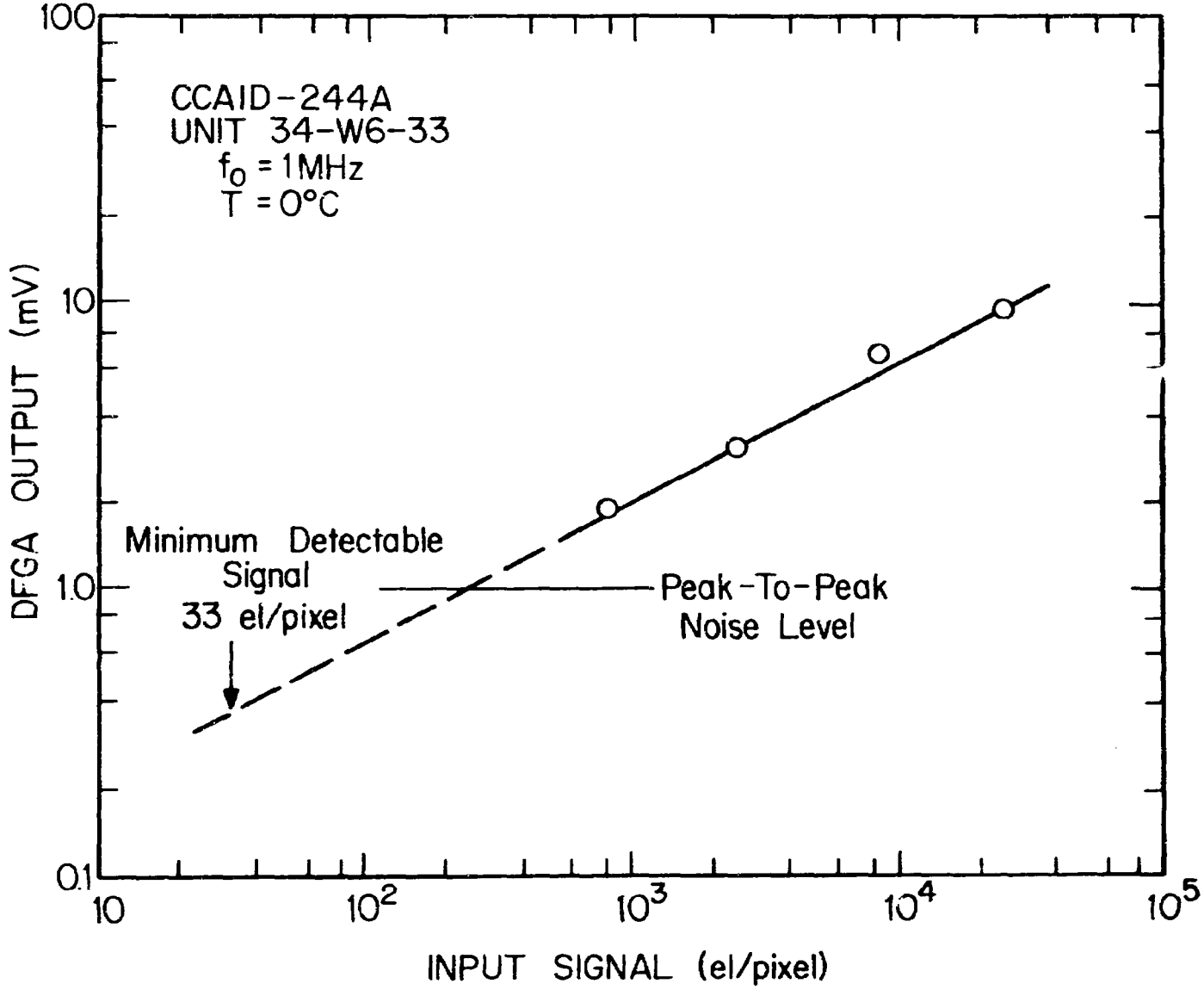


FIGURE 4-55. DFGA RESPONSE TO A 0.2 f_N BAR PATTERN VERSUS INPUT SIGNAL LEVEL

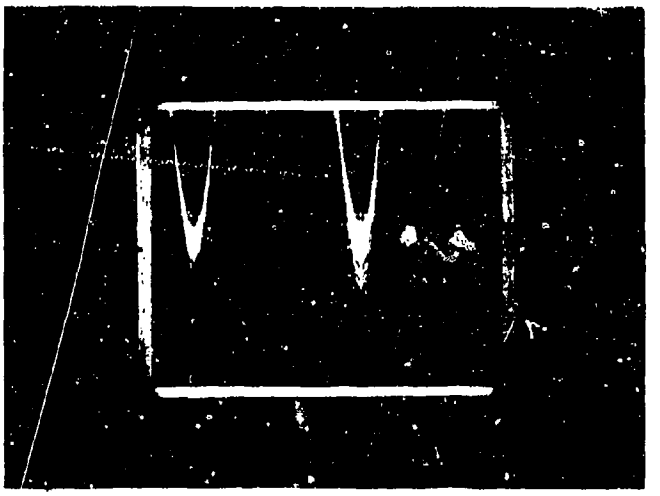


FIGURE 4-56. NOISE AT THE OUTPUT OF THE DFGA AFTER A 12X AMPLIFICATION. This photograph was taken as a part of Test No. 3 in Table 4-9. Vertical scale: 5 mV/cm. Horizontal scale: 20 ns/cm. Number of traces in this time exposure: ~150.

to-peak noise was estimated to be 1 mV. Because of its non-linear characteristic, the curve was extrapolated to half the peak-to-peak noise level, that is, to 0.5 mV, as the next step in the NES determination. For this voltage, the equivalent input signal level is 58 el/pixel. The RMS input signal level was computed by dividing this value by 2.5 giving 23 el/pixel. This corresponds to the method of estimation in the case of a linear amplifier where the peak-to-peak noise is divided by five to obtain the RMS noise.

It is unusual to encounter an amplifier with a non-linear characteristic at small signal levels. Hence, the above extrapolation should be justified by supporting information concerning the DFGA amplifier characteristics at small signal levels. Such information is provided in Figure 4-57, which shows the transfer characteristic for a DFGA with data points over the input signal range from 30 to 4×10^5 el/pixel. The NES of this unit was estimated to be approximately 15 el/pixel. The figure shows that the large signal transfer characteristic has a slope of 0.70 and that this slope is maintained down to a signal level at least as small as 100 el/pixel. The uncertainty in the data point at 30 el/pixel is such that the transfer characteristic below 100 el/pixel can lie anywhere between the extrapolation of the curve with a 0.70-slope and a 1.0-slope linear extrapolation from the 100 el/pixel data point.

It may also be noted that the gain levels of the two DFGA units under discussion, as read from the figures at the 100 el/pixel level, are both close to 6 μV/electron This consistency adds validity to the comparison of the two DFGA's.

4.3.2.4.4 Comparison of Predicted and Measured Results

Prior to this L^3 imaging investigation, it had been shown that at least one DFGA could be operated with a gain large enough for the device noise to dominate the system noise. The best gain was approximately 17 μV/el. A total system noise of 170 μV RMS was obtained when signal charge from the array was diverted away from the DFGA. If this gain and noise had been realized on any of the units tested for L^3 imaging capability, much better results would have been obtained. A prediction of results made on this basis is presented.

If it is assumed that the dark current density is 10 nA/cm^2 at room temperature, that the temperature dependence of dark current is normal, and that

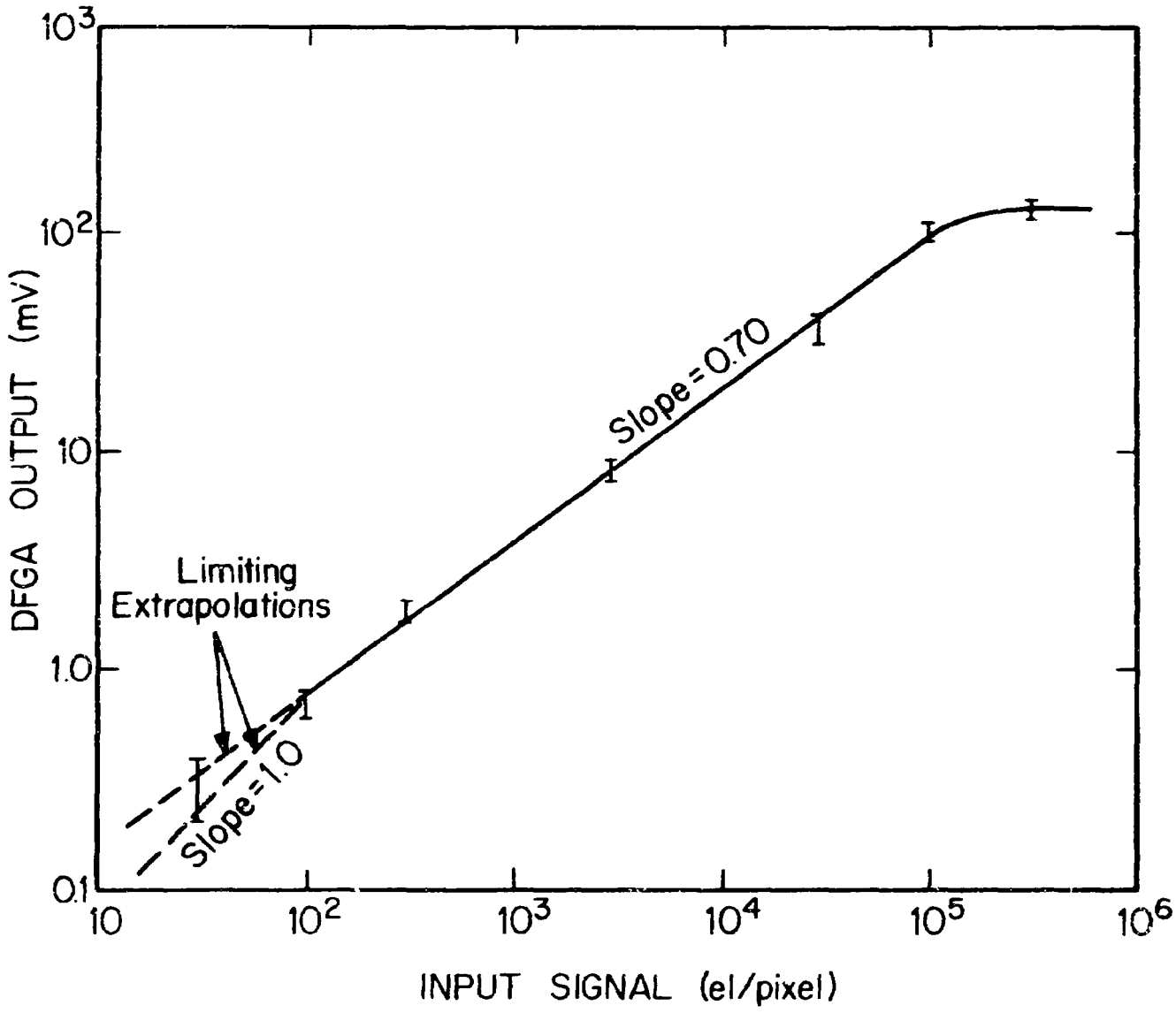


FIGURE 4-57. THE DFGA TRANSFER CHARACTERISTIC FOR A LOW-NOISE UNIT SHOWING NONLINEARITY DOWN TO AT LEAST 100 el/pixel.

the operating temperature is 0°C; the average dark charge is 1300 el/pixel and the shot noise in that average dark charge is 36 el/pixel. Although further cooling would reduce dark charge shot noise this prediction is made for the highest operating temperature of the three tests listed in Table 4-9. Another condition imposed on the prediction is the limited response bandwidth at the input to the DFGA as observed in the units studied. This response bandwidth was typically equal to the bar test pattern signal frequency, i.e., 0.2 f_N. This has the effect of smoothing the dark current shot noise from 36 el/pixel to $36\sqrt{0.2}$ = 16 el/pixel RMS dark current fluctuation. When this NES is combined by root-mean-square addition with the 10 el/pixel DFGA NES, a total NES of 19 el/pixel is predicted. As the temperature is lowered, the NES is predicted to approach 10 el/pixel.

When these predictions are compared with the best measured result, it is seen that at 0°C there is substantial agreement, i.e., an NES of 19 el/pixel. However, as the temperature was lowered, the predicted NES of 10 el/pixel was not observed. The uncertainty in the measured NES of 23 el/pixel and the inability to observe small changes in the MDS in the procedures used suggest that the system NES was possibly as high as 20 or 30 el/pixel and that this system noise dominated device noise.

With regard to a prediction of threshold signal level, it is difficult to be quantitative. From L^3 television practice, it has been found that the elemental signal-to-noise ratio for various multiple-bar targets is approximately unity; for a fourteen bar test pattern the signal-to-noise ratio at the threshold is approximately 1.2.[1] The way that this ratio scales with spatial frequency is quite complex in most L^3 television systems. If it is assumed that it varies linearly with spatial frequency the CCD element threshold signal-to-noise ratio at 0.2 f_N is predicted to be 0.24. Therefore, if the total NES had been 10 el/pixel, the threshold signal level should have been 2.4 el/pixel.[2] The discrepancy between this predicted performance and the measured results is attributed to low DFGA gain and the dominance of substantial amounts of system noise; it would not have appeared if the higher gain DFGA was available when this experiment was performed.

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(1) See for example F.A. Rosell, "Limiting Resolution of Low-Light-Level Imaging Sensors", J.O.S.A. 59 539 (May 1969).

(2) This result is very close to the n_{sw} value predicted by equation 7 of the Camera System Performance Analysis included as Section 7.2.4.1 of this report. In this case n_{sw} = 2.5 el/pixel with NES = 10, M_c=C=1, and N_r = 0.2 Nyquist.

4.4 CHARGE-COUPLED AREA IMAGING DEVICE 380 x 488A, MODEL A (CCAID-488A)

The ultimate objective of the NESC program is to obtain an area image sensor with 488 rows of 380 photoelements and all the operational features of the CCAID-244A. The CCAID-488A was the first attempt to design such a large and complex device. In order to insure adequate charge-transfer efficiency at low signal level in the interline CCD registers, an overlapping gate (or gapless), thin-oxide gap, self-aligned implanted barrier, 2-phase structure was designed. Other design modifications included less critical alignment tolerances, particularly at the interface between the vertical and horizontal registers, and the elimination of high leakage-current problems between horizontal gate electrodes.

4.4.1 Functional Elements

The organization of the CCAID-488A, shown in Figure 4-58, is similar to that of the CCAID-244A. The major sections of the chip are the photosensor array, the electrical-input register, the output register, and four amplifiers; a DDA, two FGA's and a DFGA. Unlike the 244A, the 488A possesses an oxide-gap, self-aligned vertical-register structure.

The photosensor array is composed of 488 x 380 photocells with dimensions of 15 μm x 18 μm. One vertical register gate with dimensions of 15 μm x 18 μm is associated with each photocell. An anti-blooming element is provided for each vertical register. The input register at the lower end of Figure 4-58 is a linear CCD shift register with an input diode and one input gate. This input register is included for electrical evaluation of the device. The output register carries charge from the photoarray to the output amplifiers. Each of the four output amplifier options is separately selectable. The DDA and FGA are intended for general use; the DFGA is intended primarily for low signal level applications.

4.4.2 Structural Details

A plan view of the unit cell for the 488A is shown in Figure 4-59. The unit cell dimensions are 30 μm x 36 μm, where each unit cell consists of two photoelements and two vertical gates. The structure employs two-phase clocking and gateless transfer from the photogate to the vertical registers. The dimensions shown in Figure 4-59 are nominal final device dimensions. The active area of each photoelement is 216 μm^2. Of this total, there is 100 μm^2 which has single level polysilicon. The charge storage area after lateral diffusion of channel stop is 60 μm^2. The nominal barrier width

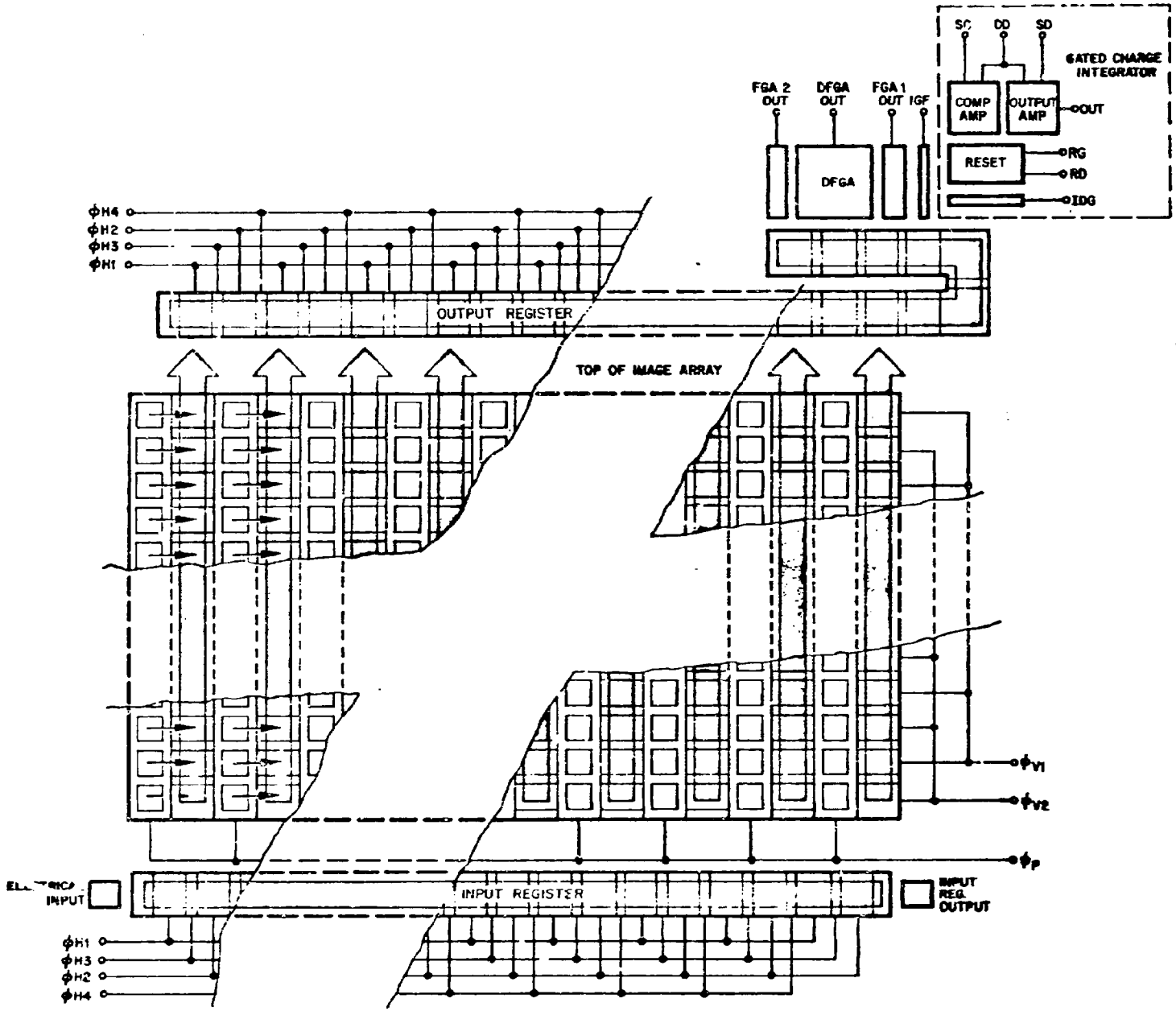


FIGURE 4-58. FUNCTIONAL LAYOUT OF CCAID-488A

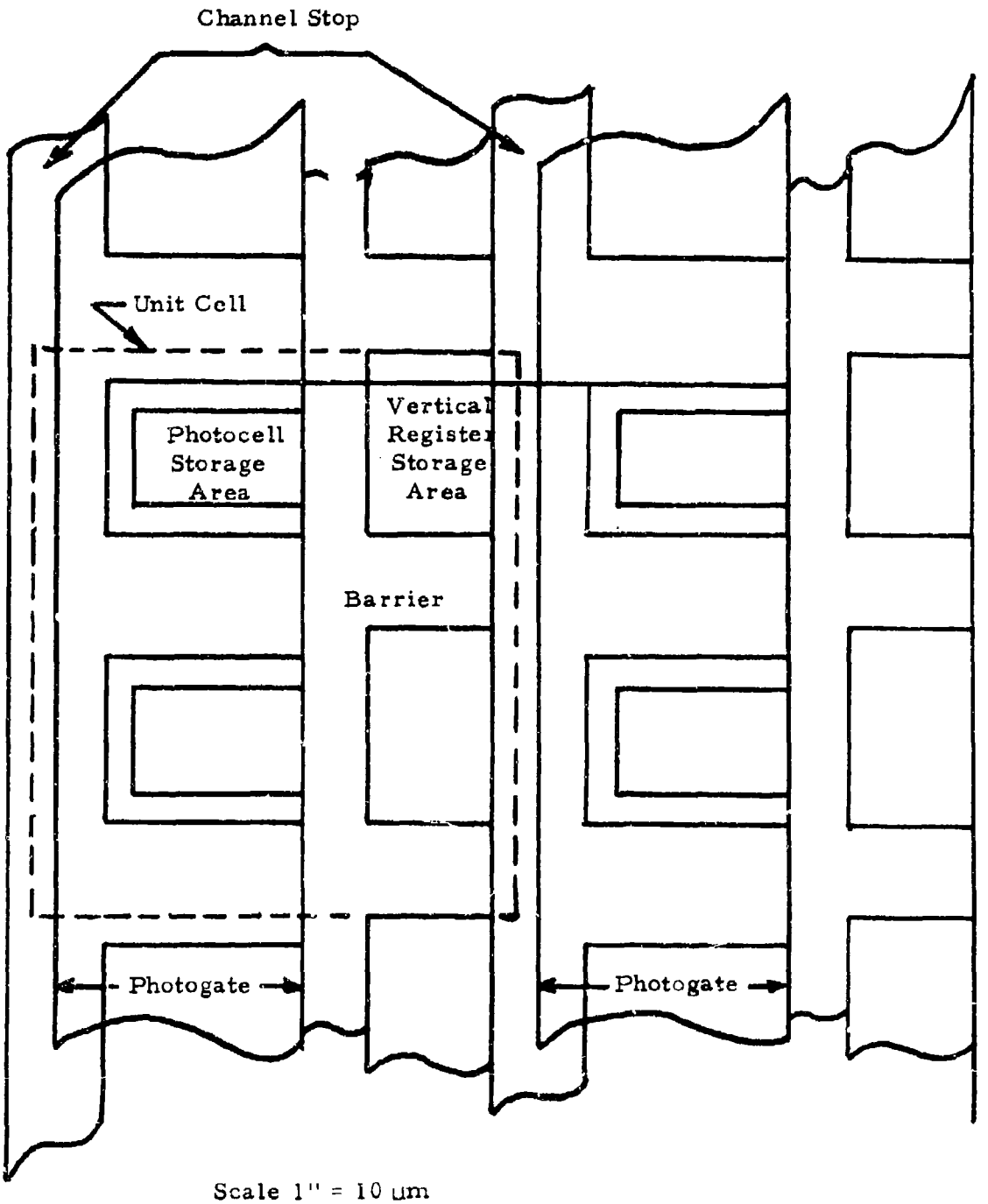


FIGURE 4-59. PLAN VIEW OF 488A UNIT CELL

between the vertical register wells is 6 μm. The nominal barrier width between the vertical register and the photocells is 4 μm. The nominal vertical register well area is 72 μm^2.

A cross-section through a vertical register of the 488A structure is shown in Figure 4-60. One of the clock-phase electrodes is provided by polysilicon; the other is provided by metallization. The length of the implanted barriers is 6 μm; the length of the storage regions is 12 μm. An important feature of this structure is that the barriers are produced by a self-aligned process. The right edge of the implanted area falls within the oxide gap between phases as shown in the figure. This self-aligned feature provides for minimum undesired perturbations in the potential profile of the CCD, which results in maximum transfer efficiency of the array. It may be noted from the figure that the oxide over the barrier of the polysilicon gate is thicker than the oxide over the storage area, and that the oxide at the front edge of the polysilicon gate electrode is thinner than the oxide over the storage area. These oxide thickness differences are a result of the processing sequence used to produce the self-alignment, and are adjusted to insure that self-alignment is obtained.

Figure 4-61 shows a cross-section through the imaging array at a right angle to the direction of charge motion in the vertical register. This cross-section includes both the photocell and the vertical register. The particular cross-section shown cuts through one of the metal-phase-electrode storage areas of the vertical register. The width of the channel stop between vertical cells is approximately 10 μm after lateral diffusion. The width of the photocell is 8 μm; the barrier is 4 μm; and the vertical register width is 7 μm. The barrier between the vertical register and the photocell is implanted at the same time as the barrier between the vertical register cells is implanted. The photocell barrier is self-aligned to the edge of the first poly, as shown in Figure 4-61. In the structure shown, the barrier is clocked by the metal phase of the vertical register. The alignment of the right edge of the barrier is provided by a photoresist mask. It is critical to insure that this barrier alignment provides sufficient width to insure that two dimensional effects do not reduce the saturation charge of the photocell significantly.

It may be noted from Figure 4-61 that the photocell storage area width and the optical window width are not the same. The photocell storage area, as defined by the channel stop edge on the left and the barrier edge on the right, is 8 μm wide. The optical window is defined by the metallization edges, and is 13 μm wide. The photosensitive area width is 13 μm,

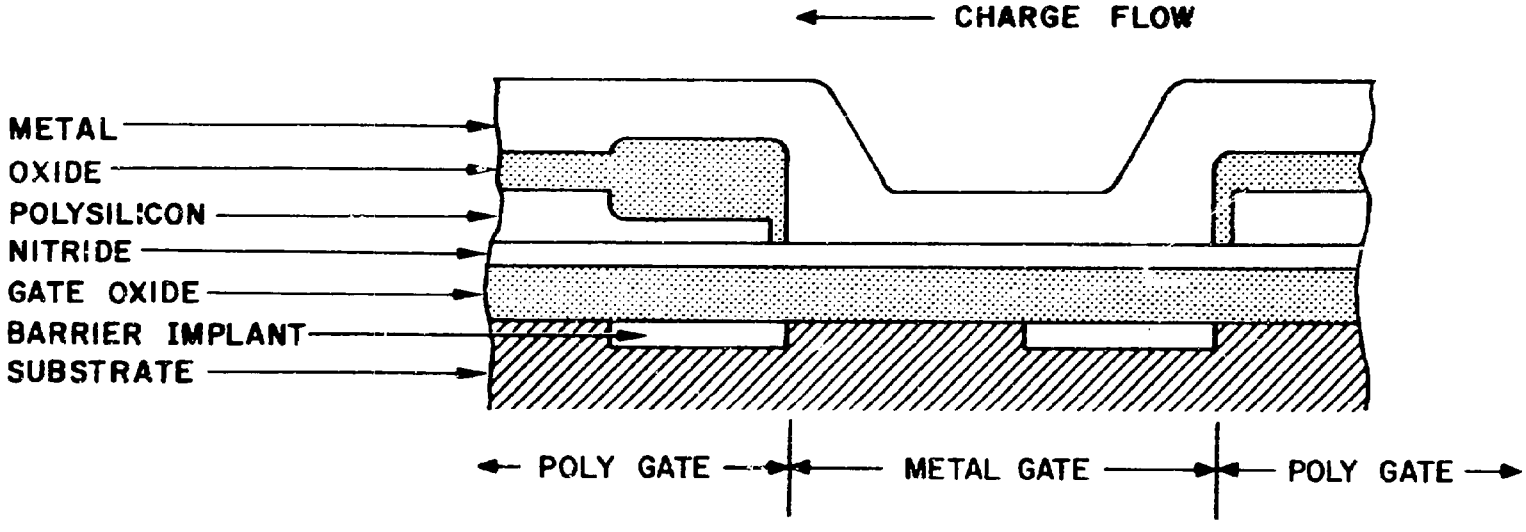


FIGURE 4-60. CROSS-SECTION THROUGH VERTICAL REGISTER

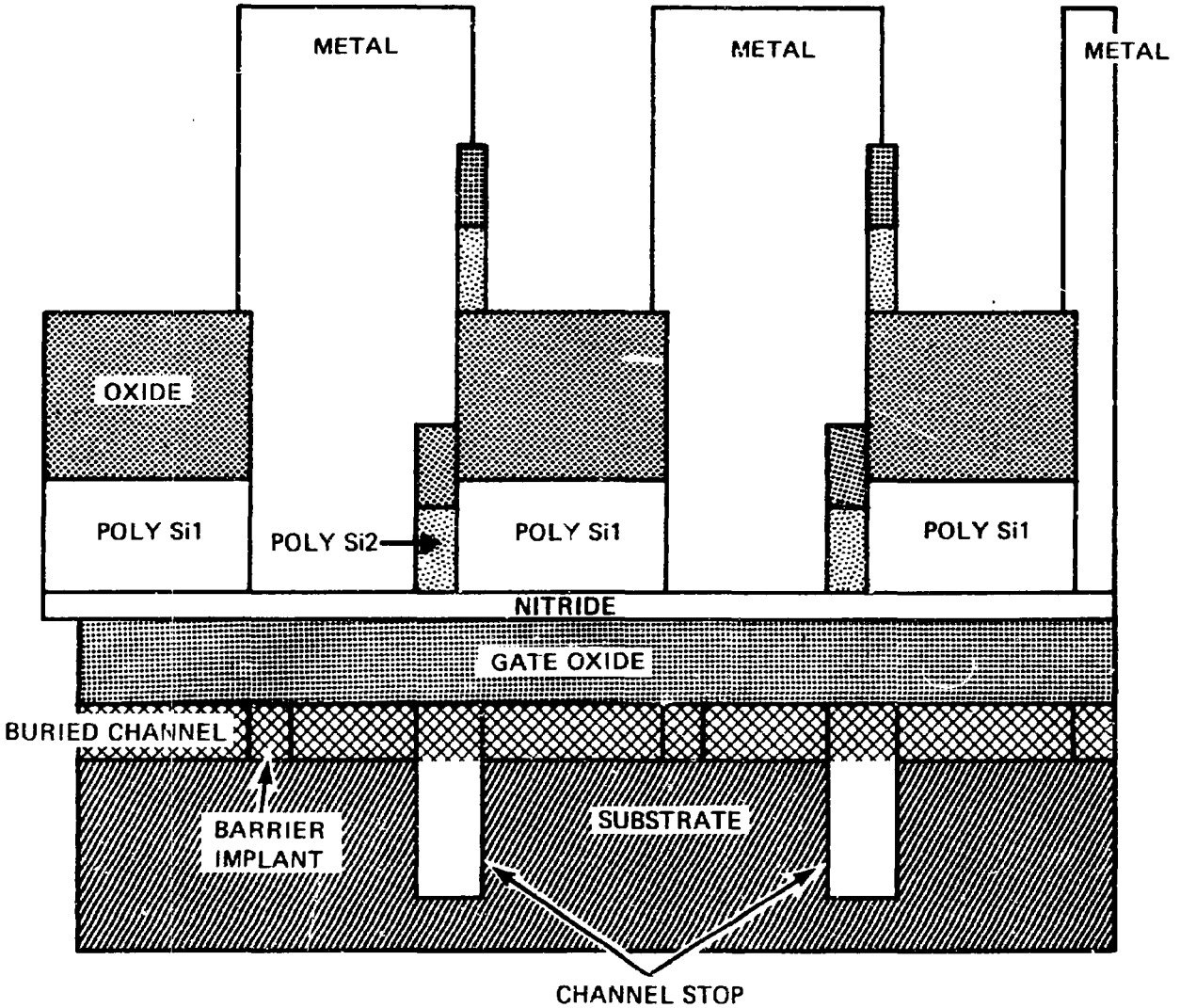


FIGURE 4-61. CROSS-SECTION THROUGH IMAGE ARRAY

of which 10 μm is single-level polysilicon and 3 μm is double-level polysilicon. The photosensor geometries have been chosen as a compromise between high photosensitivity and minimization of optical crosstalk.

4.4.3 Design Features

The major advantages of the structure of the 488A as compared with the 244A design are: (1) the oxide-gap structure provides a small unit cell with large storage capacity, while eliminating gate-to-gate leakage problems associated with undoped polysilicon gaps; (2) the self-aligned barrier structure insures maximum transfer efficiency with minimization of anomalous effects caused by misalignment of the barrier edge relative to the edge of the overlapping gate electrode; (3) the unit cell of the 488A provides for single-level polysilicon over approximately one-half of the photosensor area.

In addition to providing an oxide-gap, self-aligned structure, the 488A design has been modified to provide less critical alignment tolerances than were possible on the 244A design. The primary areas where these modifications were made are at the interfaces between vertical registers of the area array and the horizontal register. The high leakage-current regions between horizontal clock lines found in the 244A have also been eliminated.

4.4.4 Clocking

Clocking of the 488A is, by design, similar to that of the CCAID-244A. Apart from making allowances for the extra number of transfers required, there are no other differences. The input and output registers can be clocked in either four-phase or two-phase modes. Each phase must receive a minimum of 423 pulses; 380 are required to empty either of the registers and 43 to process signals through the DFGA.

For the vertical registers, 246 pulses are required to read out one field of video. As with the 244A, there is no barrier between the area array and output register; the last vertical gate (ϕ_{V1}) must be normally low, i.e., low when each horizontal line is being read out. The input register structure is similar to that of the 244A. It is, therefore, subject to the same clocking constraints discussed previously in Section 4.3.1.4.

The drive circuits used to evaluate the first units are shown in Figures 4-62, 4-63 and 4-64. The vertical logic divides the horizontal bit rate by 650; 65 horizontal bits are also allowed for the horizontal inhibit

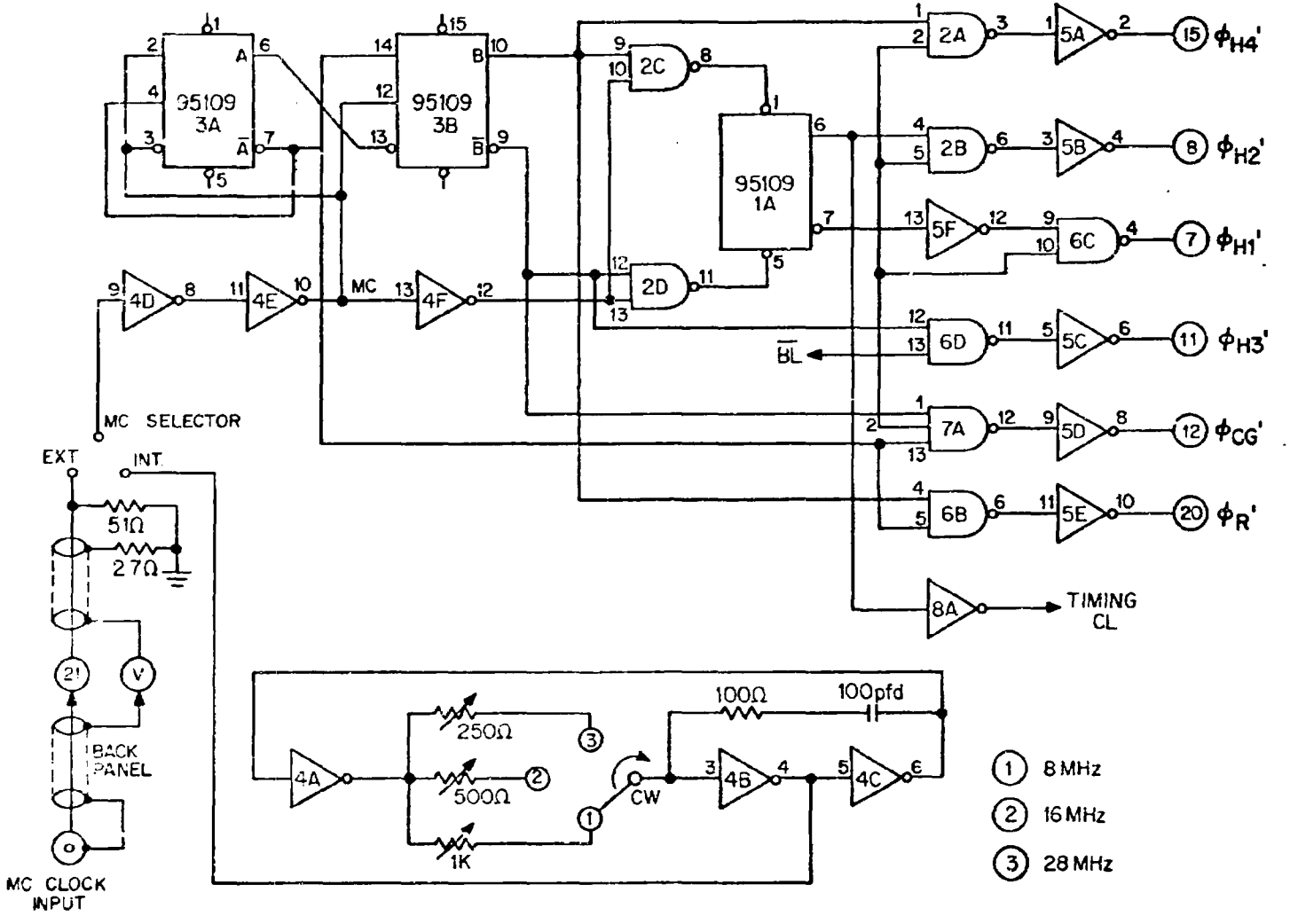


FIGURE 4-62. LOGIC FOR HORIZONTAL REGISTERS AND DFGA

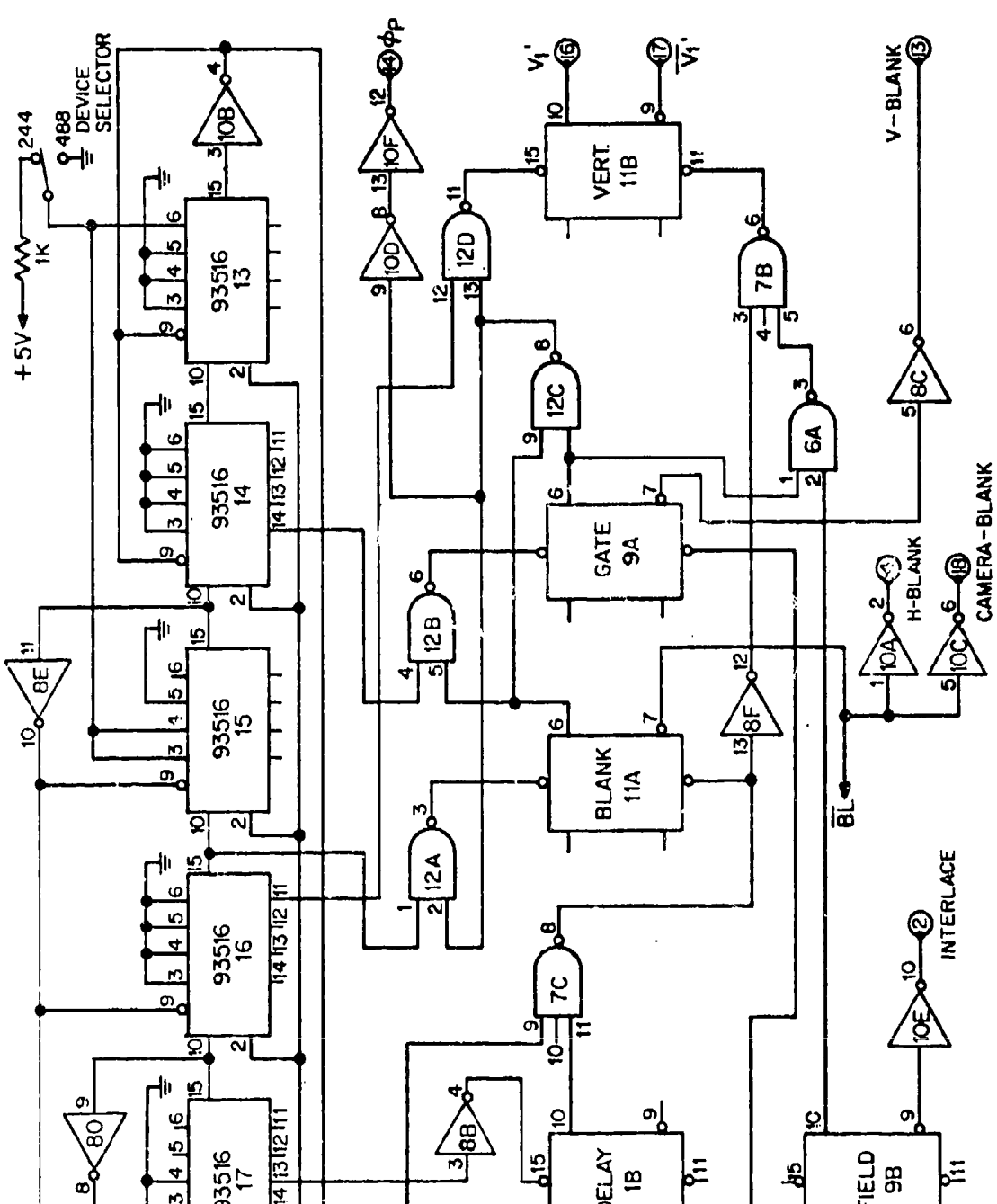
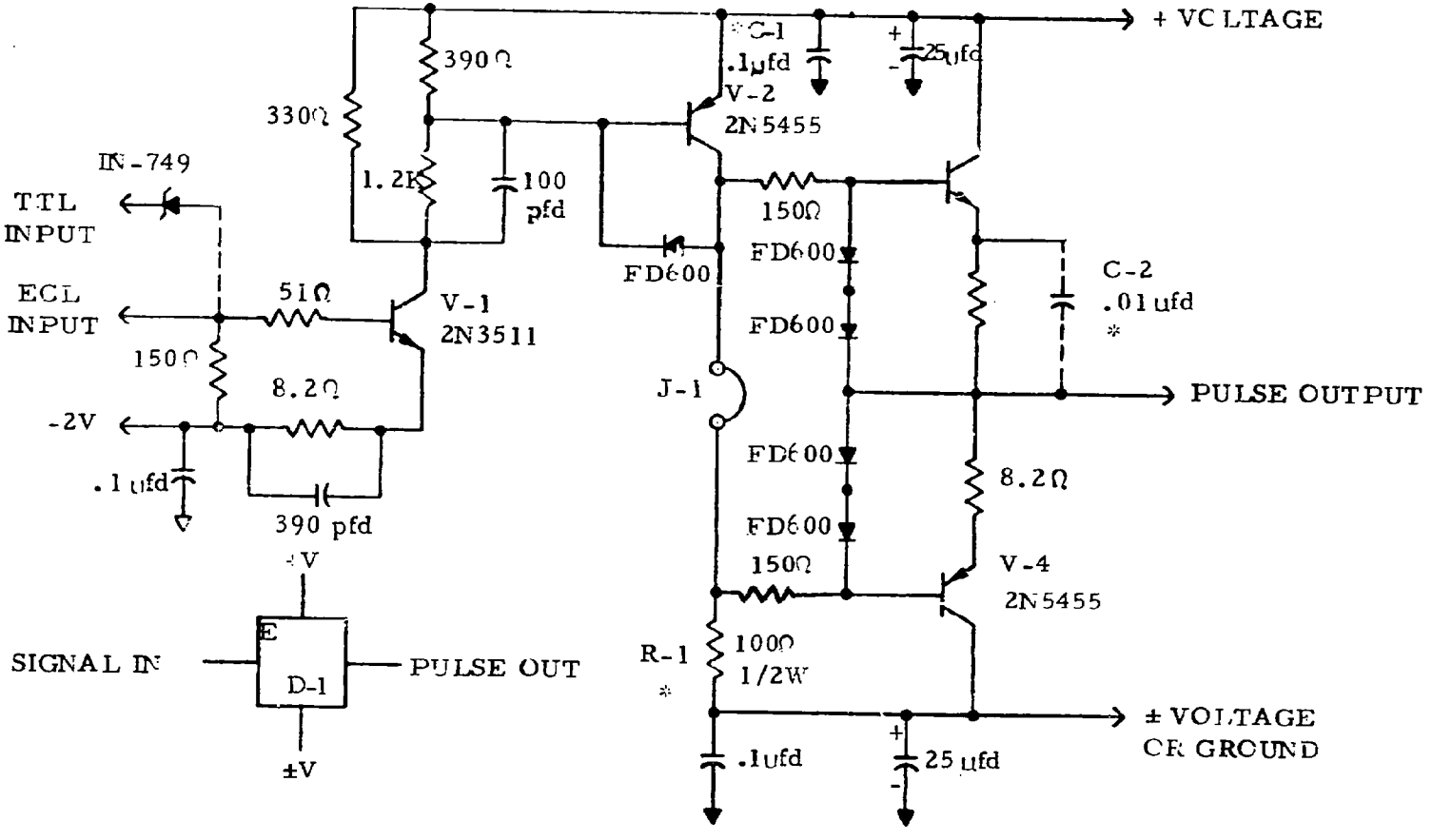


FIGURE 4-63. LOGIC FOR GENERATING VERTICAL AND PHOTOGATE PULSES



NOTES: J-1 Replaced with IN752 on ϕ_{H3} Driver.
C-1 Not installed on SE Drivers
C-2 Installed on ϕ_1 and ϕ_2 to allow faster rise time without tripping over current circuit.
R-1 Can be Increased in value for low frequency operation.
Z-1 Used only if input is TTL level, Driver is then Type T.

FIGURE 4-64. DRIVER CIRCUIT FOR 488A DEVICE

interval. Therefore, the vertical period is 650 + 65 = 715 horizontal bits. Since the horizontal clock rate is 7.16 MHz, which corresponds to a period of 140 nsec, the vertical period is $175 \times 140 \times 10^{-9} \approx 100$ μsec; the vertical clock frequency, ϕ_V, is then 10 KHz.

The frame interval generator divides the vertical clock frequency by 256 to give the corresponding field rate of $\frac{10\ \text{KHz}}{256} = 39$ Hz. The frame rate is then approximately 20 Hz. If it is desired to clock at the standard frame rate of 30 Hz with this circuit, the horizontal clock rate would become 10.7 MHz.

The timing diagrams for the 488A logic circuits are shown in Figures 4-65 and 4-66.

4.5 CHARGE-COUPLED AREA IMAGING DEVICE 190 x 244, MODEL B (CCAID-244B)

The CCAID-244B is a redesign of the 244A to the oxide-gap, self-aligned structure used on the 488A. In this redesign, the general features of the 488A are maintained, with modifications being made to the DFGA, the anti-bloom structure and the input register to provide higher performance. The 244B design also incorporates minor design adjustments that have been established as advantageous with respect to wafer-fabrication yield in view of the experience with the 244A. Table 4-10 lists the changes made from the 488A design to the 244B design.

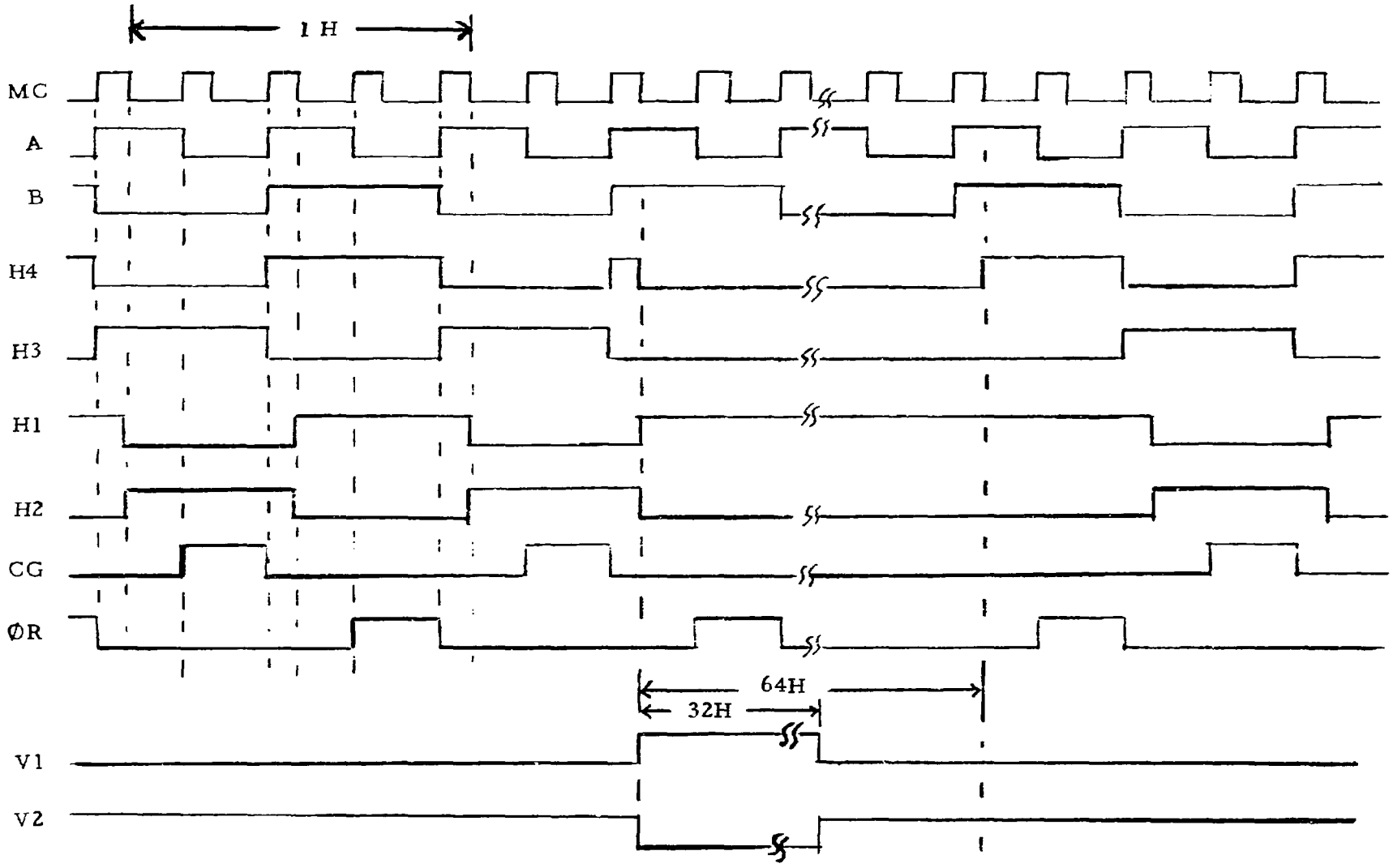


FIGURE 4-65. TIMING DIAGRAM FOR HORIZONTAL REGISTER AND DFGA LOGIC

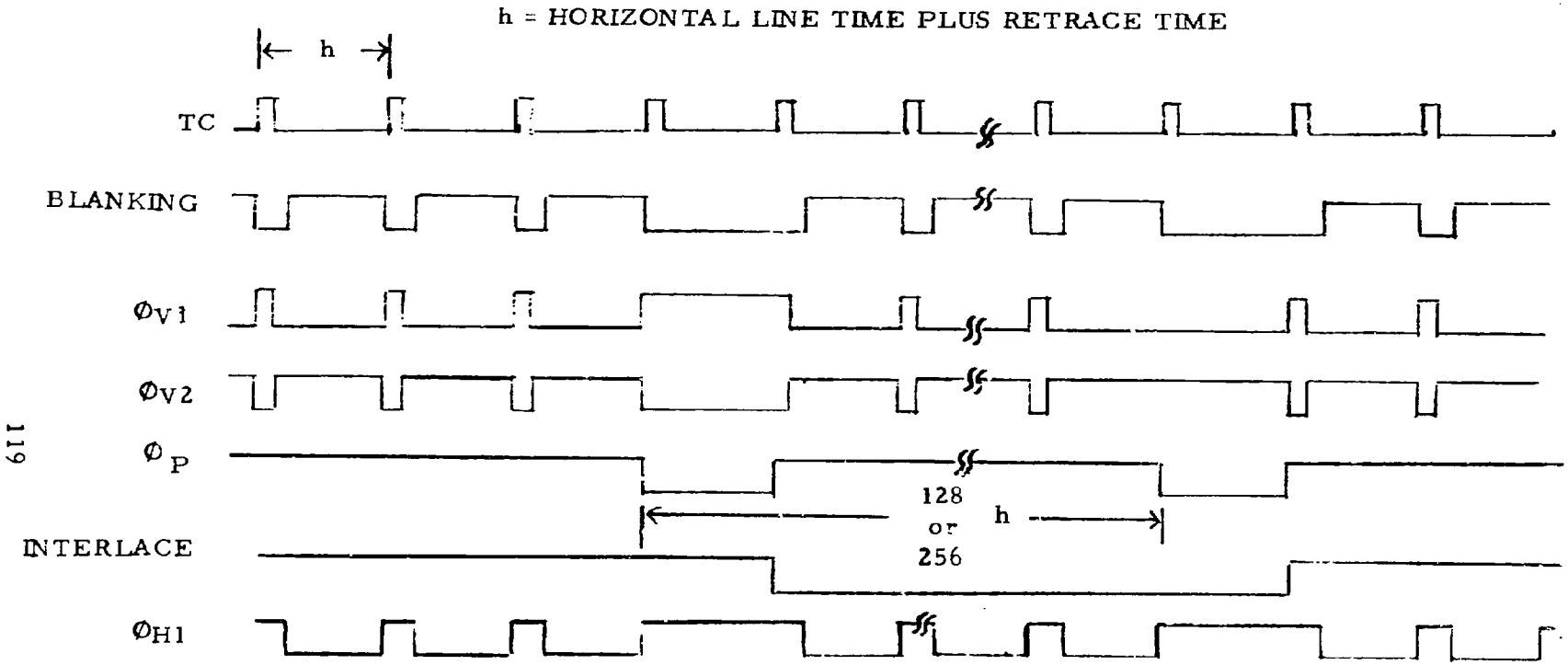


FIGURE 4-66. TIMING DIAGRAM FOR VERTICAL AND PHOTOGATE LOGIC

TABLE 4-10

CHANGES FROM 488A to 244B

1. Unit cell changed to reflect 3 μm capabilities of 10X lens - results in higher saturation level for photocell and vertical registers.

2. ABS redesigned - results in looser alignment tolerance.

3. DFGA refined for improved low-signal-level transfer efficiency.

4. Electrical input redesigned for increased linearity.

5. Diode gate protection option included.

6. Refinements established from 244A and 488A processing evaluation included for improved yield.

SECTION 5

CCD TECHNOLOGY STUDIES

5.1 INVESTIGATION OF CHARGE-TRANSFER EFFICIENCY AT LOW SIGNAL LEVELS

Both a theoretical and an experimental investigation was performed to ascertain that adequate transfer efficiency would be obtained, in a buried-channel CCD area image sensor of approximately 500 x 500 photoelements, to detect photosignals of the order of 10 electrons per pixel (picture element). The principal issue was to determine the effect of bulk traps in silicon on transfer efficiency for such a device at these low signal levels.

Although the effects of bulk traps in CCD's have been treated theoretically previously, the analysis undertaken during this program introduces new aspects of the situation. Charges are assumed not to be in a neutral region of the silicon but near the minimum of a potential well; the probability of charge being trapped depends solely on the number of charges in a potential well and the distance of the trap from the well minimum. Further, a random distribution of traps is assumed. Calculations are made relative to a set of standard or reference conditions which include temperature, well volume, trap concentration, trap energy level and trap cross-section. A principal conclusion is that for the worst-case condition analyzed, the cumulative transfer efficiency for an average dark charge per pixel of 10 electrons and an average signal charge per pixel of 10 electrons is approximately 0.8; the signal-to-noise voltage ratio is found to be 1.4.

It was recognized at an early stage in this theoretical analysis that bulk trapping is of consequence only in long registers operated at the conventional TV line rate of 15.75 KHz. At this time there was available a convenient vehicle for experimental measurements, a 256-photoelement linear imaging device with a two-phase, overlapping gate electrode, oxide gap CCD transfer register. The device was cooled to obtain an average dark charge per pixel of 4 electrons. A light spot was focused on a photoelement remote from the on-chip amplifier; the photosignal was then transferred to the amplifier at a clock rate of 15.7 KHz. This signal was compared to that for the light spot focused on an element close to the amplifier. It was observed that a 15 ± 3 electron signal underwent 238 transfers with

a one electron loss (subject to the same ± 5 electron experimental error). The data confirms the theoretical analysis that there is useful cumulative transfer efficiency after 500 transfers to detect photoelectronic signals at the 10-electron level.

5.1.1 Objective of Theoretical and Experimental Investigations

It is well known that surface channel CCD's are limited in performance by surface state trapping. On the other hand, buried-channel CCD's have been made, which perform over a very wide dynamic range without serious trapping effects. It is of particular interest in this development program to identify the limits of the capability of buried-channel structures to transfer efficiently very small signal charge packets. Because it appears feasible to have CCD amplifiers with noise-equivalent-signal levels of five electrons or less, it is desired to show that charge packets of approximately ten electrons can be transferred efficiently. Since it is an objective of this program to build area image sensors with 500 line resolution, the desired charge-transfer efficiency per transfer (η) is 0.999 or better at this level.

One limitation may be occasional interaction between the buried-channel charge packet and surface traps. A second limitation may be statistical spatial fluctuations in fixed-charge surface states that in turn cause spatial fluctuations in the buried-channel potential. A third may be bulk traps. Bulk traps can result from ion-implantation damage, imperfections in the silicon prior to wafer processing and donor-vacancy pairs. The primary objective of the investigation reported herein is to determine the extent of bulk-trapping effects on charge-transfer efficiency in buried, n-channel CCD structures.

5.1.2 Bulk Trapping Theory for CCD Area Image Sensors at Low-Light-Levels

Ideally, the signal-to-noise ratio for any pixel (picture element) of an area image sensor should approach the value that is intrinsic to the number of photons detected in that pixel. For charge-coupled image sensors, the signal-to-noise ratio is degraded by dark current, which adds noise to the signal charge packets both at the point of detection in the photoelements and along the path to the output amplifier, by the noise of the amplifier, and by transfer inefficiency and transfer noise which is associated with the hundreds of charge transfers required to bring signals to the amplifier from the more distant photosensor elements.

Cooling of the image sensor to temperatures below -50°C can reduce the dark current to one electron or less per pixel. The distributed floating-gate amplifier can provide an amplifier noise level of a few electrons. Use of a buried-channel rather than a surface-channel technique effectively eliminates the devastating effects of surface traps on transfer efficiency and the associated transfer noise at low signal levels. In its ideal form, the buried-channel device has very low transfer losses and very low transport noise. Cumulative transport efficiency can exceed ninety percent after more than 1700 transfers.[1] A high density of bulk traps, however, produces a significant deviation from the desired ideal structure and is the most serious cause of transport inefficiency and transfer noise in buried-channel CCD low-light-level image sensors which operate at reduced temperatures.

This study analyzes quantitatively the effects of bulk trapping on cumulative transfer efficiency and on signal-to-noise ratio in buried-channel CCD area imagers operating at bright-spot rms signal levels from one to one hundred electrons per pixel. A general analysis using the best available values of critical parameters such as trap concentration and trap cross-section is employed to evaluate a proposed practical area image-sensor design. The major conclusion is that, for typical trap cross-sections, a usable signal-to-noise ratio will be achieved at the ten-electron signal level with 10^{10} traps per cubic centimeter without dark charge. Approximately the same result will be achieved with 10^{11} traps per cubic centimeter if the dark charge averages ten electrons per pixel.

The initial sections of this study describe briefly the assumed device structure and its mode of operation, review previous analyses of bulk trapping in buried-channel devices, and discuss the novel aspects of the low-light-level problem and of the model implicit in the physics of the device behavior. It is shown that the determination of rms transient response at bright-spot levels of a few electrons requires a microstatistical treatment of trapping probabilities and of geometric trap positions. Subsequent sections treat in sequence the analytic assumptions and method, the specific analysis including equations, detailed calculations and a discussion of their implications, and an overall assessment of the practical significance of the results.

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(1) Kim, C-K, IEDM Technical Digest, Dec. 1974, p 55

5.1.2.1 Device Structure and Operation

The device assumed for analysis is a 500 x 500 photoelement buried-channel CCD area imager of the interline transfer type with an imaging area approximately 0.360 inch by 0.480 inch. Two-phase operation is assumed with equal times in the two phases. Operation at the conventional television line rate of 15,750 lines per second is assumed. This results in a phase time for the vertical register of 31.476 microseconds. This phase time will be shown later to be a significant variable in determining the effects of bulk traps. The phase time for the horizontal register is five hundred times smaller; it will later be seen that bulk trapping in this register does not contribute significantly to transfer inefficiency and noise at very low signal levels. Details of cell geometry and of buried-channel dopant concentration are important only insofar as they affect the shape and size of the potential well and are discussed briefly in the specific analysis.

In operation, signal charge is accumulated for one frame time in a set of photosensors which corresponds to one field. These charges are then transferred into vertical transfer registers which subsequently shift the field of charge to the horizontal register at the rate of two transfers per horizontal line time, i.e., one transfer per vertical phase time. The horizontal register transfers charge toward the output amplifier at a rate greater than 1000 transfers per horizontal line time. Transfers from photoelement to vertical register and from vertical register to horizontal register are made during the vertical blanking interval and the horizontal blanking interval, respectively. Readout of odd-line and even-line fields is alternated. In short, the device studied is relatively large in area, provides full vertical resolution, and is operated in the full NTSC mode.

As a result of this mode of operation, approximately half of the dark charge accumulates in the photosensors during the integration interval; the other half during the transfer time to the output amplifier, which is primarily the transfer time through the vertical registers. Consequently, the dark charges of the pixels most distant from the amplifier begin their histories at approximately half their final values and add the other half gradually as they move toward the output amplifier. The analysis given later assumes that all the dark charge is introduced at the photosensor. This simplification eases the computations and is judged to modify the results only slightly.

For the charge levels assumed in the analysis, the mobile charge packets move in a space where fixed charge concentrations exceed mobile charge concentrations by two to four orders of magnitude at the point of maximum concentration of mobile charge. The fixed charge concentration and the exposure of this essentially dielectric (rather than semiconducting) space to the potentials of the surrounding electrodes result in strong spatial variations of well potential and in the effective confinement of the mobile charge to a small region in the vicinity of the potential minimum of the well. The mobile charges leave one such region only to move to the next. Because the transit time from well to well is many orders of magnitude shorter than the time spent in each vertical transfer well, bulk-trapping during transit is inconsequential.

For the trap densities considered, most potential wells have no traps sufficiently close to the potential minimum to trap charge significantly. In those wells that have traps near the minimum, the trap or traps can be assumed to be randomly distributed in space about the minimum.

Those wells lacking effective traps play no part in degrading transfer efficiency or in creating trapping noise. They act as ideal mobile charge transducers, which pass onward all the charge carriers they have received. Analytically, they may as well not be there. The analysis takes advantage of this.

The statistically probable trapping behavior of a well with an effective trap is dependent on the probable initial state of the trap, on the trap parameters, on the position of the trap with respect to the potential minimum, on the number of mobile charge carriers introduced into the well, and on the time charge is held in the well. The wide variations in location of the traps with respect to well minima must be satisfactorily represented and these locations must be randomized with respect to the transport sequence as they are in an actual device.

5.1.2.2 Prior Analyses

The effects of bulk trapping on transfer efficiency and transfer noise in buried-channel charge-coupled devices has been analyzed previously by Mohsen and Tompsett[2] and by Barbe[3]. Mohsen and Tompsett consider

(2) Mohsen, A.M., and Tompsett, M.F., Transactions on Electron Devices, Vol ED-21, No. 11, Nov. 1974, p. 701
(3) Barbe, D.F., Proceedings of the IEEE, Vol. 63, No. 1, Jan 1975 p 38

large signal packets and effectively confine their analysis to regions that are electrically neutral and which, therefore, have mobile charge concentrations approximately five orders of magnitude larger than the trap concentration of 2×10^{11} traps per cm^3. They state that their model, appropriately modified, may be employed for the very low charge levels considered here. Although they identify the appropriate calculation of the effective well volume as the critical modification of their method, they do not go further. Finally, they state that their method is valid as long as the probability of trapping a carrier during its many transfers is significantly less than unity. That is to say, for example, that the cumulative transfer efficiency must be greater than approximately 35%.

Barbe presents results generally similar to those of Mohsen and Tompsett. He points out that the expressions fail when the layer of mobile charge is approximately a Debye-length thick. This criterion is independent of that proposed by Mohsen and Tompsett. He provides an approximate expression for worst-case noise based on a minimum size of the potential well as that given by the 6 kT energy contour. The effects of trapping on transfer efficiency at extremely low charge levels are not analyzed or discussed. His numerical conclusions concerning trapping noise, however, are in rough agreement with the results found here.

5.1.2.3 Novel Aspects

As indicated previously, the situation treated here differs from those analyzed previously in that the charges are not in a neutral region but rather are near the minimum of a potential well. The probability of charge trapping is determined solely by the number of charges in the well and the distance of the trap from the well minimum. The interaction between charge and trap is not only determined by trap energy and phase time, but also by the position-dependent energy of the charge with respect to the well minimum. The most effective traps are not necessarily those at the well minimum. Rather, they are those which undergo the largest average increase in the probability of being filled from the dark current condition to the signal condition.

5.1.2.4 Assumptions and Method

The critical portion of the area image sensor with respect to bulk trapping is represented by a linear sequence of 500 electrodes, each with a 5-micrometer long, 5-volt height ion-implanted or stepped oxide barrier

for two-phase operation. The potential well under each electrode is 13 micrometers long and approximately 10 micrometers wide. The buried channel has a rectangular profile 0.5 micrometer deep and a net donor concentration of 2×10^{16} atoms per cm^3. Traps are assumed to be distributed randomly through the bulk at a concentration of 10^{11} per cm^3. Mobile charges are introduced only under the first electrode. They are then transferred through the structure by alternation of phase electrode potentials between 0 and 12 volts, which is sufficient to insure the rapid and complete transfer of all charges not in bulk traps. Both dark and signal charges are modeled by Poisson series.

For the calculation of the behavior of an average set of electrodes, each potential well is assumed to have one trap within a volume of 10^{-11} cm^3 about its center. This volume is then assumed to be divided into concentric shells, each of volume 2×10^{-14} cm^3, which is 1/500th of the average volume per trap. Each potential well of the set of 500 is assumed to have its trap at the mean radius of a unique concentric shell. This assures that the assigned trap positions are reasonably averaged in space about the potential minima. The order of wells with respect to radial trap positions is then randomized with respect to the order in which charge moves through the wells in order to model practical structures more faithfully.

The spatial position of the trap with respect to the potential minimum must be translated to an energy level with respect to the minimum to allow the calculation of the electron density at the trap position which enters into the capture probability. To achieve this, the well potentials are assumed to vary quadratically about the minimum. It is further assumed that the ellipsoidal equipotentials can be transformed to those of a sphere of equal volume. Computer simulations for a buried channel of a maximum depth of approximately 0.5 micrometer show that well potential changes by 0.020 volt in approximately 0.5 micrometer in both the length direction and the transverse direction of the electrode array. The donor concentration of the buried channel results in a change of 0.020 volt in 0.0357 micrometer in the depth direction. The geometric mean of these three values is approximately 0.208 micrometer and is the radius of the equivalent sphere at the 0.020-volt contour. Its volume is approximately 4×10^{-14} cm^3. The potential can then be represented as:

$$V_r = V_{r_o} + 0.020\,(r/r_o)^2$$

where r is distance from the well minimum and r_o is 0.208 micrometer.

For this spherical well containing N_W electrons, the electron density is:

$$n_r = \frac{N_W}{(\pi/\alpha)^{3/2} r_o^3} e^{-\alpha(r/r_o)^2}$$

where $\alpha = 0.020/(kT/q)$; kT/q is 0.01925 V at -50°C.

The effectiveness of a trap in modifying charge flow is determined by its characteristic emission time τ_e and by its capture time τ_c. Emission time is given by:

$$\tau_e = \frac{e^{E_T/kT}}{v_{th}\,\sigma\,N_c}$$

where E_T is the trap energy below the conduction band, σ is the trap cross-section, N_c is the density of states in the conduction band, v_{th} is the thermal velocity of the charge carrier, and kT has the conventional definition.

Capture time is dependent on the electron density at the trap, i.e., on the magnitude of the electron energy with respect to the trap energy, where the time is equal to the emission time when the energy levels are equal. Effective electron density at the trap is determined by the number of electrons in the well, by the size and shape of the well, and by the position of the trap in space and, therefore, its energy with respect to the well minimum. Capture time is given by:

$$\tau_c = \frac{1}{v_{th}\,\sigma\,n_t}$$

where n_t is the electron density at the trap location, assuming the trap to be empty; it is the same physical quantity as n_r given above.

5.1.2.5 Summary of Assumptions

1) The critical features of the image sensor design are modeled as a 500-element linear electrode array. Each electrode possesses a built-in barrier for two-phase operation. All potential wells possess a buried channel.

2) Well potentials increase quadratically with distance from the potential minimum. Potential variations in the X-Y plane at the minimum are taken from computer solutions as an increase of 0.020 volt at 0.5 micrometer from the minimum. The same potential is reached at 0.0357 micrometer from the minimum in the Z-direction.

3) The ellipsoidal potential well can be treated as a spherical well with radial variations equal to the geometric mean of the variations in the X, Y, and Z directions. This gives 0.208 micrometer for the 0.020-volt equipotential.

4) The random distribution of traps in the silicon can be represented adequately by a forced distribution of wells where each well has a trap in a separate, assigned, volumetrically equal, concentric shell centered on the potential minimum.

5) Each well is assumed to have one or no trap; the absence of wells containing two or more effective traps does not perturb the results significantly.

6) The trap behavior is characterized by an emission time τ_e given by:

$$\tau_e = \frac{e^{E_T/kT}}{\sigma v_{th} N_c}$$

and a capture time,

$$\tau_c = \frac{1}{v_{th} \sigma n_t}$$

where:

$$n_t = \frac{N_W}{(\pi/\alpha)^{3/2} r_o^3} e^{-\alpha (r/r_o)^2}$$

7) Electrons are not trapped during transfer from one well position to the next.

8) Both signal charge and dark charge can be represented by Poisson series of appropriate average values.

5.1.2.6 Trap Distribution

The signal-to-noise ratio at the output is determined by first assigning trap positions, which are then used to calculate capture time as a function of the number of electrons in a well. After the calculation of emission time, these parameters are employed to determine trap filling probabilities. From the trap-filling probabilities, cumulative transfer efficiency and signal-to-noise ratio are found by considering in sequence the effects of movement of typical charge packets through 500 wells.

Trap positions are assigned as follows for a set of M electrodes (or wells) with a trap concentration of N_T traps per cm^3. One trap is assigned to the volume $1/N_T$ which surrounds the minimum of each potential well. This volume is subdivided into M concentric shells of equal volume. In one of the wells, the trap is assigned to the arithmetic mean radius of a first concentric shell of volume $1/MN_T$. In a second well, the trap is assigned to the arithmetic mean radius of a second concentric shell of the same volume, i.e., to a radius equal to the outer radius of the first shell plus half the incremental radius of the second shell. The sequence is followed through the Mth well and shell which is almost $N_T^{-1/3}$ from the well minimum.

The electron density in the well n_r is given by:

$$n_r = n_{r_o} e^{-\alpha(r/r_o)^2}$$

where n_{r_o} is electron density at the well minimum, as given previously.

5.1.2.7 Trap Occupancy

The parameters, τ_e and τ_c, determine the general solution to the probability of trap occupancy, f, for time, t:

$$f = ce^{-t/\tau} + \tau/\tau_c \text{ where } 1/\tau = 1/\tau_e + 1/\tau_c$$

If a trap is initially filled, then $c = 1 - f_{eq}$ where $f_{eq} = \tau/\tau_c$, and $f_f = e^{-t/\tau} + \frac{\tau}{\tau_c}(1 - e^{-t/\tau})$; f_{eq} is the time asymptote of the trap filling probability, calculated on the basis of all the electrons in the well. If a trap is initially empty, then $c = -f_{eq}$ and $f_e = \frac{\tau}{\tau_c}(1 - e^{-t/\tau})$.

From these equations, which govern the trapping behavior of a well for a particular trap location and for a specified number of electrons in the well, the behavior of a chain of wells may be found. The response of a chain of wells to dark current is first considered.

Dark charge is assumed to appear at the first well as a Poisson distribution with respect to time:

$$\overline{D_u} \quad \frac{e^{-u}u^N}{N!}$$

where u is the time-average value of the number of carriers per pixel and N is any specific number of electrons. This is a normalized distribution function, i.e.,

$$\sum_{N=0}^{\infty} \overline{D_u}(N) = 1$$

After many packets of dark charge introduced at the first well have passed through the chain of wells, there is a probable occupancy of the trap at each well, P_i. This depends on the trap parameters for the well, on the average u of the dark charge, on the distribution function, which is not necessarily Poisson after the first well, on the dark charge entering a particular well, and on the phase times. The probable occupancy, P_i, of the i_{th} well at the time charge enters, must be the same as that at the end of the transfer interval, because the well is in equilibrium with dark charge transport.

After many cycles of transport of charge of average value, for example, any individual well will have a probability P_{in} of occupancy of its trap at the time charge is introduced. For each possible quantity N of charge introduced, there will be a probable trap occupancy, f, at the end of the cycle. This probable occupancy will depend on the initial trap condition.

For a trap initially full,

$$f_f = (1 - \frac{\tau}{\tau_c})\, e^{-t_h/\tau} + \frac{\tau}{\tau_c}$$

where t_h is the time of a phase high interval. For a trap initially empty,

$$f_e = \frac{\tau}{\tau_c}\,(1 - e^{-t_h/\tau}).$$

At the end of the full cycle, these will be:

$$f_f = e^{-t_l/\tau_e}\,[\tau/\tau_c + (1 - \tau/\tau_c)\, e^{-t_h/\tau}]$$

$$f_e = e^{-t_l/\tau_e}\,\frac{\tau}{\tau_c}\,(1 - e^{-t_h/\tau})$$

where the additional term takes into account release of charge from the trap during the phase low interval, t_l. The expressions given here use a value of τ_c that assumes the availability of all electrons for trapping at the beginning of the phase-high interval. However, if the previous electrode position contains an effective trap, one electron may arrive at some time during the phase-high interval and the capture time may in such a case be significantly larger than the value assumed here. The calculated values for f_e are, therefore, in some instances a little larger than true values and the effect of the bulk trap on trapping of low-level signals is, therefore, slightly underestimated. Only 50 of 500 wells appear to participate significantly in trapping; approximately 10% of these or 5 wells are affected in the manner described because only traps in adjacent wells are involved. It is judged, therefore, that the use of the assumed value of τ_c does not materially affect the conclusions reached for the analysis. In particular, effects at dark current values of 10 electrons per pixel should be almost negligible; effects at dark current values of one electron per pixel are estimated to be less than 20%.

For any particular number of electrons, N_j, entering a well, the probability of the trap being full at the end of the cycle is:

$$F(N_j) = P_{in}\, f_f(N_j) + (1 - P_{in})\, f_e\,(N_j)$$

where τ_c in f_e is computed for N_j electrons and τ_c in f_f is computed for $N_j + 1$ because of the charge in the trap.

Where $\bar{D}_u(N_j)$ is the weighting factor for the entering charge distribution, the average probable occupancy at the end of the cycle is:

$$P_{out} = \Sigma \bar{D}_u(N_j) F(N_j)$$

Since equilibrium is assumed $P_{out} = P_{in} = P$ and,

$$P = \Sigma \bar{D}_u(N_j) \left[P f_f(N_j) + (1 - P) f_e(N_j) \right]$$

which can be solved for P to yield:

$$P = P_{in} = P_{out} = \frac{\Sigma \bar{D}_u(N_j) f_e(N_j)}{1 + \Sigma \bar{D}_u(N_j) f_e(N_j) - \Sigma \bar{D}_u(N_j) f_f(N_j)}$$

The weighting factor $\bar{E}_V(N_j)$ of the output charge distribution is given by:

$$\begin{aligned} \bar{E}_V(N_j) &= P \left[1 - f_f(N_j - 1) \right] \bar{D}_u(N_j - 1) \\ &+ P f_f(N_j) \bar{D}_u(N_j) \\ &+ (1 - P) \left[1 - f_e(N_j) \right] \bar{D}_u(N_j) \\ &+ (1 - P) f_e(N_j + 1) \bar{D}_u(N_j + 1) \end{aligned}$$

This output distribution is then used as the input distribution for the next well. Iteration of this calculation through a chain of wells gives an output distribution from the last well which depends on the input average and distribution and on the trapping behavior and sequence of the wells in the chain.

Calculations for the case of a leading signal charge packet are carried out in the same fashion except that P_{in} for the combined signal and dark charge is taken from the output part of the $\bar{D}$ results.

Cumulative transfer efficiency η_{cum}, is calculated as:

$$\eta_{cum} = \frac{\sum_{j=o}^{\infty} \overline{S + D}_{out}(N_j) \cdot N_j}{\sum_{j=o}^{\infty} \overline{S + D}_{in}(N_j) \cdot N_j}$$

where $\overline{S + D}(N_j)$ is the weighting factor for N_j charges for the combined signal and dark charge.

The signal-to-noise voltage ratio, S/N, at the output is the square root of the power ratio and is given by:

$$S/N = \left[\frac{\sum_{j=o}^{\infty} (\overline{S + D})(N_j) \left[N_j - \overline{D}\right]^2 - \sum_{j=o}^{\infty} \overline{S + D}\,(N_j)\left[N_j - \overline{S + D}\right]^2}{\sum_{j=o}^{\infty} \overline{S + D}\,(N_j)\left[N_j - \overline{S + D}\right]^2} \right]^{1/2}$$

where the weighting factors and average charges are taken at the output of the chain of wells.

5.1.2.8 Randomization

Each of the wells in the assumed chain has its trap at a different radial position. As described earlier, the wells must be so arranged in the calculation that the order with respect to the radial trap position is random with respect to the order in the chain. To minimize computing cost, this was accomplished by first computing transfer efficiency and noise with the wells arranged so that radial trap position increased monotonically through the chain. This showed that the lowest fifty trap positions caused over ninety percent of charge losses. The set of wells was, therefore, reduced to the first eighty of the radial sequence of trap locations. This allowed adequate margin. These well positions in the chain were then randomized by means of a random-number-generator sub-routine. Forward and backward runs through the same random chain were taken; results from several runs were averaged. Finally, a pseudo-random sequence was constructed which gave nearly identical results in both directions and which gave results more pessimistic than the average of the random

calculations. This was taken as the standard method of calculation, i.e., most of the calculated results are based on single runs of a flow direction-insensitive pseudo-random sequence, which predicts a conservative result.

5.1.2.9 Results and Discussion

The objective of this analysis was to predict the effect of bulk traps on practical buried-channel area photosensors at reduced temperatures. The photosensor site was assumed to be 20 μm x 20 μm and the room temperature dark-current density was assumed to be 6 nA/cm^2. Experiments showed that the dark current decreased at lower temperatures at approximately the same rate as the intrinsic carrier concentration. For such a photosensor site scanned 30 times per second in conventional TV fashion at -50°C, the dark charge is approximately one electron per pixel. This finite dark charge is assumed in order to keep traps partially occupied and thus to minimize bulk trapping effects.

The dark charge of one electron per pixel and a signal charge of one electron per pixel at -50°C were then taken as the standard or reference condition. The trap concentration was taken as 10^{11} per cm^3, a value that was the highest that seemed reasonable from published data[4, 5, 6].

This assumption was confirmed by discussions with other deep-trap researchers. The trap cross-section assigned was 4×10^{-15} cm^2, which is typical for deep traps such as gold or platinum.

The holding time of the potential well is a critical variable because only traps with emission times near the well-holding time are capable of both trapping transient charge and retaining it. The holding time assigned was 31.476 μsec, which is the phase time at a TV line rate of 15,750 lines per second.

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(4) Chan, W.W., and Sah, C.T., Journal of Applied Physics, Vol. 42, No. 12, pp 4768-4773.

(5) Walker, J.W. and Sah, C.T., Abstract DF7, Bulletin of the American Physical Society, March 1972, p 307.

(6) Fu, H.S., Chan, W.W. and Sah, C.T., Abstract DF8, loc.cit.

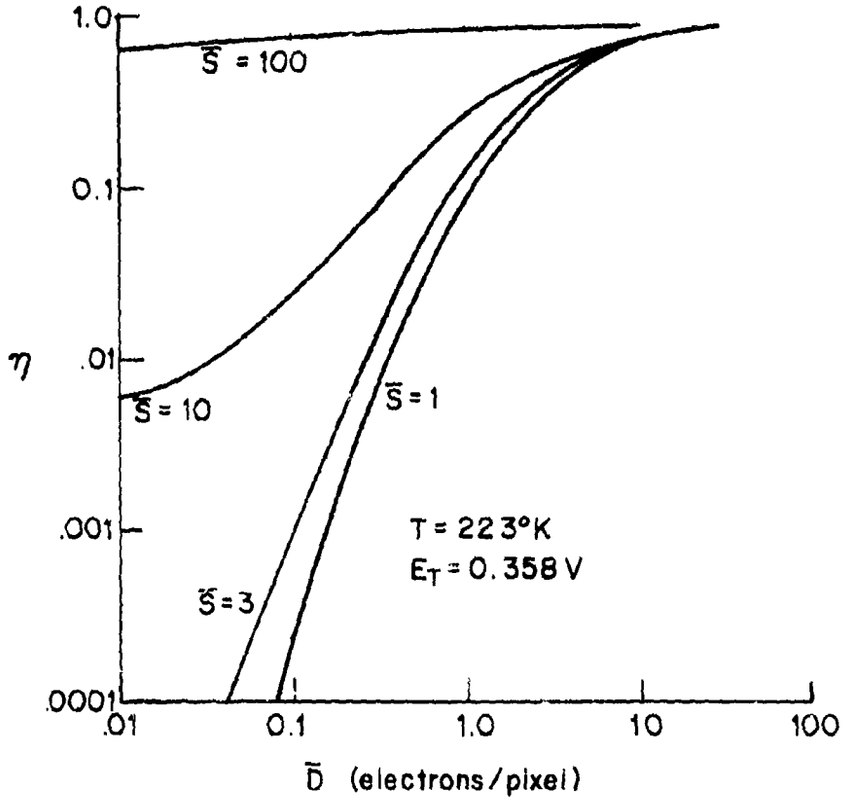

FIGURE 5-1. CUMULATIVE TRANSFER EFFICIENCY (η) VS. AVERAGE DARK CHARGE PER PIXEL ($\bar{D}$) FOR SEVERAL VALUES OF AVERAGE SIGNAL CHARGE PER PIXEL ($\bar{S}$)

With these critical parameters fixed to describe an approximate practical worst case for bulk trapping, the trap energy level, E_T, was varied in the computer program to determine the energy where the signal-to-noise ratio was the lowest. This level was found to be 0.358 V and was, therefore, used as the reference trap energy. The various parameters were then varied systematically to determine their influence on transfer efficiency and signal-to-noise ratio.

Figure 5-1 shows cumulative transfer efficiency, η, as a function of average dark charge, $\bar{D}$, for initial signal packets with average values of 1, 3, 10, and 100, and all other parameters at the standard values. Trapping effects are significant at the condition of $\bar{S} = 1$, $\bar{D} = 1$; transfer efficiency falls rapidly as the dark charge is reduced below $\bar{D} = 1$. A dark charge of 10, however, produces significant trap saturation even for $\bar{S} = 1$. All curves show an increase of transfer efficiency with an increase of dark charge. The asymptote for this example should be approximately 0.975. In all cases examined, transfer efficiency increases with dark charge as expected from physical considerations.

Figure 5-2 shows signal-to-noise voltage ratio, S/N, as a function of dark charge. It can be seen that the condition $\bar{D} = 10$, $\bar{S} = 10$ gives a signal-to-noise ratio greater than unity and approximately 63% of the maximum theoretical value of $\sqrt{5} = 2.24$ assuming both signal and dark charge are Poisson quantities. As the signal charge is increased, the dark charge at which the maximum signal-to-noise ratio is seen shifts to slightly higher values. For $\bar{D} = 10$, $\bar{S} = 100$ the signal-to-noise is more than 85% of the maximum theoretical value. The shape of the curves at low dark currents makes clear that dark charge is most important at low signal levels.

Figure 5-3 shows the variation of transfer efficiency and signal-to-noise ratio with trap energy around the minimum value for $\bar{D} = 1$, $\bar{S} = 1$. The more rapid increases toward the low trap energy side reflect the condition that as emission time becomes shorter, the trapped charge is more likely to return to the packet from which it was trapped. As trap energy increases, the trap is more likely to be filled already when the packet arrives; it is also more likely to retain any charge it traps. Figure 5-4 shows this effect strongly. The curve for $E_T = 0.358$ V is the $\bar{S} = 1$ curve of Figure 5-2. At $E_T = 0.318$ V, the signal-to-noise ratio increases monotonically as dark charge is decreased.

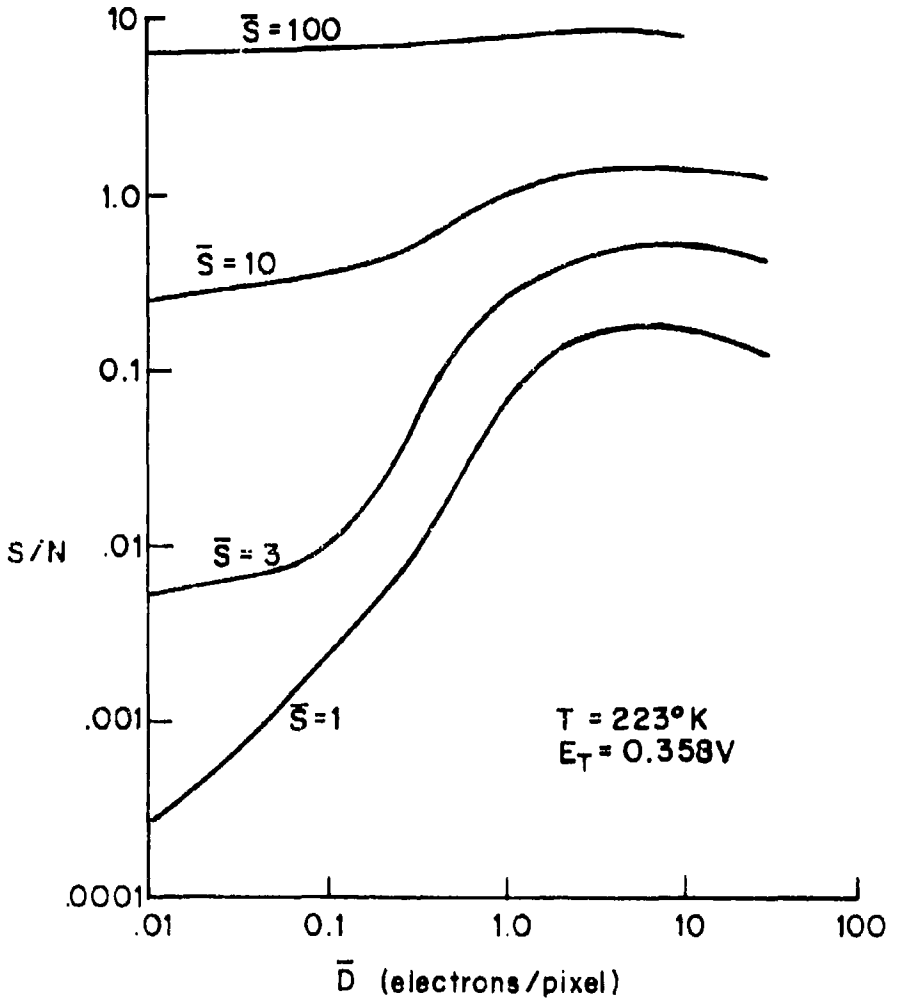

FIGURE 5-2. SIGNAL-TO-NOISE VOLTAGE RATIO (S/N) VS. AVERAGE DARK CHARGE PER PIXEL ($\bar{D}$) FOR SEVERAL VALUES OF AVERAGE SIGNAL CHARGE PER PIXEL ($\bar{S}$)

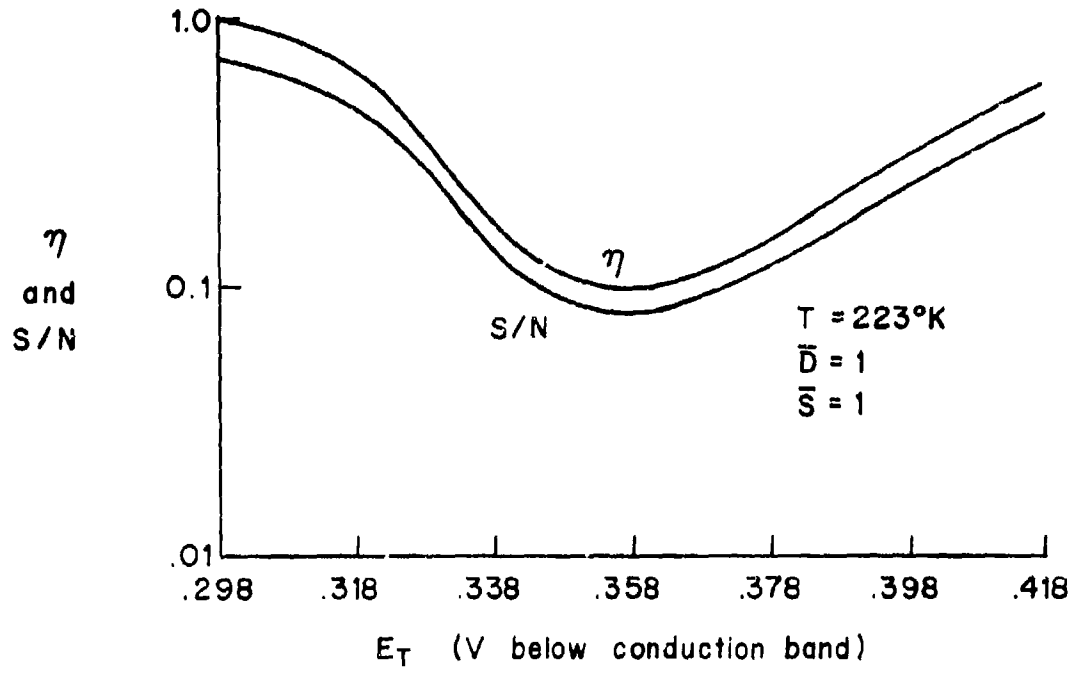

FIGURE 5-3. CUMULATIVE TRANSFER EFFICIENCY (η) AND SIGNAL-TO-NOISE VOLTAGE RATIO (S/N) VS. TRAP ENERGY (E_T)

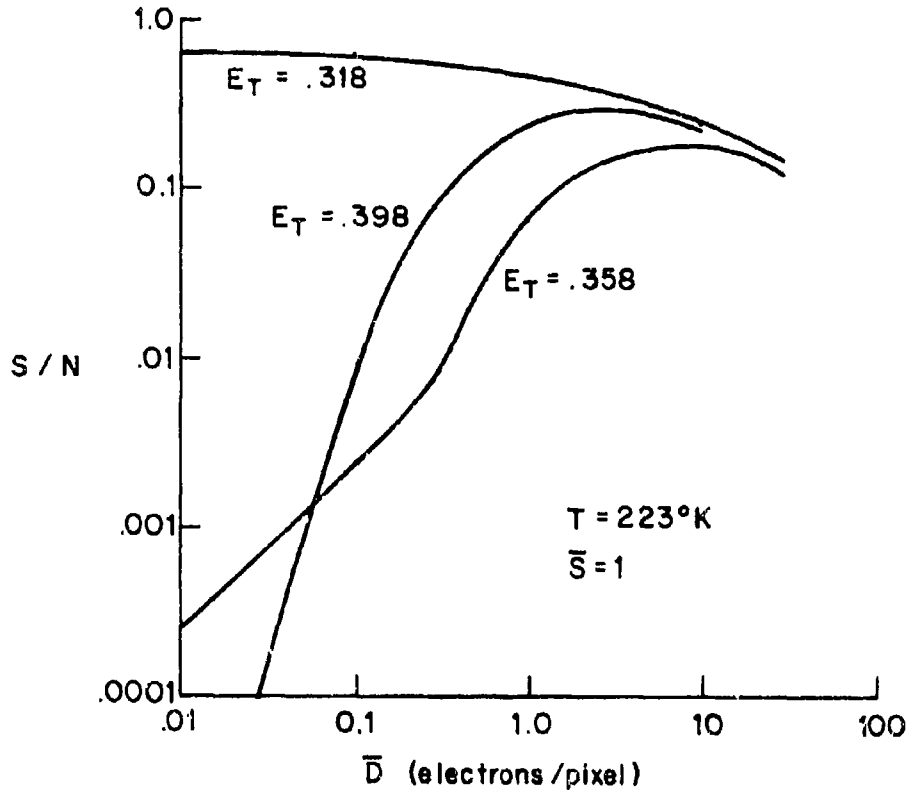

FIGURE 5-4. SIGNAL-TO-NOISE VOLTAGE (S/N) VS. AVERAGE DARK CHARGE PER PIXEL FOR SEVERAL VALUES OF TRAP ENERGY (E_T) IN VOLTS BELOW THE CONDUCTION BAND

This reflects the short emission time of the traps and the removal of dark charge from the signal packet. At the higher trap energy of 0.398 V, low dark charge results in empty traps, a corresponding lower transfer efficiency, and therefore a lower signal-to-noise ratio.

Figure 5-5 illustrates the effects of operating temperature on the signal-to-noise ratio with other parameters held constant. This includes dark charge although it is a strong function of temperature. It shows, by separation of variables,that the worst-case selection of temperature for an E_T of 0.358 V is 223°K. As the temperature increases or decreases, signal-to-noise ratio and transfer efficiency approach the high values characteristic of buried-channel devices with a low concentration of bulk traps. The strong dependence of signal-to-noise ratio on signal level for this worst-case condition is again visible.

The effects of other parameters on transfer efficiency and signal-to-noise ratio were examined by reducing their values to 10% of reference. The trap concentration, N_T, was reduced to 10^{10} per cm^3. In a separate calculation, well volume, V_W, was reduced to 10% of its standard value. In another, trap cross-section, σ, was reduced to 10% or 4×10^{-16} cm^2. The results are shown in Figures 5-6 and 5-7. The results of Figure 5-6 show that, as may be expected, the reduction of trap concentration is the most effective of these parameters for increasing transfer efficiency. It is the equivalent of shortening the CCD line from 500 wells to 50 wells. Even at a signal level of one electron, the transfer efficiency is 40% at $\bar{D} = 0.01$ and rises to almost 80% at $\bar{D} = 1$. Reduction of well volume is not as effective and should not be because the increased electron concentration of the smaller well increases the trapping probability, that is, it decreases the average capture time. Reduction of trap cross-section is the least effective since it increases emission time as well as capture time. The standard data is again the $\bar{S} = 1$ curve from Figure 5-1. Figure 5-7 shows similar results for the signal-to-noise voltage ratio.

The results discussed above treat a bright spot in a dark field. Figure 5-8 shows the results for a dark spot in an otherwise uniformly illuminated field. The uniform illumination, $\bar{U}$, is employed instead of the charge, $\bar{D}$. The dark spot is designated as a signal, $\bar{S}$, of negative sign; $\bar{S}$ is zero when its brightness is the same as the background. The solid curves connect points of equal negative signal. The dashed curves

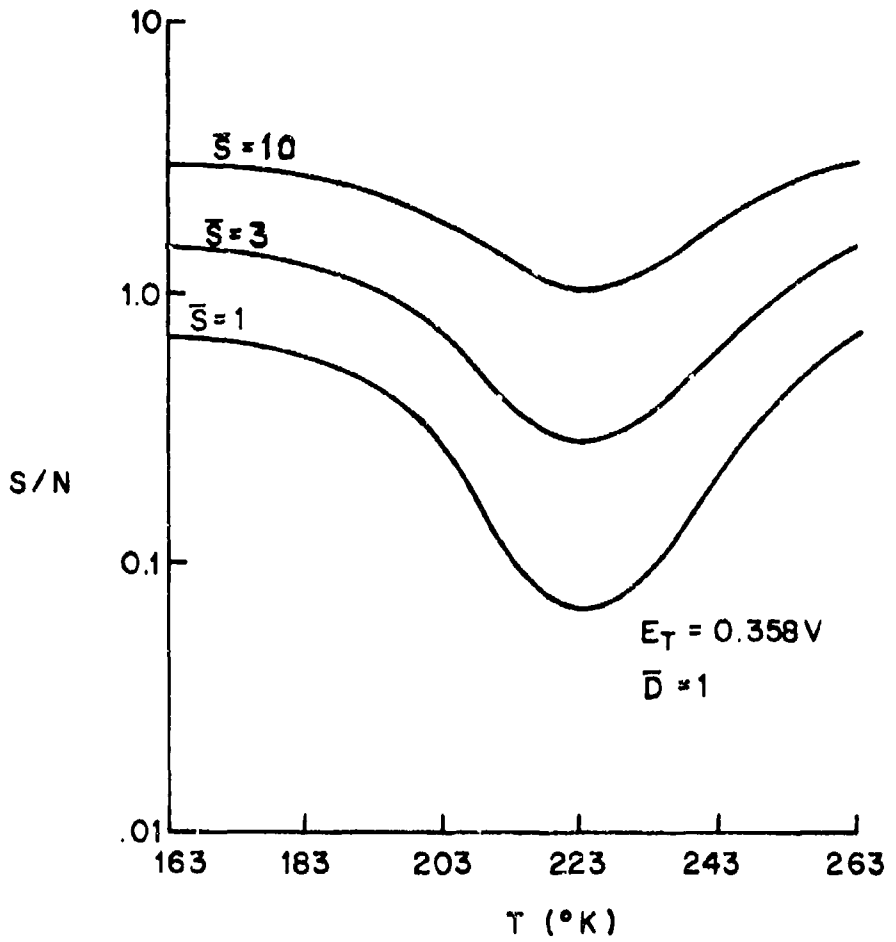

FIGURE 5-5. SIGNAL-TO-NOISE VOLTAGE RATIO (S/N) VS. TEMPERATURE(T) FOR SEVERAL VALUES OF AVERAGE SIGNAL CHARGE PER PIXEL ($\bar{S}$)

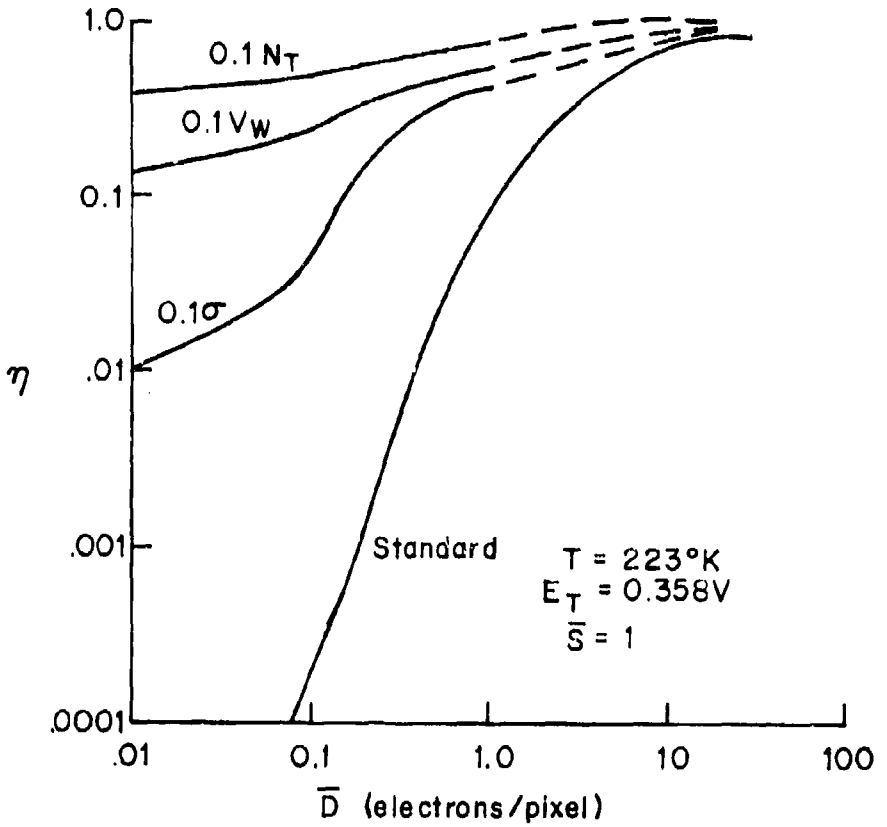

FIGURE 5-6. CUMULATIVE TRANSFER EFFICIENCY (η) VS. AVERAGE DARK CHARGE PER PIXEL ($\bar{D}$) FOR 10:1 REDUCTIONS OF CRITICAL PARAMETERS: TRAP CONCENTRATION (N_T), WELL VOLUME (V_W) AND TRAP CROSS-SECTION (σ)

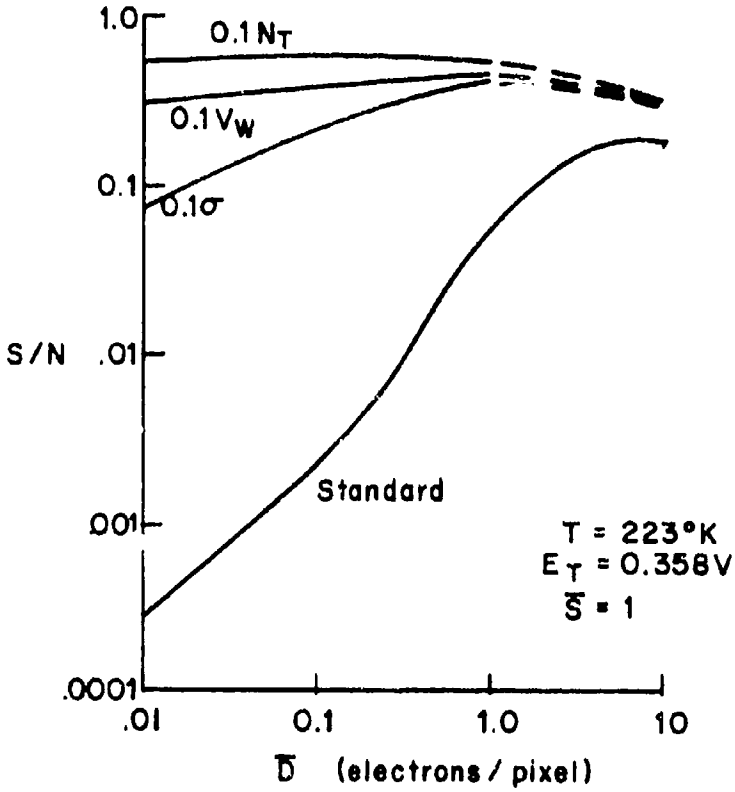

FIGURE 5-7. SIGNAL-TO-NOISE VOLTAGE RATIO (S/N) VS. AVERAGE DARK CHARGE PER PIXEL ($\bar{D}$) FOR 10:1 REDUCTIONS OF CRITICAL PARAMETERS: TRAP CONCENTRATION (N_T), WELL VOLUME (V_W) AND TRAP CROSS-SECTION (σ)

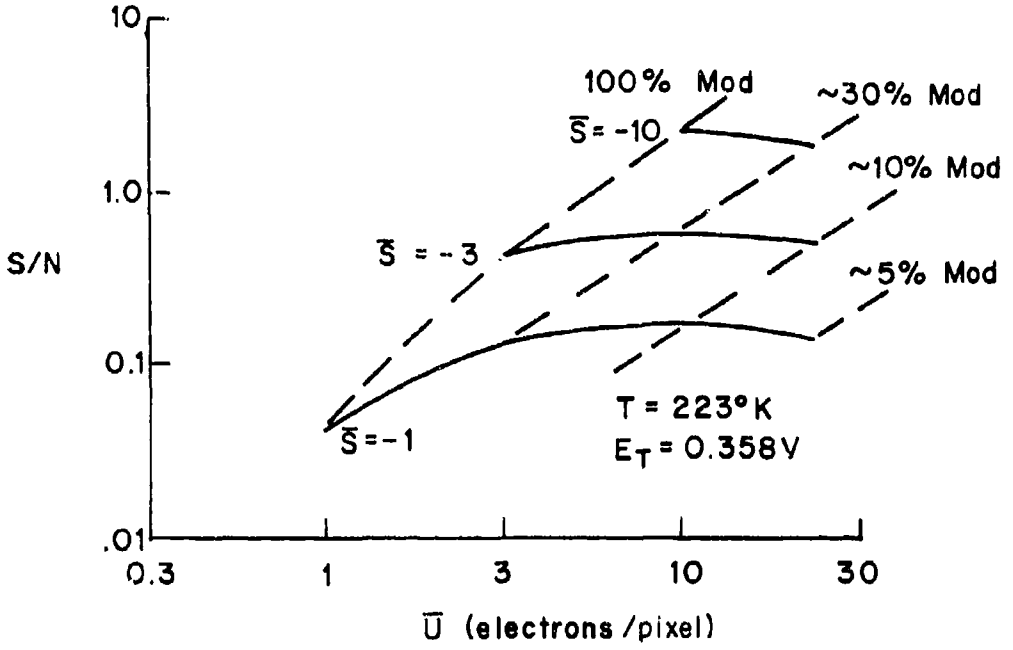

FIGURE 5-8. SIGNAL-TO-NOISE VOLTAGE RATIO (S/N) VS. AVERAGE BACKGROUND ILLUMINATION CHARGE PER PIXEL ($\bar{U}$) FOR VARIOUS VALUES OF AVERAGE DARK-SPOT NEGATIVE SIGNAL CHARGE PER PIXEL ($\bar{S}$)

Legend: ——— = $\bar{S}$
— — — = $\bar{S}/\bar{U}$

connect points of equal ratio between the negative signal and the background illumination. The curve labeled 100% modulation shows the result where the dark spot is black. For 33% modulation, the dark spot is 67% as bright as the background. For 10% modulation, it is 90% as bright. The signal-to-noise ratio at $\overline{U} = 10$, $\overline{S} = -10$ is larger than the signal-to-noise ratio for $\overline{D} = 10$, $\overline{S} = 10$, shown in Figure 5-2. In short, transmission of dark signals is comparably effective to the transmission of light signals. The transfer efficiency curves of Figure 5-9 show little difference in effective transfer of the dark spots of different amplitude. Slightly lower transfer efficiency at higher negative amplitude is expected from the lower probability of retrapping of carriers emitted into the dark spot.

Not shown in the figures are the results of an extensive study of transfer efficiency and signal-to-noise ratio at the higher horizontal register speeds. In these studies, phase time was taken as 0.1 μsec which corresponds to a 5-MHz horizontal clock. Again, the worst-case trap energy was found and parameters were varied. For a worst-case condition at $\overline{S} = 1$ and $\overline{D} = 0.0001$, transfer efficiency was 0.832 and the signal-to-noise voltage ratio was 0.912. This voltage ratio can be compared to a theoretical limit of 0.99995 for this condition. Signal-to-noise ratio, of course, decreased with an increase of dark charge, to a value of 0.627 at standard conditions where $\overline{S} = 1$ and $\overline{D} = 1$. This is approximately 10% less than the theoretical maximum of 0.707 for an ideal CCD at this point. Obviously, bulk trapping is of no consequence in horizontal registers operated at high speeds.

5.1.2.10 Conclusions

The computer study of the effect of bulk trapping at low signal level results in conclusions which support strongly the general assumptions made when the program was undertaken. These are as follows:

1) Reduction of operating temperature reduces dark charge and thereby increases the signal-to-noise ratio at low temperatures.

2) Reduction of dark current decreases transfer efficiency because bulk traps become more effective as the filling of bulk traps by dark charge is diminished.

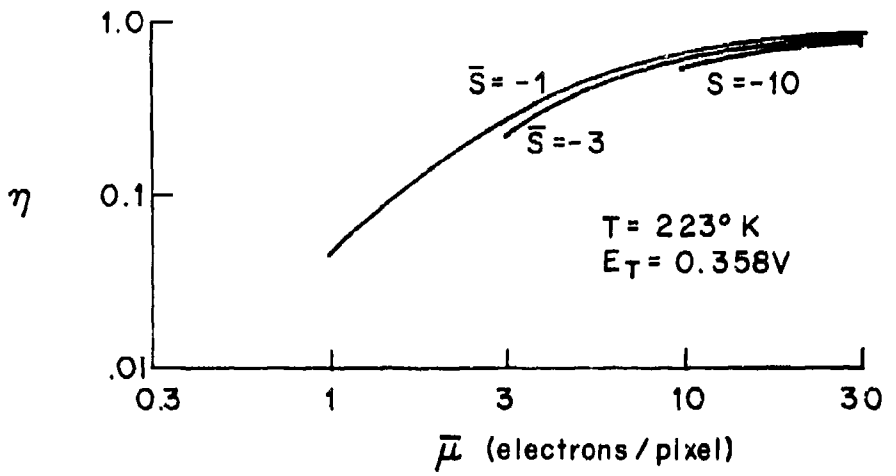

FIGURE 5-9. CUMULATIVE TRANSFER EFFICIENCY (η) VS. AVERAGE BACKGROUND ILLUMINATION CHARGE PER PIXEL ($\bar{U}$) FOR VARIOUS VALUES OF AVERAGE DARK-SPOT NEGATIVE SIGNAL CHARGE PER PIXEL ($\bar{S}$)

3) Bulk trapping can be of consequence only in long registers operated at conventional television horizontal line repetition rates, i.e., 15.750 Hz, 31.476 usec phase time for a two-phase register.

4) At the standard TV frame readout rate, a photosensor approximately 20 um x 20 um accumulates a dark charge that averages one electron per pixel at approximately -50°C. At -50°C and one electron per pixel dark charge, the worst-case trap energy is 0.358 electron volts.

5) For this temperature and trap energy, and a trap cross-section $\sigma = 4 \times 10^{-15}$ cm^2 and a trap concentration $N_T = 10^{11}$ per cm^3, operation at an average dark charge per pixel ($\bar{D}$) of 10 and an average bright-spot signal charge per pixel ($\bar{S}$) of 10 gives a useful signal-to-noise voltage ratio of 1.4.

6) Even under worst-case conditions, signal-to-noise voltage ratio in the presence of dark charge increases rapidly with signal charge; it goes to above 80% of theoretical maximum at $\bar{D} = 10$, $\bar{S} = 100$.

7) Any of several reductions of the critical parameters by a factor of 10 results in highly satisfactory signal-to-noise ratios at very low dark charge for $\bar{S} = 1$. Of these, reduction of trap concentration is the most effective, reduction of well volume is next more effective, and reduction of trap cross-section is the least effective.

8) At -50°C, traps of energy less than 0.320 electron volts or more than 0.420 electron volts are relatively inefficient traps. The increase of transfer efficiency with decreasing trap energy is more rapid than with increasing trap energy.

9) Transfer efficiency and signal-to-noise ratios for dark or gray spots are comparable to or higher than those for bright spots.

10) For a horizontal transfer rate of 5 MHz, transfer efficiency and signal-to-noise ratios in the horizontal registers are excellent under worst-case conditions.

5.1.3 Experimental Measurement of Charge-Transfer Efficiency at Low Signal Levels

A measurement has been made on the CCLID-256, at a transfer rate of 15.75 KHz, the conventional TV line rate, which shows that no more than 5 electrons are lost in a charge packet of approximately 15 electrons which undergoes 238 transfers through one of the 2-phase analog shift registers. This unit was one of several tested from a wafer-fabrication run which had uniformly higher breakdown voltages for the reset FET's. Two units from this run had low enough dark current to allow cooled operation at dark current levels below 5 electrons/pixel. Both units were tested at signal charge levels of 50 electrons or below.

A schematic of the signal processing system is shown in Figure 5-10. The central component of the system was a boxcar averager, PAR Model 162. The boxcar averager simultaneously sampled a single picture element at the two positions shown in Figure 5-11. Position "A" is the reference level where the gated diode is reset prior to receiving the signal charge. Position "B" is the level after the signal charge has passed onto the diode. In all measurements a light spot illuminating a single photoelement was manually chopped; the signal was taken as the difference between an "on" and an "off" reading.

Table 5-1 summarizes measurements made on unit 8B-W1-19. The average dark current per pixel, ≤ 4.2 electrons, was determined by turning off the reset FET for 1700 element periods and measuring the resulting integrated output. A mean signal of 16 electrons (the mean of 27 independent measurements) was observed when the light spot was positioned at photoelement 5; a mean signal of 15 electrons (the mean of 25 independent measurements) was observed when the light spot was positioned at photoelement 243. The predicted value of these two signal levels obtained from the neutral density filter attenuation factor is eleven electrons in each case.

The standard deviation, σ, and probable error of the mean P.E.M., are calculated using the expressions

$$\sigma = \left[\sum_i \frac{(\bar{x}-x_i)^2}{N} \right]^{1/2}$$

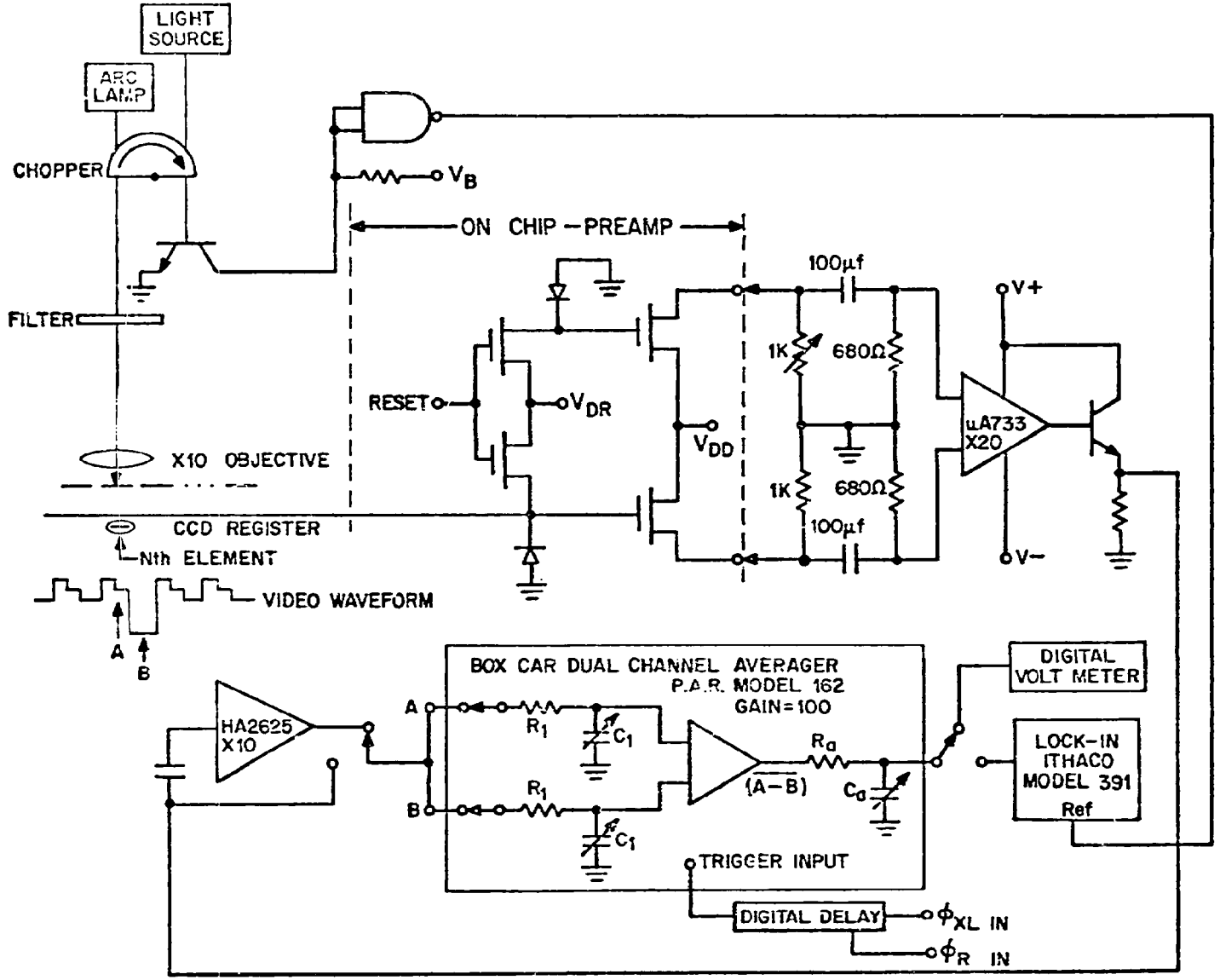

FIGURE 5-10. CIRCUIT SCHEMATIC OF THE AMPLIFIERS AND SIGNAL PROCESSORS USED IN MAKING THE LOW TEMPERATURE, LOW SIGNAL LEVEL MEASUREMENTS WITH THE CCLID-256

UNIT: 8B-W1-19

T = -87°C

F_o = 1 MHz

Scope BW = 5 MHz

Vertical Sensitivity: 1000 $\frac{\text{electrons}}{\text{division}}$

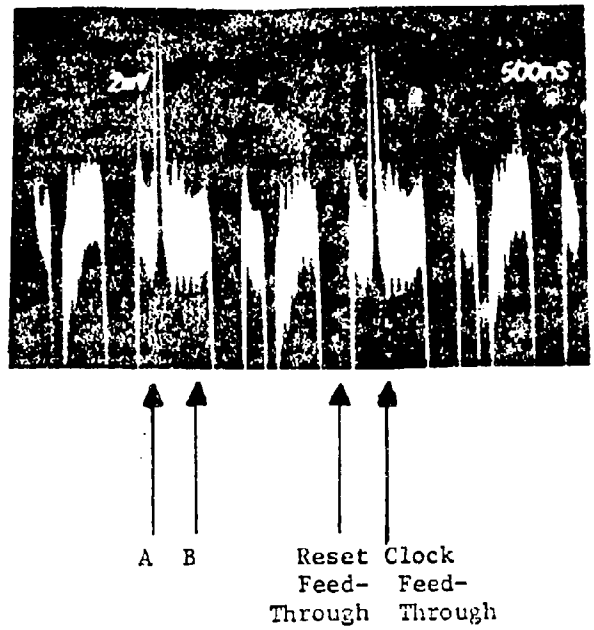

FIGURE 5-11. VIDEO TRACE AT LOW TEMPERATURE (EXPANDED SCALE)

TABLE 5-1

SUMMARY OF LOW-LIGHT-LEVEL LOW TEMPERATURE CHARGE-TRANSFER EFFICIENCY MEASUREMENTS ON CCLID-256 UNIT 8B-W1-19

f_o = 15.7 KHz

T = -110°C

$\bar{N}_{DARK}$ = 4.2 $\frac{\text{electrons}}{\text{pixel}}$

LIGHT SPOT ON PHOTO-ELEMENT NO.	NO. OF SIGNAL ELECTRONS PREDICTED	MEAN NO. OF ELECTRONS OBSERVED	STANDARD DEVIATION FROM THE MEAN ELECTRONS	NO. OF DATA POINTS	PROBABLE ERROR OF THE MEAN (ELECTRONS)	NO. OF CYCLES AVERAGED PER DATA POINT
5	11	16	28	27	3.6	40
243	11	15	25	25	3.4	40
Total observed electron loss --------		1	Probable error of total----		5	

and

$$P.E.M. = \frac{0.67}{\sqrt{N}}$$

where N is the number of measurements.

The P.E.M. value establishes a 50% confidence level that the actual mean is within ± P.E.M. of the measured mean. These data show that the charge loss in the CCD register region between the two photoelements tested is 1 ± 5 electrons. The two distributions of data points obtained from illumination at the front and rear of the array are shown in Figure 5-12.

Table 5-2 presents partial data taken on the second unit, 8B-W1-2, with the light spot remote from the amplifier at photoelement 209. At the conditions of this test the average dark current was ≤ 0.9 electron per pixel. At the 250-electron level no deviation of the observed signal charge from the predicted signal charge was observed with a P.E.M. of ± 12 electrons. At the 50-electron level there was a 25-electron deviation from the predicted value.

If small amounts of light from the unattenuated beam can leak around the neutral density filters, the observed charge may be considerably higher than predicted. In order to estimate the size of this error, the light spot was attenuated by another order of magnitude by inserting a neutral density filter "N. D. 6" (attenuation of 10^6 X) in place of the usual "N.D. 5" (attenuation of 10^5 X). Figure 5-13 presents the results of three sets of measurements as histograms. The first two histograms were made with the N. D. 5 filter. For the second histogram the number of samples averaged by the boxcar averager was increased by a factor of 10. The mean values agree within 10%. Ideally, an improvement of σ by a factor of $\sqrt{10} \simeq 3$ is expected; actually a factor of two improvement was observed. The third histogram for N.D. 6 filter shows that any light leakage or calibration error at this signal level is very small, < 4 ± 6 electrons, and does not appreciably affect previous conclusions.

In conclusion, a loss of less than 5 electrons for a 15 ± 5 electron signal after 238 transfers has been observed in the CCLID-256 device at a dark current of ≤ 4 electrons per pixel. Precise determination of this value was limited by accuracies of approximately ± 5 electrons.

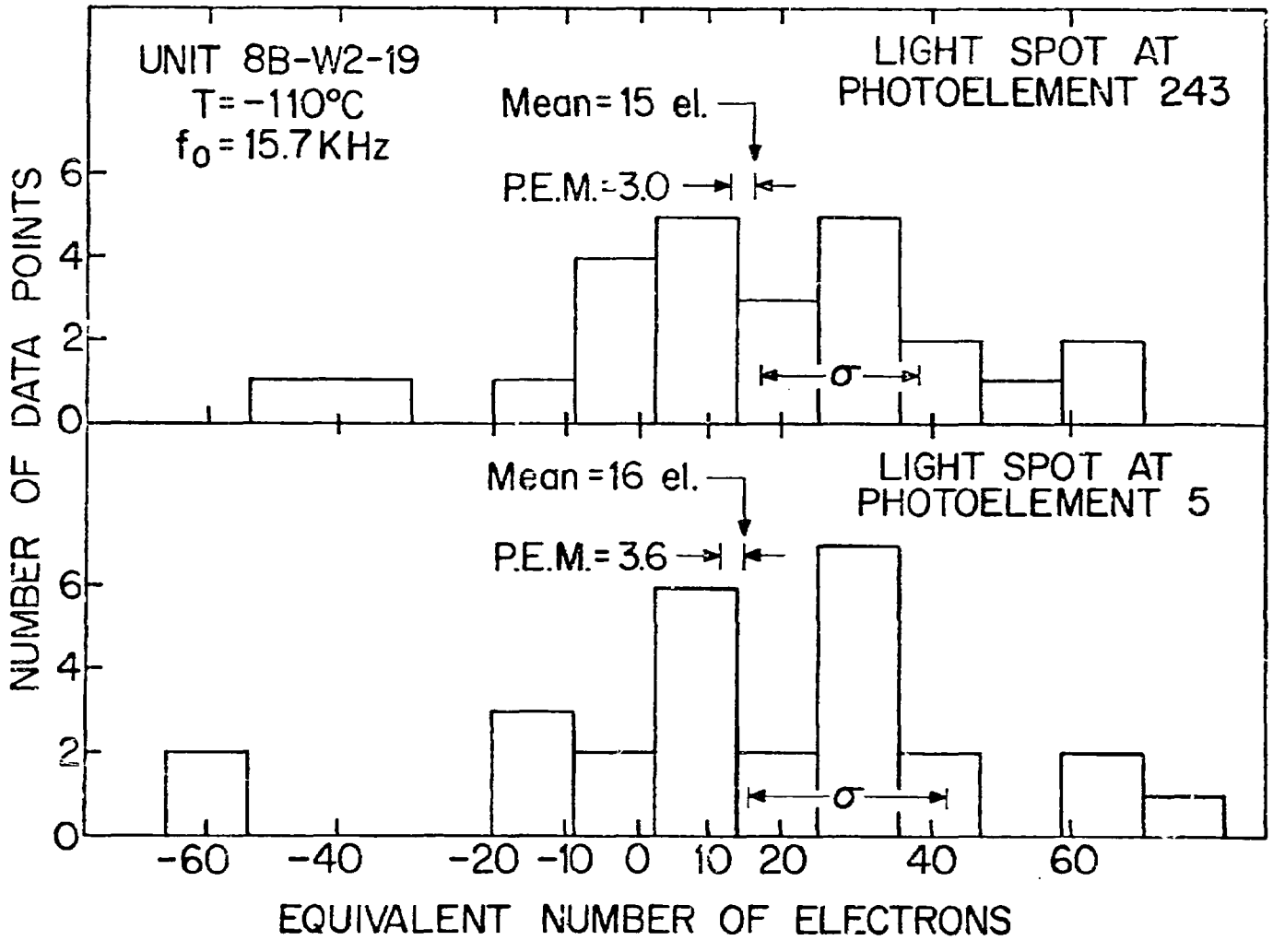

FIGURE 5-12. HISTOGRAMS OF PROCESSED SIGNAL FROM LIGHT SPOT AT PHOTOELEMENT 243 (TOP) AND PHOTOELEMENT 5 (BOTTOM). Dark current for this unit at -110°C was 4.2 electrons/pixel

TABLE 5-2

SUMMARY OF LOW-LIGHT-LEVEL LOW TEMPERATURE CHARGE-TRANSFER EFFICIENCY MEASUREMENTS ON CCLID-256 UNIT 8B-W1-2

f_c = 15.7 KHz

T = -90°C

$\overline{N}_{DARK}$ = 0.9 ± 0.3 $\frac{\text{electrons}}{\text{pixel}}$

LIGHT SPOT ON PHOTO-ELEMENT NO.	NO. OF SIGNAL ELECTRONS PREDICTED	MEAN NO. OF ELECTRONS OBSERVED	STANDARD DEVIATION FROM THE MEAN ELECTRONS	NO. OF DATA POINTS	PROBABLE ERROR OF THE MEAN (ELECTRONS)	NO. OF CYCLES AVERAGED PER DATA POINT
209	250	250	50	10	12	40
209	75	50	13	5	4	40

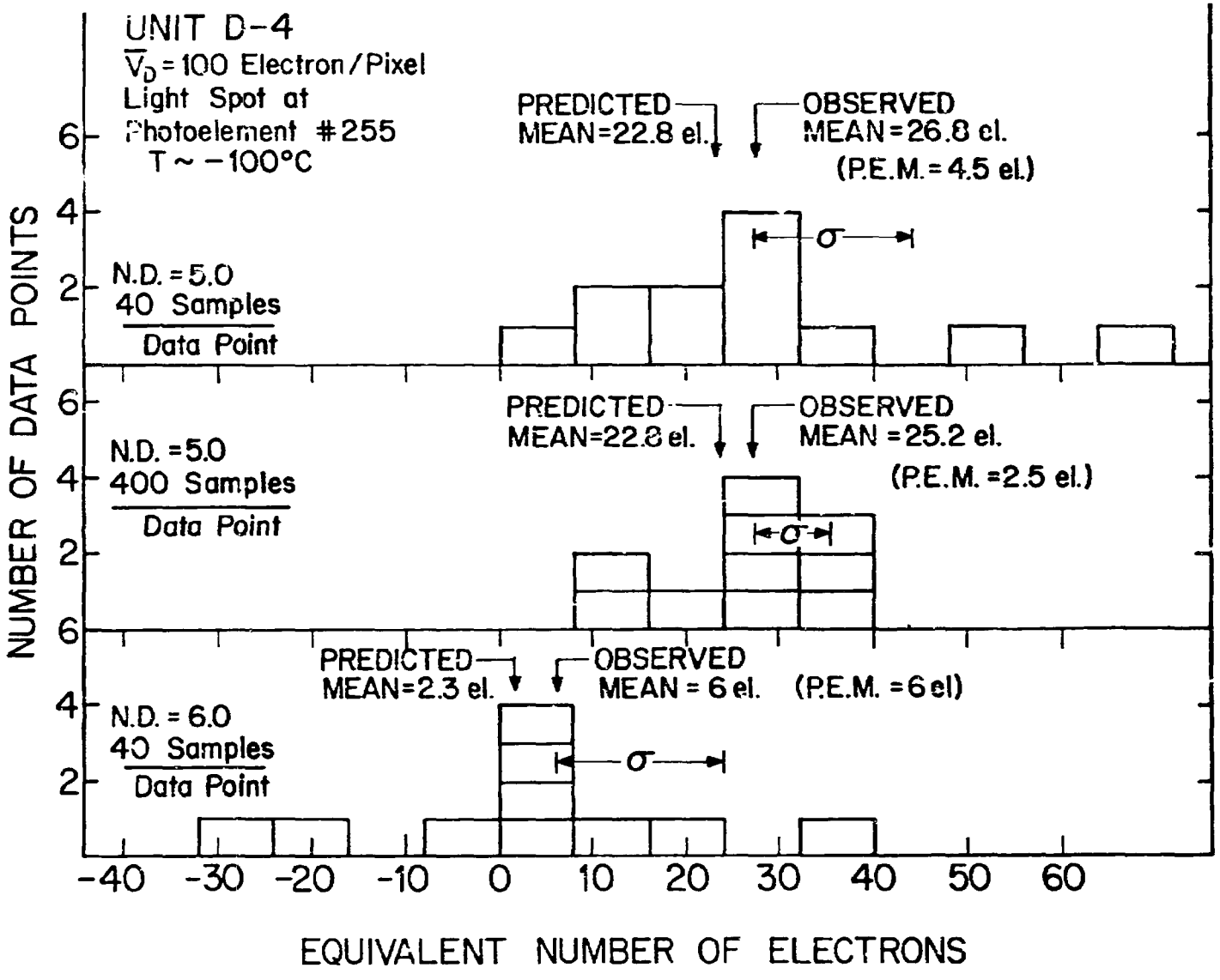

FIGURE 5-13. HISTOGRAM OF PROCESSED SIGNAL FROM LIGHT SPOT AT PHOTOELEMENT 255. The first and second figures were taken with a neutral density (N. D.) filter with 10^{+5}X attenuation. The middle figure shows the reduction in the spread of the distribution with a factor of 10 more samples/data points. The lower figure taken at N. D. 6 sets a limit to any zero offset due to light leakage.

This result is consistent with the theoretical prediction that there is sufficient cumulative transfer efficiency to transfer a signal averaging ten electrons/pixel through 500 transfers, at 15.75 KHz, at a dark charge level of ten electrons/pixel. It may also be concluded from these measurements that sources of signal loss other than bulk trapping in this charge-coupled device are small.

5.2 DISTRIBUTED FLOATING-GATE AMPLIFIER (DFGA) PROGRAM

The incorporation of the DFGA in charge-coupled area image sensors is the key element for obtaining very low-light-level response. The development of this device was supported by an independently funded program. In view of the importance of this effort to the NESC Phase II program, the Final Report of the DFGA Program is included in Appendix A of this report. The following is a reprint of the Summary and Conclusions from the DFGA report.

The concept of the floating-gate amplifier offers two principal advantages over the gated-charge integrator, which is conventionally employed as an on-chip detector-preamplifier for charge-coupled devices. The first advantage is that the floating-gate amplifier does not require a reset function, which introduces a large kTC noise component in the gated-charge integrator. The second advantage is that a charge packet may be sensed nondestructively in a CCD channel by a floating gate. In the distributed floating-gate amplifier (DFGA), a charge packet is sensed repeatedly as it passes through a CCD channel. The input signal is thereby multiplied by the number of stages employed, while the noise is increased by the square root of the number of stages used.

This report describes the design and evaluation of a 12-stage distributed floating-gate amplifier. The device possesses an input CCD channel with 12 floating gates. Each of these gates are common elements of 12 MOS transistors, which are inverting charge amplifiers. Charge from these amplifiers is gated into an output CCD channel, where the amplified signal charge is summed as it moves through this channel in synchronism with the charge in the input channel. This summed signal is then sensed by a floating-gate amplifier at the end of the output channel.

In this design the floating-gate geometry was optimized for maximum signal-to-noise ratio. The optimum operating point of the charge amplifier was then determined for this geometry. The output register was designed to store the maximum charge from all 12 charge-amplifier stages.

It is concluded from a noise analysis that shot noise in the charge amplifier is the dominant noise source in the DFGA. The noise level for all significant noise sources is predicted for the operating parameters, clock frequency and the time that the charge amplifiers are activated. It is seen that a noise equivalent signal of 17 electrons is theoretically possible for a charge-amplifier active (or on) time of 50 nsec, which corresponds to a maximum bit rate of 8 MHz.

Experimental characterization of the device showed excellent agreement with the theoretical predictions at small signal charge levels. A noise equivalent signal (NES) of 10 to 20 signal electrons was obtained at room temperature for a 50 nsec charge-amplifier activation time; and for a 3 MHz bandwidth. At high signal level, a saturation characteristic softer than predicted was observed. This effect is probably caused by charge-spreading under the floating gate at these high levels.

Experiments were conducted to identify the dominant noise source. Since the noise was found to be proportional to the square root of the total charge in the output register, it is concluded that the dominant noise source is the shot noise of the charge-amplifier in agreement with the noise analysis.

5.3 SPECTRAL RESPONSE

5.3.1 Calculations from Models

5.3.1.1 Introduction

This section treats the optimization and characterization of the spectral response of top-side illuminated charge-coupled imaging devices. Specifically, it treats the two layer polysilicon structure employed in two of the area imaging devices described in this report, the CCAID-100 BD and the CCAID-244A. This two-layer polysilicon structure with its associated dielectric layers is uniform across the area of each photoelement. In the two other area imaging devices described in this report, the CCAID-244B and the CCAID-488A, nominally one-third of the photoelement area has only a single layer of polysilicon; therefore, the optimized spectral response is expected to be higher at all wavelengths in these devices.

5.3.1.2 Example of a Computed Transmittance Spectrum

In this investigation, the optimization of the spectral response was carried out with the aid of a computer program that determined the transmittance of a multilayer structure over the spectral range from 0.4 to 1.2 μm in 0.01-μm intervals. The computer program assumed constant refractive index for silicon dioxide and silicon nitride and took into account the changing refractive index and absorption coefficient of silicon with wavelength. The polysilicon layers were assumed to have the same optical properties as bulk silicon. Although this is a good assumption, light scattering effects in the polysilicon layers are expected to modify the computed results to some extent. The computer program treated collimated light. Normal incidence was used in most cases; a few runs were made at angles up to 30 degrees from normal incidence.

Figure 5-14 shows an example of an optimized transmittance spectrum predicted by the program. The figure includes the layer thicknesses that were used, and shows the spectral band that was being optimized. This spectrum contains three maxima at close to 80% transmittance, two minima (0.5 to 0.9 μm region) at close to 25% transmittance, and an average transmittance over the otpimized band (0.73 to 0.90 μm) of 70%. These results show, by example, what can be achieved with two-layer polysilicon structures. This spectrum also shows an example of an extremely low minimum in this case, of less than 10% at 1.0 μm. Each computed transmittance spectrum contained at least one such very low minimum.

5.3.1.3 Spectral Response Optimization

In view of the complex nature of the transmittance spectra, and the extreme effects that can occur, it is preferrable to optimize for particular illumination conditions. This means either optimizing for a single wavelength, for a spectral band, or, ultimately, optimizing a convolution of the resultant response spectrum of the device and a selected illumination spectrum. The optimized band of 0.73 to 0.90 μm in Figure 5-14 was selected as a first iteration in optimizing the total response for night sky illumination conditions. The night sky spectrum extends from approximately 0.73 μm to beyond the long-wavelength response edge of silicon. The optimizing band was truncated at 0.9 μm as a result of trade-off considerations between optical crosstalk at the longer wavelengths and average in-band response.

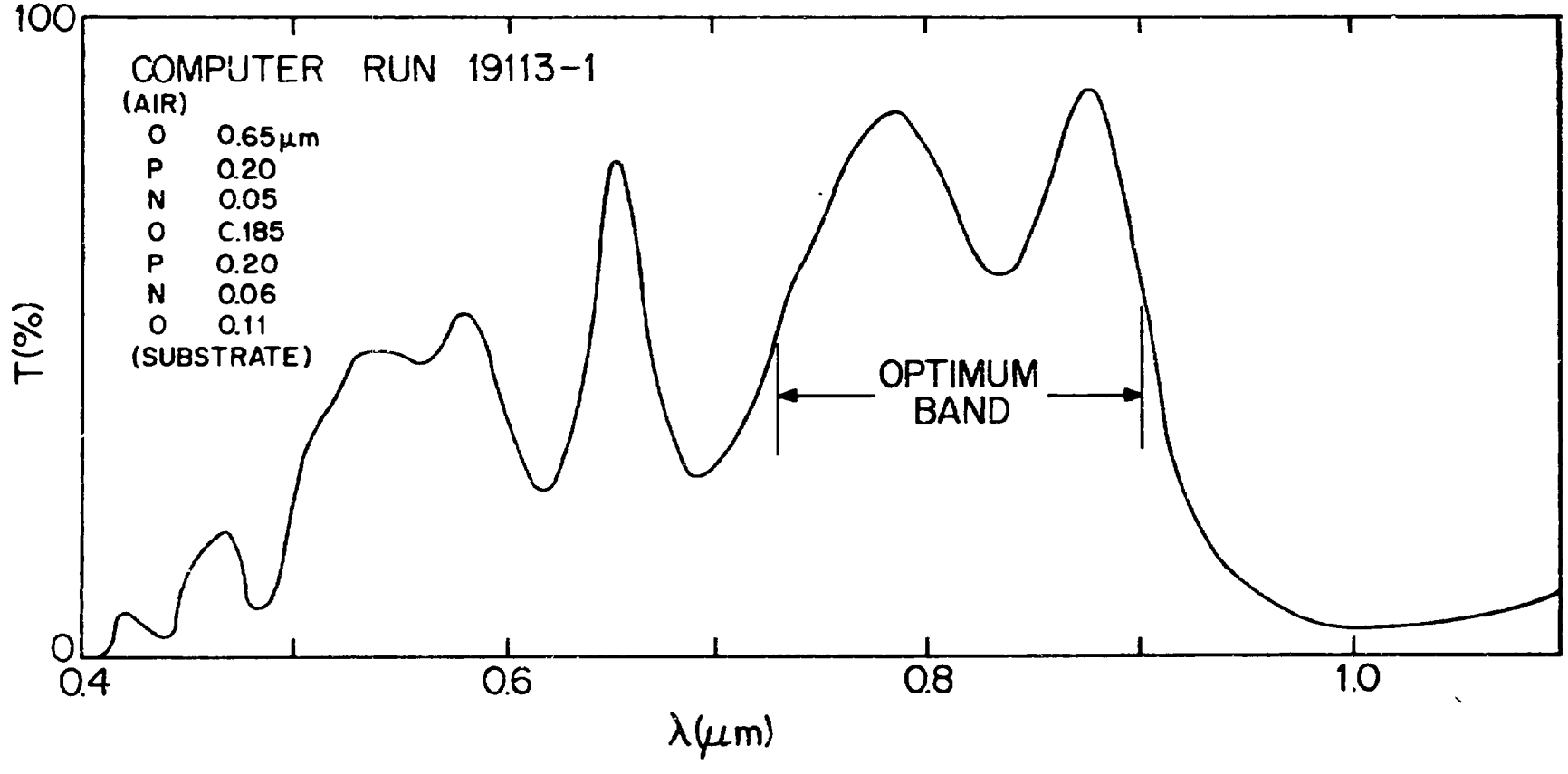

FIGURE 5-14. A COMPUTED TRANSMITTANCE SPECTRUM FOR A CCAID STRUCTURE
(P = polysilicon, O = silicon dioxide, N = silicon nitride)

A second aspect of optimization is that of specifying the number of layers, the sequence and the thicknesses that may be considered. In the example of Figure 5-14, the layer sequence was specified, and practical thickness constraints were imposed. Also, thickness control tolerances were introduced into the computer investigation to avoid hyper-critical thickness conditions.

5.3.2 Experimental Results

Figures 5-15 through 5-18 show measured spectral response curves for four devices from two wafer-fabrication runs, which were made following the computed layer-thickness specifications and using normal process-control procedures. It may be seen that one of the runs, X5, (Figures 5-15 and 5-16), has approximately the desired broadband response shape in the range of 0.73 to 0.90 μm. The spectra of the second run, X6, show a poorer approximation to the computer results. Although absolute response data for these units are preliminary, they indicate that the peak quantum efficiency is approximately 40 percent. A close microscopic examination of these devices revealed that all four samples suffer from light scattering in the lower polysilicon region. This phenomenon may explain the failure to achieve the predicted high transmittances and quantum efficiencies.

The effect of angle of incidence on spectral response was investigated both with the computer program and by experiment. At 30° from normal incidence, the three highest peaks in Figure 5-14 shift by less than 0.02 μm and the peak transmittances change by less than 3 percent. The experimental investigation consisted of comparing spectra taken with f/6 and f/2 optics. No substantial difference was seen in either the magnitudes of the peaks or of the minima.

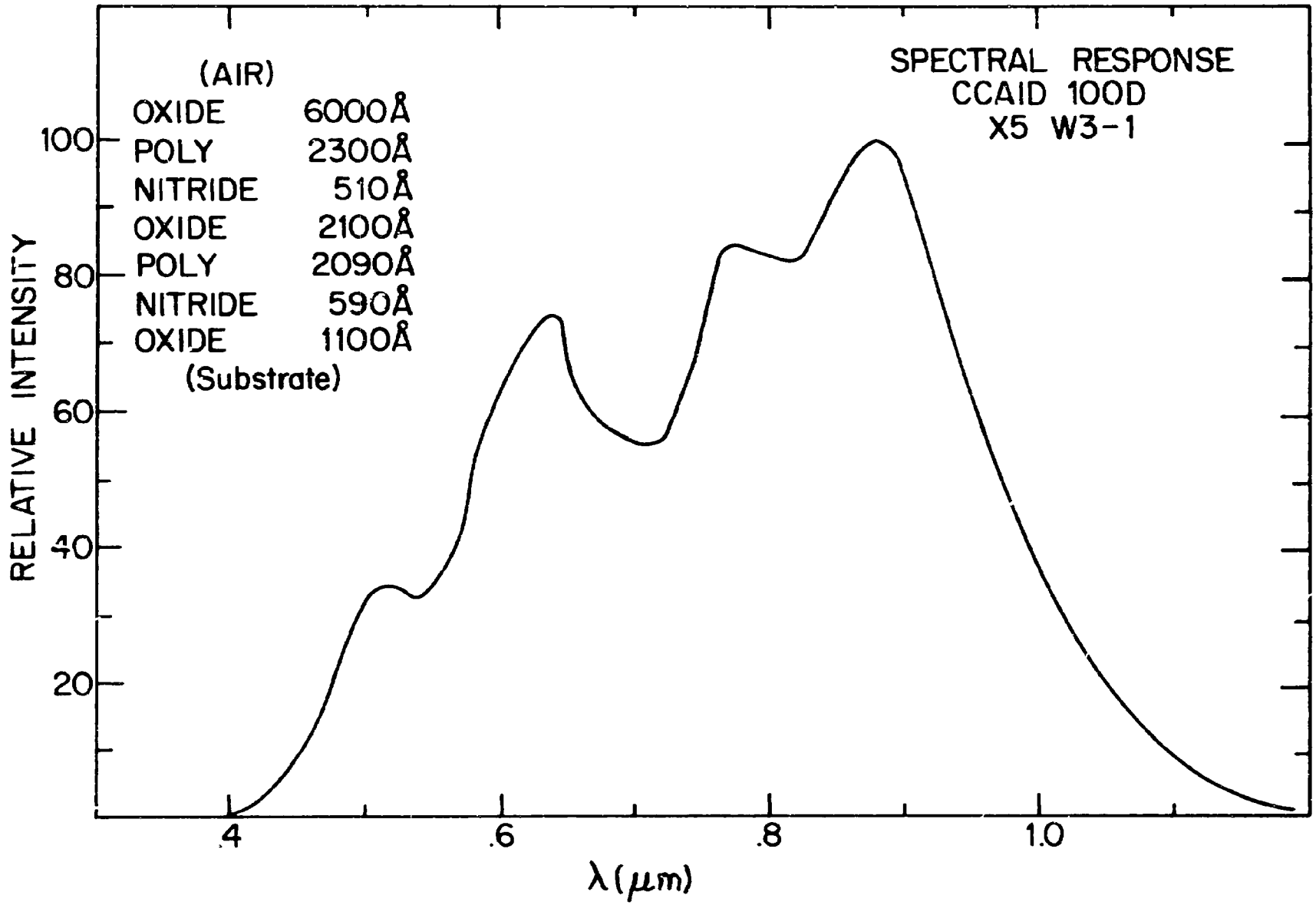

FIGURE 5-15. MEASURED RELATIVE SPECTRAL RESPONSE CURVE FOR CCAID-100D, X5-W3-1

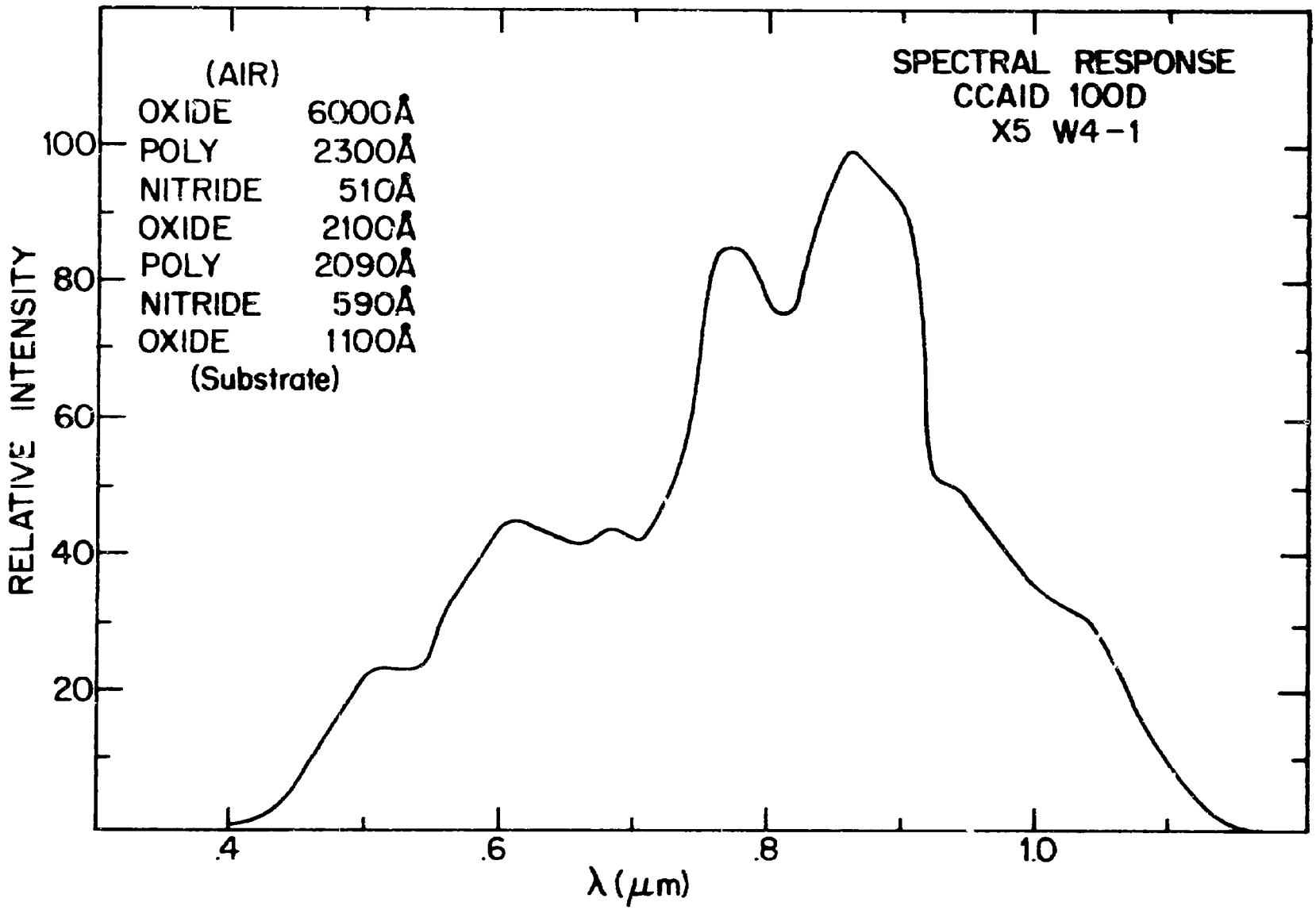

FIGURE 5-16. MEASURED RELATIVE SPECTRAL RESPONSE CURVE FOR CCAID-100D, X5-W4-1

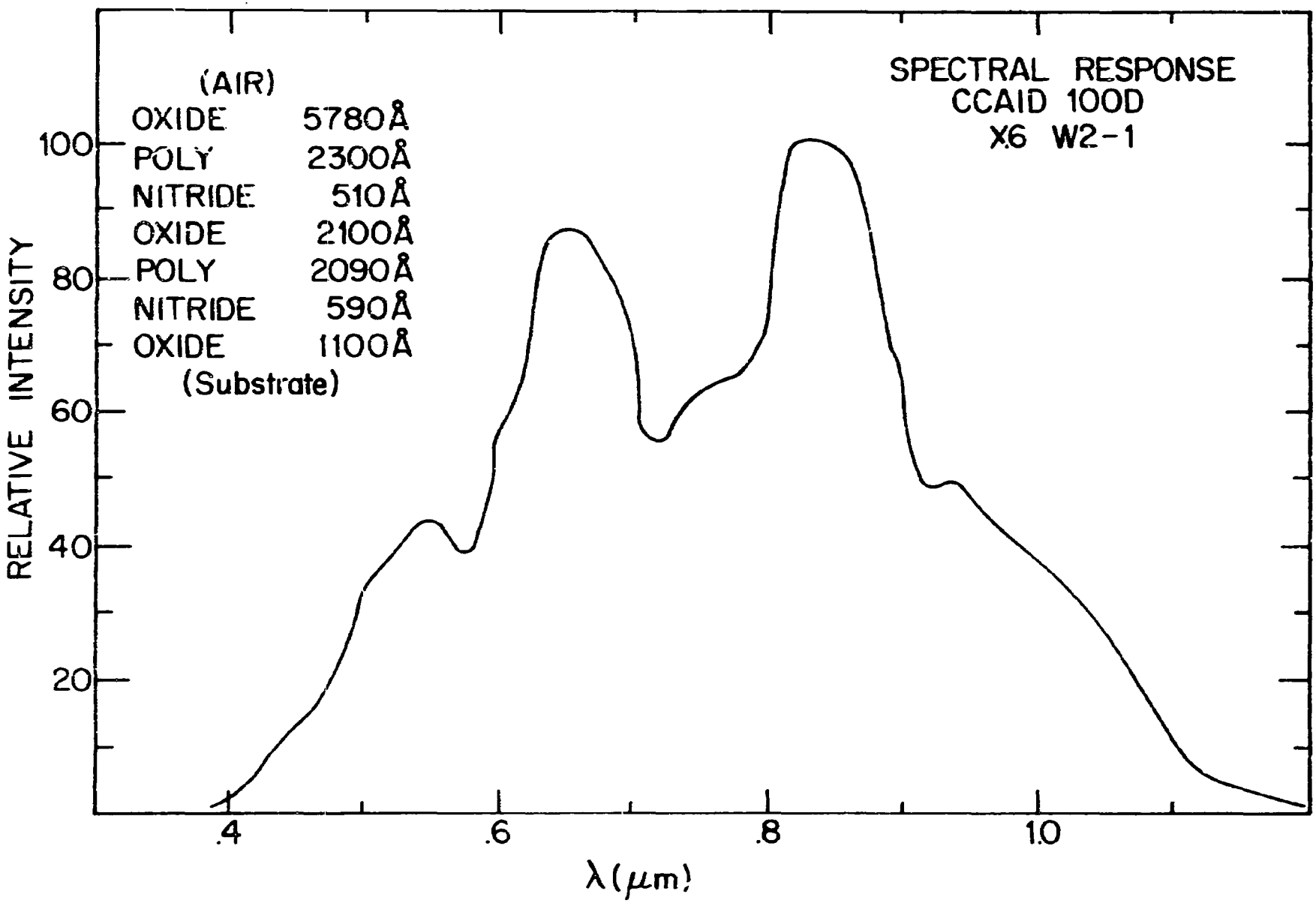

FIGURE 5-17. MEASURED RELATIVE SPECTRAL RESPONSE CURVE FOR CCAID-100D, X6-W2-1

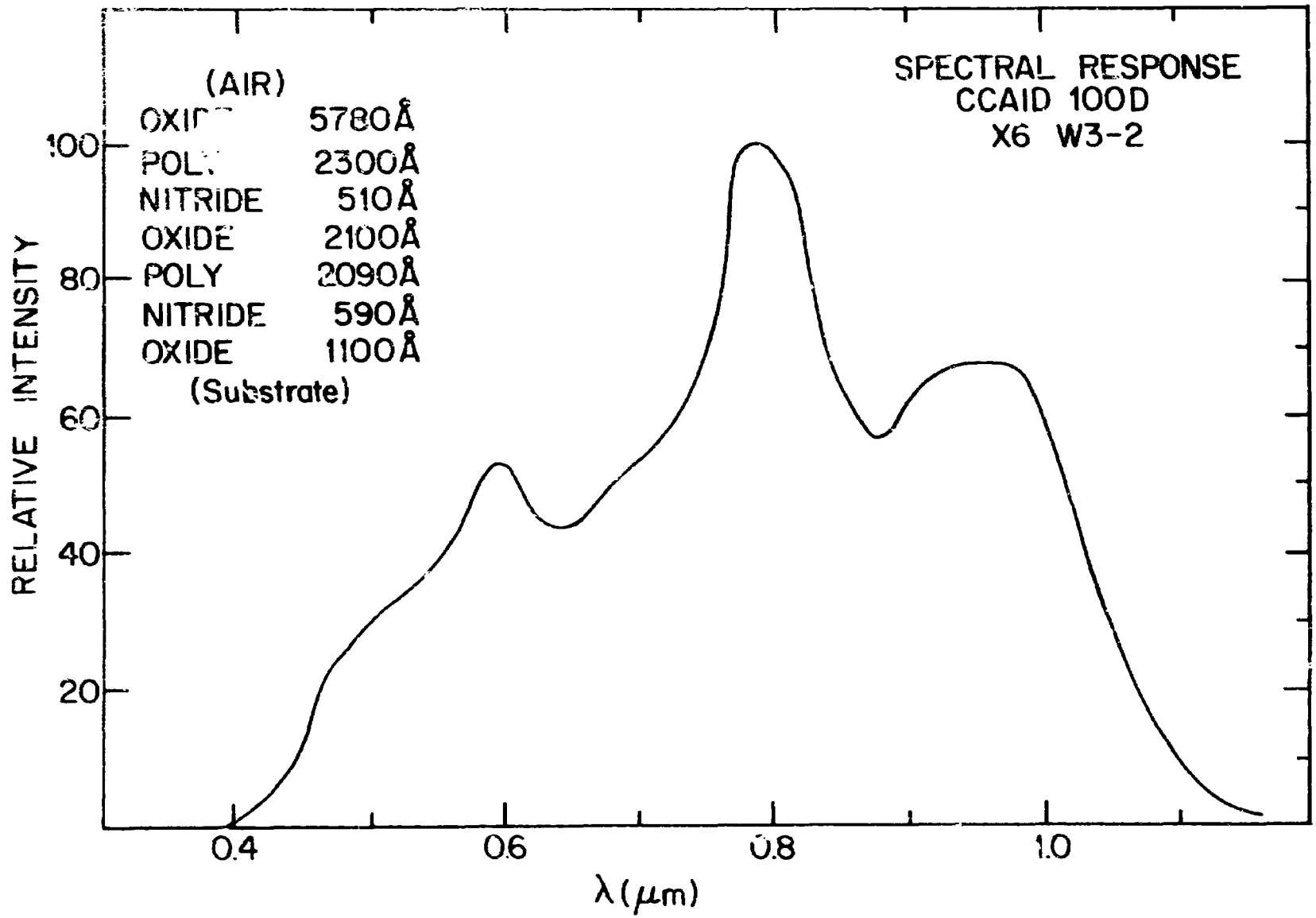

FIGURE 5-18. MEASURED RELATIVE SPECTRAL RESPONSE CURVE FOR CCAID-100D, X6-W3-2

SECTION 6

TECHNOLOGY PARAMETER STUDIES

6.1 SCOPE OF INVESTIGATION

Of those factors that impede CCD low-light-level image-sensor performance at its theoretical limit, dark-current nonuniformity caused by dark-current spikes is the most significant. In support of the NESC low-light-level CCD image sensor program, Fairchild Camera and Instrument, therefore, sponsored a long-term investigation of dark-current spikes. This investigation included the use of analytical techniques for identification of sources of dark-current spikes and process techniques for the elimination of these sources. The following sections describe initial efforts toward obtaining these goals.

One source of dark-current spikes has been correlated with a high density of stacking faults which appear after thermal processing. The nucleus of a fault is believed to be damage or stress in the silicon wafer. A method that is capable of identifying small amounts of stress in single-crystalline silicon is the x-ray double crystal diffraction technique. The initial investigations are described in Section 6.2.

Another source of dark-current spikes is a high localized concentration of contaminants. Ion microprobe mass analysis was tried as a method to identify and to locate contaminant species. Initial efforts with this analytical technique showed an unexpectedly high concentration of copper in the vicinity of the oxide-silicon interface in a processed wafer. The experimental data are given in Section 6.3.

Section 6.4 describes a set of experiments to study defects in single-crystal silicon that may be introduced during processing. Silicon wafers that were subjected to thermal oxidation to produce gate dielectric were withdrawn from the oxidation furnace at different rates. Subsequent capacitive storage-time measurements indicated different results that depended on both the rate of cooling and the initial contamination level of the silicon employed in the experiments.

6.2 X-RAY DOUBLE CRYSTAL DIFFRACTOMETER ROCKING CURVE STUDIES

In the early stages of this program, a detailed failure analysis was performed on a CCAID-100 device which exhibited an unacceptable high density of dark-

current spikes. The results of this analysis confirmed earlier studies and showed a strong correlation between stacking-fault defects and dark-current spikes.

A possible cause for stacking-fault generation during device processing is the relieving of residual damages associated with the surface preparation techniques used to slice and polish wafers prior to device processing. Another possible cause for stacking-fault generation during device processing is the relieving of residual stresses associated with the crystal growing process.

An extremely sensitive technique for studying the structure of nearly perfect crystals is double crystal diffractometry. This method can be used in a transmission mode to study bulk effects and in a reflection mode to study surface effects. As part of this program, a study was undertaken to determine if x-ray double crystal diffractometry can be developed as a non-destructive means of determining levels of residual polishing damage and/or bulk strain effects in the starting materials used to fabricate charge-coupled devices.

The basic differences between single crystal diffractometry and double crystal diffractometry is, as the name implies, the use of a second crystal in the double crystal method. Incident x-rays are diffracted off the first crystal, which must be almost perfect, to provide a parallel, angularly narrow, monochromatic x-ray beam for the second or test crystal to defract. Depending on several geometrical factors, the angular width of the x-ray beam incident on the second crystal may be as low as a few hundredths of a second of arc.

If a test crystal is aligned to diffract this beam at peak efficiency, parts of the crystal that are tilted with respect to the aligned portion by more than the beam divergence will not defract. Therefore, when the crystal is rocked or rotated through the Bragg angle, the half width of the resulting peak then becomes a very sensitive measure of the amount of lattice distortion in the test crystal.

In the first phase of this study, silicon wafers were selected from different lots of incoming material which previously had indicated a high probability of either generating or not generating stacking-faults during subsequent oxidation. Wafers from each type of material were selected and scribed in half. Half of each wafer was then given the standard oxidation test for stacking-fault generation. These tests confirmed previous results and generated samples with either high or low stacking-fault densities.

Table 6-1 presents typical stacking-fault density and x-ray half-width data obtained from both types of a sample used in this study. These data show no significant difference in the x-ray half width measured on wafers possessing either high or low potential for stacking-fault generation during subsequent processing. These results were unexpected; it was thought that back side damage may have been influencing the results. Therefore, the measurements were repeated using a front side reflection technique rather than the standard transmission technique previously used. Table 6-2 shows results of this experiment. Although a slight decrease in the half width was observed, overall no significant difference was seen using the reflection technique. In another experiment wafer 60-10C, a low stacking-fault potential wafer, was chemically etched on both sides to remove approximately 20 microns from each side and thus any residual surface damage that might have been present and influenced the half width values. As seen in Table 6-2 this process did not result in a significant reduction in the x-ray half width values.

The result of these initial investigations indicated that no significant difference in the x-ray rocking curve half widths could be determined for samples possessing either high or low probability for stacking-fault formation during subsequent processing. However, of more importance at this stage of the investigation was the indication that all of the wafers had very broad half widths; typically greater than 37 seconds of arc. These values compare with the expected values of less than 25 seconds of arc which are routinely observed for both Czochralski and float-zone silicon (ref. [1]). It is possible that the effect which gave rise to the large half width values may have also masked out the effect responsible for the differences in the stacking-fault data.

Since the initial investigation was conducted on a relatively small sample size and indicated relatively large amounts of residual stress in our starting material, a larger sample of wafers was randomly selected and submitted to x-ray rocking curve analysis. Approximately 25 microns were chemically etched from the back side of each wafer prior to investigation, to minimize any effects associated with back-side preparation techniques. Table 6-3 presents half width data measurements made by transmission for these wafers. It can be seen that none of the Fairchild-supplied wafers were as good as the control wafers used in this experiment. With the exception of wafers F and G, however, this batch of wafers showed smaller half widths than those previously seen. It can also be seen by reference to Table 6-3 that wafer G has an exceptionally large half width value. This wafer was remounted and remeasured to verify the results shown in Table 6-3 and to make certain

(1) Private Communication. Weissman, Dr. Sigmund, College of Engineering, Rutgers University, New Brunswick, New Jersey.

TABLE 6-1

STACKING FAULT AND X-RAY DOUBLE CRYSTAL DIFFRACTOMETER ROCKING CURVE DATA

SAMPLE	STACKING FAULT DENSITY (cm^{-2})	TRANSMISSION ROCKING CURVE PLANE	HALF WIDTH (SEC)
60 - 10C	30	(220)	56
30 - 16B	4×10^4	(220)	54

TABLE 6-2

STACKING FAULT AND X-RAY DOUBLE CRYSTAL DIFFRACTOMETER ROCKING CURVE DATA

SAMPLE	STACKING FAULT DENSITY (cm^{-2})	REFLECTION ROCKING CURVE PLANE	HALF WIDTH (SEC)
60 - 10C	30	(400)	40
30 - 16B	4×10^4	(400)	37
60 - 10C*	30	(400)	39

*After chemically etching approximately 20 μm from front and back side of wafer.

TABLE 6-3

X-RAY TRANSMISSION DOUBLE CRYSTAL
DIFFRACTOMETER ROCKING CURVE DATA

SAMPLE	DESCRIPTION	SURFACE ORIENTATION	FLAT DIRECTION	HALF WIDTH (Sec of Arc)
A	Rutgers University Control No. I	(211)	<110>	20.5
AA	Rutgers University Control No. II	211	<110>	15.0
B	Fairchild 4 Ω cm n-type	(111)	<211>	24.4
C	Wacker 60 Ω cm p-type (MA 20-3)	(100)	<110>	22.4
D	Wacker 60 Ω cm p-type (MA20-2)	(100)	<110>	30.1
E	Wacker 30 Ω cm p-type (730 517)	(100)	<110>	24.2
F	Wacker 45 Ω cm p-type (730 709)	(100)	<110>	37.9
G	Wacker 45 Ω cm p-type (730 509)	(100)	<110>	104
H	Wacker 30 Ω cm p-type (730 910)	(100)	<110>	30.7
I	Fairchild 1.3 Ω cm p-type (TWJ-44)	(111)	<211>	25.4
J	Wacker 3" diameter (37097)	(100)	<110>	24.2

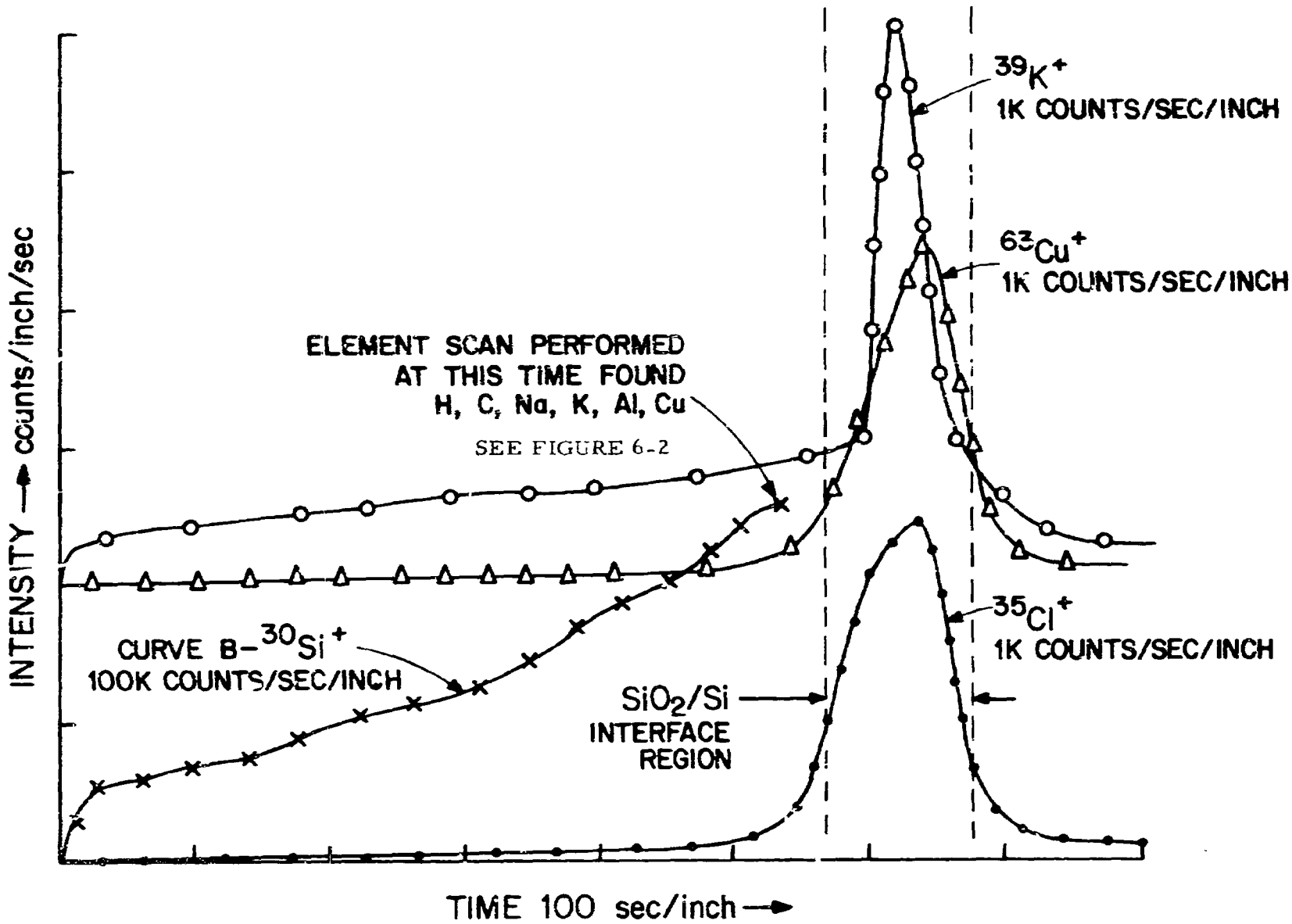

FIGURE 6-1. IMMA DATA FOR 3600 Å SILICON DIOXIDE LAYER GROWN IN A CHLORINE-CONTAINING AMBIENT

that the data were not being influenced by the experimental procedure. The second measurement confirmed the results of the first. Therefore, this wafer will be selected for further analytical studies to determine the cause of the lattice strain. Additional wafers from this batch, as well as wafers from the same batch used to supply wafer C, will be selected for further x-ray rocking curve studies.

Before these studies were pursued further, however, it was recognized that these measurements, which were obtained on apparatus at Rutgers University, were not sensitive enough for this investigation. Equipment that is specifically designed to produce the required sensitivity is being assembled in the Fairchild Semiconductor R&D Laboratory. Preliminary data indicate half width measurements of less than 2.5 seconds of arc on test wafers used in the initial setup. This implies that this double crystal diffractometer provides at least an order of magnitude improvement in sensitivity over the previously used apparatus. This increased sensitivity should enable us to differentiate lattice strain in starting material that is meaningful for interpretation of results obtained from subsequent wafer processing.

6.3 ION MICROPROBE ANALYSIS

Ion microprobe mass analysis (IMMA) was investigated as a possible analytical tool to detect contaminants in starting material as well as to detect contamination introduced during processing. In this analytical technique, the sample surface is continuously bombarded by a beam of high energy positively or negatively charged ions. Under this bombardment, the sample surface is slowly sputtered away to produce an agglomerate of secondary ions, neutral atoms, and molecular species. The secondary ions are collected and analyzed according to their mass-to-charge ratio in a mass spectrometer. Thus, in situ mass analysis can be made as a function of sputtering time. The yield of sputtered ions from the sample is affected by the surface chemistry of the sample which, in turn, is affected by the type of primary ion beam employed for sputtering. There are four combinations of primary and secondary beams that can be used for analysis: (1) positive primary beam and positive secondary beam, (2) positive primary beam and negative secondary beam, (3) negative primary beam and negative secondary beam, (4) negative primary beam and positive secondary beam.

Figure 6-1 contains reproduced IMMA data obtained from a silicon wafer that was oxidized in a chlorine-containing ambient to form a silicon dioxide layer approximately 3600 Å thick. These data were collected using a positive primary beam and negative secondary beam. This combination of beams was selected because information on the chlorine distribution in the

oxide layer was desired. It was thought that the combination of a positive primary beam and a negative secondary beam (positive sample voltage) would minimize any chlorine ion movement during the analysis caused by the primary beam and/or any surface charging in the dielectric layer. The data shown in Figure 6-1 are qualitatively correct. However, it is not satisfactory for quantitative information because of the change in silicon signal as a function of depth in the oxide layer, which should have been essentially constant for a stoichiometric film.

Figure 6-2 shows a mass-to-charge ratio scan taken in the vicinity of the oxide/silicon interface region. This scan was started at point one of Curve B, in Figure 6-1. It can be seen by reference to Figure 6-2 that a number of impurities (H, Na, K, Al, Cu) were detected. Figure 6-1 shows the profiles in depth taken for copper, chorine and potassium in this sample after those elements were found in the plot shown in Figure 6-2. As previously discussed, because there was a non-uniform silicon signal from the oxide layer during sputtering, quantitative data cannot be interpreted from the curves. However, one of the most significant features of this initial analysis was the observation of what appeared to be a significant copper concentration in the vicinity of the oxide-silicon interface. Therefore, additional IMMA studies were conducted to verify the presence of the copper in the dielectric layer.

For these studies, a primary bombarding beam of $^{16}O^-$ with an accelerating potential of 17 KeV was selected. A positive ion beam would have (1) caused sample charge-up, (2) required continuous voltage adjustment to optimize the sputtering ion yield and (3) can result in anomalous depth profiles because of ion drift within the sample.

The primary beam for these studies was raster scanned over a 75 micron x 50 micron area at an average current density of 0.53 milliamps/cm^2 to obtain the depth profiles reported. Profile information was accumulated for the mass of interest for 10-second integration periods using the electronic aperture adjusted to accept only ions sputtered from the central 6% of the scanned area. This was done to insure that none of the sputtered ions would be collected from the edges of the crater wall.

Raw data for depth profiles for $^{63}Cu^+$ is plotted in Figures 6-3 through 6-5. Each data point is the summation of 50 seconds of sputtering. Data for $30Si^-$ are also plotted to indicate the location of the SiO_2/Si interface and to establish the depth scale based on known thicknesses of the oxide layer. The $30Si^+$ signal decreases in the silicon because of work function differences between the silicon dioxide and silicon layers. The sample profile seen in Figure 6-3 is typical of the distributions encountered in all samples studied in that: (1) the $30Si^+$ signal is fairly uniform throughout the silicon dioxide

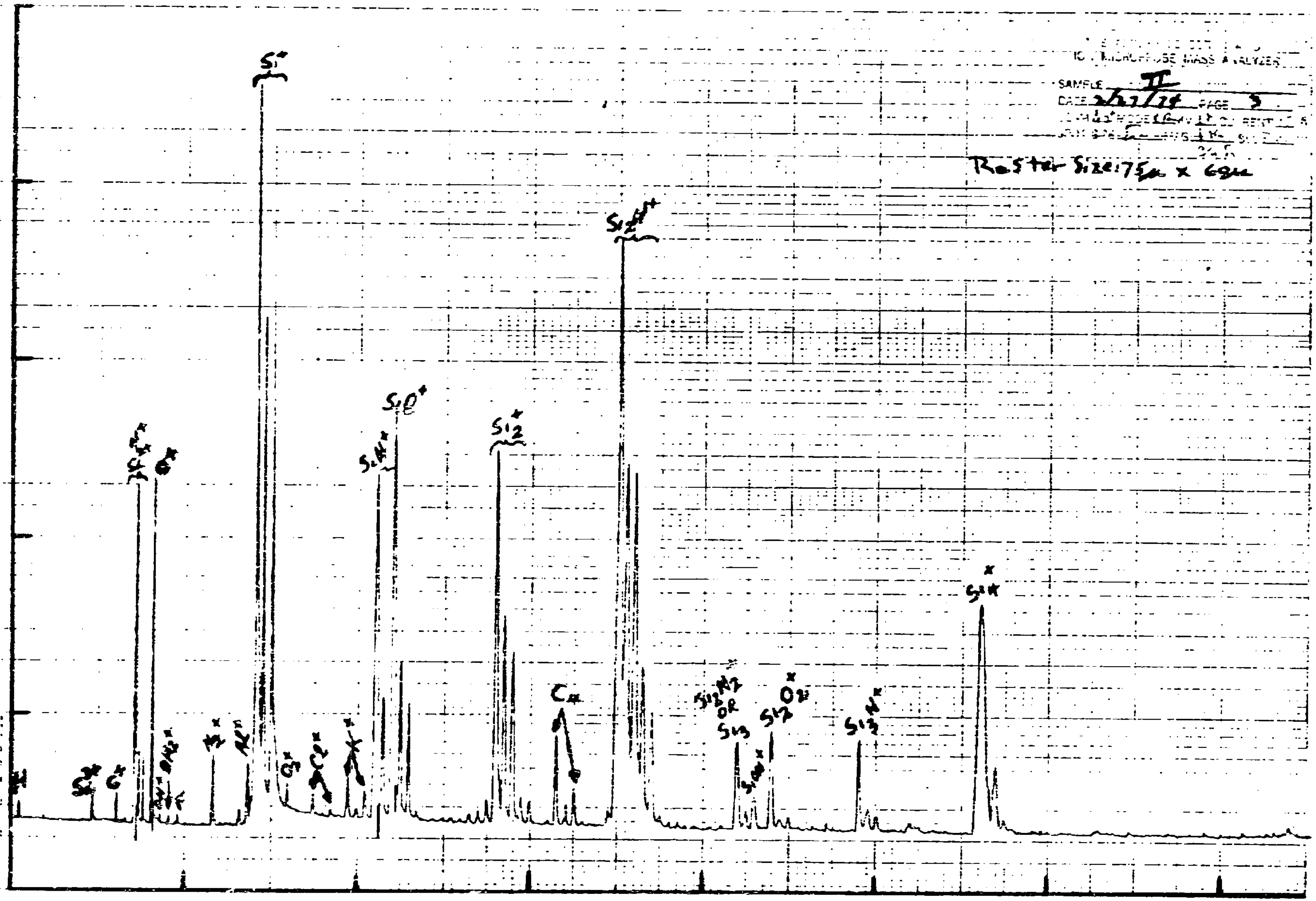

FIGURE 6-2. ION MICROPROBE MASS ANALYZER MASS-TO-CHARGE RATIO SCAN TAKEN IN THE VICINITY OF THE OXIDE-SILICON INTERFACE (See curve B of Figure 6-1)

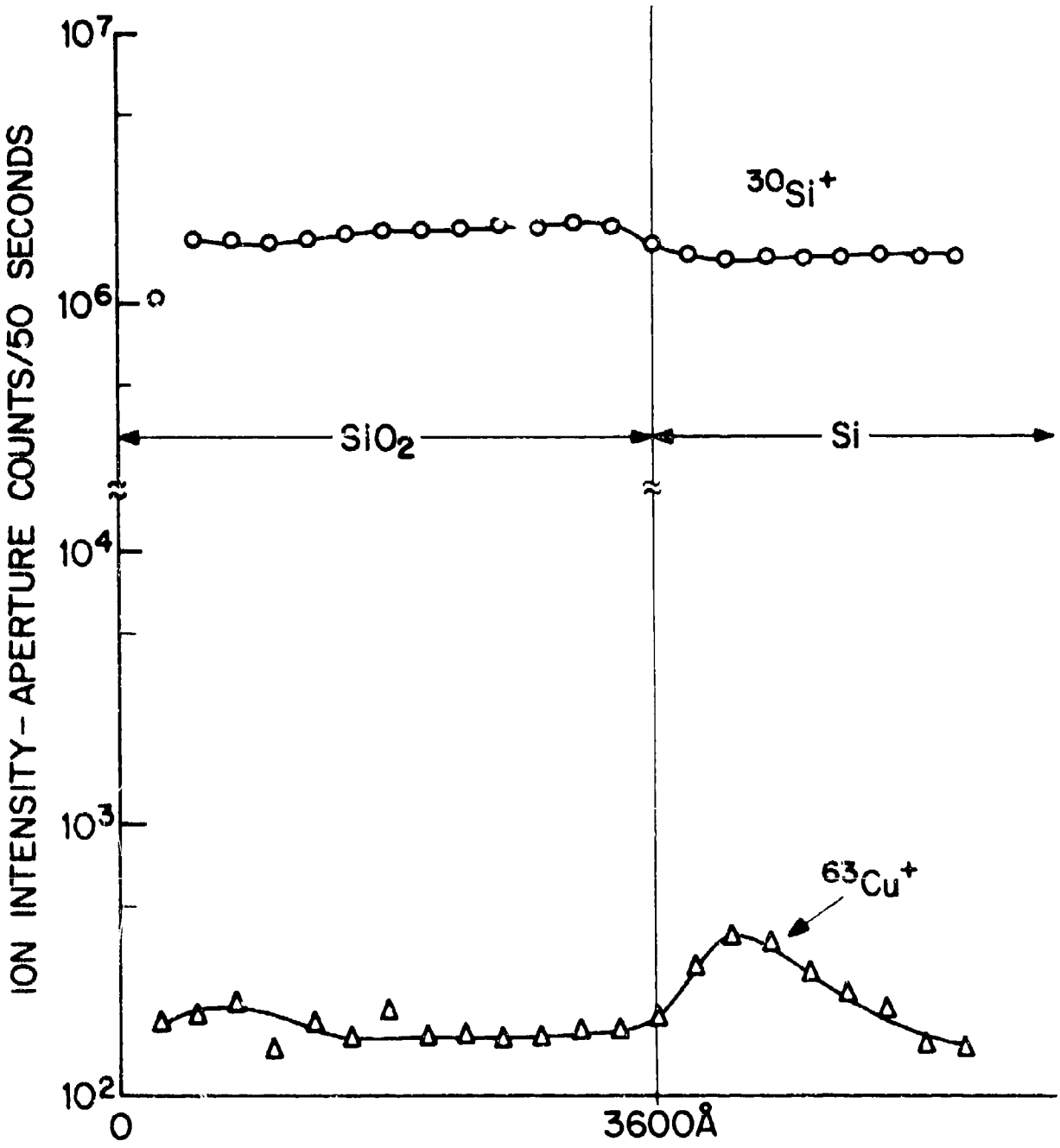

FIGURE 6-3. TYPICAL $^{63}Cu^+$ PROFILE FOR SiO_2 LAYERS GROWN IN A CHLORINE-CONTAINING AMBIENT

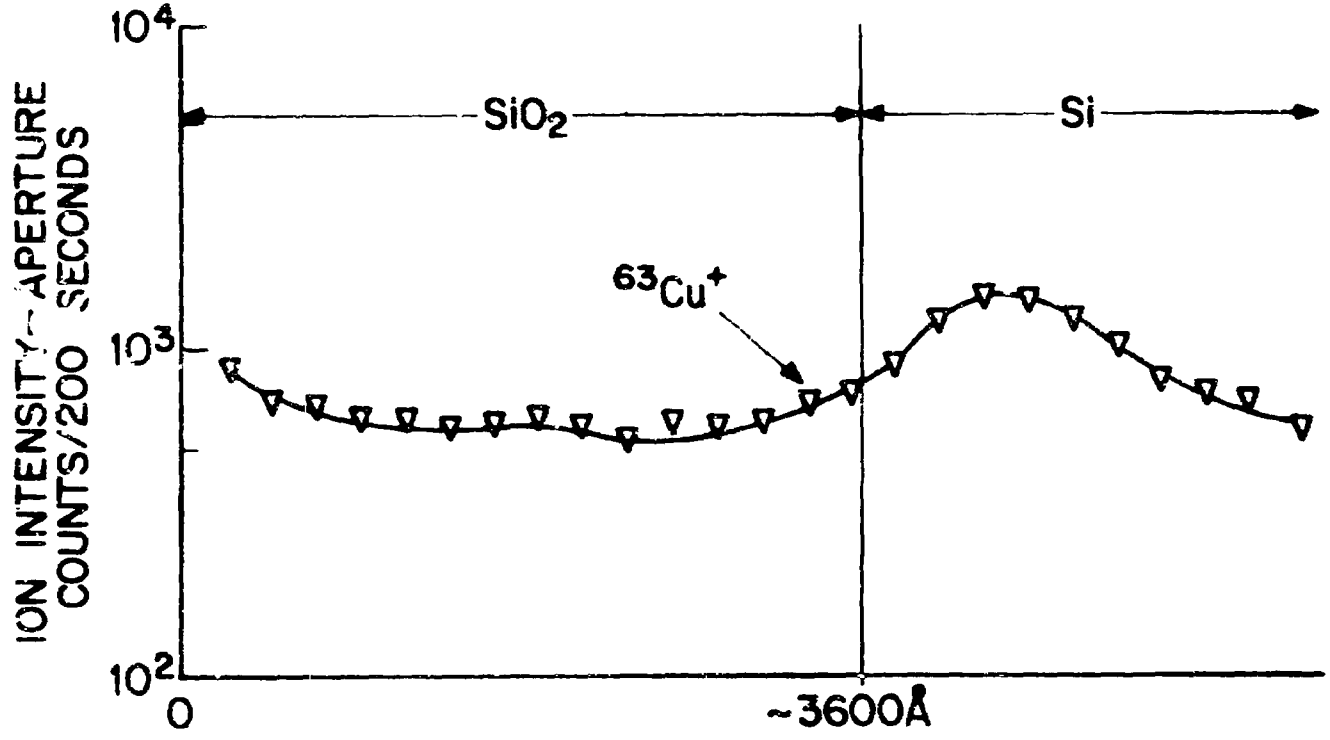

FIGURE 6-4. TYPICAL $^{63}Cu^+$ PROFILE FOR SiO_2 LAYER GROWN IN A CHLORINE-CONTAINING AMBIENT
(Same electrical aperture size as used in Figure 6-3 but sputtered area is four times larger.)

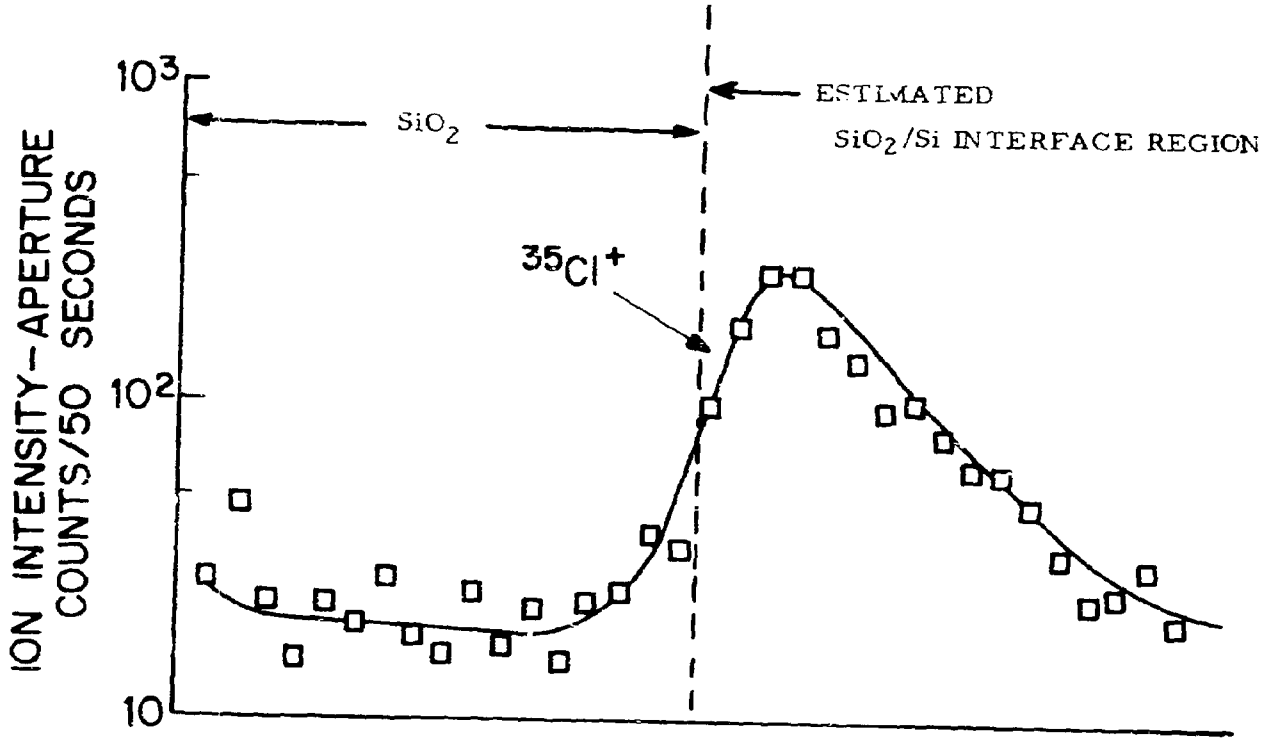

FIGURE 6-5. TYPICAL $^{35}Cu^+$ PROFILE FOR SiO_2 LAYER GROWN IN A CHLORINE-CONTAINING AMBIENT

layer, then drops at the SiO_2/Si interface and stabilizes at a somewhat lower level in the silicon substrate; (2) copper is observed to be present in the oxide layer and is enriched approximately 400 Å into the silicon substrate, where it appears at approximately twice the bulk levels. Quantitative measurements are based on a theoretical model developed to predict the relative ionization of atoms with the sputtering ion source (ref. 2).

Copper concentrations were calculated from the raw profile data at 3 depths in each of the samples: (1) in the oxide layer, (2) at the maxima in the substrate, and (3) in the bulk silicon at the end of the profile. These values are listed in Table 6-4. The maximum copper content ranges from 2.9 ppma in the control sample (non-chlorine containing oxidation ambient) to 14.+ ppma in sample I. The two special samples (SPEC 1-H and SPEC 1-S) appear to have a significantly lower copper contamination than does sample I.

One run (Figure 6-4) was made using an enlarged (4X) raster to verify that the electronic aperture was effective in eliminating undesirable crater-wall contributions to the copper profile. For subsequent tests we returned to the smaller raster, since no degradation in profile resolution was detected at the faster, (1X) raster, sputtering rate.

The chlorine concentration in sample I is profiled in Figure 6-5. This element also appeared to be enriched in a region directly below the oxide-silicon interface. However, there is some uncertainty in the exact location of the peak of the chlorine concentration, since a silicon profile was not obtained to accompany the chlorine profile. Therefore, the exact location of the oxide-silicon interface is not absolutely known. There is a possibility that the sputtering rate for the 1X raster was changed after taking the 4X raster data. An estimate of the location of the oxide-silicon interface with the chlorine data was made and is shown in Figure 6-5. This estimate was based from subsequent silicon profiles in oxide layers.

These studies have indicated significant amounts of copper contamination. Since copper is known to cause leakage currents in semiconductor structures, it is important that the source of this contamination be eliminated. Future IMMA studies will concentrate on determining if the source of contamination is in the starting material or if it is introduced during processing.

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(2) Anderson, C.A. and Hinthorne, J.R. Anal. Chem. 45, 1421 - 1434, 1973.

TABLE 6-4

ION MICROPROBE MASS ANALYSES DETERMINATION OF COPPER IN SiO_2/Si STRUCTURES

(Copper Concentration in Parts Per Million Atomic)

SAMPLE	COPPER CONCENTRATION (ppma)		
	SiO_2 LAYER	SILICON SUBSTRATE	
		Peak Concentration *	Trail Concentration **
I (3600 Å Chlorine Oxide)	1.5	14.4	4.3 - 5.4
SPEC 1-S (1000 Å Chlorine Oxide)	0.9	7.1	5.1
SPEC 1-H (1000 Å Chlorine Oxide)	0.8	4.1	1.5
CONTROL (1700 Å Non-Chlorine Oxide)	0.6	2.9	1.5

* Approximately 400 Å below interface.
** Approximately 1500-2000 Å below interface at termination of profile raster.

6.4 STORAGE-TIME DATA

A number of experiments were performed to determine those processing steps that affect storage-time measurements. For these studies a capacitor structure was used as the test vehicle. Storage-time measurements were made by applying just enough voltage to turn the device on. A voltage pulse was then applied, which sends the device into deep depletion. All measurements were made in darkness. The time it took for the capacitance to recover to an equilibrium value was taken as the storage time.

Table 6-5 lists storage-time data for devices that received identical processing, except that the pull rate out of the 1100°C oxidation furnace is a variable. The standard procedure is to perform any initial processes (gettering, etc.), which may be required prior to the oxidation with the whole wafer. Just prior to gate oxidation, the wafers are scribed in half and different pull rates are employed for the final high temperature processing step on each half wafer. Data for pull rates of 0.5 minute, 2 minutes, 40 minutes and 60 minutes are shown in Table 6-5.

The most dramatic effect noted in this table is the comparison of the data for the half-minute and 60-minute pull rates. Figures 6-6 and 6-7 show x-ray topographs taken of wafers 1C and 1D after electrical measurements and removal of all metal and oxide layers. Several observations can be made about these topographs:

1) The "A" half (labeled "1C" in Table 6-5) - Figure 6-6 has a significantly higher dislocation density than does the "B" half (labeled "1D" in Table 6-5) - Figure 6-7.

2) Except for dislocations introduced on the back side of the wafer by the identification technique used (i.e., STR 05-1B) wafer 1D is essentially dislocation-free after processing.

3) For both halves of the wafer there appear to be regions of either heavy precipitates or additional back side damage. They are labeled as area 1 in Figures 6-6 and 6-7.

The storage time data of Table 6-5 can be interpreted as indicating that there are contaminants in the wafer prior to processing, which were allowed to precipitate during the slow (one hour) pull employed on wafer 1D, which reduced the storage time of this wafer. In the case of wafer 1C, there are at least two explanations for the long storage times: (1) the pull rate was fast enough to keep the contaminants in solution, that is, the contaminant concentration

TABLE 6-5

TYPICAL STORAGE-TIME DATA OBTAINED FROM DEEP DEPLETION CAPACITANCE MEASUREMENTS

WAFER	DEVICE NUMBER & STORAGE TIMES (SEC)				
	1	2	3	4	5
1A	20	15	20	20	50
1B	28	75	5	4	4
2A	22	22	37	33	8
2B	5	5	6	6	50
3A	75	123	90	92	88
3B	3	9	50	20	90
1C	135	2	135	150	130
1D	1	0.5	1	5	1
2C	18	60	216	105	0.5
2D	2	0.5	1	1	1
3C	30	285	225	240	210
3D	0.5	0.5	0.5	1	1
4C	45	90	10	18	90
4D	1	0.5	0.5	0.5	0.5

NOTE: Each wafer scribed in half prior to gate oxidation. "A" halfs received a 2-minute pull from 1100°C following gate oxidation. "B" halfs received a 40-minute pull from 1100°C gate oxidation. "A" and "B" halfs from same wafer.
"C" halfs received a 0.5-minute pull from 1100°C gate oxidation furnace.
"D" halfs received a 60-minute pull from 1100°C gate oxidation furnace.
"C" and "D" halfs from same wafer.

FIGURE 6-6. X-RAY TOPOGRAPH OF WAFER 1C (TABLE 6-5) 0.5-MINUTE PULL RATE FROM GATE OXIDATION PROCESS

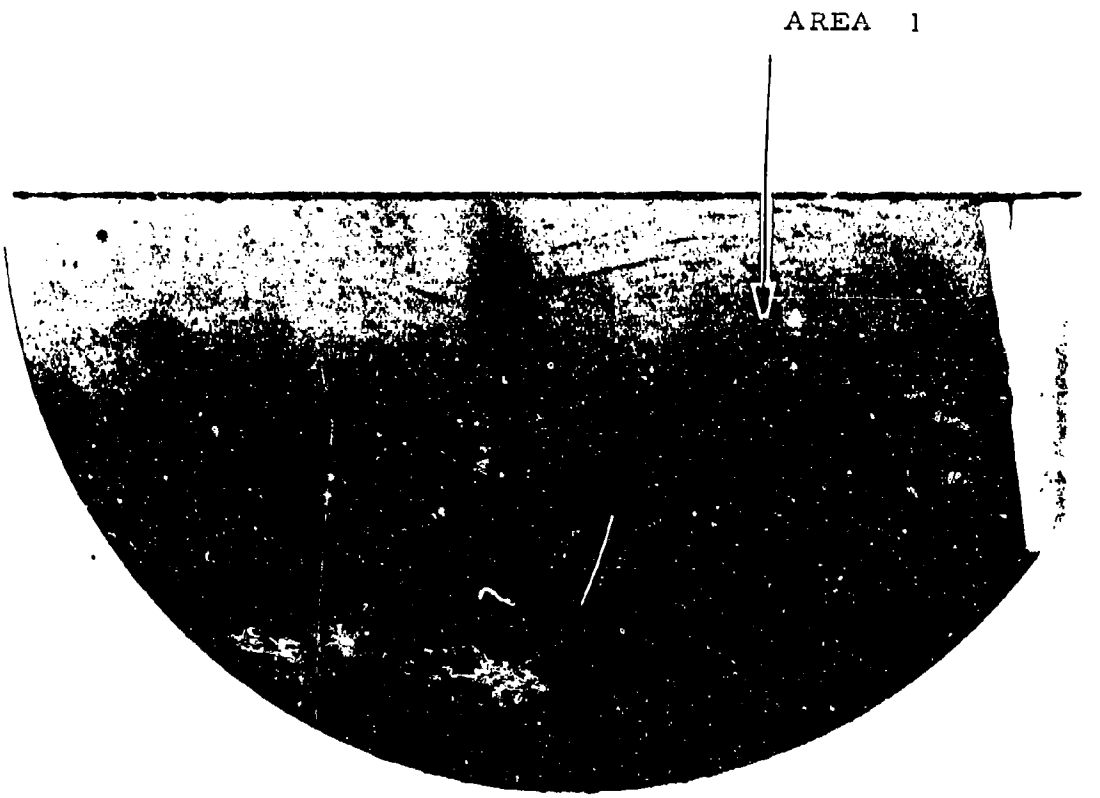


FIGURE 6-7. X-RAY TOPOGRAPH OF WAFER 1D (TABLE 6-5) 60-MINUTE PULL RATE FROM GATE OXIDATION PROCESS

was not high enough to act as a dark-current generation site and/or (2) the dislocations generated during the rapid pull rate acted as sinks for the contaminants. The localized contaminant concentration was reduced to a point where it was not high enough to act as a dark-current site.

SECTION 7

TEST INSTRUMENTATION AND TV CAMERA SYSTEMS

At the outset of the Phase II program, test instrumentation developed during Phase I was modified to facilitate characterization testing of CCAID-244 and future CCAID-488 area image sensors, as described in Section 7.1. Concurrently, a CCAID-TV Camera system development program was initiated which resulted in fixing critical device/system interface parameters, including row and column element counts, prior to final CCAID 244/488 mask design. Other results of the camera program, as described in Sections 7.2 and 7.3, include delivery of a CCAID-100 BD Camera and the generation of design concepts for the Boresight/244 and Low-Light-Level/488 TV Camera systems scheduled for delivery during Phase III.

7.1 TEST INSTRUMENTATION

The development of versatile test instrumentation during the Phase I program significantly minimized the additional effort necessary to perform tests of Phase II devices. For example, CCLID 1000B devices were evaluated with the optical test station and electronics subsystem previously described in the Phase I Final Report (Ref. ED-AX-16, October 1973). The changes required to adapt to different linear devices and to the CCAID-100 BD, were typically limited to relatively minor circuit board modifications. However, in anticipation of CCAID-244/488 test requirements, portions of the original system were redesigned to facilitate either automated or manual characterization tests at low temperature. The modified system is described in the following section.

7.1.1 CCD Area Array Automated Characterization System

The CCD Area Array Automated Characterization System is designed to permit efficient characterization of CCAID-100, CCAID-244, and CCAID-488 devices. The automated system, similar to the linear array automated system used in Phase I, has the capability for investigation of individual device parameters such as sensitivity, dynamic range, uniformity and dark current. Versatility built into the system allows for the separation of various device characteristics for detailed investigation.

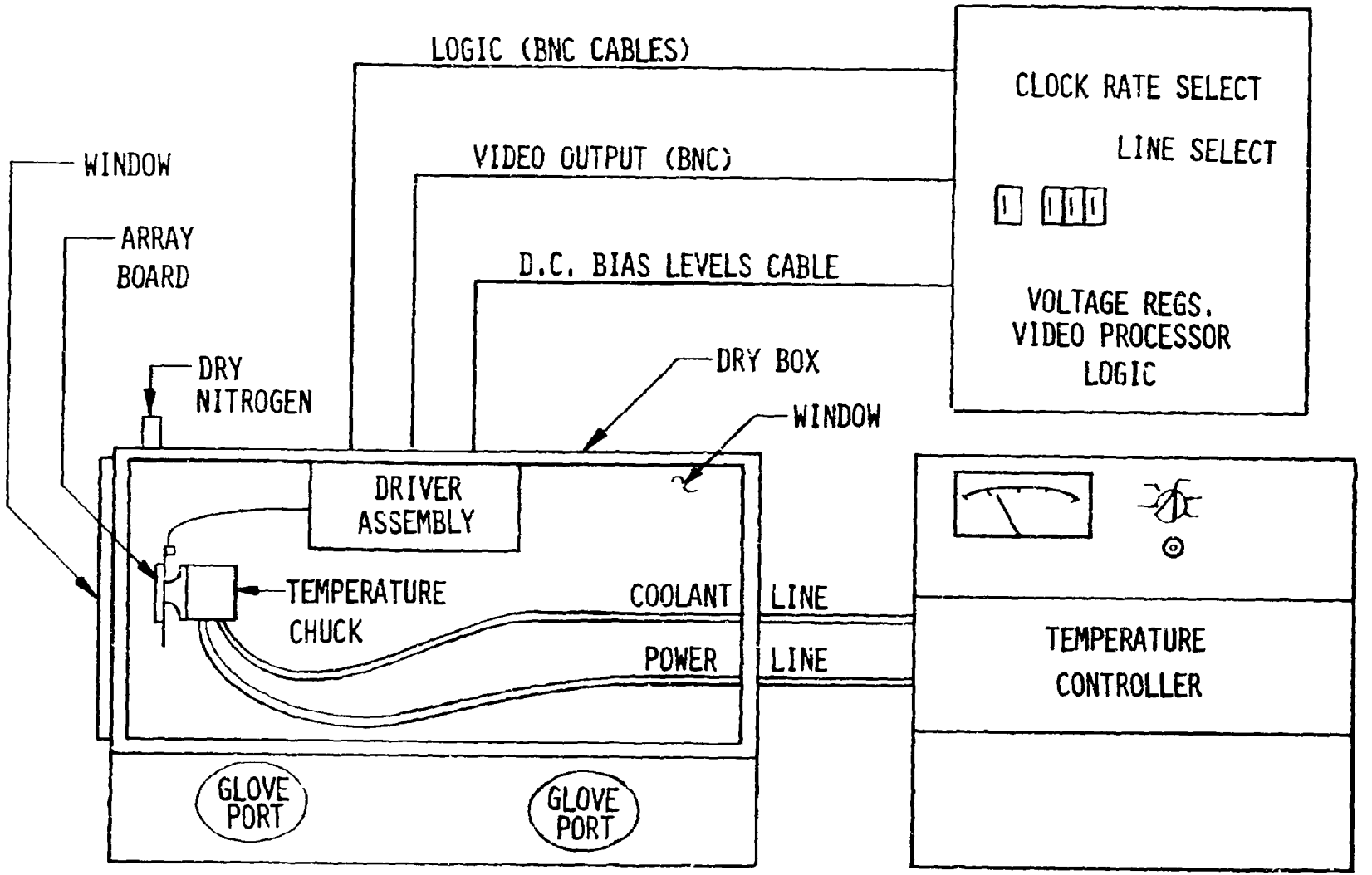


FIGURE 7-1. ENVIRONMENTAL CONTROL EQUIPMENT FOR AREA ARRAY CHARACTERIZATION SYSTEM

The characterization system contains all the logic signals and variable bias voltages necessary to exercise CCAID image sensors. All logic is fully synchronized and permits a wide range of clock rate selection. The line selector logic enables any of the array's vertical lines to be selected for automatic characterization and storage of the measurement data to magnetic tape. Individual horizontal lines may also be selected with this logic control for viewing on an oscilloscope.

Used in conjunction with the environmental control equipment, device characterization is extended throughout a range of temperatures from approximately -60°C to +130°C.

While the system has been designed specifically to investigate and characterize CCAID-244 arrays, enough flexibility exists within the system to enable testing of CCAID-100 arrays and future CCAID-488 arrays by simply replacing the plug-in array module. This is accomplished by redundancy of the circuits within the system, the ability to vary voltage levels to the the array, and a modular approach to circuit function partitioning.

The system is divided into two parts, i.e., the environmental control equipment and the electronic characterization equipment.

7.1.1.1 Environmental Control Equipment

The environmental system provides a dry nitrogen atmosphere in which the array can be operated at low temperatures. The dry atmosphere prevents condensation and icing on the array optical window during low temperature operations. This dry condition is achieved through the use of a dry box through which dry nitrogen gas is fed at a controlled rate. The dry box is fitted with optical windows to allow for external illumination of the array and to visually examine arrays under controlled test conditions. Glove ports provide access to the arrays, permitting adjustment while in the box (Figure 7-1). In the chamber, the array is mounted on a temperature control chuck. The chuck contains an internal electrical heater and is connected to an external refrigeration system. This arrangement permits variation of the chuck temperature from -60°C to +130°C. The chuck is a cylinder two inches in diameter and two inches in height.

7.1.1.2 Electronic Characterization Equipment

The electronics portion of the system consists of four assemblies; the array board, the front-end driver assembly, the main unit logic/voltage

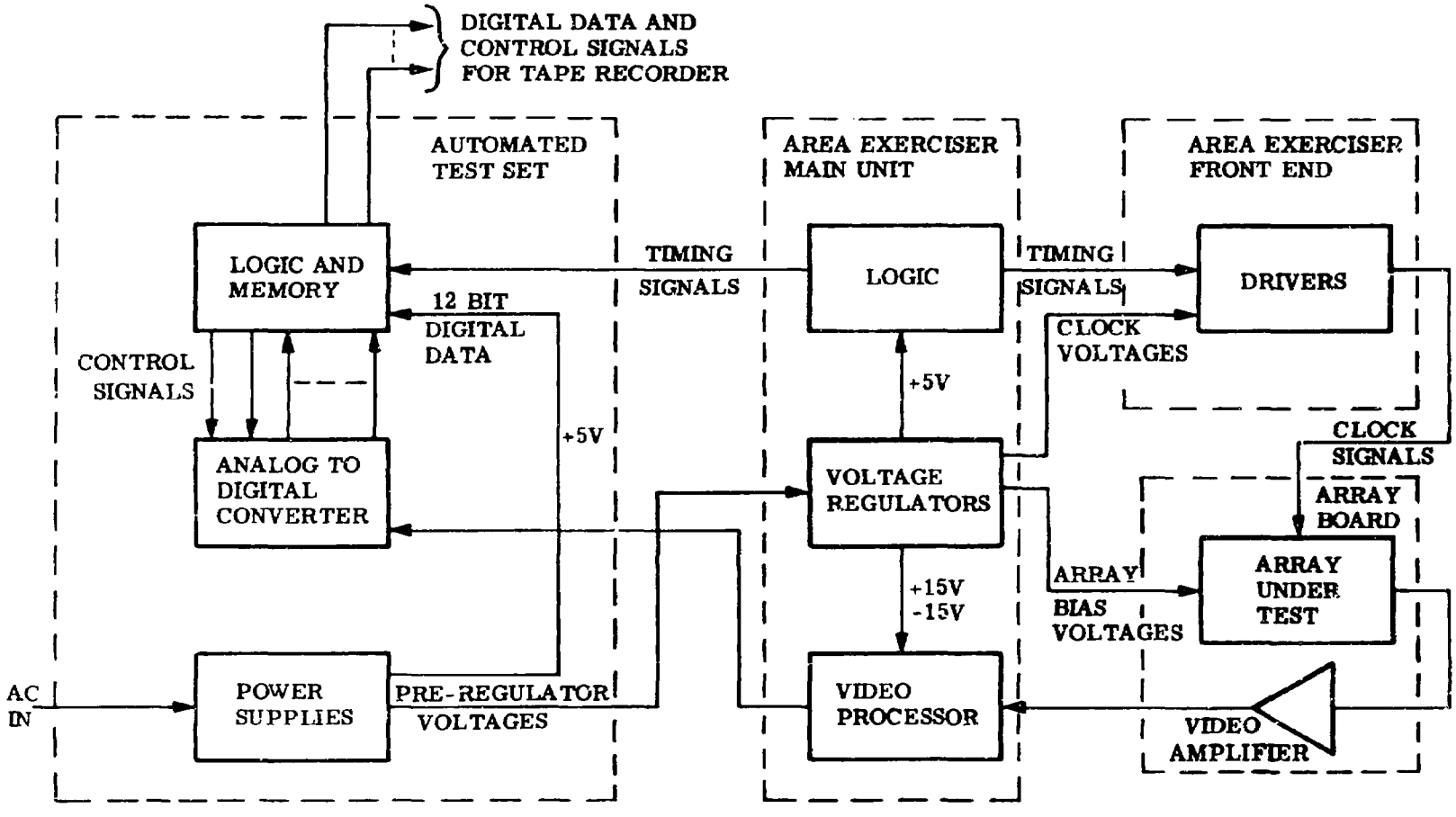


FIGURE 7-2. CCD AREA ARRAY AUTOMATED CHARACTERIZATION SYSTEM

regulator/video processor assembly, and the automated test set assembly, as shown in Figure 7-2. A separate array board is required for each type of array to be tested. These boards contain the array under test as well as the first video amplifier stage. The array board also contains a copper block which interfaces between the array and the cold plate of the temperature control chuck (Figure 7-3). The driver assembly includes amplifier stages to provide dc bias voltages and logic signal amplification. A third assembly contains the logic signal section, the video processor and the power supply regulators. Logic clocking rate is selectable via a thumbwheel switch over five frequencies up to 8 MHz. An external clocking input is also available. Individual array lines may be selected for presentation on a CRT display. This selection is made by a thumbwheel selector located on the front panel of the assembly.

The dc voltage regulators provide the basic supply voltages to the logic as well as the supplies to the amplifiers in the driver assembly. Voltage adjustment capability is available on the individual regulator boards. This feature allows simple adjustment of the logic levels and dc bias levels on the array.

7.2 CCAID TV CAMERA DEVELOPMENT

Subsequent to the completion of the Phase I device development program and laboratory evaluation of the first 100 x 100 element area imaging devices, a television camera design program was initiated. Included in program objectives were, (1) the design and construction of a CCAID-100 BD Camera System and (2) a design study of camera systems suitable for the larger area arrays to be developed during Phases II and III. These objectives were addressed concurrently to minimize start time delays for Phase II device programs requiring inputs on critical device/camera system interface parameters.

7.2.1 Camera Functional Design Requirements

Circuit functions for a TV camera using Fairchild interline-transfer image sensors with two-phase clocking are illustrated in the block diagram, Figure 7-4. With the exception of the CCD and its associated gate drive waveforms, similar functions (plus horizontal and vertical scanning functions) are necessary for conventional camera designs using vacuum tube image sensors.

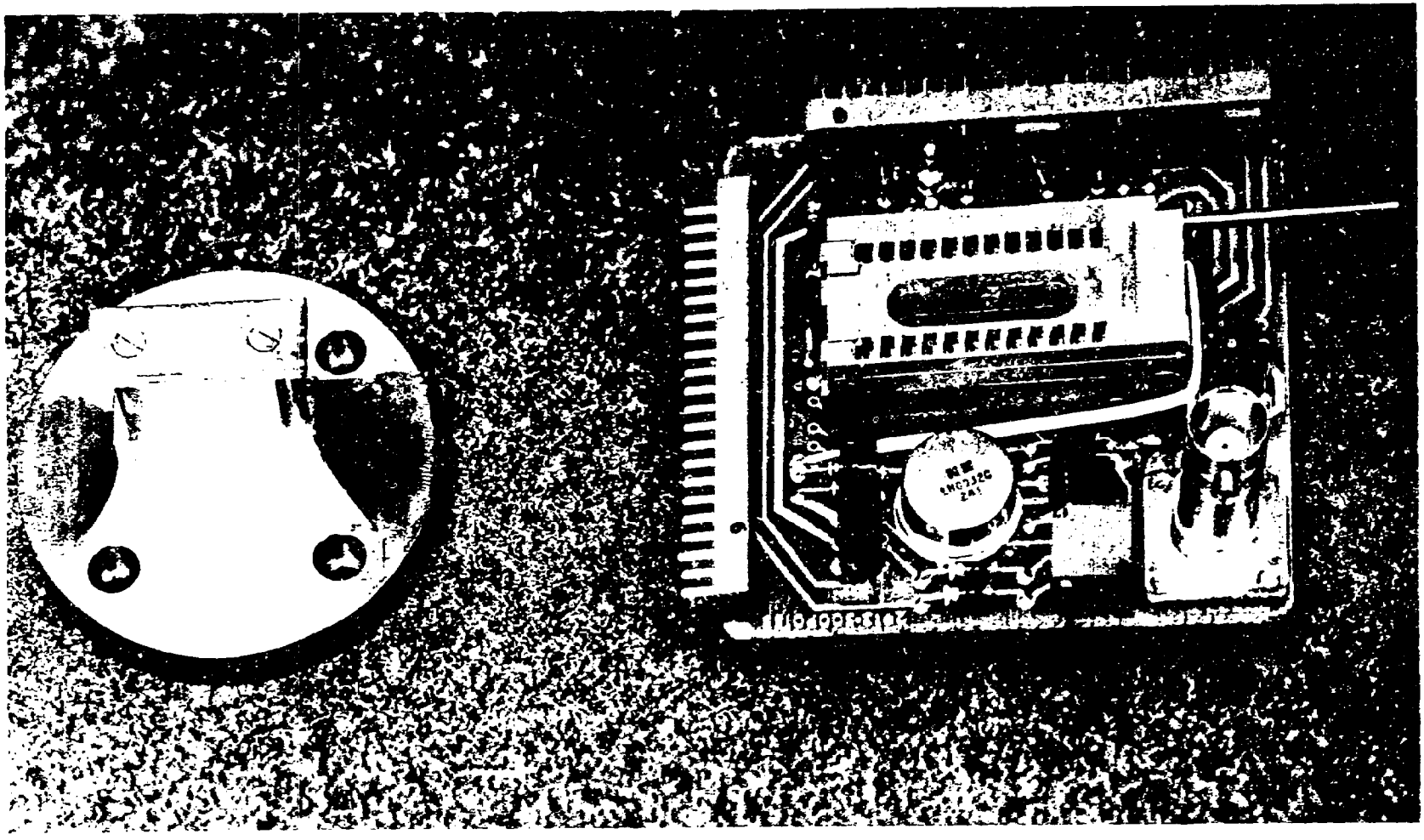


FIGURE 7-3. ARRAY BOARD AND THERMAL INTERFACE BLOCK

75P-37

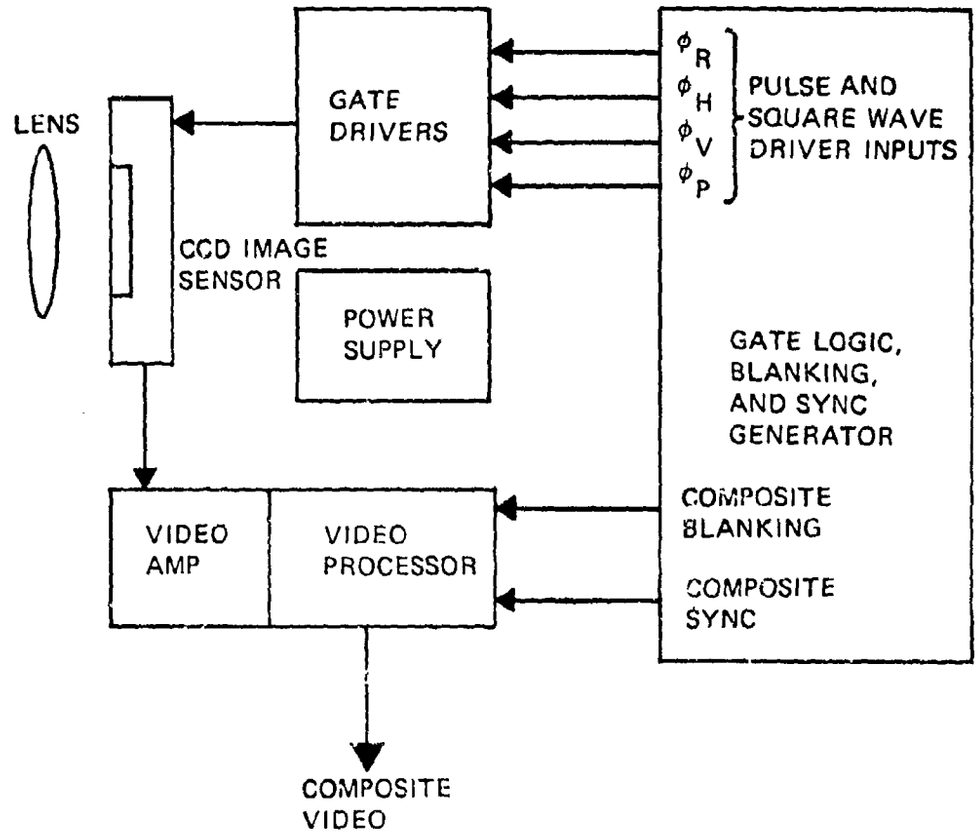


FIGURE 7-4. MONOCHROME CCAID-TV CAMERA FUNCTIONAL REQUIREMENTS

A composite sync and blanking signal generator is required for either conventional or CCD-TV Camera systems. A typical CCAID camera logic design utilizes a crystal clock at frequency $f_C = 2f_E$, where f_E is the element readout rate, to provide decoding edges for reset and sampling pulses shorter in duration than an element period. All CCD gate waveforms, including display sync and blanking, are derived from f_C by divide-down counters and combinational logic circuits.

A conventional camera design also requires relatively complex logic circuits to conform with TV system specifications such as EIA RS-170. In this case, the function of the logic is to synthesize synchronization and blanking waveforms with timing edges defined from the output of a master clock operating at a high multiple of the line scan frequency f_H. This logic requirement stimulated the development of single-chip MOS-LSI TV signal generators, such as the Fairchild 3261. The 3261 is controlled by a crystal clock operating at 910 f_H, facilitating the generation of a synchronous NTSC color subcarrier output at the nominal US standard 3.58 MHz rate. Decoding edges for either monochrome or color system outputs are derived from an on-chip square wave clock at 130 f_H.

Although existing waveform generators such as the 3261 do not provide CCD gate signal outputs, a modified CCD/RS-170 compatible design would be feasible if the CCD design conforms to system specifications. For CCD imaging sensors, conformance implies a precisely defined number of readout lines per field. Also, if the CCD sensor element counts per line are properly defined, a simplified camera logic design using a single master clock input is possible.

7.2.2 CCAID-244/488 Camera Design Considerations

CCAID-244 and CCAID-488 TV Camera design objectives were established as part of an initial Phase II task requiring the determination of camera/sensor interface parameters. These objectives included (a) full conformance to US standard 525-line system specifications for the CCAID-488 Camera and (b) compatibility with conventional TV display equipment for the CCAID-244 Camera. As described in the following paragraphs, realization of these objectives was achieved by the selection of specific camera system and related sensor design features.

7.2.2.1 CCAID-488 Camera

In accordance with 525-line system specifications nominal values required for readout scan parameters are: line rate f_H = 15750 KHz; field rate fv = 60 Hz; and frame rate f_f = 30 Hz (with 2/1 field/frame interlace).

The RS-170/3261 vertical blanking interval is (20 + 22/130) line periods/field defining a minimum of (525-40) = 485 active scan lines, hence sensor element rows per frame.

Horizontal blanking is defined as (22/130) horizontal line periods, which is equivalent to: (22/130) $(n_A + n_B) = (22/130)\, n_T$ where n_A, n_B and n_T define the active, blanked, and total number of element periods/line period, respectively. If n_T is selected to be 910/2 = 455, a single master clock can be used to satisfy the requirements for both RS-170 and CCD gate-drive waveform synthesis. For this condition, $n_B = (22/130)\, 455 = 77$, and $n_A = (n_T - n_B) = 378$. The CCAID-488B sensor design has 380 elements/row, and 488 rows, hence a few terminal rows and columns can be blanked off when blanking signal edges are properly centered with respect to the active format region.

7.2.2.2 CCAID-244 Camera

The 190 x 244 element counts of exactly half the full format 380 x 488 design were selected to facilitate operating modes which are interface-compatible with existing TV system equipment including VTR's, display monitors, and TV receivers. These compatible modes include:

1) Format Inset Mode - All camera waveforms are identical to those required for operation of a 380 x 488 sensor, except for an extension of the horizontal and vertical blanking intervals. Thus, an NTSC compatible video signal can be generated over a portion of the full display format equal to 1/2 the active height and width. The outputs from up to four cameras can be displayed on a single monitor by appropriate phasing of the active and blanking signal intervals prior to composite signal mixing.

2) Full Format, Synthetic Interlace Mode - By modifying the camera timing generator to enable counting an integral number of lines/field near the normal 262-1/2 line value, a non-interlaced display raster can be generated with horizontal and vertical scanning rates within a few percent of industry standards. A raster thus generated is "synthetically" interlaced by alternately addressing the display with video lines of normal sensor and blanking signal followed by an artificially

generated line signal with 100% blanking. During an ODD field sensor readout, lines 1, 3, 5, ---, N_{odd} of the active format contain sensor video signal while 2, 4, 6---, N_{even} are blanked off, with the video/blank line sequence reversing for the following EVEN field readout.

3) Full Format, Fast Frame Mode - Camera timing logic, including display synchronization and V-blanking signals are altered to generate a true 2/1 interlaced display with approximately half the usual number of active scan lines per field. VTR compatibility is achieved by selecting a 120-Hz vertical rate, which is an even multiple of the standard rate. Display circuit modifications are required, however, these modifications can be limited to the vertical scan generator if the horizontal scan frequency is selected to be near 15,750 Hz. Advantages of the fast frame mode include the elimination of interline display flicker, enhanced resolution for rapidly moving scene information, and reduction of dark signal effects limiting dynamic range at high operating temperatures.

4) Multiplex Modes - Other system compatible operating modes are possible if more than one CCAID-244 sensor is used. Two (or more) CCAID sensors can be arranged to view identical scene information, by utilizing optical beam splitters and a single lens, or by employing matched individual lenses in a boresight configuration. The outputs of each sensor can then be combined, i.e., multiplexed, into a single video information channel. The Boresight-244 Camera to be delivered during Phase III will utilize multiplexing principles, as described in the following section.

7.2.3 The Boresight-244 Camera Concept

Interline transfer image sensors can be operated in a unique element multiplexed-pair (E-MUX) mode with the potential for effectively doubling the image format element density in the row direction. Figure 7-5 illustrates the camera system block diagram for a boresight pair of CCAID-244 sensors.

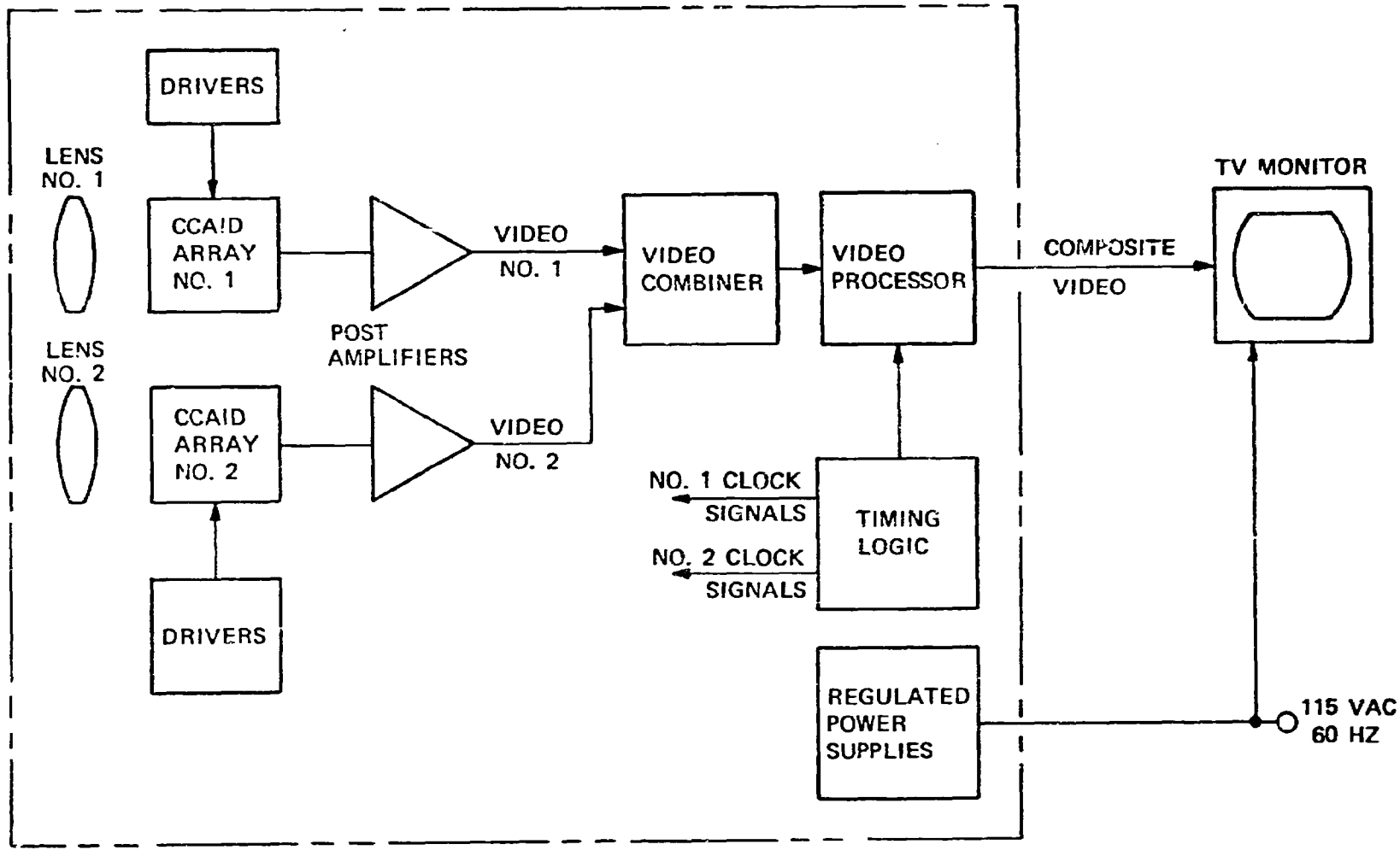


FIGURE 7-5. BORESIGHT-244 TELEVISION CAMERA SYSTEM

Implementation principles are based on two characteristics of the interline-transfer CCAID organization: (a) element aperture response in the row direction is defined by a photosensing site width ≤ 0.5 cell width, and (b) the readout signal interval corresponding to each sensing element is approximately 1/2 the element transfer period.

Figure 7-6 illustrates the 1/2 cell width offset from precise image registration necessary to superimpose the set of photosensing sites of sensor No. 2 on the corresponding set of light-shielded sensor No. 1 transport sites. Signal processing and summing yields an output signal with double the number of image samples per combined video output line, as illustrated in Figure 7-7 for the floating-gate amplifier (FGA) signals of the CCAID-244.

Readout scan parameters selected for the deliverable Boresight-244 Camera are line rate f_H = 15,750 KHz, and field rate f_V = 120 Hz, providing a composite 60 frame/second signal to a modified TV display monitor. Each camera will be capable of independent operation. In the multiplex mode, the cameras will interconnect with a control unit which operates the cameras in a master/slave relationship. In this mode, the timing circuits of the slave camera are disabled and the master camera provides synchronous timing signals to both sensors. A multiplex unit will then combine the video information from the two sensors and format them into one of the two patterns.

The video may be summed element-by-element (E-SUM-mode) for improved sensitivity or it may be interleaved along a line (E-MUX-mode) for improved horizontal resolution. Both modes are expected to demonstrate reduced aliasing as compared with single sensor operation.

Each camera will use identical vari-focal optics, with X, Y, and Θ adjustments on the slave camera to facilitate boresight alignment, as indicated in Figure 7-8.

7.2.4 Low-Light-Level CCAID-TV Camera Design

The 244/488 image sensors utilize a distributed floating-gate amplifier with a noise equivalent signal (NES) level of less than 20 electrons/pixel. As part of the initial program plan, a CCAID-488 TV Camera which demonstrates NES-limited low-light-level TV performance is scheduled for delivery during Phase III. Preliminary design effort during Phase II included a predicted performance analysis, as described in subsection 7.2.4.1. The results of this analysis highlight the need for device cooling to reduce thermally generated dark signals to negligible levels. Subsection 7.2.4.2 describes the packaging concept for camera design with thermoelectric cooling.

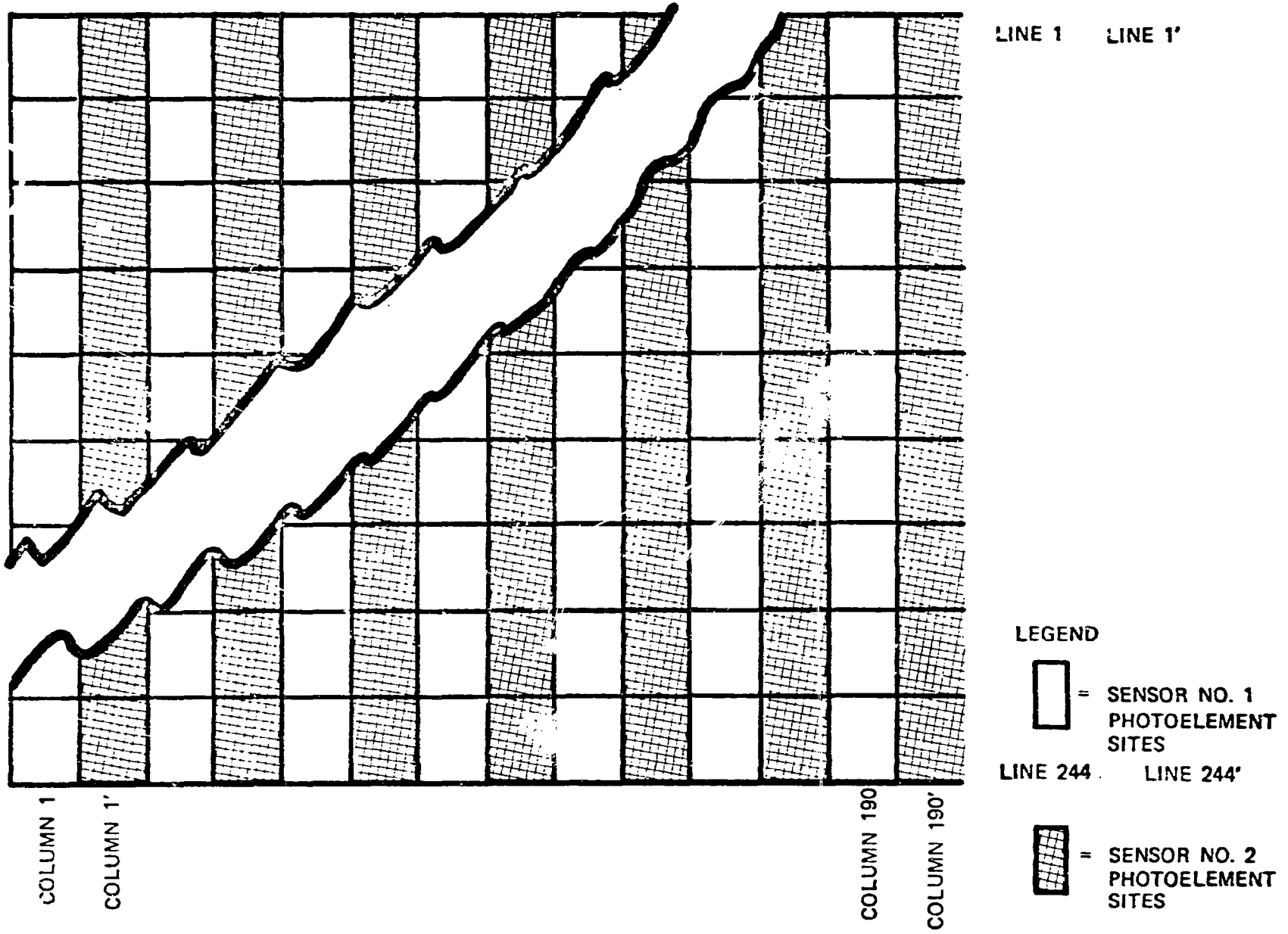


FIGURE 7-6. E-MUX SPATIAL ALIGNMENT FOR 244 x 190 SENSOR PAIR

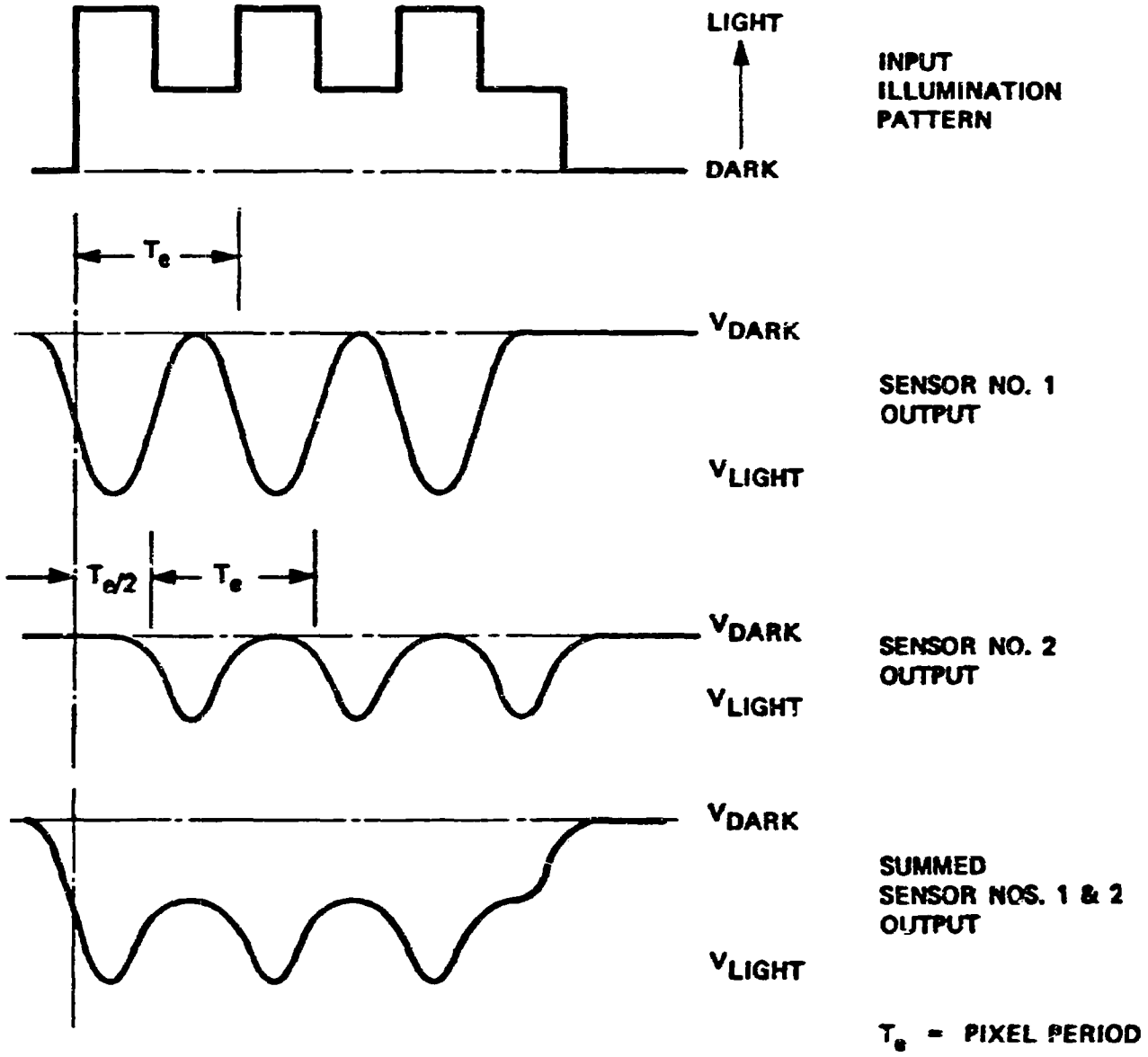


FIGURE 7-7. FGA-MULTIPLEXED PIXEL WAVEFORMS AT BEST PHASING

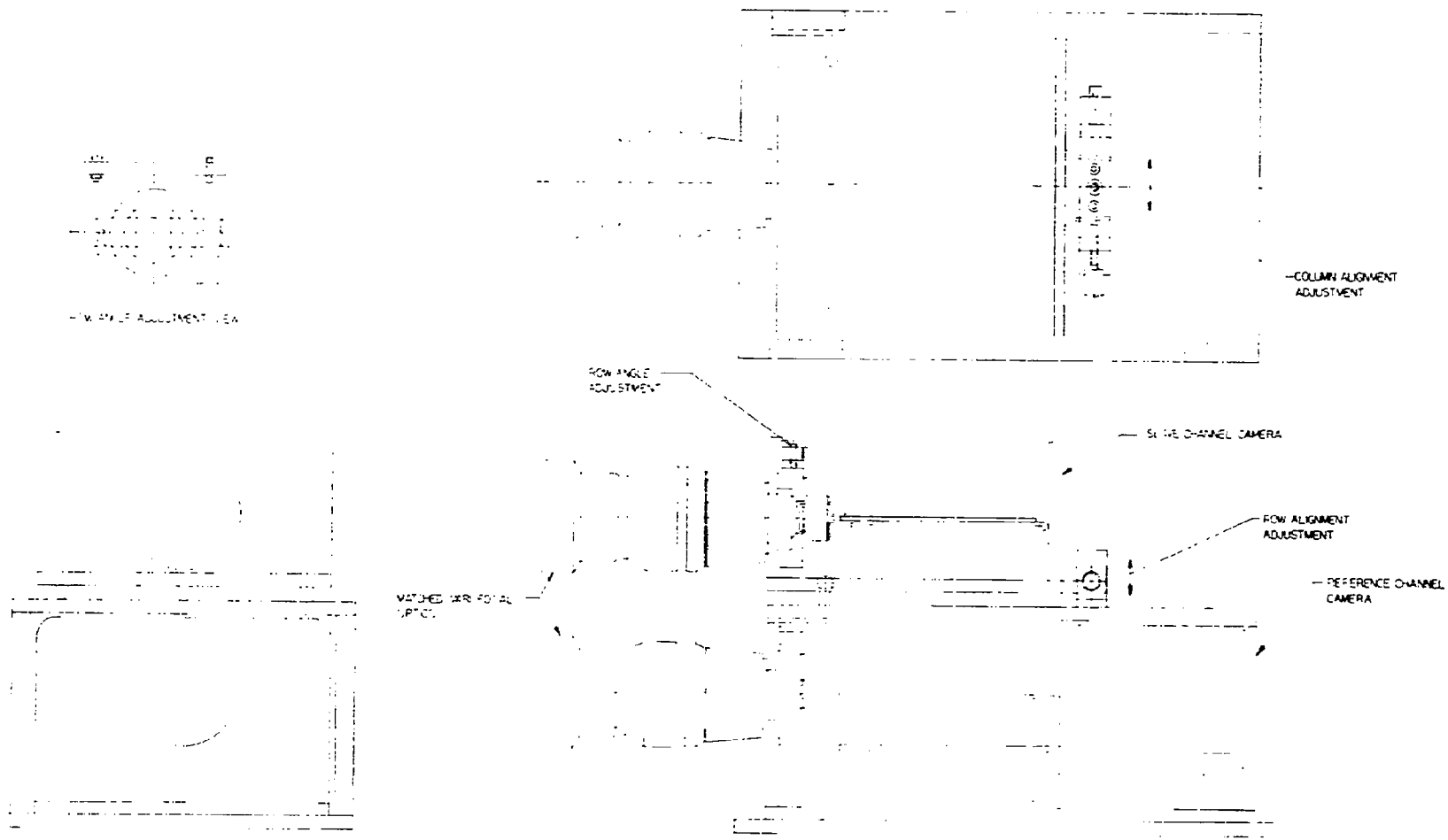


FIGURE 7-8. 244-BORESIGHT TV CAMERA CONCEPT

7.2.4.1 Camera System Performance Analysis

If a low-light-level TV system is used to view equal width multiple-bar test patterns, the observed signal-to-noise ratio is determined by the integration of signal and noise from elemental areas comprising the highlight and background regions of the displayed image. For CCAID-TV systems, the elemental areas correspond to sensor unit cells (pixels) of area A_c.

The observed signal-to-noise ratio (SNR) depends on test image geometry. For equally spaced long bar images it is convenient to define the ratio SNR_o with reference to an image resolution element (resel) of the area A_o equal in height and width to the width of a single white or dark bar space. Assuming negligible signal degradation in video processing and display, the observed resel signal, S_o, is equivalent to:

$$S_o = n_s \ (A_o/A_c) = (n_w - n_b) \ (A_o/A_c) \qquad (1)$$

where: n_s is the number of signal electrons/pixel;

n_w and n_b are the number of electrons/pixel for the highlight and background regions, respectively.

If signal and background shot noise, and amplifier noise, are the dominant components of system noise, the observed noise/resel, $\bar{N}_o$, is given by the RMS summation of noise effects for both highlight and background regions:

$$\begin{aligned} \bar{N}_o &= \bar{n}_{nt} \ (A_o/A_c)^{1/2} \\ &= (\bar{n}_{nw}^2 + \bar{n}_{nb}^2)^{1/2} \ (A_o/A_c)^{1/2} \\ &= (n_w + n_b + 2\bar{n}_{an}^2)^{1/2} \ (A_o/A_c)^{1/2} \end{aligned} \qquad (2)$$

where: $\bar{N}_o$ is observed noise, RMS electrons/resel,

$\bar{n}_{nt}$ is observed noise, RMS electrons/pixel;

$\bar{n}_{nw}$, $\bar{n}_{nb}$ are the RMS noise (electrons/pixel) contributions for highlight and background regions, respectively,

$\bar{n}_{an}$ is amplifier NES value, RMS electrons/pixel

Defining the CCAJD electron image contrast, $C_q = (n_w - n_b)/n_w$, and substituting this expression in equations (1) and (2) yields:

$$S_o = C_q \; n_w \; (A_o/A_c) \tag{3}$$

and,

$$\bar{N}_o = \left[n_w \; (2 - C_q) \; + \; 2 \; \bar{n}_{an}^{\,2} \right]^{1/2} \tag{4}$$

For the bar pattern to be observed, the threshold resel SNR_o value must be equal to or greater than $K_{s/n}$, an empirically determined constant which has been found to be near unity for 30 frame/second TV systems. Thus:

$$SNR_o = S_o/N_o \geq K_{s/n}$$

$$= C_q \, n_w \; (A_o/A_c)^{1/2} \Big/ \left[n_w \; (2-C_q) + 2\bar{n}_{an}^{\,2} \right]^{1/2}$$

which is equivalent to:

$$n_w = K_{s/n} \left[n_w \; (2-C_q) \; + \; 2\bar{n}_{an}^{\,2} \right]^{1/2} \; (A_o \, /A_c)^{1/2} \Big/ \; C_q \tag{5}$$

A quadratic solution for n_w can be obtained from equation (5), but a more useful form of the solution is obtained if the parameters determining n_w and electron image contrast, i.e., highlight signal n_{sw}, optical contrast C, dark signal n_d, and the CCAID CTF function are introduced. Figure 7-9 illustrates the functional relationships for these parameters. It is also convenient to express the final result in terms of specific device parameters and to introduce the conventional TV line per picture height (TVL/PH) definition for resolution which is functionally related to A_o/A_c. The resulting expression, with terms deleted that are not significant when $2M_cC \; (n_d + \bar{n}_{an}^{\,2})^{1/2} >> \; K_{s/n}$, is:

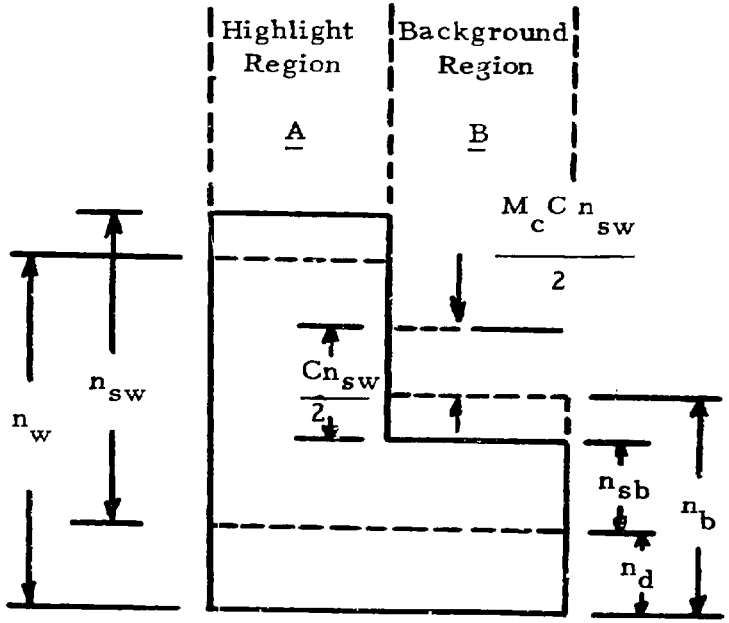
$$n_{sw} = \frac{1.63 \; K_{s/n} \; N_r}{N_t^{1/2} \, M_c C} \left[\frac{1.16 \; K_{s/n} \; N_r \; (2-C)}{N_t^{1/2}} + 1 \right] (n_d + \bar{n}_{an}^{\,2})^{1/2} \tag{6}$$

OPTICAL IMAGE CONTRAST, C

$$C = \frac{n_{sw} - n_{sb}}{n_{sw}}$$

ELECTRON IMAGE CONTRAST, C_q

$$C_q = \frac{n_w - n_b}{n_w} = \frac{M_c C\, n_{sw}}{n_w}$$



$$n_w = n_d + n_{sw} - \frac{C\, n_{sw}}{2} + \frac{M_c C\, n_{sw}}{2}$$

$$= \frac{n_{sw}}{2}(2 - C + CM_c) + n_d$$

M_c IS CCAID CONTRAST TRANSFER FUNCTION $0 \leq M_c \leq 1$

FIGURE 7-9. CONTRAST AND CTF PARAMETERS

where: n_{sw} is the threshold highlight signal at image spatial frequency f→0, electrons/pixel

$K_{s/n}$ is the threshold SNR_o value ($K_{s/n} \approx 1$ for 30 F/S systems)

N_r is the observed or required test bar horizontal resolution at best phasing, TVL/PH

N_t is the total number of CCAID pixels/frame

M_c is the CCAID contrast transfer function

C is input optical image contrast

n_d is the bias or dark electrons/pixel

$\bar{n}_{an}$ is amplifier NES, RMS electrons/pixel

For CCAID-488 sensor design parameters, and $K_{s/n} = 1$, equation (6) reduces to:

$$n_{sw} = \frac{3.8 \times 10^{-3} N_r}{M_c C} \left[2.7 \times 10^{-3} N_r (2-C) + 1 \right] (n_d + \bar{n}_{an}^2)^{1/2} \quad (7)$$

where: $N_r \leq 285$ TVL/PH, and $2M_c C (n_d + \bar{n}_{an}^2)^{1/2} \gg 1$

Assuming a total RMS noise value of 20 electrons, $M_c = 0.7$, and $C = 1$, the detection of half-Nyquist limit bars is predicted to require an n_{sw} value of approximately 22 electrons. For the expected 2854°K responsivity of 20 mA/W, a pixel size of 18 μm x 30 μm, and 1/30 second integration, the required highlight irradiance for a 22 electron signal is 10^{-5} W/m^2.

The total RMS noise is given by the last bracketed term of equation (7); n_d shot noise will be negligible if $n_d < \bar{n}_{an}^2$. For a DFGA NES of 20 electrons it is desirable to limit n_d to 80 electrons or less. The corresponding maximum dark current density with 18 μm x 30 μm cells integrating for 1/30 second is $J_{dmax} = 7 \times 10^{-11}$ A/cm^2. It has been observed that this J_{dmax} requirement can be satisfied with device operating temperatures of -30°C, as described in Section 4.2.2.3.

7.2.4.2 Camera Design with Device Cooling

A design study of thermoelectric cooling techniques for CCAID camera application was initiated during Phase II. The results of this study, which included thermal analyses and laboratory tests, were used to determine design details to be included in the CCAID-488 camera scheduled for delivery during Phase III.

Thermal analysis of several model sensor/cooler configurations confirmed that device connecting lead conductance and gas convection effects account for the major portion of the total cooler heat load, P_T. Typical model analysis results are given in Table 7-1. In this case the total load, due to the combined effects of conduction, radiation, and convection, is predicted to be less than 125 milliwatts for a hot to cold surface temperature differential $\Delta T = 75°C$. The conducted portion (equal to somewhat less than 1/2 of the total load) is kept small by the use of 0.2" long one-mil diameter gold wires in series with each of the 24 connecting leads.

The sensor/cooler enclosure shown in Figure 7-10 was used to test techniques suitable for cooled operation of devices with 24 pin DIP substrates. To minimize ambient to substrate heat transfer, the array PC board is isolated from contact with TE cooler and enclosure surfaces except for Nylon standoffs providing mechanical support. Fly leads of fine copper wire (4-mil diameter) are used to connect the PC traces to the feed throughs located in the enclosure side wall. The laboratory TE cooler was a single-stage module which was not expected to operate efficiently when required to cool from room ambient to temperatures less than -10 to -20°C. However, -10°C operation of CCAID-100 devices was achieved with a cooler power input of 2.2 watts.

The cooler implementation techniques described above, in somewhat modified form, are applicable to CCAID-488 camera design. Figure 7-11 illustrates the proposed packaging concept. The short front-end section is designed as an hermetically-sealed enclosure containing the CCD array, TE module, and a driver-preamp circuit board. The front housing also functions as a support member for C-mount optics. Hermetic integrity of the enclosure is provided by a sealed window immediately behind the lens opening, an O-ring seal at the backplate interface, and hermetic feed throughs for routing electrical connections to the circuit card section at the rear of the camera.

TABLE 7-1

TYPICAL THERMAL ANALYSIS RESULTS

CONDITION DESCRIPTION	$\dot{q}_{cd}$ (Btu/hr)	$\dot{q}_r$ (Btu/hr)	$\dot{q}_{cv}$ (Btu/hr)	P_T (mw)
1. Substrate package size 1/2" x 1/2" Ambient temperature 40°C (104°F) Surface temperature of substrate package -35°C (-31°F) 24 gold leads approximately .001" diameter x .2" long k_{gold} = 170 Btu/hr. ft.^{2}-°F/ft emissivity = .05 (assumed) area of optical window = 1/2" x 1/2"	.228	.010	.181	123
2. Same as above except for hard vacuum within the enclosure	.228	.010	0	70

q_{cd}, q_r and q_{cv} are the conduction, radiation, and convection heat transfer values, respectively (Btu/hr).

P_T is the total cold plate heat load (mw)

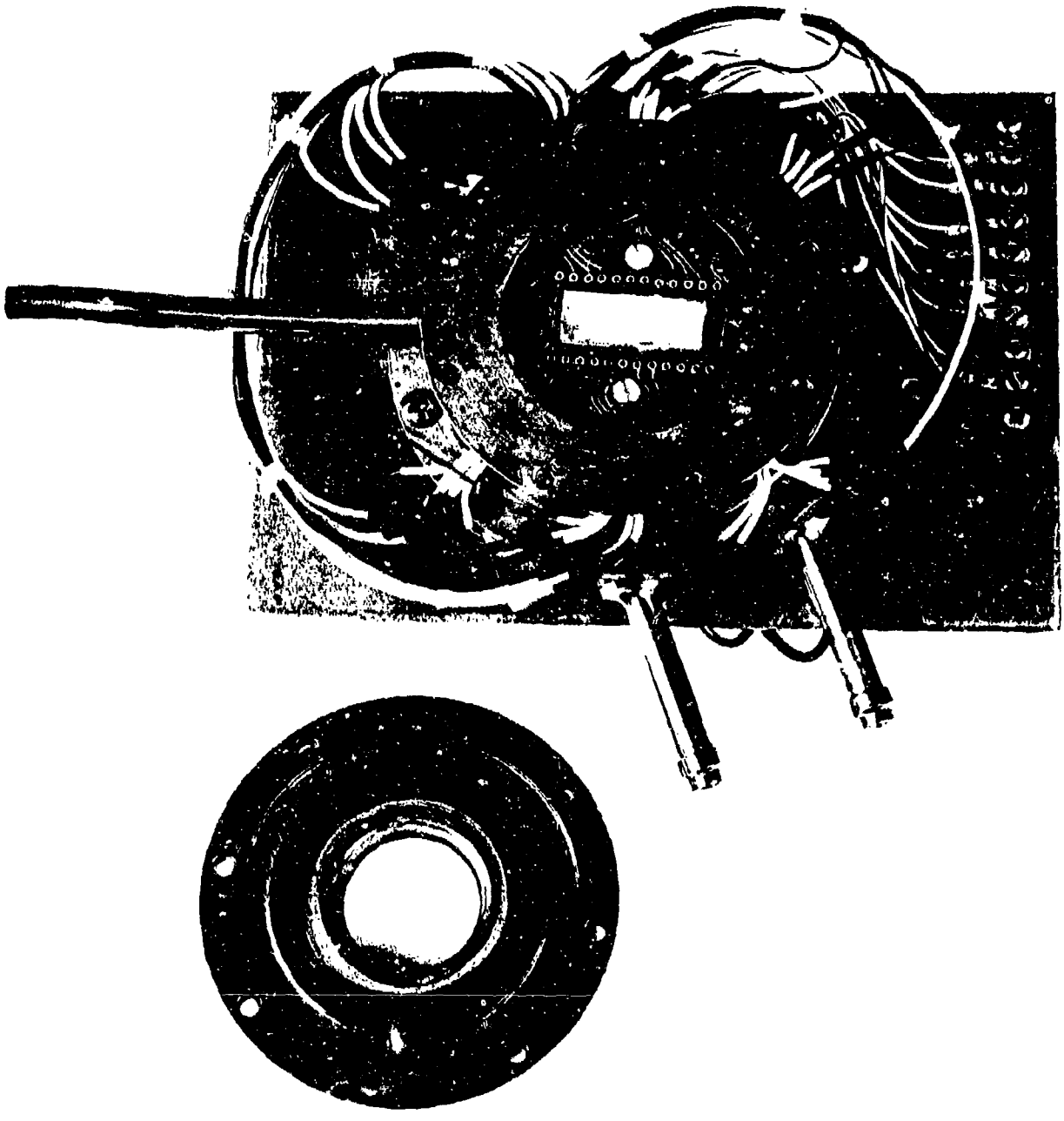


FIGURE 7-10. SENSOR/TE COOLER ENCLOSURE FOR CCAID-100BD TESTS

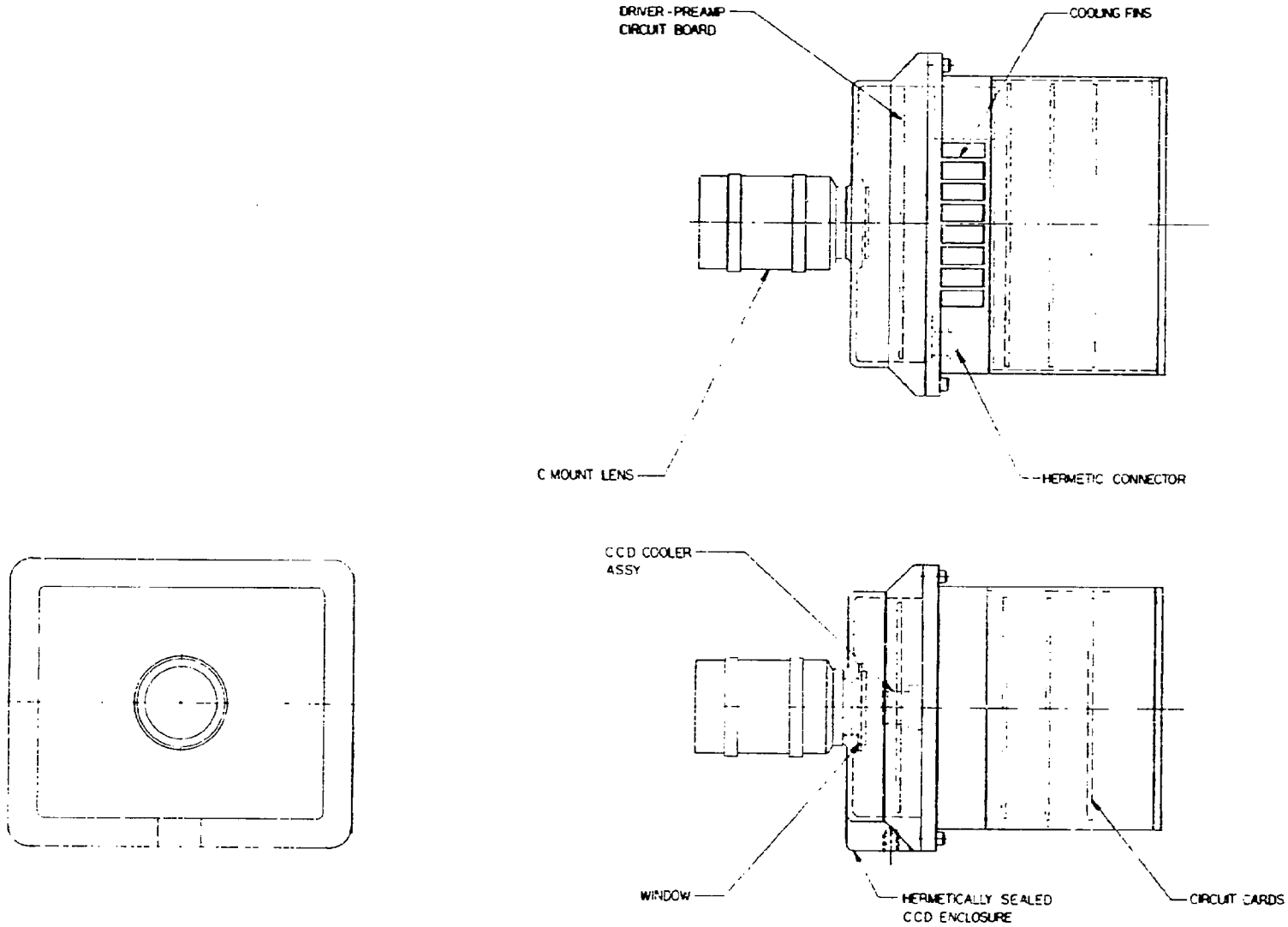


FIGURE 7-11. 488-LLLTV CAMERA CONCEPT

7.3 CCAID-100 BD TELEVISION CAMERA

A television camera system utilizing the CCAID-100 BD sensor was delivered as part of the Phase II program. The system consisted of a totally self-contained camera unit and a modified 8" Conrac display monitor, as shown in the block diagram, Figure 7-12.

The camera unit had the following features:

1) Gamma correction (linear to 0.4)

2) Level dependent horizontal aperture correction

3) Black level stabilization

4) Synchronous (crystal controlled) clock system

5) EIA compatible output (will record on any EIA/JAL video tape recorder).

6) Accepts "C" or "D" mount lenses.

7) CCAID easily replaced if camera is used as test unit.

8) All clock voltages adjustable with easy access to pots.

9) Interfaces with a Conrac 8" Display (modified vertical sweep).

10) Horizontal scan rate 15,625 lines/sec.

11) Field Rate 246 fields/sec.

12) Input power 115V AC.

Several mechanical details simplified the application of the camera for sensor testing. The printed circuit card which held the CCD was easily removed from the camera. This feature was particularly convenient when rewiring of CCD socket connections was necessary to convert from 100B to 100D array operation. In addition, the CCD socket was a zero-insertion force type enabling quick device replacement without stressing the substrate or pin connections.

The completed camera unit, with protective cover and a C-mount lens attached, is illustrated in Figure 7-13.

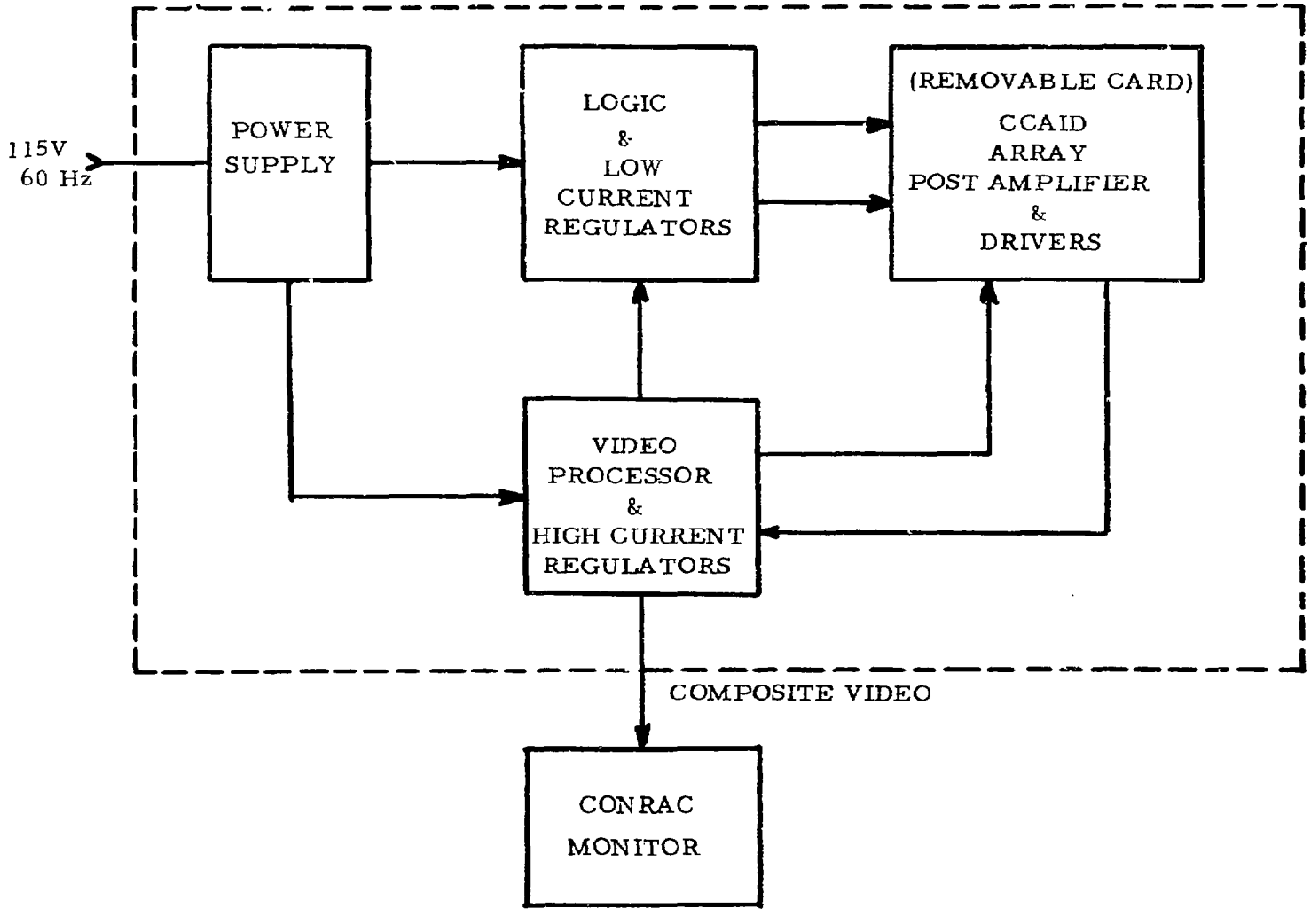


FIGURE 7-12. CCAID-100BD TELEVISION CAMERA SYSTEM

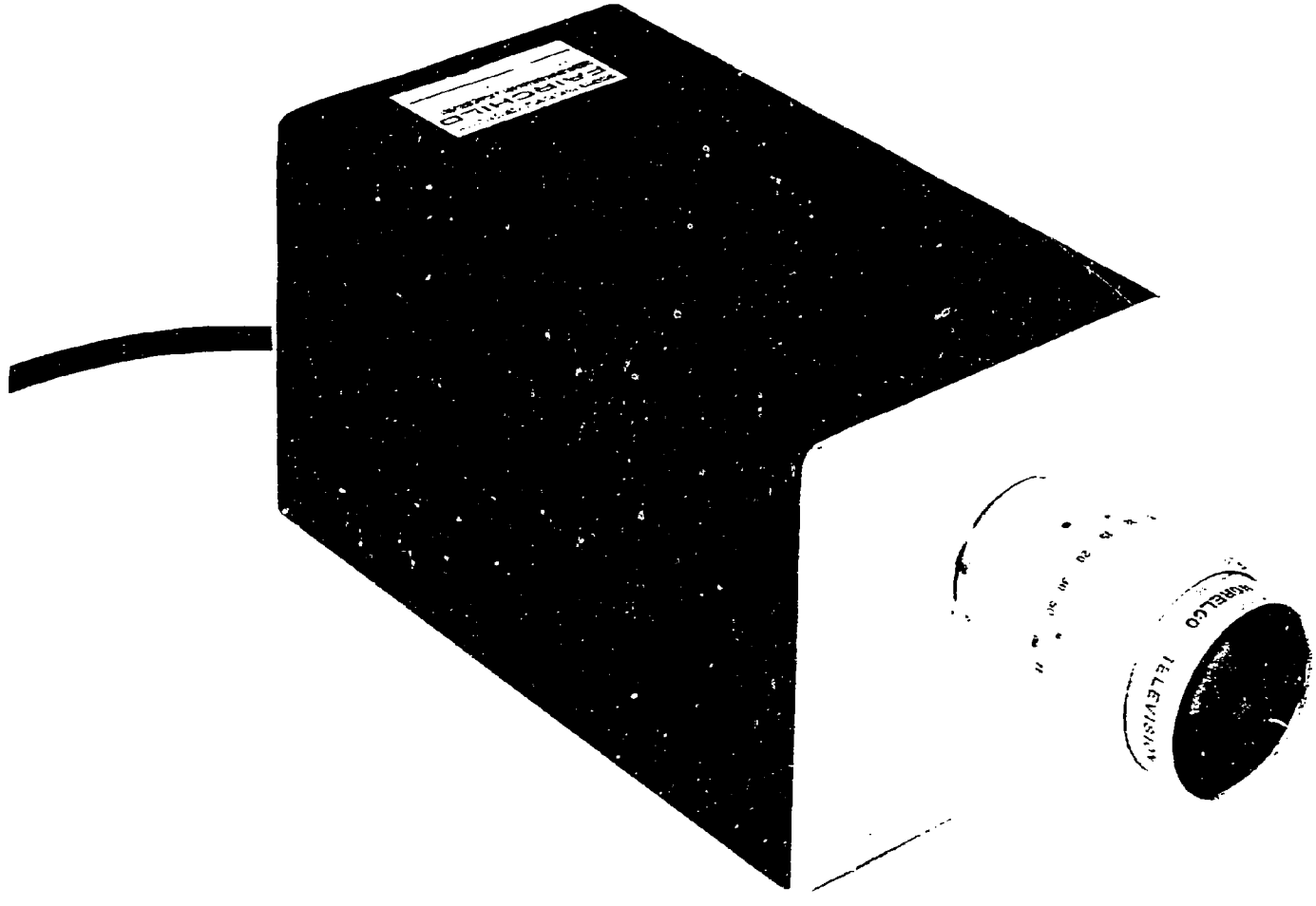


FIGURE 7-13. CCAID-100BD TELEVISION CAMERA

APPENDIX A

FINAL REPORT NO. ED-AX-53

DISTRIBUTED FLOATING-GATE AMPLIFIER

FAIRCHILD SPACE AND DEFENSE SYSTEMS
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Report No. ED-AX-53

DISTRIBUTED FLOATING-GATE AMPLIFIER (DFGA)

FINAL REPORT

October 1974
(Contract Period: August 1973 to August 1974)

for

Naval Electronics Systems Command

Contract No. N00039-74-C-0018

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LIST OF ILLUSTRATIONS (continued)

SECTION 1

INTRODUCTION

This report examines a charge detection device which directly amplifies the signal charge in a charge-coupled-device (CCD) channel. The device is based on the principle that the signal charge in a CCD channel is non-destructively sensed by a "floating-gate" electrode. By repeated sensing of the same signal charge, the signal-to-noise power ratio can be increased by a factor equal to the number of times it is detected. It is from this principle that the name of the device, distributed floating-gate amplifier (DFGA), is derived.

A test structure of the device employs twelve charge-amplifying stages to sense an extremely small amount of charge in a buried-channel CCD. RMS noise has been estimated to be approximately 13 electrons. Signal charge in the range from 30 to 10^5 electrons has been detected with a bandwidth of 3 MHz at room temperature.

The "floating-gate" concept is discussed in Section 2 for a single-stage floating-gate amplifier (SSFGA). The DFGA concept is then presented qualitatively in Section 3. The DFGA test-structure design and quantitative analysis is given in Section 4. Section 5 contains a complete noise analysis. Section 6 presents experimental results obtained with the test structure; it includes both small signal detection results and noise characterization. Conclusions derived from this effort are given in Section 7.

SECTION 2

THE FLOATING-GATE CONCEPT

2.1 THEORETICAL CONSIDERATIONS FOR A SINGLE-STAGE FLOATING-GATE AMPLIFIER

The floating-gate concept is best described by considering a single stage floating-gate amplifier (SSFGA), which is shown schematically in Figure 2.1.1. In operation, the charge to be sensed is brought under the floating gate by manipulation of the potentials of adjacent charge-coupling electrodes. This signal charge electrostatically produces a change in the potential of the floating gate. The floating gate capacitively couples the signal electrons in the CCD channel and the current in the metal-oxide-semiconductor transistor (MOST) channel; there is no conductive contact to either channel. Since the signal electrons remain isolated in the CCD channel, they may be moved downstream in the CCD channel in the conventional fashion and may be sensed repeatedly by additional floating gates. The bias electrode over the floating gate determines the dc floating gate potential as well as the potential in the CCD channel to obtain efficient charge transfer.

A cross-sectional view of an SSFGA is shown in Figure 2.1.2. In this figure, C_1 is the capacitance between the signal electrons and the floating gate; C_2 is the capacitance between the floating gate and the bias

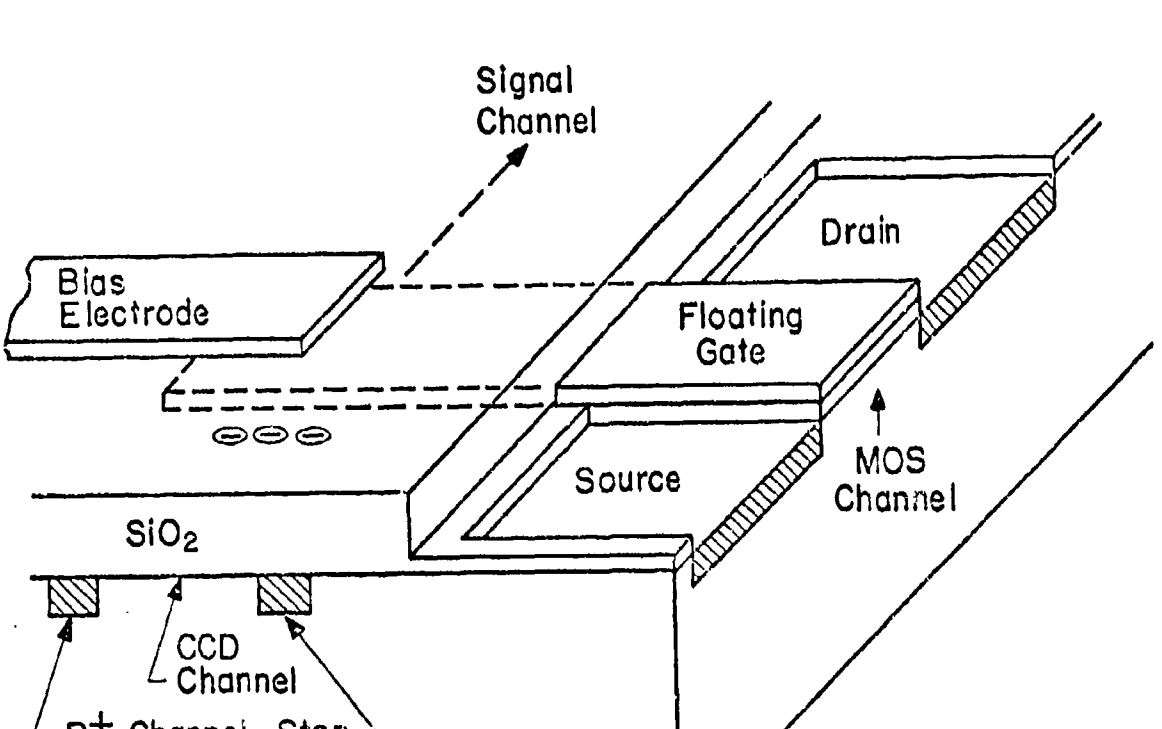


Figure 2.1.1 A Single-Stage Floating-Gate Amplifier.

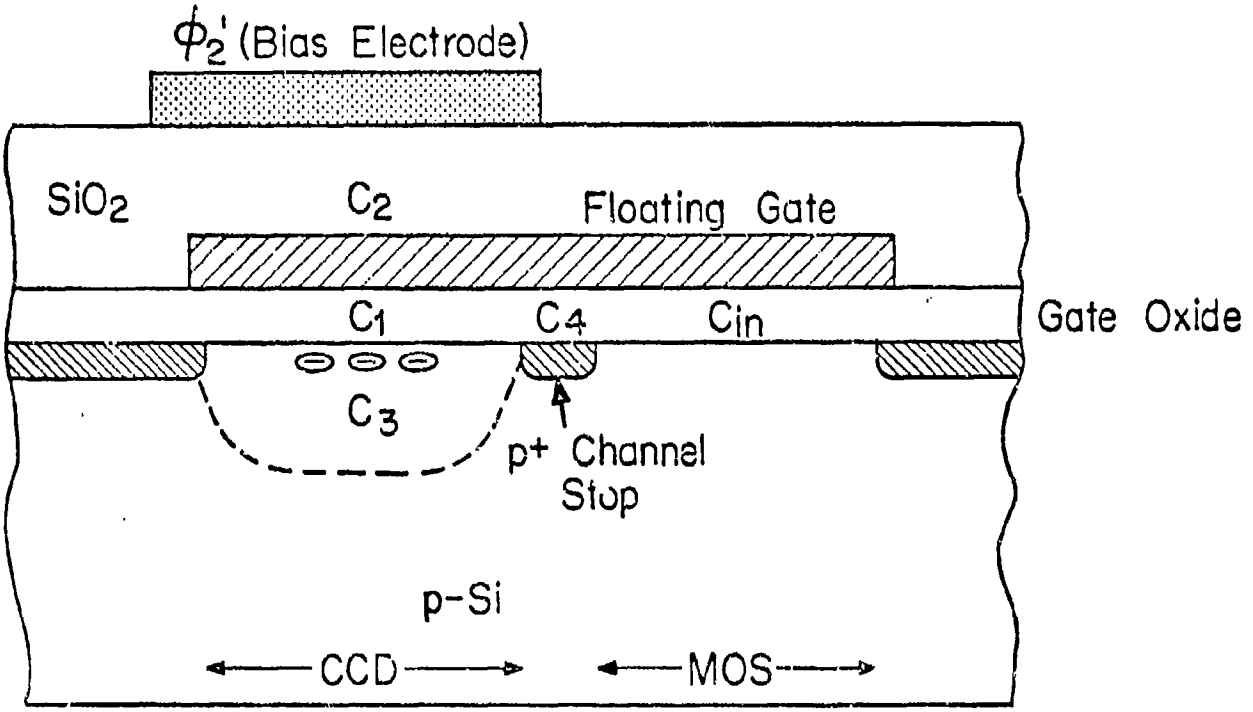


Figure 2.1.2 Cross-sectional View of an SSFGA.

electrode; C_3 is the depletion capacitance between the signal electrons and the substrate (ground); and C_4 is the stray capacitance from the floating gate to the channel stop in the substrate. The MOS transistor is represented by its input capacitance C_{in} where this value depends on the bias condition of the circuit.

If a charge of ΔQ coulombs appears under the floating gate, the voltage it produces between the floating gate and ground is:

$$\Delta V_{FG} = \frac{\Delta Q}{C_{FG}} \qquad (2.1.1)$$

where C_{FG} is defined as the floating gate capacitance and is given by:

$$C_{FG} = C_2 + C_4 + C_{in} + \frac{C_3}{C_1} \quad (C_1 + C_2 + C_4 + C_{in}) \qquad (2.1.2)$$

The floating gate responsivity is defined as:

$$R_{FG} = \frac{q}{C_{FG}} \qquad (2.1.3)$$

where q is the electronic charge.

In order to maximize the floating gate responsivity, C_1 should be maximized while C_2, C_3, C_4 and C_{in} should be minimized.

The SSFGA can be biased as a source follower by connecting a resistor R_S as shown in Figure 2.1.3. In this configuration, the final SSFGA output

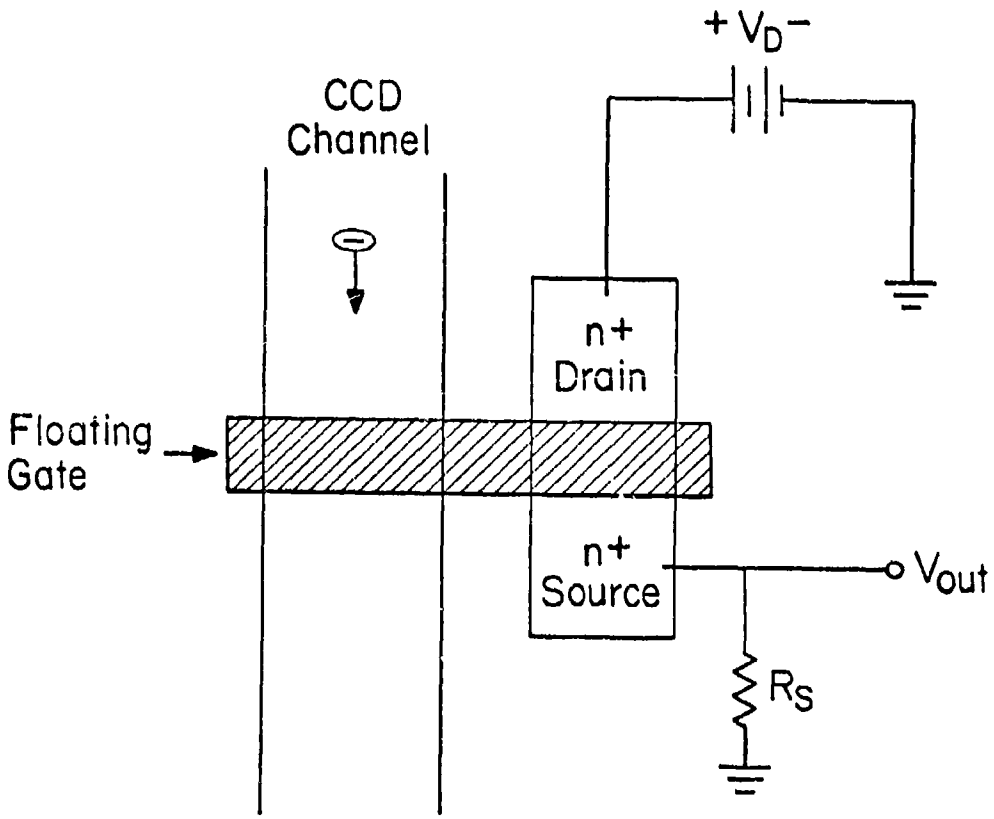


Figure 2.1.3 An SSFCA Biased in a Source-Follower Configuration.

is given by:

$$V_{OUT\ SSFGA} = R_{FG}\, N\, \frac{gmR_S}{1 + gm\, R_S} \qquad (2.1.4)$$

where N is the number of signal electrons under the floating gate in the CCD channel, gm is the transconductance of the floating gate transistor, and R_{FG} is given in equation (2.1.3).

2.2 PERFORMANCE OF A SINGLE-STAGE FLOATING-GATE AMPLIFIER

The single-stage floating-gate amplifier has been examined previously under contract N00014-72-C-0344. Excerpts of data from the final report are given for explanatory purposes.

A typical SSFGA output waveform is shown in Figure 2.2.1. It can be seen that a minimal amount of clock interference is present in the output. The SSFGA responsivity measurement is plotted in Figure 2.2.2. Since no reset of the channel potential is necessary, kTC reset noise associated with conventional gated-charge detectors does not exist in an SSFGA. Noise sources in an SSFGA are the thermal and 1/f noise in the MOST channel. Figure 2.2.3 shows that the measured SSFGA noise spectrum is indeed similar to that of an equivalent MOS transistor.

The nondestructive-signal nature of the SSFGA is illustrated in Figure 2.2.4 where a signal charge was detected with no attenuation by a conventional gated-charge detector after it had been detected by an SSFGA.

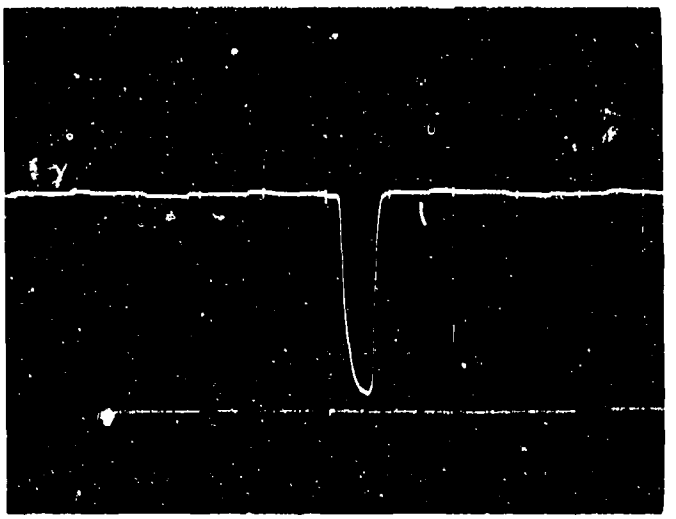


Figure 2.2.1 A Typical SSFGA Output Waveform shows Minimum Clock Interference
Horizontal scale: 1 μsec/div.
Vertical scale: 0.5 V/div.

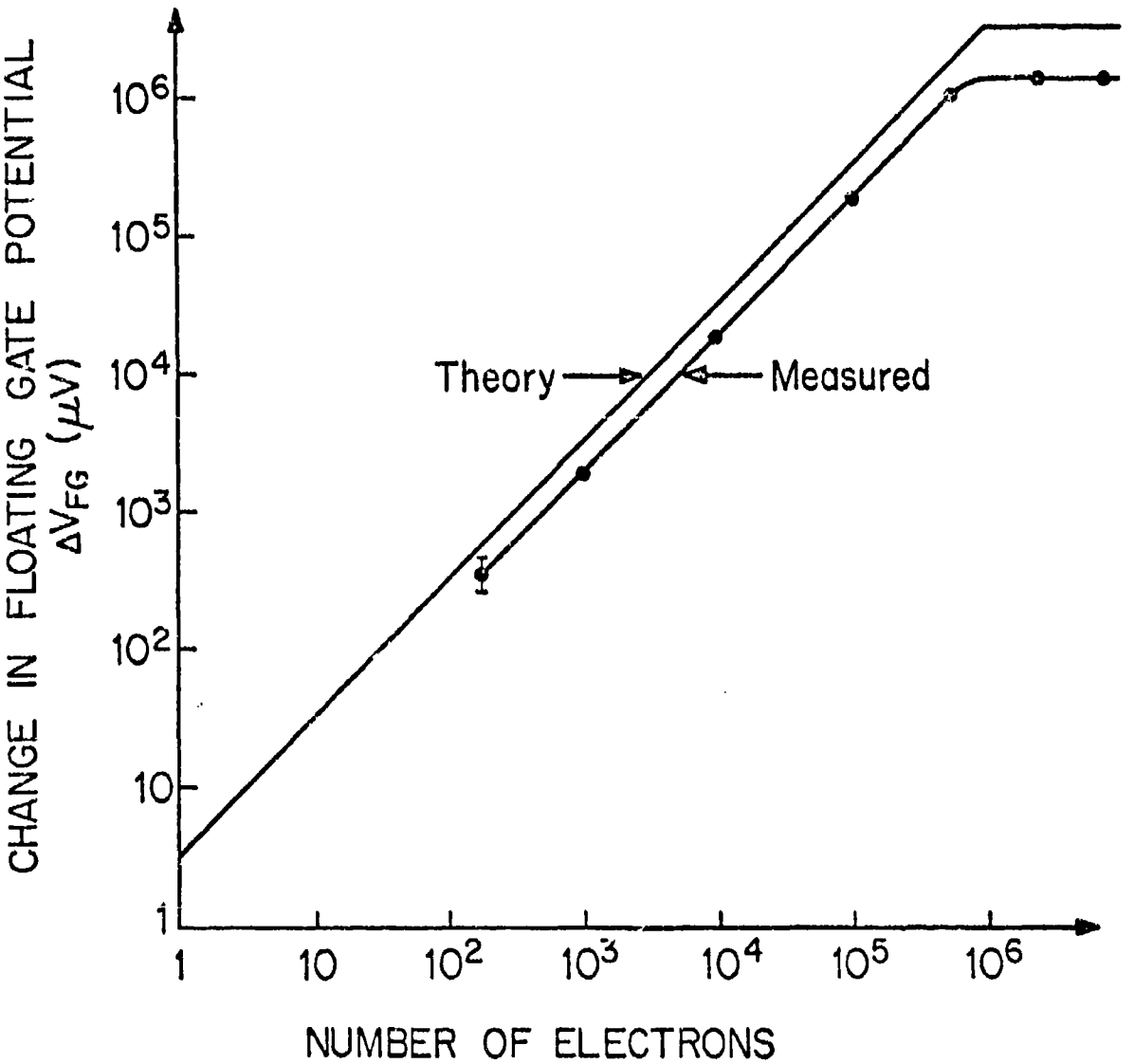


Figure 2.2.2. Sensitivity Measurement of an SSFGA

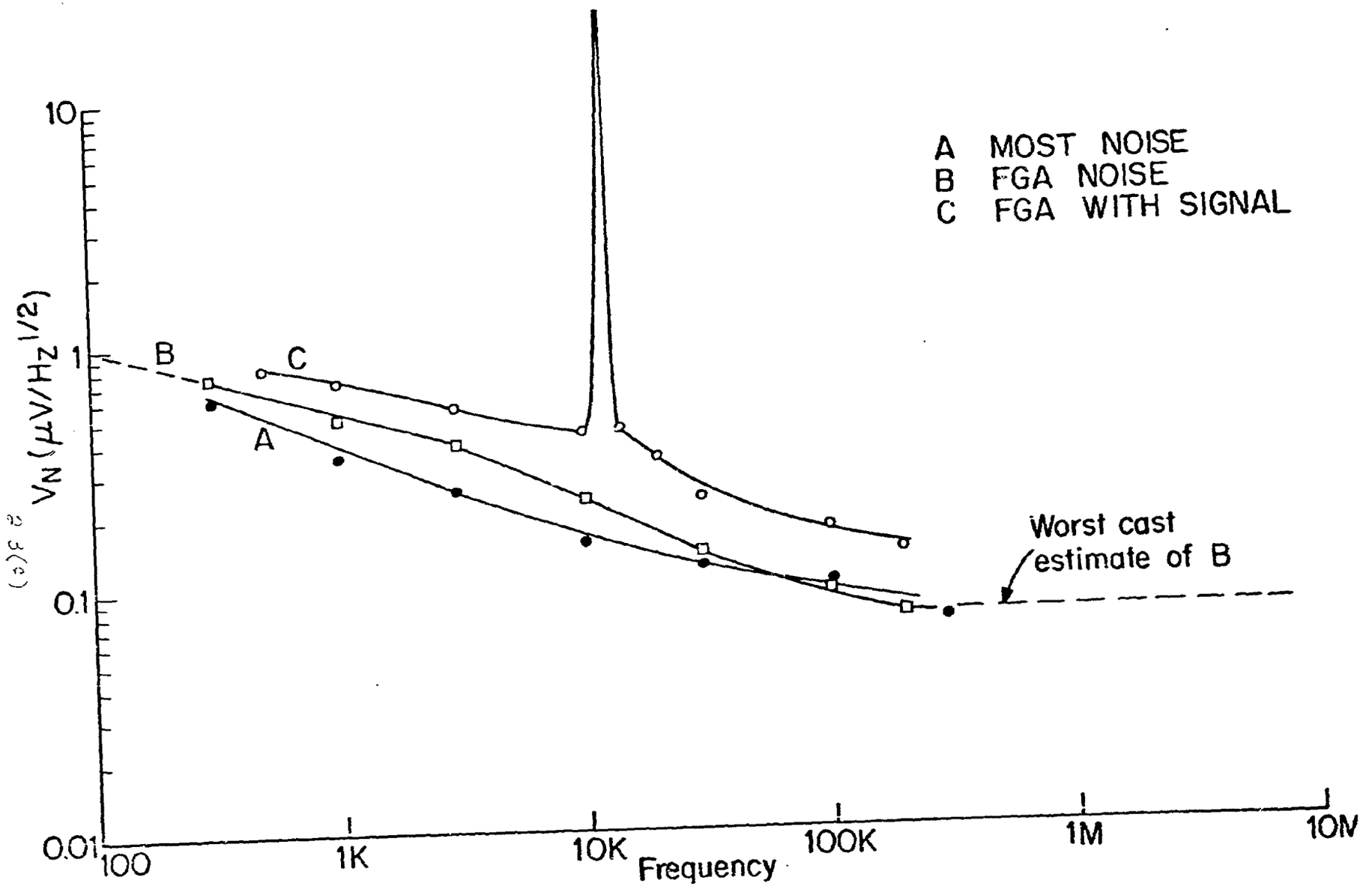


Figure 2.2.3 Measured SSFGA Noise Spectrum as Compared with that of an MOS Transistor.

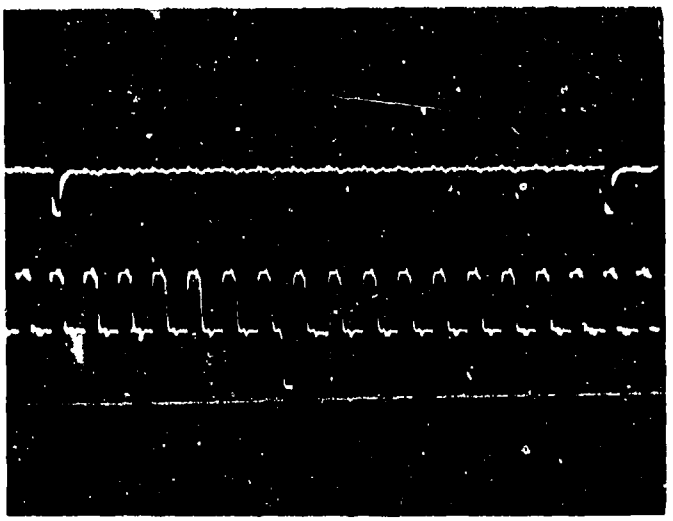


Figure 2.2.4 SSFGA and DDA Outputs show the Nondestructive Nature of an FGA
Horizontal scale: 5 μsec/div.
Vertical scale: 1 V/div.

SECTION 3

THE DISTRIBUTED FLOATING-GATE AMPLIFIER CONFIGURATION

3.1 BASIC CONCEPT

A schematic diagram of a twelve-stage DFGA is shown in Figure 3.1.1. The device consists of an input CCD register, a bank of MOST charge amplifiers with floating-gate inputs, an output CCD register, and an output amplifier. As the signal charge is transferred through the input register, each of the charge amplifiers in turn detects the signal charge with its floating gate and injects a corresponding amount of amplified charge into the output register. Since the output register is clocked by the same phase lines as the input register, output charge, which corresponds to a particular input packet, is summed in the output register and the signal is reconstructed in the same time domain. This is discussed in detail in Section 3.2. The total charge in the output register is finally detected by an output amplifier, which is an SSFGA like that in Section 2. A sink diode is provided at the end of each register to remove charge from the device.

A single DFGA charge amplifier stage consists of a source, a floating-gate, a bias electrode, a control gate, and a dc gate, which serves to minimize clock coupling from the control gate to the floating N+ diffusion, as shown in Figure 3.1.2.

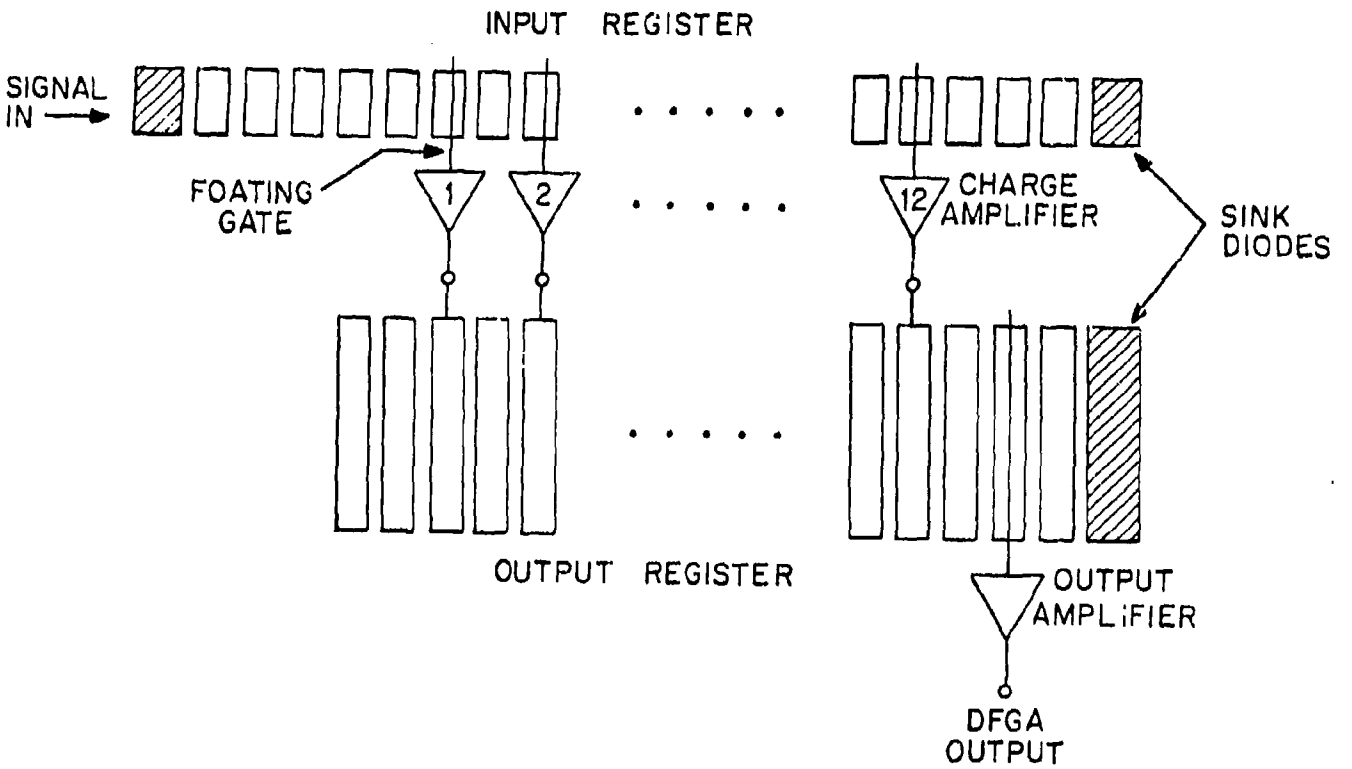


Figure 3.1.1 Schematic Diagram of a Twelve-Stage DFGA.

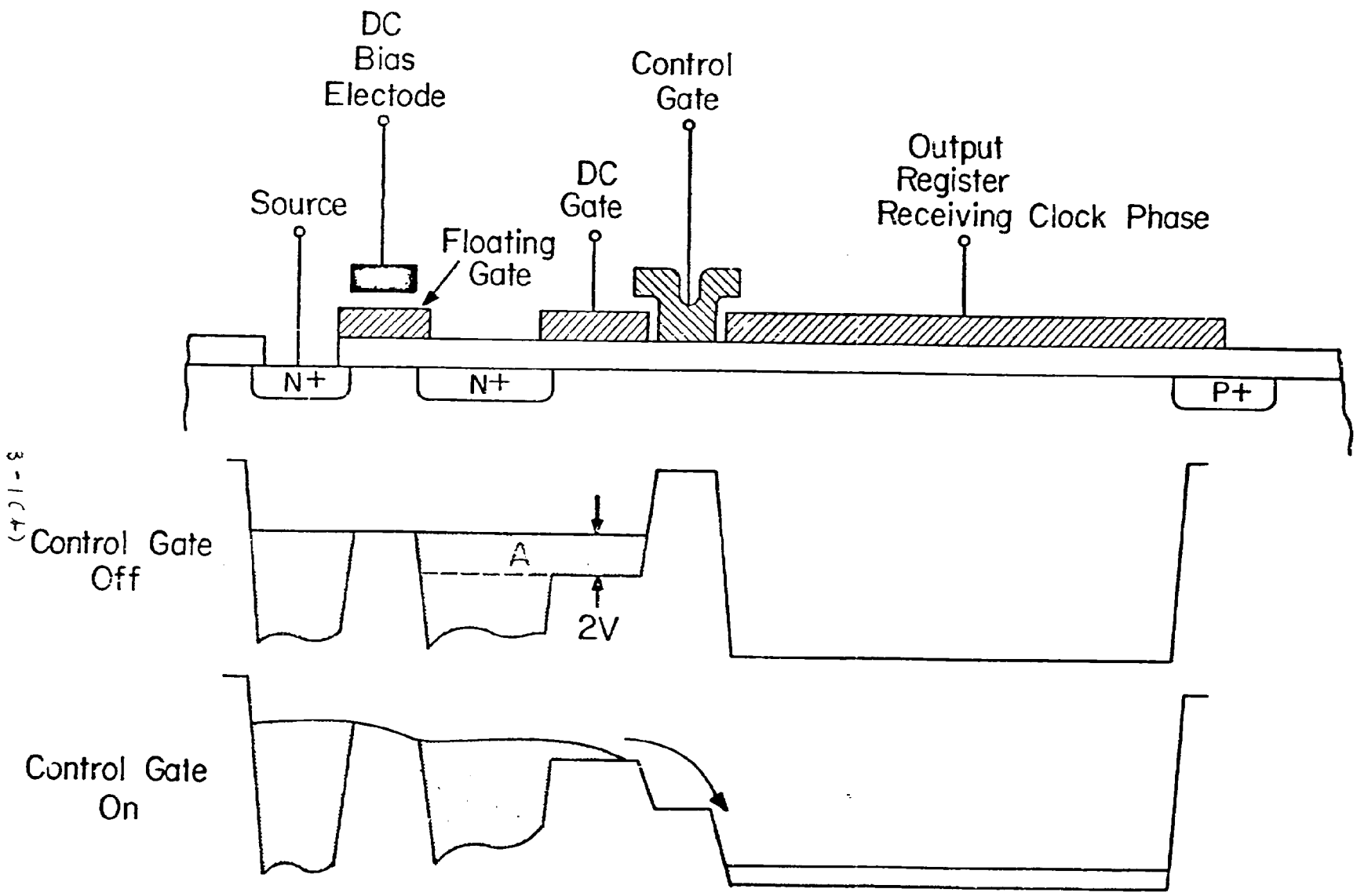


Figure 3.1.2. Cross-sectional View of the Charge Amplifier Showing the Origin of Two Noise Sources

The potential well profiles of Figure 3.1.2 show how charge control is achieved. During the period when a signal charge packet in the input register is under the floating gate, the control gate is pulsed "on" for a precise time interval. During this time interval, both a small fixed charge and a signal-dependent current flow. The small fixed charge will be considered in Section 5.3. The magnitude of the signal-dependent current is determined by the potential difference between the floating gate and the source. The larger the initial charge packet in the input register, the lower is the floating-gate potential, and, therefore, the less current that flows into the output register. The dc bias electrode controls the dc potential of the floating gate like the bias electrode of the SSFGA described in Section 2.1. The layout of the charge amplifier is presented in Section 4.

3.2 PRINCIPLES OF OPERATION

The operation of the DFGA can be illustrated by considering a hypothetical three-stage DFGA as shown in Figure 3.2.1. The input charge amplifiers are inverting amplifiers, as described in Section 3.1, in the sense that the greater the signal charge present in the input register, the less is the charge that flows into the output register. Figure 3.2.2(a) illustrates the condition when a small signal charge packet is transferred into a cell of the input register and the charge amplifier is not activated, i.e., the control gate is "off". Figure 3.2.2 (b) shows that after the activation of the charge amplifier, i.e., the control gate is "on", a large amount of the charge flows

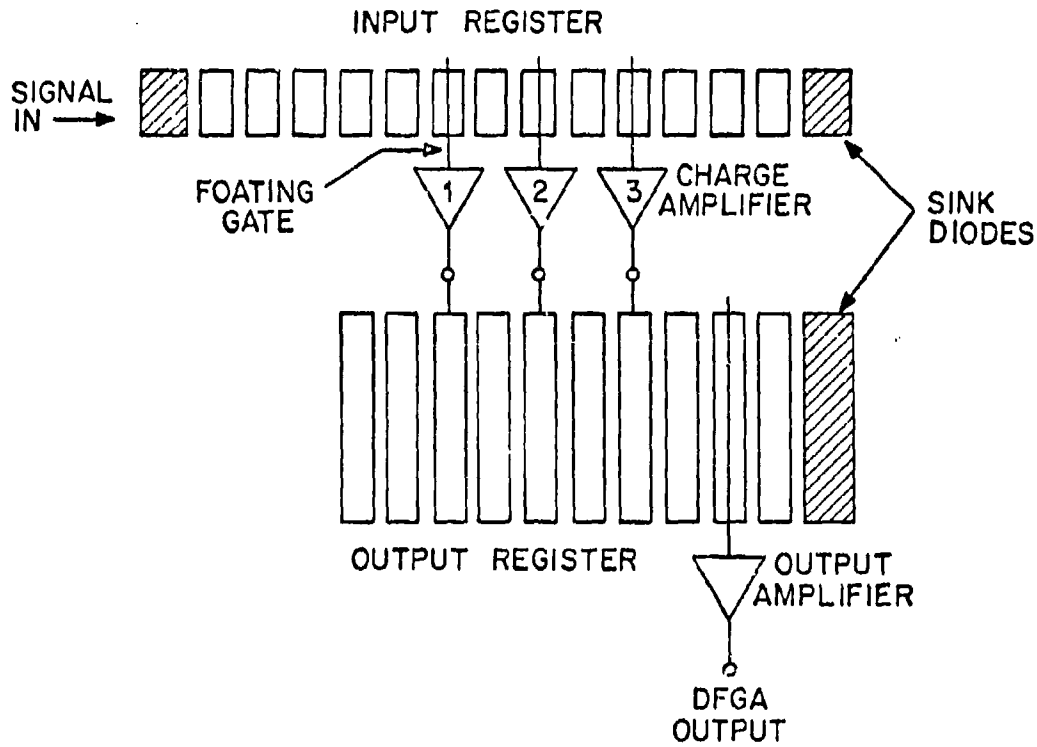


Figure 3.2.1 A Three-stage DFGA for Illustrating Basic Operations.

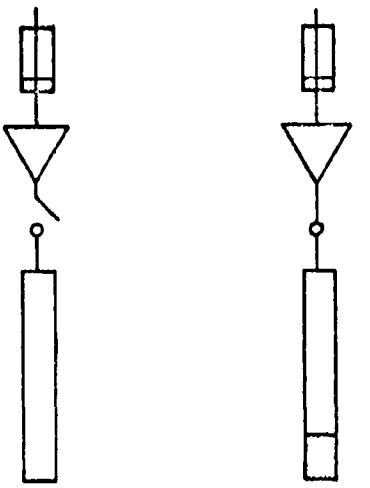


Figure 3.2.2 A Small Signal-Charge Packet in the Input Register Results in a Large Charge Packet in the Output Register.

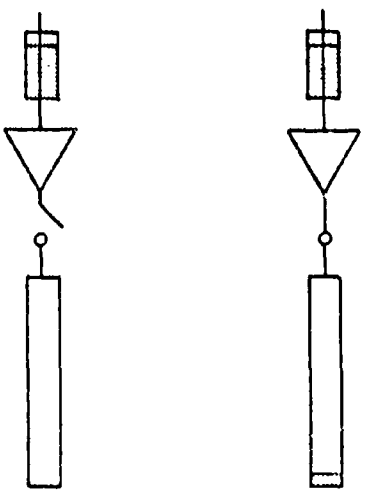
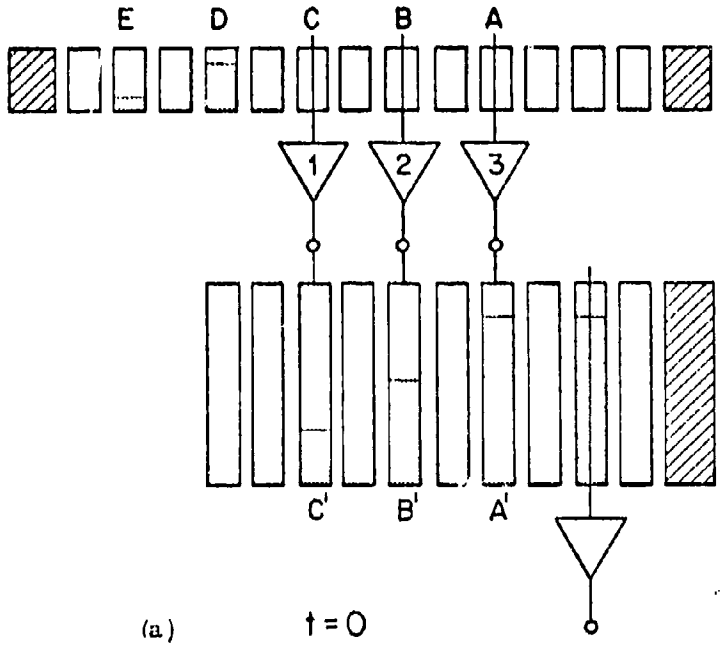


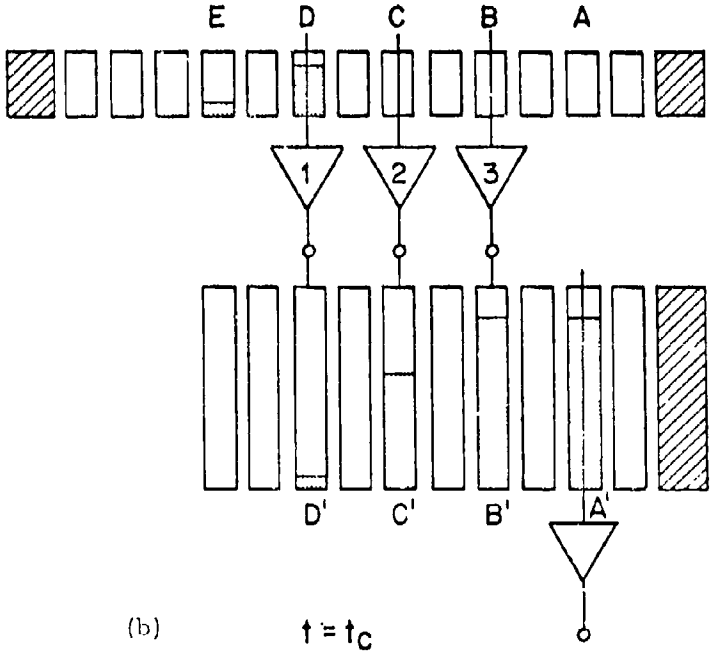
Figure 3.2.3 A Large Signal-Charge Packet in the Input Register Results in a Small Charge Packet in the Output Register.

into the output register. Figures 3.2.3 (a) and (b) show that when a large signal charge packet is present in the input register, a small amount of charge is injected into the output register when the control gate is pulsed "on".

DFGA operation can be described in the following sequence. Figure 3.2.4 (a) illustrates the initial (t = 0) charge distribution in the DFGA after a long series of empty charge packets have been transferred along the input register. Figure 3.2.4 (b) shows that one clock cycle later ($t = t_c$) a large charge packet D has been transferred under the floating gate of the first charge amplifier stage. After the control gate has been pulsed "on", a small amount of charge D' is injected into the output register. Figure 3.2.4 (c) shows that at $t = 2t_c$, charge packet D has been transferred under the floating gate of the second charge amplifier stage while the corresponding charge packet D' in the output register has also been transferred to the corresponding position. After the control gate is pulsed "on", another small amount of charge is added to the charge packet D'. Figure 3.2.4 (d) illustrates the charge conditions at $t = 3t_c$. At $t = 4t_c$, the charge packet D' has been transferred under the floating gate of the output amplifier where it produces the final DFGA output. The condition for a small charge packet that is transferred along the input register is demonstrated by charge packets E and E' in the same sequence.



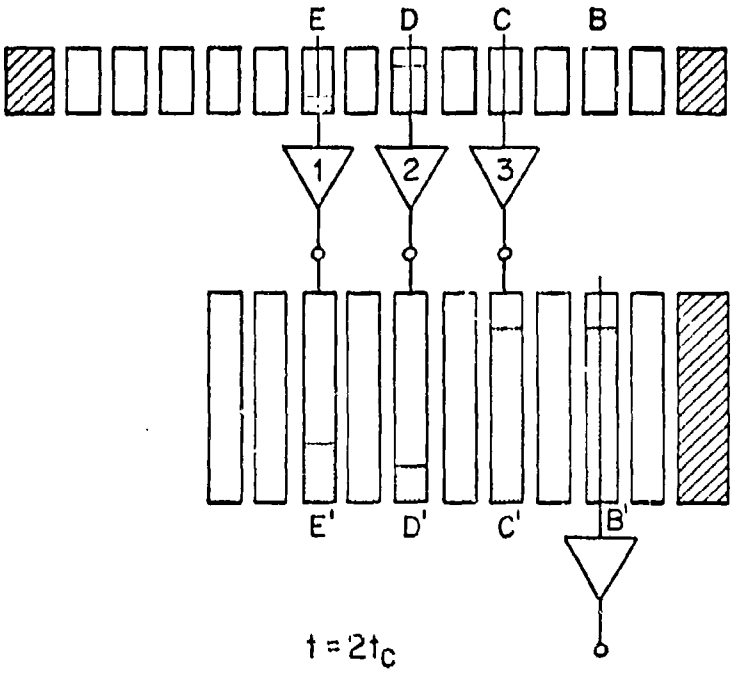
(a) $t = 0$



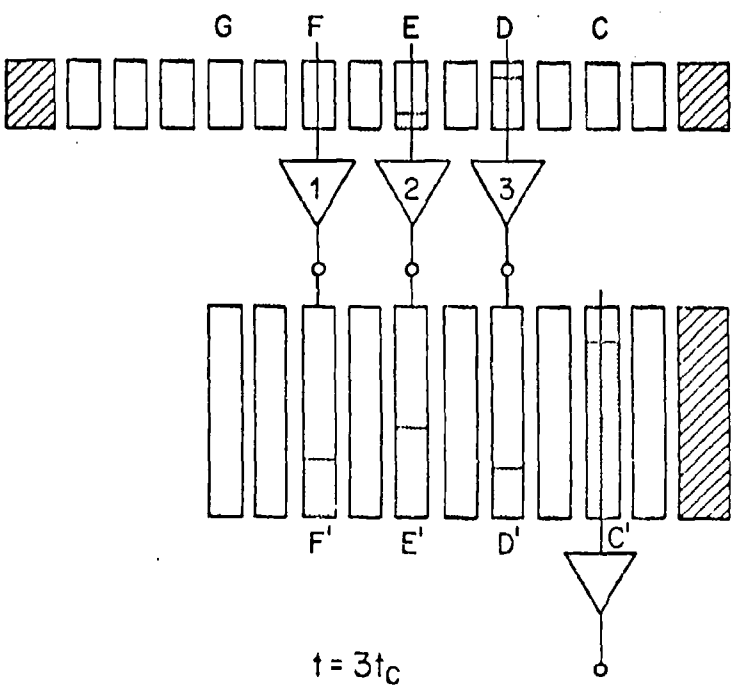
(b) $t = t_C$

Figure 3.2.4 Charge Distribution in a Three-stage DFGA at VArious Time Intervals Showing how Charge Summing is Obtained. (Sheet 1 of 3)

3.3(a)

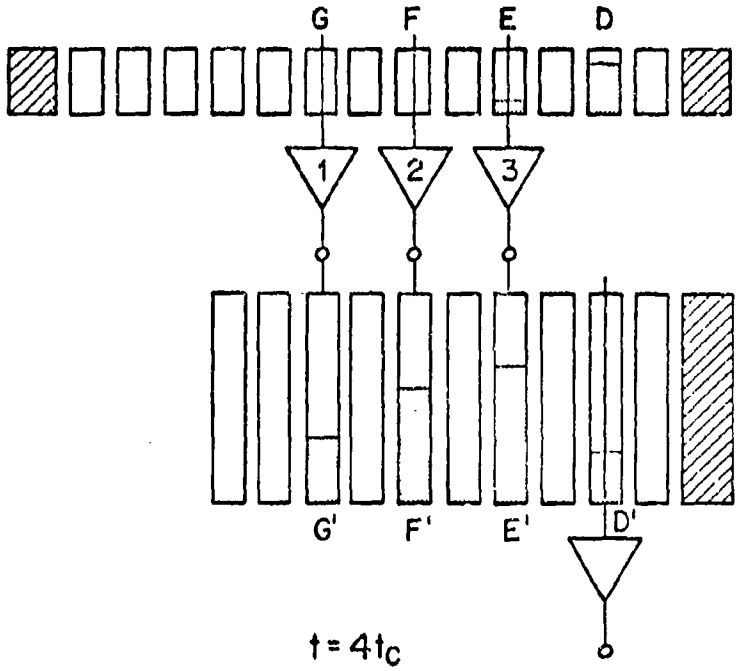


(c)

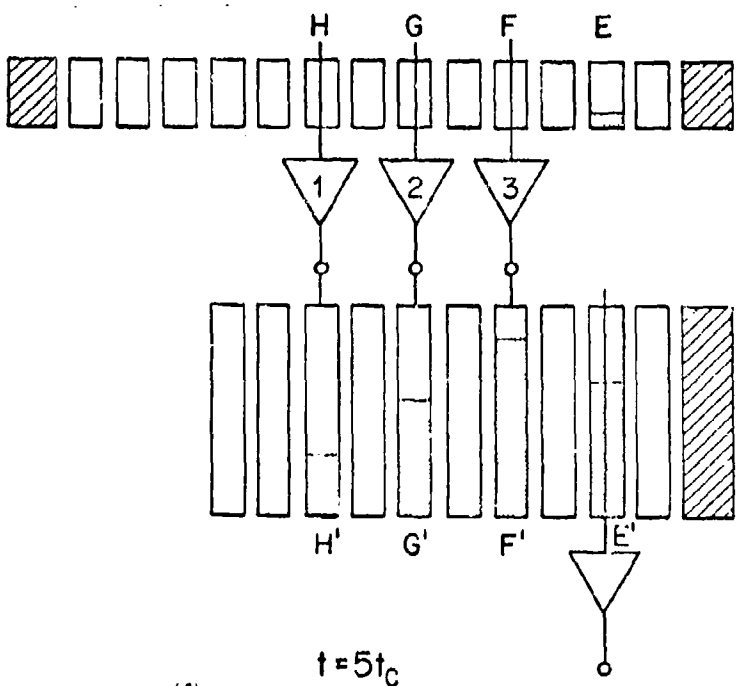


(d)

Figure 3.2.4. Sheet 2 of 3



(e)



(f)

3.3(c) Figure 3.2.4. Sheet 3of 3

At $t = 5t_c$, E' is under the floating gate of the output amplifier and D' is transferred into the sink diode. The DFGA output waveform is illustrated in Figure 3.2.5. The DFGA output that corresponds to the initial charge packet D appears at $t = 4t_c$. The DFGA output for zero initial signal charge is indicated by V_{Bias}. The signal output for D, which is the difference between the DFGA output and V_{Bias}, is designated by V_S. The DFGA output at $t = 4t_c$ corresponds to a large initial signal charge in the input register. The DFGA output at $t = 5t_c$ corresponds to the small initial signal charge packet E in the input register.

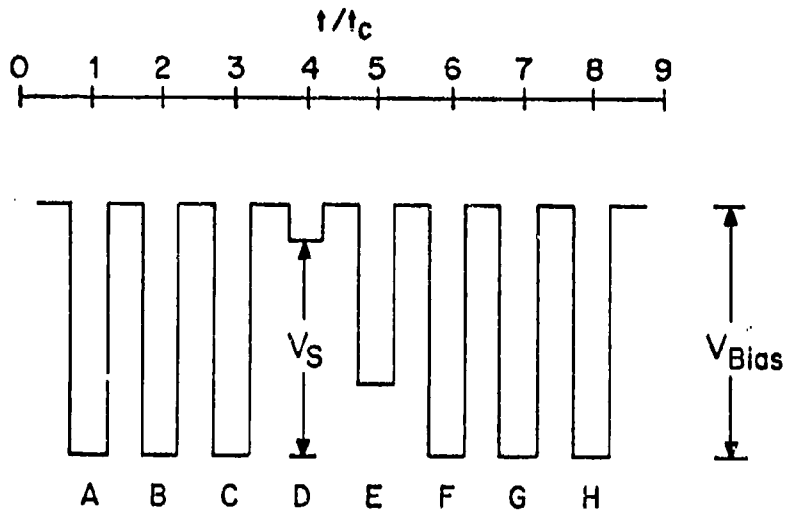


Figure 3.2.5 A DFGA Output Waveform for the Input Signal Charge Packets in Figure 3.2.4.

SECTION 4

DESIGN AND ANALYSIS OF THE DFGA TEST STRUCTURE

A photograph of the twelve-stage DFGA test structure is shown in Figure 4.1. The principal sections are labeled, namely, the input register, the charge amplifier, the output register and the output amplifier.

4.1 DESIGN OF THE INPUT REGISTER

A cross-sectional schematic view of the input register is shown in Figure 4.1.1. It may be noted that two polysilicon layers and four clock lines are employed in this design to provide maximum flexibility of clocking. The floating gates, ϕ_1 and ϕ_3, are defined by the lower polysilicon layer; ϕ_2 and ϕ_4 are defined by an overlapping polysilicon layer. An aluminum bias electrode over the floating gate controls the potential of the CCD channel in the region of the floating gate.

Several clocking modes can by employed with this double-poly overlapping-gate structure. A modified four phase clock timing diagram is shown in Figure 4.1.2. The bias electrode is connected to a dc voltage source. The CCD channel potential under the bias electrode, BE, is then half way between the channel potentials induced by the high and low levels of the $\phi_{1,\ 2,\ 3,\ 4}$ clocks. The signal charge packet is under the floating gate when ϕ_2 and ϕ_4 are low, which is approximately 20% of the cycle. A 1-1/2 phase clocking mode is illustrated in Figure 4.1.3. Here, ϕ_2 and

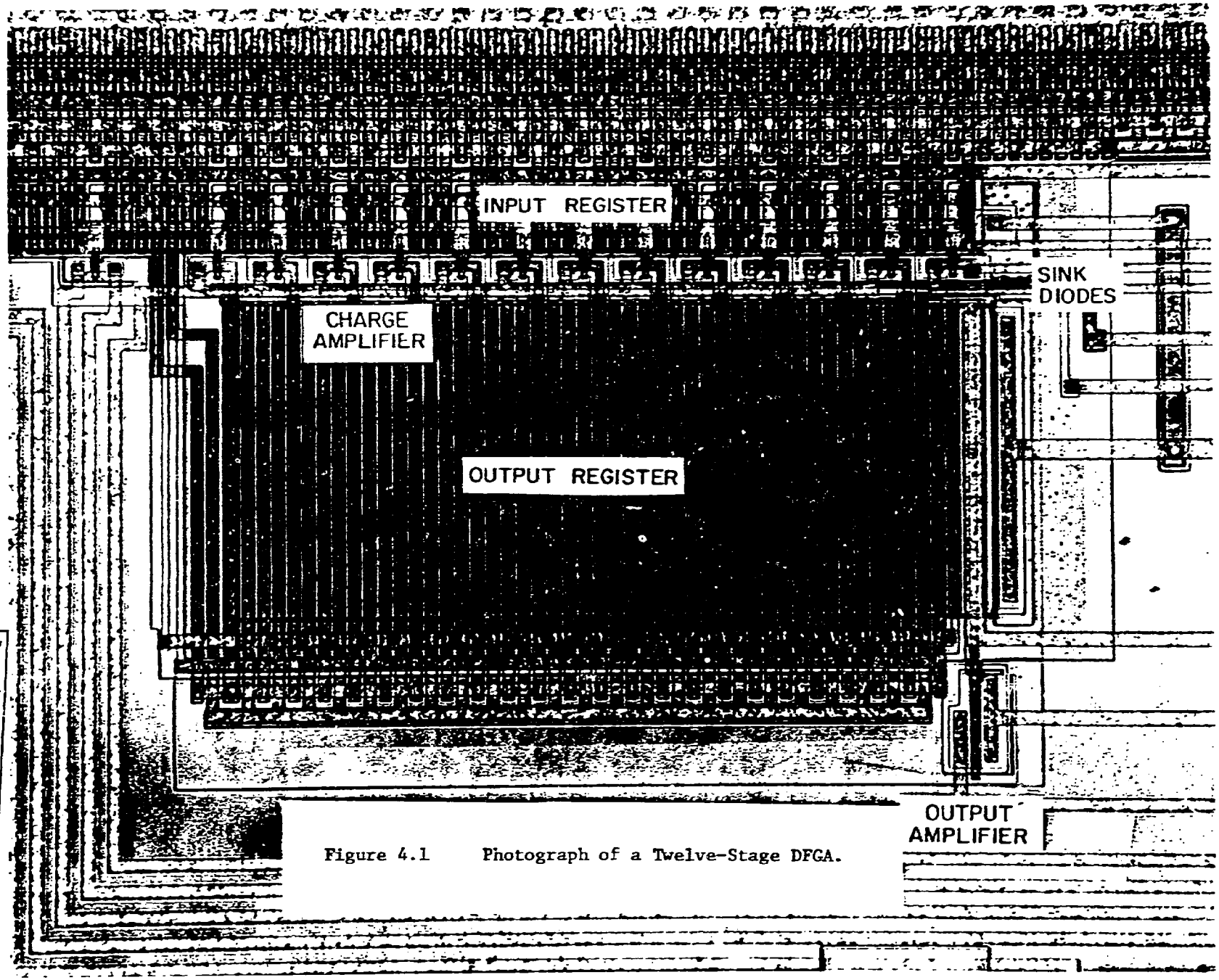


Figure 4.1 Photograph of a Twelve-Stage DFGA.

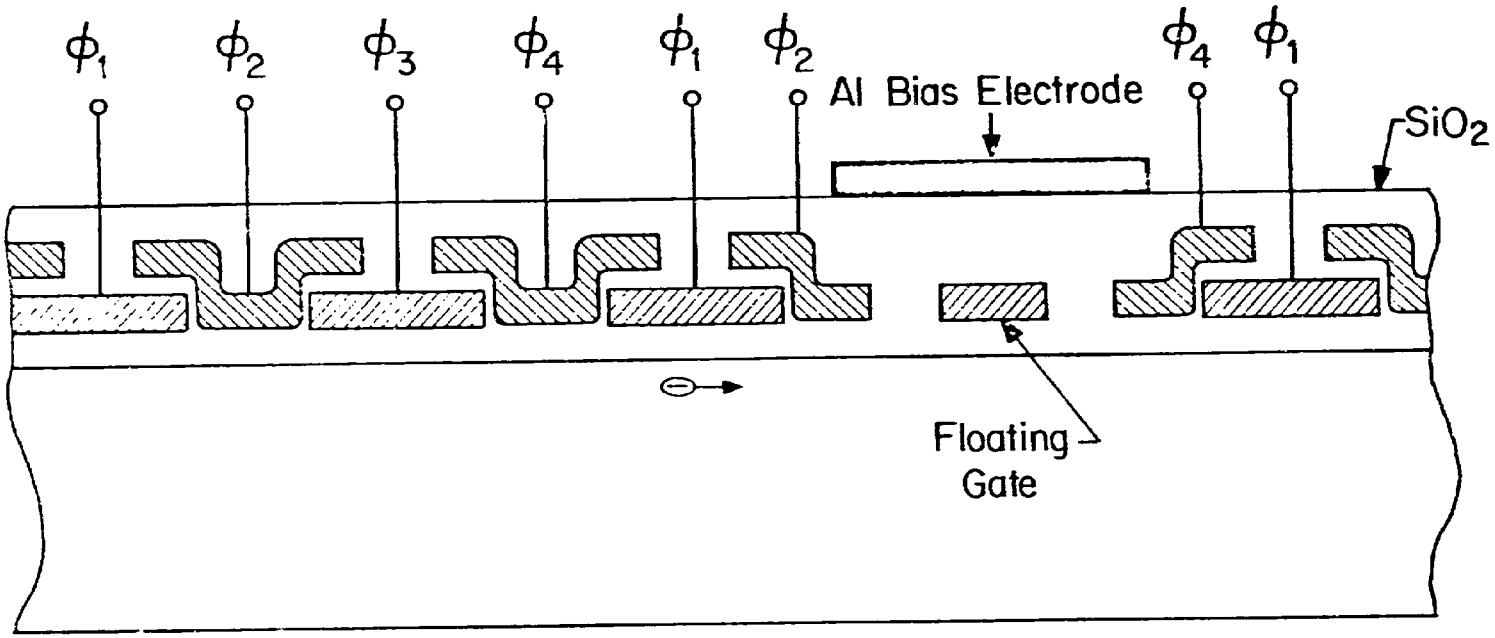


Figure 4.1.1 Cross-sectional View of the Input Register.

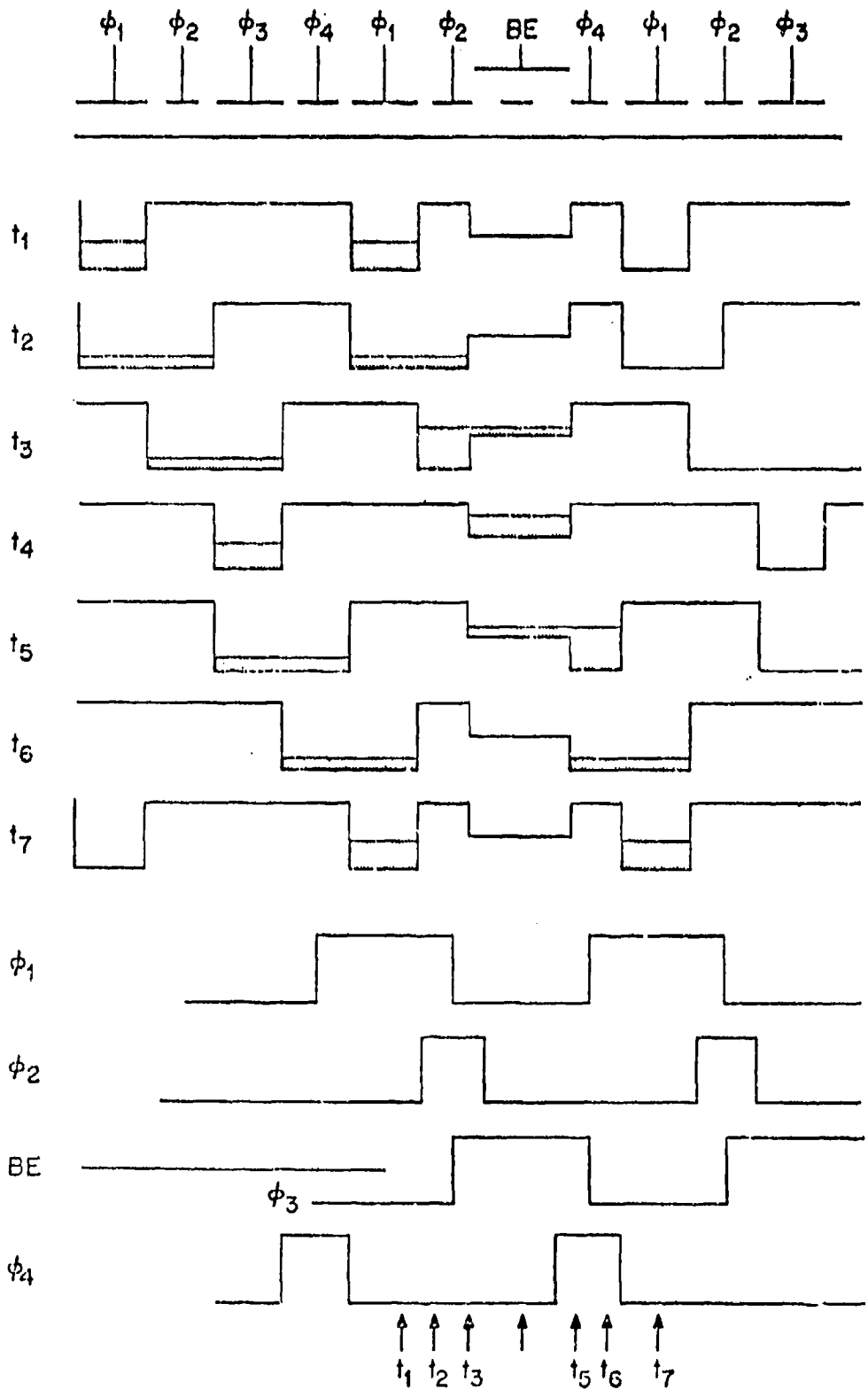


Figure 4.1.2 A Modified Four-Phase Clock.

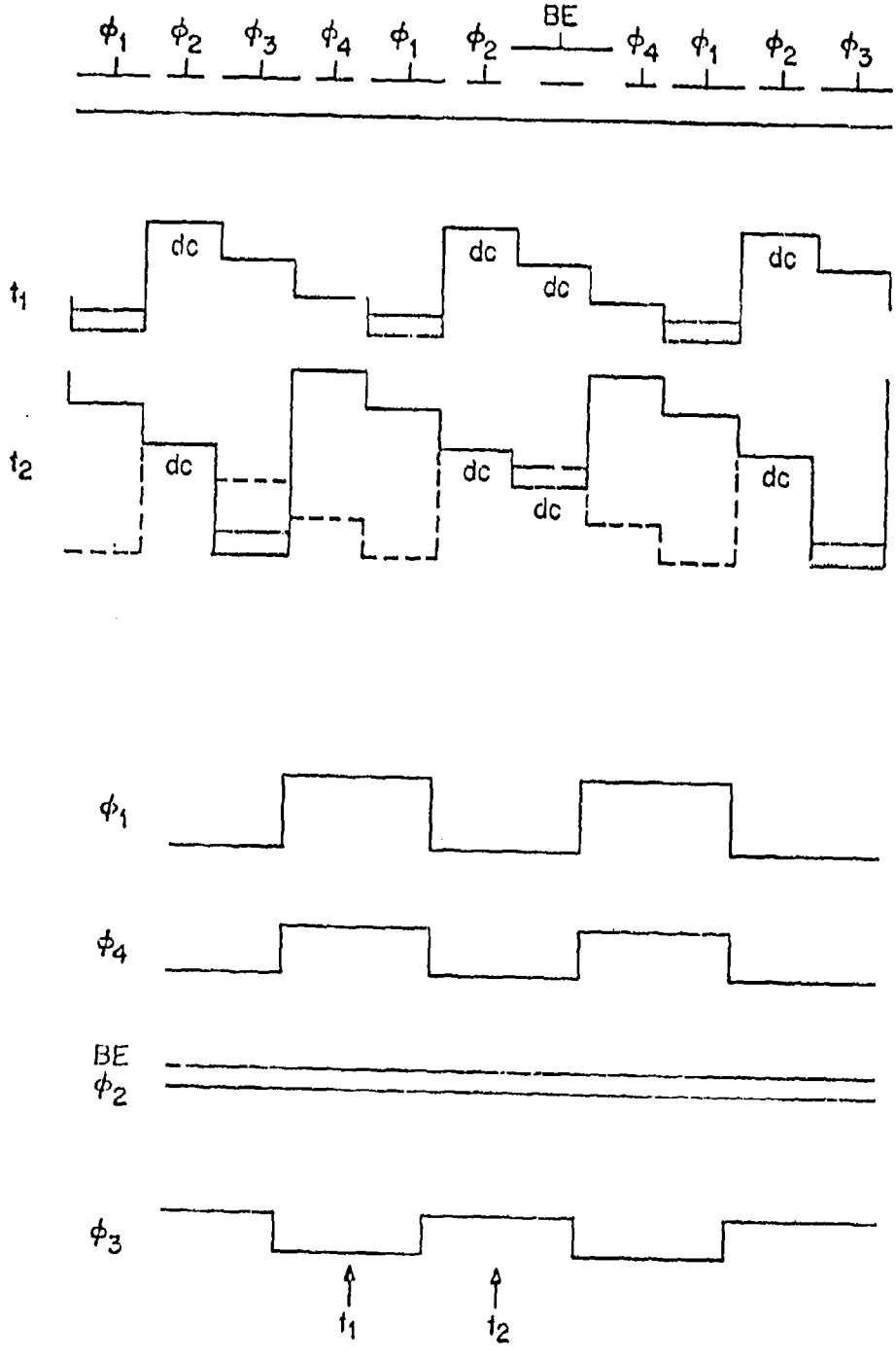


Figure 4.1.3. A 1-1/2 Phase Clocking

4-1(d)

BE are set at appropriate dc levels. Electrodes ϕ_1 and ϕ_4 are clocked in the same phase but with different amplitude. The signal charge packet can be seen to be under the floating gate approximately 40% of the cycle.

In the DFGA, the charge amplifiers are activated by turning "on" the control gate when the signal charge packet is under the floating gate, as described in Section 3.2. Since it will be seen that the signal-to-noise ratio of the DFGA is critically related to the control gate "on" time, the 1-1/2 clocking mode is preferred to the 4-phase mode.

4.2 DESIGN OF THE CHARGE AMPLIFIER

The layout of the DFGA stage is shown in Figure 4.2.1. It can be seen that the floating gate of the charge-amplifier couples the signal charge in the input register to the current flow into the output register. The basic operation of the charge amplifier was described in Section 3.1. The quantitative analysis of its design is given in this section.

The number of electrons, N_{bias}, injected into the output register when there is no signal charge in the input register is given by:

$$N_{bias} = I_D \, t_{on}/q \qquad (4.2.1)$$

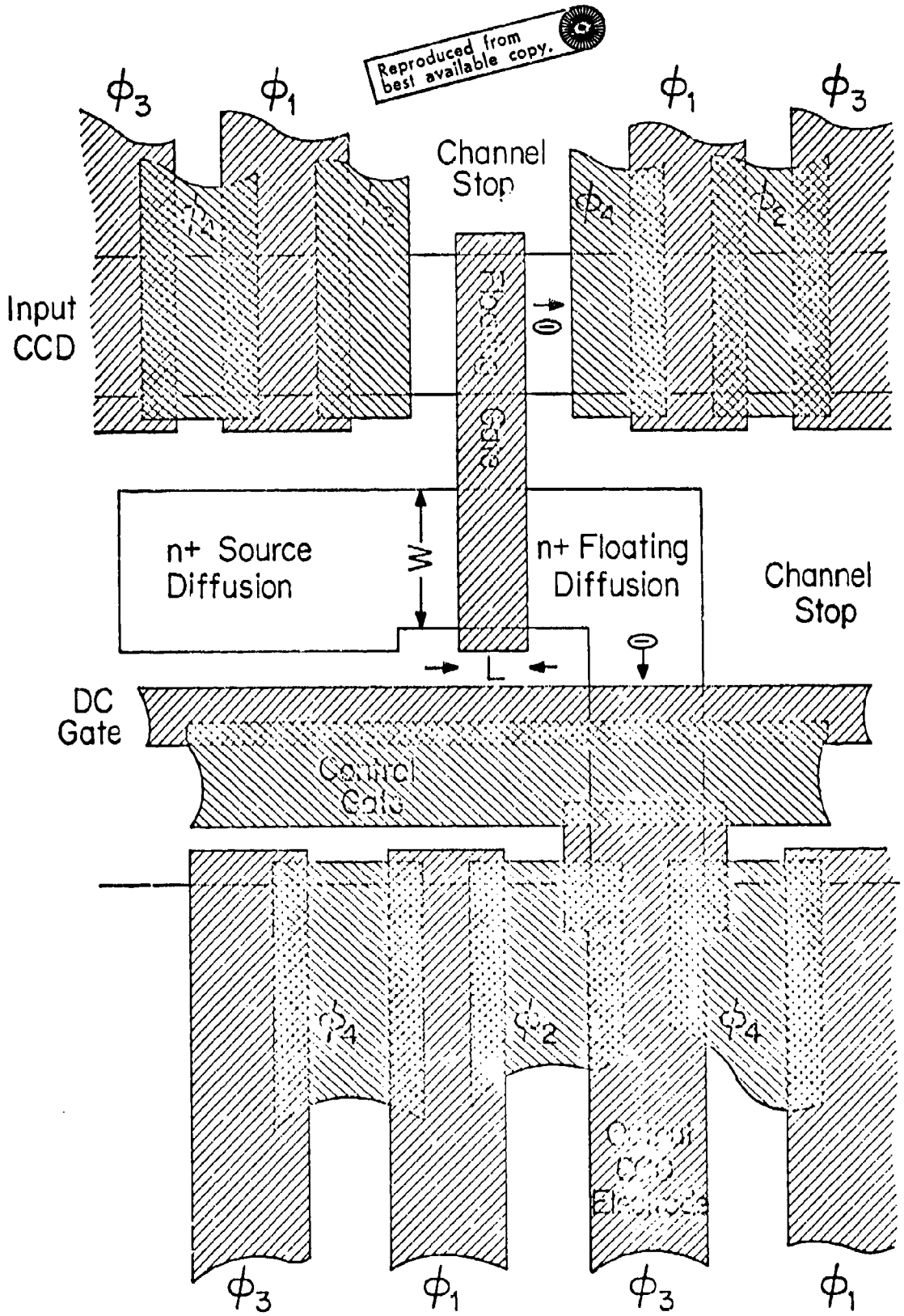


Figure 4.2.1 Layout of a Charge Amplifier in the DFGA.

4-2(a)

where i_D is the drain current of the floating-gate transistor, t_{on} is the control gate "on" time, and q is the electronic charge.

The presence of N_{in} signal electrons in the input register lowers the floating gate potential by:

$$\Delta V_{FG} = N_{in} R_{FG1} \qquad (4.2.2)$$

where R_{FG1} is the responsivity of the floating gate which is given by equation (2.3.3). The number of electrons injected into the output register is reduced by:

$$\Delta N_{out} = \Delta V_{FG} \, gm \, t_{on}/q \qquad (4.2.3)$$

where gm is the transconductance of the floating gate transistor at bias-current level I_D.

For a twelve-stage DFGA, the total output in terms of number of electrons in the output register is given:

$$\begin{aligned} N_S &= 12 \, \Delta N_{out} \\ &= 12 \, N_{in} \, R_{FG1} \, gm \, t_{on}/q \end{aligned} \qquad (4.2.4)$$

It will be shown in Section 5 that the shot noise in I_D is the dominant noise source of the DFGA. This shot noise can be given in terms of the number of electrons in the output register as:

$$(N_{shot}) = \left[\frac{12\, I_D \quad t_{on}}{q} \right]^{1/2} \qquad (4.2.5)$$

This equation assumes that N_{in} is small; I_D then remains approximately constant.

The signal-to-shot noise ratio is:

$$\frac{N_s}{(N_{shot})} = \frac{N_{in} \quad gm}{C_{FG1}} \qquad \left[\frac{12\, t_{on} \quad q}{I_D} \right]^{1/2} \qquad (4.2.6)$$

where:

$$C_{FG1} = \frac{q}{R_{FG1}}$$

It is clear that in order to maximize the signal-to-noise ratio of the DFGA, the charge amplifier should be designed for maximum $\frac{gm}{C_{FG1}\,(I_D)^{1/2}}$.

The floating gate capacitance, which was defined by equation (2.1.2), consists of five component capacitances. Among these five capacitances, only C_{in} depends on the geometry of the floating gate over the MOS channel:

$$C_{in} = K_1 WL \qquad (4.2.7)$$

where W and L are the width and length of the MOS channel, respectively, as indicated in Figure 4.2.1, and K_1 is a constant. The other components of C_{FG} depend only on the geometry of the CCD channel and are

governed by saturation charge considerations. Thus, the overall floating gate capacitance can by written as:

$$C_{FG1} = K_2 + K_3 WL \qquad (4.2.8)$$

where $K_3 = K1 \left(1 + \frac{C_3}{C1}\right)$ and K_2 includes all components that are independent of W and L.

The transistor current and transconductance are expected to be proportional to W/L:

$$I_D = K_4 \ W/L \qquad (4.2.9)$$

$$gm = K_5 \ W/L \qquad (4.2.10)$$

where K_4 and K_5 are constants.

By substituting equations (4.2.8), (4.2.9) and (4.2.10) into equation (4.2.6), it can be shown that the maximum signal-to-shot noise ratio occurs at:

$$WL = \frac{K_2}{K_3} \qquad (4.2.11)$$

From this analysis, the floating gates are designed to have:

$$W = 10 \ \mu m$$

and (4.2.12)

$$L = 5 \ \mu m$$

The resulting floating gate responsivity is expected to be 4 to 8 μV per electron dependent on process variations. Since present devices have been fabricated by a process that results in an R_{FG1} of 4 μV/el, this value is employed in subsequent discussions.

4.3 OPTIMAL BIAS CONSIDERATIONS

The signal-to-shot noise ratio of the charge amplifier was given in equation (4.2.6):

$$\frac{N_s}{(N_{shot})} = \frac{N_{in}\, gm}{C_{FG1}} \left[\frac{12\ t_{on}\ q}{I_D}\right]^{1/2} \qquad (4.2.6)$$

The optimal floating-gate geometry that maximizes this ratio was determined in Section 4.2. It can be seen that the signal-to-shot noise ratio also is a function of the bias current I_D. Since gm is also related to I_D, it is necessary to maximize the ratio $gm/(I_D)^{1/2}$ as a function of I_D. This is considered in three transistor operating regions as follows:

(A) Linear Region: $\quad V_G - V_T > V_D$

The transistor current in the linear region is given by:

$$I_D = \beta \left[(V_G - V_T)\, V_D - \frac{V_D^2}{2}\right] \qquad (4.3.1)$$

$$\beta = \frac{\mu\, C_{ox}\, W}{L} \qquad (4.3.2)$$

where V_G is the gate voltage, V_T is the threshold voltage, V_D is the drain voltage, μ is the electron mobility, C_{ox} is the gate capacitance, W and L are the width and length of the gate. The source is assumed to be at ground potential.

It can easily be shown:

$$\frac{gm}{(I_D)^{1/2}} = \left[\frac{\beta^{1/2} V_D}{(V_G - V_T) V_D - \frac{V_D}{2}^2} \right]^{1/2} \qquad (4.3.3)$$

(B) Saturation Region: $V_G - V_T < V_D$

In this region, a MOS transistor is characterized by:

$$I_D = \frac{\beta}{2} (V_G - V_T)^2 \qquad (4.3.4)$$

Therefore,

$$\frac{gm}{(I_D)^{1/2}} = (2\beta)^{1/2} \qquad (4.3.5)$$

(C) Subthreshold Region: $V_G - V_T \ll V_D$

In this region, the transistor is characterized by: (4.3.6)

$$I_D = \frac{W}{L} \mu C_{ox} \left(\frac{1}{m}\right) \left(\frac{n\ k\ T}{q}\right)^2 \exp\left[\frac{q}{mkT} (V_G - V_T - n\frac{kT}{q})\right] \left\{1 - \exp\left[\frac{-mq}{n\ k\ T} V_D\right]\right\}$$

where m and n are geometrical constants, k is the Boltzmann's constant and T is absolute temperature. It can be shown that:

$$\frac{gm}{(I_D)^{1/2}} = \frac{q}{n\ k\ T} (I_D)^{1/2} \qquad (4.3.7)$$

From the idealized transistor characteristic equations (4.3.3), (4.3.5) and (4.3.7), it may be seen that in order to maximize the $gm/(I_D)^{1/2}$ ratio, the transistor should be operated in the saturation region. In practice, however, equation 4.3.4 is valid only for a small range of I_D near the knee of the IV curve. In order to minimize the geometry of the output CCD register, which has to be large enough to store the injected charge, the charge amplifiers should be operated at the lowest current level in the saturation region. A transistor characteristic curve has been measured and the $gm/(I_D)^{1/2}$ ratio has been calculated; both are plotted as a function of the floating-gate voltage in Figure 4.3.1. The maximum $gm/(I_D)^{1/2}$ occurs at $I_D = 1\mu A$.

4.4 DESIGN OF THE OUTPUT REGISTER

Since the basic structure of the output register is similar to that of the input register, the analysis will not be repeated. One design consideration unique to the output register is its size. As indicated in Section 4.3, each of the twelve charge amplifiers is biased at $I_D = 1\mu A$ for maximum signal-to-shot noise ratio. The output register must have a charge

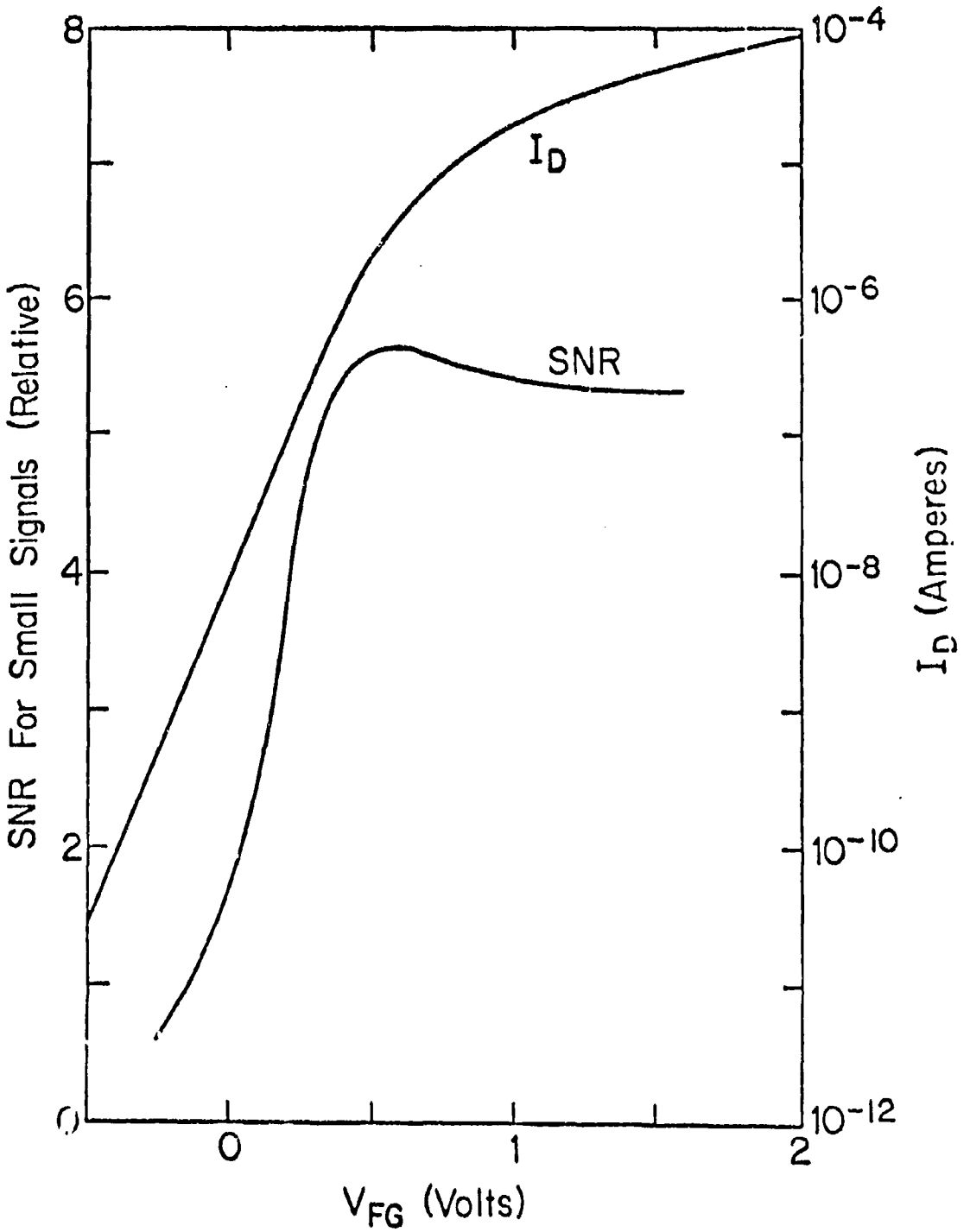


Figure 4.3.1. The Dependence of Drain Current and Signal-to-Noise Ratio on the Voltage of the Floating Gate in the DFGA

handling capability higher than

$$Q_{bias} = 12\, I_D\, t_{on} \qquad (4.4.1)$$

where $I_D = 1\mu A$.

Since the output register is designed to be 250 μm wide, it should be able to handle Q_{bias} for control gate "on" times t_{on} less than 0.13 μsec. For larger t_{on}, the bias current I_D must be reduced in order not to saturate the output register. The signal-to-shot noise ratio is expected to remain close to its value at $t_{on} = 0.13$ μsec and $I_D = 1\mu A$.

Because of the large geometry of the output register, the output single-stage FGA has a sensitivity of:

$$R_{FG2} = 0.34\ \mu V/\text{electron} \qquad (4.4.2)$$

For typical operation, the output FGA is biased as a source follower similar to that shown in Figure 2.1.3.

4.5 THE DFGA TRANSFER CHARACTERISTICS

The basic transistor characteristic curve of a charge amplifier is shown in Figure 4.3.1. When there is no signal charge in the input register, a bias current of $I_D = 1\mu A$ flows into the output register. The transconductance gm at this bias level is:

$$gm \Big|_{I_D = 1\mu A} = 1.0 \times 10^{-5} \quad \text{(amp/volt)} \qquad (4.5.1)$$

If there are N_{in} signal electrons in the input register, the corresponding signal electrons in the output register is given by equation (4.2.4) as:

$$N_s = 12\ N_{in}\ R_{FG1}\ gm\ t_{on}/q \qquad (4.2.4)$$

The final DFGA output voltage from the output FGA is:

$$V_s = 0.17 N_s\ R_{FG2}\ (\mu V) \qquad (4.5.2)$$

where R_{FG2} is the responsivity of the output FGA as given in equation (4.4.2). The factor 0.17 is the expected source-follower gain of the output FGA. By substituting equations (4.5.1), (4.2.4) and (4.4.2) into (4.5.2), the DFGA output for N_{in} signal electrons in the input register is given by:

$$V_s = 170\ N_{in}\ t_{on}\ \text{(volts)} \qquad (4.5.3)$$

where t_{on} is the control-gate "on" time in seconds and R_{FG1} is 4μV/el.

For larger signal charge packets in the input register, the bias current I_D is reduced from 1μA. Since the transconductance gm is smaller, the DFGA output swing is gradually reduced. Using Figure 4.3.1 a DFGA transfer characteristic curve can be generated as shown in Figure 4.5.1 for t_{on} of 25 and 50 nseconds.

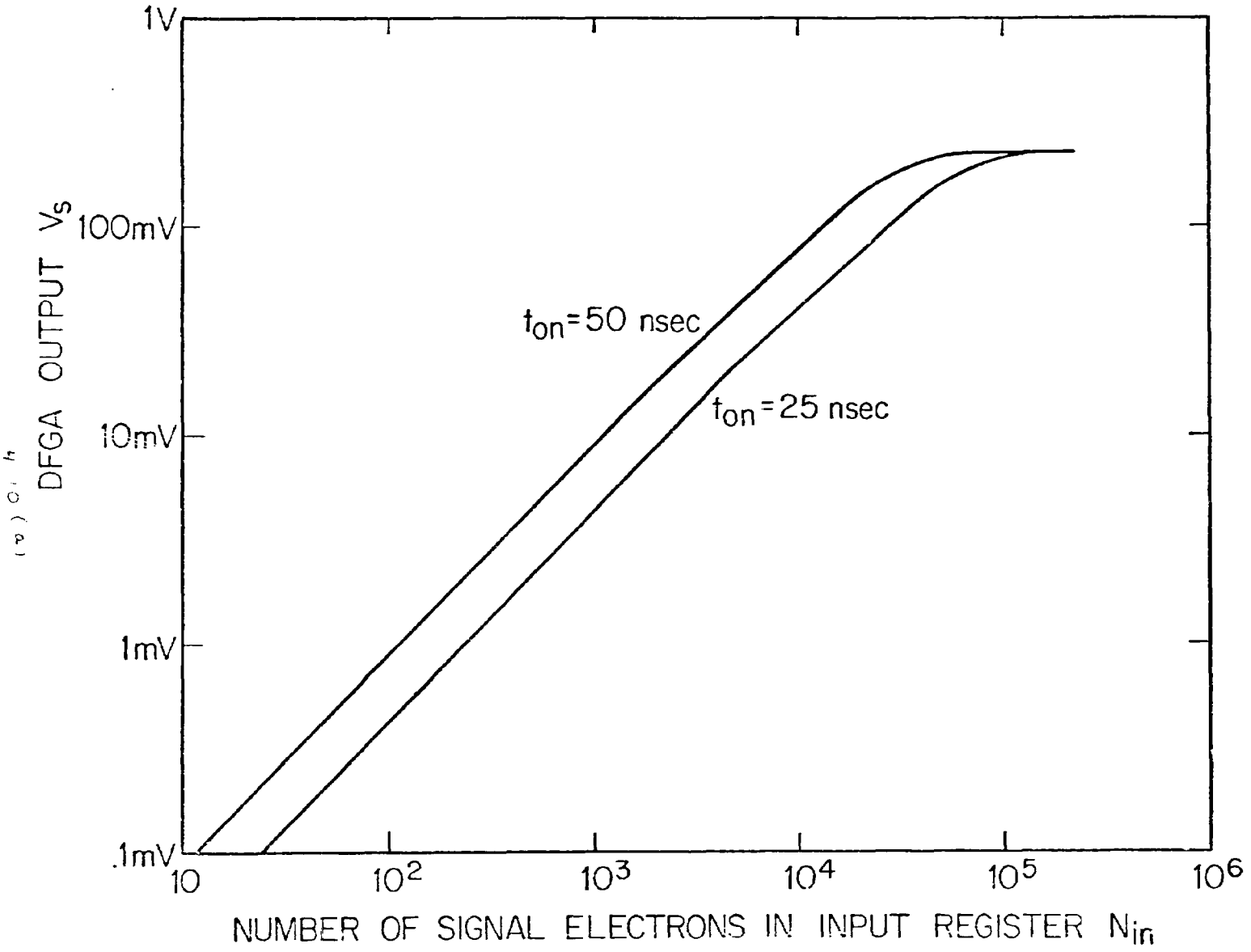


Figure 4.5.1. Theoretical DFGA Transfer Characteristic Curves

The DFGA output V_s in equation (4.5.3) was derived in terms of the control gate "on" time. Since the control gate is turned on only when the signal charge packet in the input CCD register is under the floating-gate, the control gate "on" time t_{on} is limited by the mode and frequency of the clocks. For the modified four phase clock shown in Figure 4.1.2, the clock frequency f is related to t_{on} by:

$$f \leq \frac{0.2}{t_{on}} \tag{4.5.4}$$

For the 1-1/2 clocking mode shown in Figure 4.1.3, this relationship is:

$$f \leq \frac{0.4}{t_{on}} \tag{4.5.5}$$

The maximum frequency f_{max} for a given control gate "on" time t_{on} is therefore:

$$f_{max} = \frac{0.2}{t_{on}} \quad \text{for a modified 4-phase clock;} \tag{4.5.6}$$

$$f_{max} = \frac{0.4}{t_{on}} \quad \text{for a 1-1/2 phase clock} \tag{4.5.7}$$

Using these relations, equation (4.5.3) can be written in terms of f_{max}: (4.5.8)

$$V_s = 34\, N_{in}\, (f_{max})^{-1} \text{ (volts) for the modified 4-phase clock;}$$

$$V_s = 68\, N_{in}\, (f_{max})^{-1} \text{ (volt) for a 1-1/2 phase clock} \quad (4.5.9)$$

for a clock frequency f where:

$$f \leq f_{max} \quad (4.5.10)$$

SECTION 5

NOISE ANALYSIS OF THE DFGA

The noise sources in the DFGA structure are identified in Figure 5.1. Because of the large charge gain of the charge amplifiers, the noise sources in the output CCD channel and the output FGA are expected to be negligible when they are compared with those generated before or in the charge amplifiers. In particular, the shot noise associated with the bias current I_D in the charge amplifiers will be shown to be the dominant noise source. The important noise sources are discussed separately in this section. The 1-1/2 phase clocking is assumed in this section so that the control gate "on" time t_{on} can be related to the maximum clock frequency f_{max} as:

$$t_{on} = \frac{0.4}{f_{max}} \tag{5.1}$$

R_{FG1} = 4 uV/el as discussed previously.

5.1 SHOT NOISE IN THE CHARGE AMPLIFIER

As described in Section 4.2, a small electron current I_D flows into the output register when the control gate is pulsed "on". The shot noise associated with this current flow is given in equation (4.2.5) as (N_{shot}) electrons in the output register:

$$(N_{shot}) = \left[\frac{12\ I_D\ t_{on}}{q}\right]^{1/2} \tag{4.2.5}$$

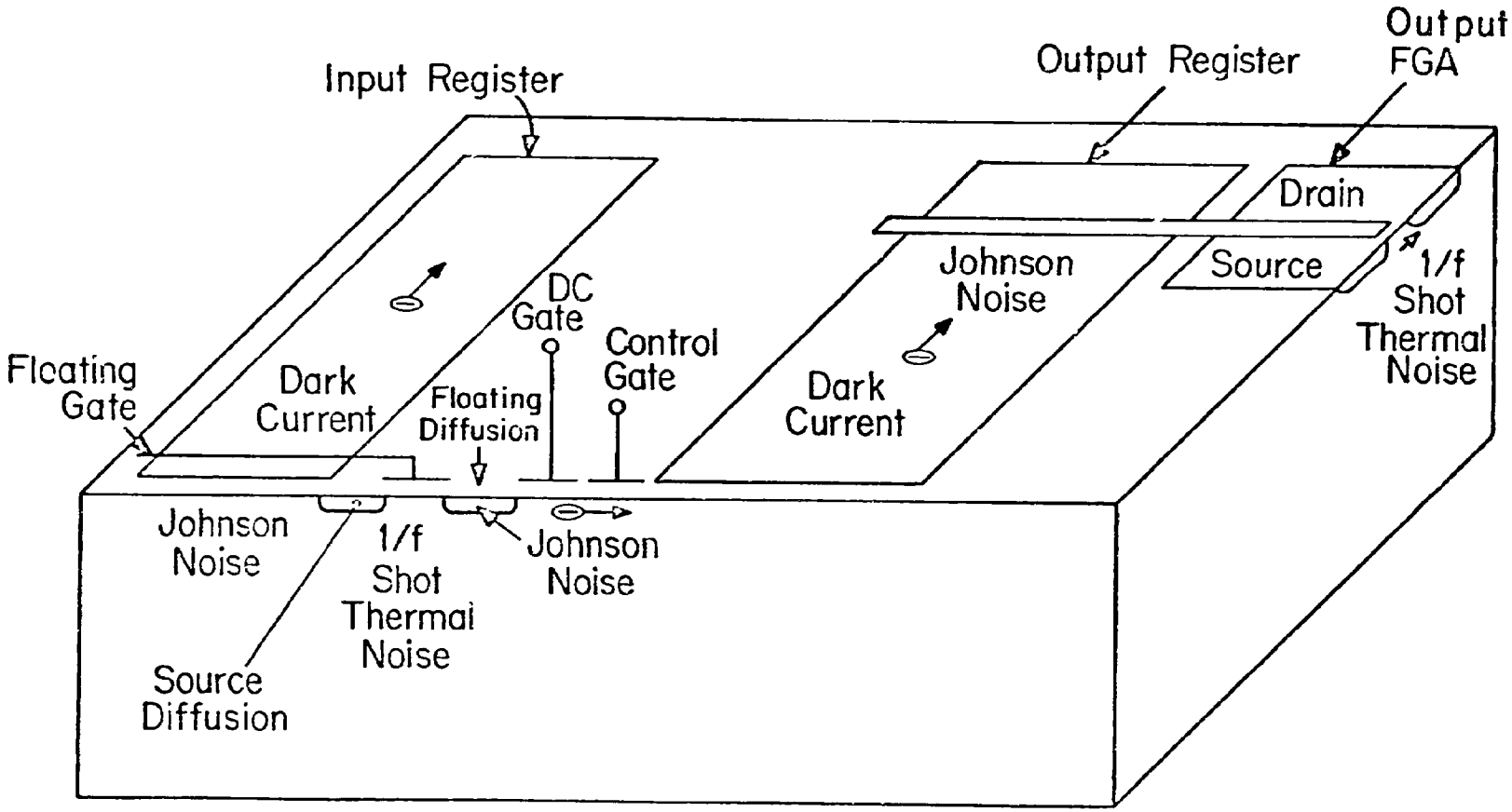


Figure 5.1. Noise Sources in the DFGA

With the assumption of 0.34 μV/electron sensitivity of the output FGA and the 0.17 source follower gain from equation (4.5.2), the resulting shot noise in a final DFGA output is:

$$(V_{shot}) = (0.17)\ (0.34)\ (N_{shot})\ (\mu V) \qquad (5.1.1)$$

Using equation (5.1) to express t_{on} in terms of the maximum clock frequency f_{max}, equation (5.1.1) can be written:

$$(V_{shot}) = (0.17)\ (0.34)\left[\frac{12\ I_D\ 0.4}{q f_{max}}\right]^{1/2} \quad (\mu V) \qquad (5.1.2)$$

For small signal charge levels, I_D is approximately 1μA. Equation (5.1.2) can be computed to be:

$$(V_{shot}) = 0.318\ (f_{max})^{-1/2} \quad \text{(volts)} \qquad (5.1.3)$$

for clock frequencies less than or equal to f_{max}.

5.2 JOHNSON NOISE IN THE CCD CHANNEL

A cross-sectional view of a charge amplifier stage in the DFGA is illustrated in Figure 5.2.1. In this figure, C_5 is the capacitance between the floating gate and the MOST channel; R is the bulk resistance between the edge of the depletion region to ground; C_1, C_2, C_3 and C_4 are similar to those defined in Section 2.1. Since an electron current flows under the MOST side of the floating gate when the charge amplifier is activated, the MOST channel is ac shorted to ground by the dc source shown in Figure 3.1.2. The small signal equivalent circuit of the charge amplifier is shown in Figure 5.2.2, where:

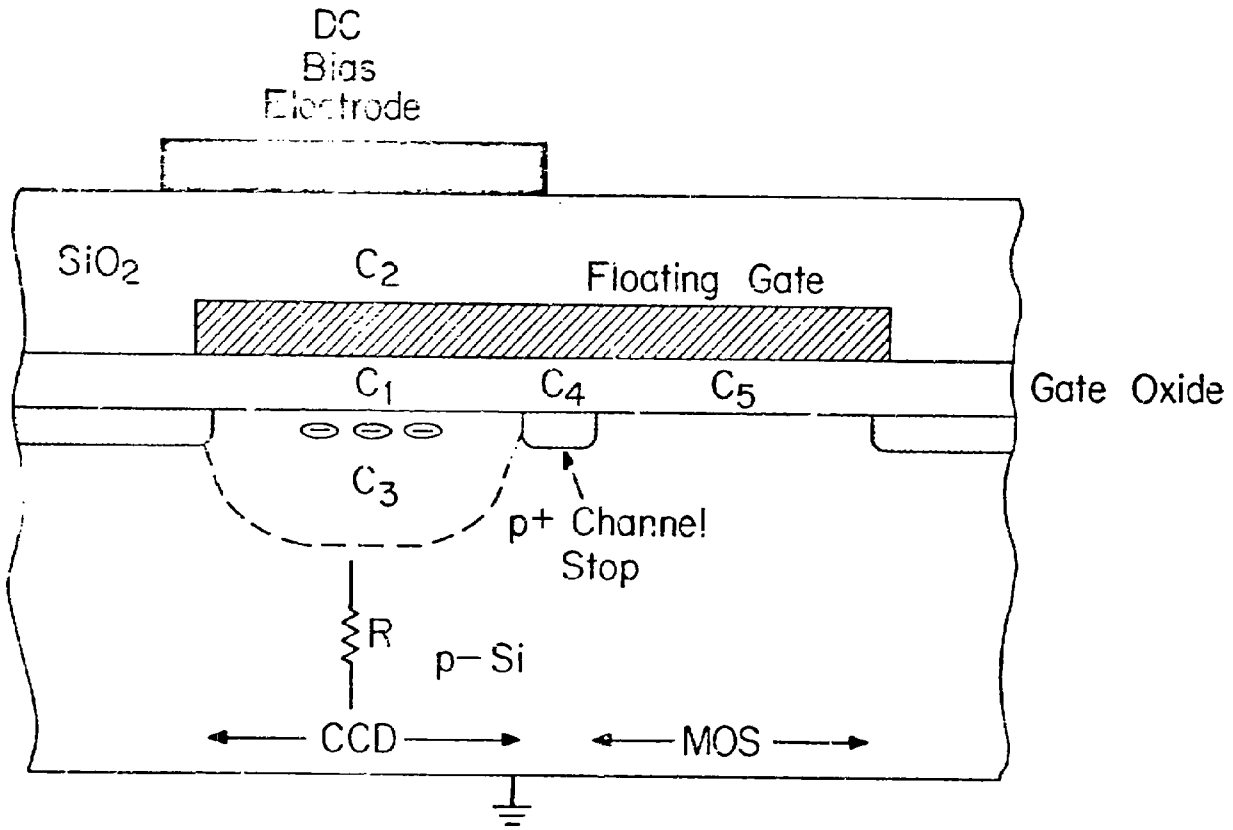


Figure 5.2.1. Cross-sectional View of a Charge Amplifier Showing the Bulk Resistance R

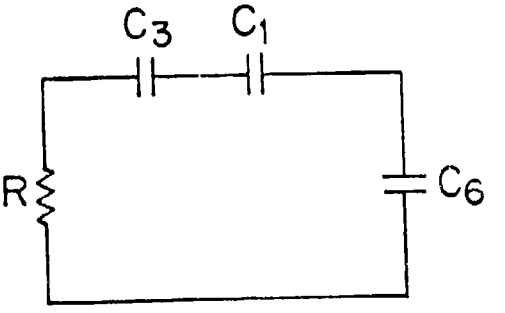


Figure 5.2.2 Small signal equivalent circuit of Figure 5.2.1 where C_6 is the parallel combination of C_2, C_4 and C_5.

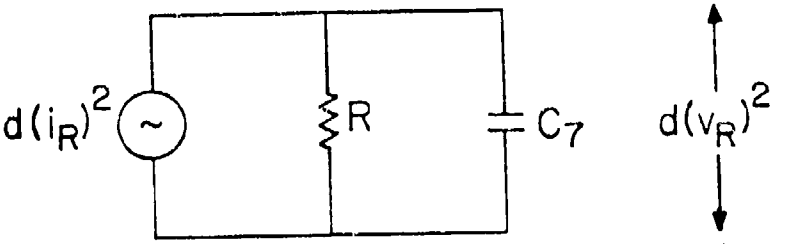


Figure 5.2.3 Equivalent circuit of Figure 5.2.2 showing the Johnson noise, $d(i_R)^2$, generated by R. C_7 is the series combination of C_3, C_1 and C_6.

$$C_6 = C_2 + C_4 + C_5 \tag{5.2.1}$$

The Johnson noise in the resistor R at absolute temperature T in a frequency interval $d\omega$ is given by:

$$d(i_R)^2 = \frac{2kT}{\pi R} \, d\omega \tag{5.2.2}$$

where k is Boltzmann's constant. The equivalent circuit including $d(i_R)^2$ is shown in Figure 5.2.3. Here, C_7 is the series combination of C_1, C_3 and C_6:

$$C_7 = \frac{C_1 C_3 C_6}{C_1C_3 + C_3C_6 + C_1C_6} \tag{5.2.3}$$

The noise voltage developed across the resistor R is given by:

$$d(v_R)^2 = \frac{R^2}{1 + \omega^2 R^2 C_7^2} \, d(i_R)^2 \tag{5.2.4}$$

Integration of equation (5.2.4) from $\omega = 0$ to $\omega = \infty$ yields the following total noise voltage $(v_R)^2$ across R:

$$(v_R)^2 = \frac{kT}{C_7}$$

or

$$(v_R) = \left(\frac{kT}{C_7} \right)^{1/2} \tag{5.2.5}$$

The noise voltage $(v_{FG})^2$ developed between the floating gate and ground is:

$$(v_{FG}) = (v_R) \frac{C_8}{C_6 + C_8} \tag{5.2.6}$$

where C_8 is the series combination of C_1 and C_3, i.e.,

$$C_8 = \frac{C_1 C_3}{C_1 + C_3} \tag{5.2.7}$$

as shown in Figure 5.2.4.

Using the capacitance values, which result in an R_{FG1} of 4 μV per electron as discussed in Section 4.2, the rms fluctuation (v_{FG}) in the floating-gate potential can be computed from equation (5.2.6) to be:

$$(v_{FG}) = 65 \ (\mu V) \tag{5.2.8}$$

The resulting noise $(v_{Johnson})$ in the DFGA output is then (v_{FG}) amplified by the gain of the DFGA:

$$(v_{Johnson}) = \frac{(v_{FG})}{R_{FG1}} \frac{1}{\sqrt{12}} \frac{V_s}{N_{in}} \tag{5.2.9}$$

where V_s/N_{in} is given in equation (4.5.9). Substitution of equations (4.5.9), (5.2.8) and R_{FG1} = 4 μV per electron into equation (5.2.9) gives the Johnson noise appearing at the DFGA output:

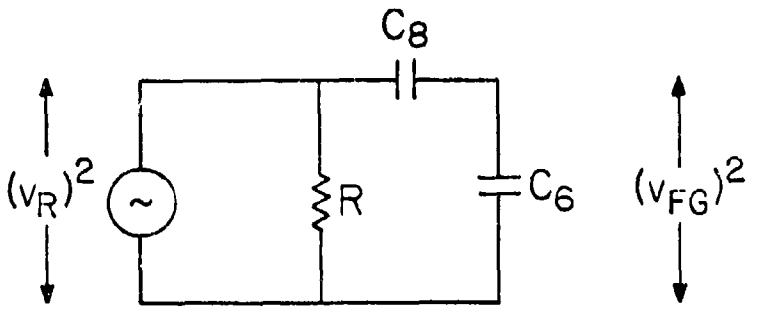


Figure 5.2.4 Equivalent circuit of Figure 5.2.3 showing the noise $(v_{FG})^2$ appearing in the floating gate. C_8 is the series combination of C_3 and C_1.

$$(v_{Johnson}) = 315\ (f_{max})^{-1}\ \text{(volt)} \qquad (5.2.10)$$

for clock frequencies less than or equal to f_{max}.

5.3 FIXED CHARGE NOISE IN THE CHARGE AMPLIFIER

The operation of the charge amplifier is illustrated in Figure 5.3.1. When the control gate is turned "off", the potential under the dc gate and in the floating diffusion area come to equilibrium with that of the source bias. When the control gate is turned "on", a fixed amount of charge, as indicated by A in Figure 5.3.1, flows into the output register before the desired bias condition can be established. The shot noise associated with this charge injection results in a noise at the final DFGA output:

$$(V_{fixed}) = (0.17)\ (0.34)\ (12C\ V/q)^{1/2}\ (\mu V) \qquad (5.3.1)$$

where C is the total capacitance of the dc gate and the floating diffusion, and V is approximately 2 volts. By substitution of proper values in equation (5.3.1), the resulting noise voltage in the final output is:

$$(V_{fixed}) = 70\ (\mu V). \qquad (5.3.2)$$

5.4 INPUT REGISTER DARK CURRENT NOISE

While the signal charge packet is transferred along the input register, thermally generated dark current is constantly added to it. The rms

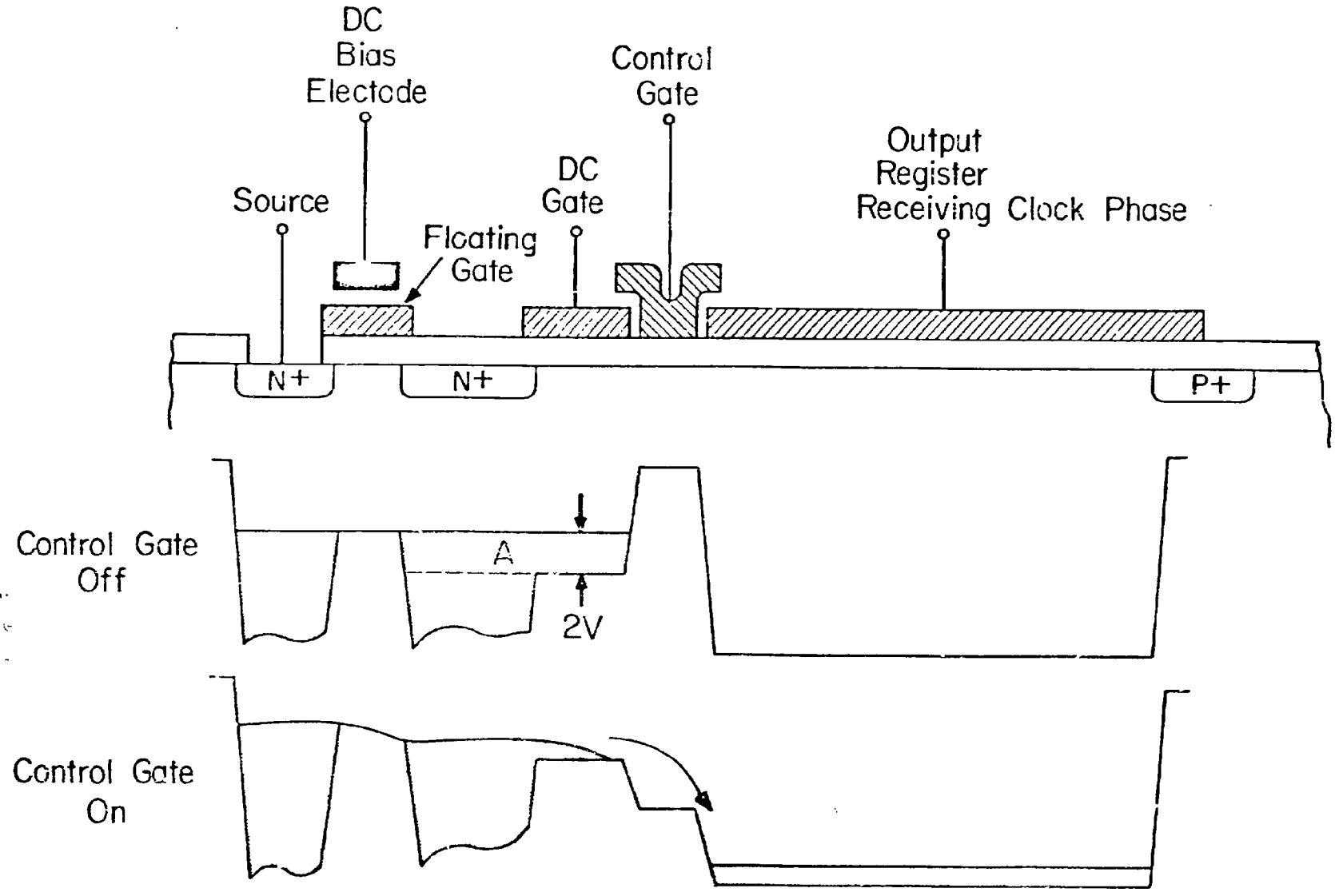


Figure 5.3.1. Cross-sectional View of the Charge Amplifier Showing the Origin of Two Noise Sources

fluctuation of the added dark charge must be considered a noise source inherent to the DFGA. Since charge amplifiers are positioned at every other cell in the DFGA, the dark charge q_{dark} added to a signal charge packet between two adjacent charge amplifiers is:

$$q_{dark} = 2 \; I_{dark} A/f \qquad (5.4.1)$$

where I_{dark} is the dark-current density, A is the cell area of the input register and f is the clock frequency in Hz. If q_{dark} is the dark charge that has been added to the signal packet when it reaches the first charge amplifier, the rms fluctuation caused in the signal packet is (m) electrons, where:

$$(m) = (q_{dark}/q)^{1/2} \qquad (5.4.2)$$

Because this noise is amplified by all twelve stages of the DFGA, the resulting noise in the final output is:

$$(V_1) = 170 \; (m) \; t_{on} \; \text{(volt)} \qquad (5.4.3)$$

where the gain factor was obtained from equation (4.5.3) and t_{on} is the control gate "on" time in seconds.

The dark charge added to the signal packet between the k^{th} and $k+1^{st}$ charge amplifier is also q_{dark}. The DFGA gain factor for this dark

charge is different because it is amplified by 12-k stages. The resulting noise voltage in the final output is:

$$(V_{k+1}) = 170\ (m)\ t_{on} \left\{ \frac{12-k}{12} \right. \quad \text{(volt)} \qquad (5.4.4)$$

The sum of all the dark-charge noise in the output is:

$$(V_{dark})^2 = \sum_{k=0}^{11} (V_{k+1})^2 \qquad (5.4.5)$$

When a dark current density of 10 nA/cm^2 is assumed and equations (5.4.1), (5.4.2), (5.4.4) and (5.4.5) are combined, the total dark-current noise at the output is:

$$(V_{dark}) = 1.26 \times 10^5 \ (f)^{-1/2} \ (f_{max})^{-1} \quad \text{(volt)} \qquad (5.4.6)$$

for clock frequency f less than or equal to f_{max}.

5.5 SUMMARY OF NOISE ANALYSIS

The predicted noise performance of the DFGA is summarized in this section. As discussed earlier, for a control gate "on" time of "t_{on}" second, the maximum frequency is:

$$f_{max} \qquad \frac{0.4}{t_{on}} \qquad (4.5.7)$$

for the 1-1/2 phase clocking mode shown in Figure 4.1.3. The clock frequency f that is employed must satisfy f < f_{max}.

The predicted noise values at room temperature are as follows:

Shot noise in charge amplifier:

$$(V_{shot}) = 318 \ (f_{max})^{-1/2} \quad \text{(volt)}$$

Johnson noise in CCD channel:

$$(V_{Johnson}) = 315 \ (f_{max})^{-1} \quad \text{(volt)}$$

Shot noise of fixed charge in charge amplifier:

$$(V_{fixed}) = 70 \ (\mu V)$$

Input register dark current noise:

$$(V_{dark}) = 1.26 \times 10^{5} \ (f)^{-1/2} \ (f_{max})^{-1} \quad \text{(volt)}$$

The overall DFGA noise is the rms sum of all the noise components:

$$(V_{noise})^2 \simeq (V_{shot})^2 + (V_{Johnson})^2 + (V_{fixed})^2 + (V_{dark})^2 \qquad (5.5.1)$$

The signal output for N_{in} electrons in the input channel is given by the equation (4.5.4):

$$V_s = N_{in} \ 68 \ (f_{max})^{-1} \quad \text{(volt)} \qquad (4.5.4)$$

The signal and noise outputs for various t_{on} values are tabulated in Table 5.5.1.

It is seen that V_s, (V_{shot}) and ($V_{Johnson}$) are related to f_{max}, i.e., the control gate "on" time. The dark current noise (V_{dark}) depends on both f_{max} and the clock frequency f employed. Frequency f is assumed to be 1 MHz in the (V_{dark}) calculation. Since (V_{fixed}) is a constant, it becomes increasingly important at higher frequencies as expected.

TABLE 5.5.1

PREDICTED DFGA NOISE PERFORMANCE

t_{on}	f_{max}	V_s/N_{in}	(V_{shot})	$(V_{Johnson})$	(V_{fixed})	(V_{dark})	(V_{noise})	NES
100 nsec	4 MHz	17.0 μV/el.	159 μV	79 μV	70 μV	31 μV	194 μV	11 el.
75 nsec	6 MHz	11.3 μV/el.	130 μV	57 μV	70 μV	21 μV	163 μV	14 el.
50 nsec	8 MHz	8.5 μV/el.	113 μV	40 μV	70 μV	16 μV	146 μV	17 el.
25 nsec	16 MHz	4.2 μV/el.	79 μV	20 μV	70 μV	8 μV	113 μV	27 el.

NOTES: Temperature = 25°C

Clock frequency $f \leq f_{max}$

(V_{dark}) calculated for f = 1 MHz

1-1/2 phase clock is assumed so that $f_{max} = \frac{0.4}{t_{on}}$

Charge amplifiers are biased at I_D = 1 μA.

$NES = \frac{(V_{noise})}{V_s/N_{in}}$

SECTION 6

EVALUATION OF A 12-STAGE DFGA

6.1 PRELIMINARY CHARACTERIZATION

In the 12-stage DFGA test structure two single-stage DFGA's are incorporated in the input register as shown in Figure 6.1.1. Because these SSFGA's have the same geometry as the floating gates in the charge amplifiers, they provide useful information on the basic properties of the DFGA, e.g., the floating gate responsivity. Transfer efficiency through the DFCA input channel can be determined by comparing the outputs of the two SSFGA's. SSFGA2 is positioned in such a way that its output is synchronous in time with the DFGA output. For signal levels that are higher than the DFGA saturation level, although lower than the saturation level of the input register, the output can be read without loss of information by switching from the DFGA output to the SSFGA2 output.

Figure 6.1.2 shows the outputs of the two SSFGA's when a signal charge packet is electrically injected into the input register. It is seen that high charge transfer efficiency through the DFGA input channel is obtained. The responsivity of the SSFGA was measured with the circuits illustrated in Figure 6.1.3. In this experiment, charge packets were electrically injected into the input register during every clock cycle. The number of electrons, N_{in}, in each packet was determined by measuring the average

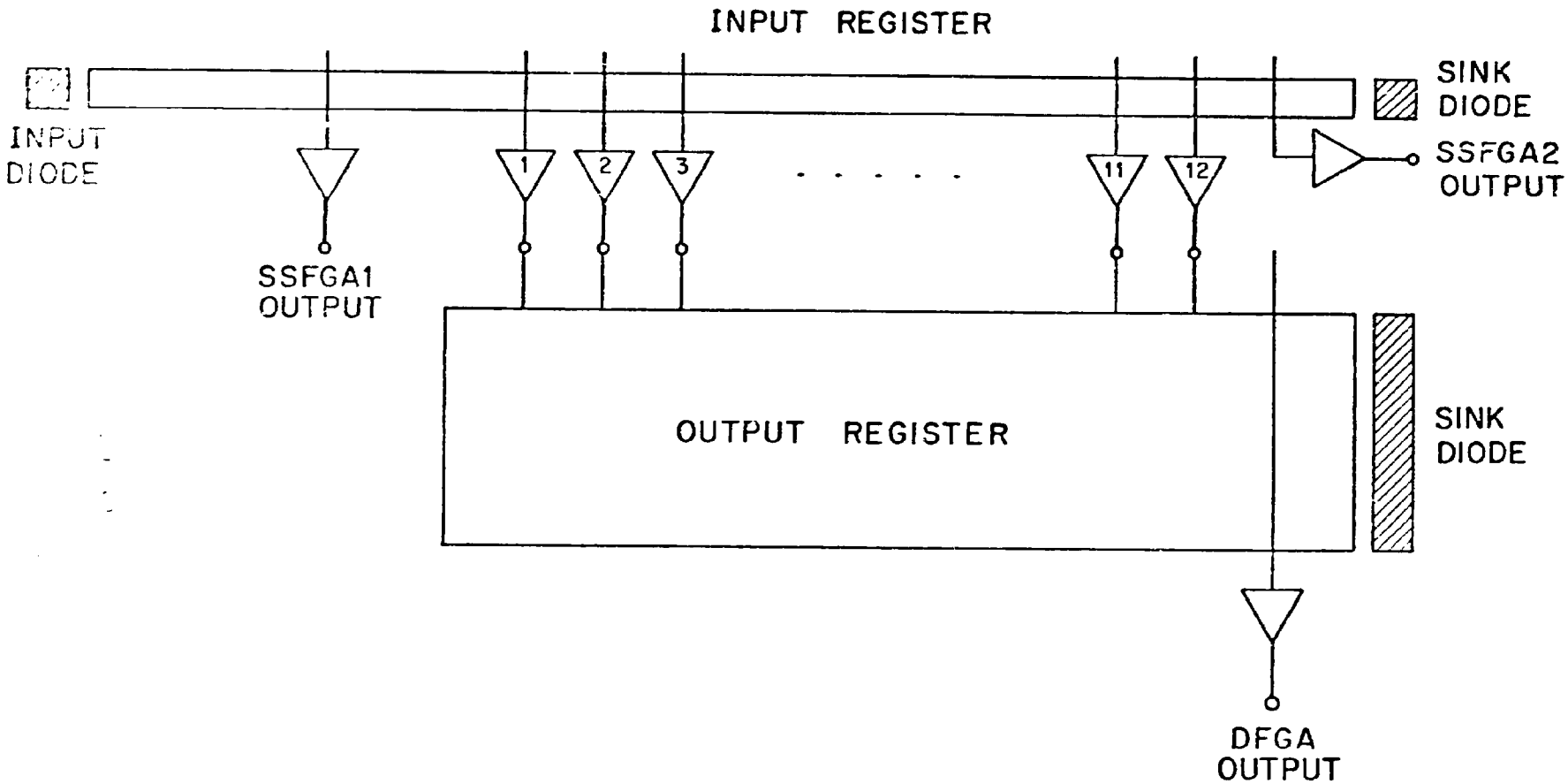


Figure 6.1.1 Layout of the 12-Stage DFGA Showing the Location of the Two SSFGA's

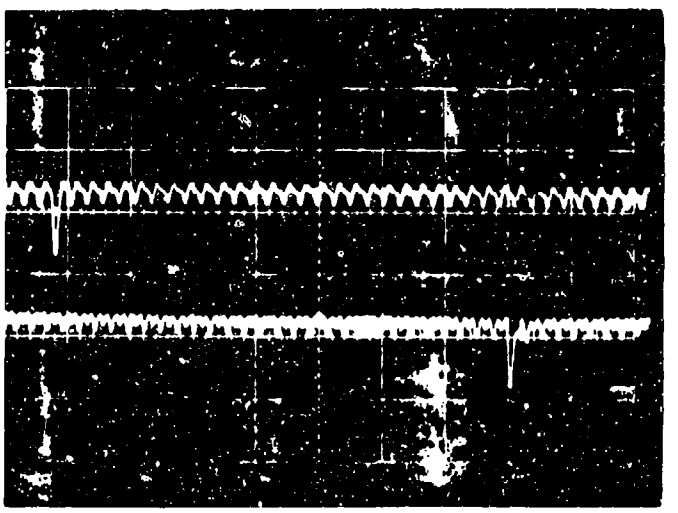


Figure 6.1.2 Outputs from SSFGA1 (top trace) and SSFGA2 (bottom trace) show High Transfer Efficiency through the DFGA Input Register.

Vertical Scale: .1V/cm

Horizontal Scale: 2μsec/cm

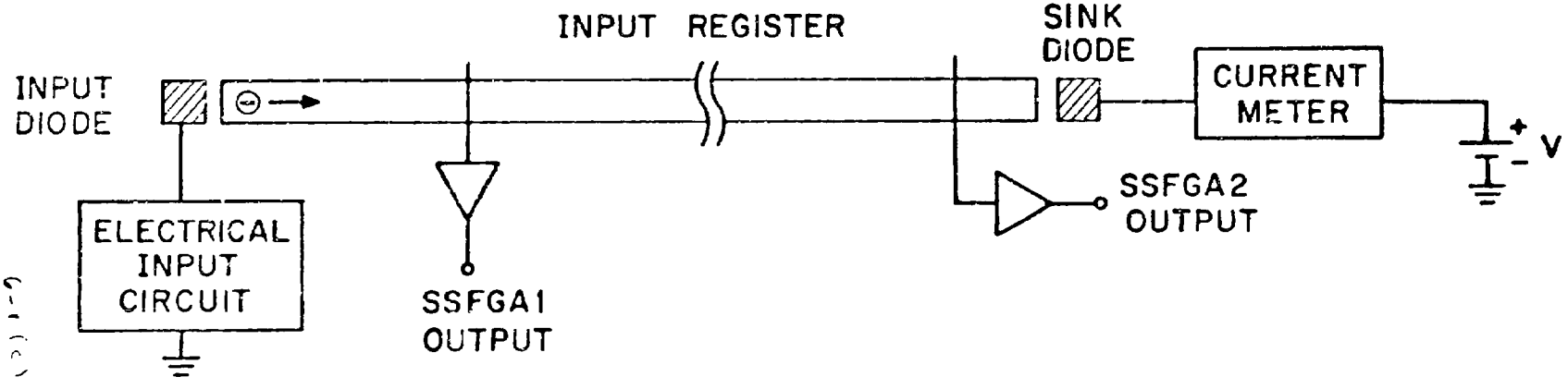


Figure 6.1.3 Circuit Schematic for Measuring the Responsivity of the SSFGA's.

electron current that flowed from the sink diode at the end of the input register. The results of this measurement are plotted in Figure 6.1.4. The input register is seen to saturate in 2×10^5 electrons. A floating-gate responsivity of approximately 3.0 μV per electron was obtained. Theoretically predicted values for this device are also plotted in the figure for comparison. The predicted floating-gate responsivity for this device was computed to be 4.0 μV per electron. Since the geometry of the floating gates in the DFGA charge amplifiers is the same as that of the SSFGA's, they too are expected to have responsivity of 3.0 μV per electron.

The floating-gate responsivity R_{FG2} of the output FGA of the DFGA can be measured in a similar manner. The charge packets in the output register, however, were obtained from the charge amplifiers. A responsivity of 0.30 μV per electron was obtained; the theoretical value is 0.34 μV per electron.

6.2 DFGA CHARACTERIZATION

Figure 6.2.1 shows the SSFGA1 and DFGA outputs when an electrically injected signal charge packet is clocked through the input channel. The basic charge inverting characteristic of the DFGA is illustrated. It may also be seen that time synchronism between these two outputs is obtained as designed. No quantitative conclusion on the responsivity of the DFGA

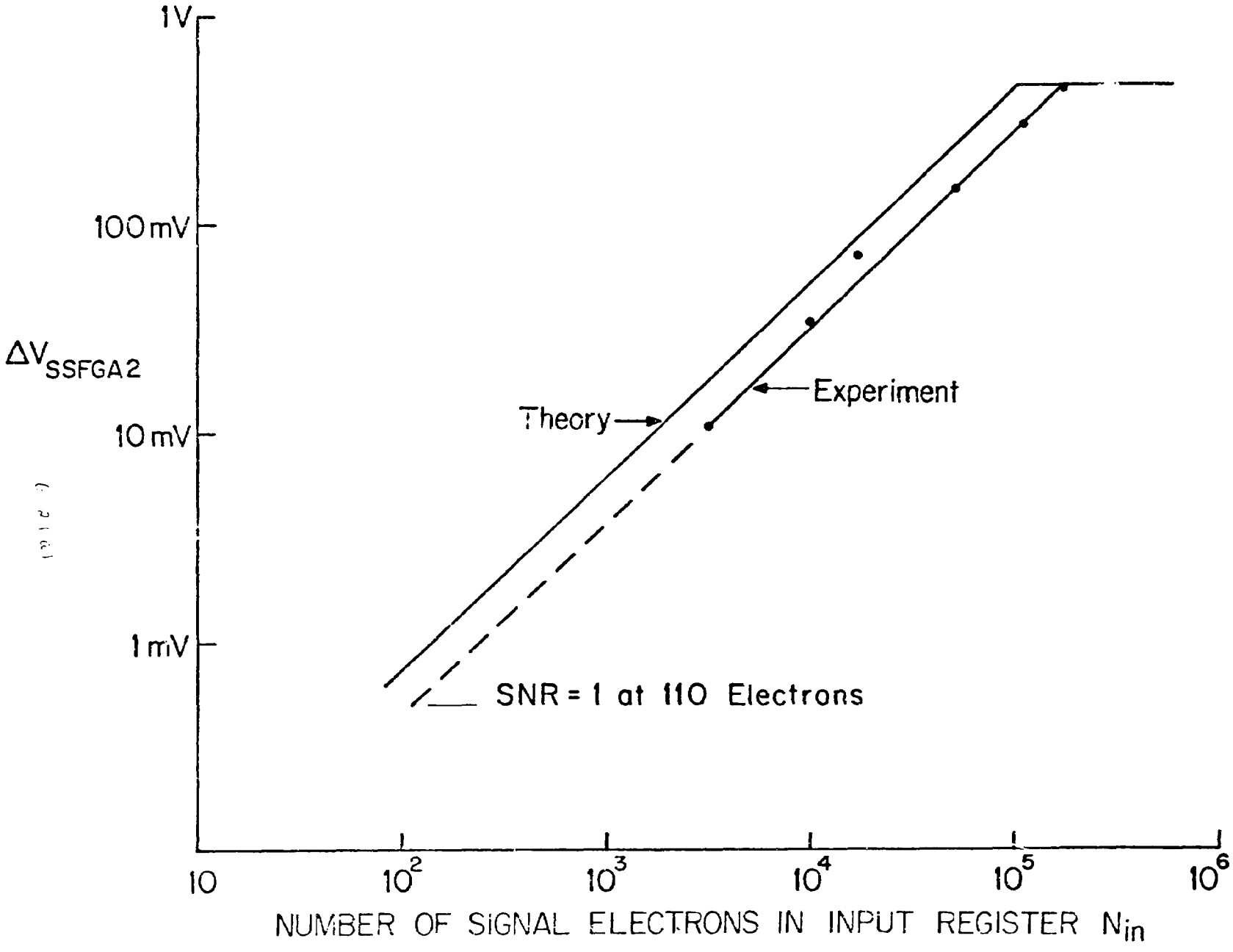


Figure 6.1.4 Single-Stage FCN Responsivity.

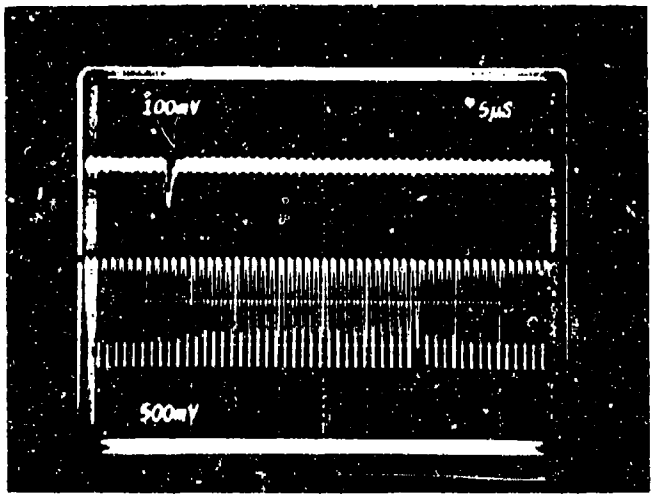
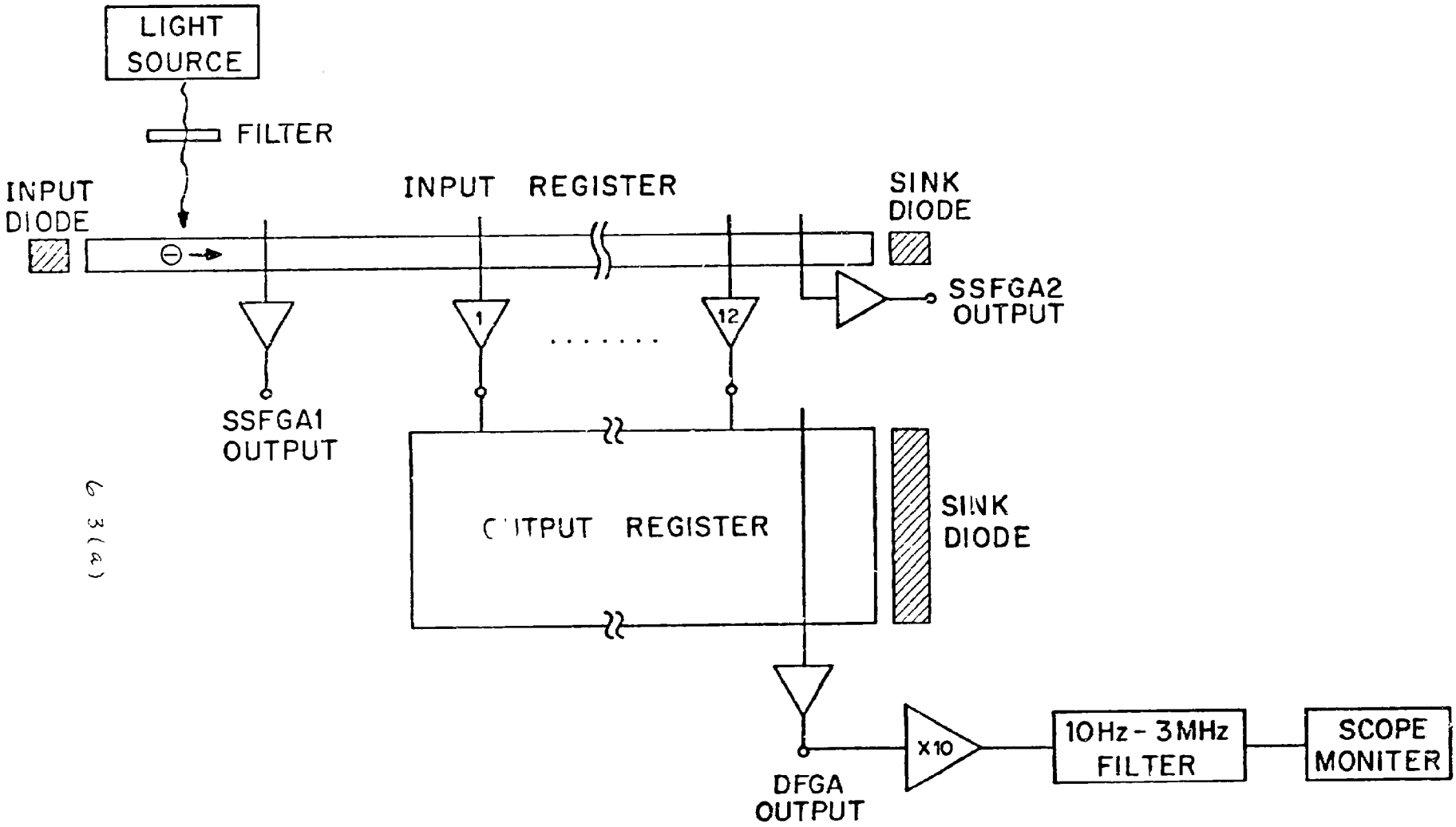


Figure 6.2.1. SSFGA1 (top trace) and DFGA (bottom trace) Outputs of a Signal Charge Packet in the Input Register

should be drawn from this figure because off-chip amplification and filtering conditions are different for the two outputs.

In order to obtain a transfer characteristic, i.e., output voltage vs. signal charge, for the DFGA, it is necessary to know exactly the magnitude of the signal charge that is present in the input register over the complete operating range. Since signal charge packets of less than 10^3 electrons cannot be accurately measured with a current meter, the optical arrangement illustrated in Figure 6.2.2 was employed to inject known quantities of charge into the DFGA. The procedure is briefly summarized as follows: A light source is focused on one element of the input register before the DFGA. The clock of the input register and the output register, since they are connected together, is held for 100 cycles to integrate the incident light for this period before a signal-charge packet is clocked to the DFCA input channel. A single signal-charge packet is obtained by this method. The number of electrons in this initial packet is obtained from the calibrated SSFGA outputs. The number of electrons, N_{in}, in the signal charge packet is then reduced by inserting neutral density filters to reduce the incident light intensity. N_{in} is assumed to be proportional to the light intensity.

In these measurements, the DFGA output is amplified by a 10X off-chip amplifier and band limited by a 10-Hz to 3-MHz filter. The register clock



6 3(a)

Figure 6.2.2 Optical Setup for Measuring DFGA Transfer Characteristic Curves.

frequency f was 1 MHz; the control gate "on" time t_{on} was set at 50 nsec. Since the DFGA signal V_s and the dominant noise source N_{shot} are related to t_{on} as indicated in equations (4.5.4), (4.5.2), and (5.2.3), this operation is approximately equivalent to f_{max} = 8 MHz, as discussed in Section 5.5. Since an ac source resistance Rs = 400 ohms is used for the output FGA, the source-follower gain is approximately 0.17, as estimated in Sections 4 and 5. Although an increase in Rs increases the amplitude of the DFGA output, it does not improve the signal-to-noise performance because the dominant noise sources appear before the output register.

The DFGA output waveform of the initial signal charge packet ($N_{in} = 10^5$ electrons) is shown in Figure 6.2.3. The outputs at reduced signal levels are shown in Figures 6.2.4 through 6.2.8. An expanded output waveform for N_{in} = 0 is shown in Figure 6.2.9. The rms noise fluctuation in the output may be seen to be approximately 1 mV. This DFGA transfer characteristic data is plotted in Figure 6.2.10. The theoretical prediction for f_{max} = 8 MHz, R_{FG1} = 3.0 μV per electron and R_{FG2} = 0.30 μV per electron is also shown. The measured rms noise of 1 mV corresponds to approximately 10 to 20 signal electrons.

The DFGA signal output Vs was related to the control gate "on" time t_{on} (in sec) as:

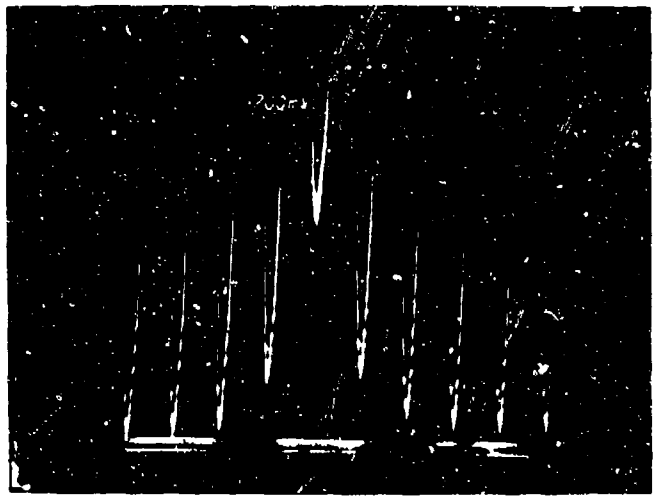


Figure 6.2.3 DFGA Output for $N_{in} = 10^5$ Electrons.

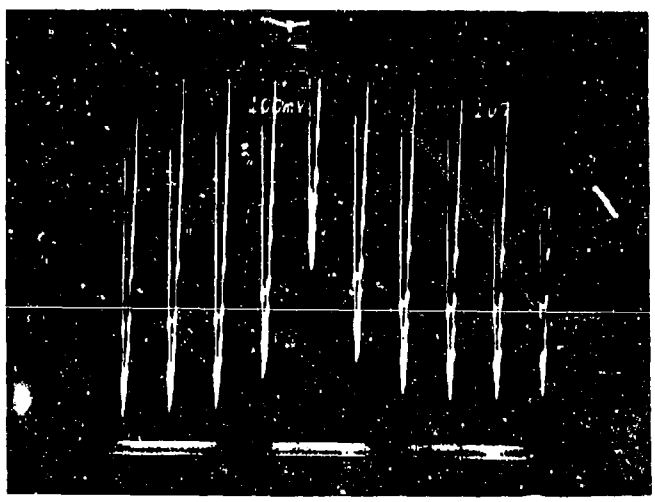


Figure 6.2.4 DFGA Output for $N_{in} = 3 \times 10^4$ Electrons.

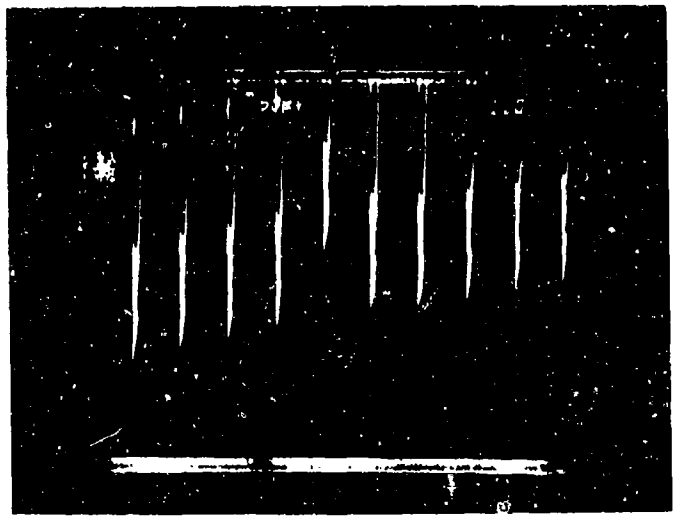


Figure 6.2.5. DFGA Output for $N_{in} = 3 \times 10^3$ Electrons

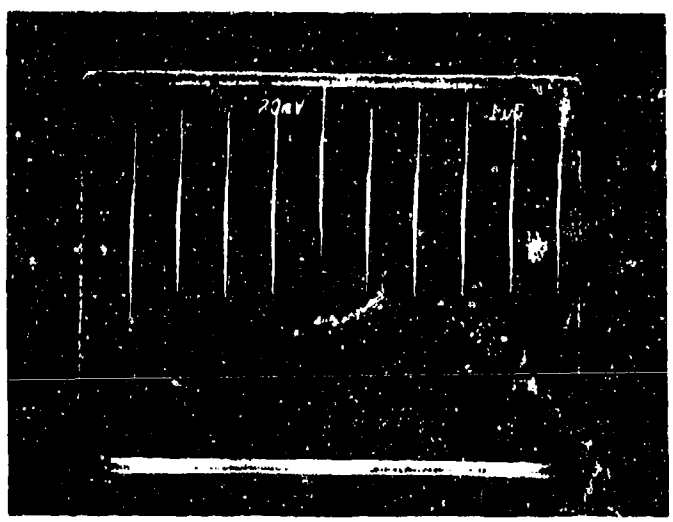


Figure 6.2.6 DFGA Output for N_{in} = 300 Electrons

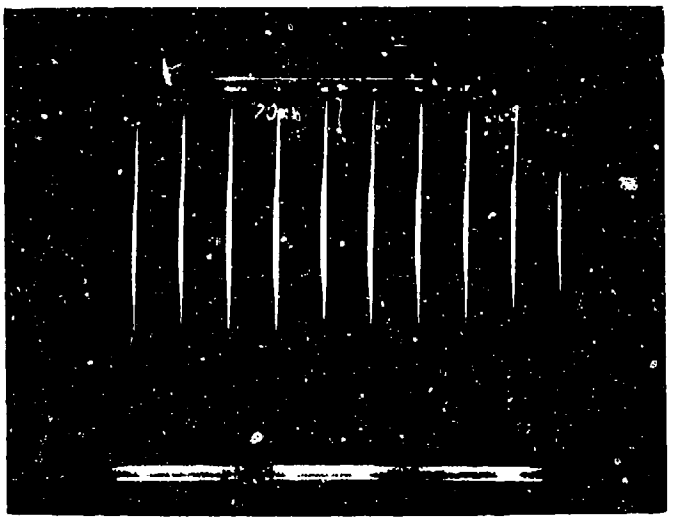


Figure 6.2.7 DFGA Output for N_{in} = 30 Electrons.

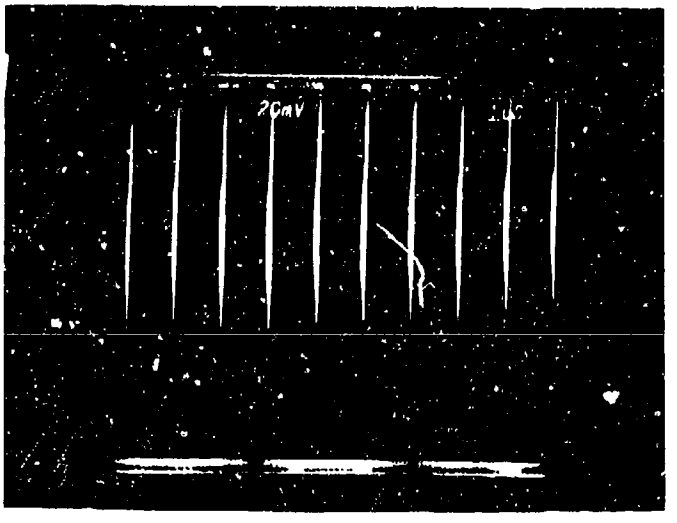


Figure 6.2.8 DFGA Output for N_{in} = 0 Electrons.

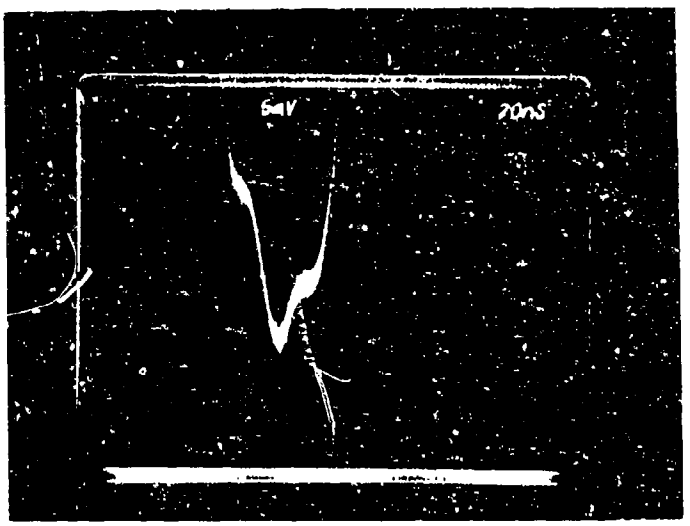


Figure 6.2.9 DFGA Noise in Dark

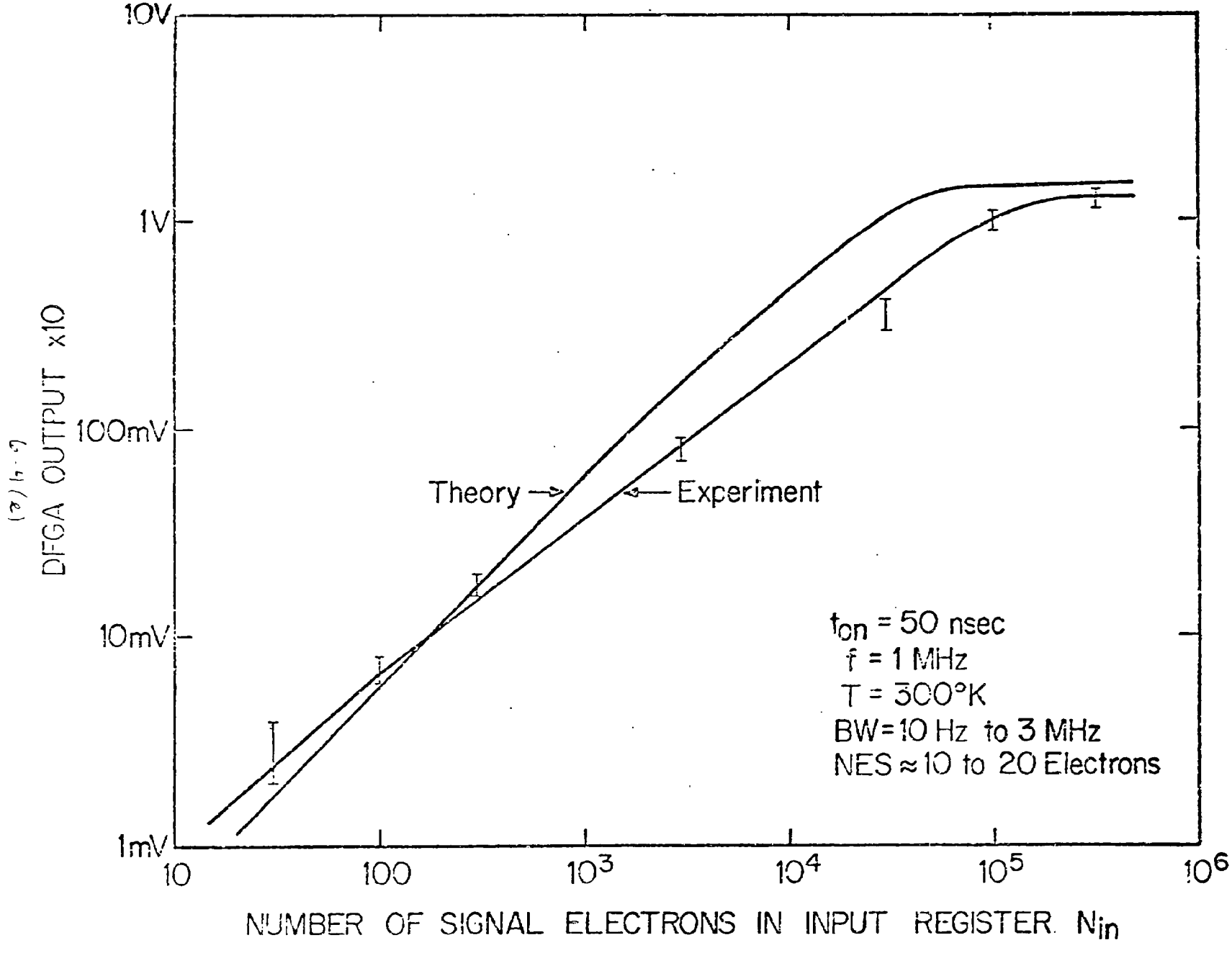


Figure 6.2.10 DFGA Transfer Characteristic Curves.

$$V_s = 170\, N_{in}\, t_{on} \quad \text{(volt)} \tag{4.5.3}$$

This relationship is evident in Figure 6.2.11 where V_s is plotted as a function of several values of t_{on} for a given N_{in}. V_s for t_{on} = 50 nsec is arbitrarily chosen as 1.

6.3 NOISE CHARACTERIZATION

The charge amplifiers in the DFGA are biased at the maximum signal-to-noise operating point of I_D ~ 1 μA, as discussed in Section 4.3. For $I_D \leq 1\,\mu A$, the transistor is characterized by the subthreshold equation (4.3.6). In this region,

$$V_s \propto V_{bias} \tag{6.3.1}$$

and

$$(V_{shot}) \propto V_{bias} \tag{6.3.2}$$

V_S is the output signal voltage and V_{bias} is the output voltage when N_{in} = 0 as indicated in Figure 3.2.5. A similar DFGA output waveform is also illustrated in Figure 6.3.1. The noise voltage at two different positions in the waveform are indicated by V_{N1} and V_{N2}. V_{N1} represents the DFGA output noise voltage. V_{N2} is the DFGA output voltage when the charge in the output register is not being sensed by the output FGA. Therefore, V_{N2} represents the noise of the output FGA; V_{N1} represents the noise from all noise sources of the DFGA, as shown in Figure 5.1.

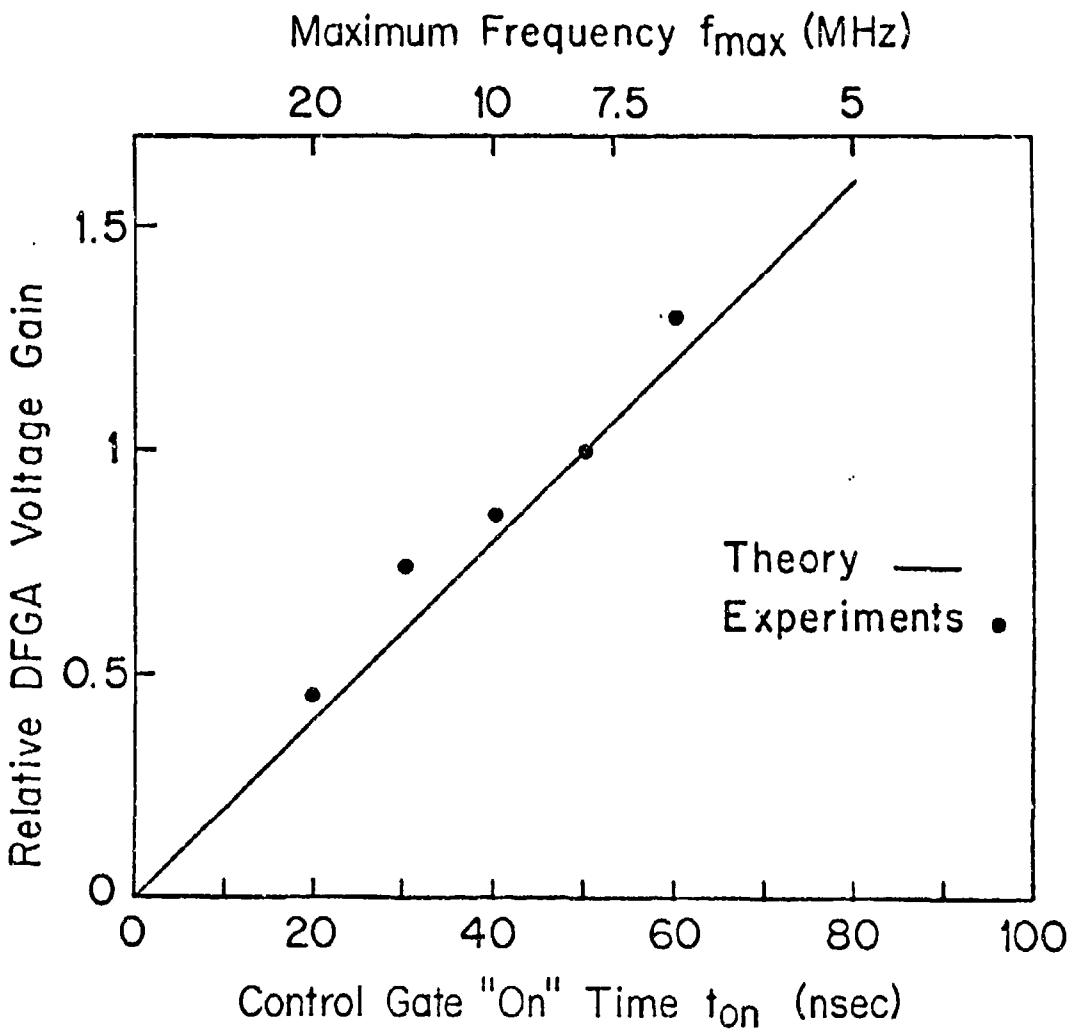


Figure 6.2.11 DFGA Gain vs. Control Gate "on" Time.

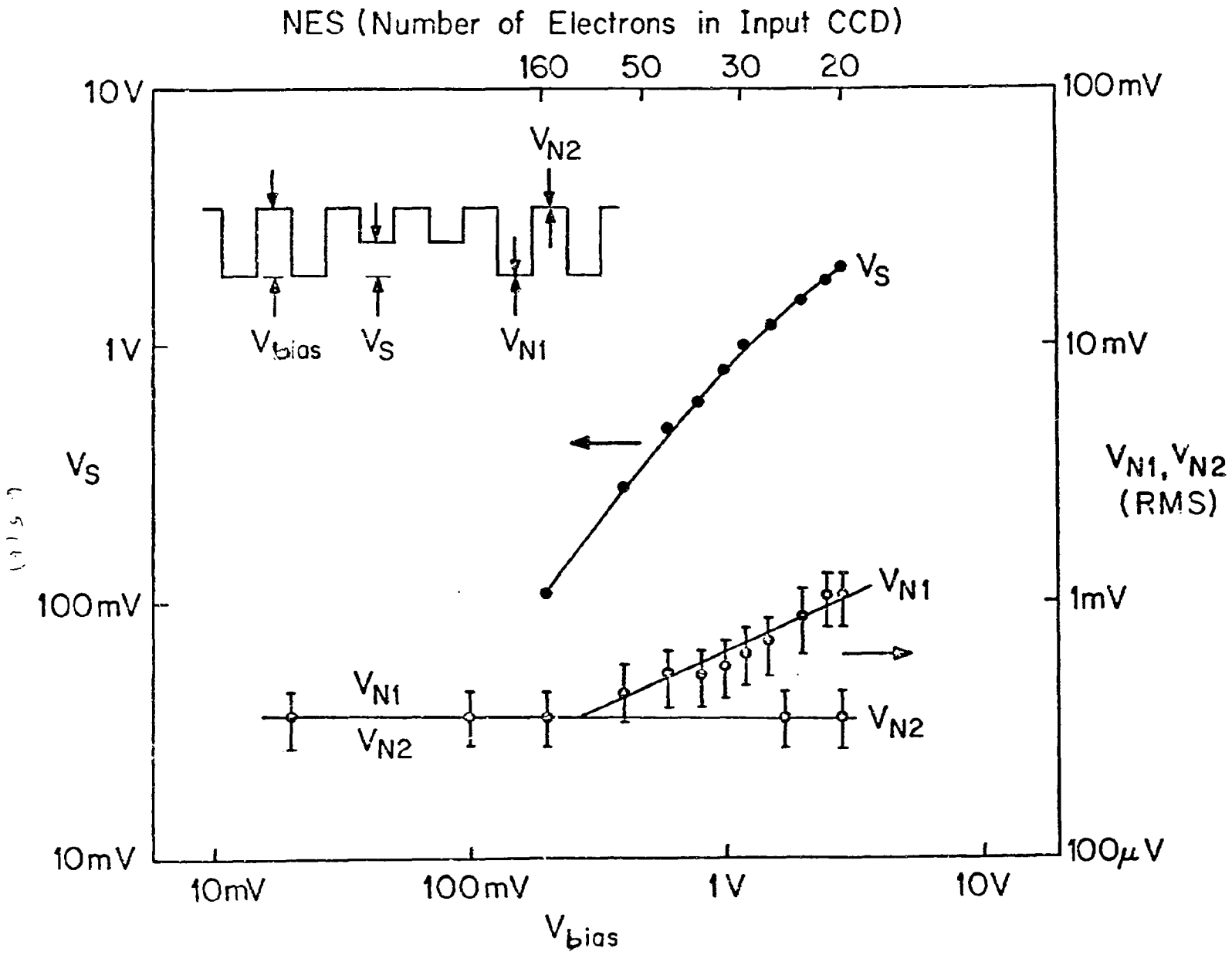


Figure 6.3.1 DFGA Noise V_{N1} Shows Shot-Noise Like Behavior.

The operating point, I_D, of the charge amplifiers can be changed by variation of the source voltage designated in Figure 3.1.2. As I_D is reduced from 1 μA, both the gain (gm and V_s) and the bias charge (V_{bias}) are reduced. For a constant signal in the DFGA input channel, V_s is plotted as a function of V_{bias} in Figure 6.3.1. The measured FGA output noise voltage, V_{N1}, is also plotted as a function of V_{bias} in the same figure. It may be seen that the relationship:

$$V_{N1} \propto V_{bias}^{1/2}$$

is obtained. This indicates that the dominant noise source in the DFGA is shot noise in the charge amplifier, as discussed in Section 5.

V_{N2} is the noise associated only with the output FGA. That it is independent of V_{bias}, is demonstrated by the measurements plotted in Figure 6.3.1.

6.4 SUMMARY OF THE EXPERIMENTAL RESULTS

A 12-stage DFGA has been fabricated and evaluated. Signal electrons ranging from 30 to 10^5 were detected with a control gate "on" time t_{on} of 50 nsec and with 10 Hz to 3 MHz bandwidth at room temperature. The rms noise for the same condition corresponds to approximately 13 electrons. The effect of control gate "on" time and bias level of I_D have also been experimentally verified. Noise measurements at different bias conditions indicate that shot noise in the charge amplifiers is the dominant noise source of the DFGA as predicted.

SECTION 7

SUMMARY AND CONCLUSIONS

The concept of the floating-gate amplifier offers two principal advantages over the gated-charge integrator that is conventionally employed as an on-chip detector-preamplifier for charge-coupled devices. The first advantage is that the floating-gate amplifier does not require a reset function, which introduces a large kTC noise component in the gated-charge integrator. The second advantage is that a charge packet may be sensed nondestructively in a CCD channel by a floating gate. In the distributed floating-gate amplifier (DFGA), a charge packet is sensed repeatedly as it passes through a CCD channel. The input signal is thereby multiplied by the number of stages employed, while the noise is increased by the square root of the number of stages used.

This report describes the design and evaluation of a 12-stage distributed floating-gate amplifier. The device possesses an input CCD channel with 12 floating gates. Each of these gates are common elements of 12 MOS transistors, which are inverting charge amplifiers. Charge from these amplifiers is gated into an output CCD channel, where the amplified signal charge is summed as it moves through this channel in synchronism with the charge in the input channel. This summed signal is then sensed by a floating-gate amplifier at the end of the output channel.

In this design the floating-gate geometry was optimized for maximum signal-to-noise ratio. The optimum operating point of the charge amplifier was then determined for this geometry. The output register was designed to store the maximum charge from all 12 charge-amplifier stages.

It is concluded from a noise analysis that shot noise in the charge amplifier is the dominant noise source in the DFGA. The noise level for all significant noise sources is predicted for the operating parameters, clock frequency and the time that the charge amplifiers are activated. It is seen that a noise equivalent signal of 17 electrons is theoretically possible for a charge-amplifier active (or on) time of 50 nsec, which corresponds to a maximum bit rate of 8 MHz.

Experimental characterization of the device showed excellent agreement with the theoretical predictions at small signal charge levels. A noise equivalent signal of 10 to 20 signal electrons was obtained at room temperature for a 50 nsec charge-amplifier activation time, and for a 3 MHz bandwidth. At high signal level, a saturation characteristic softer than predicted was observed. This effect is probably caused by charge-spreading under the floating gate at these high levels.

Experiments were conducted to identify the dominant noise source. Since the noise was found to be proportional to the square root of the total charge

in the output register, it is concluded that the dominant noise source is the shot noise of the charge-amplifier in agreement with the noise analysis.