ARL-TR-8940 ● APR 2020

Ka-Band Front-End Monolithic Microwave Integrated Circuits (MMICs) and Transmit–Receive (T/R) Modules Testing

by John E Penn and Ali Darwish

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14. ABSTRACT

The US Army Combat Capabilities Development Command Army Research Laboratory has been evaluating and designing efficient broadband high-power amplifiers, switches, and high-dynamic-range low-noise amplifiers for use in networking and communications at millimeter wave frequencies. Gallium nitride monolithic microwave integrated circuit (MMIC) technology has superior performance in power amplifier applications as well as for low-noise amplifiers with high dynamic range and the ability to survive large, potentially damaging input power levels without the need for additional limiters at the system level. This technology works well for high-power solid-state switches as well. Compact MMIC transmit–receive modules for use in Ka-band (±28 GHz) applications, particularly transceiver arrays, were designed and submitted to Qorvo, Inc., for fabrication. This technical report documents the testing, analysis, evaluation, and lessons learned from these high-performance MMIC circuits.

15. SUBJECT TERMS
microwave, monolithic microwave integrated circuit, MMIC, mmW, amplifier, transceiver, gallium nitride, GaN

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1. Introduction

The US Army Combat Capabilities Development Command Army Research Laboratory (ARL) has been evaluating and designing efficient broadband high-power amplifiers for use in sensors, communications, networking, and electronic warfare (EW). ARL submitted designs of Ka-band low-noise amplifiers (LNAs), power amplifiers (PAs), and transmit–receive (T/R) switches using Qorvo Inc.'s high-performance 0.15-μm gallium nitride (GaN) fabrication process. These amplifiers were fabricated as one- and two-stage designs as well as integrated T/R modules for bidirectional transceivers as part of a recent ARL Qorvo Prototype Wafer Option (PWO), which yields many different designs from two full 4-inch GaN wafers. This technical report documents testing and analysis of these designs, as well as lessons learned for improvements to future design efforts. (See ARL-TR-8855 for documentation of these designs.[1])

2. Low-Noise Amplifiers

The key component for a Ka-band transceiver is the LNA, which, when implemented in GaN, has the added advantages of high dynamic range and robust survivability to high-power interference signals. These LNAs were designed with a goal of several gigahertz bandwidth centered around 28 GHz. Various matching topologies, stabilizing approaches, and tradeoffs of gain versus noise figure were explored for two high-electron-mobility transistor (HEMT) sizes, using the limited devices in the process design kit (PDK) that had noise data, for 5-V or 10-V biases. These designs were intended for 10-V operation, so while they work over biases of 5 V to 28 V, the targeted optimal performance is at 10 V with a typical 100-mA/mm drain current. The LNAs were designed as two-stage amplifiers, with the first stage optimized for low noise figure. Even though the first stages were not designed for optimal use as a standalone amplifier, they were fabricated as test circuits for testing and analysis of the two-stage LNAs. There were two designs based on a 4- × 25-μm and a 6- × 25-μm HEMT, each trading off stability, noise figure, return loss, and gain. Initially, the larger 6- × 25-μm LNA design seemed a narrower band stable design compared with a potentially broader band gain with the smaller HEMT size but with a riskier tradeoff of stability versus stability.

Figure 1 shows a plot of measurements (solid) versus simulations (dash) of the small signal s-parameters of the first-stage 6- × 25-μm LNA, at the nominal 10-V DC bias. While the shapes are similar, the actual gain is higher but slightly narrower band. A similar comparison plot is shown in Fig. 2 for the same LNA measured at 5 V. The shift to a lower frequency, both simulated and measured, is noted at the

lower 5-V bias. Recall that the design was intended for 28 GHz at 10-V operation, but could be used at the lower 5-V operation for a slightly lower frequency band operation, or conversely, over slightly higher frequency bands for DC voltages higher than 10 V. An electromagnetic (EM) resimulation of the full one-stage LNA layout was repeated to eliminate the possibility of unsimulated parasitic interaction among the input match, source inductance, and output match of this very compact layout. But, the full EM layout result was similar to the original simulation where those three EM layouts were independent sections. The higher gain peak could be explained by lower than expected source inductance, or could be due to typical process variation in fabrication.

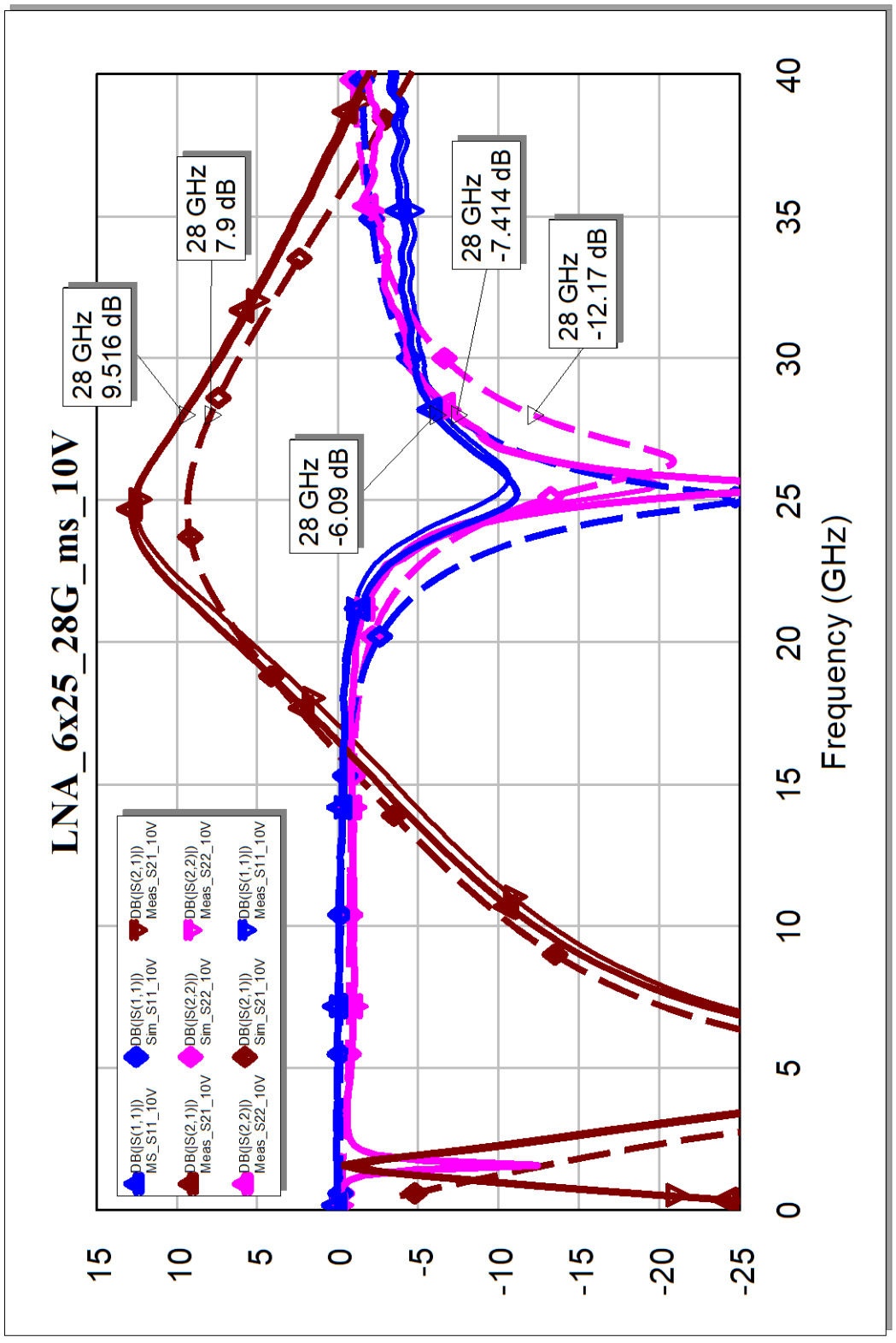

Fig. 1 Measured (solid) vs. simulation (dash) one-stage 6- × 25-µm LNA (10 V)

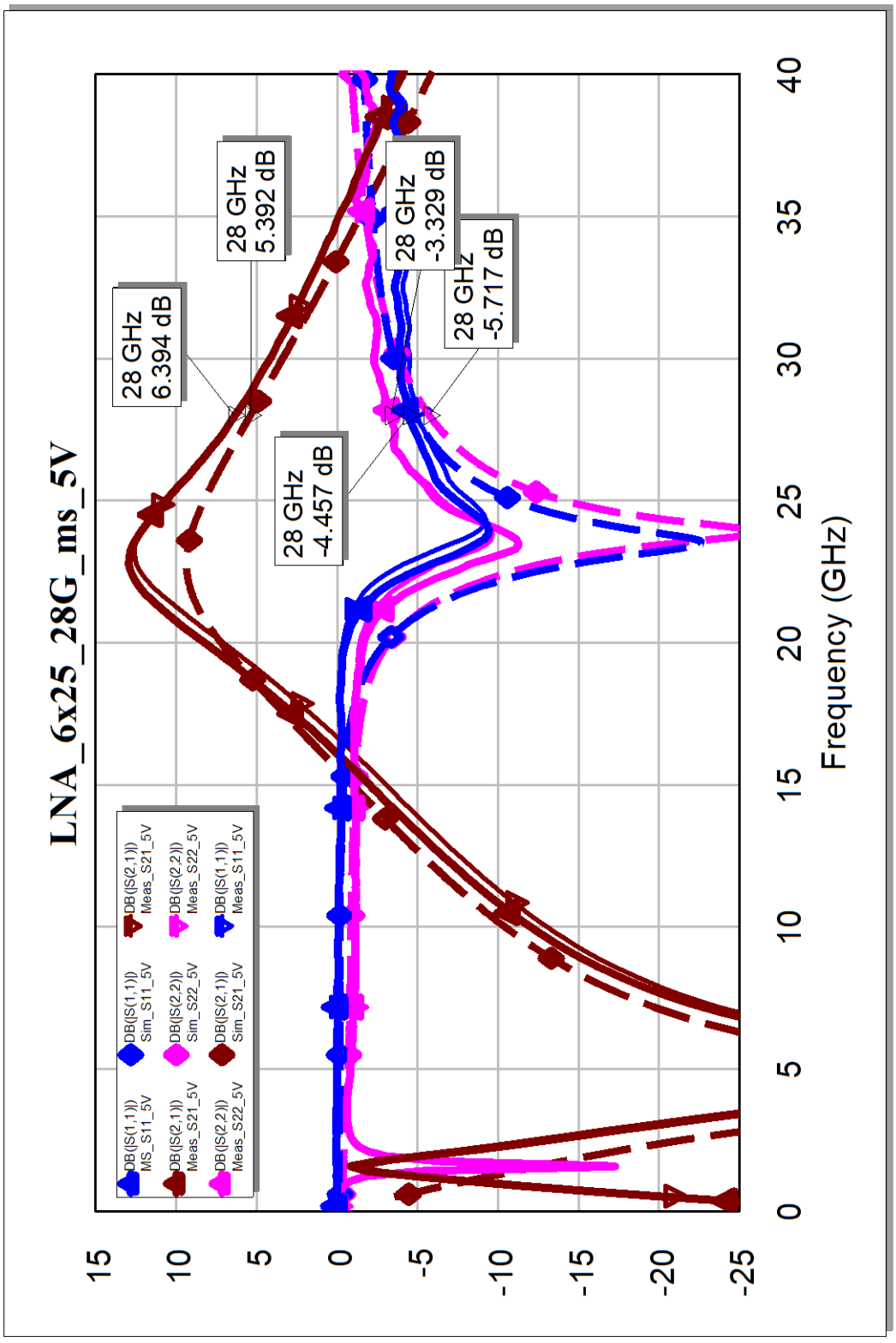

Fig. 2 Measured (solid) vs. simulation (dash) one-stage 6- × 25-µm LNA (5 V)

With the other 4- × 25-μm LNA, there is excellent agreement between measured and simulated performances. Figure 3 shows measured (solid) versus simulation (dash) plot of the small signal s-parameters of the first stage 4- × 25-μm LNA, at the nominal 10-V DC bias, while Fig. 4 is the same comparison but at 5-V DC bias. Once again, the peak performance shifts down a few GHz at the lower 5-V bias but agrees well with the linear simulation. It should be noted the nonlinear device models for the 4- × 25-μm and 6- × 25-μm HEMTs did not agree nearly as well as the linear models; possibly they only fit well for higher voltages or possibly these particular models need updating. As a standalone one-stage amplifier, the 4- × 25-μm first-stage shows broader, but lower, gain in comparison with the 6- × 25-μm LNA.

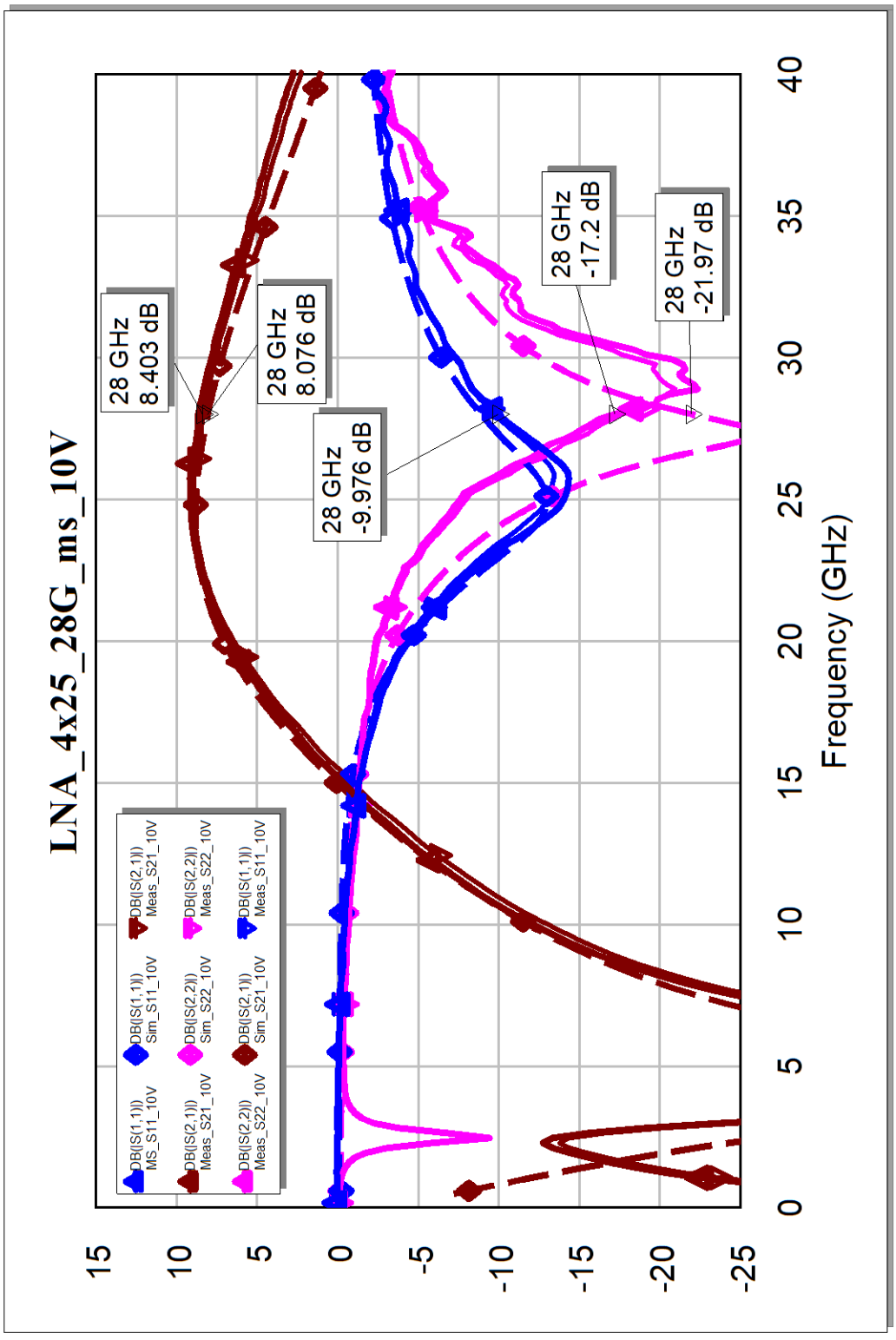

Fig. 3 Measured (solid) vs. simulation (dash) one-stage 4- × 25-µm LNA (10 V)

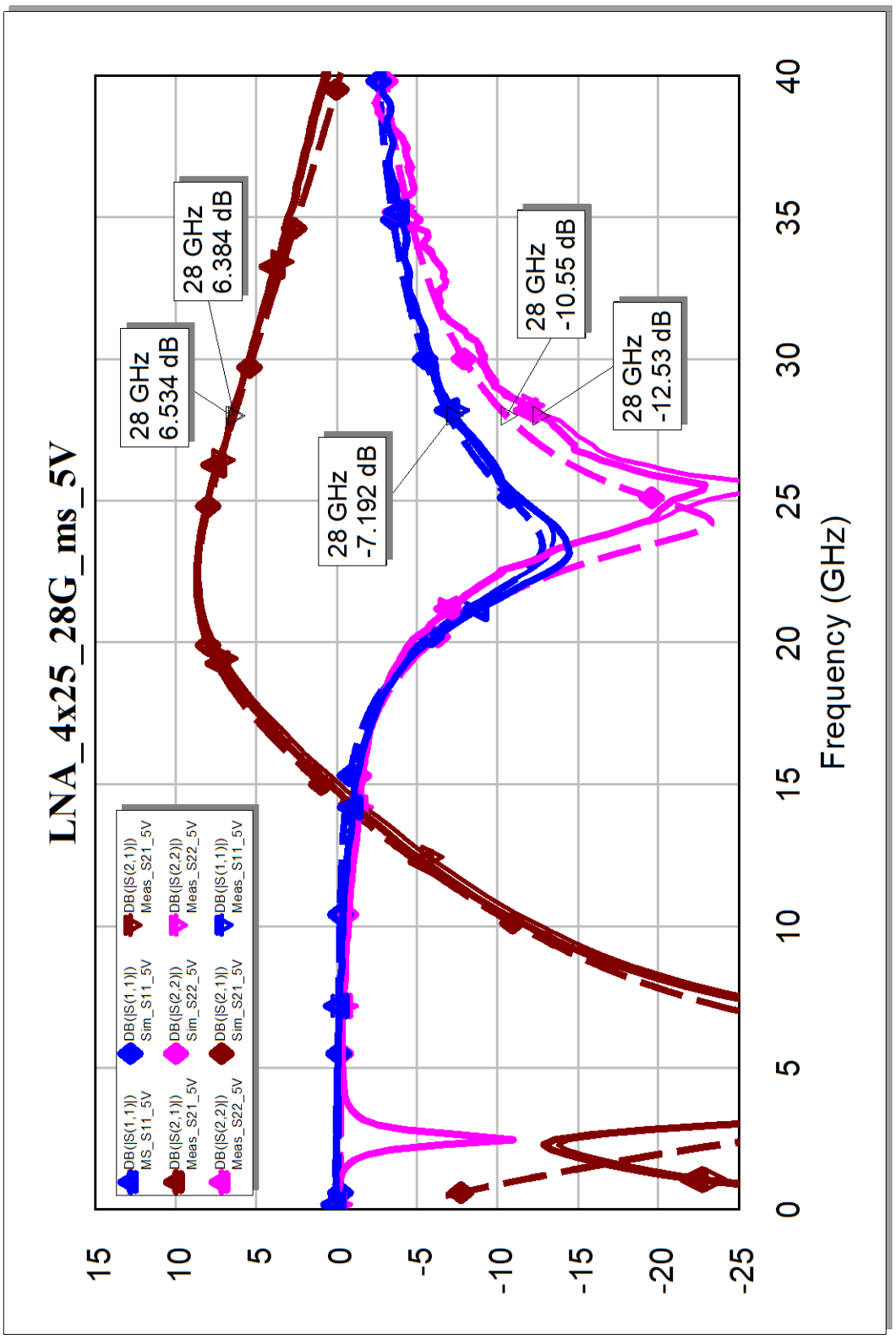

Fig. 4 Measured (solid) vs. simulation (dash) one-stage 4- × 25-µm LNA (5 V)

For the two-stage LNA design of the 6- × 25-μm HEMT, the gain peak is even more pronounced than the one-stage; otherwise, the gain curve follows the prediction. There is also an unstable region, as the input match is very poor right at the gain peak, especially at the lower 5-V DC bias. Figure 5 shows measured (solid) versus simulation (dash) plot of the small signal s-parameters of the two-stage 6- × 25-μm LNA at 10-V DC bias, while Fig. 6 is the same comparison at 5-V DC bias. It may be that the high gain peak of more than 20 dB at 26–27 GHz at 10 V, and closer to 25 GHz at 5 V, could be due to typical process variation. Fortunately, the other two-stage 4- × 25-μm LNA, which uses less DC power (20 mA vs. 30 mA), yields broader band gain, and was included in the T/R module layouts of these first-pass designs.

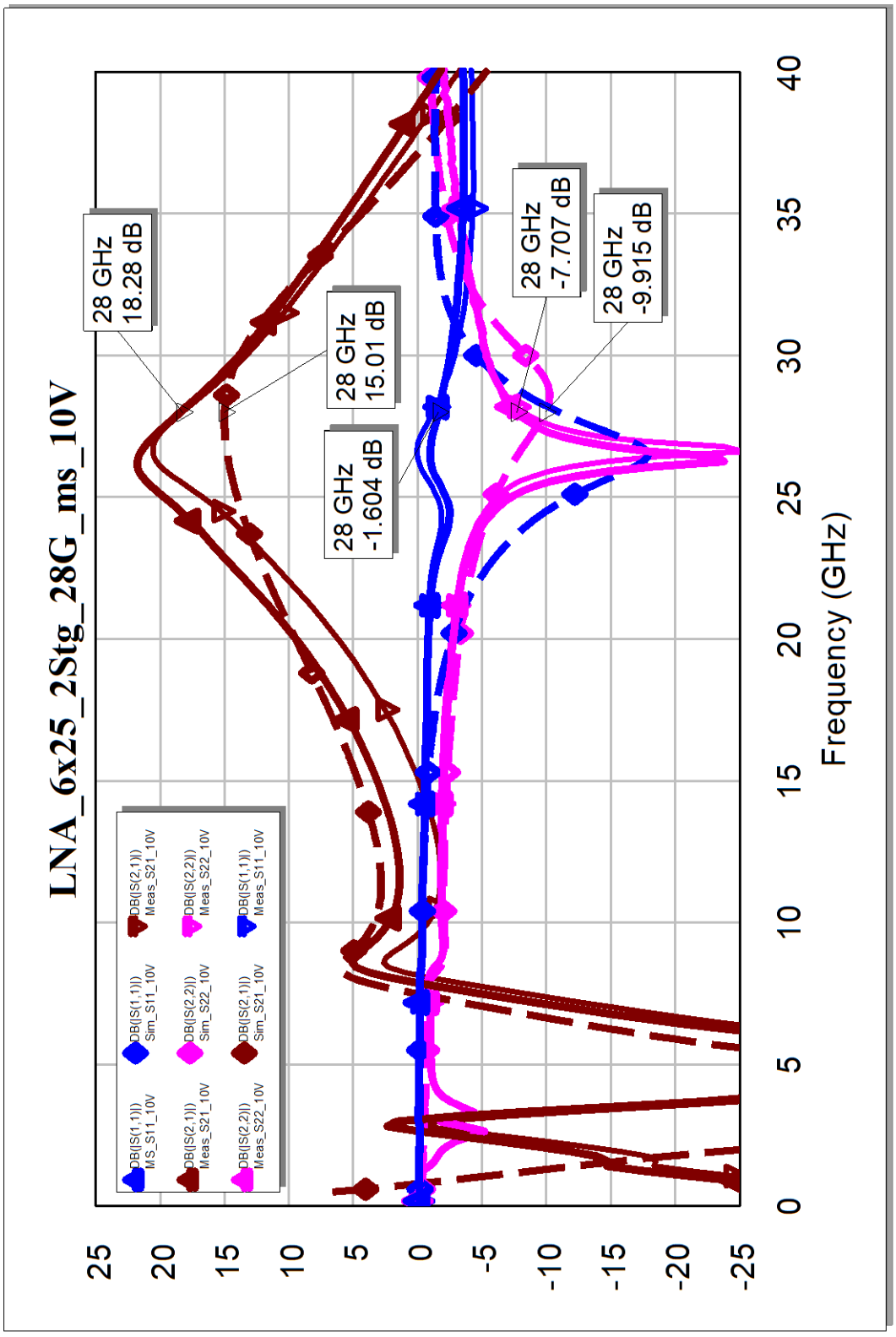

Fig. 5 Measured (solid) vs. simulation (dash) two-stage 6- × 25-µm LNA (10 V)

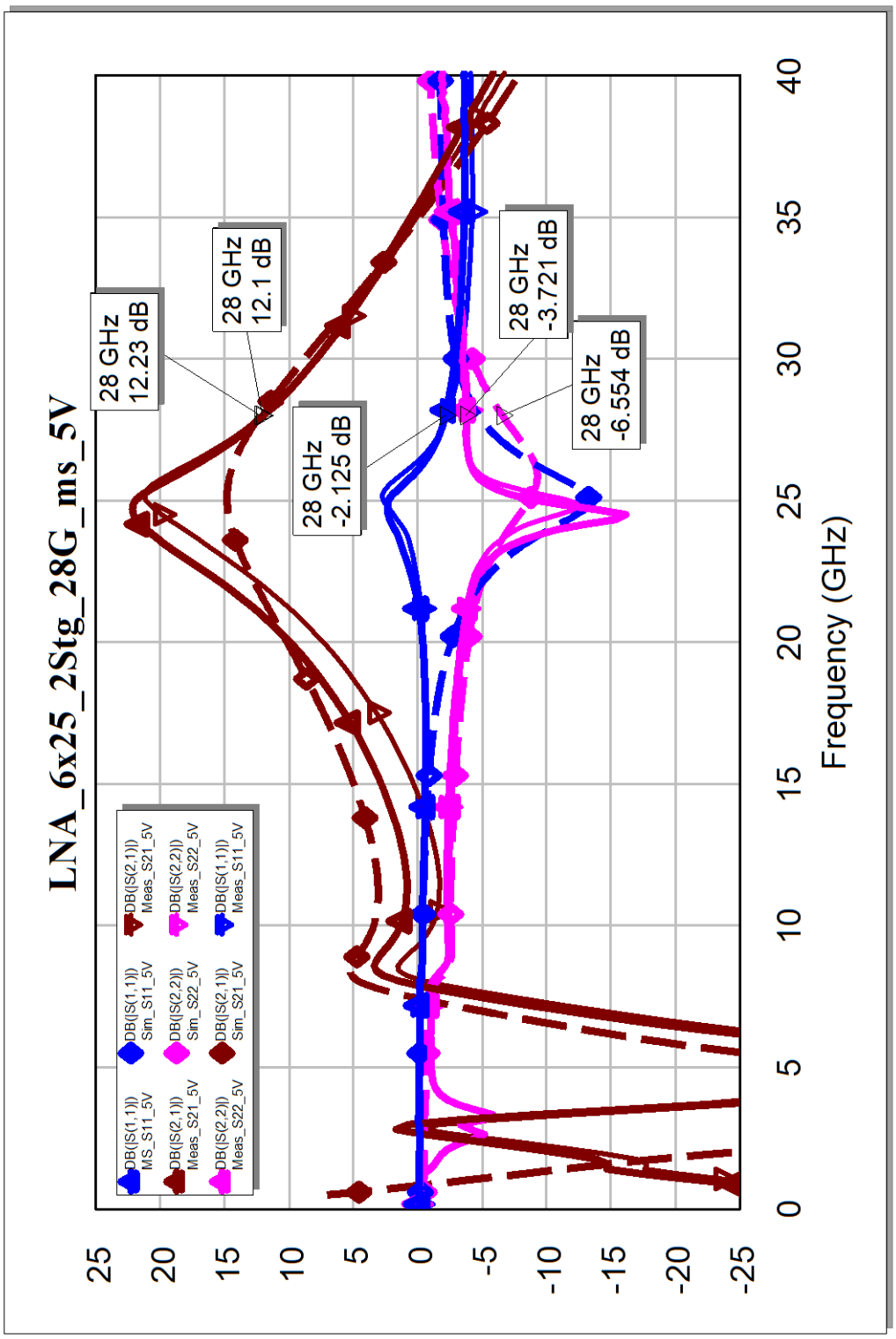

Fig. 6 Measured (solid) vs. simulation (dash) two-stage 6- × 25-µm LNA (5 V)

As with the first-stage, the two-stage 4- × 25-μm LNA shows very good agreement between measured and simulated performances. Figure 7 shows a measured (solid) versus simulation (dash) plot of the small signal s-parameters of the two-stage 6- × 25-μm LNA at 10-V DC bias, while Fig. 8 is the same comparison at 5-V DC bias. There is the slight downshift of gain performance by a few GHz between the design biased at 10 V versus 5 V. The minimal differences between measured and simulated s-parameters are within typical process variation and/or typical modeling accuracy. The noise figure still needs to be measured for these LNA designs to verify the expected performance, particularly for the 4- × 25-μm LNA design included in the T/R modules. Poor return loss and potential instability of the two-stage 6- × 25-μm LNA design may make noise-figure measurements difficult, or result in higher than expected noise figure.

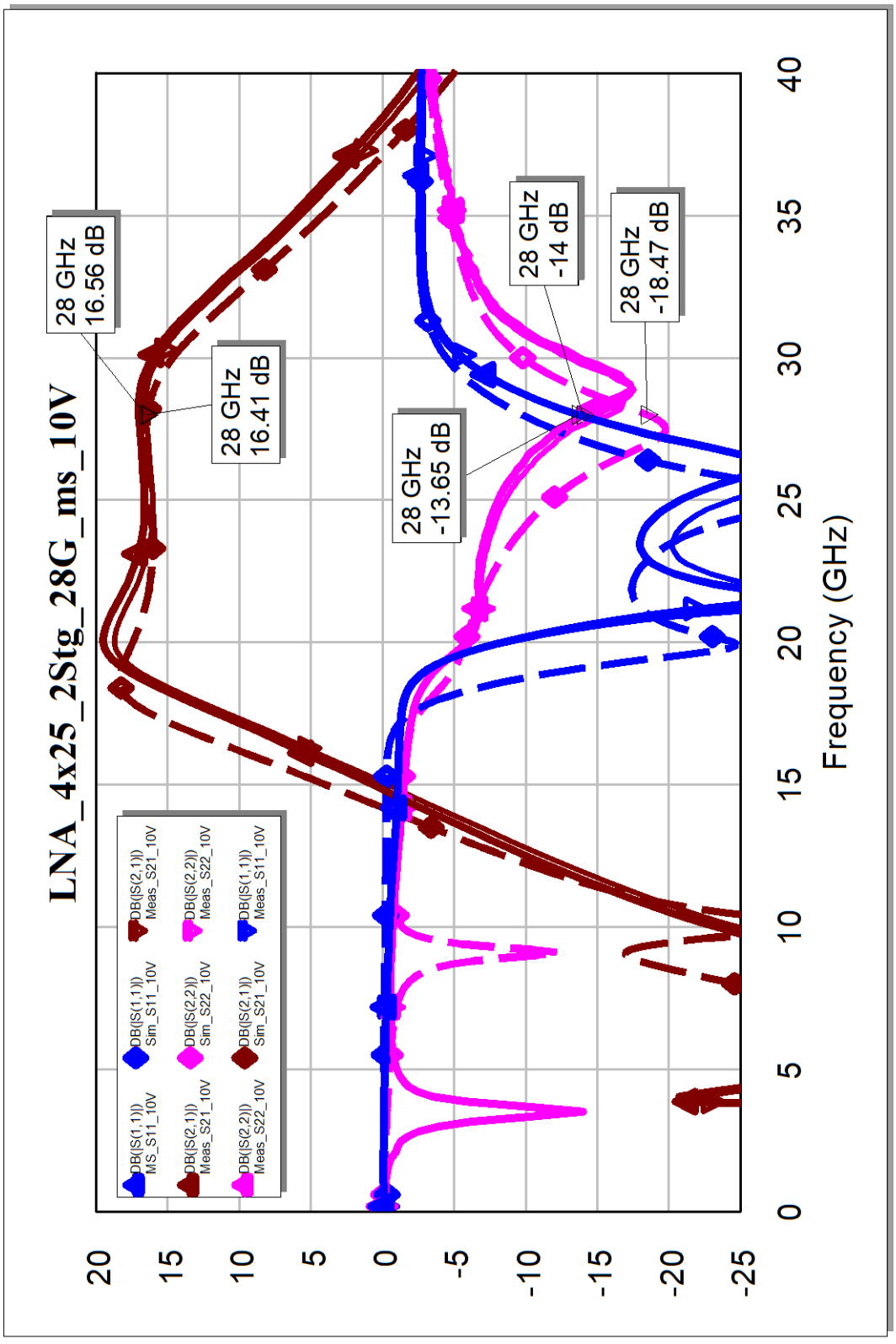

Fig. 7 Measured (solid) vs. simulation (dash) two-stage 4- × 25-µm LNA (10 V)

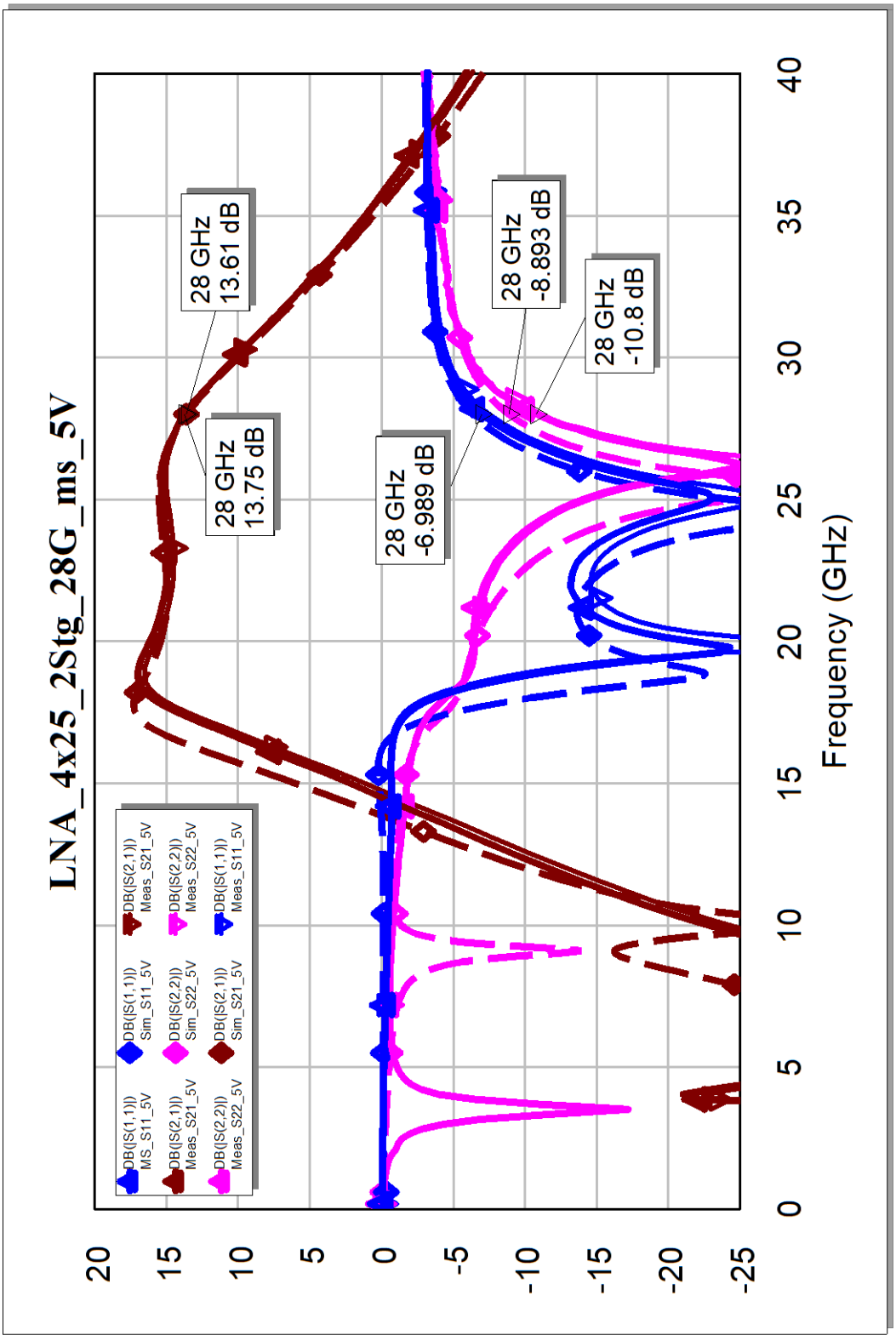

Fig. 8 Measured (solid) vs. simulation (dash) two-stage 4- × 25-µm LNA (5 V)

3. Power Amplifiers

Designs for a Ka-band transceiver included efficient PAs with an output power goal near 1 W at 28 GHz. The PA design variations comprised a 4- × 50-μm HEMT as both a driver and output stage and an 8- × 50-μm HEMT as an output stage. The designs were optimized for nominal DC biases of 28 V (100 mA/mm), but should operate well at 20 V with less output power. To achieve sufficient gain, a two-stage amplifier was designed with an output stage matched for power and efficiency. Both the 4- × 50-μm and 8- × 50-μm one-stage PAs were fabricated standalone for test and evaluation. Small signal s-parameters are measured first to verify gain and stability before measuring power performance.

Figure 9 shows measured (solid) versus simulation (dash) plots of the small signal s-parameters of the 4- × 50-μm PA at the nominal 28-V DC bias. Measurements at 20 V are also shown, though the results shift down in frequency and exhibit slightly lower gain. This trend continues for measurements at 10 V and 5 V as the gain bandwidth shifts lower in frequency and drops in gain for lower drain voltages. Gain is also typically a function of drain current, with good gain exhibited for a typical 100-mA/mm bias, with even more gain at 150 mA/mm, and only a slight increase of gain at 200 mA/mm. Simulations with the HEMT models predict similar small signal performance between 20 V and 28 V, while measurements show a larger variation between 20-V and 28-V DC biases.

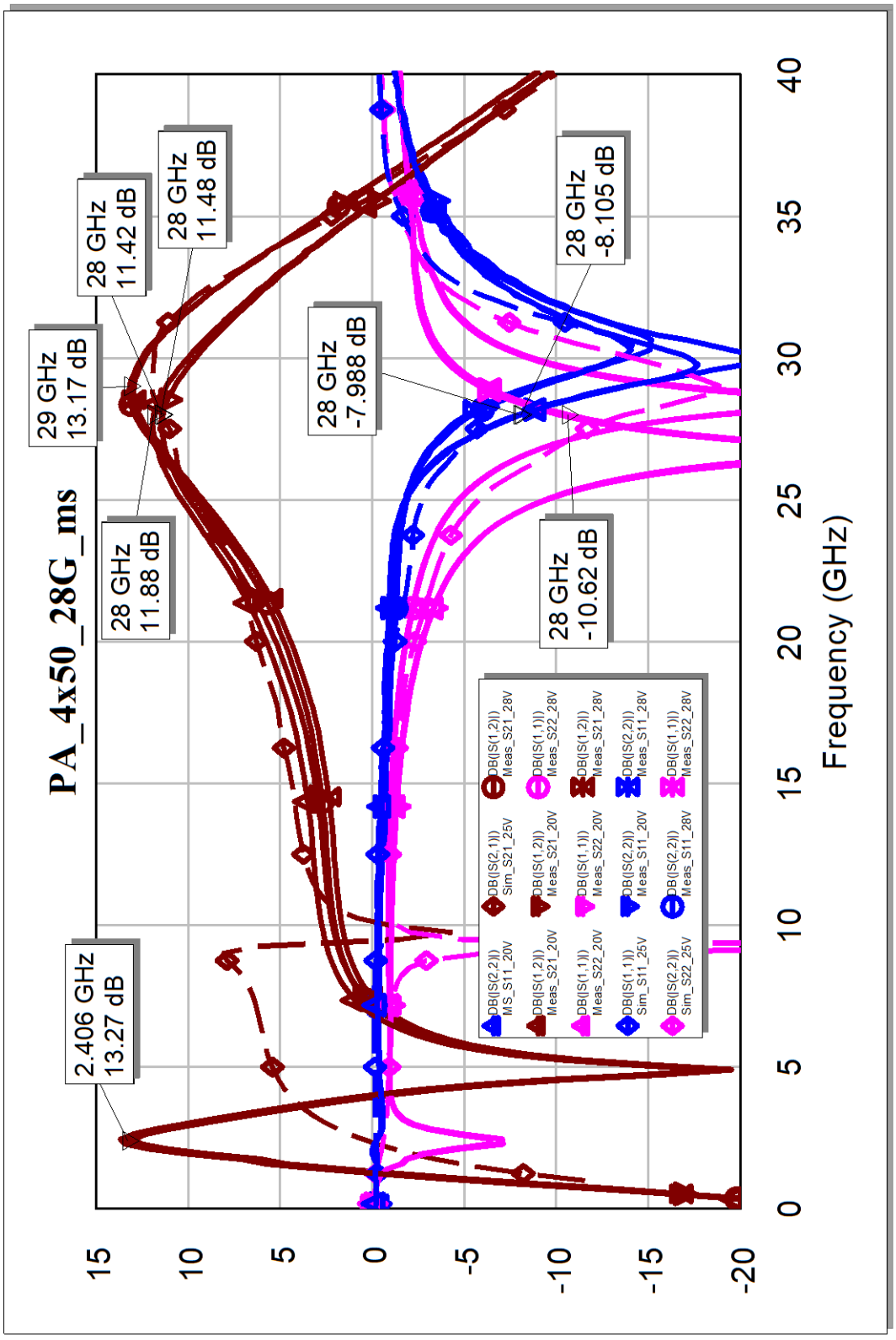

Fig. 9 Measured (solid) vs. simulation (dash) one-stage 4- × 50-µm PA (20 V, 28 V)

Figure 10 shows measured (solid) versus simulation (dash) plots of the small signal s-parameters of the 8- × 50-μm PA at the nominal 28-V DC bias. Measurements at 20 V are also shown, with a similar down shift of gain versus frequency and slightly lower gain. Note the slightly narrower gain peak of the larger 8- × 50-μm HEMT PA compared with the previous 4- × 50-μm PA.

Two different two-stage amplifiers were designed; both used the 4- × 50-μm PA as a driver stage, while one used the 4- × 50-μm as an output stage and the other used the larger 8- × 50-μm output stage to achieve more than 1 W of output power. The plot in Fig. 11 shows good agreement between measurements (solid) and simulations (dash) of the small signal s-parameters of the two-stage 4- × 50-μm PA at 20-V and 28-V DC bias. This PA yields very good broadband gain, up to 24 dB (28 GHz, 28 V). Figure 12 shows measured (solid) versus simulation (dash) plots of the small signal s-parameters of the two-stage 4- × 50-μm, 8- × 50-μm PA at 20-V and 28-V DC bias. This also has excellent gain near 25 dB with good agreement, though the input match is poorer than expected. This could be due to typical process variation, or the bias may need to be adjusted to improve the agreement to simulations.

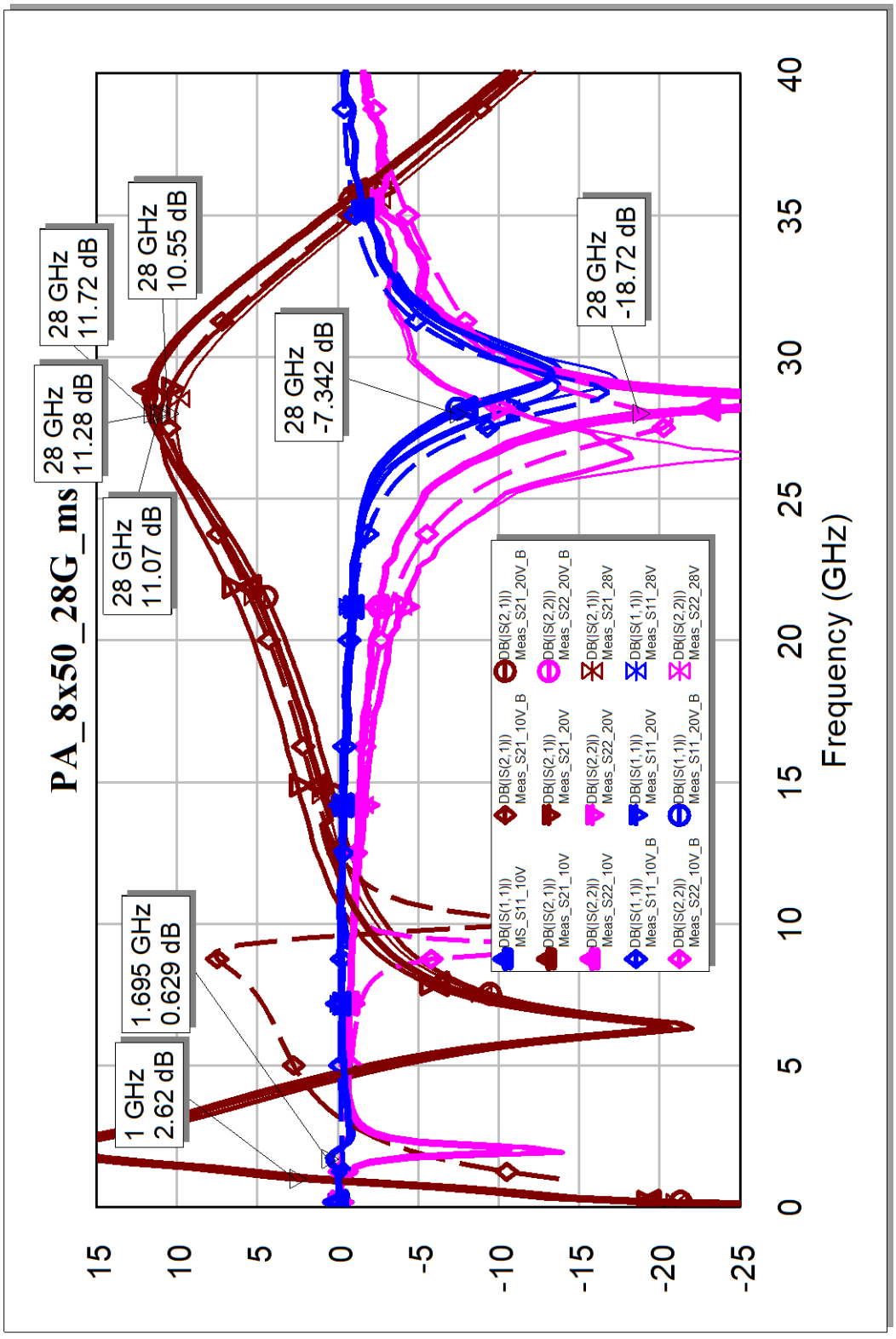

Fig. 10 Measured (solid) vs. simulation (dash) one-stage 8- × 50-µm PA (20 V, 28 V)

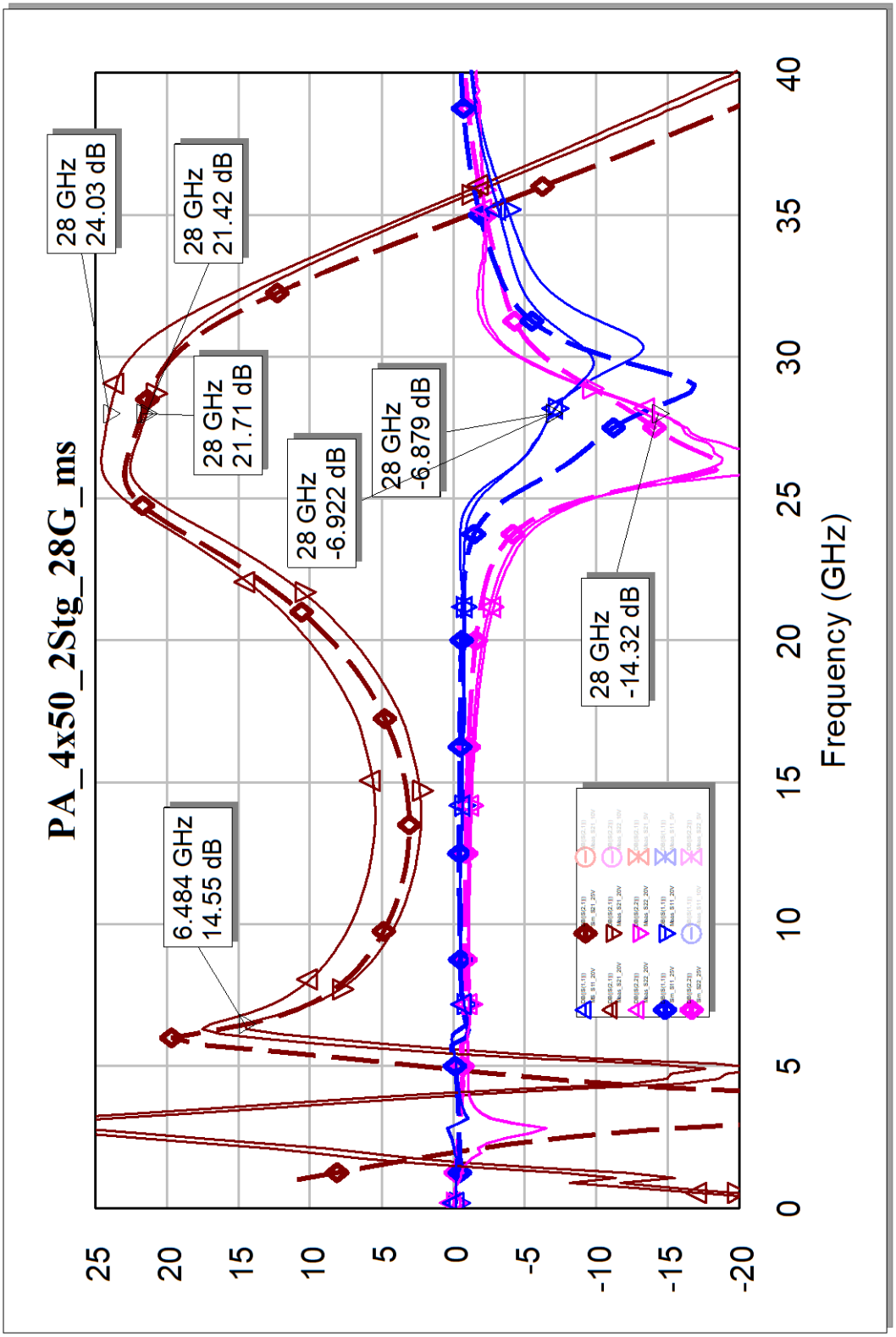

Fig. 11 Measured (solid) vs. simulation (dash) two-stage 4- × 50-µm, 4- × 50-µm PA (20 V, 28 V)

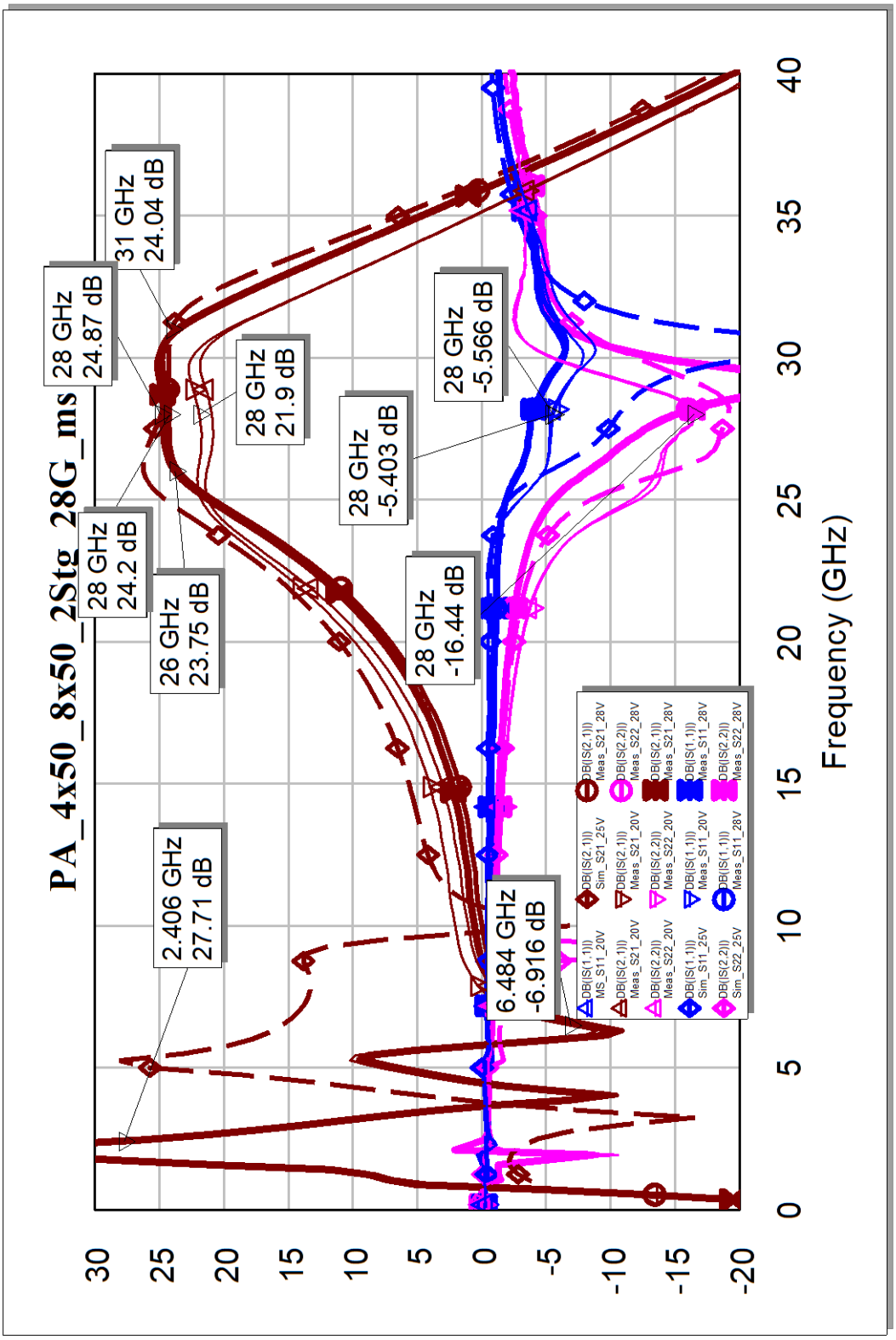

Fig. 12 Measured (solid) vs. simulation (dash) two-stage 4- × 50-µm, 8- × 50-µm PA (20 V, 28 V)

Power measurements of the one-stage PAs were performed at 20 V and 28 V. Figure 13 shows output power (blue), power-added efficiency (PAE; magenta), and gain (brown) in measured (solid) versus simulation (dash) plots of the of the 4- × 50-μm PA at the nominal 20-V DC bias and at frequencies around 28 GHz (see Fig. 13's legend). The small signal gain is a little low, possibly because the currents were about 75 mA/mm instead of the nominal 100–150 mA/mm. PAE is rising when it reaches 29% and has not started to peak or roll off, while still below the expected 37%–40% peak. Measured output power achieves 1/3 W, which is lower than expected, but the measured PA has not yet reached the same compression level. Similarly, Fig. 14 shows output power (blue), PAE (magenta), and gain (brown) in measured (solid) versus simulation (dash) plots of the 4- × 50-μm PA at the desired 28-V DC bias and at frequencies around 28 GHz (see legend). PAE is rising when it reaches 30% and has not started to peak or roll off, while still below the simulated 31%–35% peak. Measured output power achieves the 1/2-W goal (27 dBm), which is still lower than simulated, but has not yet reached the same compression level.

For the larger 8- × 50-μm one-stage PA, Fig. 15 shows output power (blue), PAE (magenta), and gain (brown) in measured (solid) versus simulation (dash) plots of the 4- × 50-μm PA at the nominal 20-V DC bias and at frequencies around 28 GHz (see legend). Measured output power achieves 1 W, while PAE peaks at 30%–31%—well below the expected 35%–42% peak. Figure 16 shows output power (blue), PAE (magenta), and gain (brown) in measured (solid) versus simulation (dash) plot of the 8- × 50-μm PA at the desired 28-V DC bias and at frequencies around 28 GHz (see legend). Measured output power achieves 1.45 W, well above the 1-W goal, and a peak PAE of 34% is very good, though slightly below simulations. For the two-stage PAs the output powers should match the single-stage PA measurements, but the PAE will be lower because DC power is needed to drive the first stage, cutting into overall two-stage amplifier PAE but adding 12 dB more gain. Simulations match well with measured results for the two-stage 4- × 50-μm PA, especially at the design DC bias of 28 V.

Figure 17 shows output power (blue), PAE (magenta), and gain (brown) in measured (solid) versus simulation (dash) plots of the power performance of the two-stage 4- × 50-μm PA at the nominal 20-V DC bias and at frequencies around 28 GHz (see legend). Likewise, Fig. 18 shows a similar plot at a 28-V DC bias, achieving an output power of 0.7 W at a peak PAE of 27%. For the larger two-stage 4- × 50-μm driving an 8- × 50-μm two-stage PA, simulations match well with measured results, especially at the design DC bias of 28 V. Figure 19 shows output power (blue), PAE (magenta), and gain (brown) in measured (solid) versus simulation (dash) plots of the power performance of the two-stage 4- × 50-μm PA

at the nominal 20-V DC bias and at frequencies around 28 GHz (see legend). Likewise, Fig. 20 shows a similar plot at a 28-V DC bias, achieving an output power of 1.5 W at a peak PAE of 30%.

The power amplifiers worked well with more than 20-dB small signal gain for the two-stage amplifiers over several GHz of bandwidth around 28 GHz. Nonlinear models predicted the measured results reasonably well, particularly at 28 V. The output power goals of 1/2 W and 1 W were achieved with 0.7-W peak for the 4- × 50-μm PA and 1.4 W for the 8- × 50-μm PA (28 V). DC bias affects the measured results at 20 V more than expected, as the gain tended to shift lower in frequency, while the nonlinear model predicted a similar shift if operated at an even lower DC bias by several volts.

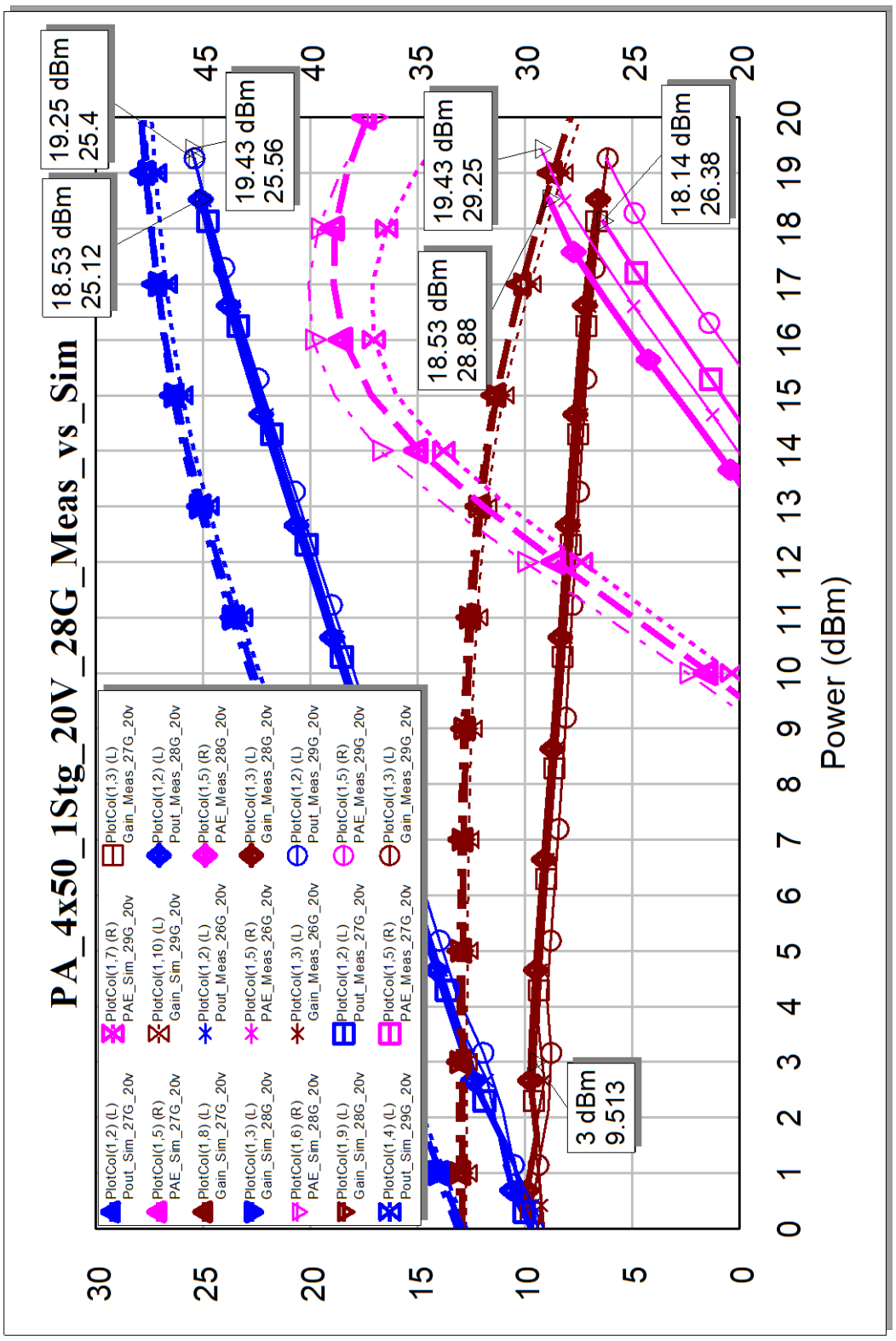

Fig. 13 Measured (solid) vs. simulation (dash) one-stage 4- × 50-µm PA (20 V)

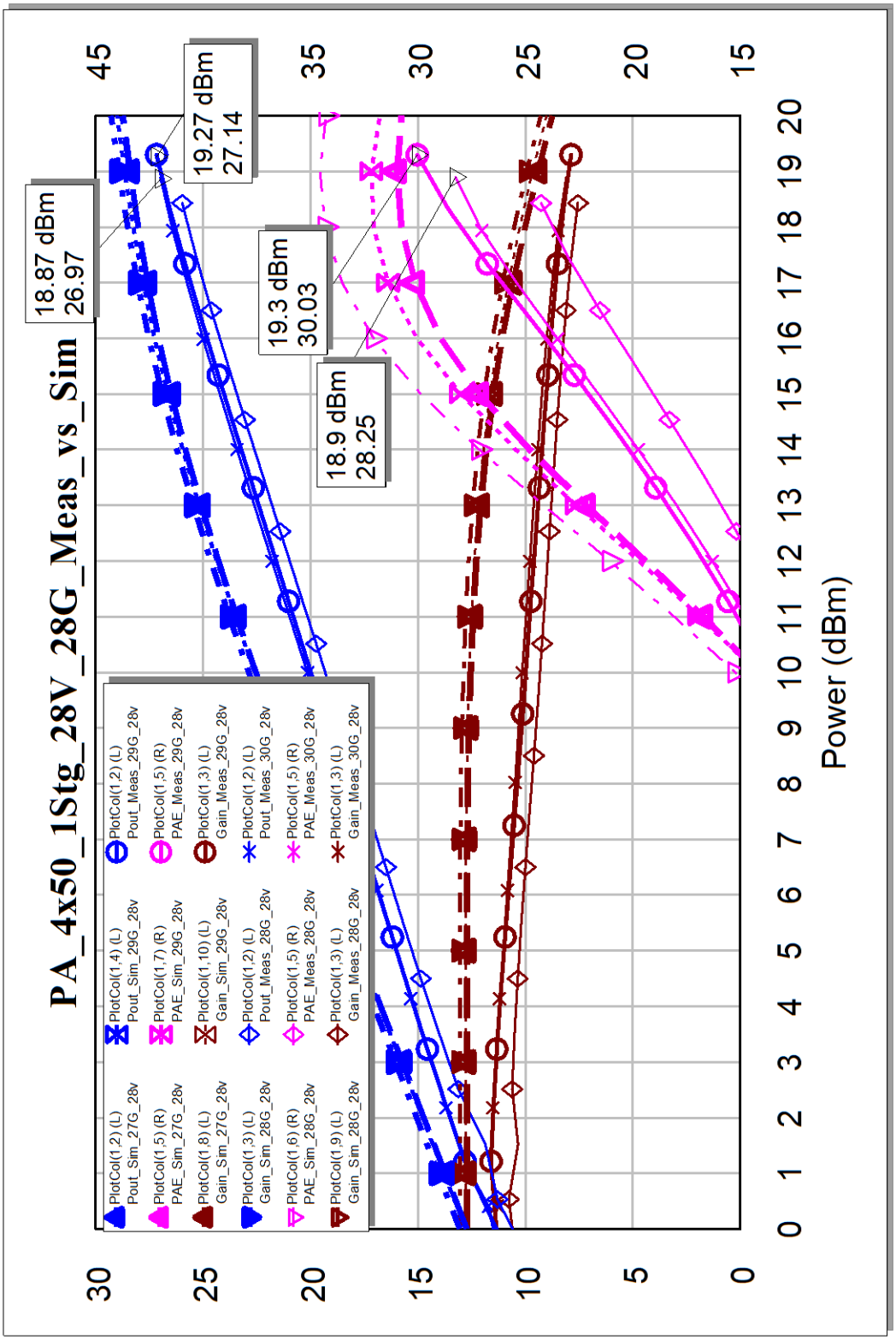

Fig. 14 Measured (solid) vs. simulation (dash) one-stage 4- × 50-µm PA (28 V)

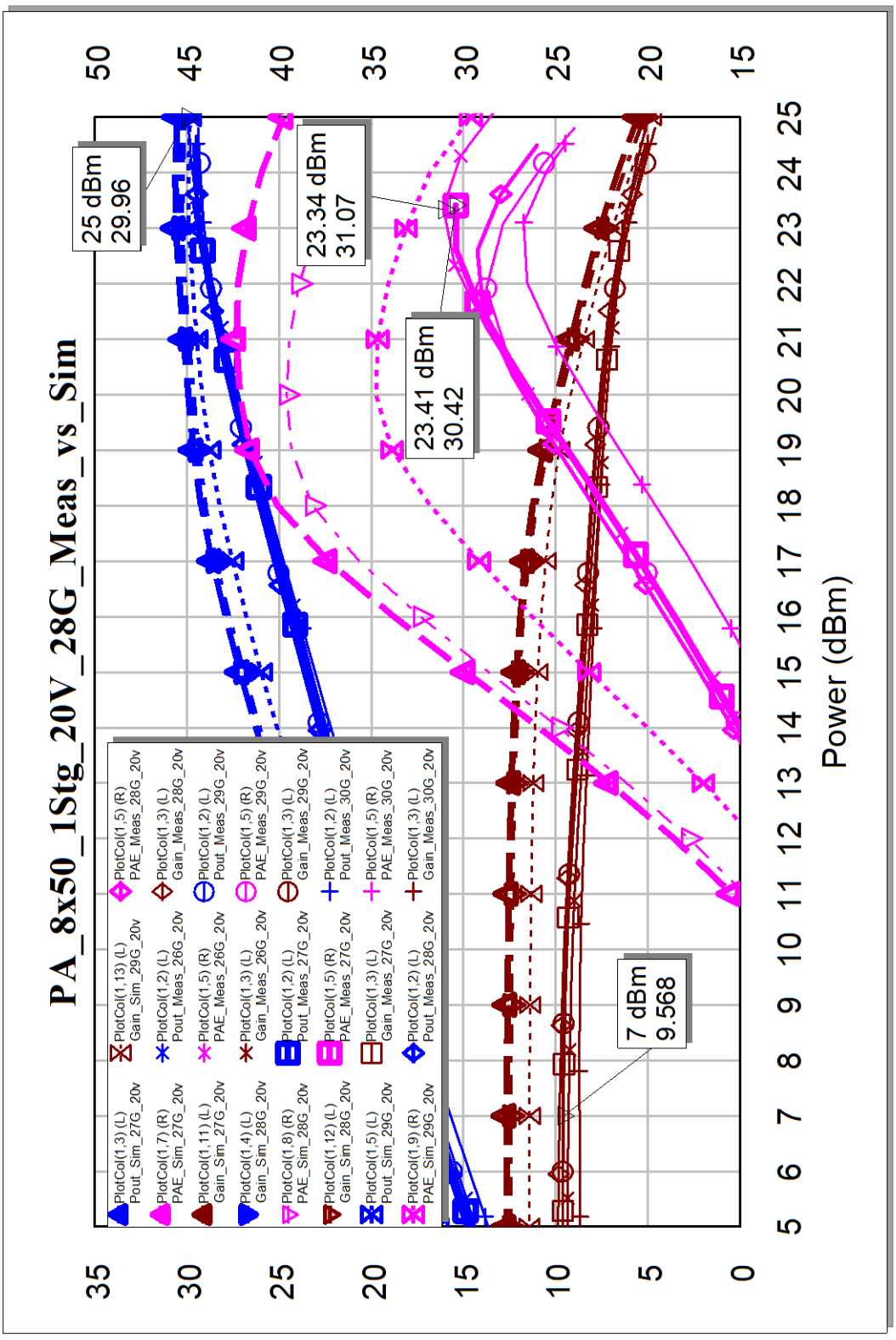

Fig. 15 Measured (solid) vs. simulation (dash) one-stage 8- × 50-µm PA (20 V)

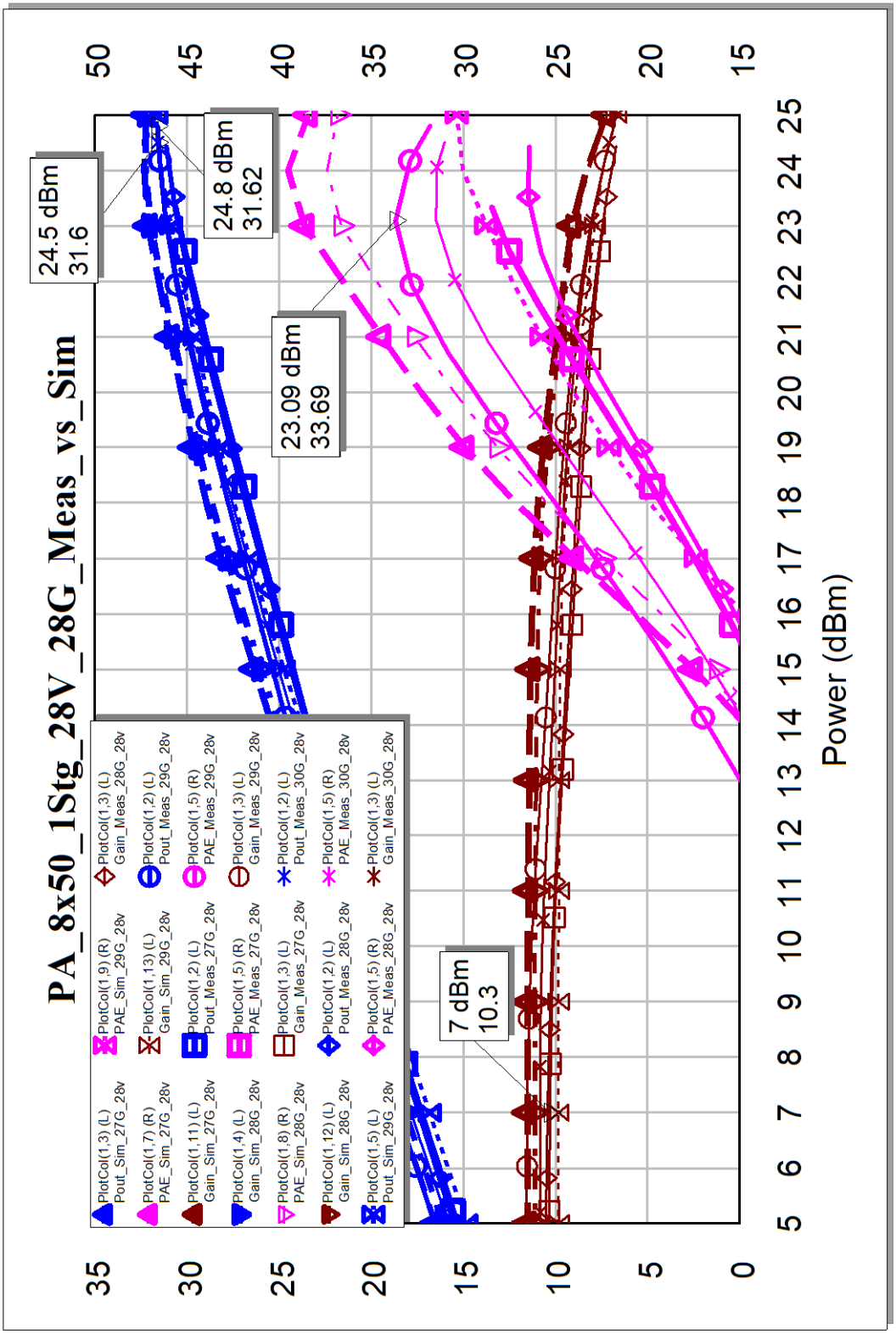

Fig. 16 Measured (solid) vs. simulation (dash) one-stage 8- × 50-µm PA (28 V)

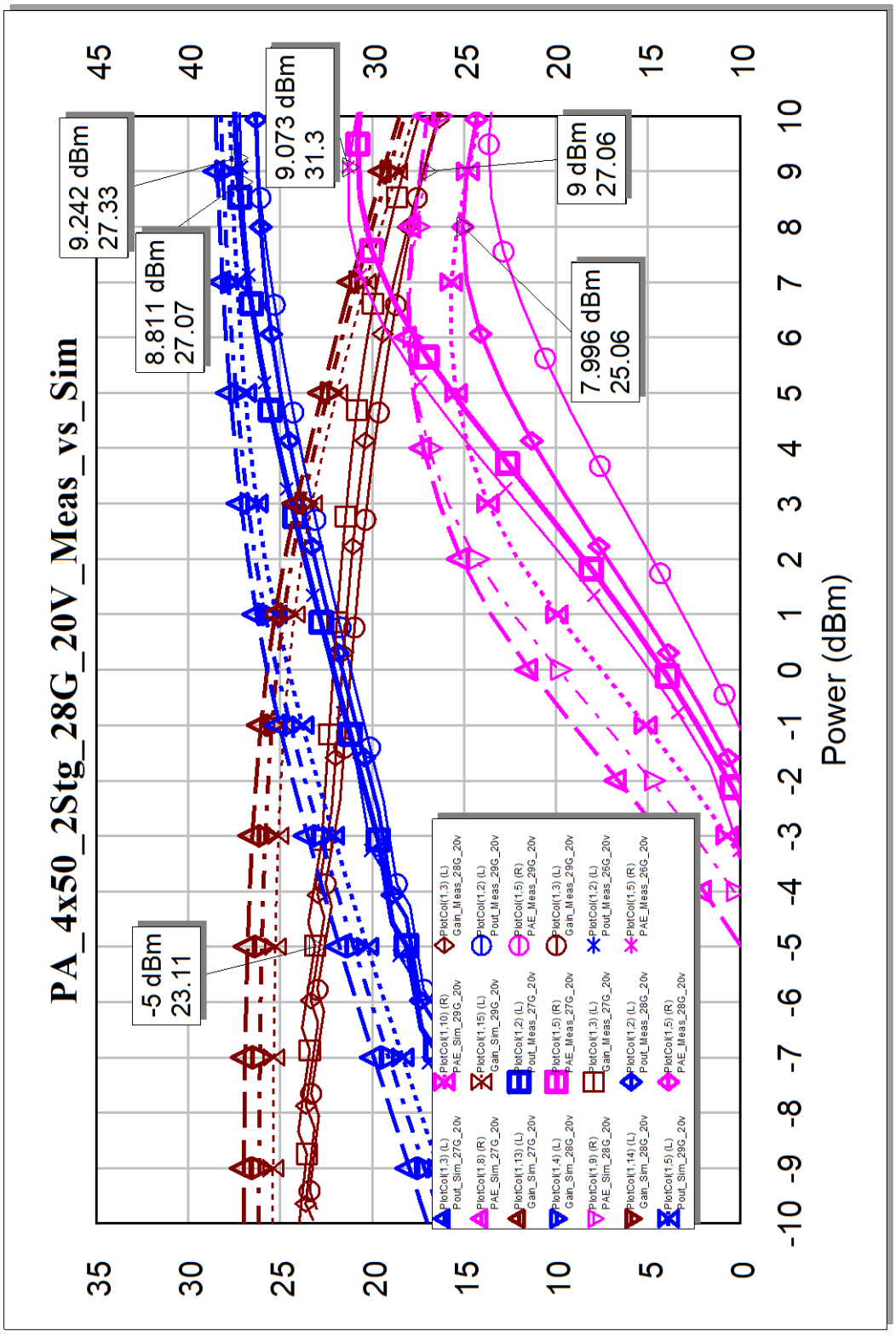

Fig. 17 Measured (solid) vs. simulation (dash) two-stage 4- × 50-µm PA (20 V)

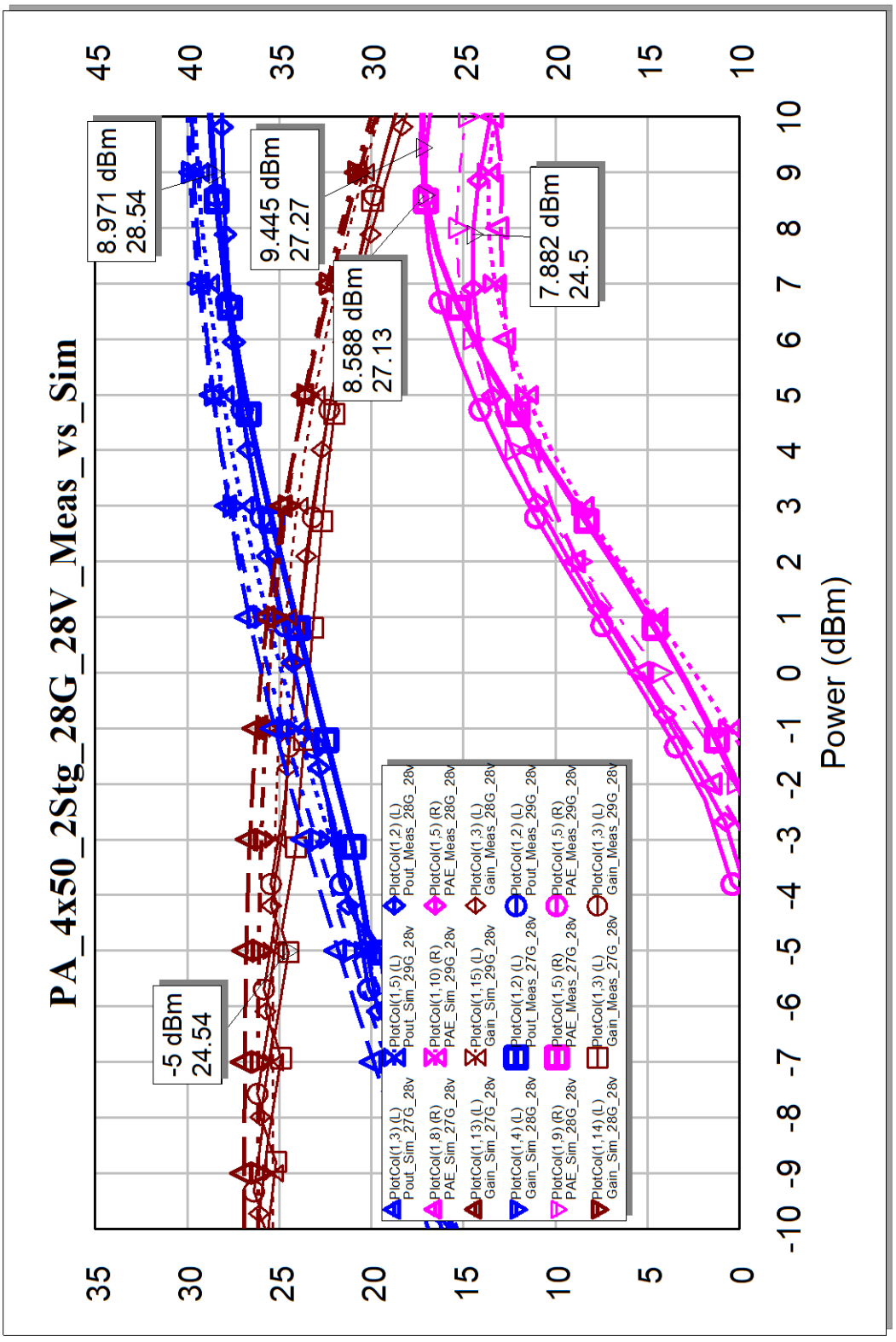

Fig. 18 Measured (solid) vs. simulation (dash) two-stage 4- × 50-µm PA (28 V)

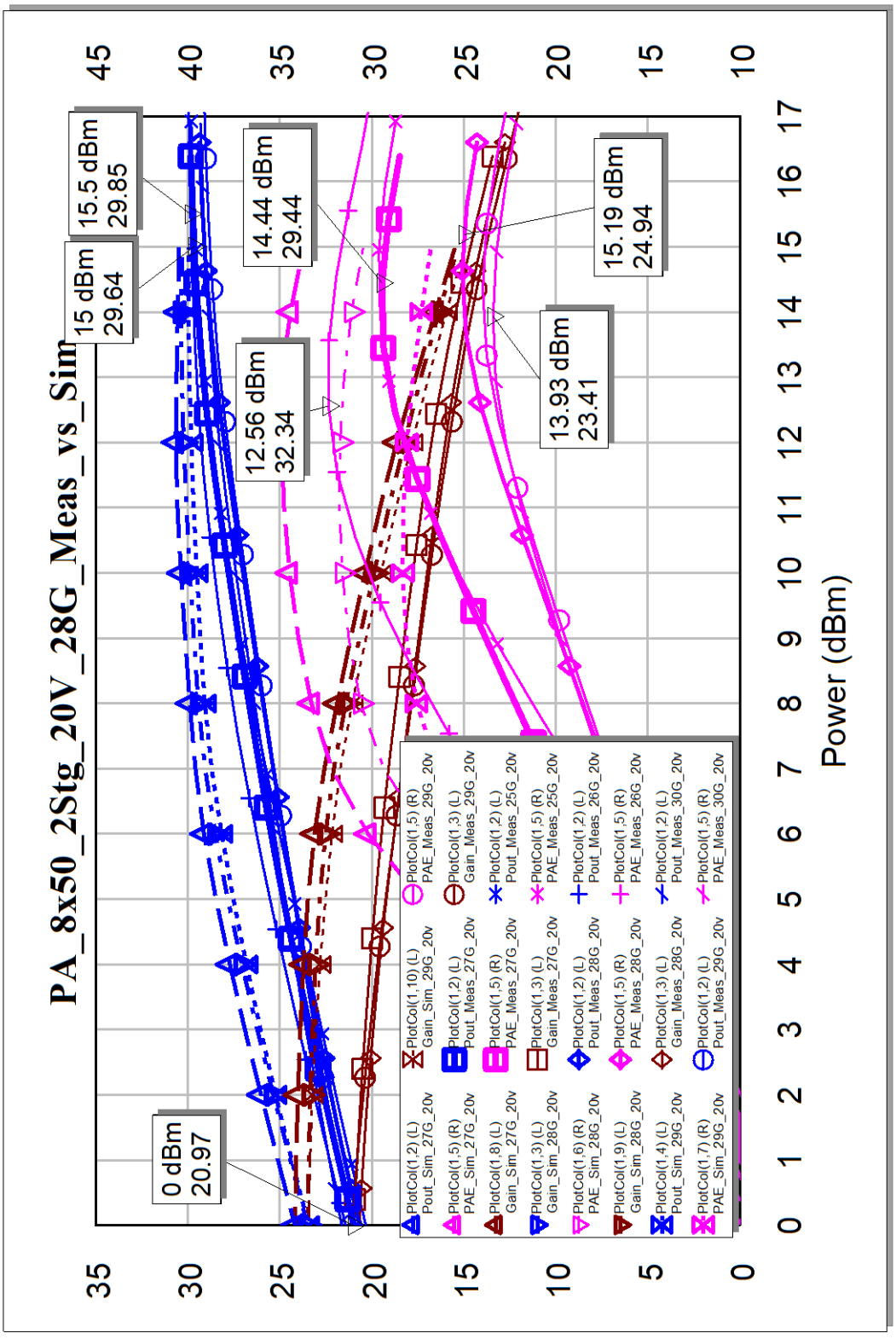

Fig. 19 Measured (solid) vs. simulation (dash) two-stage 8- × 50-µm PA (20 V)

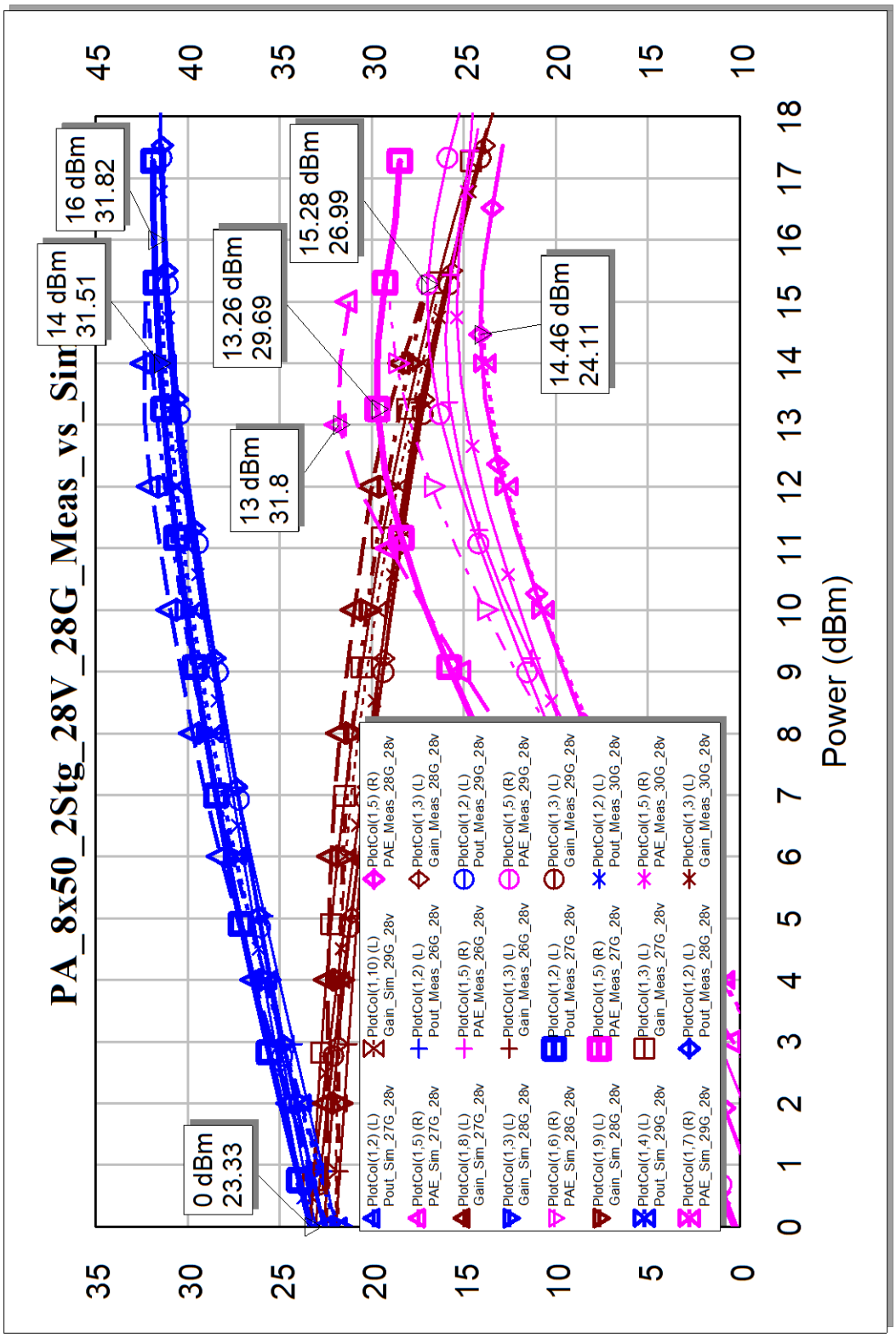

Fig. 20 Measured (solid) vs. simulation (dash) two-stage 8- × 50-µm PA (28 V)

4. Switches

An earlier ARL T/R switch design in 0.25-μm GaN was intended to operate up to 18 GHz, but its topology would not be sufficient for Ka-band operation. In these Ka-band T/R switch designs, the parasitic capacitance of the switch HEMTs was compensated for by adding parallel monolithic microwave integrated circuit (MMIC) inductors to provide several gigahertz of bandwidth around 28 GHz. The first single-pull double-throw (SPDT) switch used shunt (0.2-mm) and series (0.35-mm) HEMTs with parallel MMIC inductors to compensate for the capacitance. Each switch has three ports that were measured with a 2-port network analyzer, with the third port terminated with an uncalibrated 50-Ω load. Figure 21 shows the "ON" state, simulated (dash/dot) versus measured (solid) small-signal performance for this switch design, where the measured insertion loss of 1.3–1.4 dB at 28 GHz agrees well with the original linear switch models. Figure 22 shows the "OFF" state, simulated (dash/dot) versus measured (solid) small-signal performance for this switch design, where the measured isolation (brown) is more than 20 dB across the band centered at 28 GHz. The measurements agree well with the simulations, which was a pleasant surprise for a first-pass success given the compensating spiral inductors are comparable in size to the HEMT devices in this very high-frequency design.

For the second SPDT switch design, shunt (0.2-mm) HEMTs were used with 1/4-wave equivalent, 50-Ω microstrip lines. The layout was compacted by shortening the microstrip 1/4-wave line lengths by adding shunt capacitances to offset an increased line impedance. Figure 23 shows the Switch no. 2 "ON" state, simulated (dash/dot) versus measured (solid) small-signal performance for this switch design, where the measured insertion loss of 1.5 dB minimum (25 GHz) and 1.8 dB at 28 GHz agrees reasonably well with the original linear switch models. Figure 24 shows the "OFF" state, simulated (dash/dot) versus measured (solid) small-signal performance for this switch design, where the measured isolation (brown) is only about 15 dB best-case across the band. The performance of this switch looks as if it shifted down a little from the desired band but is very close in comparison to simulations. The tradeoff among size, complexity, and performance makes this single-shunt switch Design no. 2 similar in insertion loss to the series/shunt switch Design no. 1 and size, but the isolation is not as good as the series/shunt design.

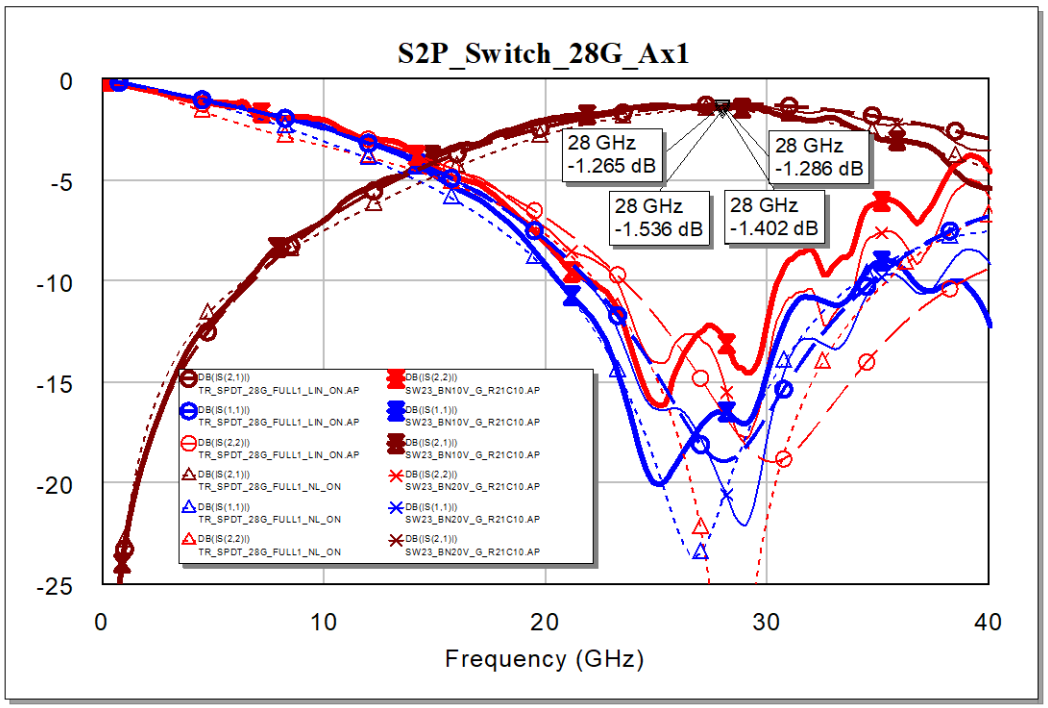

Fig. 21 Measured (solid) vs. simulation (dash) T/R Switch no. 1 "ON"

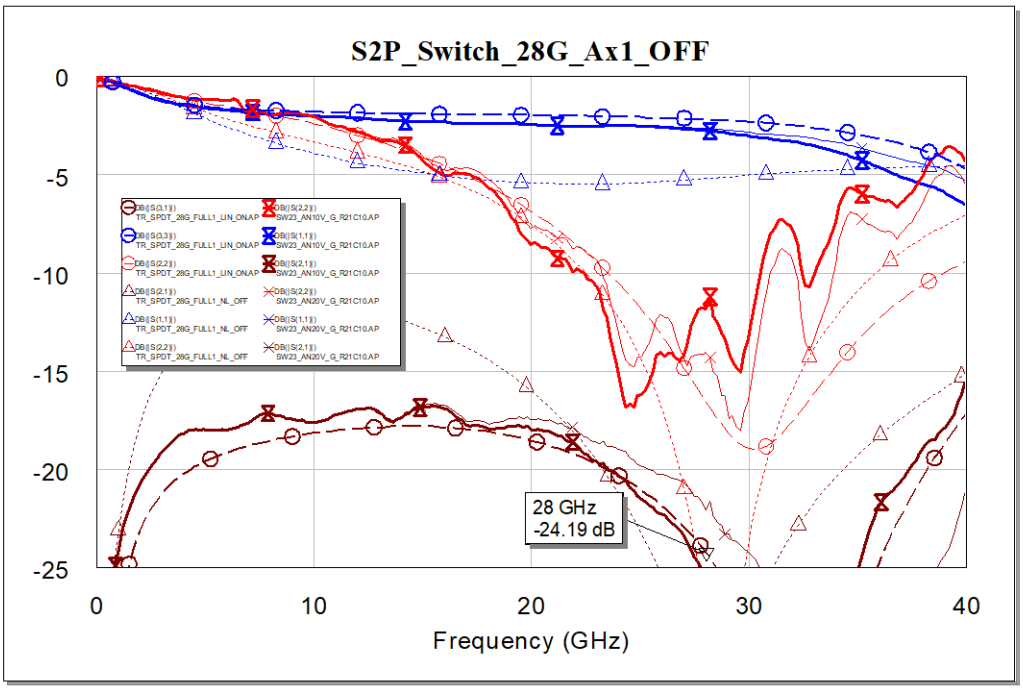

Fig. 22 Measured (solid) vs. simulation (dash) T/R Switch no. 1 "OFF"

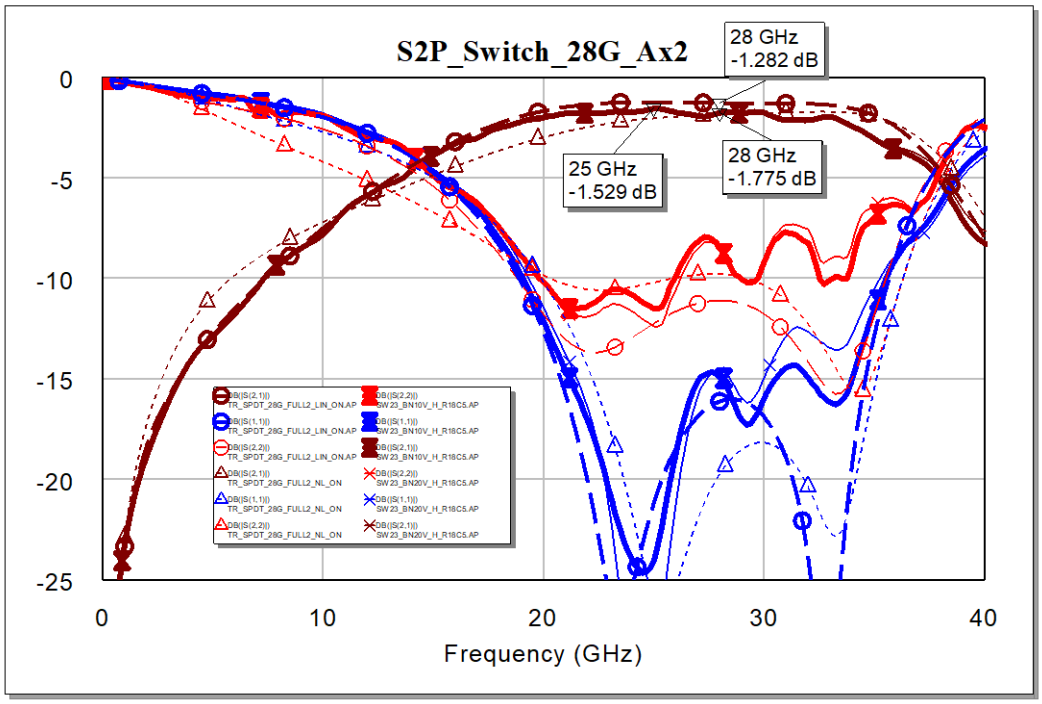

Fig. 23 Measured (solid) vs. simulation (dash) T/R Switch no. 2 “ON”

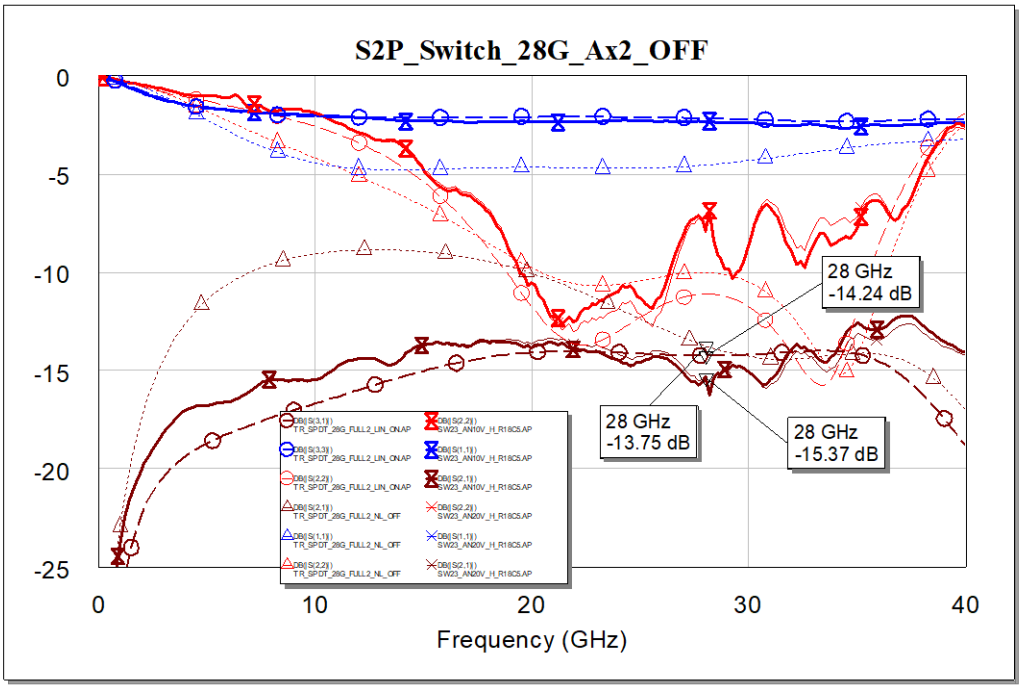

Fig. 24 Measured (solid) vs. simulation (dash) T/R Switch no. 2 “OFF”

5. Ka-Band T/R Modules 1, 2, and 3: SPDT T/R Switch, PA, and LNA

The first complete Ka-band T/R front end (TRS1) combines the two-stage 8- × 50-μm PA, the two-stage LNA, and one SPDT series/shunt (SPDT–SS) switch as shown in the die photo of Fig. 25. This layout has a common "antenna" connection, an input for the LNA path, and an output for the PA path. The series/shunt design has better isolation than the SPDT shunt-only (SPDT–SO) switch, and when in the receive mode requires the PA is off (DC bias off) and when in the transmit mode requires the LNA is off (DC bias off).

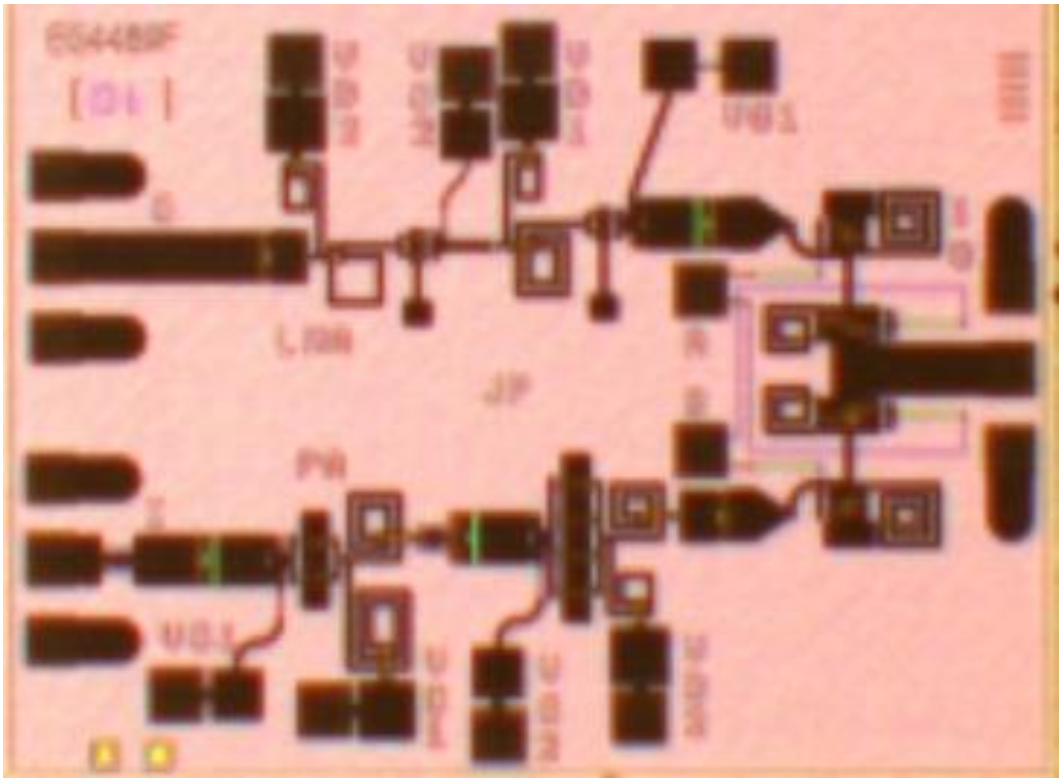

Fig. 25 Die photo of T/R Module 1: SPDT–SS, PA, and LNA

A second Ka-band T/R front end (TRS2) combines the two-stage 8- × 50-μm PA, the two-stage LNA, and two SPDT–SO switches as shown in the die photo of Fig. 26. This layout has two common connections, which change the signal flow direction right to left for the LNA path and left to right for the PA path, as shown. The SPDT–SO switch requires that the PA is off (DC bias off) in the receive mode and that the LNA is off (DC bias off) in the transmit mode.

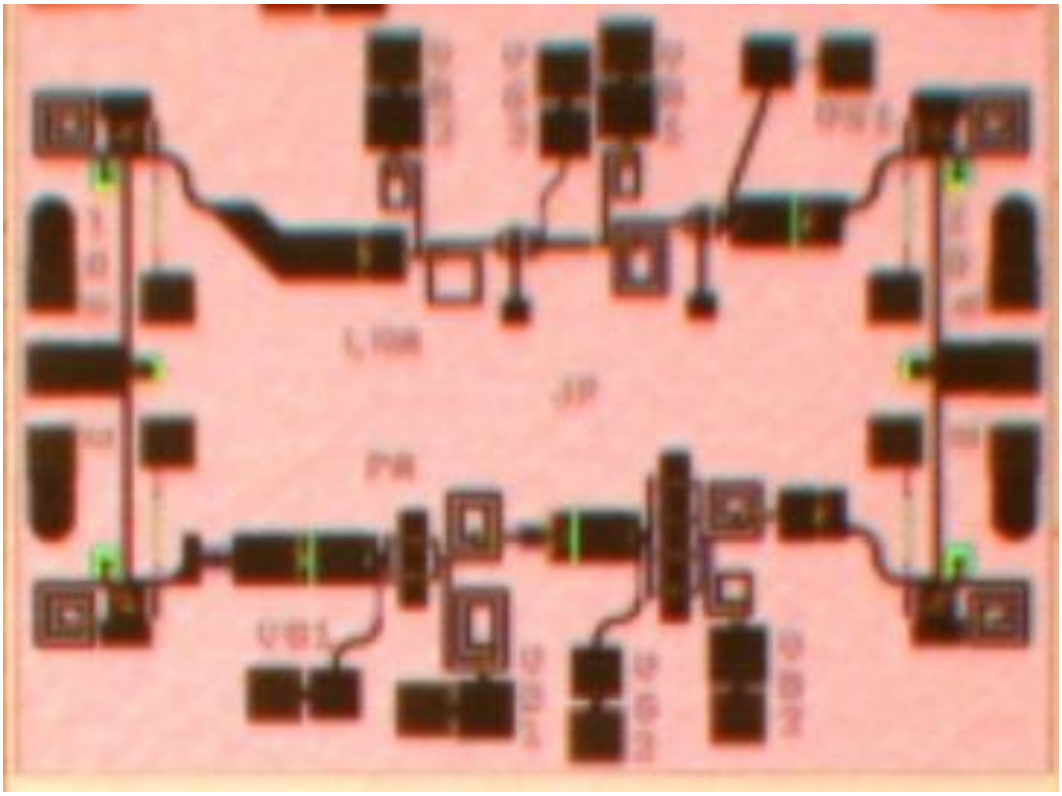

Fig. 26 Die photo of T/R Module 2: two SPDT–SO's, PA, and LNA

The third complete Ka-band T/R front end (TRS3) combines the two-stage 8- × 50-μm PA, the two-stage LNA, and two SPDT–SS switches as shown in the die photo of Fig. 27. This layout has two common connections, which change the signal flow direction right to left for the LNA path and left to right for the PA path as shown. The SPDT–SS has better isolation than the SPDT–SO switch, and while in the receive mode requires the PA is off (DC bias off) and in the transmit mode requires the LNA is off (DC bias off).

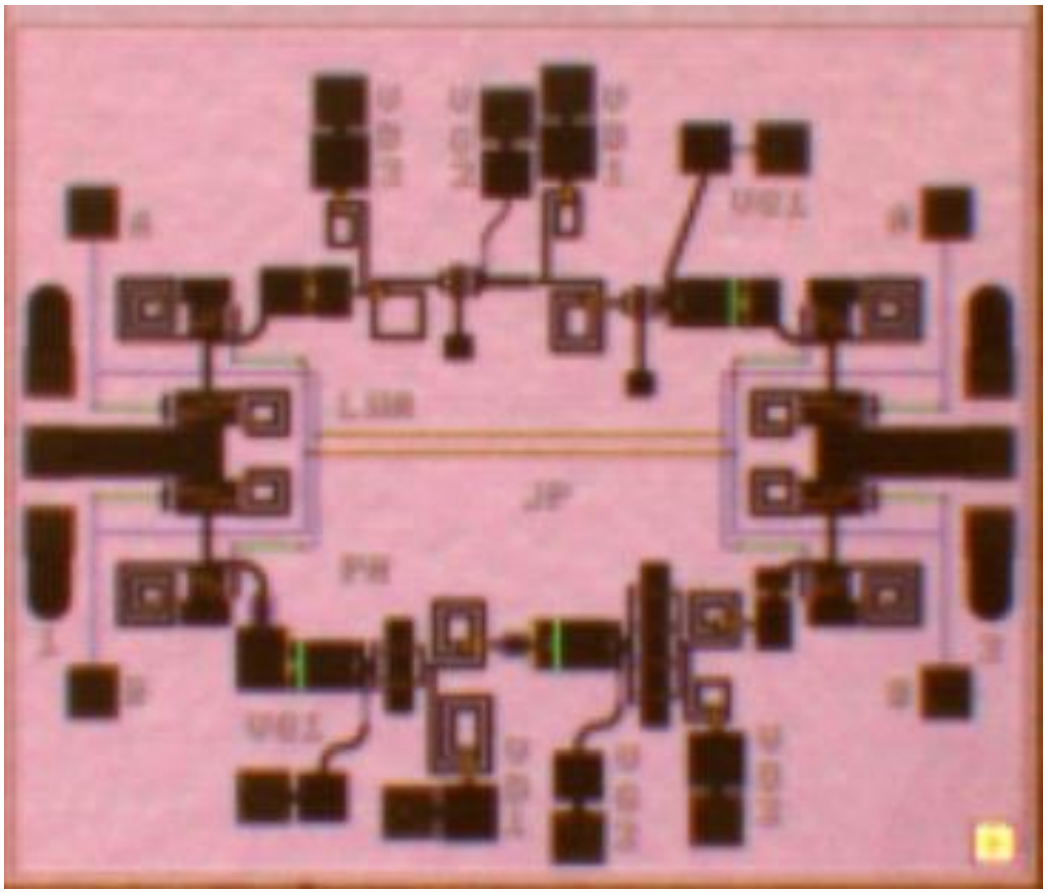

Fig. 27 Die photo of T/R Module 3: two SPDT–SS's, PA, and LNA

Several versions of the T/R module were fabricated. The first architecture is common, with a single switch to toggle between receive and transmit modes. In the receive mode, the loss of the SPDT switch adds to the noise figure as it is loss in front of the LNA. Likewise, in the transmit mode the loss of the switch reduces the output power, which also reduces the effective efficiency (PAE). The SPDT was designed for reasonable insertion loss over several GHZs of bandwidth around 28 GHz with the power-handling goal of 1.5 W or more using GaN HEMTs as the switch devices.

The second and third T/R module versions use two SPDT switches for a common input/output and bidirectional amplification. As with the first version, the loss of two switches will affect the overall gain in both directions, but the most significant loss of performance will be due to the single-switch loss at the input of the LNA, which also affects the output of the PA. Version 2 of the T/R module uses the SPDT–SO switch design and Version 3 uses the SPDT–SS design. Control of the A and B switch inputs will operate the T/R modules in receive or transmit mode. Since the gate currents of HEMTs are virtually zero mA, the A and B signals for both switches on the left and right of the layout in TRS3 are connected together so

that one can drive both switches from either of the two A and B DC bond pads. It would have simplified the operation of TRS2 as well if that same common connection of the two A and B DC bond pads had been connected within the die, but was overlooked in the design process. For testing, the common A and B switch pads were connected with wire bonds. The three module variations were tested in the receive (LNA) and transmit (PA) directions for comparison of performance.

The LNAs were designed for 10-V operation but could be operated at 5 V as well. There is a significant shift as the DC bias is increased from 5 V, 10 V, 20 V, and 28 V, though all of the amplifiers can operate over a large range of DC bias; the best bias is 10 V for the LNAs, with the typical 100-mA/mm to 150-mA/mm currents. Gain tended to increase as bias currents increased from 100 mA/mm to 150 mA/mm, with only a very slight increase from 150 mA/mm to 200 mA/mm. For these small two-stage LNAs with 4- × 25-μm HEMTs, nominal bias was 20 mA, with slightly better gain at 30 mA. Small signal simulations (dot/dash) of the receive mode (LNA) versus measurements (solid) for T/R Module 1 show broadband gain and match quite well within expected process variation and simulation accuracy (Fig. 28). Note the measurement at 8 V starts to shift down in frequency relative to the two 10-V measurements (20 mA and 30 mA), but is actually closer to the simulations (e.g., 10 V) achieving good broadband gain. Small signal simulations (dot/dash) of the receive mode (LNA) versus measurements (solid) for T/R Module 2 show broadband gain and match quite well at 10 V within expected process variation and simulation accuracy (Fig. 29). Note the good gain, which is lower than TR1's since we now have the loss of two SPDT switches. Also shown are measured results at 15 V showing gain starts to peak at each end of the band, showing less flatness than at the designed-for 10 V, but still works well.

Finally, small signal simulations (dot/dash) of the receive mode (LNA) versus measurements (solid) for T/R Module 3 show broadband gain and match quite reasonably well at 10 V within expected process variation and simulation accuracy (Fig. 30). This design peaks even more than the prior two versions, and measured results show the increasing uneven gain with increasing biases of 8 V, 10 V, 12 V, and 15 V. There may be some interaction with the parasitics of the switch, or layout, that is causing more of a resonance than expected. It is clear the single-switch version has the best comparison to simulations and has the best gain. All simulations for the LNA used the small signal linear models for the 4- × 25-μm HEMTs; large signal HEMT models for the small 4- × 25-μm and 6- × 25-μm HEMTs were considerably less accurate in predicting the small signal LNA performance, and possibly the nonlinear models were optimized for a fit at the higher 28-V bias of a PA. Next, small signal and then power performance measurements were performed for the transmit path (PA) in each of the three T/R modules.

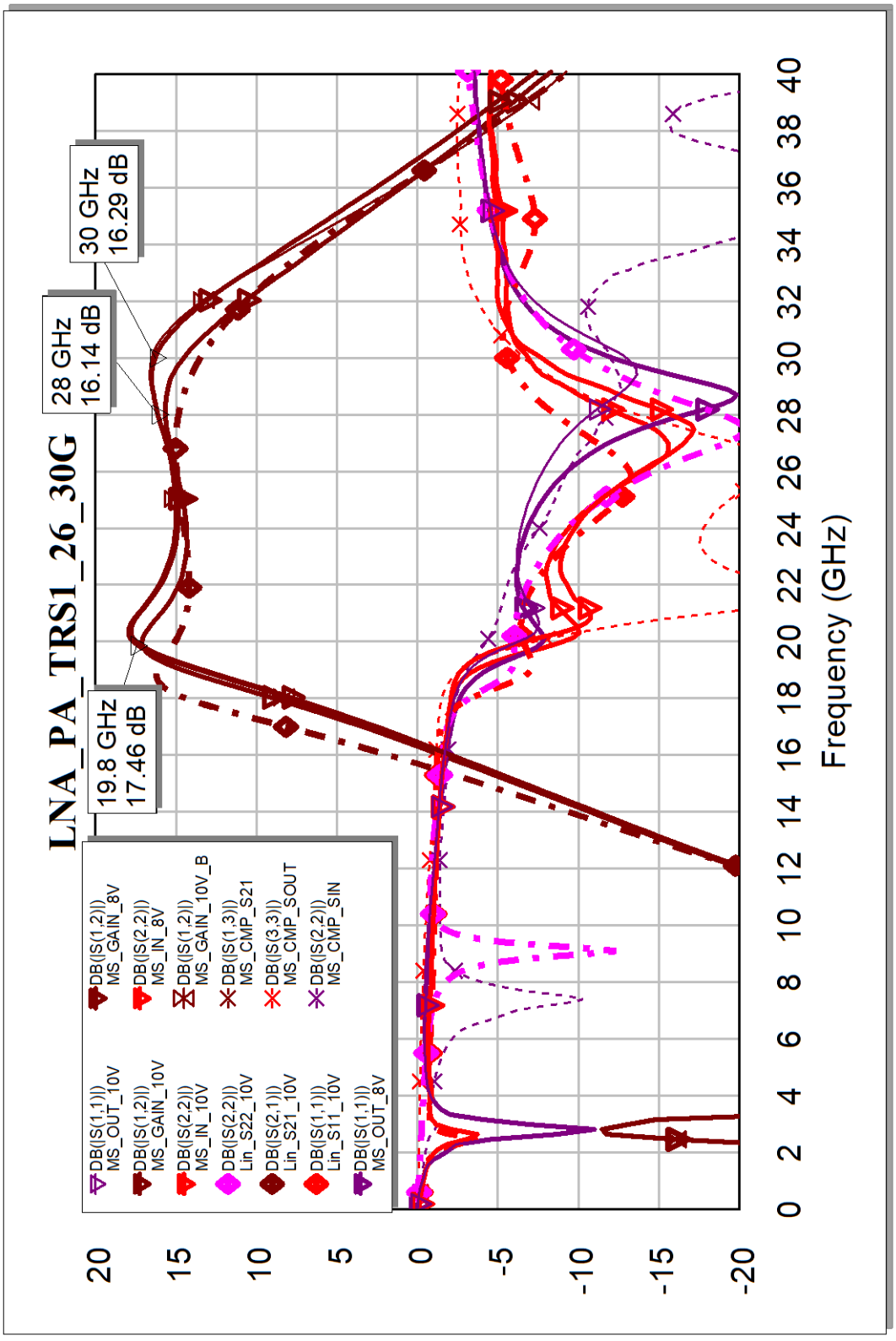

Fig. 28 Measured (solid) vs. simulation (dash) TRS1 LNA measured (10 V)

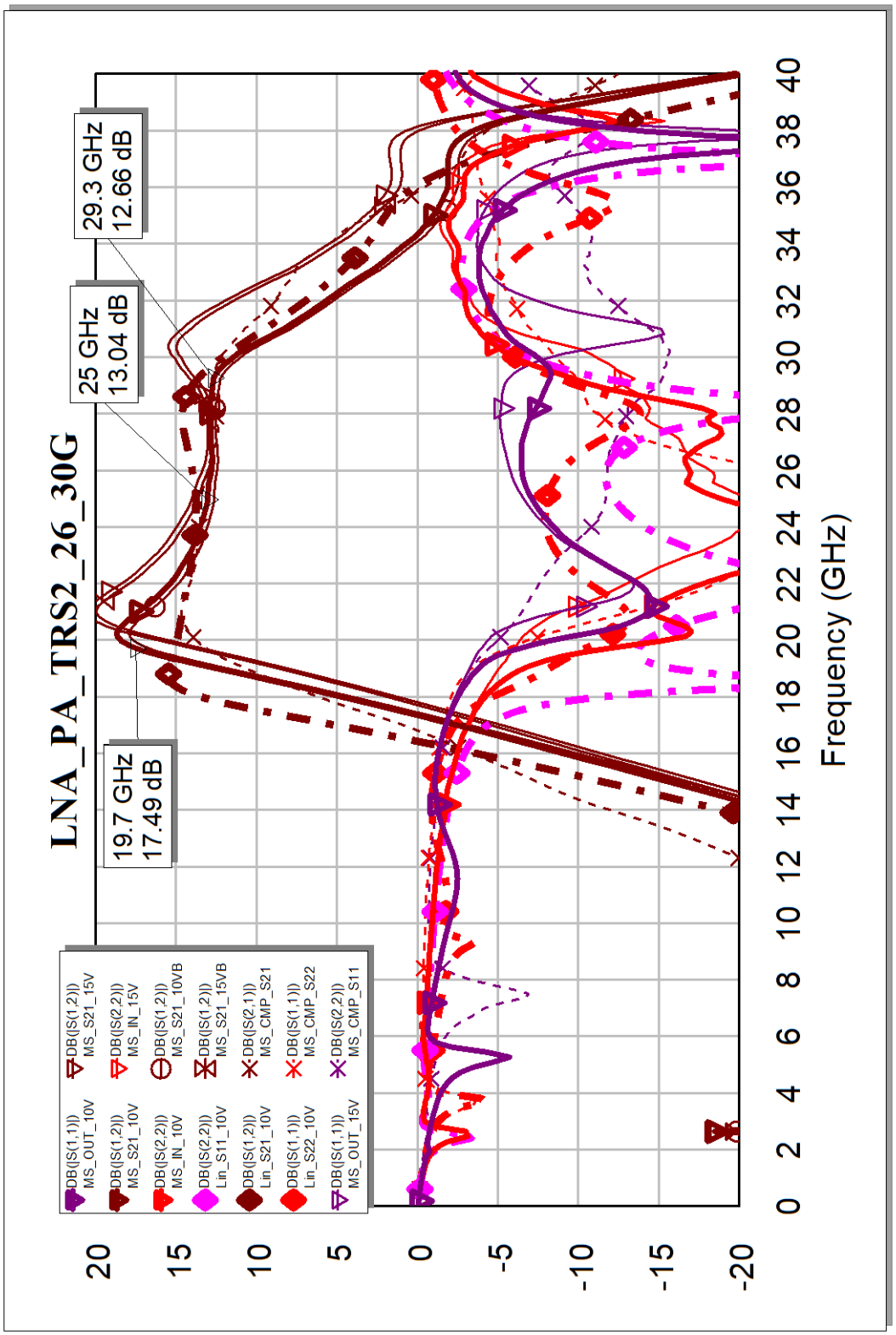

Fig. 29 Measured (solid) vs. simulation (dash) TRS2 LNA measured (10 V)

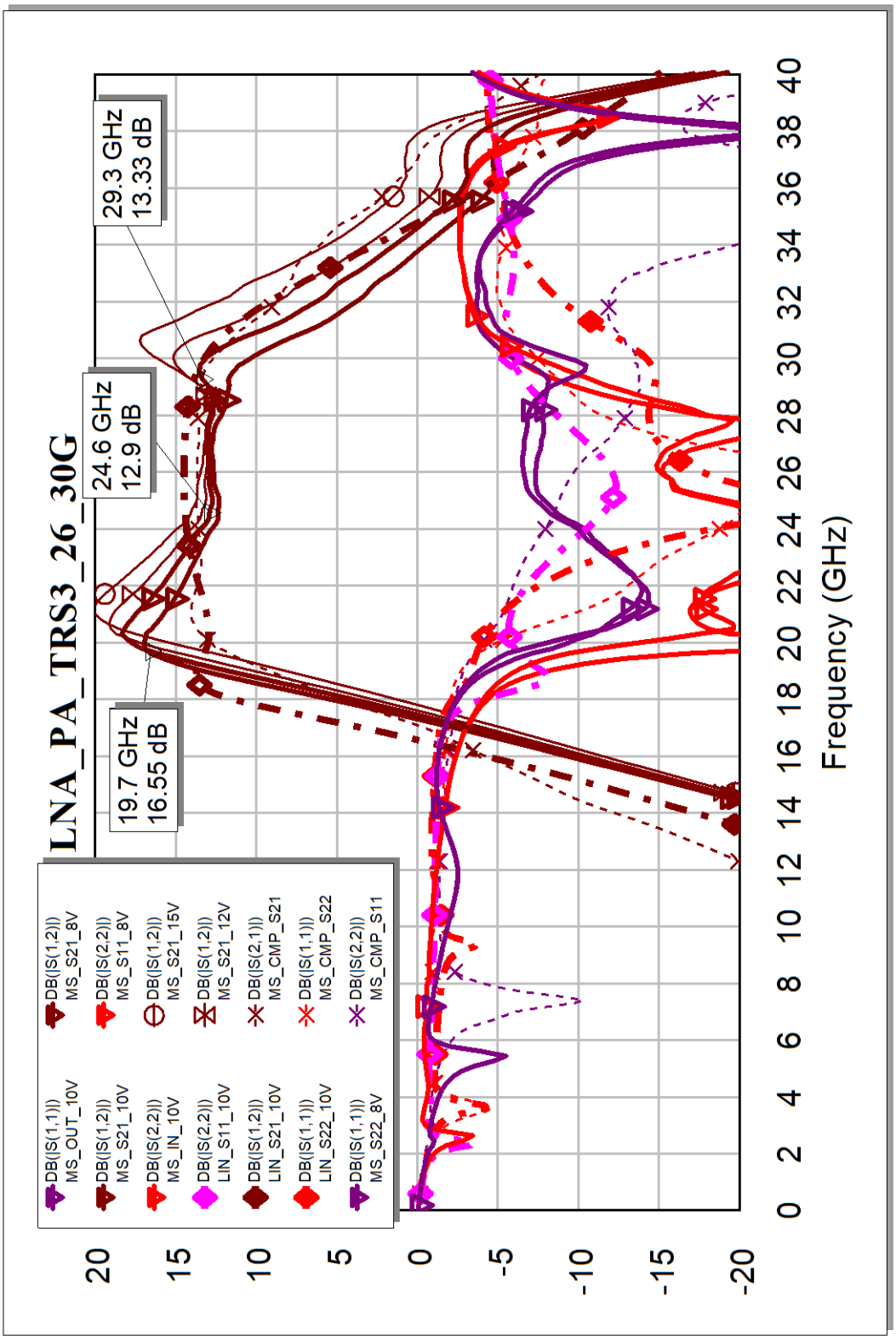

Fig. 30 Measured (solid) vs. simulation (dash) TRS3 LNA measured (10 V)

The PAs were designed for 28-V operation but could be operated at 20 V as well. As mentioned previously, there is a significant shift as the DC bias is increased from 5 V, 10 V, 20 V, and 28 V, though all of the amplifiers can operate over a large range of DC bias; the best bias is 28 V for the PAs, with the typical 100-mA/mm to 150-mA/mm currents. As noted, gain tended to increase as bias currents increased from 100 mA/mm to 150 mA/mm, with only a very slight increase from 150 mA/mm to 200 mA/mm. For these PAs with a 4- × 50-μm HEMT, plus an 8- × 50-μm HEMT, nominal bias was 60 mA, with slightly better gain at 90 mA. Small signal simulations (dot/dash) of the transmit mode (PA) versus measurements (solid) for T/R Module 1 show broadband gain and match quite well within expected process variation and simulation accuracy (Fig. 31), with best gain and match at 28-V bias. The small signal gain of the PA for the next two modules showed an unexpected dip in the gain, which could not be explained easily. A simulation based on cascading the s-parameters of the individual SPDT switch measurements with the PA measurements does not show this dip but does predict a slightly narrower bandwidth than initially predicted (dash lines with X in the next two figures are the cascaded s-parameter predictions based on individual SPDT and PA measurements).

While the gain bandwidths of the amplifiers and switches incorporating resonating parallel inductors are both good, any mismatch in the bandwidth centers will tend to narrow the composite bandwidth. This seems to explain the narrower bandwidth predicted by cascading measurements of the individual circuits. Still, the gain depression is unexplained; possibly, there are some unsimulated parasitics in the full layout that are not captured by EM-simulating individual pieces of the layout. Small signal simulations (dot/dash) of the transmit mode (PA) versus measurements (solid) for T/R Module 2 show a dip in the broadband gain and do not match as well as the previous module (Fig. 32), though the best gain is at 28V bias with poor input and output match. The gain dip is slightly less but also appears in the small signal measurements (solid) of the transmit mode (PA) shown versus simulations (dot/dash) for T/R Module 3 (Fig. 33); again, the best gain is at 28-V bias but the PA has poor input and output match.

Power performance was also measured around 28 GHz for T/R Modules 1 and 2—which have the gain dip that might be expected to drop performance dramatically. Measurements of T/R Module 3 were attempted but the data were not useful, and any additional measurements will be long delayed due to the current health crisis. Already, it is clear the single SPDT version has the best performance and comparison to simulations. Efficiency is sometimes higher at lower voltages, 20 V, while output power was often best at 28 V, as it was designed to be.

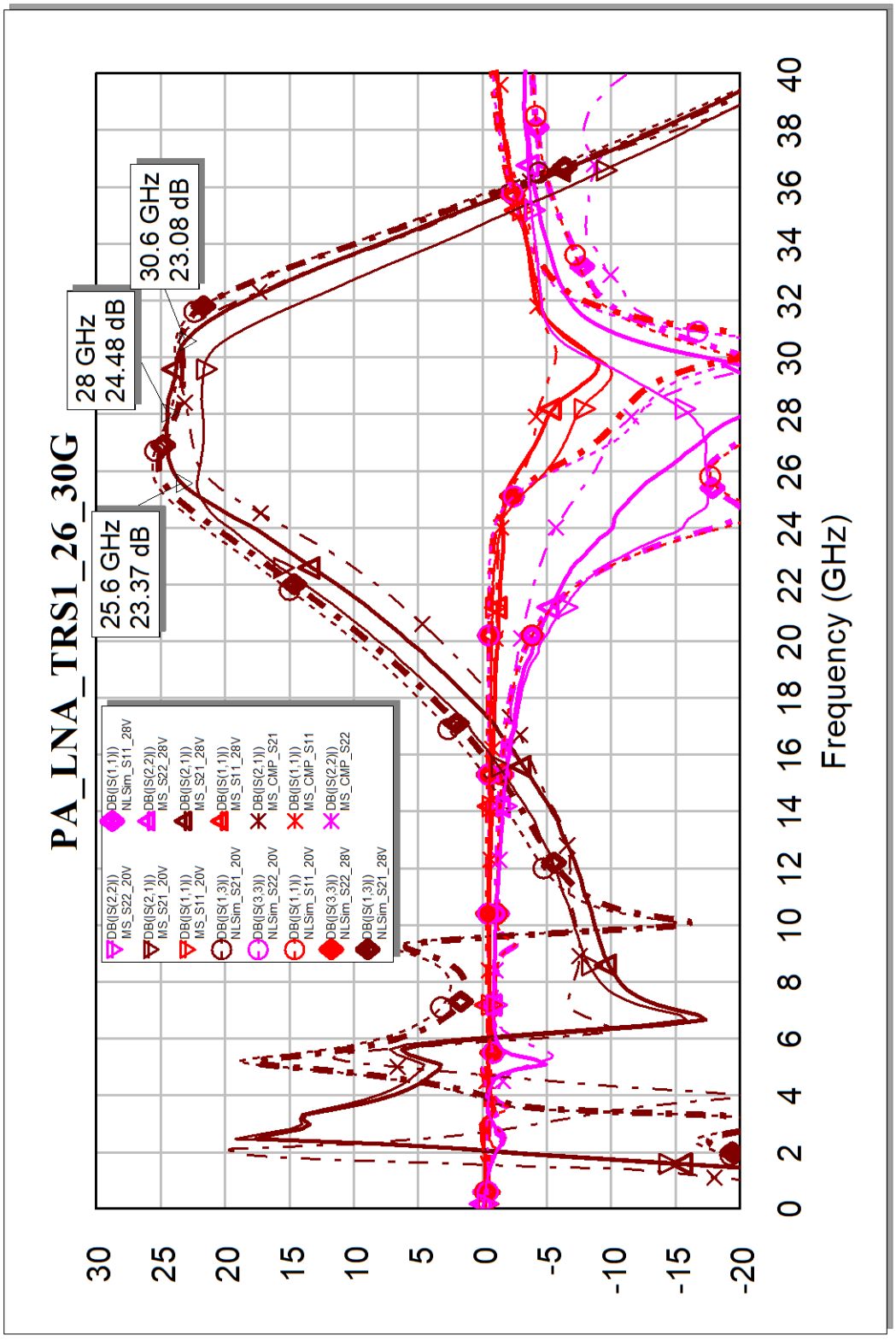

Fig. 31 Measured (solid) vs. simulation (dash) TRS1 PA measured (28 V)

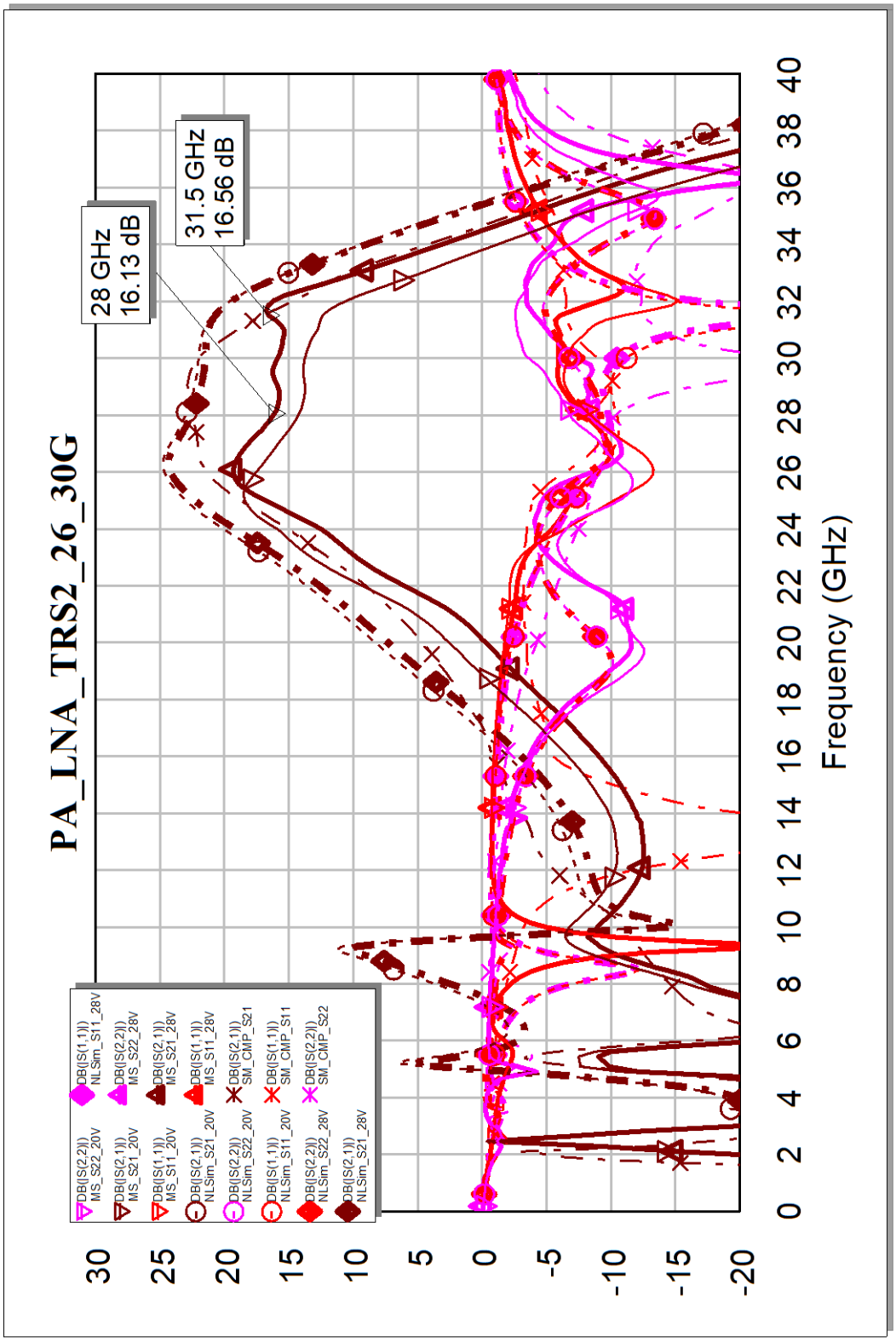

Fig. 32 Measured (solid) vs. simulation (dash) TRS2 PA measured (28 V)

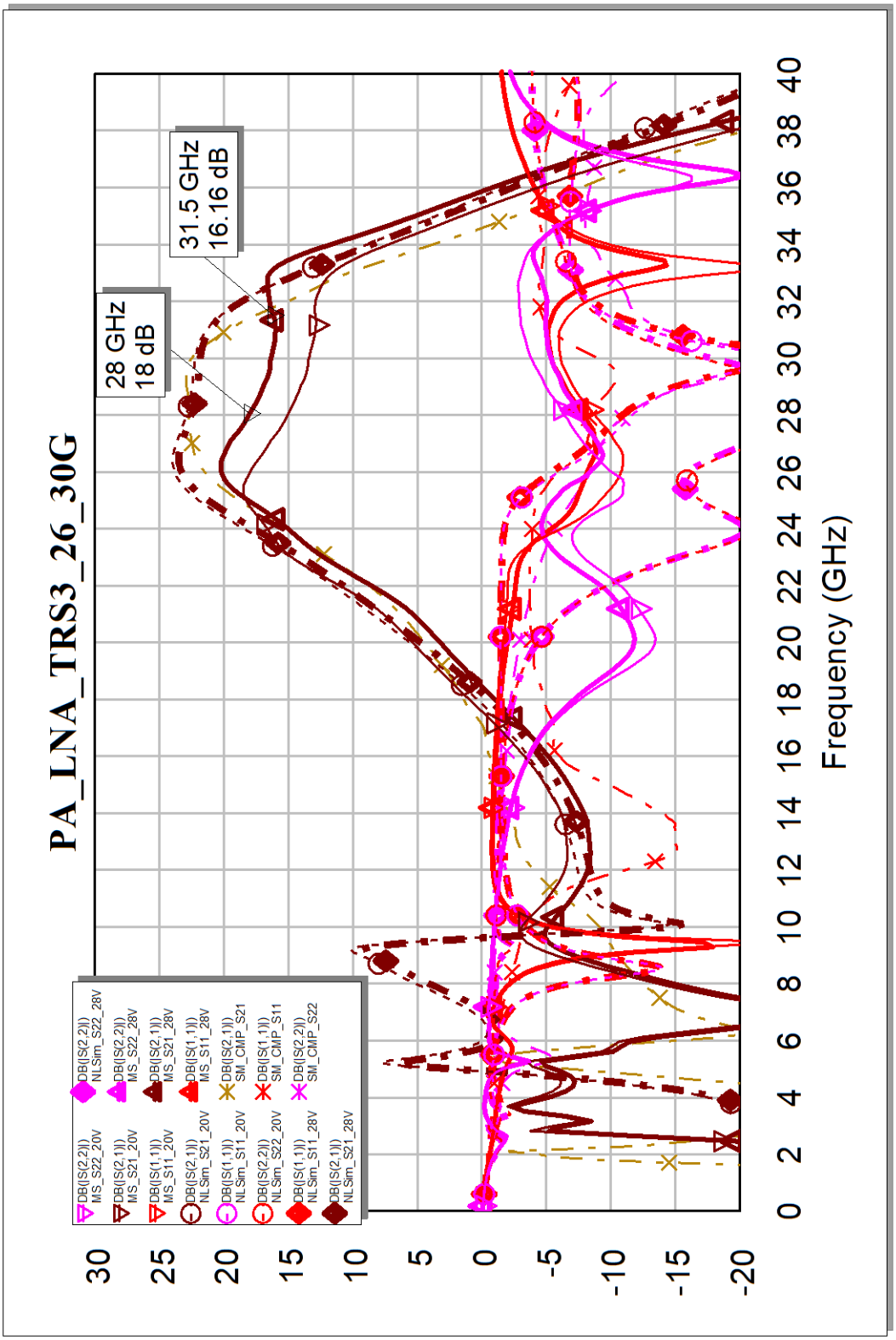

Fig. 33 Measured (solid) vs. simulation (dash) TRS3 PA measured (28 V)

Figure 34 shows output power (blue), PAE (magenta), and gain (brown) measured (solid) versus simulation (dash) in plots of power performance of the transmit mode (PA) of T/R Module 1 at the nominal 20-V DC bias and at frequencies around 28 GHz (see legend). Likewise, Fig. 35 shows a similar plot at a 28-V DC bias, achieving an output power of about 1 W at a peak PAE of 20%. The 1.5-dB insertion loss of the SPDT switch affects the PA performance and the result matches expectations, showing that the switch is actually handling 1.5 W of input power at the peak. Figure 36 shows output power (blue), PAE (magenta), and gain (brown) measured (solid) versus simulation (dash) in plots of power performance of the transmit mode (PA) of T/R Module 2 at the nominal 20-V DC bias and at frequencies around 28 GHz (see legend). Likewise, Fig. 37 shows a similar plot at a 28-V DC bias, achieving an output power of only 0.5 W at a peak PAE of 11%–15%. The prior gain dip in the small signal performance is showing more loss than the typical 1.5-dB insertion loss of the SPDT switch, which affects the PA performance. The performance loss is higher than predicted; a full EM simulation of the entire layout may help eliminate the possibility of unexpected parasitic coupling. There seems to be more interaction of the SPDT switches and PA in module Versions 2 and 3. At least Module 1 is performing as expected; there are some lessons to be learned before a second-iteration design would be performed on the Ka-band modules with SPDT switches common to a bidirectional LNA and PA combination. Unfortunately, noise-figure measurements have not been performed yet on the individual LNAs or T/R modules; those will be delayed, possibly for a future report.

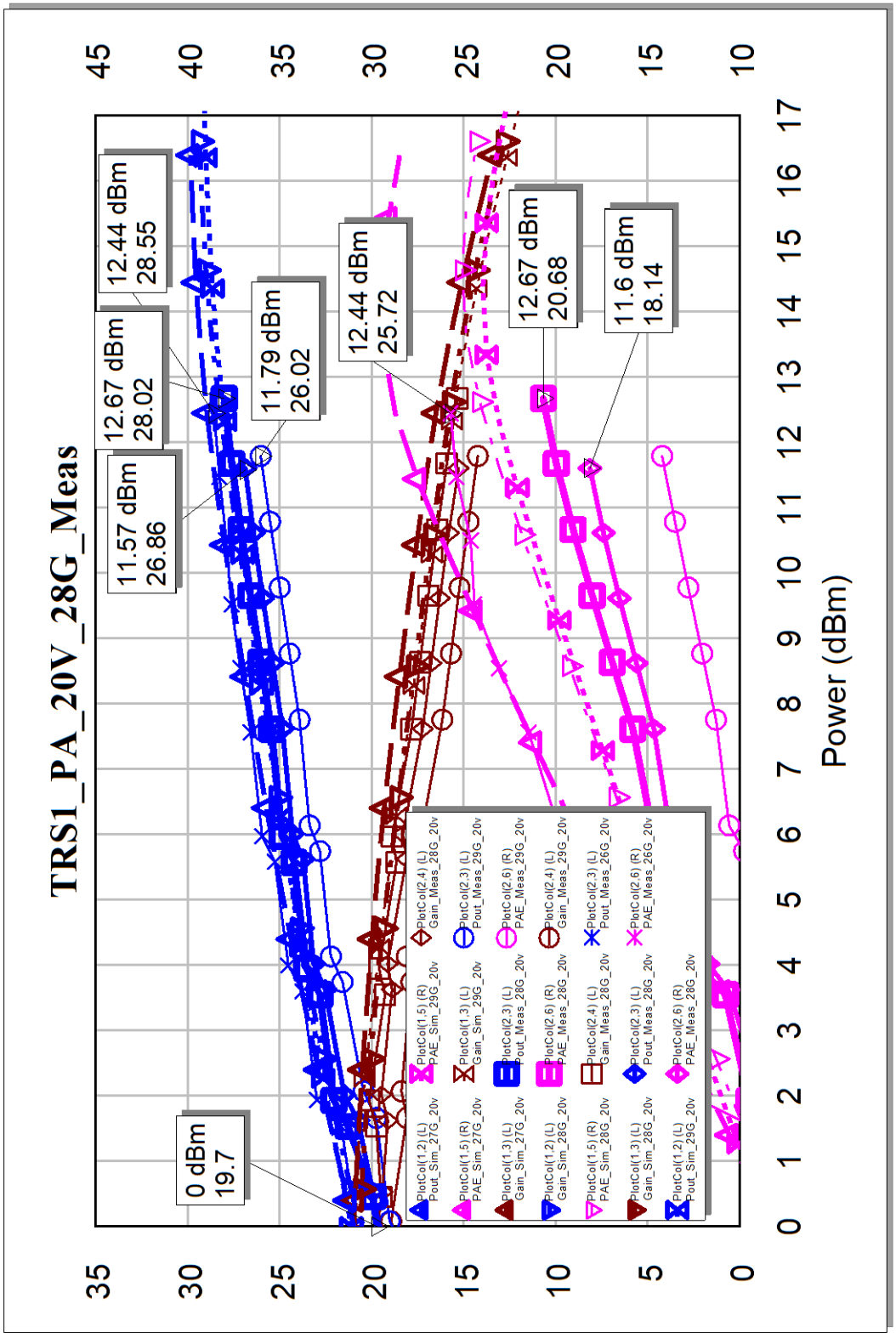

Fig. 34 Measured TRS1 PA (solid) vs. measured PA (dash) (20 V)

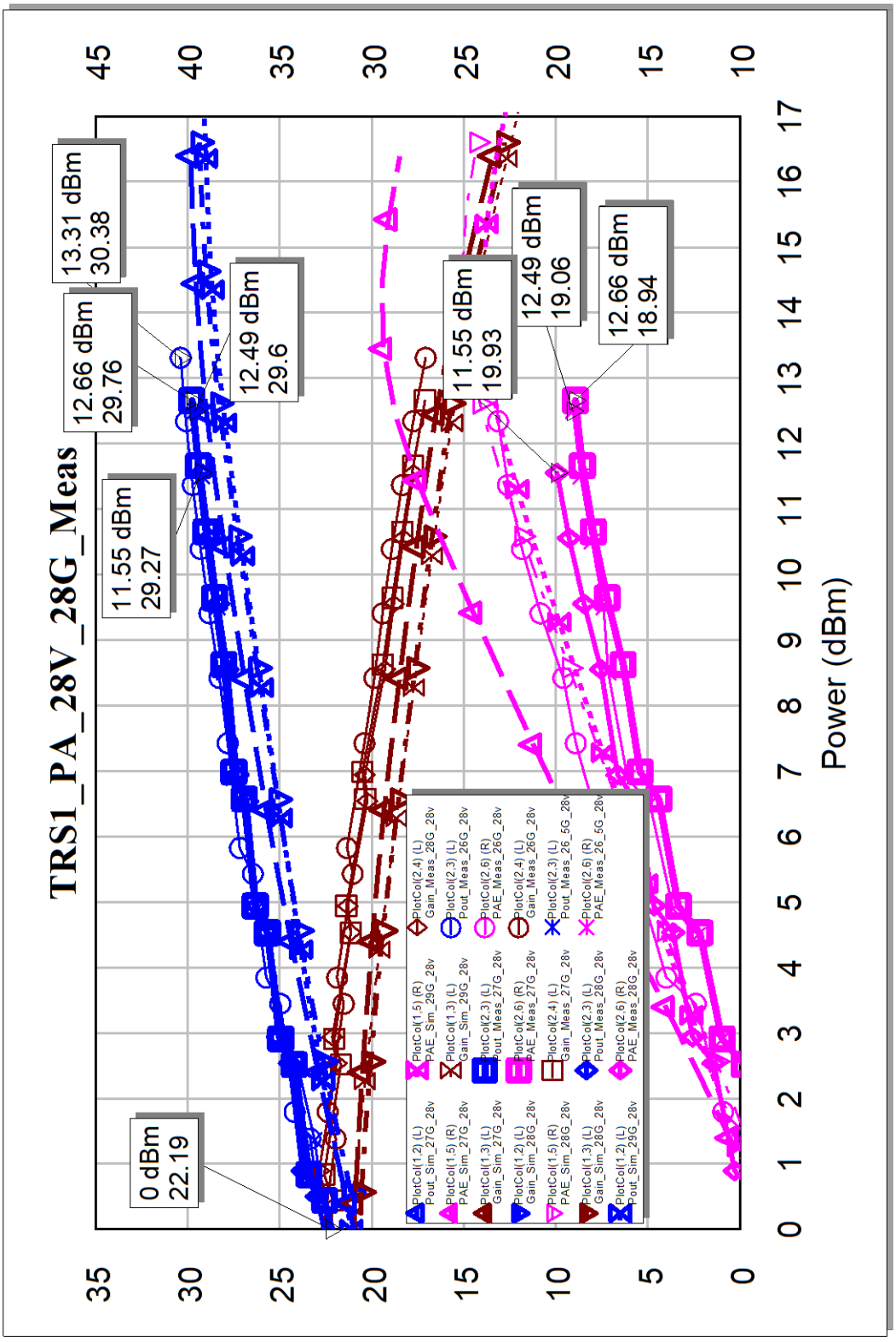

Fig. 35 Measured TRS1 PA (solid) vs. measured PA (dash) (28 V)

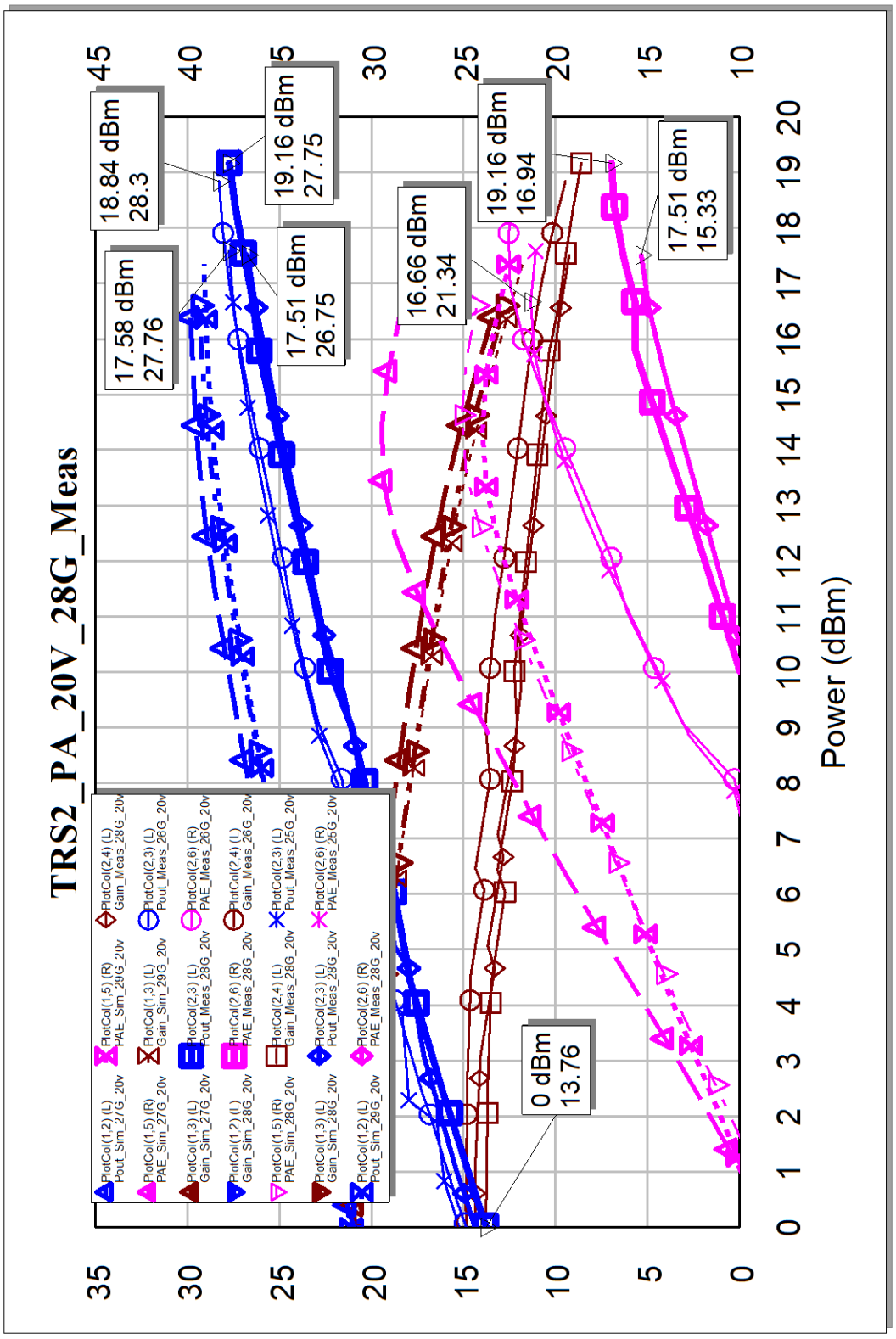

Fig. 36 Measured TRS2 PA (solid) vs. measured PA (dash) (20 V)

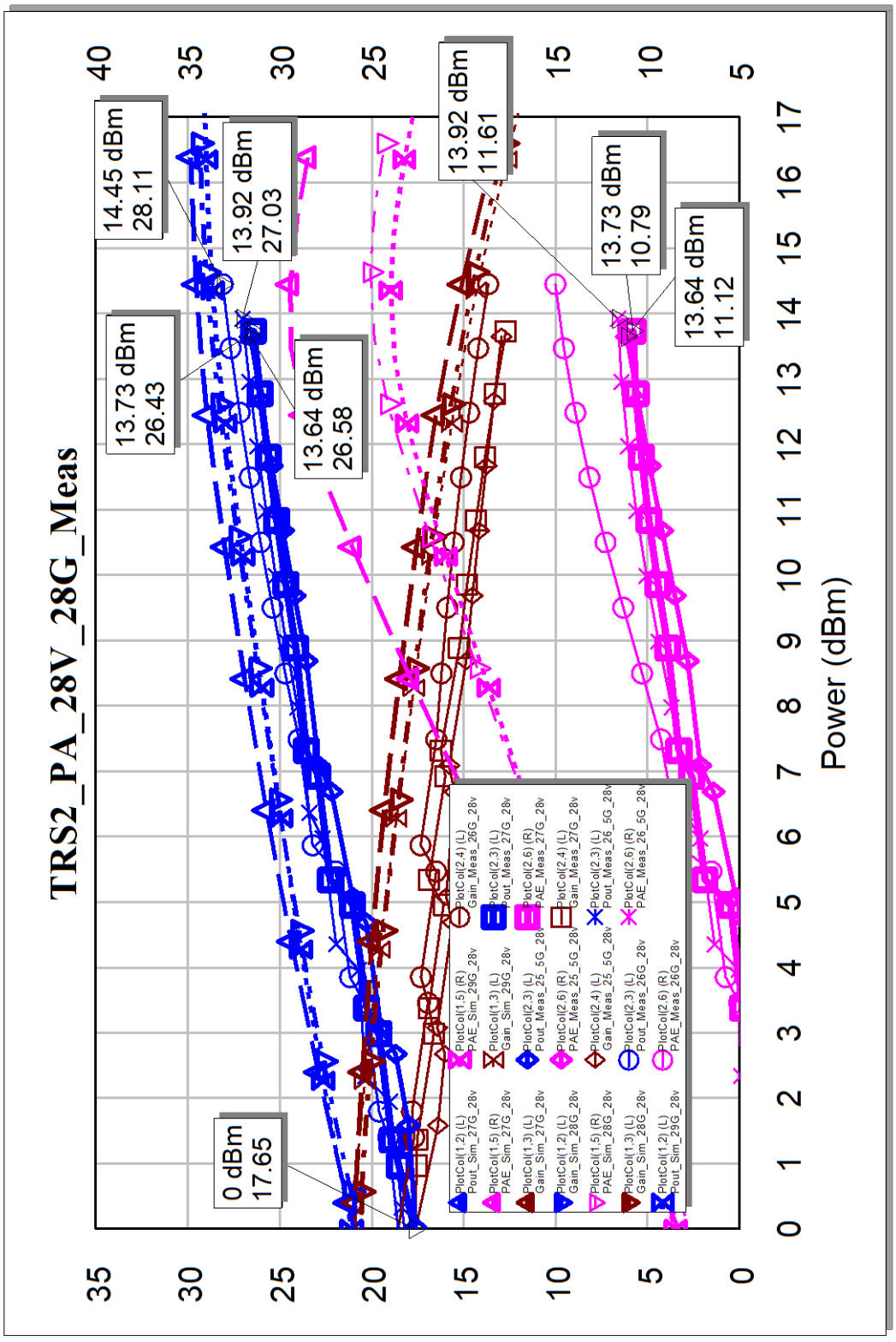

Fig. 37 Measured TRS2 PA (solid) vs. measured PA (dash) (28 V)

6. Comments Regarding the DC Bias of Amplifiers

As mentioned previously, the DC bias has a significant effect on noise performance, power performance, and small signal performance. The LNAs were generally designed for 10-V operation, which fits best with simulations, but the amplifier should operate over quite a range of biases up to 28 V. Linear models for the LNAs typically use 5-V or 10-V biases, with 100-mA/mm or 150-mA/mm drain currents. Figure 38 shows the two-stage LNA with thicker, solid measured lines for the 10-V biases, which agree well with the simulations (dash), while the solid, thinner lines are measured at 5 V with less gain and a slight downshift in the frequency band. This was pretty typical for the power amplifiers, which were generally designed for 28-V operation, but could also operate at lower voltages. Figure 39 shows the two-stage PA with thicker, solid measured lines for the 28-V bias, which agree well with the simulations (dash), while the solid thinner lines are measured at 20 V, 10 V, and 5 V with less gain and a slight downshift in the frequency band as the drain voltage is lowered. Gain drops considerably at the 5-V bias.

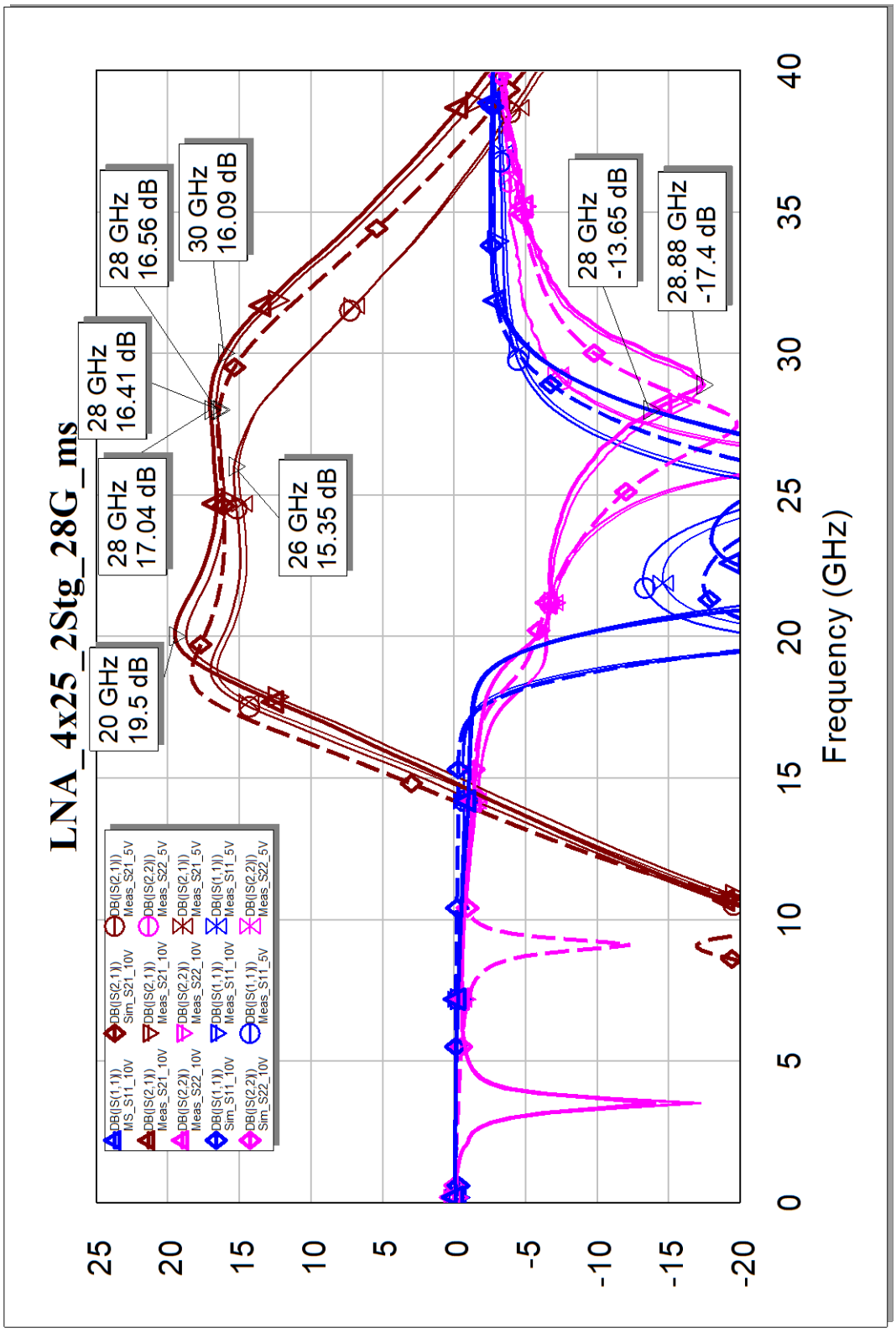

Fig. 38 Measured (solid) vs. simulation (dash) two-stage 4- × 25-µm LNA (5 V, 10 V)

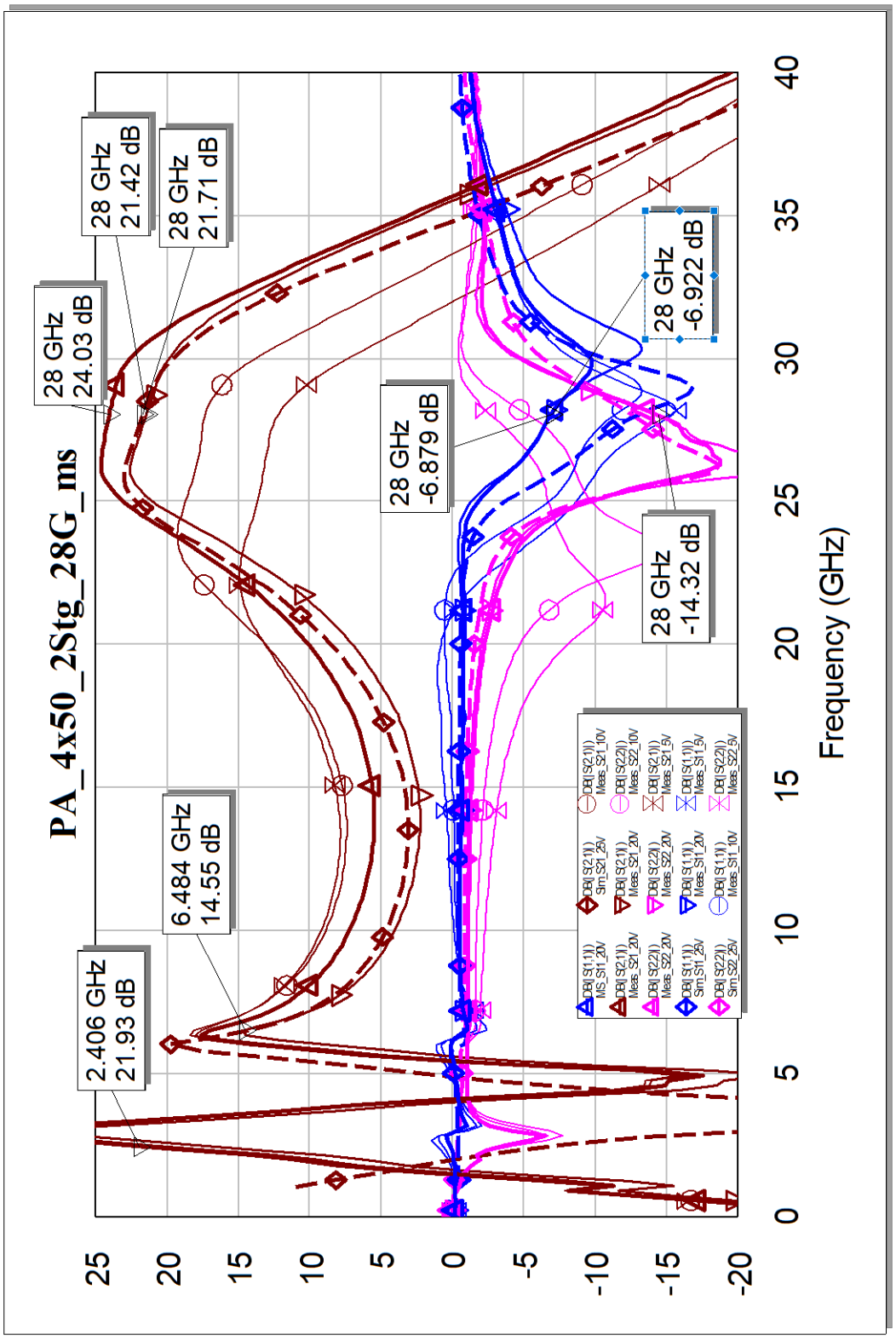

Fig. 39 Measured (solid) vs. simulation (dash) two-stage 4- × 50-µm, 8- × 50-µm PA (5 V, 10 V, 20 V, 28 V)

7. Large Axiem EM Simulation of T/R Modules 1, 2, and 3

The largest performance differences appeared in the T/R modules containing two switches, at the common input/outputs of the bidirectional amplifiers. With only a single series/shunt switch on the common input/output (antenna connection) of T/R Module 1, the performance closely matched expectations. While all of the individual matching elements and interconnect were EM-simulated in a full composite simulation of the layout, there was a need to eliminate possible unsimulated parasitics among the EM subcircuits, which might be causing some of the resonances observed in the measurements. A simple simulation that cascaded the measured s-parameters of the individual switch and amplifiers predicted broadband flat gain, but did not predict the dips, peaks, or resonances measured in the full T/R Modules 2 and 3. It did predict a slightly narrower bandwidth than originally predicated, but slight shifts are not significant as there could be slight misalignments between the bandwidth of the switches and amplifiers. The misaligned bands tend to amplify small differences due to process variation or small model errors that result in a slightly narrower bandwidth.

Surprisingly, the 46-port EM simulation of the full layout of T/R Module 3 completed successfully after cleaning up a few errors in the EM port definitions and in the connections of the final schematic. Figure 40 shows a plot of the T/R module, which fits within a 2-mm × 1.5-mm die. For EM simulation, the active devices are removed and replaced with port connections for later resimulation with the s-parameters obtained from the EM simulation. Some of the HEMTs have two ports for their gate and drain connections with grounded source terminals, while other HEMTs use all three ports for gate, drain, and source such as when used as switches or in the LNAs where source inductance is used for feedback. After removing the active devices, and also the ground–signal–ground (GSG)* launches that resulted in a simplified to 50-Ω microstrip in and out, Fig. 41 shows the 2-D view of the Axiem EM simulation of T/R Module 3, while Fig. 42 is its corresponding 3-D mesh. A DC simulation at zero frequency is included to verify the DC-bias pad connections and proper isolation of the desired RF match from the external DC supplies. Port connector elements in the schematic (Fig. 43) simplify the connections to the HEMT devices in the switches and amplifiers. The HEMTs on the left and right side of the schematic are part of the T/R switches and can be toggled between the linear switch model (presumed to be more accurate) and the nonlinear switch model. At the top are the two 4- × 25-μm HEMTs for the LNA, and the 4- × 50-μm and 8- × 50-μm HEMTs at the bottom are for the PA, each of

* The GSG is a coplanar microwave transmission structure.

which can be toggled between a linear or nonlinear model. When simulated as a receiver, the A and B switch inputs are set and the LNA is biased appropriately (e.g., 10 V) while the PA bias is off (e.g., 0 V). Likewise, when simulated as a transmitter, the A and B switch inputs are reversed and the PA is biased appropriately (e.g., 28 V) while the LNA bias is set to "OFF" (e.g., 0 V). Figure 44 shows the annotated DC bias of the PA at 28 V and 150 mA/mm when simulated in the transmit mode, thus verifying the DC and RF performance of the layout (Axiem EM). Using the full EM Axiem simulation with the "typical" HEMT model still does not exactly match the measurements but it does differ considerably from prior simulations and starts to show the nonflat gain with resonances, or peaks, in the gain (see Fig. 45). The simulations differ considerably between linear versus nonlinear models for the HEMT switches, and varying DC biases of the PA, but mostly it seems to reveal the design sensitivity to layout parasitics, modeling errors, and interaction of the subcircuits in the full layout. In receive mode, a full layout EM simulation of the LNA (Fig. 46) at a DC bias of 6 V, not 10 V, shows a reasonable fit on the high side of the bandwidth, but does not match as well on the lower side. It predicts a dip in the gain and a resonance at the low end that does not show up in prior simulations or in the actual measurements. Possibly, process variation could explain the discrepancy; since a full layout EM simulation is feasible this could yield useful information for a future redesign. An updated PDK design kit was installed and used to resimulate with unchanged results. Some of the full T/R modules were mounted in a fixture with coaxial connectors, which showed a similar sensitivity to wire bond interactions creating gain peaks. Probe testing of the modules as die with wire bonds to decoupling chip capacitors provided the best match to simulations.

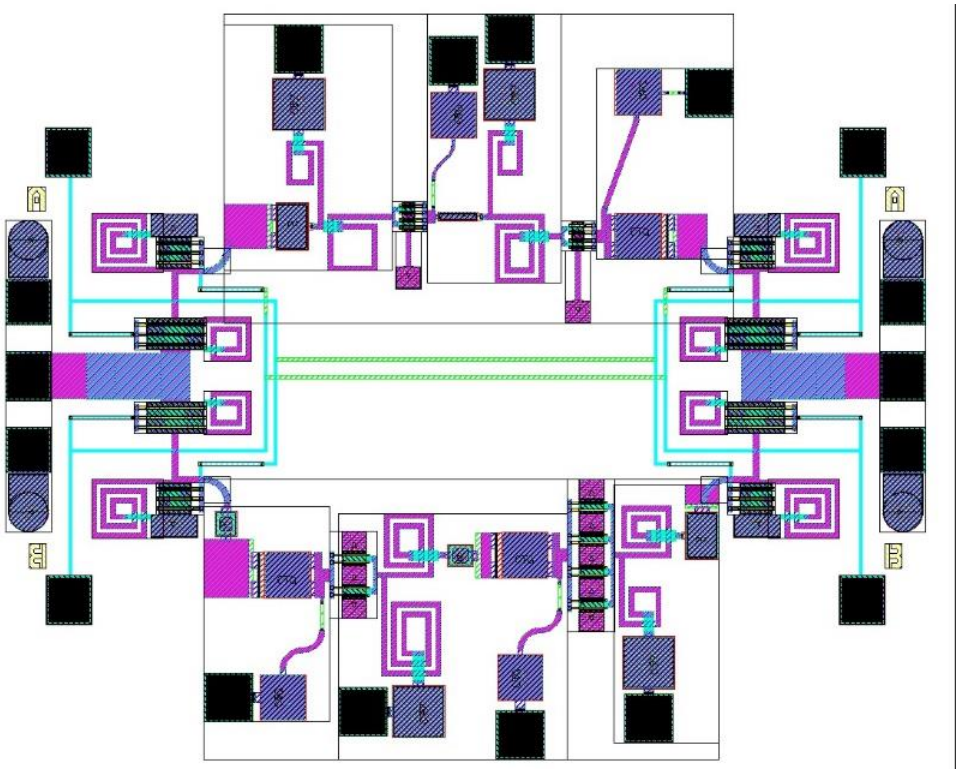

Fig. 40 Layout plot of T/R Module 3: LNA at top, PA at bottom (2 mm × 1.5 mm)

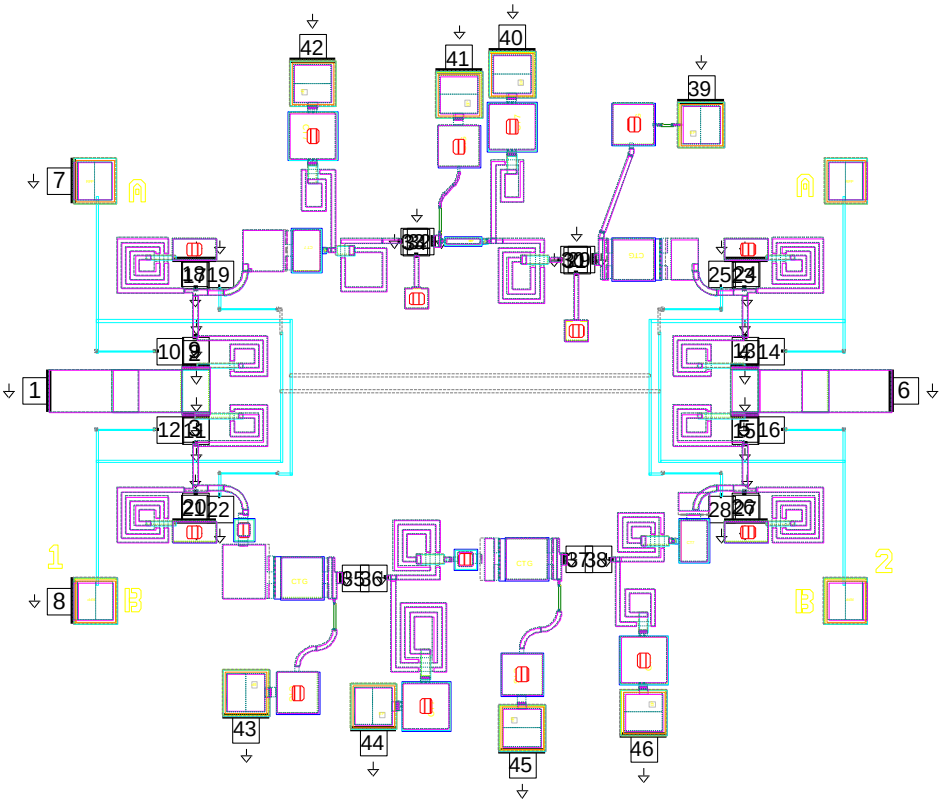

Fig. 41 2-D Axiem EM plot of T/R Module 3 (46 ports)

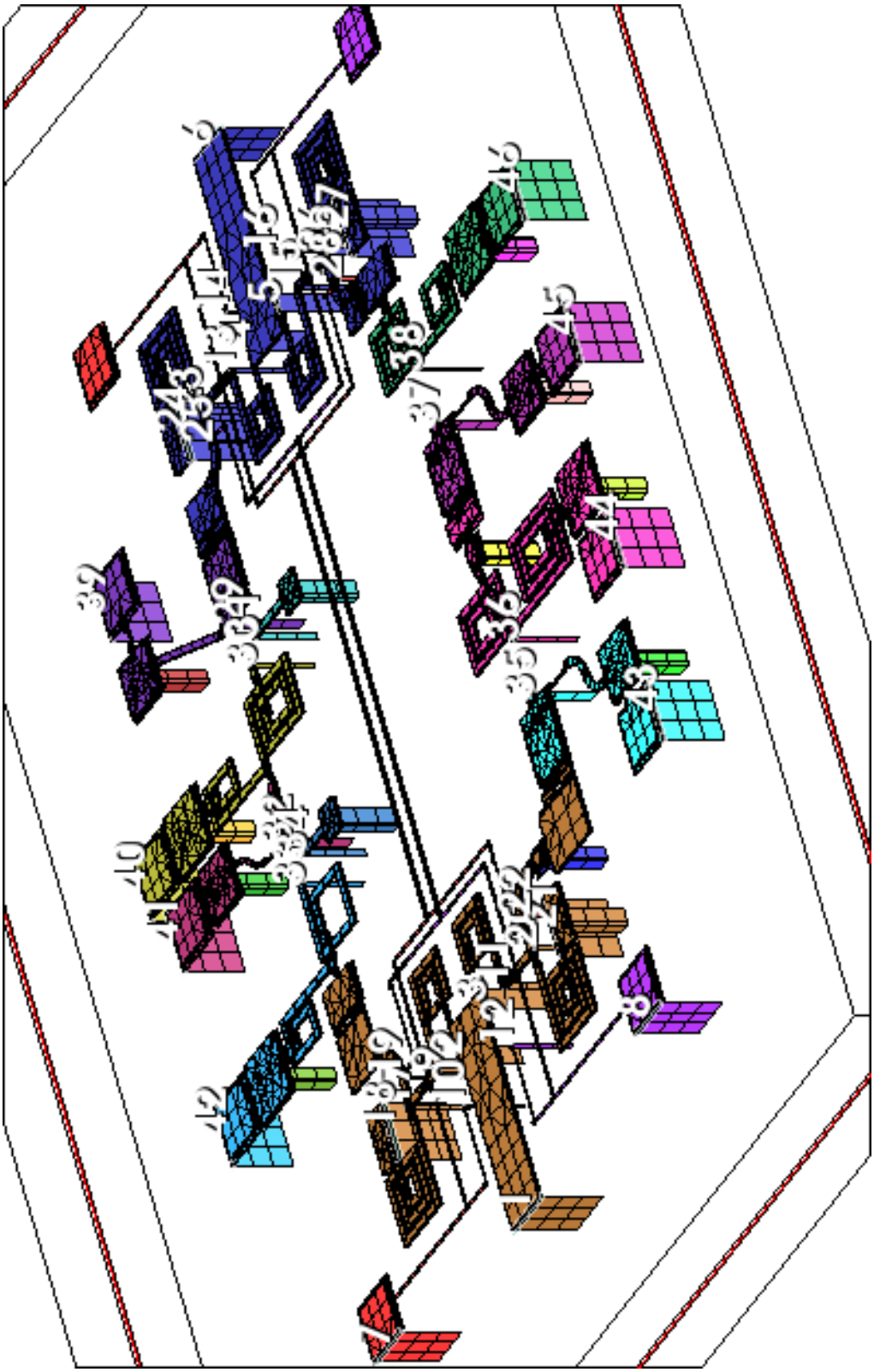

Fig. 42 3-D Axiem EM mesh plot of T/R Module 3 (46 ports)

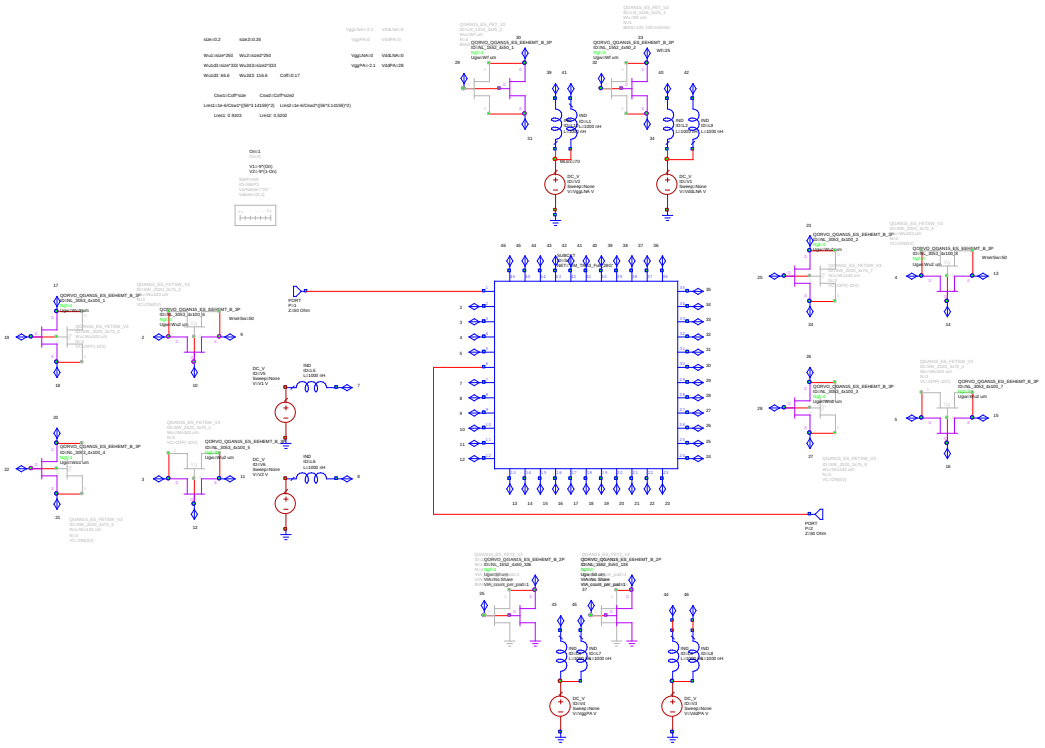

Fig. 43 Schematic for EM simulation of T/R Module 3 (46-port subcircuit)

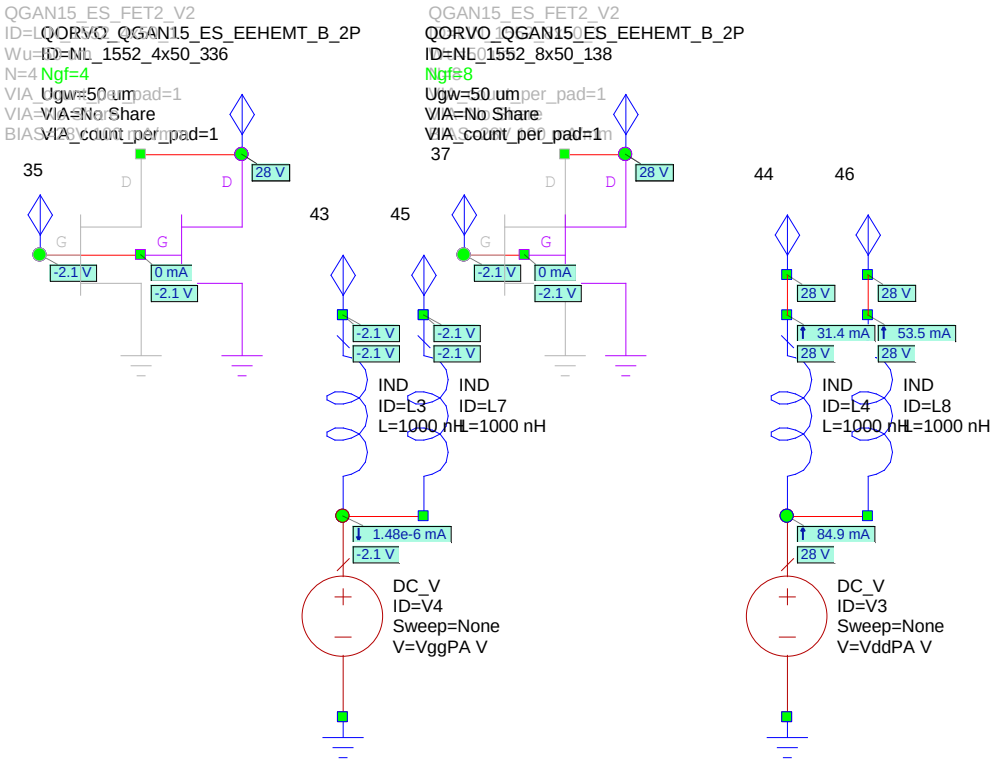

Fig. 44 DC annotation of PA HEMTs verifying bias of physical layout for TRS 3 (28 V; 150 mA/mm)

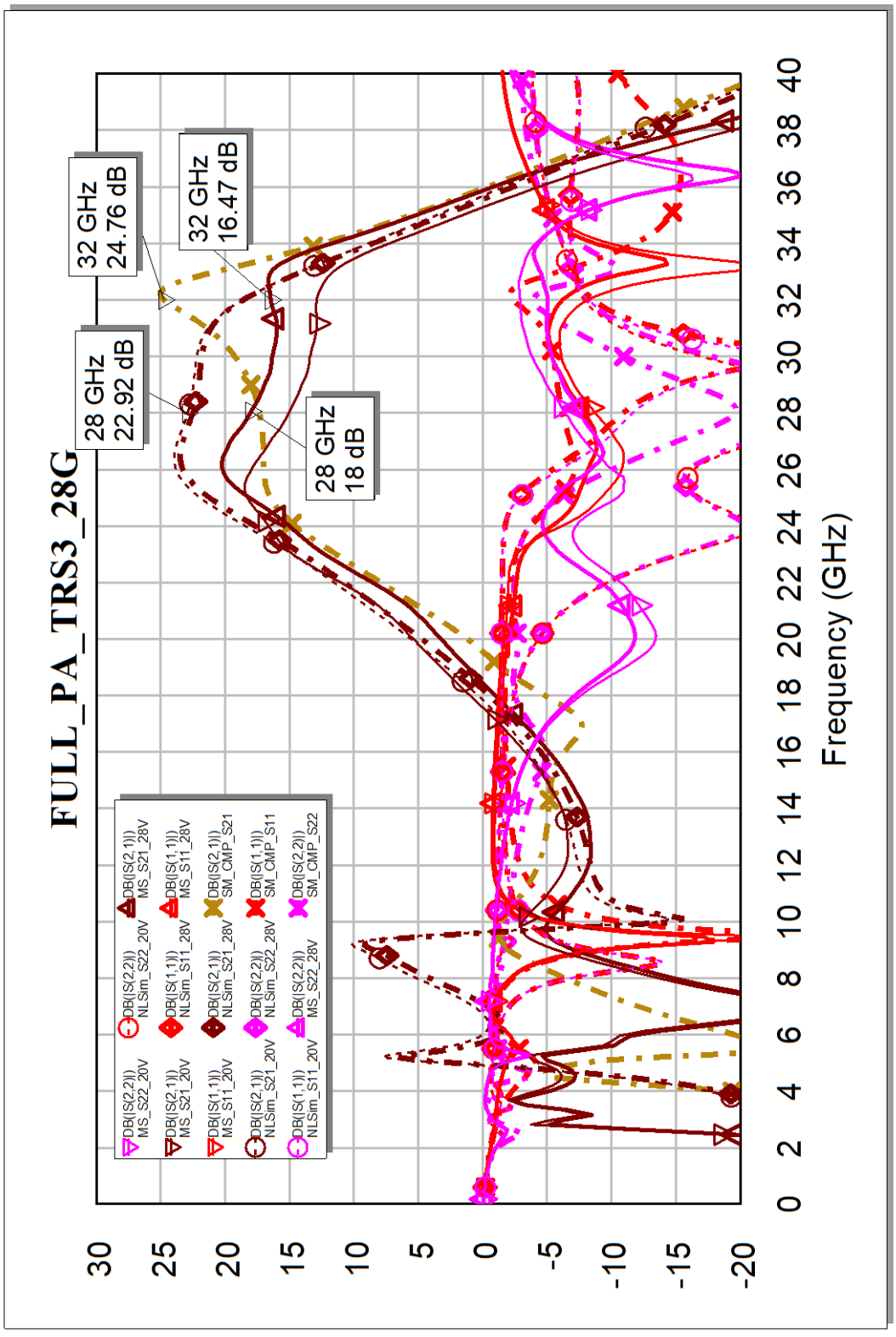

Fig. 45 Measured (solid) vs. simulation (dot) full EM layout, TRS 3 transmit PA (28 V)

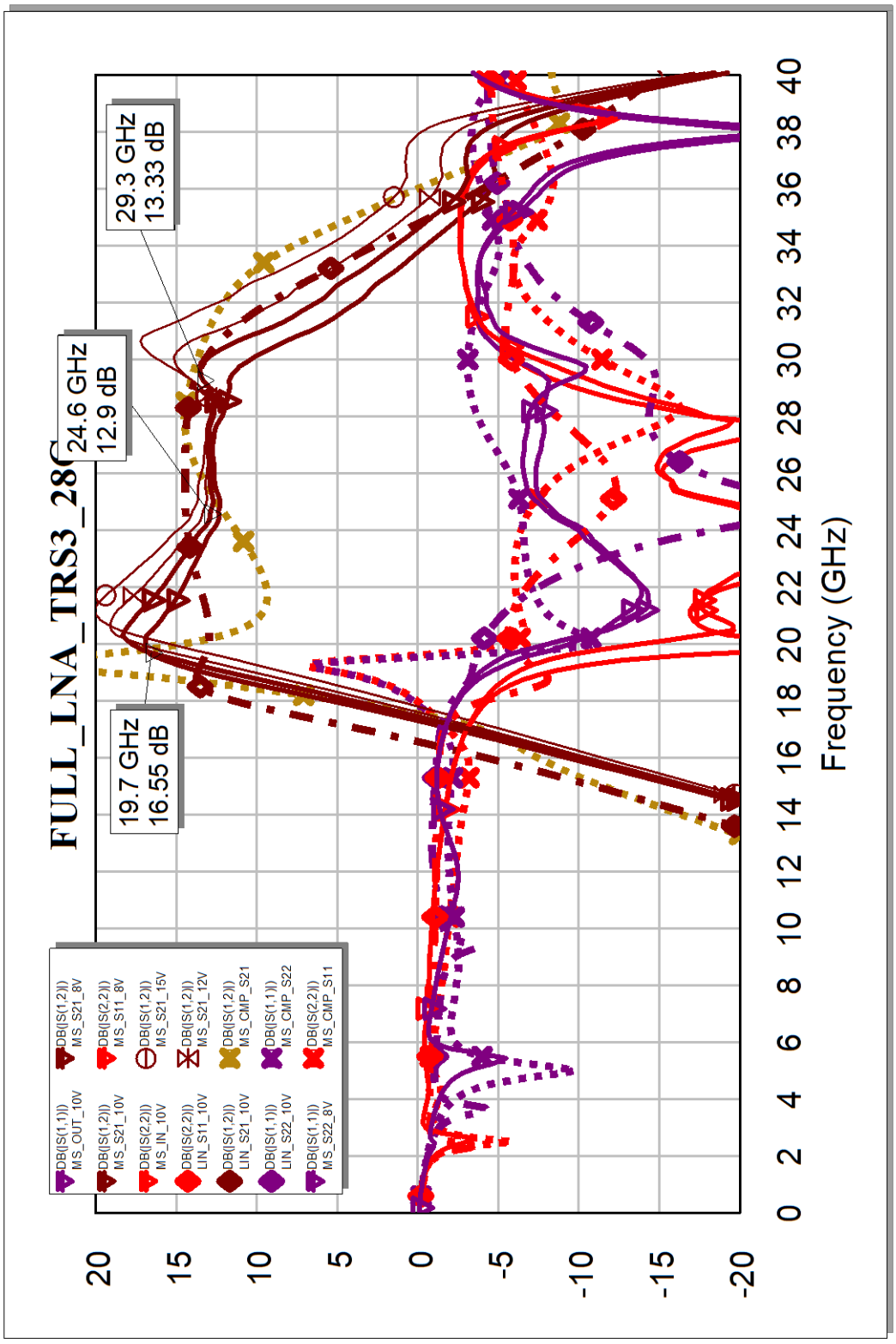

Fig. 46 Measured (solid) vs. simulation (dot) full EM layout, TRS 3 receive LNA (6 V)

Given the success of an Axiem EM simulation of the full T/R module layout of Variation 3 with dual SPDT–SS switches, a full Axiem EM simulation of the T/R Module 2 layout was performed. Figure 47 shows a plot of the T/R Module 2, which fits within a 2-mm × 1.5-mm die. For EM simulation, the active devices are removed and replaced with port connections to enable later resimulation using the s-parameters obtained from the EM simulation. Some of the HEMTs have two ports for their gate and drain connections with grounded source terminals, while other HEMTs need three ports for gate, drain, and source such as when used as switches or in the LNAs for source inductance feedback. After removing the active devices, and also the GSG launches, which resulted in a simplified to 50-Ω microstrip in and out, Fig. 48 shows the 2-D view of the Axiem EM simulation of T/R Module 2, while Fig. 49 is its corresponding 3-D mesh. A DC simulation at zero frequency is included to verify the DC-bias pad connections and proper isolation of the desired RF match from the external DC supplies. Port connector elements in the schematic (Fig. 50) simplify the 36 connections to the HEMT devices in the switches and amplifiers. The HEMTs on the left and right sides of the schematic are part of the shunt-only T/R switches and can be toggled between the linear switch model (presumed to be more accurate) and the nonlinear switch model. At the top are the two 4- × 25-μm HEMTs for the LNA, and the 4- × 50-μm and 8- × 50-μm HEMTs at the bottom are for the PA, each of which can be toggled between a linear or nonlinear model.

When simulated as a receiver, the A and B switch inputs are set and the LNA is biased appropriately (e.g., 10 V) while the PA bias is set to off (e.g., 0 V). Likewise, when simulated as a transmitter, the A and B switch inputs are reversed and the PA is biased appropriately (e.g., 28 V) while the LNA bias is set to “OFF” (e.g., 0 V). Figure 51 shows the annotated DC bias of the LNA at 6 V and 100 mA/mm when simulated in the transmit mode, thus verifying the DC and RF performance of the layout (Axiem EM). Using the full EM Axiem simulation with the “typical” HEMT model matches better than the full TRS 3 simulation in the prior discussion, but the fit is better when the nonlinear models are biased at a much different DC bias, not at the nominal bias. For the PA in receive mode, the bias is 14 V instead of 28 V, and for the LNA in receive mode it matches better at 6 V instead of 10 V, as measured. Figure 52 shows measured versus simulations for the transmit mode, with good match to the dips and peaks of the measured 28-V modules, while a better simulation fit used a lower 14-V DC bias for the PA. The gain is considerably lower than the prior simulations and certainly lower than predicted by cascading the individual measured subcircuits. In receive mode, the LNA simulations shown in Fig. 53 show a reasonable fit on the high side of the bandwidth for the full EM simulation and match the gain peak on the lower side as well. But, this uses a 6-V DC bias for a better fit with the simulation instead of 10 V, as measured. Possibly

process variation could explain the discrepancy but a full layout EM simulation is feasible and might yield useful information in a future redesign.

In the layout, the A and B switch biases were not connected between the left side SPDT switch and the right side SPDT switch, as they were in Module 3. In simulations, a 1.4-nH inductor modeled the wire bond connections of the A and B switch bias pads during actual testing. Surprisingly, given the isolating resistors on the gates of the switches, there was a minor but noticeable sensitivity to the wire bond inductance affecting the gain of the two-stage amplifier. Maybe a redesign could tweak the two-stage amplifier designs for less sensitivity to variation and mismatch. In future runs it would be good to add testable HEMT devices to test and verify the models and evaluate the accuracy of each linear and nonlinear HEMT model. Also, testable HEMTs would be needed in a switch configuration layout to verify the SPDT design on future fabrications.

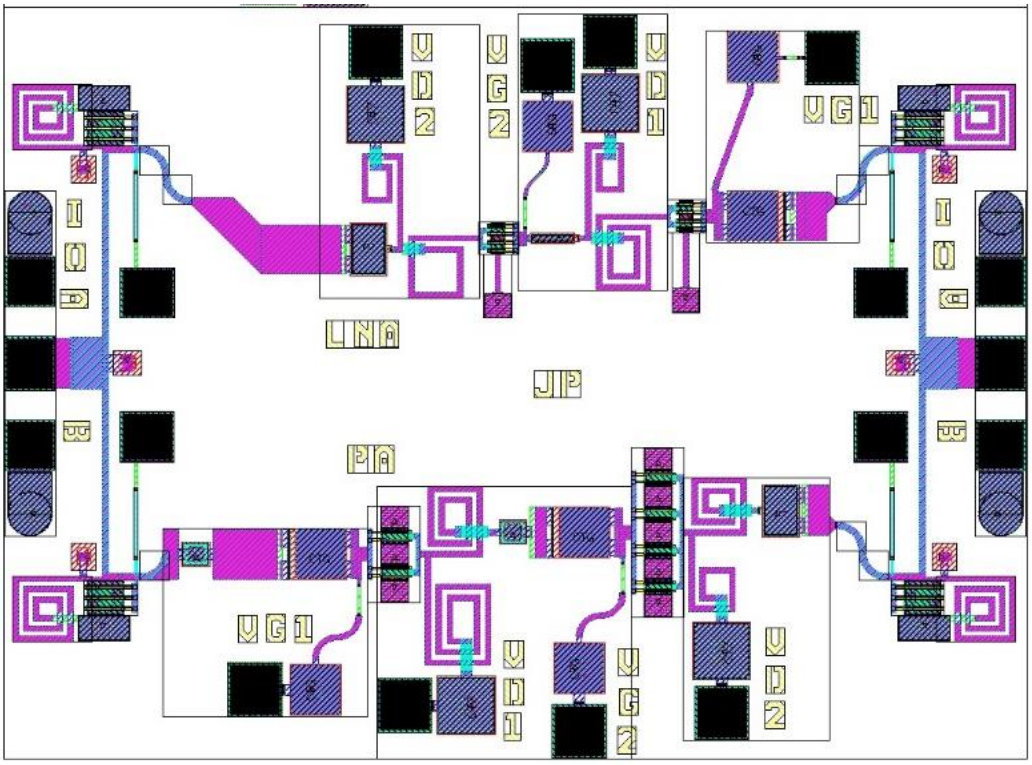

Fig. 47 Layout plot of T/R Module 2: LNA at top, PA at bottom (2 mm × 1.5 mm)

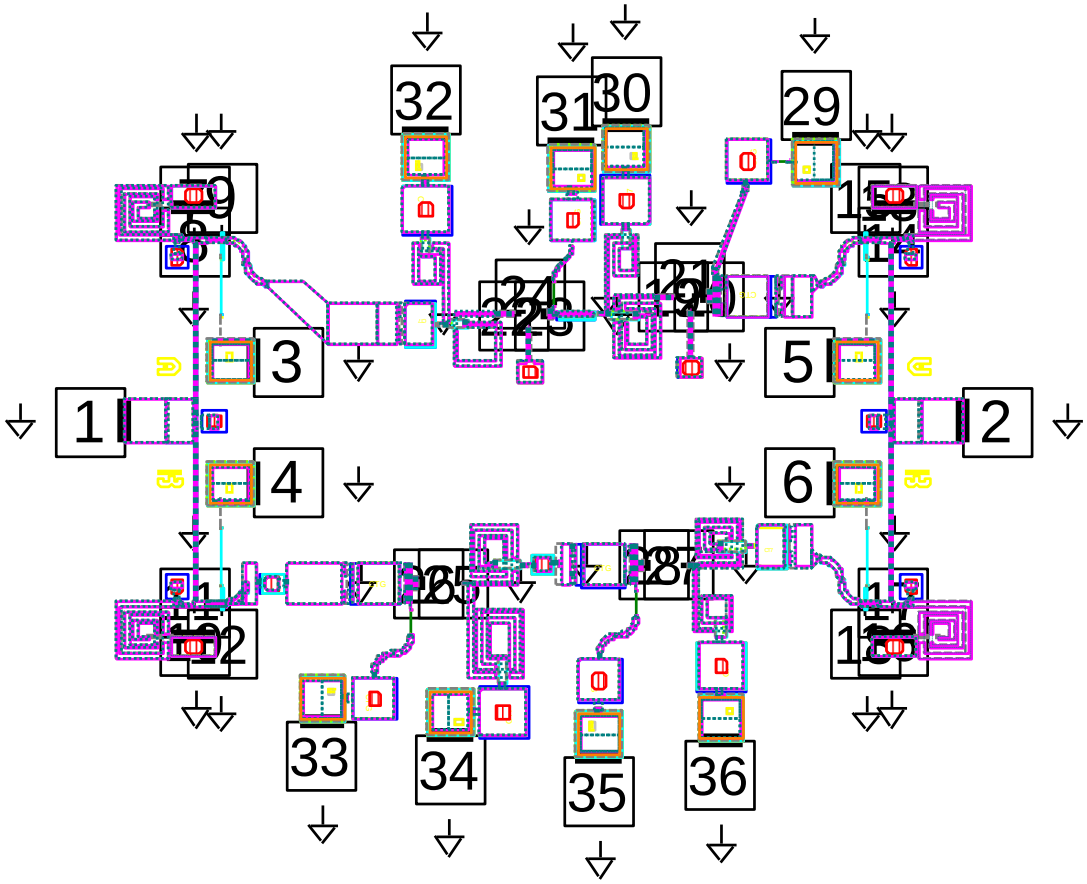

Fig. 48 2-D Axiem EM plot of T/R Module 2 (36 ports)

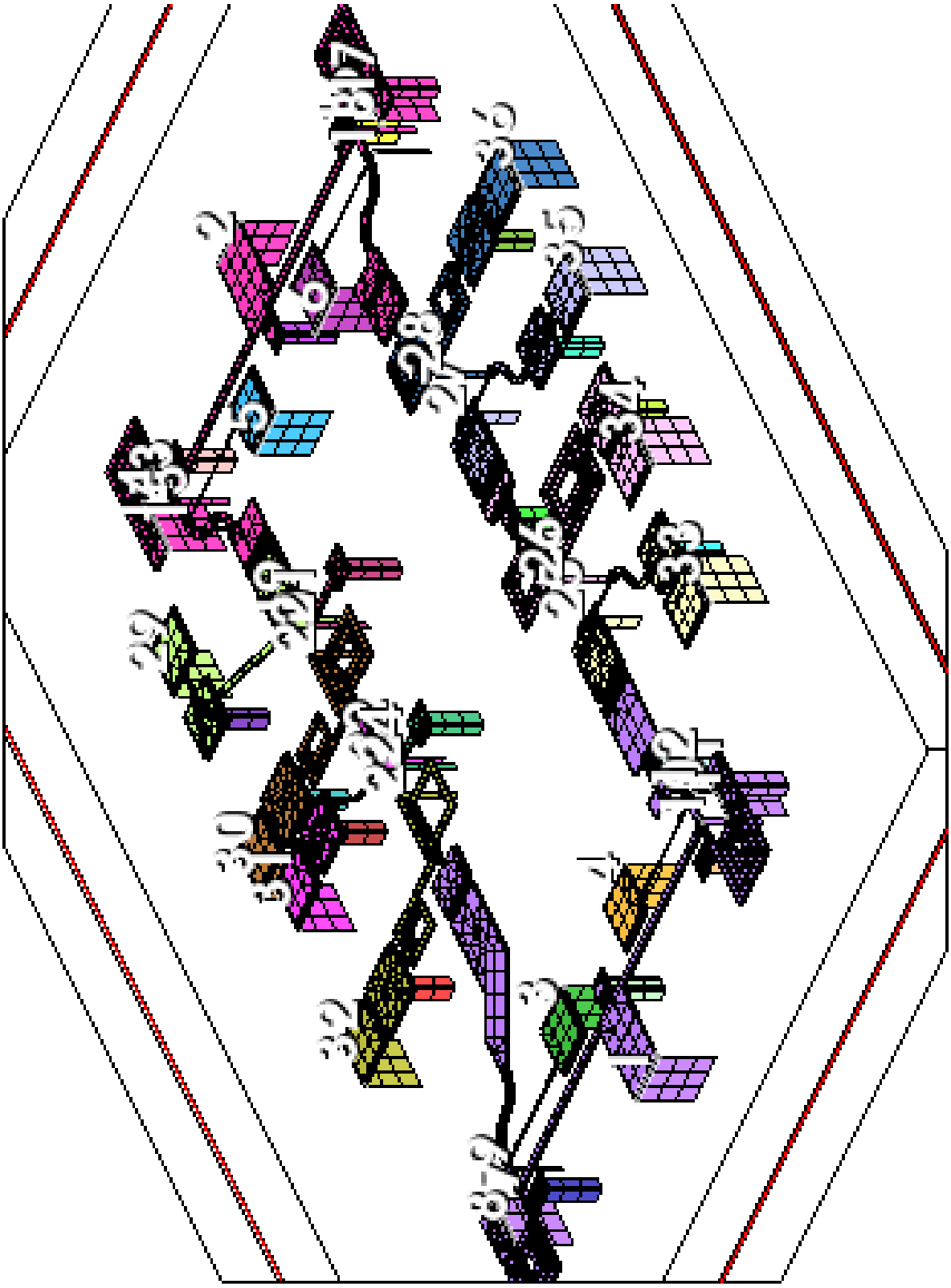

Fig. 49 3-D Axiem EM mesh plot of T/R Module 2 (36 ports)

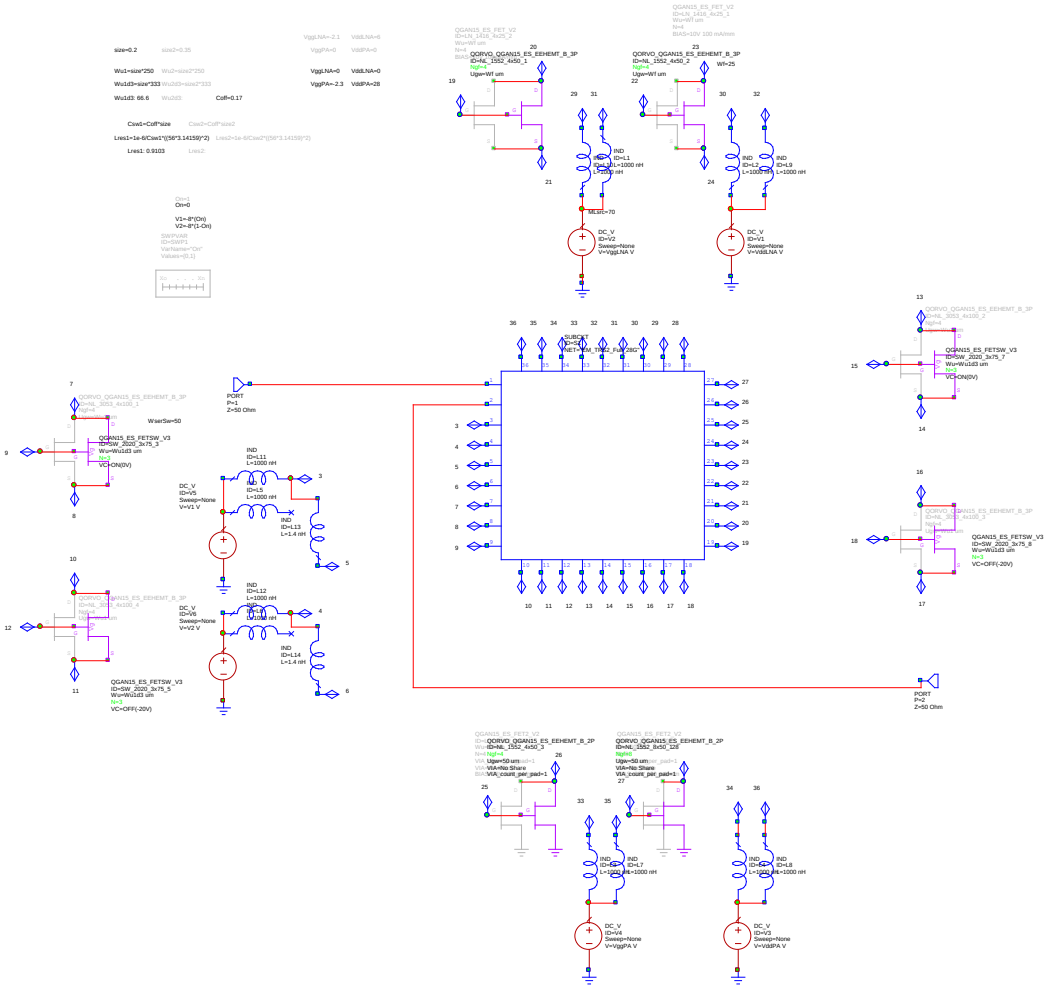

Fig. 50 Schematic for EM simulation of T/R Module 2 (36-port subcircuit)

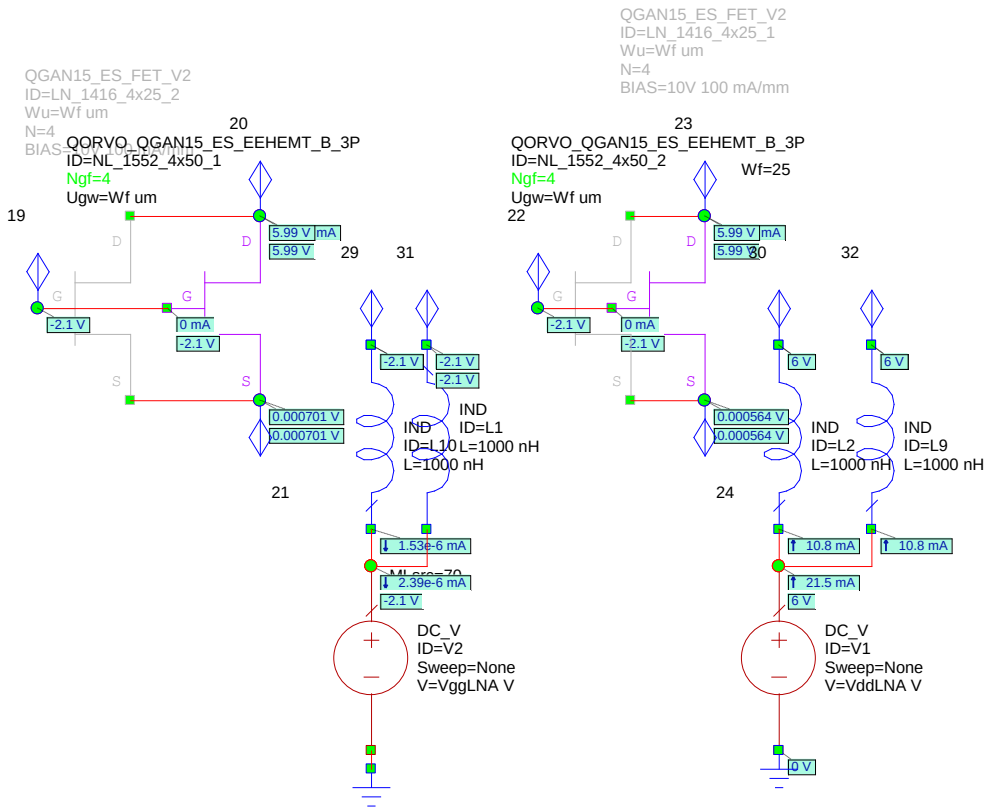

Fig. 51 DC annotation of LNA HEMTs verifying bias of physical layout for TRS 2 (6 V; 100 mA/mm)

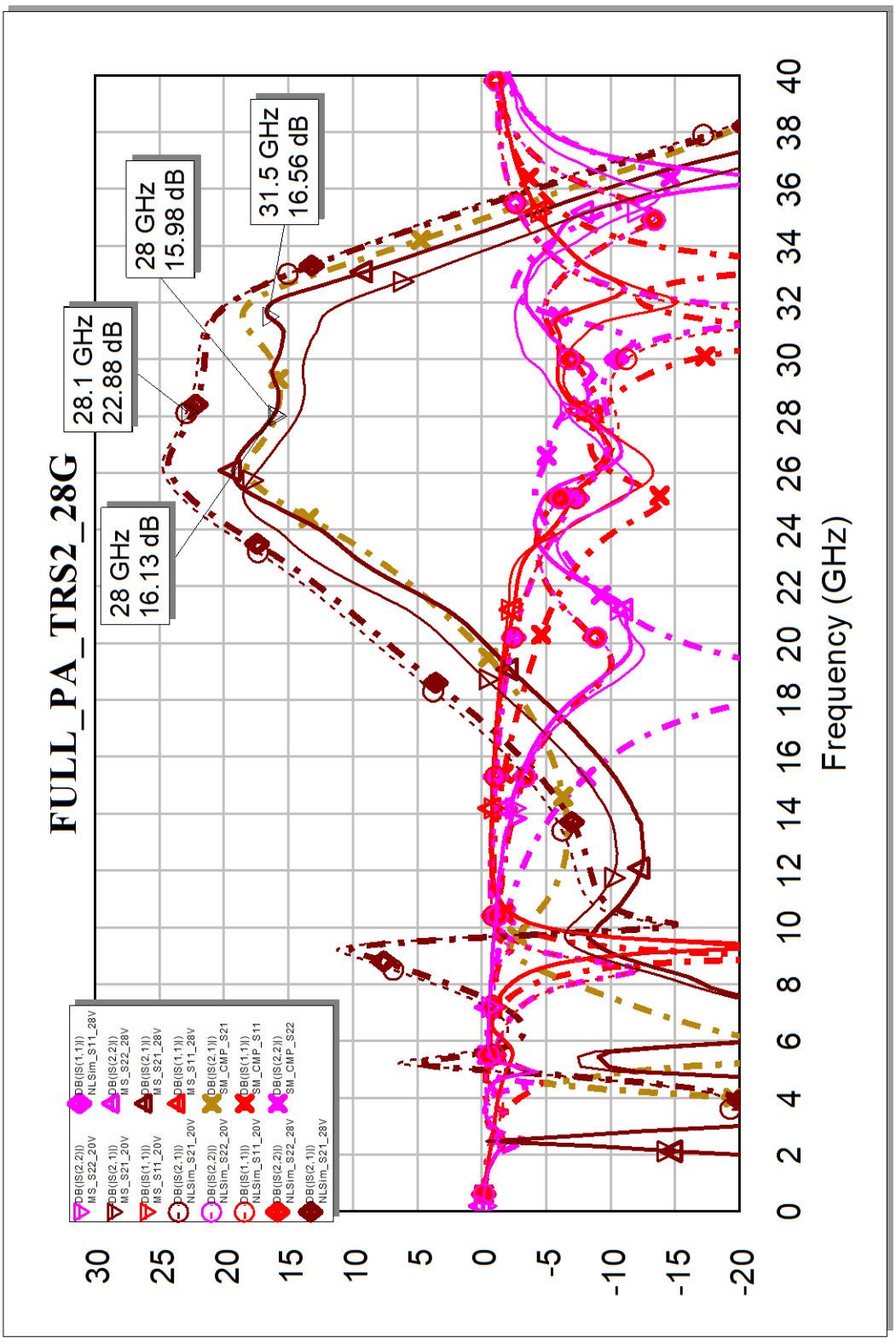

Fig. 52 Measured (solid) vs. simulation (dot) full EM layout, TRS 2 transmit PA (14 V)

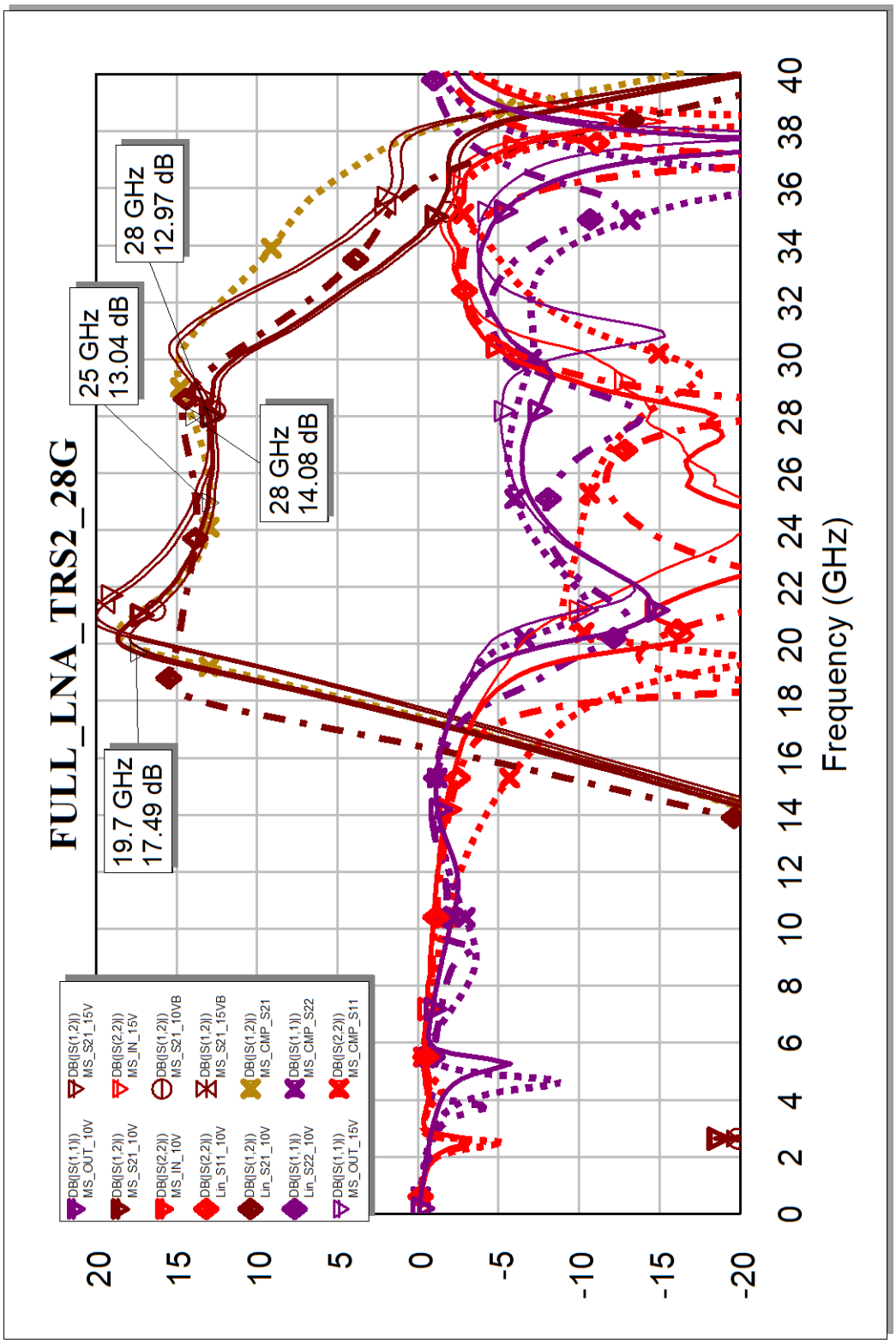

Fig. 53 Measured (solid) vs. simulation (dot) full EM layout, TRS 2 receive LNA (6 V)

Even though the results of T/R Module 1 compared well with simulations, for completeness a full Axiem EM simulation of the T/R Module 1 layout was performed. Figure 54 shows a plot of the T/R Module 1, which fits within a 2-mm × 1.5-mm die. For EM simulation, the active devices are removed and replaced with port connections for later resimulation with the s-parameters obtained from the EM simulation. Figure 55 shows the 2-D view of the Axiem EM simulation of T/R Module 2, while Fig. 56 is its corresponding 3-D mesh. A DC simulation at zero frequency is included to verify the DC-bias pad connections and proper isolation of the desired RF match from the external DC supplies. Port connector elements in the schematic (Fig. 57) simplify the 35 connections to the HEMT devices in the switches and amplifiers. The HEMTs on the right side of the schematic are for the series/shunt T/R switches and can be toggled between the linear switch model (presumed to be more accurate) and the nonlinear switch model. At the top are the two 4- × 25-μm HEMTs for the LNA, and the 4- × 50-μm and 8- × 50-μm HEMTs at the bottom are for the PA, each of which can be toggled between a linear or nonlinear model. When simulated as a receiver, the A and B switch inputs are set and the LNA is biased appropriately (e.g., 10 V) while the PA bias is set to "OFF" (e.g., 0 V). Likewise, when simulated as a transmitter, the A and B switch inputs are reversed and the PA is biased appropriately (e.g., 28 V) while the LNA bias is set to "OFF" (e.g., 0 V).

Figure 58 shows the annotated DC bias of the PA at 28 V and 100–150 mA/mm when simulated in the transmit mode, thus verifying the DC and RF performance of the layout (Axiem EM). For the PA in receive mode, the bias is 14 V instead of 28 V, and for the LNA in receive mode it matches better at 6 V instead of 10 V, as measured. Figure 59 shows measured versus simulations for the transmit mode, with good match to the measured 28-V modules but with the full EM simulation at a much lower 14-V DC bias for the PA. Figure 60 shows measured versus simulations for the receive mode, but with a 6-V DC bias for the simulation instead of 10 V, as measured.

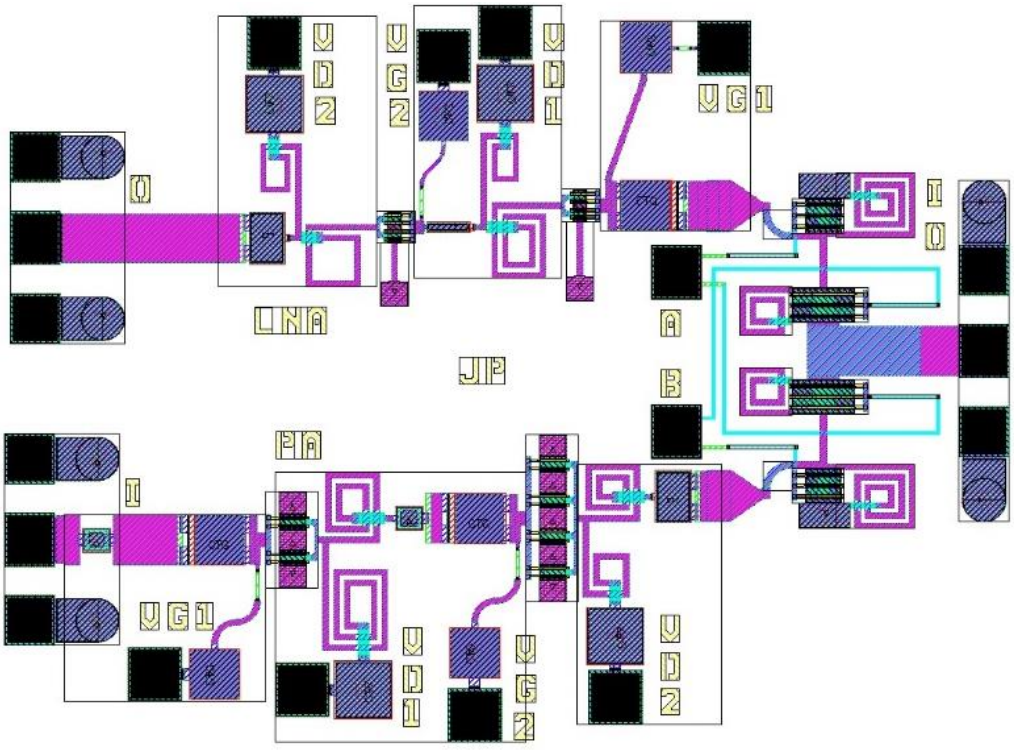

Fig. 54 Layout plot of T/R Module 1: LNA at top, PA at bottom (2 mm × 1.5 mm)

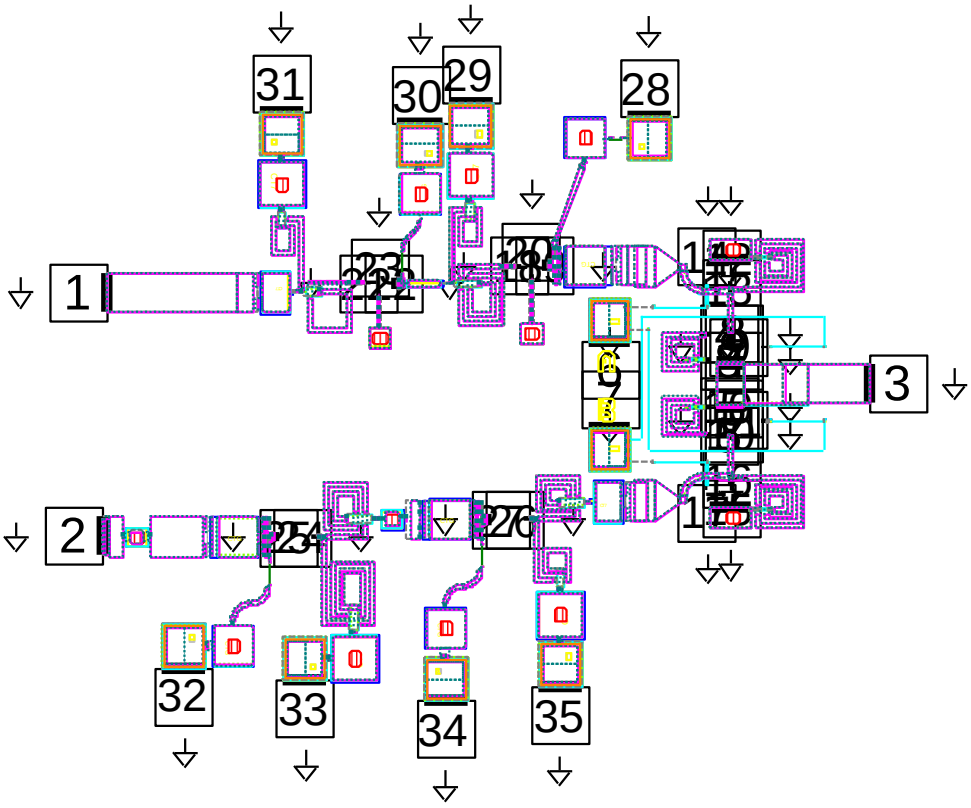

Fig. 55 2-D Axiem EM plot of T/R Module 1 (35 ports)

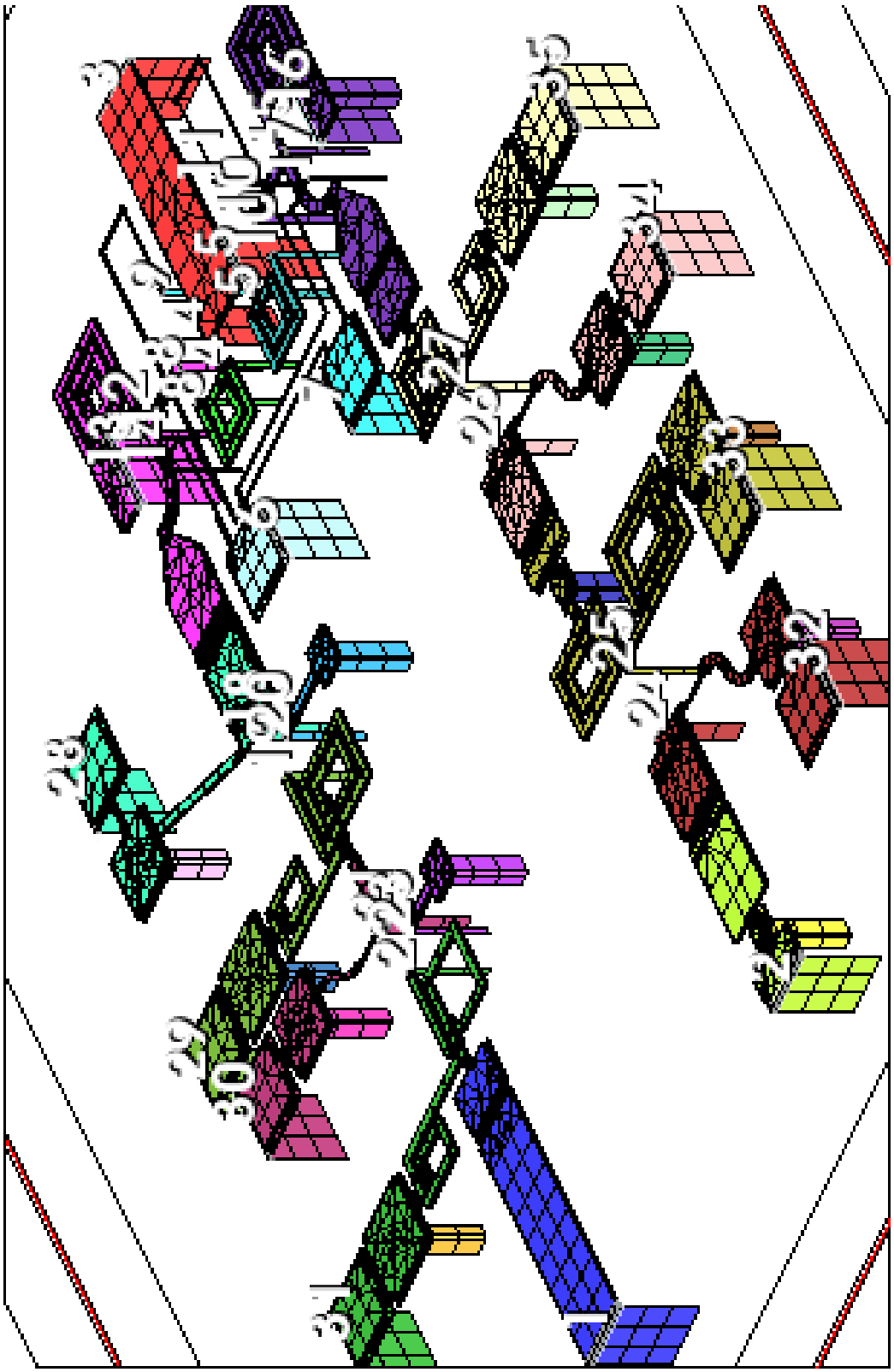

Fig. 56 3-D Axiem EM mesh plot of T/R Module 1 (35 ports)

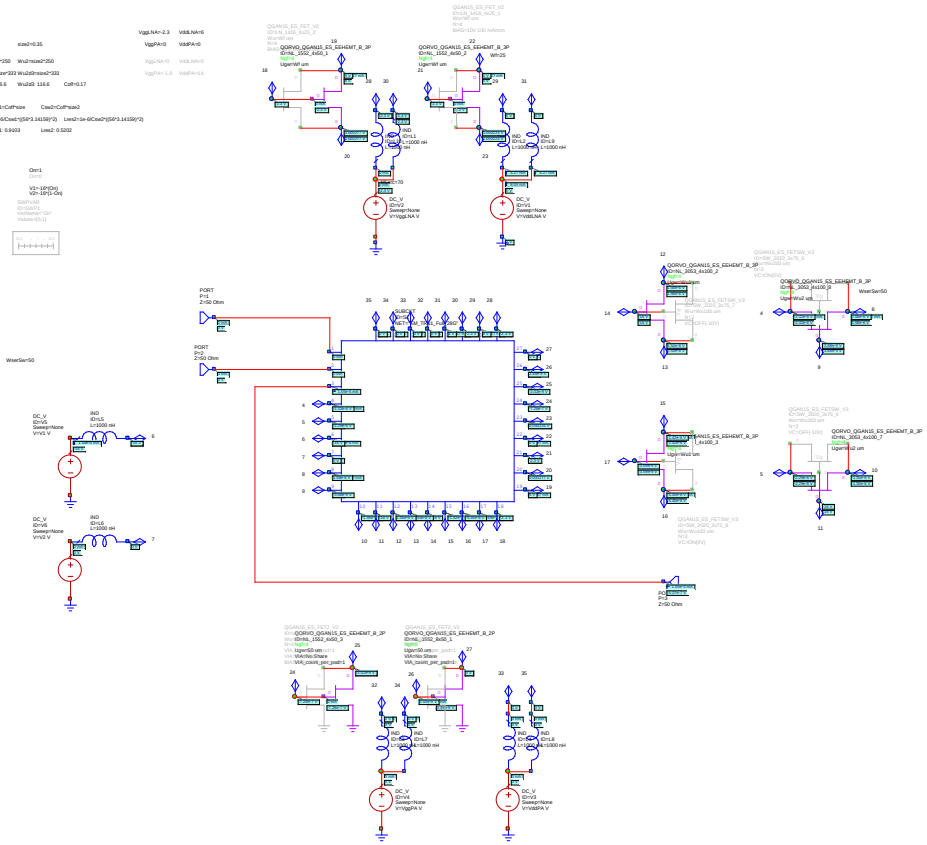

Fig. 57 Schematic for EM simulation of T/R Module 1 (35-port subcircuit)

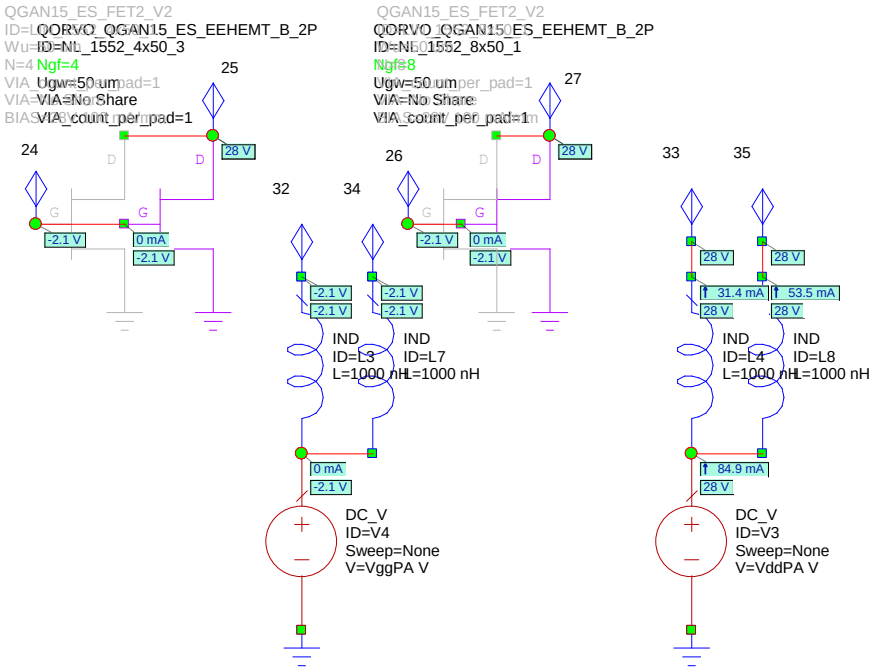

Fig. 58 DC annotation of PA HEMTs verifying bias of physical layout for TRS 1 (28 V; 150 mA/mm)

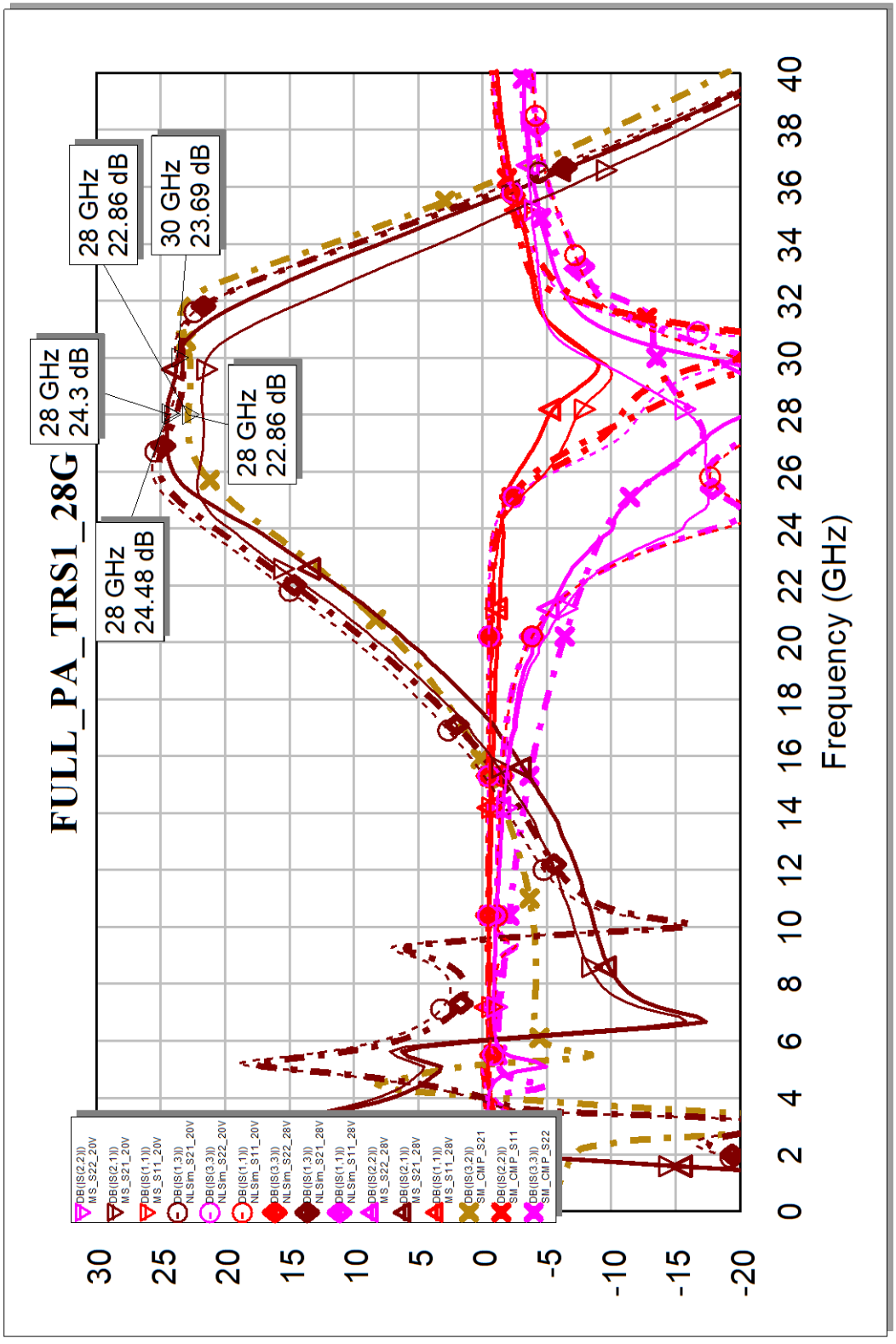

Fig. 59 Measured (solid) vs. simulation (dot) full EM layout, TRS 1 transmit PA (14 V)

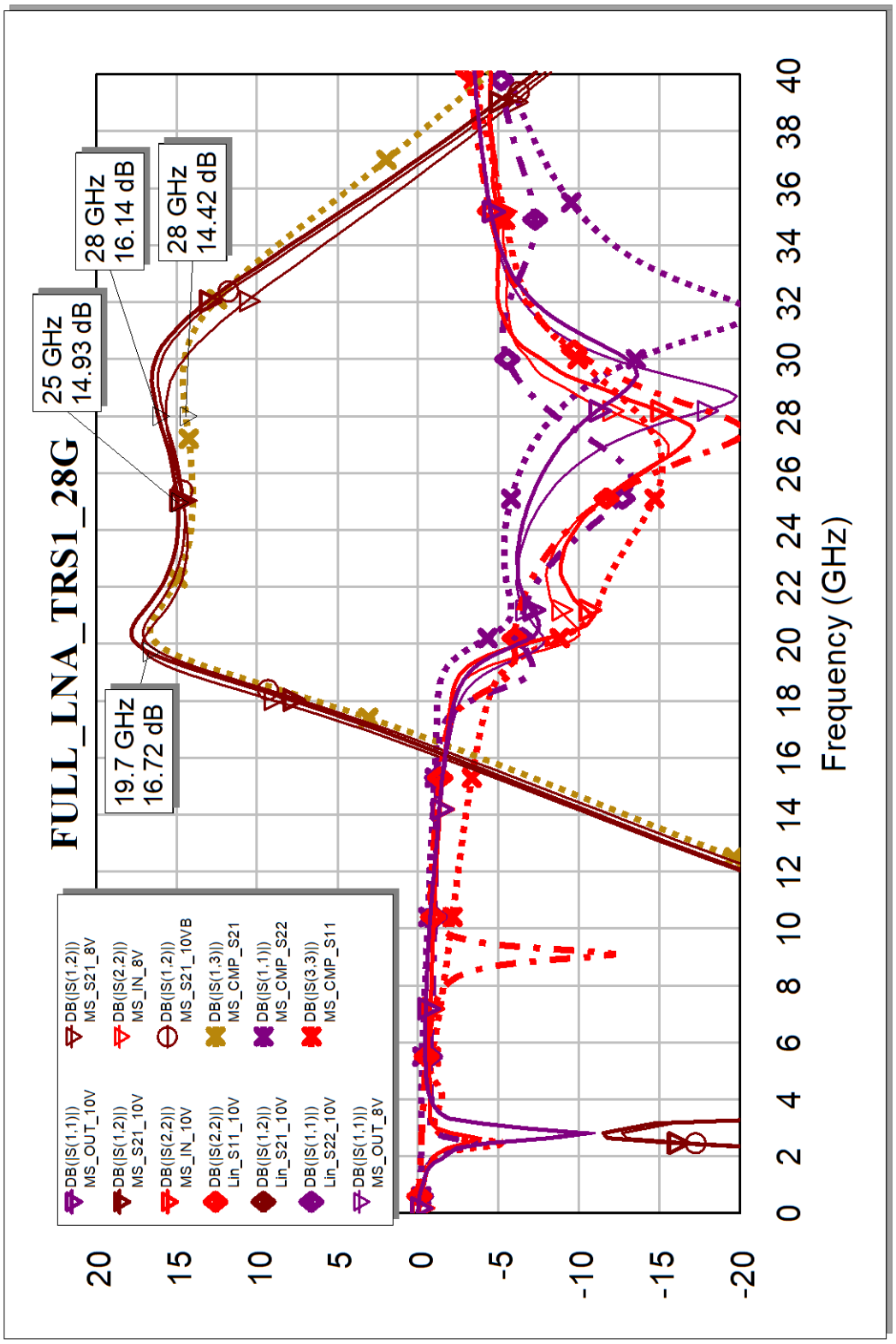

Fig. 60 Measured (solid) vs. simulation (dot) full EM layout, TRS 1 receive LNA (6 V)

Given that the full layout EM simulation worked so well for linear simulations, the power performance simulations were revisited for the T/R modules. Figure 61 shows output power (blue), PAE (magenta), and gain (brown) measured (solid) versus simulation (dash) in plots of power performance of the transmit mode (PA) of T/R Module 1 at the 28-V DC bias and at frequencies of 26–29 GHz (see legend). Figure 62 shows output power (blue), PAE (magenta), and gain (brown) measured (solid) versus simulation (dash) in plots of power performance of the transmit mode (PA) of T/R Module 2 at the 28-V DC bias and at frequencies of 26–30 GHz (see legend). Finally, Fig. 63 shows output power (blue), PAE (magenta), and gain (brown) measured (solid) versus simulation (dash) in plots of power performance of the transmit mode (PA) of T/R Module 3 at the 28-V DC bias and at frequencies of 26–30 GHz (see legend). These full layout EM simulations compared well with measured results of the transmit (PA) of all three modules.

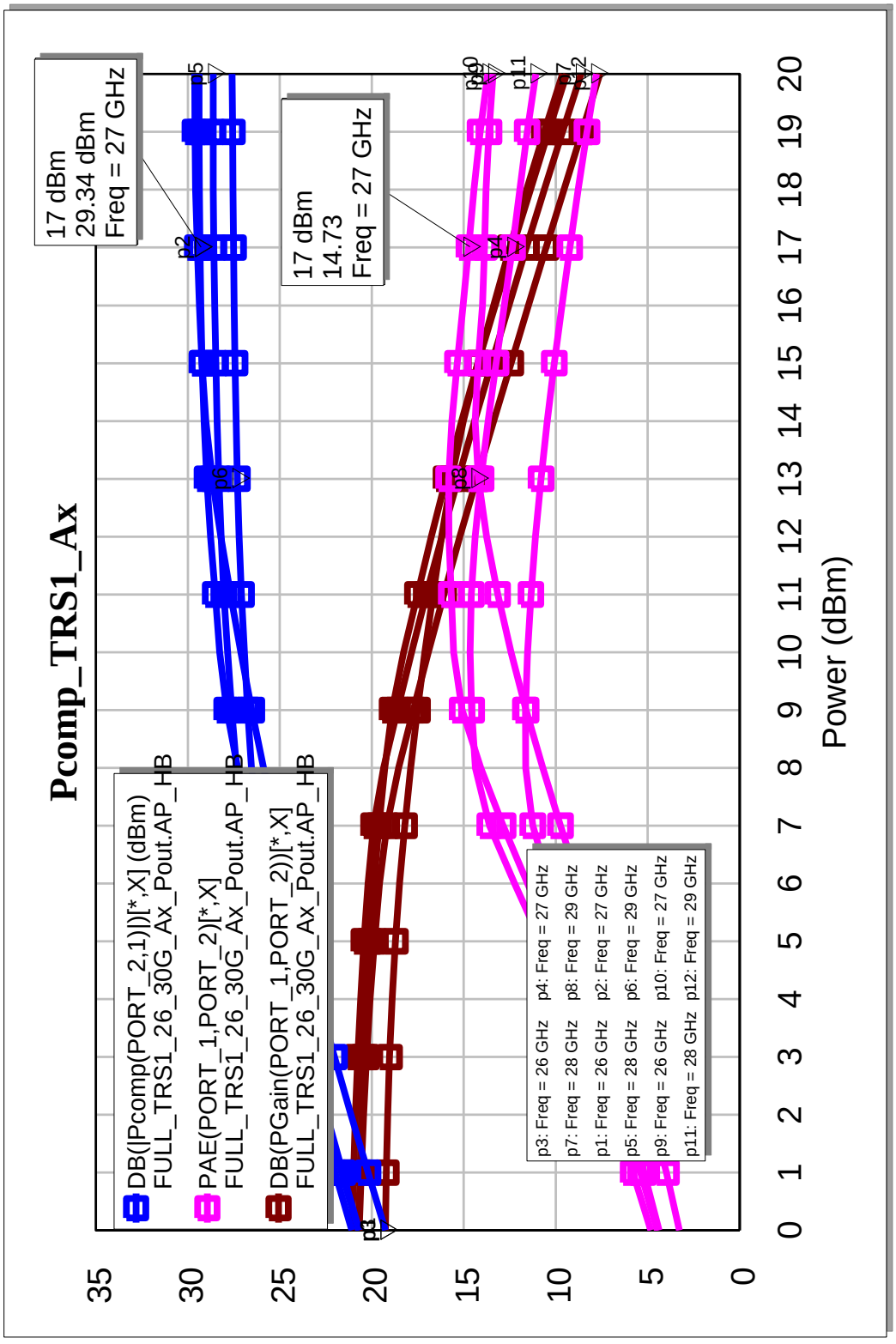

Fig. 61 Power performance simulation (pout, PAE, gain) full EM layout, TRS 1 PA (28 V)

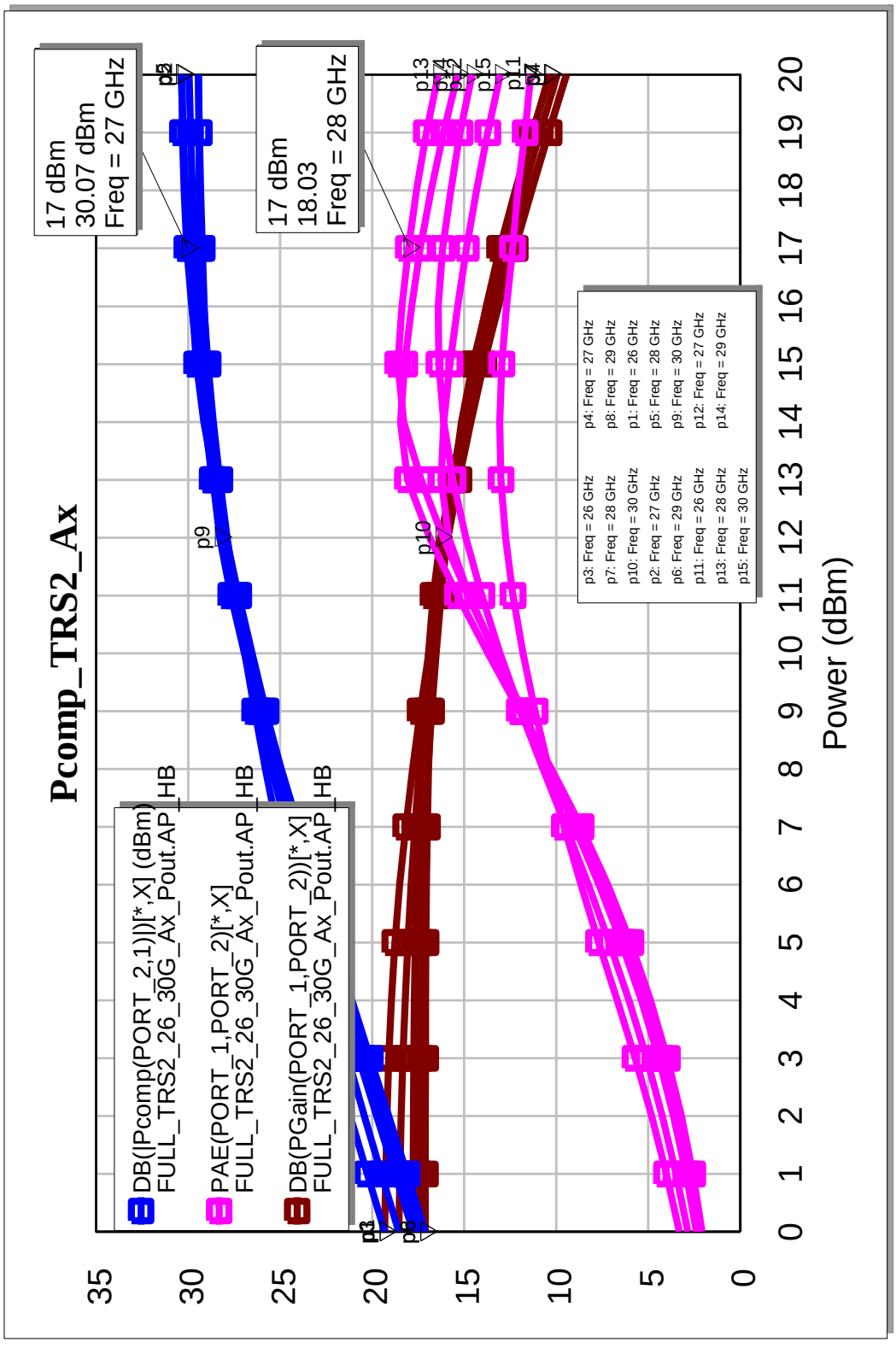

Fig. 62 Power performance simulation (pout, PAE, gain) full EM layout, TRS 2 PA (28 V)

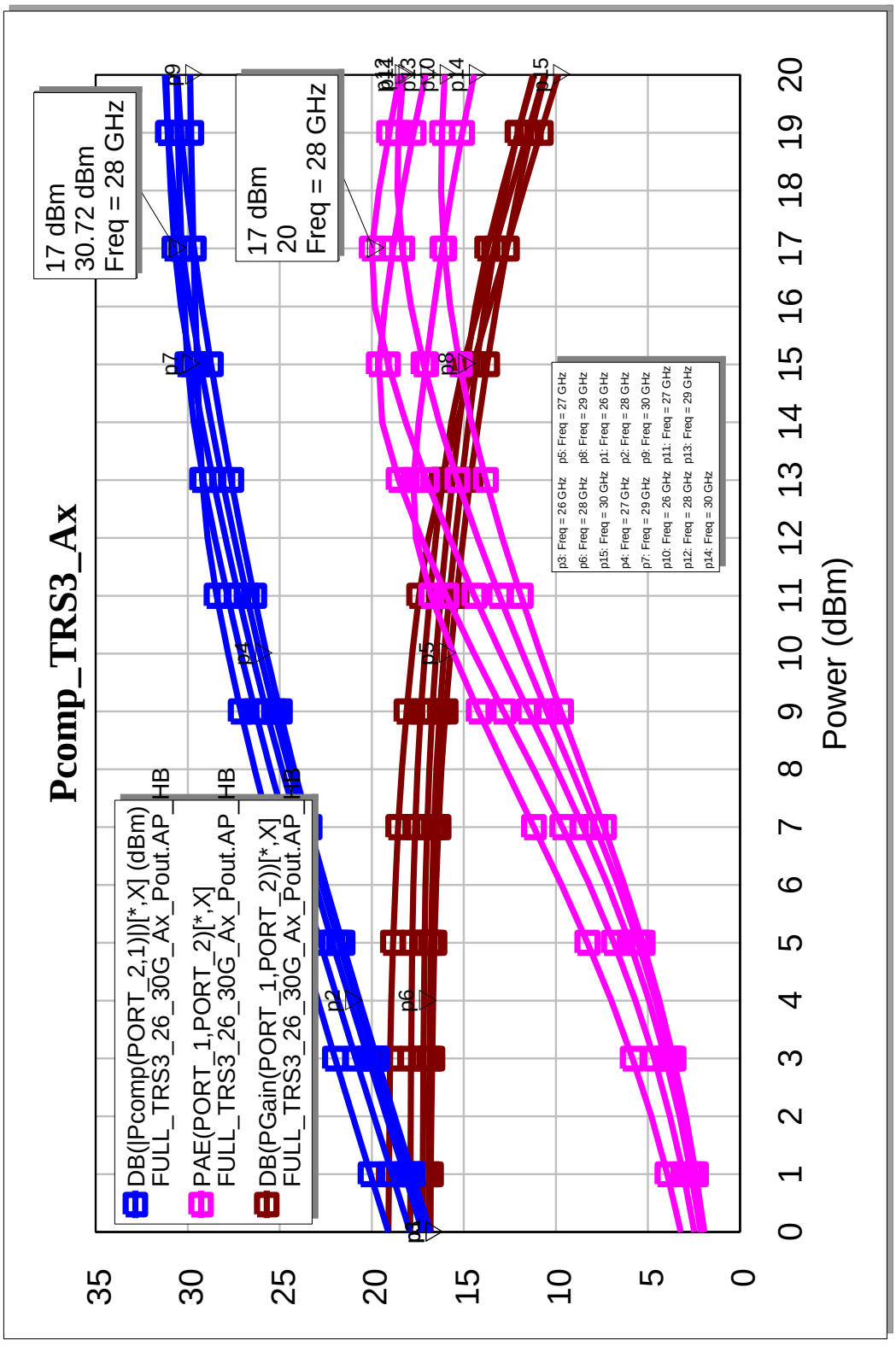

Fig. 63 Power performance simulation (pout, PAE, gain) full EM layout, TRS 3 PA (28 V)

8. Summary and Conclusion

The US Army Combat Capabilities Development Command Army Research Laboratory (ARL) has been evaluating and designing efficient, broadband, high-power amplifiers for use in sensors, communications, networking, and electronic warfare. ARL submitted designs of Ka-band low-noise amplifiers, power amplifiers, and transmit–receive switches using Qorvo's high-performance 0.15-μm gallium nitride fabrication process. These designs for a Ka-band and T/R module using Qorvo's 0.15-μm GaN process were fabricated and tested, and were documented in a prior technical report.[1] The goals were for broad Ka-band circuits with excellent performance in extremely compact sizes. The transmit power goal was 1/2 W to 1 W, so one-stage and two-stage power amplifiers using 4- × 50-μm and 8- × 50-μm HEMTs were designed and tested with good comparison with the original simulations. For the LNAs, models were provided for a couple of HEMT sizes, so two alternate approaches were used: one with a 4- × 25-μm and the other with a 6- × 25-μm HEMT. The 4- × 25-μm one- and two-stage LNAs matched very well with prior simulations. Unfortunately, noise measurements have not been done to verify the expected performance, but the hope is to complete those in the future. It is difficult to get around the parasitic switch capacitance of an "OFF" HEMT switch at these high Ka-band frequencies, so a spiral inductor was used to achieve several GHz of optimal performance for two different SPDT designs: one with a series and shunt switch configuration and the other with only a single shunt switch combined with a compact equivalent quarter-wave line circuit. Both SPDT switches worked surprisingly well and compared well with simulations. The insertion loss of the two switches were comparable but the isolation was better with the series/shunt SPDT switch.

Individual amplifier circuits were very successful, as were the individual switch designs. Three variations of a T/R module were fabricated for comparison and to increase the chances of success. The first module used a single series/shunt SPDT switch to connect the LNA and PA to a common input/output, typically the "antenna" connection. This T/R Module 1 worked quite well and performance was as expected considering the 1.5 dB of insertion loss for the switch, which affects the noise figure of the receiver and the efficiency and output power of the transmitter. Two module variations with two SPDT switches for a common input/output on both the left and right of the layout, to make a bidirectional amplifier, were fabricated. All the layouts fit in a small 2-mm × 1.5-mm die size. One variation used the shunt switch plus 1/4-wave line approach while the other used the series/shunt switch approach. These last two modules varied more noticeably from initial predictions, possibly due to process variation, sensitivity to mismatch, and the reactance of the switches of the SPDT. Some variance could be

due to unsimulated layout parasitics, though a full EM simulation of their layouts was performed, making that possibility seem less likely. Future redesigns could tweak these broadband designs; possibly, a different T/R switch would help. Measurements of the individual amplifiers and switches in a 50-Ω system predict results closer to the original simulations, yet the actual measurements show much more sensitivity to DC biases, parasitics, and intercircuit mismatch. Overall, most designs performed close to expectations. Amplifiers were stable at many biases, though due to large performance changes with drain bias, LNAs are best at 10-V bias and the power amplifiers at 28 V. Some of the modules were packaged and the wire bonds need to be very short, otherwise they tend to resonate in the band and create peaks in the normally flat several-GHz gain bandwidth. Larger systems may use isolators, and so forth, to reduce interactions among successive components, but isolators and attenuators can be large, while these designs were intended for compact, efficient, good performance.

9. References

1. Penn JE, Darwish A. Ka-Band front-end monolithic microwave integrated circuits (MMICs) and transmit–receive (T/R) modules. Adelphi (MD): CCDC Army Research Laboratory (US); 2019 Nov. ARL-TR-8855.

List of Symbols, Abbreviations, and Acronyms

2-D	2-dimensional
3-D	3-dimensional
ARL	US Army Research Laboratory
DC	direct current
EM	electromagnetic
EW	electronic warfare
GaN	gallium nitride
GSG	ground–signal–ground
HEMT	high-electron-mobility transistor
LNA	low-noise amplifier
MMIC	monolithic microwave integrated circuit
PA	power amplifier
PAE	power-added efficiency
PDK	process design kit
PWO	Prototype Wafer Option
RF	radio frequency
SPDT	single-pull double-throw
SPDT–SO	SPDT shunt only (switch)
SPDT–SS	SPDT series/shunt (switch)
T/R	transmit–receive

1 (PDF)	DEFENSE TECHNICAL INFORMATION CTR DTIC OCA
1 (PDF)	CCDC ARL FCDD RLD CL TECH LIB
10 (PDF)	CCDC ARL FCDD RLS E
1 (HC)	R DEL ROSARIO
	A DARWISH
	FCDD RLS ER
	T IVANOV
	P GADFORT
	S HAWASLI
	K KINGKEO
	K MCKNIGHT
	J PENN (1 HC)
	E VIVEIROS
	J WILSON