AFRL-RY-WP-TR-2020-0045

SCALABLE MILLIMETER-WAVE ARRAYS BASED ON DUAL-USE 3D HETEROGENEOUS ARCHITECTURES

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APRIL 2020
Final Report

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
April 2020	Final	22 July 2016 – 30 June 2019

4. TITLE AND SUBTITLE
SCALABLE MILLIMETER WAVE ARRAYS BASED ON DUAL-USE 3D HETEROGENEOUS ARCHITECTURES

5a. CONTRACT NUMBER
FA8650-16-1-7644

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
N/A

6. AUTHOR(S)
Harish Krishnaswamy

5d. PROJECT NUMBER
N/A

5e. TASK NUMBER
N/A

5f. WORK UNIT NUMBER
Y1JL

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Columbia University
116th and Broadway
New York, NY 10027

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Air Force Research Laboratory
Sensors Directorate
Wright-Patterson Air Force Base, OH
45433-7320
Air Force Materiel Command
United States Air Force

Defense Advanced Research Projects Agency
(DARPA/MTO)
675 North Randolph Street
Arlington, VA 22203

10. SPONSORING/MONITORING AGENCY ACRONYM(S)
AFRL/RYDI

11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)
AFRL-RY-WP-TR-2020-0045

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with The Under Secretary of Defense memorandum dated 24 May 2010 and AFRL/DSO policy clarification email dated 13 January 2020. This report is available to the general public, including foreign nationals. This material is based on research sponsored by Air Force Research laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) under agreement number FA8650-16-1-7644. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies of endorsements, either expressed or implied, of AFRL and DARPA or the U.S. Government. Report contains color.

14. ABSTRACT
This project explored the frequency-division multiple access (FDMA) concept to enable 4-element multiple-input and multiple-output (MIMO) transmit and receive arrays at 60 GHz and 28GHz with a single wire interface. Such arrays enable many functionalities in large-scale mm-wave MIMO arrays that cannot be supported by traditional phased arrays, including full digital beamforming, simultaneous multi-beam formation, mm-wave spatial multiplexing, and per-power amplifier digital pre-distortion. A 28GHz 4-element MIMO beam-space array with simultaneous spatial filtering and single wire frequency-domain multiplexing has been demonstrated in 65nm complementary metal-oxide-semiconductor. Also demonstrated was a novel 60GHz 4-element MIMO transmitter with a single-wire interface that multiplexes the baseband signals of all elements (and the local oscillator reference) through frequency-domain multiplexing.

15. SUBJECT TERMS
frequency-division multiple access, transmit and receive arrays, digital beamforming

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT:	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON (Monitor)
a. REPORT	b. ABSTRACT	c. THIS PAGE			Paul Watson
Unclassified	Unclassified	Unclassified	SAR	33	19b. TELEPHONE NUMBER *(Include Area Code)* N/A

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1.1 Design and Measurement of 28 GHz MIMO Multi-BeamFlexer (Multi-Beamformer and Frequency domain multi-pLexer)

A 28GHz 4-element multiple input multiple output (MIMO) beam-space array with simultaneous spatial filtering and single wire frequency-domain multiplexing has been demonstrated in 65nm complimentary metal oxide semiconductor (CMOS). We propose a reconfigurable harmonic rejection mixer (HRM) based beam-space receive (RX) architecture that achieves both (a) multi-beam formation/spatial filtering through harmonic weighting and (b) frequency-domain multiplexing of multiple beam-space outputs to preserve full MIMO field-of-view for four elements with a single intermediate frequency (IF) interface (see Figure 1). System is capable of single element radio frequency (RF) to baseband (BB) gain of ~17 decibels (dB) across odd harmonics (1st, 3rd, 5th and 7th) of low frequency LO2 with a noise figure (NF) of 6-8 dB across bands.

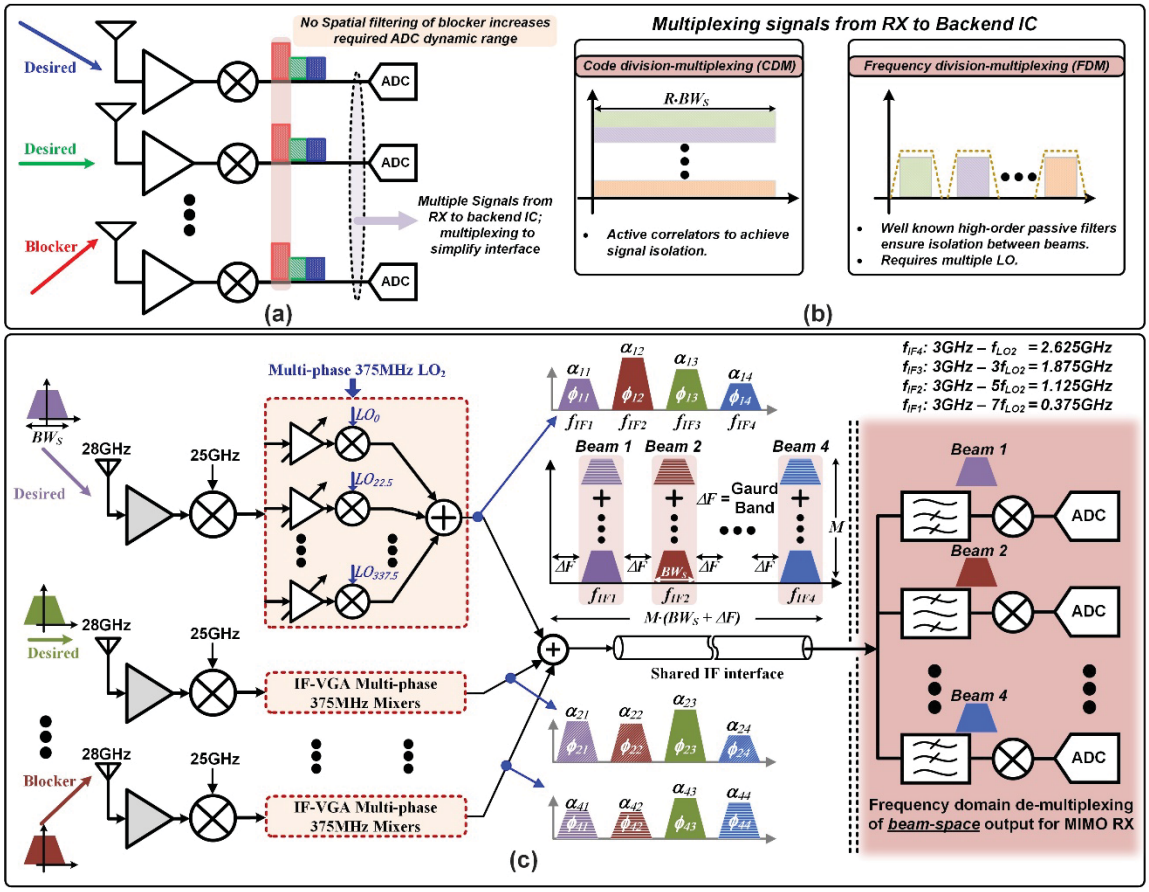

Figure 1: (a) Digital Beamforming in presence of a Blocker, (b) Multiplexing Solutions for efficient IF Interfaces, and (c) Proposed 28-GHz MIMO Beam-Space Array with simultaneous Spatial Filtering and single Wire Frequency-Domain Multiplexing

1.2 Design and Measurement of 60 GHz MIMO Transmitter Based on Frequency Domain Multiplexing

We also demonstrated a novel 60 GHz 4-element MIMO transmitter with a single-wire interface that multiplexes the baseband signals of all elements (and the LO reference) through frequency-domain multiplexing (see Figure 2). The proposed architecture has been implemented in 45 nm RF silicon on insulator (SOI) CMOS for experimental demonstration. The single-wire interface can support 8GHz total IF bandwidth across the 4 channels with 30-40dB spurious free dynamic range (SFDR). Each transmit (TX) in the array achieves 20-35 dB conversion gain and 8.8-10.9 dBm OP1dB while maintaining a channel-to-channel isolation > 30 dB. System level measurements show the ability of the MIMO chip to form multiple simultaneous independent beams carrying independent signals.

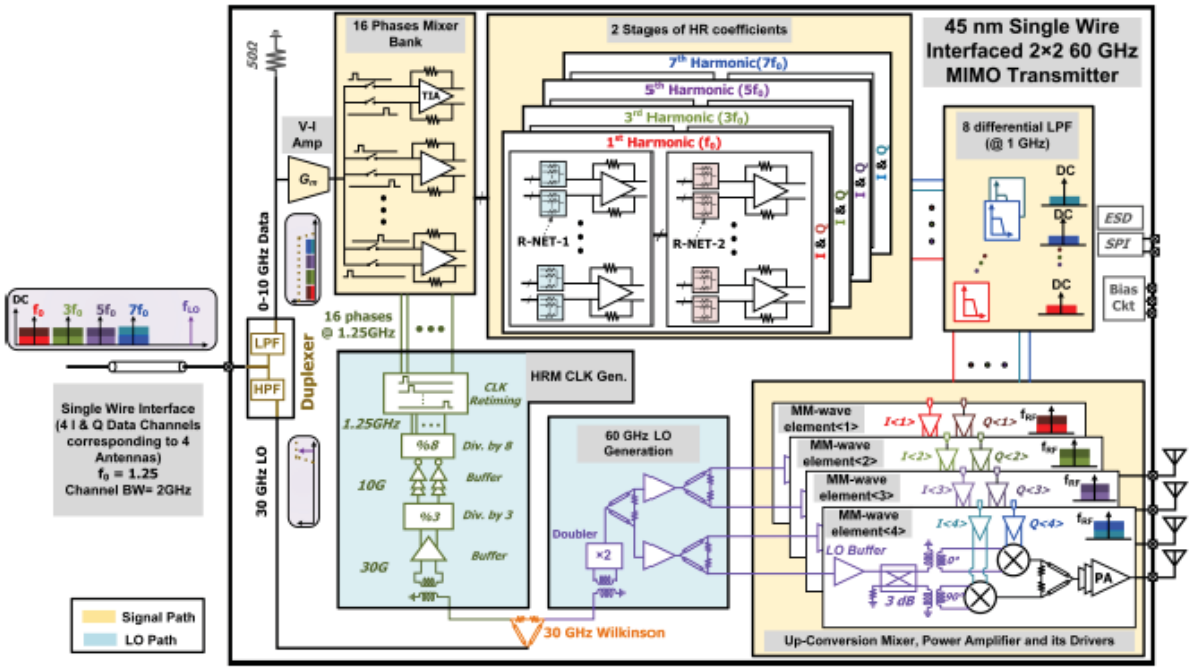

Figure 2: Proposed approach for a Scalable Tiled MIMO Array with a BB Interface over a Single Wire with Frequency-Domain Duplexing

The 60 GHz MIMO TX array with frequency-domain BB multiplexing on a single-wire interface was implemented in 45 nm RF SOI CMOS

2. 28 GHZ MIMO MULTI-BEAMFLEXER DETAILED RESEARCH SUMMARY

2.1 Introduction to 28 GHz MIMO Multi-BeamFlexer

High data-rate wireless links at mm-wave have motivated the development of scalable, dense arrays with hundreds of elements [1, 2]. The evolution from multiple-input single- output phased arrays towards multi-beam/MIMO arrays presents significant challenges. Firstly, increasing the number of beamforming blocks and outputs to preserve signals from every element increases integrated circuit (IC) area and makes compact on-package signal routing challenging. This limits a scalable unit-tile approach with $\frac{\lambda}{2} \times \frac{\lambda}{2}$ spacing. Secondly, it is important to include spatial filtering in such MIMO arrays to mitigate blockers and reduce analog to digital convertor (ADC) dynamic range requirements (Figure 1(a)) [3–5]. Thirdly, traditional digital beamforming requires the full aggregate IF interface bandwidth and all ADCs to operate irrespective of number of beams. Given dynamic operating environments, it is desirable to have array architectures that support power-scalable configurability from phased-array to multi-beam array to full field-of-view (FoV) MIMO arrays.

A single coaxial interface with frequency domain multiplexing (FDM) of local oscillator (LO), and IF (after array combining) has been demonstrated for scalable arrays at 60GHz [1]. However, only the combined signal is preserved and element-level signals are not available for multi-beamforming. Signals from different elements can be multiplexed on to a single IF interface through CDM [2, 3] or FDM. Code domain multiplexing (CDM) requires the use of cascaded active correlators to achieve high isolation between signals leading to power consumption challenges. FDM can leverage well-known high-order passive filter design for improved isolation but requires multiple on-chip LO. Additionally, while spatial filtering prior to digitization has been demonstrated through beamformers [4–6], forming multiple beams or nulls requires larger number of beam-formers leading to increased IC area [5, 6].

2.2 Proposed 28 GHz MIMO Multi-BeamFlexer

In this work, we propose a reconfigurable harmonic-mixing based beam-space RX architecture that achieves both (a) multi-beam formation/spatial filtering through harmonic weighting and (b) frequency-domain multiplexing of multiple beam-space outputs to preserve full MIMO field-of-view for four elements with a single IF interface (Figure 1(c)). The proposed beam-space concept results in a compact 3.4mm x 3.1mm four-element 28GHz array in 65nm CMOS, capable of forming four independent beams with ≥ 400MHz 3dB bandwidth (BW) and FDM on to a single IF interface. The array consumes 450mW and achieves ≥ 27 dB beam-to-beam isolation over 150MHz BW, while consuming 28.1mW/stream/beam and occupying 10.46mm^2 (0.67mm^2/element/stream) at 28GHz. Concurrent MIMO measurements with two wireless 28GHz beams are shown at 400Mb/s (100Mb/s, 16QAM) data rate demonstrating mm-wave MIMO operation.

2.3 Design of 28 GHz MIMO Multi-BeamFlexer

While the system diagram is shown in Figure 3, block level design is described in this section. 28-GHz input is down-converted to the IF using a 2-step down-conversion. First down-conversion utilizes a high frequency LO1 (25GHz) to convert the received RF input to 3 GHz f_{IF0} and the second down-conversion is a harmonic mixing operation which translates the f_{IF0} to four different IF frequencies of f_{IF1}, f_{IF2}, f_{IF3} and f_{IF4}.

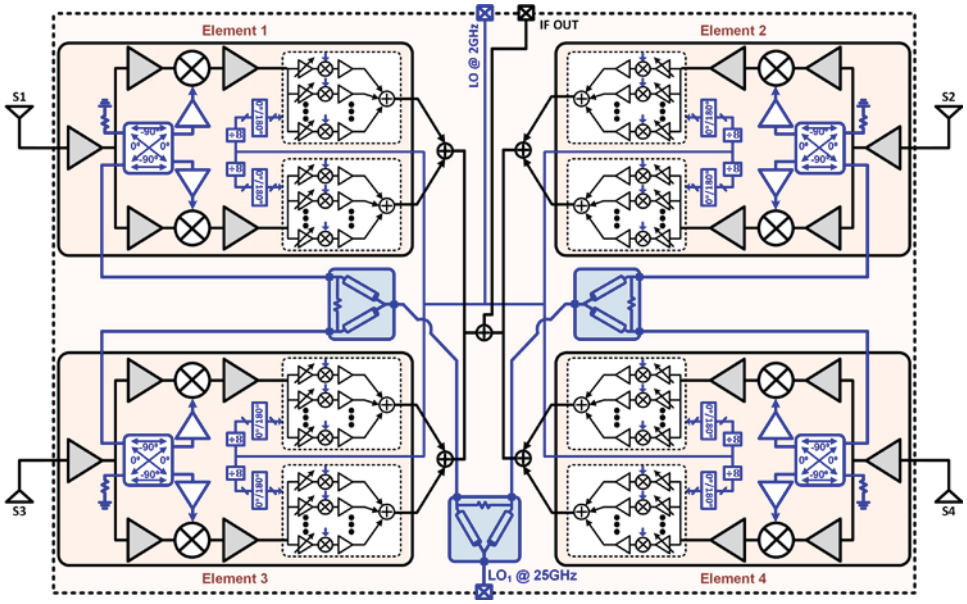

Figure 3: System Architecture of proposed 28-GHz MIMO Beam-Space Array with simultaneous Spatial Filtering and Single Wire Frequency-Domain Multiplexing

28 GHz Signal Path: In each element, the RF input is amplified by a source-degenerated low noise amplifier (LNA), split into I and Q paths and down-converted to 3GHz by the LO1 Gilbert-cell mixer as shown in Figure 4. LNA stage is input matched to 50 Ω with on-chip LC network, and IC pad to printed circuit board (PCB) wire-bond inductance is absorbed in to an on-board CLC-LC network which provides wide-band match around frequency of interest. Single-ended I and Q LNAs aren't source degenerated to extract higher gain from the stage and don't have input and output 50 Ω match. Two baluns convert I and Q LNA outputs to differential and drive Gilbert cell balanced mixers with 1-bit tunable loads at IF1. High-frequency mixer is driven by buffer LO1 network mentioned in Section 2.2.

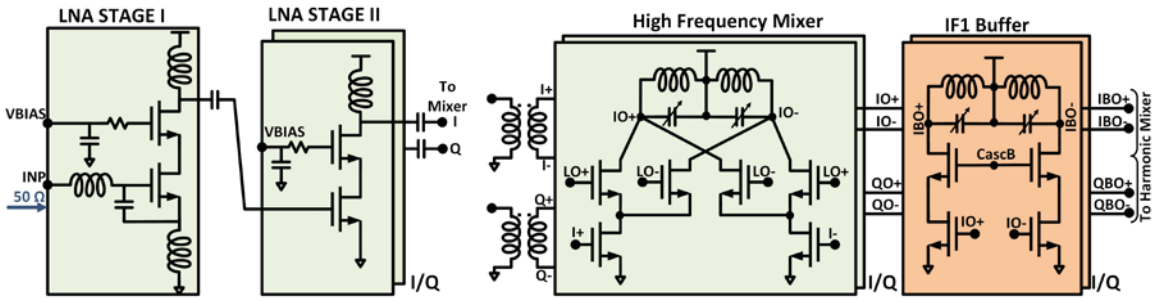

Figure 4: 28 GHz Signal Path with LNA, high Frequency Gilbert-Cell Mixer and IF Buffer to drive 8-path IF

LO Path: 25GHz high frequency quadrature LO1 is required for each element to drive the first down-conversion mixer. The LO1 distribution as shown in Figure 5 consists of three Wilkinson dividers to symmetrically divide the input power among 4-elements. Further, each element generates quadrature signals from local hybrid couplers. Balun converts the single-ended LO1 to differential and output is then buffered to drive the Gilbert-cell mixer.

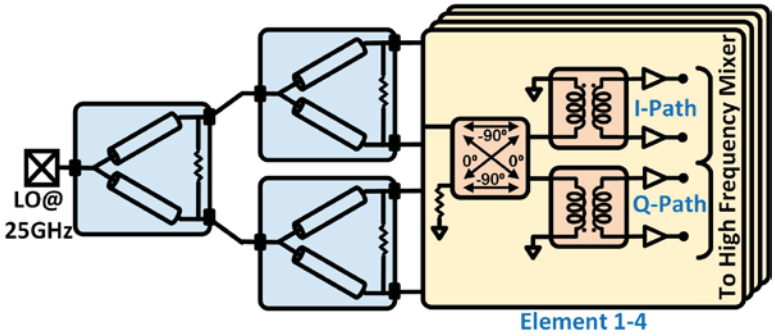

Figure 5: 25 GHz LO1 Distribution Network to drive the 4-Elements' I and Q High-Frequency Mixers

Harmonic mixer and IF path: As shown in Figure 1, the input signal in each element is multiplied with 50 % duty-cycle 16-phase LO2 in the proposed scheme. Each mixer creates IF outputs corresponding to LO2 fundamental and odd harmonics. Applying suitable weights to each of the multi-phase mixers creates down-converted IF signals with independent desired phase/amplitude at f_{IF1}, f_{IF2}, f_{IF3} and f_{IF4}.

IF path includes a 4-bit variable gain amplifier (VGA) consisting of scaled complementary-gm cells to assign the appropriate weights to each phase of the LO2. Setting the appropriate weights coefficients leads to desirable elemental phase and gain at the IF outputs. Please note that the phase and gain for each element and at each of f_{IF1}, f_{IF2}, f_{IF3} and f_{IF4} can be set independent of each other as shown in Figure 1(c). IF path utilizes passive mixer topology for harmonic mixing, it is followed by an inverter based transimpedance amplifier (TIA) which acts a buffer and ensures the current mode operation of the VGA and passive mixer as shown in Figure 6(a). Output are then buffered before the summing stage and buffers are designed appropriately to ensure wide-band IF operation as well low common mode gain as shown in Figure 6(b).

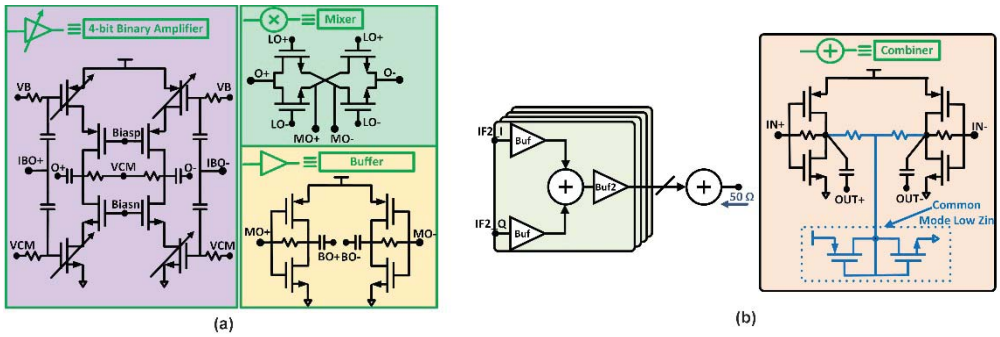

Figure 6: 4-bit VGA, Passive Mixer, and Summing Buffers in the IF Path

2.4 Measured Performance

28 GHz MIMO Multi-Beamflexer is implemented in 65nm CMOS and occupies 3.150mm x 3.375mm area as shown in Figure 7. The multi-beam capabilities of the array are shown in Figure 10 where the array is configured to receive from beams pointing at -30˚, -15˚, 0˚, and 45˚ angle-of-incidence (AoI) at f_{IF1}, f_{IF2}, f_{IF3} and f_{IF4}, respectively demonstrating concurrent multi-beam operation as well as the FDM of beam-space outputs. The array also supports spatial nulling to reject interferers [4–6] as shown in Figure 10 where four independent 20dB to 35dB spatial nulls are formed for each elements output which is also FDM to f_{IF1}, f_{IF2}, f_{IF3} and f_{IF4}.

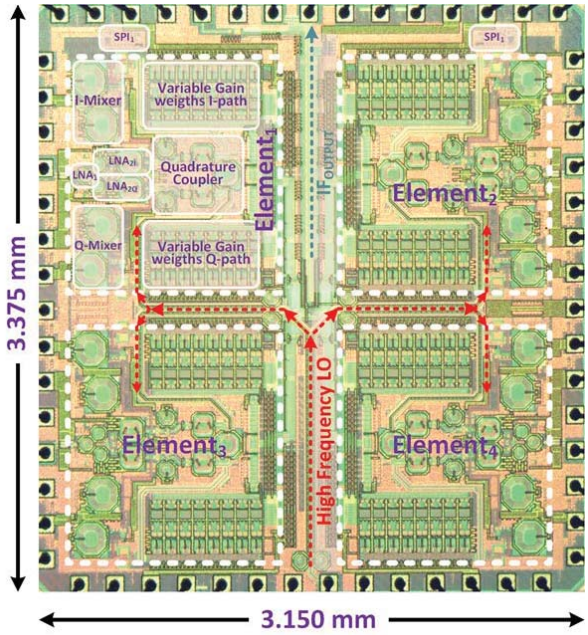

Figure 7: Die Micro-Photograph of 4-element 28 GHz Spatial Filtering and Frequency Multiplexing MIMO Array

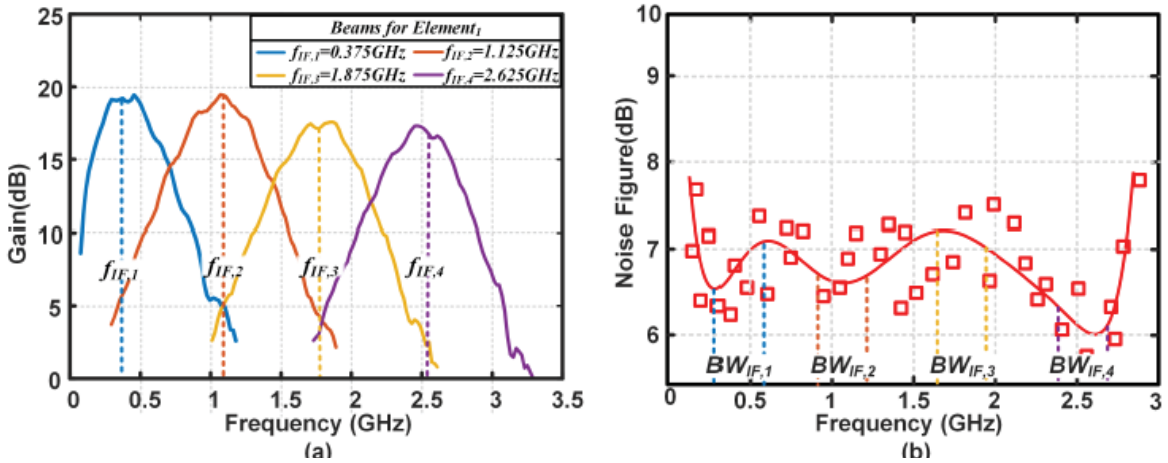

Figure 8: Single-Element (a) RF to BB Gain and (b) NF measured when Element configured to translate Output to four IF Frequencies

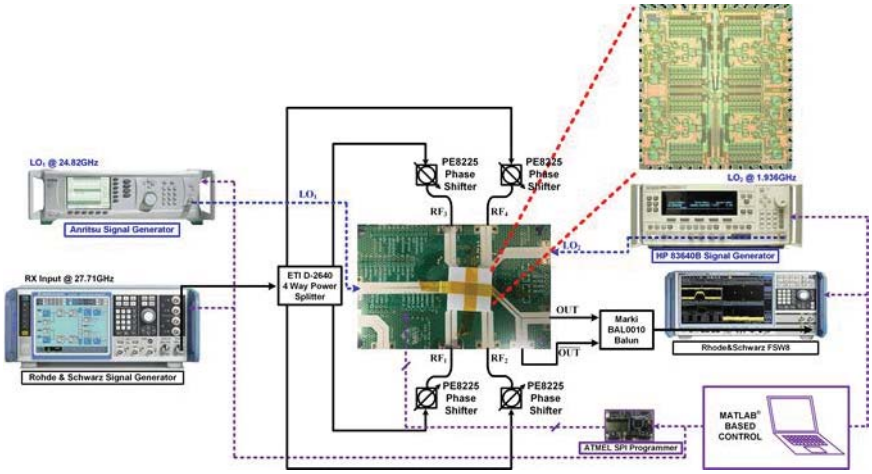

Figure 9: Measurement Setup to demonstrate Spatial Filtered and Frequency Multiplexed Beamforming using the 28 GHz MIMO Array

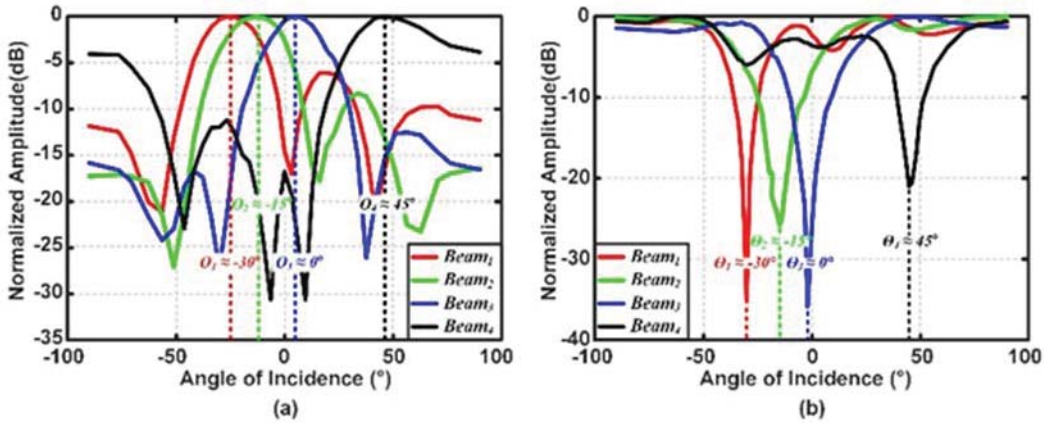

Figure 10: (a) Measured Pattern for four Beams formed using Weighted Harmonic Mixing, demonstrating Multi-Beam Formation as well as Frequency-Domain Multiplexing of Beams and (b) Measured Pattern with Array configured to form Spatial Nulls

This is further demonstrated in Figure 11, where the patterns at f_{IF1}, f_{IF2}, and f_{IF4} are configured such that they are nulled at the AoI corresponding to the peak of beam at f_{IF2}. A 150MS/s 64-QAM modulated signal is fed through an external phase-shifter array, and Figure 11 shows the relative power in the desired beam at f_{IF3} and the residue at f_{IF1}, f_{IF2}, and f_{IF4} (limited by theoretical spatial nulling bandwidths, phase/amplitude resolution). The FDM achieves ≥27dB beam-space isolation demonstrating the feasibility of multi-beam MIMO operation.

A 28GHz aperture-coupled patch antenna for wireless over-the-air (OTA) testing is built on a 3 layer Rogers4350B PCB as shown in Figure 12. Bottom layer on the PCB acts as path antenna and the middle-layer is slotted ground plane. 4-antennas spaced λ apart are connected to the southwest connectors via 50Ω feed line. S-parameters are measured for input matching and $S_XX \geq 10$ across the frequency of interest.

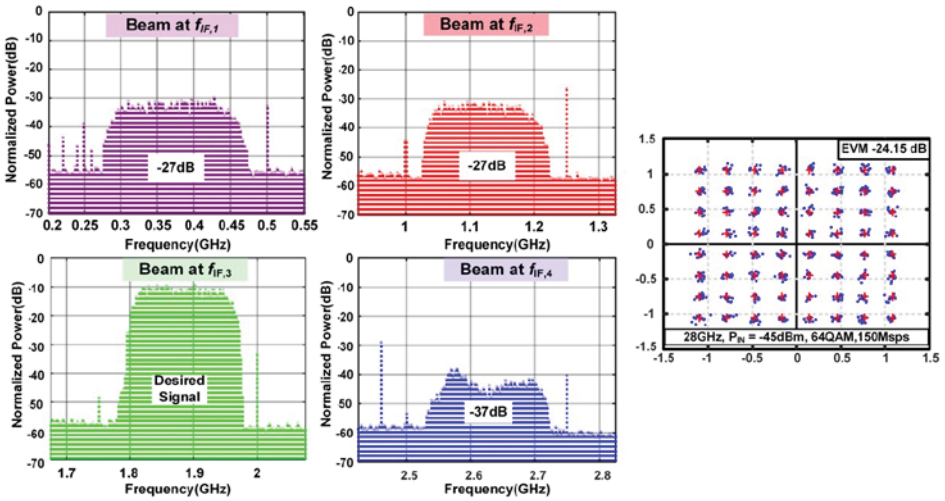

Figure 11: Measured Beam-to-Beam Isolation with Array forming Peak for AoI_x at f_{IF3} while forming Nulls at that AoI for Beam Outputs at f_{IF1}, f_{IF2} and f_{IF4}

The array shows 27 dB isolation from beam-to-beam for 150MHz BW 64QAM signal at 28GHz

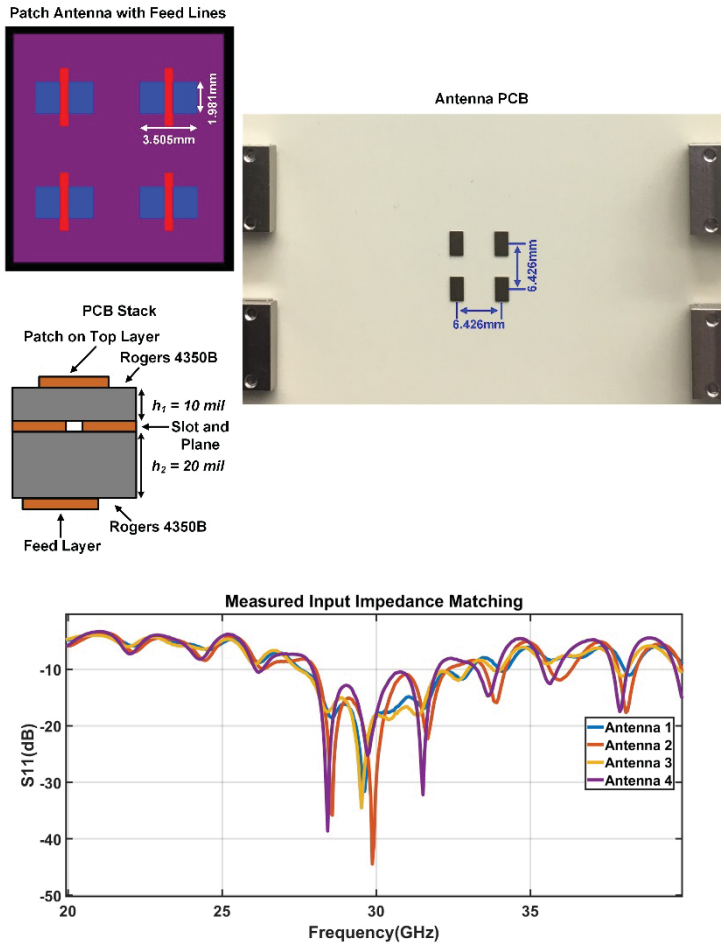

Figure 12: (a) 28GHz Aperture-Coupled Patch Antenna use for Wireless OTA Testing and (b) Measured Input Match (Sxx) for the 4 Antennas

Figure 13(a,b) shows OTA wireless measurements where two 28GHz modulated sources, S_{rc1} and S_{rc2} with equal power radiate towards the array through horn antennas. The four-element IC is connected to a 2x2 28GHz aperture-coupled patch antenna array for wireless measurements. In the first case, S_{rc2} is assumed to be a blocker and is nulled by ≥ 25dB at the RX. The error vector magnitude (EVM) for the 400Mb/s 16QAM wireless signal in Figure 5 only degrades from -27.9dB to -20.2dB with the blocker demonstrating spatial filtering in the RX. In the second case, both S_{rc1} and S_{rc2} are assumed to be desired signals and the RX is configured to receive S_{rc1} and null S_{rc2} at f_{IF1} and vice versa at f_{IF2}.

Figure 13(c) shows the measured EVM for the wireless 2-stream MIMO demonstrating ≤ -16dB EVM for 400Mb/s on both streams concurrently. The IC is compared to state-of-the-art in Figure 13(c). The proposed beam-space FDM RX array is the first to combine both multi-pattern spatial filtering and frequency-domain multiplexing and achieves state-of-the-art power/element/stream at 28GHz. Table 1 shows the performance of the system in comparison with the state-of-the-art beamformers/nullers.

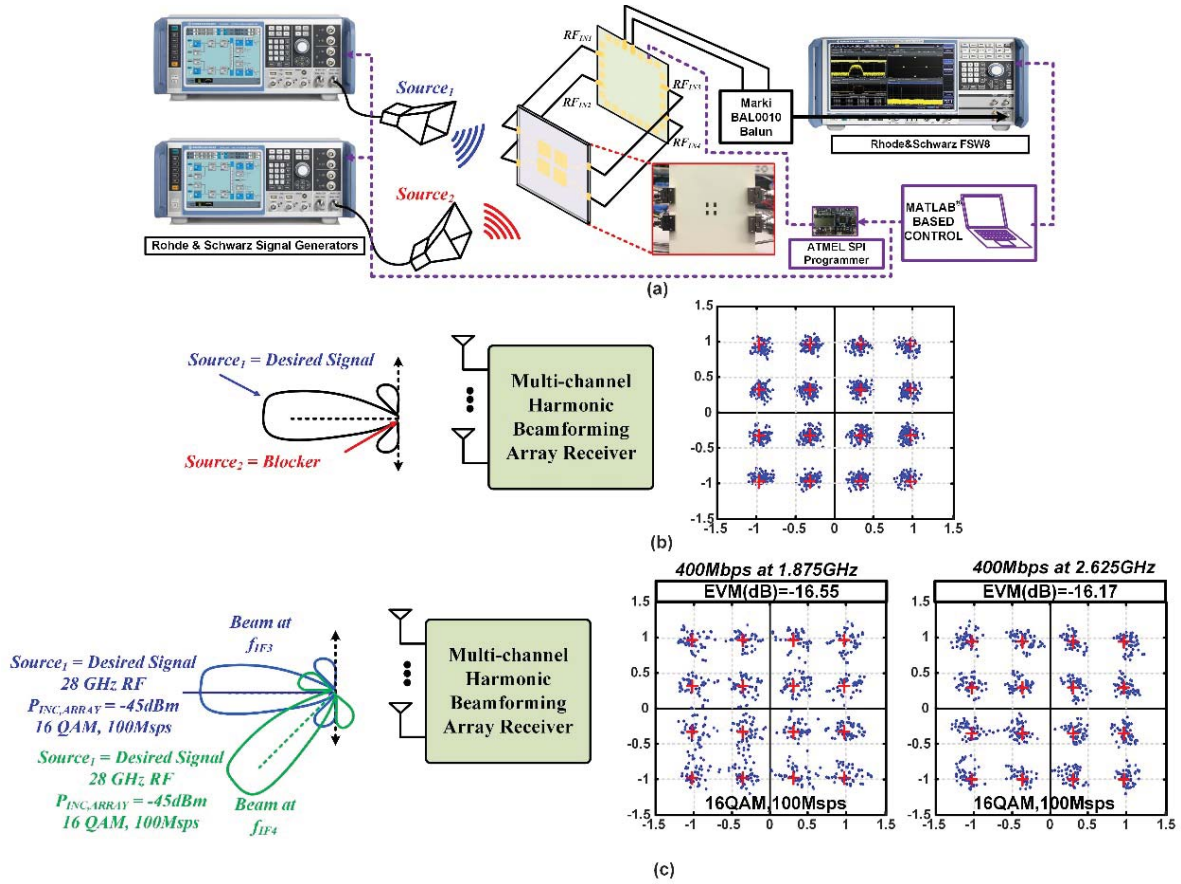

Figure 13: (a) Measurement Setup for OTA Testing, (b) Measured Performance with Beam Nulling (≥ 25dB nulling) shows EVM degrades from -27.95dB to -20.2dB with Source2 enabled, and (c) Measured Performance with two Beams simultaneously incident shows EVM of -16.55dB at 1.875GHz and -16.17dB at 2.625GHz, respectively, for the two Directions

Table 1. Comparison with State-of-the-Art Beamformers/Nullers

[Reference]	[5]	[4]	[6]	[7]	[3]	[8]	[9]	This work
Technology	65nm CMOS	65nm CMOS	45nm RFSoI	65nm CMOS	65nm CMOS	0.18um CMOS	0.18um CMOS	65nm CMOS
Freq.(GHz)	10	0.1-1.7	27-41	27-29.75, 35-38.75	29.2	5.4	5.25	28
No. of Elements	4	4	4	4	4	2	2	4
No. of Outputs	4	4	4	2	4	2	2	4
No. of Beamformers/Null	1	1	3	2	NA	NA	NA	4
IF/RF Multiplexing	No	No	No	No	4x1 Code Domain	2x1 Complex Freq. Domain	2x1 Code Domain	4x1 Freq. Domain
Power (mW)	145.1	140-160	340	310	NR	60.2	75.6	450
Power/Beam/ Element (mW)	NA	35-40	85	52.5	75/element	30.1/element	37.8/element	28.1
Chip Area (mm^2)	3.8	2.25/1.69	23.4	4.5	5.75	2.47	2.32[d], 4.11[e]	10.6
Area/Beam/ Element*	NA	0.56/0.42	5.85	0.46	1.44	1.24	1.16[d], 2.06[e]	0.66
Single Element Conversion Gain (dB)	NR	41	36	33:27-29.75GHz	16	43	21-85	$\geq$ 16
Rx BW (MHz)	NR	NR	NR	2750	NR	NR	45	$\geq$ 450
NF (dB)	8	1.7-4.6	4.3-6.3	5.7: 27-29.75GHz	10	5.5	6.2	6-7.8
P_{1dB} (dBm)	NR	NR	NR	-30:27-29.75GHz	-20	NR	NR	-36.9
Notch Depth (dB)	20	32	62/50/51	NR	No	No	No	27-37
Ch. to Ch. Multiplexing Isolation (dB)	NA	NA	NA	NA	20	NR	NR	27

3. 60 GHZ MIMO TX DETAILED RESEARCH SUMMARY

3.1 Efficient IF Interfaces for MIMO Arrays

Digital MIMO arrays represent the next paradigm for communication and radar systems, enabling spatial multiplexing [10], enhanced radar resolution through virtual arrays [11] and digital beamforming for user discovery/tracking in highly mobile scenarios. Increasing maturity of mm-wave ICs has led to several demonstrations of large-scale *phased* arrays with hundreds of elements at mm-wave [12, 13]. However, digital beamforming (DBF)/MIMO arrays demand per-element digitization, resulting in I/O challenges at mm-wave for large signal bandwidths.

In a large-scale mm-wave array, to ease the scalability, a single-wire interface is desirable to connect each mm-wave MIMO RF front-end chipset to the digital signal processing (DSP) unit. Although serializer/deserializer (SERDES) is traditionally used in high-speed links in computing systems and networks, SERDES circuits are challenged with high-speed operation, intensive equalization, and robustness, and hence require power-hungry buffers and equalizers. The resultant area and power directly impact overall array efficiency and scalability. An alternative is an analog single-wire interface where multiple-element IF signals co-exist on a single-wire using code-domain multiple access (CDMA). However, code-domain multiplexing similar to [14] is not an efficient solution for extremely wideband radios, e.g. 60 GHz WiGig, as code-to-code isolation directly trades off with code length, and consequently signal bandwidth.

In this work, we explore frequency-domain multiplexing of IF/BB signals on a single wire for mm-wave MIMO scalable transmitters. A 60 GHz 4-element MIMO TX with a single- wire interface is implemented in 45nm RF SOI CMOS which can demultiplex 4 signals with 2 GHz Bandwidth (total BW of 10 GHz including guard bands) that are frequency multiplexed on odd harmonics of 1.25 GHz. The key insight is that while higher-order code-domain filters are inaccessible, higher-order frequency-domain filters may be implemented to enhance channel-to-channel isolation without excessive increase in the guard bands. A two-stage wideband harmonic-rejection mixer is employed to separate each elements IF signal from the single-wire interface to zero-IF frequencies with high channel-to-channel isolation.

3.2 Proposed Frequency-Domain Multiplexing on Single-Wire Interface

The proposed architecture that enables the single-wire interface using frequency domain multiplexing is shown in Figure 14. The IF data signals for 4-element TX are placed at the first, third, fifth, and seventh harmonic of 1.25 GHz. A multi-phase low-duty-cycle harmonic-reject mixer is then used with multiple parallel reconstruction weighting banks, each of which reconstructs one of the harmonics while rejecting the others. In order to reduce the mismatch (systematic and random) between real rational and ideal irrational coefficients, and consequently achieve better harmonic rejection, two stages of harmonic rejection (HR) have been used [15]. Unlike [15], these two stages are implemented in the baseband (compared to one stage in the baseband and one stage in RF) which enables us to share a single 16-phase mixer between all desired output paths. This results in lower power consumption and easy LO routing while

maintaining high harmonic rejection. In order to demultiplex four high bandwidth data channels and have a practical LO frequency, we use only odd harmonics of 1.25GHz. The different data channels are then upconverted to the desired 60GHz operating frequency using a conventional TX. The 60 GHz TX array contains four separate TX MIMO elements. Furthermore, multiple chips can be tiled to increase number of channels in the MIMO system.

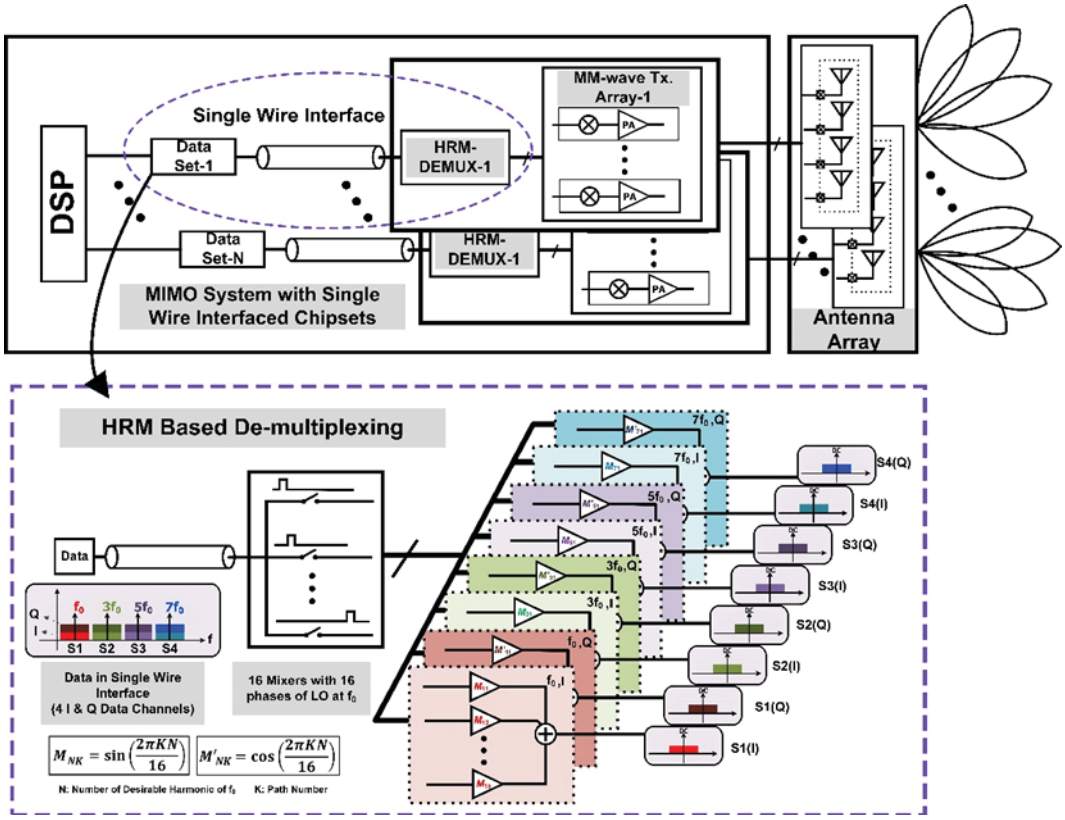

Figure 14: Frequency-Domain Multiplexing-based 4-Element TX in 45nm RF SOI CMOS

3.3 Design of the 60GHz MIMO TX

The block diagram of a 45nm radio frequency silicon on insulator (RFSOI) CMOS 60 GHz 4-element MIMO TX with an frequency division multiple access (FDMA) based IF data and LO reference single-wire interface is shown in Figure 15(a). As mentioned earlier, a duplexer made of a parallel combination of a low pass filter (LPF) and a high pass filter (HPF) is deployed to separate the 0-to-10 GHz IF data from the 30 GHz LO reference. The 30 GHz LO reference is divided by 24 to generate 16-phase of 1.25 GHz clock required by HRM which downconvert each channel into zero-IF using 16-phase of mixing product. Cascading two-stage of HRM enhances the inter-channel leakage to 40 dB in all channels Moreover, the 60 GHz LO is generated by passing the 30 GHz LO reference through a doubler circuit. A 90 hybrid coupler is used to generate the 60 GHz LOs with 0 and 90 phases for performing quadrature upconversion mixing. A 1 GHz, 5th-order elliptic filter is deployed to suppress out-of-band higher-order harmonics at the output of the HRM which results in a clean output mask.

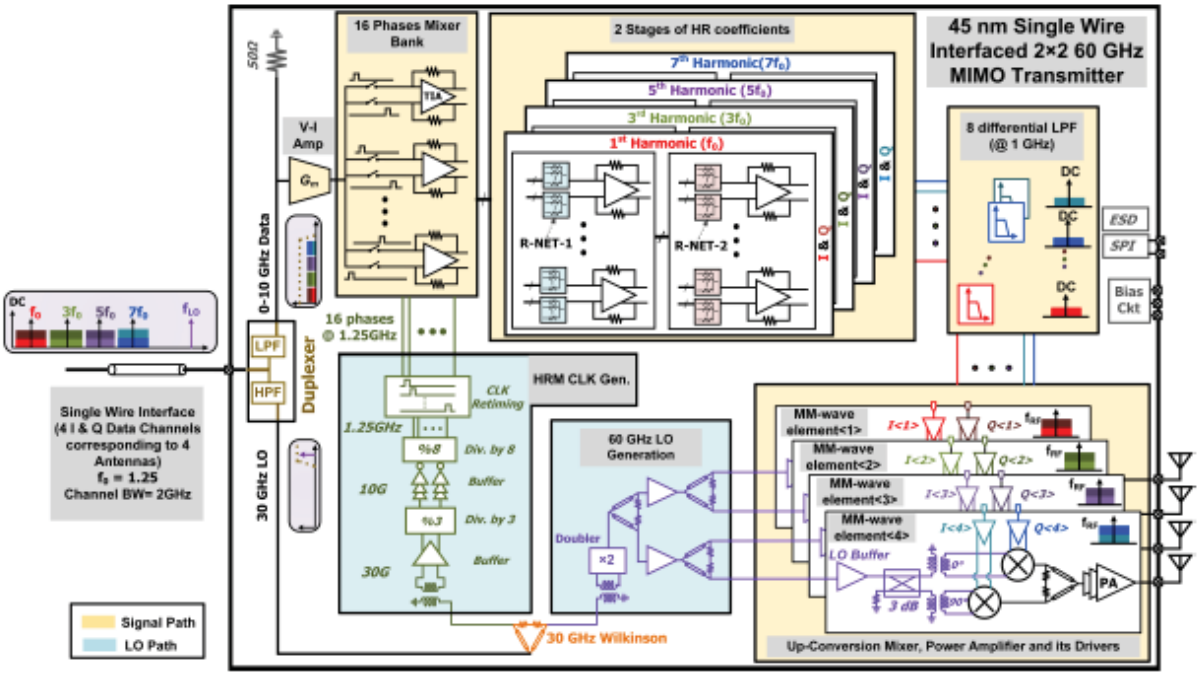

Figure 15: Block Diagram of the implemented 4-Element MIMO TX with FDMA-based IF/BB Data Multiplexing in 45nm RF SOI CMOS

3.3.1 Duplexer

The duplexer circuit details are presented in Figure 16(a), which include the parallel combination of an HPF and an LPF to separate the direct current (DC)-to-10 GHz IF data and the 30 GHz LO signal from the single wire input. The LPF is a passive 5th-order low-pass elliptic filter. Although the pass-band is chosen to be 15 GHz to make sure the filter roll-o does not degrade the IF signal BW (DC-to-10 GHz), it has around 40 dB out-of-band rejection to succulently suppress the 30 GHz reference (see S21 in Figure 16(b)). Similarly, the HPF is also a passive 5th-order high-pass elliptic filter which can reject the IF signal between DC-to-10 GHz by 40 dB with minimum loss at 30 GHz (see S31 in Figure 16(b)).

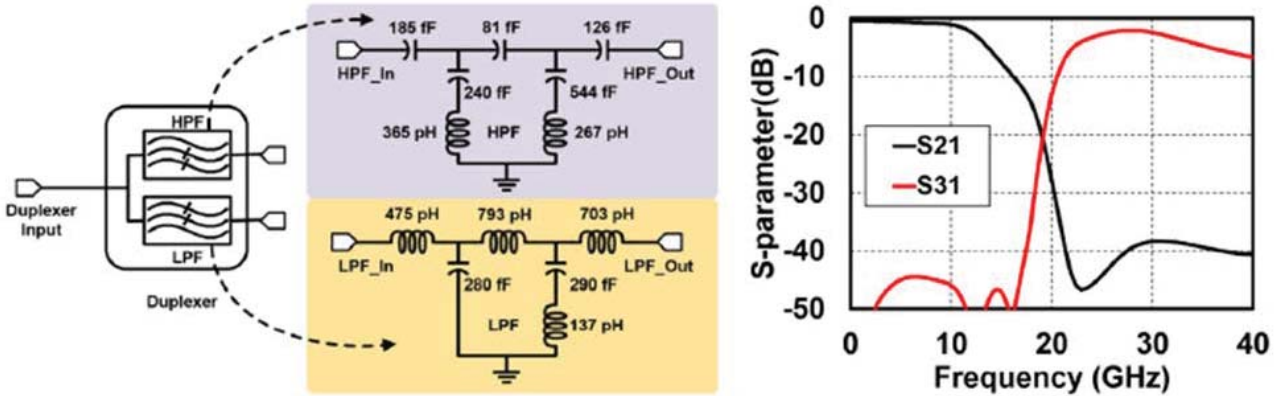

Figure 16: (a) Circuit Implementation of the Duplexer that includes a HPF and LPF to divide the DC-10 GHz IF Data and the 30 GHz LO Signal from the Single Wire Input and (b) Simulated Performance of the Duplexer

3.3.2 Harmonic Reject Mixer

Figure 17(a) shows the circuit diagram of the two-stage HRM. A simple inverter is used at the input as the transconductor to amplify the input signal. A current-mode passive mixer samples input IF signals that are lying at 1st, 3rd, 5th and 7th harmonics of 1.25GHz with 16-phases. Then, sampled signals are buffered using an inverter-based TIA which does not require common-mode feedback and provides common rejection. The ratios required between different samples to achieve harmonic rejection are [0, √(2 - √(2))/2, √ (2)/2, √(2+√(2))/2,1]. These ratios are approximated by a ratio of integer numbers as [0,4,7,9,10] in the first stage and [0,5,9,12,13] in the second stage of the HRM. Post-layout inter-channel HR simulations are shown in Figure 17(b) where the response from the input to all HRM channel outputs are simulated using PSS+PAC in Cadence Spectre. The inter-channel HR is > 40 dB between all channel pairs.

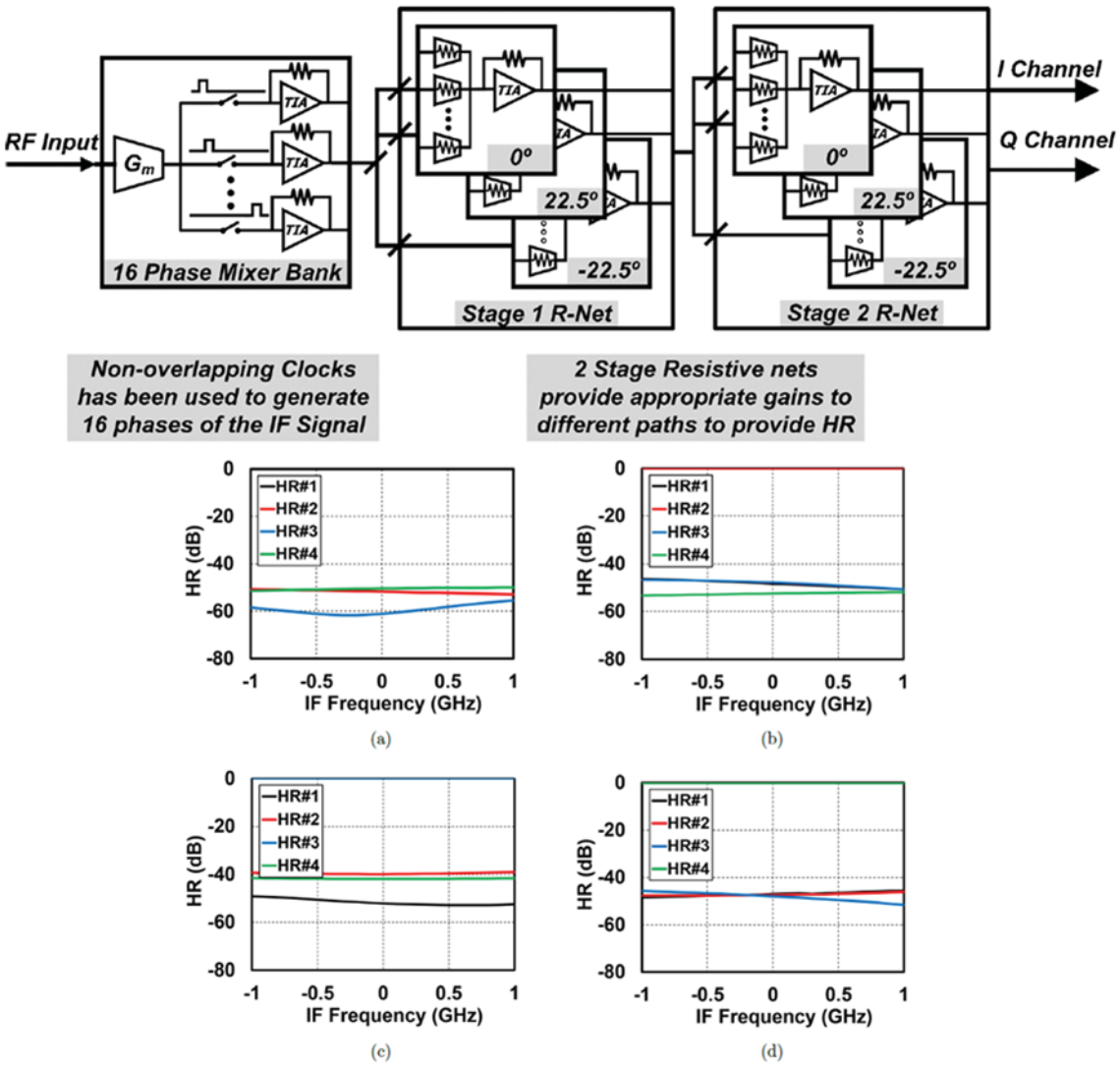

Figure 17: (a) Circuit Implementation of the 2-Stage HRM and (b) Post-Layout Inter-Channel HR Simulation shows HR better than > 40 dB between all Channels

3.3.3 5 GHz LPF

The LPF is a passive 5th-order low-pass elliptic filter. To minimize the LPF area consumption, inductors are implemented differentially which decreases the inductor area by a factor of $2\times(1+k)$, where the factor 2 is due to the fact that sides of differential inductors are implemented on top of each other. $(1 + k)$ takes into account the mutual inductance between positive and negative sides of the differential inductor. Figure 18(b) shows simulation results of the designed LPF where the pass-band corner is around 1 GHz, and suppresses the harmonics at > 1.5 GHz (adjacent channel) by > 40 dB.

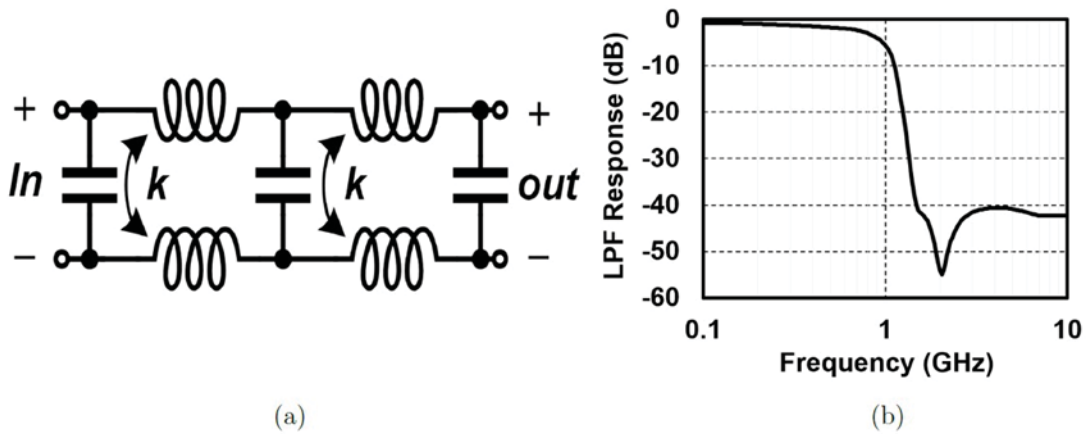

Figure 18: The 5th Order Differential Passive Elliptic LPF - (a) Circuit Diagram and (b) Simulated Performance

3.3.4 60 GHz Mixer

A doubly-balanced Gilbert-cell mixer is used as an upconversion mixer to upconvert each element's BB data to 60 GHz (Figure 19(a)). A balun is employed to convert the single-ended LO signal to differential. A varactor is used at the output of the balun to provide up to 15° programmable phase shift which can be used to enhance I and Q mixer image rejection. Furthermore, a programmable IF amplifier is used to provide initial gain. Figure 19(b) presents the mixer simulation results.

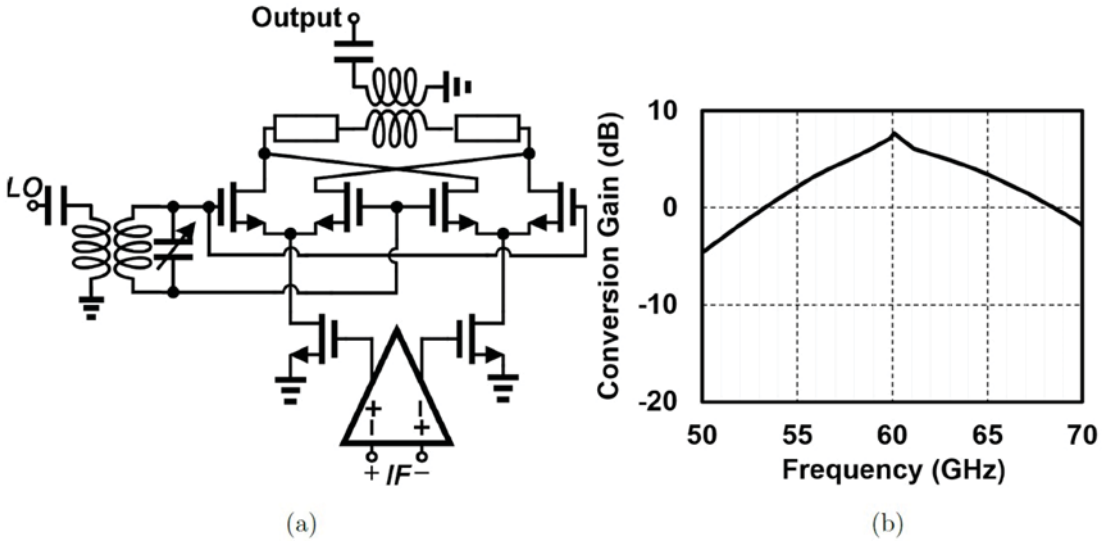

Figure 19: Doubly-balanced Gilbert-Cell Mixer used as Upconversion Mixer with BB Amplifier - (a) Circuit Diagram and (b) Simulated Conversion Gain

3.3.5 60 GHz PA

Figure 20(a) depicts the two-stage class-E-like power amplifier (PA) implemented by stacking two 78×1.25 μm/40 nm coating-body devices to increase the voltage swing at the load. Device sizes, supply voltages, bias voltages, and gate capacitor values are selected based on the theoretical analysis and considerations described in [16]. A multiplicity-based device layout is used to keep a good balance between fmax and fT. The PA achieves a simulated saturated output power of +14 dBm with 22% power-added efficiency (PAE) at 60 GHz, shown in Figure 20(b).

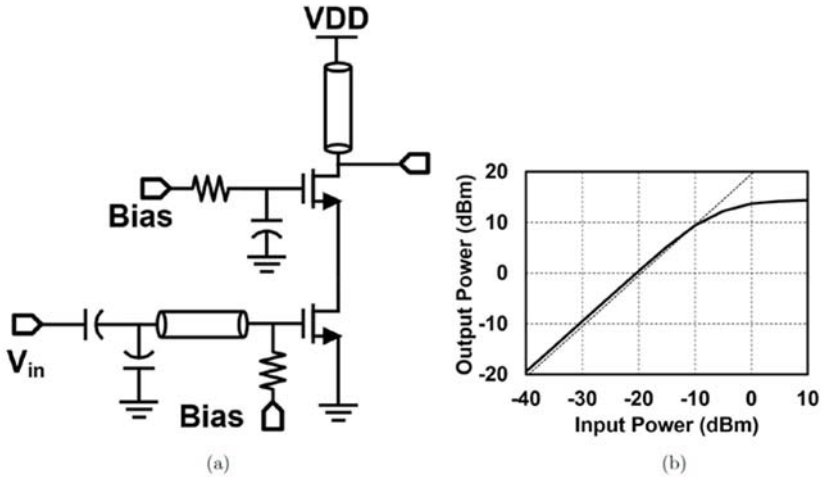

Figure 20: Two Stage Stacked PA - (a) Circuit Diagram and (b) Simulated Performance

3.3.6 LO Path

As shown in Figure 21, the 30 GHz LO, which is separated from the single wire using the duplexer, is fed into a Wilkinson power divider to provide two LO paths - the HRM LO path, and the mm-wave LO path. In the HRM LO path, after amplification, 16 phases of 1.25 GHz are generated using a 50% percent duty cycle divide-by-3 circuit (to generate 10 GHz) followed by a differential Johnson counter divide-by-8 circuit (to generate different phases at 1.25 GHz). These signals are buffered and also retimed with the 10 GHz LO to generate non-overlapping LOs while increasing the phase accuracy. In the mm-wave LO path, the 30 GHz input is fed into a doubler to generate the 60 GHz LO to be used in the mm-wave upconversion mixers. Buffers and Wilkinson power dividers after the doubler generate four 60 GHz LOs for different channels.

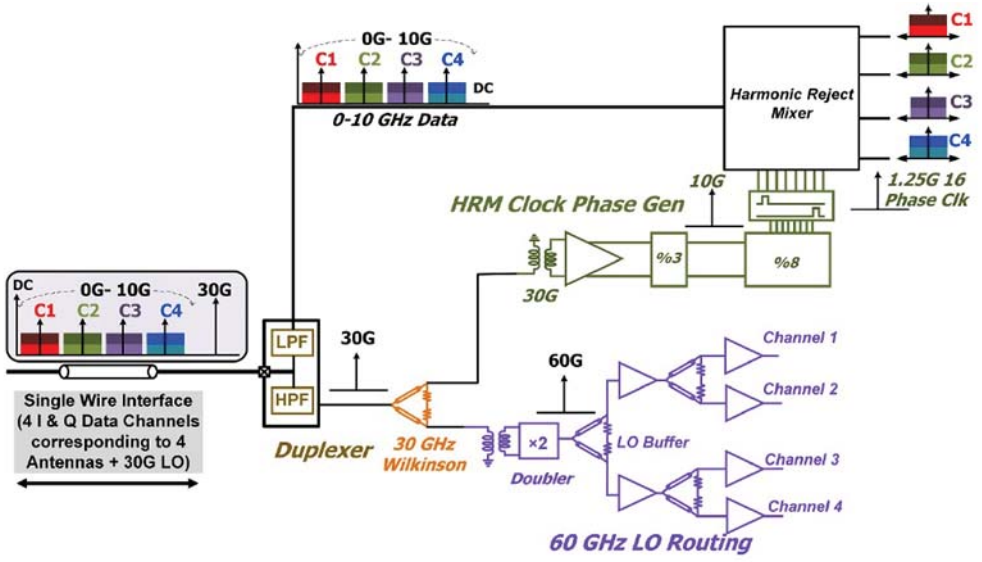

Figure 21: LO Path Architecture

3.4 Measurement Results

Figure 23(a) shows the chip micrograph of the 45nm RF SOI 4-element MIMO TX. The chip measures 3.2 mm × 4.9 mm, and is flip-chip mounted on a Rogers-4350B PCB through 75 µm C4 solder bumps, which in turn is mounted on another FR4 PCB for power supply connections. The PCB RF trace losses are de-embedded, but the measurements include the 1-2 dB loss expected from the C4-PCB interface which is not de-embedded in the results in all measurements. Figure 22(a) shows the measured conversion gain to each TX output and channel-to-channel isolation for three sample chips across frequency. The gain is more than 30 dB for the first two channels and more than 20 dB for the next two.

This gain variation arises from several factors, including inherent gain differences in the downconversion of different harmonics, gain roll off from DC to 10 GHz in the harmonic rejection mixer, and some systematic routing differences on chip. However, the access to per-element IF streams would enable the compensation of this gain difference easily in DSP. The conversion gain BW of the channels is ≈ 1.2 GHz. This BW is limited by the millimeter-wave part, and the 3 dB BW of the HRM de-multiplexer itself is higher than 2GHz. The worst-case measured isolation (difference between lowest gain for the main channel and highest gain for spurious channels) across 3 different chips is annotated on the figure. This isolation between channel 1 and channels 2, 3, and 4 is better than 40/ 45/ 40 dB, channel 2 and channels 1, 3, and 4 is better than 40/ 40/ 40 dB, channel 3 and channels 1, 2, and 4 is better than 45/ 35/ 35 dB, and channel 4 and channels 1, 2, and 3 is better than 30/ 40/ 30 dB respectively. These channel-to-channel isolations imply that the net spurious leakage to a desired channel from the other channels would be more than 30dB weaker, more than sufficient to handle complex modulation formats such as 64-QAM orthogonal frequency-division multiplexing (OFDM).

The measured large-signal characteristics for each MIMO TX output are shown in Figure 22(b). The OP1dB ranges from 8.8-10.93 dB, while the saturated output power ranges from 9.1-12.5 dBm. Drain efficiency of the whole chip as a function of input power is also measured

and can be seen in Figure 22(b). The DC power consumption of the whole chip is 220 mW/channel at 6dBm output power for each channel.

Figure 23(b) shows the measurement setup that is used to demonstrate simultaneous multi-beam formation capability. Utilizing four phase locked loop (PLL) boards, four signals are generated at frequencies equal to 1.2 GHz, 1.35 GHz, 3.7 GHz, and 3.85 GHz. These signals along with the 30 GHz LO are all combined and fed to the chip using a single coaxial cable. Two outputs of the chip, element 1 and element 2, are connected to a 2-element aperture-coupled patch antenna array. The 1.2 GHz and 1.35 GHz signals fall within the bandwidth of the first channel (0-2.5 GHz) and are up-converted to 60.05 GHz and 59.90 GHz respectively. The 3.7 GHz and 3.85 GHz signals fall within the bandwidth of the second channel (2.5GHz-5 GHz) and are also up-converted to 60.05 GHz and 59.90 GHz respectively. Applying different phase shifts to different input signals enables us to steer the 59.90 GHz and 60.05 GHz beams simultaneously to two different directions. Figure 23(c) shows the measured radiation patterns for the two different frequencies.

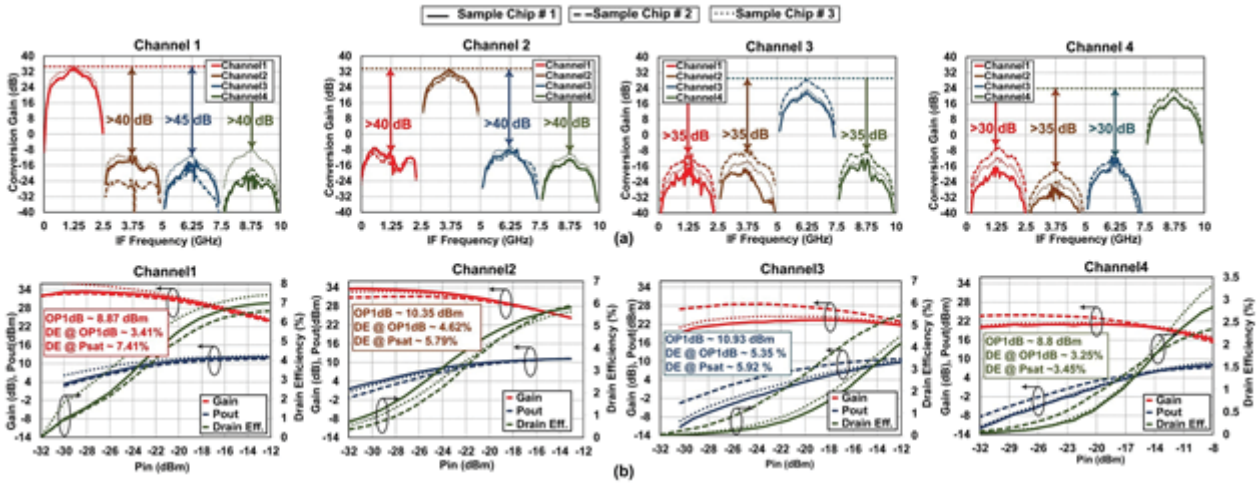

Figure 22: Measurement Results for three different Chips

(a) Gain of each channel and channel-to-channel isolation (numbers show the worst case among the sample chips), and (b) gain, output power and drain efficiency as a function of input power for all channels. The inset in each figure shows the Psat, OP1dB and drain efficiency at OP1dB for the 3rd sample.

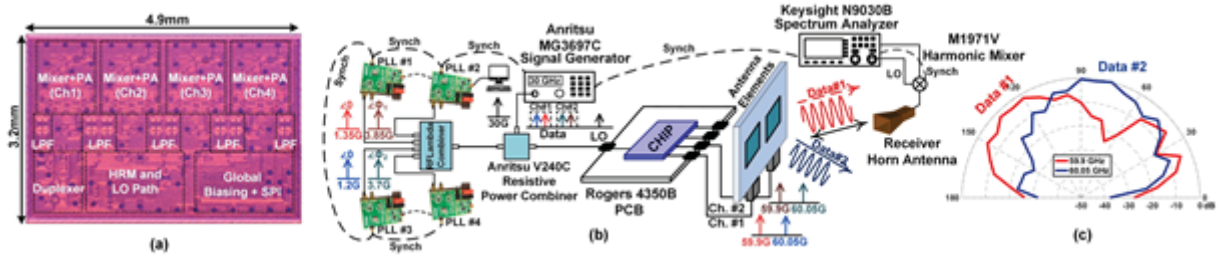

Figure 23: (a) Chip Micrograph, (b) Measurement Setup to demonstrate Simultaneous Formation of Multiple Beams carrying Independent Signals, and (c) Antenna Pattern measured for two Simultaneously-Transmitted Frequencies, 59.9GHz and 60.05GHz

In Table 2, this work is compared to the state-of-the-art mm-wave MIMO transmitters and receivers with and without a single-wire interface. This is the first work to support a single-wire interface for an mm-wave MIMO array with high aggregate BW and high channel-to-channel isolation.

Table 2. Comparison to the State-of-the-Art mm-wave MIMO Transmitters and Receivers with and without a Single-wire Interface

	Broadcom JSSC 2014	Intel ISSCC 2018	Intel ISSCC 2019	Oregon State Uni. RFIC 2019	This Work
Architecture	Phased-Array Tx/Rx	2-Way Pol. MIMO Tx/Rx	Digital Tx with 2-Way Pol. MIMO	4-element MIMO RX	4-element MIMO TX
Single-Wire Interface	Yes (IF data, Control, LO ref and DC)	No	No	CDMA based (IF data and LO)	FDMA based (IF data and LO)
Operation Freq.	60 GHz	60 GHz	60 GHz	28 GHz	60 GHz
# of Elements	16 (Tx), 16 (Rx)	1 (dual polarization)	1 (dual polarization)	4	4
MIMO Streams	1	2	2	4	4
IF Data BW	2 GHz	3.47[1] GHz	3.52[3] GHz	400 MHz	8 GHz
Gain (dB)	N/R	N/R	N/R	16 (Rx)	20 – 35
OP_{1dB} (dBm)	+5.2[2]	N/R	N/R	N/A	8.8 – 10.9
OP_{sat} (dBm)	9[2]	4	11.5[3]	N/A	9.1 – 12.5
Channel-to-Channel Isolation	N/A	N/A	N/A	20dB	30-40dB
P_{DC} (mW/element)	74.4	210	182	73 (Rx)	220
Technology	40nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS	45nm CMOS-SOI
Active Area mm^2/element	1	3.9	3.24[4]	1.44	3.92

4. CONCLUSION

In this project, we explored the FDMA concept to enable a 4-element MIMO Tx and Rx arrays at 60 GHz and 28GHz with a single wire interface. Such arrays enable many functionalities in large-scale mm-wave MIMO arrays that cannot be supported by traditional phased arrays, including full digital beamforming, simultaneous multi-beam formation, mm-wave spatial multiplexing, and per-PA digital pre-distortion. Topics for future research include expanding the single-wire interface to support transceivers with T/R switching and carrier aggregation.

5. REFERENCES

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LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ACRONYM	DEFINITION
ADC	Analog to Digital Convertor
AOI	Angle of Incident
BB	Broadband
BW	Bandwidth
CDM	Code Domain Multiplexing
CDMA	Code Domain Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
DBF	Digital Beamforming
DC	Direct Current
DSP	Digital Signal Processing
EVM	Error Vector Magnitude
FDM	Frequency Domain Multiplexing
FDMA	Frequency Division Multiple Access
FOV	Field of View
HPF	High Pass Filter
HR	Harmonic Rejection
HRM	Harmonic Rejection Mixer
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MIMO	Multiple Input Multiple Output
NF	Noise Figure
OFDM	Orthogonal Frequency-Division Multiplexing
OTA	Over the Air
PA	Power Amplifier
PAE	Power-Added Efficiency
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RF	Radio Frequency
RFSOI	Radio Frequency Silicon on Insulator
RX	Receive
SERDES	Serializer-Deserializer
SFDR	Spurious Free Dynamic Range
SOI	Silicon on Insulator

ACRONYM	DEFINITION
T/R	Transmit/Receive
TIA	Transimpedance Amplifier
TX	Transmit
VGA	Variable Gain Amplifier