

Ka-Band Front-End Monolithic Microwave Integrated Circuits (MMICs) and Transmit– Receive (T/R) Modules

by John E Penn and Ali Darwish

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John E Penn and Ali Darwish Sensors and Electron Devices Directorate, CCDC Army Research Laboratory

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The US Army Research Laborat and high-dynamic-range low-no Gallium nitride (GaN) monolith amplifier applications as well as damaging, input power levels w high-power, solid-state switches applications, particularly transce could build on this effort by add	tory has been evaluation is amplifiers for us in microwave integration for low-noise amplithout the need for a state well. Compact eiver arrays, were doing functionality, in	ating and designing se in networking rated circuit (MM lifiers with high c additional limiters MMIC transmit/r esigned and subm ntegrating new fer	ng efficient br and communi (IC) technolog lynamic range s at the system eccive modul hitted to Qorv atures in a sin	roadband high-power amplifiers, switches, ications at millimeter wave frequencies. gy has superior performance in power e and the ability to survive large, potentially n level. This technology works well for les for use in Ka-band (28 GHz \pm) o for fabrication. Future transceiver designs gle GaN MMIC, or using 3-D packaging to
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Contents

List	of Fi	gures	iv
1.	Intr	oduction	1
2.	Full	Reticle Plot	1
3.	Ka-l	Band Low-Noise Amplifiers	2
4.	Ka-l	band Power Amplifiers	12
5.	Sing	gle-Pull Double-Throw Switches	21
6.	Ka E	Band T/R Modules	26
	6.1	Ka-band T/R Module 1, SPDT T/R Switch, PA, and LNA	26
	6.2	Ka-band T/R Module 2, SPDT T/R Switch, PA, and LNA	29
	6.3	Ka-band T/R Module 3, SPDT T/R Switch, PA, and LNA	32
	6.4	Ka-band T/R Modules, Broadband Power Amplifiers (CKT6)	35
7.	Ka-l	oand T/R Circuits, Broadband Amplifiers (CKT7)	36
8.	Shu	nt SPDT T/R Switch and Other Design Circuits (CKT8)	37
9.	Ka-l	band T/R Module, Broadband S/X Power Amplifiers (CKT9)	38
10.	Sun	nmary and Conclusion	40
List	of Sy	mbols, Abbreviations, and Acronyms	41
Dist	ribut	ion List	42

List of Figures

Fig. 1	ARL reticle layout for Qorvo's 0.15- μ m GaN high-electron-mobility transistor (HEMT) process (10 × 10 mm)
Fig. 2	Noise figure, stability, and gain circles for the 6- × 25-µm HEMT (Lsrc=0.04 nH, 28 GHz)
Fig. 3	S-parameter simulation for an ideally matched one-stage LNA ($6 \times 25 \ \mu m$)
Fig. 4	S-parameter simulation for an ideally matched two-stage LNA ($6 \times 25 \ \mu m$)
Fig. 5	S-parameter simulations for the MMIC (thin) and EM (thick) two-stage LNA (6 \times 25 $\mu m)$
Fig. 6	S-parameter simulation for an ideally matched one-stage LNA (4 \times 25 μ m)
Fig. 7	S-parameter simulation for an ideally matched two-stage LNA ($4 \times 25 \ \mu m$)
Fig. 8	S-parameter simulations for the MMIC (thin) and EM (thick) two-stage LNA (4 \times 25 $\mu m)9$
Fig. 9	Layout of the one-stage LNA ($6 \times 25 \ \mu m$)
Fig. 10	Layout of the two-stage LNA ($6 \times 25 \ \mu m$)
Fig. 11	Layout of the one-stage LNA ($4 \times 25 \ \mu m$)
Fig. 12	Layout of the two-stage LNA $(4 \times 25 \mu\text{m})$
Fig. 13	Output power and PAE vs. input power for the 4-× 50-μm HEMT (28 V, 28 GHz)
Fig. 14	Output power and PAE vs. input power for the $8 - \times 50$ -µm vs. $4 - \times 50$ -µm HEMT (28 V)
Fig. 15	S-parameter simulation for an ideally matched one-stage PA ($4 \times 50 \ \mu m$)
Fig. 16	S-parameter simulation for an ideally matched one-stage PA ($8 \times 50 \ \mu m$)
Fig. 17	Output power and PAE vs. input power for the $4- \times 50-\mu m$ PA-EM (solid); ideal (dash)
Fig. 18	Output power and PAE vs. input power for the $8 - \times 50$ -µm PA-EM (solid); ideal (dot)
Fig. 19	EM simulation of the one- and two-stage PA layouts (8 \times 50 μ m) 19
Fig. 20	EM simulation of both two-stage PAs (4 \times 50 and 8 \times 50 μ m)
Fig. 21	Layout of the one-stage PA (4 \times 50 μ m)
Fig. 22	Layout of the two-stage PA ($4 \times 50 \ \mu m$, $4 \times 50 \ \mu m$)

Fig. 23	Layout of the one-stage PA (8 \times 50 $\mu m)$	21
Fig. 24	Layout of the two-stage PA (4 \times 50 $\mu m,$ 8 \times 50 $\mu m)$	21
Fig. 25	SPDT Ka-band series/shunt switch simulation (linear/nonlinear)	22
Fig. 26	SPDT Ka-band shunt 1/4 wave line switch simulation (linear/nonlinear)	23
Fig. 27	SPDT Ka-band nonlinear power simulation (both designs)	23
Fig. 28	Layout of the SPDT Ka-band series/shunt switch	24
Fig. 29	Layout of the SPDT Ka-band shunt 1/4 wave line switch	25
Fig. 30	Layout of the T/R Module 1, SPDT, PA, and LNA	26
Fig. 31	Simulation of the T/R Module 1, LNA and SPDT vs. LNA only	27
Fig. 32	Simulation of the T/R Module 1, PA and SPDT vs. PA only	28
Fig. 33	Layout of the T/R Module 2, SPDT, PA, and LNA	29
Fig. 34	Simulation of the T/R Module 2, LNA and SPDT vs. LNA only	30
Fig. 35	Simulation of the T/R Module 2, PA and SPDT vs. PA only	31
Fig. 36	Layout of the T/R Module 3, SPDT, PA, and LNA	32
Fig. 37	Simulation of the T/R Module 3, LNA and SPDT vs. LNA only	33
Fig. 38	Simulation of the T/R Module 3, PA and SPDT vs. PA only	34
Fig. 39	Plot of the Ka-band T/R modules, broadband PAs—CKT6 (4 \times 2 mm	n) 35
Fig. 40	Plot of the Ka-band T/R modules, broadband PAs—CKT7 (4 \times 4 mm	n) 36
Fig. 41	Plot of the Ka-band T/R modules, broadband PAs—CKT8 (4 \times 4 mm	n) 37
Fig. 42	Plot of the Ka-band T/R Module 3, broadband PAs—CKT9 (4×2 mm)	39

1. Introduction

The US Army Combat Capabilities Development Command Army Research Laboratory (ARL) has been evaluating and designing efficient broadband highpower amplifiers for use in sensors, communications, networking, and electronic warfare. ARL submitted designs of Ka-band low-noise amplifiers (LNAs), power amplifiers (PAs), and transmit–receive (T/R) switches, using Qorvo's highperformance 0.15-µm gallium nitride (GaN) fabrication process. These amplifiers were fabricated as one- and two-stage designs as well as integrated T/R modules for bidirectional transceivers as part of a recent ARL Qorvo Prototype Wafer Option (PWO), which yields many different designs from two full 4-inch GaN wafers. Other technical reports will document other designs, while this one concentrates on the Ka-band designs.

2. Full Reticle Plot

ARL contracted for Qorvo's PWO, whose total cost exceeds a single smaller Prototype Chip Option but is much less expensive per unit area, providing many designs and additional control of the fabrication schedule. Qorvo's PWO will yield multiple copies of designs from a custom reticle replicated across two full 4-inch wafers. To meet multiple program requirements, including these Ka-band designs, the PWO was used by the Electronics Branch III/V Design Team for multiple designs across the 10- \times 10-mm reticle shown in Fig. 1.



Fig. 1 ARL reticle layout for Qorvo's 0.15-µm GaN high-electron-mobility transistor (HEMT) process (10 × 10 mm)

3. Ka-Band Low-Noise Amplifiers

Designs for a Ka-band transceiver were explored starting with key circuits that would be needed, such as LNAs in GaN, which have the added advantages of high dynamic range and robust survivability to high-power interference signals. A requirement of a few gigahertz bandwidth around 28 GHz was assumed for all designs. Devices with noise data in Qorvo's 0.15-µm GaN process design kit were limited to a few sizes, including a 4- × 25-µm and 6- × 25-µm device at nominal DC biases of 10 V and 100 mA/mm. Various matching topologies, stabilizing approaches, and tradeoffs of gain versus noise figure were explored for the two HEMT sizes. To achieve sufficient gain, a two-stage amplifier was desired with a first stage matched for low noise and a second stage that could be designed to emphasize gain. Overall, the noise figure is dominated by the first stage of the LNA. Ideal matching elements were then converted to lossy monolithic microwave integrated circuit (MMIC) elements, retuning those matching circuits to minimize

the impacts on the noise figure, as well as gain, bandwidth, stability, and size. Final layouts were electromagnetic (EM) simulated for the most accurate predictions, including physical interconnect, parasitic coupling, and DC connectivity. Electrical design rules, such as current carrying limitations, are checked manually and were discussed in the design reviews held at ARL.

Both the 4- \times 25-µm and 6- \times 25-µm LNAs used source inductance to provide a tradeoff between return loss, noise figure, and stability. Figure 2 shows a simulation plot of the noise figure and gain circles, which are brought closer together due to the source inductance. The two-stage 6- \times 25-µm LNA had good gain and bandwidth around 28 GHz, while the two-stage 4- \times 25-µm LNA had an interstage match that yielded a large gain bandwidth, but was a riskier approach with regard to stability. Ideal noise figures of less than 1.4 dB increased slightly to 1.7 dB when lossless matching elements were replaced with compact low-loss MMIC elements. Larger, lower-loss matching circuits might improve the noise figure in future designs, but the current tradeoff of size and performance yielded two promising designs. The first stage of both two-stage LNAs was fabricated as well for individual test and verification. Note that the input and output matches of these one-stage LNAs were not retuned for optimal one-stage LNA performance, but were the original matches designed for optimal performance as a two-stage LNA.



Fig. 2 Noise figure, stability, and gain circles for the 6- \times 25- μ m HEMT (Lsrc=0.04 nH, 28 GHz)

Figure 3 shows the simulation of the initial ideal design of a one-stage $6 - \times 25$ -µm LNA with an about 8-dB small-signal gain. The ideal two-stage design $6 - \times 25$ -µm LNA increases the gain above 16 dB with only a 0.2-dB increase in the noise figure, as shown in Fig. 4. Once the ideal elements are replaced with lossy MMIC elements, the gain drops to about 15 dB and the noise figure increases to about 1.9 dB for the two-stage $6 - \times 25$ -µm LNA. Figure 5 shows the final EM simulation (thick lines) of the final layout of the $6 - \times 25$ -µm LNA, which is adjusted to nearly match the original linear MMIC models (thin lines).



Fig. 3 S-parameter simulation for an ideally matched one-stage LNA (6 × 25 μm)



Fig. 4 S-parameter simulation for an ideally matched two-stage LNA (6 × 25 μm)





Figure 6 shows the simulation of the initial ideal design of a one-stage $4- \times 25$ -µm LNA with an about 8-dB small-signal gain. The ideal two-stage design $4- \times 25$ -µm LNA increases the gain above 18 dB with only a 0.2-dB increase in the noise figure and with excellent gain bandwidth, as shown in Fig. 7. Once the ideal elements are replaced with lossy MMIC elements, the gain drops to about 16 dB, the gain bandwidth is reduced slightly, and the noise figure increases to about 1.8 dB for the two-stage $4- \times 25$ -µm LNA. Figure 8 shows the EM simulation (thick lines) of the final layout of the $4- \times 25$ -µm LNA, which is adjusted to nearly match the original linear MMIC models (thin lines).



Fig. 6 S-parameter simulation for an ideally matched one-stage LNA (4 × 25 μm)



Fig. 7 S-parameter simulation for an ideally matched two-stage LNA ($4 \times 25 \mu m$)





Layouts of the compact 6×25 -µm one- and two-stage LNAs are shown in Figs. 9 and 10. Gate bias pads and drain bias pads are used on chip metal–insulator–metal (MIM) decoupling shunt capacitors, with additional resistors on the gates, to isolate the DC connections from the RF match. Similarly, the layouts of the compact 4×25 -µm one- and two-stage LNAs are shown in Figs. 11 and 12.



Fig. 9 Layout of the one-stage LNA ($6 \times 25 \ \mu m$)



Fig. 10 Layout of the two-stage LNA ($6 \times 25 \mu m$)



Fig. 11 Layout of the one-stage LNA ($4 \times 25 \ \mu m$)



Fig. 12 Layout of the two-stage LNA ($4 \times 25 \mu m$)

4. Ka-band Power Amplifiers

Designs for a Ka-Band transceiver included efficient PAs in GaN. Estimating output power based on watts per millimeter of HEMT periphery, and also keeping the HEMT size appropriate for the 28-GHz design frequency, an output power goal near 1 W resulted in two single-stage HEMT PAs. One PA is based on a 4- \times 50-µm device and the other is based on an 8- \times 50-µm device, both at nominal DC biases of 28 V and 100 mA/mm. Various matching topologies, stabilizing approaches, and tradeoffs of output power and power-added efficiency (PAE) were explored for the two HEMT sizes. To achieve sufficient gain, a two-stage amplifier was desired with an output stage matched for power and efficiency and a first stage that could be designed to emphasize gain. Overall, power and efficiency are dominated by the output stage of the PA. Ideal matching elements were then converted to lossy MMIC elements, retuning those matching circuits to minimize the impacts on power performance, as well as gain, bandwidth, stability, and size. Final layouts were EM simulated for the most accurate simulations to include physical interconnect, parasitic coupling, and DC connections. Electrical design rules, such as current carrying limitations, are checked manually and were discussed in the design reviews held at ARL.

Figure 13 shows a power performance simulation of the 4- \times 50-µm HEMT with ideal lossless matching circuits, achieving 0.83 W and 44% PAE at 3-dB gain compression. Nearly twice the power and similar efficiencies for the larger

 $8- \times 50-\mu m$ ideal lossless single-stage PA are shown in comparison to the $4- \times 50-\mu m$ PA (Fig. 14). The ideal $8- \times 50-\mu m$ HEMT PA should yield 1.6 W and 43% PAE. Gain for the ideal one-stage $4- \times 50-\mu m$ PA was above 10 dB (Fig. 15), and the $8- \times 50-\mu m$ PA gain was similar but slightly lower (Fig. 16). After converting to lossy MMIC matching circuits and EM simulating the final PA layouts, the single-stage $4- \times 50-\mu m$ PA predicts 0.75 W of output power and 38% PAE as shown in Fig. 17. Figure 18 shows the $8- \times 50-\mu m$ PA EM simulations predicting a respectable 39% PAE and 1.4 W of output power.











Fig. 15 S-parameter simulation for an ideally matched one-stage PA (4 × 50 μm)



Fig. 16 S-parameter simulation for an ideally matched one-stage PA (8 × 50 μm)







Fig. 18 Output power and PAE vs. input power for the 8- × 50-µm PA-EM (solid); ideal (dot)

A two-stage PA using the $8 - \times 50$ -µm device as the output stage and a $4 - \times 50$ -µm device for a driver stage results in a 20-dB small-signal gain over several gigahertz. Figure 19 shows the small-signal gain of the two-stage PA versus the single $8 - \times 50$ -µm PA. A second two-stage PA used the $4 - \times 50$ -µm as both the driver and

output power stages resulting in about 1-dB more gain. Figure 20 shows the smallsignal gain of the two-stage PA with $4 - \times 50$ -µm driver and output HEMTs versus the two-stage PA with a $4 - \times 50$ -µm driver and an $8 - \times 50$ -µm output HEMT.



Fig. 19 EM simulation of the one- and two-stage PA layouts (8 × 50 µm)



Fig. 20 EM simulation of both two-stage PAs (4×50 and $8 \times 50 \mu m$)

Layouts of the compact one-stage 4×50 -µm PA and two-stage 4×50 -µm/ 4- × 50-µm PA are shown in Figs. 21 and 22. Gate bias pads and drain bias pads are used on chip MIM decoupling shunt capacitors, with additional resistors on the gates to isolate the DC connections from the RF match. Similarly, the layouts of the compact one-stage 8- × 50-µm PA and two-stage 4- × 50-µm/8- × 50-µm PA are shown in Figs. 23 and 24.



Fig. 21 Layout of the one-stage PA ($4 \times 50 \mu m$)



Fig. 22 Layout of the two-stage PA ($4 \times 50 \ \mu m$, $4 \times 50 \ \mu m$)



Fig. 23 Layout of the one-stage PA (8 × 50 μm)



Fig. 24 Layout of the two-stage PA ($4 \times 50 \ \mu m$, $8 \times 50 \ \mu m$)

5. Single-Pull Double-Throw Switches

Designs for a Ka-band transceiver required T/R switches. An earlier T/R switch in 0.25-µm GaN was designed to operate up to 18 GHz, but would not be sufficient for Ka-band. Compensating the parasitic capacitance of the switch HEMTs by adding parallel MMIC inductors worked well for the required several gigahertz bandwidth around 28 GHz. The first single-pull double-throw (SPDT) switch used shunt (0.2 mm) and series (0.35 mm) HEMTs with parallel MMIC inductors resulting in a 1.25-dB insertion loss with good return loss at 28 GHz. Figure 25

shows the simulated small-signal performance for this switch design, where the nonlinear model estimated about 0.3-dB more insertion loss. The linear switch models are more accurate than the nonlinear models and predict lower losses. For the second SPDT switch design, shunt (0.2 mm) HEMTs were used with 1/4 wave 50- Ω microstrip lines. To compact the layout further, the 1/4 wave microstrip lines were reduced in length by narrowing their width while compensating the resulting higher impedance lines with shunt capacitance to ground at each end of these shorter lines. Figure 26 shows the simulated small-signal performance for the shunt-only HEMT switch design, where the nonlinear model estimated about 0.6-dB more insertion loss. Nonlinear simulations, shown in Fig. 27, verify that both designs have reasonable loss at the maximum 32-dBm (1.6-W) output power of the 8- × 50-µm PAs. The compact layout of the series/shunt SPDT Ka-band switch is shown in Fig. 28, and the shunt-only SPDT switch is shown in Fig. 29.



Fig. 25 SPDT Ka-band series/shunt switch simulation (linear/nonlinear)



Fig. 26 SPDT Ka-band shunt 1/4 wave line switch simulation (linear/nonlinear)



Fig. 27 SPDT Ka-band nonlinear power simulation (both designs)



Fig. 28 Layout of the SPDT Ka-band series/shunt switch



Fig. 29 Layout of the SPDT Ka-band shunt 1/4 wave line switch

6. Ka Band T/R Modules

6.1 Ka-band T/R Module 1, SPDT T/R Switch, PA, and LNA

A complete Ka-band T/R front end combines the two-stage $8- \times 50$ -µm PA, the two-stage LNA, and one shunt/series SPDT switch, as shown in the layout plot of Fig. 30. This layout has a common "antenna" connection, an input for the LNA path, and an output for the PA path. The series shunt SPDT design has better isolation than the shunt-only SPDT switch, but in operation it would be desirable to turn off the PA (DC bias off) in the receive mode and turn off the LNA (DC bias off) in the transmit mode. EM simulations of the layouts for the T/R module verify that the amplifiers work as expected after factoring in the 1 dB or so of switch loss. Small-signal simulations of the LNA path versus the standalone LNA show similar gain and return loss over the operating band (Fig. 31). Likewise, small-signal simulations of the PA path versus the standalone PA show similar gain and return loss over the operating band (Fig. 32).



Fig. 30 Layout of the T/R Module 1, SPDT, PA, and LNA









6.2 Ka-band T/R Module 2, SPDT T/R Switch, PA, and LNA

A second Ka-band T/R front end combined the two-stage $8 - \times 50$ -µm PA, the two-stage LNA, and two shunt-only SPDT switches, as shown in the layout plot of Fig. 33. This layout has two common connections, which change the signal flow direction, right to left for the LNA path and left to right for the PA path, as shown. The shunt-only SPDT switch requires that the PA is off (DC bias off) in the receive mode and the LNA is off (DC bias off) in the transmit mode. EM simulations of the layouts for the T/R module verify that the amplifiers work as expected after factoring in the 2 dB or so of switch loss. Small-signal simulations of the LNA path versus the standalone LNA show similar gain and return loss over the operating band (Fig. 34). Likewise, small-signal simulations of the PA path versus the standalone PA show similar gain and return loss over the operating band (Fig. 35).



Fig. 33 Layout of the T/R Module 2, SPDT, PA, and LNA



Fig. 34 Simulation of the T/R Module 2, LNA and SPDT vs. LNA only





6.3 Ka-band T/R Module 3, SPDT T/R Switch, PA, and LNA

A third complete Ka-band T/R front end combined the two-stage $8 - \times 50$ -µm PA, the two-stage LNA, and two shunt/series SPDT switches as shown in the layout plot of Fig. 36. This layout has two common connections, which change the signal flow direction, right to left for the LNA path and left to right for the PA path, as shown. The series shunt SPDT has better isolation than the shunt-only SPDT switch, but in operation it would be good to turn off the PA (DC bias off) in the receive mode and turn off the LNA (DC bias off) in the transmit mode. EM simulations of the layouts for the T/R module verify that the amplifiers work as expected after factoring in the 2 dB or so of switch loss. Small-signal simulations of the LNA path versus the standalone LNA show similar gain and return loss over the operating band (Fig. 37). Likewise, small-signal simulations of the PA path versus the standalone PA show similar gain and return loss over the operating band (Fig. 38).



Fig. 36 Layout of the T/R Module 3, SPDT, PA, and LNA









6.4 Ka-band T/R Modules, Broadband Power Amplifiers (CKT6)

Ka-band (± 28 GHz) PA, LNA, and T/R switch were designed for use in network communications. Two variations are included on this die—the top T/R circuit has common RF connections on the left and right with a shunt switch arrangement to choose a PA flowing left to right as a transmitter or an LNA flowing from right to left as a receiver. For the lower T/R circuit, there are separate RF connections on the left for the PA and the LNA with a shunt/series switch arrangement to provide directional connections to a common "antenna" RF connection on the right. There are also two versions of Dr Sami Hawasli's broadband PA included on this die. This circuit can be subdiced to 2×2 mm using a pseudo saw street that leaves a gap in the backside metal (see the die plot of Fig. 39).



Fig. 39 Plot of the Ka-band T/R modules, broadband PAs—CKT6 (4 × 2 mm)

7. Ka-band T/R Circuits, Broadband Amplifiers (CKT7)

The one- and two-stage versions of the Ka-band (28 GHz \pm) PAs, LNAs, and the shunt/series T/R switch for use in network communications are included as probetestable standalone circuits on this die. Additional designs include a broadband nonuniform low-noise distributed amplifier and a few other broadband amplifiers and test circuits. A test 8- \times 50-µm HEMT and a test 4- \times 50-µm HEMT are included on this die layout. These test HEMTs can be DC and RF tested at ARL to analyze and verify circuit performance. The layout of the 4- \times 4-mm die is shown in Fig. 40.



Fig. 40 Plot of the Ka-band T/R modules, broadband PAs—CKT7 (4 × 4 mm)

8. Shunt SPDT T/R Switch and Other Design Circuits (CKT8)

Frequency multipliers, broadband amplifiers, a few test circuits, and the shunt-only T/R switch for use in network communications are included as probe testable standalone circuits on this die. A test $4- \times 50-\mu m$ HEMT is included on this die layout (bottom middle). This test HEMT can be DC and RF tested at ARL to analyze and verify circuit performance. The layout of the $4- \times 4$ -mm die is shown in Fig. 41.



Fig. 41 Plot of the Ka-band T/R modules, broadband PAs—CKT8 (4 × 4 mm)

9. Ka-band T/R Module, Broadband S/X Power Amplifiers (CKT9)

We designed a Ka-band (28 GHz \pm) PA, LNA, and T/R switch for use in network communications. This third T/R module variation has common RF connections on the left and right with a series/shunt switch arrangement to choose a PA flowing left to right as a transmitter or an LNA flowing from right to left as a receiver. One of Dr Hawasli's broadband PAs is included in the middle this die. At the top of the die is a parallel combined S- to X-band power amplifier by John Penn using two parallel combined 10- × 150-µm HEMTs. This circuit can be subdiced to 2- × 2.3-mm top and 2- × 1.7-mm bottom using a pseudo saw street that leaves a gap in the backside metal (see the die plot of Fig. 42).



Fig. 42 Plot of the Ka-band T/R Module 3, broadband PAs—CKT9 (4 × 2 mm)

10. Summary and Conclusion

GaN MMIC technology has superior performance in PA applications as well as for LNAs with high dynamic range and the ability to survive large potentially damaging input power levels without the need for additional limiters at the system level. This technology works well for high-power solid-state switches as well. All of these benefits were utilized in developing T/R modules for use in Ka-band (28 GHz \pm) applications, particularly transceiver arrays. PAs, LNAs, and T/R switches for use in network communications were designed and submitted to Qorvo for fabrication. When the designs return, they will be tested and documented in subsequent reports. Future transceiver designs could build on this effort by adding functionality, integrating new features in a single GaN MMIC, or using 3-D packaging to utilize the best integrated circuit technology for the particular function to create compact systems in a package.

List of Symbols, Abbreviations, and Acronyms

3-D	three-dimensional
ARL	Army Research Laboratory
DC	direct current
EM	electromagnetic
GaN	gallium nitride
HEMT	high-electron-mobility transistor
LNA	low-noise amplifier
MIM	metal-insulator-metal
MMIC	monolithic microwave integrated circuit
PA	power amplifier
PAE	power-added efficiency
PWO	Prototype Wafer Option
RF	radio frequency
SPDT	single-pull double-throw
T/R	transmit-receive

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