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Transport Property Studies of Structurally Modified Graphene

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The transport properties of two-dimensional (2D) materials can be dramatically modified by introducing nano- to atomic-scale porous patterns, such as periodic pores (antidots). Despite numerous studies, the electron and phonon transport processes in such a periodic porous structure are still not fully understood, which hinders the future development of these metamaterials.

In this project, we have advanced the electrical studies of GALs and further applied the knowledge to other 2D materials such as tellurene. The energy sensitivity to scattering is extracted and used to justify the major scattering mechanism of charge carriers. For thermal studies, valuable insights can be gained from comparable nanoporous films. Beyond antidot lattices, the nanoslot pattern is also explored as an effective approach to tune the thermoelectric properties of general 2D materials and thin films.

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Final Performance Report (11/01/2015 – 12/31/2018)

(YIP) Transport Property Studies of Structurally Modified Graphene

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Overview

The goal of this proposal is to better understand how to tune the transport properties of graphene by fabricating periodic nanopores (antidots) across single-atomic-layer graphene, called graphene antidot lattices (GALs). Unrestricted to GALs, nanoporous structures can be patterned across ***general two-dimensional (2D) materials or thin films*** to modify their transport properties for specific applications.

GALs have a wide range of applications, including gas sensing [1], thermoelectric power generation and cooling [2, 3], optoelectronic devices [4], magnetics [5, 6], spintronics [7, 8] and waveguides [9]. This project focuses on thermoelectrics applications. In general, a better thermoelectric material should have a high electrical conductivity σ, a high Seebeck coefficient S, and a low thermal conductivity k. The combination of these properties leads to a high dimensionless figure of merit (ZT), defined as $ZT = S^2\sigma T/k$, where T represents the absolute temperature. Despite its many advantages in other research fields, pristine graphene has a low *ZT* due to its ultra-high thermal conductivity k and low power factor $S^2\sigma$, the latter of which results from the low S of semi-metal graphene.

GALs provide an effective approach to improve the low ZT of pristine graphene, by simultaneously reducing the high thermal conductivity but increasing the power factor. With quantum confinement of electrons in the ultrafine nanoporous structure, an electronic bandgap can be opened in a GAL to convert semimetal graphene into a semiconductor, which will benefit the S and thus $S^2\sigma$. On the other hand, the thermal conductivity can also be reduced by antidot scattering of phonons. With ultrafine porous features, the phonon dispersion can also be modified to further lower the thermal conductivity, known as phononic effects. A high ZT is anticipated in this case to benefit thermoelectric applications. As a slightly "unconventional" viewpoint, a high $S^2\sigma$ alone can also be critical to thermoelectric energy conversion. One example can be the active cooling of high-power electronics [10].

In this project, one focus was on the electrical measurements of GALs. As a novel approach, the *energy sensitivity to scattering* was extracted for charge carriers to identify the major scattering mechanisms of charge carriers. To gain insights into the thermal transport, temperature-dependent thermal studies were carried out on comparable periodic nanoporous Si films and $In_{0.1}Ga_{0.9}N$ films, with detailed structure studies on pore-edge defects. Beyond nanopore-drilled samples, thermoelectric studies of nanoslot-patterned thin films were carried out as another promising metamaterial with adjustable electron and phonon transport.

This report is organized as follows:

I. Electrical properties of GALs and new studies on tellurene
II. Phonon studies of periodic nanoporous thin films
III. New studies of nanoslot-patterned thin films
IV. Summary

The following papers have been published or accepted for now:

1. Q. Hao, Y. Xiao. "Electron Monte Carlo Simulations of Nanoporous Si Thin Films — The Influence of Pore-Edge Charges," *Journal of Applied Physics*, accepted.
2. D. C. Xu, S. Tang, X. Du, Q. Hao. "Detecting the major charge-carrier scattering mechanism in graphene antidot lattices," *Carbon* **144**, 601-607 (2019).
3. Q. Hao, D. C. Xu, H.B. Zhao, Y. Xiao, and F. J. Medina. "Thermal Studies of Nanoporous Si Films with Pitches on the Order of 100 nm — Comparison between Different Pore-Drilling

Techniques," *Scientific Reports* **8**, 9056 (2018).
4. Q. Hao, D. C. Xu, and H. B. Zhao. "Thermal investigation of nanostructured bulk thermoelectric materials with hierarchical structures: An effective medium approach," *Journal of Applied Physics* **123**, 014303 (2018).
5. D. C. Xu, Q. Wang, X. W. Wu, J. Zhu, H. B. Zhao, B. Xiao, X. J. Wang, X. L. Wang, Q. Hao (corresponding author). "Largely reduced cross-plane thermal conductivity of nanoporous $In_{0.1}Ga_{0.9}N$ thin films directly grown by metal organic chemical vapor deposition," *Frontiers in Energy* **12**, 127-136 (2018).
6. Q. Hao, D. C. Xu, X. Ruden, B. LeRoy, X. Du. "Thermoelectric Performance Study of Graphene Antidot Lattices on Different Substrates," *MRS Advances* **2**, 3645-3650 (2017).
7. Q. Hao, D. Xu, Y. Xiao, B. Xiao, H. Zhao. "Nanostructures for Reduced Lattice Thermal Conductivity — Case Studies for Nanopores and Grain Boundaries," *ECS Transactions* **80**, 67-75 (2017).
8. Q. Hao, H.B. Zhao, and D.C. Xu. "Thermoelectric studies of nanoporous thin films with adjusted pore-edge charges," *Journal of Applied Physics* **121**, 094308 (2017).
9. Q. Hao, H. B. Zhao, D. C. Xu. "High-throughput ZT predictions of nanoporous bulk materials as next-generation thermoelectric materials: A material genome approach," *Physical Review B* **93**, 205206 (2016).
10. M. G. Tuo, D. C. Xu, S. LI, M. Liang, Q. Zhu, Q. Hao, H. Xin. "Nonlinear microwave characterization of CVD grown graphene," *IEEE Antennas and Wireless Propagation Letters* **15**, 1557-1560 (2016).
11. Q. Hao, Y. Xiao, H. B. Zhao. "Characteristic length of phonon transport within periodic nanoporous thin films and two-dimensional materials," *Journal of Applied Physics* **120**, 065101 (2016).

One theoretical paper is currently under review:
1. Q. Hao, Y. Xiao, Q. Y. Chen, "Determining Phonon Mean Free Path Spectrum by Ballistic Phonon Resistance within a Nanoslot-Patterned Thin Film," submitted to *International Journal of Heat and Mass Transfer*.

A review paper on phonon transport within periodic nanoporous materials is currently under preparation, in collaboration with Prof. Fabio Semperlotti at Purdue University. This paper will be published in *ES Materials & Manufacturing* launched in 2018, for which I am one of the co-founding editors. One theoretical paper on thermoelectric properties of thin films with a periodic array of patterned nanoslots will be submitted soon. Three more experimental papers are under preparation and some preliminary results are given in Sections I.G, II.G, and III.

As invited talks, the work has been presented in the 2017 Collaborative Conference on Materials Research, 232nd ECS Meeting, 7th Annual World Congress of Nano Science & Technology-2017, and AiMES 2018 Conference. The progress of this project has also been presented at the 2016 and 2017 APS March Meeting, 2016 ASME IMECE conference, 2017 MRS Spring Meeting, and 2017 International Conference on Thermoelectrics. Two talks are now scheduled for the 2018 MRS Spring Meeting in April 2019.

During my sabbatical in Fall 2018, department seminars based on this project were given at UCLA, Purdue University, Hong Kong University of Science and Technology, the University of Hong Kong, and Chinese University of Hong Kong.

I. Electrical properties of GALs and new studies on tellurene

Electrical properties of representative GALs have been studied, with a focus on the mechanisms of charge carrier scattering. This work is in collaboration with Prof. Xu Du at Stony Brook University and Prof. Shuang Tang at SUNY Poly. Compared with existing electrical studies on GALs [2], ***gate-dependent power factors*** are first measured and compared between different nanoporous patterns.

In principle, the electron mean free paths (MFPs) in GALs are mostly restricted by the ultrafine nanoporous structures so that MFPs in pristine graphene on different substrates have very limited influence on the electrical properties. In our preliminary experimental studies at the room temperature, no big difference can be found between electrical properties of GALs on different substrates [11]. This provides important guidance for the real application of GALs, where suspending such fragile structure is not feasible in most cases. For the detailed electrical studies here, a SiO_2/Si substrate is selected without losing the generality [12].

I.A Electrical measurements of GALs on SiO_2

Monolayer GALs with hexagonal or square arrays of nanopores (antidots) were fabricated for the proposed study. Nanofabricated thermal and/or electrical probes were deposited onto each GAL to ensure intimate thermal/electrical contacts between these probes and the sample. Figure I-1 presents the scanning electron microscopy (SEM) image of a real setup. More details are shown in the inset. A gate voltage can also be applied from the back of the degenerately doped Si substrate to tune the Fermi level and thus the electrical properties of the GALs.

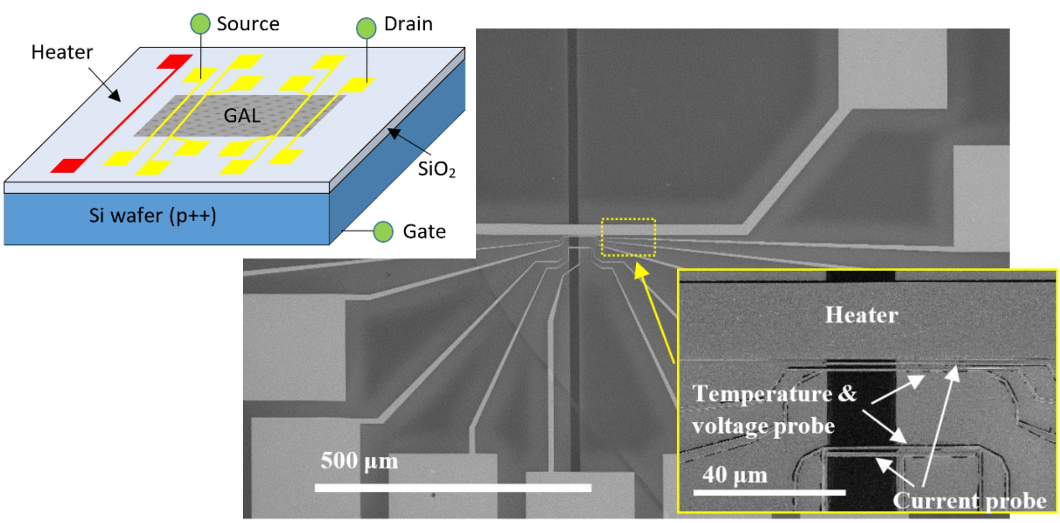


Figure I-1. SEM images of the measurement setup, with the upper left inset as the measurement scheme and the bottom right inset as the GAL region to be measured.

The electrical conductivity σ is measured with the standard four-probe technique. Two outer electrodes (source and drain) are used for 1-kHz AC current injection, while the inner two electrodes are used to measure the voltage drop. For the convenience of σ measurements, the CVD graphene is trimmed as a strip with patterned periodic nanopores.

The same setup is also used to measure the Seebeck coefficient (S) simultaneously. Using a micro-fabricated heater near the left side of the sample, a temperature gradient can be created. To avoid current leakage from the heater to the sample, the graphene layer between the heater and its nearest electrode for the current injection (i.e., the source terminal in Fig. I-1 inset) is cut with a focused ion beam (FIB). Two inner electrodes are now used as thermometers, with the local temperature T obtained from their temperature-dependent electrical resistance. The metal-line heater is much wider than the measured GAL strip so that the temperature variation along the two metal-line thermometers can be neglected. A similar setup has been used in the Seebeck measurements of nanoporous Si films [13]. In addition to the temperature gradient measurements, the same two inner probes are also used to measure the voltage drop ΔV. With the temperature difference ΔT between two metal-line thermometers, the slope of the ΔT-ΔV curve is extracted to compute $S=-d\Delta V/d\Delta T+S_{Au}$, in which S_{Au} is the compensated Seebeck coefficient of the Au voltage probes [14].

Figure I-2 displays the SEM images of two representative samples. The center-to-center distance between adjacent pores, also called pitch, are fixed as 30 nm. The neck width is 14.2±1 nm for both patterns. All nanopores are accurately defined by electron beam lithography (EBL). The original monolayer graphene is purchased from *Graphenea Inc*. These graphene samples are grown on a Cu foil through chemical vapor deposition (CVD) and then transferred onto a SiO_2/Si substrate. In a recent work also using CVD-grown graphene, GALs are fabricated with block copolymer (BCP) self-assembly as the mask for reactive ion etching (RIE) [2]. Only roughly hexagonal patterns can be defined by the BCP film. In contrast, the use of EBL in our study allows better structure controls for fundamental studies.

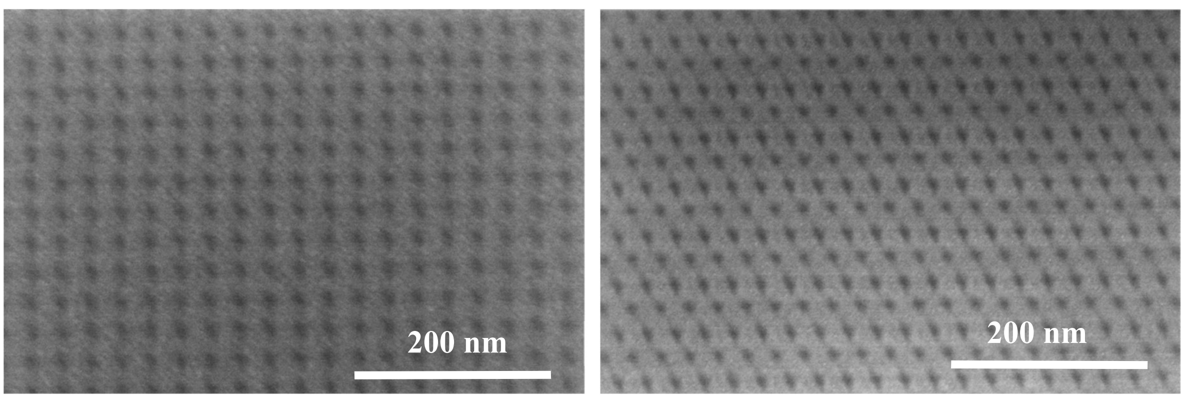


Figure I-2. SEM images of GALs with a square (left figure) and hexagonal array (right figure) of nanopores.

I.B Bandgap extraction of GALs

As the Arrhenius plot, Figure I-3 shows the temperature-dependent electrical conductivity σ corresponding to the OFF conductance, as the minimum electrical conductance under an applied gate voltage. With these temperature-dependent σ values, the bandgap E_g can be extracted by fitting [15]

$$\sigma_{OFF} = \sigma_0 \exp\left[-E_g/(2k_BT)\right], \quad \text{(I-1)}$$

where σ_0, k_B and T are a fitted constant, the Boltzmann constant and absolute temperature, respectively. Equation (1) attributes the temperature dependence of σ to thermally activated charge carriers. A band gap E_g ≈47.4 meV is extracted for the square pattern, in comparison to E_g ≈53 meV for the hexagonal pattern. With a given pitch P=30 nm and averaged pore diameter d ≈15.8 nm, the hexagonal pattern has stronger quantum confinement for charge carriers and thus a larger

E_g with a consistent neck width P-d between adjacent nanopores, whereas the square pattern has an expanded neck width $\sqrt{2}P$-d between the second-nearest-neighbor nanopores. Other than the neck width, the hexagonal pattern also has a 17% smaller characteristic length. Based on the ***mean beam length (MBL) used for radiation***, the characteristic length for a periodic 2D nanoporous structure is proportional to the solid-region area of one period divided by the pore perimeter [16, 17]. A smaller characteristic length indicates more influence from nanopores. These bandgap values are comparable to reported E_g ≈60 meV for a single-layer hexagonal GAL with a neck width n=12 nm [2]. This reported band gap is estimated with the same technique. In their measurements, σ at zero gate voltage is wrongly used instead of σ_{OFF} in an early study [15]. However, the divergence is usually small here.

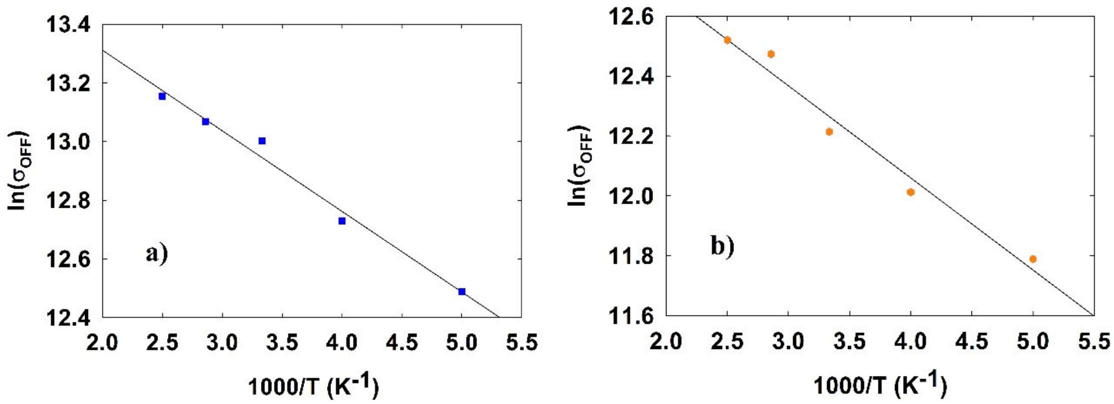


Figure I-3. Temperature-dependent σ_{OFF} for (a) square and (b) hexagonal patterns.

I.C Gate-voltage-tuned electrical properties

Figures I-4 (a) and (b) present the gate-voltage-tuned electrical conductivity σ and Seebeck coefficient S at 300 K. Away from the charge-neutrality point, a negative gate voltage can induce holes within the material as the "hole side." On the right side of both figures, a positive gate voltage can lead the sample into the "electron side." In the vicinity of the charge-neutrality point, the Seebeck coefficients of co-existing electrons and holes can largely cancel out. For GALs, n-type doping is observed here and is consistent with one previous study [2]. Again the hexagonal pattern leads to a smaller σ because of its smaller characteristic length and thus stronger charge carrier scattering due to nanopore boundaries and pore-edge-trapped charges. All measurement results are further compared to those reported for uncut pristine single-crystal graphene on a SiO_2 or hexagonal boron nitride (h-BN) substrate, measured with a similar setup [18]. For these undoped single-crystal samples, the charge neutrality point lies approximately at V_g=0 V. In this case, S and $S^2\sigma$ are both zero without an applied gate voltage. With antidots, reduced electrical conductivities are observed in GALs, whereas Seebeck coefficients are generally enhanced with band gaps opened in GALs. Compared to the existing electrical measurements of hexagonal single- and bi-layer GALs using a commercial setup with pressure contacts (TEP-600, Seepel Instrument, Korea) [2], the electrical properties measured in our work are more accurate due to the much better thermal contacts between the sample and deposited metallic probes. Although electrical contacts may not be a concern for σ measurements, the measurements of temperature difference ΔT across the GAL can be largely affected by the thermal contact between the sample and the thermal probes. When the thermal contacts were not good, $S = -\Delta V/\Delta T$ can be underestimated due to overestimated ΔT. As well acknowledged in the literature, this S

underestimation [19] may not be consistent due to possibly improved thermal contacts at elevated temperatures. In this aspect, metal deposition can ensure good thermal contact and is also used for thermal measurements of graphene using a microdevice [20]. In the reported data for single-layer hexagonal GALs on a SiO_2/Si substrate, the room-temperature S changes from 5±2 μV/K for pristine CVD graphene to -12±5 μV/K for a hexagonal GAL with neck width *n*=12 nm and an estimated band gap E_g ≈60 meV [2]. On the contrary, a dramatically improved $S = -190$±80 μV/K is found for a bilayer GAL with neck width *n*=8 nm and a much smaller E_g ≈25 meV. This contradiction may be attributed to the large uncertainties due to poor thermal contacts in the Seebeck coefficient measurements. In this work, more accurate measurements suggest significant Seebeck enhancement and the gate-voltage-dependent S is further measured to better understand the electron transport.

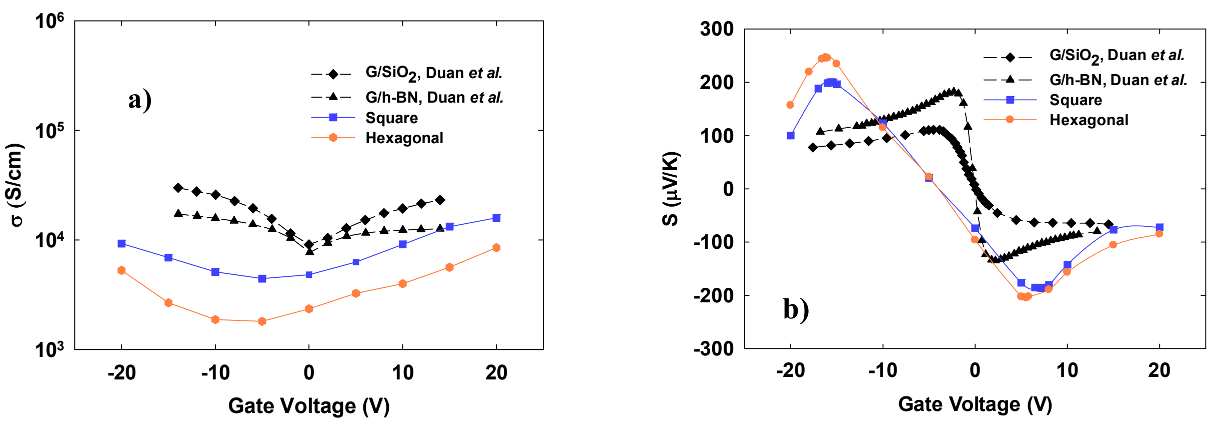


Figure I-4. Gate-voltage-tuned (a) electrical conductivities and (b) Seebeck coefficients at room temperature. All data are further compared with pristine single-crystal graphene on h-BN and SiO_2 substrates [18].

I.D Extracting the major scattering mechanism of charge carriers

Using the maximum $|S|$ for both the p and n types, the carriers' energy sensitivity (j) to scattering (CEStS) of GAL samples with square and hexagonal patterns are further calculated using an open-access code developed by Prof. Shuang Tang as our collaborator [21]. The CEStS can be described as, $j = -[d(\tau^{-1})/(\tau^{-1})]/(d\varepsilon/\varepsilon) = d(ln\tau)/d(ln\varepsilon)$, where τ is relaxation time, ε is the carrier's energy referring to the edge of the corresponding valley. This j indicates the energy dependence of τ. With a constant j, the power law $\tau \sim \varepsilon^j$ may apply.

The extracted j in Figure I-5 reflects a statistical measure of the average values of j for all existing scattering sources. For electrons and holes, their j values diverge from the averaged value within 10% and the averaged j value is plotted here. In principle, a positive j value indicates an increased relaxation time $\tau(\varepsilon)$ with increased charge-carrier energy ε, i.e., **a high-pass filter for charge carriers**. Such energy filtering can be found for a potential barrier at nanostructured interfaces [22] and the electric field around ionized impurities [14]. For GALs, the scattering mechanisms with j>0 include scattering by ionized center, thermal ripples and/or trapped charges at pore edges. The scattering by ionized centers [23, 24] and thermal ripples [25] has been well studied for graphene, giving relatively long MFPs for charge carriers. Besides these, analytical modeling of trapped charge scattering at the pore edges of general porous 2D materials and thin films has also been developed [16]. The trapped charges lead to a cylindrical electric field around each pore to scatter nearby charge carriers. When the spacing between adjacent nanopores is decreased below the MFPs of charge carriers in bulk graphene, the scattering by ionized centers and thermal ripples is negligible [26, 27] so that scattering by pore-edge-trapped charges becomes dominant. With a smaller characteristic length and stronger influence from pore-edge-trapped charges, the hexagonal pattern yields a larger j value for a GAL.

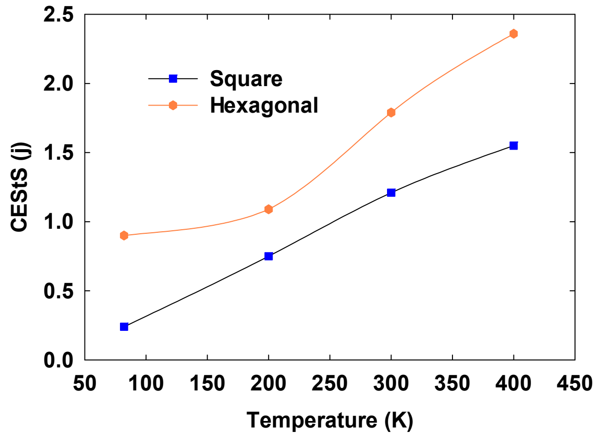


Figure I-5. The CEStS (j) of GALs with (a) a square array and (b) a hexagonal array of nanopores.

I.E Gate-voltage-enlarged power factors of GALs at varied temperatures

By tuning the gate voltage at each temperature, the power factor can be largely enhanced. Figures I-6 (a)-(d) shows the optimized gate voltage V_g to maximize $|S|$, the corresponding σ, S, and $S^2\sigma$ at different temperatures, respectively. At V_g around 5 V, the GALs show n-type properties (i.e., electron side), while p-type properties are shown at V_g around -15 V (i.e., hole side). For the same GAL, the power factors of both types are very close. Between the two GALs, the square pattern exceeds the hexagonal pattern for the power factor enhanced by V_g. The results are compared with that measured for pristine single-crystal graphene on h-BN and SiO_2 substrates, with a fixed gate voltage and thus constant carrier concentration at all temperatures [18]. At 400 K, a remarkable power factor of 554 $\mu W/cm{\cdot}K^2$ is achieved in the p-type GAL with a square pattern, which is far beyond the best power factors of bulk thermoelectric materials, e.g., ~50 $\mu W/cm{\cdot}K^2$ for BiSbTe alloys at 300 K [14].

The thermal conductivity k is not measured here to evaluate the thermoelectric figure of merit (ZT), where ZT is defined as $ZT = S^2\sigma T/k$, with T as the absolute temperature [14]. However, k is anticipated to be high according to the existing two-laser Raman thermometry measurements on suspended hexagonal monolayer GALs, which gives k ≈337±26 W/m·K for neck width n=12 nm, and k ≈579±42 W/m·K for n=16 nm close to the room temperature [2]. Such a high thermal conductivity can be suppressed by the presence of a substrate [28] but the reduction is anticipated to be limited. The resulting low ZT is not desirable for refrigeration applications. Typical thermoelectric refrigerators usually cool down an object to a temperature lower than that for the heat-rejection junction. In this case, a low k of the thermoelectric material is preferred to block the backward heat conduction and ZT is used to evaluate the material effectiveness. However, this is not the case for electronic cooling in which the hot spot to be cooled always has the highest temperature within the device [10]. In this case, **a high k (for passive cooling via heat conduction) combined with a high $S^2\sigma$ (active cooling)** are required to better dissipate the heat from the hot spot. With their extremely high power factors and thermal conductivities, GALs can be ideal for such "active coolers" in electronic devices.

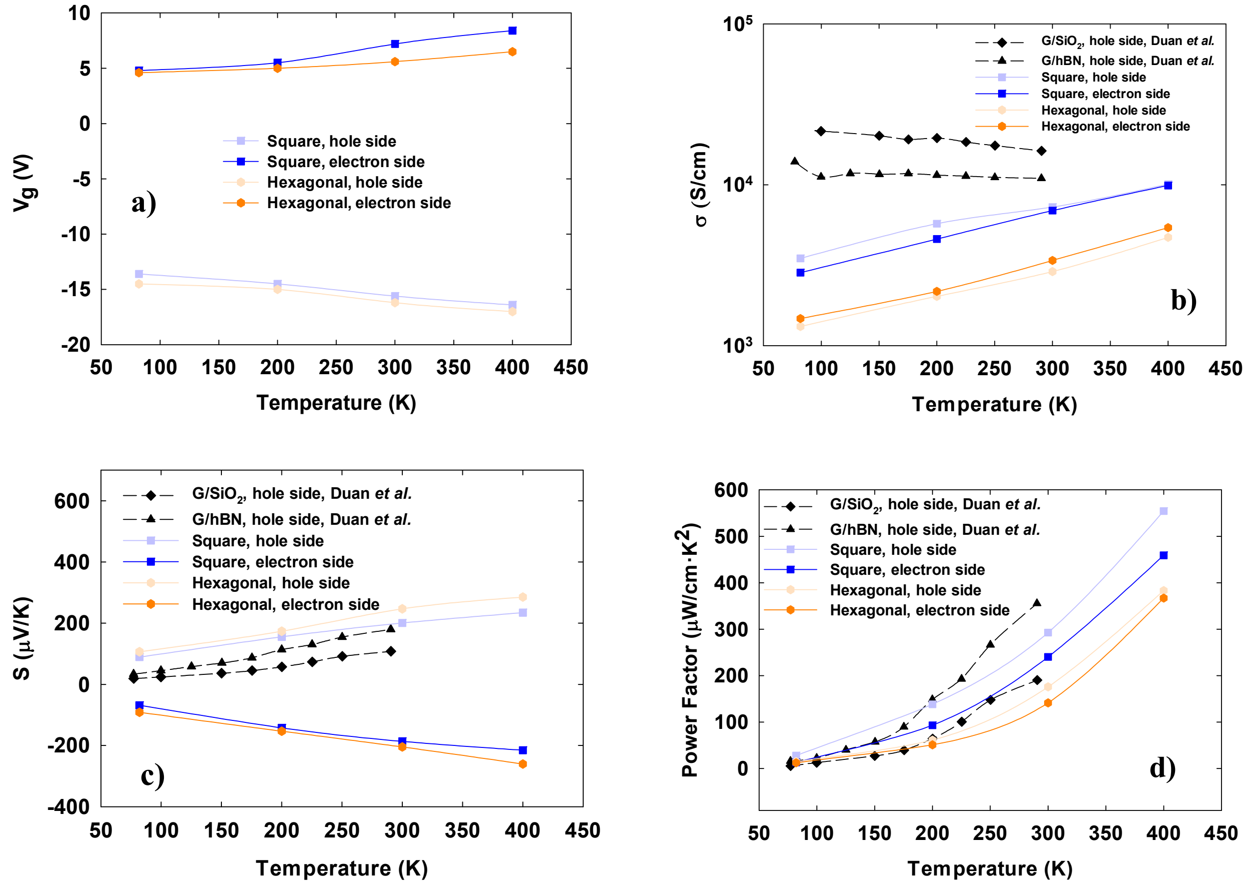


Figure I-6. Temperature-dependent (a) optimized gate voltage for maximum $|S|$, (b) the corresponding electrical conductivity, (c) peak Seebeck coefficient, and (d) power factor of measured GALs. All results are compared to those measured for pristine graphene with a fixed gate voltage and thus carrier concentration [18].

I.F Analytical Modeling vs. Electron Monte Carlo (MC) simulations

An analytical model has been developed to predict the electrical properties of a 2D material with a cylindrical potential field around each pore, resulting from the pore-edge-trapped charges [16]. The influence of the local potential field is averaged over the whole solid volume when an effective scattering rate is derived using the Fermi's golden rule. In principle, however, charge carriers are only affected by an electric field within the depletion region. Some errors are thus expected when an effective scattering rate for the whole solid volume is used.

In a more rigorous treatment, numerically solving the electron Boltzmann transport equation (BTE) is not feasible when the distribution function depends on too many parameters, e.g., location, direction, electron band, and energy. In this aspect, electron MC simulations [29-34] should be pursued as an alternative to solving the electron BTE. In these simulations, individual electrons are tracked for their movement and scattering processes. The influence of the energy barrier can be exactly included as the force applied to an electron within the depletion region. When steady states are achieved, the results from these simulations will statistically approach the solution of the BTE. As one big advantage, complicated geometry and detailed energy-dependent electron transport can be fully incorporated.

To compare, electron MC simulations are carried out on two-dimensional periodic nanoporous Si thin films with pore-edge charges and thus a potential barrier around each pore. The simulated electrical conductivities for varied temperatures (Figure I-7a) and pore-edge barrier heights (Figure I-7b) are compared to those predicted by the aforementioned analytical model as the dashed lines. Here circular pores are considered for an analytical model, whereas square pores are considered in the electron MC simulations to be consistent with rectangular subcells as spatial "bins" to count the local carrier concentration. All calculations assume 1.0×10^{20} cm^{-3} as the electron concentration, 80 nm pore perimeter, and a 60 nm pitch of the aligned pores. In general, the two predictions agree with each other.

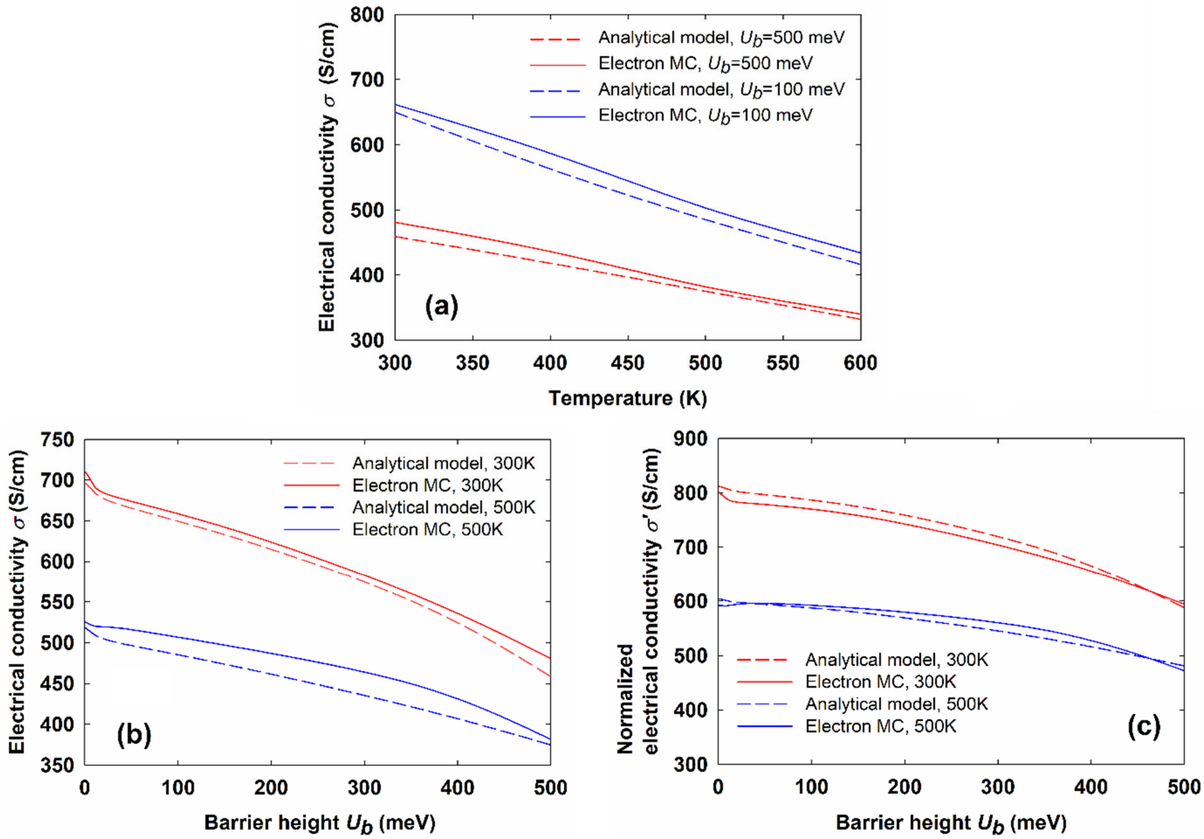


Figure I-7. (a) Temperature-dependent σ for U_b of 500 meV and 100 meV. (b) The barrier-height-dependent electrical conductivity at 300 K and 500 K. (c) Normalized electrical conductivity $\sigma' = \sigma/F(\varphi)$. The analytical model assumes circular pores, whereas the electron MC simulations assume square pores. All calculations have the same 80 nm pore perimeter with a 60 nm pitch of the aligned pores.

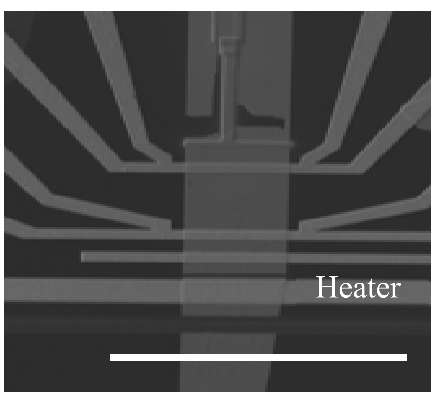
Some of the electrical conductivity reduction can be attributed to the reduced number of charge carriers due to pore-edge trapping. Figure I-7c presents normalized electrical conductivity with a factor of $F(\varphi) = 1 - \varphi$, where the effective porosity φ is determined by the percentage of the area within the depleted region, including the hollow region. This normalized electrical conductivity σ' can be viewed as that for a solid thin film with a uniform carrier concentration n and the same pore-edge electric field to scatter charge carriers. Compared with σ, this σ' decays slower with increased barrier heights. Again the analytical model and electron MC simulation yield very close predictions.

I.G Electrical studies of tellurene

Beyond graphene, electrical measurements are also extended to tellurene as a promising 2D material for various device applications [35]. For mass production, this novel 2D material can be synthesized with a substrate-free solution process with a low cost and high productivity. This synthesis technique is in contrast with typical 2D materials grown on a substrate, with generally low yield and high cost for some systems. The obtained tellurene exhibits controllable thicknesses from a few to tens of nanometers, and lateral sizes up to 100 μm. For tellurene transistors, they can be stable in the ambient for over two months, with on/off ratios and current densities on the order of 106 and 550 mA/mm, respectively. The thickness-dependent carrier mobility reaches the highest values ~700 $cm^2/V{\cdot}s$ for a thickness of ~16 nm.

A similar gate-voltage-dependent electrical property measurement was carried out on tellurene samples provided by Prof. Wenzhuo Wu at Purdue University. Figure I-8a displays the measurement setup, similar to Figure I-1. All electrical measurements are along the long axis of the trapezoidal sample that is anisotropic for transport properties [35]. Figure I-8b further shows the preliminary results for a representative sample. Due to its intrinsically high p-type doping, the sample cannot be converted into n-type within the regime of the gate voltage (-20 to 20 V). A new power supply is purchased (up to 250 V) to obtain a full picture of voltage-dependent electrical properties. A journal paper is under preparation for the electrical studies of this novel 2D material.

(a)



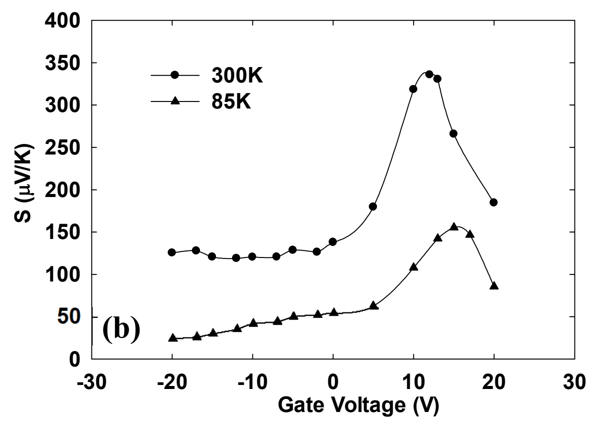


Figure I-8. (a) SEM image of the measurement setup (scale bar as 50 μm). (b) Gate-voltage-dependent Seebeck coefficients of representative tellurene.

II. Phonon studies of periodic nanoporous thin films

Thermal measurements usually require suspended samples. However, it is hard to carry out such measurements on a GAL because extremely fragile GALs can be easily damaged during the sample preparation. Without losing the generality, the in-plane k of periodic nanoporous Si films [36] and the cross-plane k of nanoporous $In_{0.1}Ga_{0.9}N$ films [37] are studied to gain some insights of phonon transport within periodic nanoporous structures.

In general, thermal transport within periodic nanoporous structures can be more complicated than simple diffusive phonon scattering on pore edges. For widely studied periodic nanoporous Si films, inconsistency can often be found among experimental and theoretical studies of reduced lattice thermal conductivity for varied nanoporous patterns. Such divergence can be partially attributed to measurement errors and pore-edge damage introduced by varied nanofabrication techniques, namely RIE [38-45], deep RIE (DRIE) [13, 46-48], and a FIB [49]. In our studies, attention is thus paid to the ***impact of the employed pore-drilling technique***. In general, increased pore-edge defects are anticipated for FIB drilling with typically more surface damages [50]. Improvement on the thermal measurements is also emphasized to obtain reliable data for phonon transport analysis. Based on our current understanding for phonon transport within nanoporous films and other periodic nanostructures, a review paper is under preparation, in collaboration with Prof. Fabio Semperlotti at Purdue University.

II.A Current understanding for phonon transport within periodic nanoporous Si films

Figure II.1 shows selected data from reported in-plane k_L of periodic nanoporous Si films at room temperature. All measurement data are divided by $1-\Phi$ to obtain the k_L for the solid counterpart, with Φ as the porosity. The line is by calculations assuming bulk-like phonon transport and diffusive phonon scattering by pore edges [17, 51]. A **"universal curve"** is plotted here, where the MBL of the porous structure (also see Section I.B) is used to modify the bulk phonon MFPs with the Matthiessen's rule. The computed k_L is close to the predictions from complicated phonon MC simulations. First-principles bulk phonon MFPs in Si [52] are used here. As pointed out in our study, this MBL functions as the characteristic length of the porous structure, similar to the diameter of a nanowire [17]. For 2D porous thin films, this MBL is given as $MBL = 4A_{Solid}/P_{Pore}$, in which A_{Solid} is the solid area within a period and P_{Pore} is the pore diameter. The use of MBL allows direct comparison between data with varied pitches and porosities, giving dramatically redueced complexity. In addition, both the hexagonal and square patterns can be included in the same universal curve. Besides some studies (e.g., Ref. [42] here), the in-plane k_L at room temperature was much lower than the universal curve. Further considering the diffusive phonon scattering by the top and bottom surfaces of a thin film did not largely reduce the divergence for ~100 nm or shorter pitches.

In one hypothesis, the observed k_L reduction has been attributed to the coherent phonon transport within the periodic nanoporous structure [15, 42, 53, 54], which can modify the phonon dispersion and thus lower the k_L. At 300 K, such "phononic effects" can be critical to superlattices with atomically smooth interfaces and <5 nm periods [55]. However, the studied nanoporous thin films usually have a structure feature size of ~10 nm to micrometers, which is much larger than the dominant phonon wavelength for Si (1–10 nm at 300 K [56, 57]). In addition, the usually rough pore edges should diffusively scatter phonons so that the phonon phase and coherence are destroyed. The phononic effects are anticipated to be weak in this case. More recent comparison studies between periodic and aperiodic nanoporous films further suggested negligible phononic effects above 10 K for films with 300 nm pitches [43], and above 14 K for Si nanomeshes with >100 nm pitches [47]. This conclusion was also supported by measurements on Si nanoporous films with 200–300 nm pitch, where incoherent phonon transport was confirmed at 300–1000 K [58].

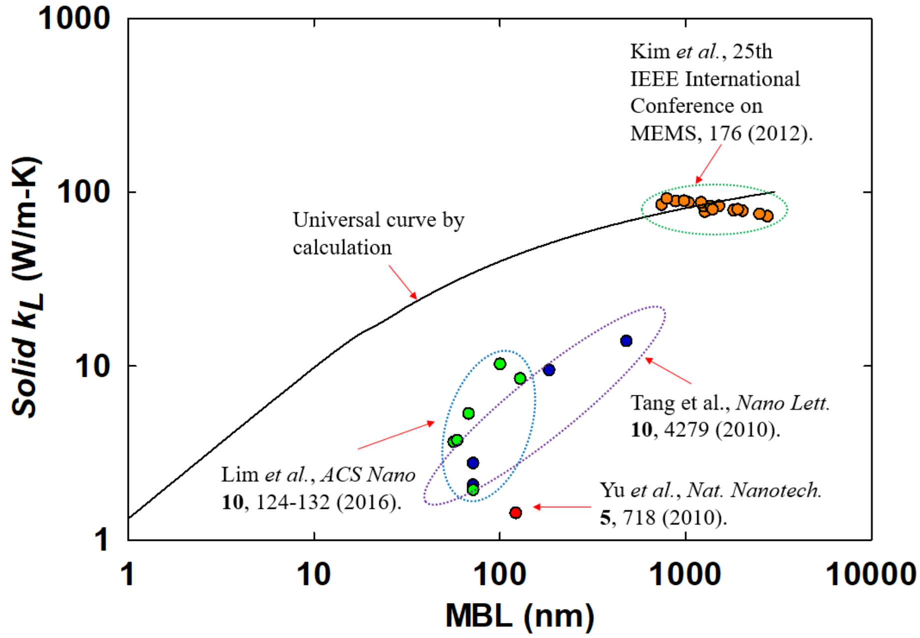


Figure II-1. Comparison between predicted (a universal curve) and measured (symbols) in-plane solid k_L of porous Si films at 300 K.

Only considering incoherent phonon transport, calculations for nanoporous films [56] agreed well with the measurements by El-Kady *et al.* for nanoporous films with 500–900 nm pitch, 7–38% porosity, and 500 nm film thickness [59]. Similarly, agreement with theoretical modeling was also found in our cross-plane k measurements on nanoporous $In_{0.1}Ga_{0.9}N$ films with 450–900 nm pitches and a fixed 300 nm pore diameter [37] (see Section II.E). This contradicted with earlier cross-plane thermal measurements on nanoporous Si films with sub-micron feature sizes, where phononic effects were proposed to explain the k_L reduction [53]. For even smaller features, the measurement data of nanoporous films with a ~34 nm pitch [15] were successfully explained with a slightly expanded effective pore diameter to account for the pore-edge amorphization and oxidation [57]. These pore-edge defects were emphasized in molecular dynamics simulations [60, 61] and were found in the transmission electron microscopy (TEM) [13] or SEM [43, 44] studies of real samples. As one example to show the influence of fabrication-introduced surface defects on phonon transport, k of RIE-patterned Si nanowires [62] was far lower than that for Si nanowires synthesized by the vapor-liquid-solid method [63].

For phonon transport analysis of nanoporous thin films, different bulk phonon MFPs and phonon dispersions employed may lead to some divergence. On the other side, accuracy of some cited measurements should also be questioned. In some studies, a thin-film sample was transferred onto a micro-device for measurements. The possibly large thermal contact resistance between a thin film and the microdevice may overshadow the thermal resistance of the film itself and lead to large underestimation for reported k value [13, 15]. Some unphysical fluctuations were found in temperature-dependent k values, indicating possible variation of the sample-device thermal contact during thermal measurements [13, 15]. Furthermore, some distortion and damage of a fragile nanoporous film during the film transfer and the following fabrication processes may also strongly affect k_L. Such issues were addressed in more recent studies using an integrated device fabricated from the same Si film or using micro time-domain thermoreflectance measurements on a suspended sample, where the measured k values were mostly comparable to or higher than the theoretical predictions at 300 K [39-43, 46-48].

II.B Simultaneous measurements of k and specific heat C

The measured suspended film was fabricated from the 220-nm-thick device layer of a silicon-on-insulator (SOI) wafer. The nanoporous film and the four-probe electrical probes to the film were defined by EBL and then etched by DRIE, as shown by the SEM image in Figure II-2a. The measured nanoporous film was 20 μm in length and 2 μm in width. The diameter/pitch combinations of aligned nanopores included 300/600, 200/400, 100/200, and 50/150 nm. The three larger porous patterns showed well-defined pore shape and generally <5 nm uncertainties in pore diameters (Figure II-2b). However, the smallest 50-nm-diameter pores became irregular after etching and the averaged porosity Φ was estimated as 31% using software (ImageJ) to read the SEM image (Figure II-2c). The effective pore diameter was estimated as 94 nm. The porous film was fully suspended by etching off the underneath oxide layer. Because the employed Si layer has a very low electrical conductivity (5–10 S/m), the whole structure was further coated with a 10-nm-thick Cr adhesion layer and then a 40-nm-thick Pt layer. The metallic coating was used as both heater and electrical-resistance thermometer in thermal studies. In comparison, similar nanoporous films were also fabricated using a FIB for the 300/600 nm and 200/400 nm patterns. Instead, 10-nm-thick Cr and 20-nm-thick Au layers were coated onto FIB samples. Unlike DRIE drilling, even smaller pores could not be fabricated due to the limited aspect ratio for FIB drilling.

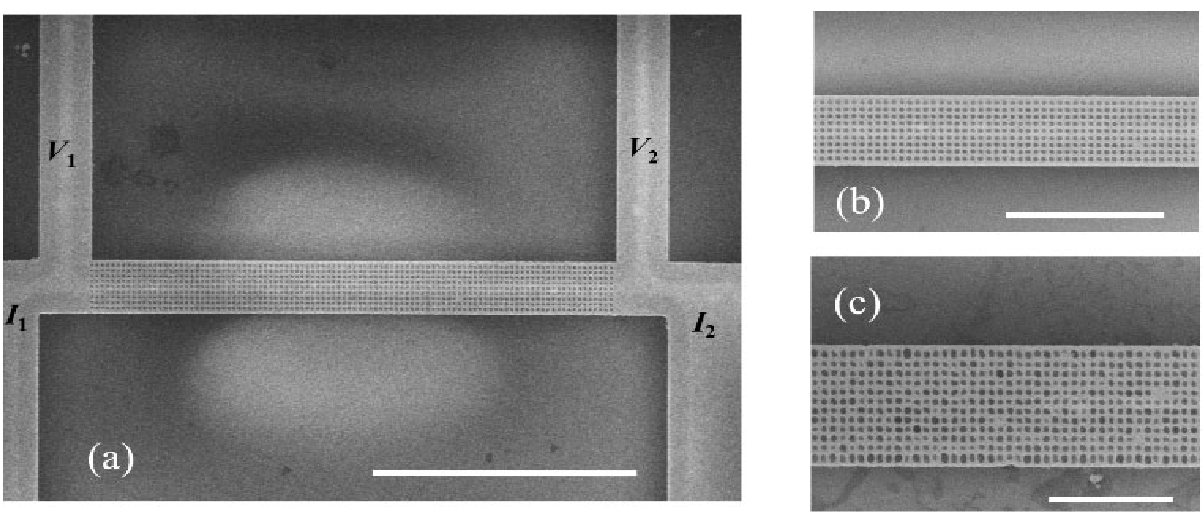


Figure II-2. (a) Suspended nanoporous Si film (pitch/diameter as 200/100 nm) with four electrical probes for thermal measurements and (b) SEM image of nanopores on this film. (c) Film with irregular pores slightly over-etched from 50 nm diameter. Scale bars are 10, 4, and 2 μm, respectively.

The challenge in the thermal studies of nanoporous thin films lies in that k_L can be affected by both the phonon dispersion modification and the scattering by amorphous pore edges. These two effects are difficult to be distinguished in the k_L analysis. In this work, this issue is addressed with specific heat measurements on a suspended nanoporous Si film, in addition to its in-plane k measurements. In physics, C is solely dependent on the phonon dispersion, whereas k_L also relies on the phonon scattering. The C and k_L measurements shown here can be applied to general nanoporous Si films to better understand the influence of amorphous pore edges and phononic effect on their k_L. Both the in-plane $k \approx k_L$ and volumetric specific heat C of a nanoporous film can be extracted from 3ω measurements developed for suspended samples [64]. The measured specific heat per unit volume, C, is divided by $1 - \Phi$ to obtain the C value for the corresponding solid film.

In data analysis, the effective thermal conductance of the measured film also includes the contribution from the metal layer. The thermal conductance and thus k of the nanoporous Si film can be obtained by subtracting the metal layer contribution. For the in-plane thermal conductance G_m of the metal layer, the Wiedemann–Franz law suggests $k \approx k_E = L\sigma T$ and thus $G_m = LT/R$, in which R is the electrical resistance of the metal layer. The employed Lorenz number L has been determined for a suspended Cr/Pt film that is deposited in the same condition as the metallic coating for nanoporous Si films.

II.C Structure characterization of nanopores

The pore-edge roughness was examined with an SEM [43, 44] for a suspended nanoporous thin film before the metal coating was deposited (Figure II-3a). Such rough pore edges were typically amorphous and often oxidized. In an early study, it was hypothesized that the effective pore diameter should be expanded by the ~200 nm surface roughness of micro-pores drill by DRIE [46]. For DRIE-drilled samples in this study, the width of amorphous edges was roughly 13, 25, 45, and 40 nm for pore sizes of 50(94), 100, 200, and 300 nm, respectively.

(a) (b) (c)

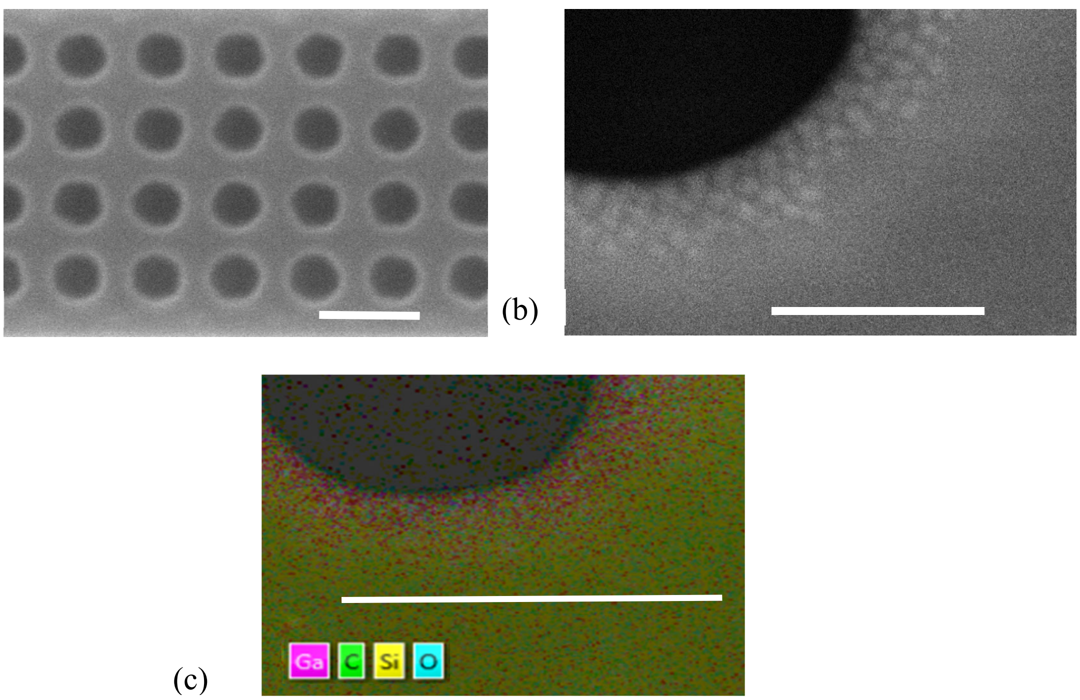


Figure II-3. (a) Top-view SEM image of a suspended Si film with 200-nm-diameter nanopores. (b) Dark-field TEM image of a 70-nm-thick Si film with a 200-nm-diameter pore drilled by a FIB. (c) Element mapping with EDX for a 250-nm-diameter pore drill by a FIB on the 70-nm-thick Si film. Scale bars are 500, 100, and 250 nm from (a) to (c), respectively.

For FIB drilling, the damage induced may include an amorphous surface layer of ~10 nm thickness, Ga ion implantation, lattice defects (vacancies, interstitials, and dislocations), and large atom displacement within the collision cascade that extends tens of nanometers from the targeted surface [50]. Because the current 220 nm film thickness was too thick for TEM studies, the pore-edge defects were cross-checked with a TEM using a 70-nm-thick film drilled with a FIB. For 200-nm-diameter pores, the amorphous region was 50–70 nm wide (Figure II-3b). Further check with energy dispersive x-ray spectroscopy (EDX) identified Ga ion implantation both within and outside the amorphous edge (Figure II-3c).

II.D Temperature-dependent k and C

Representative ~100 nm nanoporous patterns were investigated for their impact on k. As the reference, a solid film was measured and its room-temperature k≈86 W/m·K agreed well with k≈85 W/m·K in previous studies [65]. For each nanoporous pattern, two to four samples were measured for films drilled by DRIE. At room temperature, the standard deviation of k was within 2.3–5.1% of the average k values for each pattern, which suggested high repeatability of our measurements. In addition, two FIB-drilled samples were measured and showed k lower than that for films drilled by DRIE.

Figure II-4 compares the measurements and simulations for temperature-dependent $k \approx k_L$ of all nanoporous thin films. Considering the amorphous pore edges in Fig. 5, the effective pore diameters are 120, 150, 290, and 380 nm for the 50(94), 100, 200, and 300 nm pore diameters in DRIE-drilled films, respectively. For FIB-drilled films, the effective diameters for 200 and 300 nm pore diameters are increased by 100 nm. The Ga ion implantation during FIB cutting can further lower k with stronger point-defect scattering of phonons. Such effects are not considered here to simplify the analysis. In general, the measurement data agree well with predictions by phonon MC simulations using effective pore diameters.

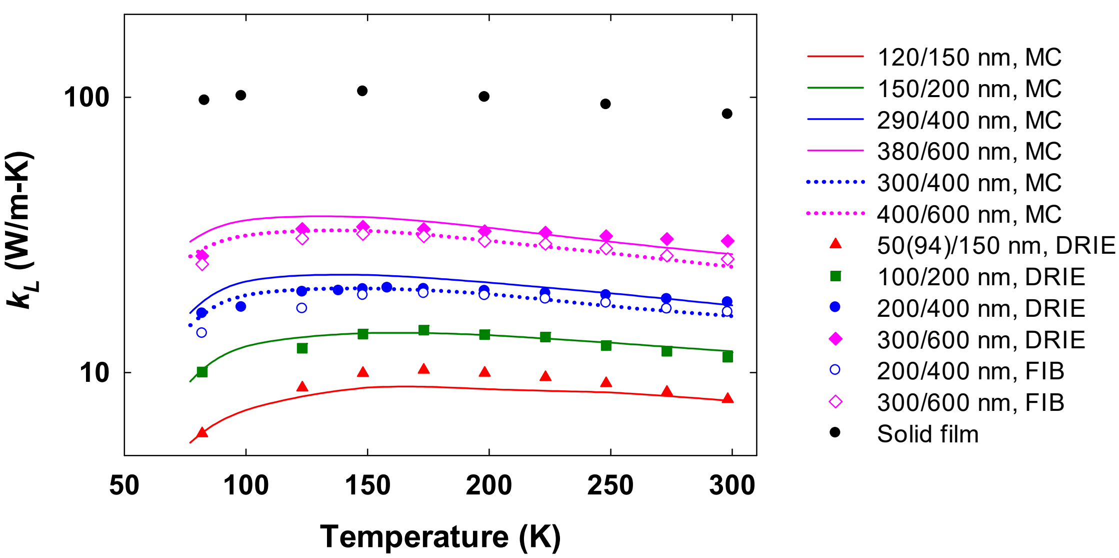


Figure II-4. Temperature-dependent k_L of the solid and nanoporous Si thin film (symbols), in comparison to predictions by MC simulations (lines) using an effective pore diameter indicated in the legend. The diameter/pitch combinations are given in the legend. The color of lines matches the corresponding measurement data. The solid lines are for DRIE samples and the dashed lines are for two FIB samples.

As one highlight of this work, Figures II-5a and 5b present the corresponding solid volumetric specific heat C for bilayer films patterned with DRIE and a FIB, respectively. For nanoporous films, all measured C values are divided by $(1-\Phi)$ without considering the impact of amorphous pore edges. In comparison, C is also computed using the bulk specific heat for each material layer and their thicknesses. In SEM examination of the FIB-cut cross section, ±5 nm thickness uncertainties have been found in the Si and metallic layers. The corresponding range of the prediction is indicated by the green band. Good agreement can be observed between the solid film (filled black circle) and the prediction. In spite of the large variation in the structure dimension, all data for nanoporous films are consistent among themselves, indicating negligible phonon dispersion modifications. Some divergence of solid C is found for nanoporous films, which can be attributed to the inaccuracy in Φ and additional pore-edge defects. Nevertheless, the solid C values of nanoporous Si films still follow the trend for a solid film. Our conclusion here contradicts with previously claimed phononic effects for a Si film with pitches of 500–800 nm [53].

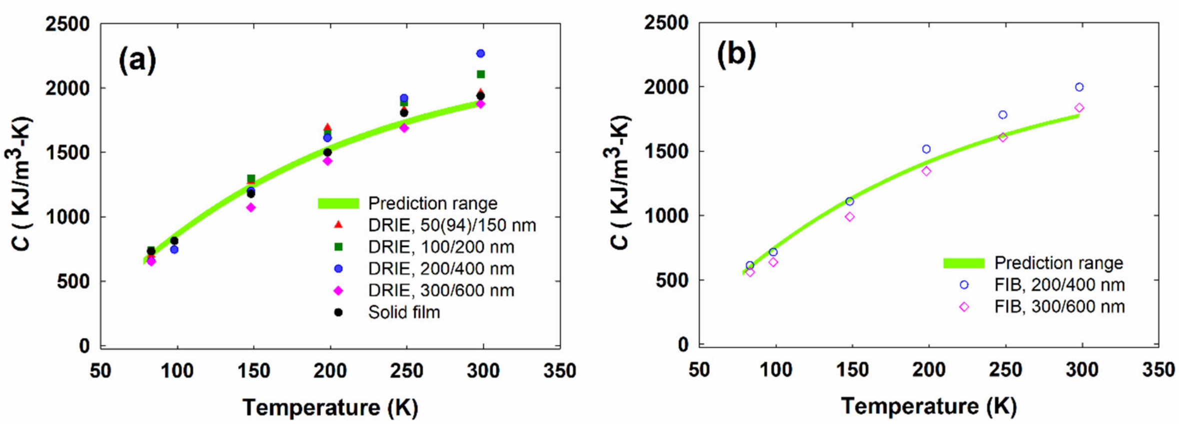


Figure II-5. Temperature-dependent solid C of bilayer films drilled by (a) DRIE and (b) a FIB, in comparison to the prediction using bulk C values for metals and Si.

II.E Cross-plane thermal studies of nanoporous $In_{0.1}Ga_{0.9}N$ films

The understanding of phonon transport in nanoporous Si films and 2D materials can be extended to general alloy films. Here we have extended the study to nanoporous $In_{0.1}Ga_{0.9}N$ thin films that can be used for on-chip thermoelectric cooling to effectively remove heat from the hot spot within GaN-based transistors. To integrate such thermoelectric coolers with a GaN transistor, the selected thermoelectric materials should have a thermal expansion coefficient close to that for GaN for better compatibility. Along this line, GaN-based alloys are recommended for such thermoelectric devices [66]. For GaN alloys, the power factor $S^2\sigma$ can be better than those for the state-of-the-art high-temperature thermoelectric materials such as Si_xGe_{1-x} alloys [67]. Following this, an even high ZT can be achieved in nanoporous films of GaN alloys, with a reduced lattice thermal conductivity and bulk-like electrical properties.

Figures II-6a and 6b show the SEM images of representative nanoporous films. Different from reported nanoporous Si films with nanofabricated pores by dry etching [13, 38, 39, 42, 45, 46, 48, 53, 68, 69], our nanoporous $In_{0.1}Ga_{0.9}N$ films were ***directly grown*** on the substrate, with the nanopores defined by SiO_2 pillars as masks. After the high-temperature growth, SiO_2 nanopillars were removed with hydrogen fluoride to obtain the nanoporous pattern. In contrast with nanofabricated pores, directly grown nanopores have ***minimized pore-edge defects*** to eliminate the influence of amorphous pore edges on *k*, as proposed for nanoporous Si films [57].

Cross-plane *k* has been measured for fabricated $In_{0.1}Ga_{0.9}N$ thin films via the time-domain thermoreflectance (TDTR) method. These measurements are carried out by Prof. Xiaojia Wang at University of Minnesota Twin Cities. TDTR is an optical-based, accurate, and robust technique applicable of probing various thermal properties, including thermal conductivity, interfacial thermal conductance, and heat capacity of sample systems ranging from thin films, bulk substrates, to nanoparticles. Prior to thermal measurements, a 55-nm-thick layer of aluminum was coated onto the whole wafer by electron beam deposition to serve as the optical transducer.

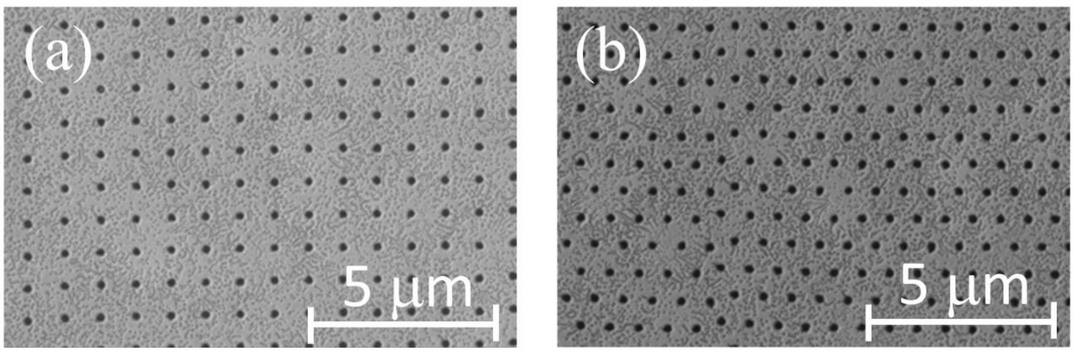


Figure II-6. SEM images of nanoporous $In_{0.1}Ga_{0.9}N$ films with (a) aligned pores or (b) hexagonally aligned pores.

Figure II-7 shows the measured cross-plane *k* (symbols) compared to phonon transport modeling (line) assuming bulk phonon MFPs and diffusive pore-edge phonon scattering. The uncertainty due to thermal penetration into the substrate is indicated with error bars. In addition, the contribution of electronic thermal conductivity k_E is estimated to be <0.1 W/m·K for a film with similar compositions at 300 K [70]. Therefore, $k \approx k_L$ is assumed in the current analysis. In general, the experimental data agree well with the modeling. More details for the modeling and experiments can be found elsewhere [71].

In previous studies on the cross-plane k_L of nanoporous Si films with comparable structure dimensions, it was suggested that phononic effects may play an important role in the k_L reduction [53]. The measured low *k* values cannot be fully explained with diffusive pore-edge scattering of phonons [56]. In contrast, our work clearly shows that ***diffusive phonon scattering by pore edges alone can explain the measurement results***. Our conclusion is thus aligned with the analysis that suggests negligible phononic effects for ~100 nm or larger periodic porous structures [45, 56, 57]. The low *k* found for Si films may be attributed to structural damage in real films, which can be introduced by nanopore drilling with dry etching or other steps in the fabrication process. Such unintentional damage is minimized with direct MOCVD growth of nanoporous films.

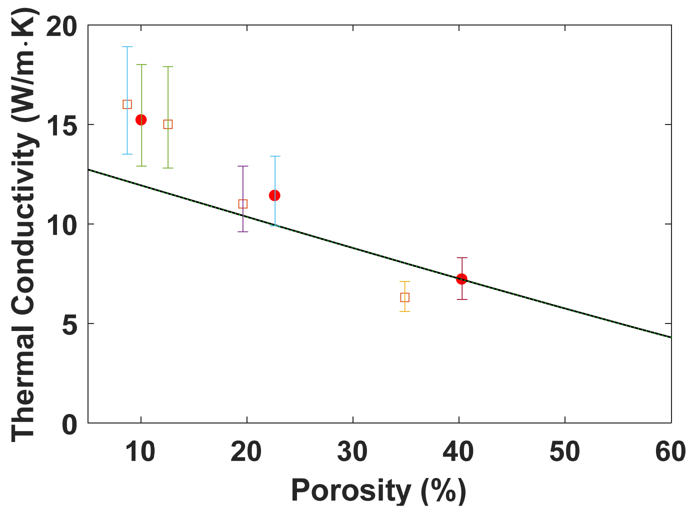


Figure II-7. Comparison between the measured and predicted *k* values for tri-layered nanoporous GaN-based films. Here filled circles are for hexagonal patterns, whereas empty squares are for patterns on a square lattice.

II.G Nanoporous thin films with added periodic nanopores

In the literature, phononic effects are justified by *a)* comparing different films with periodic and aperiodic patterns [43, 47] and *b)* specific heat measurements in our recent study [36]. As a new approach, the same suspended 70-nm-thick Si film has been repeatedly measured for its thermal resistance with added rows of 70-nm-diameter and 140-nm-pitched nanopores drilled with a FIB. This concept can be compared to previous studies on photon transmission over a Bragg reflector with different numbers of periodic layers [72]. Based on wave optics, the transmittance should decrease to a constant value over a certain number of layers, whereas the ray tracing technique (i.e., particle view) predicts a continuously reduced photon transmittance with an increased number of layers.

The proposed thermal measurements were carried out on thin-film samples fabricated into a suspended T-junction microdevice (Figure II-8a), with the measured part being the short beam of the device. In Figure II-8a, two additional short beams were patterned above the long beam to help protect this beam during the suspension process. These two supporting beams were cut with a FIB after suspending the device by etching off the SiO_2 layer underlying the device. Additional rows of pores were drilled with a FIB between separated measurements (Figures II-8b and 8c). Some small distortion on the edge was observed due to overheating of the short beam during the cutting process. Along the long beam, a metallic heater/thermometer was deposited. For electrically conductive films, the whole device was coated with 30-nm-thick SiN_x for electrical insulation. Similar T-junction devices were used to measure thermal conductivities of various nanostructures [73, 74]. In comparison, the proposed microdevice was fabricated from the same thin film to eliminate the ***critical sample-device thermal contact*** (see discussions in Section II.A) that may significantly increase the measured in-plane thermal resistance of a sample and yield misleading results [73, 75].

In measurements, the electrical resistance R_e of the heater/thermometer line is calibrated as a function of temperature. In high-vacuum measurements, a dc current is passed through the metal line to create a temperature difference across the short beam. The average temperature rise of the long beam, $\Delta\bar{T}$, can be extracted from R_e variation. The in-plane thermal resistance of the short beam can be extracted by comparing $\Delta\bar{T}$ of a device with and without the short beam (Figure II-9 as the temperature profiles). The latter case (i.e., long beam only) will yield the in-plane thermal resistance of the long beam itself. In practice, the reference device with only the long beam can be prepared in the same way as T-junction devices, or by cutting off the short beam of a device using a FIB after all measurements. In our measurement, FIB cutting was used to ensure the long-beam calibration was consistent with the measured device.

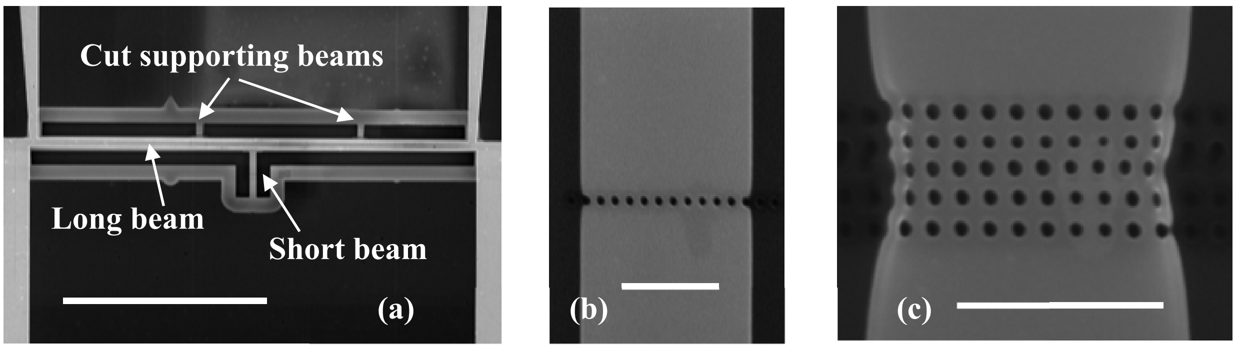


Figure II-8. SEM image of the T-junction device with pores drilled on the short beam: (a) Overview of the device; (b) short beam with one row of pores; and (c) short beam with five rows of pores.

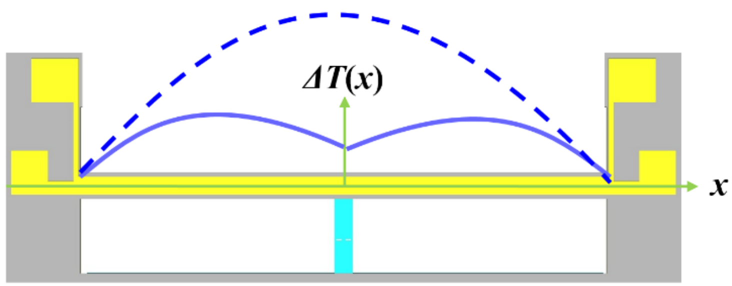


Figure II-9. Temperature profile along the long beam with the short beam (*solid line*) and without the short beam (*dashed line*). The short beam will be cut with a FIB for the latter measurement.

Figure II-10 shows the measured thermal resistance of the short beam with increased number of pore rows. It can be observed that additional rows introduced comparable amount of thermal resistances. If wave effects for heat conduction is strong, large difference should be observed between the thermal resistances of films with one row and three rows of pores, as the latter starts to induce phonon interference within a periodic structure. However, the current results do not show such contrast. Considering only the classical phonon size effects, phonon MC simulations are currently carried out to compare with these measurement results. A journal paper is under preparation and a presentation is scheduled for MRS Spring Meeting in Phoenix (April 22, 2019).

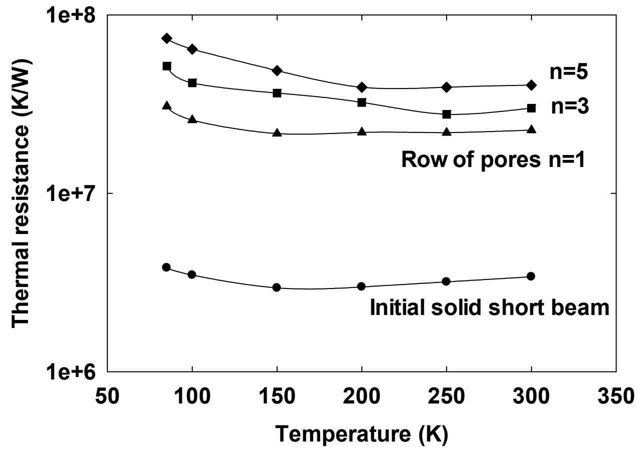


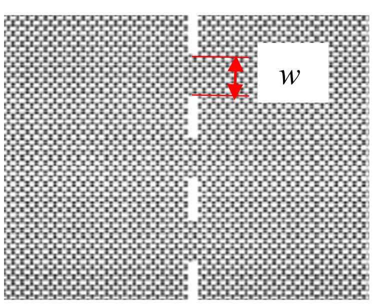
Figure II-10. Temperature-dependent thermal resistance of a Si short beam with increased rows of nanopores drilled by a FIB.

III. New studies of nanoslot-patterned thin films

III.A Analytical model to predict the reduced lattice thermal conductivity

Different from nanoporous thin films, different nanoporous patterns are also explored for the potential ZT enhancement. Particular attention has been given to nanoslot-patterned thin films and 2D materials (e.g., graphene in Figure III-1a [76]), with the neck width w between adjacent nanoslots much shorter than the majority phonon MFPs to dramatically reduce k_L. When w is still longer than the MFPs of charge carriers, the electrical properties can be conserved, leading to enhanced ZTs.

The k_L reduction due to nanoslot patterns is related to the so-called "ballistic thermal resistances" for phonons passing through a geometrical constriction with its size D comparable with or shorter than the MFP Λ of these phonons. For the nanoslot patterns, D is simply w to restrict the phonon transport. In this situation, phonons with $\Lambda>D$ have fewer opportunities to be scattered near the constriction. In particular, phonons with $\Lambda \gg D$ travel ballistically away from the constriction location, in analogy to thermal radiation over a region with a characteristic length ~Λ. The actual heat flux can be much lower than the predictions by the Fourier's law that assumes diffusive phonon transport. Figure III-1b shows the temperature profile of a represented Si thin film with patterned nanoslots.

(a) 

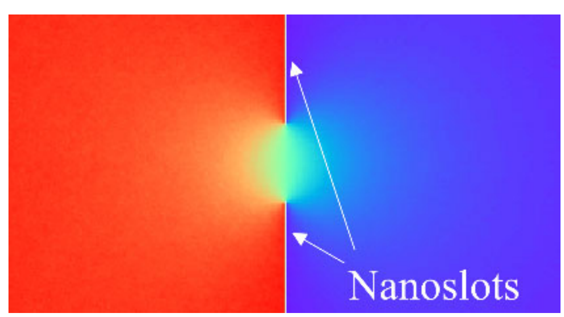
(b) 

Figure III-1. (a) Patterned graphene with ballistic thermal resistance R_b introduced for the narrow neck width W between nanoslots. (b) Simulated temperature profile near the narrow gap between nanoslots drilled on a thin film.

Figure III-2 shows the studied nanoslot-patterned thin film sandwiched between two thermal reservoirs, which is consistent with typical measurements using two isothermal membranes bridged by the measured thin film [13, 38].

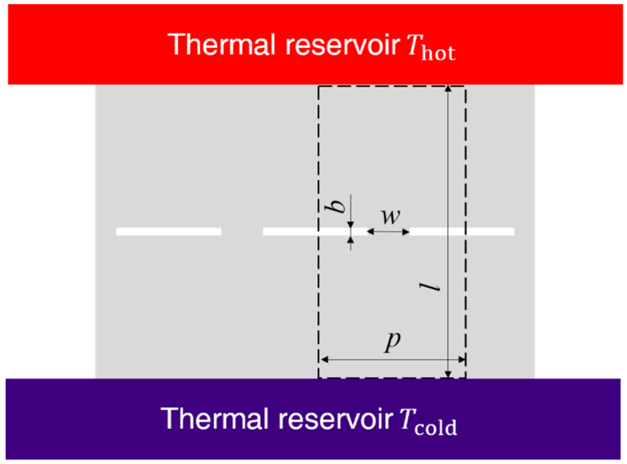


Figure III-2. Illustration of a thin film with a row of periodic nanoslots pattered, with pitch p, neck width w, depth b and film length l. A single period is enclosed with the dashed line.

For k_L predictions, the suppression function S will be used for the analysis, which can replace the time-consuming phonon MC simulations. Considering diffusive phonon scattering by nanoslot edges, this factor describes the reduction of heat flow due to the drilled nanoslot pattern for phonons with a given MFP. For a 2D material with fixed p and l, the lattice thermal conductivity for nanoslot patterns can be evaluated by $k_L = \int_0^\infty \mathrm{S}(\eta) k_L(\Lambda) \mathrm{d}\Lambda$, in which $\eta = \Lambda/w$, $k_L(\Lambda)$ is the spectral lattice thermal conductivity of phonons with a MFP Λ in the pristine 2D material. For a very small depth b in Figure III-2 (e.g., sub-10 nm with EBL resolutions), its impact on k_L can be neglected. The same $\mathrm{S}(\eta)$ can also be applied to quasi-2D thin film with smooth top and bottom surfaces. In the literature, $k_L(\Lambda)$ is available for graphene with varied defects [77] for above calculations. Figure III-3 shows the $\mathrm{S}(\eta)$ function computed for fixed b=5 nm, l=1 μm and p=500 nm, using phonon MC simulations assuming a constant phonon MFP for all phonons (crosses).

An analytical model of $\mathrm{S}(\eta)$ has also been derived in our recent work (under review now) and is plotted as lines in Figure III-3. Assuming the 2D nanoporous pattern introduces a characteristic length L_C to modify Λ_{eff}, the suppression factor is

$$S(\eta) = \frac{\left(\frac{1}{\Lambda_{eff}} + \frac{1}{L_C}\right)^{-1}}{\Lambda_{eff}} H_w = \frac{L_C}{\Lambda_{eff} + L_C} H_w = \frac{L_C}{\eta w + L_C} H_w, \tag{III-1}$$

Here H_w is the Fourier-law correction factor to account for the reduced heat-transfer cross section area due to nanoslots (see our studies on nanoporous Si film with similar correction factors [17]), whereas L_C further addresses the influence of the nanopattern on phonon transport. By evaluating $S(\eta \to \infty)$ and comparing it to an available solution for completely ballistic phonon transport across a nano-neck in Figure III-1b [78], L_c is determined as

$$L_c = \frac{w}{p} \frac{3l}{4H_w}. \tag{III-2}$$

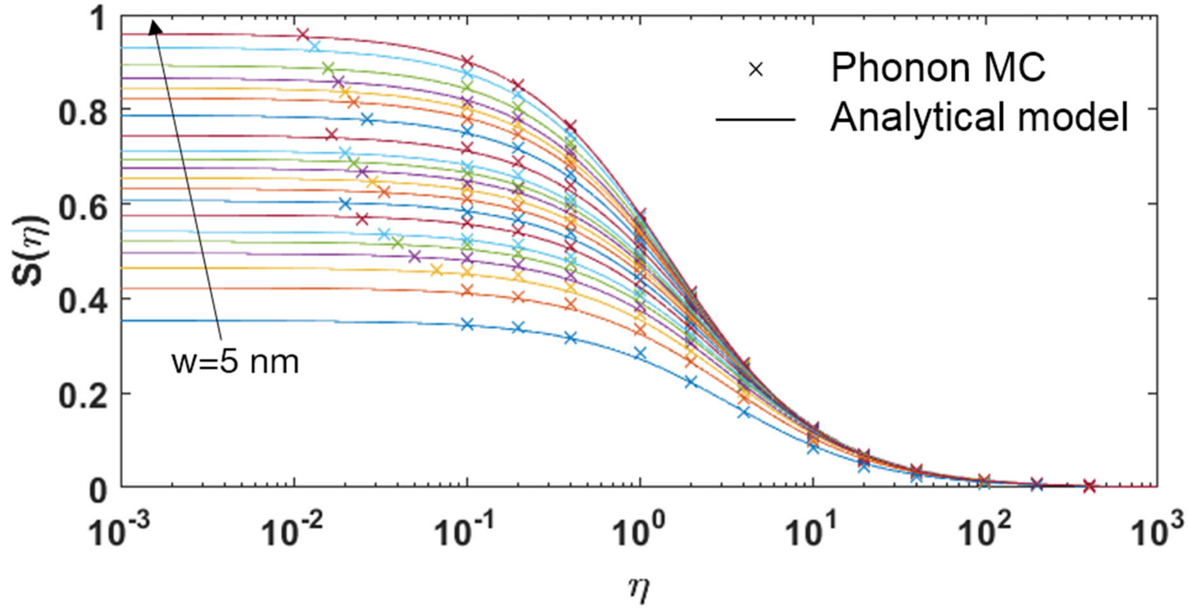


Figure III-3. S(η) for a 2D material or a quasi-2D thin film with one row of patterned nanoslots in its middle. The film length l=1 µm, nanoslot pitch p=500 nm, and depth b=5 nm are fixed. From the bottom to top curves, the neck width w= 5, 10, 15, 20, 25, 30, 40, 50, 60, 70, 80, 90, 100, 120, 150, 180, 200, 220, 250, 300 and 350 nm, respectively. The lines are predicted with L_c given in Equation (III-2).

Figure III-4 further compares L_C directly fitted in Figure III-3 based on Equation (III-1) and predicted by Equation (III-2). The divergence is within 5% for most w values.

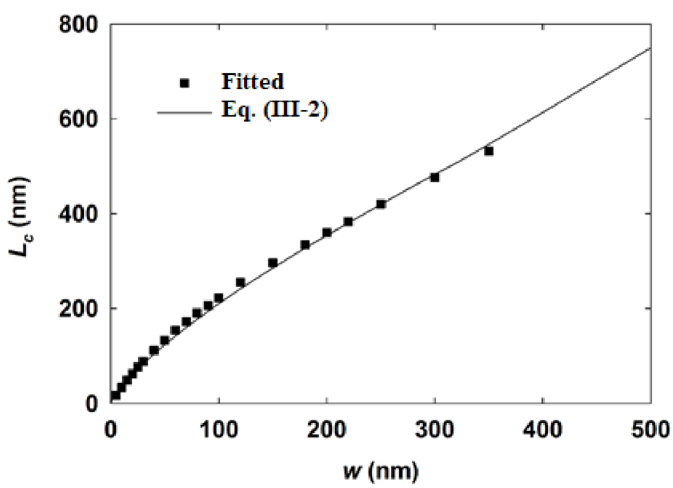


Figure III-4. Comparison between derived and fitted L_c.

When diffusive phonon scattering exists on film surfaces, the effective in-plane phonon MFP (Λ_{eff}) can be computed by modifying the bulk phonon MFP with the specularity of phonon reflection and the film thickness, known as the Fuchs-Sondheimer model [79]. With the computed in-plane spectral lattice thermal conductivity $k_L(\Lambda_{eff})$ for a solid thin film, the lattice thermal conductivity can now be computed as $k_L = \int_0^\infty \mathrm{S}(\eta) k_L(\Lambda_{eff}) \mathrm{d}\Lambda_{eff}$, where $\mathrm{S}(\eta)$ is unchanged from that for 2D materials.

III.B Probing ballistic thermal resistance introduced by nanoslots

Figure III-5 shows a fabricated T-junction device, in which a single neck was patterned with EBL in the middle of the short beam (inset). The nanofabrication was largely similar to the device in Section II.G. The metal-line-covered long beam was 100 μm long. The gap w between two nanoslots was roughly 130 nm. The device was fabricated from the device layer of a SOI wafer and the top Si film was 70 nm thick. A 30-nm-thick SiN_x layer was coated onto the device for electrical insulation, prior to depositing the metallic heater/thermometer line. The device was suspended by etching off the underlying SiO_2 layer.

In thermal measurements, the thermal resistance of a nanoslot-patterned short beam are currently measured at 30–400 K. After all measurements are completed, the short beam will be cut with a FIB for the self-heating test of the long beam, as the reference case (see Section II.G). The contribution from the SiN_x layer will be estimated and subtracted from the short-beam thermal conductance using reported k values for SiN_x coatings [80]. Such measurements will be repeated for other samples with different neck widths. A journal paper is under preparation for this work.

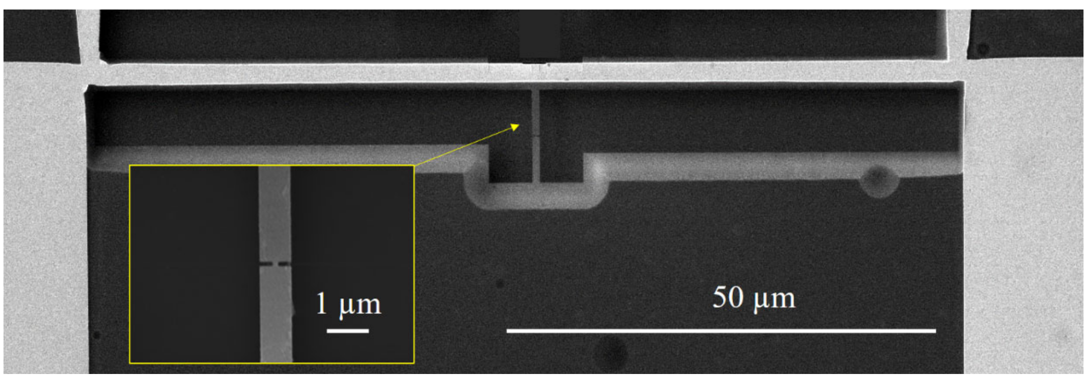


Figure III-5. SEM image of a T-junction device, with the inset showing the detail of the short beam with a single neck in the middle.

VI. Summary

In summary, we have advanced the electrical studies of GALs and further applied the knowledge to other 2D materials such as tellurene. The energy sensitivity to scattering is extracted and used to justify the major scattering mechanism of charge carriers. For thermal studies, valuable insights can be gained from comparable nanoporous films. Beyond antidot lattices, the nanoslot pattern is also explored as another approach to tune the thermoelectric properties of general 2D materials and thin films. A better understanding of such structures can enhance the existing understanding of transport processes within a nanostructure, particularly for the "ballistic thermal resistance."

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