URANIUM DIOXIDE ACTINIDE DETECTION DEVICE INTERFACE DESIGN FOR SPACE APPLICATIONS

THESIS

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AFIT-ENG-MS-19-M-050

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Abstract

Attention concerning the proliferation of nuclear weapons and materials has generated many research initiatives to detect, identify, and locate radiation emitted by actinides. In support of this effort, the 'Fission Induced Neutron Detection of Nuclear Materials' (FIND'NM) program was established to comprise a joint effort to explore this issue. The objective also co-extends the Air Force Research Laboratory uranium doxide (UO_2) detection sample growth, characterization, and electrical interface research. AFIT's study accomplishes the design and fabrication of a space-tolerant PCB to support a UO_2-based neutron detector. Further design considerations are made with the expectation of the platform to be inside an in-orbit satellite. The PCB will interface a satellite, which in turn will relay transferred data to researchers on the ground for later processing.

The scope of the research is to provide a low-cost commercial-off-the-shelf solution with signal integrity and operational stability in mind. The study performed by LTC Dugan [16] and Lt Col Young [44] provided the basis from which the project stems. These circuit behavioral characteristics narrowed the components considered to accommodate the low-amplitude and fast-pulse output required from a device. Three distinct amplifier designs were required due to changes in the accepted theoretical electrical characteristics of the sensor.

By circuit simulation, the three presented amplifier systems demonstrate the desired output for each sensor model, within a particular envelope of operation. The system can capture, collate, and disseminate data generated while operating within specified parameters.

The completed and operational PCB presents a proof-of-concept that Space com-

pliance devices can be made more cost-efficient by utilizing design aspects already included in larger system designs. The flexibility of the FPGA signal processing system can be used to try multiple operating configurations, ultimately resulting in an ASIC to further reduce the cost given large scale deployment of a unique design. Small detection devices like this could be installed on most orbital satellites and transmit data about areas of interest where actinide particle activity is detected.

Acknowledgements

I dedicate this thesis to my Air Force family, friends, and loved ones. To my spouse, for all the sleepless nights, thesis revisions, and cups of coffee; I could not have accomplished any of this without your unwavering support and encouragement thought this year. Thank you, my love. To my mother and father, for the faith and love you have in me. You knew I could do this, with all my heart, thank you.

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And finally, to my MEMS and VLSI friends: you offered help without asking, pushed without complaint and gave it everything you had. You made this unforgettable, and I hope our paths cross over and over in the future.

Cheers to you all,

Jennifer N. Ramos

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List of Abbreviations

Abbreviation		Page
B	boron	1
HgI_2	mercury diiodide	1
U	uranium	1
Th	thorium	1
FIND'NM	Fission Induced Neutron Detection of Nuclear Materials	1
AFRL	Air Force Research Laboratory	1
AFIT	Air Force Institute of Technology	2
CSRA	Center for Space Research and Assurance	2
UO_2	uranium dioxide	2
PCB	printed circuit board	2
LEO	Low-Earth-Orbit	2
Si	silicon	6
Ge	germanium	6
GaAs	gallium arsenide	6
CMOS	complementary metal-oxide-semiconductor	6
IV	Current-Voltage	9
JFET	Junction Field-Effect Transistor	10
PIN	p-type Intrinsic n-type	12
OPAMP	Operational Amplifier	15
TIA	Transimpedance Amplifier	15
ADC	Analog-to-Digital Converter	18
FPGA	Field-Programmable Gate Array	20

Abbreviation		Page
IC	integrated circuit	20
ASIC	Application-Specific Integrated Circuit	20
SEE	Single-Event-Effects	20
DC	direct current	20
MEO	Medium Earth Orbit	21
COTS	commercial off-the-shelf	22
Sv	Sievert	23
O	Oxygen	26
NASA	National Aeronautics and Space Administration	28
ICD	Interface Control Document	30
R	resistor	38
C	capacitor	38
CNVST	Conversion time	42
SoC	System-on-a-Chip	43
SPI	Serial Peripheral Interface	44
UART	Universal Asynchronous Receiver-Transmitter	44
LDO	low dropout	45
SDK	Software Development Kit	47
VHSIC	Very High Speed Integrated Circuit	47
VHDL	VHSIC Hardware Description Language	47
BOM	bill of materials	51
TVAC	Thermal-Vacuum	53
D-D	deuterium-deuterium	55
OSU	Ohio State University	55

Abbreviation		Page
LEU	Low-enriched uranium	55
LED	Light Emitting Diode	67
ESD	electrostatic discharge	80
SMT	surface mount technology	96

URANIUM DIOXIDE ACTINIDE DETECTION DEVICE INTERFACE DESIGN FOR SPACE APPLICATIONS

I. Introduction

Due to the growing concern for the proliferation of nuclear weapons and materials, actinide detectors have generated significant attention. To impede proliferation, research has been instituted to determine if actinide detectors could be created from alternate materials. These materials can range from boron (B) and mercury diiodide (HgI_2), to more nuclear reactive elements such as uranium (U) and thorium (Th) [8]. Emerging detectors have the potential to be smaller and more widely utilized within different environments [36]. These new detectors can conceivably be placed in more covert locations while utilizing arrays of detectors to determine range, strength or direction of a radiation source [13].

Fission Induced Neutron Detection of Nuclear Materials (FIND'NM) is a parallel effort program to design a functional payload interface circuit design, a neutron detecting crystal formation, and a reliable interface for the resulting crystal (including contact adhesion and characteristic envelope of the samples). This thesis covers design, fabrication and testing of the circuit design based on characteristic assumptions in support of this effort.

The intent of this research is a proof-of-concept to fabricate and test a device design that will interface a neutron-detecting device/crystal, supplied by the Air Force Research Laboratory (AFRL). This system will comply with CubeSat and military standards for manufacturing as well as survive environmental testing required for space flight hardware. The device will be designed with variability in mind and can

be further modified to accommodate differing radiation detector sample versions.

Through mutual interest, the Air Force Institute of Technology (AFIT) Physics, AFIT Electrical Engineering, and Center for Space Research and Assurance (CSRA) departments have partnered with AFRL in the pursuit of furthering the field of radiation detection. While the exact specifications of the samples can only be theorized at the time of writing, this design will offer solutions for an interface device that can encompass three operating assumptions based on the detector behavior throughout the project: a transistor, a diode, or a resistor.

1.1 Research Objectives

The focus of this research is to address the interface challenge between a theoretical radiation detector made of a hydro-thermally grown crystal sample of uranium dioxide (UO_2) and the host satellite. This research explores the following questions:

1. Can a low-cost printed circuit board (PCB), constrained by space tolerance and CubeSat standard, be designed to support an experimental uranium dioxide thermal-neutron detector?

2. Will the PCB subsystem work together to capture and transmit data back to the user?

3. Will the PCB survive operating environmental conditions (mimicking Low-Earth-Orbit (LEO)) and how will these conditions affect the functional circuitry?

1.2 Thesis Overview

This thesis will cover the design, fabrication, and testing of hardware to support differing versions of UO_2 samples (provided by AFRL) that would theoretically detect

thermal neutrons. The device will ultimately become a deliverable payload for flight testing in April of 2019. This thesis is broken into the following chapters:

Chapter II will encompass relevant concepts behind a theoretical radiation detector and what considerations drive later component decisions in the hardware design. Chapter III is the methodology section detailing the components used, the design of the hardware subsystems and the testing proposed for device functionality in a space environment. Chapter IV will detail the results of all testing on each board and their resulting design change requirements. Chapter V will give conclusions, final design payload, and recommendations for future work to be accomplished.

II. Background

Uranium dioxide (UO_2) is a semiconducting material with a significant thermal neutron scattering cross-section. Although UO_2 has been subject to extensive thermal and electrical studies due to its use as a nuclear fuel [22], its use as a radiation detection medium is a novel concept. This research effort focuses on a PCB device to interface this dual function material. The following conceptual foundation will be separated into three areas of interest:

- UO_2 detection understanding
- Components and subsystems of an an interfacing PCB
- Operational environment and inherent hazards

2.1 Radiation Detection

There are two major types of radiation detectors: reactive detectors (e.g. Geiger tube detectors, neutron bubble dosimeter) and solid-state detectors. Some gas reactive detectors consist of a conducting cylinder with a wire along its axis filled with an insulating gas such that a voltage applied between the cylinder and wire produces almost no current. Ionizing radiation passing through the tube will produce free ion pairs that are attracted to the wire and cylinder, forming a current that is detected. Others, such as scintillators, convert radiation energy into light and rely on photomultipliers to generate an output current. These detectors are useful in producing a prompt output that reveals the existence and relative intensity of ionizing radiation.

A solid state radiation detector is composed of two sections: the detector material and the electrical interface. The detector material, which converts radiation into conduction electrons or free charged particles, is composed of a radiation reactive

agent [8]. Note that this research is interested in actinide particles, which are any of the fifteen metallic elements from Actinium (atomic number 89) to Lawrencium (atomic number 103) in the periodic table [3]. Each of these elements have radioactive isotopes with uranium being the element of interest here because it has a fairly large probability for fissioning (fission cross-section) by a neutron [3].

There are many materials (isotopes) that have high interaction cross sections with neutrons. However, for detection, the interaction probability (cross section), final products of the interaction (e.g. electrons or charges particles) and their energy that make the desirable (or not) as a radiation detector. The electrical interface portion is designed to convert the charged particles products from the interaction in the detector material into an electrical signal since radiation neutrons do not create conduction electrons directly [8]. Two sub-classes of solid-state detectors are identified: indirect-conversion (e.g. thin-film-coated detectors or conversion layer detectors) and direct-conversion (e.g. solid form or homogeneous detectors) [11]. Thin-film-coated detectors are created using a reactive material coated Si-semiconductor like that stated in research conducted by Litovchenko et al. [26]. Litovchenko experimented with ^{235}U mounted to an Al-substrate and attached to a Si surface barrier detector to achieve thermal and epithermal neutron detection [26]. This research will primarily focus on solid-state detectors since they are an efficient way to take advantage of uranium, its high neutron cross section and high energy output via fission, utilizing the quality UO_2 samples theorized for this research.

Uranium was shown to be a reasonable detection medium upon a Si-base, the next progression is to utilize the semiconductive properties of UO_2 to make a homogeneous device. The UO_2 sample utilized in this project and present in research by Lt Col Young [44] and LTC Dugan [16], shows much promise as an electronic material as well.

For current solid-state devices incorporating uranium, detection is through fission of an atom following neutron capture. The kinetic energy deposition of the ionized daughter fragments translate through the semiconducting material result in electron-hole pairs. This generation of electron hole pairs in the presence of an electric field (p-n junction) giving a brief electrical pulse that can be seen at the device terminals.

In theory, for UO_2, the kinetic energy of the fission fragments offers the greatest opportunity to convert a neutron interaction to an electronic signal (200 MeV), even though other materials like boron have larger interaction cross-sections but only releases 2.5 MeV in the daughter products (alpha and ionized lithium). A downside to the large release of energy by fission is that fragmentation and translation of the daughter fragments does irreparable damage the lattice structure of the solid-state detector. However, the amount of damage is a very small fraction of the device (only in the ion tracks). The damage caused by these interactions results in displacements, which can persist for long periods and eventually reduce electronic performance. It should not be confused with other radiation damage, (i.e. ionizing radiation) which would add additional noise to the signal. Damaging radiation will be discussed later in this chapter.

2.2 Uranium Dioxide (UO_2) Detector

According to a paper by Thomas Meek [28], uranium oxides have intrinsic electrical and electronic properties similar to those intrinsic properties of semiconductor materials such as silicon (Si), germanium (Ge), and gallium arsenide (GaAs) [40]. The dielectric constant of UO_2 is 22 at room temperature while Si and Ge are at 12 and 14, respectively [28]. This characteristic may make uranium oxides suitable for creating higher density integrated circuits with higher breakdown voltages than current silicon-based electronics, without suffering complementary metal-oxide-semiconductor (CMOS)

tunneling breakdown due to smaller nanometer size features [28]. These characteristics make UO_2 a viable material for creating a new type of conductive junction [28]. In addition to the promising behavior of a semiconductor, UO_2 also shows potential as a material for neutron detection because of the high energy output from fission [11]. Uranium oxides may also be more resistant to displacement radiation damage, due to the high atomic mass of uranium, making them more desirable for space survivability [11, 28].

2.2.1 Hydro-thermally Grown UO_2 Samples.

Attention must be given to the physical device characteristics. This includes how the device is created, and the parallels that can be utilized in their place. These sample devices provided by Dr. Mann, AFRL Growth Specialist, are created by employing a hydrothermal growth process. In this case, a hydrothermal process refers to the process of mineral formation under similar conditions as found within the earth [10, 44].

The entire operation is explained in a dissertation "Evaluation of Hydrothermally Synthesized Uranium Dioxide for Novel Semiconductor Applications" written by Lt Col Young (2016). Young also details how the internal aqueous solution of working fluid, growth nutrient, and mineralizer are used to create the sample crystal structure though the use of a Bridgeman autoclave as depicted in Figure 1.

To understand how the samples are grown, the Bridgeman autoclave system is broken down into two major zones: a dissolution zone and crystal-growth zone [44]. The temperature differentiation in each zone forces the aqueous solution, which fills the entire autoclave, to transport dissolved nutrient from the warmer dissolution zone to the cooler growth zone in a turbulent, convective flow [43]. Once in the growth zone, the nutrient may deposit on a dangling seed crystal (transport growth reaction)

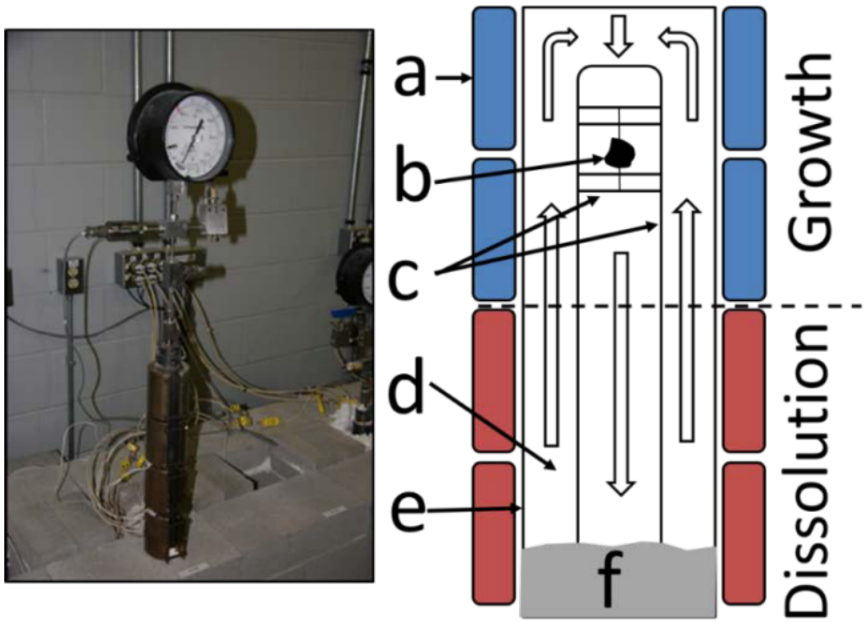


Figure 1: (Left) Image of the Bridgeman autoclave system with growth chamber, heater bands and pressure gauge. (Right) Ampoule diagram depicting the following areas: (a) heating elements for temperature regulation, (b) suspended seed crystal, (c) wire support structure to hold crystal within growth zone, (d) mineralizer solution convection zone which transports dissolved nutrient to growth zone, (e) Autoclave ampoule housing tube, (f) feedstock or nutrient that is kept warmer than the rest of the tube to dissolve and flow up to growth zone. [44]

or coat the walls of the chamber (a heterogeneous nucleation reaction) [44]. Growth time and temperature variations are crucial to growing a p-type UO_2 layer or n-type UO_2 layer on the seed crystal, though specifics are currently being researched [44].

Once the growth process is concluded, the resulting sample is a geode-like structure with the seed crystal nested inside the reactive agents. The samples are then processed by cutting the crystal in half, revealing the intrinsic seed crystal and supporting silver wire. Theoretically, this would give access to the hidden n-type UO_2 layer as well as the possible contact wires through the intrinsic material. However, this is a desired theoretical design and has yet to be proven functional or accurate. An example of a possible cross section of a fully grown and cut UO_2 sample can be seen in Figure 2.

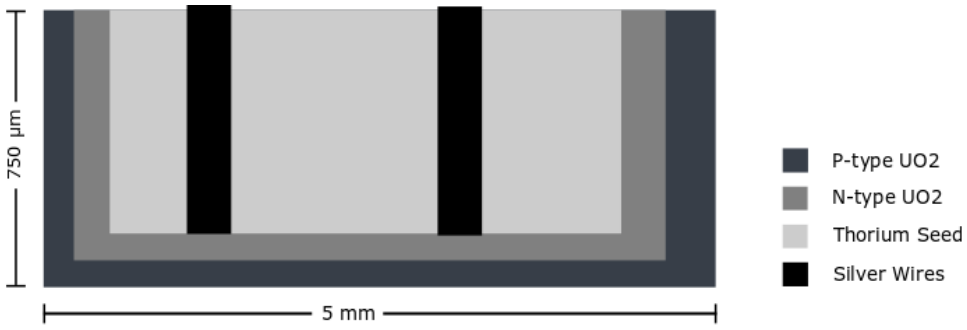


Figure 2: Diagram of Radiation detection sample cross-section the hardware system is theoretically designed around. This sample is composed of a Thoria Layer in the center as an intrinsic seed layer, with n-type and p-type UO_2 grown around. This is the conceptual sample after processing at the Air Force Research Lab.

Once the crystals are grown, preliminary research is conducted into creating a characteristic envelope of the operational outputs of each sample. This includes research to interface the resultant device (e.g contact adherence study, Current-Voltage (IV) characteristics of the material, structural package protection) which will not be covered in this investigation. Some of the packaged samples can be see in Figure 3. This parallel effort will use developing assumptions based on preliminary behavior of

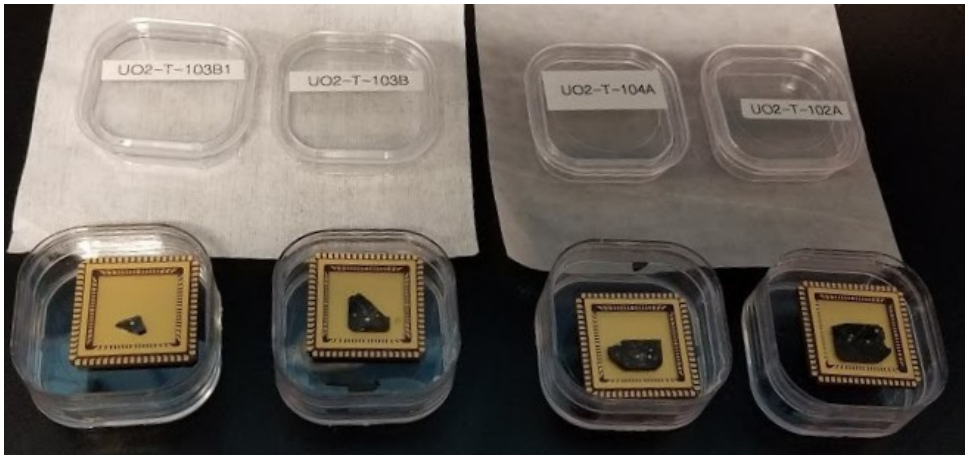


Figure 3: Photo of four Hydro-thermally grown Uranium Dioxide detection samples in surface-mount chip carriers.

previous samples.

2.2.2 Equivalent component comparison.

To develop the payload system in parallel with the sample, a stand-in system was put into place. After preliminary testing by LTC Dugan [16], there are three prevailing theories on what type of device the sample will mimic or simulate: a transistor, a photo-diode, or a photo-resistor. For competency, these sections will focus only on general functionality of each equivalent device.

2.2.2.1 Junction Field-Effect Transistor.

A Junction Field-Effect Transistor (JFET) model is composed of three components: a source, a gate and a drain, as depicted in Figure 4. A JFET has a narrow piece of high-resistivity semiconductor material forming a 'channel' of either n-type or p-type silicon for the majority carriers to flow through [31, 29]. To interface this channel, two ohmic electrical connections are formed at either end (drain and the source) [31]. A JFET requires the gate to generate a depletion region, which can adversely affect this

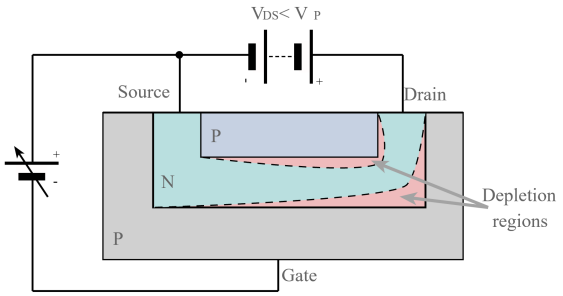


Figure 4: A diagram of Junction Field Effect Transistor showing layers of P-N-P type and depletion region when the gate is being activated.

flow, resulting in a change in output from the device [14, 31]. Should a UO_2 sample device be able to be constructed as a transistor, the detected radiation particles would cause the device channel to alter the current flow, thus creating a pulse detectable above the background radiation floor.

2.2.2.2 Photo-diode.

A diode is composed of positively doped (p-type) and negatively doped (n-type) regions pressed against one another. The interface layer is known as the depletion region, an area depleted of the majority carriers. Holes in the p-type layer and electrons in the n-type layer combine in equal numbers along the diode. This leaves the ionized atoms (also known as space charge since they do not move) of each region behind, creating an electric field across the depletion region. This electric field will act upon any charges that enter the depletion region, guiding them to the n or p region depending on their charge. As a voltage acts upon the diode these carriers conduct electrical flow [37]. The p- and n- regions are associated with an anode and cathode reference pins for functionality and are direction specific [12, 37]. If the photodiode is reverse-biased, the depletion region is maximized as well as the electric field [38].This is the typical state of a photodiode as it maximizes the response by increasing the

volume and the separation of conduction electrons and holes. Note that a diode is said to be reverse-biased when the cathode is made more positive than the anode [39]. In a photodiode, this reverse current (known as the dark current) flows in the absence of illumination and contributes to noise [37], but has currents that are typically fairly low (10's of fempt-amps for quality diodes). This sets a noise floor for detection. When light particles are absorbed in the photodiode they create electron-hole pairs and the electric field across the depletion region separates them inducing an electrical current to flow. In the case of a PIN diode, an intrinsic layer resides between the p-type and n-type regions [39, 38, 37]. The intrinsic layer is a large depletion region, and can be tailored to optimize the frequency response of specific light [38]. The operation of the PIN diode is shown in Figure 5 [38]. The operation of a photodiode is similar, except the detection regions is substantially smaller.

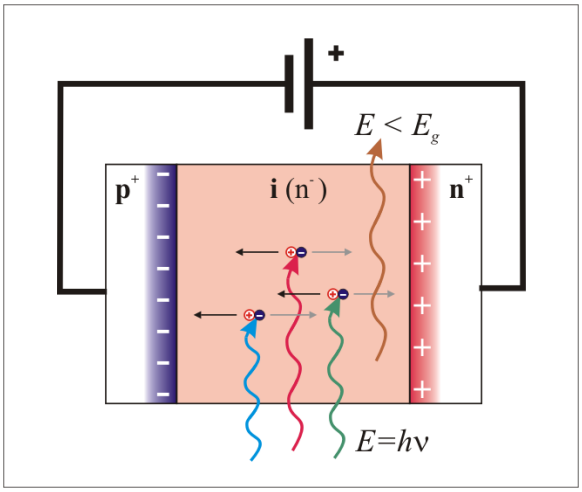


Figure 5: Internal operation of a p-type Intrinsic n-type (PIN) photodiode

When light energy (E), which can be defined as

$$E = h\nu \tag{1}$$

where h is Planck's constant and ν is the frequency of light (Hz), is smaller than the band-gap energy, E_g, of the detector, light passes without exciting the particles into the conduction band [38] [12]. An equivalent circuit is utilized in simulation and can be seen in Figure 6 [9].

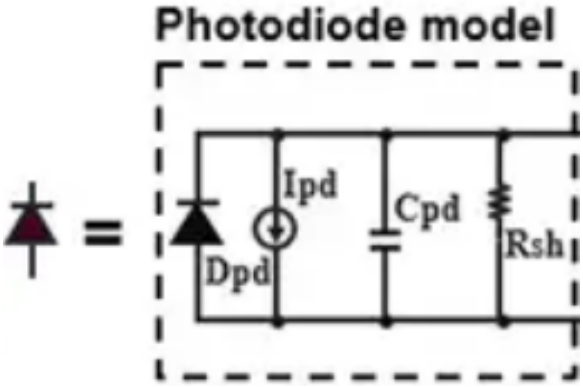


Figure 6: An equivalent circuit for a photodiode to be utilized for simulation. (Image source: Digi-Key Electronics)

A photodiode can be broken down into its basic 4 components, a diode (Dpd), a current source (Ipd), a capacitance (Cpd) and a resistance (Rpd) associated with it [9]. These values are unique to the type of photodiode and can be attained using the data-sheet for simulation. If a diode structure can be synthesized utilizing UO_2 as the semiconducting material (homojunction), it could theoretically function in much the same way.

2.2.2.3 Photo-resistor.

A photo-resistor device is composed of a single resitive material that behaves much like the PIN diode intrinsic layer [38]. A unique characteristic of a photo-resistor is that it behaves like a standard resistor until light is absorbed in it, creating electron hole pairs [37]. Due to carrier generation resultant from the incident light, the resistance of

the device is reduced, sometimes by several orders of magnitude, for example, going from a value of 1MΩ to 1kΩ depending on the light intensity [12]. A conceptual model of a photoresistor can be seen in Figure 7 [21]. This model is useful if the UO_2 p-type or n-type crystal oxidizes or homogenizes the crystal completely, giving no characteristic diode rectification. At the conclusion of this research, this was the most prevailing methods for device functionality, though it was not explored with the proof-of-concept of the interface board.

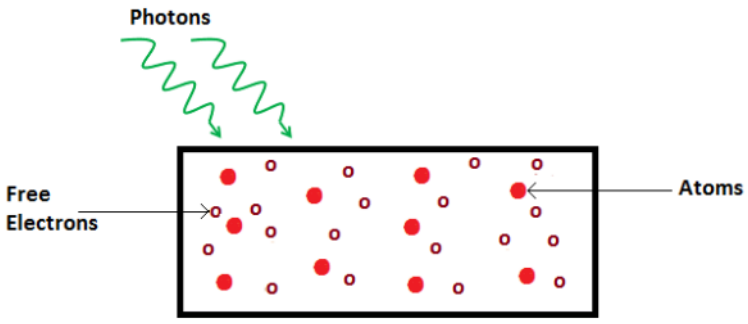


Figure 7: Example of the operation of a photoresistor. Light particles interact with the material of the resistor allowing electrons to pass more freely through the resisting material.

2.3 Interface considerations

To attain information from a detector following a radiation absorption event the signal must be passed to multiple sub-systems to capture, digitize, process, and transmit the data to be analyzed. This can be broken into three major sub-systems:

- Signal Capture
- Signal Processing

- Power Distribution

2.3.1 Signal Capture.

Once a signal is generated from the sample, a subsystem is necessary to capture and digitize the input for processing. Based on the assumed device characteristics detailed in Section 2.2.2, the output of the device will be an analog signal of some current (likely in the mA range) over some very short pulse width. An amplification circuit is introduced to assist the signal processing sub-system with capturing any output produced by the detection media. For this application, an Operational Amplifier (OPAMP) and Transimpedance Amplifier (TIA) are used to amplify the source signal. The OPAMP is an IC that is used to increase a very small voltage to a higher voltage, while a TIA utilizes OPAMPs to convert a very small current into a voltage of higher magnitude [30]. An operational amplifier has an internal circuit structure that can be used to calculate the amount of amplification to be produced. This equivalent schematic can be seen in Figure 8.

By using the analysis presented in 'Electric Circuits' by Dr. James Nilsson and Ms. Susan Riedel [30], V_{out} is calculated using the following equation:

$$V_{out} = \frac{-A + (R_o/R_f)}{\frac{R_s}{R_f}\left(1 + A + \frac{R_o}{R_i}\right) + \left(\frac{R_s}{R_i} + 1\right) + \frac{R_o}{R_f}}(v_s) \tag{2}$$

We see from the Equation (2) that A is the gain from the amplifier and v_S is the source voltage applied. R_i is the input resistance over the input terminals, R_o is the finite output resistance inside of the OPAMP, while R_f and R_s are the external feedback and source resistances, respectively.

While an Operational amplifier utilizes v_s as an input voltage, a TIA only requires

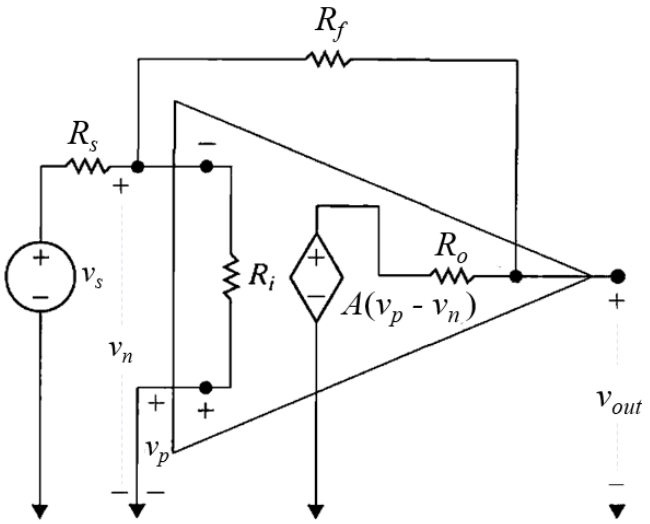


Figure 8: A realistic model of an inverting-amplifier circuit where v_p and v_n are the input voltages across the positive and negative terminal, respectively. [30]

the source current, i_s. This configuration is calculated by utilizing Ohm's Law which expresses voltage as a function of the current [30], which can be rewritten such that

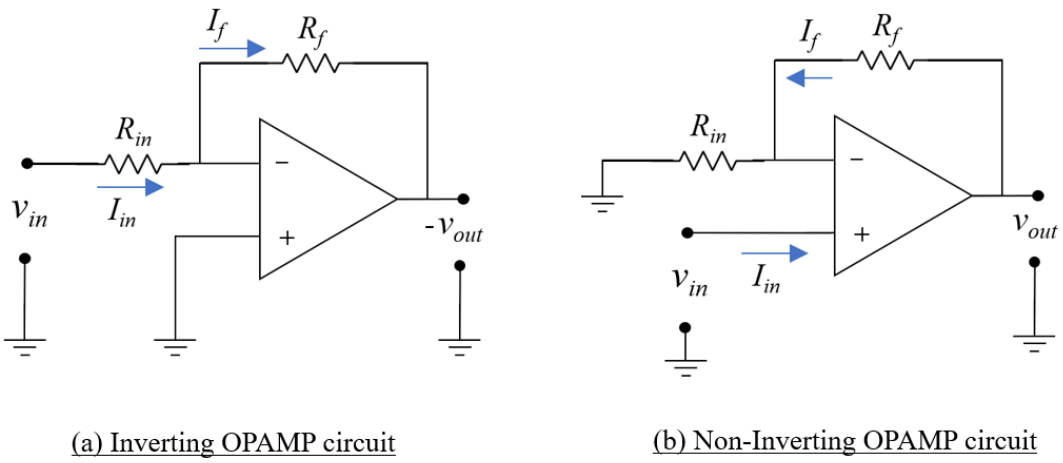
$$v_s = i_s \cdot R_s \tag{3}$$

By replacing the voltage with the equivalent current equation from eq. (3) into eq. 2 the output voltage from a TIA reduces to the following:

$$V_{out} = \frac{A \cdot R_f - (R_o \cdot R_s)}{-R_o + R_f(-1 + R_s(R_i \cdot A + R_o + 2R_i} (i_s) \tag{4}$$

These values are attained by using the data-sheets provided along-side the components chosen, often times calculated for the users. Since this is the case for most of the amplifiers implemented in this research, the equations can be simplified to their

base components: A, R_f, R_{in}, v_{in}, and v_{out}. The configuration of these equations now depend upon their intended purpose. For this research, the main implementation for the operational amplifiers is an inverting and non-inverting amplification configuration as illustrated in Figure 9.



(a) Inverting OPAMP circuit

(b) Non-Inverting OPAMP circuit

Figure 9: A depiction of an inverting (a) and non-inverting (b) amplifier circuit configuration.

If the operational amplifier is used as an inverting circuit configuration, the equations reduce to:

$$A = \frac{v_{out}}{v_{in}} = -\frac{R_f}{R_{in}} \tag{5}$$

In a non-inverting amplification circuit, a simplified form is

$$A = \frac{v_{out}}{v_{in}} = 1 + \frac{R_f}{R_{in}} \tag{6}$$

By swapping a resistance element to a reactive element, the functionality of the OPAMP can change to become another type of operand (e.g differential amplifier or

integral amplifier).

Once a signal is amplified, it can be accompanied by high frequency amplified noise, or jitter, within the traces. To alleviate this jitter, many of the signals are forced through a low pass filter capacitor. A capacitor's complex reactance (X_c) is given by:

$$X_c = \frac{1}{j\omega C}\Omega \tag{7}$$

where ω is the frequency, and C the capacitance and $j = \sqrt{-1}$ [30]. For a low-frequency signal, impedance will be relatively high and will not effect the signal passing to the Analog-to-Digital Converter (ADC). Conversely, for a high frequency signal, the impedance will be quite low and the signal will travel through it straight to ground [30]. The "Low-pass filter" name points to the allowance of low frequency signals to pass by the capacitor unaffected.

The resulting voltage signal after passing through the filters is then passed to an ADC to convert the analog voltage into usable data for the signal processing sub-system. An IC (such as the LTC2389) is used to take an input voltage sample, assign a value to it based on a reference signal, then output as a set of binary numbers. There are two stages to an ADC, the sampling stage and the quantizing stage [37]. In the sampling stage, the input signal is read and held by a buffering capacitor until the next read interval is triggered by some input interval τ. The input signal is compared to a reference voltage in the ADC, which then assigns a value to the output signal [37]. An example of the sampling conversion is provided in Figure 10. Once the signal is sampled and converted to a voltage within a usable range (specific to the ADC), the quantizing stage assigns a numerical value to the sampled voltage [37]. This numerical value falls within a set output, often 2^n bits, depending on the type of ADC. This

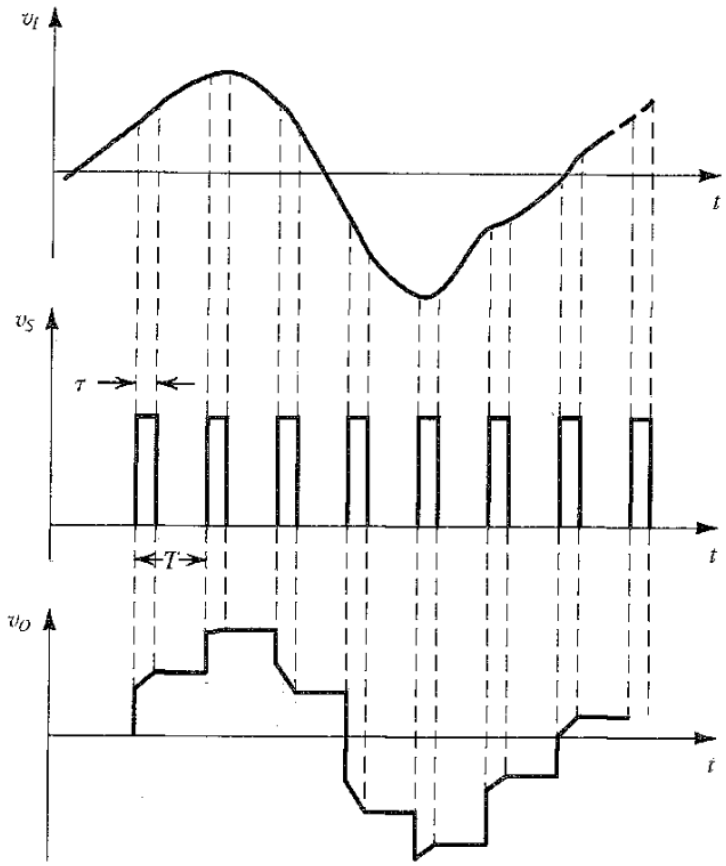


Figure 10: An example of the Sampling stage of the ADC. v_I shows the raw input signal, v_s is the sampling signal against the control voltage over some interval τ. v_o is the output signal to be fed to the converter and quantized into a binary word. [37]

digitized signal consists of binary code, which is a set of 0s and 1s that can be utilized by a processor.

2.3.2 Signal Processing/Transmission.

To interface the signal capture sub-system and the transmitting Satellite system, a Field-Programmable Gate Array (FPGA) processor is utilized. An FPGA is an integrated circuit (IC) chip that is capable of being programmed after manufacturing. An FPGA chip was selected based on processing and memory capability to support an incoming signal from the sample equivalent explained in section 2.2.2. Due to the lack of knowledge regarding the actual behavior of the UO_2 device, an FPGA was an obvious choice because of its flexibility in capturing the incoming data. Once the system is proved out using an FPGA, an Application-Specific Integrated Circuit (ASIC) can be implemented and widely produced to accommodate the detector requirements. The chip will need to be robust and will likely require reprogramming due to Single-Event-Effects (SEE) due to the space environment. SEE is the result of space radiation disrupting the transistor logic or memory on a chip and can be intermittent or permanent, depending upon the location and type of damage [39]. These events cause corruption in data and programming and will have to be considered when designing a supporting device [39].

2.3.3 Power Distribution system.

To ensure the power is properly distributed to several critical voltage lines required by the other subsystems to function, the board will utilize direct current (DC) to DC voltage converters. A voltage converter is a circuit that takes a source voltage level and converts it to another [17], for example, taking a 12V input voltage and converting it to a stable 5V output. Electronic voltage regulators utilize solid-state

semiconductor devices to smooth out variations in the flow of current. In most cases, they operate as variable resistors; that is, resistance decreases when the electrical load is heavy and increases when the load is lighter.

2.4 Operating Environment

To better define the design specification, the program FIND'NM collaborators specified the use of an actinide detection system utilization in a space environment. To ensure reasonable utilization of the detection sample and proper testing scope for a resultant device the device requirements limited the survivability to Low-Earth-Orbit.

Orbits can be broken down into three major areas: Low Earth Orbit, (LEO), Medium Earth Orbit (MEO), and High-Earth-Orbit. These orbits are depicted in Figure 11. LEO is an orbit around the earth located between 160 km (99 mi) and

Figure 11: Graphic representing the orbital bands around the earth. Primary area of interest is the LEO belt (white).

2,000km (1,200 mi) above the earth surface and has a period of approximately 84 to 127 minutes [1]. This orbit is the most valuable for experimentation as it allows for multiple passes over the same area for data collection. MEO is the region of space around Earth above LEO (altitude of 2,000 km (1,243 mi) above sea level) and below geostationary orbit (altitude of 35,786 km (22,236 mi) above sea level) [1]. Satellites in this region are commonly used for navigation, communication, and geodetic/space environment science [1]. MEO encompasses geosynchronous orbit, where satellites can stay in one place relative to the earth's surface without much drift [1]. High Earth orbit is a geocentric orbit with an altitude entirely above that of a geosynchronous orbit (35,786 kilometres (22,236 mi)) [1].

2.4.1 Environmental effects of LEO.

The LEO environment contains a number of hazards that range from radiation due to the sun's exposure to small debris hurtling at over 11,000 kilometers per hour (7000 mph) [1].

2.4.1.1 Radiation.

In true space interest, designing a low-cost, commercial off-the-shelf (COTS) space-effective hardware payload, the system must account for the damaging radiation affecting the system devices, power lines and interacting materials. This radiation can increase background noise and reduce electronic performance which will decrease the likelihood that a neutron will be detected correctly [35]. High energy space radiation has 2 components: an electronic component (interaction with atomic electrons), and a nuclear component (interaction with the nucleus). For this research, only atomic interactions are considered.

Radiation is the number one cause of failures for most electronics operating in

the LEO environment [34]. Radiation damage can be classified into two categories: ionizing and non-ionizing. Ionizing radiation damage is due to radiation stripping atomic electrons from atoms in a material that create electron-hole pairs as they travel. This added population of conduction electrons (and holes) can cause current disruptions in electronic circuits masking important signals, or if large enough, create permanent damage to the circuit elements resulting in malfunctions. Non-ionizing radiation damage is due to collisions between high-energy radiation particles and atoms in a material. This collision can displace an atom from its the lattice to another energetically favorable position, resulting in a Frenkel defect (an interstitial atom and a vacancy in a lattice site). This damage can result in reduced performance by reducing electron mobility, or creating recombination sites that reduce carrier lifetime. [32] In space both ionizing radiation and non-ionizing radiation damage often occur at the same time and can be from the same interaction, creating a complex time dependent response that can last from milliseconds to years. These interactions and some of the effects are shown in Figure 12 [32].

Differing types of radiation come from different sources, much of the charged particles within LEO is generated by the sun. These charged particles are carried by solar wind, which comes into contact with the Earth's magnetic field [27]. This magnetic field works to deflect most of the charged particles, but some become trapped in an area referred to as the Van Allen Radiation Belt. Figure 13 illustrates area of particle concentrations.

Charged particles, from sources like the sun, are attributed to many satellite failures such as the Telstar in 1962 and other commercial satellites [7]. The average exposure rate calculated in Sievert (Sv) (J/kg), a derived unit of ionizing radiation dose, among the LEO band is 2-16μSv/hr [42]. Another source of radiation is galactic cosmic rays generated outside of the solar system. These rays are primarily composed

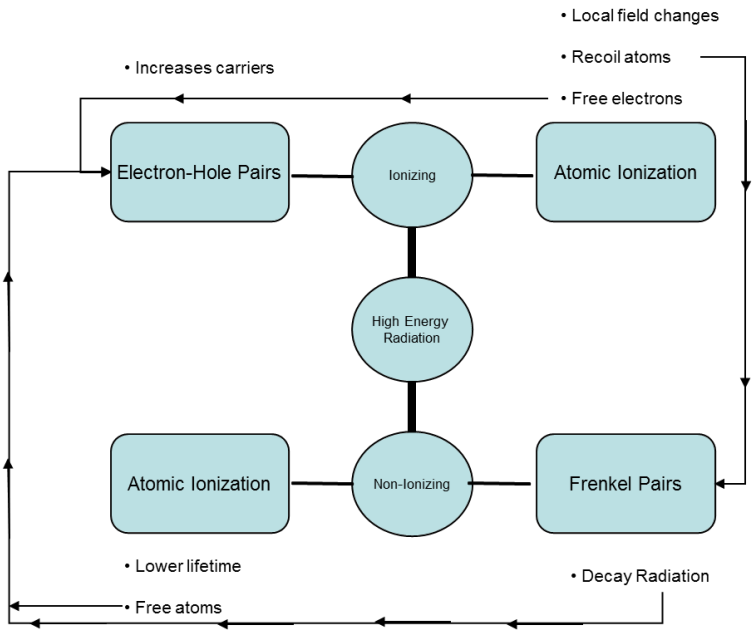


Figure 12: Interaction and effects of damaging radiation on electronics.

of protons, making up about 85%, alpha particles generating approximately 14% and the remaining 1% is composed of free elections and heavy ions [27]. Many of these lower energy particles are deflected by the Earth's magnetic field, but particles with high energy are able to penetrate the magnetic boundary [27] and tamper with satellite systems.

To protect against damaging radiation particles, satellites employ shielding for their electronics. According to research conducted by Luz Martines [27], protons and pure energy rays (e.g., Gamma rays) that make contact with bulk shielding lose energy per millimeter thickness of material. This is due to the interactions of the material's electrons and high impedance density. To stop a 1MeV particle from interacting and damaging the PCB, the shielding would have to be approximately 1cm thick Aluminum [27]. Any particle with an energy higher then that (e.g. 1-10 MeV) could be stopped by lead, due to it's high electron count and other material properties

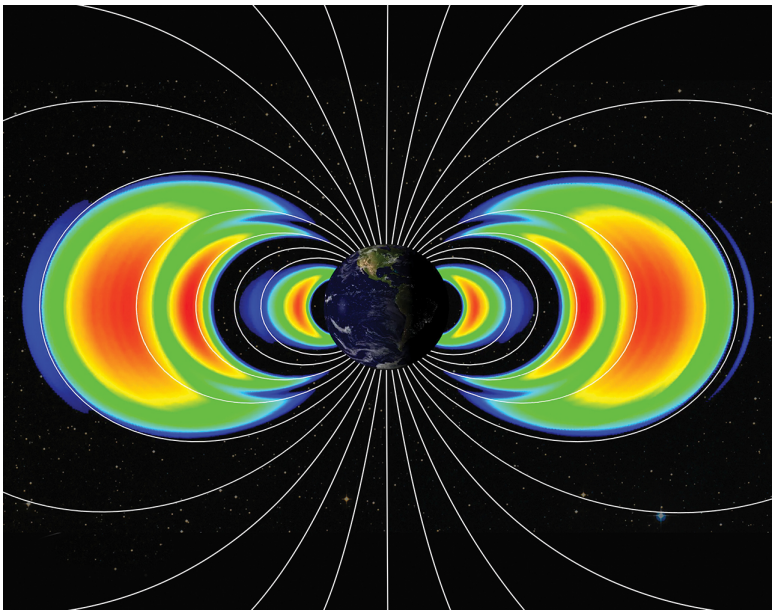


Figure 13: Image of the concentration of particles within the Van Allen Radiation Belt. Shortly after launch on Aug. 30, 2012, particle detection instruments aboard NASA's twin Van Allen Probes revealed to scientists the existence of a new, transient, third radiation belt around Earth. Credits: NASA's Goddard Space Flight Center/Johns Hopkins University, Applied Physics Laboratory

described in her research [27].

Neutrons, however, are not affected by the same electrical properties of shields as other radiation because they are neutral [26]. This means that even with shielding to thwart most radiation, the desired radiation, in this case neutrons, will still be able to penetrate and trigger the UO_2 sensor.

2.4.1.2 Chemical reactivity.

As the altitude increases, elements that cause reactions with other materials, namely Oxygen (O), become more prevalent. Oxygen on the earths surface is commonly in the form of O_2, and O_3 is known as ozone, but a single atom of O is known as atomic oxygen. Atomic oxygen doesn't exist naturally for very long on Earth's surface, as it is very reactive element [5]. However, in higher orbits, atomic oxygen can make up as much as 95.9% of the atmosphere, with nitrogen making up only 4.1%. Atomic oxygen is dependant on solar activity and increases as periods of sun spot activity rises. Collision with atomic oxygen, since satellite systems orbit earth are in constant motion around the sun, causes destruction of organic polymer bonds and a loss of material [5]. Metals, such as exposed copper or aluminum, become brittle and can give way to channeling, severing the connectivity of the traces. This loss due to oxidation, contribute to the working life and durability of materials as well as the protective coating surrounding critical components [5].

2.4.1.3 Temperature and Thermal cycling.

The thermal environment LEO poses is a substantial factor in space hardware design. Temperatures reached by sun-facing or space-facing surfaces may differ by a drastic amount, affecting electronic components as the system moves in and out of sunlight [18]. This causes thermal-cycling as the spacecraft orbits the earth, being

eclipsed from the sun's rays at least once every orbit [18]. Thermal cycling can cause issues such as heat transfer, material migration, and materials degradation [18].

Heat rejection is also a concern when dealing with high density components or high voltage traces. In absence of convection (due to a lack of air), most practical heat removal from space hardware is by conduction and radiation [18]. Heat transfer, for electrical hardware, is primarily handled by conduction utilizing large mounting areas or thermally conductive adhesives to leach away heat [18]. As metals repeatedly cycle through hot and cold temperatures, the constant expansion and contraction causes the material to fatigue and crack over time. In cases of extreme heat, some of the components may experience melting or combust resulting in broken components or traces.[6] In extreme cold, materials may delaminate from their original location or break due to material shrinkage [18].

2.4.1.4 Debris.

Orbital debris such as payloads, spent rockets stages, fragments of rockets and satellites, various hardware and ejecta litter LEO and pose a hazard to orbiting space systems. Among this debris are also meteoroids, small chunks of rock or iron, often the remnants of comet orbits or sporadic particles emitted by the asteroid belt [6]. According to NASA Glenn Research Center, micrometeoroid (microscopic particles) also pose a great risk to spacecraft, causing an impact crater 10x that of the the impacting particle [5]. Examples of micrometeroid impacts in bulk materials are shown in Figure 14.

These floating projectiles are a threat to spacecraft by causing structural damage, surface erosion from collisions with smaller objects, and surface effects that cause changes in thermal, electrical, and optical properties of the hardware on board [6].

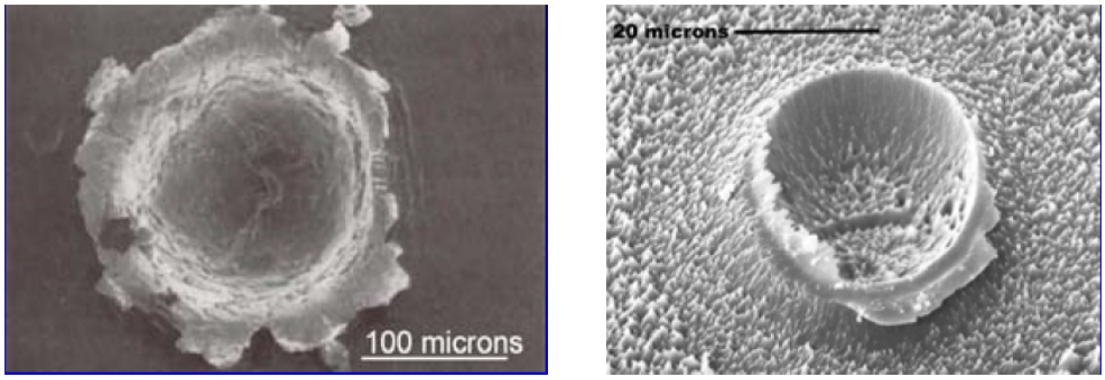


Figure 14: Impacts shown are in bulk materials, (a) Aluminum and (b) atomic oxygen textured Teflon. Images credit to NASA Glenn Research Center[5]

2.4.2 CubeSat Housing.

The CubeSat design standard was created by California Polytechnic State University San Luis Obispo and Stanford University's Space Systems Development Lab in 1999 [41]. Since then the standard has been adopted by hundreds of organizations worldwide including National Aeronautics and Space Administration (NASA) [41]. CubeSat developers include not only universities and educational institutions, but also private firms and government organizations [41].

Unlike other small satellites (weighing less than 300kg or 1,100lbs), a CubeSat must conform to a set of specific control factors which govern it's size, weight, and shape. CubeSats vary in size, but are all based on the standard CubeSat unit (i.e. 1U). A 1U CubeSat is a 10 cm x 10 cm x 11 cm cuboid with a mass of 1 to 1.33 kg [41]. Often, larger size CubeSat configurations are desired, and 2U, 3U and 6U sizes have grown in popularity [41]. An example of a 1U and 3U CubeSat configuration can be seen in Figure 15.

Figure 15: Example of a 1U (left) and 3U (right) CubeSat configuration for launch.

The CubeSat is the protective housing the PCBs utilize to survive the space environment. Though the chassis will provide some protection, testing is still accomplished to ensure an interfacing PCB does not fall prey to the internal conditions.

III. Methodology

Interfacing a theoretical UO_2 neutron detector and providing meaningful data for future research is a complicated situation with many areas of flexibility and trade-offs. The immediate goal of this research is to develop and deliver a payload PCB that is able to support three different input devices: a JFET, a photodiode, and a photoresistor. Each input type is considered a modification upon the original version (i.e., V1.0, V1.1, and V1.2) with similar operating component choices but different input assumptions. Implementation of lessons-learned from one version to subsequent versions may be integrated and documented as time permits. Due to the limited time and resources, a proof-of-concept will be the ultimate goal of this experiment. Before deployment, each sub-system must be tested for functionality in extreme environments.

3.1 Assumptions/Limitations

The PCB must be produced using available resources, interface specifications, and accommodate a still-theoretical thermal neutron sensor, of which has undefined device characteristics. To that end, understanding the available design constraints decreases the endless component choices which require careful analysis and planning. Most constraints come from the PCB Stack Interface Control Document (ICD)[15] provided by the FIND'NM program sponsors. The ICD details the specifications to conform to the allotted payload placement and the input lines for the satellite transmission system circuitry.

3.1.1 Operating environment.

The operating environment further narrows the considered components to populate the payload PCB. The survival temperature range of each component and noise

interference requirements when selecting low ESD or radiation hardened hardware are critical characteristics to consider. The CubeSat payload host satellite will orbit within the LEO band [15] and therefore exposed to the hazards discussed in Section 2.4. The satellite housing encloses the PCB stack, protecting it from harmful temperature fluctuations caused by the Sun and the vacuum of space. The PCB and components must be manufactured to withstand electronic temperature limits in a space environment [33].

Table 1: [33] Typical spacecraft component temperature limits according to Fundamentals of Space Systems by Vincent Pisacane .

Component or Subsystem	Operating Temperature (°C)	Survival Temperature (°C)
General electronics	−10 to 45	−30 to 60
Batteries	0 to 10	−5 to 20
Infrared detectors	−269 to −173	−269 to 35
Solid-state particle detectors	−35 to 0	−35 to 35
Motors	0 to 50	−20 to 70
Solar panels	−100 to 125	−100 to 125

The internal temperature fluctuation inside of the satellite housing can range from -10°C to 45°C. However, the temperatures can fluctuate to between -40°C to 71°C during launch or traversing to orbit [15], thus further constraining component survival rating to maintain functionality. More robust components reduce the risk of system malfunction if it exceeds minimum environment specifications. COTS components can function in environments with temperature fluctuations of -55°C to 100°C, which far exceeds minimum specifications.

To define a sufficient product testing scope, achieving a more precise understanding of the existing hazards the equipment may face can be an asset. PCB components are known to be the most vulnerable to space conditions 2.4.1; however, the project scope assumes that the CubeSat housing is composed of adequate radiation shielding [41, 15],

thus protecting the payload and therefore relieving research resources necessary for protecting the PCB from detrimental high energy particles and additional, otherwise notable, radiation.

Note that neutrons are not affected by common shielding of CubeSats. Because Neutrons lack a charge, they pass through materials without much interaction unless they collide with an atom. This may cause a slight loss of energy and a change in direction, but are otherwise not stopped as other radiation would be. Thus, the radiation we desire should not be filtered by the on-board shielding.

TID exposure can range from 4 krad(Si)/yr to 40 Krad(Si)/yr [4]; therefore it is reasonable to assume the CubeSat contains a minimum performance of 10 mils of aluminum. However, information related to protection from radiation or the operational life expectancy of the payload is absent from the FIND'NM program specifications. Consequently, each PCB component selected is such that the highest operating duration is achieved, despite the unknown housing thickness or shielding installed on the host satellite. Although, if a worst case scenario occurs (i.e., radiation shielding is unavailable), the operation life of the PCB will have a likely time to failure of 1 year [4].

3.1.2 Circuit Board constraints.

According to the PCB Stack ICD [15] provided by the sponsor, the dimension of the payload are constrained to the following dimensions as seen in Figure 16:

- Board width: 2.91 inches
- Board Length: 2.75 inches
- Board thickness: 0.063 inches

To interface the host satellite functions, specific components must be placed on the PCB. The main connector, a Molex 80-pin plug positioned on the top of the PCB

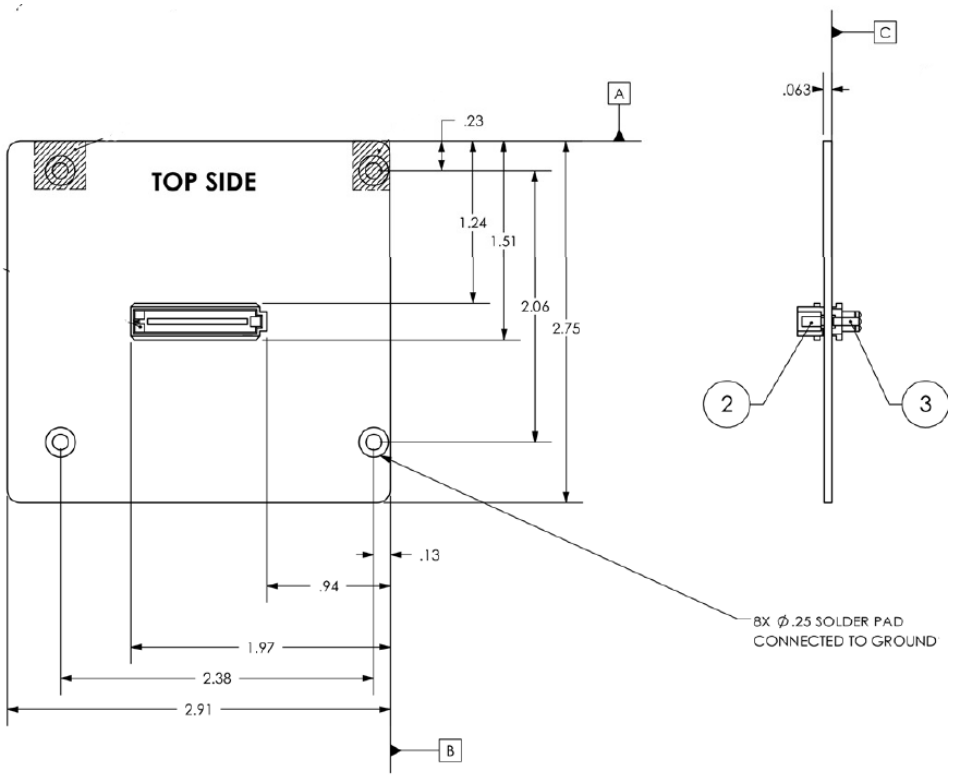


Figure 16: Cube-sat payload Dimension requirement for circuit board size, mount placement, and connector interface[15].

and an 80-pin receptacle placed on the bottom of the PCB positioned according to Figure 16 is a mandatory plug. This connector provides the PBC payload with a 12V DC power supply generated from the Satellite as well as common ground for all boards within the payload. Each board will have a current limit on the DC voltage input of 2 Amps and have a dedicated power supply line. The PCBs can only pull power from their dedicated pin configuration and no two payload boards will be powered concurrently. The Molex connector, as seen in Figure 17 will also provide access to

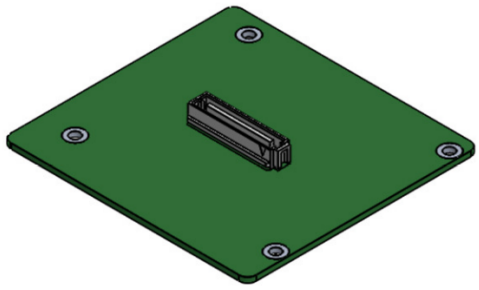


Figure 17: A 3-D rendered image of a Molex 80-pin 46557-6145 connector placement requirement per the Greenlit ICD [15]

the satellite transmission lines, which will be utilized to package and send batches of data back to earth for post processing. Each experimental PCB within the stack will have a dedicated window of operation, though that exact specification has not been released to date.[15]

Two mounting holes located on the top of the PCB have shaded "keep out" areas where components cannot be placed. All vias, the wells connecting multiple layers of a PCB, must be fabricated with greater than 0.3mm diameter and all traces have a minimum width of 0.2mm. Components are required to stay within a 4mm height on the top of the PCB and 3mm height on the bottom. This provides enough clearance between boards in the PCB stack to ensure there is no component contact. The

fabricated PCBs are required to be manufactured in two configurations depending on their intended use. All "prototype" boards (which is of primary focus in this research) will be manufactured to the IPC-600 specification, while all "flight" boards are to be manufacture to the MIL-P-55110 standard.[15]

Critical components are to remain the same between the minor revisions to minimize drastic functionality differences in testing and behavior of operation. For this thesis, a critical component is referred to those components that govern the board operation as a device. These items are those encompassed within the Signal Processing and Power supply sub-systems, specifically the FPGA, voltage converter, programming chip and all required supporting components for operation of those ICs.

3.1.3 Data Interface protocol.

Data examination from the radiation sensor is requisite for the project. To transport the collated data for later processing, the satellite broadcasts it to the ground. The PCB is tasked with packaging and then sending the data to the host satellite using the provided data bus transmission lines [15]. This subsystem is considered finalized once the PCB can complete a handshake with the receiver and transfer uncorrupted data. No further subsystem revisions is anticipated.

3.2 Hardware Design Considerations

A CubeSat payload board design is largely based on COTS and hobbyist hardware. This allows for flexibility under a constrained timeline and offers reliable and well tested product. The hobbyist boards act as a quick-turn-around test bench for software manipulation and plug-and-play component testing and is well documented. The PCB interface design can be separated into three major subsystems shown in Figure 18: Signal Capture, Signal Processing, and Power supply.

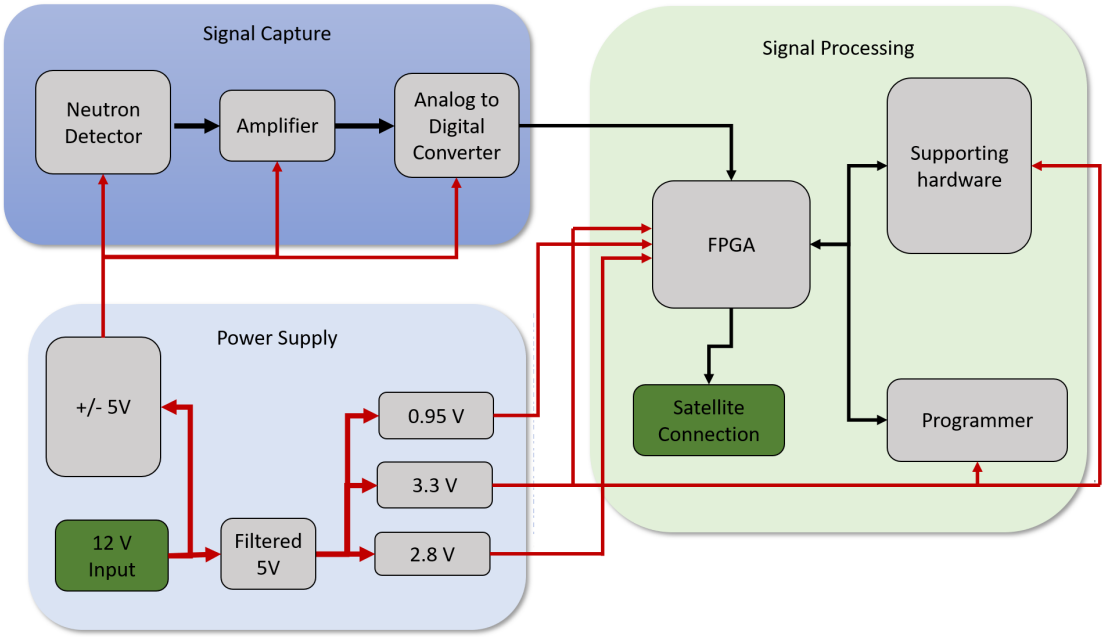


Figure 18: Block diagram of the proposed device design detailing subsystems and general component features.

3.2.1 Signal Capture.

Section 2.2.2 identifies three functional models for the theoretical neutron detection device. The potential candidates were presented for consideration during various phases of the project stemming from AFRL feedback. During the early stages of the project, initial assumptions and testing suggests the device functions as a JFET; hence Board V1.0 was designed and fabricated with a JFET compatible configuration. After verifying the V1.0 PCB, the claimed device characteristics were revised to behave as a diode-type device. Therefore, the V1.1 PCB was modified to compensate for the major change of the signal-capture subsystem. Of course, this requires further simulation and fabrication verification. Before populating the board, the detection sample was again revised; the sensor was modified to behave like a resistor. Digital simulations of the newly revised V1.2 board was conducted, however scheduling constrained PCB testing and fabrication to only V1.0 and conceptual a V1.1 PCB revision. Each sensor

redesign, in turn, called for a redesign of the amplification circuit.

3.2.2 Detection sample socket.

A surface-mount chip-carrier (or "flat-pack") seen in Figure 19 interfaces the board. The flat-pack is able to support a sensor sample of up to 0.75in $\times$ 0.75in and provides a hardy support structure to keep the samples free from handling/jostling which needed to be limited due to the fragility of each structure. The flat-pack also provides a removable component that can be fitted to all V1.X boards and therefore offers a convenient method for interfacing other contacts attached to the samples. An epoxy

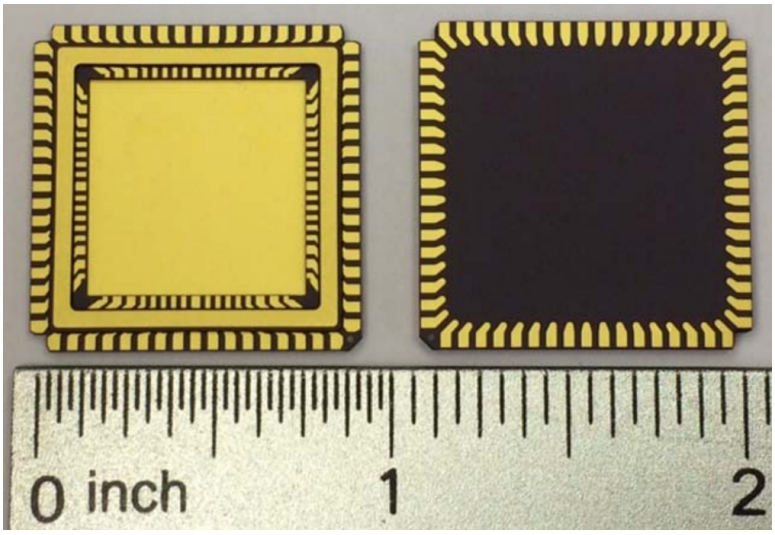


Figure 19: The carrier is gold plated and is intended to interface and protect the detection sample while adhered to the PCB.

adhesive protects each sample and silver paint is used to promote conduction to the ground plane. The epoxy is recommended by NASA for low out-gassing products, an effect in which the surrounding resin may crack or explode due to atmospheric pressure variations between the ground and orbit. Once the samples contacts are adhered, an additional epoxy dome will be poured over the sample to further protect it from general handling and anticipated flight vibrations.

3.2.2.1 JFET-type input model amplification.

The V1.0 PCB was largely influenced by the expertise of Mr. James Herner, Electronics Specialist/Electrical Engineer CSRA, in support of the FIND'NM project. Despite disclosed PCB constraints, the support for the detector sample is otherwise early in development. The two-stage signal capture amplifier uses the OPAMPS LT6018 and AD8067 (Appendix A) since the sensor was expected to perform like a low output JFET. For completeness, the now depreciated amplifier is explained in the following:

The first stage of the amplifier is a pulse shaping amplifier configured as a charge integrator using LT6018. This includes an RC circuit feedback to elongate a short pulse. The signal gain is increased using an AD8067 in a non-inverting configuration, see Figure 20. A high-pass filter is embedded between the two amplifying stages to help mitigate unwanted noise from saturating the output. The pull-down resistors sink the source input while no source is applied to ensure noise does not interfere with the source pulse. This configuration causes the signal, steady at a nominal -1.5V output, to drop to zero briefly. The two OPAMPs can be compounded in the following equation:

$$V_{out} = \left(1 + \frac{R_{f2}}{R_5}\right) \int_0^t \frac{C_f}{R_{f1} \cdot C_f}(V_{in})\mathrm{d}t \tag{8}$$

The resistor (R) and capacitor (C) values are found in Figure 20.

3.2.2.2 Photo-diode input model amplification.

The assumption basis changed partway through the project, influencing the V1.1 design by adjusting the amplification circuit to support a photodiode operation. The

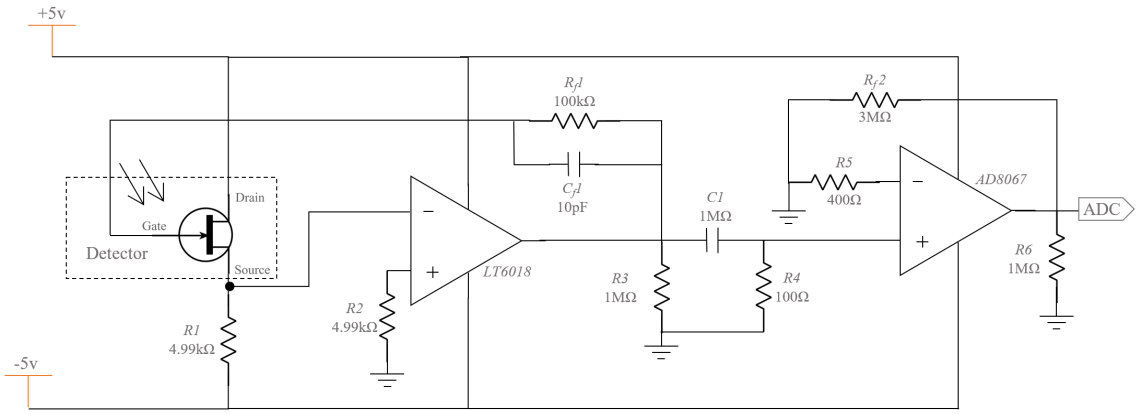


Figure 20: Amplification circuit design to support the JFET operation theory. Utilizes two operation amplifiers to convert the current drop over the JFET into a positive output voltage going to the ADC.

amplification circuit was simplified by implementing a TIA that was specialized for photodiode operation. More specific characteristic information regarding the OPA380 can be found in Appendix A.

By utilizing the simplified equations for a non-inverting amplifier in equation 5 and substituting $V_{in} = R_{in} \cdot I_{in}$, the voltage out ($v_{out}$) seen in Figure 21 is calculated to be the following:

$$V_{out} = R_f \cdot I_{in}. \tag{9}$$

Assuming the input is the approximated 50μA source, the amplification should be approximately 2.5V output. This TIA utilizes a parallel RC circuit to mitigate any degenerative feedback. Without the capacitor in place, the amplifier would experience oscillation outside of the initial pulse signal. Instead, the TIA should output a steady, low noise signal that can be utilized by the ADC.

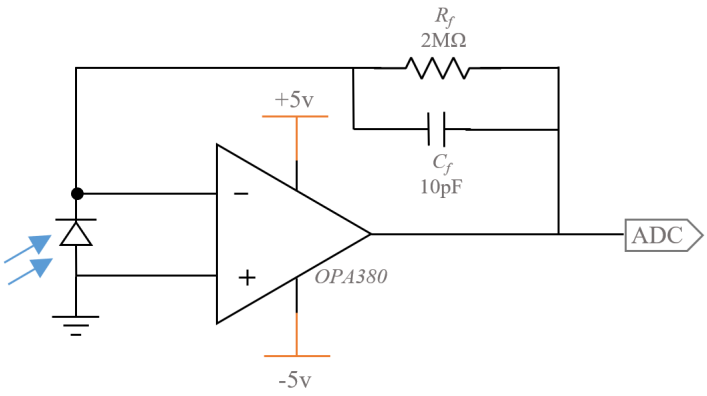


Figure 21: The amplification configuration for the photodiode equivalent circuit utilizing the OPA380 in an inverting circuit configuration. The OPA380 TIA will capture the current draw from the photodiode and convert it to a usable voltage for the ADC.

3.2.2.3 Photo-Resistor Input-Model.

Toward the end of the research, the operating assumption was again altered in favor of a more resistive device. This simplified the circuit considerably in the V1.2 design, utilizing a voltage divider circuit and a non-inverting OPAMP configuration to achieve a signal output. The output voltage for Figure 22 is the following:

$$V_{out} = (V_{source} \cdot \frac{R_{photo}}{R_1 + R_{photo}}) \cdot (1 + \frac{R_f}{R_{in}}). \tag{10}$$

V_{source} is the 5V bias line, R_1 is the voltage controller, R_{in} is the amplification controller, R_f is the feedback resistance, and R_{photo} is the variable resistance sample, in this case a photoresitor. Note that R_1 is part of the voltage divider and must be tuned to support the specific sample input. In this case, R_1 was held at 2KΩ to support the photo resistor value and give a solid output signal.

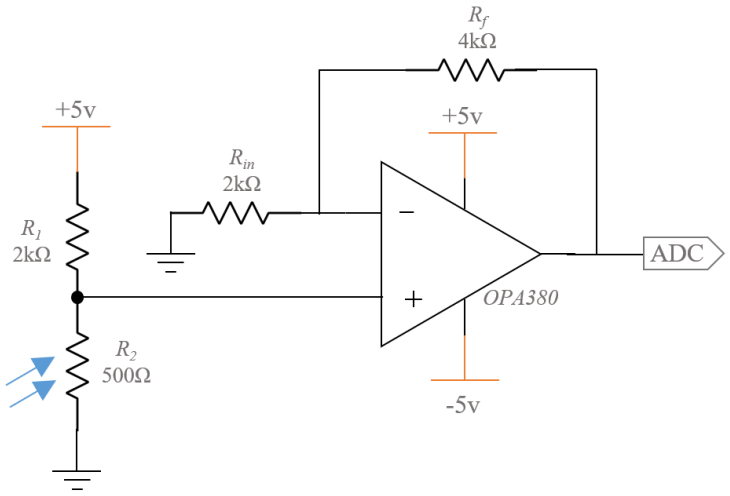


Figure 22: The amplification configuration for the photoresistive equivalent circuit utilizing the OPA380 in a non-inverting circuit configuration. The OPA380 TIA will capture the voltage spike from the photoresistor and convert it to a usable voltage for the ADC.

3.2.2.4 Analog-to-digital Converter (ADC).

The output from the amplification circuit is currently a raw analog signal, thus an ADC system is implemented to convert it to binary data that the FPGA can store and transmit. This subsystem is composed of two components: an LT6201 buffer, and an LTC2389 ADC. The buffer requires the -5V and +5V source voltages, each being equipped with a low pass filtering capacitor to ensure low/no frequency oscillation of the DC voltage. This buffer ensures the ADC receives a strong, clean signal from the amplifier circuit for reliable operation. If the reference signals are jittery, this will alter the difference calculations and give incorrect conversion output. From this buffer, the signal is subject to another low pass filter, utilizing the filters to alleviate the high frequency noise within the signal source lines. This input configuration is recommended by Linear Technology as seen in Figure 23.

For more in-depth information regarding the ADC and buffer part specifications,

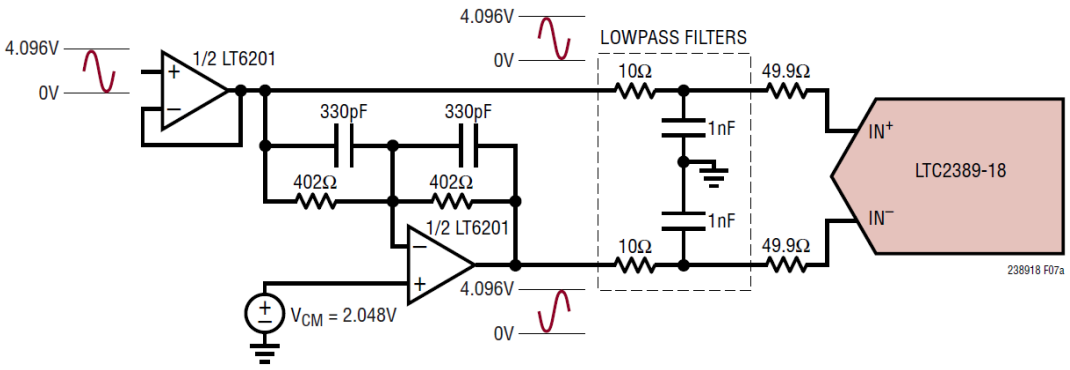


Figure 23: The recommended operation of the ADC utilizing a buffer and reference voltage signal to convert a single-ended signal to a fully-differential signal [24].

refer to the Appendix A. The ADC is powered by a 5V source passing through an array of low-pass capacitors in an attempt to catch unique oscillations within the line. This smooths out the input voltage considerably which assists the ADC with easier conversion.

The ADC is controlled by three major lines: Conversion time (CNVST), BUSY and an 18-bit Data bus. The LTC2389-18 is controlled by sending a falling edge on CNVST, which initiates the conversion process. Once begun, the conversion cannot be restarted until the current conversion is complete. One timing nuance that must be considered is the CNVST reset to high timing, which has to happen within 40ns from the start of the conversion or after the conversion is complete to ensure no errors occur in the digitized results. Converter status is indicated by the BUSY output, which remains high while the conversion is in progress. Once the conversion is complete, the results are then passes to the FPGA using a 18-bit register. Software to control the ADC with the μcontroller FPGA can be found in Appendix D and a more detailed explanation is in Section 3.3.

3.2.3 Signal Processing Design.

To ensure the Payload is kept within a COTS constraint, the FPGA selected is based on the Artix-7 FPGA System-on-a-Chip (SoC) Development Board by Digilent as seen in Figure 24. This board implements the Xilinx Artix-35T FPGA and fits the desired compatibility with the ADC mentioned in section 3.2.1. The FPGA is supported by specific voltage and array of feedback capacitors that attenuate the incoming signal for proper function of the FPGA. The PCB design was largely based upon the development board as a means for testing and proving subsystems before hardware was affixed.

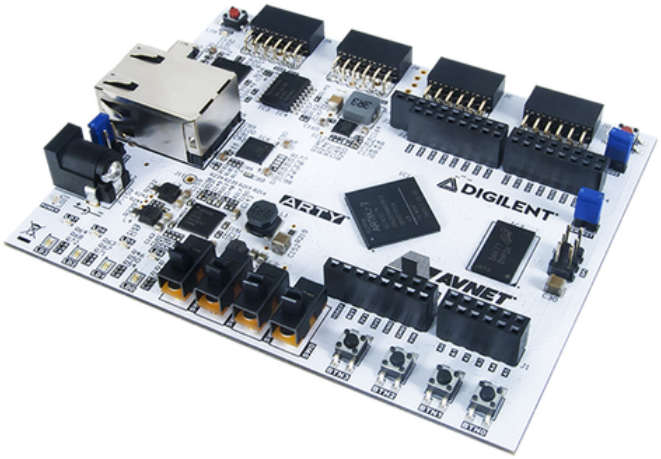


Figure 24: The Artix-7 Development board for makers and hobbyist by Digilent. A good portion of the FPGA design encompasses a similar implementation of the Xilinx Artix-35T FPGA [19]

3.2.3.1 Power requirements.

To power the FPGA, three different voltages are required for clean operation: 1.8V, 3.3V, and 0.95V. To mitigate any jitter or slew in the operational voltages for the FPGA, each input line is designed with an array of low-pass filtering capacitors

situated near the FPGA, seen in Figure 25. Each of these capacitors is a differing package size or differing value to filter out the wide spectrum of high frequency noise within the input voltages. This cleans the signal as best as possible as the IC is vulnerable to any high frequency oscillation.

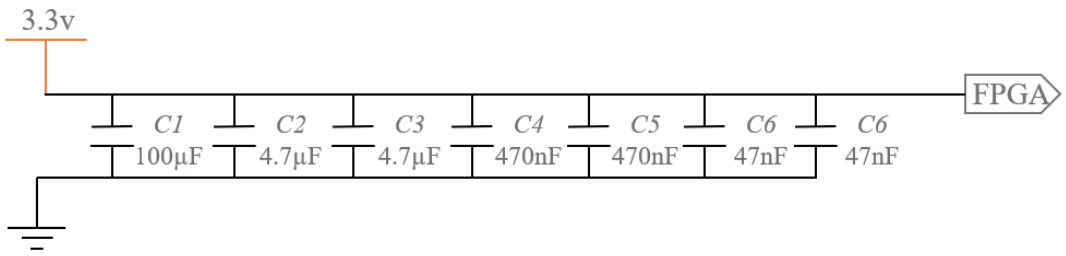


Figure 25: The configuration of parallel capacitors of differing package type and value to mitigate jitter within a DC voltage line.

3.2.3.2 FPGA Peripherals.

The FPGA is connected to a Quad-Serial Peripheral Interface (SPI) (Micro-N25Q128A13ESF40), which enables the FPGA to automatically read configuration files at power-on. This also allows the FPGA the ability to re-flash itself in the event of a SEE error and is implemented by way of a forced power cycle every 168 working hours.

The FPGA is programmed using a 6-pin JTAG header which interfaces the JTAG port on the Artix-7 FPGA. This header also interfaces the Quad-SPI to flash the FPGA programming files. This interface requires a unique programming unit which attaches to a MicroUSB cable, available through Diligent Inc.

External communication (sending data to the host) is handled by the Universal Asynchronous Receiver-Transmitter (UART) bus, enabling the transmit and receive lines to interface the molex terminal and output data. These circuit schematics can be

found in Appendix B. The FPGA also interfaces the external ADC, which required an 18-bit bus to provide data back to the FPGA. The specifics were discussed in Section 3.2.2.4.

3.2.4 Power supply.

The input from the satellite host system is a 12V DC supply voltage according to the sponsor ICD [15]. This supply will be parsed into 5 required power lines for component and board operation: +5V, -5V, 3.3V, 1.8V and 0.95V.

To attain the step-down voltage of ±5V, the design utilizes a LTM8049, which is a power module DC/DC converter. Note that more detailed characteristic information can be found in Appendix A. This component is desired for its dual output capability, reducing the footprint space on the limited PCB area. The power configuration is based on the recommended circuit design from Linear technologies to attain the desired output, the circuit is depicted in Figure 26. The raw ±5V lines are then separately fed into a series inductor and shunt capacitors to filter out noise within the generated lines. These schematic drawings can be found in Appendix B. It is especially crucial to ensure the +5V line is filtered as it is the source signals for the operational amplifiers. The 12V line is also passed through a second 5V DC-to-DC step-down regulator, LTM8022, to ensure there is no voltage drop contamination from the amplification subsystem going to the FPGA.

The 5V terminal is then passed to an ADP5052, a Analog Devices 5-channel Integrated Power solution. It combines four buck regulators (Dc-to-DC step-down regulators), and a 200mA low dropout (LDO) regulator. More detailed information regarding this component can be found in Appendix A. For this research, the FPGA only required the use of the 3 buck regulators. To attain the desired output voltage from each regulator, a feedback loop ties the output voltage back to a feedback sensing

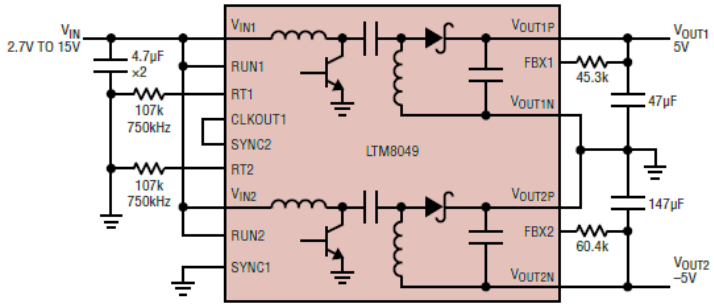


Figure 26: The recommended configuration for the DC-to-DC step-down converter configuration from a 12V input to a ±5V output. [25]

circuit within the chip. A feedback resistor, which is unique to the channel for fixed output, influences the voltage input bleeding off excess voltage to ground. A schematic of the entire board circuit drawings can be found in Appendix B.

3.3 Software Design Consideration

The FPGA is a flexible element of this project, able to be modified to test certain functionality. For this research, the FPGA was utilized as a processor to collect and transmit data. To set up the processing unit, the ARTY board was used as a test bench to confirm adequate code functionality before flashing the interface PCB.

To enable the processing unit, Vivado from Xilinx, Inc. is used to compile and flash a block schematic based source file. These are defined as software SoC, or soft SoC, FPGA configurations and are designed graphically using a tool called Vivado IP Integrator. This tool contains pre-built peripheral blocks which contain timers, controllers and a unit containing the Microblaze processing configuration. The IP Integrator enables the chip to utilize the external SPI flash, oscillator, and ADC while configuring the system for output using the I2C output lines. Tutorials and board specific configuration files can be found on the Xilinx support site [20].

Once the processing interface is established, pictured in Figure 27, the chip must trigger the ADC to gather the converted signal data and transmit it back to the waiting console which stores the information for processing. To interface the external

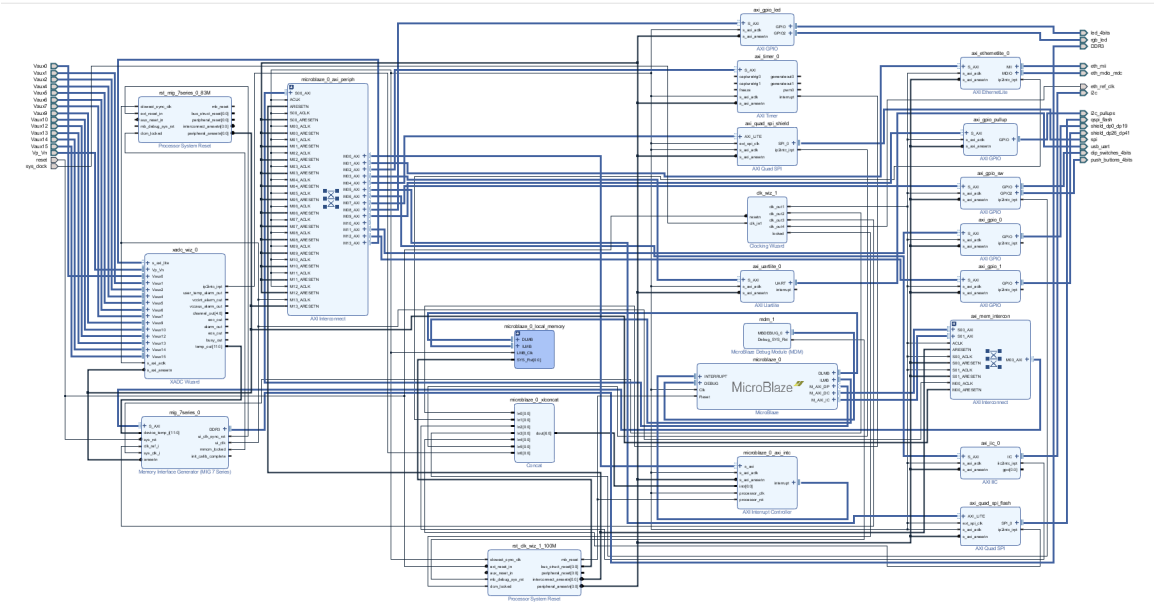


Figure 27: Vivado's IP Integrator software defined graphical programming using the MicroBlaze IP core and peripherals to enable the FPGA to function.

ADC, the FPGA is loaded with a user defined peripheral block using a combination of Vivado's Block schematics and the Xilinx Software Development Kit (SDK). The FPGA is considered a Very High Speed Integrated Circuit (VHSIC), thus the interface program was written in VHSIC Hardware Description Language (VHDL). The code utilized can be found in Appendix D. Note that the FPGA constraint file needs to be altered to point to the desired output pins, which can be seen in Table 6.

Data expected from the V1.0 (utilizing the V1.1 amplification update) interface boards will be a list of binary values captured from the ADC and sent to UART. This information should be consistent, showing adequate operation of each subsystem, not affected by environmental factors.

3.4 PCB layout and Fabrication

PCB layout is a time intensive secondary process with a wide breath of creative design aspects. Specific steps to populate V1.0 boards and modifications needed to accommodate V1.1 amplification are detailed in Appendix C. Depending on the component, there are specific requirements for PCB layout. Some data sheets detail the maximum allowed distance from an IC to a component (E.g. the FPGA switching capacitors) or expressly give a component layout that mitigate issues between certain hardware.

For example, Figure 28 shows the recommended PCB layout to ensure optimal operation of the ADP5052. These layout considerations ensure proper operation of the board such that no interference, as in the case with the ADP5052 and its accompanying inductors, is seen by the sensitive traces.

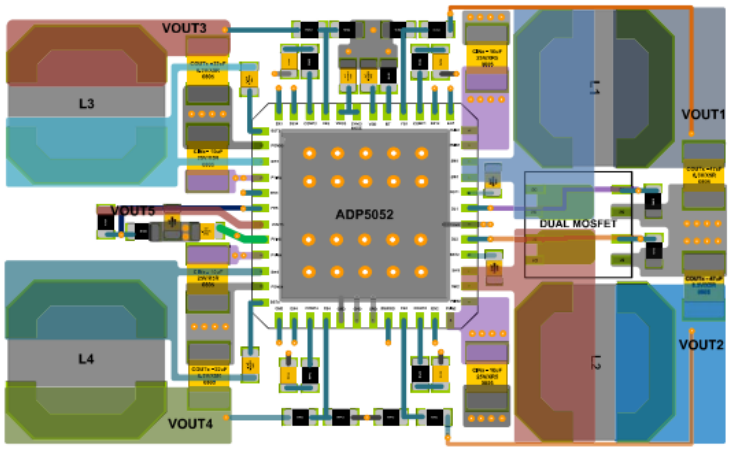


Figure 28: The typical PCB layout of the ADP5052 component to reduce interference caused by crossing traces beneath the inductors. [2]

Altium Designer 18.1.9 was used to route PCB components and later generate the required output files for fabrication. All typical or recommended PCB layout configurations (if they are required for the component), can be found in the corresponding

component data sheets.

For components in which time synchronization is considered, a PCB design approach called length-tuning is used. This technique entails etching traces in an accordion-like shape to adjust the overall length of the line and therefore causing a change in signal latency to a receiver. The implementation of length-tuning from the ADC to the FPGA can be seen in Figure 29.

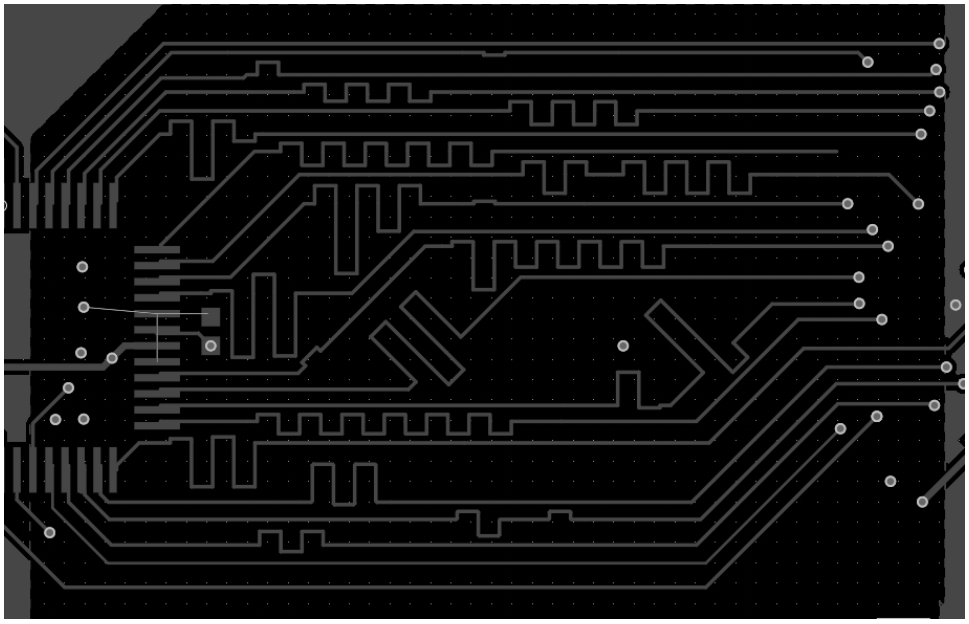
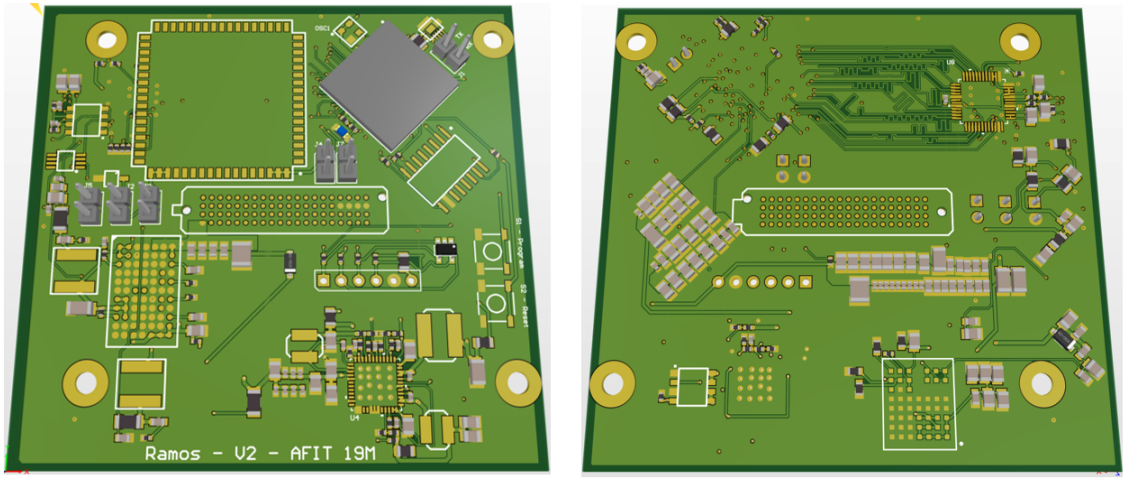


Figure 29: Data lines from an ADC to the FPGA require length-tuning to force data to arrive at the same time.

Fabrication of both V1.0 and V1.1 boards was handled by Advanced Circuits Inc due to the limited capabilities of manufacturing the PCBs in-house. The final PCB layout for V1.1, in Figure 30 was rendered using Altium 18.1.9 and shows the placement of the FPGA, capacitor banks and other components before fabrication. Note that many of the original components from the V1.0 board are still present but have been modified for space and signal integrity.

Due to availability of parts, the V1.1 boards were finished with immersion gold to assist with adhering a lead component. This differed from the V1.0 silver plating,



(a) PCB Layout Front (b) PCB Layout Back

Figure 30: A rendering of the Version 2 PCB before manufacturing using the Altium 3D placement tool.

best for non-leaded components. V1.0 of the PCB was also manufactured with a number components not intended to be used in the flight configuration but required for testing/troubleshooting. These hardware pieces (i.e. a 12V jack, a USB socket) were replaced by a modified Molex socket and cable in later versions.

3.5 Simulation and Digital tools

Simulations were conducted on the amplification circuit design due to the variability of feedback desired for each unique input. Each input source was simulated using LTspice XVII to ensure adequate design and desired feedback component values using a realistic Amplifier operation model. The photodiode component was replaced by an equivalent circuit, detailed in Section 2.2.2.2, since the program did not carry a photodiode model.

The PCB design was created using the Altium CAD software utilizing the Schematic to PCB capability. Altium was also utilized to generating the production files required to manufacture the PCBs, covered in Section 3.4, as well as generate the bill of

materials (BOM) required to populate the PCBs.

3.6 Testing

Environmental testing was conducted on the PCBs to ascertain the functionality of the circuit in a space-type environment. Each sub-system was proved to function individually before being subject to destructive conditions. After testing, each sub-system was retested for degradation or failure. Individual power supplies (5V, 3.3V and 2.8v) are able to be attached and confirm function of all sub-systems as intended. The PCBs will then be powered in full and baseline signal reading on a silent board documented for each unique board. This "baseline" operation helps to reduce issues pertaining to single point failures and prepares each board for further testing and design focus.

3.6.1 Function tests.

A shunt is designed into the circuit at the interface of each of the subsystems to isolate any problems throughout the PCB. This acts as a controllable split in the trace and were placed throughout the design. Many of the ICs, the FPGA included, have the potential to be catastrophically damaged in the event any of the other subsystems incurred a short or were incorrectly routed during PCB layout. Each subsystem was inspected and proved to adequately function based on the following methodology.

3.6.1.1 Power supply sub-system.

Due to the unavailability of the LTM8049 from the manufacturer within the limited time constraints, a generated voltage of $\pm$5V was applied to the output lines in place of the component. The sub-system was still subject to a 12V input, to ensure the other converter, LTM8022, gave the correct output and signal quality was checked

before connecting to a second subsystem.

3.6.1.2 Signal capture.

The signal processing sub-system was designed with two jumpers and an output header to test the functionality of the amplifiers and act as interface lines for each component. This allowed the system to be checked for shorts, isolate in input, and note a noise baseline from the OPAMP/TIA components. These jumpers also allowed the detection circuit to be replaced with a generated signal to ensure predictable output through the amplifiers. Functionality was deemed successful if the system returned an amplified signal that would be detected on an oscilloscope.

3.6.1.3 Signal processing.

The FPGA system is dependent on the power supply sub-system and requires the successful operation of the ADP5052 voltage step-down converter to function properly. The FPGA support circuit was designed with a programming header and an output jumper for transmit and receive lines. The FPGA was tested in three stages: Power-on, Flash successful, and power-on-flash successful. The FPGA power supply was deemed successful if the FPGA could be powered on and could connect to an input, such as a computer for programming. The FPGA function was successful if the IC could be programmed with the operational program and transmit feedback through the communication lines. Finally, the power-on-flash test was successful if the PCB power could be cycled and the SPI re-flash the FPGA with the required operational program.

3.6.2 Thermal-Vacuum Test.

Thermal fluctuation testing was conducted using a Thermal-Vacuum (TVAC) chamber to ensure components and PCB are able to withstand both survivability temperature ranges and Operational temperature ranges as discussed in section 3.1.1. The use of a TVAC chamber allows the boards to be subject to both temperature and degassing elements of space operation.

3.6.2.1 Survivability Testing.

The survivability test was to confirm the failure point of the printed circuit boards. This test mimics worst case temperature ranges to pinpoint the subsystems that fail. Note: each subsystem has connectors that will isolate it from each stage. This was not a powered test. The test consisted of the following scenarios:

- Cold Survival: Unpowered PCB subject to -30C (no required time duration), set back to ambient temperature and removed for failure analysis
- Hot Survival: Unpowered PCB subject to 60C (no required duration), cooled back to ambient temperature and removed for failure analysis

Note that in this case, failure analysis refers to subjecting the PCB to the functionality testing in search of any major sub-system or component failures due to the extreme conditions. This may point to the need for more insulation or redundancy to protect the components that failed.

3.6.2.2 Functionality Testing.

The functionality test is used to confirm the board function over a specific known range of temperatures inside the CubeSat housing. These tests require the PCB to be turned on and processing data while the temperature fluctuates. The system under

test is connected to a signal generator to mimic incoming data along the amplifier circuit, a 5V power supply, and two transmit lines for data collection. This set-up will be referred to as the powered PCB. The test consists of the following scenarios:

- Powered PCB at ambient temperature will remain for 2-10 minutes of initial data collection to confirm operation and initial conditions.
- Powered PCB will then be subject to decrease in temperature to -10C. The temperature will maintain at -10C for 2-10 minutes for data collection.
- PCB will be returned to ambient temperature
- Powered PCB will be subject to temperature increase to 45C and remain from 2-10 minutes for data collection.
- Powered PCB will then be allowed to return to ambient temperature
- Powered PCB will remain for 2-10 minutes at ambient temperature for post experiment data collection to confirm any damage/change in signal quality.

3.6.2.3 TVAC Test Matrix.

The test matrix for TVAC testing can be seen in Table 2.

3.6.3 Vibration Test.

To get into orbit, the PCB will have to survive a myriad of vibration and gravitation forces acting upon in it. Vibration testing will give insight into how well the PCB will fare during a lunch. The test is set up using an unpowered PCB that will be mounted on a vibration test apparatus located at AFIT. The PCB is subject to vibrations mimicking launch type conditions as recommended by subject matter experts facilitating testing. The PCB then undergos functionality testing as stated above to identify which subsystem, if any, failed and what precautions are required to mitigate issues.

Table 2: TVAC test matrix for survival and functionality testing.

Version	Board Number	Temp (°C)	Duration (min)	Sub-system Status
V1	1	60	5	Power-supply: pass/fail Signal Capture: Signal Processor:
V1	1	-30	5	Power-supply: pass/fail Signal Capture: Signal Processor:
V1	2	45	60	Power-supply: adequate? Signal Capture: Signal Processor:
V1	2	-10	60	Power-supply: adequate? Signal Capture: Signal Processor:

3.6.4 Radiation Detection validation.

A device will be subjected to a neutron source while fully operational to validate if the system responds to neutrons as expected. This testing will be conducted at AFIT using the deuterium-deuterium (D-D) source. Ionizing radiation testing will be conducted through Ohio State University (OSU) using their Low-enriched uranium (LEU) solid plate fuel source Cobalt-60 Underwater irradiator. Another option for testing would be the Cyclotron Institute at Texas A&M University, which has a radiation effects facility that offers a wide range of testing availability. The primary area of interest is the vacuum test chamber available for radiation testing.

3.6.4.1 Radiation Detection Test Matrix.

The test matrix for radiation hardening testing can be seen in Table 3. Testing will be conducted on V1.1 amplification circuit on the modified board, the board that was a modified version of V1.0, and the finished PCB, the fully populated V1.1 PCB.

Table 3: Source and TID test matrix.

Version	**Source**	Total Dose (hrs)	Functional	Noise: G/D/F
V1.1 (modified PCB)	D-D D-D C-60	2krad 4krad 2 krad		
V1.1 (Finished PCB)	D-D C-60 LEU	2krad 2krad 2krad		

3.7 Data Analysis

All data collected from each test will be compared against baseline operation of the same tests to mark improvement or degradation based on the adjustments made. This will allow for marked improvements to be incorporated into the final device and ensure the system capable of supporting a UO_2 radiation detector device depending on its operation type.

IV. Simulation Analysis and Test Results

This chapter presents the results of the experiments shown in Chapter III. The first section introduces the project overview followed by the V1.0 simulations and sub-section functionality testing performed. Subsequent sections present the simulation and collected data from the V1.1 and V1.2 designs before discussing the testing recommended for follow-on research effort.

4.1 Project overview

The interface device was slated to be designed, fabricated, and tested throughout six months in preparation for joint testing of the detection samples in conjunction with this research effort. This would allow for sufficient testing and modifications to be made to the PCB system. Initially, the PCB was designed to be a single version to accommodate environmental testing and radiation hardening of the first-generation detection samples released by AFRL. A detection sample can be seen adhering to the V1.0 PCB in Figure 31. However, because this was a parallel effort, sample characterization information was not available.

Therefore, a surrogate system was implemented to assist with the design of the PCB. Each surrogate required different support designs as the operation characteristics of the sample evolved. Each new characteristic change needed a revision of the design and PCB refabrication to accommodate the new operating sample. This was required because the amplification system design was specific to the sample operating conditions.

Testing was performed between each design revision. Each sub-system is tested for functionality and some troubleshooting was required to fix some manufacturing and population errors. Before data and environmental testing could be accomplished on the V1.0 complete boards, the input design conditions changed which rendered

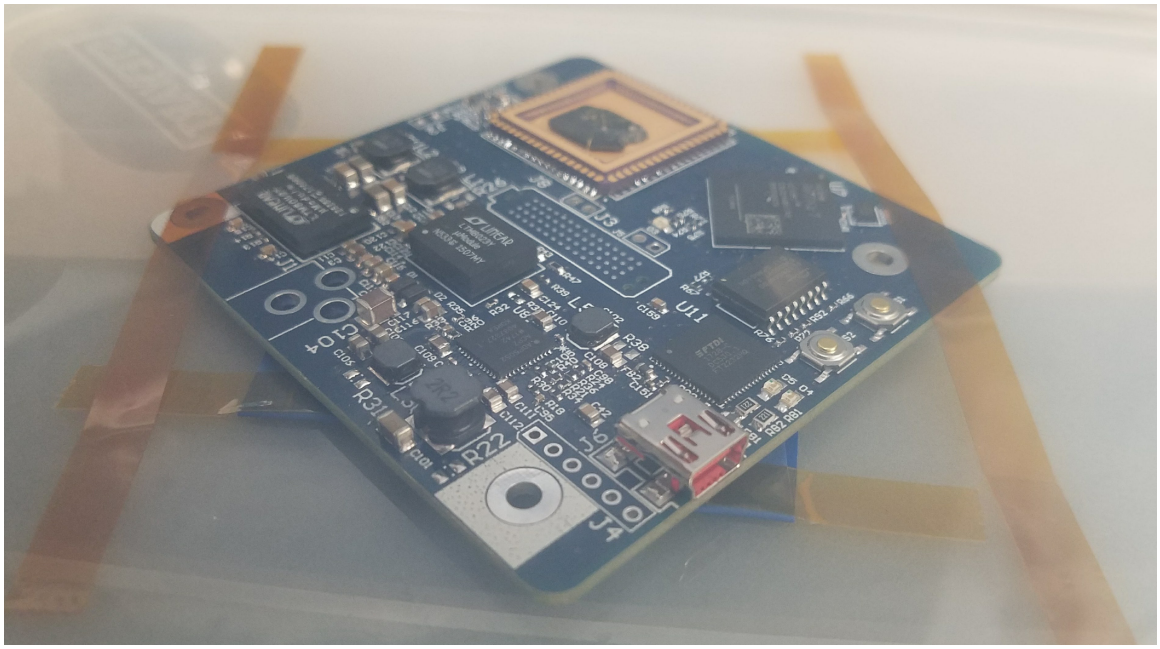


Figure 31: Version 1.0 PCB with a detection sample package adhered in preparation of initial testing. The sample and PCB are contained within a protective box while being held steady to avoid damaging the fragile crystal. This was the only version to be fully populated (including the only voltage regulator available) before transferring to AFRL for testing which, due to input characteristic changes, was not accomplished.

the signal capture sub-system unusable for the new input device. V1.1 modified this sub-system while utilizing the already functional signal processing and power supply design into a new PCB. This new design was then submitted to manufacturer, but the delay in ordering and revisions for unavailable parts delayed the V1.1 boards considerably. After fabrication of the V1.1, but before component population, the input device characteristics changed for a third time. Though the third board revision was planned, only the proof of concept for data capture utilizing an external circuit was accomplished. This section documents the results of each test conducted on the PCB, as well as discussion of simulation results where testing was not attainable within the constrained time-frame.

4.2 Version 1.0

The Version 1.0 PCB was fabricated by Advanced Circuits but the electrical components were populated by hand. Details on Fabrication equipment used and specific steps can be found in Appendix C while the schematics containing relevant components values can be found in Appendix B. The resulting boards after component population and solder-flow can be seen in Figure 32.

This PCB was tested to confirm adequate functionality of each subsystem. This testing and troubleshooting took approximately 3 weeks to complete before signal integrity tests could be performed utilizing the programming code in Appendix D.

4.2.1 Amplification Simulation results.

To assist with amplification design, the signal capture sub-system was simulated using an assumed input signal of 50μA at a 50MHz frequency to confirm that the amplifiers did not reach saturation if bombarded with particles. The results of a single pulse from the V1.0 amplification output can be seen in Figure 33. As seen in the

Figure 32: Version 1.0 PCB just after solder flow for surface mount components. Pictured are (left) board number 2 back and (right) board number 3 front.

graph, the output voltage of -1.5V is a steady reading that can be sampled by the ADC to ensure the system is still operational. The input of the signal pulse drops the voltage from a constant -1.5V output to 0V briefly due to the configuration of the OPAMPs and DC filtering capacitor between the OPAMPs. This voltage drop would be seen by the FPGA and a noticeable spike appears in the data. It is spanned over 1μs, elongating the initial pulse of 20ns. This ensures the ADC, which samples at 70ns intervals has the opportunity of catching a pulse of such short duration.

4.2.2 Sub-system testing.

Upon testing, it was still assumed that only the V1.0 device would be the primary focus of the project, so each sub-system was tested for operation. However, before the V1.0 PCB was slated for environmental testing, the input assumption changed and effort was redirected to support the V1.1 assumption change and PCB fabrication instead. Thus the V1.0 amplification system was never testing with real-world input.

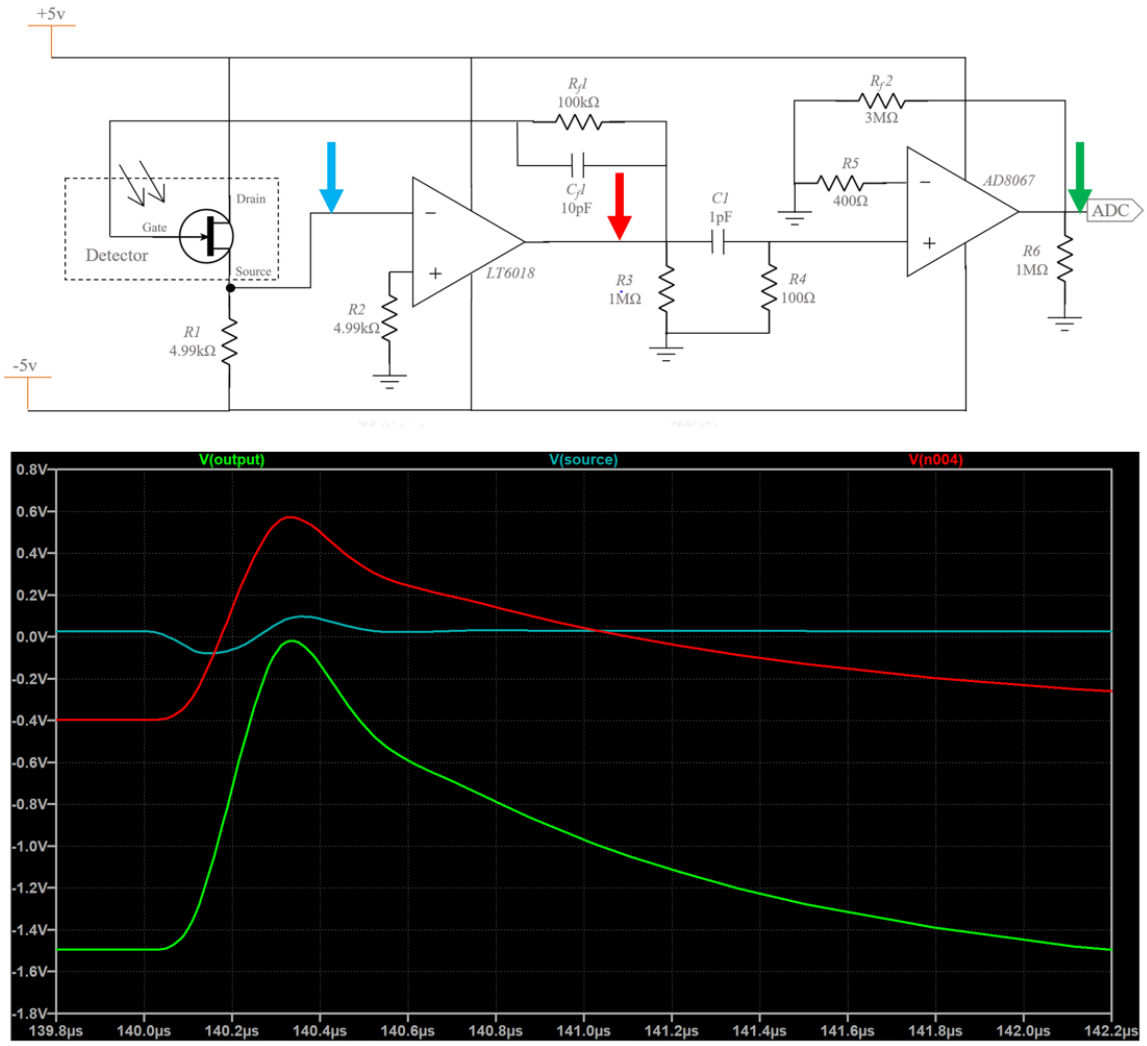


Figure 33: Simulation results utilizing the amplification configuration recommended to support a JFET surrogate operation. Each probe is color coded on the circuit (top) to correspond with the output graph (bottom).

4.2.2.1 Power Supply.

Due to a missing component, the LTM8049, the device required an external DC voltage of ±5V over the missing component output lines. This was handled by interfacing the positive and negative 5V terminals with two male jumper pins. These provided an easily removable voltage line that would be removed if the part was replaced. Each of the 5 differing voltages were then measured utilizing a multimeter to ensure there was not a voltage loss over the other voltage source lines. A list of the required voltage lines and their measured output can be found in Table 4. A 12V DC voltage source was also applied by the Power Jack to check the other voltage regulators for proper function. Once each voltage line was confirmed operational within a 1% voltage tolerance, jumpers connected the secondary sub-systems.

Table 4: Measured voltage source lines at sub-system interface.

Schematic (V)	**Measured (V)**
+5	5.01
-5	-4.993
3.3	3.27
2.8	2.78
0.95	0.946

4.2.2.2 Signal Capture.

Each amplification system was designed to accommodate the JFET detection device and was tested for adequate bias power and terminal signal continuity. Note that this amplification system only supports the input behavior of the JFET input surrogate device and was rendered useless once the input behavior of the sample was changed. Efforts to test this sub-system were discontinued in favor of the V1.1 PCB design to accommodate the new device parameters instead. This subsystem is

deprecated by the V1.1 and V1.2 amplifier requirement changes.

4.2.2.3 Signal Processing.

Extra components are included in the test version of the V1.0 board used only as interface terminals during prototyping. Among these components are a USB interface plug for data acquisition and a female power jack used for the 12V input power supply. The USB interface support IC failed due to proprietary software not attainable for this project. Instead a 6-pin header was utilized for JTAG programming and two wires were spliced into exposed traces for send/receive UART communication as explained in Section 3.2.3.2. These changes, known as white-wiring, allowed for the PCB to be further utilized without requiring another round of fabrication. The data transmission lines were connected to a modified USB cable and a COM terminal. This allows the user to communicate with the data port without the use of legacy hardware such as a DB25 parallel port or a RS-232 serial connector.

After the FPGA was configured using the MicroBlaze IP from Vivado, the device confirmed operation by sending a message back to terminal. PuTTY, which is a free and open-source terminal emulator, serial console, and network file transfer application was then used to interface the MicroBlaze UART circuitry with a baud rate of 9600bps. The FPGA flash executed a script in which "Hello World" is sent back through the UART to the user terminal. After successful execution, the program was modified to obtain the desired data from the connected FPGA ADC ports. Data collected included ambient temperature of the operating FPGA and signal input, which went unchanged at 0.013V, see Appendix E.

4.3 Version 1.1

Recall that V1.1 is a modified version of the V1.0 board, in which the amplifier circuit accommodates a surrogate photodiode input instead of a JFET measuring instrument. Although a board was fabricated to replace the V1.0 PCB, critical manufacturing and design errors prevented the board from being fully populated. Instead, part of the V1.1 PCB was used as a breakout-board to connect and use the photodiode and amplifier circuit for while also utilizing the already functional V1.0 board components. Information regarding the V1.1 modifications on the V1.0 PCB and the necessary interface lines for each board can be found in Appendix C.

4.3.1 Fabrication issues of V1.1 PCB.

There are three major issues regarding the V1.1 PCB which ultimately moved the decision to utilize it as a break-out board instead of a stand-alone PCB: the trace size of the internal layers of the PCB, a missing via connecting a critical data line, and the proximity of the timing capacitors to the FPGA.

Although the FPGA can theoretically be functional, given the timing capacitors are within a max allowable distance, the function may be degraded or unreliable. This oversight was not an issue with V1.0, since the capacitor positions were carefully monitored during board layout. Due to the differences between the V1.0 and V1.1 FPGA capacitor banks and since the V1.0 signal-processing sub-system was already tested to be reliable, it was decided that the V1.0 system was used instead.

The integral voltage lines running throughout the V1.1 PCB are still functional within the board, but the main concern is the heat generated by large voltages running through a small trace on an internal layers of the PCB. Ideally, the traces encompassing any power lines are at least 50 mil in width to dissipate heat through the board without damaging the layers, though large polymer pads are preferred. This board lacks the

added width and could pose a problem once the voltage is applied.

A manufacture error resulted in a missing via (the electrical connection between PCB layers) which connects one data line, D(15), to the FPGA. It is believed that this can be worked around in the future by altering the output configuration of the ADC to reduce the measurement output resolution to 12 bits instead of 18 bits, but this was not attainable within the limited time frame.

4.3.2 Simulation results of V1.1.

The simulation of the V1.1 signal capture sub-system utilized the photodiode circuit as discussed in section 2.2.2.2. The simulation inputs were held at 50μA at a 20ns (50MHz) pulse. This was used to ensure the TIA dissipated the signal pulse adequately and there was no amplifier saturation. Note that this was not the experimental frequency used. The output seen in Figure 34 shows the amplification of 4V.

This was an adequate voltage increase, ensuring the ADC would pick up a discernable pulse from the amplification signal. The design met operational intent of this PCB and was incorporated into the PCB layout of the V1.1 board.

4.3.3 V1.1 Experimental results.

Utilizing the functional subsystems of the V1.0 boards, the V1.1 break-out amplification system was used to prove that the total PCB system indeed captured, converted and relayed signal back through the UART. The FPGA was flashed with the supporting ADC program to obtain signal output (found in Appendix D) and the PCB was attached to a USB interface to collect data using PuTTY's session log. Each run was modified to suit a number of different operating conditions detailed in Appendix E.

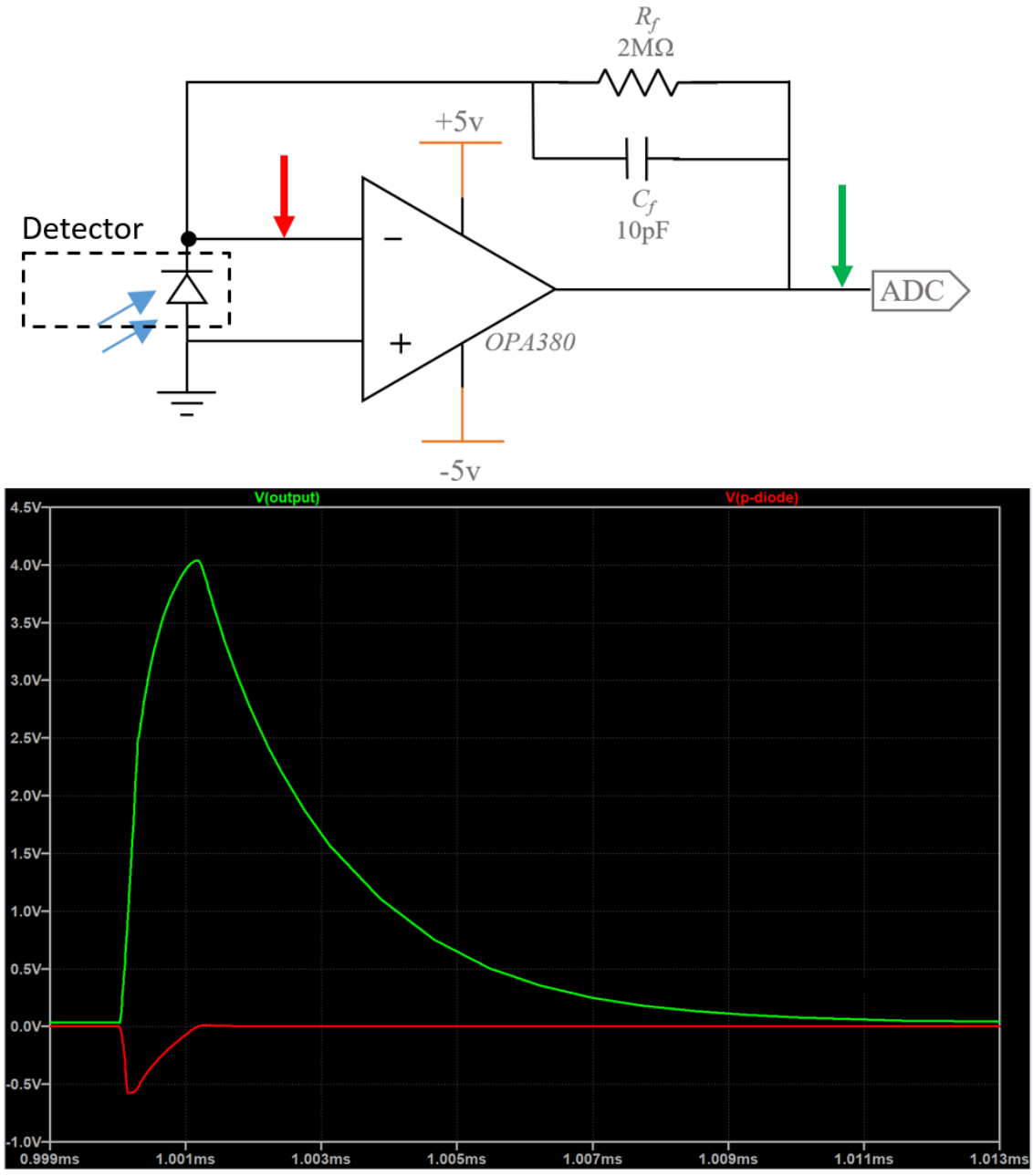


Figure 34: Simulation results utilizing the amplification configuration that will support a surrogate diode operation. Each probe is color coded on the circuit (top) to correspond with the output graph (bottom). The input voltage, seen in red is amplified to over 4V output, seen in green.

The circuit tested was the V1.1 modified breakout detailed in Appendix C which was connected via female header wires. The photodiode input device was placed before a Light Emitting Diode (LED) controlled by a Bus Pirate chopper circuit, which pulsed the LED at differing frequencies for testing. The LED was pulsed at speeds of 1kHz and 4kHz to attain output and check for noise. Note that this pulse was utilized to verify the board functionality by cycling the LED at a 50% duty cycle. This was easily covered by the sampling rate of the ADC and would be transmitted without bandwidth concerns through the UART for logging.

The resultant data, seen in Figure 35, reveals a noise floor jitter of approximately 1V but the amplifier signal output is relatively discernible. The largest signal was still over 4 Volts demonstrating that the amplified signal, even with amplifying the noise from the input, can still reveal a definite strike.

4.4 Version 1.2

The final PCB version analyzed during this research was a last minute design change of the sensor. Time constraint did not allow a revised PCB design to be implemented. Instead, the design was constructed using components placed on a breadboard to test a proof-of-concept; simulations and data collection attempts were successful.

4.4.1 Simulation results of V1.2.

For V1.2, the simulation utilizes a voltage divider circuit with a variable photo-resistor as discussed in section 3.2.2.3. This capitalized on the ability to control the source voltage and tailor the input resistor (the resistor closest to the voltage source) to accommodate the resistive value of the input detection device. Since the value of the detection sample was unknown, the assumption was made that the resistive

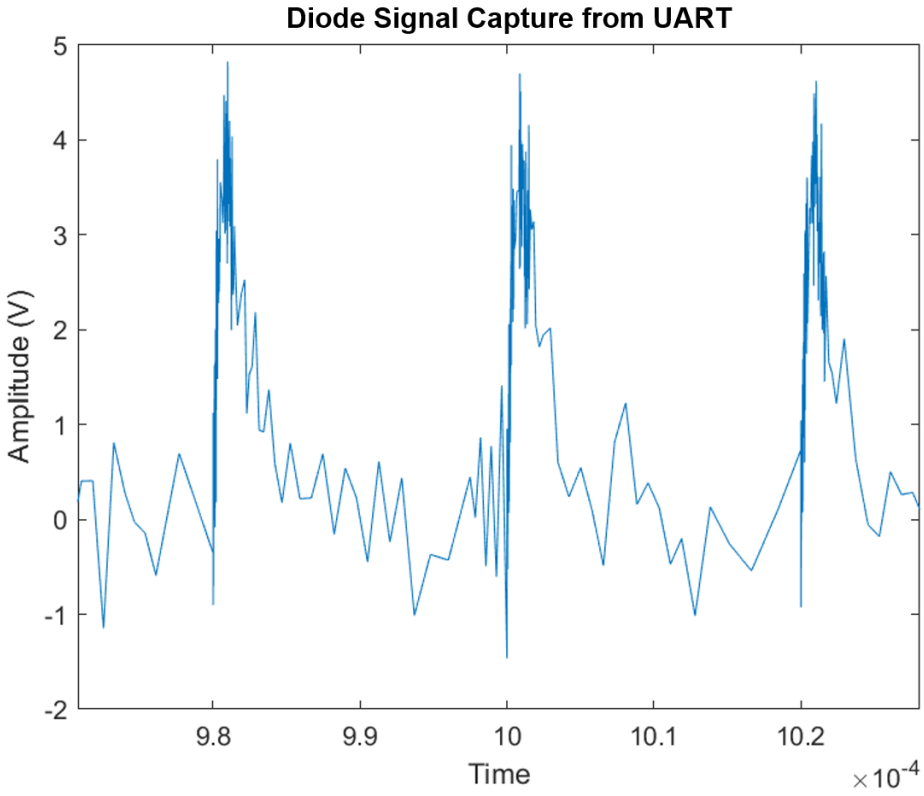


Figure 35: Version 1.1 modification data output captured by the ADC, processed by the FPGA and transmitted over UART utilizing a Bus Pirate LED chopper. This graph has been enhanced to see the wave output.

property would be small, but the behavior is analogous to the resistive properties of the stand-in device. If the photoresistor was within the 200 Ω to 730 Ω range, as seen in Figure 36, the input would not be encompassed by accompanied noise before amplification. If the resistance of the sample is greater than 730 Ω, the present circuit configuration will result in amplifier saturation.

4.4.2 V1.2 experimental results.

The FPGA remained flashed with the same ADC capture programming as the V1.1 board testing, but the circuit under test was the V1.2 photo-resistor input circuit. The circuit was set up much like the V1.1 testing and utilized a chopper at a slower 1kHz pulse for initial data collection; the results can be seen in Figure 37. Multiple runs were performed using this set-up, which can be found in Appendix E. Though a small amount of jitter can be seen, the signal follows the expected output. This jitter is likely due to the through-hole breakout board and the white-wire connections transferring the data to the ADC. Like the photodiode break-out system, the amplification system was connected using header pins.

4.5 Environmental Results

Thermal analysis, vibration testing, and radiation hardening was not accomplished on the PCBs due to delays in manufacturing and testing availability. Thermal-cycling testing was designed to ensure the system could survive the hazards within the CubeSat payload bay. It was also a method to determine if the sub-systems signal strength degraded with temperature change.

Vibration testing was desired to reveal delamination issues, or component fatigue issues that caused signal deviations or permanent damage. The vibration testing was intended to mimic real-world launch conditions, and determine if the PCB and

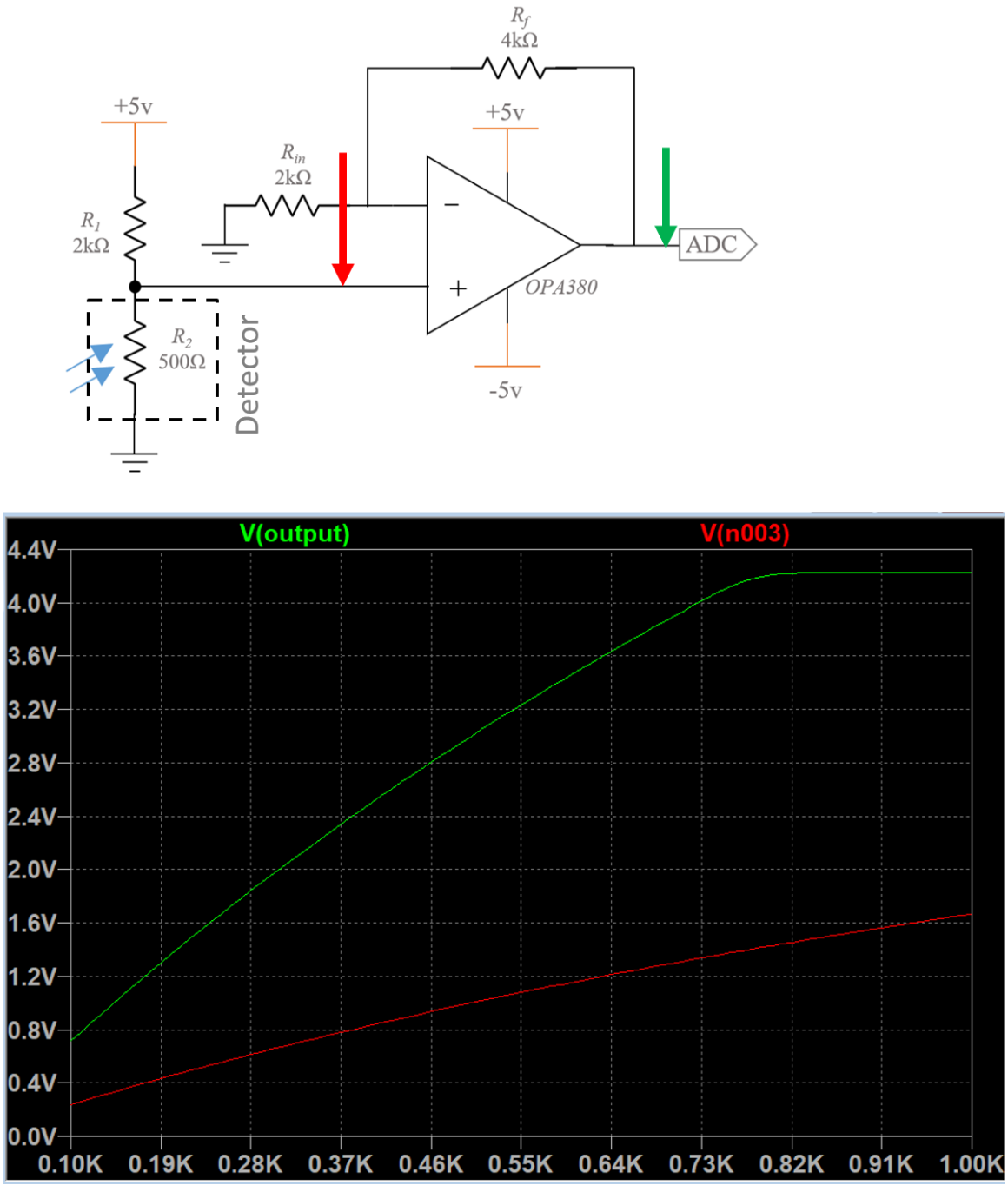


Figure 36: Simulation results utilizing the amplification configuration that will support a surrogate photoresistor operation. Each probe is color coded on the circuit (top) to correspond with the output graph (bottom). The amplification is shown as the resistor value ranges from 100Ω to 900Ω.

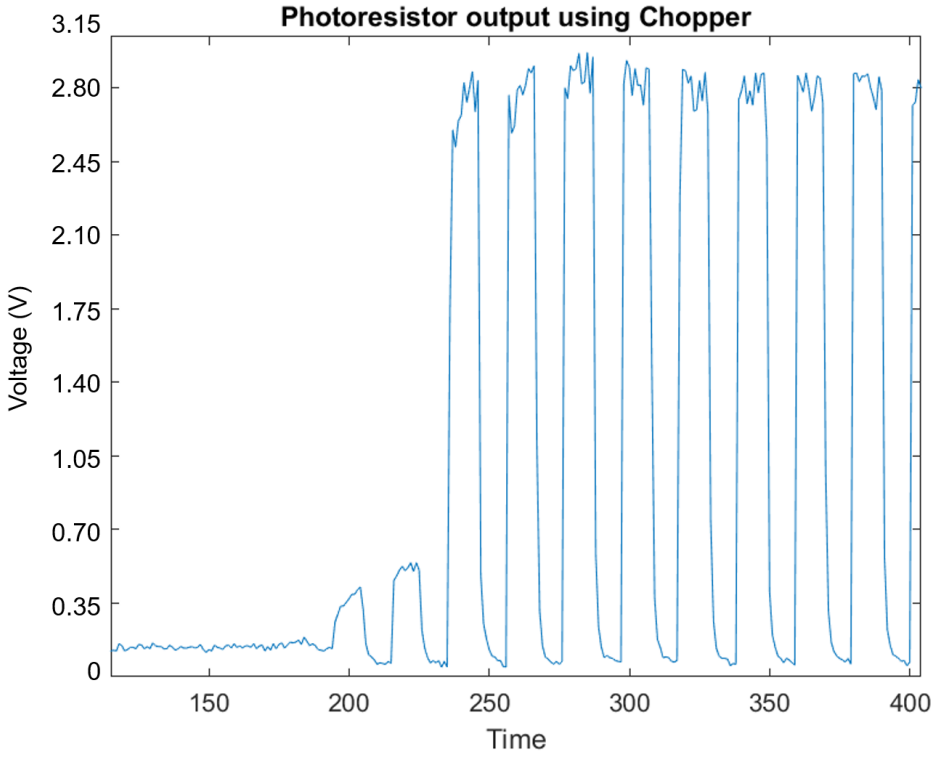


Figure 37: Version 1.2 modification LED chopper data transmitted over UART, magnified to see the signal shape and jitter. The time variable is a counter, with each tick being a 5μsecond span.

detection sample would survive and continue to function once activated by the host.

Radiation hardening was initially planned to irradiate 2 PCBs (Board 1 and Board 2) at 2 separate facilities (Board 1 testing to be handled by AFRL, and Board 2 to be tested at OSU) while a third PCB was kept as a control. The radiated boards would each be subject to two radiation doses to mimic lifetime radiation and to identify the sub-system subject to fail first. This would have identified those sub-systems that require modifications as well as the development of methods for mitigating these issues in the future. Recall that there is no minimum survival time, so ensuring the boards were capable of survival of up to a year without issues was deemed an attainable goal for a prototype. This is highly recommended in the future with both the detection sample on and off the PCB. This will show the difference between the noise generated by the board and the radiation signal produced by the sample. This will also give a relative operational life span, detailing improvements or minimum shielding desired from the host. Radiation testing would also be a good source of jitter, or noise, identification since LEO contains many types of radiation as detailed in Section 2.4. Some ICs may incur and transmit radiation induced noise, which could wash-out any captured signal from the detection sample.

V. Conclusions and Recommendations

Factors which hindered the testing and fabrication of secondary devices notwithstanding, the information amassed during this research displayed viability and may warrant further exploration. However, a number of elements will require improvement to increase the viability of the device.

5.1 Simulation and Data Conclusions

Simulation results revealed that the device is indeed functional and successful experiments accomplished goal 1 and 2; however more testing is necessary to attain goal 3. Though the input of the board for functionality is reasonably simple, this is necessary to attain environmental testing fluctuations of the signal for later analysis. This research sets the baseline of operation for these devices given their theoretical inputs.

5.1.1 V1.1 experimental results.

The system was able to successfully attain data from the surrogate device and relay it back to the user. The proof-of-concept for a detection device constrained by a small input current (from 10 to 100μA) with a duration of anything longer than a 40ns pulse will be adequately amplified by the V1.1 board. Should the pulse be faster than this, the ADC is the limiting factor and a faster, more expensive, alternative must be used. If the input current is above the 100μA threshold, the resistor and capacitor feedback values would need to be adjusted to tuned in the amplifier to fit the sample.

The signal captured from the ADC was relatively close to the simulation output, being larger in amplitude by 0.5V. This may be due to the tolerance of the power

supplies, likely outputting more that ±5V. Unfortunately, the signal was noisy but this was likely attributed to the poor connection between the V1.1 amplification break-out board and the V1.0 processing system. Noise could be generated in the two female-to-male connections supplying the amplifier with power as well as the header connection utilized for transferring the amplified signal to the ADC. To hinder this noise in the signal, it is recommended the amplification be incorporated into it's own supporting board which utilizes the filters and low impedance hardware detailed in Chapter 3. Another option may be incorporating differing frequency filters if there is an underlying jitter identified in the signal.

5.1.2 V1.2 experimental results.

The V1.2 sub-system, utilizing the tested voltage divider and feedback values, was adequately designed to accept a resistance value of 100Ω to 730Ω. When the stand-in photoresistor was pulsed at a high frequency, the captured output showed slowed dissipation voltage. If bombarded with particles, there may be a large fluctuating signal block instead of reading each pulse individually. This will still adequately point to a functional signal collector, which demonstrates proof-of-concept. However, if the resistive fluctuation were less than 100Ω between dark and emitter resistance, the amplifier would not produce a pulse and the amplification circuit would require a redesign to capture a minuscule resistive change instead.

The resultant pulse amplification came out to be approximately 2.8V, but that value is dependant on the resistive change with light intensity (explained in Chapter 2). It is possible that with a higher light source would have produced larger resistance fluctuations, but for the purpose of proof-of-concept, this experiment was adequate. Though noise was also evident in this system as well, it was less drastic, only getting up to 0.35V of noise at the worst point. This may be attributed to the type of

photoresistor used or the through-hole component tolerances which are bigger and less prone to small noise issues.

5.2 Conclusions and Significance

After testing, the V1.1 and V1.2 amplification sub-systems showed a marked improvement over the initial board simulation. Note that this board is only capable of adequate operation if the input device behaves as a diode within the 10μA to 1mA output range or a resistor from the 100Ω to 730Ω range. Anything outside of these operational ranges will need revisions of the resistor and capacitor choices to widen support bandwidth.

This device is capable of supporting device behavior constrained by the capabilities of the ADC. Since the chosen low-noise, high sampling ADC is only capable of sampling 2.5Msps, which is a 70ns sampling period, the signal being captured must be longer than this to be captured. Otherwise, the ADC may never see the change and never relay the spike to the FPGA. However, this is not to say that this is a hard-stop. Other ADCs exist that sample at higher rates, but that capability comes at a higher price tag than was available for this project.

The intent of the testing of this device was to provide a known operation baseline for a range of input types. Testing the device regarding noise fluctuation, load, and signal strength will be crucial to refining feedback variables such as the resistors, for the UO_2 detector. The known behavior of these PCBs will act as a starting point for increasing or decreasing feedback as necessary. It should be noted that each UO_2 sample, provided for this project, have failed to show consistent electrical characteristics and one sample may behave drastically different, or not at all, from another. Therefore it is possible that each PCB will need to be refined to support a unique sensor.

If given the opportunity to influence the behavior of the sample in question, the simplest device to implement into a circuit design would be a resistive-type design. Assuming it would behave with a large resistive drop over the circuit upon impact and, ideally, maintain a signal longer than 1μs, the only major supporting circuity required would be the voltage divider resister and a minor OPAMP to amplify the voltage drop. Note that this conclusion is based on the device behavior under the current, assumed parameters and any major change in resistive behavior (small resistance drop, ¡1Ω in value) would need further analysis to determine support-ability.

5.3 Recommendations

In light of the work accomplished, there are still a wide range of areas that would benefit from further testing.

5.3.1 Environmental Testing.

The PCB would benefit from environmental testing including Thermal fluctuation utilizing a TVAC system or equivalent vacuum system to mimic space. Vibration testing is also recommended to ensure the detection sample is able to survive and remain operational given the extreme abuse of space launch. Radiation testing at differing locations such as OSU's ionizing reactor, Los Alamos thermal-neutron generator, and Texas A&M's heavy ion beams provide a range of source types, subjecting both the board and sample to a wide variety of radiation particles.

Environmental testing would also identify single-point areas of failure that would benefit from redundancy. Critical failure points such as the power regulation circuits and ADC components could be easily duplicated. In this case, PCB space becomes the limiting factor, only able to support components that fit on the already complicated surface.

5.3.2 UO_2 Characteristic Envelope.

Although it may be possible to develop a more flexible platform to accommodate a myriad of functionally different sensors, the return-on-investment will be greatest if the device characteristics data are provided and a single purpose device is produced to support it. Note that it has been stated that is it possible that each sample may be drastically different, so an envelope would be needed for each sample until the manufacturing process can produce identical operational samples.

5.3.3 Complete Operation.

Testing should be performed on two final identical systems, one with a detection sample, one without. This will reveal the true operating nature of the detection sample and isolate possible PCB interference with the sample operation. This will also reveal if more filters or more input channels (from contacts interfacing the sample in different areas) are required.

5.4 Future Work

Once the sample is able to output a reliable signal on a fully functional PCB, the next step would be to focus on other features such as density sensitivity. The theory is to configure the detection samples in an array, similar to that of a solar panel, to collect particle density measurements. If the panel picks up a higher number of signals while passing over a specific area, this could trigger a "cone of interest" upon the surface that may warrant further investigation or precaution when performing operations. This will ultimately protect the warfighter from unnecessary exposure and prevent possible mass destruction.

Appendix A. Hardware specifications

1.1 Signal Capture Components

1.1.1 LT6018.

The LT6018 is Linear Technologies low noise performance precision operation amplifier. The internal structure is composed of a proprietary blend of components which offer low $1/f$ noise [23] as seen in Fig. 38.

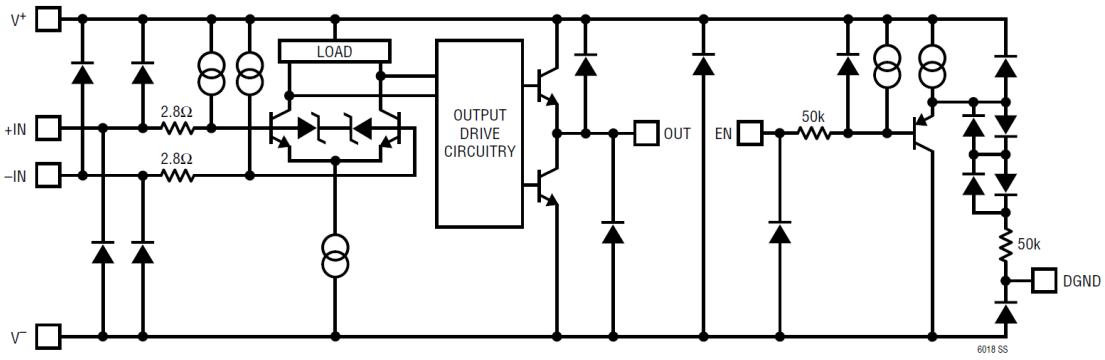


Figure 38: Internal schematic of the LT6018 functional logic [23].

This operation amplifier is specially designed to handle precision data acquisition and low noise precision signal processing. It is built to handle a supply voltage of up to 36V with an input current of ±10mA. The OPAMP has an operating temperature range of -40°C to 125°C with a survival rating between -65°C and 150°C. Linear technologies has provided a table of suggested feedback values to ensure low noise stable operation of the LT6018 as seen in Fig. 39. This was used in conjunction with simulation to determine which resistors and capacitors would provide the most desired output when going to the ADC. This was also associated with a recommended photodiode amplifier circuit, which was adapted to meet the design needs of the JFET amplification circuit design. This recommended circuit can be seen in Fig. 40.

GAIN	R_G	R_F	C_F	RTI NOISE, f = 1kHz ($nV/\sqrt{Hz}$)
2	500Ω	500Ω		2.48
2	1k	1k	5pF	3.46
2	2k	2k	5pF	5.20
5	200Ω	800Ω		2.08
10	100Ω	900Ω		1.73
101	10Ω	1k		1.27
201	5Ω	1k		1.23
201	50Ω	10k		1.51

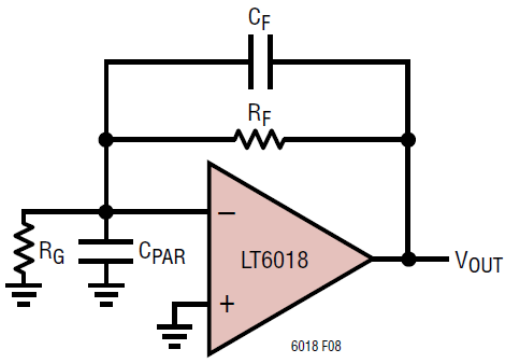


Figure 39: The suggested feedback components for low noise stable operation of the LT6018 [23].

Low Noise Extended Output Swing 1M TIA Photodiode Amplifier

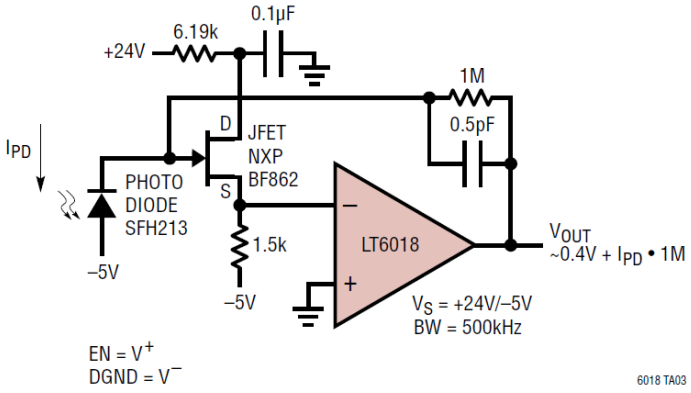


Figure 40: The recommended circuit configuration for the low noise output swing 1MΩ TIA Photodiode Amplifier. [23]

1.1.2 AD8067.

Analog Devices produced the AD8067, a high gain bandwidth fast FET OPAMP. This OPAMP is specially configured to accommodate a FET input allowing for low noise and a low input bias current of 0.6pA. It is used for applications that require high speed and low infput bias current. The common applications this OPAMP is used for are: Precision High Gain Amplifier, Photodiode amplifier, and high bandwidth composite amplifier. It is rated to operate over the industrial temperature range of 40°C to 85°C. Note that this components has an electrostatic discharge (ESD) warning, requiring the used to take proper precautions to avoid degradation or failure of the component.

1.1.3 OPA380.

The OPA380 is a high-speed, precision transimpedance amplifier with specific applications for optical amplifiers, photodiode monitoring, and precision I/V conversion. Internally, the TIA is composed of two operation amplifiers in a feedback configuration as seen in Fig. 41. This TIA converts a high frequency current input into a larger

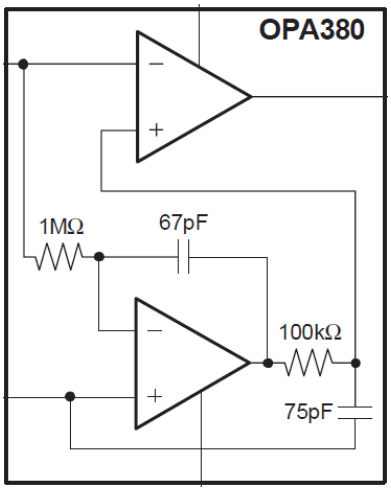


Figure 41: Internal configuration of the OPA380 Transimpedance amplifier.

magnitude voltage output.

1.1.4 LTC2389 ADC.

The Linear Technology LTC2389 is a high-speed, low-noise 18-bit ADC with 2.5Msps (samples-per-second). The ADC has a customizable bus supporting 18-bit, 16-bit, 8-bit, or Serial output. A functional block diagram can be seen in Fig. 42. It

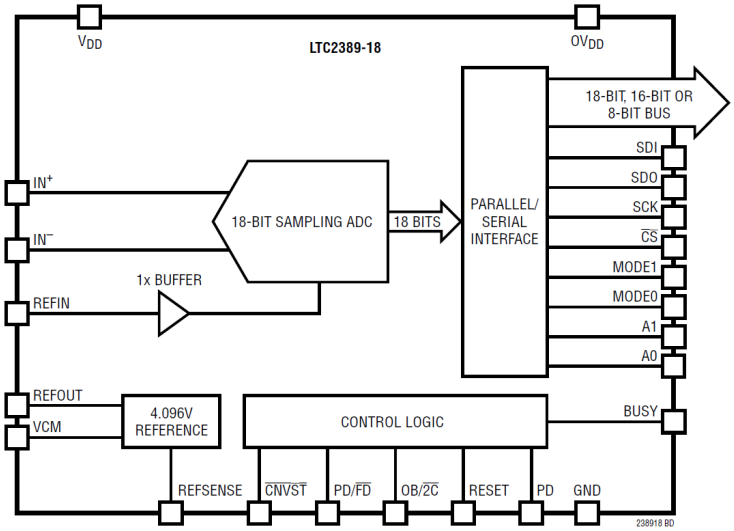


Figure 42: A conceptual block diagram representing an analog-to-digital converter which converts an input signal to binary code for use by a digital controller.

has a minimum acquisition time of 77ns utilizing the internal clock inside the IC. It is controlled by an input pulse, which begins the conversion, sending a busy flag. Once this flag clears, data can be acquired and a new conversion trigger sent.

1.1.5 ADP5052.

The ADP5052 is an Analog Devices 5-channel integrated power solution with quad buck regulators and a 200 mA LDO regulator. The regulator has a wide input range, which can support 4.5V up to 15V. The chip is rated for temperatures ranging from

-40°C to 125°C for operation temperatures, but can survive from -65°C to 150°C during storage (power off). [2]

The Buck regulators allow for four separate input voltages, eliminating the need for multiple regulation units on the same board. They also include peak current-limit protection which can be programmed to use small inductors (enabling low current applications). [2]

The ADP5052 allows for both adjustable and fixed output voltage settings. To adjust to voltage (utilized in this research) an external resistor is used to set the output voltage through a feedback reference voltage. [2] To limit the degradation of the output voltage accuracy due to feedback bias current, Analong Devices recommends that the bottom resistor in the divider is not too large. To set the voltage divider, the following equation is used:

$$V_{OUT} = V_{REF} \cdot (1 + (R_{TOP}/R_{BOTTOM}) \tag{11}$$

Where V_{OUT} is the output voltage, V_{REF} is the feedback reference voltage: 0.8 V for Channel 1-4, R_{TOP} is the feedback resistor from V_{OUT} to Feedback and R_{BOTTOM} is the feedback resistor from Feedback to ground.

Circuit board layout recommendation image can be found in Fig. 28.

Appendix B. Schematic Drawings

Altium Designer 18.1.9 (Build 240) was utilized for schematic design. Each schematic block was connected via top-level block design as pictured in Fig. 43. This block design ensured each schematic was connected in the final PCB layout.

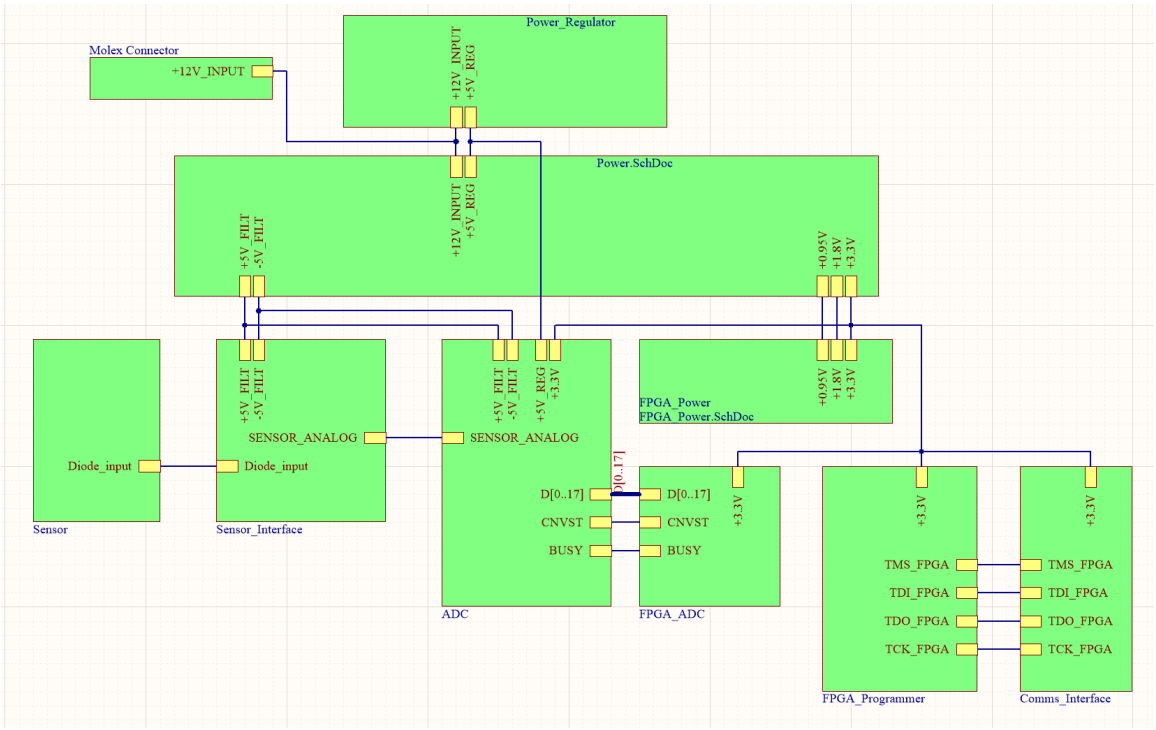


Figure 43: Block diagram showing the interface connections from one schematic to another.

The FPGA is broken into bank blocks within each schematic. The banks correspond to a section of pins within the FPGA and make it more schematic friendly.

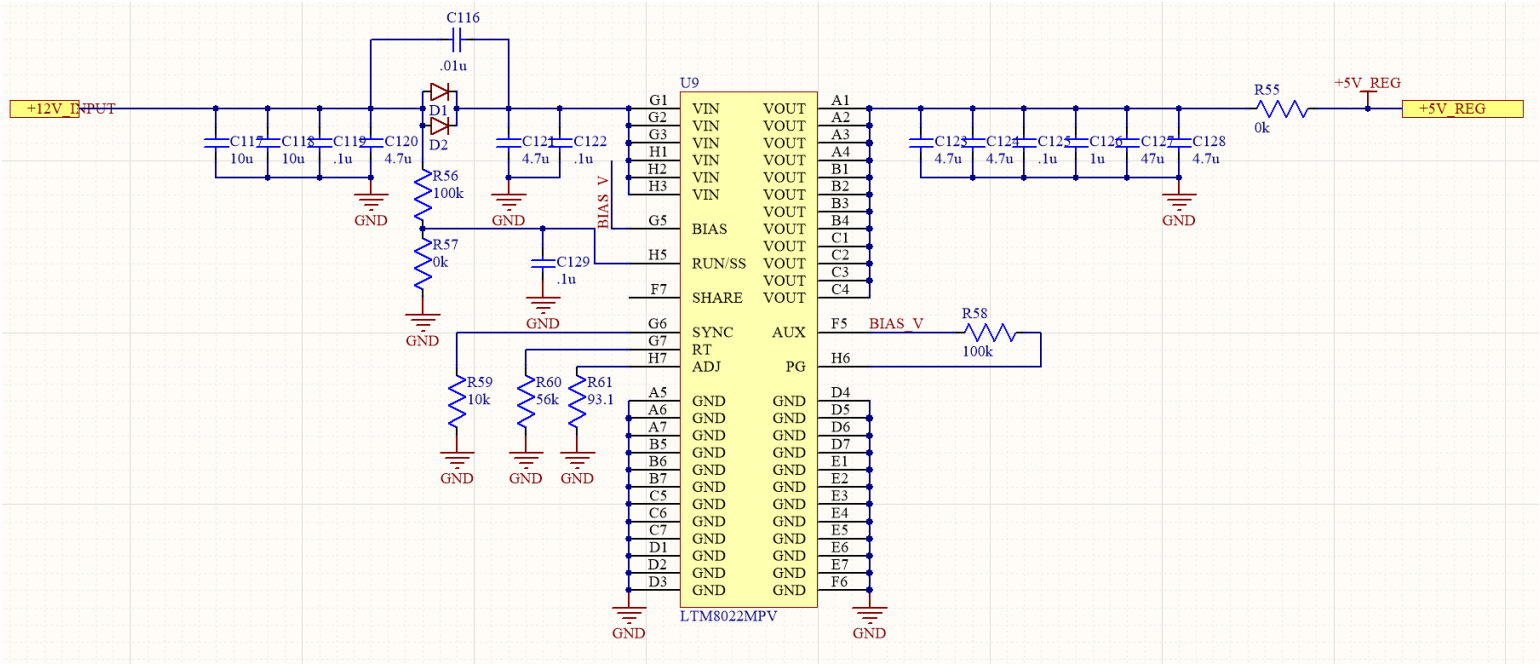


Figure 44: Schematic of the LTM8022 Voltage converter. This component drops in input voltage from the host (12V) to a 5V input for the FPGA. Refer to Appendix A for specific component information.

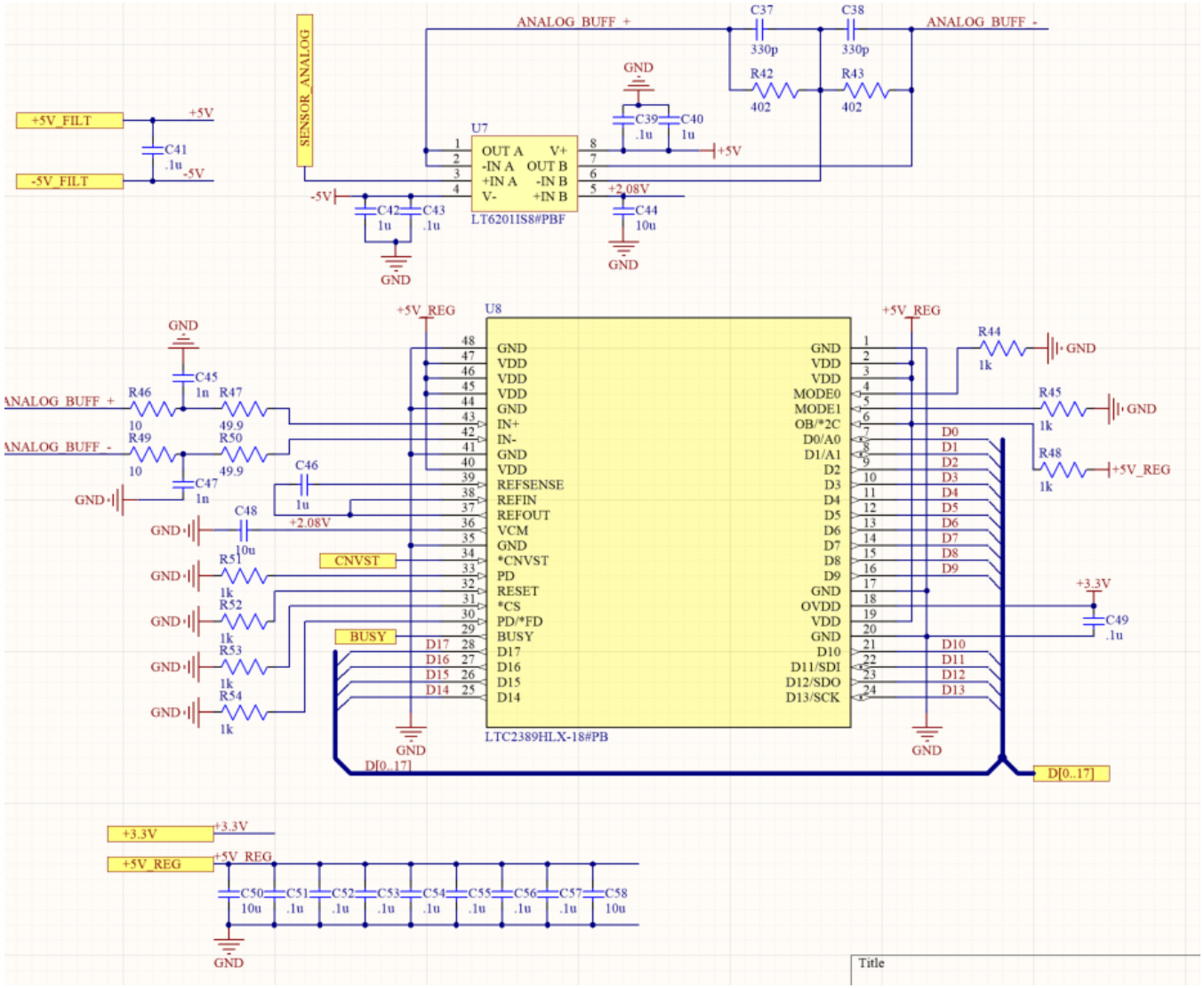


Figure 45: Schematic depicting the external LTC2389 ADC chip in the Signal Capture Sub-system. This schematic includes the LT6201 Buffer circuit and the ±5V input to drive the buffer. The output is passed through a filter before going into the ADC for capture. The 18-bit bus D(0:17) is shown to connect to the FPGA, along with the two control lines CNVST, and BUSY. The schematic also depicts the filter on the regulated 5V line to power the ADC.

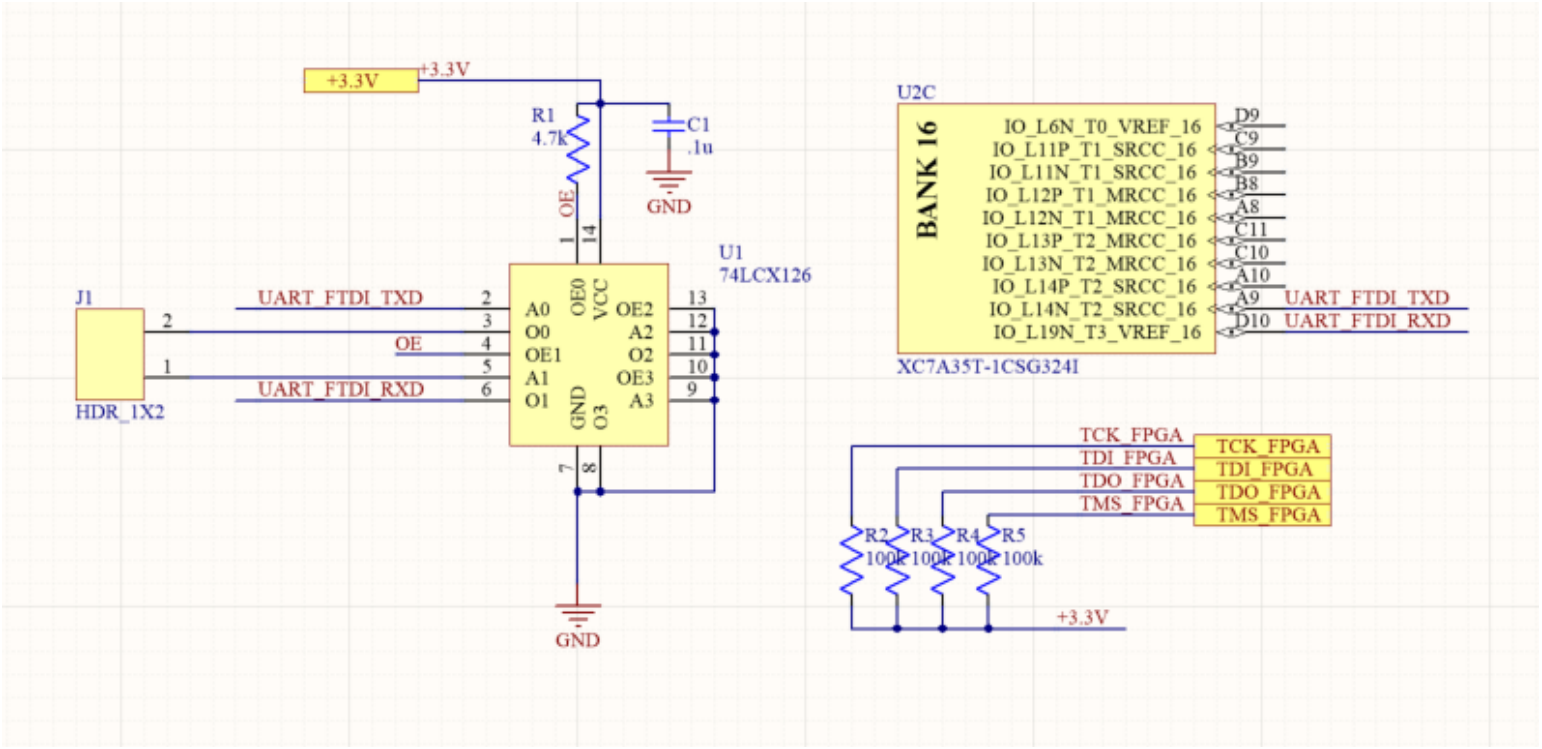


Figure 46: Pictured are the Bank16 from the FPGA which contain the UART communication lines connected to a 74LCX126 Low voltage quad buffer This buffer then forwards the signal to a 2-pin header for external communication. There are 4 FPGA voltage lines that stem from the 3.3V source generated on the schematic as well.

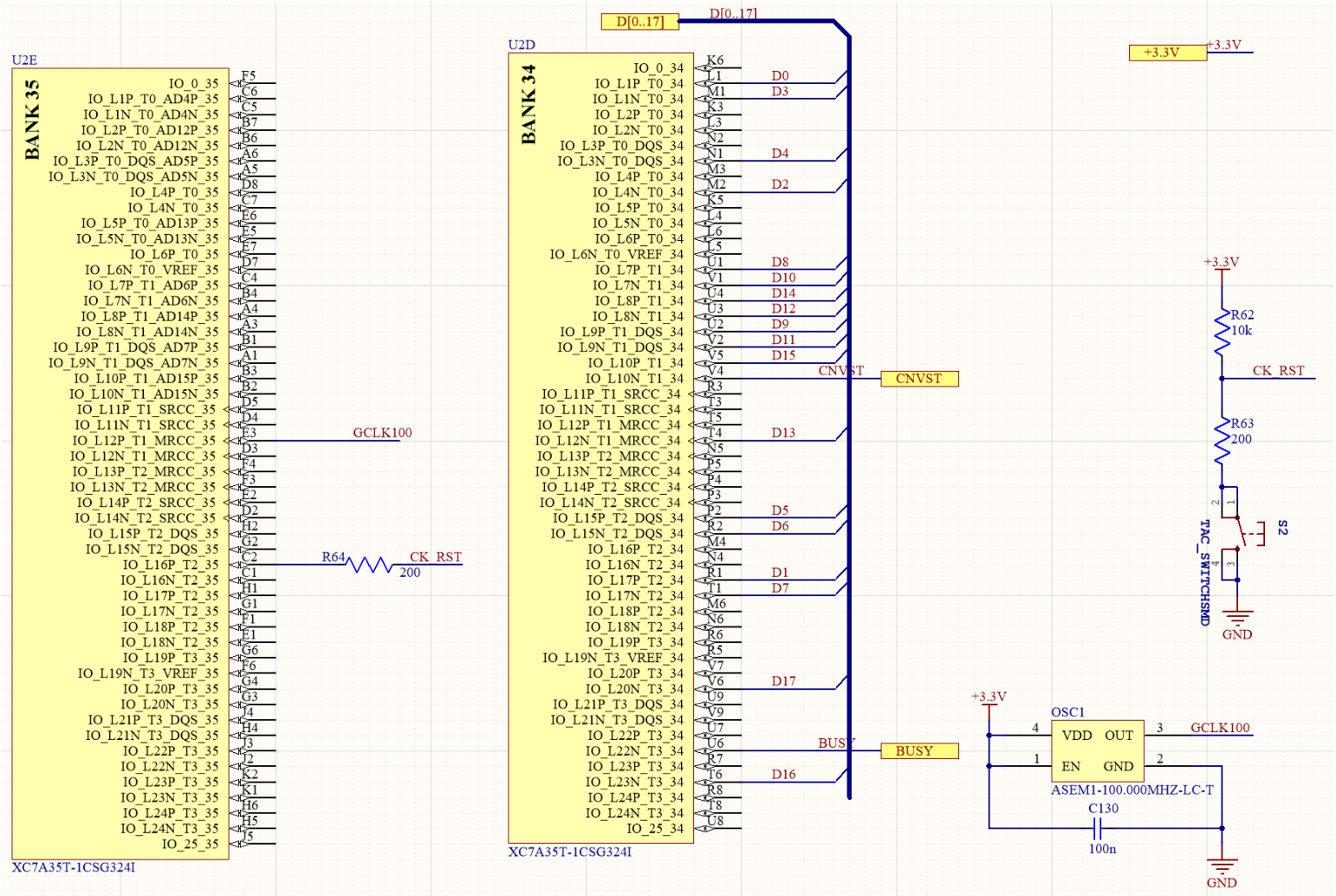


Figure 47: This schematic shows the other half of the ADC, attached to the FPGA Bank 34. Bank 35 controls the reset function and interfaces the Oscillator for timing. The reset button is shown on the right of the schematic.

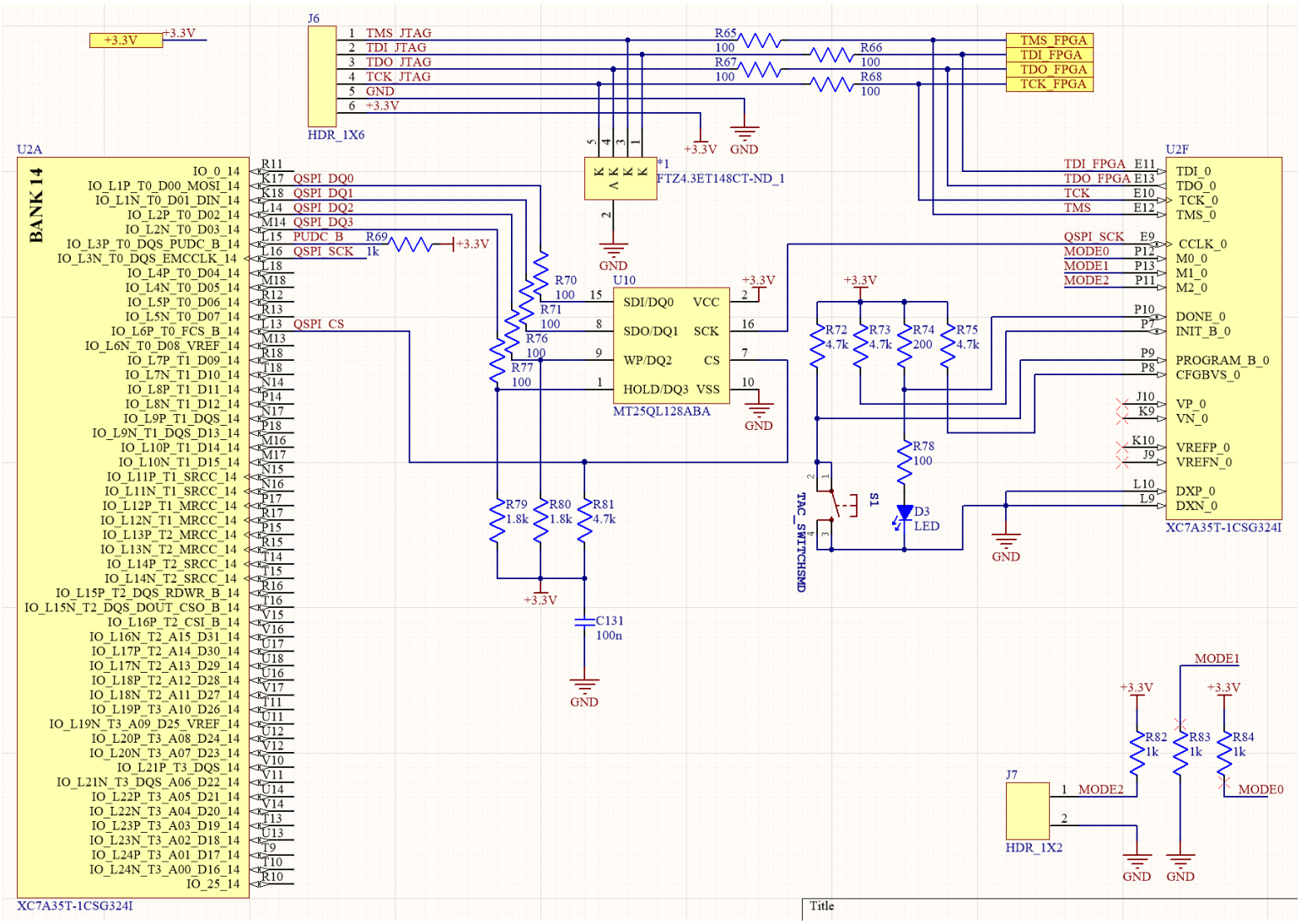


Figure 48: Schematic of the FPGA bank 14 and a programming bank, which interface the N125QL reprogramming chip. There is a programming button and LED which allow the user to confirm programming as well as reset the chip. On the top is a 6-pin header which handles the JTAG communication/programming, this is driven by the FPGA voltage lines in the Communication Figure 46. On the bottom right, there is a 2-pin header between MODE2 and ground, this allows the FPGA to either be programmed on its own, or forced the FPGA to pull the program from the SPI chip.

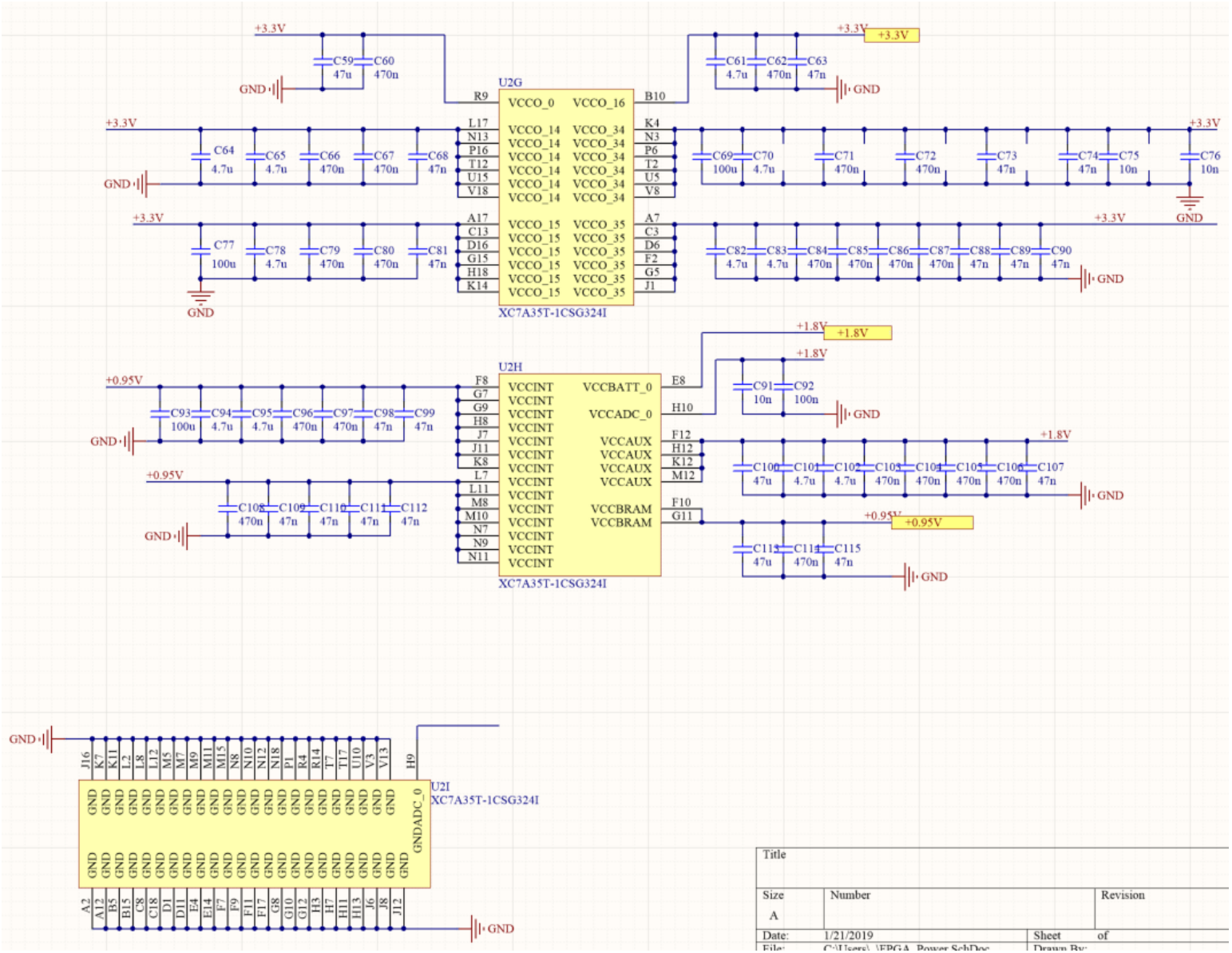


Figure 49: Schematic details the Power inputs that support the FPGA functionality. Each input voltage line is subject to a capacitor bank to reduce signal noise/jitter for a clean operation of the FPGA. The bottom left is a ground bank, which is tied to common ground.

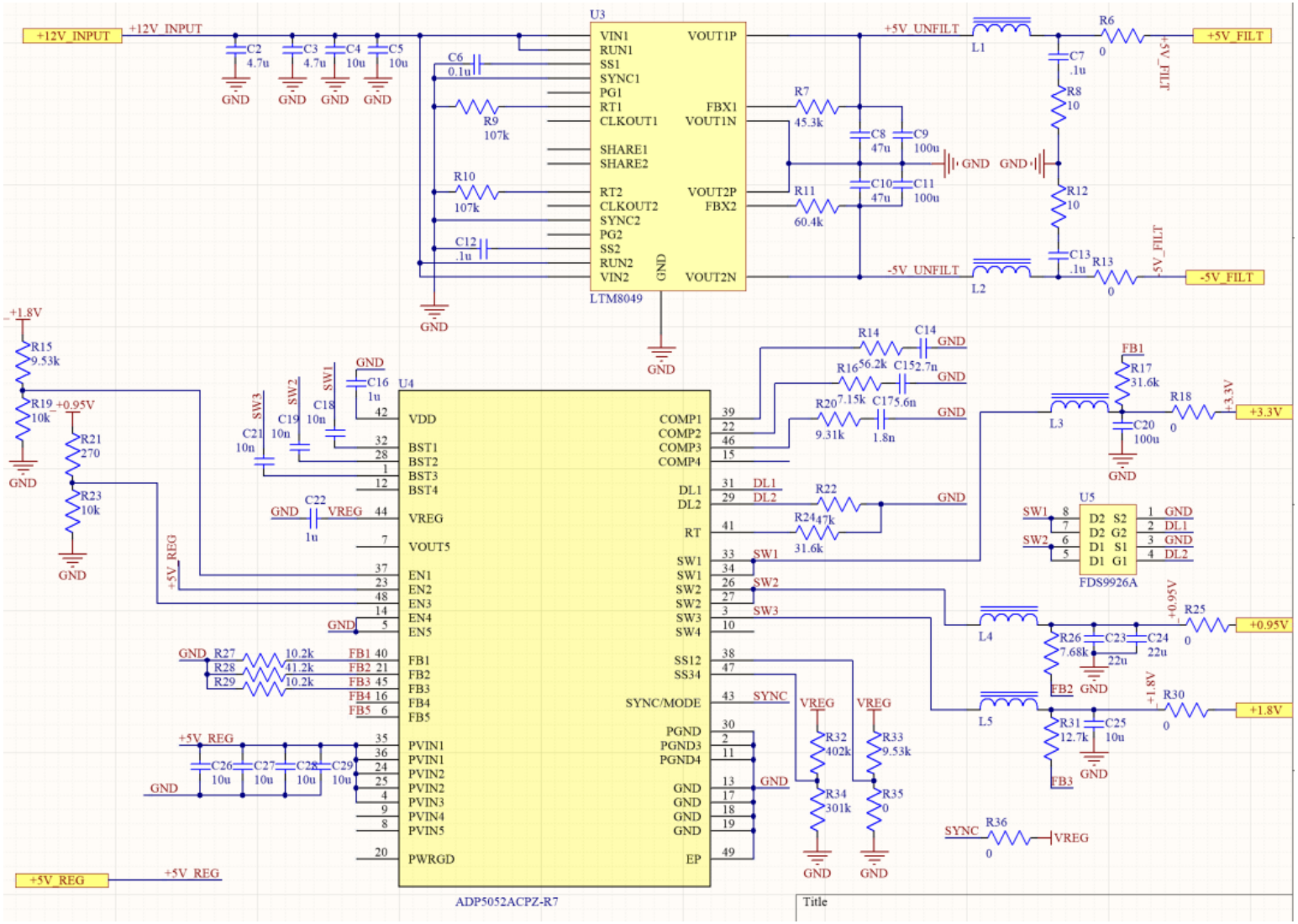


Figure 50: Schematic of the ADP5052 voltage regulator and the LTM8039 converter. The ADP5052 converts the input 5V line into the required 3.3V, 1.8V and 0.95V for FPGA functionality. The LTM8039 converts the input 12V line to the ±5V supplies. These supplies are passed through filters to reduce jitter before being utilized in the signal capture sub-system.

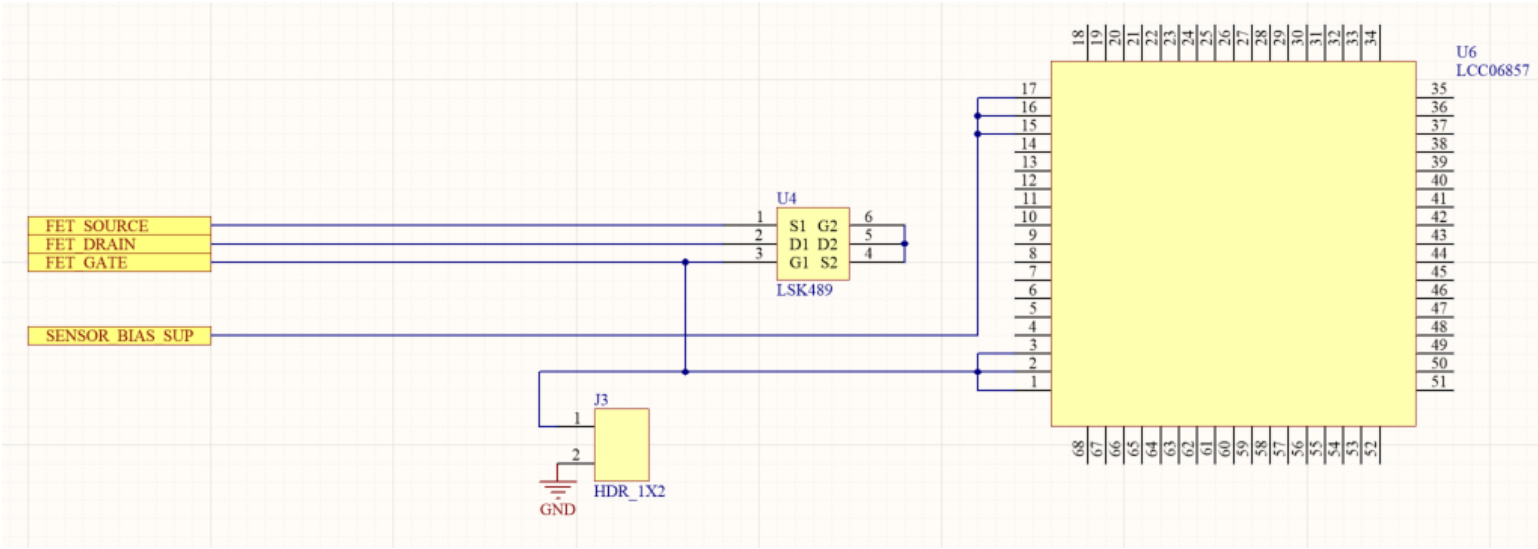


Figure 51: This schematic shows the interface between the sample and the amplification circuit for V1.0. The LCC06857 is the flatpack the sample will be adhered to. The output is then passed through a LSK489 JFET and the output sent to the amplification circuit.

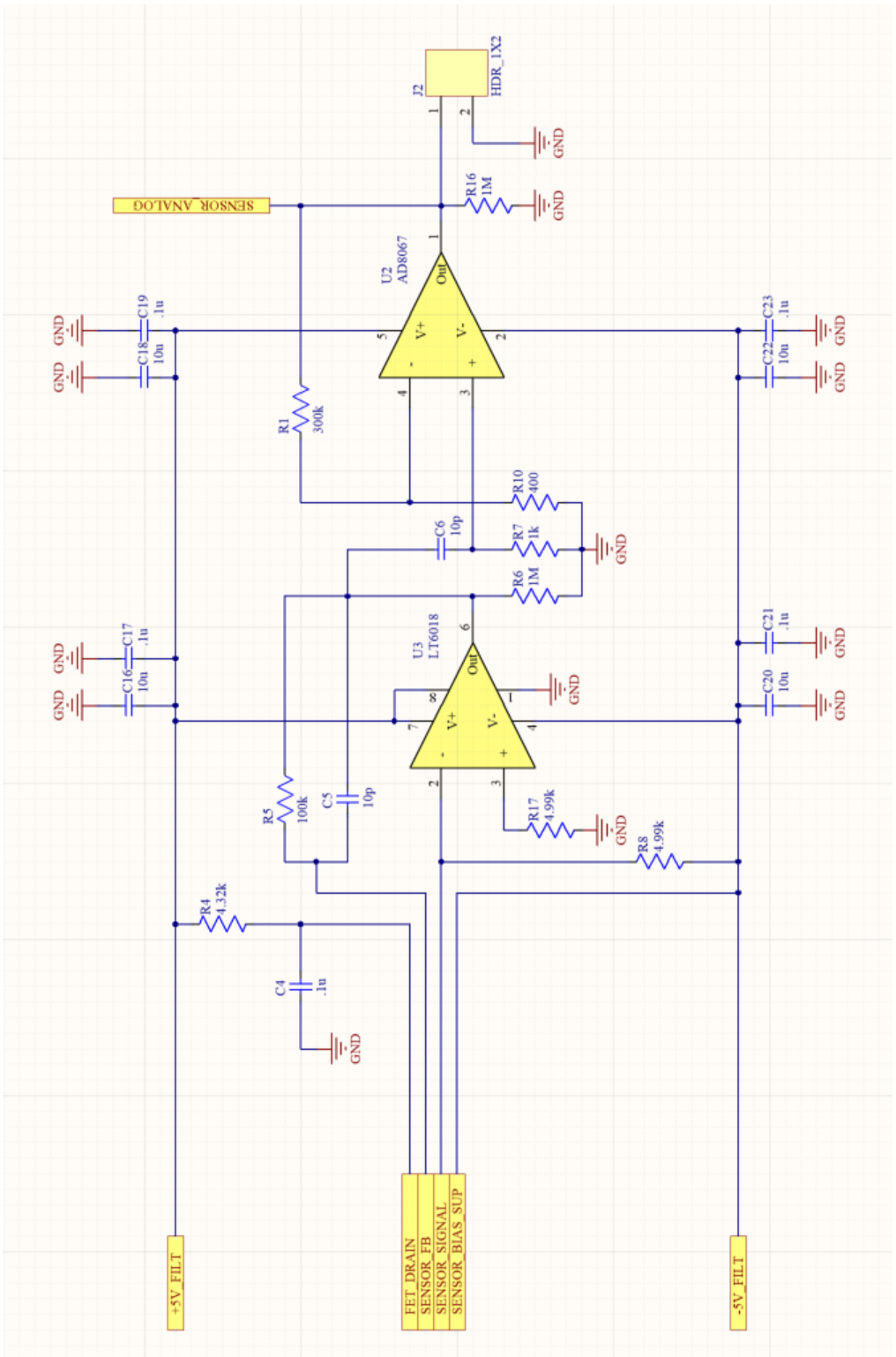


Figure 52: Schematic shows the amplification circuits for V1.0, utilizing two amplifiers as explained in Section 3.2.2.1

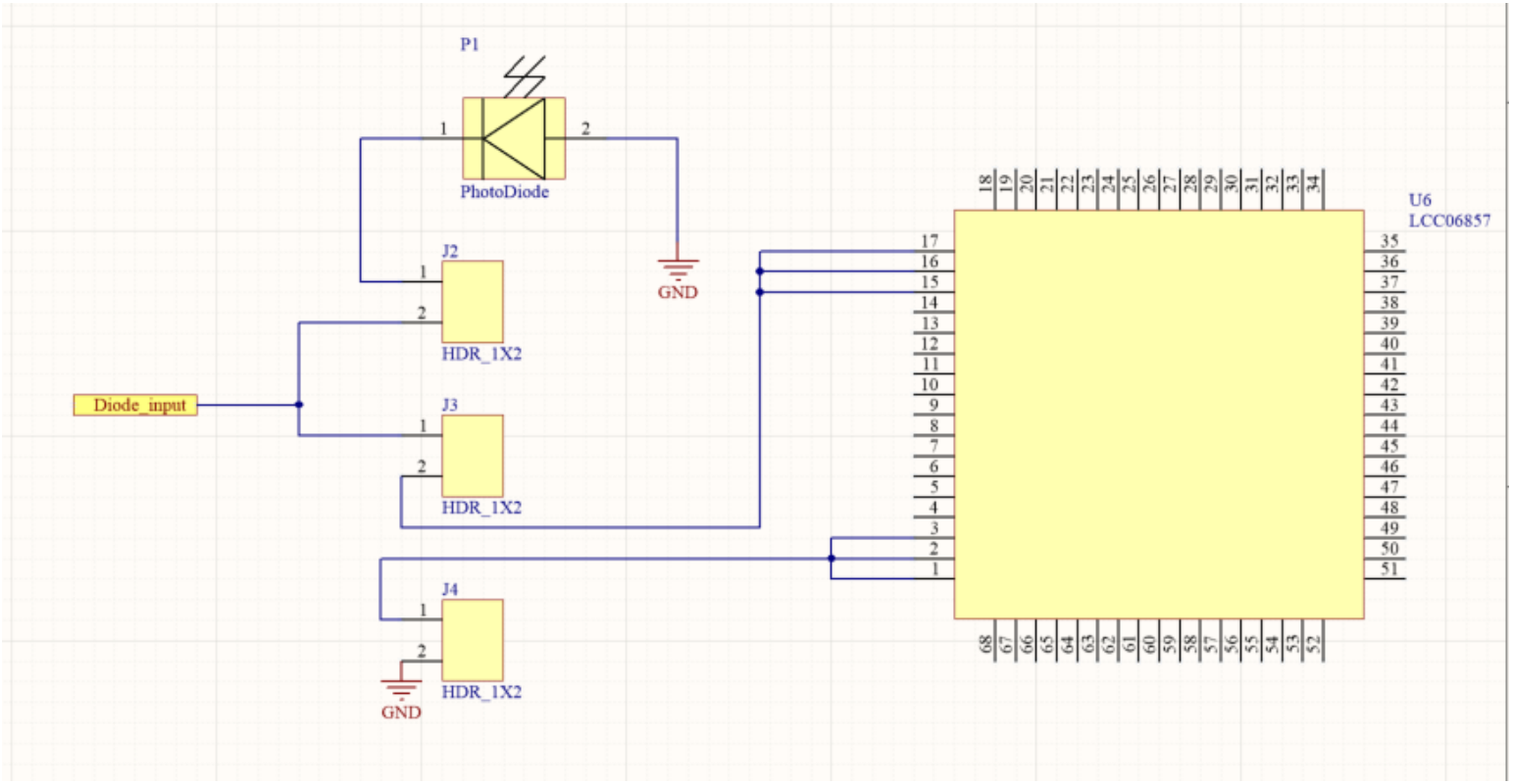


Figure 53: This schematic shows the interface between the sample and the amplification circuit for V1.1. The LCC06857 is the flatpack the Sample will be adhered to. The flatpack is then routed to a header awaiting a jumper for pass-through. This 2-pin header is a prototype component, and will be removed for flight testing. P1 is the equivalent photodiode utilized for proof-of-concept. It also requires a jumper for pass-through to allow the amplifier circuit to be utilized.

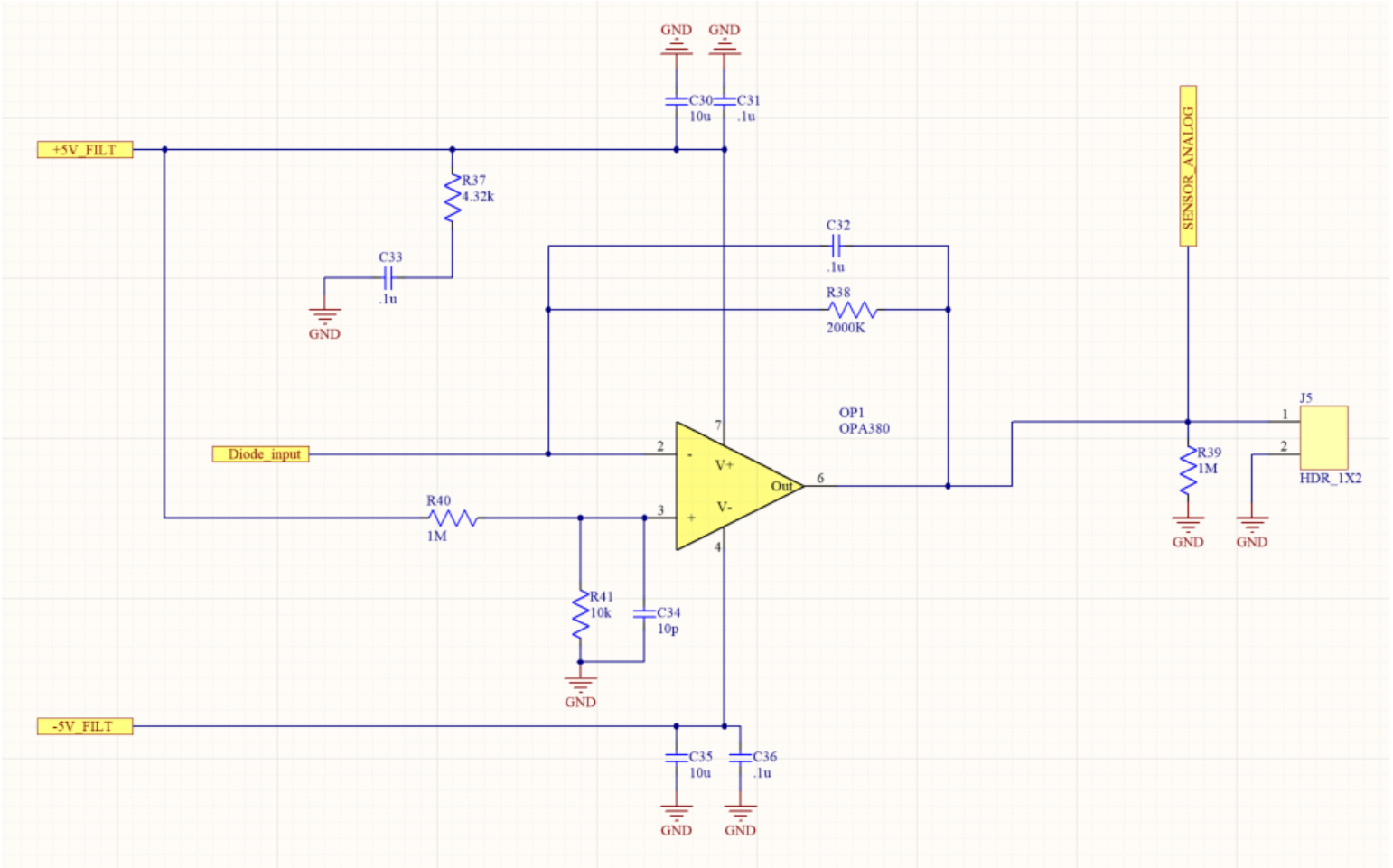


Figure 54: Schematic shows the amplification circuits for V1.1 utilizing a TIA OPA380. The reference ±5V lines are each filtered for jitter and the RC feedback ensured the TIA does not oscillate when an input is received.

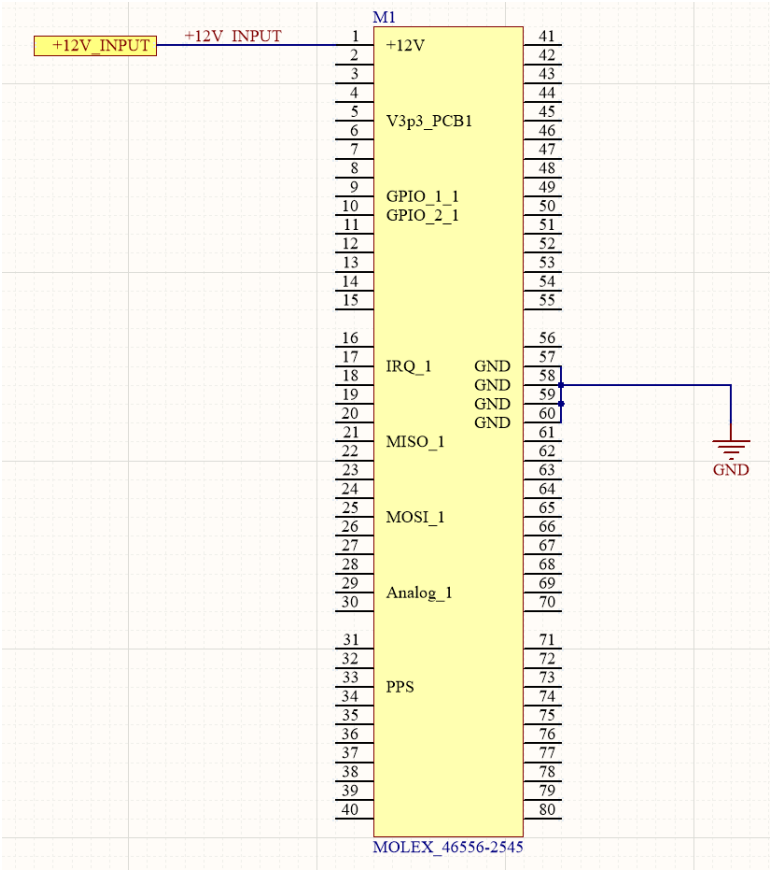
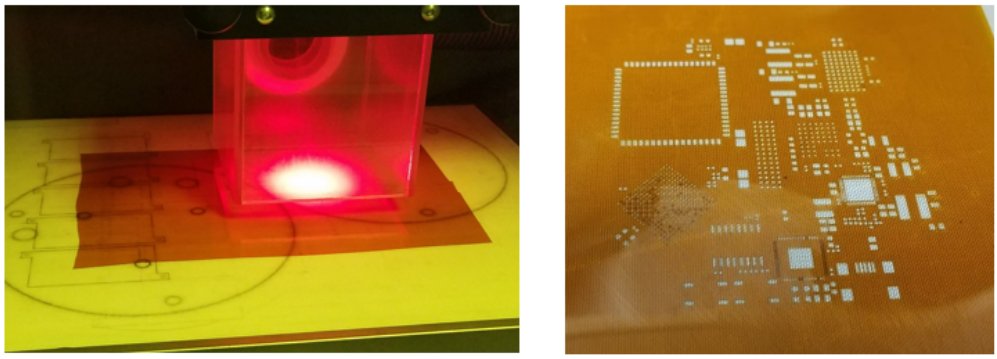


Figure 55: This is the Molex 80-pin connector required to interface the Host satellite. For proof-of-concept, the connector is placed on the board to ensure all other components are able to fit adequately. This connector provides the required 12V input and ground much like the final interface plug. The surface pads beneath each pin will have a via to transfer signal through the PCB to the following experimental payload board.

Appendix C. Fabrication and Modifications

The board after fabrication required component population. A solder mask was created utilizing the solder pad output file from Altium Designer and a laser cutter. The complete solder mask can be seen in Fig. 56. Once the mask is adhered to the



(a) Laser cutting mask (b) Complete Solder mask

Figure 56: Photo of the (a) laser cutting a solder mask and (b) the completed mask. The mask is adhered to the PCB using a removable tape while a light coating of solder is spread over the film. The thickness of the film is approximately 0.4 mm which gives ample solder to adhere components during solder-flow during bake.

PCB, a layer of solder is spread over the holes, and the mask is then removed leaving the pads soldered and ready for components. For the IC components careful alignment by the surface mount technology (SMT) component placement system (pictured in Fig. 57) at AFIT was required. The system aligned the bottom pads with the board solder with the use of an optical camera overlay, and placed the parts precisely for solder flow. There were 3 components, including the very tightly spaced FPGA that the SMT placement system was used for.

Each component is placed onto the solder over their designated pads before the PCB is then heated to 225°C to achieve solder flow and adhere to components to the

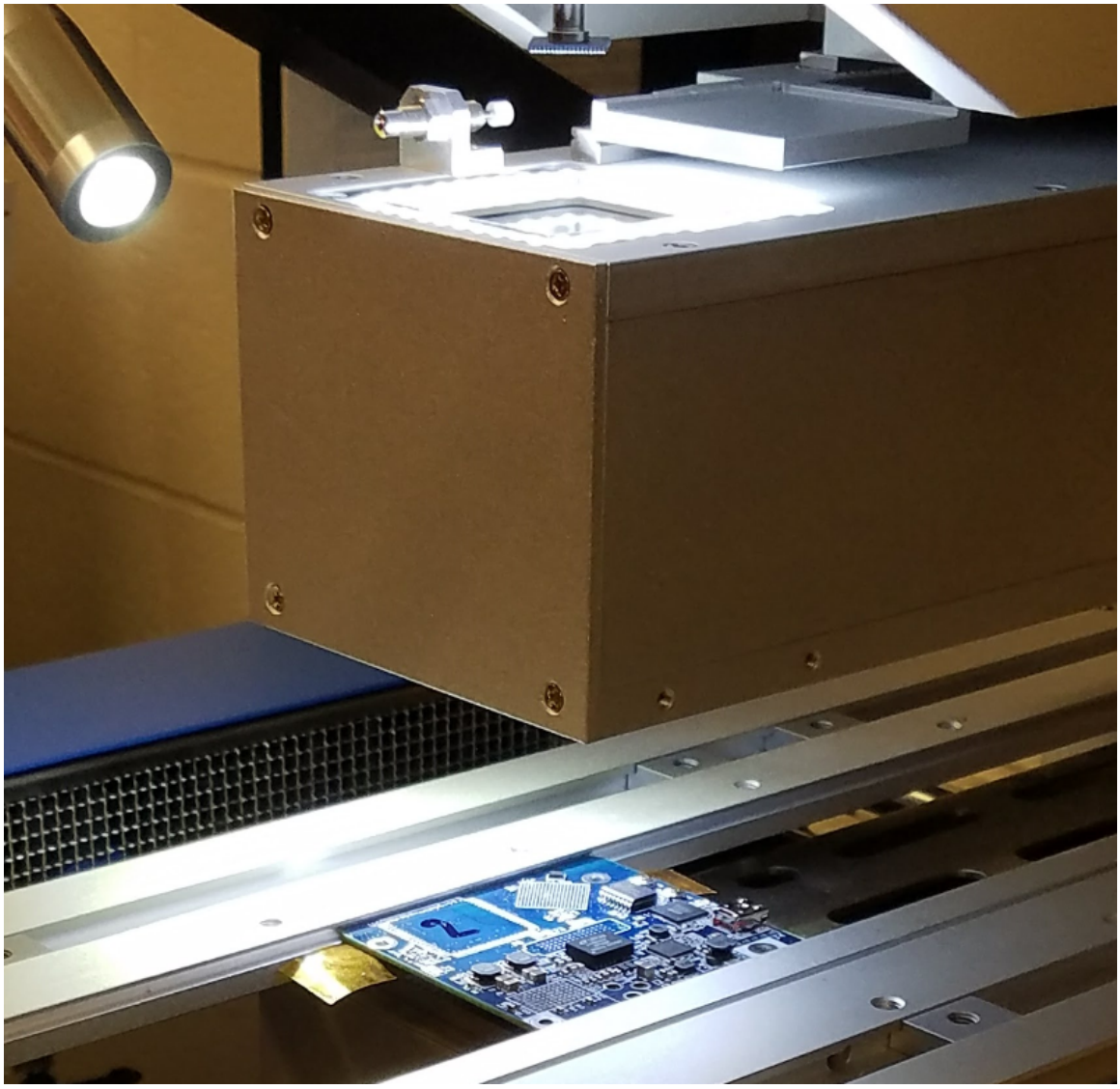


Figure 57: Photo showing the SMT component placement system aligning the FPGA to the correct place upon the board before setting it in place.

PCB. Once this is accomplished, the boards are ready for subsystem testing. The V1.0 boards can be seen in Fig. 32 post solder flow in section 4.2.

3.0.1 V1.1 modifications.

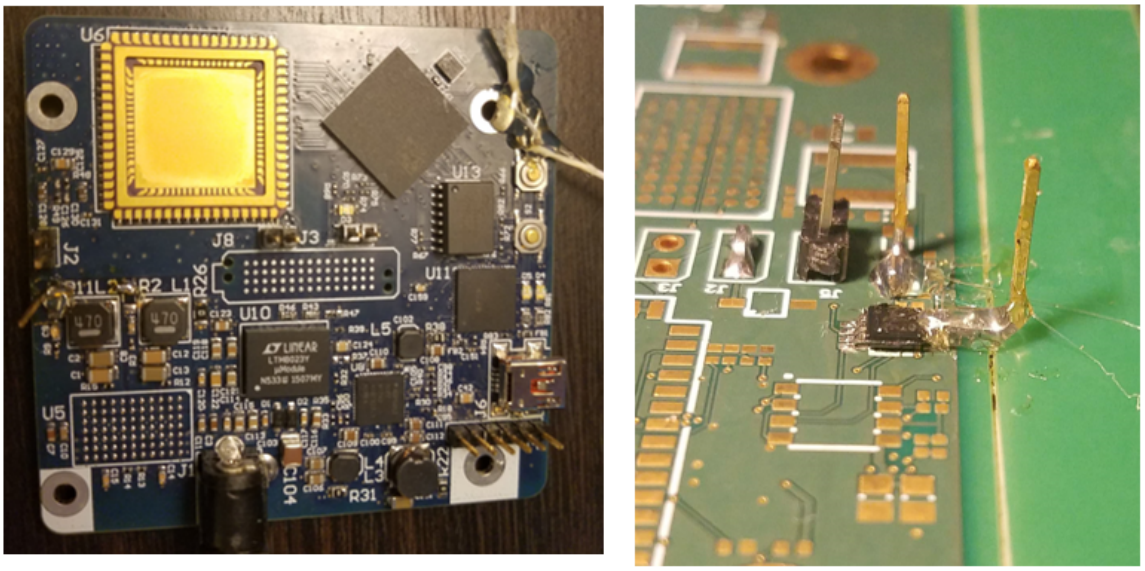
To convert the V1.0 Board to accommodate the V1.1 amplification system, the following modifications were required of the V1.0 Boards. This was accomplished on V1.0 board three due to missing components on board two and board one being utilized at AFRL.

The following components need to be removed completely: R12, R1, R10, C6, C5, U2. A number of other components need to be replaced to allow functionality of the V1.1 breakout boards, these replacements can be seen in Table 5.

Table 5: Components replacement table to convert the V1.0 boards to the V1.1 campatable system.

Remove	**Add**	**Remove**	**Add**
R38	2MΩ	C32	1pF
R40	10kΩ	C34	1pF
R41	Short to GND	U3	OPA380
R39	10kΩ	C5	1pF
R17	(Stacked) 5kΩ	R17	1pF (stacked)

Once these component replacements are complete, the UART connections to the USB must be severed by cutting the traces on the top layer. Wires were soldered to the to allow UART communication to be interfaced during TVAC testing. This modification can be seen in Fig. 58.



(a) Modified V1.0 PCB (b) Modified Breakout V1.1

Figure 58: Image showing the external lines that provide the V1.0 PCB with the ±5V input and UART out for data collection.

Appendix D. Software specifications

The software controller utilizes two interface programs to acquire a signal from the detector sample as explained in Section 3.3. Below is the reference table connecting the data lines from the ADC to the FPGA. This corresponds to the C code to interface the FPGA. There are three separate batches of Code presented in this section: Vivado

Table 6: Corresponding Data and control lines from the ADC and their corresponding FPGA input pad. These are used to program a configuration file for input/output handling in the FPGA.

ADC	FPGA	ADC	FPGA	ADC	FPGA
D0	L1	D9	U2	CNVST	V4
D1	R1	D10	V1	BUSY	U6
D2	M2	D11	V2		
D3	M1	D12	U3		
D4	N1	D13	T4		
D5	P2	D14	V4		
D6	R2	D15	V5		
D7	T1	D16	T6		
D8	U1	D17	V6		

constraint files, XADC internal ADC C code, and External ADC interface code.

4.0.1 Constraint Code for interfacing the FPGA.

```
##ChipKit Signals
set_property -dict { PACKAGE_PIN C5    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux4_v_n }]; #IO_L1N_T0_AD4N_35 Sch=ck_an_n[0]
set_property -dict { PACKAGE_PIN C6    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux4_v_p  }]; #IO_L1P_T0_AD4P_35 Sch=ck_an_p[0]
set_property -dict { PACKAGE_PIN A5    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux5_0_v_n  }]; #IO_L3N_T0_DQS_AD5N_35 Sch=ck_an_n[1]
set_property -dict { PACKAGE_PIN A6    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux5_0_v_p  }]; #IO_L3P_T0_DQS_AD5P_35 Sch=ck_an_p[1]
set_property -dict { PACKAGE_PIN B4    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux6_0_v_n  }]; #IO_L7N_T1_AD6N_35 Sch=ck_an_n[2]
set_property -dict { PACKAGE_PIN C4    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux6_0_v_p  }]; #IO_L7P_T1_AD6P_35 Sch=ck_an_p[2]
set_property -dict { PACKAGE_PIN A1    IOSTANDARD LVCMOS33 }
        [get_ports { Vaux7_0_v_n  }]; #IO_L9N_T1_DQS_AD7N_35 Sch=ck_an_n[3]
```

```
16  set_property -dict { PACKAGE_PIN B1    IOSTANDARD LVCMOS33 }
17          [get_ports { Vaux7_0_v_p  }]; #IO_L9P_T1_DQS_AD7P_35 Sch=ck_an_p[3]
18  set_property -dict { PACKAGE_PIN C14   IOSTANDARD LVCMOS33 }
19          [get_ports { Vaux0_v_n  }]; #IO_L1N_T0_AD0N_15 Sch=ck_an_n[5]
20  set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 }
21          [get_ports { Vaux0_v_p  }]; #IO_L1P_T0_AD0P_15 Sch=ck_an_p[5]
22
23  set_property -dict { PACKAGE_PIN J10    IOSTANDARD LVCMOS33 }
24          [get_ports {  Vp_Vn_v_p }];
25  set_property -dict { PACKAGE_PIN K9     IOSTANDARD LVCMOS33 }
26          [get_ports {  Vp_Vn_v_n }];
27
28  # ChipKit Digital I/O On Inner Analog Header
29  # Note: These pins will need to be connected to the XADC
30  # core when used as differential analog inputs (Chipkit analog pins A6-A11)
31
32  set_property -dict { PACKAGE_PIN B7    IOSTANDARD LVCMOS33 }
33      [get_ports { ck_an_p[6]}]; #IO_L2P_T0_AD12P_35 Sch=ad_p[12]
34  set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 }
35      [get_ports { ck_an_n[6] }]; #IO_L2N_T0_AD12N_35 Sch=ad_n[12]
36  set_property -dict { PACKAGE_PIN E6    IOSTANDARD LVCMOS33 }
37      [get_ports { ck_an_p[7] }]; #IO_L5P_T0_AD13P_35 Sch=ad_p[13]
38  set_property -dict { PACKAGE_PIN E5    IOSTANDARD LVCMOS33 }
39      [get_ports { ck_an_n[7] }]; #IO_L5N_T0_AD13N_35 Sch=ad_n[13]
40  set_property -dict { PACKAGE_PIN A4    IOSTANDARD LVCMOS33 }
41      [get_ports { ck_an_p[8] }]; #IO_L8P_T1_AD14P_35 Sch=ad_p[14]
42  set_property -dict { PACKAGE_PIN A3    IOSTANDARD LVCMOS33 }
43      [get_ports { ck_an_n[8]  }]; #IO_L8N_T1_AD14N_35 Sch=ad_n[14]
44
45  #External ADC Interface
46  set_property -dict {PACKAGE_PIN L1 IOSTANDARD LVCMMOS33}
47      [get_ports {D[0]}
48  set_property -dict {PACKAGE_PIN R1 IOSTANDARD LVCMMOS33}
49      [get_ports {D[1]}
50  set_property -dict {PACKAGE_PIN M2 IOSTANDARD LVCMMOS33}
51      [get_ports {D[2]}
52  set_property -dict {PACKAGE_PIN M1 IOSTANDARD LVCMMOS33}
53      [get_ports {D[3]}
54  set_property -dict {PACKAGE_PIN N1 IOSTANDARD LVCMMOS33}
55      [get_ports {D[4]}
56  set_property -dict {PACKAGE_PIN P2 IOSTANDARD LVCMMOS33}
57      [get_ports {D[5]}
58  set_property -dict {PACKAGE_PIN R2 IOSTANDARD LVCMMOS33}
59      [get_ports {D[6]}
60  set_property -dict {PACKAGE_PIN T1 IOSTANDARD LVCMMOS33}
61      [get_ports {D[7]}
62  set_property -dict {PACKAGE_PIN U1 IOSTANDARD LVCMMOS33}
63      [get_ports {D[8]}
64  set_property -dict {PACKAGE_PIN U2 IOSTANDARD LVCMMOS33}
65      [get_ports {D[9]}
66  set_property -dict {PACKAGE_PIN V1 IOSTANDARD LVCMMOS33}
67      [get_ports {D[10]}
68  set_property -dict {PACKAGE_PIN V2 IOSTANDARD LVCMMOS33}
69      [get_ports {D[11]}
```

```
set_property -dict {PACKAGE_PIN U3 IOSTANDARD LVCMMOS33}
    [get_ports {D[12]}
set_property -dict {PACKAGE_PIN T4 IOSTANDARD LVCMMOS33}
    [get_ports {D[13]}
set_property -dict {PACKAGE_PIN V4 IOSTANDARD LVCMMOS33}
    [get_ports {D[14]}
set_property -dict {PACKAGE_PIN V5 IOSTANDARD LVCMMOS33}
    [get_ports {D[15]}
set_property -dict {PACKAGE_PIN T6 IOSTANDARD LVCMMOS33}
    [get_ports {D[16]}
set_property -dict {PACKAGE_PIN V6 IOSTANDARD LVCMMOS33}
    [get_ports {D[17]}

set_property -dict {PACKAGE_PIN V4 IOSTANDARD LVCMMOS33}
    [get_ports {CNVST}
set_property -dict {PACKAGE_PIN U6 IOSTANDARD LVCMMOS33}
    [get_ports {BUSY}
```

4.0.2 Demonstration code for the internal FPGA ADC utilizing the Arty board.

```
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
#include "xsysmon.h"
#include "xparameters.h"
#include "sleep.h"

#define SYSMON_DEVICE_ID  XPAR_SYSMON_0_DEVICE_ID
#define XSysMon_RawToExtVoltage(AdcData)
        ((((float)(AdcData))*(1.0f))/65536.0f)

static XSysMon SysMonInst;
static int SysMonFractionToInt(float FloatNum);

int main()
{
        u32 TempRawData,VccIntRawData,ExtVolRawData;
        float TempData,VccIntData,ExtVolData;
        int xStatus;
        XSysMon_Config *SysMonConfigPtr;
        XSysMon *SysMonInstPtr =&SysMonInst;

    init_platform();

    SysMonConfigPtr = XSysMon_LookupConfig(SYSMON_DEVICE_ID);
    if(SysMonConfigPtr == NULL) printf("Lookupconfig_FAILURE\n\r");

    xStatus = XSysMon_CfgInitialize(SysMonInstPtr, SysMonConfigPtr,
                SysMonConfigPtr->BaseAddress);
    if(XST_SUCCESS !=xStatus) printf("CfgInitialize_FAILURE\n\r");
    XSysMon_GetStatus(SysMonInstPtr);

```

```
33      while(1)
34      {
35          while((XSysMon_GetStatus(SysMonInstPtr)& XSM_SR_EOS_MASK) != XSM_SR_EOS_MASK);
36
37              TempRawData = XSysMon_GetAdcData(SysMonInstPtr,XSM_CH_TEMP);
38              TempData = XSysMon_RawToTemperature(TempRawData);
39              printf("\r\nThe Current Temp is %0d.%03d Celsius.\r\n",(int)(TempData),
40                      SysMonFractionToInt(TempData));
41
42          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN+4);
43          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
44          printf("The Current Vaux4 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
45                  SysMonFractionToInt(ExtVolData));
46          usleep(500000);
47
48          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN+5);
49          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
50          printf("The Current Vaux5 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
51                  SysMonFractionToInt(ExtVolData));
52          usleep(500000);
53
54          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN+6);
55          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
56          printf("The Current Vaux6 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
57                  SysMonFractionToInt(ExtVolData));
58          usleep(500000);
59          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN+8);
60          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
61          printf("The Current Vaux8 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
62                  SysMonFractionToInt(ExtVolData));
63          usleep(500000);
64
65          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN+15);
66          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
67          printf("The Current Vaux15 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
68                  SysMonFractionToInt(ExtVolData));
69          usleep(500000);
70
71          ExtVolRawData = XSysMon_GetAdcData(SysMonInstPtr, XSM_CH_AUX_MIN);
72          ExtVolData = XSysMon_RawToExtVoltage(ExtVolRawData);
73          printf("The Current Vaux0 is %0d.%03d Volts. \r\n", (int)(ExtVolData),
74                  SysMonFractionToInt(ExtVolData));
75          usleep(5000000);
76          }
77      cleanup_platform();
78      return 0;
79  }
80
81  int SysMonFractionToInt(float FloatNum)
82      {
83          float Temp;
84          Temp = FloatNum;
85          if(FloatNum <0){
86                  Temp = -(FloatNum);
```

```
87          }
88          return ( ((int)((Temp -(float)((int)Temp)) *(1000))));
89  }
```

Appendix E. Signal output

As explained in Section 4.3.3, a Bus Pirate was utillized as a chopper circuit to generate an input for functional testing. An image of the Bus Pirate generator can be seen in Figure 59.

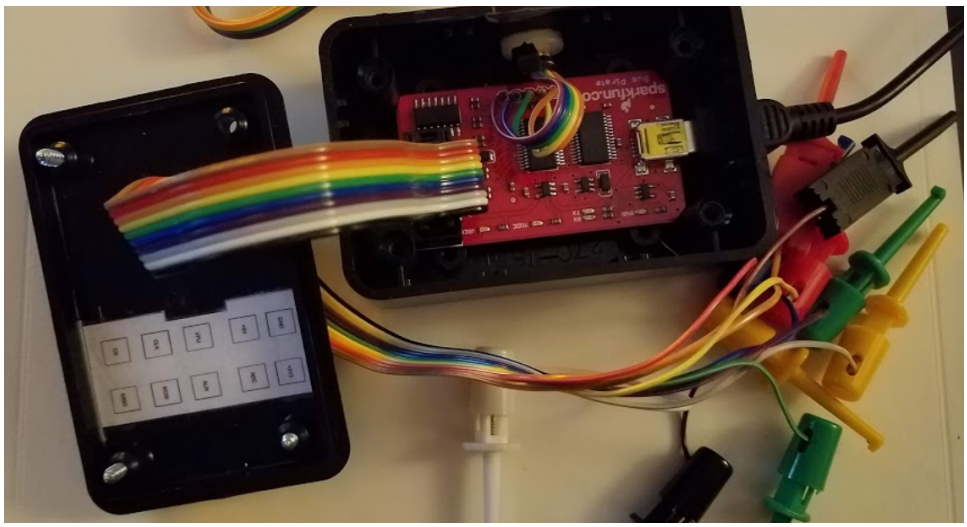


Figure 59: A Bus Pirate is an open source universal bus interface that talks to most chips from a PC serial terminal. This system generates signals desired to test the prototype PCB.

Other graphs of the results can be found here, though all of the significant findings can be found in Chapter 4.

5.1 V1.1 signal output

Simulation: Output from the simulation (Fig. 60).

Photodiode circuit was bypassed, an input signal of 50uA at 5MHz was input, the signal was then sampled to test ADC, finding noise in the lines. This might be attributed to a poor connection from the generator to the ADC in Fig. 61

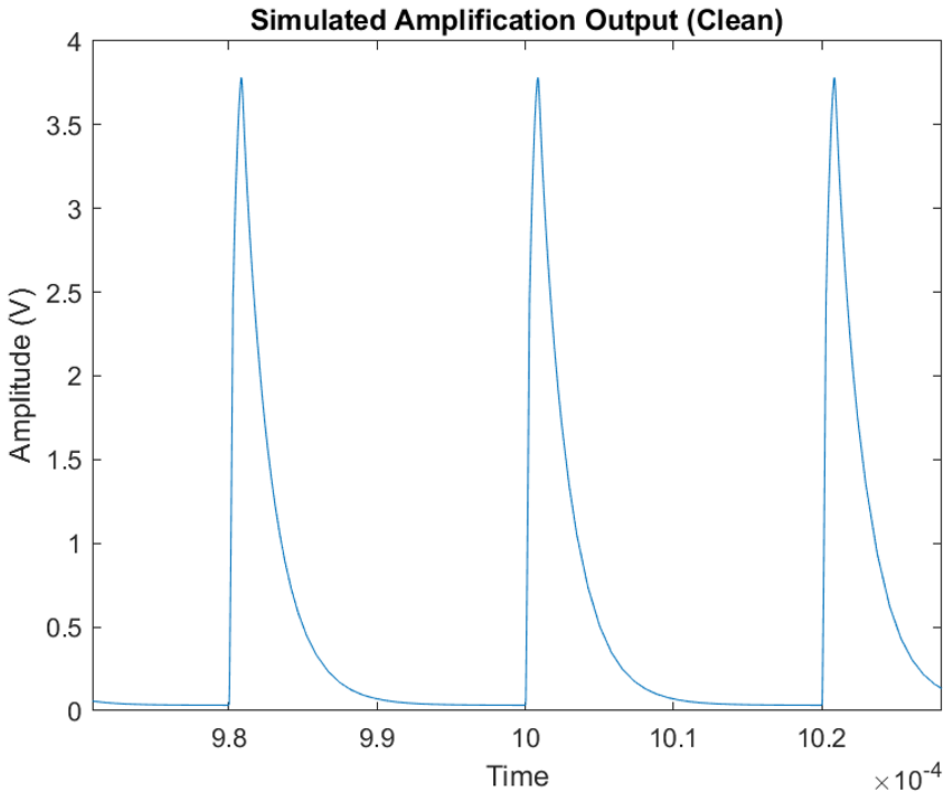


Figure 60: Version 1.1 simulated signal output from the Amplification circuit.

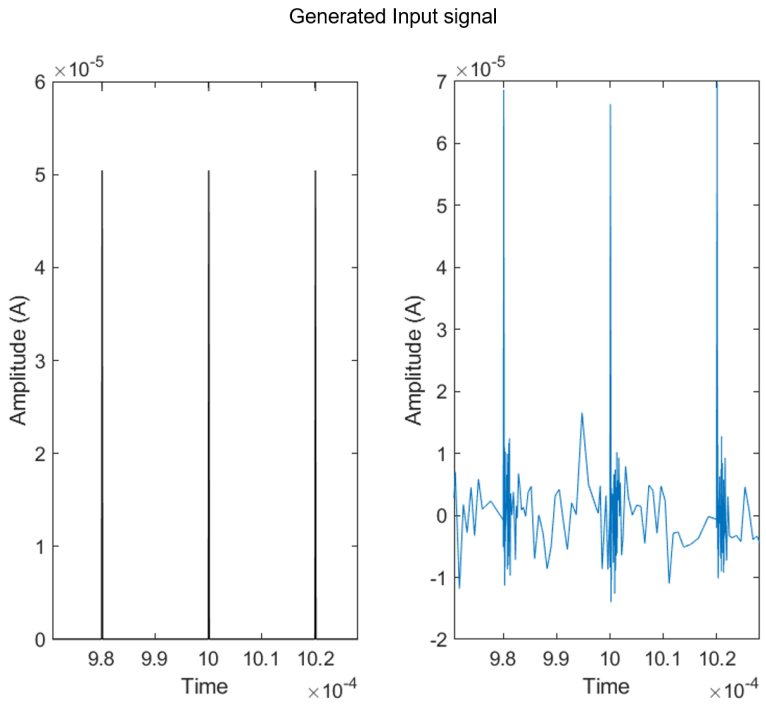


Figure 61: Version 1.1 generated pulse signal input at 50μA at 1MHz pulse. This showed the noise captured by the ADC and output to the FPGA.

5.2 V1.2 Signal output

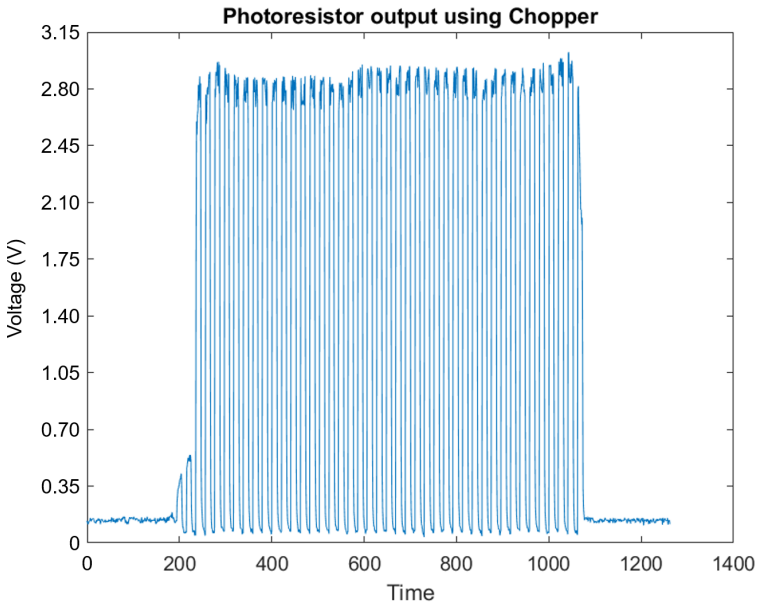


Figure 62: Version 1.2 modification under LED chopper data transmitted over UART showing one brief test span.

UART output measures without photoresistor circuit connected, photoresistor circuit then connected to measure dark voltage fluctuation (Fig. 63. Graph then enhanced to take note of the average voltage of 0.38V dark voltage output. (Fig. 64).

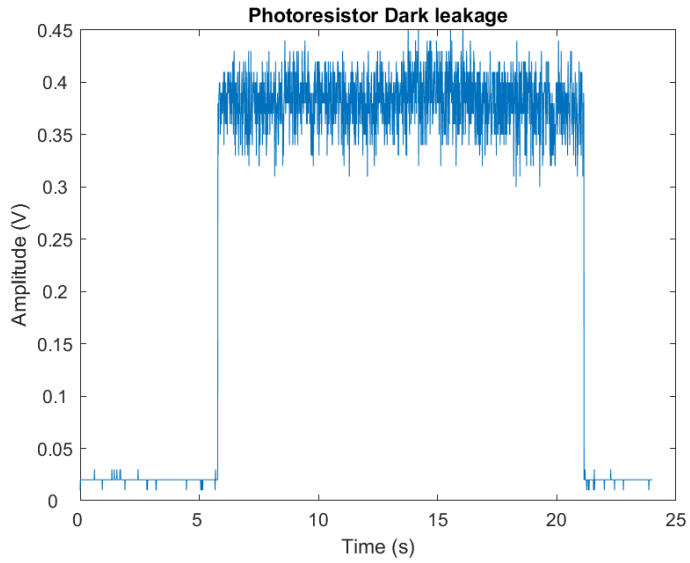


Figure 63: Voltage output when the photoresistor is not stimulated by light, also known as dark voltage.

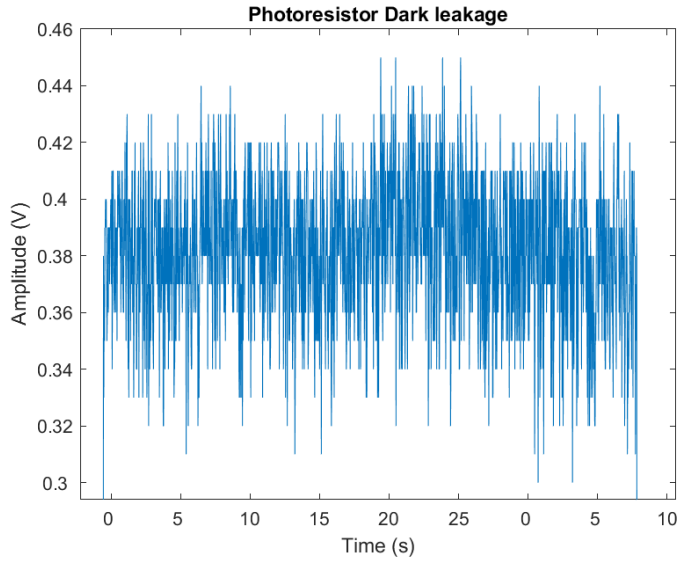


Figure 64: Graph of the voltage fluctuation from the photoresistor when no loght is applied.

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14. ABSTRACT

Attention concerning the proliferation of nuclear weapons and materials has generated many research initiatives to detect, identify, and locate radiation particles emitted by actinides. In support of this effort, the 'Fission Induced Neutron Detection of Nuclear Materials' (FIND'NM) program was established to comprise a joint effort to explore this issue. The objective also co-extends the Air Force Research Laboratory Uranium Dioxide (UO_2) detection sample growth, characterization, and electrical interface research. AFIT's study accomplishes the design and fabrication of a space-tolerant PCB to support a UO_2-based neutron detector. Further design considerations are made with the expectation of the platform to be inside an in-orbit satellite. The PCB will interface a satellite, which in turn will relay transferred data to researchers on the ground for later processing.
The scope of the research is to provide a low-cost commercial-off-the-shelf solution with signal integrity and operational stability in mind. The study performed by LTC Dugan [16] and Lt Col Young [44] provided the basis from which the

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