4MHz to 15MHz Radhard Hybrid CMOS/GaN Buck Converter with 88.6% Peak Efficiency

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***Abstract*— This paper presents a hybrid CMOS/GaN buck converter that exhibits up to 88.6% measured peak efficiency operating at switching frequencies of 4MHz to 15MHz, with a high conversion ratio from an input voltage of 14V to an output of 1.5V (6A) / 5V (5A). This work presents an integrated CMOS gate driver solution in 0.35um CMOS. The CMOS integrated circuit (IC) includes the gate driver and the closed-loop controller for directly driving a GaN power stage. The presented controller technique uses voltage mode control with an innovative cascode driver architecture to allow 3.3V CMOS devices to effectively drive GaN devices that require 5V gate signal swing. Furthermore, the power converter is designed to operate under 400MRad of total dose, thus enabling its use in high-radiation environments.**

Keywords—GaN buck converter, DC-DC converter, high conversion ratio, radhard power electronics

I. Introduction

Recent advancements in power converter applications, such as automotive point-of-load converters (PoL), space power management, wireless and computational electronics, and high particle physics instrumentation, demand buck converters with high load currents and large step-down conversion ratios. There is a need for small form factor, high-efficiency, medium power (10W to 50W) converters to support these emerging applications. Unfortunately, integrated solutions do not exist that achieve high load currents, and these power converters have historically used high power silicon-based devices operating at <200 kHz switching frequencies [1] with large physical output filters and low efficiencies.

The DC-DC converter architecture presented in this work is implemented in GaN-on-silicon (GaN-on-Si) and paired with a high-voltage radiation-hardened CMOS chip packaged in a single unit, as illustrated in Fig. 1. This work addresses key challenges with designing radiation-hardened, small form-factor power converters, including: maintaining high efficiency at high switching speeds, minimization of ringing at critical nodes with high switching frequency to improve electromagnetic compatibility, design innovation to use low voltage-rated devices to drive the high voltage GaN, high gate drive current capability, design for high-radiation environments, efficient board (PCB) design for high frequency applications, and thermal management of power dissipation at heavy loading conditions. Discussion of these design challenges, implementation details, and a full suite of measurement results are presented within this work.

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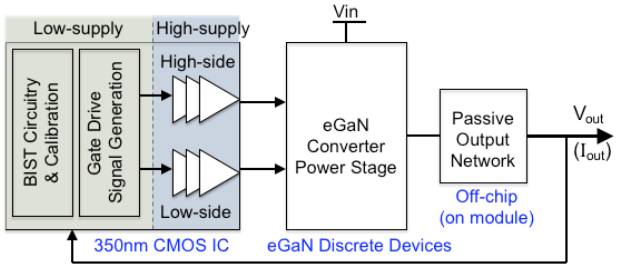

Fig. 1. Conceptual diagram illustrating hybrid converter architecture using CMOS controller and driver IC.

Section II describes the presented converter architecture and provides details of the high frequency gate driver design for GaN switches using low voltage transistors. Section III describes the custom layout strategy for the IC to ensure its radiation robustness. Section IV presents the detailed measurement results of the prototype converter for various performance evaluations, and Section V concludes this paper with a performance summary.

II. Presented Converter Architecture

A. Converter Performance Requirements

The presented switched-mode buck configuration detailed in Fig. 2 is designed to provide a minimum of 5A of current at an output voltage of 1.5V/5V, with state-of-the-art power efficiency. Additionally, the proposed design employs switching (clocking) speeds over 10MHz in an effort to reduce passive device sizing and decrease physical area for module-level integration [2]. The converter uses a GaN-based power stage together with radiation-hardened CMOS-based drivers, feedback, and compensator. The CMOS integrated circuit (IC) is divided into two voltage domains: a high voltage (18V) domain and a low-voltage (3.3V/5.0V) domain. The logic and controller circuitry are performed at 3.3V, with an on-chip radhard linear regulator providing the 3.3V supply from a 5V internally generated supply. With the radiation hardening strategy highlighted in this work, the low voltage devices have

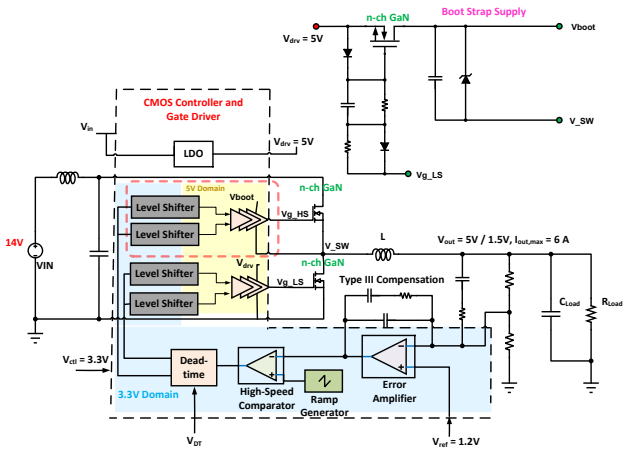

Fig. 2. Detailed block diagram of the presented hybrid CMOS/GaN buck converter.

shown to be immune to total dose effects at 400 megarad (Mrad) levels [3]. The low-side gate driver circuitry is implemented at 5V, whereas the high-side gate driver circuits use some high-voltage devices. The components in the high voltage domain (18V) are subject to degradation in harsh environments, but these devices have also been radiation hardened using radhard layout techniques described in Section III. The system is designed to maximize converter efficiency for large conversion ratios by implementing a CMOS gate driver to control the GaN power stage, thus using an optimal division of functionality between the GaN and silicon CMOS.

B. Converter Architecture

Based upon the selection of EPC enhancement mode gallium nitride (eGaN) power devices as well as a 0.35µm mid-voltage commercial CMOS process technology, the DC-DC power converter of Fig. 2 uses a single-stage synchronous GaN architecture that consumes the smallest area because it requires only one output inductor and two power devices. The CMOS integrated circuit (IC) that includes all controller and driver circuitry. The feedback compensation requires off-chip resistors and capacitors. The output filter is also implemented off-chip with a high current air core inductor to support applications with high magnetic fields, such as the Large Hadron Collider (CERN). The designed IC employs a voltage mode control with external Type-3 compensation for the following advantages: single feedback loop for lowest complexity design, constant switching frequency to eliminate frequency hopping for EMI, good noise margin due to large amplitude ramp waveform, and a low impedance power output, which provides better cross regulation when using multiple output supplies. The limitations of this control method are slow loop response to load transients and loop gain variation when changing the input voltage.

An on-chip linear regulator provides conversion of the 15V input to a 5V regulated supply for the on-chip driver. The 3.3V regulated voltage used to supply the logic circuitry is generated from a second linear regulator that converts 5V to 3.3V. The error amplifier uses a NMOS input folded-cascode topology, with its output fed to the positive input of the high-speed comparator [4]. The negative input of the comparator is connected to the ramp generator's output, which has a programmable frequency implemented from internal switches. The output of the comparator is then fed into the dead time circuit, which generates two non-overlapping PWM signal outputs. The discrete GaN power devices operate like N-channel FETs. Hence, the gate driving signal swings need to be higher than the GaN devices' source voltages, and a bootstrap circuit is used to provide this higher voltage. The dead time output is voltage shifted using a level-shifter before going to the PWM's input to control the high-side driver.

The CMOS driver and controller are integrated on a single IC capable of switching a GaN gate capacitance (200-300pF) load at a switching frequency of 15MHz. Brief details for the critical circuits are given in the following sub-sections, with their associated simulation results. The PVT and Monte-Carlo have been performed for the individual circuit blocks. The closed loop stability analysis has been performed across PVT and Monte-Carlo.

C. CMOS Gate Driver

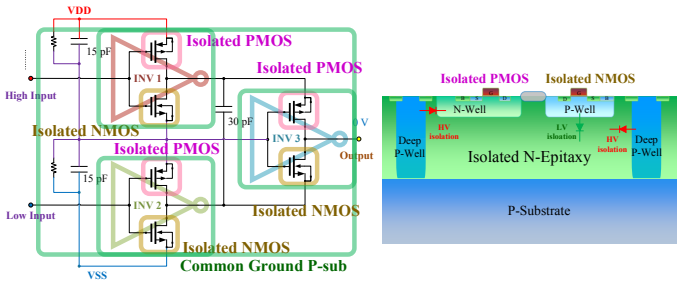

Fig. 3. Schematic of the House of Cards (HoC) cascode implementation using low voltage transistors to drive the high voltage GaN, and cross-section of the inverter with different layers for layout.

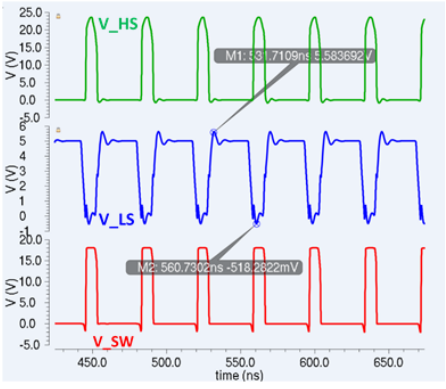

Fig. 4. Post-extracted transient simulation of the HS and LS PWM output signals.

This work presents a novel "House of Cards" (HoC) driver architecture that cascodes transistors to enable low voltage silicon transistors to directly drive GaN power devices, which require 5V signal swings. In this work, a 5V driving voltage must be generated using the 3.3V MOS transistors, which have thin gate oxide and are thus inherently tolerant to radiation-induced V_T shift. The intermediate node of a capacitive and resistive divider is used to provide the transient current requirements for driving the GaN switches while maintain a stable DC voltage. The switching behavior is also controlled by the level shifter, as detailed in the next sub-section. The capacitive divider needs accurate inter-digitization layout techniques for matching and performance. The final output stage is a floating inverter block, where the PMOS and NMOS source terminals are shifted with the input signal levels such that both these PMOS and NMOS will only experience a maximum of 2.5 V across their V_{DS}, V_{DB} or V_{SB}. Fig. 3 shows the schematic diagram of the cascode output driver and the cross-section of an isolated PMOS and NMOS pair in the twin-well n-epitaxy process. Each transistor has its bulk connected to its source terminal, while the local common ground is connected to p-substrate. The three inverters connected together form a cascode inverter chain. Fig. 4 plots the post-extracted simulation results with 20MHz switching frequency. In this simulation, the input and output bondwire inductances are modeled, and the rise/fall time of the PWM signals is about 3ns and the maximum voltage level of the PWM output is below 5.5V. The drive strength of the driver has an average of 350mA and 1A peak current capability for a maximum switching frequency of 20MHz and load capacitance of 300pF.

D. Level-Shifter

The level shifter is designed using a cross-coupled inverter stage shown, as shown in Fig. 5 [5]. This block provides the desired signal swing for the cascode device in the driver stage (high side/low side). The presence of the high voltage (HV) bootstrap demands the need for 25V HV transistors because the eGaN gate needs 5V V_{GS} swing. To drive the cascoded output driver, a complementary signal pair with one swing ranging from 2.5-5V and the other one from 0-2.5V are required (Fig. 6). The level shifter block uses a radiation-tolerant 3.3V thin gate-oxide LDMOS provided in the 0.35um CMOS technology, which is connected to the V_L node in the isolated HV domain. Simulation results in Fig. 6 show the timing diagram and the voltage levels between the level shifter's input and high-side (HS) and low-side (LS) outputs at 20 MHz, with 2-3ns dead-time and 20% duty cycle. The transistors' W/L scaling is chosen to keep the delay matched between the HS and LS outputs.

E. Other Supporting Circuitry

Dead Time: The dead time circuit (or non-overlapping clock generator) uses a standard cross-coupled circuit. The dead time can be configured by varying the voltage potential on the control node through an external analog pin.

Comparator: The high-performance comparator consists of three stages: pre-amplification, decision feedback, and post amplification (output buffer). The comparator is designed to operate up to 20MHz of switching frequency. It is current-controlled with the decision feedback stage using a cross

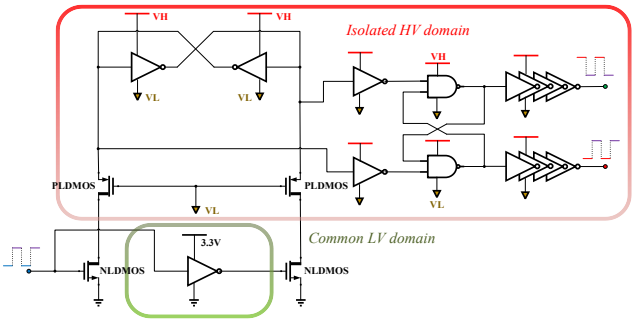

Fig. 5. Schematic of the level-shifter, highlighting the high-voltage and low-voltage domains.

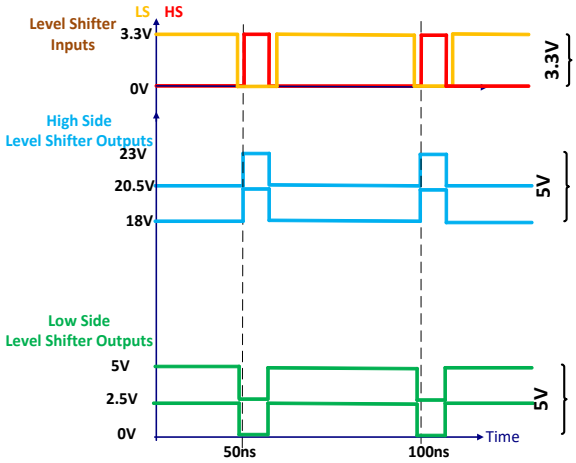

Fig. 6. Level-shifter's timing diagram showing inputs, low-side outputs, and high-side outputs.

coupled architecture. There are no high impedance nodes in the circuit other than input and output, thus enabling high speed operation.

Error amplifier: The error amplifier is used as the first stage of the controller [4], and it senses the output feedback voltage and controls the PWM pulse width. The amplifier has a DC gain of about 75dB and unity gain cross-over frequency of 62MHz. This ensures the low steady-state error between the output and desired feedback node that is set by the reference voltage. With a 20MHz switching frequency, the control loop bandwidth is selected to be 750 kHz to ensure sufficient loop response time for a transient event. External Type III compensation is used to provide design flexibility.

Ramp Generator: The ramp generator shown in Fig. 7 is implemented by a negative feedback loop with a desired voltage hysteresis controlled by the high and low switching voltage levels [4]. The ramp is generated with a Schmitt trigger, NAND gate, and inverter in the feedback loop. The NAND gate has a trigger input for circuit startup. Its output is fed to the inverter, forming an oscillator circuit. The capacitor charge and discharge paths have different resistances (pull-up or pull-down) and provide the desired ramp output. This output controls the charge and discharge slope of the ramp waveform. The frequency for the ramp can be set using one of two methods: 1) setting different values of bias currents, or 2) switching-in different resistances for the pull-down path. The

desired transient hysteresis is controlled by the number of current sinking transistors (multipliers) and the capacitive charging loads.

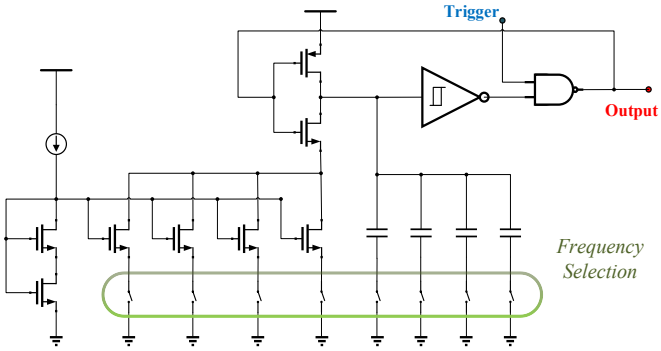

Fig. 7. Schematic of the ramp generator.

III. Radiation Hardening Techniques

CMOS circuits operating in a high-radiation environment suffer from total ionizing dose (TID), SEE (single event effects), and displacement damages (DD). Several radhard by design techniques (RHBD) have been employed in this design to increase the radiation tolerance of the CMOS circuits [6,7]. Annular layout for NMOS transistors, or enclosed layout transistor (ELT), has been used to reduce radiation-induced leakage at the edge of the transistor, especially for the NMOS transistors [8].

An octagonal gate for the ELT layout is used in this work to reduce edge crowding common at the corners of rectangular gate ELT shapes. A fully customized ELT NMOS transistor p-cell library with different physical profiles was created for this converter design. Fig. 8 gives an example of an ELT NMOS transistor. The initial schematic design needs a 10µm/0.4µm size NMOS transistor. By going through a custom design procedure, Fig. 8 demonstrates a corresponding annular layout with exact verified W/L value of 10.5958µm/0.4203µ, which has both sizes and ratio very close to the initial target size.

Fig. 9 provides an example of an inverter layout using the ELT NMOS. The layout for the PMOS transistors is a conventional inter-digitated two-edge layout. The size for the inverter is 10.5958µm/0.4203µm with 8 multipliers. The extracted simulation shows that simulation matches with original schematic results closely.

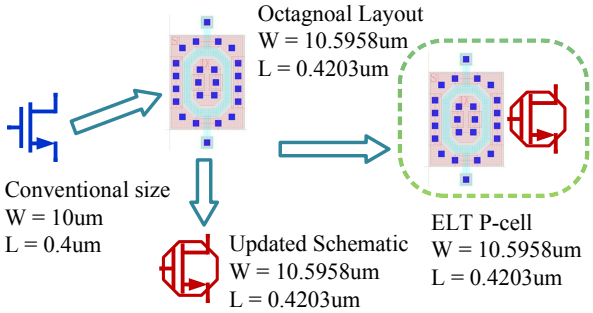

Fig. 8. Procedural flow for parameter calculation of the ELT transistors from the foundry-provided conventional (non-radhard) transistor.

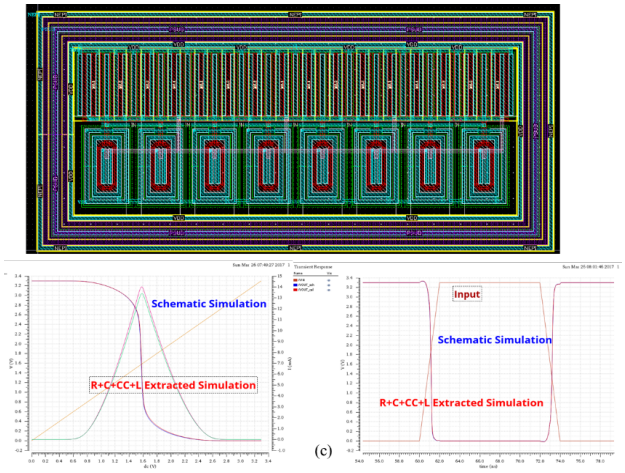

Fig. 9. ELT layout of the RHBD inverter with the transfer characteristics and transient performance showing that the extracted simulation closely matches with schematic simulation.

IV. Implementation and Measurement Results

The fabricated prototype converter board is shown in Fig. 10(a), which includes test-points for debugging and stand-alone IC characterization. The board size is 8.7cm × 9.2cm. The effective area of the converter when eliminating the debug connectors is 3.5cm x 4cm. A die photo highlighting the various functional blocks of the fabricated IC is shown in Fig. 10(b). Table I summarizes the converter results with different combinations of input and output voltages and switching frequency. Fig. 11 plots the measured converter's efficiency as a function of output load current for different switching frequencies and 14V input to 5V output conversion. The results show that the converter achieves peak efficiency of 88.2% for lower switching frequency of 4MHz. The efficiency drops to 72% for a high switching frequency condition due to increased switching losses. Fig. 12 shows the efficiency as a function of output load current for the power converter system at 4MHz switching frequency including the driver and feedback logic circuit losses. The results show that the converter achieves peak efficiency of 80% for a small conversion ratio at 6V input to 1.5V output.

Fig. 13 plots the measured steady state response of the converter's output for a 14V input to 1.5V output, operating at different loading conditions from light load (1A) to full load (6A). The output voltage ripple for the 1.5V output is ~10mV. The high frequency ringing of the switch node is coupled to the output node during measurements. The bandwidth limit of the oscilloscope is not used for these measurements. The inductor ripple current is ~1A due to use of 0.5µH of inductor for the output filter. This value was used to reduce the inductor ripple current and increase efficiency.

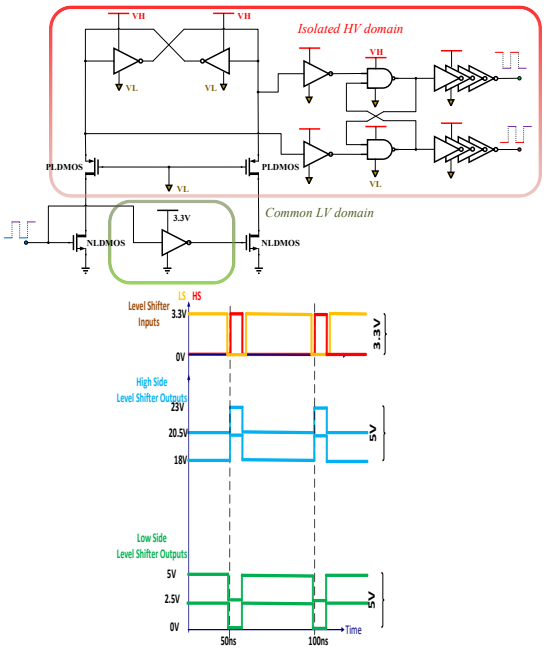

Fig. 10. (a) Fabricated prototype buck converter, and (b) Fabricated CMOS IC in 0.35um process technology.

TABLE I
SUMMARY OF CONVERTER RESULTS

Measurement	1	2	3	4
Vin	14 V	14 V	14 V	14 V
Vout	1.5 V	5 V	5 V	5 V
Conversion Ratio	10:1	3:1	3:1	3:1
Maximum Frequency	4MHz	4MHz	10MHz	15MHz
Maximum Load Current	6 A	5 A	5 A	3.4 A
Maximum Efficiency	70.9%	88.6%	80.6%	72.8%

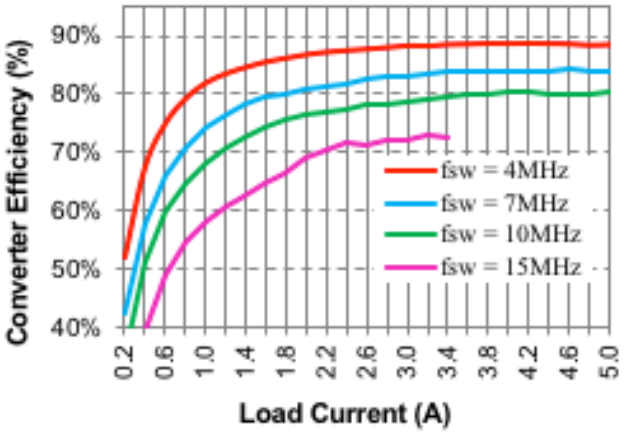

Fig. 11. Measured efficiency versus load current for a 14V input to 5V output conversion with varying switching frequencies. A switching frqeuency of 4MHz gives 88.6% peak converter efficiency.

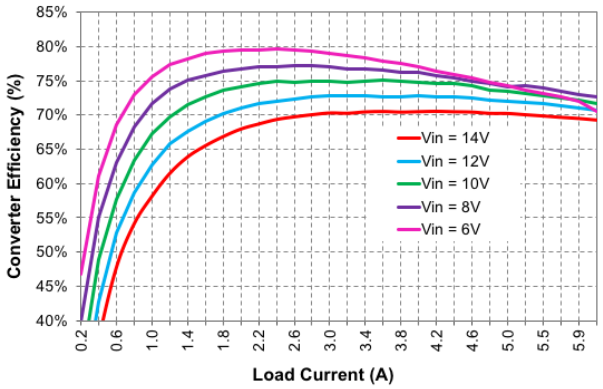

Fig. 12. Measured efficiency versus load current at 4MHz switching frequency for 1.5V output voltage and varying input voltages.

V. CONCLUSION

This work presents a buck converter that is implemented using CMOS for the controller and driver functionality and EPC eGaN devices for the power stage. The hybrid converter is designed for total dose radiation levels up to 400Mrad. The design strategy to achieve this radiation robustness has been detailed in this work. Furthermore, the converter achieves best-in-class efficiency at MHz switching speeds. The high performance was achieved through: 1) hybrid architecture, 2) novel level shifter and driver architectures, 3) minimization of thermal resistance, and 4) aggressive management of gate ringing. The performance summary in Table II provides a comparative analysis of the measurements from this work with similar existing work. It has been demonstrated that the presented solution significantly reduces physical form factor (size) from state-of-the-art CMOS solutions by providing an integrated power converter solution that achieves both high frequency and high current.

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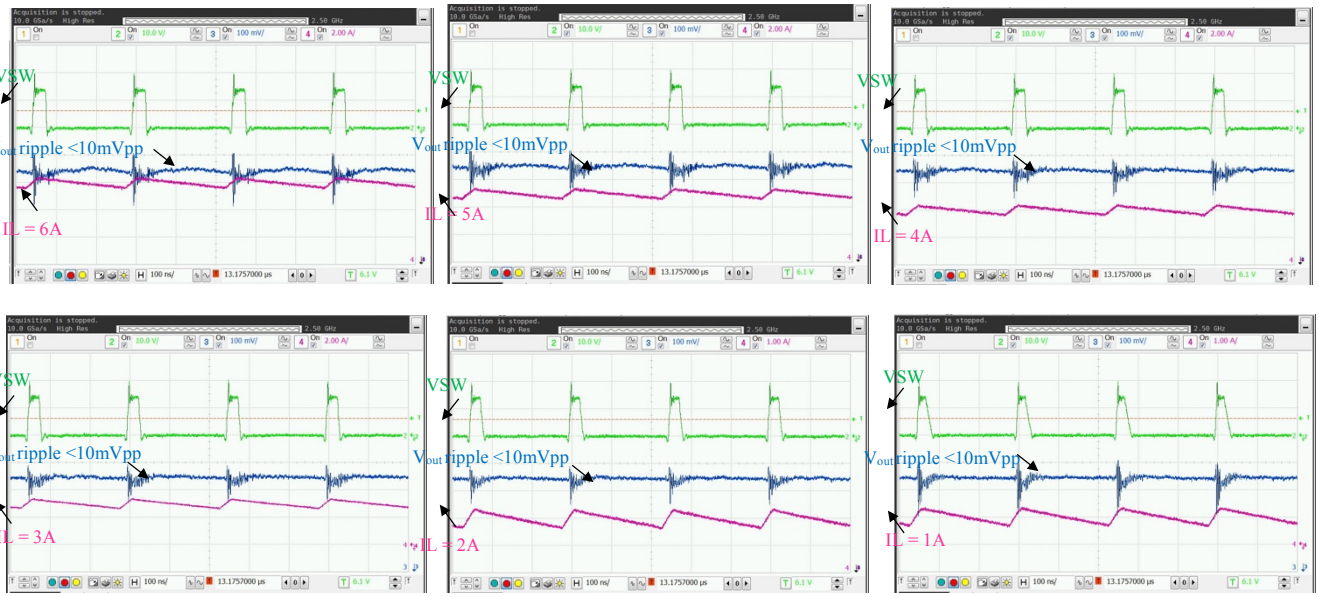

Fig. 13. Measured efficiency versus load current for a 14V input to 5V output conversion with varying switching frequencies. A switching frqeuency of 4MHz gives 88.6% peak converter efficiency.

TABLE II: PERFORMANCE SUMMARY OF PRESENTED WORK COMPARED TO PRIOR ART

Parameters	**[9]**	**[10]**	**[11]**	**[8]**	**[12]**	**[13]**	**[14]**	**This work**	**This work**
Year	2017	2016	2016	2014	2015	2017	2017	2018	2018
Technology	0.18µm	40nm	90nm	0.35µm	-	-	0.18µm	0.35µm	0.35µm
Publication	JSSC	PEL	TPE	REDW	TPE	TPE	JSSC	-	-
V_{in} (V)	8.0	3.3	3.3	12	48	24	2.0	14.0	14.0
V_{out} (V)	1.0	2.4	1.8	5	3.3	5	0.8	1.5	5.0
Duty cycle	0.125	0.727	0.545	0.42	0.069	0.208	0.40	0.107	0.357
Architecture	Multi-phase (3)	Single-phase	Single-phase	Single-phase	Coupled Inductor	Transformer SEPIC	Multi-phase (4)	Single-phase	Single-phase
Power-stage switching devices	Custom GaN	LDMOS	LDMOS	LDMOS	Discrete MOSFET	GaN EPC2015	LDMOS	GaN EPC2014C	GaN EPC2014C
Max. f_{sw} (MHz)	40	100	1	3	0.1	7	9.5	4	15
Filter Inductor (µH)	0.150.	0.06	4.7	1.5	86	0.27	0.33	0.5	0.141
I_{max} (A)	0.198	0.30	0.50	4	15	2	6	6	3.4
Output Ripple (mV)	N.A.	N.A.	24	6	N.A.	N.A.	17.6	10	50
Transient Response ΔV_{out} (mV) / ΔT_R (µs)	N.A.	N.A.	<50/25	<200/25	<320/500	N.A.	N.A.	<80/25	<80/60
Die Area (mm^2)	8	0.048	0.94	N.A.	N.A.	N.A.	12.5	8.32	8.32
Peak η (%)	76% @ 51mA	91.5% @ 0.15A	89.7% @ 0.5A	87% @ 3A	95% @ 2.5A	73.4% @ 2A	69% @ 3A	70.5% @6A	72.6% @3.4A