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POWER/AREA-EFFICIENT I/O AND WRITE CIRCUITS FOR MEMRISTOR CROSSBAR ARRAY BASED NEUROMORPHIC COMPUTING SYSTEM

SAN FRANCISCO STATE UNIVERSITY

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FINAL TECHNICAL REPORT

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13. SUPPLEMENTARY NOTES

14. ABSTRACT

In this project, we designed and implemented several critical analog integrated circuit blocks to support theneuromorphic computing using memristor crossbar array. Specifically, we designed and implemented the*high-speed integrate-and-fire circuit* (H-IFC) for the energy-efficient spike-based neuromorphic computingsystem, and the *digital-to-analog convertor* (DAC), the *trans-impedance amplifier* (TIA), and the pipelined*analog-to-digital convertor* (ADC) for the high-performance level-based neuromorphic computing systemusing Global Foundry 0.13□m standard CMOS technology.

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1.0 SUMMARY

The overarching research goal is to develop power/area efficient integrated circuits to facilitate the neuromorphic computing system based on the recently-developed memristor crossbar array technology. In this project, we designed and implemented several critical analog integrated circuit blocks to support the neuromorphic computing using memristor crossbar array. Specifically, we designed and implemented the *high-speed integrate-and-fire circuit* (H-IFC) for the energy-efficient spike-based neuromorphic computing system, and the *digital-to-analog convertor* (DAC), the *trans-impedance amplifier* (TIA), and the pipelined *analog-to-digital convertor* (ADC) for the high-performance level-based neuromorphic computing system using Global Foundry 0.13μm standard CMOS technology.

2.0 INTRODUCTION

The bio-inspired neuromorphic system has the potential to realize high-efficiency computing [1]. Traditionally, the neuromorphic computing system is implemented in conventional digital integrated circuits and requires a large amount of memory [2]. However, its power consumption and size prevent its widespread adoption.

Li and Wu *et al*. have demonstrated that a neuromorphic computing system using *memristor crossbar array* (MCA) has superior pattern association and classification capability [3]. The MAC technology also has the potential to realize a massively-parallel, large-scale neuromorphic computing system. The recently-developed memristor technology [4] provides a promising path to have a large memory without consuming a large amount of power or size [5, 6].

Several research groups have explored the hardware implementation of a neuromorphic system [7, 8]. The power/area efficiency of the I/O circuits, which facilitate the MCA based neuromorphic computation, have deep impact on the overall system computation efficiency [9] and [10]. The objective of this project is to develop power/area efficient I/O circuit

In this three-year project, the team at San Francisco State University (SFSU) has designed and implemented high efficient analog circuits that are part of the neuromorphic processor chip developed by Duke University (Duke) and University of Massachusetts Amherst (UMass). Duke has designed and implemented the MCA based neuromorphic controller systems, while UMass has developed MCA technology. We designed and implemented *high-speed integrated-and-fire circuit* (H-IFC) for the spiking-based design and digital-to-analog convertor (DAC), *trans-impedance amplifier* (TIA) and *analog-to-digital convertor* (ADC) for the level-based design. The aforementioned circuits have been implemented through chip fabrications at Global Foundries using standard 0.13 μm CMOS process.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

The memristor crossbar array technology has the potential to build a massively-parallel, high-efficiency neuromorphic computing system [11]. When implemented in hardware, the performance of the I/O circuits could dramatically impact the system's overall performance.

Two types of neuromorphic computing systems are developed in this project: an energy-efficient spike-based design and a high-performance level-based design. Due to the differences in the two designs, two sets of I/O circuits are developed. For the spike-based design, the input circuit is to produce a frequency-modulated pulse train with the same amplitude and duration, and the output circuit is to produce equal amplitude/duration pulses whose frequency is modulated by the output current from the memristor. For the level-based design, the input circuit is to produce an amplitude-modulated voltage signals with 4-bit resolution, while the output circuit is to read out the resulting current from the memristor, and digitize it to a 4-bit word. The design objective is to achieve these functions with high accuracy and speed. To support the matrix vector multiplication, the input circuit is needed for each memristor row and the output circuit is needed for each memristor column. Thus, the power consumption and the chip area of the I/O circuits must be minimized for a massively-parallel memristor crossbar array.

The generate approach to develop these analog circuit blocks is (1) conceptualize the circuit topology, (2) spice simulation to validate the concept, (3) layout the circuit based on the Global Foundry 0.13μm technology, (4) integrate the analog blocks with the rest of the circuit system, and (4) characterize the individual circuit blocks (carried out in

3.1. SFSU) and the whole circuit system (carried out by Duke team).

The Design Concept

Memristor crossbar array has been proved to efficiently perform matrix-vector multiplication in neuromorphic algorithms. By referring the circuit diagram in Figure 1, the matrix-vector multiplication can be realized as follows: (1) represent the input vector as a set of input voltage signals to *wordlines* (WLs) of the memristor crossbar; (2) transfer the mathematical matrix to the resistance state of the memristors in the array; and (3) collect the currents at the *bitlines* (BLs) as the output vector of the matrix-vector multiplication operation.

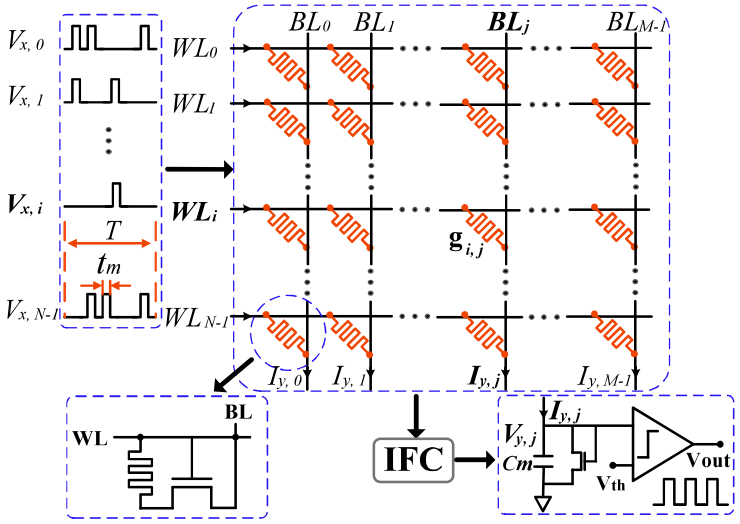

Figure 1: An overview of the spiking-based neuromorphic design (From Duke University)

3.2. Design 1: Analog Circuits for the Spike-based Controller

In the spike-based design, the objective of the circuit is to sense the electric current at each BL. Conventionally, a *trans-impedance amplifier* (TIA) and an *analog-to-digital convertor* (ADC) will do the job. To reduce the power consumption and the chip area, a high-speed integrate-and-fire circuit (H-IFC) that is able to readout the current from the memristor without a TIA or an ADC, which are more power hungry.

3.2.1 High-speed Integrate and Fire Circuit

The IFC's architecture and the operating principle are illustrated in Figure 2. Different from the conventional IFCs used in neuron modeling [12], the proposed H-IFC [13, 14] requires that the time constant of the memristor and the sensing capacitor (τ=Rmem × Cs) is much smaller than the duration of the input pulse. A small value-sensing capacitor is always preferred to reduce the overall circuit area. When the voltage pulse is applied to the memristor, the voltage across the sensing capacitor increases, as $v_{Cs} = v_{in}\left(1 - e^{-t/\tau}\right)$. When the reference voltage of the comparator, V_{REF}, is set to be 0.7 V (~33% of v_{in}), the time period that the sensing capacitor takes to rise from zero and V_{REF} (Δt) is less than τ. Because of the short charging time, the expression of v_{cs} can be linearized as

$$v_{Cs} = v_{in}(t/\tau) = (v_{in}/R_{mem})(t/C_s) = i_{in}(t/C_s).$$

The comparator resets v_{cs} back to zero when v_{cs} reaches V_{REF}. The voltage across the sensing capacitor is briefly sketched in Figure 2. The time period of each pulse (Δt) can be derived as:

$$\Delta t = \frac{V_{REF} C_s}{i_{in}}$$

In other words, the frequency of the voltage signal across the sensing capacitor is proportional to the current, which is the matrix calculation result from the memristor crossbar array.

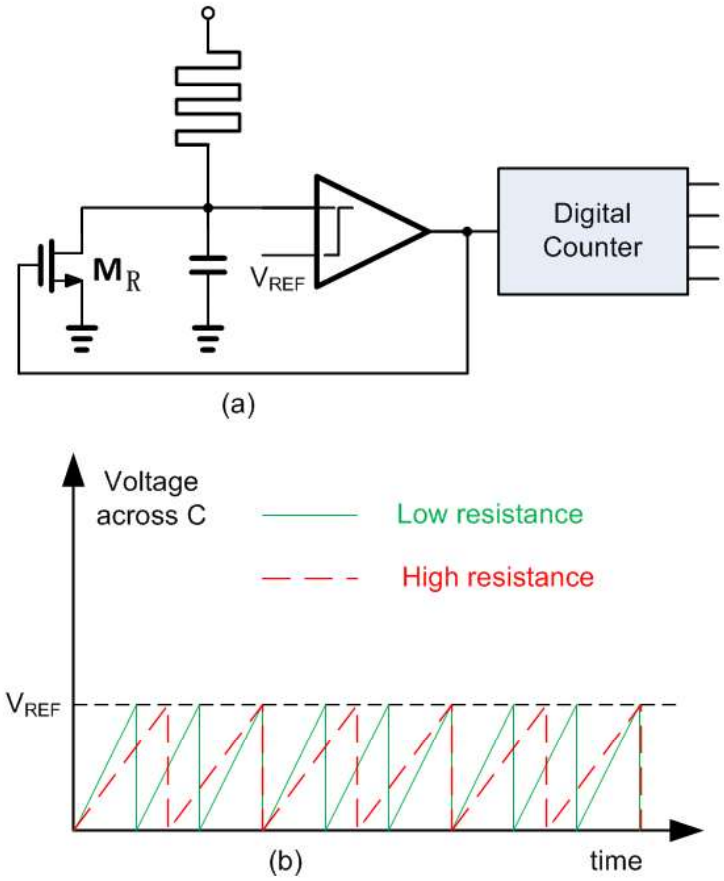

Figure 2: (a) The circuit architecture (b) The operating principle of the proposed H-IFC

The design of the H-IFC is described in Figure 3**.** The voltage across the sensing capacitor and the output spikes are plotted in Figure 4**.** In the design, C_S is 153 fF, which is the smallest *metal-insulate-metal* (MIM) capacitor provided by the PDK. The reset time clearly slows down the output spike although the delay time of the comparator is less than 1 ns. Thus, the frequency of the output spike could be saturated when i_{in} is high. The power consumption reaches 220 µW when the period of the output spikes reaches 1.4 nsec.

The sensing capacitor, C_S, was implemented using a MIM capacitor. In IBM 0.13-µm technology, the MIM capacitor occupies a large area because it uses thick metal layer (top-3 metal layer).

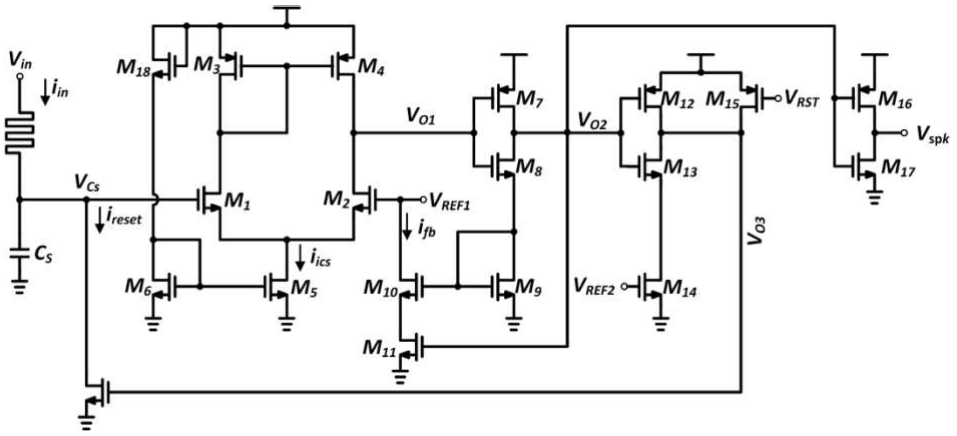

Figure 3: The schematic of the H-IFC

The delay of the IFC is a critical to the performance of the spiking neuromorphic system. The design parameters, mainly the transistors' aspect ratio and current level, were carefully selected so that the delay of the H-IFC is shorter than the minimum BL integrating time.

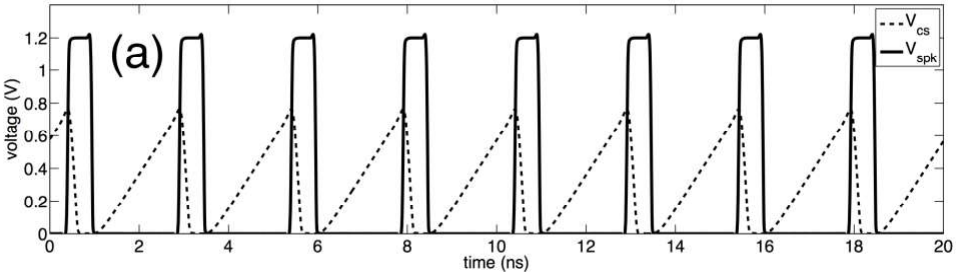

Figure 4: The voltage across *Cs* and output spikes versus time

To produce the digital output from the pulses generated by the H-IFC, a 6-bit synchronous counter, illustrated in Figure 5, is used to generated the digital output with a single *CLK* input. The synchronous counter contains 6 full-adders and 6 D-flip-flops. Once the power is applied to the circuit, the full-adder array starts counting the digital number automatically. The *U/P* selecting signal is used to select the counting condition. The counter either counts from 6b'000000 to 6b'111111 if *U/P* is set to be low (*U/P* = 0), or counts from 6b'111111 to 6b'000000 if *U/P* is set to be high (*U/P* = 1). By applying the *CLK* signal to trigger the D-flip-flop array, the digital number will be generated. The speed of the 6-bit synchronous counter is determined by the *CLK*.

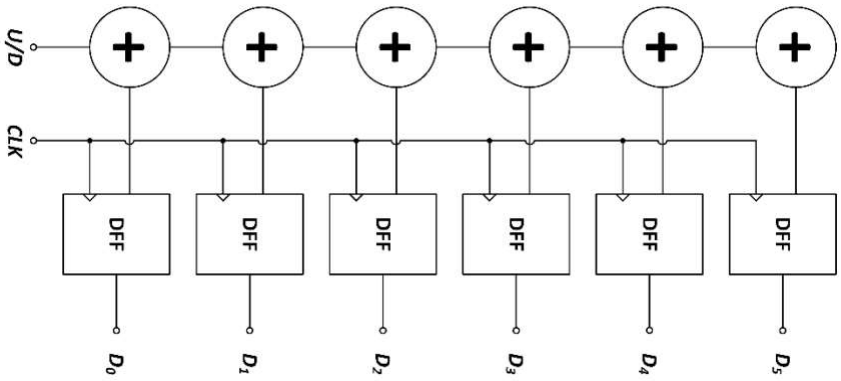

Figure 5: The simplified schematic of 6-bit Synchronous Counter

Figure 6 shows the simulation result of the proposed 6-bit synchronous counter with count-up condition (*U/P* = 0) and 20 MHz operating frequency. The digital output number increases 1-bit per full clock cycle (0.1 µs per increment).

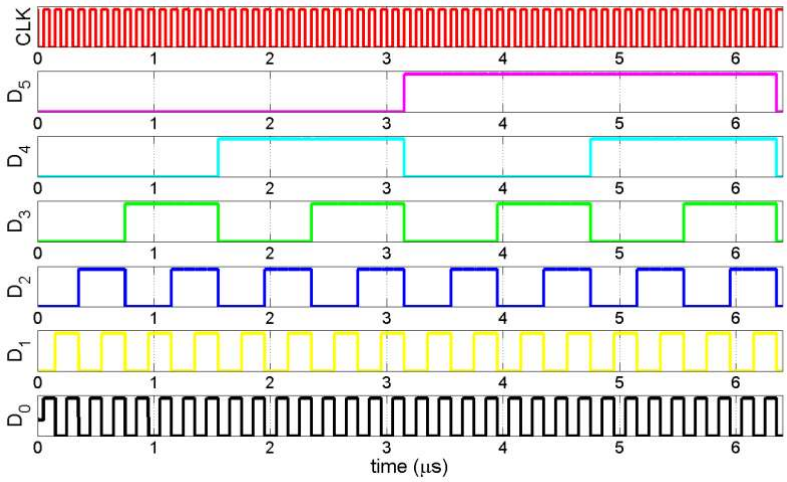

Figure 6: Waveform of the 6-bit Synchronous Counter

3.3. Design 2: Analog Circuits for the Level-based Controller

In the level-based design, the memristor crossbar array is used to carry out matrix vector multiplication. As depicted in Figure 7, the input vector is the voltage signal that is applied to each row, and the output vector is the current from each column. The current represents the product of the multiplication based on Ohm's Law. In this project, we have designed and implemented the following three analog circuit blocks: the *digital-to-analog converter* (DAC), the *trans-impedance amplifier* (TIA), and the *analog-to-digital convertor* (ADC). The DAC is used to convert the input digital word into the voltage amplitude that is applied to each row. The TIA and the H-IFC together convert the

output current of each column into the output digital word. The ADC is put into the test key to gauge its feasibility in this application.

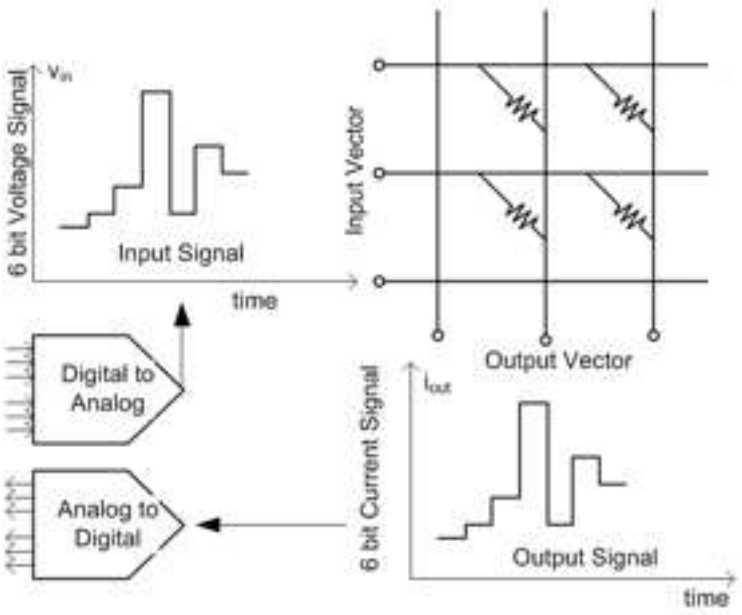

Figure 7: The simplified diagram of the I/O circuits in the level-based design

3.3.1 Digital-to-Analog Convertor

To achieve high-speed and linearity, a 4-bit current-steering DAC consists of a cascode current mirror and an amplifier, is depicted in Figure 8. In a current-steering DAC, each bit turns on or off a branch of a binary weighted current. As depicted in Figure 8, a constant gate voltage is applied to a set of NMOS with the binary weighted channel width [15]. Consequently, each branch produces a binary weighted current. By controlling the ON or OFF of each binary weighted branch current, the sum of the output current (I_{DAC}) is proportional to the input digital word. The weighted branch can be obtained by varying the widths of the transistors.

A cascode current mirror is used to duplicate the same amount of I_{DAC} to be applied to an operational amplifier, which is used to convert the input current from the cascoded current mirror and produce an output voltage. The amount of current that is delivered to the two-stage wide-swing operational amplifier is determined by the input digital word.

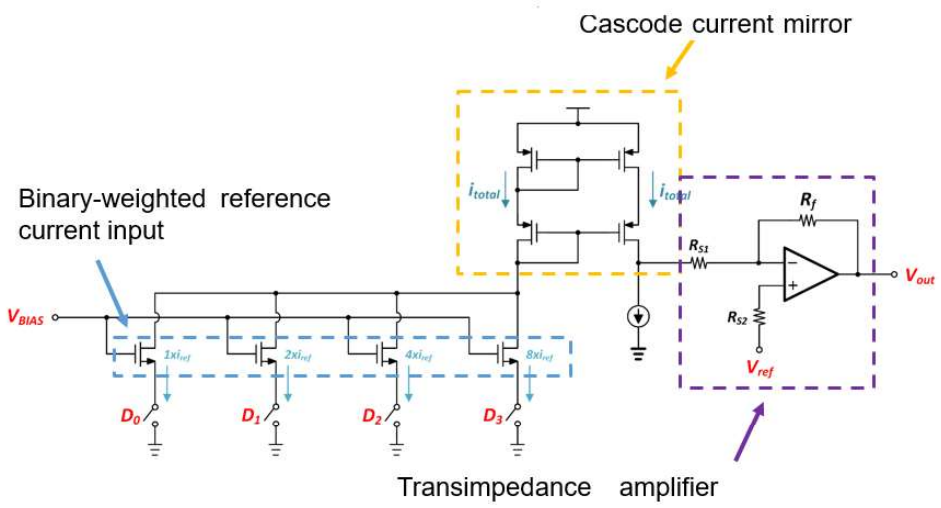

Figure 8 The schematic of the 4-bit current steering DAC

The two-stage wide-swing operational amplifier is designed using the folded-cascode structure as shown in Figure 9. The simulation shows the amplifier has the gain of 69 dB and the unit-gain bandwidth of 446 MHz.

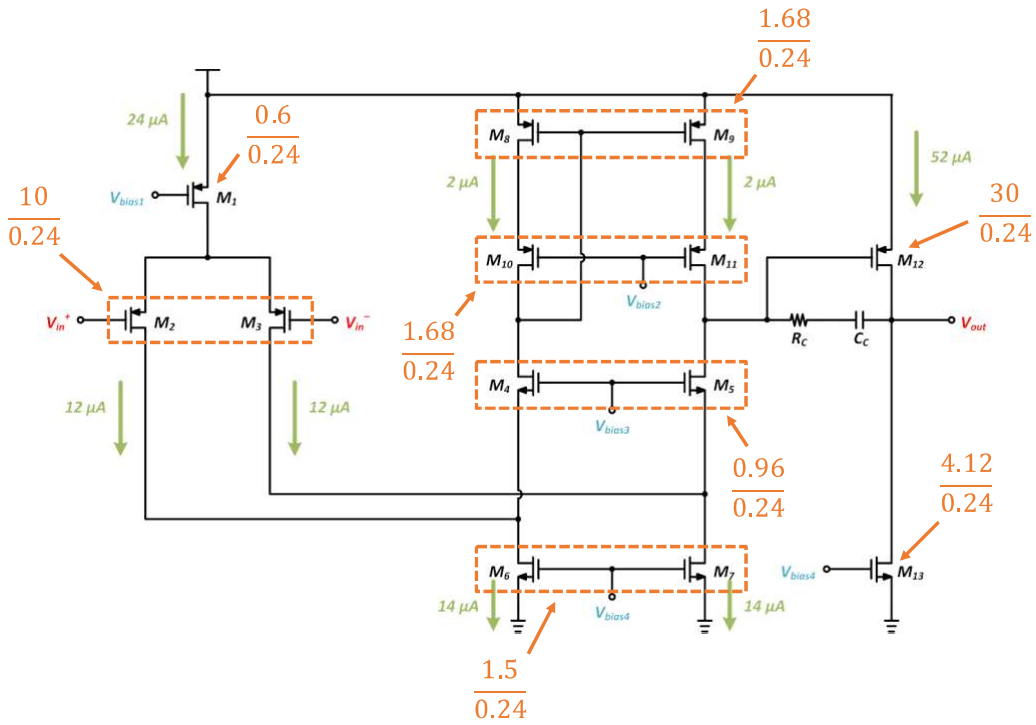

Figure 9: The schematic of the two-stage wide-swing operational amplifier

The 4-bit current-steering DAC's output voltage versus its input word is shown in Figure 10. The operating frequency of the current steering DAC is ~50MHz. The size of the

circuit is about 22 × 48 μm^2. The power consumption is about 1.1 mW when the sample rate is at 50 MHz.

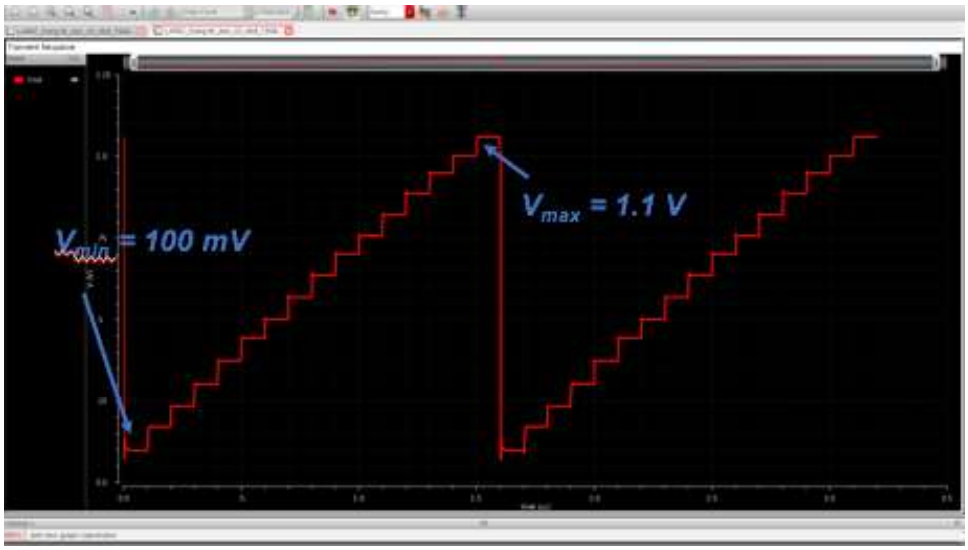

Figure 10: The simulation results of the current-steering DAC

3.3.2 Trans-impedance Amplifier

A wide dynamic range TIA is designed to convert the bit-line current from the memristor crossbar into the current with capability to drive an IFC or an ADC for its accurate current readout. An amplifier with a low and fixed input voltage is created, which can duplicate the BL current and offer high output voltage that has enough driving capability for the IFC or the ADC.

Figure 11 illustrates the proposed TIA. Current mirror pair consisting of M1 and M2 operates in the linear region. Attaining the target of having a low and fixed V_{in}, a negative feedback created by operational amplifier OP1 and transistor M1 establishes a virtual short between the input node and the reference node. Once the reference voltage (V_{ref}) is given by 0.1 V, V_{in} is clamped on 0.1 V. Another negative feedback loop consists of OP2 and M5 forces V_Z tracking to V_{in}, which indicates M1 and M2 share the same value of V_{DS}, which is fixed at 0.1 V. Meanwhile, the gate-to-source voltages (V_{GS}) of M1 and M2 are provided by the output voltage of OP1, which can offer V_{eff} of M1 and M2 higher than 0.1 V (V_{DS}), and make M1 and M2 work in linear region.

OP1 and OP2, shown in Figure 11, are operational amplifiers that are responsible for creating negative feedback loops [16]. The low frequency gain of the op-amp is 58 dB and the gain-bandwidth product is 1.54 GHz.

The operating principles of the current-to-voltage converter are similar with the proposed current amplifier. The (V_{out}) can be gained by multiplying the output resistor (R_O) and the output current that sent by transistor M6 (I_{out}). The difference between the current-to-voltage converter and the current-to-current amplifier is that the converter is used to receive large output voltage swing and to have high accuracy of the V_{out}.

To increase the output voltage swing, there is a current reduction of k ($0 < k < 1$) in both current pairs of M1 and M2, and M3 and M4. This reduction results in smaller I_{DS} of M5 and M6 together with lower V_{eff} of M6. Consequently, the maximal V_{out}, which can be expressed as $V_{out(max)} = V_{DD} - V_{eff}$, can be increased.

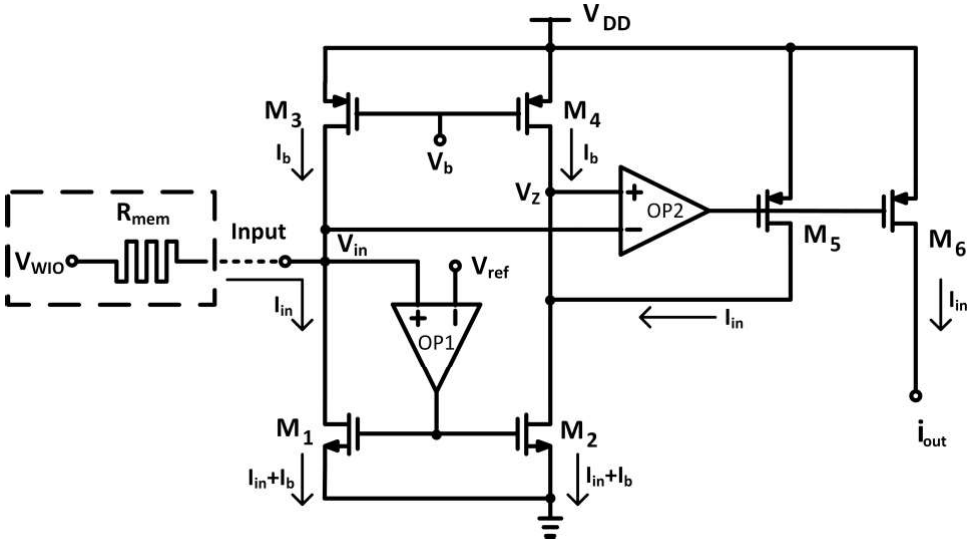

Figure 11: The simplified schematic of the proposed current amplifier

The R_L resistor, which is placed at the drain of M6, is another alteration that can enhance the accuracy between the current and V_{out}. Without the R_L, V_{DS5} is fixed at 1.1 V meanwhile V_{DS6} is changing with the I_{out} and represented as $V_{DS6} = V_{DD} - (I_{out} \times R_O)$. The disparity between V_{DS5} and V_{DS6} will result in an error in this current mirror and cause the low accuracy of V_{out}. Once R_L is inserted, the V_{DS5} becomes to $V_{DS5} = V_{DD} - (I_{out} \times R_L + 0.1\ V)$. An appropriate R_L makes V_{DS5} track to V_{DS6} and receive a high accuracy of V_{out}.

To evaluate the performance of the current-to-voltage converter, an input current swept from 0 μA to 400 μA is applied. The result in Figure 12 shows that the observed V_{out} has a goodness of fit as $R^2 = 0.999$, which indicates the high accuracy and linearity.

The power consumption of the current-to-voltage is slightly lower than the current-to-current amplifier because of the current reduction in the current mirror. With the various input current of 0 μA - 400 μA, the power consumption is from 1.68 mW to 2.1 mW.

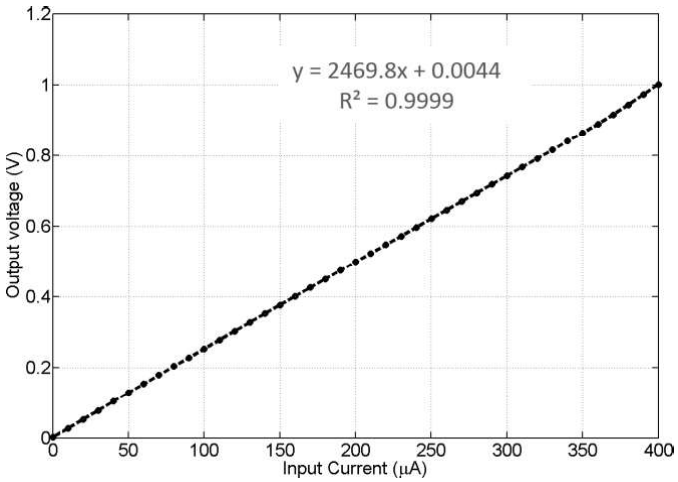

Figure 12: The characteristic i-v curve of the current-to-voltage converter

3.3.3 Analog-to-Digital Convertor

A 6-bit 1.5b/stage pipelined ADC with redundancy algorithm is created to read the analog voltage signal into digital word. For each bit-line, the sum of the current through each memristor is sent to a TIA. The TIA is used to convert current signals into voltage signals, and then is read by the ADC.

The pipelined ADC designed in the project is composed of six stages, as depicted in Figure 13. The first stage is implemented with a sample and hold amplifier (SHA), which eliminates the variation of input signal that can corrupt the conversion process. The rest of the five stages are implemented with the Multiplying DAC (MDAC) to reconstruct the analog residue voltage from the previous stage [17]. Traditional pipelined ADC always has a SHA at front of each MDAC stage, which consumes significant amount of power. The proposed pipelined ADC uses the SHA-less architecture, which implements the SHA only in the first stage, to overcome this drawback.

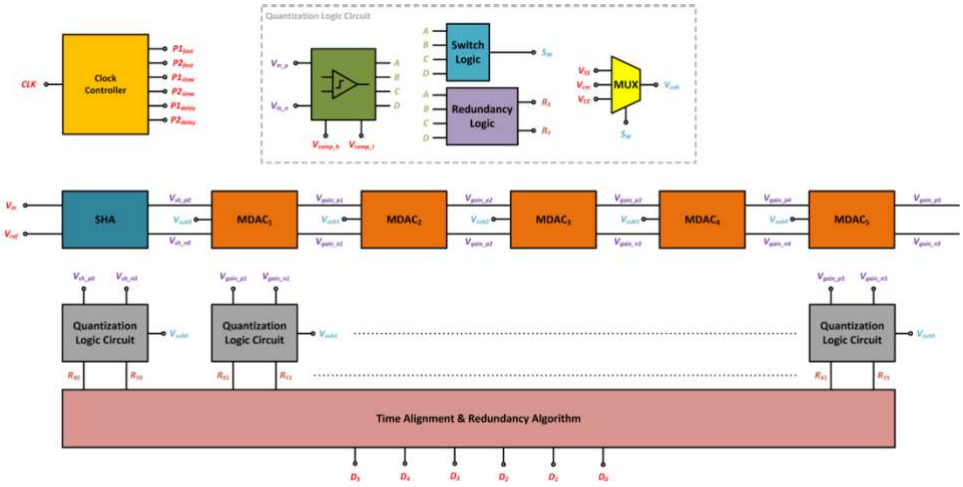

Figure 13: Simplified schematic of 6-bit 1.5b/stage pipelined ADC

As shown in Figure 13, the analog input, V_{in}, is first sampled and held by the SHA. The output from the SHA, V_{sh}, is quantized into a 2-bit digital code by four cascoding comparators and a digital encoder; meanwhile, this output is increased up by a factor of 2 and fed to the next MDAC stage. The amplified voltage signal is then subtracted by the subreference voltage, V_{sub}, which is determined based on the quantized signal from the previous stage. The analog residue, V_{gain}, continues through the pipeline, providing 2-bit per stage until it reaches the last MDAC stage. Furthermore, because the quantized bit from each stage are generated at different time instances, all the bits corresponding to the same sample are time-aligned with shift register before feeding it to the redundancy algorithm logic circuit. Finally, the redundancy algorithm logic circuit reconstructs the shifted quantized bit from each stage and digitizes into the 6-bit digital code corresponding to the analog input.

In the traditional 1 b/stage pipelined ADC, the analog residue is only compared with the reference voltage, $\frac{1}{2}V_{DD}$, by a comparator, which limits the accuracy of the resolution. The 1.5 b/stage redundancy algorithm conceptually consists of replacing each given comparator with two different levels of reference voltage, as illustrated in Figure 14, which are surrounded at the original $\frac{1}{2}V_{DD}$ level. By doing this, the residue of each stage is now half of what it previously was.

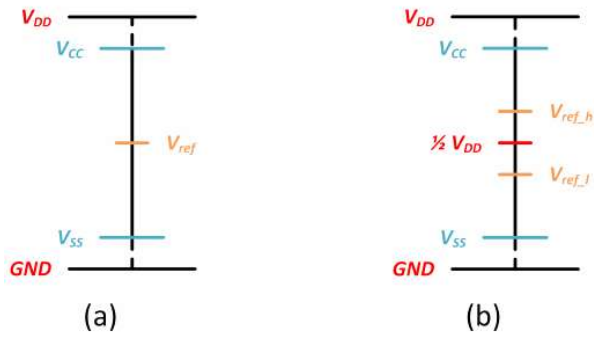

Figure 14: (a) traditional 1 b/stage pipelined ADC; (b) proposed 1.5 b/stage pipelined ADC

The redundancy algorithm logic circuit, as depicted in Figure 15, contains a cascading shift register and full-adder to process the output code. In the proposed pipelined ADC architecture, the first stage needs to wait until the last stage finishes the quantization of its corresponding analog input, in order to synchronously trigger the full-adder in the redundancy algorithm logic circuit.

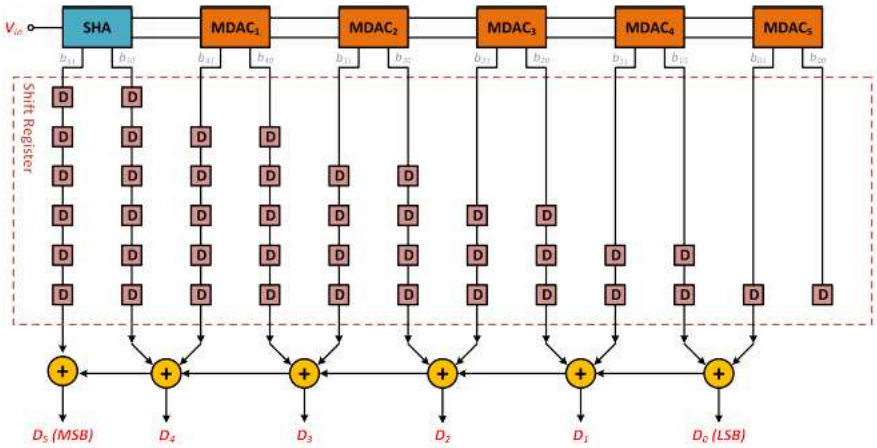

Figure 15: Simplified schematic of redundancy algorithm logic circuit

To digitize the output code based on the six 2-bit redundancy code, six full-adders are implemented to sequentially combine the redundancy bit, as depicted Figure 16.

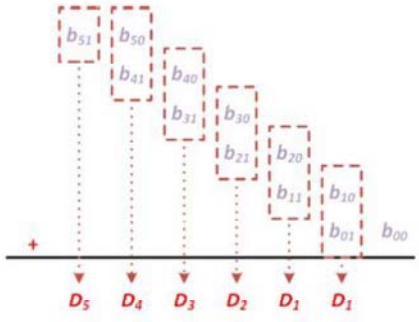

Figure 16: Summation technique of 1.5 b/stage redundancy bit

The 6-bit pipelined ADC is designed using 0.13 μm CMOS technology from Global Foundry. The expected results are summarized in Table 1. The design was incorporated in Chip 3 in Duke University report.

Table 1: Summary of Design Performance

Specification	Performance Result
Technology	IBM 130 nm CMOS
Area	0.176 mm^2
Resolution	6-bit
Input Dynamic Range	1 V_{pp} (0.1 V to 1.1 V)
Supply Voltage	1.2 V
Reference Voltages	$V_{ref} = 0.6$ V $V_{comp\_l} = 0.475$ V and $V_{comp\_h} = 0.725$ V $V_{SS} = 0.1$ V and $V_{CC} = 1.1$ V
Sampling Frequency	$\leq$ 20 MS/s
DNL	-0.3 to +1 LSB
INL	-2 to +1 LSB
SNR	29.98 dB
Power Consumption	12.67 mW

4.0 RESULTS AND DISCUSSION

4.1. System-level Testing in Duke University

We have incorporated our designs into two tapeouts: one for the spike-based system and the other one for the level-based system. The spike-based system chip contains the H-IFC as the part of the output circuit. The level-based system chip has the DAC as the part of the input circuit, and the TIA and H-IFC as the output circuit[1]. The system level tests show both systems are functional, as indicated by Prof. Li's report.

4.2. Testing of H-IFC

A PCB board is designed and fabricated for testing the H-IFC, which is one of the test keys in the tapeout. The input of the H-IFC is connected to a variable resistor and a power supply. The variable resistor is used to emulate the memristor. The output signals are monitored with an oscilloscope. The illustration and the actual setup depicts in

[1] Due to its size and power consumption, the pipelined ADC is not part of the level-based system controller. The output circuit of the level-based design still uses the TIA and the H-IFC as suggested in the original proposal.

Figure 17. The measured the spike period versus input current, which includes 4-stage frequency divider, bond pad of the chip, and the testing cable, is plotted in Figure 18. The measurement meets the expectation based on the original circuit simulation, as depicts in Figure 18. The same measurement is performed on two identical chips. The performance from two different chips are consistent with each other.

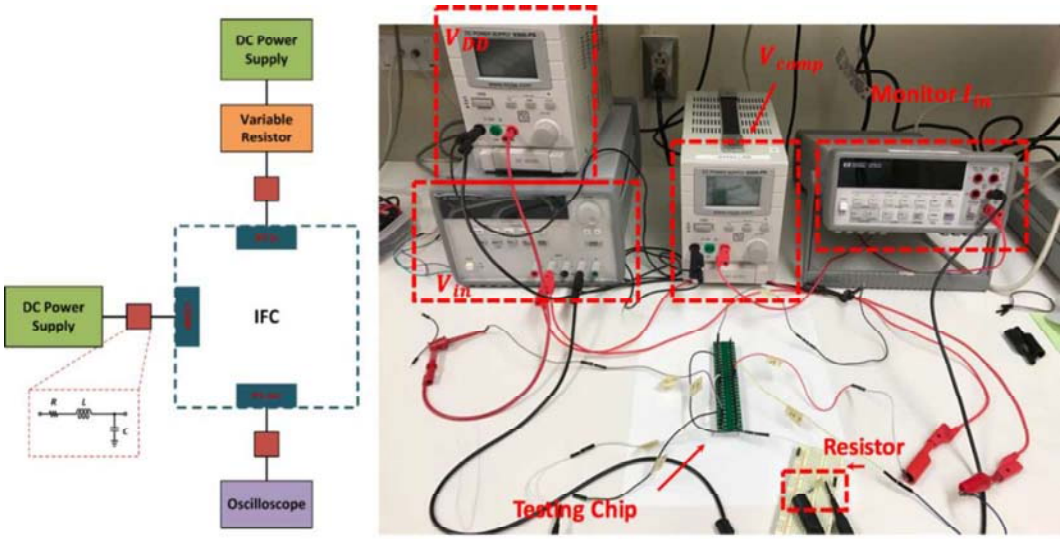

Figure 17: Test setup for the H-IFC

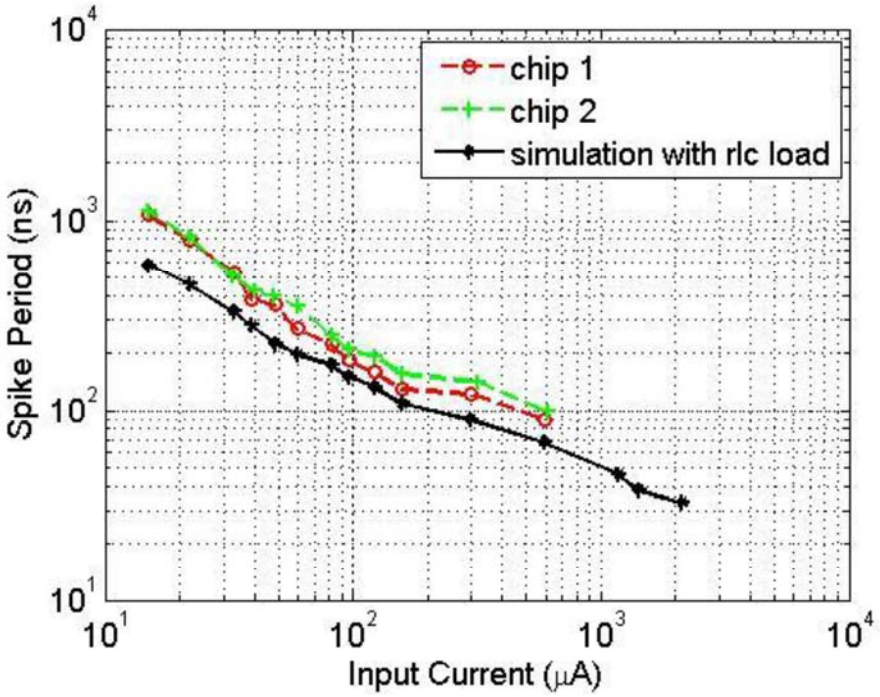

Figure 18: The measured spike period versus current

4.3. Testing of DAC

The chip for the level-based system has the test key for the DAC. The chip and its associated PCB testing board is shown in Figure 19.

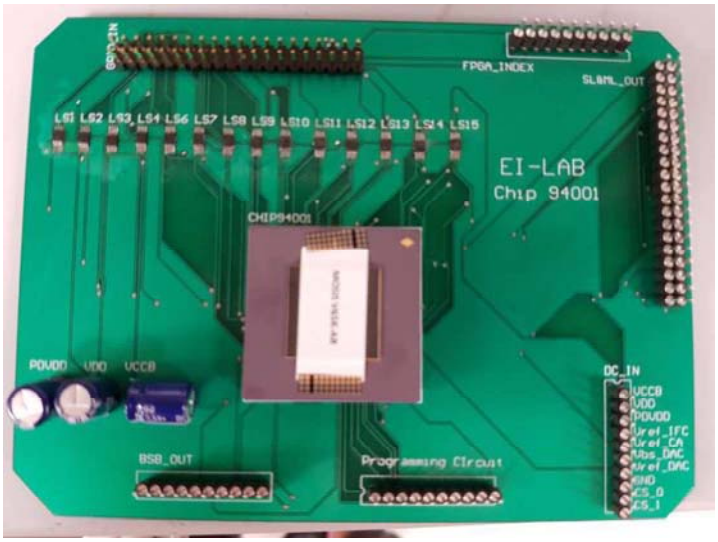

Figure 19: PCB testing board for DAC, TIA and ADC

The DAC testing setup is illustrated in Figure 20. To save input/output pins, a 4-bit digital counter is used to generate the digital input with one step up per clock. The DAC output is connected to a KΩ range resistor. The voltage across the resistor is monitored by an oscilloscope.

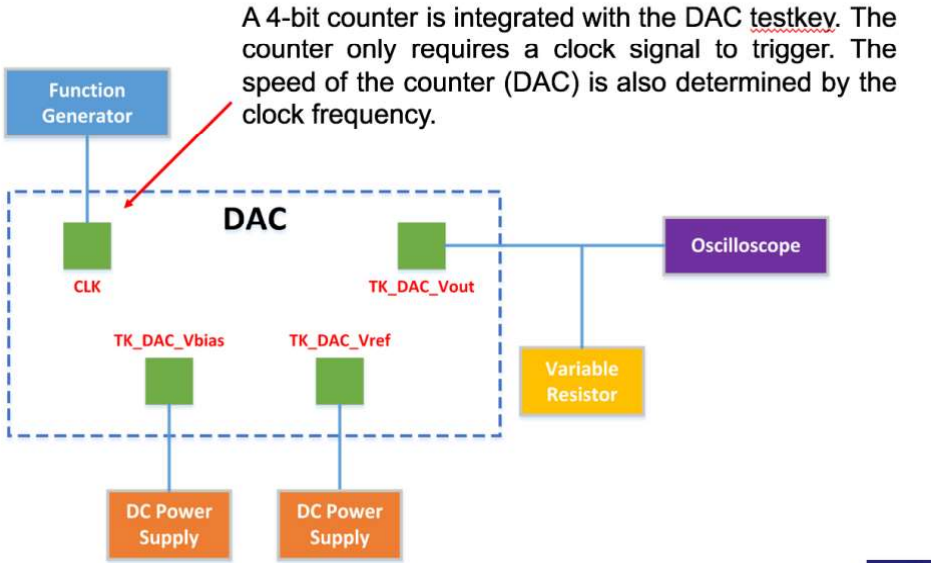

Figure 20: The test setup for the DAC

The measured output waveform is shown in Figure 21. The plot shows that the DAC is functional. The sweeping range is consistent with the design, from 0.1V ~ 1.1V

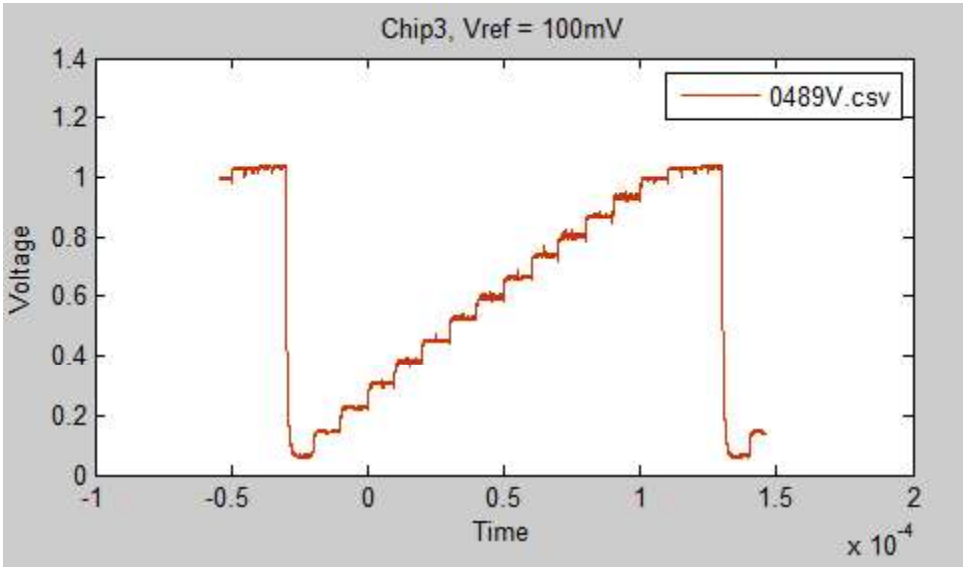

Figure 21: The DAC output waveform

4.4. Testing of the TIA

The TIA testing setup is illustrated in Figure 22. The input current is introduced by the DC power supply and a variable resistor. The output is applied to a load resistor in series with a *digital current meter* (DCM). The DCM reports the current at the output. The output current versus input current is plotted in Figure 23. The output current is able to linearly tracks with the input current.

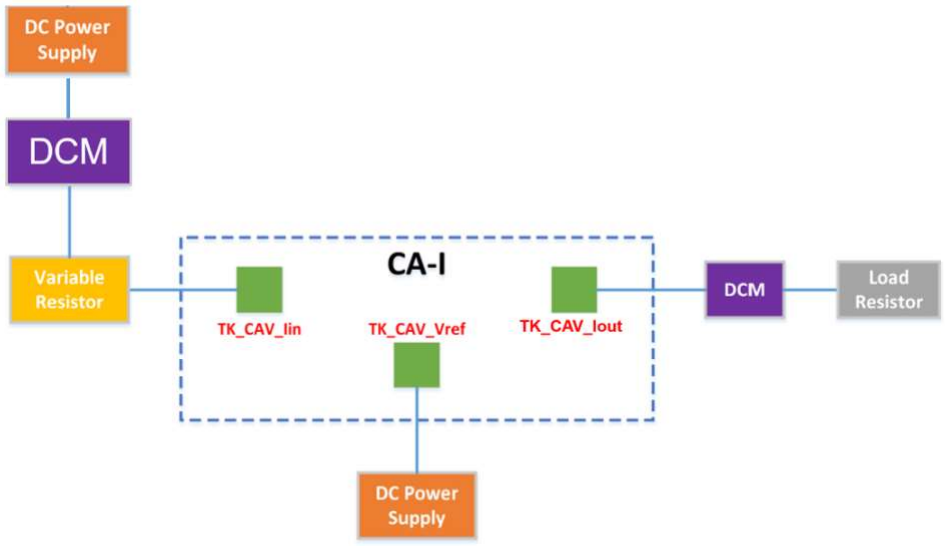

Figure 22: The test setup for the TIA

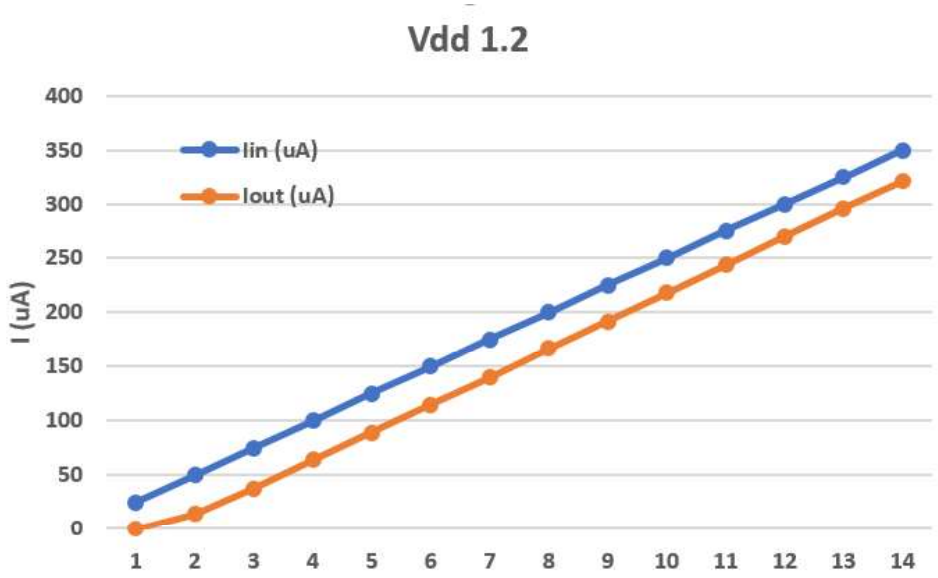

Figure 23: The TIA's input and output current

4.5. Pipelined ADC

The ADC is part of the test key. A parallel-to-serial convertor is included to reduce the number of required output pads. As mentioned in Duke University report, the digital signals that feed into these blocks are not strong enough to drive the convertor. The stand-alone ADC test is not successful.

5.0 CONCLUSIONS

In this project, we investigated and implemented analog circuit blocks for spike-based and level-based controllers, which support neuromorphic computing using memristor crossbar array. We participated two tapeouts organized by the team in Duke University. The circuits that were proposed in the original proposal: H-IFC, DAC, and TIA, have been proven functional as part of the overall system, and as stand-alone test circuits.

6.0 REFERENCES

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APPENDIX A – PUBLICATION

1) C. Liu, B. Yan, C. Yang, L. Song, Z. Li, B. Liu, Q. Wu, H. Jiang, Y. Chen, and H. Li, "A Spiking Neuromorphic Design with Memristor Crossbar," Proceedings of the 51st Annual Design Automation Conference (DAC), June 2015, article no. 14.

2) X. Liu, M. Mao, B. Liu, H. Li, Y. Chen, B. Li, Y. Wang, H. Jiang, M. Barnell, Q. Wu, and J. Yang, "RENO: A High-efficient Reconfigurable Neuromorphic Computing Accelerator Design" Proceedings of the 51st Annual Design Automation Conference (DAC), June 2015, article no. 66.

3) C. Liu, Q. Yang, B. Yan, J. Yang, X. Du, W. Zhu, H. Jiang, Q. Wu, M. Barnell and H. Li, "A Memristor Crossbar Based Computing Engine Design Optimized for High Speed and Accuracy", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 2016.

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5) H. Jiang, W. Zhu, F. Luo, K. Bai, C. Liu, X. Zhang, J. J. Yang, Q. Xia, and H. Li, "Cyclical Sensing Integrate-and-Fire Circuit for Memristor Array Based Neuromorphic Computing," IEEE International Symposium on Circuits and Systems (ISCAS), May 2016.

6) C. Liu, Q. Yang, C. Zhang, H. Jiang, Q. Wu and H. Li, "A Memristor based Neuromorphic Engine with a Current Sensing Scheme in Artificial Neural Network Applications," Asia and South Pacific Design Automation Conference (ASPDAC), January 2017.

APPENDIX B – PRESENTATIONS

1) Meeting name: The 16th International Symposium on Quality Electronic Design
Purpose: Public tutorial
Location: Santa Clara, CA
Date: March 2015
Attendees from this project: Hao Jiang
Presentation: Neuromorphic Computing based Processors

2) Meeting name: IEEE International Symposium on Circuits and Systems (ISCAS) 2016
Purpose: Public conference
Location: Montreal, Canada
Date: May 2016
Attendees from this project: Hao Jiang
Presentation: "Cyclical Sensing Integrate-and-Fire Circuit for Memristor Array Based Neuromorphic Computing"

APPENDIX C – ABSTRACT

In this project, we designed and implemented peripheral analog integrated circuits to facilitate the neuromorphic computing using memristor crossbar array. Specifically, we designed and implemented the high-speed integrate-and-fire circuit for the energy-efficient spike-based neuromorphic computing system, and the digital-to-analog convertor, the current amplifier, and the pipelined analog-to-digital convertor for the high-performance level-based neuromorphic computing system using Global Foundry 0.13μm standard CMOS technology.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ADC	Analog-to-Digital Conversion
AFRL	Air Force Research Lab
BL	Bitline
DAC	Digital-to-Analog Conversion
DCM	Digital Current Meter
H-IFC	High-speed Integrate-and-Fire Circuit
LTD	Long Term Depression
LTP	Long Term Potentiation
MCA	Memristor Crossbar Array
MDAC	Multiplying DAC
MIM	Metal-Insulator-Metal
PDK	Product Development Kit
SHA	Sample and Hold Amplifier
SRAM	Static Random Access Memory
ReRAM	Resistive Random Access Memory
TIA	Trans-Impedance Amplifier
WL	Wordline