Radiation Effects in Graphene Field Effect Transistors (GFET) on Hexagonal Boron Nitride (hBN)

THESIS

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Abstract

Hexagonal boron nitride (hBN) has been proposed as an improved substrate material in place of SiO_2 for graphene electronic devices, especially graphene field effect transistors (GFETs), because of its lattice match to graphene and the absence of dangling chemical bonds on its planar surface. The performance of GFETs on hBN substrates is becoming increasingly well documented, but little is known about the tolerance of these devices to high doses of ionizing radiation, such as that encountered in many potential DoD applications. In this study, the current-voltage transconductance curves of top-gated GFET devices were measured before and after exposure to 1.7 Mrad (SiO_2) total dose from ^{60}Co gamma rays. Post-irradiation, the devices showed a distinct positive voltage shift in the charge neutrality point (a.k.a. Dirac point) of the transconductance curves averaging 1.3 volts. This shift suggests an increase in the effective hole doping of the graphene caused by a net trapped charge density of $3x10^{12}$ electrons cm^{-2} at one of the graphene interfaces, or possibly trapped electrons at the interface between the hBN layer and the underlying sapphire substrate. The voltage shift associated with this trapped charge was observed to build up for two days post-irradiation before saturating and remaining stable at room temperature. The post-irradiation magnitude of source-drain current showed a slight increase at the Dirac point, staying within 10% of the pre-irradiation levels. The carrier mobility extracted from the transconductance curves also showed a slight increase, remaining on average within 25% of pre-irradiation levels. Possible mechanisms for radiation-induced hole doping of the graphene are briefly

considered, but additional experiments are required to distinguish between these possibilities. The observation of only modest changes in the transconductance curves following this relatively high total ionizing dose shows promise for the radiation resistance of these devices.

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Dedicated my mother who handed me a check to apply to Purdue because "you won't make any money studying political science".

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I. Introduction

1.1 Hypothesis

The governing hypothesis of this research is that hexagonal boron nitride is a radiation tolerant substrate material for graphene field effect transistors. From previous research, a shift in the Dirac point towards higher applied gate voltages is expected after irradiation due to environmental effects, such as oxidation, and breaking of hydrogen bonds and reforming into diatomic gas molecules [1, 2].

1.2 Motivation

If the mission has stringent operational requirements, would those components perform to standard when placed in an environment where they are subjected to radiation? This result could impact mission planning, as it would require alternatives, such as to simply avoid the environment or the shield the components from the environment. In space or some nuclear reactor applications, there is no way to simply avoid operating in an irradiation environment. Shielding takes up valuable real estate and adds weight which are critical considerations in space or nuclear reactor radiation environments. There is therefore a pursuit of electronic materials that can withstand the radiation expected in high radiation environments.

Electronics in high radiation environments are sensitive to interactions that can cause malfunctions. One such interaction is charge buildup in oxides and insulators caused by high energy electrons, protons or cosmic rays [3, 4]. Electronics that are used in the space environment or in high radiation areas will need to be of such a design that the radiation does not significantly degrade device operation. Building redundant mechanisms in the electronic systems may not be enough if all devices suffer from the same radiation effects.

Since the creation of metal-oxide-semiconductor field-effect transistors (MOSFETs), a steady decrease in size, known as scaling, of the devices has occurred. While this has increased the processing power density by adding transistors to integrated circuits, it has created a new concern due to short channel effects. Most microelectronic devices continue to use the semiconductor silicon as a basis for device construction. As the devices shrink, the field regions (those surrounding the device) have more of an effect on the transistor, and characteristics of the device shift away from what is expected from larger area devices. Moore's Law which states that the number of devices on circuits should double every two years. The devices are expected to reach a level too small for silicon to be used as a basic building material due to short channel effects. The short channel effects of concern are barrier lowering and velocity saturation which can cause a shift in the threshold voltage.

Drain induced barrier lowering is caused by the threshold voltage roll-off lowering the threshold voltage to a point that the transistor turns on. In longer channels the source and drain are far enough apart that the substrate and gate shield carriers from fields caused by the drain voltage. In short channels, the drain voltage can create a field close enough to the channel to make it possible for carriers to travel through the channel at lower applied voltages.

Velocity saturation is the maximum velocity a charge carrier can attain in the presence of electric fields. For increasingly smaller scaled transistors the electric fields created may be smaller than the average travel length of carriers and can lead to ballistic transport where the carriers behave as photons. When a device reaches velocity saturation, the current does not react linearly to applied voltage in accordance to Ohm’s law. This can be used as an advantage if trying to limit current or a hindrance when current is needed to be variable. Graphene have been viewed as a material that may be able to take advantage of the ballistic transport regime.

Threshold voltage roll-off occurs when the channel depletion region becomes smaller than the drain and source depletion widths. The voltage needed to turn the channel on decreases. This, in turn, makes the threshold voltage less negative for p-channel devices and less positive for n-channel devices.

A bold prediction is that by 2020, devices will be too small to continue contemporary scaling after reaching the 7 nm process technology node [5]. The nodes have been defined as half scaling of previous devices. Every time the chip industry scales down it requires even more precise machinery. Intel has stated that 10 nm chips are as far as they will go with scaling silicon devices [6]. Other means under consideration for obtaining comparable performance gains are using more lightweight and pliable materials or finding ways to increase the electrical performance of the smaller scale devices. Use of all-metallic transistors has been proposed, but these would need to be atomically thin due the screening of the electric field at extremely short distances [7]. Since 2005, the

International Technology Roadmap on Semiconductors has encouraged the “More than Moore” concepts such as system on chip and system in package concepts [8]. The emphasis in these designs will be beyond complementary metal-oxide-silicon (CMOS) technology. The emerging research from the roadmap is focused on a new switch to process information exploiting a new state variable to provide functional scaling beyond scaled CMOS. Some of the design types that can go beyond CMOS are carbon based nano-electronics, spin-base devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system switches [8]. This research investigates the carbon-based nano-electronics part of the roadmap by examining graphene field effect transistors (GFET) before and after gamma irradiation.

Graphene has been proposed due to its high conduction properties and 2-D structure. Graphene has a very high electrical conductivity (10^8 S/m) and can be intrinsically hole and electron carrier dominant. This ambipolar field effect enables graphene to be tuned continuously between electrons and holes [9]. The unique nature of graphene’s charge carriers makes it of great interest to the device designers. Its charge carriers mimic relativistic particles with the Fermi velocity replacing the speed of light. However, when graphene is used as the active layer in a field effect transistor, its conduction can be dominated by environmental effects. Another 2-D material, hBN is uniquely qualified as both a supporting substrate material and a passivating dielectric. Its use as a dielectric is appealing due to the ability to allow a substrate-supported geometry while retaining the quality achieved with a suspended sample [10]. It also has shown to be a good radiation shield when used to encapsulate graphene [2]. The combination of these two materials is intended to make very thin electronic devices which can withstand irradiation and not suffer from short channel effects that would be expected from the scaling of silicon devices. From scaling theory, short channel effects can be suppressed by thin channel regions [11]. Taking advantage of the two dimensional nature of graphene, field effect transistors can be made with extremely thin channels. The scaling theory applies to semiconducting channels with band gaps. This creates the need to induce a gap in the GFET which is done in this research by combining graphene with hBN. Graphene is considered as a channel conductor because of its advantages as a two dimensional material. Those advantages include its flexibility, ultra-lightweight mass, and mechanical strength. In this research, graphene as a channel material in a field effect transistor was analyzed to determine if such a device would be affected by gamma irradiation at fluxes of typical operational radiation environments.

1.3 Background

Radiation effects on electronics have been studied and there are known degradation mechanisms that need to be mitigated to ensure high quality performance of electronic systems. High energy electrons created by photon interactions can ionize atoms, generating electron-hole pairs. The creation of electron-hole pairs in insulating materials can cause long term effects through charge trapping. Charge trapping in a gate material can invert the channel interface causing leakage current to flow in the off state condition resulting in an increase in the static power supply current of an integrated circuit [3]. This can lead to poor performance of electronics dependent upon ohmic layers.

Radiation can also affect devices in other ways at different dose rates. For examples in low dose rate environments, field dependent device performance can change due to enhanced low dose rate sensitivity (ELDRS). The ELDRS effect is only observed over long time exposures and cannot be replicated using high dose rates in shorter times. Depending upon the device structure and radiation type can lead to stochastic effects, such as single event effects, which changes the experimental methodology. These types of effects were not considered as part of the present work.

Despite size and mobility limitations, silicon remains the primary semiconductor materials in modern devices. However, it is considered to be at or beyond the limit where further scaling can be applied. Graphene is thus being investigated as a replacement for silicon in certain applications. Specifically graphene field effect transistors are being considered to replace silicon field effect transistors in high density, high current applications. Since graphene is known to be exceptionally radiation tolerant, the device performance degradation is largely due to the underlying substrate or adjacent insulating layer [2]. Silicon dioxide as a substrate is known to be affected by radiation, so its use limits electron mobility in GFETs due to the additional scattering mechanisms induced by the substrate including charged impurities [12]. This has also been a motivating factor in seeking materials that allow greater mobility within the constraints of small GFETs.

1.4 Research Objective

The primary objective of this research is to analyze the total ionizing dose radiation hardness of GFETs that employ hBN substrates.

1.5 Previous Research

There have been previous studies concerning graphene field effect transistors and hexagonal boron nitride. Previous AFIT research focused on hBN as a thin film layer in metal insulator silicon devices [13, 14] and as a field effect transistor [15]. The irradiation was conducted at the Ohio State University's ^{60}Co gamma irradiation facility. The gamma total ionizing dose matches that used for past research and is representative of the dose that is accumulated over the mission life of some satellites operating in harsh space radiation environments [13].GFET response to proton and x-ray irradiation was found to be strongly dependent on the environmental factors at the graphene/material or graphene/air interface following irradiation [15]. Substrate displacement damage and atmospheric adsorbents were determined to impact the radiation hardness of graphene. One reported mechanism for degradation has been the generation of reactive oxygen and ozone due to gamma rays interactions [1].

Results from Zhang, C. et al. with encapsulated graphene hBN devices showed modest shifts in the current and Dirac point of the graphene. The devices were fabricated with a graphene monolayer between an upper and lower 30 nm hBN layer and exposed to a 10 keV x-ray source. Charge trapping near the graphene/BN interface was observed after x-ray exposure, but the shifts in the current and Dirac point were relatively small and may not inhibit device performance [2]. Their Dirac point shifts were evaluated in stages during irradiation with doses up to 1 Mrad (SiO_2) resulting in a negative shift with each stage, thereby a Dirac shift moving more to the positive applied voltage.

Childres, I. et al. exposed GFET to a 30 keV electron beam, which caused negative shifts in the Dirac point of the device. This was attributed to n-doping in the graphene from radiation interactions in the substrate. The graphene samples were fabricated by mechanical exfoliation onto a boron-doped Si wafer covered with 300 nm of SiO_2. In addition to the Dirac point shift there was also an observed reduction in the mobility indicating a doping of the graphene caused by the interaction of the electron beam and substrate [16].

An investigation of total ionizing dose effects in GFETs on passivated SiO_2/Si substrates by Cress et al. indicated that increases in the concentration of positive oxide trapped charges near the interface limited mobility in holes and electrons [17]. They found that an electron mobility degradation was more rapid than hole degradation by correlating electron density and minimum conductivity. Their team used CVD grown graphene and transfer to form back-gate graphene test structures and that were irradiated using a ^{60}Co source at a rate of 950 rad (Si)/s for both 100 and 80 hours.

Oxide charge trapping near the graphene/SiO_2 channel interface was identified as the main contributing mechanism to radiation-induced degradation by Esqueda et al. They concluded that GFET devices with top-gated structures are susceptible to total ionizing dose effects from the buildup of oxide-trapped charges [18]. The devices used top-gated GFETs with epitaxial graphene layers grown on Si-faced 6H-SiC substrates via Si sublimation. The devices were exposed to a ^{60}Co source with a dose rate of 910 rad (Si)/s to a total dose of 1000 krad (Si).

The work of Francis et al. indicates that the local environment can significantly affect the radiation response of graphene devices. Their team used back-gated GFETs with graphene films transferred onto a thermally grown SiO_2 on a silicon substrate [15]. The devices were irradiated with 10 keV x-ray source to 2 Mrad (SiO_2). An increase in the drain current attributed to oxygen-related doping was found after radiation-induced holes annealed.

The study by Kleut et al. found the graphene was mildly p-type with dose following gamma-irradiation [19].. Their samples were few-layer graphene thin film surfaces and they were irradiated (unbiased) 25, 50, and 110 kGy (2.5, 5, 11 Mrad). The samples were prepared using a crystalline graphite powder suspended in deionized water. The mixture was sonicated in an ultrasonic bath and then put through a centrifuge. The films were pressed against a glass substrate and filter paper was used to dry the film. The films were irradiated with a ^{60}Co source in air.

The dissertation of Alexandrou demonstrated mechanisms of ionized charge buildup in the substrate and displacement damage effects on GFET performance as well as impacts from atmospheric adsorbents from the surrounding environment [1]. The irradiation was conducted using a ^{60}Co source at 1 kGy/hr (100 krad (Si)/hr) to 2.2 kGy (220 krad (Si)) and 26.5 kGy (2.65 Mrad (Si)). The Dirac shift observed in these devices was to the positive voltage and drain current increased after irradiation.

II. Theory

2.1 History of Graphene

Graphene was first isolated by Andre Geim and Konstantin Novosolev in 2004 by repeatedly removing flakes from bulk graphite with adhesive tape. They were awarded the 2010 Nobel Prize in Physics “for groundbreaking experiments regarding the two-dimensional material graphene” [20]. In a letter to the editor of APS News in January 2010, Geim cites the earliest paper of epitaxial growth graphene to 1975’s Surface Science and an even earlier 1962 German observation of atomically thin graphic fragments in Naturforschung. The Canadian theoretical physicist P.R. Wallace had his “The Band Theory of Graphite” published in Physical Review in 1947 in which graphite as a semiconductor with zero activation energy was discussed. Even though the theory and research into graphene had been ongoing it was not until the 21st century that monolayers of graphene were produced. The same Geim and Novoselov were published in 2004 reporting a naturally occurring two-dimensional material they described as a flat fullerene molecule [7]. Their team was able to make graphene films by mechanical exfoliation, that is, repeated peeling of the graphite. Once in the flat monolayer, graphene can be stretched, rolled, combined, or just shaped into the geometry that is desired.

Graphene is a strong 2-D allotrope of carbon. The 2-D nature of graphene means that charge carriers are confined to a surface just one atom thick which may enable device scaling beyond silicon’s [21]. The structure of graphene can exist in its 2-D structure due to carbon to carbon bonds that are so strong they prevent thermal fluctuations from destabilizing the structure. There is no intrinsic energy band gap in graphene. To use traditional transistor theory a band gap must be realized to differentiate between on and off states. One way to introduce a band gap is using a substrate that makes two carbon sub-lattices inequivalent, thus separating electron and hole current is the graphene structure [22].

The high carrier mobility within graphene is of prime interest for transistor applications. When measured independently of a substrate, graphene has a mobility of ~9.5 x 10^5 cm^2/ (Vs) [11]. The ambipolar nature of graphene makes it difficult for applications that require an off state but the advantage is that it allows for fast switching, by changing form hole to electron dominated currents. With the expected large on-state current density and transconductance per gate capacitance, graphene has the potential to offer excellent switching characteristics and short-circuit current-gain cutoff frequency [23]. There are two transport regimes in graphene. Charge carriers can have ballistic transport at room temperature where they can travel without scattering for several hundreds of microns. Graphene transport can also be diffusive and temperature dependent due to impurities and interactions with other transistor material [24]. Interactions with the substrate play a major role in limiting the mobility in graphene, as well as surface charge traps, interfacial phonons, or fabrication residues that may lead to mobility degradation [25].

There are many ways to produce graphene. Among the most popular are mechanical exfoliation, epitaxial graphene, or chemical vapor deposition (the method used in the present research). The mechanical exfoliation technique is simply applying adhesives over and over to the graphite surface and peeling. This is a very time consuming and imprecise method but can still result in high quality crystallites. Epitaxial graphene is grown over support substrates and requires carbon-containing substrates, like SiC, This method is compatible with current electronic fabrications techniques such as growing graphene on SiO_2 substrates. Chemical vapor deposition (CVD) is a method that allows large scale films of graphene onto thin metal layers. The metal is exposed to a flow of hydrocarbon gas at high temperatures causing saturation of the metal. This is followed by rapid cooling which leads to a decrease in the solid solubility of carbon in the metal and precipitation of carbon in graphitic films [25].

2.2 Hexagonal Boron Nitride

Hexagonal boron nitride (hBN) is composed of alternating nitrogen and boron atoms that form a 2-D hexagonal geometric layer arrangement. It has a theoretical lattice constant of 0.2536 nm and interlayer distance of 0.354 nm [26]. These properties are very close to that of graphene, which has a lattice constant of 0.246 nm and interlayer distance 0.335 nm [27]. The atoms in each layer of hBN are bound together by strong covalent bonds and the stacked layers are held together by weaker van der Waals bonds. This material is chosen as a substrate layer due to its lattice structure being the same honeycomb sp^2-bonded layers as graphene and because the van der Waals bonds are inert in the vertical direction. The hBN is an insulating material with an absence of free electrons due to a strong covalent B-N bond. The hBN is an appealing substrate because it has an atomically smooth surface that is relatively free of dangling bonds and charge traps [10]. It has a direct band gap in the 5.5 eV range. For electronic applications, the crystalline form of hBN is of greatest interest. This is a simple crystal structure that can be grown by chemical vapor deposition (CVD). Single crystalline structures contain fewer charge trapping centers which allows for electrons and holes generated in ionizing radiation to be quickly removed [28]. Using hBN as a substrate should allow irradiated GFETs to perform similarly to pre-irradiation levels as measured in *I-V* curves through these advantageous crystalline properties. It is suggested currently that hBN can be very tolerant of high doses of radiation, but due to non-ideal crystalline hBN which can be produced at this time, radiation-induced dielectric breakdown and trapped charge buildup have been identified as potential failure mechanisms [29, 14].

2.3 hBN/Graphene Heterostructures

Graphene and hexagonal boron nitride (hBN) heterostructures have attracted considerable attention in recent years to maintain graphene's unique properties with ideal two-dimensional protective layers of hBN for use in a wide range of potential applications [30]. The interface heat conduction becomes a major limiting factor for the development of high performance graphene based devices. By introducing hydrogen to react with carbon in the heterostructures of graphene/hBN, the interfacial thermal resistance between graphene and h-BN can be reduced by 76.3%, indicating an effective approach to manipulate the interfacial thermal transport [31]. Epitaxial growth has been proposed and researched for single-domain graphene on hBN [32]. This growth seeks to limit the drawbacks of the transfer process such as structural uncertainties of lattice orientation, sample uniformity, and interface contamination. It has been shown experimentally that the relative amount of hBN to graphene can modify the physical properties of the heterostructures [33]. Increasing the hBN concentration and cluster size results in band gap opening [34, 35], and decreasing the relative amount of hBN increases the electrical conductivity [36]. In the Xu, B. et al. study it was found that the number of mid-gap states depended on the geometric shape and size of the BN material [34].

2.4 Graphene Field Effect Transistor (GFET)

The graphene field effect transistor is a transistor using a graphene layer between two electrodes and the application of a gate voltage to govern the conductivity of the graphene. The graphene layer is the channel through which current conducts. The benefits of graphene as a channel are primarily in its 2-D nature. This only allows conduction to occur in the horizontal but not vertical direction. The boundaries on particle movement allow electrons to travel at greater speeds and act as massless particles. The electron dynamics in graphene are best modeled by a relativistic Dirac equation, which describes a linear relation between energy and momentum in which the Fermi velocity of electrons or holes replaces the speed of light. The dispersion curve then implies that the electron's mass vanishes throughout a large range of momentum values in the crystal lattice. The vanishing parameter indicates that the velocity of the electrons confined on graphene remains constant and their transport properties become like those of massless particles [37]. Graphene is very sensitive to its surrounding environment.

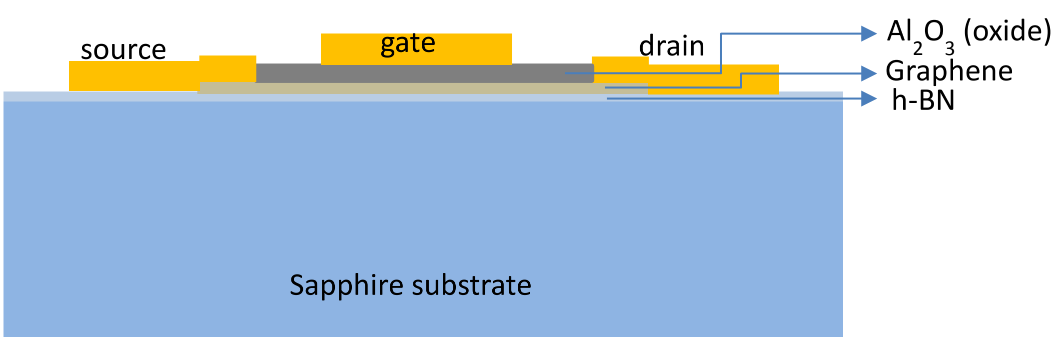


Figure 1. Top gated hBN GFET Cross Section

These sensitivities require a passivation layer. The devices tested are top gated GFETs with a metal gate of nickel and gold, source and drain nodes of titanium, platinum, and gold, and an aluminum oxide layer placed on top of the graphene monolayer. The hBN layer is between the graphene layer and sapphire substrate as shown in Figure 1. An oxide layer of 20 nm thick aluminum oxide and the thin layer of hBN which is a few nanometers thick surrounds the graphene layer, which is 1-2 nm thick. The sapphire substrate layer is around 350 microns. The source and drain contacts are layered metals of 20 nm Ti, 30 nm, Pt, and 350 nm of Au. The gate contact is 50 nm of Ni on top of 300 nm of Au. The GFETs were created from a standard mask with differing gate lengths from 0.5 to 10 micrometers and a standard gate width of 150 microns. The pads used for measurements are labeled in Figure 2.

In a top-gated field effect transistor, the top gate is the control electrode of the transistor. Applying positive voltage to the gate forms an electric field through the oxide to induce charge carriers in the graphene channel. The carrier density can be controlled

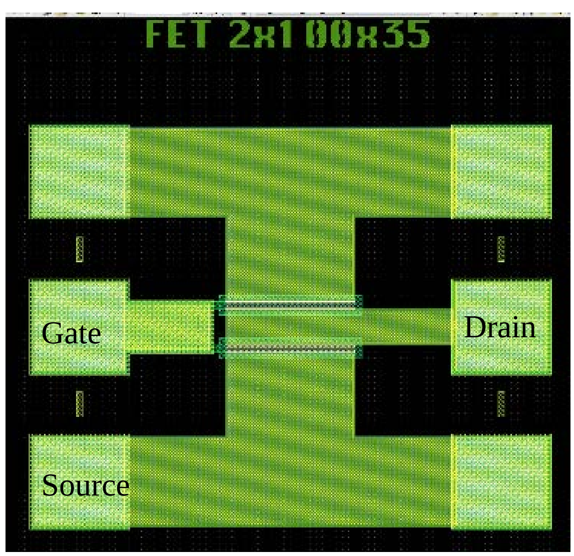


Figure 2. Top gated hBN GFET Top View

by the applied voltage. The applied voltage across the GFET causes current to be carried between the source and drain through the graphene channel. The ambipolar nature of graphene allows GFETs to operate without being doped.

The fabrication of top-gated GFETS requires a uniform gate dielectric deposition technique on graphene with high dielectric constant and reduced interface states density [38]. The transistors made for this research were fabricated by AFRL but contracted out for the application of graphene to a private company, Graphenea. Graphenea uses a chemical vapor deposition technique to grow graphene films on various substrates.

A goal of producing graphene transistors is to reach terahertz integrated circuits. One group achieved 100 GHz cutoff frequency from a two inch graphene wafer [39]. Another group produced one-two layered epitaxial graphene on SiC which produced the first RF graphene field-effect transistor [23]. Their research have shown that the GFET performances have surpassed that of GaAs transistors. The major innovation has been using an interfacial polymer layer separating graphene from its metal gate dielectric [25]. The mobility of CVD graphene transferred onto multilayer hBN is comparable to that of exfoliated graphene [40].

2.5 Radiation Effects on Graphene Structures

The nature of hBN is that it has very few dangling bonds which means that degradation of devices using hBN as a substrate are reduced compared to the degradation of SiO_2 substrate devices. Displacement damage is caused by Compton scattered electrons through high energy photon interactions.

Gamma irradiation can have an impact on GFET performance by creating electrically active defects in substrates and increasing the trap density between interfaces [1]. Other studies have shown displacement damage mechanisms on graphene’s lattice structure [41]. Gamma rays interact with materials ejecting electrons by three processes that are energy dependent: photoelectric effect, Compton scattering, or pair production. In the photoelectric effect, the gamma rays interact with the atom with enough energy to eject an electron from the target atom. The atom does recoil but carries very little kinetic energy. The ejected electron carries the energy of the incident photon less the binding energy required for its ejection. Compton scattering is the inelastic scattering of a photon with an electron. The gamma ray deflects off the target electron which recoils with some imparted energy from the gamma. Pair production can only occur above 1.022 MeV and is the process whereby the gamma ray becomes an electron-positron pair. The scattering of electrons creates particles which are free to interact with materials in the oxide or at the interface.

Surface damage is caused by the build-up of trapped charges in the dielectric layer. The created electron-hole pairs that either recombine or are moved by the electric field (built-in or applied). The electrons move toward the interface and holes toward metal contacts. The electrons with higher mobility are able to escape recombination and move into the substrate. The less mobile holes can get trapped at the interface which increases the oxide positive space charge. Chemical changes at the graphene interface also leads to net hole or electron doping of the graphene. The ionizing radiation produces new energy levels in the band structure at the interface. These new levels can be occupied by either electrons or holes and change the oxide charge. It is expected from other studies that the effects seen in this research will be from ionizing radiation creating additional oxide and interface traps.

The effect of radiation on GFET device performance was determined by quantifying changes in the *I-V* curves through the device gate at different bias points. Both I vs. V and Dirac point measurements were used as key to analysis. Total current at a bias point can indicate the relative change in mobility for both electron dominated current (+V gate) and holes (-V gate) The Dirac point is defined as that voltage at which the carrier domination shifts; the point where dI/dV=0. The location of this point indicates the trapped carrier species within the gate. Mobility and trap density can be calculated from the *I-V* curves and their changes. Transconductance is the ratio of the change in drain current to the change in gate voltage and can be used to calculate the mobility using the *I-V* curves. Transconductance can be determined from the *I-V* curves by taking the slope of the *I-V* curve. It is the measure of transistor amplification.

The field effect mobility is calculated using Equation (1) which shows a linear dependence on transconductance, g_m. Transconductance is calculated by using Equation (2). Transconductance is found by taking the average slope only on the left hand side of the *I-V* curve. This side was chosen as it was fully developed on all devices and could give a standard basis of comparison. Equation (3) is used to calculate the gate capacitance per unit area, C_g, using the oxide capacitance per unit area, C_{ox}. The oxide capacitance per unit area, C_{ox}, is a fixed property of the oxide materials and is found using equation (4) and the thickness of 20 nm and dielectric constant of aluminum oxide of 9.1.

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_g V_{DS}} \quad (1)$$

$$g_m = \frac{\mathrm{dID}}{\mathrm{dVgs}} \quad (2)$$

$$C_g = C_{ox} \quad (3)$$

$$C_{ox} = \frac{\varepsilon \varepsilon_o}{t_{ox}} \quad (4)$$

Using Equation (5) the change in charge trapss can be calculated. The change in traps show a buildup of radiation-induced trapped charges that image charge into the graphene layer. The positive voltage shifts indicate negative trapped charges [18].

$$\Delta V_{Dirac} = \frac{-q \Delta N_{ot}}{C_{ox}} \quad (5)$$

Defects in insulators can act as oxide charge traps. Radiation induced ionization can charge the traps, thereby establishing a fix electric field. Since radiation can induce either positive or negative charge traps, then the field can results in either the collection of electrons or holes; depending upon the trap charge sign. Positive charged traps will cause a negative voltage shift and negative charged traps cause a positive voltage shift. Oxide traps become charged with the introduction of electrons and holes into the dielectric while applying a gate bias. The charging of traps by radiation cause lateral shifts in the Dirac point.

There exist in the hBN material, sites of boron and nitrogen that have substitutional impurities of carbon atoms. The hydrogen atoms bonded to these carbon impurities can be broken by a large enough dose of radiation via interaction with radiation-induced holes The holes breaks the bond between hydrogen and the carbon on a boron site. Then the hydrogen attaches to carbon in the graphene which has a binding energy on par with the adsorption energy of the boron replaced carbon. The binding energy for hydrogen to attach to a carbon on a nitrogen site is low enough that it will usually seek to recombine with that carbon atom even when knocked loose. However, the energy necessary for diffusing hydrogen to attach to graphene carbon atoms is low enough that if they are free simultaneously they are more likely to form a hydrogen molecule [2]. The process is shown in the work by Zhang, et al [2] with the carbon substitutional impurities highlighted. The migration of holes and hydrogen to eventual two atom hydrogen molecule leaves an unpassivated carbon impurity on a nitrogen site, which is an acceptor type defect that causes an increase in hole concentration in graphene and a positive shift in the Dirac point.

Charge trapping affects the Dirac point based primarily on the charge of the traps. Modeling the gate oxide/graphene interface as a parallel plate capacitor, positive traps will induce negative charge in the graphene and shift the Dirac point to the left. Negative charge traps will induce positive charge in the graphene and shift the Dirac point to the right.

At positive applied gate bias, radiation-generated electrons are driven away from the interface region, and there is a lower recombination rate of diffusing holes. The hole diffusion is promoted by the direction of the applied external electric field [42]. This leads to a faster build-up of positive charge within the oxide. Diffusing holes can also support build-up of negatively charged defects at the interface. The devices in this research were not biased during irradiation. A positive bias would have the potential to magnify the hole interactions at the interface.

III. Methodology

3.1 Experiments

Electrical characterization measurements were collected using a Keithley Semiconductor Characterization System 4200 (SCS-4200) and Signatone analytic probe station (Figure 3). Gamma irradiation was conducted using the Ohio State University's Gamma Irradiation Facility. The Gamma Irradiation Facility is a ^{60}Co source surrounded by a 10 foot deep pool of water.

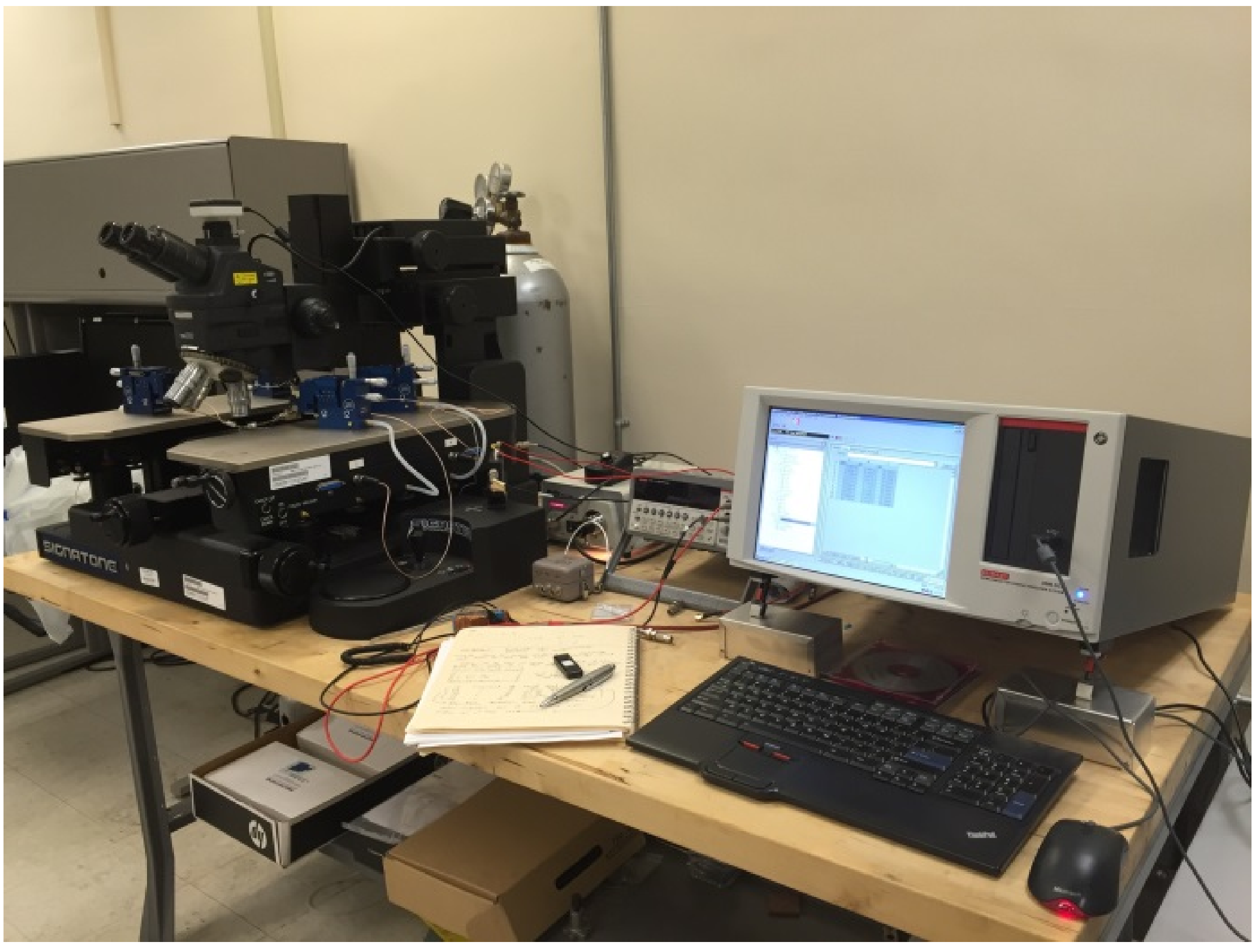


Figure 3. Probe station and SCS-4200 at AFIT

The experimental devices were placed on a dry platform that fits within a 7-inch tube and can be lowered to a desired height based on the OSU calibration graph (Figure 4) to achieve a desired dose as shown in the graph. The facility gives a dose rate of 26 krad/h (Si). The time needed for 3 Mrad (Si) (1.7 Mrad (SiO_2)) dose was 115.4 hours (4.83 days) at the optimum position in the irradiator.

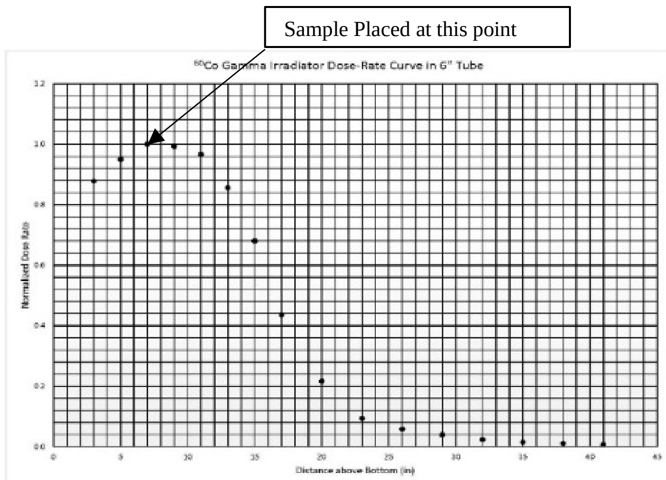


Figure 4. OSURR ^{60}Co irradiator calibration graph.

3.2 Approach

A wafer of over 70 reticles of 36 GFETs was produced by AFRL. Seven individual reticles were selected to analyze based on the recommendations of AFRL personnel to use the central reticles. The seven reticles with corresponding devices are located on the wafer as shown in Figure 5. Figure 6 shows the generic mask for each of the reticles and how the 36 devices were tracked with the grid pattern.

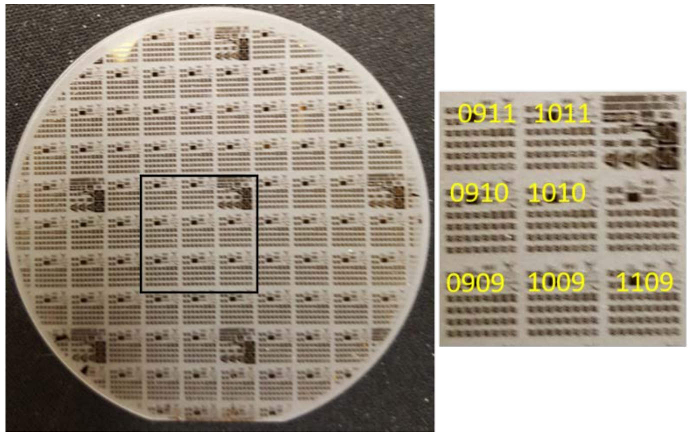


Figure 5. Device F7642 (left) and close-up (right) of reticles measured, as boxed in left side.

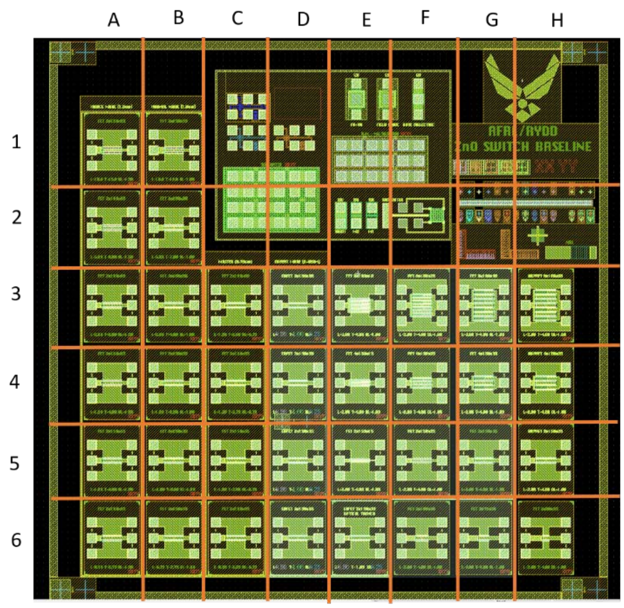


Figure 6. Generic mask for each reticle.

Pre-irradiation device characterization was an important step in the data collection process. This step identified which of the devices showed measurable responses to the gate bias sweeps in preparation for post-irradiation analysis. Once received from AFRL the devices were tested using the SCS-4200 and probe station. The first test was to identify the working devices on the reticle, by performing a gate sweep to measure drain and source current versus applied gate voltage. The sweep was done with gate voltages varying from -8 to 8 V in 0.05 V steps and keeping the drain bias fixed at 0.1 V and the source bias fixed at 0 V. An example of the desired *I-V* curve resulting from this is shown in Figure 7. This figure shows the two regions of conduction in the GFET by different carrier types and the distinct low point where the carrier type changes. The negative applied bias shows a drain current representing hole conduction in the graphene. The positive applied gate bias shows drain current representing electron conduction in the graphene. The minimum current between the two is the Dirac point where the hole and electron conduction dominated behaviors intersect. The position of the Dirac point indicates intrinsic doping levels of the substrate [42].

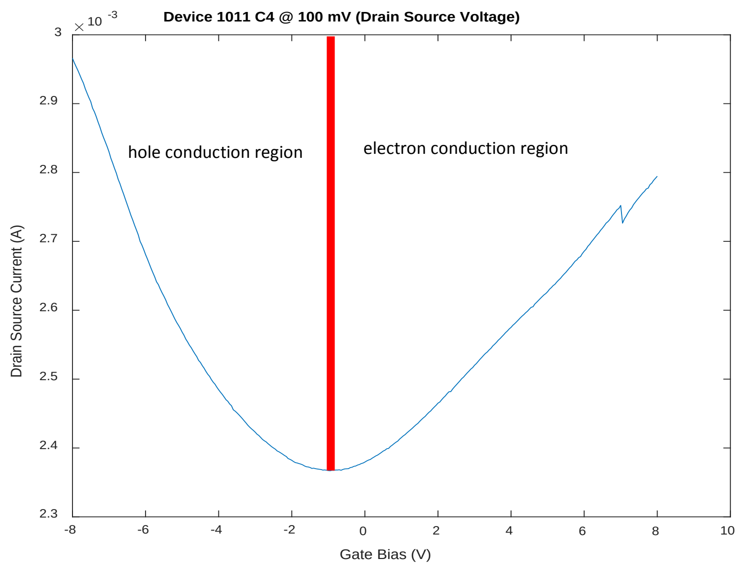


Figure 7. I-V Curve

The drain current was also measured with varying drain voltage while keeping gate voltage constant. These measurements resulted in a linear relation between the applied voltage and current and an increase in drain current from pre- to post-irradiation as shown in Figure 8. The measurements were taken with gate voltages at 0, -3, and -6 V and drain voltages increasing from 0 to 0.25 V in 0.001 V increments.

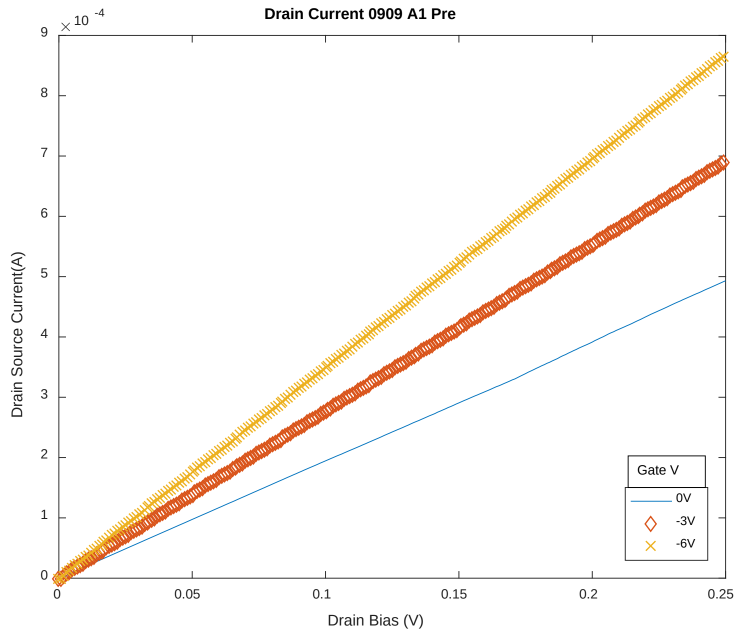


Figure 8. Drain current holding gate voltage steady pre-irradiation.

These measurements demonstrated an increase in current post-irradiation that occurred in the first measurement two hours after irradiation and was of the same magnitude after 192 hours of room temperature storage.

While measuring devices it was found that the reticle functional yield was low. This was not surprising given the maturation level of this the material and methods for fabrication and the potential for ESD and physical damage to the reticles [44]. The initial SiO_2 channel substrate devices were all unusable either in this first step or post-irradiation due to damage caused by the probe needles that were too thick. After determining a thinner needle was needed, the probes were reset and there were a total of 55 devices found to provide voltage responses from the hBN channel substrate set. The current of all three probes (gate, source, and drain) was measured to ensure the comparisons made were that of drain current and distinguishable from leakage current domination (e.g. ohmic or noise response). In Figure 11, the leakage current of a typical device is shown for measures across several days. The leakage current remained well below that of the drain current never reaching above 10^{-8} A, while the drain current was measured from 10^{-4} to 10^{-3} A on all devices.

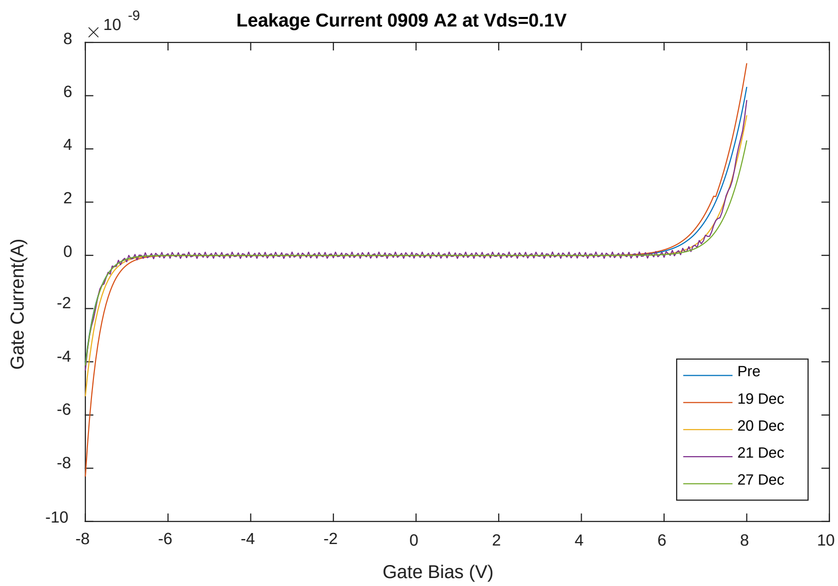


Figure 9. Leakage Current over Gate Voltage Sweeps

Post-irradiation measurements were taken 2 hours after irradiation of 1.7 Mrad (SiO_2) in order to reduce recovery.

3.3 Methods

The characterizations of the SiO_2 devices pre-irradiation were conducted using the probe station. 10 of the most consistent devices were chosen from the functioning set. For initial characterization, the compliance was set as 0.1 A, the drain bias was set as 0.1 V, and the source bias was kept at 0 V. A voltage sweep was conducted with the applied voltage starting from -8V to 8 V in 0.05 V steps.

Initial measurements were made with probe tips model SE-T, which are 5 microns thick. After initial measurements of the SiO_2 substrate GFETs, it was discovered that the probes were causing damage to the contact surfaces, leaving the SiO_2 substrate GFETs unusable. The probes were changed to SM-35 probe tips, a 0.7 micron thick tip, for the remainder of the project; which only included hBN reticles. There were seven reticles of 36 GFETs that were tested prior to irradiation. Out of the 252 devices tested, 55 were found to function as a GFET gate. These 55 were measured in gate voltage sweeps and drain voltage sweeps to gather increased data for post-irradiation comparisons.

IV. Results and Analysis

4.1 Overall Results

Pre-irradiation measurements of the GFETs provided drain-source currents of 10^{-4} to 10^{-3} A in a generally parabolic shape with applied gate V. Due to current stressing concerns (these are research devices and have no protection circuitry) the applied voltage was limited from -8 to +8 V. The minimum current (Dirac point) was somewhere near 0 V applied gate bias. Only five of the 55 measured devices did not exhibit this in the pre-irradiation measurements. Three devices exhibited substantially different currents for the positive and negative gate voltage. Two devices exhibited a sharp reduction in current near the Dirac point, an example of which is shown in Figure 10.

Following irradiation, the hBN GFET drain current increased, followed by a slow recovery to pre-irradiation levels with a shift in the Dirac point. An example of large shifts are shown in Figure 10. The initial Dirac point shift indicates a shift towards dominant hole conduction.

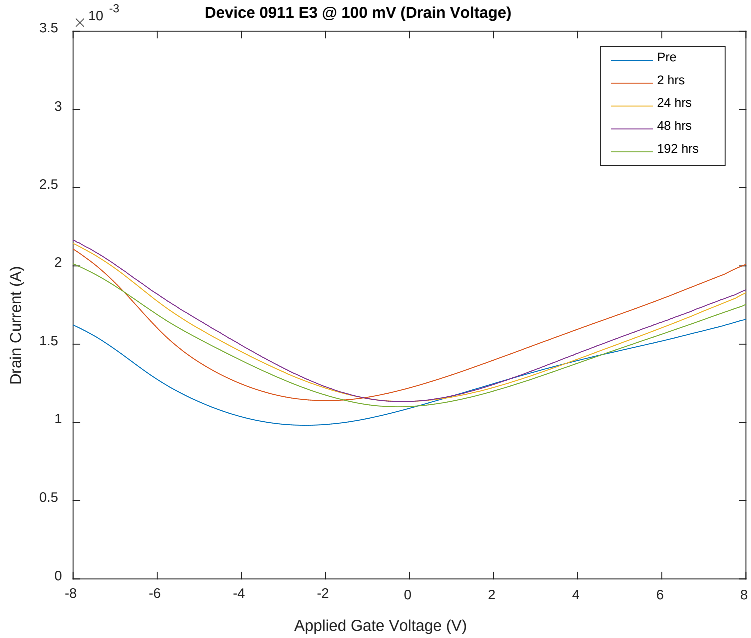


Figure 10. Drain current measurements after irradiation for device 0911 E3.

The drain current generally decreased with time after the irradiation. After 7 days with no bias applied and held at room temperature, 43 of the hBN devices drain currents were reduced at the Dirac point from their initial post-irradiation measurement by an average of -34.24 microamps; 24 devices less than a 5% increase or decrease, 19 had a difference between 5-9%, and 12 were over 10% with two of those over 40%.This was full recovery for most devices. However, 7 continued to recover with minor changes. The Dirac point voltage shift for all hBN devices was positive and it recovered to varying degrees following irradiation.

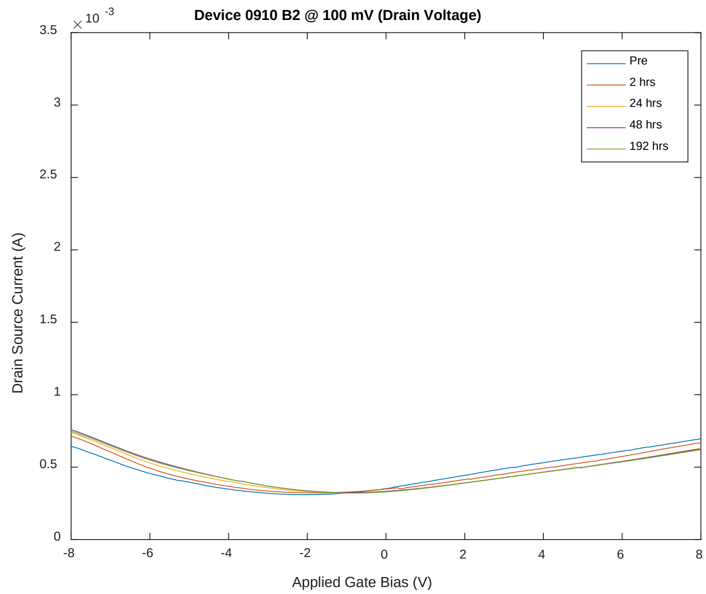


Figure 11. Drain current measurements conducted after irradiation for device 0910 B2 GFETs.

As shown in Figure 10 with device 1109 E3, the hBN device had a 30% increase in drain current after irradiation, which was reduced to a 12% increase after 192 hours of recovery. In Figure 11 with Device 0910 B2, the drain current change is negligible with the drain current increased with positive applied gate voltage, suggesting an increase in electron carrier mobility.

Table 1 provides the results of a calculation of the mobility in cm^2/Vs, assuming a channel length dependence for post-irradiation times. These values were calculated using the transconductance method utilizing equations (1)-(4) on page21. The values are an average of the devices that were measured with each channel length. Table 2 provides the average shift in Dirac point of all devices as measured post-irradiation. The Dirac shift has no correlation to channel length and the values were calculated taking all devices' values. Table 3 shows the overall average normalized mobility of all devices to pre-irradiation measurements.

Table 1. Calculated Hole Mobility pre and post-irradiation grouped by channel

Time Post-Irradiation										
L_{ch} µm	Pre	Std Dev	~2 hrs	Std Dev	24 hrs	Std Dev	48 hrs	Std Dev	192 hrs	Std Dev
0.5	7.05	1.9	7.95	1.3	7.83	1.4	6.79	4.5	8.07	1.5
1.5	44.44	14.0	48.47	16.1	38.82	12.3	47.94	11.5	44.34	12.8
2	44.39	14.8	53.57	15.4	46.73	13.9	54.63	13.9	51.53	13.1
5	59.65	16.3	67.01	12.5	63.74	11.6	65.77	14.1	67.98	10.5
10	93.09	34.1	103.70	13.8	91.9	13.6	98.49	8.3	94.55	11.2
	Mobility (cm^2/Vs)									

Table 2. Average Dirac point shift of all devices from pre-irradiation

Time (hrs)	Shift (V)	Std Dev
2	0.55	0.35
24	1.33	0.52
48	1.35	0.45
192	1.34	0.54

Table 3. Overall mobility changes from pre-irradiation

Time (hrs)	μ/μ_0	Std Dev
2	1.25	0.50
24	1.13	0.54
48	1.24	0.67
192	1.22	0.58

The calculated mobilities in Table 1 are below other published findings of suspended graphene; about 30,000 – 60,000 cm^2/V s [45]. The introduction of band gaps have decreased mobility as measured in the work by Wang et al. in nanoribbon field effect transistors. Their measured values of mobility were reported as 200 cm^2/Vs in nanoribbon devices [46]. The cause of the drastic mobility decrease in this case is likely to be that the graphene in these devices is below a gate oxide with expected interface defects that will degrade mobility.

It is unknown at what location charge trapping occurs in the devices. The most likely locations are the interfaces between the materials. The region where the sapphire substrate meets the hBN channel substrate is a distinct possibility. It is unclear what mechanism would create a negative trapped charge. The hBN/graphene interface is also a region where charge trapping may occur. This would be due to several bonds being broken by the radiation energy and recombination of separated particles.

4.2 Post-irradiation Device Groupings

In order to assess radiation damage causality, the devices were grouped by response and device parameter. Fifty-five devices were divided into five groupings according to their post-irradiation response. There were no channel length correlations to these groupings as each group had several devices with each channel length. Each grouping had devices across the seven measured reticles. The groups all had similar characteristics in Dirac shifts while correlations in the current changes due to radiation were inconclusive. There was no correlation to device location on the wafer.

4.2.1 Group I: Increased drain current for positive and negative gate voltage

Twenty-two out of 55 devices, 38%, showed a distinct increase in drain current with negative applied gate voltage following irradiation. However, for these same devices there were both increases and decreases in drain current with positive gate voltage. The

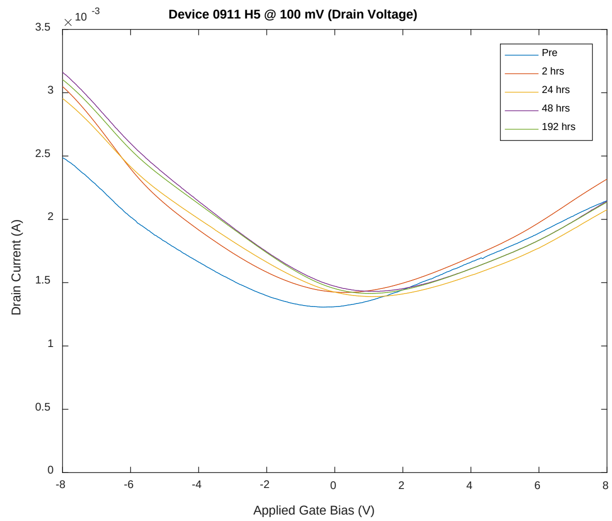


Figure 12. Current increases for negative voltages. No distinct increase or decrease over the following days at positive voltages.

drain current at the Dirac point increased on average of 9% on the first 24 hours post-irradiation, then the average drain current fluctuated within 3% of each previous day. The overall average decreased on 24 hours and 196 hours, with a minor but measurable increase at 48 hours. This grouping's shift in the Dirac points was positive during the initial 72 hours, then shifted negative 196 hours post-irradiation. Figure 12 shows a device from this grouping. The drain current for negative gate voltage increases and decreases throughout the measurement period.

4.2.2 Group II: Increased drain current for negative drain current only

Group II devices demonstrated an increase in drain current when negative gate voltage was applied and a decreased drain current when the positive gate voltage was applied. Sixteen devices, 28%, were in this group. This grouping consistently exhibited increased (magnitude) of drain current at the Dirac point, with an average Dirac point drain current increase of 1% following the first 24 hours post-irradiation and a measurable decrease at 196 hours of less than 1%. This group's Dirac shift was smaller than Group I or III at 48 hours. Figure 13 is a measurement for a device in this group.

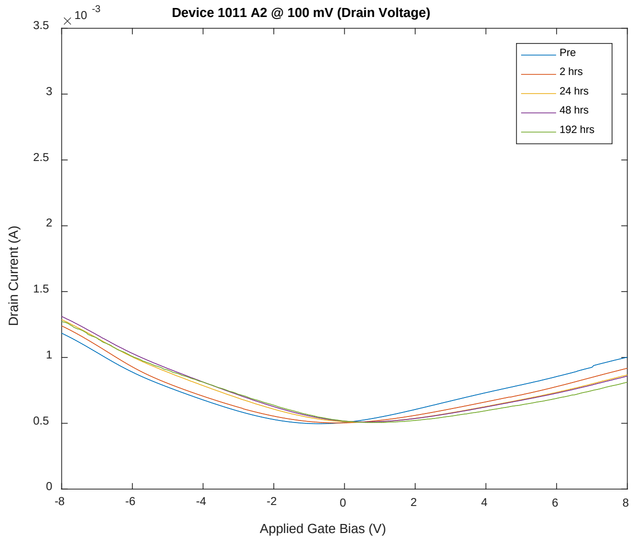


Figure 13. Pre- and post-irradiation drain current for group II.

4.2.3 Group III: Increased drain currents for all gate biases

Group III devices had post-irradiation drain currents greater than pre-irradiation. Fourteen devices, 24%, were in this group. Four devices had drain current increases more than double the pre-irradiation. These are shown in Figure 14 and were discarded from the group averaging. Figure 15 shows a typical measurement taken for devices in this group. The measured current of these ten devices shows an average increase of 18% from pre- to post-irradiation (24 hours) drain currents then a decrease and increase of 5%. This grouping’s Dirac shift started to shift towards the negative voltages in the third day post-irradiation. On the eighth day measurements it showed another average shift to the negative of 0.02 V.

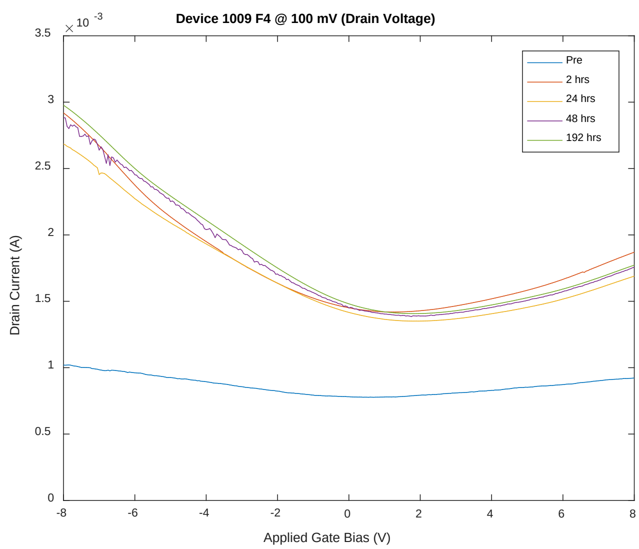


Figure 14. Pre- and post-irradiation drain current for group III.

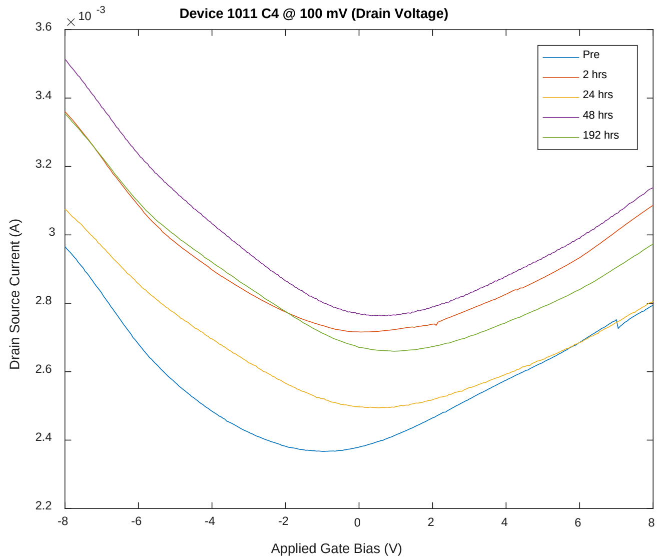


Figure 15. Representative device samples from Group III.

4.2.4 Group IV: Solo device (outlier)

Group IV includes a single device of interest, with an increase in drain current at all gate biases immediately following irradiation. The Dirac point current increased by 33% 2 hours following irradiation then gradually decreased to the pre-irradiation levels in the following measurements. Figure 16 shows the *I-V* curves measured for this solo device.

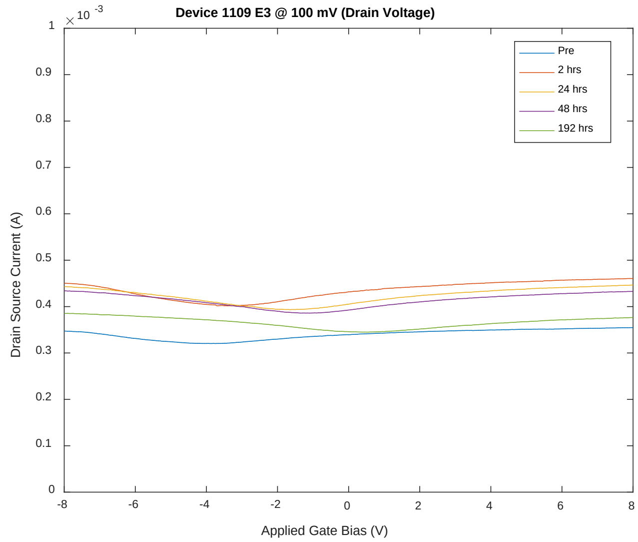


Figure 16. Group IV representative drain current measurement.

4.2.5 Group V: Mid-range change devices

Group V had five devices where the post-irradiation drain current was near the average pre-irradiation values. Figure 17 shows the typical *I-V* measurements taken of this grouping. No analysis of the current was done as the measurements appear to be an anomaly that would not provide additional information that the other 49 devices provide.

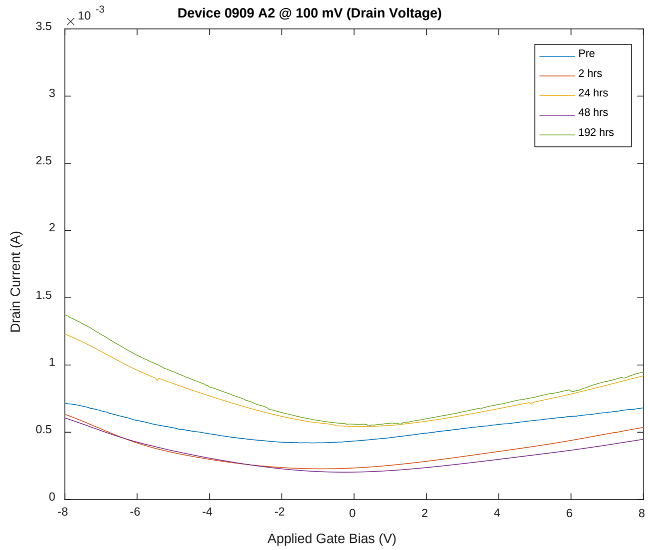


Figure 17. Group V representative device drain current measurements.

4.3 Dirac Point Shift Observations

The hBN devices, regardless of channel length, had Dirac points shift towards the positive applied gate bias following irradiation. In Figure 18 the measured Dirac points show a cluster near zero before irradiation where the average was -0.45 V. At 24 and 48 hours following irradiation the averages were +0.09 V and +0.88 V, respectively, which remained steady for the remaining measurements. Table 4 shows the average Dirac point and standard deviation of all measured devices.

Table 4. Average Dirac point of all devices by day

Time (hrs)	Avg	Std Dev
Pre	-0.45	0.94
2	0.09	1.01
24	0.88	1.05
48	0.90	0.88
192	0.89	0.82

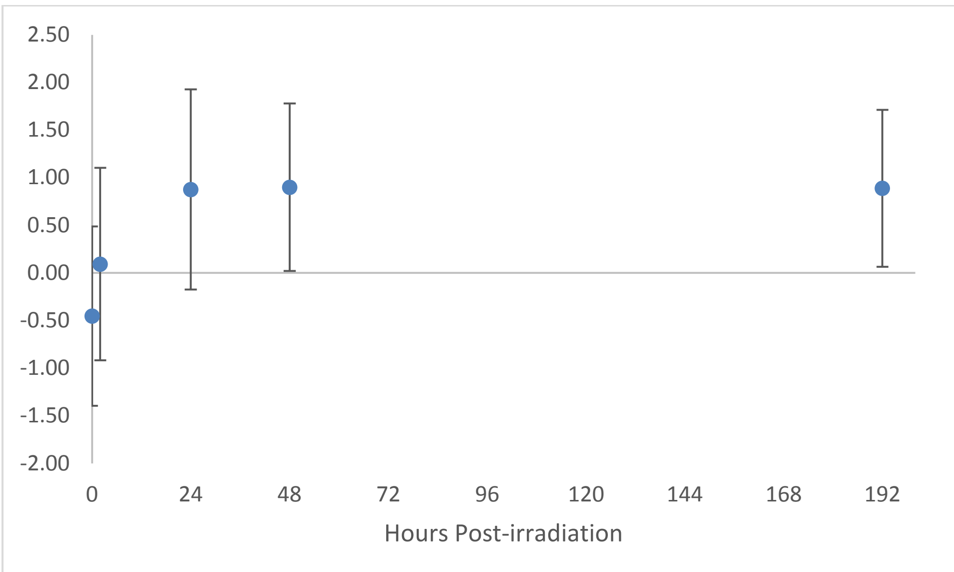


Figure 18. Average Dirac Point of total devices on days measured pre and post-irradiation

This result demonstrates the immediacy of the radiation induced damage and that little room temperature annealing occurred. This indicates the presence of a permanent defect that can be attributed to the total ionizing dose received of 1.7 Mrad (SiO_2).

When comparing only with regards to channel length the Dirac point changes as shown in Table 5, there is a similar trend with the average Dirac point becoming more positive the first two days then either a slowing positive trend or slightly negative on days

3 through 8. All devices showed a shift in the Dirac point towards the positive applied voltage after irradiation, with six showing a slight negative return (over one standard deviation below average) after one week.

Table 5. Average Dirac point change by channel length by day.

L_{ch}(micron)	**0.5**	**Std Dev**	**1.5**	**Std Dev**	**2**	**Std Dev**	**5**	**Std Dev**	**10**	**Std Dev**
Time										
Pre→2hrs	0.55	0.37	0.67	0.32	0.58	0.27	0.44	0.44	0.39	0.47
2→24 hrs	0.62	0.26	0.61	0.43	0.92	0.51	0.84	0.70	0.71	0.43
24-→48 hrs	0.34	0.62	0.09	0.32	-0.10	0.56	-0.10	0.51	-0.01	0.27
48 →192 hrs	-0.25	0.50	-0.08	0.42	0.08	0.46	0.01	0.37	0.08	0.25
	Difference (V)									

By grouping devices characterized by channel length instead of grouped by irradiation responses, the devices are compared in Tables 6 and 7. The overall result shown in these tables and in Figures 19 and 20 is that the drain current measured at the Dirac point post-irradiation does not change significantly. The groupings in Figure 20 confirm this, it shows the current at the Dirac point never going above 10% of pre-irradiation value for Groups I or II. Figure 20 is normalized to the current at the Dirac point by channel length and shows the average over all days for each length never rising above 12% of pre-irradiation current. Table 6 shows that the devices on the far end of the channel length spectrum recorded a lower magnitude of current at the Dirac point. This may indicate a preferential channel length (1-2 micron range) where higher changes post-irradiation occur. Shorter and longer lengths may be the more stable lengths of the devices. Figure 21 shows the average current at the Dirac point by device's channel length. It shows that the changes follow a similar up down pattern for all lengths except the five micron group. It also shows that the current at the Dirac point does not rise more than 12% from the pre-irradiation levels. This rise in current can be attributed to radiation-induced defects increasing carrier concentration [47].

Table 6. Average Dirac Point Current by Length by hour

L_{ch}(micron)	**0.5**	**Std Dev**	**1.5**	**Std Dev**	**2**	**Std Dev**	**5**	**Std Dev**	**10**	**Std Dev**
Time Post										
Pre	.778	.118	1.81	.109	1.20	.253	.430	.074	.226	.029
~2 hrs	.851	.072	1.91	.117	1.33	.257	.437	.128	.233	.028
24 hrs	.834	.076	1.69	.185	1.29	.242	.472	.082	.233	.029
48 hrs	.857	.071	1.93	.082	1.32	.252	.434	.134	.234	.028
8 days	.841	.080	1.85	.099	1.30	.257	.473	.083	.234	.029
	Drain Current (mA)									

Table 7. Average Dirac Point Current Change by Length by Day

L_{ch}(m)	**0.5**	**Std Dev**	**1.5**	**Std Dev**	**2**	**Std Dev**	**5**	**Std Dev**	**10**	**Std Dev**
Time										
Pre→2 hrs	72.6	93.9	103	71.4	133	129	7.98	98.6	7.35	7.36
2 → 24 hrs	16.3	23.2	-226	136	-45.4	45.2	34.7	117	.006	0.894
24 → 48 hrs	22.2	20.6	242	136	33.8	29.1	-37.7	125	.746	1.13
48 → 192 hrs	-16.0	15.3	-77.0	48.2	-20.2	29.9	38.4	134	-.488	0.983
	Difference (μA)									

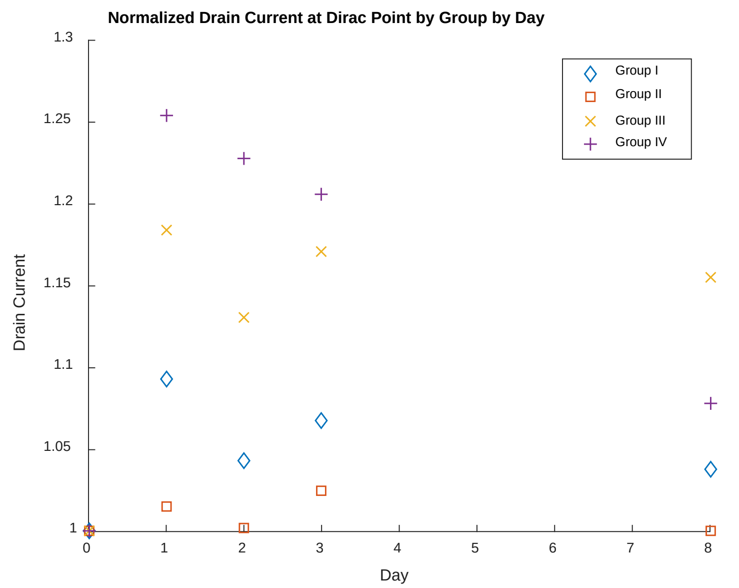


Figure 19. Drain current by groups normalized to pre-irradiation value.

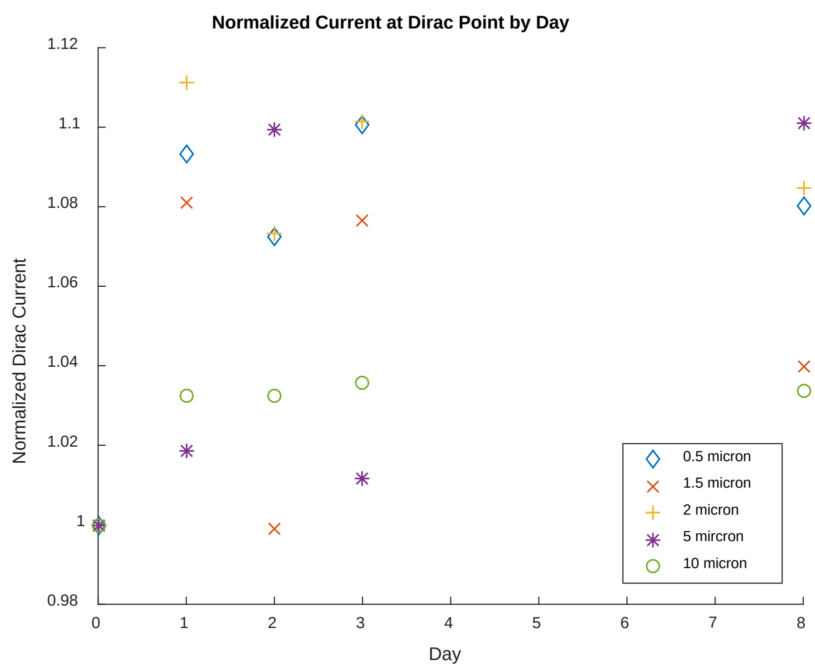


Figure 20. Drain current by channel length normalized to pre-irradiation value

4.4 Observations related to Mobility

The study by Lu S. et al. with graphene quantum dots found that oxidation and reduction increases with radiation dose [48]. A possible similar mechanism after irradiation could be the cause of the immediate increase in mobility after irradiation where the graphene during irradiation had damage to its carbon bonds then subsequently gained more carbon-hydrogen bonds in the increasing irradiation.

In SiO_2/graphene devices, there is a degradation of carrier mobility due to increased scattering mechanisms resulting from a buildup of oxide-trapped charges near the channel interface [49]. In the devices tested in this research, there was an observed increase in mobility immediately following irradiation with a gradual decrease over the eight days of room temperature annealing. Figure 22 shows the normalized mobility by channel length. There is an immediate increase after irradiation then a decrease to near pre-irradiation levels at all channel lengths except 1.25 microns. There was only one 1.25 micron device. It would be expected that with more 1.25 micron channel length devices a very comparable curve to the other channel lengths changes would occur.

To extract mobility from the *I-V* curves, the transfer length method was used by comparing gate lengths and total resistances to get contact and sheet resistance. This method is described in the work by Zhong et al. [50] using the calculated resistance versus channel length. The pre-irradiation chart used to extract contact resistance and sheet resistance is shown in Figure 21.

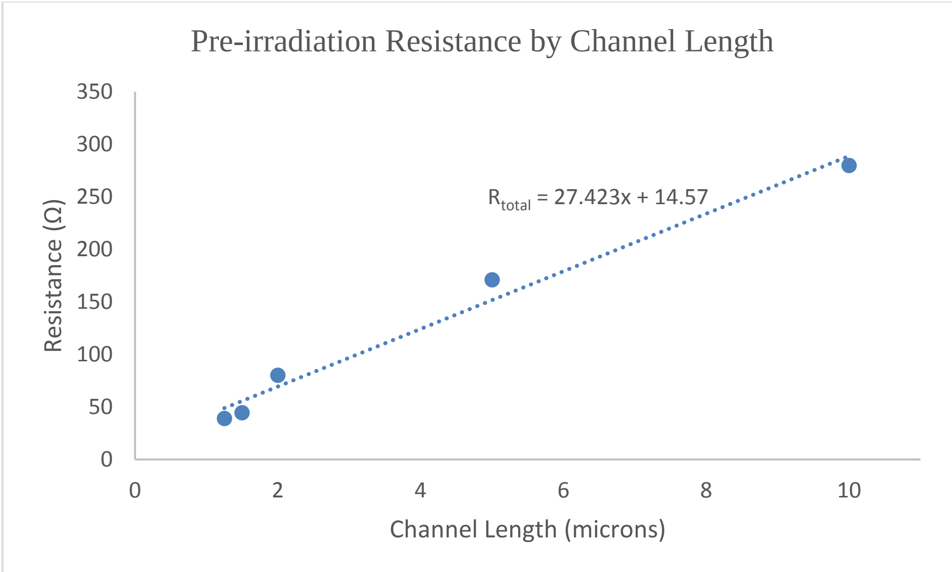


Figure 21. Pre-irradiation resistance by channel length used to extract mobility.

The fitted linear line in the chart is representative of equation (6) with the slope equal to the sheet resistance, R_{sheet} divided by channel width and the y-intercept is equal to two times the contact resistivity, R_c, divided by channel width. The values used to determine the resistance were the current at 3 to 5 volts less than the device's Dirac point, as shown in equation (6).

$$R_{total} = \frac{L_{ch} R_{sheet}}{W_{ch}} + \frac{2R_c}{W_{ch}} \quad (6)$$

Using the extracted sheet resistance, mobility was calculated using equations (7) and (8) where n_0 was assumed to be of 10^{12} cm^{-2} and $|V_g\text{-}V_{Dirac}|$ is 4 which was the midpoint of the region used to extract resistance, 3 to 5 volts less than the device's Dirac point.

$$n(V_g - V_{Dirac}) = \sqrt{n_0^2 + (C_g|V_g - V_{Dirac}|)^2} \tag{7}$$

$$\mu = \frac{1}{qnR_{sheet}} \tag{8}$$

Table 8 shows the calculated mobility normalized to each channel length's pre-irradiation value. The devices used in this research had extremely thin channel and substrate layers compared to the SiO_2/graphene devices. This difference in material thickness would lead to less chance of traps being formed in the channel layers which corresponds to the increased mobility. Figure 22 graphically shows the normalized mobility in Table 8.

Using this method illustrates the effect of contact resistance becoming more pronounced for smaller channel lengths. The pre-irradiation contact resistance calculated from the trend line is 14.57 Ω. As the channel length gets smaller, the resistance of the channel decreases to the point that contact resistance becomes a dominant effect and skews the mobility calculation of the devices.

Table 8. Normalized mobility by time and by channel length

	Time Post-Irradiation				
L_{ch} (microns)	Pre	~2 hrs	24 hrs	48 hrs	8 days
0.5	1	1.05	1.02	1.06	1.05
1.5	1	1.11	0.95	1.13	1.07
2	1	1.24	1.17	1.24	1.19
5	1	0.97	1.10	0.97	1.15
10	1	1.01	1.00	1.05	1.05

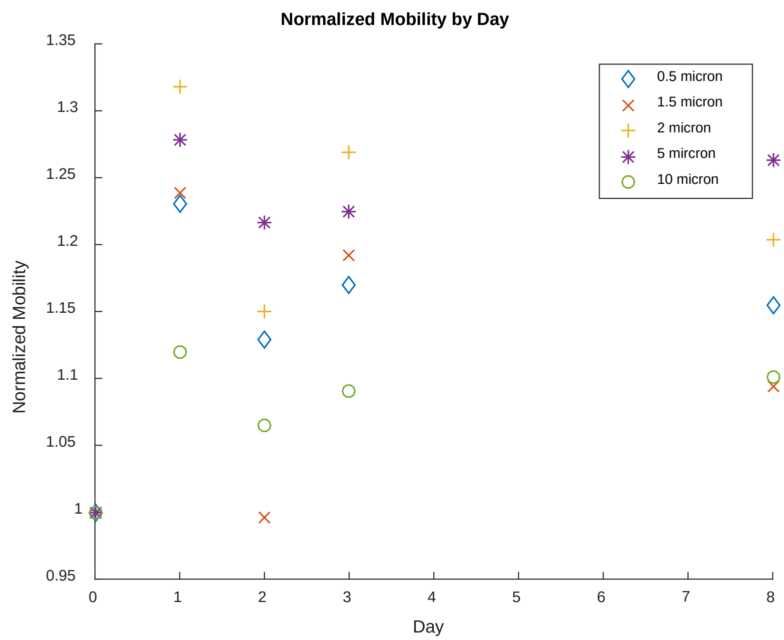


Figure 22. Normalized mobility by day.

4.5 Oxide/Substrate Trap Density

Charge traps can be formed in the devices at either the graphene interfaces or in the bulk material, in this case sapphire. The nanometer scale of the graphene/hBN layers would suggest the trapping more likely to occur in the sapphire region. The increase seen over time of calculated trap density might be attributed to charged hydrogen converted into traps [51]. Over long periods of time, protons could be released and seek favorable reactions with other materials such as the oxygen in sapphire which then would form an oxide traps. Another possible mechanism for the increase in traps over time is trapped electrons between the hBN layer and the underlying sapphire substrate.

Assuming the trapped charge is located near the graphene interface, table 9 shows the change in trapped charges by channel length and the overall average by day in the last row. Figure 23 shows the changes normalized to the first day by each channel length. The trapped charges increase in the second day for all the devices then the changes remain near even in days three and eight. This second day is also where the average Dirac point plateaus, and it can be seen in Table 9 that the trapped charge density did not change significantly from Day 3 to Day 8. The shift can also be attributed to gamma irradiation causing p-doped behavior in graphene which has been found in previous works [17].

Table 9. ΔN_{tc} by channel length and by day

Hours After Irradiation								
L_{ch}(µm)	2	+/-	24	+/-	48	+/-	192	+/-
	($x10^{12}$)	($x10^{11}$)	($x10^{12}$)	($x10^{11}$)	($x10^{12}$)	($x10^{11}$)	($x10^{12}$)	($x10^{11}$)
0.5	1.38	2.92	2.94	1.89	3.79	4.57	3.17	2.35
1.5	1.68	3.27	3.21	5.25	3.44	4.81	3.23	2.55
2	1.46	1.35	3.77	2.94	3.50	2.23	3.70	3.81
5	1.42	2.05	3.22	6.55	2.96	3.40	2.98	3.78
10	1.37	2.24	2.77	4.86	2.75	3.32	2.95	3.79
[redacted]								
Overall	1.47	9.41	3.34	1.76	3.40	1.53	3.37	1.84
cm^{-2}								

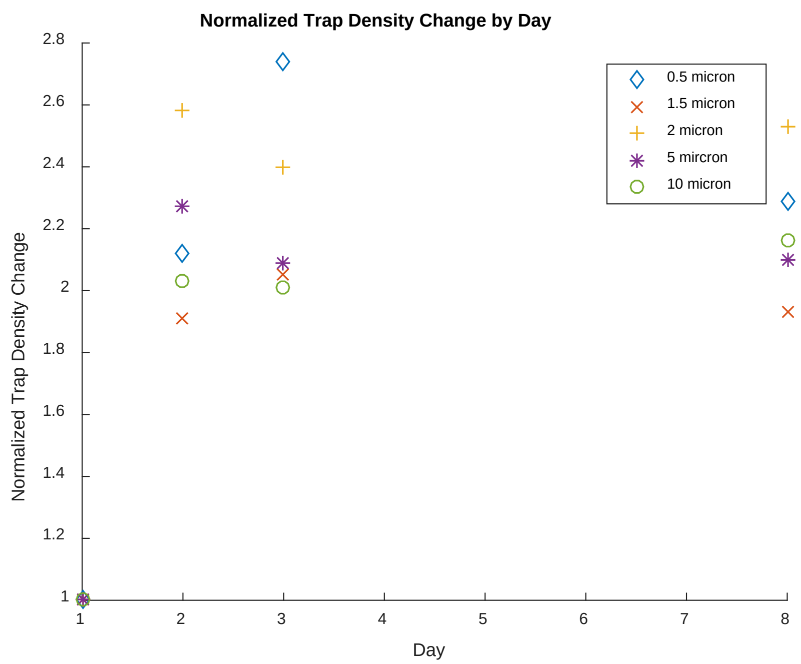


Figure 23. Trap density change normalized to first post-irradiation value

V. Conclusions and Recommendations

5.1 Research Findings

The hBN GFETs exhibited a mostly inconsistent but measurable variation in post-irradiation response to drain current for the applied gate voltage. after 1.7 Mrad (SiO_2) of ^{60}Co gamma irradiation. All 55 of the hBN devices had a positive Dirac point shift indicating hole dominated conduction over an increasing bias range after irradiation. The average shift in the Dirac point was 0.78 V, with one device having a shift of over 4 V, from initial measurements to the first 48 hours. Little recovery was observed past 72 hours, indicating a permanent post-irradiation condition at room temperature. This means that if hBN is used as a passivation for graphene based transistors using the present technology, gate voltage shifts of this magnitude must be tolerable.

A possible cause of the Dirac shift is the ionization of the hydrogen atoms attached to impurity sites in the hBN. This is the finding of the work of Zhang et al. Their team describes the effect of high radiation doses causing hydrogen atoms attached to carbon in boron sites to be separated from their bonds then finding a bond with a carbon in graphene. The bonds between hydrogen and the carbon in nitrogen sites are harder to break. The hydrogen from these carbon atoms likely re-bond when these bonds are broken unless the hydrogen attaches to graphene, which has a lower energy threshold for bonding than with the carbon in nitrogen sites [2]. This is plausible given the growth techniques. passivation thickness, and exposure to air for these devices. No hermetic packaging or amendments were made to reduce hydrogen and nitrogen exposure (e.g. sealing within argon.) An increase in hole concentration in graphene occurs from these processes and is related to a positive shift in the Dirac point along with radiation induced electron trapping in the hBN layer.

When grouped either by channel length or drain current the only consistency is in the shift in the Dirac point. The drain current at the Dirac point from the groups I and II, (page 38-40), which contains the majority (38 of 55) of the irradiated devices, stays within 10% of the pre-irradiation level. The overall trend of increased drain current after irradiation and return to pre-irradiation values is observed in these devices as well. From pre-irradiation to the first post-irradiation measurement, three of the 38 devices showed a decrease in drain current at the Dirac point. From the first post-irradiation measurements to 192 hours later, 29 of the 38 showed a decrease in drain current. These variations were small and demonstrated the overall consistency of drain current indicating little change to resistance after irradiation.

5.2 Future Work

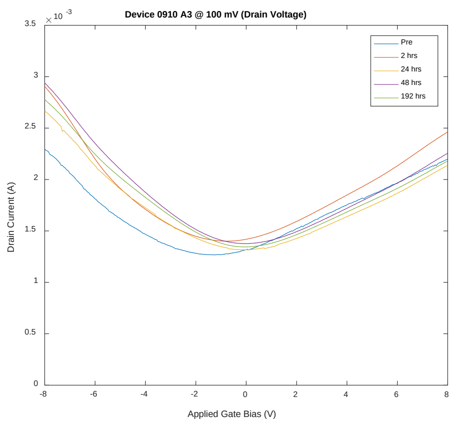
In order to make consistent determinations as to the radiation hardness and performance of hBN GFETs in radiation applications, this technology must be matured, especially regarding surface interfaces with hydrogen and nitrogen. Packaging of the devices, along with manufactured contacts and gas barriers would allow for analysis of the device potential to the furthest extent. The work of Prochazka et. al. is an examples of such isolation techniques [42]. This type of experimental is warranted given the results of the current study.

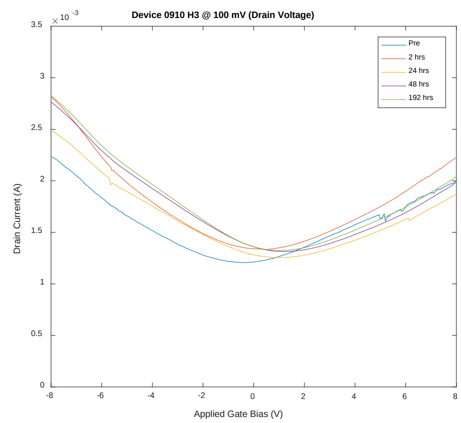
Additionally, exposure to other types of radiation at different energies is necessary. Graphene/hBN devices are being proposed as a substitute for SiO_2 substrate devices in a variety of applications. It would be beneficial to compare the hBN devices to those of SiO_2 substrate devices in identical environments. This would allow for the elimination of factors that only occurred during one of the evaluations.

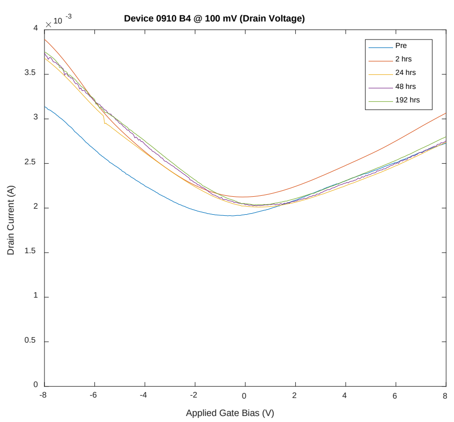
The devices were only evaluated before and after irradiation. Evaluation in-situ would be beneficial to assess radiation damage relationships to a better fidelity.

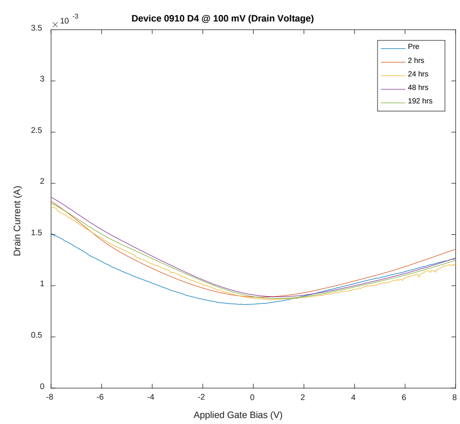
Appendix A: I-V Curves in Groupings

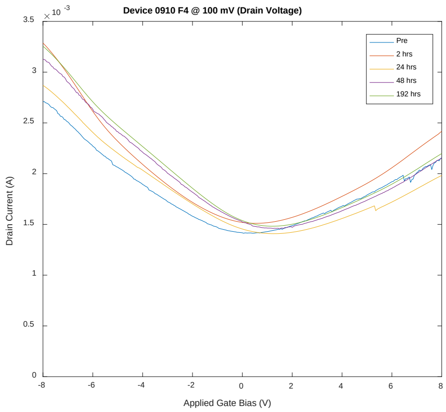
Group I (Increase in post-irradiation current at negative voltages, Current is mixed at positive voltages, 22 devices)

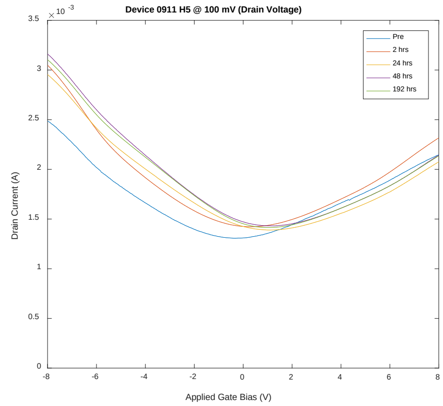


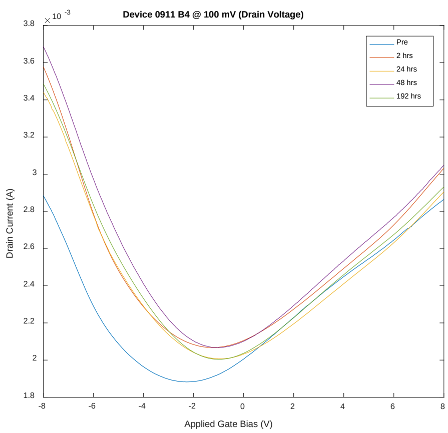


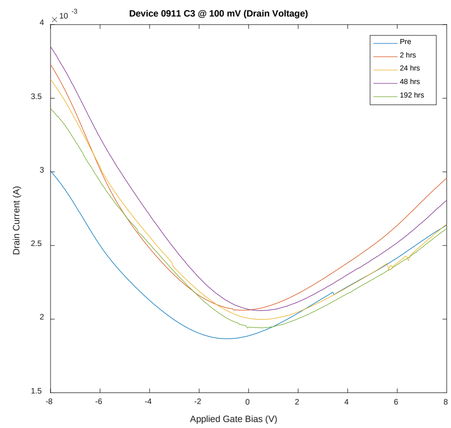


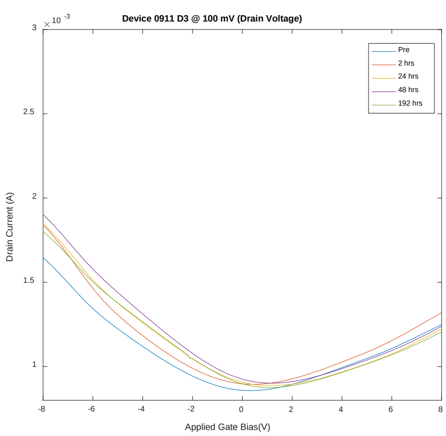


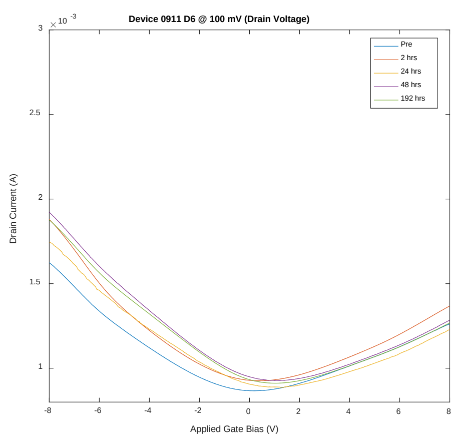

Device 0910 F4 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

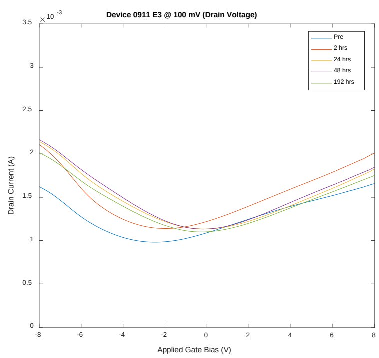

Device 0911 H5 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

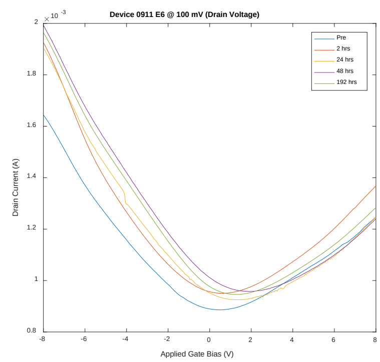

Device 0911 B4 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

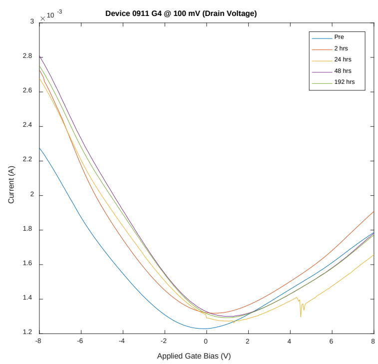

Device 0911 C3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

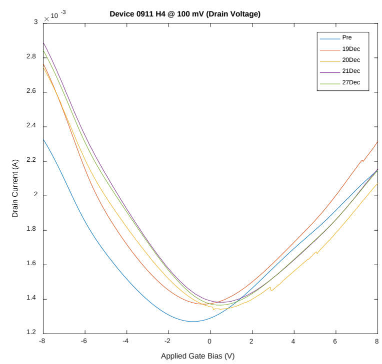

Device 0911 D3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias(V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

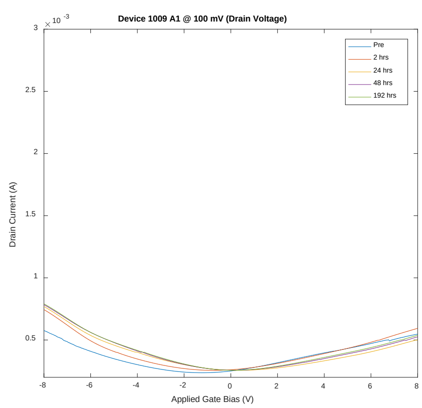

Device 0911 D6 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

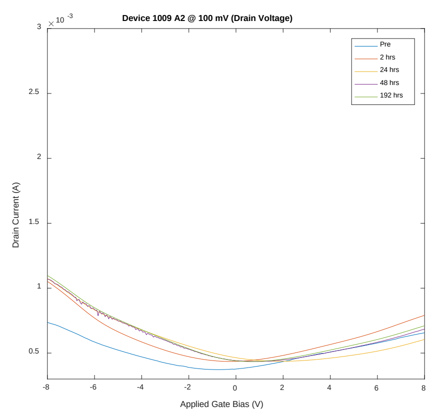

Device 0911 E3 @ 100 mV (Drain Voltage)
×10^-3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

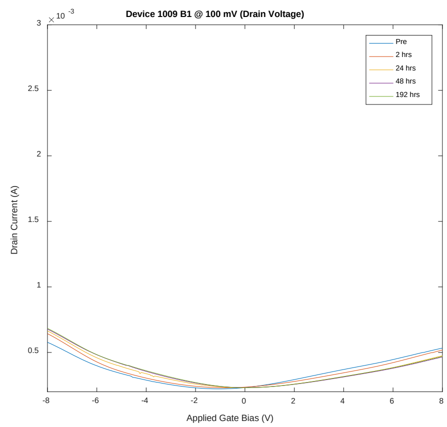

Device 0911 E6 @ 100 mV (Drain Voltage)
×10^-3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

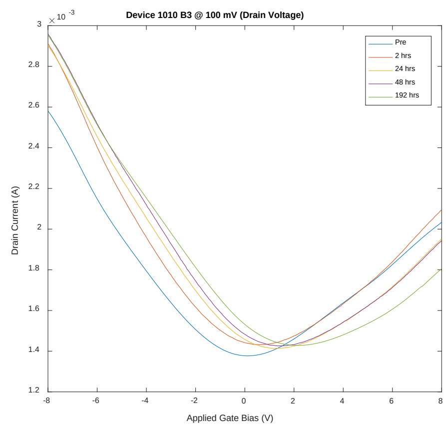

Device 0911 G4 @ 100 mV (Drain Voltage)
×10^-3
Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

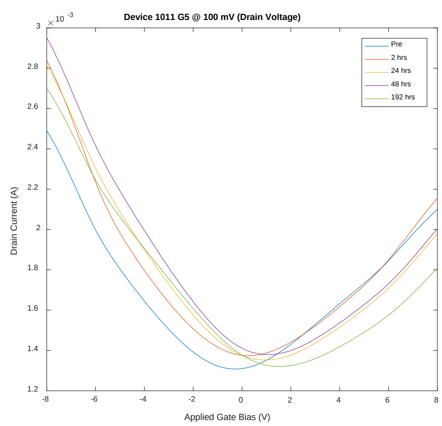

Device 0911 H4 @ 100 mV (Drain Voltage)
×10^-3
Drain Current (A)
Applied Gate Bias (V)
Pre
19Dec
20Dec
21Dec
27Dec

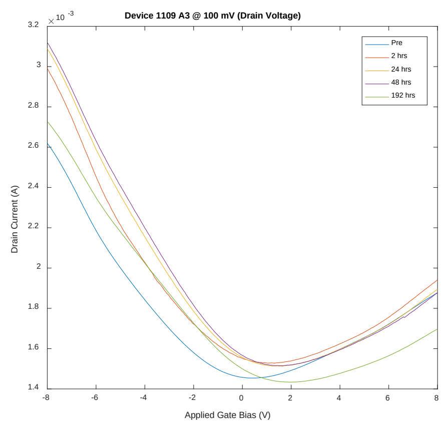

Device 1009 A1 @ 100 mV (Drain Voltage)
×10^-3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

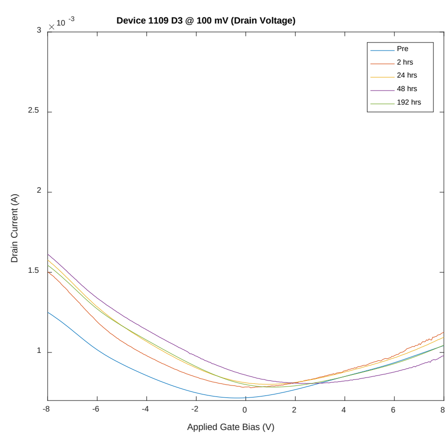

Device 1009 A2 @ 100 mV (Drain Voltage)
×10^-3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs


Device 1009 B1 @ 100 mV (Drain Voltage)
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

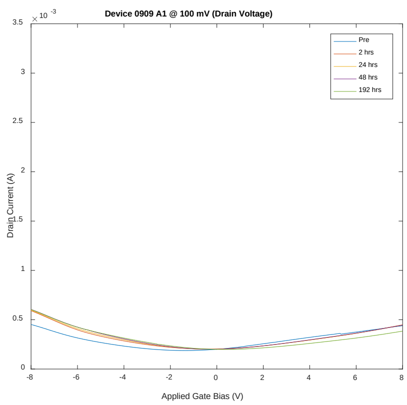

Device 1010 B3 @ 100 mV (Drain Voltage)
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

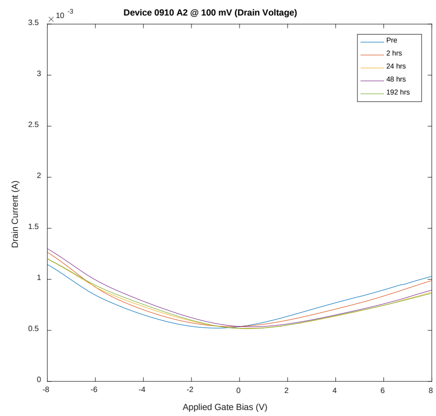

Device 1011 G5 @ 100 mV (Drain Voltage)
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

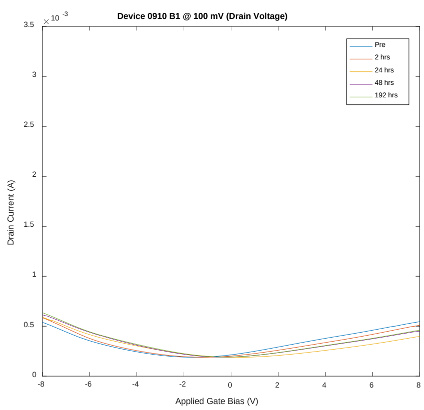

Device 1109 A3 @ 100 mV (Drain Voltage)
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

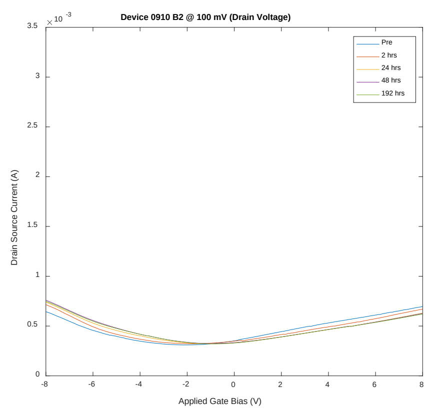

Device 1109 D3 @ 100 mV (Drain Voltage)
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

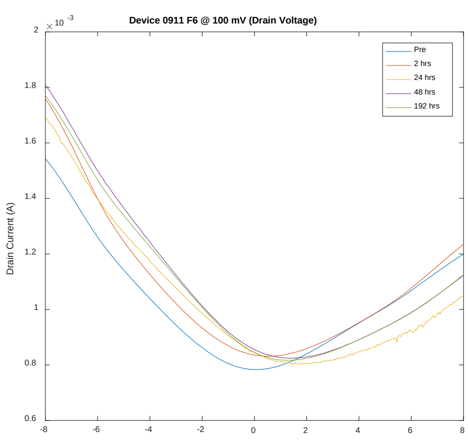
Group II (Increase in post-irradiation current at negative voltages, decrease post-irradiation current at positive voltages, 16 devices)

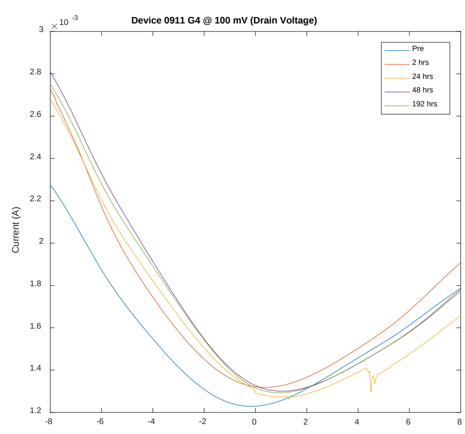


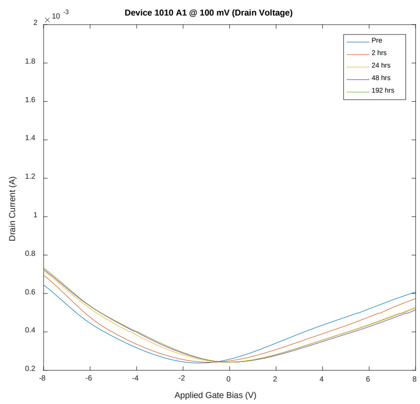


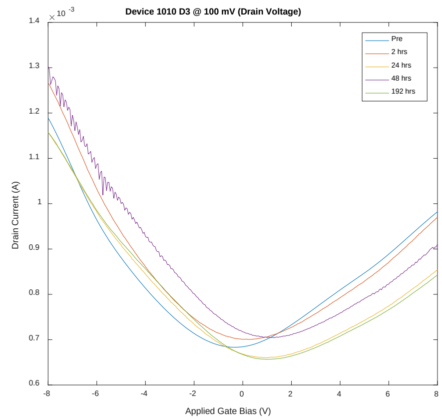


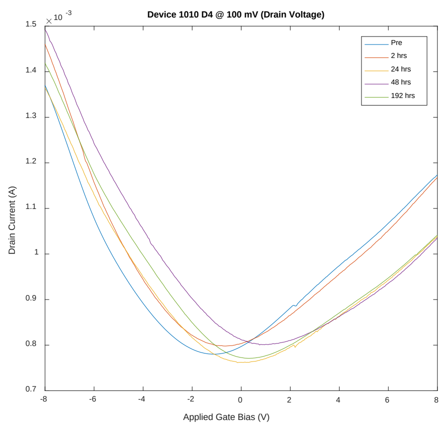


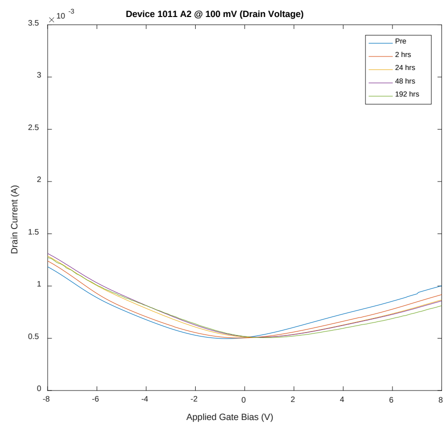


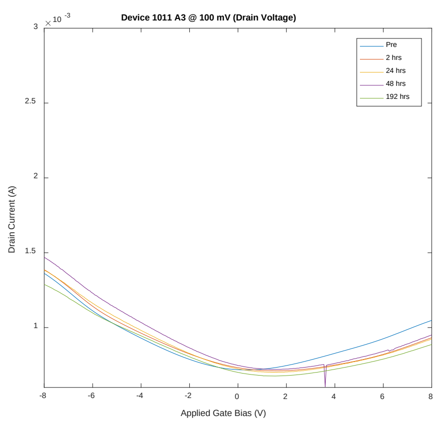


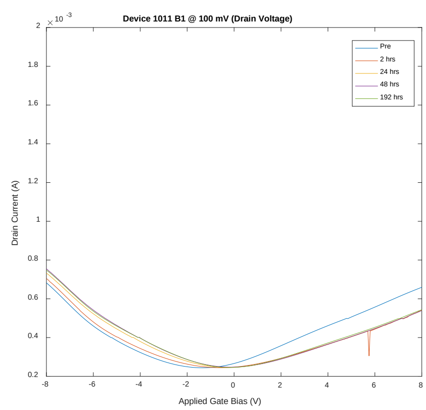

Device 1010 A1 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

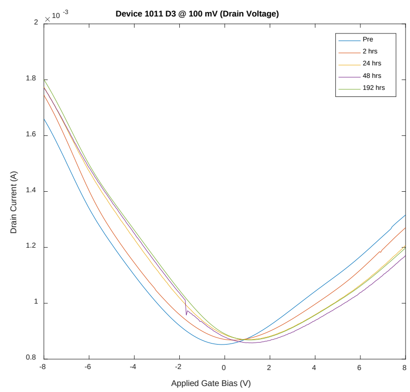

Device 1010 D3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

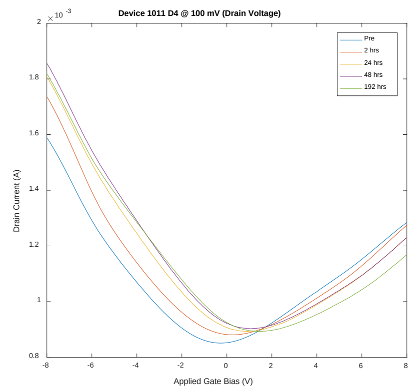

Device 1010 D4 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

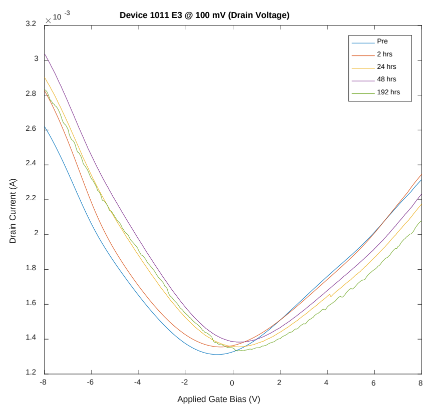

Device 1011 A2 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

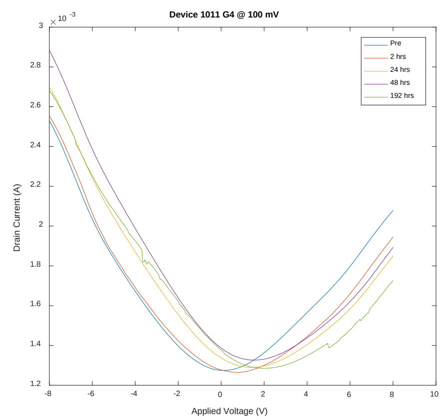

Device 1011 A3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs


Device 1011 B1 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

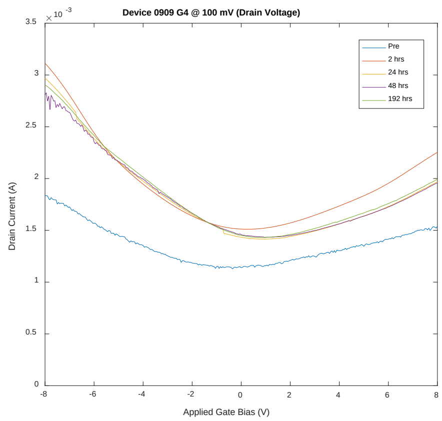

Device 1011 D3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

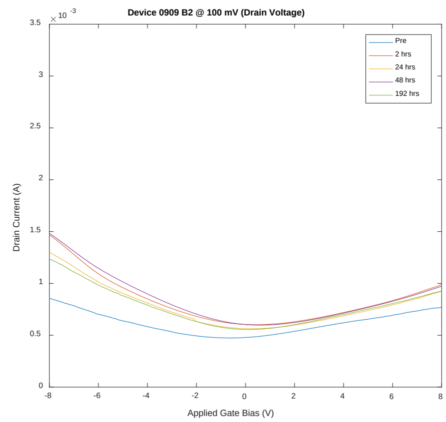

Device 1011 D4 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

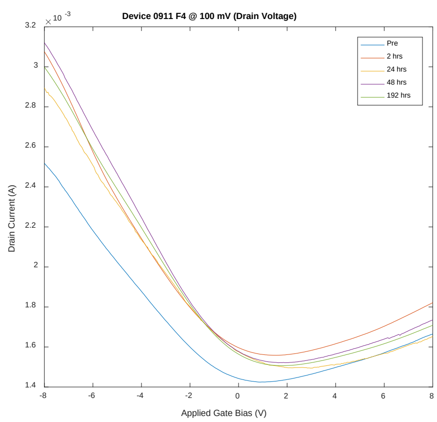

Device 1011 E3 @ 100 mV (Drain Voltage)
×10 -3
Drain Current (A)
Applied Gate Bias (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

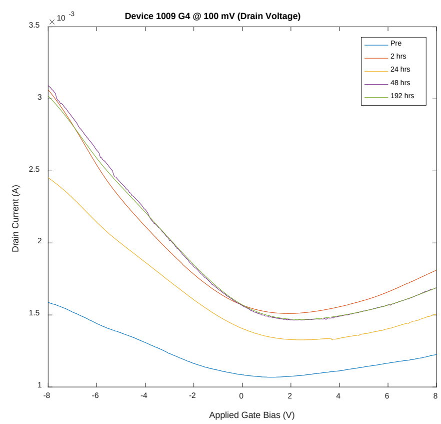

Device 1011 G4 @ 100 mV
×10 -3
Drain Current (A)
Applied Voltage (V)
Pre
2 hrs
24 hrs
48 hrs
192 hrs

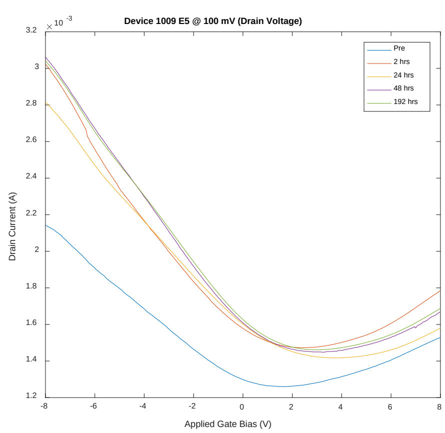
Group III (Significant increase in post-irradiation current at all voltages, no decrease over time, 14 devices)

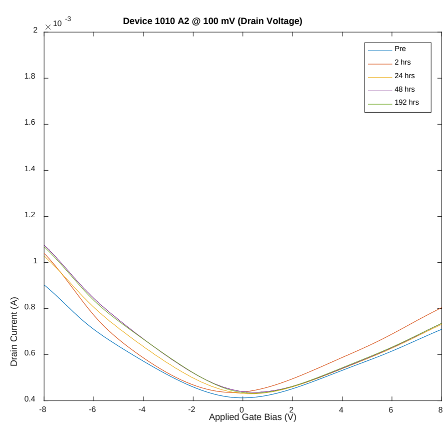


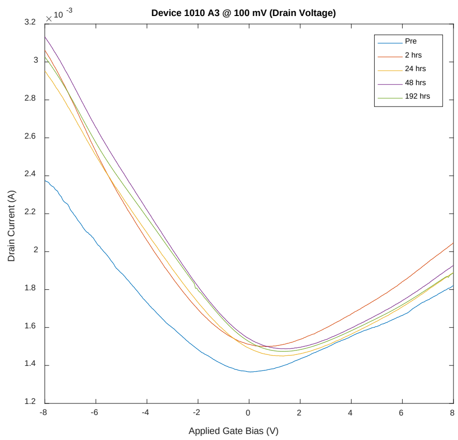


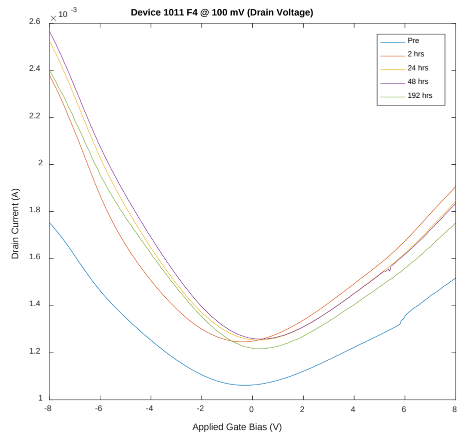


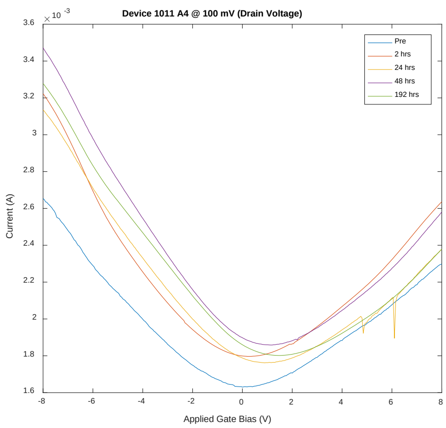


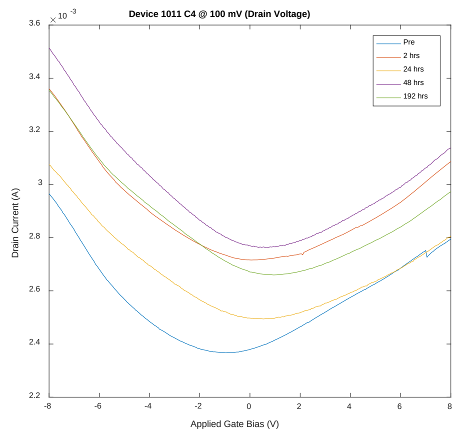




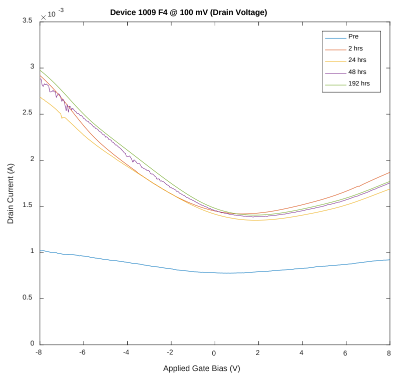

Device 1010 A3 @ 100 mV (Drain Voltage)
×10⁻³
Pre
2 hrs
24 hrs
48 hrs
192 hrs
Drain Current (A)
Applied Gate Bias (V)

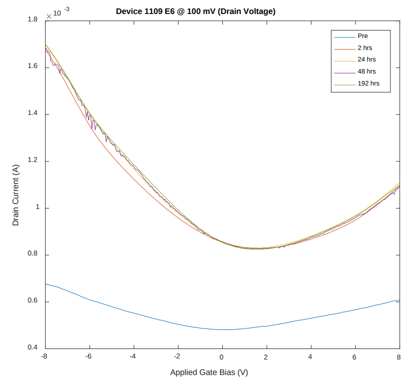

Device 1011 F4 @ 100 mV (Drain Voltage)
×10⁻³
Pre
2 hrs
24 hrs
48 hrs
192 hrs
Drain Current (A)
Applied Gate Bias (V)

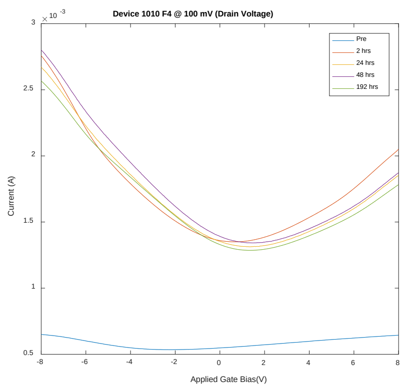

Device 1011 A4 @ 100 mV (Drain Voltage)
×10⁻³
Pre
2 hrs
24 hrs
48 hrs
192 hrs
Current (A)
Applied Gate Bias (V)

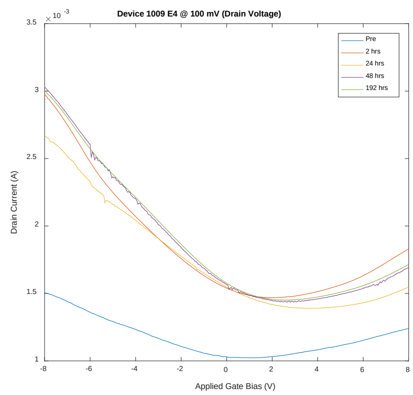

Device 1011 C4 @ 100 mV (Drain Voltage)
×10⁻³
Pre
2 hrs
24 hrs
48 hrs
192 hrs
Drain Current (A)
Applied Gate Bias (V)

Subgroup III-W (drastically different pre and post-irradiation curves)

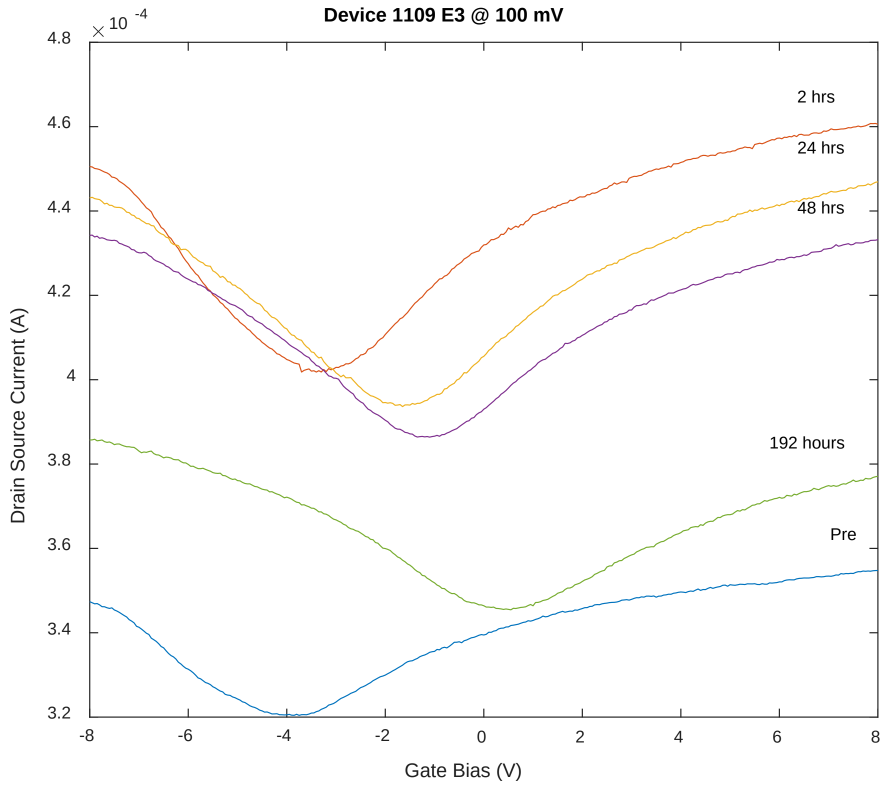




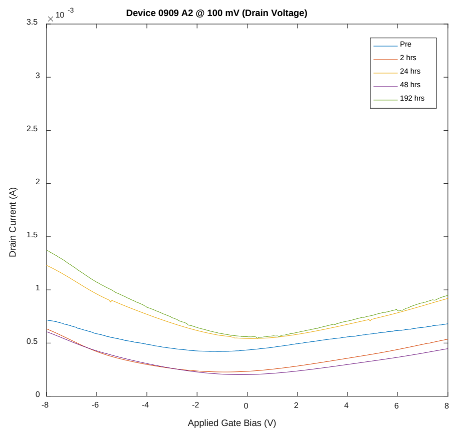


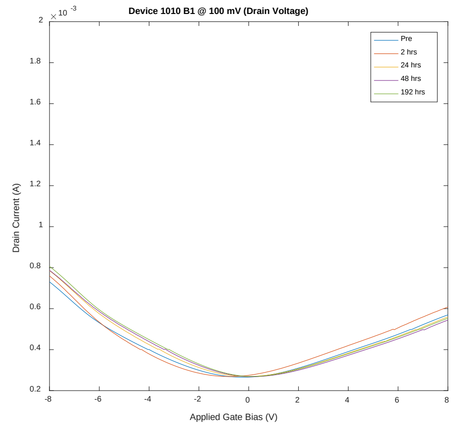


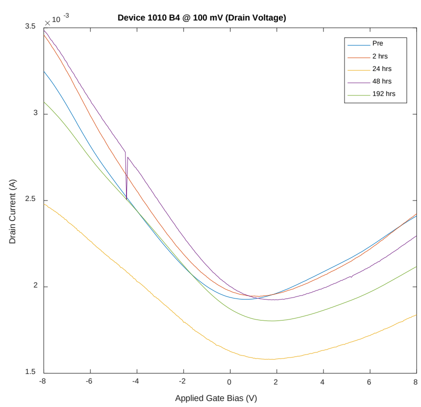
Group IV (Significant current increase post-irradiation at all voltages, gradual decrease to pre-irradiation current levels, 1 device)

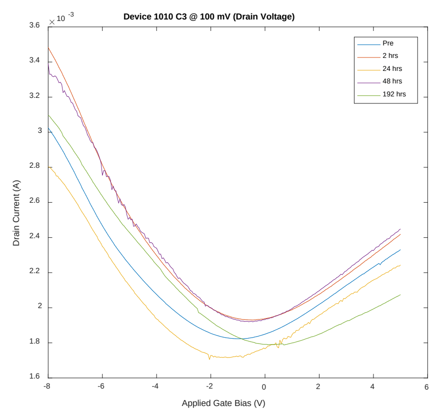


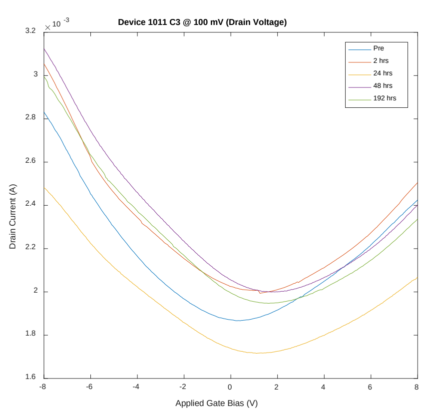
Group V (Pre-irradiation current somewhere in the middle of post-irradiation levels, 5 devices)



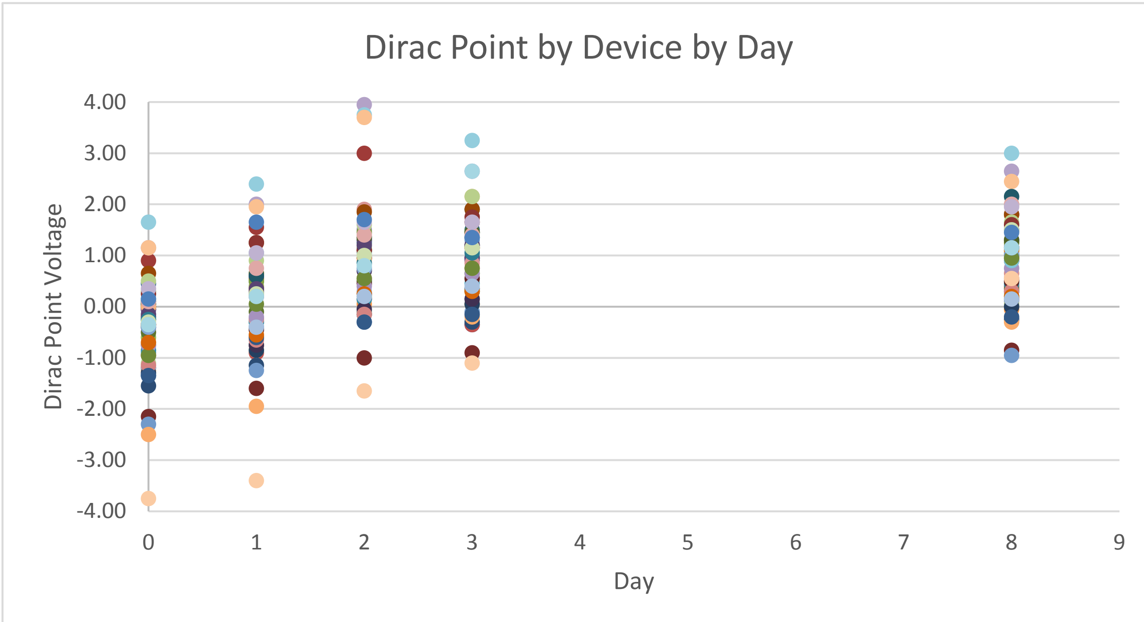




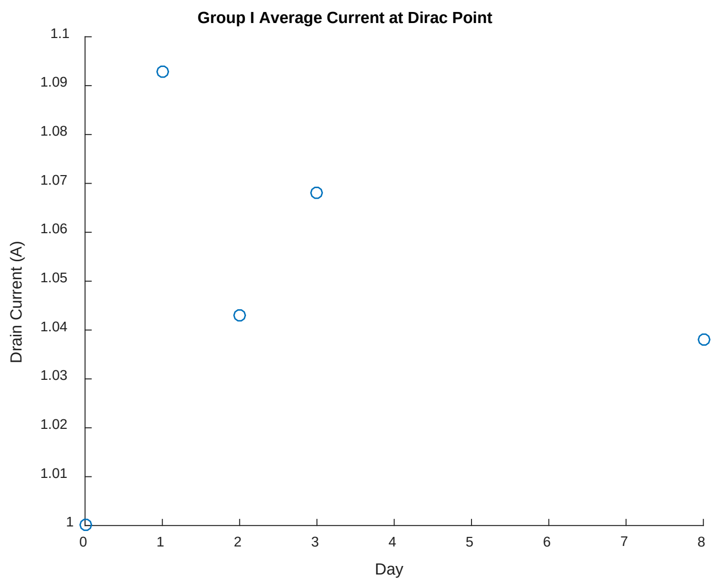


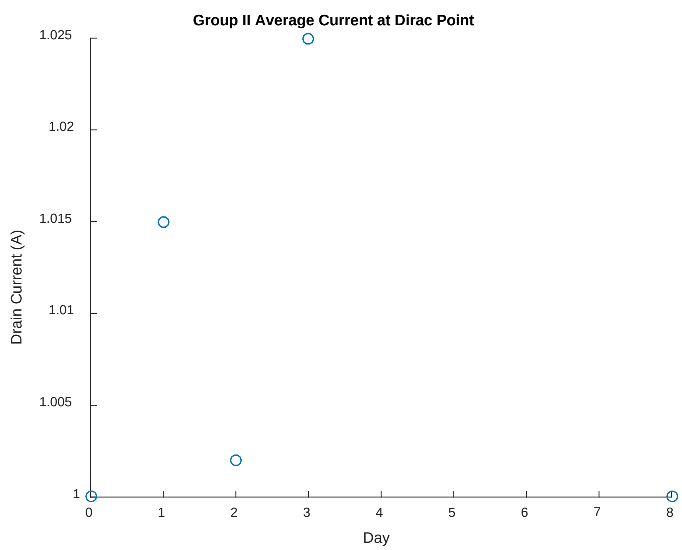


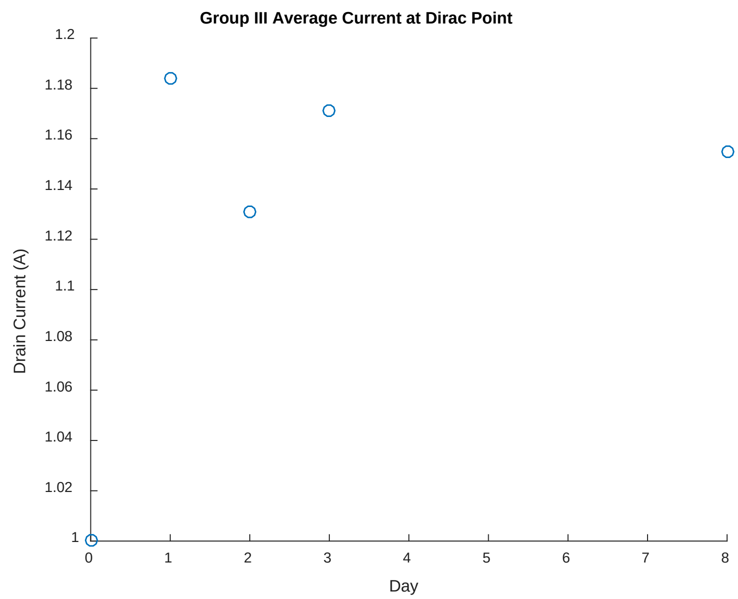
Appendix B: Dirac Point Voltage of All Devices by Day

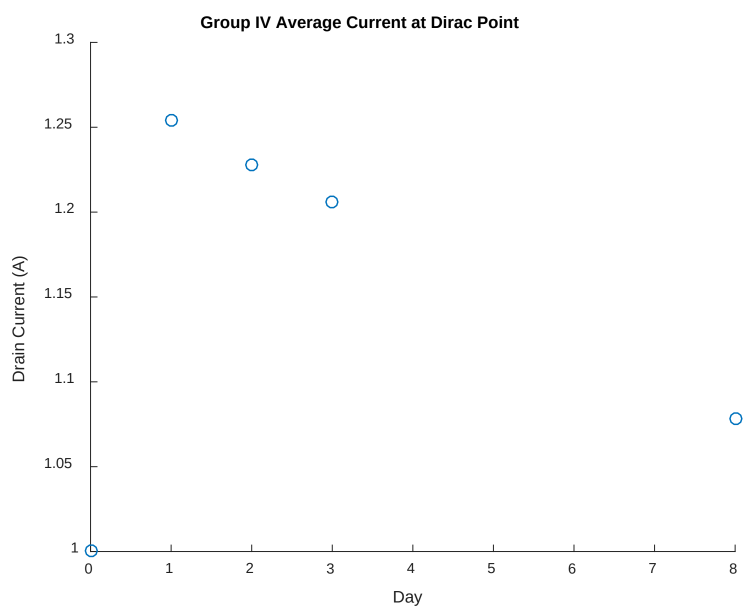


Appendix C: Average Dirac Point Currents by Group by Day

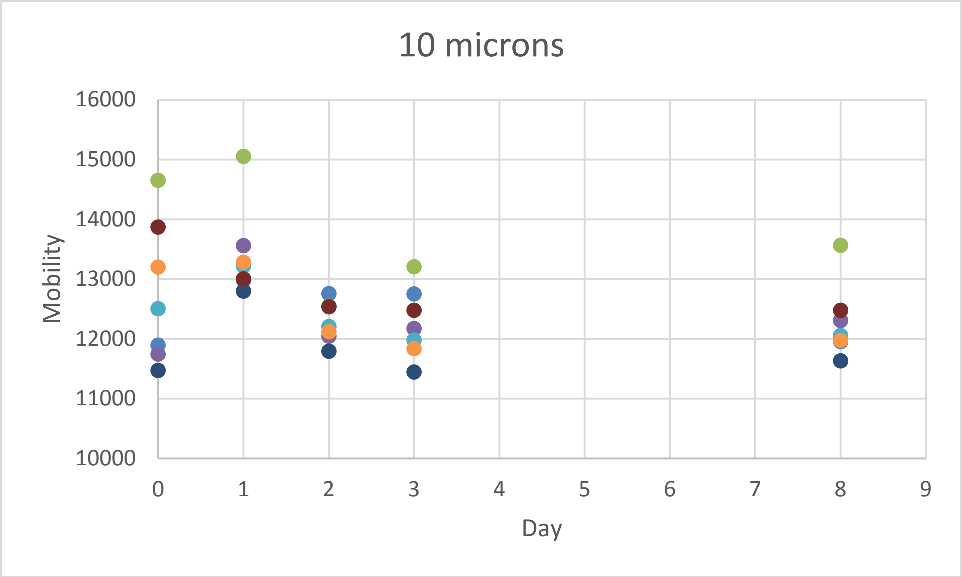


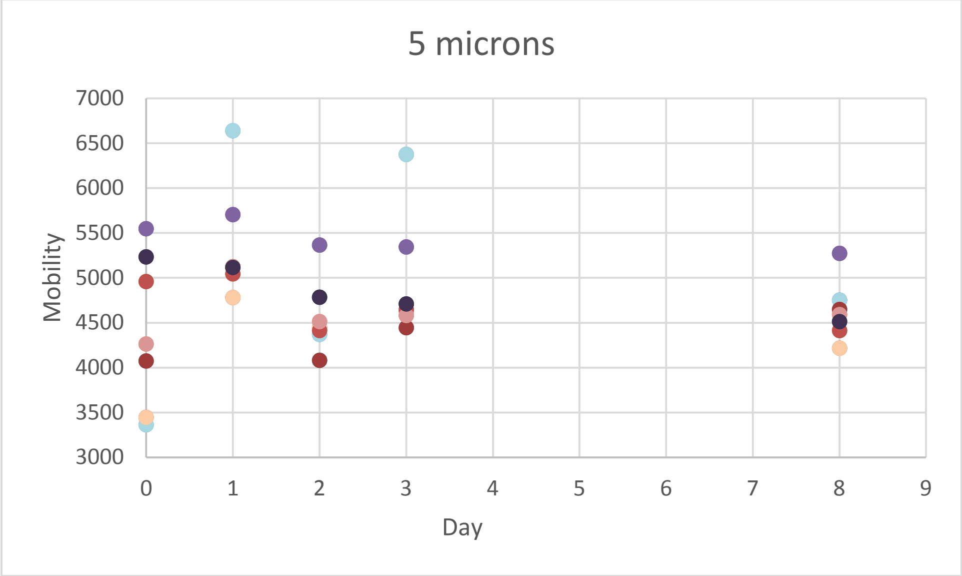


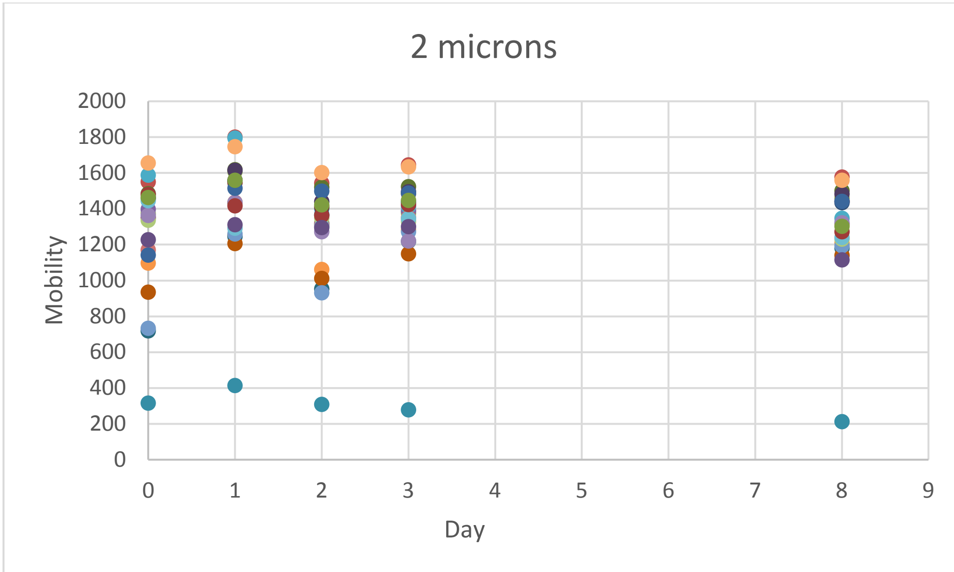

Group III Average Current at Dirac Point
Drain Current (A)
1.2
1.18
1.16
1.14
1.12
1.1
1.08
1.06
1.04
1.02
1
0
1
2
3
4
5
6
7
8
Day

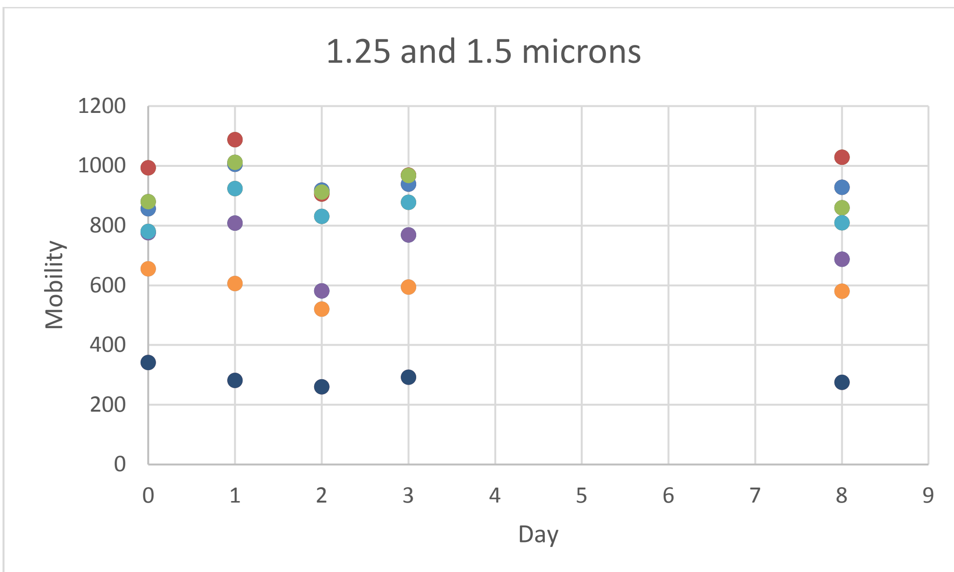

Group IV Average Current at Dirac Point
Drain Current (A)
1.3
1.25
1.2
1.15
1.1
1.05
1
0
1
2
3
4
5
6
7
8
Day

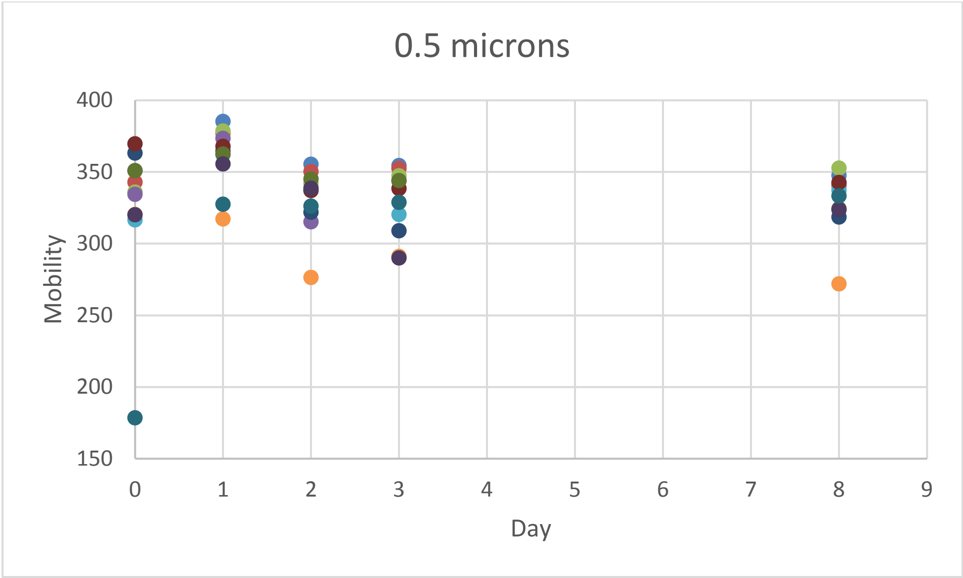
Appendix D: Mobility by Day by Channel Length






2 microns
Mobility
Day
2000
1800
1600
1400
1200
1000
800
600
400
200
0
0
1
2
3
4
5
6
7
8
9


1.25 and 1.5 microns
Mobility
Day
1200
1000
800
600
400
200
0
0
1
2
3
4
5
6
7
8
9


0.5 microns
Mobility
400
350
300
250
200
150
0
1
2
3
4
5
6
7
8
9
Day

Appendix E: Dirac Point Voltage by Channel Length

10 Micron Devices Dirac Point Voltage by Day							
Day	0909 A1	0910 B1	1009 A1	1009 B1	1010 A1	1010 B1	1011 B1
0	-1.35	-1.55	-1.20	-1.10	-1.30	-0.20	-1.35
1	-0.40	-1.15	-0.75	-0.85	-0.85	-0.75	-0.60
2	-0.30	0.25	0.30	-0.10	-0.15	-0.05	-0.30
3	-0.35	-0.30	0.15	0.05	0.05	0.15	-0.15
8	0.30	-0.25	0.10	0.05	0.00	0.15	-0.20

5 Micron Devices Dirac Point Voltage by Day							
Day	0909 A2	0909 B2	0910 A2	0910 B2	1009 A2	1010 A2	1011 A2
0	-1.20	-0.60	-0.90	-2.15	-0.75	0.00	-0.75
1	-0.90	0.40	-0.30	-1.60	-0.25	-0.45	-0.20
2	0.15	0.20	0.50	-1.00	1.90	0.45	0.40
3	-0.35	0.65	0.45	-0.90	0.85	0.55	0.65
8	0.40	0.20	0.30	-0.85	0.65	0.50	0.75

1.25 Micron Devices Dirac Point Voltage by Day
1011 C4
-0.95
0.05
0.55
0.75
0.95

2 Micron Devices Dirac Point Voltage by Day

Day	0910 G4	0910 A3	0910 F4	0910 H3	0911 E3	0911 F4	0911 F6	0911 G4	0911 H4	0911 H5
0	-0.35	-1.25	0.05	-0.35	-2.50	0.90	0.00	-0.05	-0.85	-0.35
1	0.20	-0.75	0.50	0.55	-1.95	1.55	0.50	0.30	-0.30	0.35
2	0.95	0.05	1.25	0.95	-0.15	3.00	1.45	1.30	0.15	1.10
3	0.95	0.05	1.50	1.20	-0.20	1.65	1.45	0.90	0.35	1.15
8	0.95	-0.05	1.15	0.95	-0.30	1.80	1.25	1.00	0.45	1.10

Day	1009 E4	1009 E5	1009 G4	1010 A3	1010 B3	1010 G4
0	1.15	1.65	1.15	0.05	0.10	0.50
1	2.00	2.40	1.95	0.65	0.60	0.90
2	3.95	3.75	3.70	1.35	1.10	1.60
3	2.65	3.25	2.15	1.45	1.35	2.15
8	2.65	3.00	2.45	1.30	2.15	1.65

Day	1011 A3	1011 E3	1011 F4	1011 G4	1011 G5	1109 A3	1109 E3
0	-0.25	-0.70	-0.35	0.10	-0.30	0.35	-3.75
1	1.05	-0.55	-0.40	0.75	0.25	1.05	-3.40
2	1.05	0.25	0.20	1.40	1.00	1.65	-1.65
3	1.20	0.30	0.40	1.40	1.15	1.65	-1.10
8	0.90	0.20	0.15	2.00	1.50	1.95	0.55

1.5 Micron Devices Dirac Point Voltage by Day

Day	0910 B4	0911 B4	0911 C3	1010 B4	1011 A4	1011 C3
0	-0.50	-2.30	-0.95	0.65	0.00	0.25
1	-0.10	-1.25	-0.25	1.25	0.25	1.25
2	0.50	-0.10	0.55	1.85	0.90	1.10
3	0.30	-0.10	0.35	1.90	1.15	1.75
8	0.35	-0.95	0.55	1.80	1.50	1.60

0.5 Micron Devices Dirac Point Voltage by Day

Day	0911 D3	0911 D5	0911 D6	0910 D4	0911 E6	1010 D3	1010 D4	1011 D3	1011 D4	1109 D3	1109 E6
0	0.30	-0.05	0.15	-0.40	0.45	-0.40	-1.15	-0.15	-0.25	-0.35	0.15
1	0.50	0.60	0.35	0.25	0.60	0.25	-0.65	0.35	0.25	0.20	1.65
2	1.15	1.50	1.35	0.70	1.30	0.75	-0.15	1.20	0.85	0.80	1.70
3	1.15	1.45	1.15	0.95	1.90	1.30	0.75	1.20	1.05	2.65	1.35
8	1.10	1.25	1.05	0.90	1.30	1.00	0.30	1.15	1.50	1.15	1.45

Appendix F: Dirac Point Current by Channel Length

10 Micron Devices Dirac Point Current by Day

Day	0909 A1	0910 B1	1009 A1	1009 B1	1010 A1	1010 B1	1011 B1
0	1.88E-04	1.89E-04	2.36E-04	2.22E-04	2.38E-04	2.65E-04	2.44E-04
1	2.03E-04	1.89E-04	2.56E-04	2.31E-04	2.42E-04	2.68E-04	2.44E-04
2	2.02E-04	1.88E-04	2.56E-04	2.31E-04	2.42E-04	2.69E-04	2.46E-04
3	2.03E-04	1.91E-04	2.56E-04	2.31E-04	2.42E-04	2.68E-04	2.47E-04
8	2.01E-04	1.91E-04	2.56E-04	2.30E-04	2.42E-04	2.69E-04	2.45E-04

5 Micron Devices Dirac Point Current by Day

Day	0909 A2	0909 B2	0910 A2	0910 B2	1009 A2	1010 A2	1011 A2
0	4.20E-04	4.73E-04	5.22E-04	3.10E-04	3.73E-04	4.13E-04	4.97E-04
1	2.27E-04	6.02E-04	5.37E-04	3.22E-04	4.35E-04	4.36E-04	5.03E-04
2	5.24E-04	5.64E-04	5.20E-04	3.22E-04	4.37E-04	4.30E-04	5.08E-04
3	2.03E-04	5.98E-04	5.35E-04	3.24E-04	4.35E-04	4.37E-04	5.10E-04
8	5.45E-04	5.55E-04	5.16E-04	3.20E-04	4.34E-04	4.33E-04	5.06E-04

2 Micron Devices Dirac Point Current by Day

Day	0909 G4	0910 A3	0910 F4	0910 H3		
0	1.13E-03	1.27E-03	1.41E-03	1.21E-03		
1	1.51E-03	1.40E-03	1.51E-03	1.33E-03		
2	1.42E-03	1.31E-03	1.41E-03	1.25E-03		
3	1.43E-03	1.37E-03	1.45E-03	1.31E-03		
Day	0911 E3	0911 F4	0911 F6	0911 G4	0911 H4	0911 H5
0	9.82E-04	1.42E-03	7.83E-04	1.23E-03	1.27E-03	1.31E-03
1	1.14E-03	1.56E-03	8.31E-04	1.32E-03	1.37E-03	1.42E-03
2	1.13E-03	1.49E-03	8.03E-04	1.26E-03	1.34E-03	1.39E-03
3	1.13E-03	1.52E-03	8.24E-04	1.30E-03	1.38E-03	1.43E-03
8	1.10E-03	1.51E-03	8.17E-04	1.29E-03	1.37E-03	1.41E-03

Day	1009 E4	1009 E5	1009 G4	1010 A3	1010 B3	1010 G4
0	1.02E-03	1.26E-03	1.07E-03	1.37E-03	1.38E-03	1.31E-03
1	1.47E-03	1.47E-03	1.51E-03	1.50E-03	1.43E-03	1.28E-03
2	1.39E-03	1.42E-03	1.33E-03	1.45E-03	1.41E-03	1.24E-03
3	1.43E-03	1.45E-03	1.47E-03	1.49E-03	1.43E-03	1.26E-03
8	1.45E-03	1.46E-03	1.47E-03	1.47E-03	1.43E-03	1.27E-03

Day	1011 A3	1011 E3	1011 F4	1011 G4	1011 G5	1109 A3	1109 E3
0	1.44E-03	1.31E-03	1.06E-03	1.27E-03	1.31E-03	1.45E-03	3.20E-04
1	1.42E-03	1.36E-03	1.25E-03	1.26E-03	1.37E-03	1.53E-03	4.02E-04
2	1.40E-03	1.36E-03	1.25E-03	1.29E-03	1.35E-03	1.51E-03	3.94E-04
3	1.44E-03	1.38E-03	1.26E-03	1.33E-03	1.38E-03	1.52E-03	3.86E-04
8	1.36E-03	1.33E-03	1.22E-03	1.29E-03	1.32E-03	1.43E-03	3.45E-04

1.5 Micron Devices Dirac Point Current by Day

Day	0910 B4	0911 B4	0911 C3	1010 B4	1011 A4	1011 C3
0	1.91E-03	1.88E-03	1.87E-03	1.93E-03	1.63E-03	1.87E-03
1	2.12E-03	2.07E-03	2.06E-03	1.94E-03	1.80E-03	1.99E-03
2	2.01E-03	2.01E-03	2.00E-03	1.58E-03	1.76E-03	1.72E-03
3	2.02E-03	2.07E-03	2.06E-03	1.92E-03	1.86E-03	2.00E-03
8	2.03E-03	2.00E-03	1.94E-03	1.80E-03	1.80E-03	1.95E-03

1.25 Micron Devices Dirac Point Current by Day

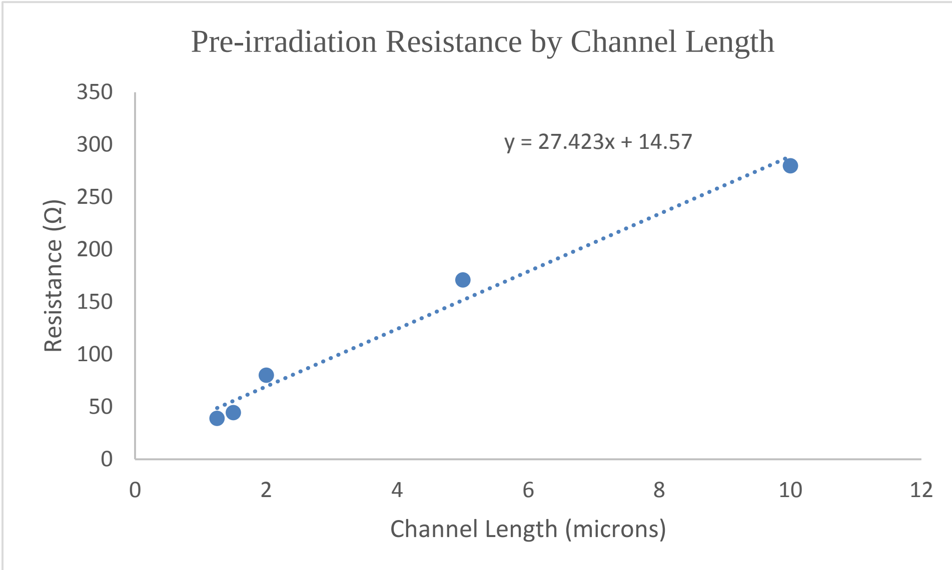
Day	1011 C4
0	2.37E-03
1	2.72E-03
2	2.49E-03
3	2.76E-03
8	2.66E-03

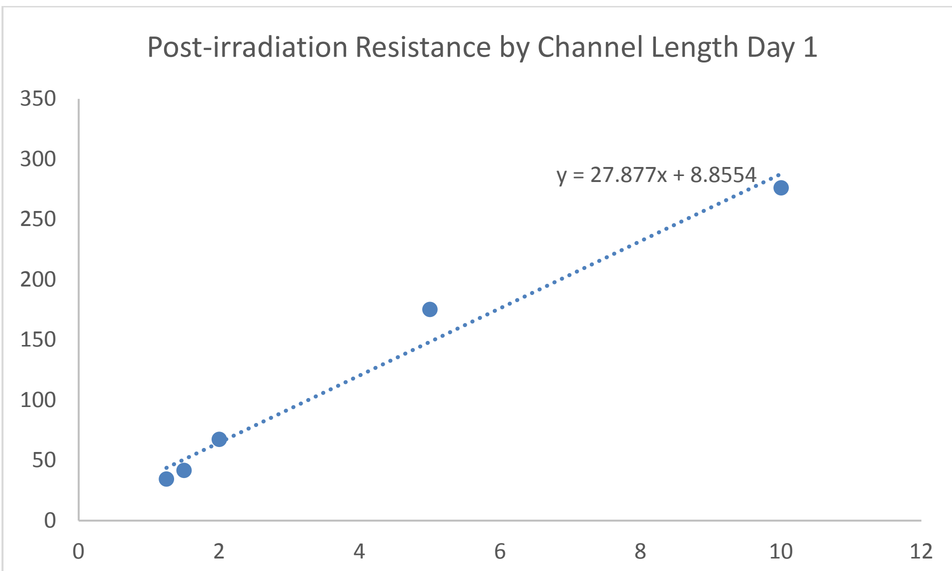
0.5 Micron Devices Dirac Point Current by Day

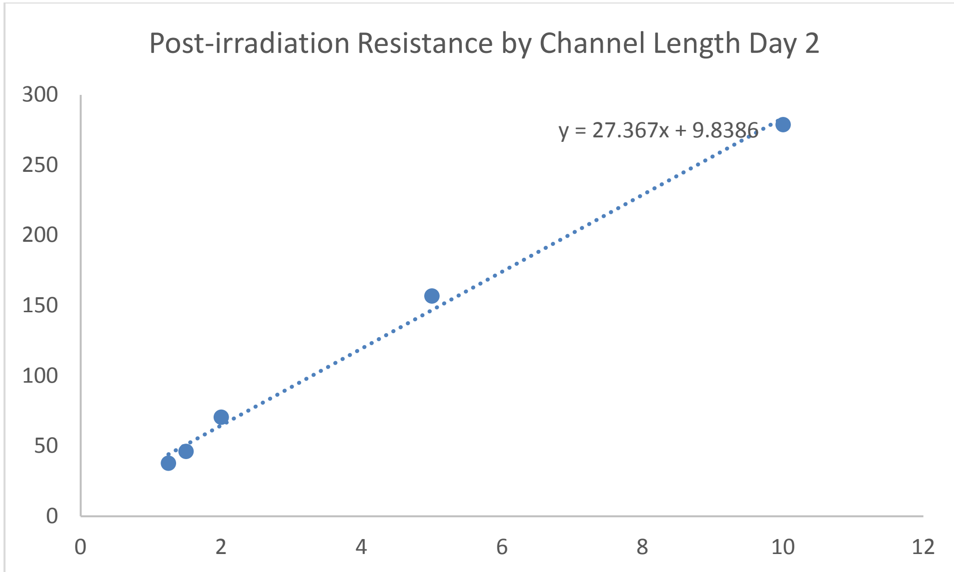
Day	0910 D4	0911 D3	0911 D5	0911 D6	0911 E6	1010 D3
0	8.17E-04	8.57E-04	7.69E-04	8.67E-04	8.86E-04	6.83E-04
1	8.89E-04	8.94E-04	8.43E-04	9.26E-04	9.51E-04	7.01E-04
2	8.63E-04	8.87E-04	8.00E-04	8.87E-04	9.25E-04	6.60E-04
3	8.92E-04	9.01E-04	8.47E-04	9.27E-04	9.57E-04	7.04E-04
8	8.76E-04	8.76E-04	8.41E-04	9.12E-04	9.46E-04	6.57E-04

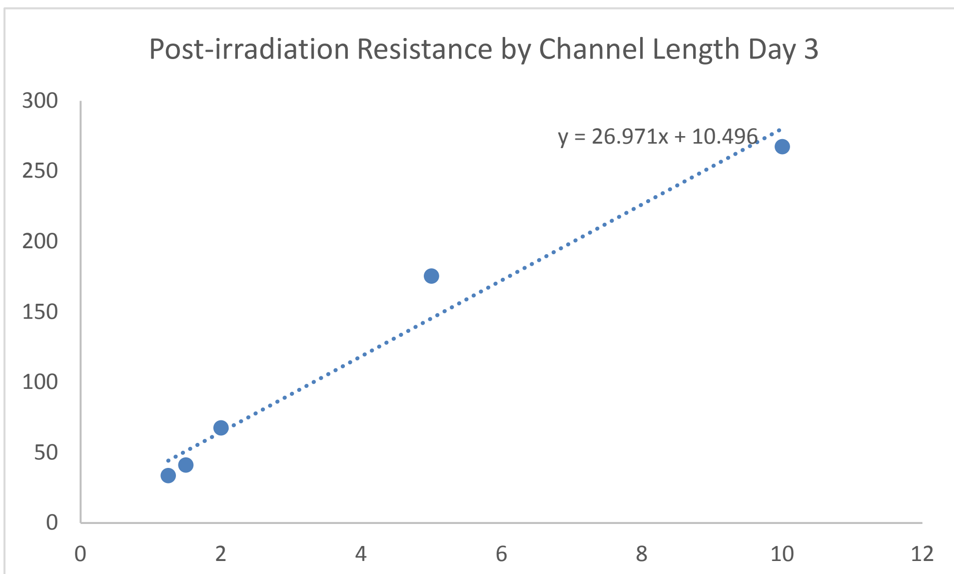
Day	1010 D4	1011 D3	1011 D4	1109 D3	1109 E6
0	7.80E-04	8.52E-04	8.51E-04	7.16E-04	4.81E-04
1	7.98E-04	8.68E-04	8.81E-04	7.79E-04	8.28E-04
2	7.62E-04	8.70E-04	8.93E-04	8.01E-04	8.30E-04
3	8.01E-04	8.58E-04	9.03E-04	8.06E-04	8.26E-04
8	7.71E-04	8.69E-04	8.93E-04	7.84E-04	8.24E-04

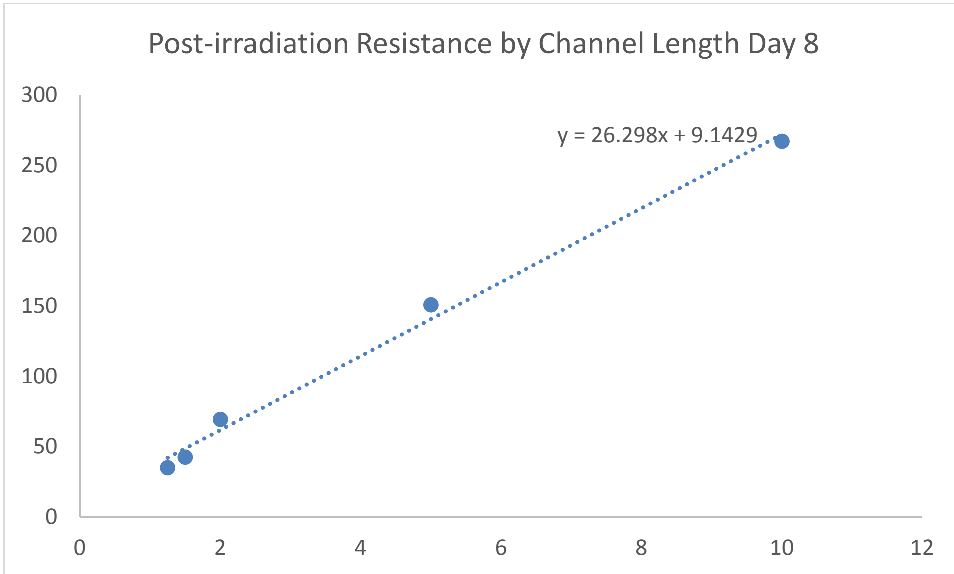
Appendix G: Resistance by Channel Length by Day






Post-irradiation Resistance by Channel Length Day 2
y = 27.367x + 9.8386
300
250
200
150
100
50
0
0
2
4
6
8
10
12


Post-irradiation Resistance by Channel Length Day 3
y = 26.971x + 10.496
300
250
200
150
100
50
0
0
2
4
6
8
10
12


Post-irradiation Resistance by Channel Length Day 8
y = 26.298x + 9.1429
300
250
200
150
100
50
0
0
2
4
6
8
10
12

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14. ABSTRACT

Hexagonal Boron Nitride (hBN) has been proposed as a better substrate material in place of SiO_2 for graphene electronic devices, especially Graphene Field Effect Transistors (GFETs), because of its lattice match to graphene and the absence of dangling chemical bonds on its planar surface. The performance of GFETs on hBN substrates is becoming increasingly well documented, but little is known about the tolerance of these devices to large doses of ionizing radiation, such as that encountered in many DoD satellite orbits. In this study, the current-voltage transconductance curves of top-gated GFET devices were measured before and after exposure to 1.7 Mrad (SiO_2) total dose from ^{60}Co gamma rays. Post-irradiation, the devices showed a distinct positive voltage shift in the charge neutrality point (a.k.a. Dirac point) of the transconductance curves averaging 1.3 Volts. This shift suggests an increase in the effective hole doping of the graphene caused by a net trapped charge density of $3x10^{12}$ electrons cm^{-2} at one of the graphene interfaces, or possibly trapped electrons at the interface between the hBN layer and the underlying sapphire substrate. The voltage shift associated with this trapped charge was observed to build up for two days post-irradiation before saturating and remaining stable at room temperature. The post-irradiation magnitude of source-drain current showed a slight increase at the Dirac point, staying within 10% of the pre-irradiation levels. The carrier mobility extracted from the transconductance curves also showed a slight increase, remaining on average within 25% of pre-irradiation levels. Possible mechanisms for radiation-induced hole doping of the graphene are briefly considered, but additional experiments are required to distinguish between these possibilities. The observation of only modest changes in the transconductance curves following this relatively high total ionizing dose shows promise for the radiation resistance of these devices.

15. SUBJECT TERMS
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