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POWER ANALYSIS OF AN ENTERPRISE WIRELESS COMMUNICATION ARCHITECTURE

by

Howen Q. Fernando

September 2017

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POWER ANALYSIS OF AN ENTERPRISE WIRELESS COMMUNICATION ARCHITECTURE

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ABSTRACT

Technological advancements in Software Defined Radios (SDR), high-speed serial buses, and high-performance computing systems have brought us a power reduction breakthrough in military wireless communications. This thesis develops and analyzes a model to demonstrate that an enterprise computing architecture for Software Defined Radios results in significant power savings between 11% and 13% under ordinary operational loads. The thesis presents easy-to-understand mathematical power consumption models and simulations of general military communications systems in an Expeditionary Command, Control, Communications, and Computers (C4) scenario. The comparison of regular versus enterprise SDR architectures exposes the power savings realized in the Enterprise Wireless Communications (EWC) architecture.

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LIST OF ACRONYMS AND ABBREVIATIONS

ADC	Analog to Digital Converter
AEP	Application Environment Profile
API	Application Program Interface
BBU	Base Band Unit
C4	Command Control Communications and Computers
CERDEC	Communications-Electronic Research, Development and Engineering Center
COMCAS	Conference on Microwaves, Communications, Antennas and Electronic Systems
DAC	Digital to Analog Converter
DOD	Department of Defense
DSA	Dynamic Spectrum Allocation
EW	Electronic Warfare
EWC	Enterprise Wireless Communication
FPGA	Field Programmable Gate Array
GPP	General Purpose Processors
HSSI	High Speed Serial Interface
IEEE	Institute of Electrical and Electronics Engineers
InTop	Integrated Topside
IPS	Instructions per Second
IoT	Internet of Things
JTNC	Joint Tactical Networking Center
L-RTac	Long-Range Tactical
L-RTacAJ	Long-Range Tactical Anti-Jam
M-RTac	Medium-Range Tactical
MORA	Modular Open Radio Architecture
N/A	Not Applicable
NPS	Naval Postgraduate School
OV-1	Operational Viewpoint - 1
PAM	Pulse-Amplitude Modulation

PRIME	Ph.D. Research in Microelectronics and Electronics
R&D	Research and Development
RF	Radio Frequency
RHM	Radio Head Module
Rx	Receiver
S-RTac	Short-Range Tactical
SCA	Software Communications Architecture
SDR	Software Defined Radio
SOF	Special Operations Forces
SPAWAR	Space and Naval Warfare
SSC	SPAWAR Systems Center
SWaP	Size Weight and Power
SWaP-C	Size Weight Power and Cost
TREND	Towards Real Energy-efficient Network Design
Tx	Transmitter
U	Unclassified
UAS	Unmanned Aircraft System
USB	Universal Serial Bus
USSOCOM	United States Special Operations Command

I. INTRODUCTION

The increasing demand for wireless communications in the military increases the amount of energy needed for missions. The Internet of Things (IoT) movement (Thomas, McPherson, and Irvine 2016), which has already manifested itself in the battlefield, is driving people's increasing appetite for wireless connectivity. The Operational Viewpoint-1 (OV-1) in Figure 1 illustrates the necessity for communications and how an Expeditionary Command, Control, Communications, and Computers (C4) Node is the hub of the communications network. Figure 1 also illustrates how an Expeditionary C4 Node is isolated from any energy supply infrastructure.

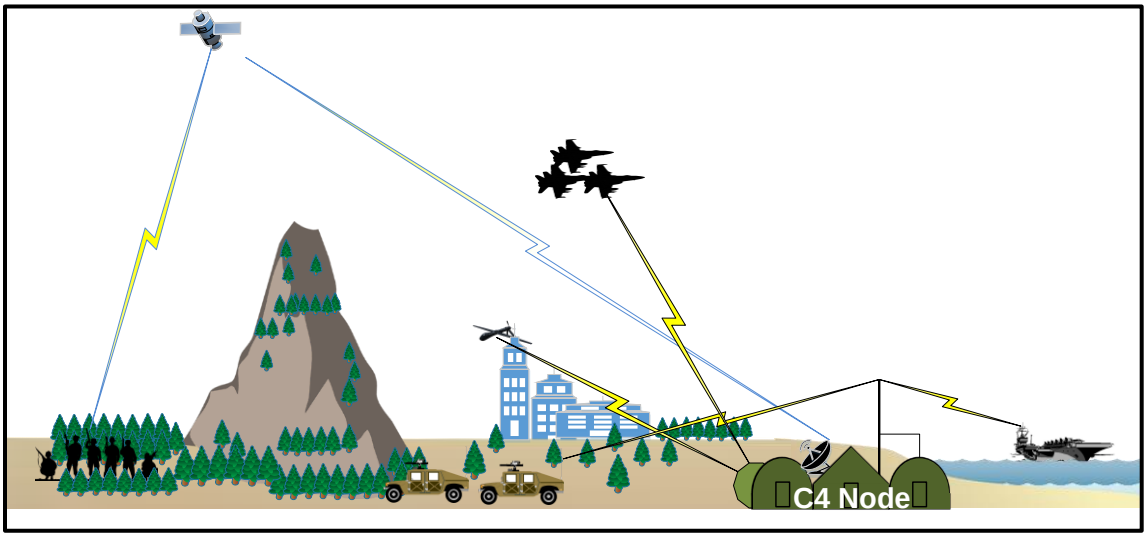

Figure 1. OV-1 Diagram of an Expeditionary C4 Node

Industry is now using the Enterprise Wireless Communication (EWC) architecture approach for cellular base stations to address the increasing demand while matching the processing capacity requirement (Conte 2012). The U.S. Army and the U.S. Navy have research and development (R&D) projects that use the EWC architecture approach. However, the extant research has not looked at the EWC architecture as a power-saving mechanism, because the research is first addressing the need for connectivity (Hasik 2017). This thesis hypothesizes that EWC architecture for

Expeditionary C4 nodes reduces powered redundancies such as processors, and power supplies, thereby reducing overall power consumption.

A. BACKGROUND

Figure 2 shows the EWC architectural concept, which includes Radio Head Modules (RHM) (Conte 2012), an Enterprise Server, and Terminals. The RHM, located near the antenna, translates Radio Frequency (RF) signals to digital signals and vice versa. The enterprise server, which Conte (2012) calls "base band unit (BBU) in large cabinets" (7), implements the software functions of a Software Defined Radio (SDR) (Conte 2012). The enterprise server modulates information for transmission, and the RHM synthesizes the modulated data into RF signals for the antenna to radiate (Intelligence & Information Warfare Directorate 2017). Likewise, the antenna receives the RF signals, the RHM digitizes the RF signals, and the enterprise server demodulates the digitized RF (2017). The terminals execute applications to perform higher-level functions like user interfaces, integrated displays, and maintenance functions (Intelligence & Information Warfare Directorate 2017).

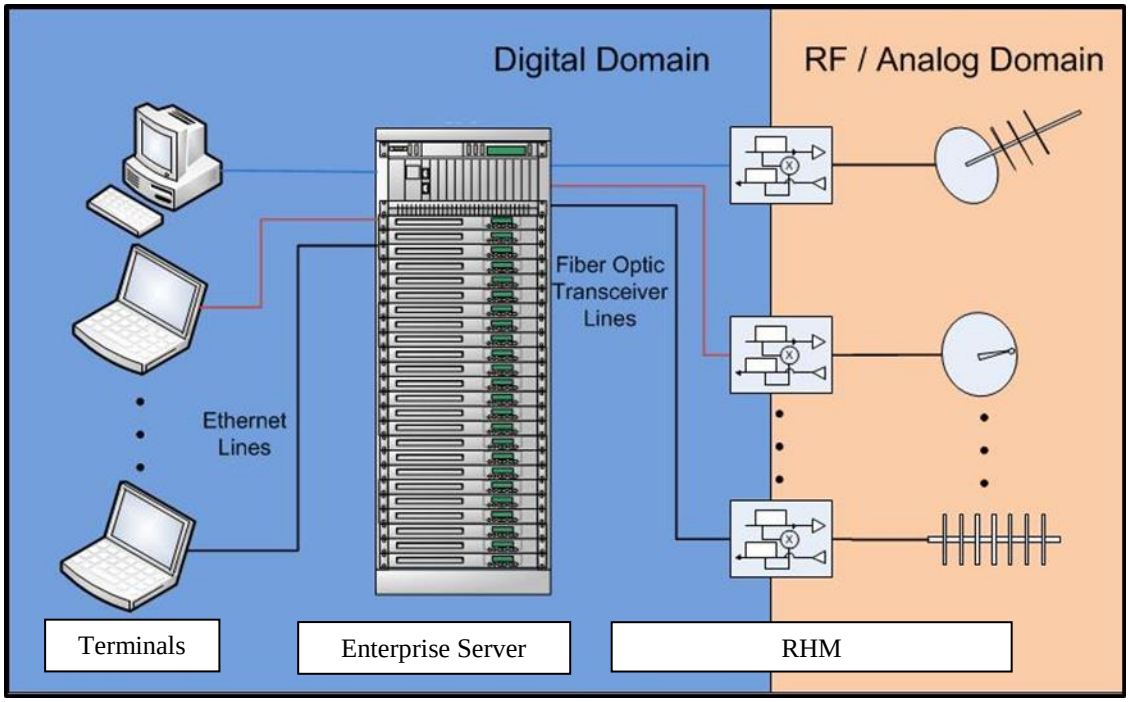

Figure 2. EWC Architecture

The EWC architecture has all the advantages of an enterprise system (Goldworm and Skamarock 2007), such as improved reliability, improved maintainability and affordability, and could reduce the power requirement of the system. Currently, Expeditionary C4 nodes employ a collection of disparate communication systems, which have redundant power systems and processing systems. An enterprise system incorporates redundant back up processing sub-systems that remain powered off when not required. An enterprise architecture allows for easier and inexpensive upgrade of the enterprise server when performance and higher efficiency processors become available. Moreover, software is portable from the older enterprise system to the next generation enterprise system (Goldworm and Skamarock 2007).

This thesis analyzes the power consumption used for communication systems in an Expeditionary C4 node by using mathematical modeling and simulation. Another type of power consumption analysis, which requires power measurements on actual hardware, is out of scope for this thesis due to resource and time constraints. The power consumption of subsystems provides the baseline for the mathematical models. The

power state of sub-systems for different power modes, and the usage profiles provide the equations for the model. Mathematical models of generalized communication systems in an Expeditionary C4 node provide the basis for the simulation of power consumption. The power simulation provides a comparison and analysis of both existing and enterprise-based communication architecture. The analysis also identifies other potential power savings for future systems.

B. OBJECTIVE

The main objective is to determine any significant power consumption reduction in wireless communication systems used for Expeditionary C4 node missions when adopting an enterprise approach. It is necessary to mathematically model and simulate the current architecture communication systems and their equivalent EWC architecture version to derive and compare their power consumptions. It is also necessary to research power parameters of various communication systems for the mathematical model.

C. BENEFITS TO THE DEPARTMENT OF DEFENSE

SDR technology meets the unique communications requirements of the military and the EWC architecture is a conceivable evolution of SDRs for the military. While industry tends to use hard-coded highly integrated solutions for communications, the military needs the flexibility of SDRs. With the increasing need for wireless communications (Arnold et al. 2010), the EWC architecture approach has potential to improve Size Weight, Power, and Cost (SWaP-C), and could improve maintainability, reliability, and usability.

This thesis focuses on the potential power consumption improvements by adopting the EWC architecture approach to benefit Expeditionary C4 nodes. Expeditionary C4 nodes have limited power, necessary support, and back-up systems. It is difficult to sustain extended Expeditionary C4 node operation, with such demand for power and logistical infrastructure, and with such strain to supply and logistics lines.

Although beyond the scope of this thesis, the EWC architecture should also reduce the amount of support and back-up system requirements (Schilling 2000). The

high degree of modularity in the EWC architecture system leads to smaller sub-units that require less back-up volume/weight for transport. Modular components and flexibility of physical configuration improves maintainability and usability. In general, there should be a reduction in the required resources to operate the system (Schilling 2000).

The EWC architecture is a paradigm shift that may "disrupt" the current architectural concepts of future communication systems, creating an evolutionary change with immense potential. This concept is now within the means of current technology, with relatively low-risk and high potential payoff. Follow-on to this thesis could extend into more research and development in exploring more performance improvements such as the following:

Navy Benefit—Spectrum and Waveform Maneuverability in Ship Communications: The EWC architecture could re-route any function requiring communications, to any available infrastructure and RF channel; thus maintaining the function in adverse conditions.

United States Special Operations Command (USSOCOM)—Integrated Modular Communications: Bulky disparate units create undue burden and danger to Special Operations Forces (SOF). The EWC architecture would reduce Size Weight and Power (SWaP) by using a single processing sub-system as an enterprise-based communication system. As an example, a SOF warfighter may easily plug a satellite-based communication module into the enterprise processor when needed. Once plugged-in, it automatically runs the corresponding waveform software—much like a Universal Serial Bus (USB) peripheral.

Army—Soldier-based Enterprise System: Soldiers, who now communicate more information, are starting to use a selection of wearable modular systems that communicate wirelessly with one another. The EWC architecture system would reduce the SWaP by using a singular processing/computing module to run user applications and to implement waveform algorithms. This approach would make it easier to integrate various systems used by a soldier and to create interoperability between various wearable tactical communication systems.

Joint—Dynamic Spectrum Allocation (DSA): The federal government has auctioned-off the spectrum to industry; requiring future systems the ability to move to a different spectrum band on-demand. The enterprise architecture would have an inherent mechanism to manage spectrum allocation dynamically. The spectrum becomes completely visible to the enterprise system; allowing the enterprise to easily determine allocation.

D. EXTERNAL ORGANIZATIONS

Three organizations within the Department of Defense (DOD) are leading the way for EWC architecture implementation. The Joint Tactical Networking Center (JTNC), the U.S. Army Communications-Electronic Research, Development and Engineering Center (CERDEC), and the U.S. Navy Space and Naval Warfare (SPAWAR) Systems Center (SSC) – Pacific are able to contribute uniquely to realize EWC architecture in the DOD.

1. JTNC

The JTNC is the joint DOD organization in charge of the Software Communications Architecture (SCA) standard. JTNC provided information, from their publicly released documents on SCA and corresponding Application Program Interfaces (API). The SCA is an enabler to the EWC architecture, thus the JTNC organization is relevant for future reference.

2. U.S. Army CERDEC

CERDEC is a U.S. Army research center developing and testing a limited EWC architecture implementation for vehicular use called Modular Open Radio Architecture (MORA) (Intelligence & Information Warfare Directorate 2017). The research process performed for this thesis led to the author's discovery of MORA. MORA, which is in the development phase, does not have a requirement for power efficiency. MORA developers explained the enterprise approach in saying that "shared hardware devices reduce SWaP impact by allowing systems to use common processing resources and user interface devices" (2017). CERDEC is a R&D hub for the U.S Army and would likely be a stakeholder for the information in this research and a partner for any future EWC

architecture effort for Expeditionary C4 requirements (Intelligence & Information Warfare Directorate 2017).

3. U.S. Navy SSC—Pacific

SSC–Pacific is a U.S. Navy research center collaborating with ONR to develop and test an EWC implementation called Integrated Topside (InTop) (Tavik et al. 2010). Discovery of the InTop effort occurred during the research process performed for this thesis. InTop, which is for shipboard use does not have a requirement for power efficiency. However, EWC architecture may have utility for the U.S. Marine Corps Expeditionary C4 nodes and SSC–Pacific may be a relevant collaborator for future work (Tavik et al. 2010).

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II. ENABLING TECHNOLOGIES

Technologies have matured or reached a milestone advancement that allow the realization of EWC architecture. These technologies are SDRs, Enterprise Processing Systems, Modular Open Systems Architectures (MOSA), and High-Speed Serial Interfaces (HSSI).

A. SDR

The introduction of Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC), and the performance improvements in General Purpose Processing brought us SDRs (Brannon 2004). Initially, the 1980s brought us digital radios from the introduction of ADCs and DACs. Early digital radios allowed the use of simple waveforms in specialized digital subsystems to implement modulators and demodulators. Digital radios modulate digital information into an analog signal for transmission, and digitize demodulated incoming analog signals. In the 1990s, General Purpose Processor (GPP) technology improved enough to allow a wide variety of waveforms to run in the GPP; thus giving rise to the SDR (Brannon 2004).

Today's technologies of high-speed ADCs and DACs, in conjunction with high-speed processing systems, have reached milestone advancement in SDRs. Today's SDRs can implement complex modulation and demodulation algorithms in software to increase the amount of digital information transmitted and received, at any given frequency and time.

Figure 3 shows the architectural pattern that is common to all SDRs. This architectural pattern is the basis for creating the mathematical model used in this thesis.

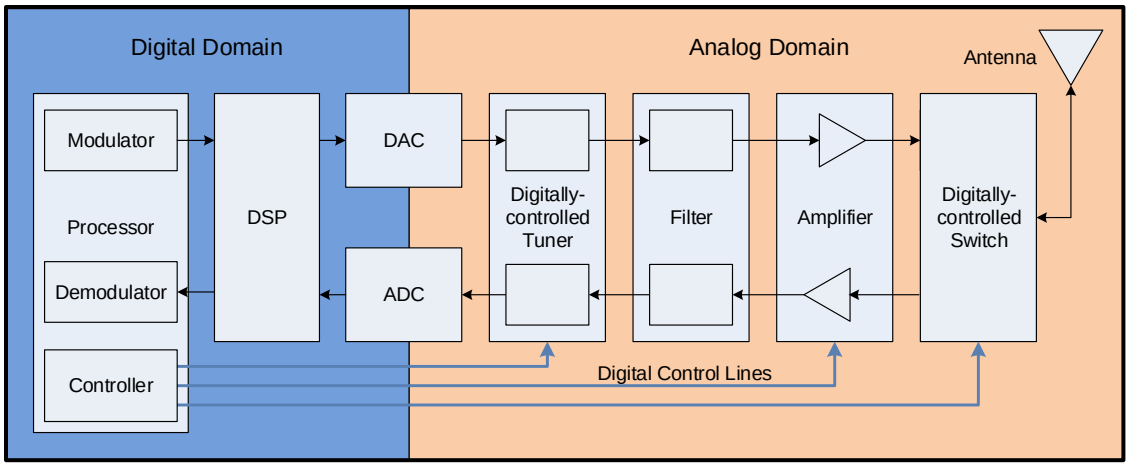


Figure 3. SDR Architecture. Adapted from Arnold et al. (2010), Baliga et al. (2011), and Thomas, McPherson, and Irvine (2016).

B. ENTERPRISE PROCESSING SYSTEMS

Advancements in processing performance and high-speed processing node connectivity have brought about an enormous processing capability (Goldworm, and Skamarock 2007). Processing nodes now have multiple processor with multiple processing cores that can process more data and faster than ever before. Moreover, processing capability scales up with the addition of processing nodes that communicate with other processing nodes at very high speeds. Interconnected processing nodes form a high-performance computing environment called cluster. A large cluster is the technology behind cloud computing. A cluster, or enterprise-computing environment, can process multiple waveforms simultaneously (Goldworm, and Skamarock 2007).

C. MOSA

MOSA provides a framework for streamlining the implementation of waveforms in an enterprise environment. MOSA provides the mechanism to use interoperable waveform software modules in an enterprise environment. MOSA can also provide an abstraction between the hardware and the software to allow plug and play capability for any waveform to run within the enterprise. SCA is a specific example of MOSA that creates a highly modularized architecture, which detaches the waveform application from the underlying hardware platform (DOD Waveform Standards Directorate 2016). SCA

simplifies the implementation of multiple waveforms in SDR (2016). Figure 4 shows the SCA, which is a DOD standard architecture to enable portability/reusability and interoperability of the waveform applications across hardware platforms; thereby reducing total life cycle cost attributed to repeated re-implementation of software on new hardware platforms (DOD Waveform Standards Directorate 2016).

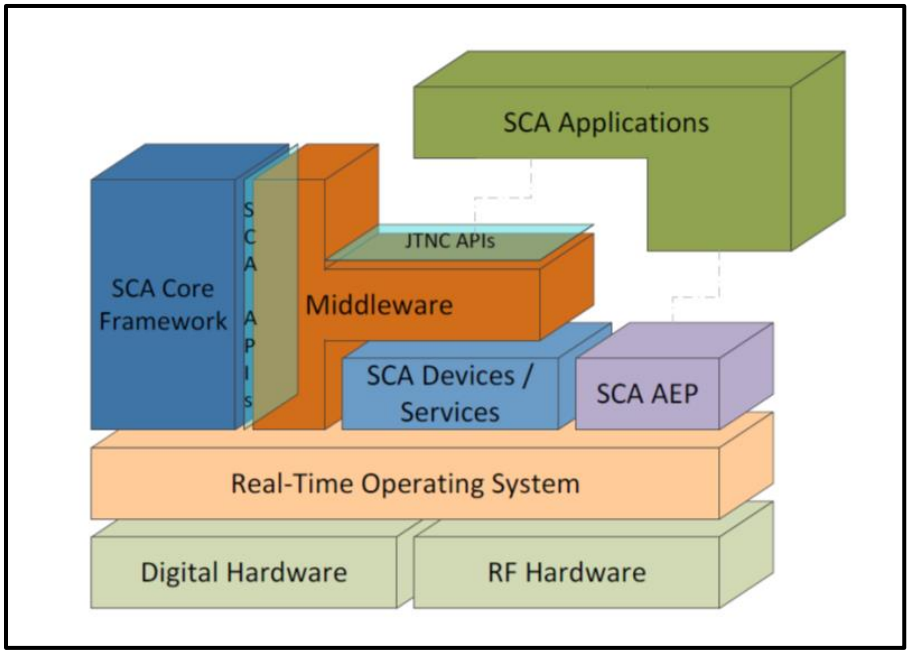


Figure 4. Layered View of SCA Adapted from DOD Waveform Standards Directorate (2016)

D. HSSI

The enterprise server needs to transmit and receive digital signals to and from the RHM at very high speeds. The digital signals, which require more than 10 gigabits per second of data throughput, would be too expensive to implement via parallel interface. The latest serial ports implemented in Field Programmable Gate Arrays (FPGA) has reached 10s of gigabits per second, and the industry leaders in FPGA systems have also announced one terabit per second dual mode serial port capability in the future (Xilinx 2017).

Figure 5 shows the RHM, which adds a high-speed serial interface over fiber optics to the modulator/demodulator in the enterprise server. By design, the RHM resides by the antenna to attain a high Signal to Noise Ratio (SNR), which is strongest by the antenna and preserved as a discrete value in the ADC digitization process.

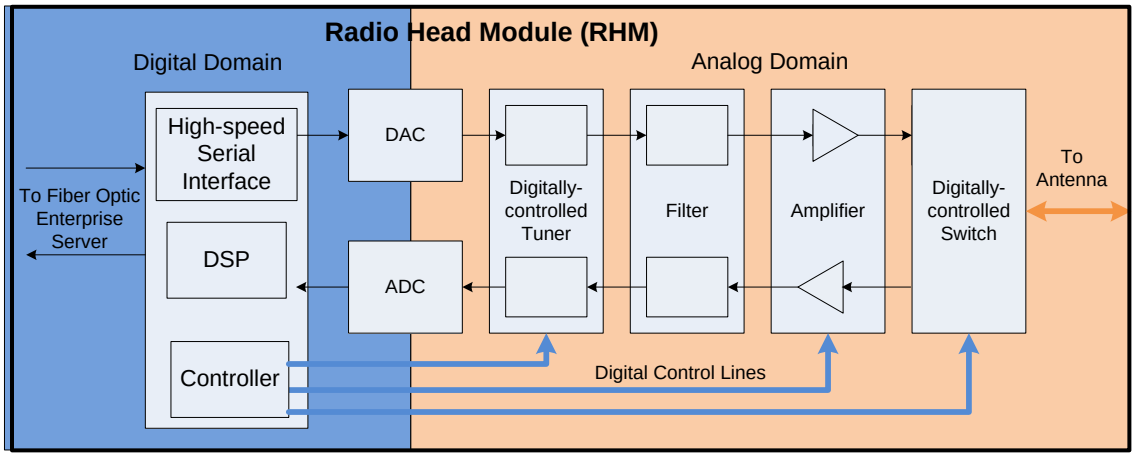


Figure 5. Architectural View of the RHM

III. METHODOLOGY

A. KEY PERFORMANCE PARAMETERS

The general parameter in this thesis is power, which is the rate of energy use. The unit for Power is Watts—equivalent to Joules/second. Instantaneous Power and Power Consumption are two forms of power measurements us as the Key Performance Parameters for this thesis.

1. Instantaneous Power

Equation 1 shows the formula for calculating the total instantaneous power of the SDR from each component in the architecture shown in Figure 6. This formula is the basis for the mathematical model.

Equation 1. Total Instantaneous Power

$$\text{Power}_{\text{Total}}\,(\text{Watts}) = P_{MOD} + P_{DEM} + P_{CON} + P_{DSP} + P_{DAC} + P_{TxTun} + P_{RxTun} + P_{TxFltr} + P_{RxFltr} + P_{TxAmp} + P_{RxAmp} + P_{Switch}$$

Where:

P_{MOD}	=	Instantaneous Power Contribution of the Modulator (Watts)
P_{DEM}	=	Instantaneous Power Contribution of the Demodulator (Watts)
P_{CON}	=	Instantaneous Power Contribution of the Controller (Watts)
P_{DSP}	=	Instantaneous Power Contribution of the DSP (Watts)
P_{DAC}	=	Instantaneous Power Contribution of the DAC (Watts)
P_{TxTun}	=	Instantaneous Power Contribution of the Tx Tuner (Watts)
P_{RxTun}	=	Instantaneous Power Contribution of the Rx Tuner (Watts)
P_{TxFltr}	=	Instantaneous Power Contribution of the Tx Filter (Watts)
P_{RxFltr}	=	Instantaneous Power Contribution of the Rx Filter (Watts)
P_{TxAmp}	=	Instantaneous Power Contribution of the Tx Amplifier (Watts)
P_{RxAmp}	=	Instantaneous Power Contribution of the Rx Amplifier (Watts)
P_{Switch}	=	Instantaneous Power Contribution of the Switch (Watts)

The instantaneous power consumption of components is the input to the model and simulation used for this thesis. Instantaneous power consumption is the power used by a system or component at any given time—the unit is Watts. Research of system and component description, and Subject Matter Expert (SME) interview provided the

instantaneous power consumption of components. Figure 6 shows the component architecture of an SDR and the different instantaneous power consumption labels used in the mathematical model.

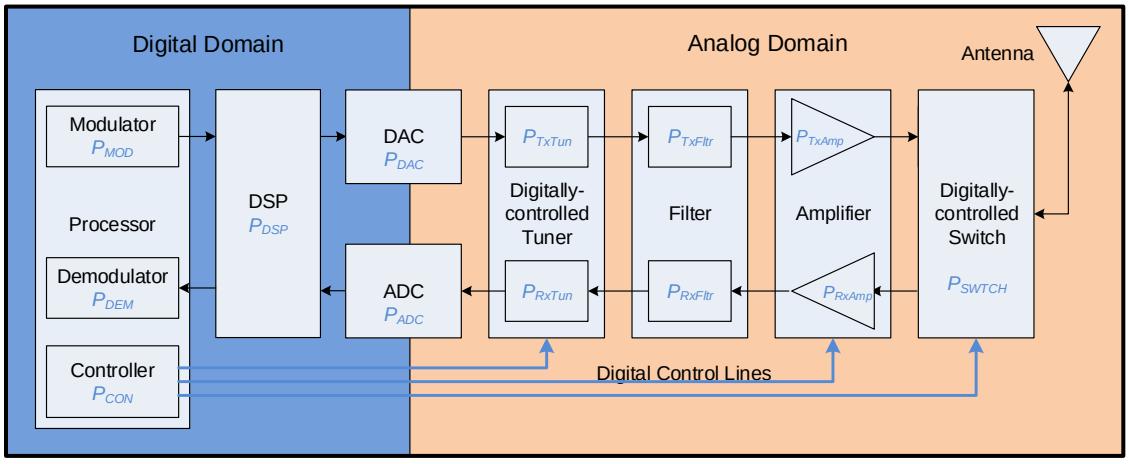


Figure 6. SDR Power Architecture

2. Power Consumption

Power consumption parameter is the output of the simulation and comparison point for the analysis. Power consumption is the amount of energy used for a given span of time—the unit is Watt-Hour. Equation 2 shows the power consumption formula, which uses the total instantaneous power calculated in Equation 1.

Equation 2. Power Consumption

PowerConsumption (Watt-Hr) = $Power_{Total} \; x \; Time$

Where:

$Power_{Total}$	=	Total Instantaneous Power (Watts)
$Time$	=	Time (Hours)

B. POWER CONSUMPTION SIMULATION

Power consumption is the basis for the simulation of various SDRs in this thesis. Power consumption, based on researched instantaneous power characteristics, is calculated and assigned to each architectural component for every power mode—sleep, standby, transmit, and receive. The total power consumption for each mode is an aggregate of each component's power consumption in that mode.

The efficiency of the power supply used in the system or sub-system modifies the total power consumption. Traditional SDRs use linear power supplies, which add very little noise to the system. However, linear power supplies perform at 40–60% efficiency. The simulation used 50% efficiency. An enterprise-based SDR implements the modulator and demodulator at the enterprise system, which uses a more efficient switching power supply. Switching power supplies perform at 70–85% efficiency. The simulation used 77.5% efficiency for modulator and demodulator components in the simulation of the enterprise architecture (Acopian n.d.).

1. Instantaneous Power in Sleep Mode

The sleep mode is the state when the SDR is not transmitting or receiving. An SDR with an active power management capability turns off power domains or puts low-power-capable devices in the low-power state. Figure 7 shows components in low-power state as grayed-out components. In this state, the controller is usually in stand-by and is responsible for bringing back components from the low-power state. SDRs without active power managers have sleep mode power characteristics that are equal to their standby mode characteristics.

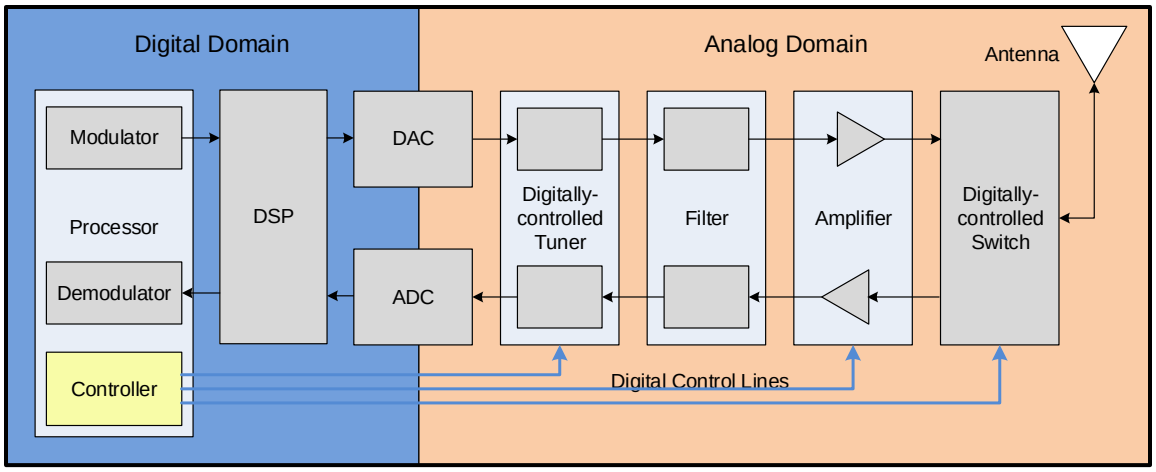


Figure 7. SDR Architecture in Sleep Mode

2. Instantaneous Power in Standby Mode

The standby mode is the state when the SDR is waiting to transmit or receive. This means components in the system are in a regular power state but are not yet running at capacity. Figure 8 illustrates components in standby as yellow-shaded components.

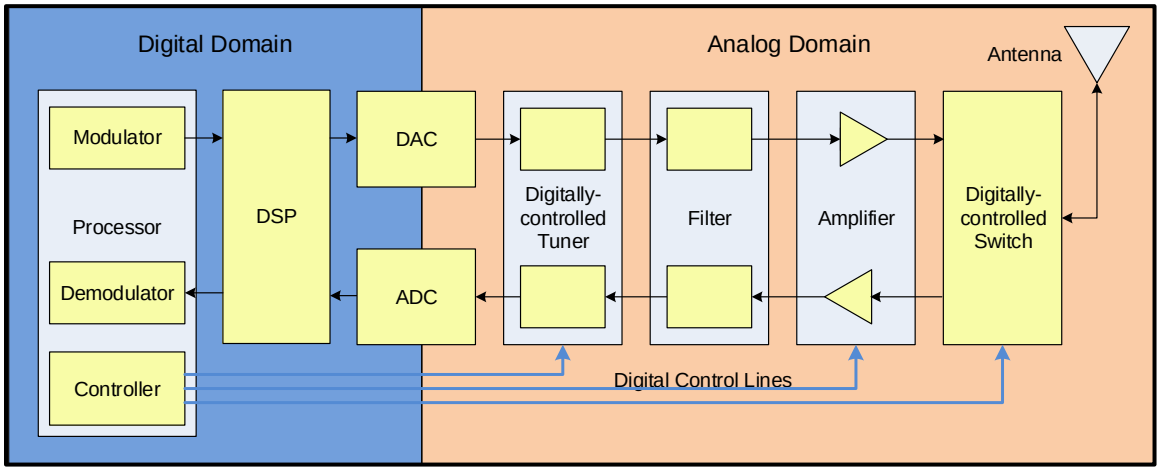


Figure 8. SDR Architecture in Stand-by Mode

3. Instantaneous Power in Transmit Mode

The transmit mode is the state when the SDR is actively transmitting signals. In this mode, the processor creates modulated digital signals for DAC conversion to analog

signals. The analog signals go thru the amplifier for amplification then radiation from the antenna. This means the whole transmit chain is on and the processor is running, while the receive chain is on stand-by. Figure 9 shows the whole transmit chain in green, and the receive chain in yellow.

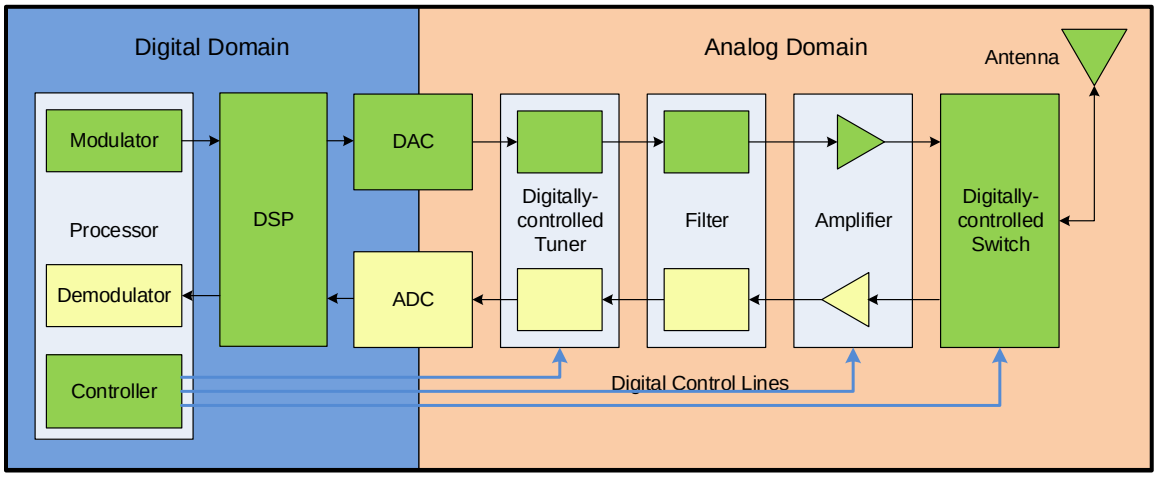


Figure 9. SDR Architecture in Transmit Mode

4. Instantaneous Power in Receive Mode

The receive mode is a state where the SDR is receiving actual information Over the Air (OTA). In this mode, the antenna captures radiated signals, for amplification, conversion to digital signals, and demodulation by the processor. This means the whole receive chain is on and the processor is performing the modulation process, while the transmit chain is on stand-by. Figure 10 shows the receive chain in green, and the transmit chain in yellow. Although a SDR can transmit and receive at the same time (full duplex), it is only modeled in half duplex for simplification.

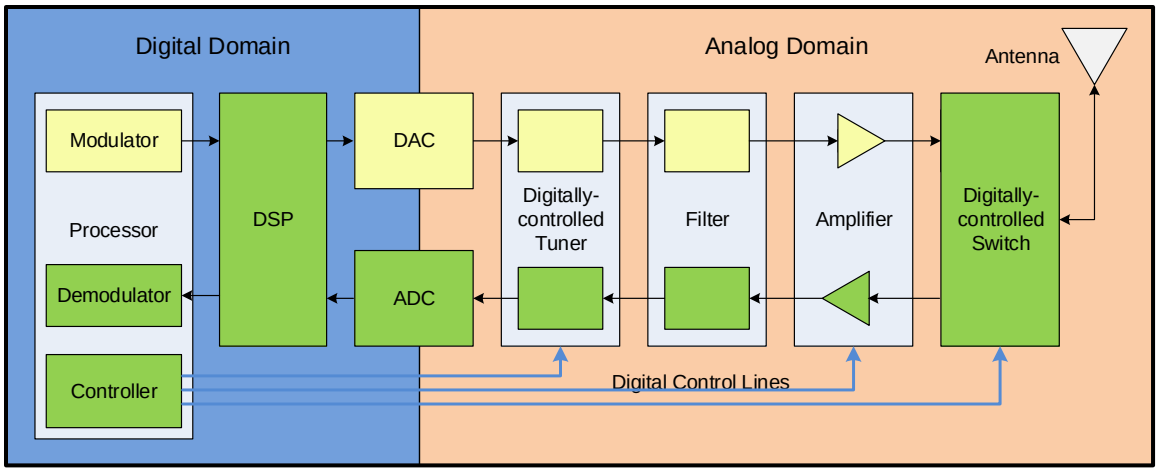


Figure 10. SDR Architecture in Receive Mode

5. Average System Weekly Power Consumption

Since instantaneous power varies throughout the operational scenario, this thesis simulates average power consumptions for three usage conditions—light usage, medium usage, and heavy usage. Table 1 shows how each usage condition has varied duty cycles for each mode. Equation 3 shows the calculation of Average System Weekly power consumption.

Table 1. Usage Profiles

Mode	Light Usage Duty Cycle	Medium Usage Duty Cycle	Heavy Usage Duty Cycle
Sleep	10%	0%	0%
Standby	30%	20%	0%
Transmit	30%	40%	50%
Receive	30%	40%	50%
Total	100%	100%	100%

Equation 3. Average System Weekly Power Consumption

$$AveSystemWeeklyPower\ (Watt\text{-}Hr) = (P_{SLEEP} \times DC_{SLEEP} + P_{STDBY} \times DC_{STDBY} + P_{TX} \times DC_{TX} + P_{RX} \times DC_{RX}) \times Time / PwrSupEff$$

Where:

P_{SLEEP}	= Total Instantaneous Sleep Power of the System (Watts)
P_{STDBY}	= Total Instantaneous Standby Power of the System (Watts)
P_{TX}	= Total Instantaneous Transmit Power of the System (Watts)
P_{RX}	= Total Instantaneous Receive Power of the System (Watts)
$Time$	= Hours in a Week (Hours)
$PwrSupEff$	= Power Supply Efficiency (%)
DC_{SLEEP}	= Duty Cycle of Sleep Mode (%)
DC_{STDBY}	= Duty Cycle of Standby Mode (%)
DC_{TX}	= Duty Cycle of Transmit Mode (%)
DC_{RX}	= Duty Cycle of Receive Mode (%)

C. GENERAL MILITARY COMMUNICATION SYSTEMS

An Expeditionary C4 node may have many tactical communications systems to communicate with various tactical assets. This thesis only used four general types to simplify the mathematical model and simulation. The general types are Short-range Tactical (S-RTac), Medium-range Tactical (M-RTac), Long-range Tactical (L-RTac), and Long-range Tactical Anti-Jam (L-RTacAJ).

1. S-RTac System Description

The S-RTac System represents a short-range tactical communication system with old technology and without power management. The S-RTac is typical for security and logistics operations communications within premises.

2. M-RTac System Description

The M-RTac System represents a medium-range tactical communication system with moderately recent technology and with some power management. The M-RTac System is typical for ground tactical communications.

3. L-RTac System Description

The L-RTac System represents a long-range tactical communication system, with new technology, power management, and a medium complexity waveform. The L-RTac System is typical for ground to air tactical communications.

4. L-RTacAJ System Description

The L-RTacAJ represents a long-range tactical communication system, with new technology, power management, and a complex anti-jam waveform. The L-RTacAJ System is typical for ground to air communications with Unmanned Aircraft Systems (UAS) and air-based weapons systems.

IV. CURRENT ARCHITECTURE

Figure 11 depicts an Expeditionary C4 node with the four general military communications systems described in Chapter III, Section.C. Just like in existing C4 nodes, these four systems are disparate communication systems that do not combine and share processing resources.

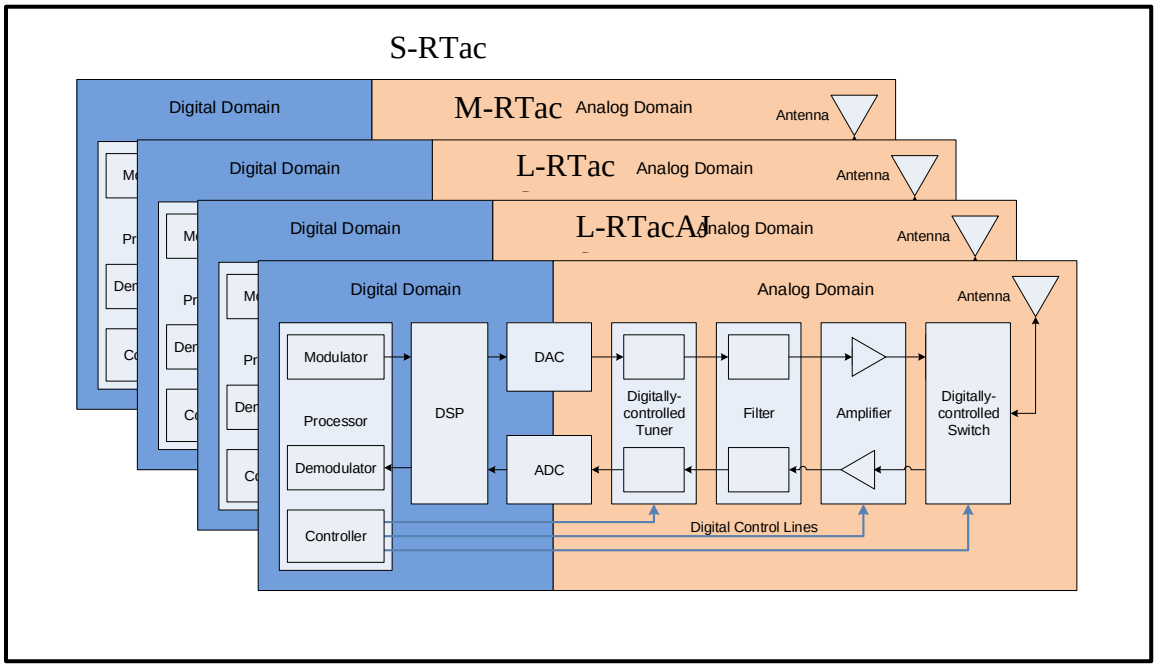


Figure 11. Current Architecture of Multiple SDR Systems

A. CURRENT ARCHITECTURE MODELS

The component power values assigned to the four different systems come from research of similar commercial systems, component specifications, and other power studies.

Table 2 describes the power models used for the power simulations of the four general military communication systems. The article by Baliga et al. (2011) provides general power values for various types of systems. The article by Thomas, McPherson, and Irvine (2016) provides the use of power modes in the model. The article by Arnold et

al. (2010) describes the effect of power efficiency in the models and provides amplifier power values. A personal interview with Manuel Uhm and Tim Fountain at the Wireless Innovation Forum, Oulu, Finland (2017) provides a SME verification and validation of the model.

Table 2. Current Architecture Models

Mode-Based Component Instantaneous Power															
Mode	Modulator (W)	Demodulator (W)	Controller (W)	DSP (W)	DAC (W)	ADC (W)	Tx Tuner (W)	Rx Tuner (W)	Tx Filter (W)	Rx Filter (W)	Tx Amp (W)	Rx Amp (W)	Switch (W)	Power Supply Efficiency	Total Power (W)
S-RTac															
Sleep	2.0	2.0	0.4	1.0	1.5	1.5	0.4	0.4	0.5	0.5	11.0	2.8	1.1	50%	50.1
Standby	2.0	2.0	0.4	1.0	1.5	1.5	0.4	0.4	0.5	0.5	11.0	2.8	1.0	50%	49.9
Transmit	15.0	2.0	0.5	1.0	1.5	1.5	0.4	0.4	0.5	0.5	11.0	2.8	1.0	50%	76.1
Receive	2.0	15.0	0.5	1.0	1.5	1.5	0.4	0.4	0.5	0.5	11.0	2.8	1.0	50%	76.1
M-RTac															
Sleep	0.2	0.2	0.2	0.3	0.2	0.2	0.1	0.1	0.3	0.3	44.0	11.0	0.5	50%	115.2
Standby	1.5	1.5	0.4	0.6	1.0	1.0	0.3	0.3	0.5	0.5	44.0	11.0	0.5	50%	126.2
Transmit	12.0	1.5	0.6	1.2	1.0	1.0	0.3	0.3	0.5	0.5	44.0	11.0	1.0	50%	149.8
Receive	1.5	12.0	0.6	1.2	1.0	1.0	0.3	0.3	0.5	0.5	44.0	11.0	1.0	50%	149.8
L-RTac															
Sleep	0.1	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.4	0.4	80.0	20.0	0.1	50%	203.6
Standby	0.5	0.5	0.3	1.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	0.5	50%	211.2
Transmit	30.0	0.5	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	273.6
Receive	0.5	30.0	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	273.6
L-RTacAJ															
Sleep	0.1	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.4	0.4	80.0	20.0	0.1	50%	203.6
Standby	0.5	0.5	0.3	1.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	0.5	50%	211.2
Transmit	30.0	0.5	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	273.6
Receive	0.5	60.0	0.5	4.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	337.6

Adapted from Arnold et al (2010), Baliga et al. (2011), Thomas, McPherson, and Irvine (2016), and Uhm and Fountain, personal communication, (2017).

The zero delta for power between sleep and standby modes in the S-RTac System indicates the absence of power management. The modulator and the demodulator in the S-RTac System, which usually run on processors, have some inherent power management mechanisms that result in some difference between the two higher and the two lower modes.

The gap between sleep and standby power modes in the M-RTac System is the result of power management. The amplifiers in the M-RTac System are more powerful for the increased range. The effect of newer technology in this system is more evident in the modulator and demodulators, which both run on processing hardware.

The amplifiers in the L-RTac System use more power to achieve the long range. The low sleep power is indicative of new technologies. This system also uses more power for modulation and demodulation for the increased complexity of the waveform.

The amplifiers in the L-RTacAJ use more power to achieve the long range. This system also uses more processing power on the demodulator for added anti-jam capability.

B. CURRENT ARCHITECTURE SIMULATIONS

This section provides the current architecture mathematical simulations of the S-RTac, M-RTac, L-RTac, and L-RTacAJ systems, which uses Equation 3. Table 3 shows the one-week simulation results for light usage, medium usage and heavy usage of the four general military communication systems.

Table 3. Current Architecture Average Power Consumption

Mode	Light Usage		Medium Usage		Heavy Usage	
	Duty Cycle	Weekly Power Consumption	Duty Cycle	Weekly Power Consumption	Duty Cycle	Weekly Power Consumption
S-RTac						
Sleep	10%	842 W-Hr	0%	W-Hr	0%	0 W-Hr
Standby	30%	2515 W-Hr	20%	1677 W-Hr	0%	0 W-Hr
Transmit	30%	3835 W-Hr	40%	5114 W-Hr	50%	6392 W-Hr
Receive	30%	3835 W-Hr	40%	5114 W-Hr	50%	6392 W-Hr
Total	100%	11028 W-Hr	100%	11904 W-Hr	100%	12785 W-Hr
M-RTac						
Sleep	10%	1935 W-Hr	0%	W-Hr	0%	0 W-Hr
Standby	30%	6360 W-Hr	20%	4240 W-Hr	0%	0 W-Hr
Transmit	30%	7550 W-Hr	40%	10067 W-Hr	50%	12583 W-Hr
Receive	30%	7550 W-Hr	40%	10067 W-Hr	50%	12583 W-Hr
Total	100%	23396 W-Hr	100%	24373 W-Hr	100%	25166 W-Hr
L-RTac						
Sleep	10%	3420 W-Hr	0%	W-Hr	0%	0 W-Hr
Standby	30%	10644 W-Hr	20%	7096 W-Hr	0%	0 W-Hr
Transmit	30%	13789 W-Hr	40%	18386 W-Hr	50%	22982 W-Hr
Receive	30%	13789 W-Hr	40%	18386 W-Hr	50%	22982 W-Hr
Total	100%	41644 W-Hr	100%	43868 W-Hr	100%	45965 W-Hr
L-RTacAJ						
Sleep	10%	3420 W-Hr	0%	0 W-Hr	0%	0 W-Hr
Standby	30%	10644 W-Hr	20%	7096 W-Hr	0%	0 W-Hr
Transmit	30%	13789 W-Hr	40%	18386 W-Hr	50%	22982 W-Hr
Receive	30%	17015 W-Hr	40%	22687 W-Hr	50%	28358 W-Hr
Total	100%	44869 W-Hr	100%	48169 W-Hr	100%	51341 W-Hr

C. CURRENT ARCHITECTURE ANALYSES

The analyses provides more details from the simulation. The analyses uses the average weekly power consumption of each component to show how each component contributed to the total weekly power consumption. The analyses also verifies the values of the total weekly power consumption by adding all the component weekly power consumption. Equation 4 shows the formula for computing the average weekly power consumption of each component.

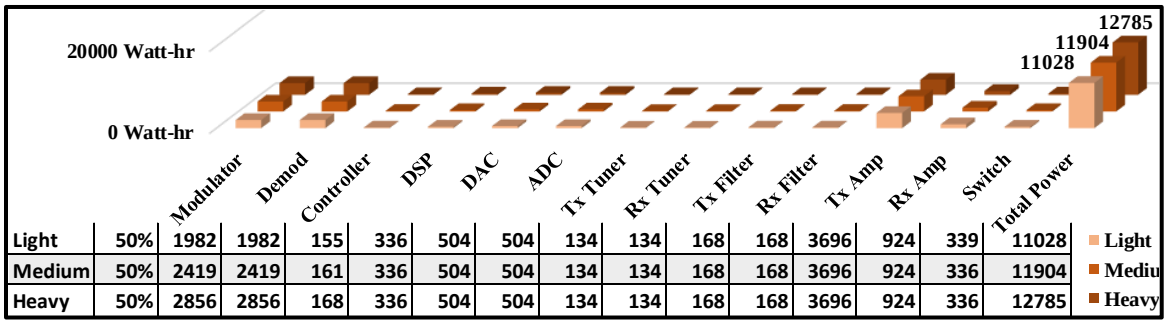
Equation 4. Average Weekly Component Consumption

$$AveWeeklyComponentPower\ (Watt\text{-}Hr) = (P_{SLEEP} * DC_{SLEEP} + P_{STDBY} * DC_{STDBY} + P_{TX} * DC_{TX} + P_{RX} * DC_{RX}) * Time / PwrSupEff$$

Where:

P_{SLEEP}	=	Instantaneous Sleep Power of a Component (Watts)
P_{STDBY}	=	Instantaneous Stand-by Power of a Component (Watts)
P_{TX}	=	Instantaneous Transmit Power of a Component (Watts)
P_{RX}	=	Instantaneous Receive Power of a Component (Watts)
Time	=	Hours in a Week (Hours)
PwrSupEff	=	Power Supply Efficiency (%)
DC_{SLEEP}	=	Duty Cycle for Sleep Mode (%)
DC_{STDBY}	=	Duty Cycle for Standby Mode (%)
DC_{TX}	=	Duty Cycle for Transmit Mode (%)
DC_{RX}	=	Duty Cycle for Receive Mode (%)

The analysis captured in Figure 12 verifies the weekly power consumption values calculated in the S-RTac simulation.

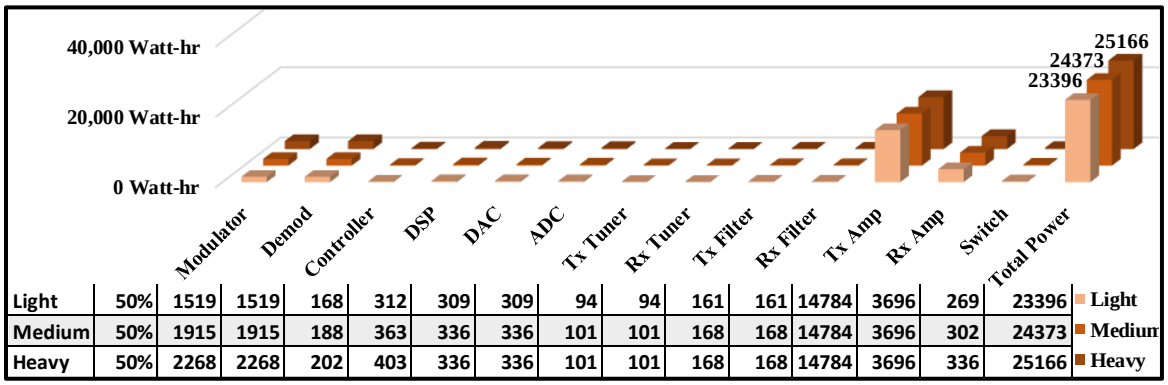


Light	50%	1982	1982	155	336	504	504	134	134	168	168	3696	924	339	11028	Light
Medium	50%	2419	2419	161	336	504	504	134	134	168	168	3696	924	336	11904	Mediu
Heavy	50%	2856	2856	168	336	504	504	134	134	168	168	3696	924	336	12785	Heavy

Figure 12. S-RTac Current Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 3696 Watt-Hours for light, medium and heavy usage. The next highest is the Modulator and the Demodulator, both at 1982 Watt-Hours for light usage, 2419 Watt-Hours for medium usage, and 2856 Watt-Hours for heavy usage. The total average weekly consumptions do not vary much across different usage—11028 Watt-Hours for light, 11904 Watt-Hours for medium, and 12785 Watt-Hours for heavy.

The analysis captured in Figure 13 verifies the weekly power consumption values calculated in the M-RTac simulation.

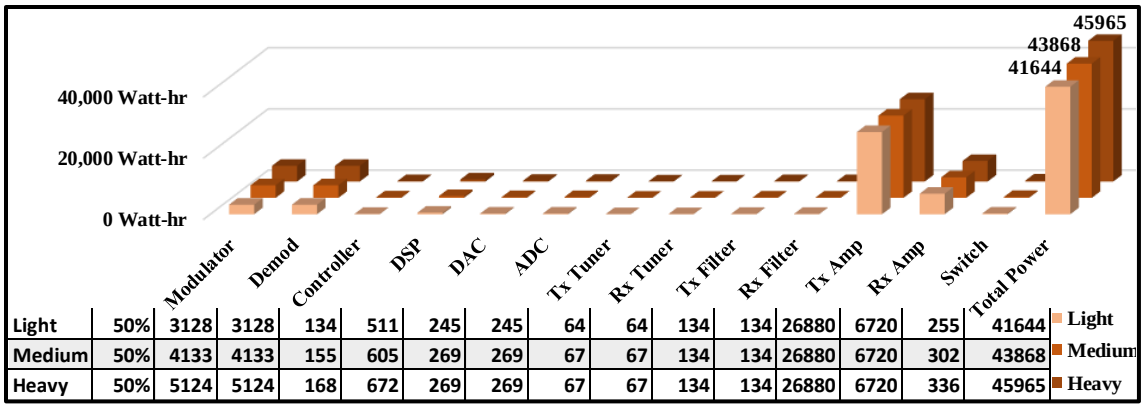


Light	50%	1519	1519	168	312	309	309	94	94	161	161	14784	3696	269	23396
Medium	50%	1915	1915	188	363	336	336	101	101	168	168	14784	3696	302	24373
Heavy	50%	2268	2268	202	403	336	336	101	101	168	168	14784	3696	336	25166

Figure 13. M-RTac Current Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 14784 Watt-Hours for light, medium and heavy usage. The second highest is the Receiver Amplifier at 3696 Watt-Hours for light, medium, and heavy usage. The third highest is the Modulator and the Demodulator, both at 1519 Watt-Hours for light usage, 1915 Watt-Hours for medium usage, and 2268 Watt-Hours for heavy usage. The total average weekly consumptions vary a little across different usage—23396 Watt-Hours for light, 24373 Watt-Hours for medium, and 25166 Watt-Hours for heavy.

The analysis captured in Figure 14 and Table 12 verifies the weekly power consumption values calculated in the L-RTac simulation.

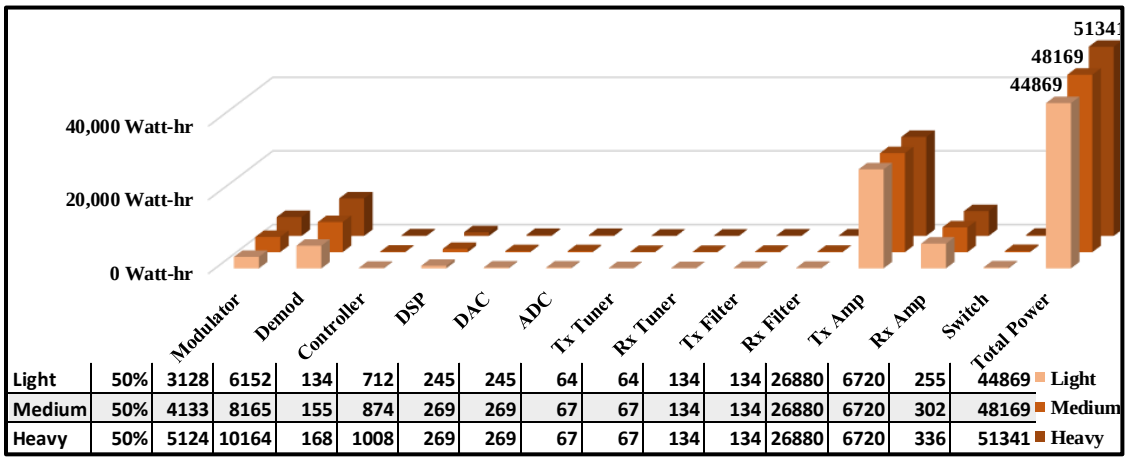


Light	50%	3128	3128	134	511	245	245	64	64	134	134	26880	6720	255	41644
Medium	50%	4133	4133	155	605	269	269	67	67	134	134	26880	6720	302	43868
Heavy	50%	5124	5124	168	672	269	269	67	67	134	134	26880	6720	336	45965

Figure 14. L-RTac Current Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 26880 Watt-Hours for light, medium, and heavy usage. The second highest is the Receiver Amplifier at 6720 Watt-Hours for light, medium, and heavy usage. The third highest is the Modulator and the Demodulator, both at 3128 Watt-Hours for light usage, 4133 Watt-Hours for medium usage, and 5124 Watt-Hours for heavy usage. The total average weekly consumptions vary significantly across different usage—41644 Watt-Hours for light, 43868 Watt-Hours for medium, and 45965 Watt-Hours for heavy.

The analysis captured in Figure 15 and Table 13 verifies the weekly power consumption values calculated in the L-RTacAJ simulation.



Light	50%	3128	6152	134	712	245	245	64	64	134	134	26880	6720	255	44869
Medium	50%	4133	8165	155	874	269	269	67	67	134	134	26880	6720	302	48169
Heavy	50%	5124	10164	168	1008	269	269	67	67	134	134	26880	6720	336	51341

Figure 15. L-RTacAJ Current Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 26880 Watt-Hours for light, medium, and heavy usage. The second highest is the Receiver Amplifier at 6720 Watt-Hours for light, medium, and heavy usage. The third highest, and now different consumption from the Modulator, is the Demodulator, at 6152 Watt-Hours for light usage, 8165 Watt-Hours for medium usage, and 10164 Watt-Hours for heavy usage. The total average weekly consumptions vary significantly across different usage—44869 for light, 48169 for medium, and 51341 for heavy.

V. EWC ARCHITECTURE

The EWC version of the Expeditionary C4 node utilizes enterprise-processing systems. Figure 16 is the EWC architecture of the four generalized types of communication systems in this thesis. The hardware architecture uses a RHM for each communication system. The four RHMs all connect to the enterprise for the modulation and the demodulation process. The enterprise side of the models uses switching power supplies—typical for enterprise systems with 77.5% efficiency. The RHM side of the models uses low-noise linear power supplies—typical for radio systems with 50% efficiency.

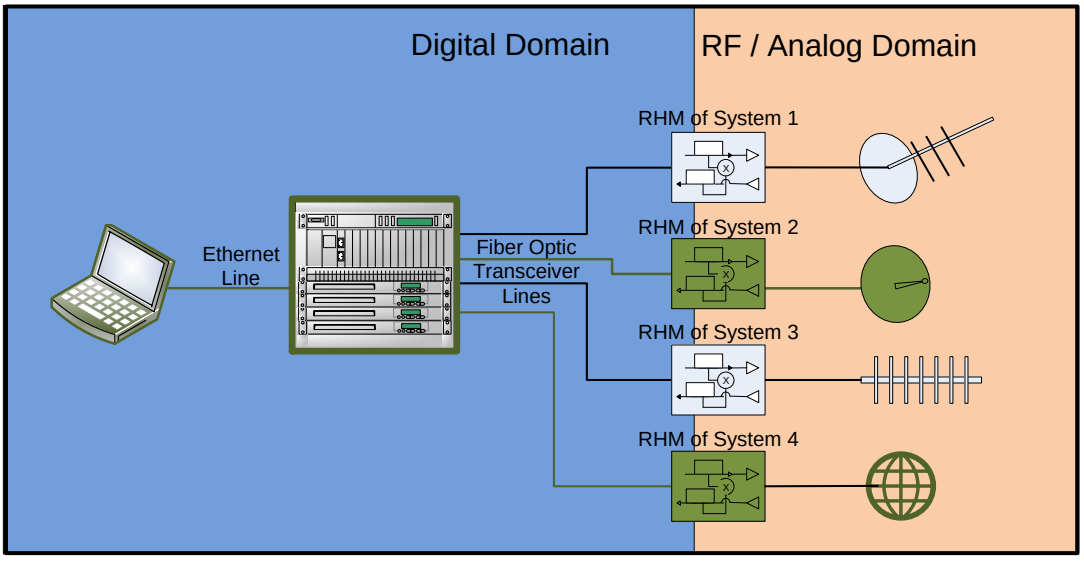


Figure 16. EWC Architecture of Multiple SDR Systems

A. EWC ARCHITECTURE MODELS

The EWC architecture system model and description uses the same values from the original current architecture model when applicable. The original current architecture separated into two sections—the RHM in dark blue, and the Enterprise in orange.

Table 4 describes the power model for the power simulation of the four general military communication systems.

Table 4. EWC Architecture Power Models

Mode-Based Component Instantaneous Power																			
Mode	Enterprise				Radio Head Module (RHM)														Total Power (W)
	Modulator (W)	Demodulator (W)	Power Supply Efficiency (%)	Sub-Total Power (W)	High-speed Serial (W)	Controller (W)	DSP (W)	DAC (W)	ADC (W)	Tx Tuner (W)	Rx Tuner (W)	Tx Filter (W)	Rx Filter (W)	Tx Amp (W)	Rx Amp (W)	Switch (W)	Power Supply Efficiency	Sub-Total Power (W)	
S-RTac																			
Sleep	0.1	0.1	78%	0.3	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.4	0.4	10.0	2.5	0.1	50%	28.2	28.5
Standby	0.5	0.5	78%	1.3	0.2	0.3	0.5	0.8	0.8	0.2	0.2	0.4	0.4	11.0	2.8	0.5	50%	36.1	37.4
Transmit	10.0	0.5	78%	13.5	0.4	0.5	1.0	0.8	0.8	0.2	0.2	0.4	0.4	11.0	2.8	1.0	50%	38.9	52.4
Receive	0.5	10.0	78%	13.5	0.4	0.5	1.0	0.8	0.8	0.2	0.2	0.4	0.4	11.0	2.8	1.0	50%	38.9	52.4
M-RTac																			
Sleep	0.1	0.1	78%	0.26	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.4	0.4	40.0	10.0	0.1	50%	103	103.5
Standby	0.5	0.5	78%	1.29	0.2	0.3	0.5	0.8	0.8	0.2	0.2	0.4	0.4	40.0	10.0	0.5	50%	109	109.9
Transmit	10.0	0.5	78%	13.55	0.4	0.5	1.0	0.8	0.8	0.2	0.2	0.4	0.4	40.0	10.0	1.0	50%	111	124.9
Receive	0.5	10.0	78%	13.55	0.4	0.5	1.0	0.8	0.8	0.2	0.2	0.4	0.4	40.0	10.0	1.0	50%	111	124.9
L-RTac																			
Sleep	0.1	0.1	78%	0.26	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.4	0.4	80.0	20.0	0.1	50%	203	203.7
Standby	0.5	0.5	78%	1.29	0.2	0.3	1.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	0.5	50%	210	210.9
Transmit	30.0	0.5	78%	39.35	0.4	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	213	252.8
Receive	0.5	30.0	78%	39.35	0.4	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	213	252.8
L-RTacAJ																			
Sleep	0.1	0.1	78%	0.3	0.1	0.1	0.2	0.1	0.1	0.1	0.1	0.4	0.4	80.0	20.0	0.1	50%	203	203.7
Standby	0.5	0.5	78%	1.3	0.2	0.3	1.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	0.5	50%	210	210.9
Transmit	30.0	0.5	78%	39.4	0.4	0.5	2.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	213	252.8
Receive	0.5	60.0	78%	78.1	0.4	0.5	4.0	0.8	0.8	0.2	0.2	0.4	0.4	80.0	20.0	1.0	50%	217	295.5

The instantaneous power consumption of components across different modes in the EWC version of the S-RTac System are lower than the current architecture version of the S-RTac System due to the old technology and the absence of power management in the original S-RTac System.

The instantaneous power consumption of components in the EWC version of the M-RTac System are moderately lower than the current architecture version of the M-RTac System due to the relatively newer technology represented in the current architecture.

The standby instantaneous power consumptions of components in the EWC version of the L-RTac System are equal to the current architecture version of the L-RTac System due to the new technology represented in the current architecture.

The instantaneous power consumptions of components in the EWC version of the L-RTacAJ System are equal to the current architecture version of the L-RTacAJ System due to the new technology already in the current architecture version.

B. EWC ARCHITECTURE SIMULATIONS

This section provides the enterprise architecture mathematical simulations of the S-RTac, M-RTac, L-RTac, and L-RTacAJ systems. The simulations use Equation 3. Table 5 shows the simulation results for one-week light usage, medium usage, and heavy usage of the four general military communication systems in the EWC architecture.

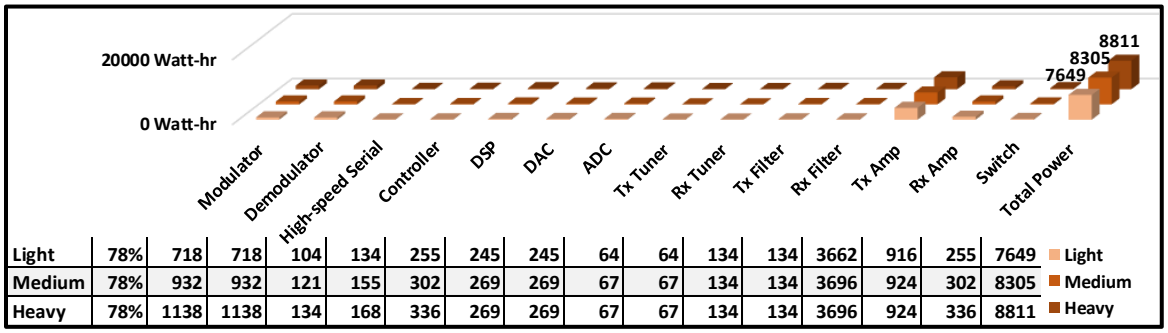
Table 5. EWC Architecture Average Power Consumption

Mode	Light Usage		Medium Usage		Heavy Usage	
	Duty Cycle	Weekly Power Consumption	Duty Cycle	Weekly Power Consumption	Duty Cycle	Weekly Power Consumption
S-RTac						
Sleep	10%	478 W-Hr	0%	0 W-Hr	0%	0 W-Hr
Standby	30%	1884 W-Hr	20%	1256 W-Hr	0%	0 W-Hr
Transmit	30%	2643 W-Hr	40%	3525 W-Hr	50%	4406 W-Hr
Receive	30%	2643 W-Hr	40%	3525 W-Hr	50%	4406 W-Hr
Total	100%	7649 W-Hr	100%	8305 W-Hr	100%	8811 W-Hr
M-RTac						
Sleep	10%	1738 W-Hr	0%	0 W-Hr	0%	0 W-Hr
Standby	30%	5538 W-Hr	20%	3692 W-Hr	0%	0 W-Hr
Transmit	30%	6297 W-Hr	40%	8397 W-Hr	50%	10496 W-Hr
Receive	30%	6297 W-Hr	40%	8397 W-Hr	50%	10496 W-Hr
Total	100%	19871 W-Hr	100%	20485 W-Hr	100%	20991 W-Hr
L-RTac						
Sleep	10%	3421 W-Hr	0%	0 W-Hr	0%	0 W-Hr
Standby	30%	10629 W-Hr	20%	7086 W-Hr	0%	0 W-Hr
Transmit	30%	12739 W-Hr	40%	16985 W-Hr	50%	21231 W-Hr
Receive	30%	12739 W-Hr	40%	16985 W-Hr	50%	21231 W-Hr
Total	100%	39528 W-Hr	100%	41056 W-Hr	100%	42463 W-Hr
L-RTacAJ						
Sleep	10%	3421.46	0%	0.00	0%	0.00
Standby	30%	10628.87	20%	7085.91	0%	0.00
Transmit	30%	12738.84	40%	16985.13	50%	21231.41
Receive	30%	14891.41	40%	19855.22	50%	24819.02
Total	100%	41680.58	100%	43926.26	100%	46050.43

C. EWC ARCHITECTURE ANALYSES

Similar to the Current architecture Simulation Analyses, the EWC architecture simulation analyses provides more details from the simulation by calculating the average weekly power consumption of each component in the EWC architecture. The analyses also verifies the values of the total weekly power consumption by adding all the component weekly power consumption. Each component's contribution to the total weekly power consumption also provides a method to compare the differences in power consumption of each component in Current and EWC architectures.

The analysis captured in Figure 17 verifies the average weekly power consumption from the S-RTac EWC architecture simulation.

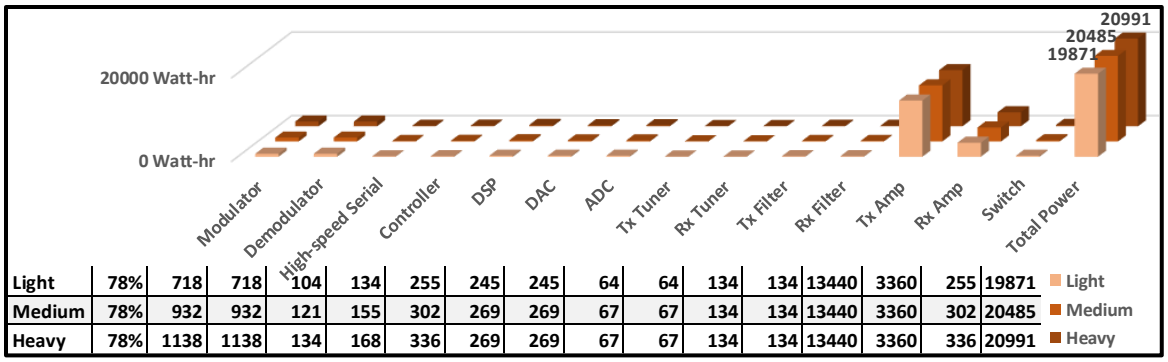


Light	78%	718	718	104	134	255	245	245	64	64	134	134	3662	916	255	7649
Medium	78%	932	932	121	155	302	269	269	67	67	134	134	3696	924	302	8305
Heavy	78%	1138	1138	134	168	336	269	269	67	67	134	134	3696	924	336	8811

Figure 17. S-RTac EWC Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 3662 Watt-Hours for light usage, and 3696 for both medium and heavy usage. The next highest are the Modulator, Demodulator, and Receiver Amplifier. The Modulator and Demodulator values are both at 718 Watt-Hours for light usage, 932 Watt-Hours for medium usage, and 1138 Watt-Hours for heavy usage. The Receiver Amplifier is at 916 Watt-Hours for light usage, and 924 for both medium and heavy usage. The total average weekly consumptions do not vary much across different usage—7649 Watt-Hours for light usage, 8305 Watt-Hours for medium usage, and 8811 Watt-Hours for heavy usage.

The analysis captured in Figure 18 verifies the average weekly power consumption from the M-RTac EWC architecture simulation.

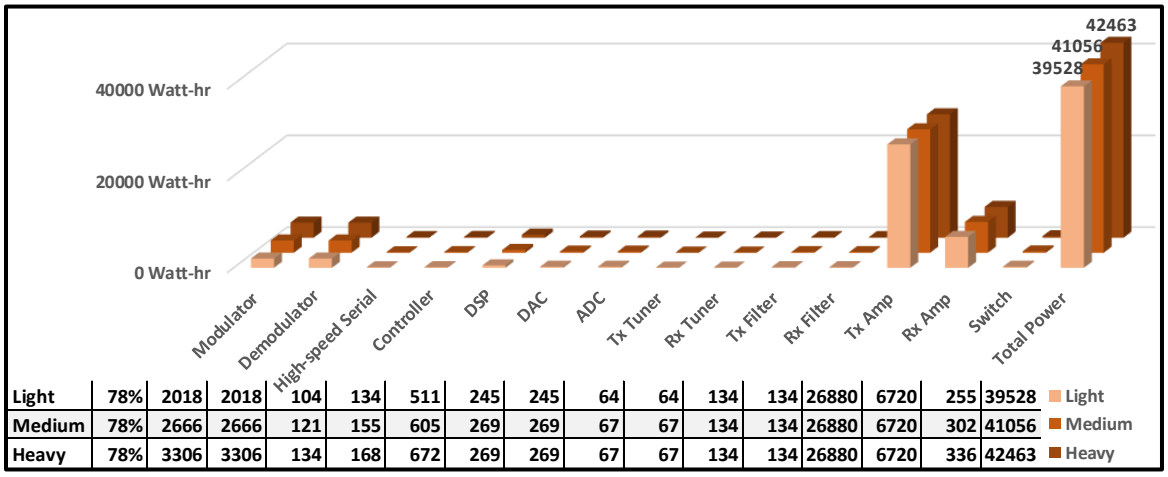


Light	78%	718	718	104	134	255	245	245	64	64	134	134	13440	3360	255	19871	Light
Medium	78%	932	932	121	155	302	269	269	67	67	134	134	13440	3360	302	20485	Medium
Heavy	78%	1138	1138	134	168	336	269	269	67	67	134	134	13440	3360	336	20991	Heavy

Figure 18. M-RTac EWC Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 13440 Watt-Hours for light, medium, and heavy usage. The second highest is the Receiver Amplifier at 3360 Watt-Hours for light, medium, and heavy usage. The third highest are the Modulator and the Demodulator, both at 718 Watt-Hours for light usage, 932 Watt-Hours for medium usage, and 1138 Watt-Hours for heavy usage. The total average weekly consumptions vary a little across different usage—19871 Watt-Hours for light usage, 20485 Watt-Hours for medium usage, and 20991 Watt-Hours for heavy usage.

The analysis captured in Figure 19 verifies the average weekly power consumption from the L-RTac EWC architecture simulation.

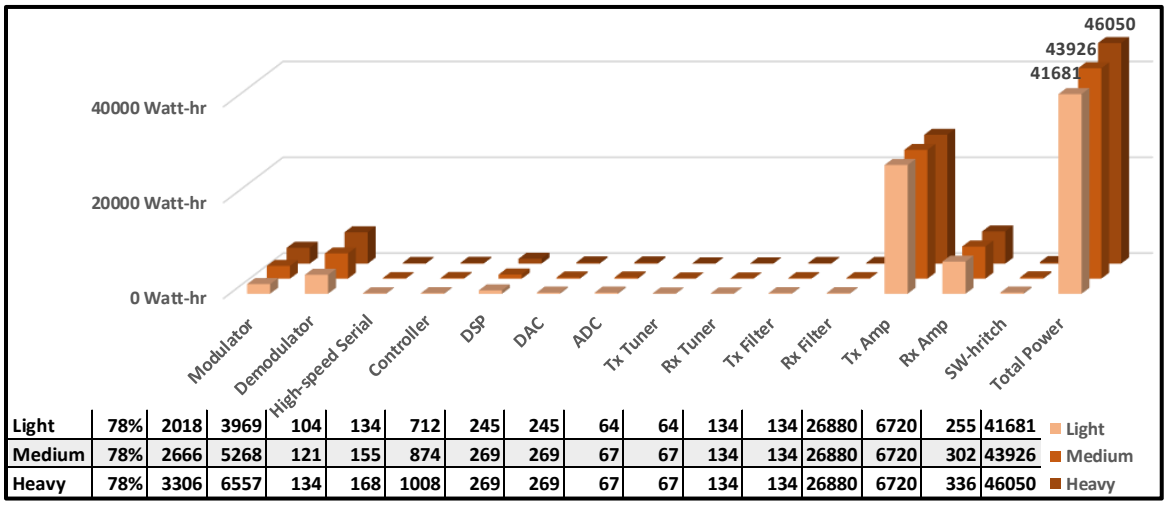


Light	78%	2018	2018	104	134	511	245	245	64	64	134	134	26880	6720	255	39528	Light
Medium	78%	2666	2666	121	155	605	269	269	67	67	134	134	26880	6720	302	41056	Medium
Heavy	78%	3306	3306	134	168	672	269	269	67	67	134	134	26880	6720	336	42463	Heavy

Figure 19. L-RTac EWC Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 26880 Watt-Hours for light, medium, heavy usage. The second highest is the Receiver Amplifier at 6720 Watt-Hours for light, medium, and heavy usage. The third highest are the Modulator and the Demodulator, both at 2018 Watt-Hours for light usage, 2666 Watt-Hours for medium usage, and 3306 Watt-Hours for heavy usage. The total average weekly consumptions vary significantly across different usage—39528 Watt-Hours for light usage, 41056 Watt-Hours for medium usage, and 42463Watt-Hours for heavy usage.

The analysis captured in Figure 20 verifies the average weekly power consumption from the L-RTacAJ EWC architecture simulation.



Light	78%	2018	3969	104	134	712	245	245	64	64	134	134	26880	6720	255	41681
Medium	78%	2666	5268	121	155	874	269	269	67	67	134	134	26880	6720	302	43926
Heavy	78%	3306	6557	134	168	1008	269	269	67	67	134	134	26880	6720	336	46050

Figure 20. L-RTacAJ EWC Architecture Component Power Simulation

The Transmitter Amplifier consumes the highest weekly power, at 26880 Watt-Hours for light, medium, and heavy usage. The second highest is the Receiver Amplifier at 6720 Watt-Hours for light, medium, and heavy usage. The third highest is the Demodulator, at 3969 Watt-Hours for light usage, 5268 Watt-Hours for medium usage, and 6557 Watt-Hours for heavy usage. The total average weekly consumptions vary significantly across different usage—41681 Watt-Hours for light usage, 43926 Watt-Hours for medium usage, and 46050 Watt-Hours for heavy usage.

VI. COMPARATIVE ANALYSES

The comparative analyses of both current architecture and EWC architecture simulations expose the power consumption improvements from the EWC architecture. The comparisons use the formulas in Equation 5 and Equation 6 to calculate percent improvement of operational duration and the percent reduction of energy use.

Equation 5 is the formula for calculating the improvement in operational duration for the performance comparisons.

Equation 5. Operational Duration Improvement

$$\text{OperationalDurationImprovemt (\%)} = (AveWeeklyPower_{CA} / AveWeeklyPower_{EA}) - 1$$

Where:

$AveWeeklyPower_{CA}$ = Average Weekly Power Consumption of Current Architecture (Watt-Hr)

$AveWeeklyPower_{EA}$ = Average Weekly Power Consumption of EWC Architecture (Watt-Hr)

Equation 6 is the formula for calculating the improvement in energy reduction for the performance comparisons.

Equation 6. Energy Reduction Improvement

$$\text{EnergyRedImprovemt (\%)} = (AveWeeklyPower_{CA} - AveWeeklyPower_{EA}) / AveWeeklyPower_{CA}$$

Where:

$AveWeeklyPower_{CA}$ = Average Weekly Power Consumption of Current Architecture (Watt-Hr)

$AveWeeklyPower_{EA}$ = Average Weekly Power Consumption of EWC Architecture (Watt-Hr)

A. SYSTEM COMPARISONS

System comparisons show the performance improvements of every system in each usage condition. Improvements vary differently for every system and for different usage conditions. The values calculated in this comparison indicate a substantial power consumption improvement from the EWC architecture. Table 6 shows the improvements in Operational Duration and Energy Reduction from implementing the four general military communications systems in the EWC architecture.

Table 6. Current versus EWC Architecture Performance Comparison

Usage	Weekly CA Consumption	Weekly EA Consumption	Duration Improvement	Energy Reduction	Energy Reduction
S-RTac					
Light	11028	7649	44%	3378	31%
Medium	11904	8305	43%	3599	30%
Heavy	12785	8811	45%	3973	31%
M-RTac					
Light	23396	19871	18%	3524	15%
Medium	24373	20485	19%	3888	16%
Heavy	25166	20991	20%	4175	17%
L-RTac					
Light	41644	39528	5%	2116	5%
Medium	43868	41056	7%	2812	6%
Heavy	45965	42463	8%	3502	8%
L-RTacAJ					
Light	44869	41681	8%	3189	7%
Medium	48169	43926	10%	4243	9%
Heavy	51341	46050	11%	5290	10%

Figure 21 illustrates that a 43% Operational Duration improvement in the S-RTac System increases operating time up to 10 weeks with the same amount of energy resource that only allows 7 weeks duration in the current architecture. Figure 22 illustrates that a 30% Energy Reduction in the S-RTac System allows 30% less energy for the same operational duration.

The percent energy reduction is higher in the S-RTac System than others are because this thesis uses old technology to represent the current architecture, and new technology to represent the EWC architecture. Most S-RTac current architecture systems

are older and an S-RTac EWC architecture system is still only a concept. A separate model and simulation using new technology for both current architecture and EWC architecture results in energy reduction around 10%.

Figure 21 illustrates that a 20% Operational Duration improvement in the M-RTac System increases operating time up to six weeks with the same amount of energy resource that only allows five weeks duration in the current architecture. Figure 22 illustrates that a 15% Energy Reduction in the M-RTac System allows 15% less energy for the same operational duration.

The percent energy reduction in the M-RTac System is moderately higher than others are because this thesis uses relatively newer technology to represent the current architecture, and new technology to represent the EWC architecture. Most M-RTac current architecture systems are moderately newer and an M-RTac EWC architecture system is still only a concept. A separate model and simulation using new technology for both current architecture and EWC architecture results in energy reduction around 5%. The transmitter (Tx) and receiver (Rx) power consumptions do not benefit from the EWC architecture, and only improves when the technology improves.

Figure 21 illustrates that a 7% Operational Duration improvement in the L-RTac System increases operating time up to 15 weeks with the same amount of energy resource that only allows 14 weeks duration in the current architecture. Figure 22 illustrates that a 6% Energy Reduction in the L-RTac System allows 6% less energy for the same operational duration.

Both current architecture and EWC architecture versions of the L-RTac use new technology, reflecting power consumption improvements solely from the architectural change to EWC architecture. The only component power consumptions affected by the architectural change are the power consumptions of the modulator and demodulator.

Figure 21 illustrates that a 10% Operational Duration improvement in the L-RTacAJ System increases operating time up to 11 weeks with the same amount of energy resource that only allows 10 weeks duration in the current architecture. Figure 22

illustrates that a 9% Energy Reduction in the L-RTacAJ System allows 9% less energy for the same operational duration.

Both current architecture and EWC architecture versions of the L-RTacAJ use new technology, reflecting power consumption improvements solely from the change to EWC architecture. The Modulator and Demodulator power consumptions, which use more power for the AJ capability of the waveform, are the only power consumption contributions affected by the change to EWC architecture.

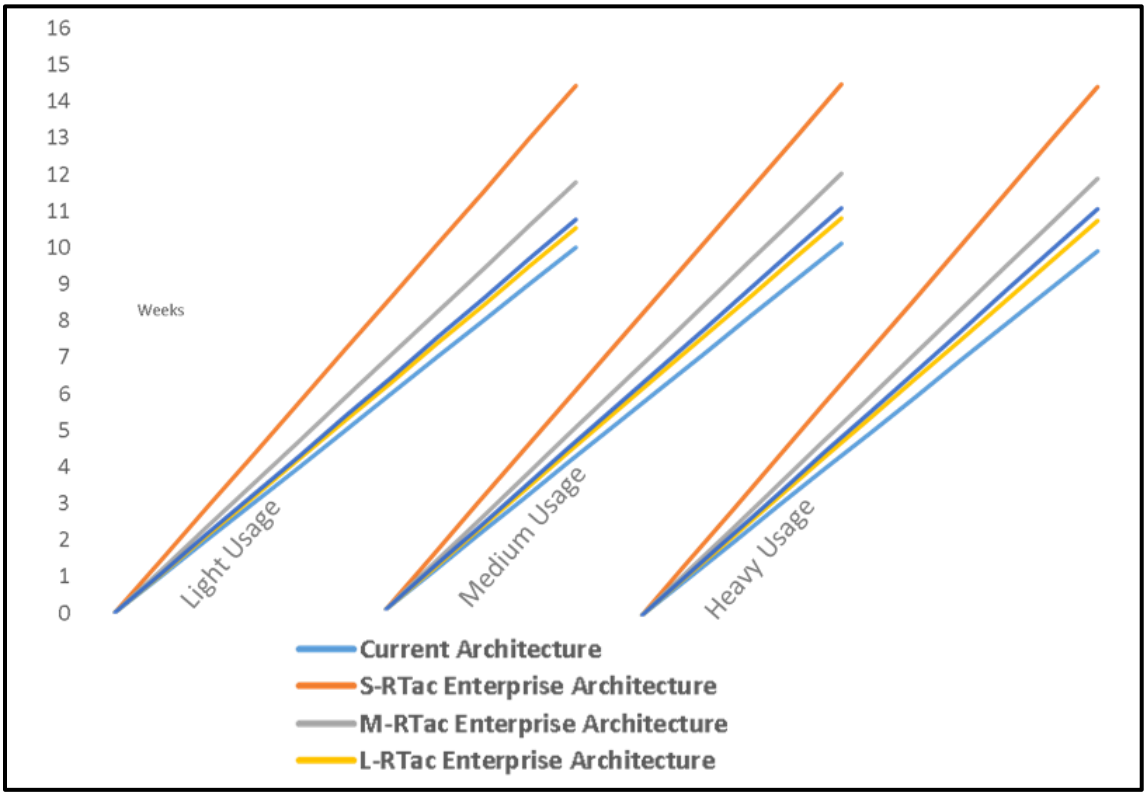


Figure 21. Duration Comparison For Equal Energy Consumption

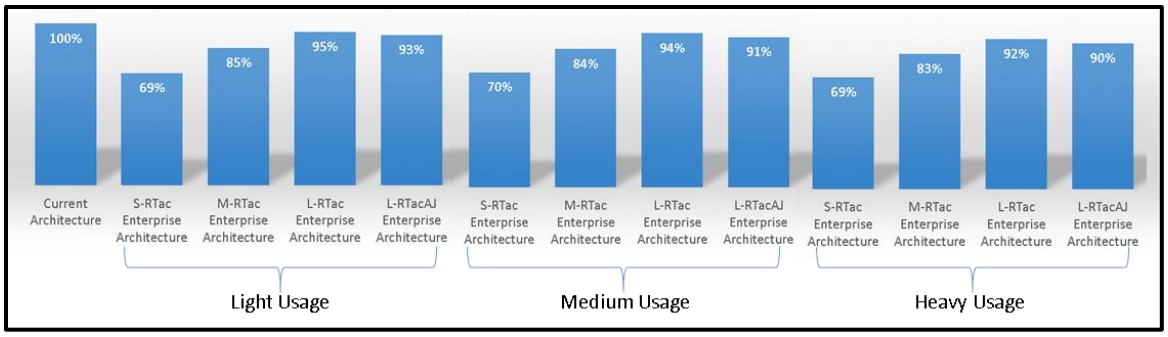


Figure 22. Consumption Comparison

B. COMBINED SYSTEM COMPARISONS

This comparison sums all the different weekly consumptions from each system to derive the overall comparison values.

Table 7 shows the improvements in Operational Duration and Energy Reduction from implementing S-RTac, M-RTac, L-RTac, and L-RTacAJ Systems in the EWC architecture. Figure 23 illustrates that a 10% Operational Duration improvement increases operating time up to 11 weeks with the same amount of energy resource that only allows 10 weeks duration in the current architecture. Figure 24 illustrates that a 10% Energy Reduction allows 10% less energy for the same operational duration.

Table 7. Combined Current versus EWC Architecture Performance Comparison

Usage	Weekly CA Consumption (W-Hr)	Weekly EA Consumption (W-Hr)	Duration Improvement (%)	Energy Reduction Delta (W-Hr)	Energy Reduction (%)
Light	120936	108729	11%	12207	10%
Medium	128315	113773	13%	14542	11%
Heavy	135257	118316	14%	16941	13%

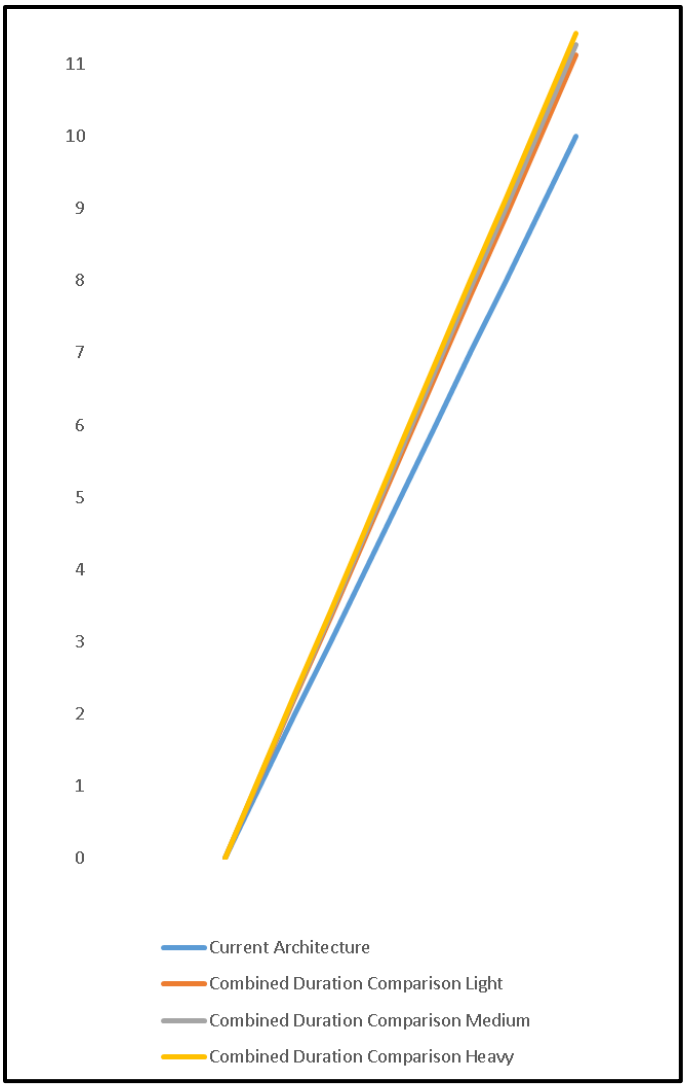


Figure 23. Combined Duration Comparison For Equal Energy Consumption

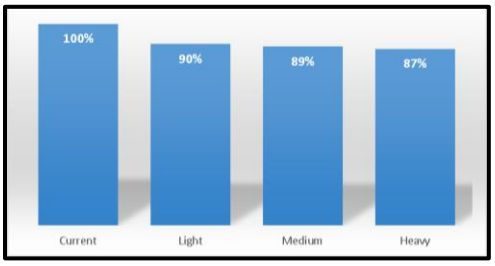


Figure 24. Combined Consumption Comparison

VII. CONCLUSION AND RECOMMENDATIONS

The straightforward power analyses through mathematical modelling and simulation is sufficient to conclude that the EWC architecture concept reduced significant power consumption in an Expeditionary C4 Node. This thesis achieved its objective without analyzing additional power savings mechanisms in enterprise processing. In general, the underutilization of processing reduces efficiency (Baliga et al. 2011). However, the model for processor utilization maximization becomes exponentially more complicated due to the randomness of waveform processing occurrence. Additionally, waveform-specific processing specifications, in instructions per second (IPS), are unobtainable and would vary for different types of processors, making it necessary to test actual hardware and implement actual waveforms in software. The concise analyses resulted in easily understandable explanations of the power reductions achieved in the EWC architecture.

The EWC architecture concept is already a reality in the commercial world. The cellular industry is driving future efficiency enhancements of Radio Head Modules, which include efficient technologies in power supplies, Tx amplifiers, and Rx amplifiers. The push for efficiency in the enterprise computing industry is already in crescendo. The enterprise computing industry's knows that its primary bottleneck is power consumption (Arnold et al. 2010).

A follow-on proof-of-concept effort is necessary to prove the concept in actual hardware. The omission of additional power savings from the model created a substantial margin for error, which should ensure the reliability of the comparative analyses. However, the data generated by the models are still only relative values. Actual hardware implementation will provide absolute data and will determine the added power savings from enterprise processing. Real systems would also demonstrate possible emergent capabilities in Network Management, Dynamic Spectrum Allocation, Coalition Interoperability, and Electronic Warfare (EW).

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