



AFRL-RY-WP-TR-2017-0144

**MULTI-BEAM RADIO FREQUENCY (RF) APERTURE
ARRAYS USING MULTIPLIERLESS APPROXIMATE
FAST FOURIER TRANSFORM (FFT)**

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AUGUST 2017

Final Report

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REPORT DOCUMENTATION PAGE					Form Approved OMB No. 0704-0188				
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1. REPORT DATE (DD-MM-YY) August 2017		2. REPORT TYPE Final		3. DATES COVERED (From - To) 17 March 2016 – 17 March 2017					
4. TITLE AND SUBTITLE MULTI-BEAM RADIO FREQUENCY (RF) APERTURE ARRAYS USING MULTIPLIERLESS APPROXIMATE FAST FOURIER TRANSFORM (FFT)				5a. CONTRACT NUMBER FA8650-16-1-7610					
				5b. GRANT NUMBER					
				5c. PROGRAM ELEMENT NUMBER 61101E					
6. AUTHOR(S) Dr. Arjuna Madanayake, Viduneth Ariyaratna, and Jajath Akram (University of Akron) Dr. Renato J. Cintra and Diego Coelho (Federal University of Pernambuco)				5d. PROJECT NUMBER 1000					
				5e. TASK NUMBER N/A					
				5f. WORK UNIT NUMBER Y1FC					
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border-right: 1px solid black; padding: 5px;">University of Akron 302 E. Buchtel Avenue Akron, OH 44325-3904</td> <td style="padding: 5px;">Federal University of Pernambuco Recife, PE, Brazil</td> </tr> </table>				University of Akron 302 E. Buchtel Avenue Akron, OH 44325-3904	Federal University of Pernambuco Recife, PE, Brazil	8. PERFORMING ORGANIZATION REPORT NUMBER			
University of Akron 302 E. Buchtel Avenue Akron, OH 44325-3904	Federal University of Pernambuco Recife, PE, Brazil								
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border-right: 1px solid black; padding: 5px;">Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Force</td> <td style="padding: 5px;">Defense Advanced Research Projects Agency DARPA/MTO 675 North Randolph Street Arlington, VA 22203</td> </tr> </table>				Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Force	Defense Advanced Research Projects Agency DARPA/MTO 675 North Randolph Street Arlington, VA 22203	10. SPONSORING/MONITORING AGENCY ACRONYM(S) AFRL/RYP			
				Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Force	Defense Advanced Research Projects Agency DARPA/MTO 675 North Randolph Street Arlington, VA 22203				
11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S) AFRL-RY-WP-TR-2017-0144									
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.									
13. SUPPLEMENTARY NOTES This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with SAF/AQR memorandum dated 10 Dec 08 and AFRL/CA policy clarification memorandum dated 16 Jan 09. This material is based on research sponsored by Air Force Research laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) under agreement number FA8650-16-1-7610. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation herein. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies of endorsements, either expressed or implied, of Air Force Research Laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) or the U.S. Government. Report contains color.									
14. ABSTRACT Fast Fourier transforms (FFTs) are <i>fast algorithms</i> for the computation of the discrete Fourier transform (DFT) with low computational complexity. FFT owes its popularity to the fact that the parent algorithm – the DFT – is of critical importance in a wide range of applications, such as wireless communications, data networks, sensor networks, cognitive radio, radar and beamforming, imaging, filtering, correlation and radio-astronomy. In this report approximate transforms that closely follow the DFT have been studied and found. The approximate-DFT (a-DFT) transforms are derived to have acceptable performance in terms of achieving spatial multi-beams.									
15. SUBJECT TERMS aperture arrays, fast Fourier transform, discrete Fourier transform, digital array processing, antenna beamformers									
16. SECURITY CLASSIFICATION OF: <table style="width: 100%; border: none;"> <tr> <td style="width: 33%; border-right: 1px solid black; padding: 5px;">a. REPORT Unclassified</td> <td style="width: 33%; border-right: 1px solid black; padding: 5px;">b. ABSTRACT Unclassified</td> <td style="padding: 5px;">c. THIS PAGE Unclassified</td> </tr> </table>			a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified	17. LIMITATION OF ABSTRACT: SAR		18. NUMBER OF PAGES 160	
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified							
19a. NAME OF RESPONSIBLE PERSON (Monitor) Stephen L. Hary 19b. TELEPHONE NUMBER (Include Area Code) N/A									

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1. EXECUTIVE SUMMARY

Approximate transforms that closely follow the discrete Fourier transform (DFT) have been studied and found. The approximate-DFT (a-DFT) transforms are derived to have acceptable performance in terms of achieving spatial multi-beams. It has been found that a-DFTs achieve almost DFT performance albeit at a multiplier count of zero. Therefore the transforms reduce the well-known $O(N\log N)$ multiplier complexity of fast Fourier transform (FFT) algorithms to zero for a N -point transform. Sparse factorization for each derived matrix has also been computed to reduce the adder complexity involved.

Approximate transforms for 8-, 16-, 32-, and 64-point transforms have been found which have zero multiplier complexity. Frequency response analysis have been given for each case depicting the error performance.

A 2.4 GHz, 16-element receive-mode multi-beamforming system has been implemented in lab for verifying the performance of the beams generated by the approximate transforms for 8- and 16-point transforms. Beam measurements have been obtained and are reported for the 8- and 16-point cases. Beam patterns pertaining to the respective exact transform have also been measured for comparison purpose. It has been verified that the beam patterns corresponding to a-DFT transforms closely follow the beams obtained for the respective exact version.

1.1 List of Contributors

Dr. Arjuna Madanayake (University of Akron, Principal Investigator (PI)), Dr. Renato J. Cintra (Federal University of Pernambuco, collaborator), Viduneth Ariyaratna (University of Akron, Research Assistant (RA)), Najath Akram (University of Akron, RA), Diego Coelho (Federal University of Pernambuco, RA), Sravan Pulipati (University of Akron, RA-experimental setup).

1.2 Acknowledgments

The PI Arjuna Madanayake and collaborator Renato Cintra gratefully acknowledge Dr. Ken Plaks at the Defense Advanced Research Projects Agency (DARPA) and Dr. Stephen Hary at the Air Force Research Laboratory (AFRL) for their support.

2. INTRODUCTION

FFTs are *fast algorithms* for the computation of the DFT with low computational complexity. FFT is a famous algorithm in digital signal processing (DSP). FFT owes its popularity to the fact that the parent algorithm – the DFT – is of critical importance in a wide range of applications [1], such as wireless communications, data networks, sensor networks, cognitive radio, radar and beamforming, imaging, filtering, correlation and radio-astronomy. FFTs efficiently compute an N -point DFT, where the DFT itself is an $N \times N$ linear transform that splits N -samples of a signal to its constituent frequency components.

The FFT is widely used in a massive collection of applications realized using embedded systems based on fixed-point digital arithmetic (for example, two's complement number system). The FFT is an important algorithm for communications, radar and sensor systems. The FFT transforms perfectly in theory within these systems in an ideal world. The exact FFT is never realized because digital architectures are subject to fixed-point eff such as quantization, rounding, saturation and truncation. Nonetheless, FFTs are a component of a lossy scheme as a result of practical hardware implementation. Multi-beamforming is achieved in today's systems using FFT algorithms to perform the DFT operation. Fast Fourier transform is used for the computation of the DFT with low computational complexity. Computational complexity associated with performing an N -point DFT operation is $O(N^2)$. FFT reduces the above computational complexity to $O(N \log_2 N)$. Cooley-Tuckey, Duhamel and Winograd are some popular FFT algorithms that can be found in the literature [1-3]. Table 1 tabulates the associated complexities of those popular DFT algorithms for 8-point and 16-point transforms.

Table 1. Arithmetic Complexity Comparison

A-DFT	Algorithm	Complex Adders	Complex Multipliers	Real Adders	Real Multipliers	Lower Bound Heidermann
8-point	Radix-8	24	2	58	6	4
	Cooley-Tukey Radix-2	24	5	73	15	4
	Winograd (8-point)	26	2	62	6	4
16-point	Radix-2	64	17	213	51	20
	Radix-4	64	10	178	30	20
	Split-Radix	64	10	178	30	20
	Winograd (16-point)	74	10	198	30	20

2.1 DFT-based Multi-beams

One of the most important applications of the FFT in military systems would be the realization of radio frequency (RF) antenna array processing systems for electronically-steerable multi-beam transmit and receive aperture arrays. Such multi-beam antennas are extremely important for RF sensing, communications, and radar systems, such as active electronically scanned array (AESA) radars and digital array radar (DAR). The application of an N -point FFT along the array samples, at each time frame, for a uniform linear array (ULA) of antenna elements (see Figure 1) yields N number of simultaneous RF beams. Using available FFT algorithms, the computational complexity (complex-multiplier and complex-adder complexity) for an N -point ULA is

$O(N \log_2 N)$. For rectangular apertures of size $N \times N$ antennas, the application of an N point 2-D FFT, at each time sample, spatially across the aperture yields N^2 independent RF beams (see Figure 2). In such a system, a 2-D DFT is computed on the rectangular/square array by computing N 1-D N -point DFTs along rows, then finding another N 1-D DFTs along columns, taking the outputs of the row-wise DFTs as the inputs to the column-wise transforms. In terms of N -point DFT cores, we need $2N$ N -point cores to compute a single $N \times N$ 2-D transform. The hardware complexity associated with achieving such N^2 beams for an $N \times N$ rectangular aperture is $O(N^2 \log_2 N^2)$.

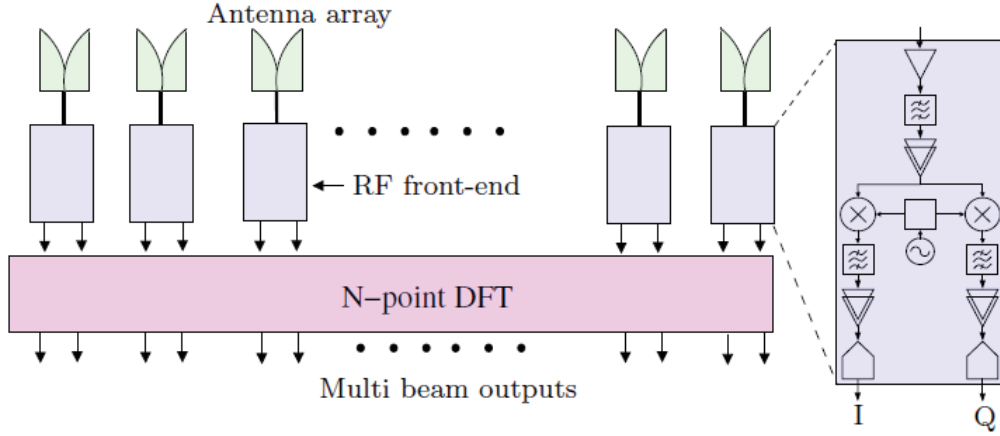


Figure 1: N-beam Array Processing System using a Linear Array

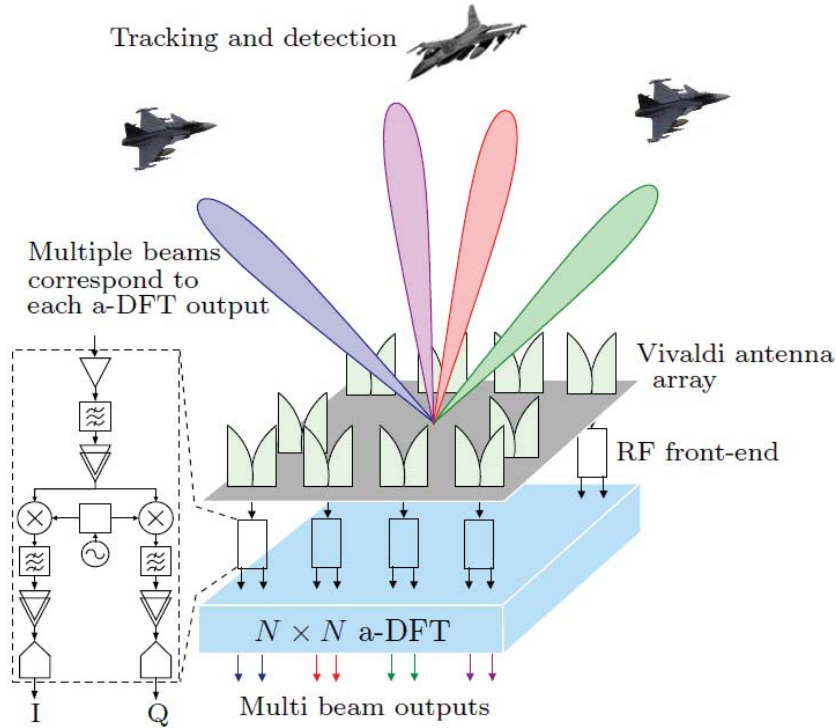


Figure 2: Operation of N Point 2-D FFT for obtaining N^2 Simultaneous Beams

3. APPROXIMATE-DFT ALGORITHMS

The exact FFT is never realized because digital architectures are subject to fixed-point effects such as quantization, rounding, saturation and truncation. Nonetheless, FFTs are a component of a lossy scheme as a result of practical hardware implementation. Rather than aim for an exact DFT via the infinite-precision realization of an FFT only to live with the residual errors that are unavoidable in practice, it makes sense to allow a tolerable deviation and find an approximation to the DFT that will have a tiny amount of deviation in its filterbank responses. By doing so, approximate-DFTs can achieve circuit complexities and power consumption that are substantially lower than that of best available FFT cores.

Approximate-DFT (a-DFT) algorithms compute the DFT at significantly lower circuit area, critical path latency, and power consumption for a particular very-large-scale integration (VLSI) platform. The algorithms are trained to find acceptably small deviations in the DFT filterbank responses in the stopband of each filter to achieve a reduction in complexity and power consumption.

Implemented approximate-DFT matrices are multiplierless. Further, the adder complexity is reduced through matrix factorization. The lower bounds are well defined for FFT algorithms and since this approach is an approximation of the exact DFT, such lower FFT bounds are no longer relevant. For example, consider $y = 1.013x_1 - 0.999x_2$ requires extensive multiplication hardware while $y \approx x_1 - x_2$ requires no multiplication hardware. Applications that utilize the fixed-point FFT, which can tolerate a baseline error level, can be replaced with these a-DFTs.

Replacement of the FFT with the a-DFTs can bring down the computational complexity of an N -element N -beamformer's complexity from $O(N \log_2 N)$ to zero and for an $N \times N$ rectangular aperture, from $O(N^2 \log_2 N^2)$ to zero. With the corresponding sparse-factorization, this reduction will be achieved without increasing the adder complexity. If a fully parallel implementation of a digital multiplier is k times larger than a parallel adder circuit, then it can be shown that, on this approach, for large N , the percentage saving of VLSI real-estate due to adoption of a multiplierless FFT approximation is asymptotic to $k/(1 + k)$. In brief, this approach works by accommodating a small and bounded (tolerable) computational error - which in turn, leads to low-complexity multi- beam aperture arrays.

The subsequent subsections would introduce the approximate transforms that have been found for 8-, 16-, 32-, and 64-point transforms.

3.1 8-point Approximate DFT Algorithm

The matrix form of the 8-point DFT approximation found is given in (1) [4, 5].

$$\hat{\mathbf{F}}_8 = \frac{1}{2} \cdot \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \end{bmatrix} \quad (1)$$

It can be seen that $\hat{\mathbf{F}}_8$ has only elements consisting of 0, ± 1 , ± 2 which can be realized using only adder and bit-shift operations, implying the use of zero multipliers.

$\hat{\mathbf{F}}_8$ can be factorized to further reduce the adder complexity:

$$\hat{\mathbf{F}}_8 = \mathbf{P} \times \text{diag}(\mathbf{I}_2, \mathbf{A}_1, \mathbf{A}_3) \times \mathbf{D}_2 \times \text{diag}(\mathbf{B}_2, \mathbf{I}_2, \mathbf{A}_4) \times \mathbf{D}_1 \times \text{diag}(\mathbf{B}_4, \mathbf{A}_2) \times \mathbf{B}_8.$$

$$\mathbf{B}_n = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \otimes \mathbf{I}_{n/2},$$

where I_n is the identity matrix of order n and $\otimes$ denotes the Kronecker product.

$$\mathbf{A}_1 = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \quad \mathbf{A}_3 = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \quad \mathbf{A}_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \quad \mathbf{A}_4 = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix}$$

$$\mathbf{D}_1 = \text{diag}(1, 1, 1, 1, 1, 1/2, 1, 1/2), \quad \mathbf{D}_2 = \text{diag}(1, 1, 1, j, 1, j, j, 1).$$

$$\mathbf{P} = [e_1|e_5|e_3|e_6|e_2|e_8|e_4|e_7]^T$$

where e_i is the 8-point column vector having a 1 at the i^{th} position and 0 elsewhere.

Adders Only Signal Flow Graph for 8-point a-DFT

Due to the coefficients of $\hat{\mathbf{F}}_8$ being small integer coefficients, Eq. (1) can be implemented such that the system contains only adders. The adders only signal flow graph is shown in Figure 3.

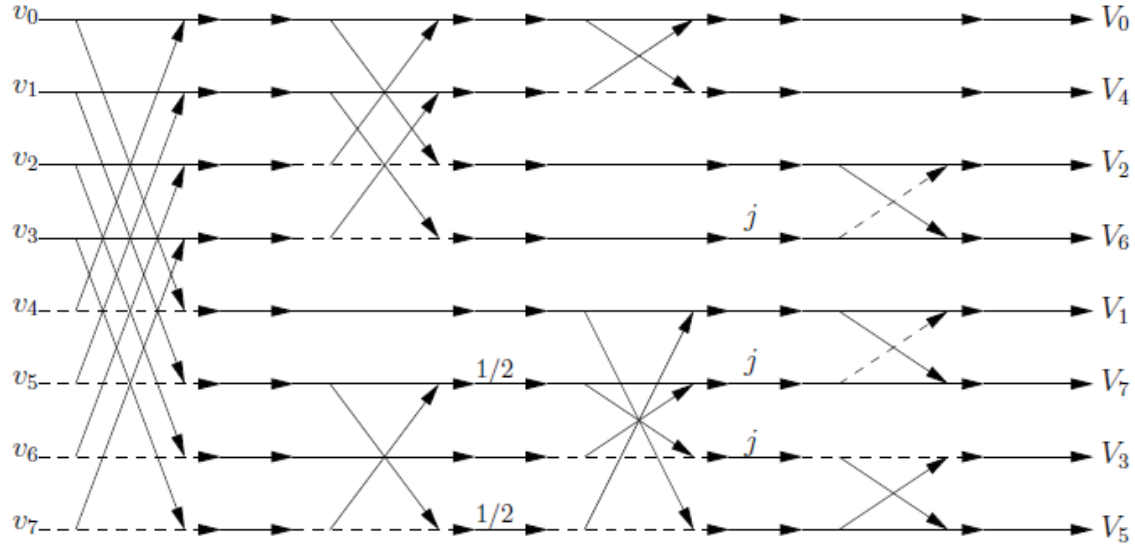


Figure 3: Signal Flow Graph of 8-point a-DFT

Frequency Responses and Errors

Closed-form beam patterns obtained using the 8-point a-DFT algorithm and FFT are shown in Figure 4. Figure 4 (a) shows the exact DFT beams and Figure 4 (b) shows the beams obtained using the 8-point a-DFT. Figure 4 (c) shows the error between the two transforms. The 1-D closed-form beam patterns obtained using the 8-point a-DFT algorithm and FFT for a Nyquist spaced ULA are shown in Figure 5.

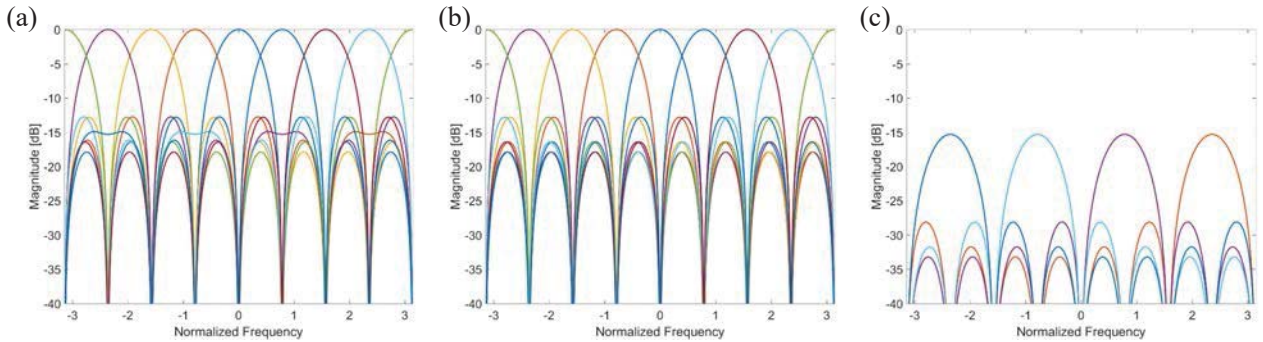


Figure 4: Closed-form Beam Patterns obtained using the 8-point a-DFT Algorithm and FFT

(a) Exact DFT Beams, (b) beams obtained using the 8-point a-DFT, and (c) error between the two transforms.

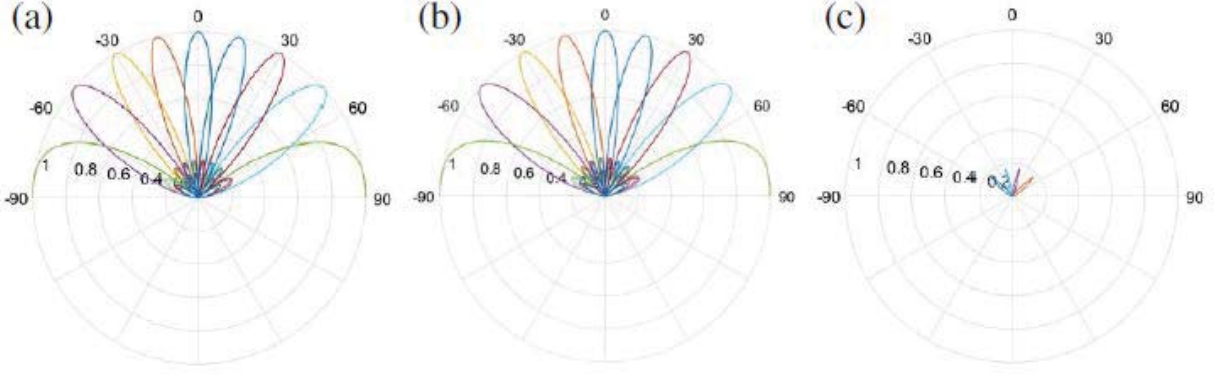


Figure 5: 1-D Closed-form Beam Patterns obtained using the 8-point a-DFT Algorithm and FFT for a Nyquist spaced ULA

(a) Exact DFT Beams, (b) beams obtained using the 8-point a-DFT, and (c) error between the two transforms.

Comparison of 8-point a-DFT with Reduced Precision FFT

It would be logical to investigate the performance of implementing the exact FFT algorithms with its twiddle factors W_N^k heavily undersampled (by reducing precision of the coefficients).

Here, $W_N^k = e^{j2\pi k/N}$ where $0 < k < N - 1$ and N is the size of the DFT. The signal flow graph for 8-point radix-2 FFT algorithm is shown in Figure 6. The places where the twiddle factors are involved in the signal flow graph are highlighted in red. When the precision of these coefficients is reduced, the hardware complexity will reduce with a cost of reduction of the accuracy output frequency response. By comparing the performance of the filter bins, one would be able to see the role of the a-DFT, which is multiplier free (with coefficients having only bit shifts). It can also be seen that the performance is much better than when using a lower precision implementation of the FFT. The red. When the precision of these coefficients is reduced, the hardware complexity will reduce with a cost of reduction of the accuracy output frequency response. By comparing the performance of the filter bins, one would be able to see the role of the a-DFT, which is multiplier free (with coefficients having only bit shifts). It can also be seen that the performance is much better than when using a lower precision implementation of the FFT. The plots compare the frequency responses of exact FFT and the proposed a-DFT algorithm for each bin of the transform. For comparison purposes, we have considered a reduced precision of 4-bits for each frequency bin for the exact-DFT twiddle factors.

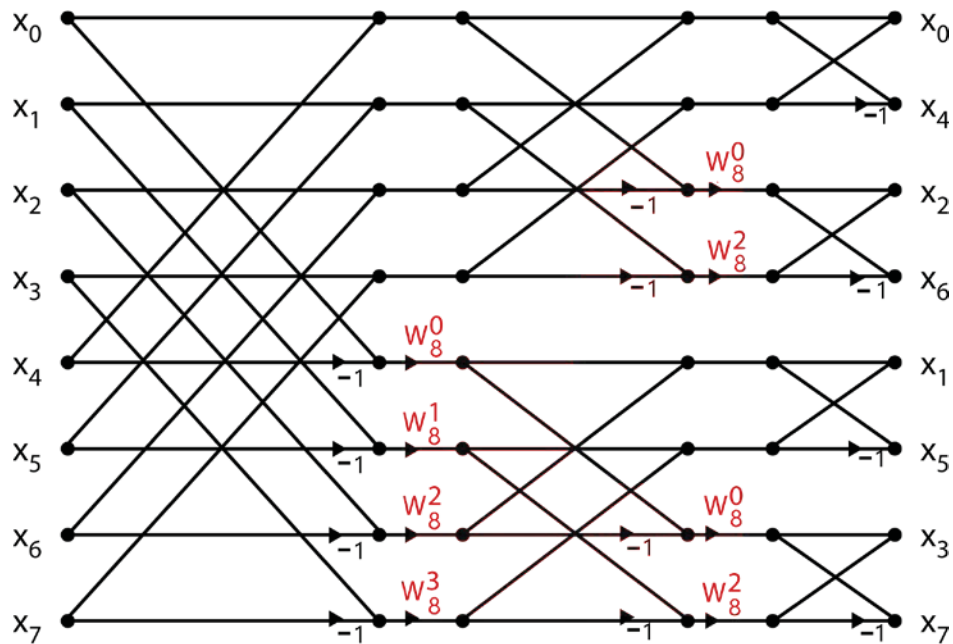


Figure 6: Signal Flow Graph for 8-point Radix-2 FFT

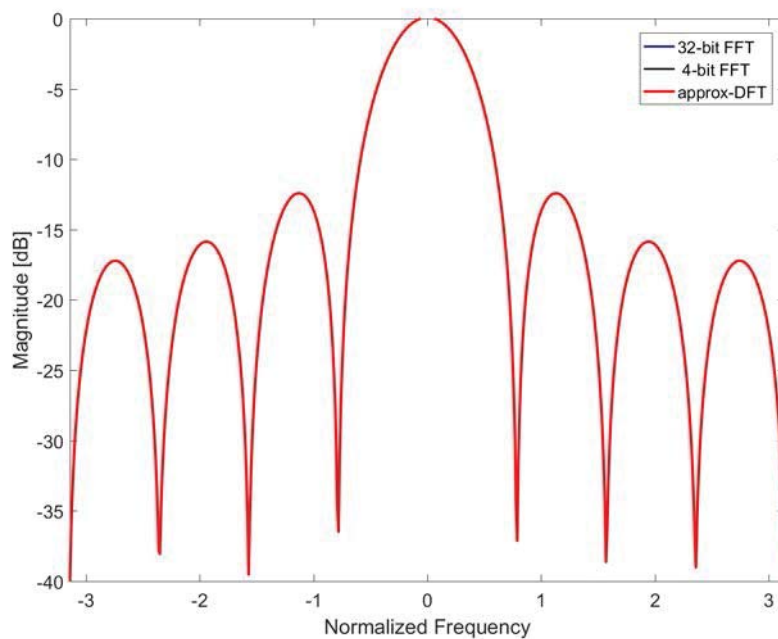


Figure 7: Output Comparison for Bin 1

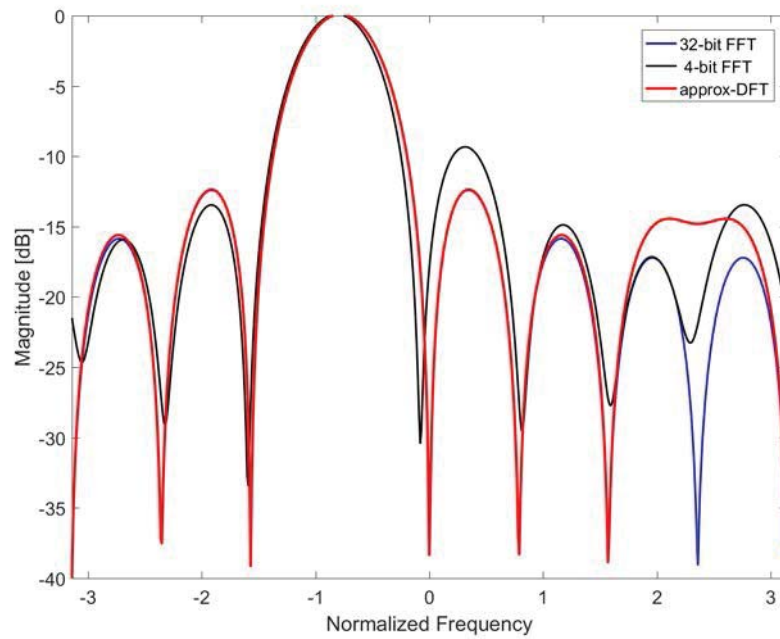


Figure 8: Output Comparison for Bin 2

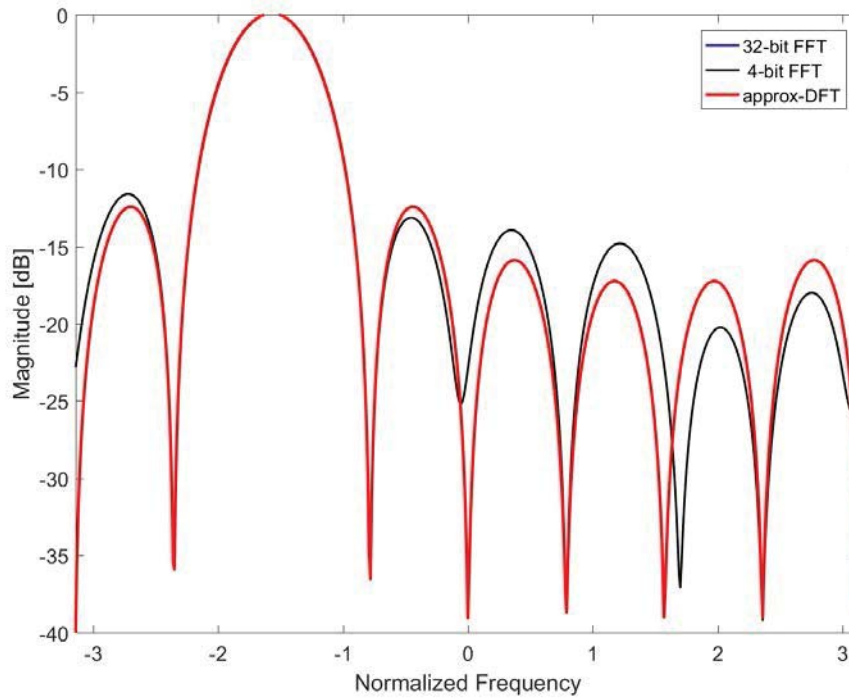


Figure 9: Output Comparison for Bin 3

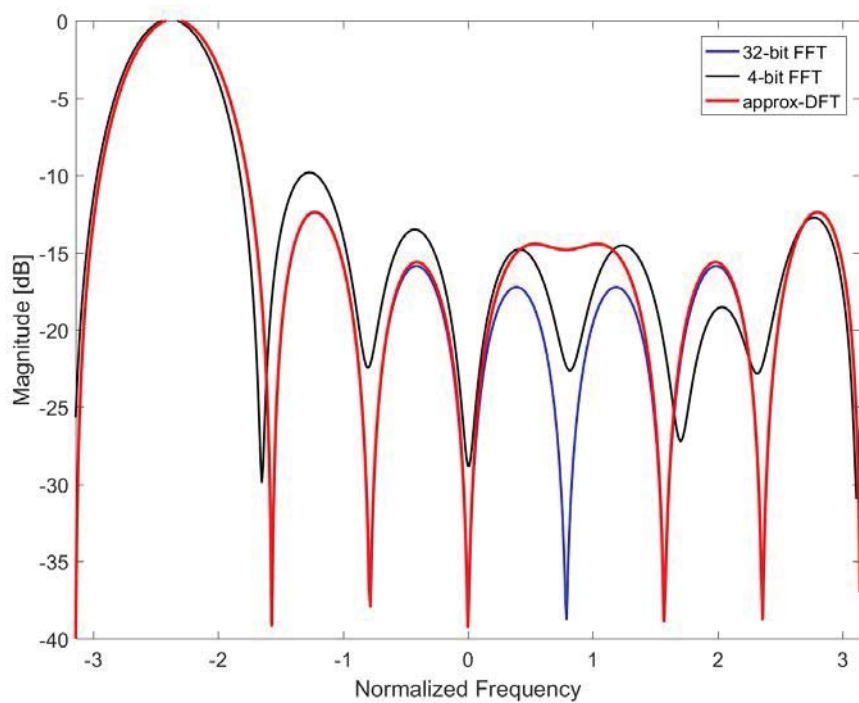


Figure 10: Output Comparison for Bin 4

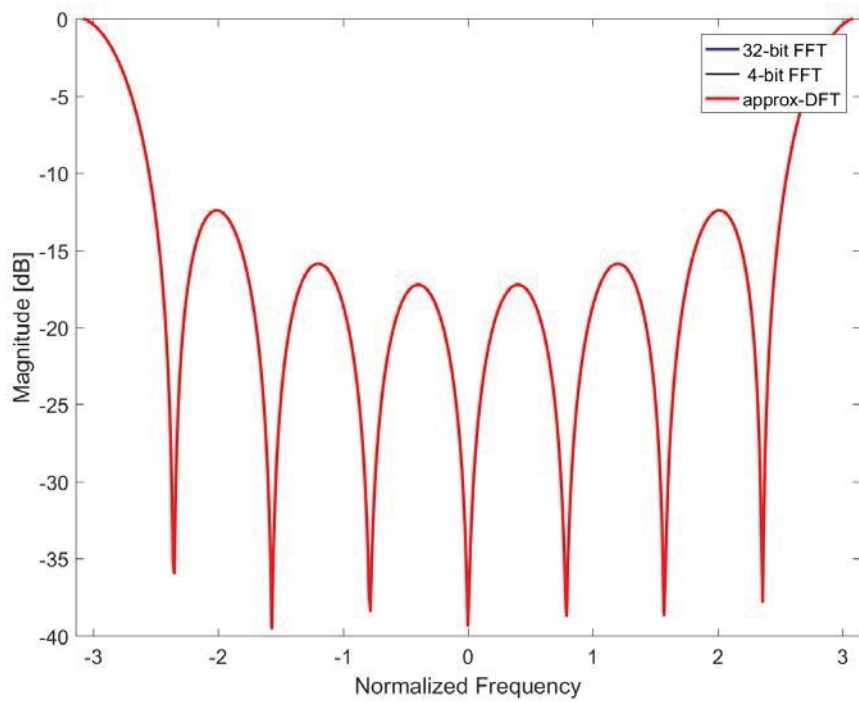


Figure 11: Output Comparison for Bin 5

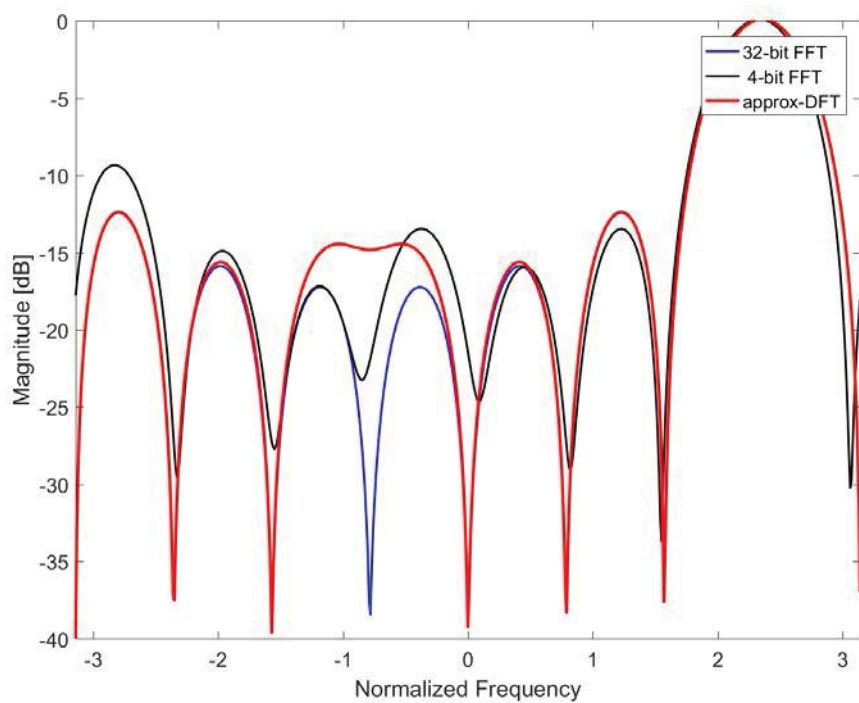


Figure 12: Output Comparison for Bin 6

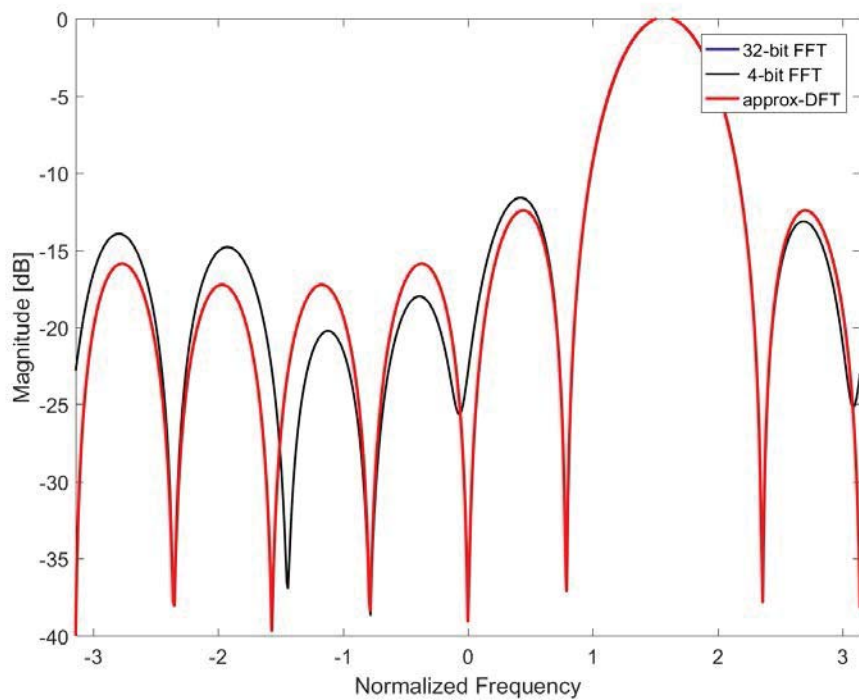


Figure 13: Output Comparison for Bin 7

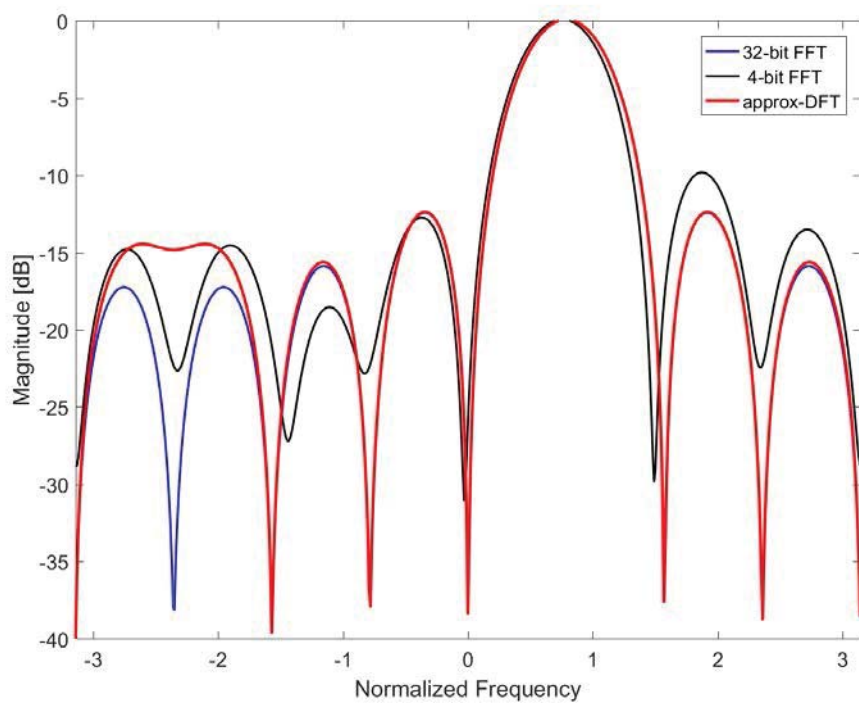


Figure 14: Output Comparison for Bin 8

3.2 16-point Approximate DFT Algorithm

$\hat{\mathbf{F}}_{16}$ denotes the 16-point a-DFT matrix. For ease of illustration, the matrix is divided into four quadrants as shown in Eq. (2).

$$\hat{\mathbf{F}}_{16} = \frac{1}{2} \begin{bmatrix} \mathbf{A}_{00} & \mathbf{A}_{01} \\ \mathbf{A}_{10} & \mathbf{A}_{11} \end{bmatrix} \quad (2)$$

$$\mathbf{A}_{00} = \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 2-1i & 1-1i & 1-2i & -2i & -1-2i & -1-1i & -2-1i \\ 2 & 1-1i & -2i & -1-1i & -2 & -1+1i & +2i & 1+1i \\ 2 & 1-2i & -1-1i & -2+1i & 2i & 2+1i & 1-1i & -1-2i \\ 2 & -2i & -2 & +2i & 2 & -2i & -2 & +2i \\ 2 & -1-2i & -1+1i & 2+1i & -2i & -2+1i & 1+1i & 1-2i \\ 2 & -1-1i & +2i & 1-1i & -2 & 1+1i & -2i & -1+1i \\ 2 & -2-1i & 1+1i & -1-2i & 2i & 1-2i & -1+1i & 2-1i \end{bmatrix},$$

$$\mathbf{A}_{01} = \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ -2 & -2+1i & -1+1i & -1+2i & 2i & 1+2i & 1+1i & 2+1i \\ 2 & 1-1i & -2i & -1-1i & -2 & -1+1i & +2i & 1+1i \\ -2 & -1+2i & 1+1i & 2-1i & -2i & -2-1i & -1+1i & 1+2i \\ 2 & -2i & -2 & +2i & 2 & -2i & -2 & +2i \\ -2 & 1+2i & 1-1i & -2-1i & 2i & 2-1i & -1-1i & -1+2i \\ 2 & -1-1i & +2i & 1-1i & -2 & 1+1i & -2i & -1+1i \\ -2 & 2+1i & -1-1i & 1+2i & -2i & -1+2i & 1-1i & -2+1i \end{bmatrix},$$

$$\mathbf{A}_{10} = \begin{bmatrix} 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -2+1i & 1-1i & -1+2i & -2i & 1+2i & -1-1i & 2+1i \\ 2 & -1+1i & -2i & 1+1i & -2 & 1-1i & +2i & -1-1i \\ 2 & -1+2i & -1-1i & 2-1i & 2i & -2-1i & 1-1i & 1+2i \\ 2 & +2i & -2 & -2i & 2 & +2i & -2 & -2i \\ 2 & 1+2i & -1+1i & -2-1i & -2i & 2-1i & 1+1i & -1+2i \\ 2 & 1+1i & +2i & -1+1i & -2 & -1-1i & -2i & 1-1i \\ 2 & 2+1i & 1+1i & 1+2i & 2i & -1+2i & -1+1i & -2+1i \end{bmatrix},$$

$$\mathbf{A}_{11} = \begin{bmatrix} 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ -2 & -2+1i & -1+1i & -1+2i & 2i & 1+2i & 1+1i & 2+1i \\ 2 & -1+1i & -2i & 1+1i & -2 & 1-1i & +2i & -1-1i \\ -2 & 1-2i & 1+1i & -2+1i & -2i & 2+1i & -1+1i & -1-2i \\ 2 & +2i & -2 & -2i & 2 & +2i & -2 & -2i \\ -2 & -1-2i & 1-1i & 2+1i & 2i & -2+1i & -1-1i & 1-2i \\ 2 & 1+1i & +2i & -1+1i & -2 & -1-1i & -2i & 1-1i \\ -2 & -2-1i & -1-1i & -1-2i & -2i & 1-2i & 1-1i & 2-1i \end{bmatrix}.$$

$\hat{\mathbf{F}}_{16}$ can be factorized to further reduce the adder complexity. The factorization is comprised of 6 stages, which is given by

$$\hat{\mathbf{F}}_{16} = W_5 W_4 W_3 W_2 D_1 W_1.$$

Matrices pertaining to the factorization stages are shown below.

$$W_5 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},$$

$$W_4 = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},$$

[illegible]

[illegible]

$$W_1 = \begin{bmatrix} 2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & -2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -2 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & -2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The matrix factors $W_{1,2,3,4,5}$ consist of sparse matrices having non-zero elements -2,-1,1,2 only, and $D_1 = 1/2 \text{ diag}(1, 1, 1, 1, 1, 1, 1, 1, 1, j, j, j, j, j, j, j, j)$.

Adders Only Signal Flow Graph for 16-point a-DFT

The factorization for $\hat{\mathbf{F}}_{16}$ can be used to develop the 16-point a-DFT matrix which is shown in Figure 15.

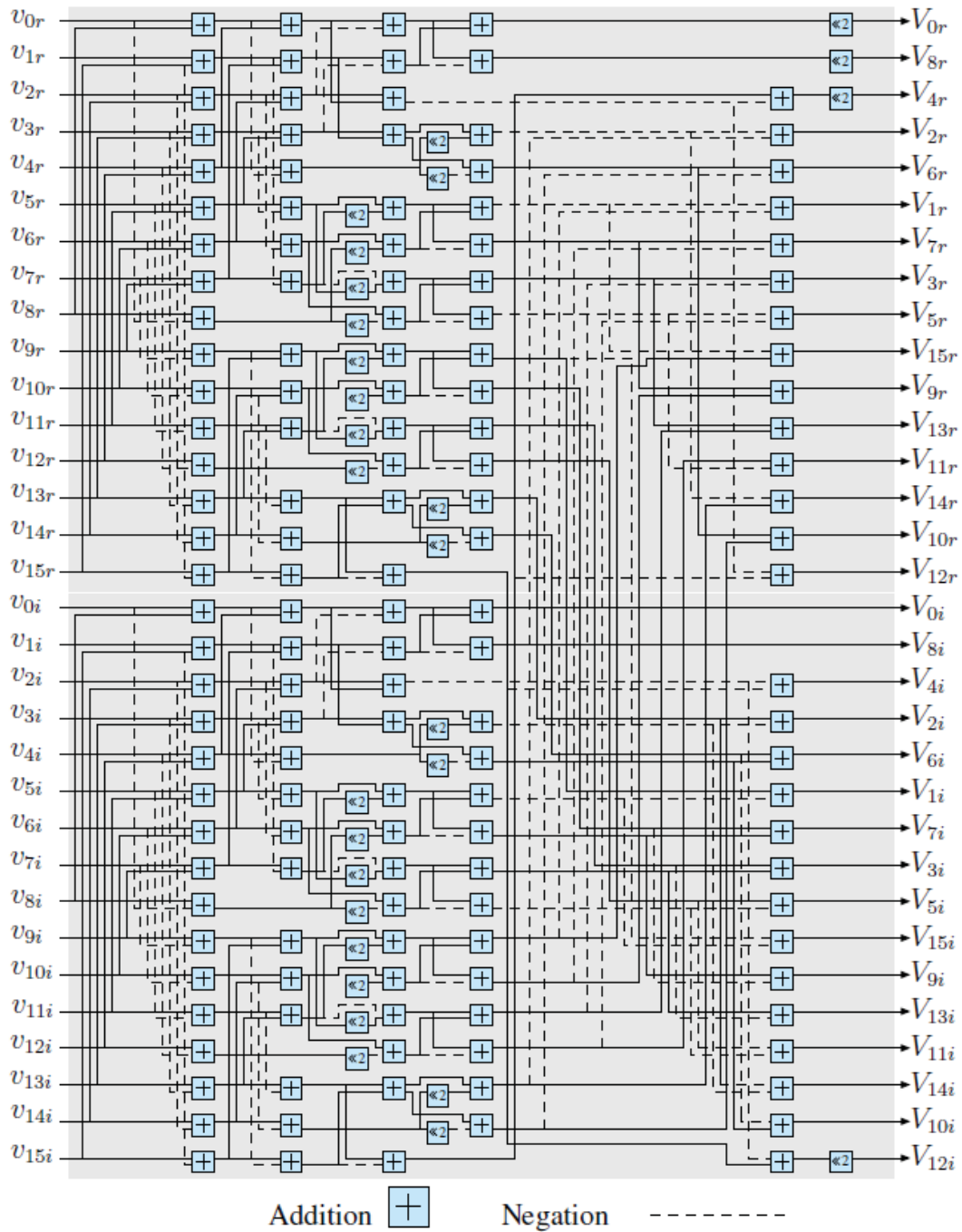


Figure 15: Signal Flow Graph of 16-point a-DFT

Frequency Responses and Errors

The 1-D closed-form beam patterns obtained using the 16-point a-DFT algorithm and FFT for a Nyquist spaced ULA are shown in Figure 16.

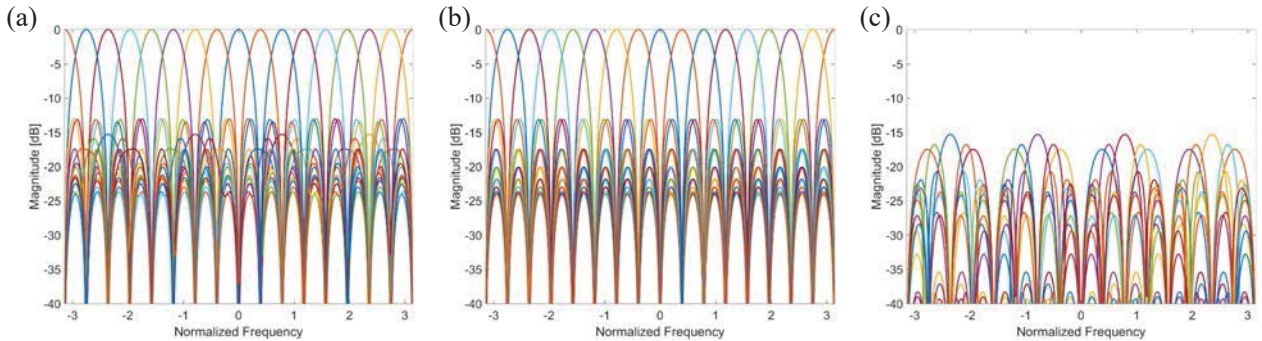


Figure 16: 1-D Closed-form Beam Patterns obtained using the 16-point a-DFT Algorithm and FFT for a Nyquist spaced ULA

(a) Exact DFT Beams, (b) beams obtained using the proposed 16-point a-DFT, and (c) error between the two transforms.

Closed-form beam patterns obtained using the 16-point a-DFT algorithm and DFT for a Nyquist spaced ULA are shown in Figure 17.

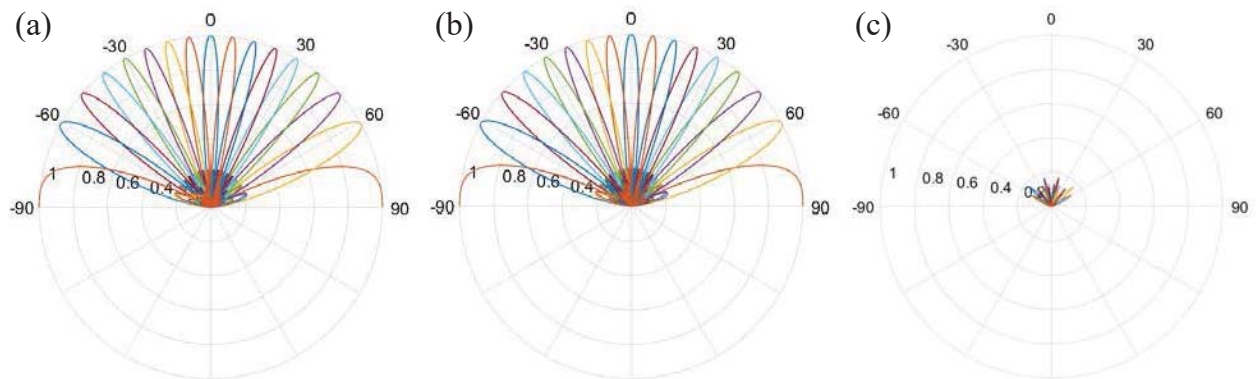


Figure 17: Closed-form Beam Patterns obtained using the 16-point a-DFT Algorithm and DFT for a Nyquist spaced ULA

(a) Exact DFT Beams, (b) beams obtained using the proposed 16-point a-DFT, and (c) error between the two transforms.

Comparison of 16-point a-DFT with Reduced Precision FFT

The comparison for all the exact FFT bins and the a-DFTs with reduced precision implementation of the DFT coefficient is repeated for the 16-point case. The following plots compare the frequency responses of exact FFT and the proposed a-DFT algorithm for each bin of the transform. For comparison, we have considered a reduced precision of 4-bits for each frequency bin for the exact-DFT, twiddle factors.

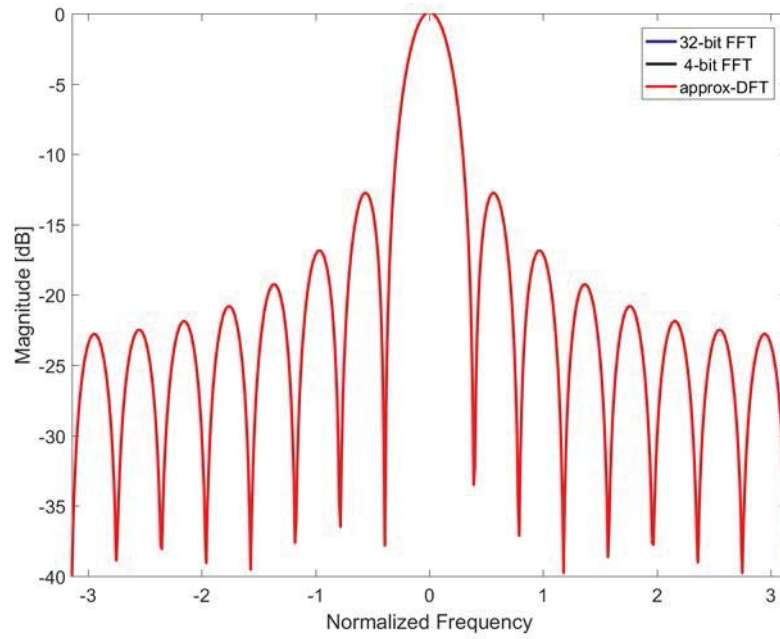


Figure 18: Output Comparison for Bin 1

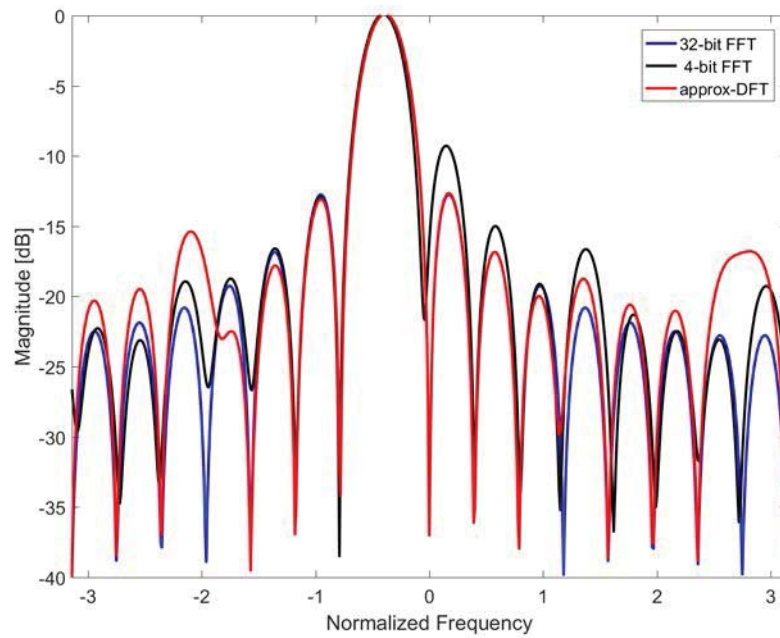


Figure 19: Output Comparison for Bin 2

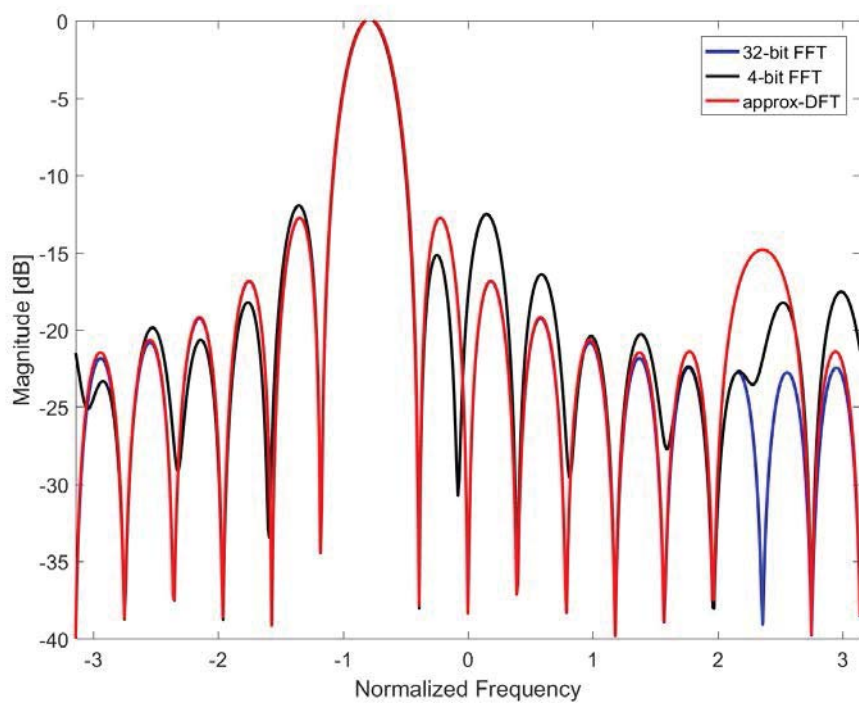


Figure 20: Output Comparison for Bin 3

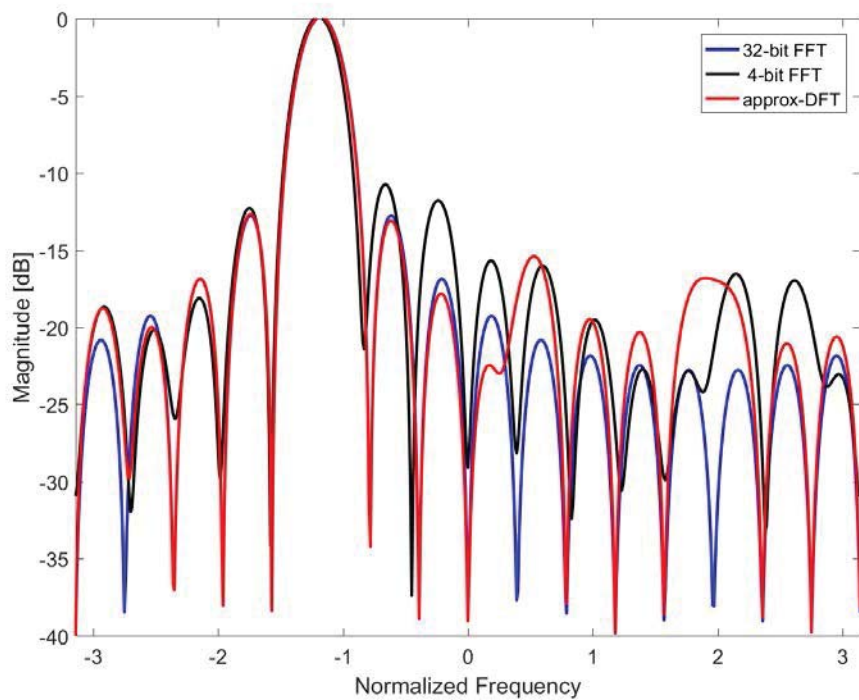


Figure 21: Output Comparison for Bin 4

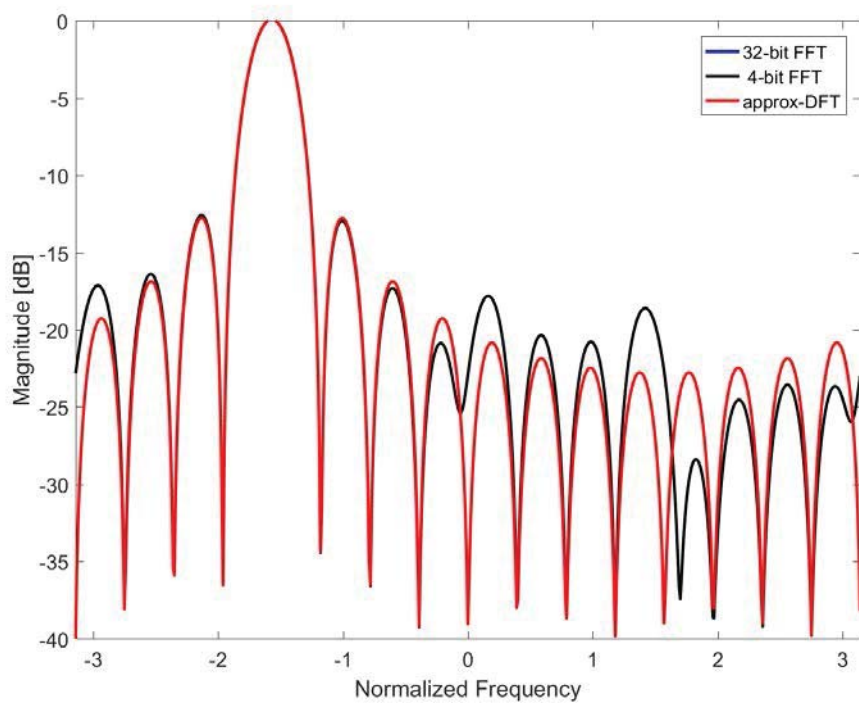


Figure 22: Output Comparison for Bin 5

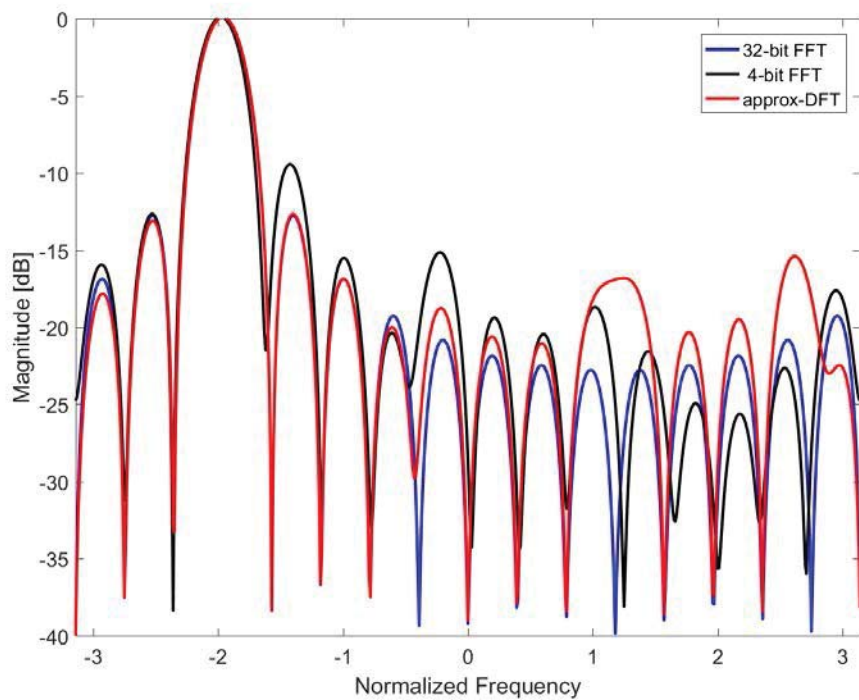


Figure 23: Output Comparison for Bin 6

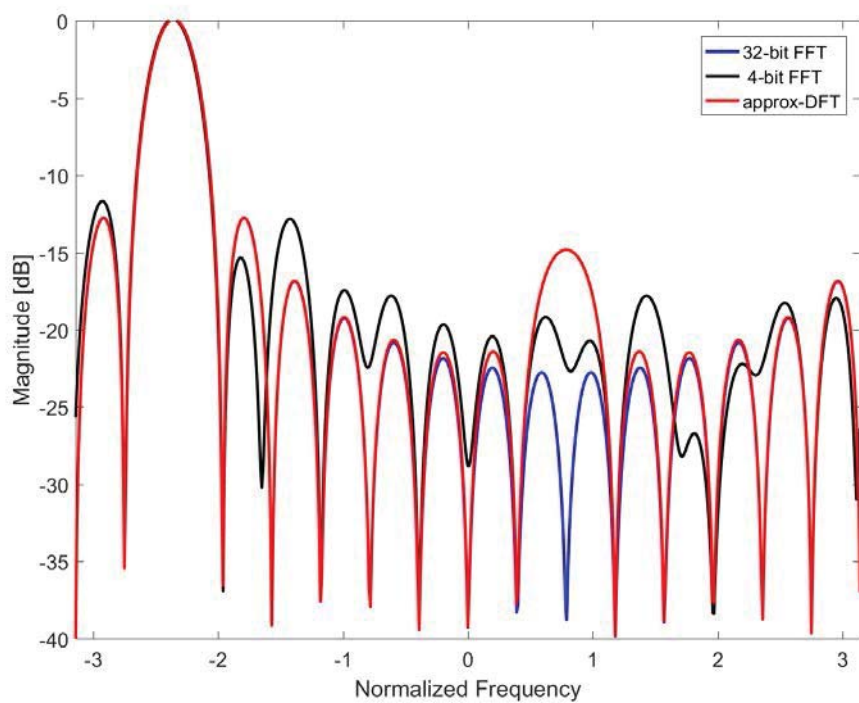


Figure 24: Output Comparison for Bin 7

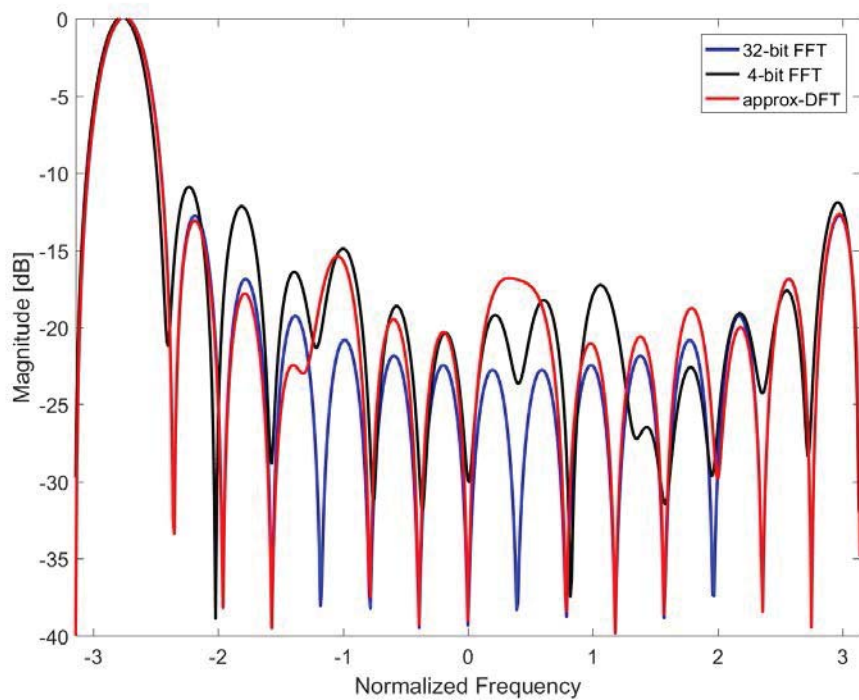


Figure 25: Output Comparison for Bin 8

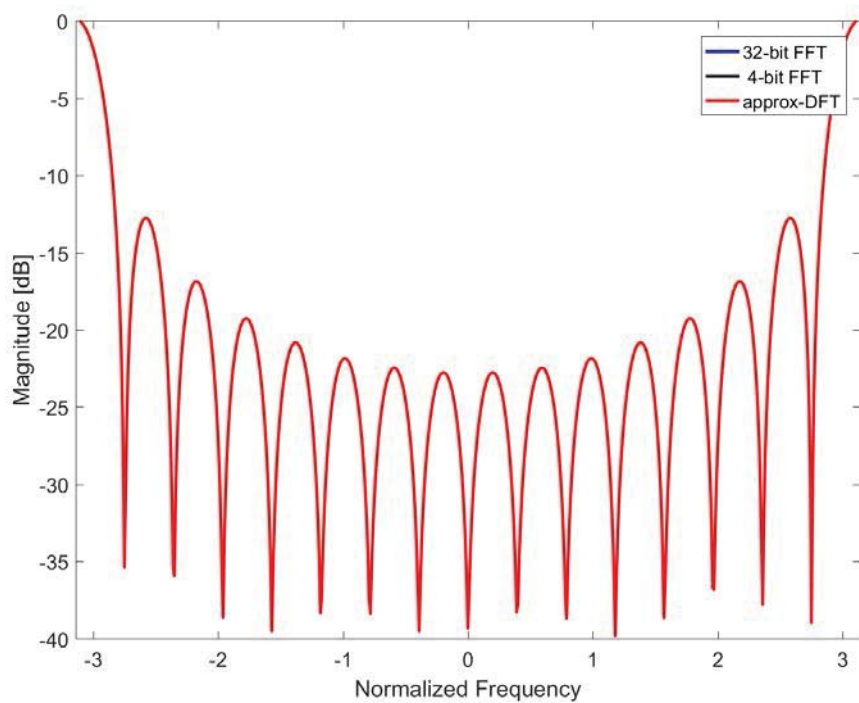


Figure 26: Output Comparison for Bin 9

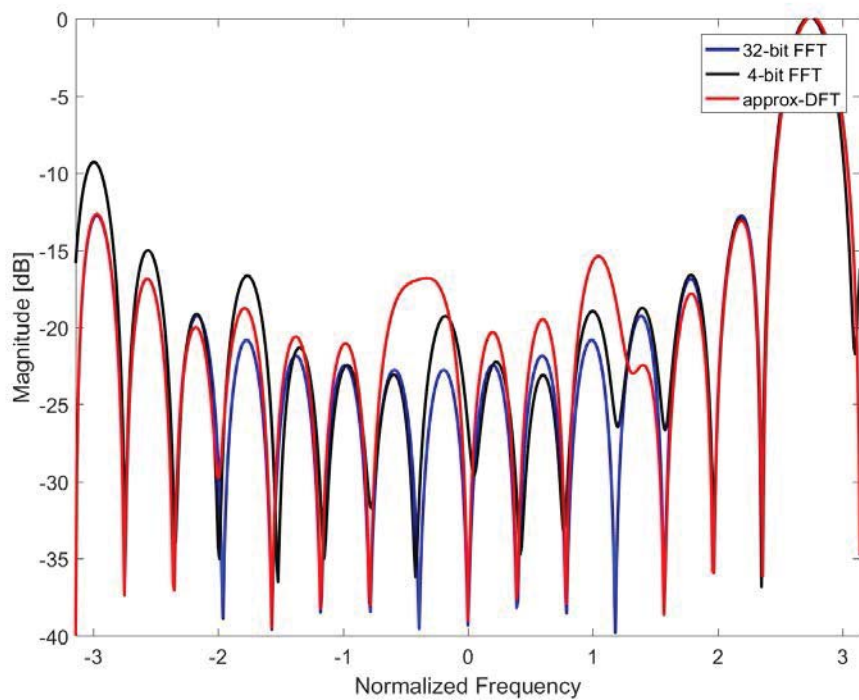


Figure 27: Output Comparison for Bin 10

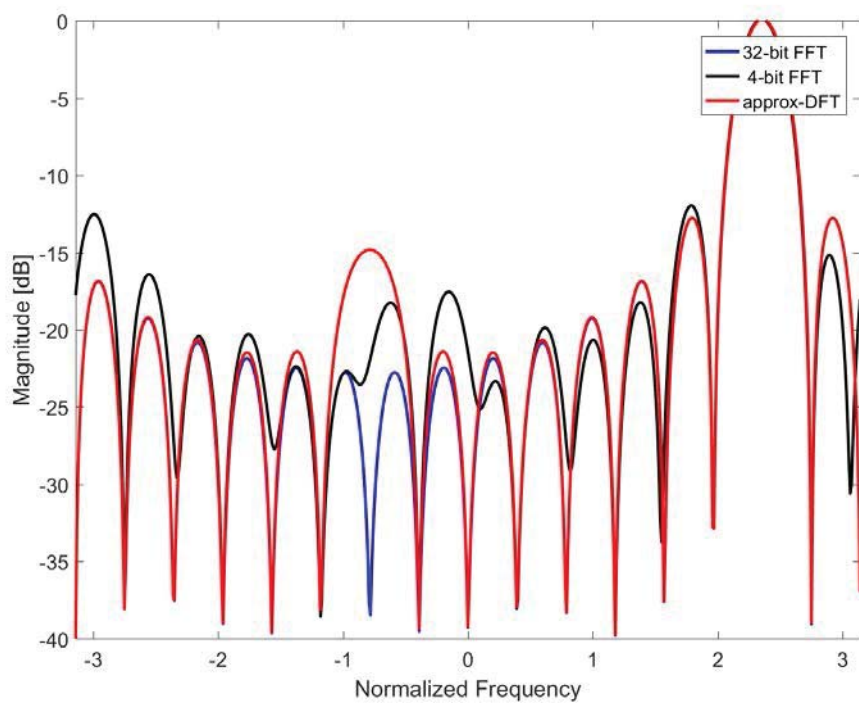


Figure 28: Output Comparison for Bin 11

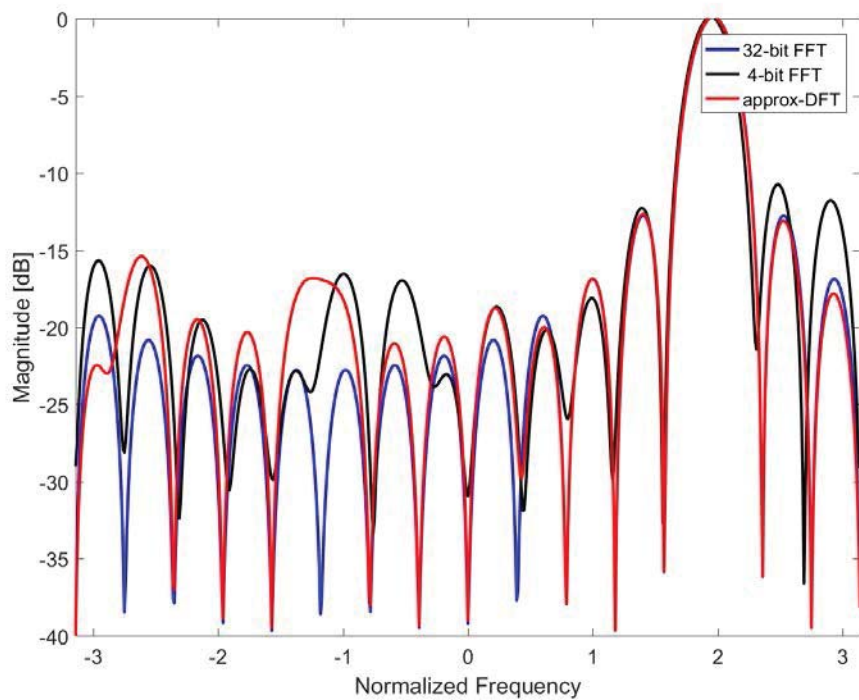


Figure 29: Output Comparison for Bin 12

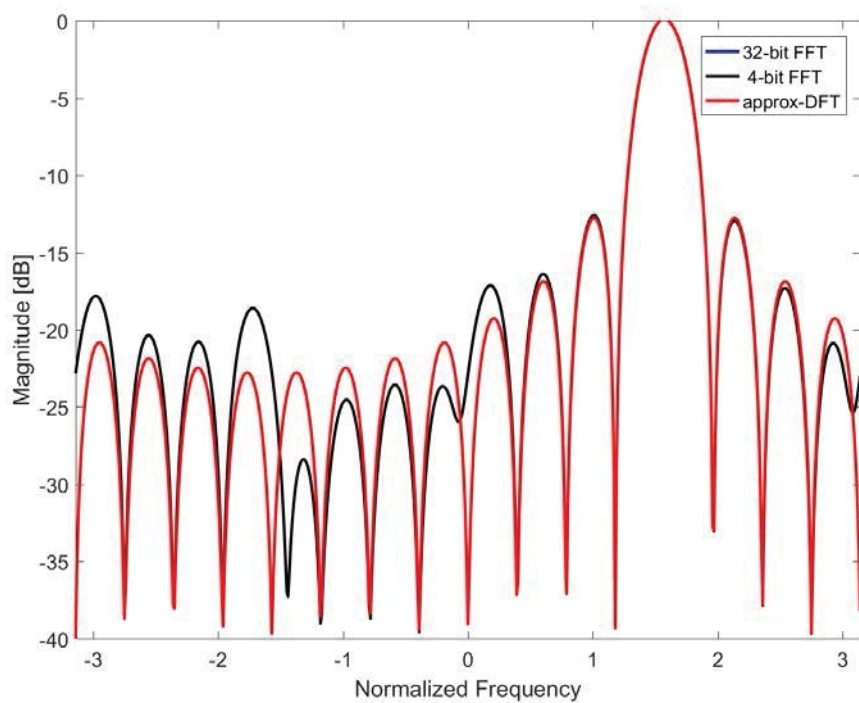


Figure 30: Output Comparison for Bin 13

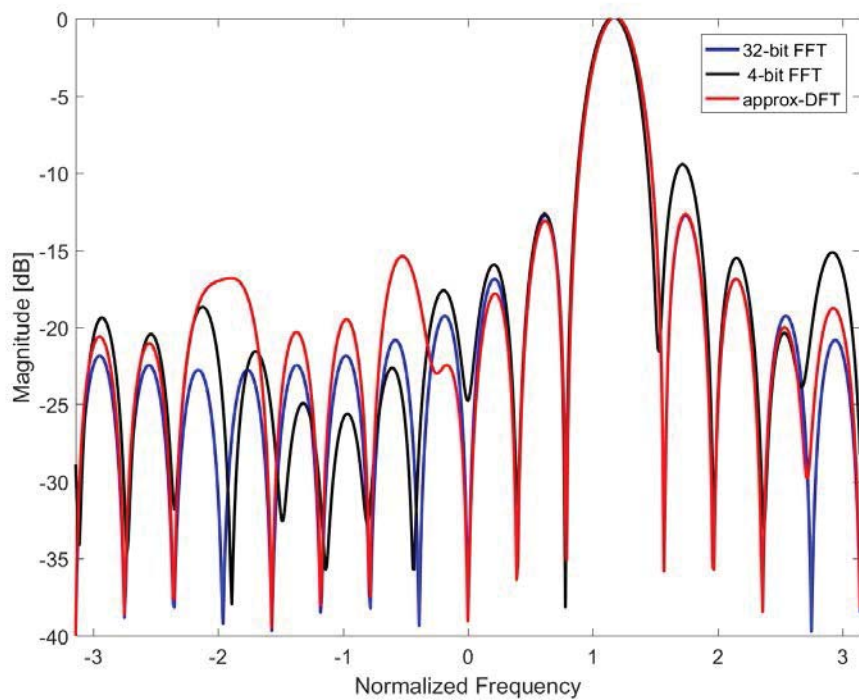


Figure 31: Output Comparison for Bin 14

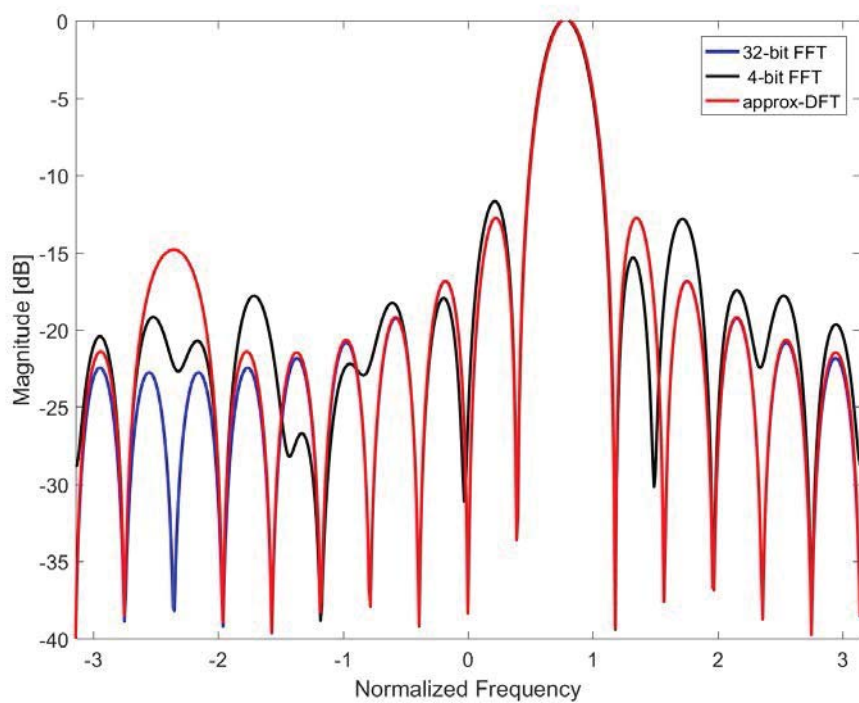


Figure 32: Output Comparison for Bin 15

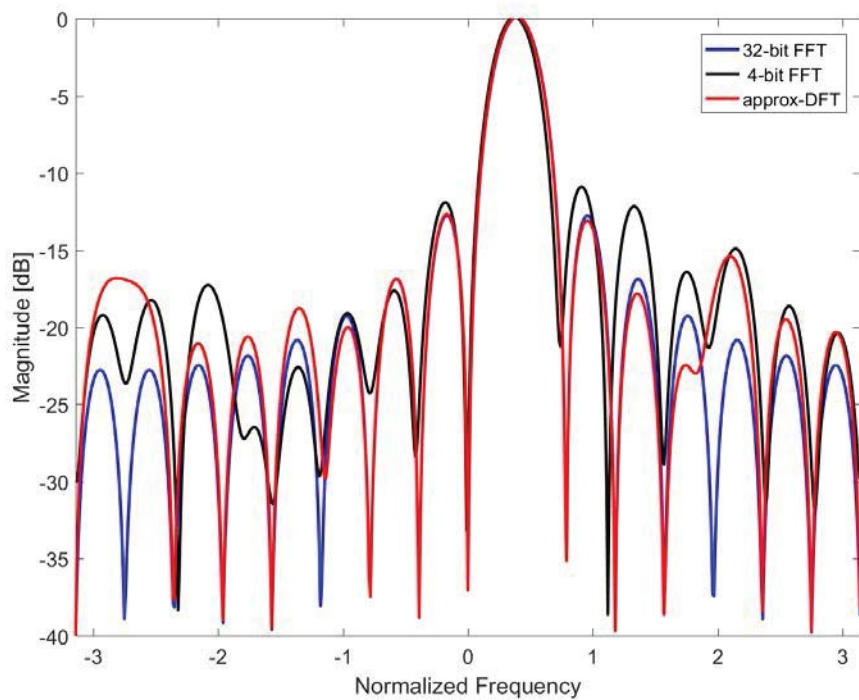


Figure 33: Output Comparison for Bin 16

$$\mathbf{A}_{11} = \begin{bmatrix} 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ -1 & 1 & -1 & 1-1i & -1+1i & 1-1i & 1i & -1i & 1i & -1i & 1i & -1-1i & 1+1i & -1-1i & 1 & -1 \\ 1 & -1 & 1-1i & 1i & -1i & 1i & -1-1i & 1 & -1 & 1 & -1+1i & -1i & 1i & -1i & 1+1i & -1 \\ -1 & 1-1i & 1i & -1i & 1+1i & -1 & 1 & -1+1i & -1i & 1+1i & -1 & 1 & -1+1i & -1i & 1i & -1-1i \\ 1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i & 1 & -1+1i & -1i & 1+1i & -1 & 1-1i & 1i & -1-1i \\ -1 & 1-1i & 1i & -1 & 1-1i & 1i & -1 & 1-1i & 1i & -1-1i & 1 & 1i & -1-1i & 1 & 1i & -1-1i \\ 1 & 1i & -1-1i & 1 & 1i & -1 & 1-1i & 1i & -1 & -1i & 1+1i & -1 & -1i & 1 & -1+1i & -1i \\ -1 & -1i & 1 & -1+1i & -1-1i & 1-1i & 1i & -1 & -1i & 1 & 1i & -1-1i & 1-1i & 1+1i & -1 & -1i \\ 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i & 1 & 1i & -1 & -1i \\ -1 & -1i & 1 & 1+1i & -1+1i & -1-1i & -1i & 1 & 1i & -1 & -1i & 1-1i & 1+1i & -1+1i & -1 & -1i \\ 1 & 1i & -1+1i & -1 & -1i & 1 & 1+1i & 1i & -1 & -1i & 1-1i & 1 & 1i & -1 & -1-1i & -1i \\ -1 & -1-1i & -1i & 1 & 1+1i & 1i & -1 & -1-1i & -1i & 1-1i & 1 & 1i & -1 & -1i & -1 & 1-1i \\ 1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i & 1 & 1+1i & 1i & -1+1i & -1 & -1-1i & -1i & 1-1i \\ -1 & -1-1i & -1i & -1i & 1-1i & 1 & 1 & 1+1i & 1i & -1+1i & -1 & -1 & -1-1i & -1i & -1i & 1-1i \\ 1 & 1 & 1+1i & 1i & 1i & 1i & -1+1i & -1 & -1 & -1 & -1-1i & -1i & -1i & -1i & 1-1i & 1 \\ -1 & -1 & -1 & -1-1i & -1-1i & -1-1i & -1i & -1i & -1i & -1i & -1i & 1-1i & 1-1i & 1-1i & 1 & 1 \end{bmatrix}.$$

$\hat{\mathbf{F}}_{32}$ can be factorized to reduce the adder complexity. This derived factorization consists of eight stages and is given by

$$\hat{\mathbf{F}}_{32} = W_8 W_7 W_6 W_5 W_4 W_3 W_2 W_1,$$

where W_k ($k = 1, \dots, 8$) are shown below.

$$\mathbf{W}_8 = \begin{bmatrix} \mathbf{w}_8^{00} & \mathbf{w}_8^{01} \\ \mathbf{w}_8^{10} & \mathbf{w}_8^{11} \end{bmatrix}$$

$$\mathbf{w}_8^{00} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1i & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1i & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1i & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1i \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1i & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1i & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1i & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{w}_8^{10} =$$

$$\mathbf{w}_8^{01} =$$

$$\mathbf{w}_8^{11} =$$

$$\mathbf{W}_7 = \begin{bmatrix} \mathbf{w}_7^{00} & \mathbf{w}_7^{01} \\ \mathbf{w}_7^{10} & \mathbf{w}_7^{11} \end{bmatrix}$$

[illegible]

[illegible]

$$\mathbf{w}_7^{01} =$$

$$w_7^{11} =$$

$$\mathbf{W}_6 = \begin{bmatrix} \mathbf{w}_6^{00} & \mathbf{w}_6^{01} \\ \mathbf{w}_6^{10} & \mathbf{w}_6^{11} \end{bmatrix}$$

$$\mathbf{w}_6^{00} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{w}_6^{10} =$$

$$\mathbf{w}_6^{01} =$$

$$\mathbf{w}_6^{11} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{W}_5 = \begin{bmatrix} \mathbf{w}_5^{00} & \mathbf{w}_5^{01} \\ \mathbf{w}_5^{10} & \mathbf{w}_5^{11} \end{bmatrix}$$

[illegible]

[illegible]

[illegible]

$$\mathbf{w}_5^{11} = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \end{bmatrix}$$

$$\mathbf{W}_4 = \begin{bmatrix} \mathbf{w}_4^{00} & \mathbf{w}_4^{01} \\ \mathbf{w}_4^{10} & \mathbf{w}_4^{11} \end{bmatrix}$$

[illegible]

[illegible]

[illegible]

$$\mathbf{w}_4^{11} =$$

$$\mathbf{W}_3 = \begin{bmatrix} \mathbf{w}_3^{00} & \mathbf{w}_3^{01} \\ \mathbf{w}_3^{10} & \mathbf{w}_3^{11} \end{bmatrix}$$

$$\mathbf{w}_3^{00} =$$

$$\mathbf{w}_3^{10} =$$

$$\mathbf{w}_3^{01} =$$

$$\mathbf{w}_3^{11} =$$

$$W_2 = \begin{bmatrix} w_2^{00} & w_2^{01} \\ w_2^{10} & w_2^{11} \end{bmatrix}$$

[illegible]

[illegible]

[illegible]

$$\mathbf{w}_2^{11} =$$

$$\mathbf{W}_1 = \begin{bmatrix} \mathbf{w}_1^{00} & \mathbf{w}_1^{01} \\ \mathbf{w}_1^{10} & \mathbf{w}_1^{11} \end{bmatrix}$$

$$\mathbf{w}_1^{00} =$$

$$\mathbf{w}_1^{10} =$$

$$\mathbf{w}_1^{01} =$$

$$w_1^{11} =$$

Frequency Responses and Errors

Closed-form beam patterns obtained using the 32-point a-DFT algorithm and FFT are shown in Figure 34. Figure 34 (a) shows the exact DFT beams and Figure 34 (b) shows the beams obtained using the proposed 32-point a-DFT. Figure 34 (c) shows the error between the two transforms.

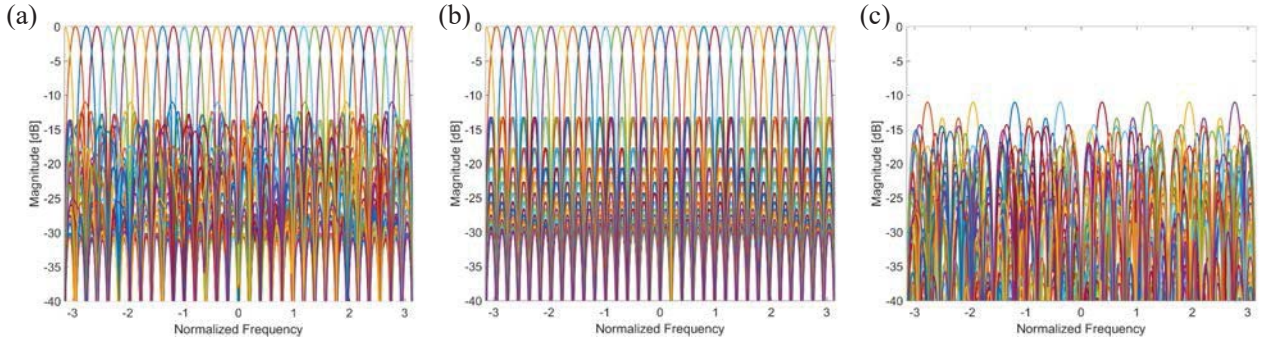


Figure 34: Closed-form Beam Patterns obtained using the 32-point a-DFT Algorithm and FFT

(a) Exact DFT beams, (b) beams obtained using the proposed 32-point a-DFT and (c) error between the two transforms

The 1-D closed form beam patterns obtained using the 32-point a-DFT algorithm and FFT for a Nyquist spaced ULA are shown in Figure 35.

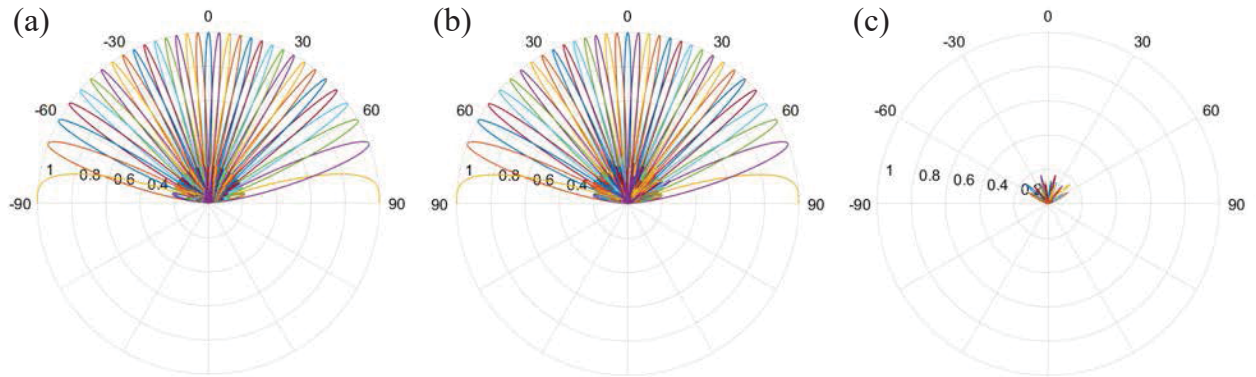


Figure 35: 1-D Closed-form Beam Patterns obtained using the 32-point a-DFT Algorithm and FFT for a Nyquist spaced ULA

(a) Exact DFT Beams, (b) beams obtained using the proposed 16-point a-DFT, and (c) error between the two transforms

Comparison of 32-point a-DFT with Reduced Precision FFT

The comparison for all the exact FFT bins and the a-DFTs with reduced precision implementation of the DFT coefficient is repeated for the 32-point case. The following plots compares the frequency responses of the exact FFT and the proposed a-DFT algorithm for each

bin of the transform. For comparison, we have considered a reduced precision of 4-bits for each frequency bin for the exact-DFT twiddle factors.

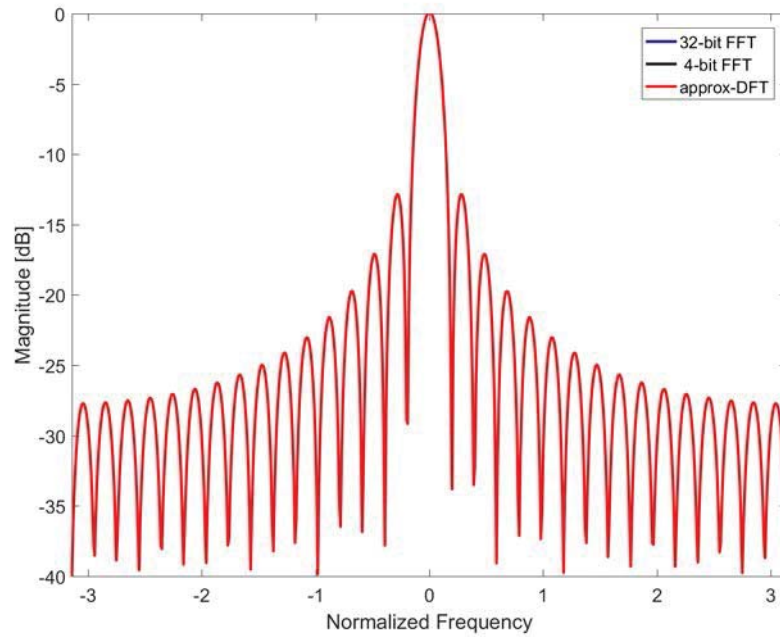


Figure 36: Output Comparison for Bin 1

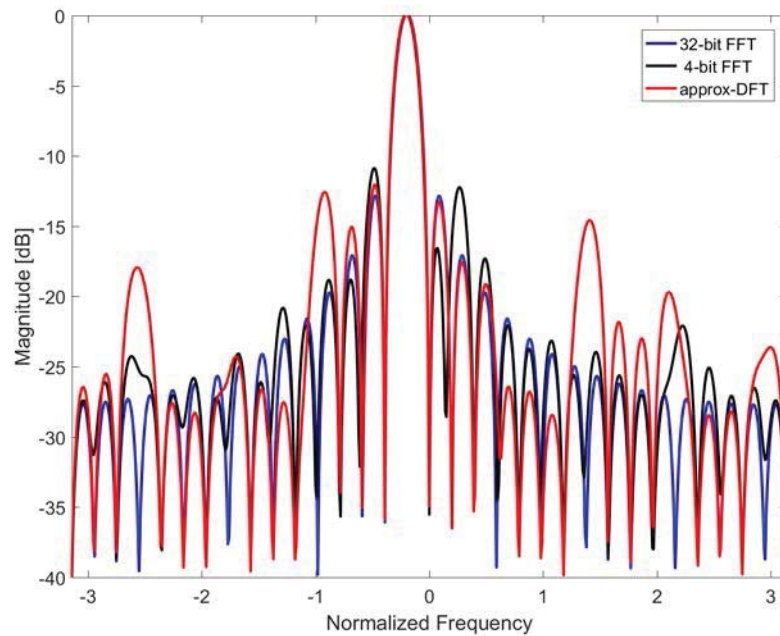


Figure 37: Output Comparison for Bin 2

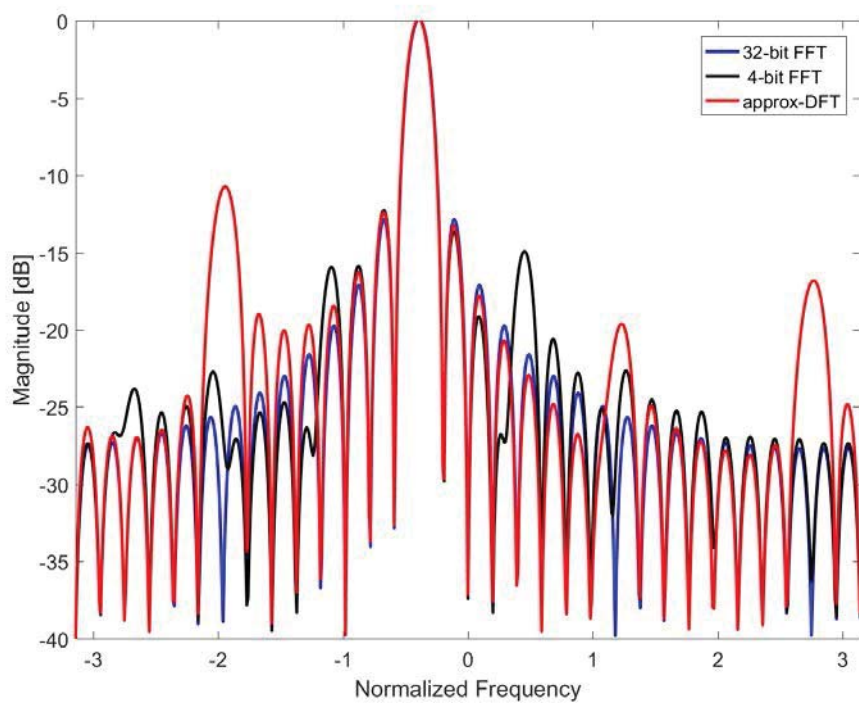


Figure 38: Output Comparison for Bin 3

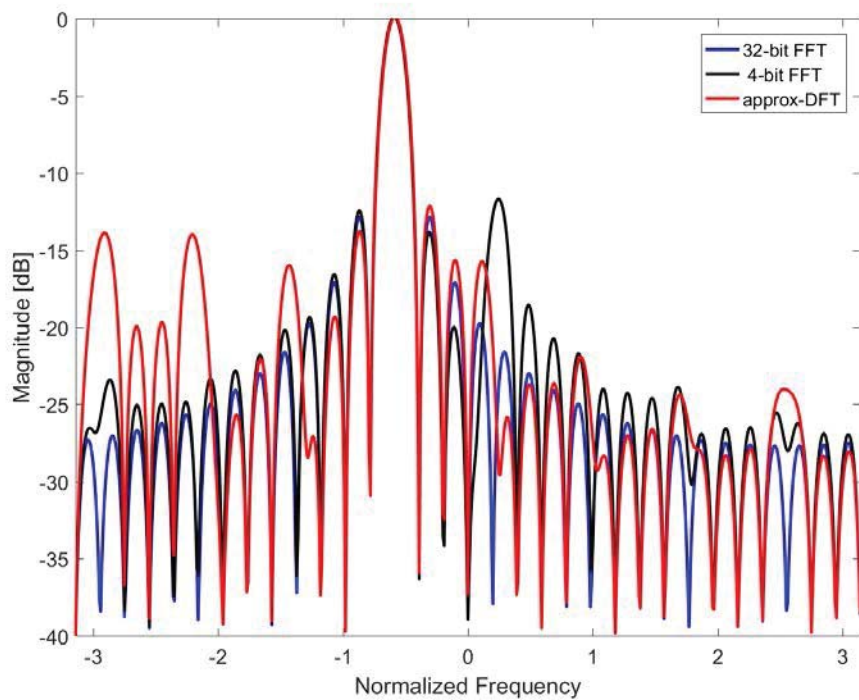


Figure 39: Output Comparison for Bin 4

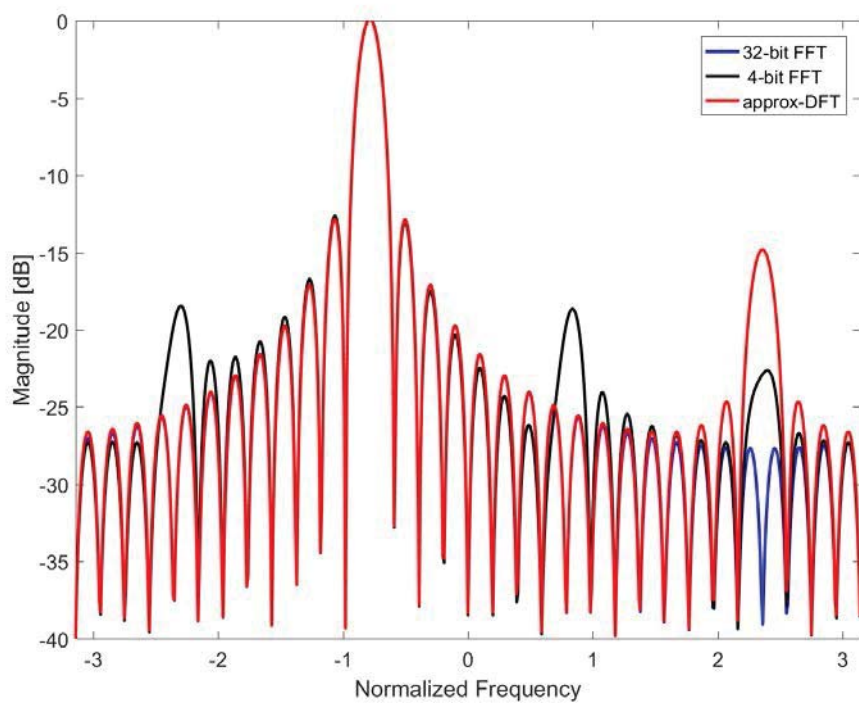


Figure 40: Output Comparison for Bin 5

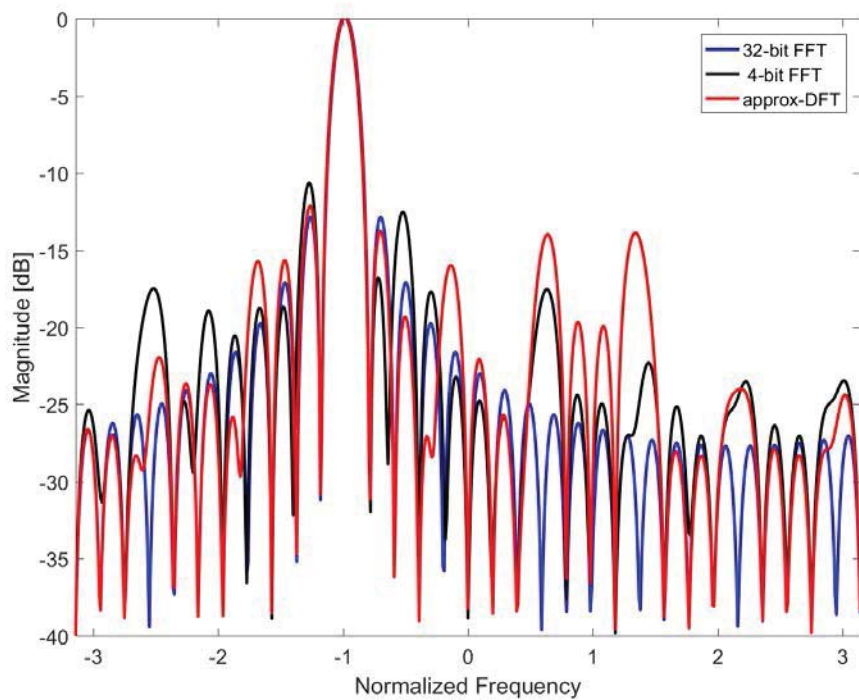


Figure 41: Output Comparison for Bin 6

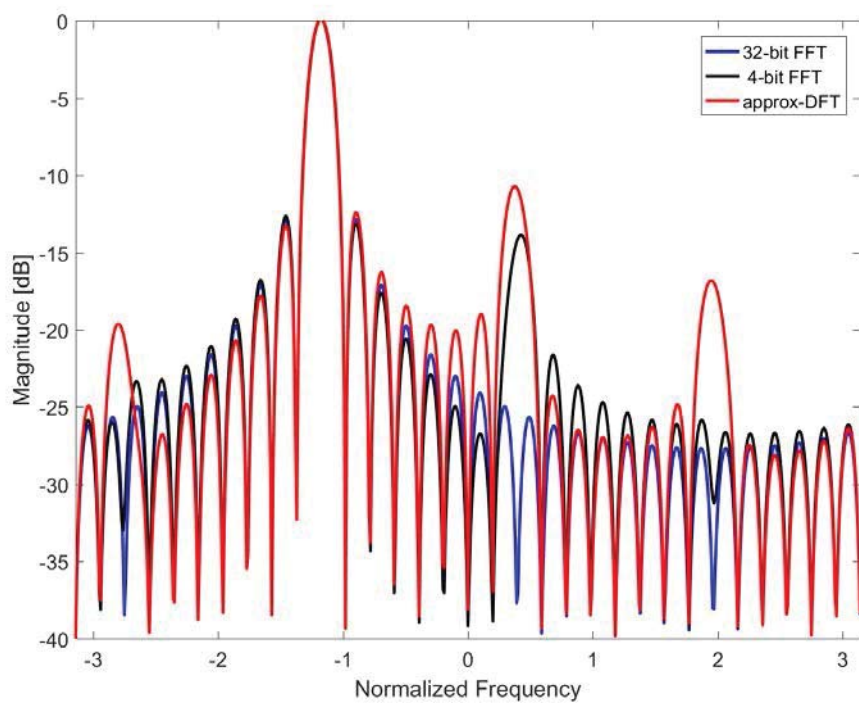


Figure 42: Output Comparison for Bin 7

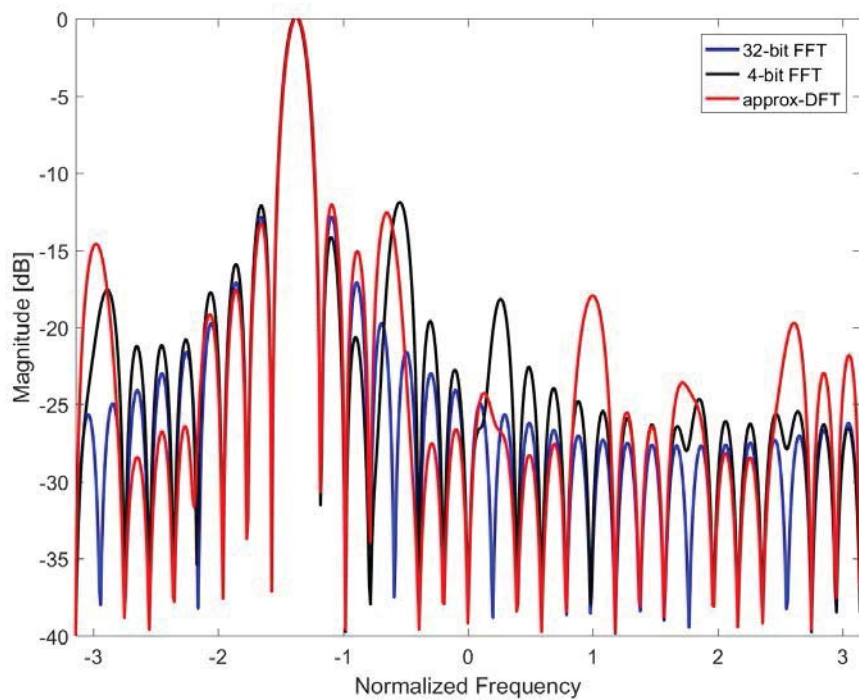


Figure 43: Output Comparison for Bin 8

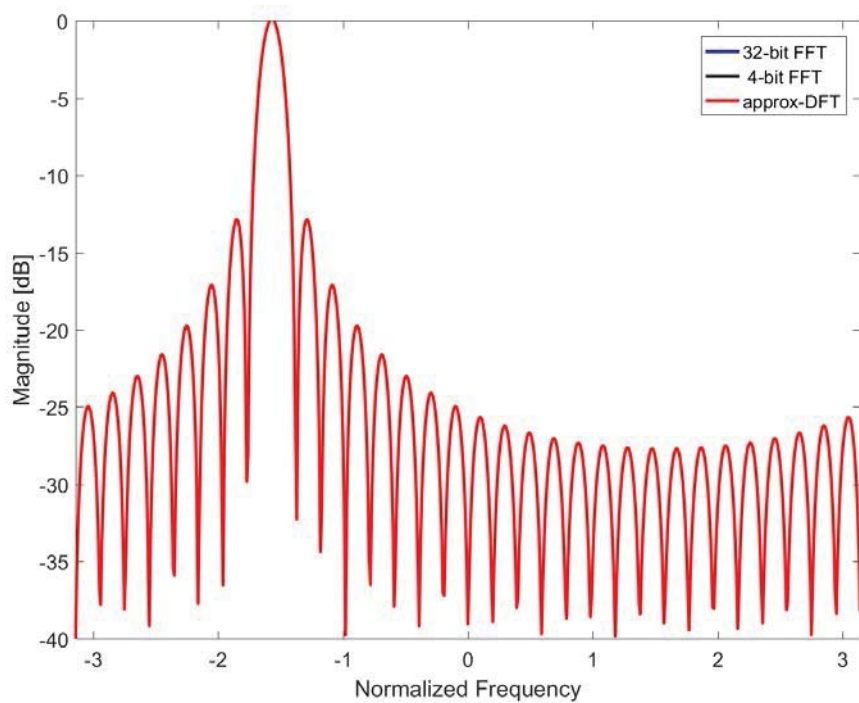


Figure 44: Output Comparison for Bin 9

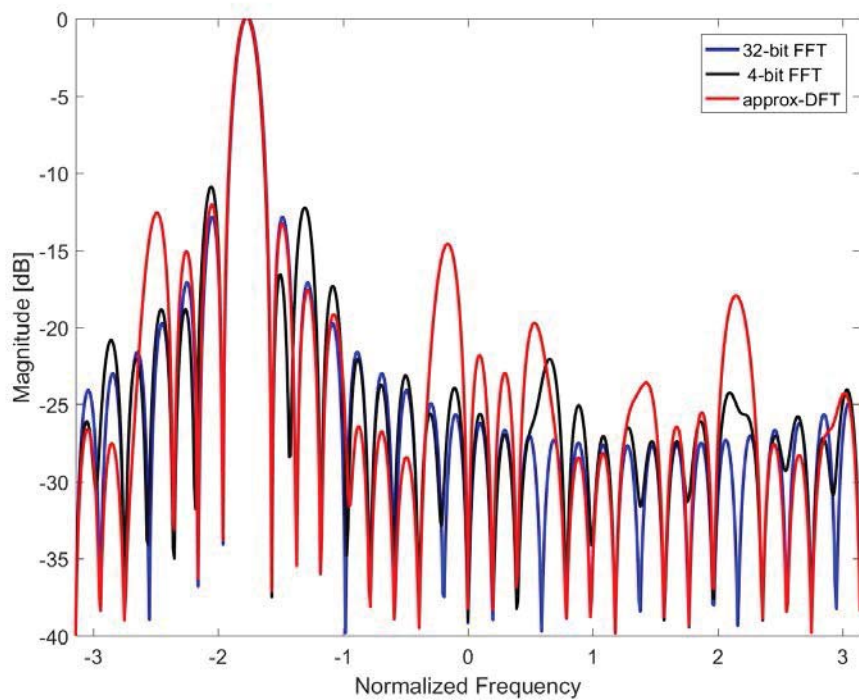


Figure 45: Output Comparison for Bin 10

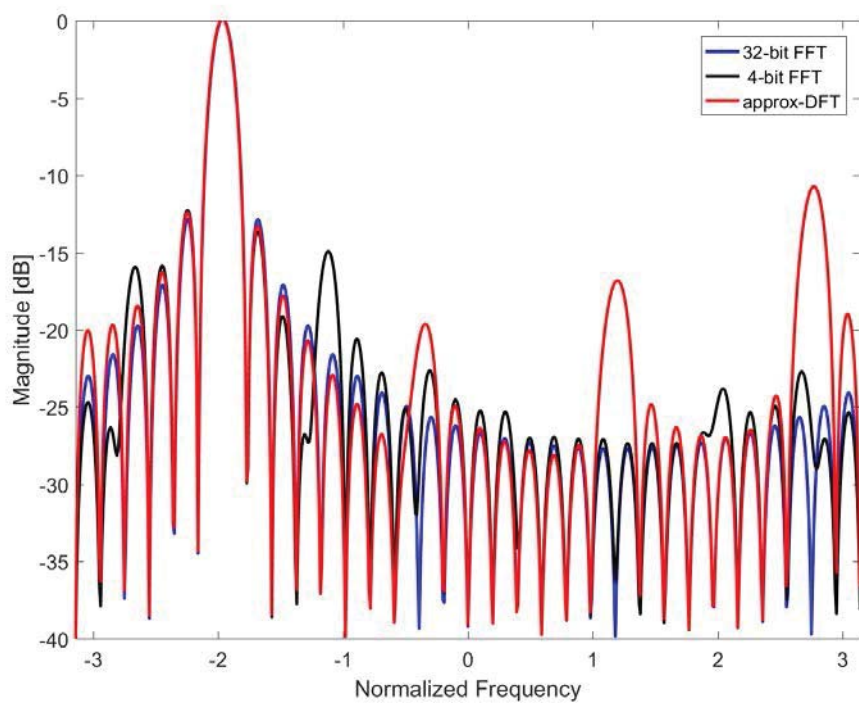


Figure 46: Output Comparison for Bin 11

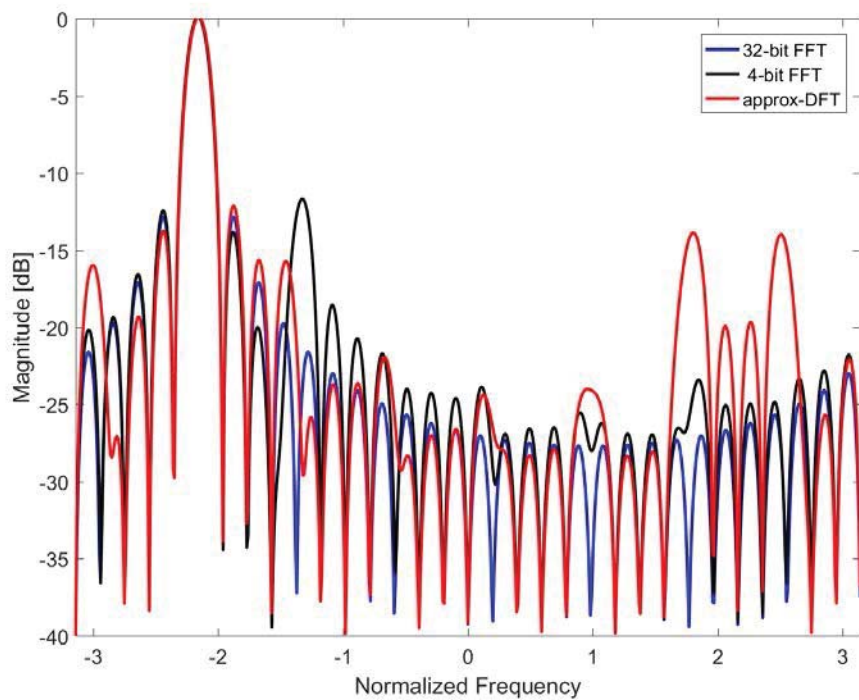


Figure 47: Output Comparison for Bin 12

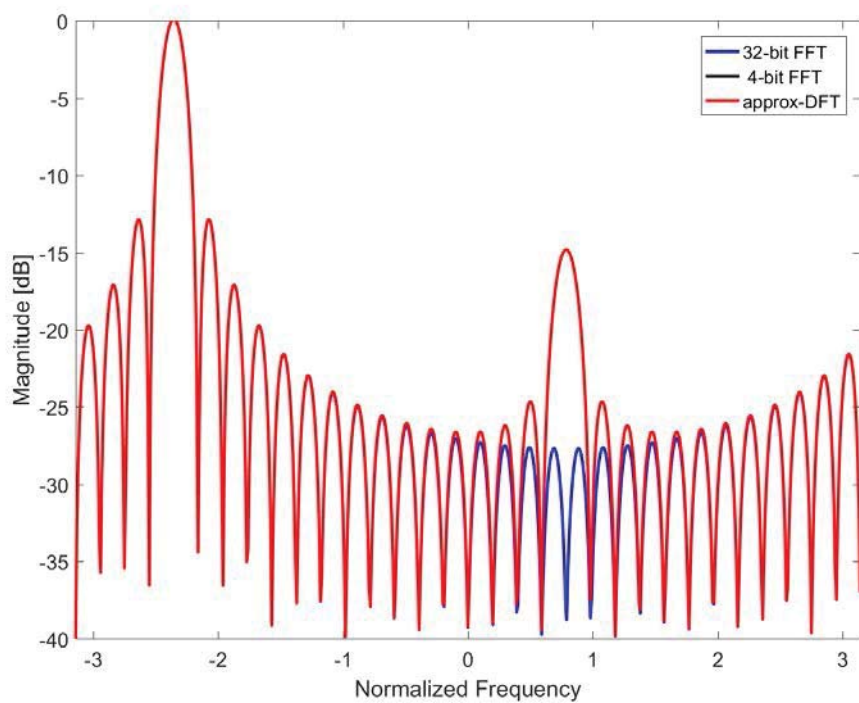


Figure 48: Output Comparison for Bin 13

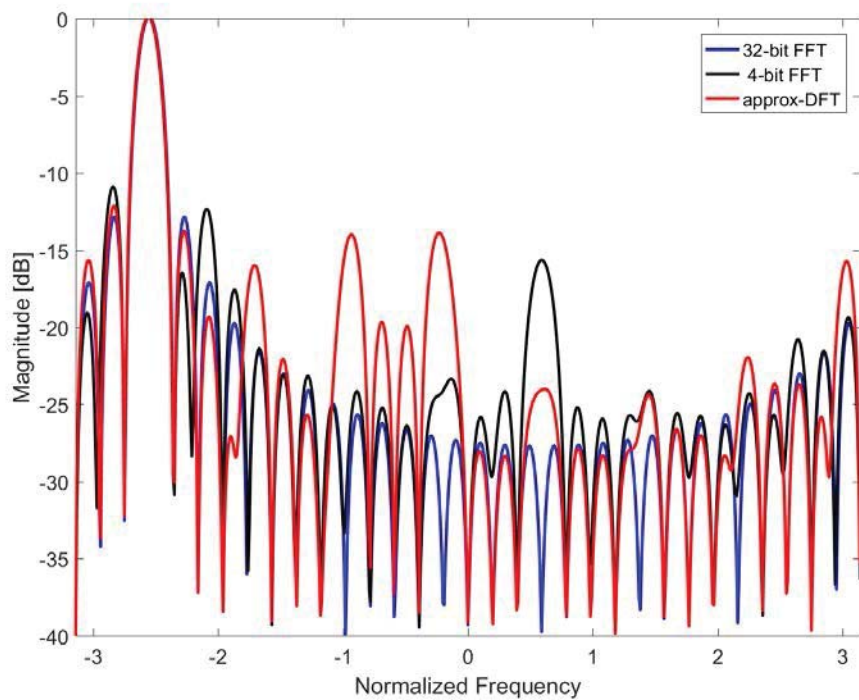


Figure 49: Output Comparison for Bin 14

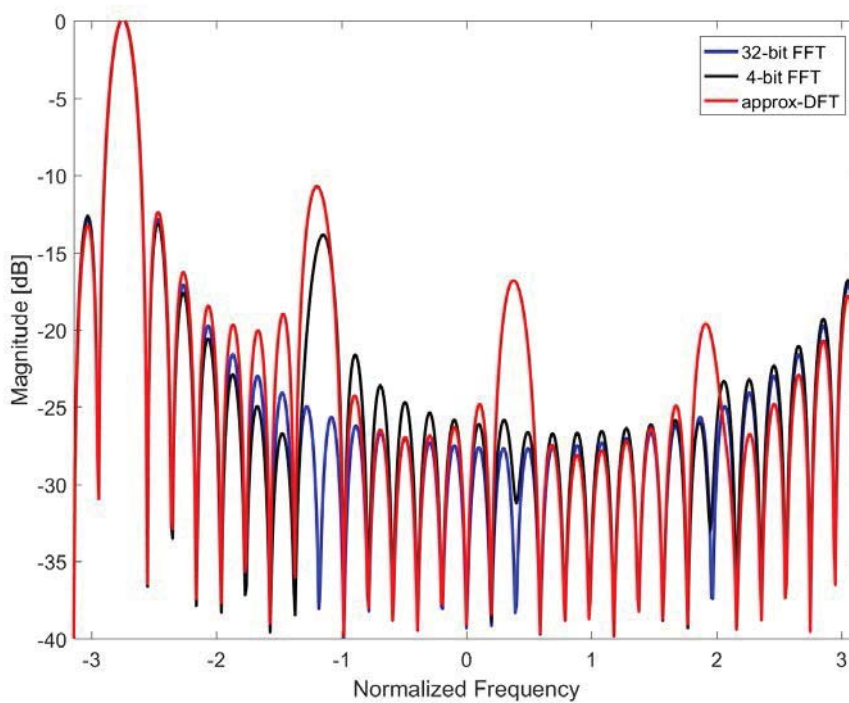


Figure 50: Output Comparison for Bin 15

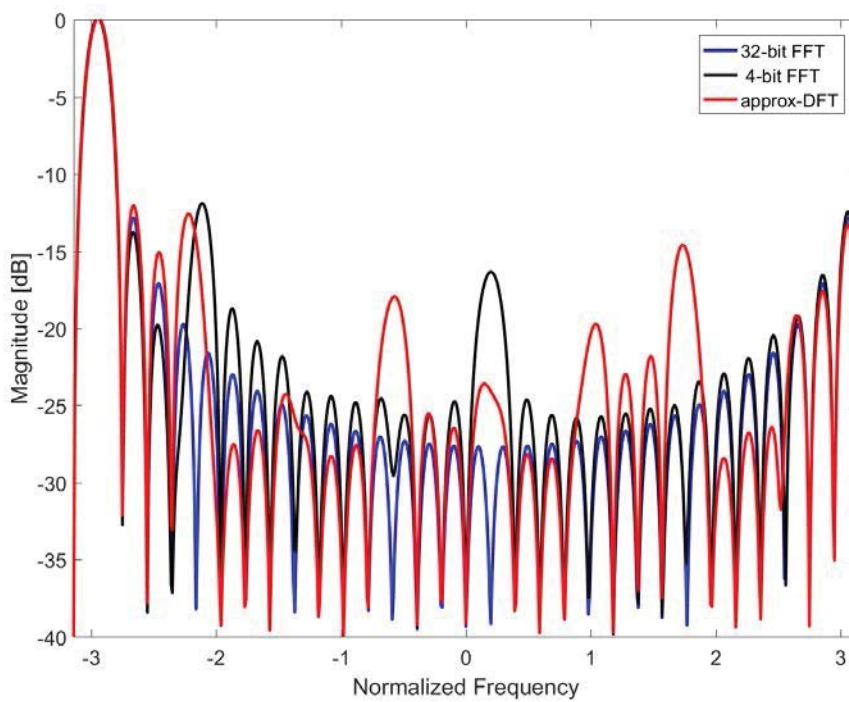


Figure 51: Output Comparison for Bin 16

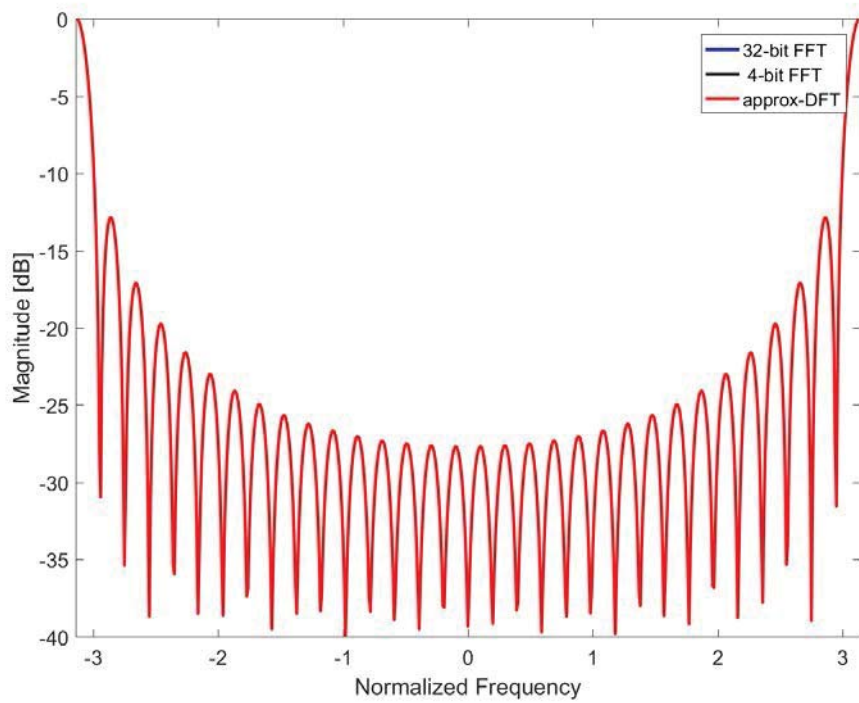


Figure 52: Output Comparison for Bin 17

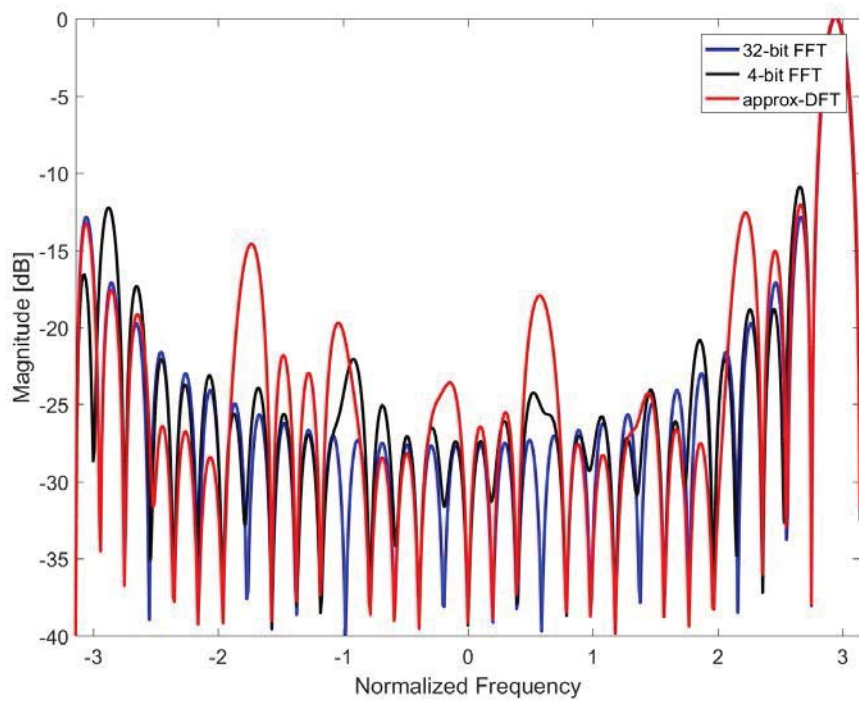


Figure 53: Output Comparison for Bin 18

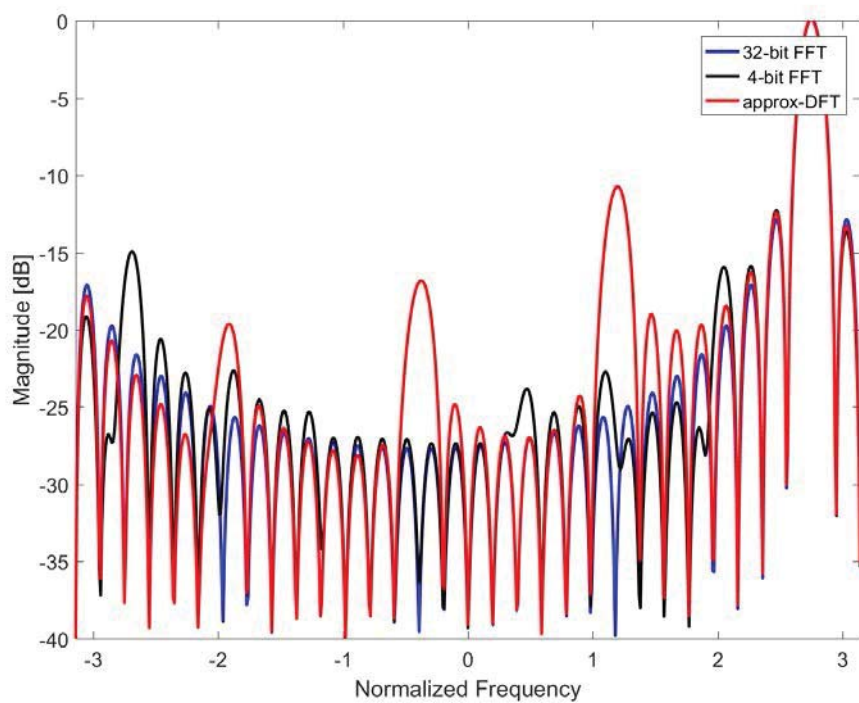


Figure 54: Output Comparison for Bin 19

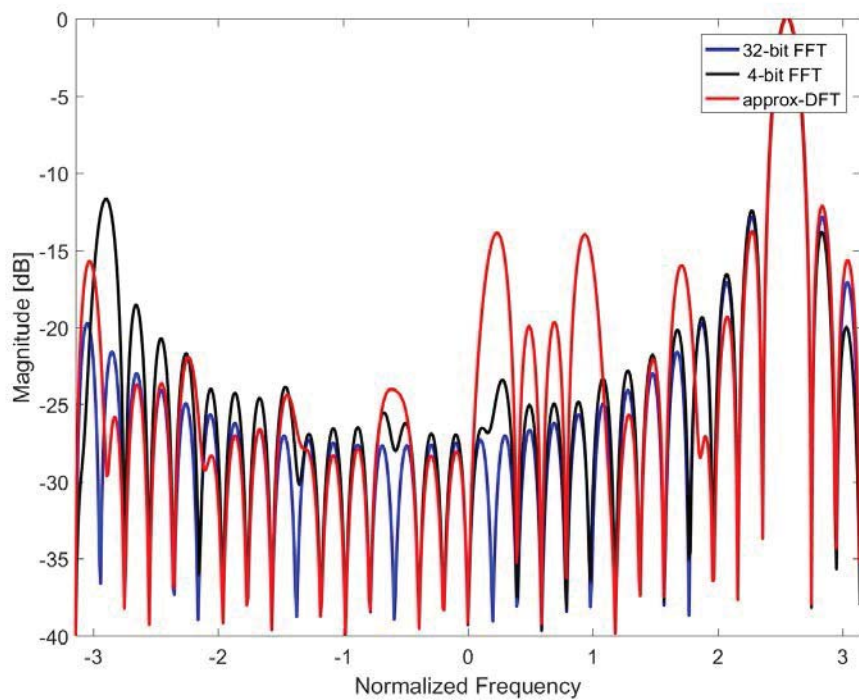


Figure 55: Output Comparison for Bin 20

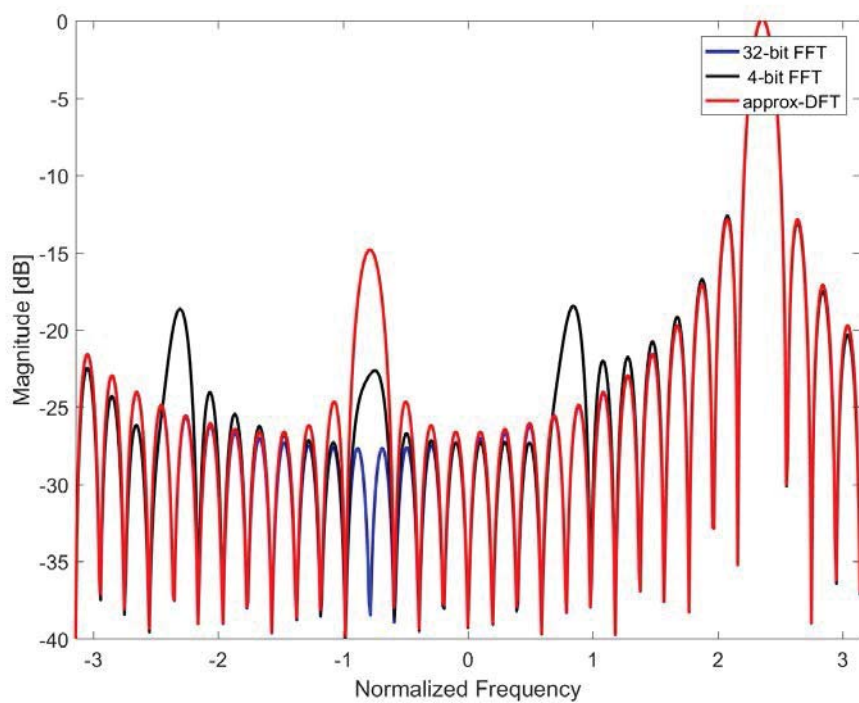


Figure 56: Output Comparison for Bin 21

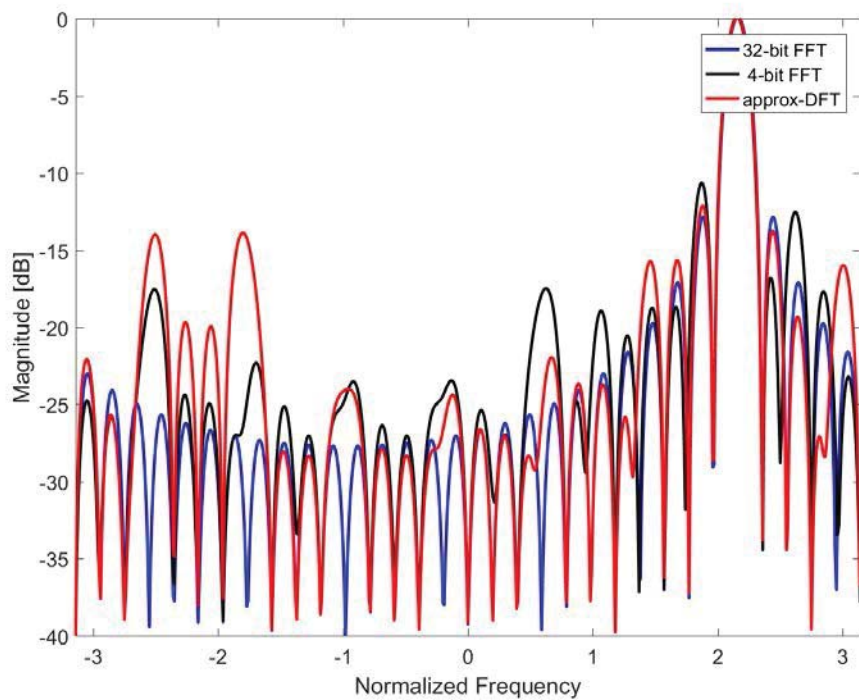


Figure 57: Output Comparison for Bin 22

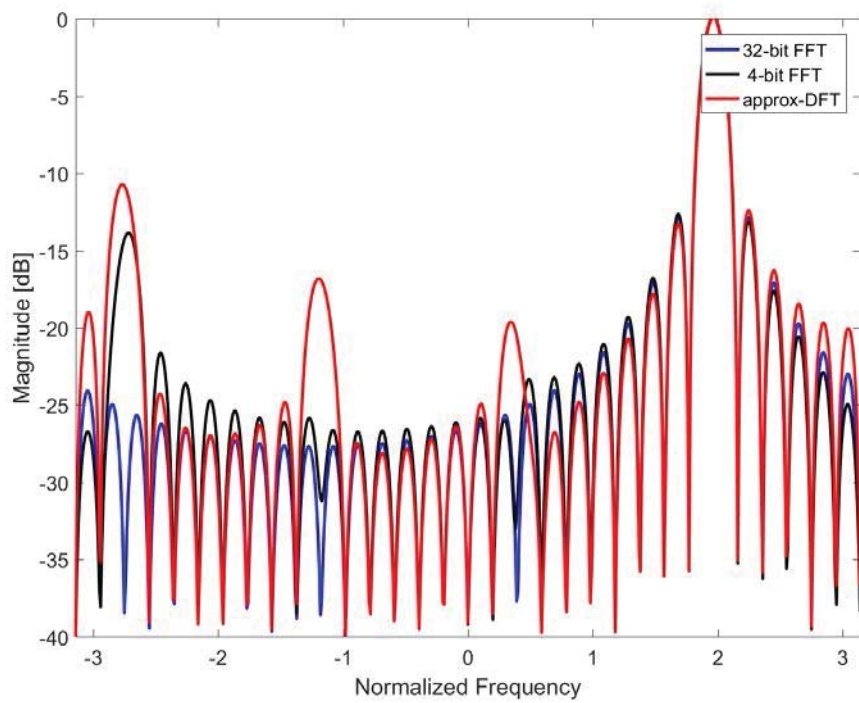


Figure 58: Output Comparison for Bin 23

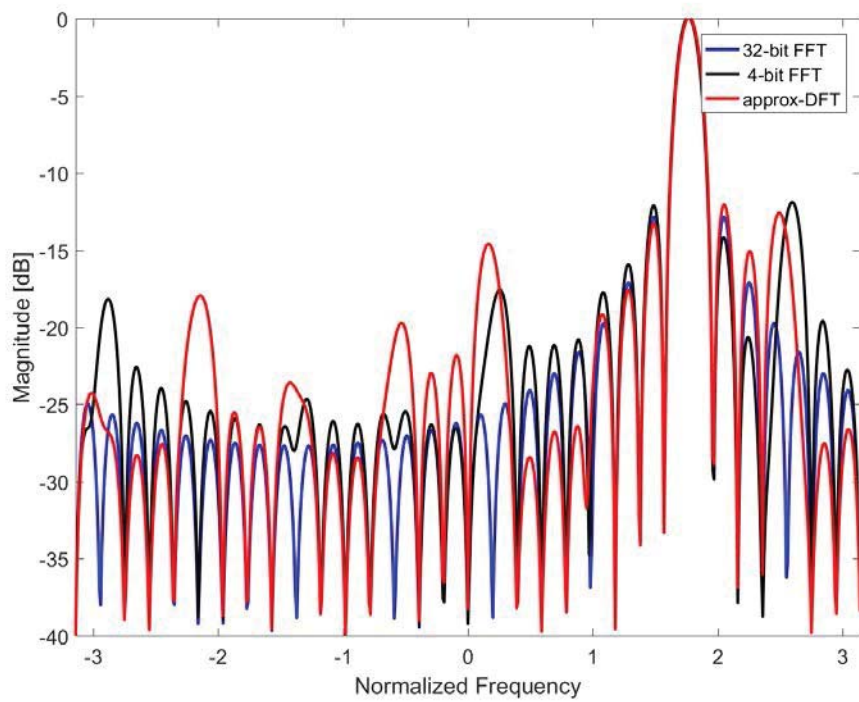


Figure 59: Output Comparison for Bin 24

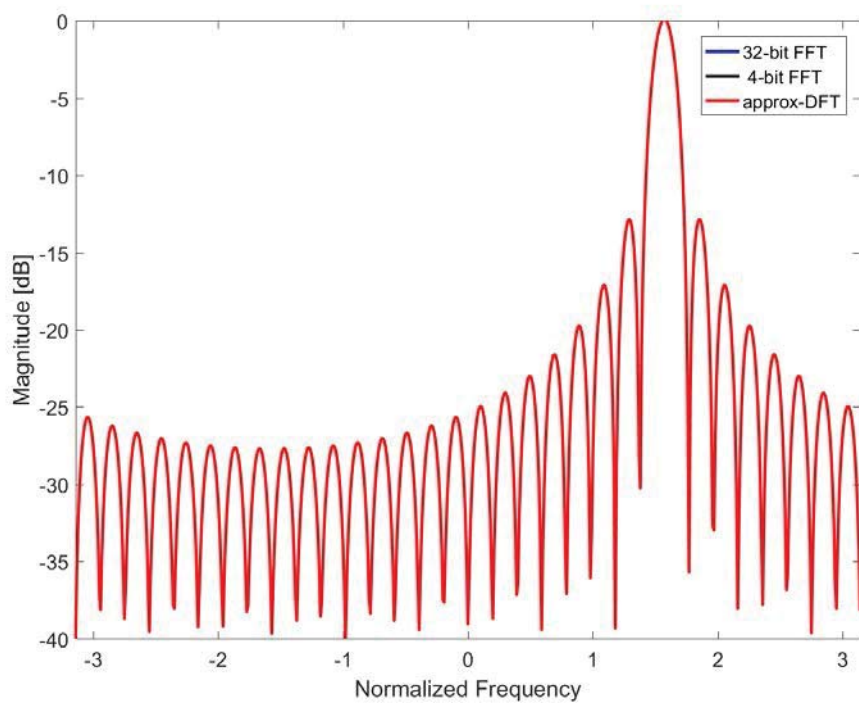


Figure 60: Output Comparison for Bin 25

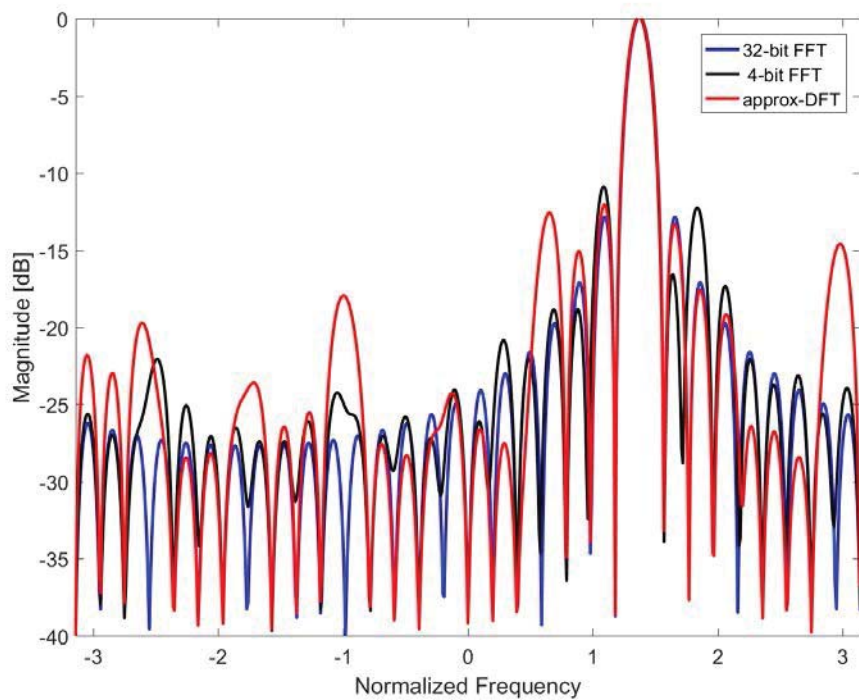


Figure 61: Output Comparison for Bin 26

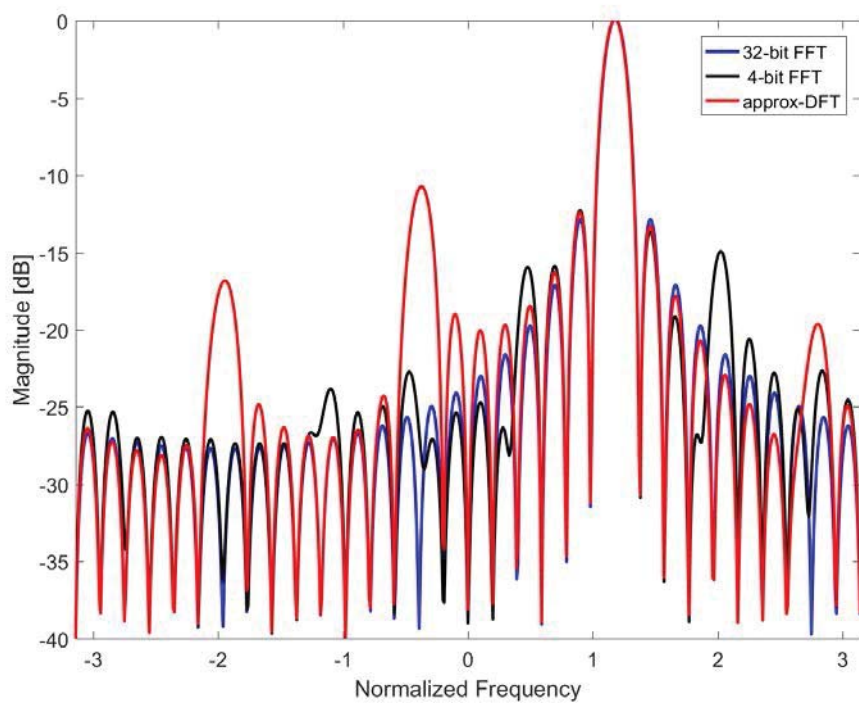


Figure 62: Output Comparison for Bin 27

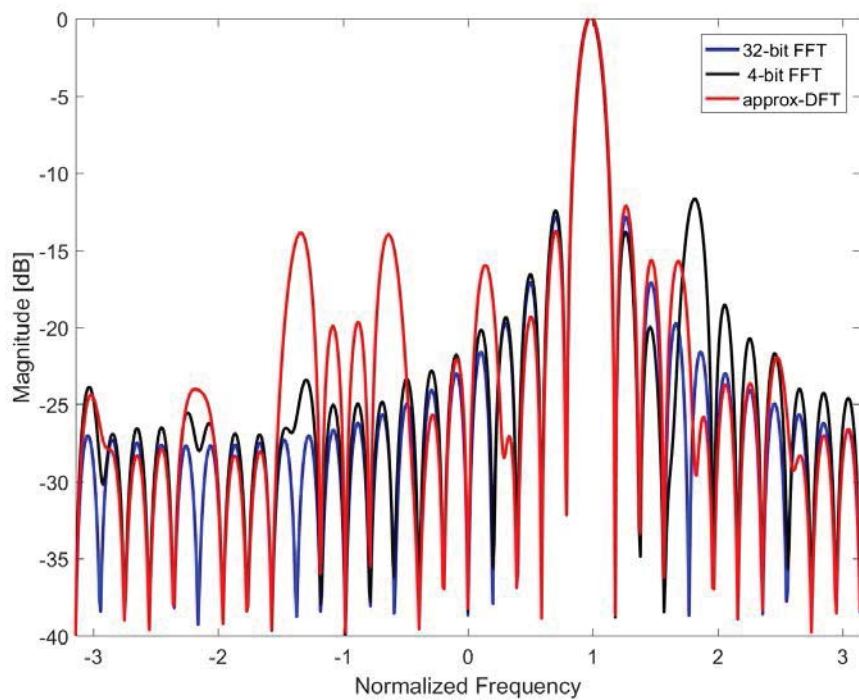


Figure 63: Output Comparison for Bin 28

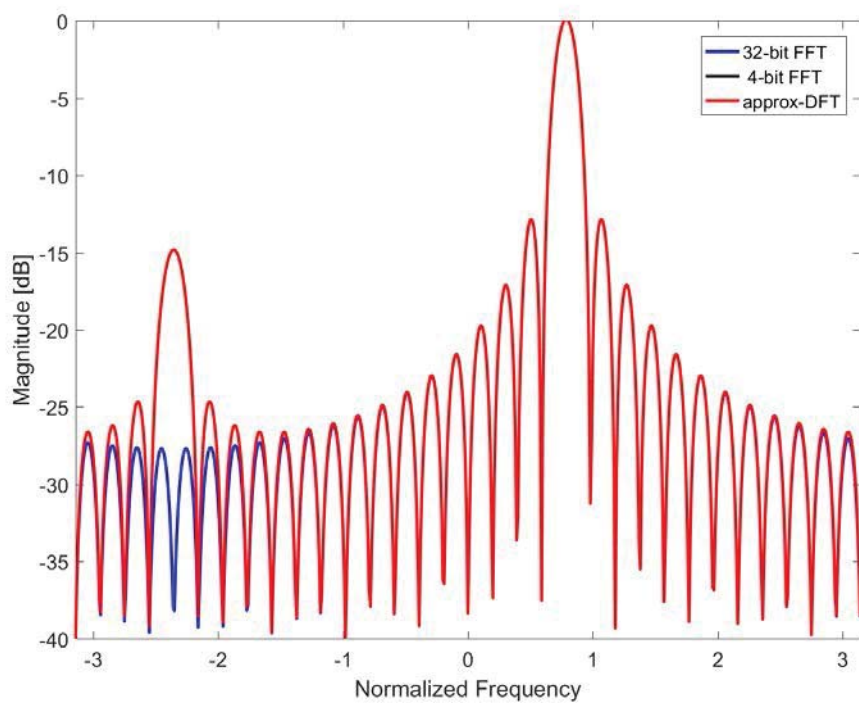


Figure 64: Output Comparison for Bin 29

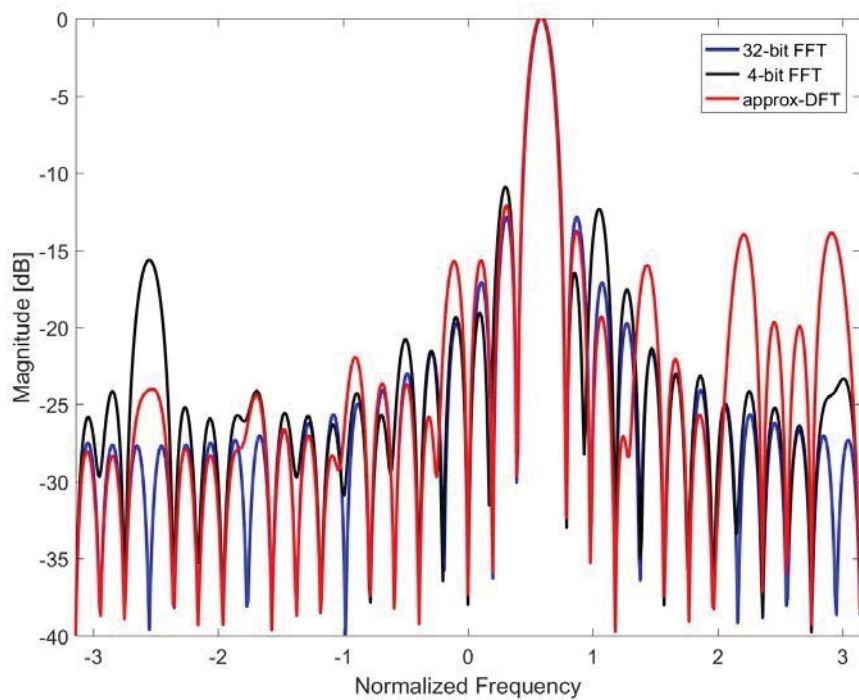


Figure 65: Output Comparison for Bin 30

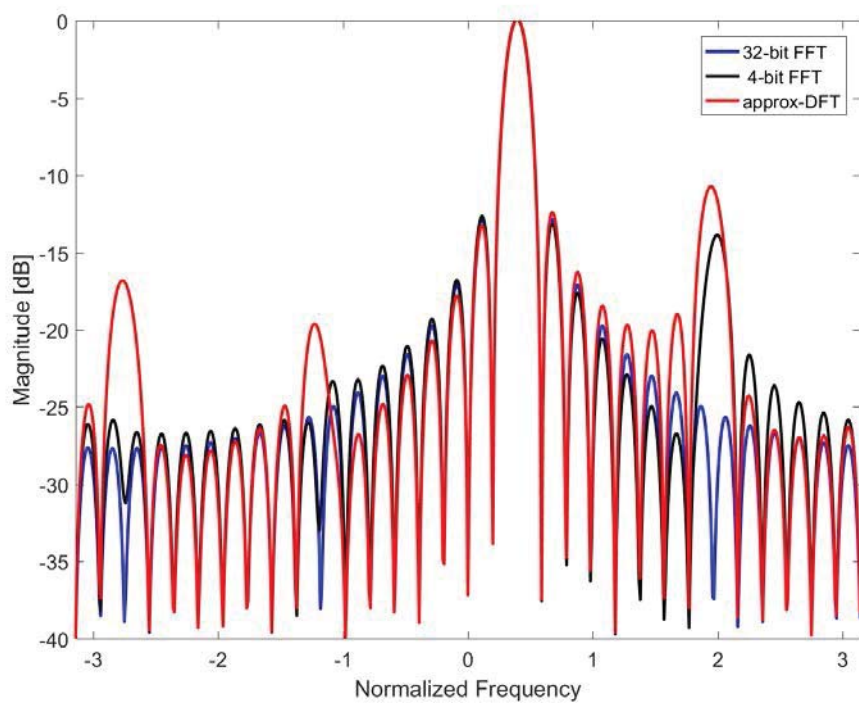


Figure 66: Output Comparison for Bin 31

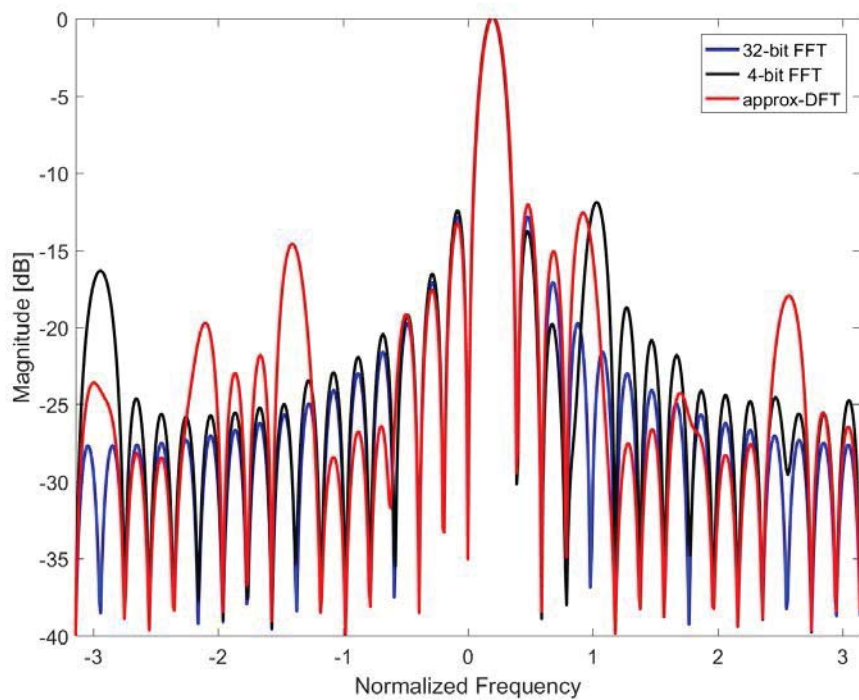


Figure 67: Output Comparison for Bin 32

3.4 64-point Approximate DFT Algorithm

Different candidate matrices for the 64-point approximate DFT were obtained based on the realization complexity and the closeness to the exact DFT (governed by a defined threshold parameter α). These matrices were analyzed to find the matrix that yields the lowest hardware realization complexity for which the performance is acceptable for beamforming applications.

The frequency responses of the filter bank beams for $\alpha = 1$ and 2 are shown in Figure 68. According to that the plots it can be seen that the matrix arising from $\alpha = 1$ which has the lowest complexity gives acceptable performance in beamforming. 64-point a-DFT matrix for $\alpha = 1$ ($\hat{\mathbf{F}}_{64}$) is given below. For convenience of representation we use the following notation to denote the matrix:

$$\hat{\mathbf{F}}_{64} = \begin{bmatrix} \mathbf{R}_{00} & \mathbf{R}_{01} \\ \mathbf{R}_{10} & \mathbf{R}_{11} \end{bmatrix} + j \begin{bmatrix} \mathbf{I}_{00} & \mathbf{I}_{01} \\ \mathbf{I}_{10} & \mathbf{I}_{11} \end{bmatrix}$$

[illegible]

$$\mathbf{I}_{00} =$$

$$I_{10} =$$

$\hat{\mathbf{F}}_{64}$ can be factorized to reduce the adder complexity. $\hat{\mathbf{F}}_{64}$ has been factorized into 12 stages, which can be denoted as

$$\hat{\mathbf{F}}_{64} = W_{12}W_{11}W_{10}W_9W_8W_7W_6W_5W_4W_3W_2W_1,$$

where, W_i ($i = 1, 2, \dots, 12$) denotes a sparse matrix. W_i s are shown below.

Following notation is used to denote the factorized matrices.

$$\mathbf{W}_i = \begin{bmatrix} \mathbf{R}_i^{00} & \mathbf{R}_i^{01} \\ \mathbf{R}_i^{10} & \mathbf{R}_{11} \end{bmatrix} + j \begin{bmatrix} \mathbf{I}_i^{00} & \mathbf{I}_i^{01} \\ \mathbf{I}_i^{10} & \mathbf{I}_i^{11} \end{bmatrix} \quad \text{where } i = 1, 2, \dots, 12.$$

Note that $W_1, W_3, W_5, W_7, W_9, W_{11}$ and W_{12} are real matrices.

[illegible]

$$\mathbf{R}_1^{10} =$$

$$R_1^{01} =$$

$$\mathbf{R}_1^{11} =$$

$$R_2^{00} =$$

$$\mathbf{R}_2^{10} =$$

$$R_2^{01} =$$

[illegible]

$$\mathbf{I}_2^{00} =$$

$$\mathbf{I}_2^{10} =$$

$$\mathbf{I}_2^{01} =$$

$$\mathbf{I}_2^{11} =$$

$$\mathbf{R}_3^{00} =$$

$$\mathbf{R}_3^{10} =$$

$$\mathbf{R}_3^{01} =$$

$$\mathbf{R}_2^{11} =$$

[illegible]

$$\mathbf{R}_4^{10} = \begin{bmatrix}$$

[illegible]

$$R_4^{11} =$$

$$\mathbf{I}_4^{\text{OO}} =$$

$$I_4^{10} =$$

$$I_4^{01} =$$

$$\mathbf{I}_4^{11} =$$

$$\mathbf{R}_5^{00} =$$

[illegible]

75

[illegible]

[illegible]

[illegible]

[illegible]

$$R_6^{01} =$$

$$\mathbf{R}_6^{11} =$$

$$\mathbf{I}_6^{00} =$$

$$\mathbf{I}_6^{10} =$$

$$\mathbf{I}_6^{01} =$$

$$\mathbf{I}_6^{11} =$$

$$\mathbf{R}_7^{00} =$$

$$\mathbf{R}_7^{10} =$$

$$R_7^{01} =$$

[illegible]

Approved for public release; distribution is unlimited.

$$R_8^{01} =$$

$$\mathbf{R}_g^{11} =$$

$$\mathbf{I}_8^{00} =$$

[illegible]

83

$$\mathbf{R}_g^{00} =$$

$$\mathbf{R}_q^{10} =$$

$$R_9^{01} =$$

$$\mathbf{R}_9^{11} =$$

$$\mathbf{R}_{10}^{00} =$$

$$\mathbf{R}_{10}^{10} =$$

$$R_{10}^{01} =$$

$$\mathbf{R}_{10}^{11} =$$

$$\mathbf{I}_{10}^{00} =$$

[illegible]

87

$$\mathbf{R}_{11}^{00} =$$

$$\mathbf{R}_{11}^{10} =$$

$$R_{11}^{01} =$$

$$\mathbf{R}_{11}^{11} =$$

$$\mathbf{R}_{12}^{00} =$$

$$\mathbf{R}_{12}^{10} =$$

$$R_{12}^{01} =$$

$$\mathbf{R}_{12}^{11} =$$

Frequency Responses and Errors

Figure 68 (a) and (b) show the Matlab simulated beams using the obtained approximate matrices for $\alpha = 1$ and 2. Figure 68 (c) shows the beams corresponding to the exact DFT.

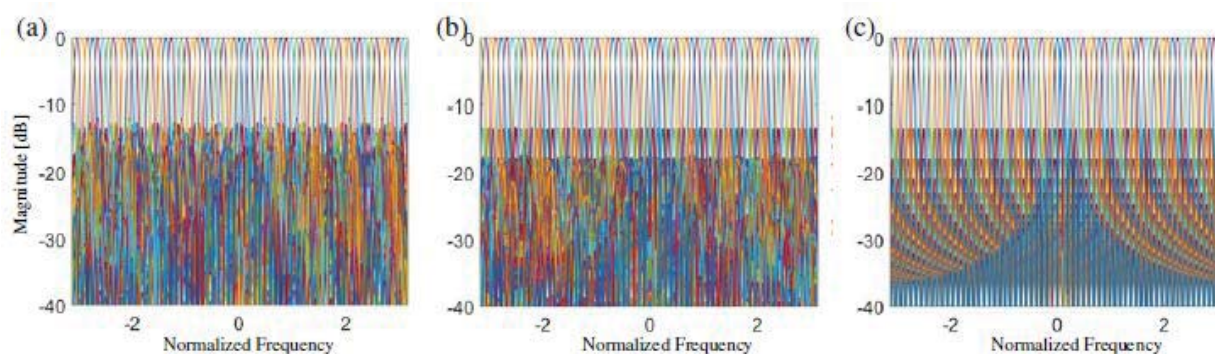


Figure 68: Simulated Beams (a) $\alpha = 1$, (b) $\alpha = 2$, and (c) exact 64-point DFT

Figure 69 (a) shows the simulated 64-point a-DFT beams and (b) shows the corresponding beams for using the exact DFT. Figure (c) depicts the error between the magnitude responses.

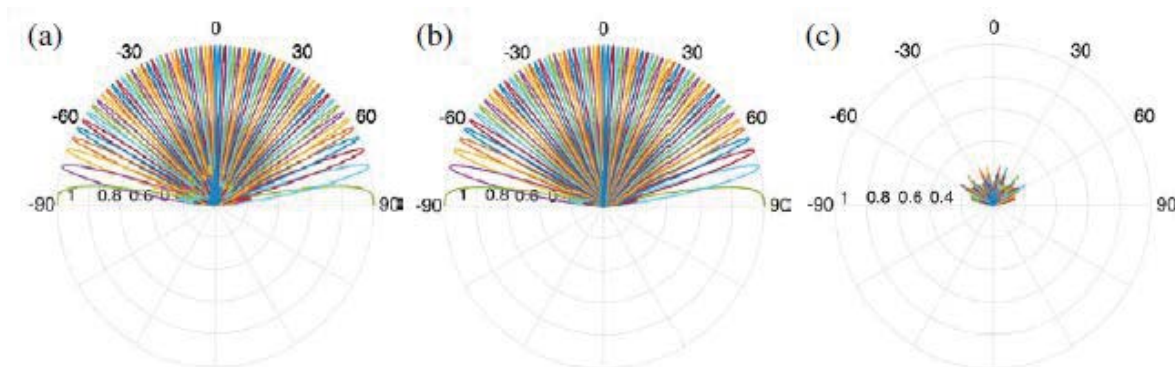


Figure 69: (a) Simulated a-DFT Beams, (b) Corresponding Exact DFT Beams, and (c) Error between Magnitude Responses

The beam outputs pertaining to all the bins of 64-point a-DFT are shown below.

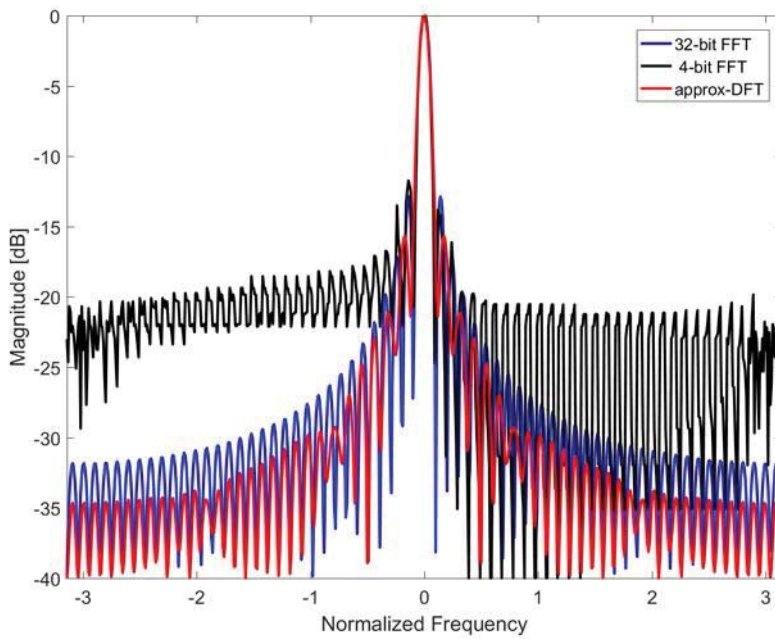


Figure 70: Output Comparison for Bin 1

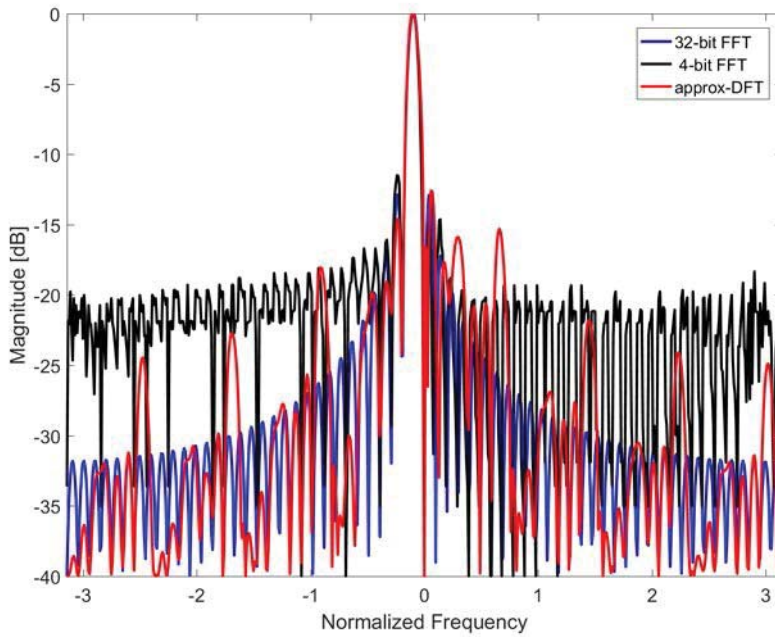


Figure 71: Output Comparison for Bin 2

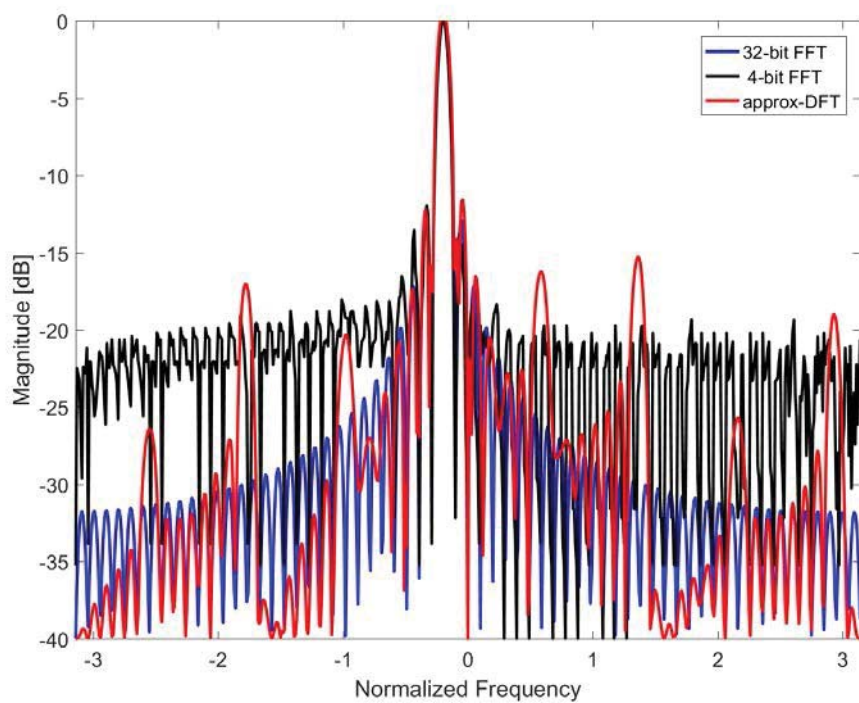


Figure 72: Output Comparison for Bin 3

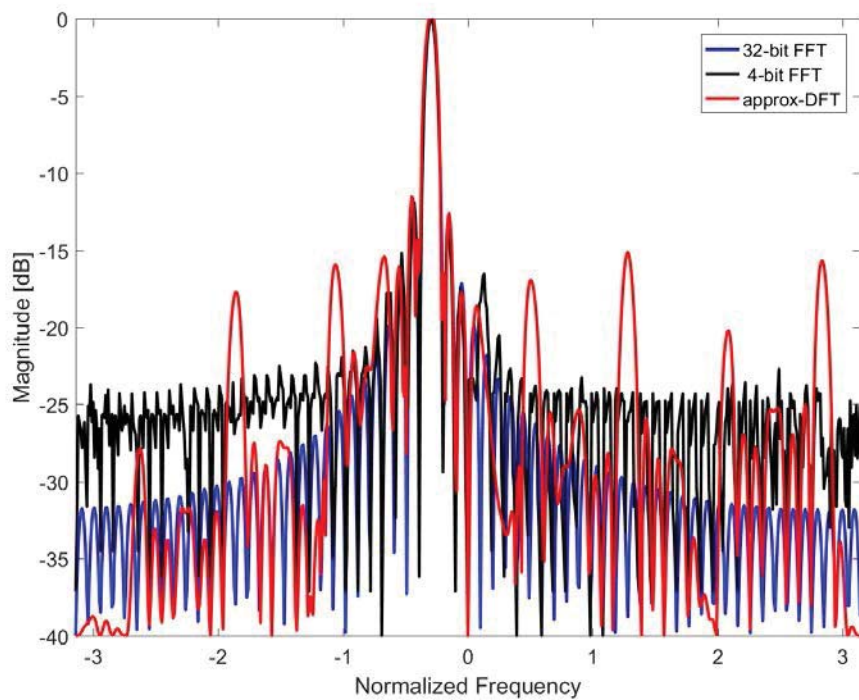


Figure 73: Output Comparison for Bin 4

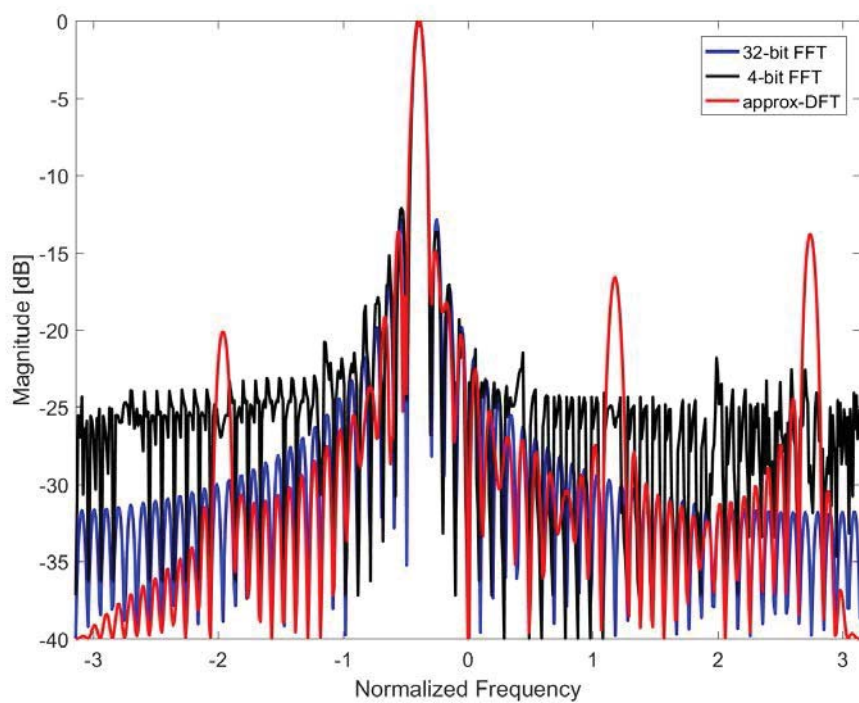


Figure 74: Output Comparison for Bin 5

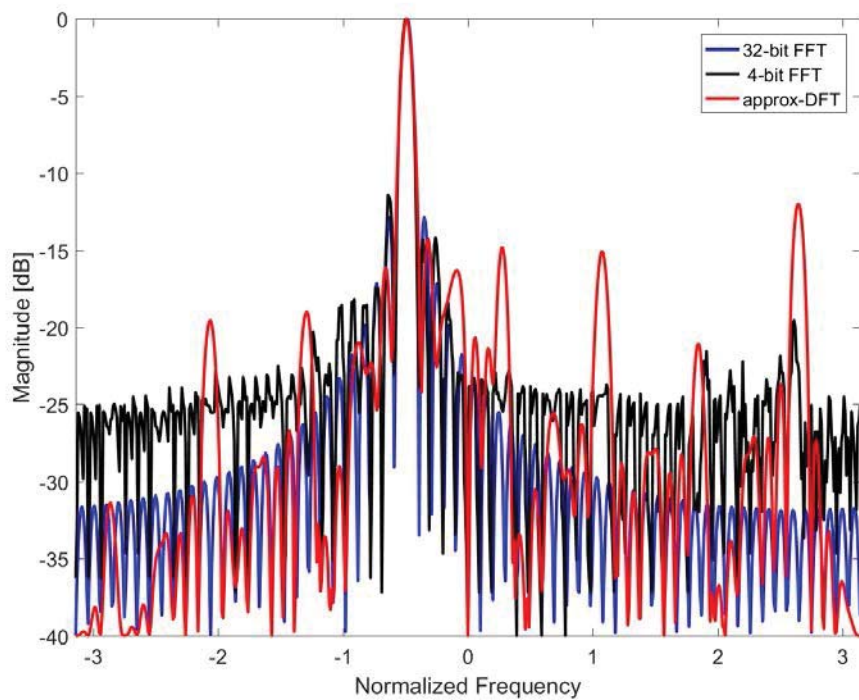


Figure 75: Output Comparison for Bin 6

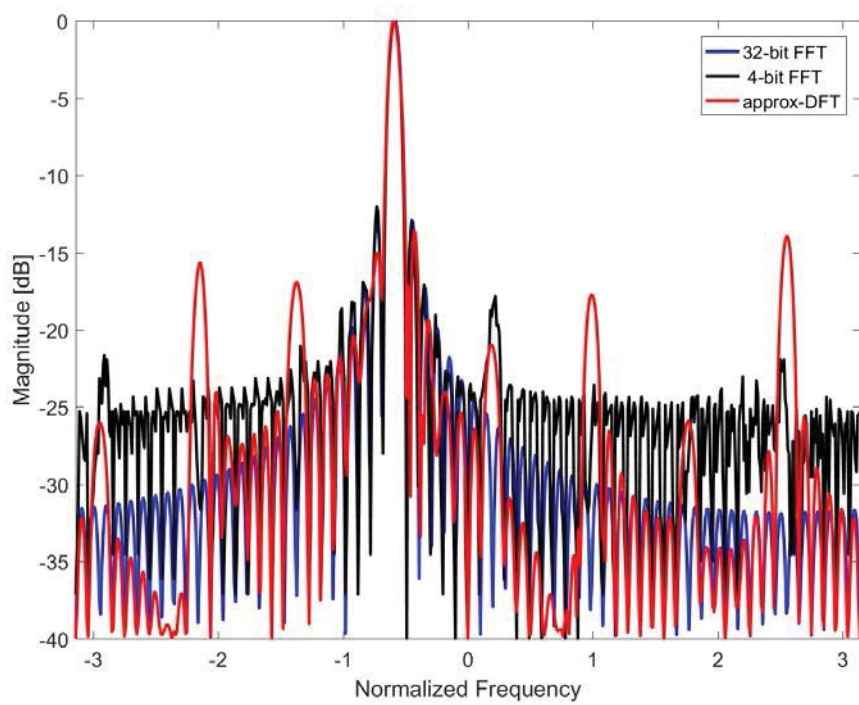


Figure 76: Output Comparison for Bin 7

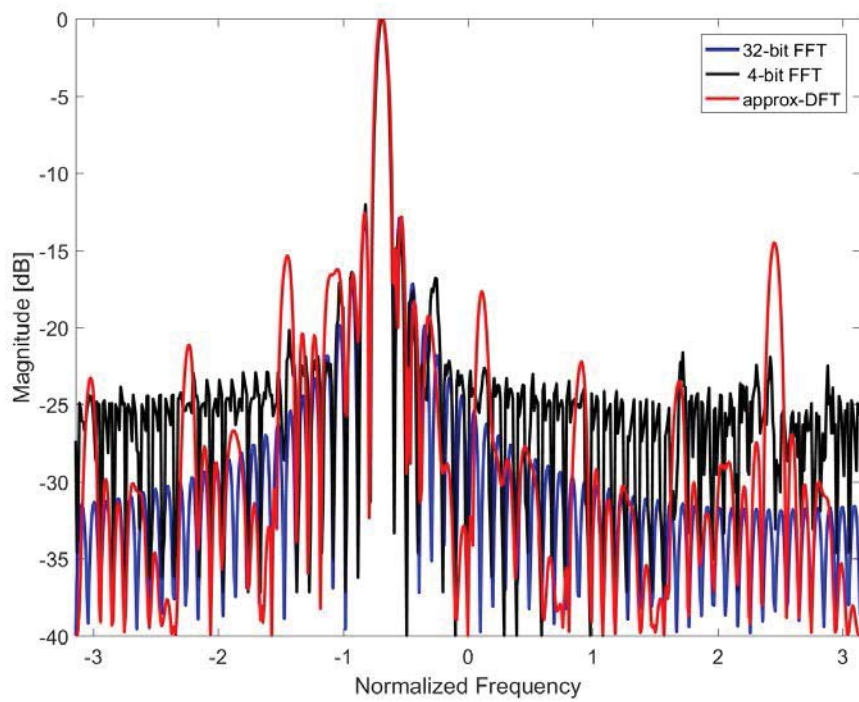


Figure 77: Output Comparison for Bin 8

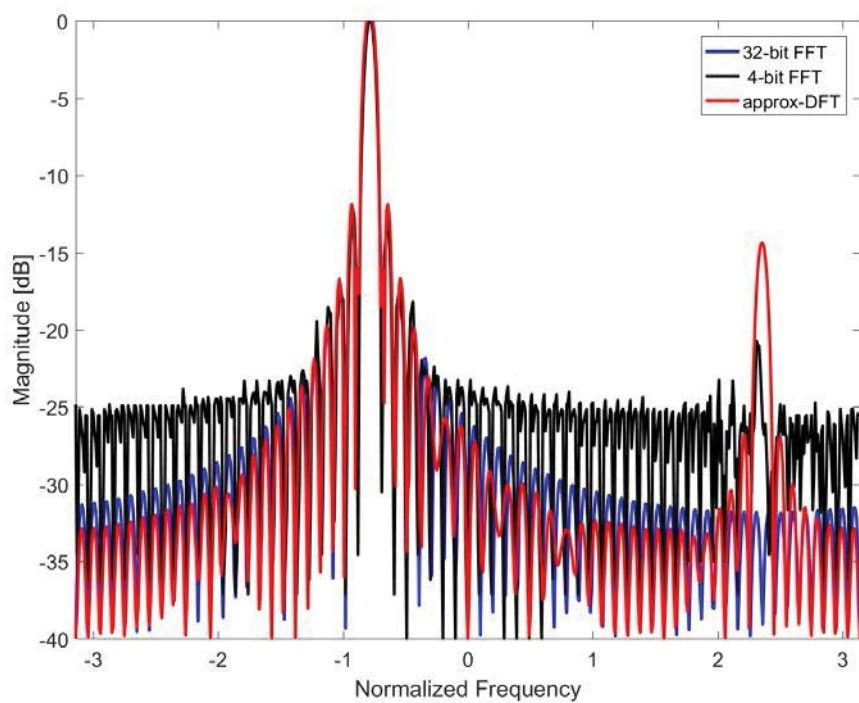


Figure 78: Output Comparison for Bin 9

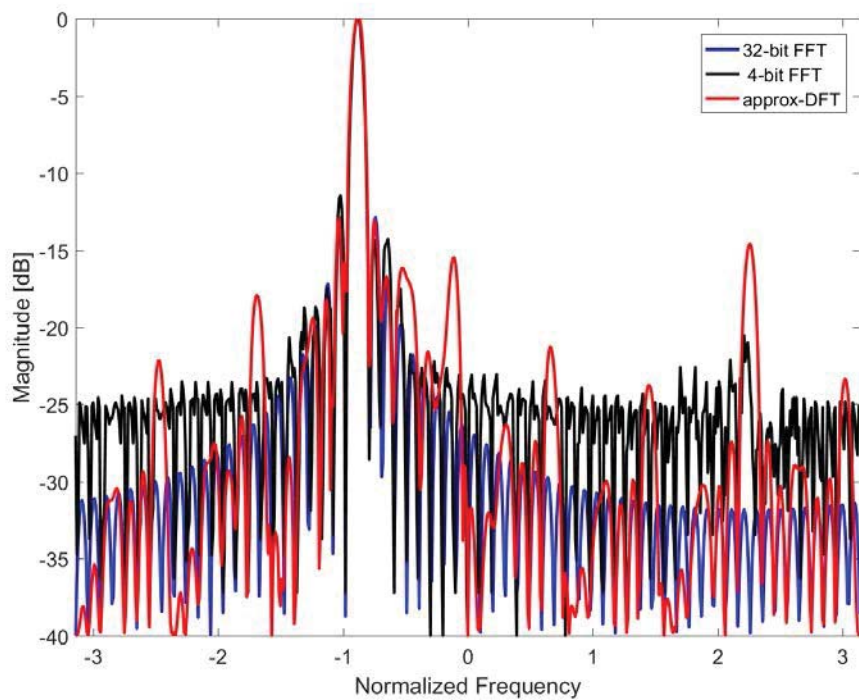


Figure 79: Output Comparison for Bin 10

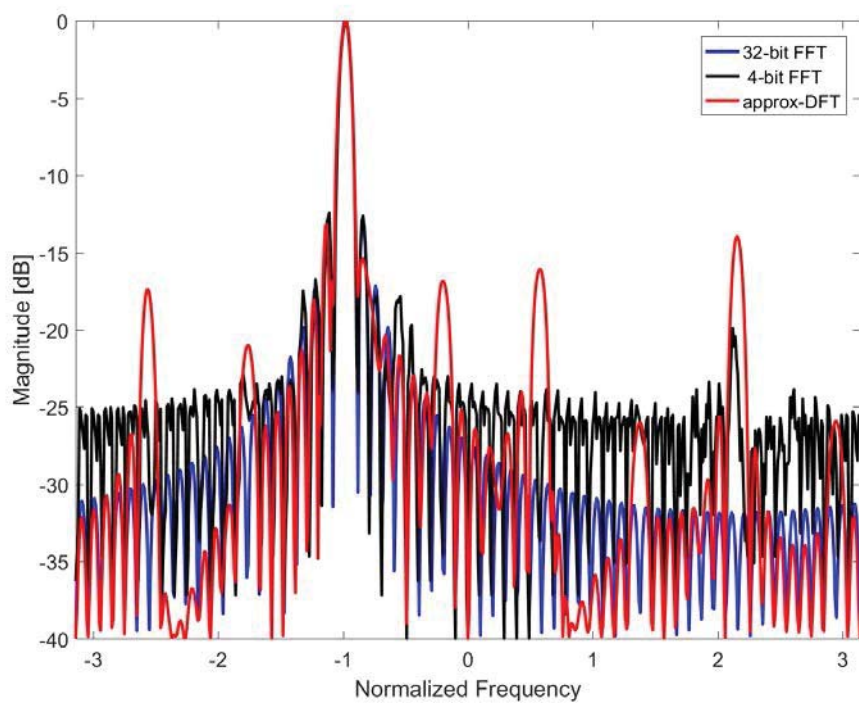


Figure 80: Output Comparison for Bin 11

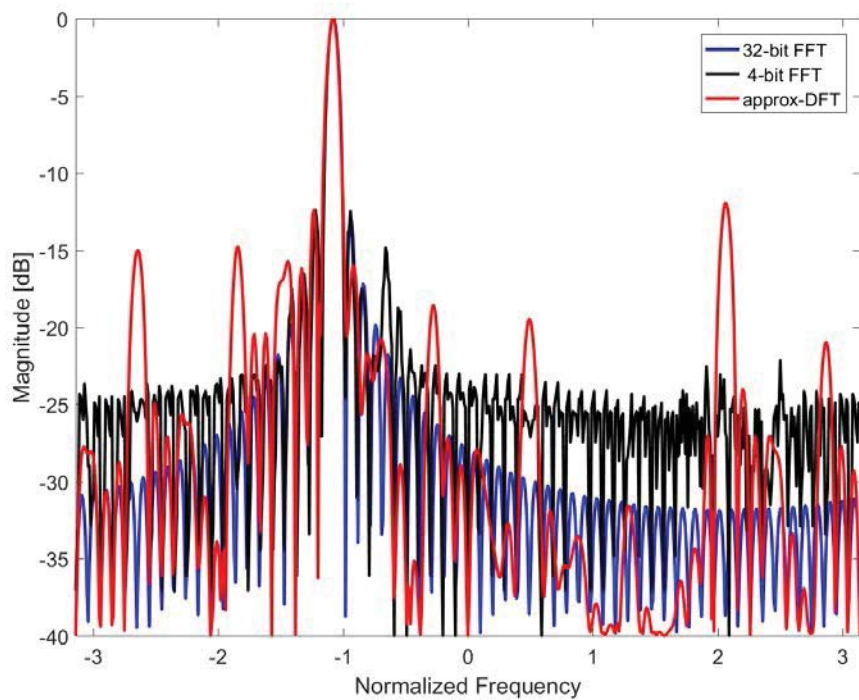


Figure 81: Output Comparison for Bin 12

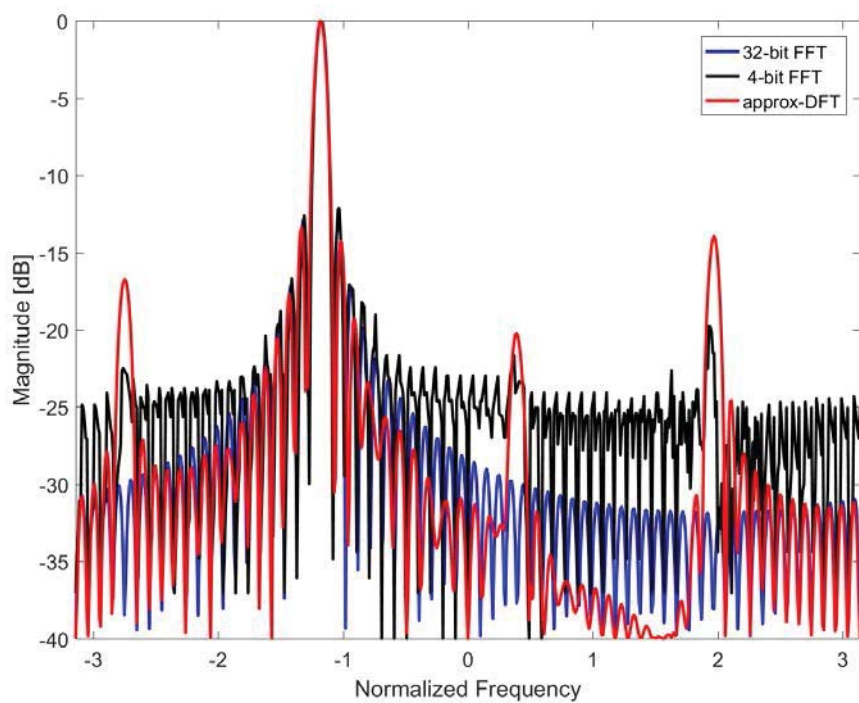


Figure 82: Output Comparison for Bin 13

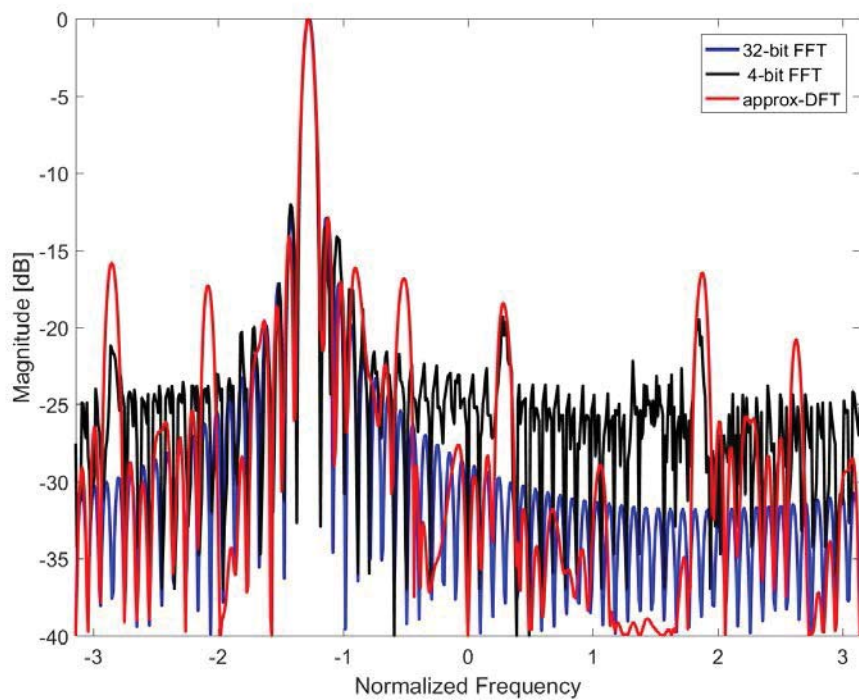


Figure 83: Output Comparison for Bin 14

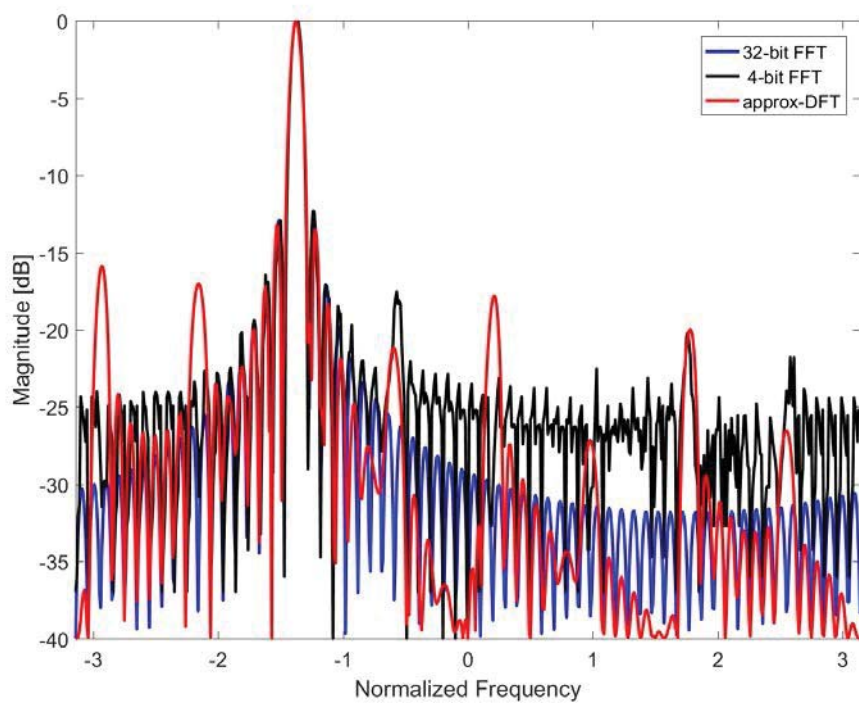


Figure 84: Output Comparison for Bin 15

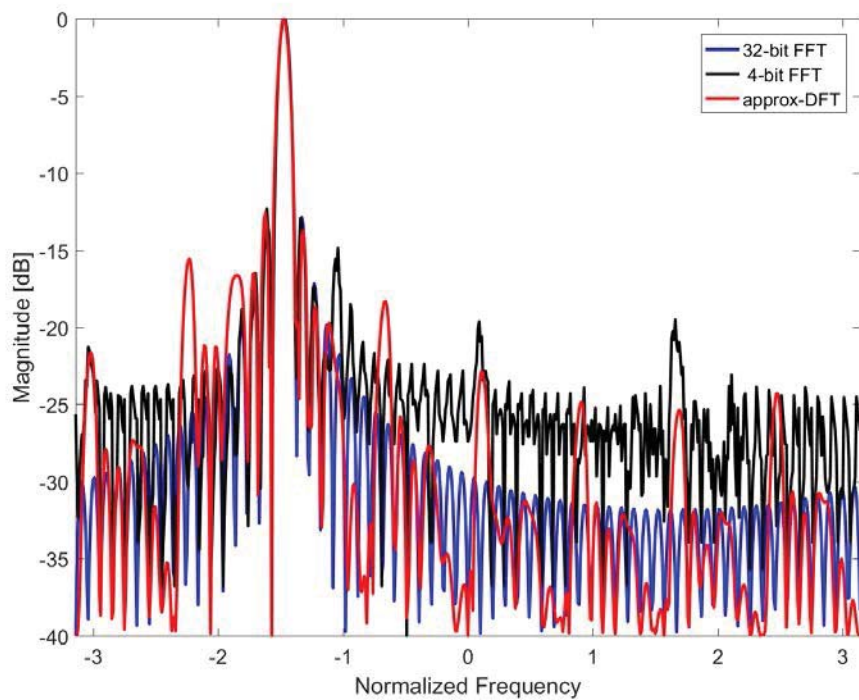


Figure 85: Output Comparison for Bin 16

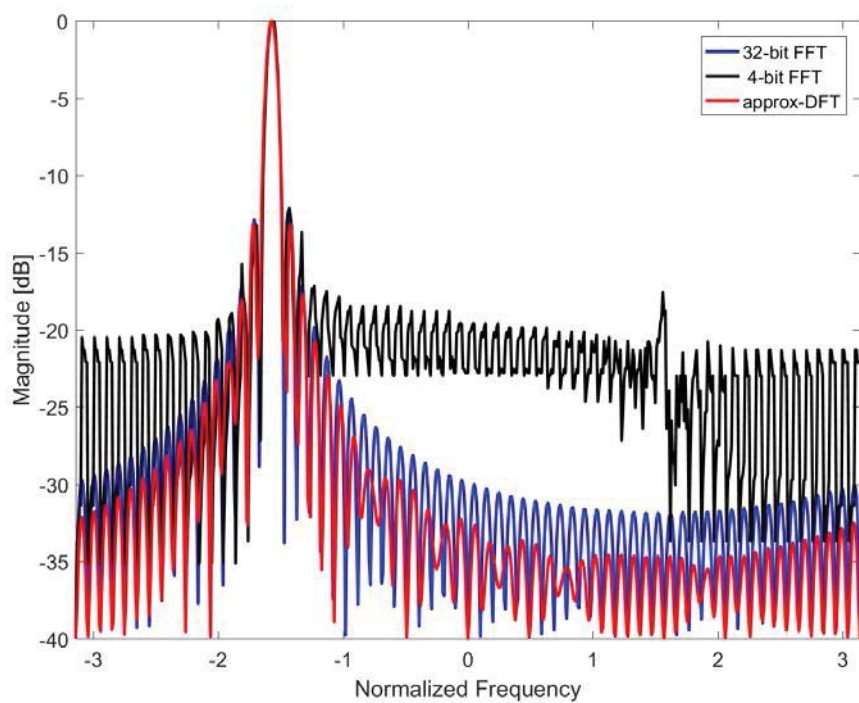


Figure 86: Output Comparison for Bin 17

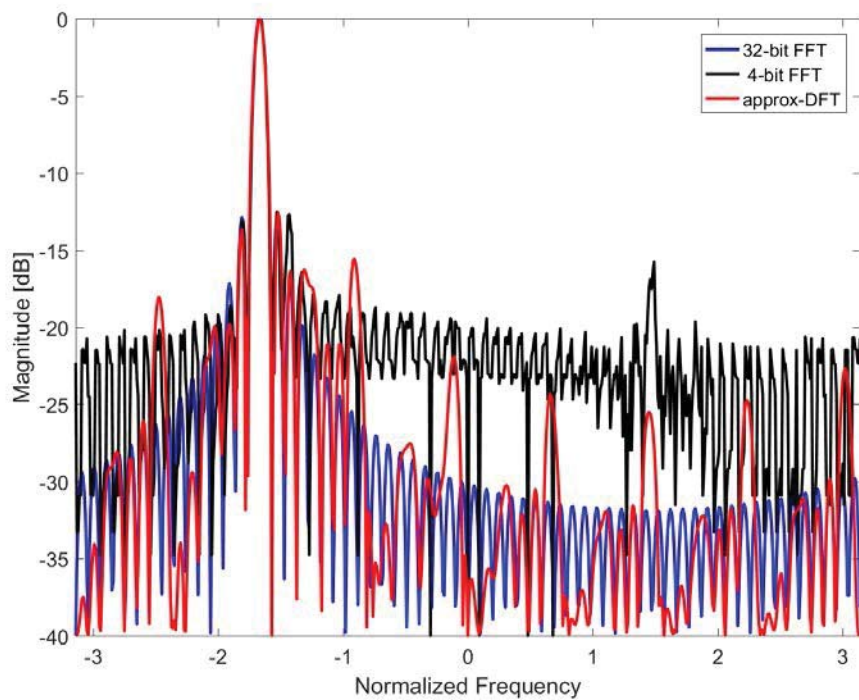


Figure 87: Output Comparison for Bin 18

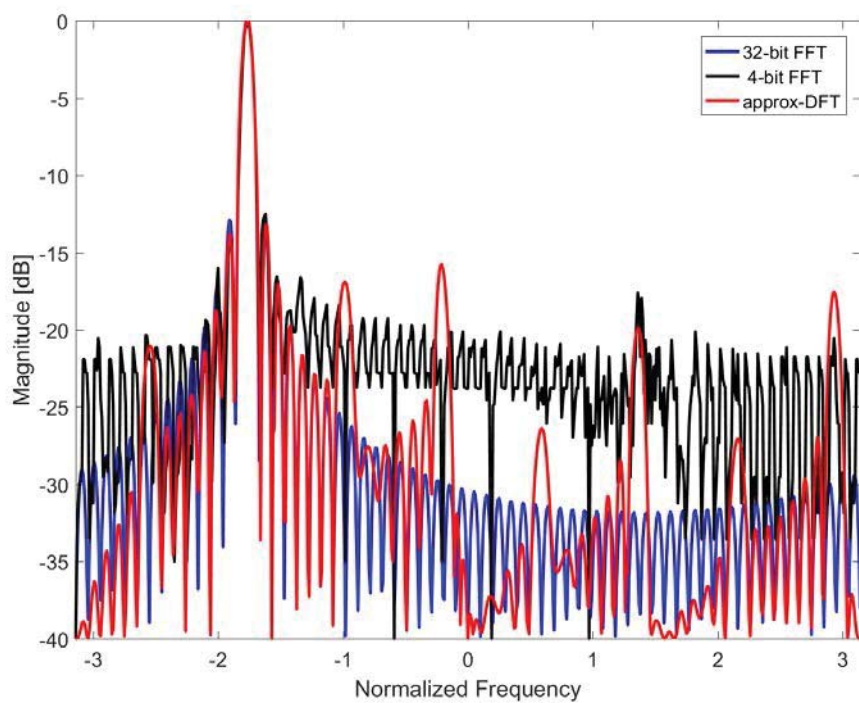


Figure 88: Output Comparison for Bin 19

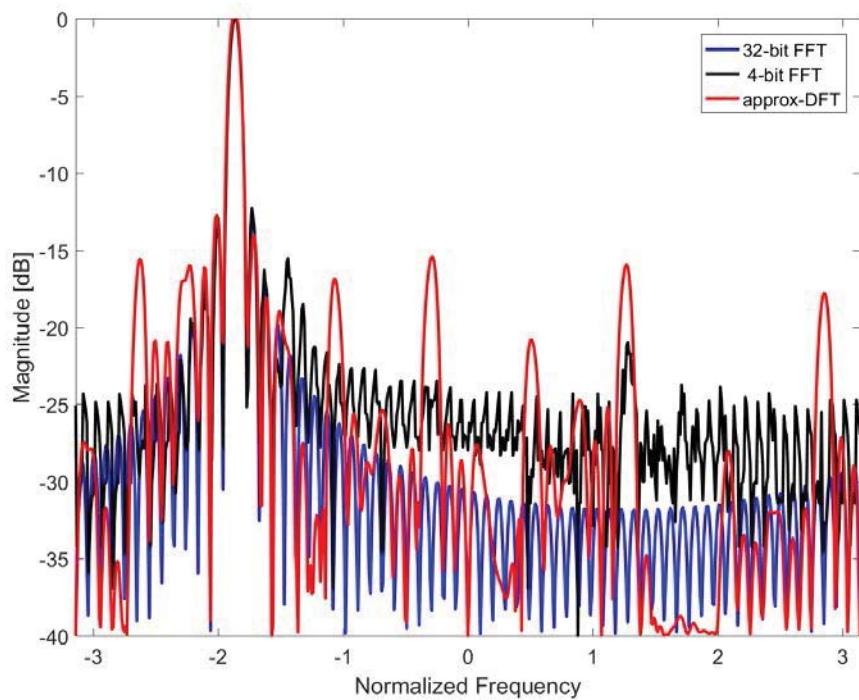


Figure 89: Output Comparison for Bin 20

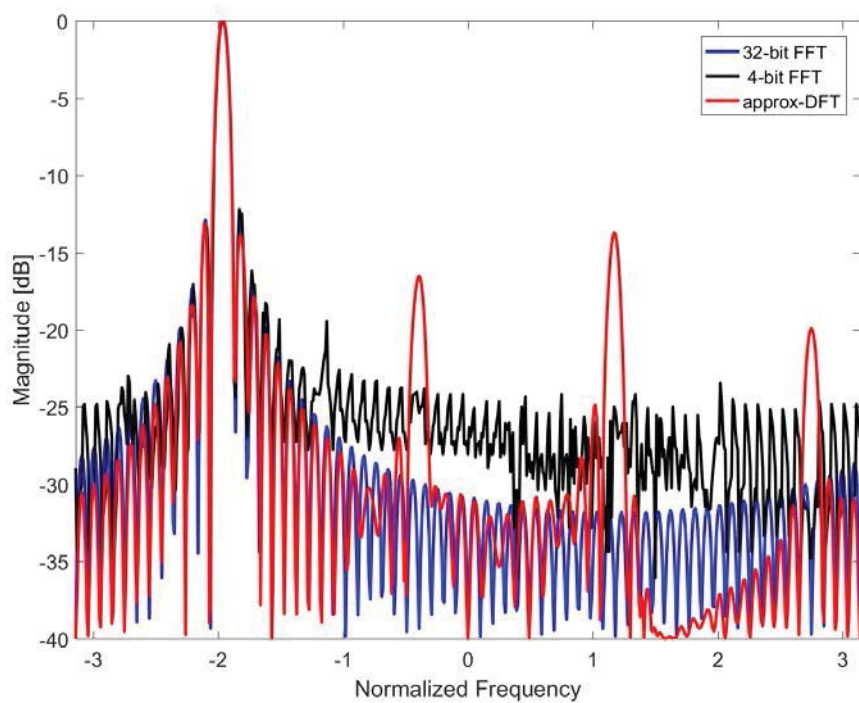


Figure 90: Output Comparison for Bin 21

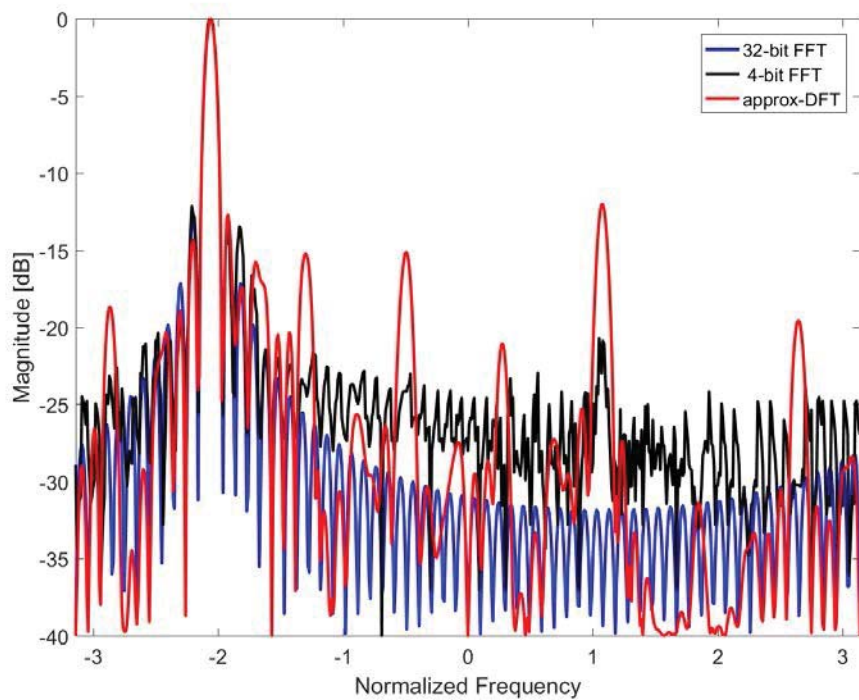


Figure 91: Output Comparison for Bin 22

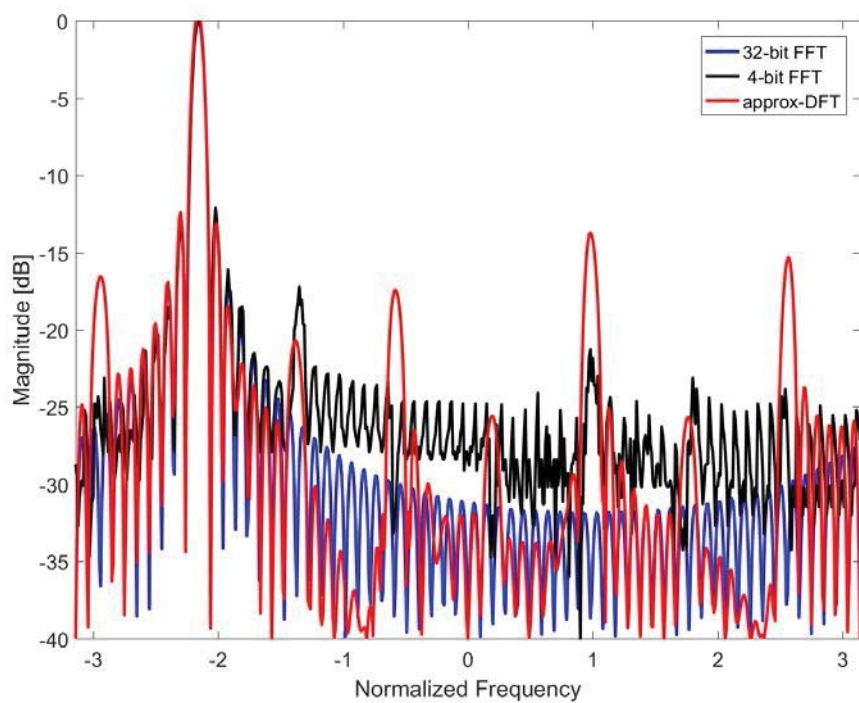


Figure 92: Output Comparison for Bin 23

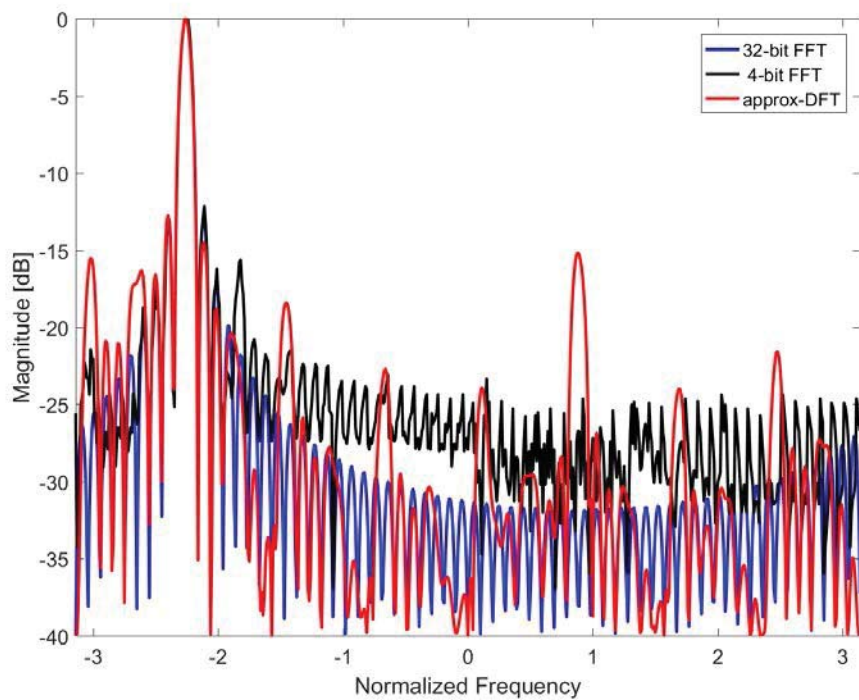


Figure 93: Output Comparison for Bin 24

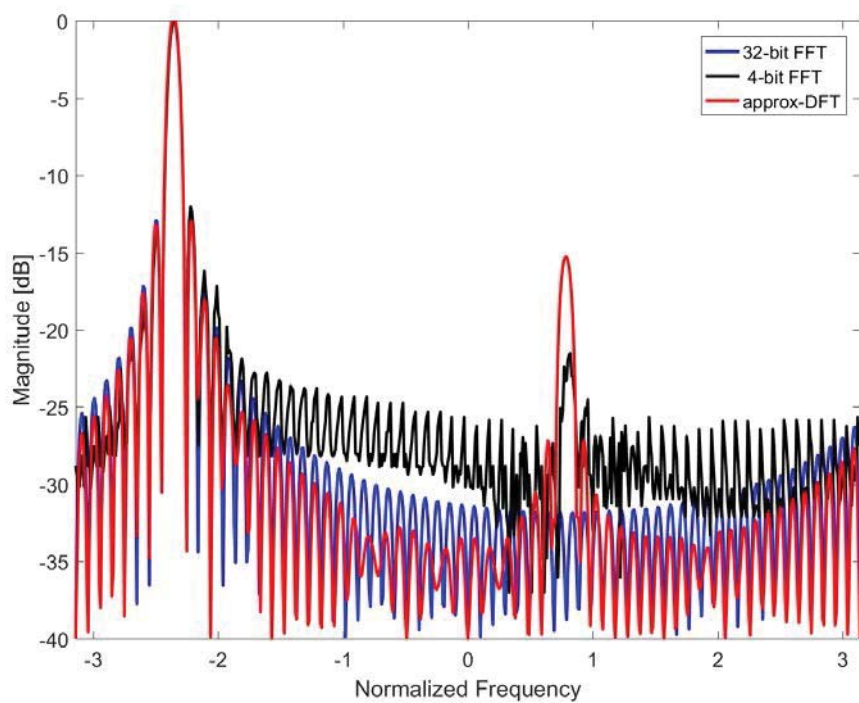


Figure 94: Output Comparison for Bin 25

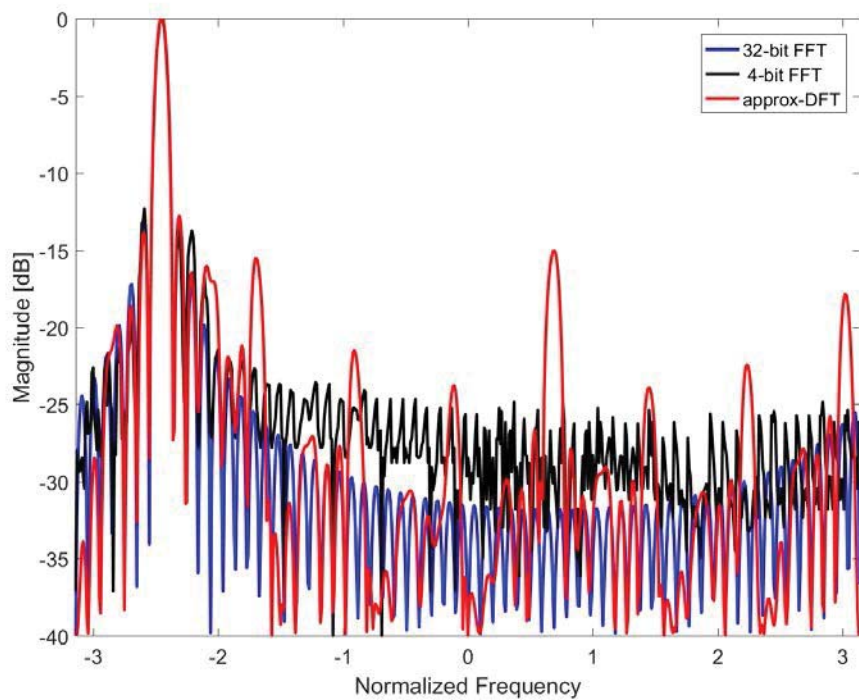


Figure 95: Output Comparison for Bin 26

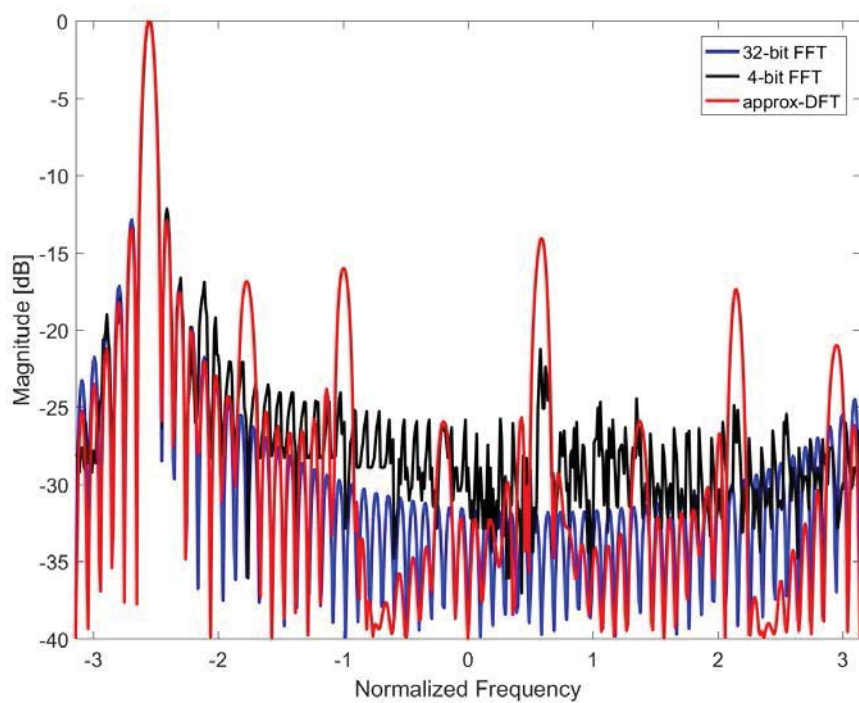


Figure 96: Output Comparison for Bin 27

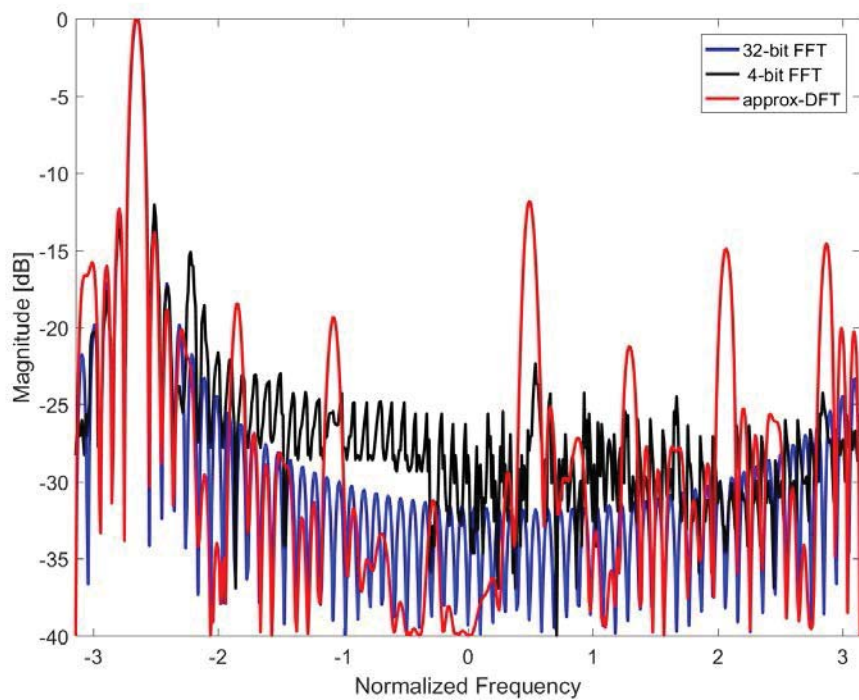


Figure 97: Output Comparison for Bin 28

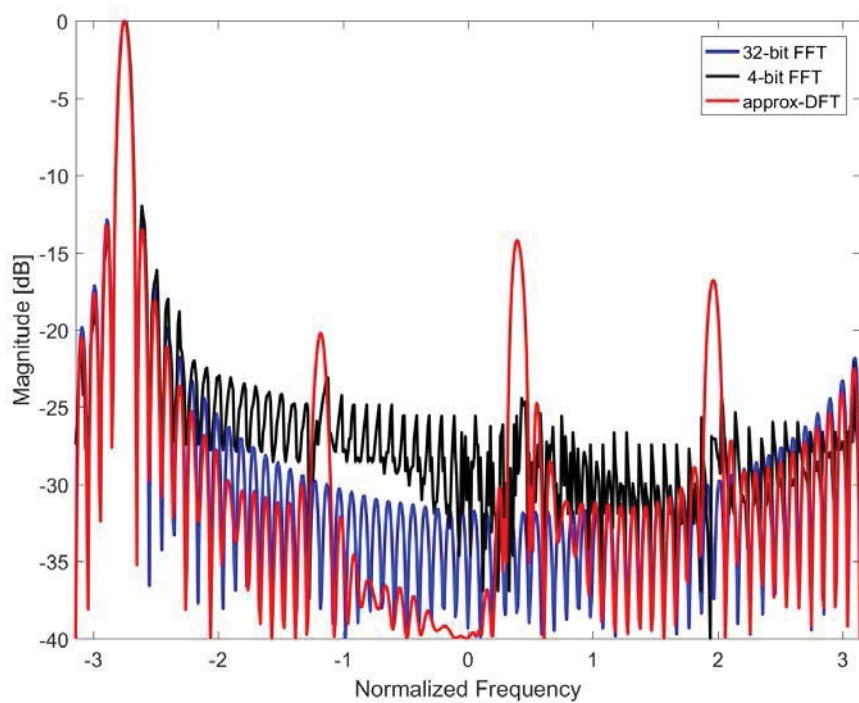


Figure 98: Output Comparison for Bin 29

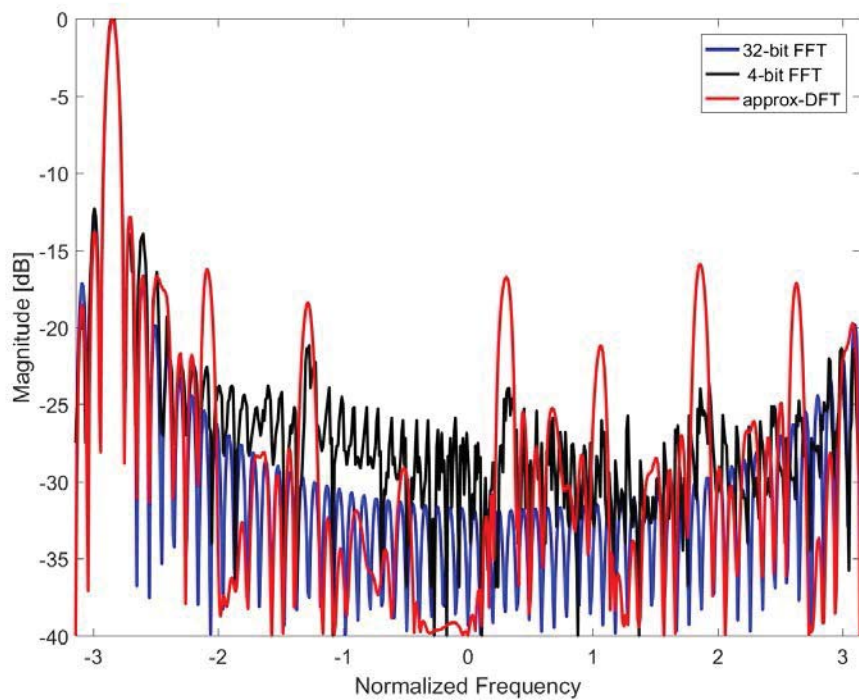


Figure 99: Output Comparison for Bin 30

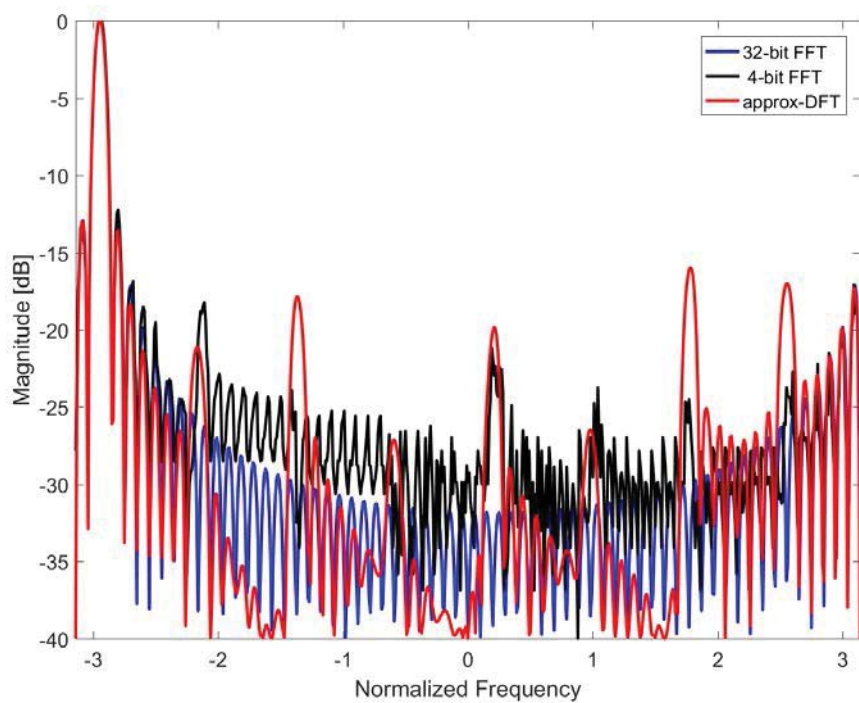


Figure 100: Output Comparison for Bin 31

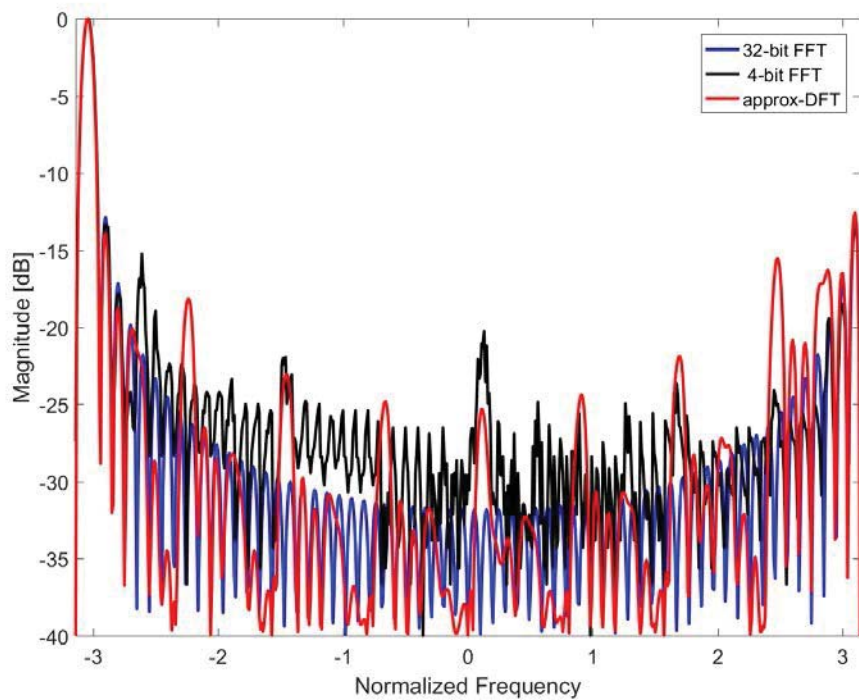


Figure 101: Output Comparison for Bin 32

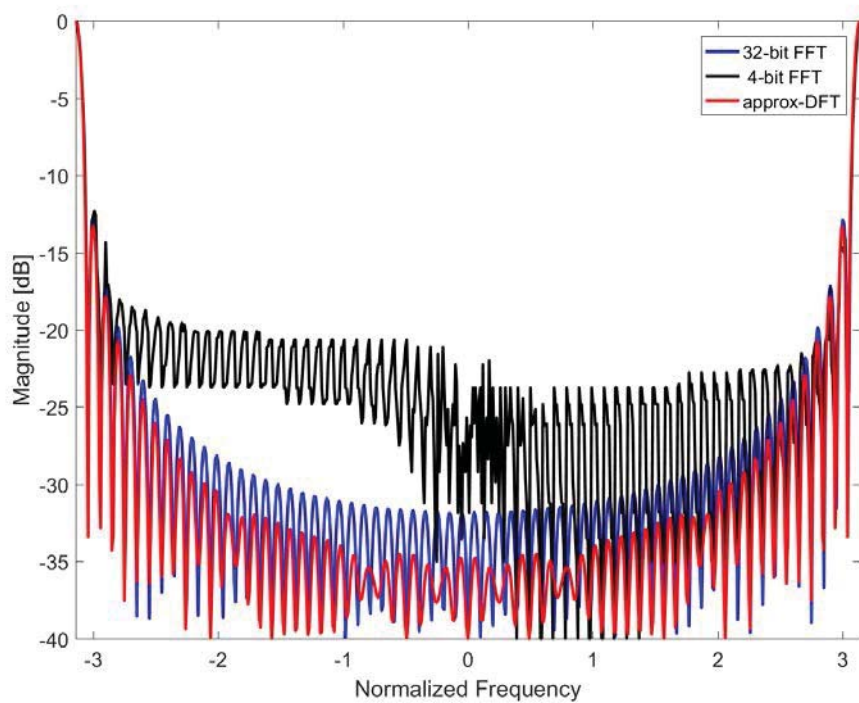


Figure 102: Output Comparison for Bin 33

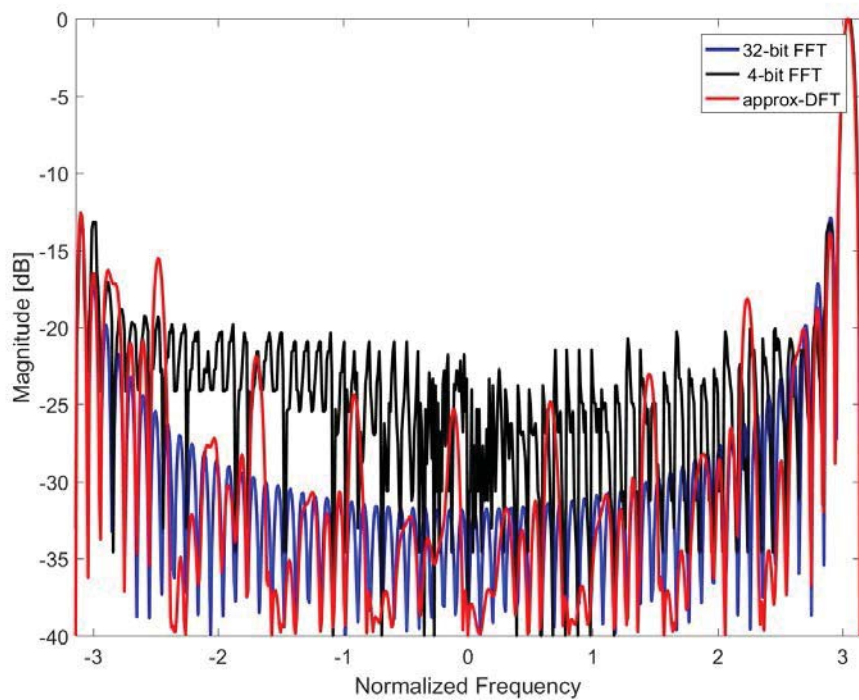


Figure 103: Output Comparison for Bin 34

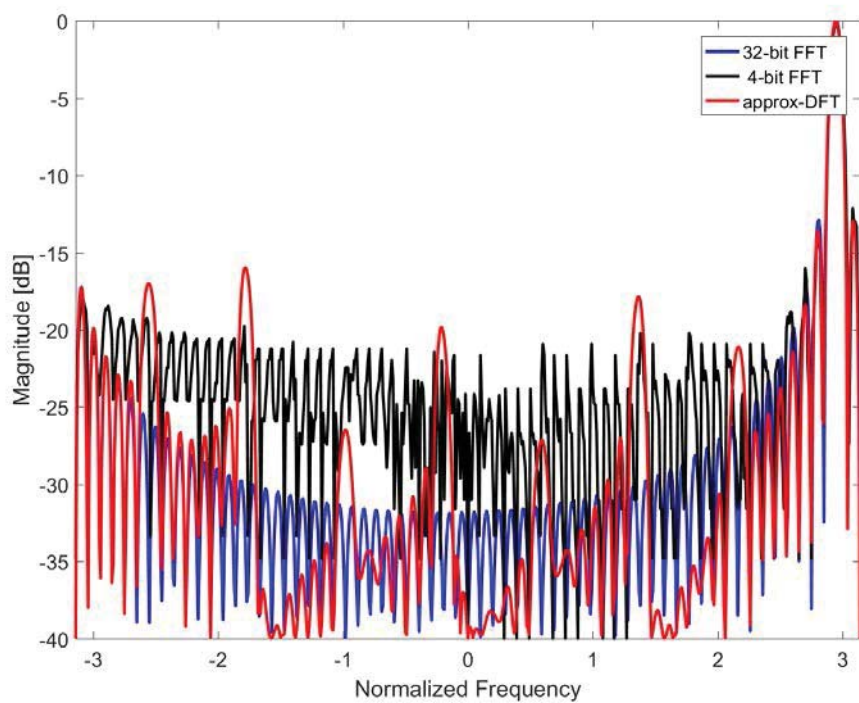


Figure 104: Output Comparison for Bin 35

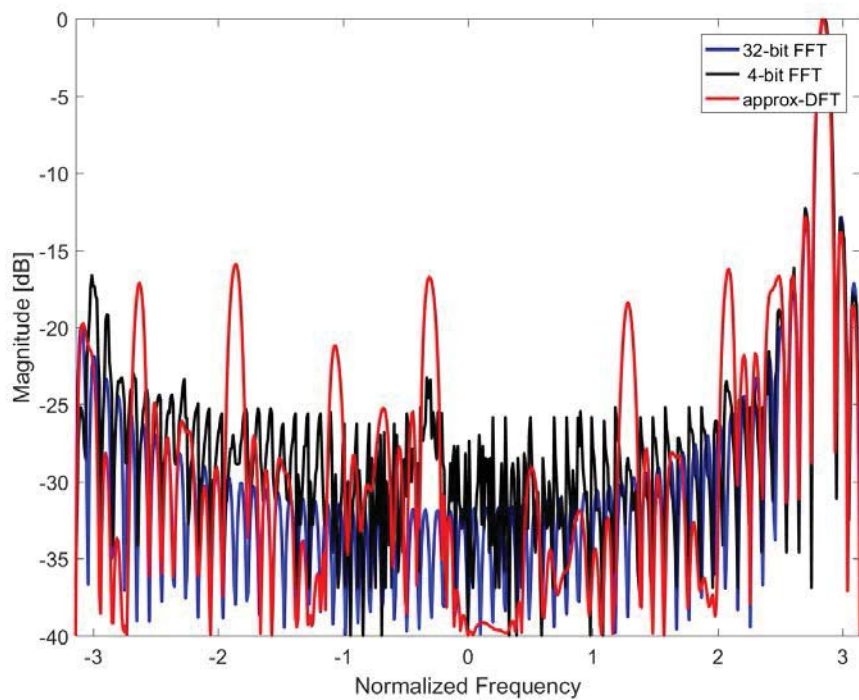


Figure 105: Output Comparison for Bin 36

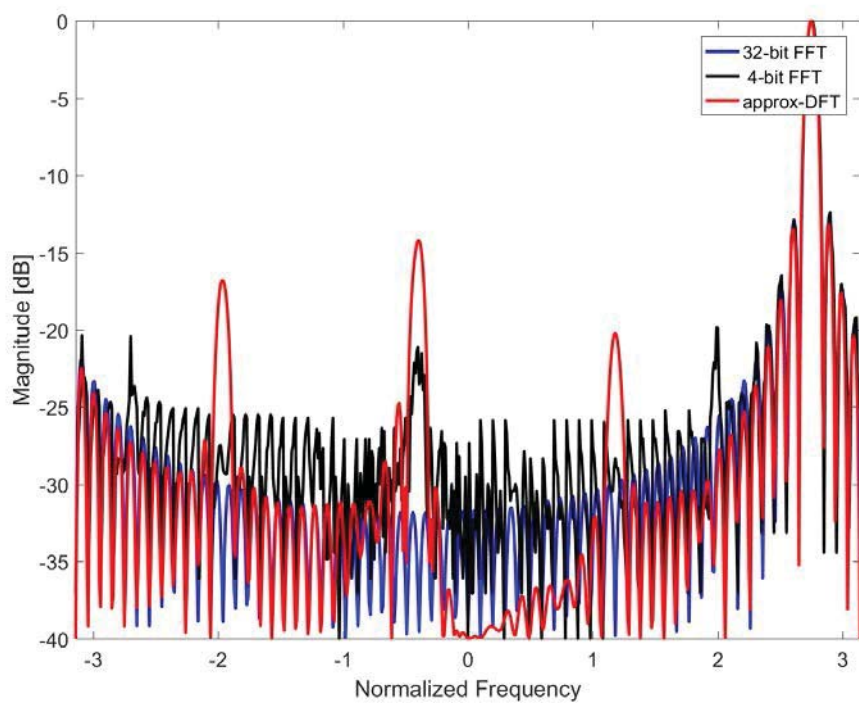


Figure 106: Output Comparison for Bin 37

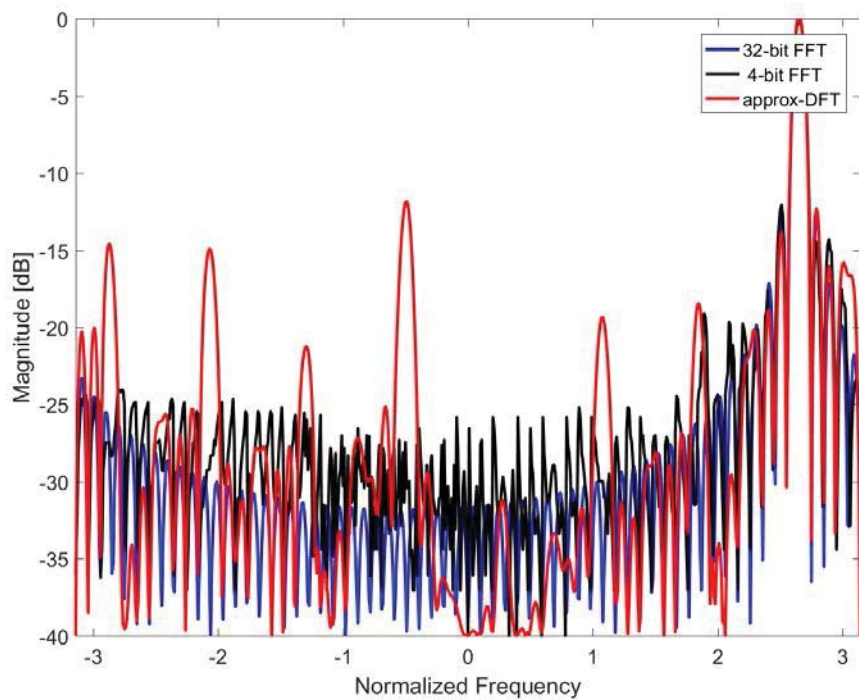


Figure 107: Output Comparison for Bin 38

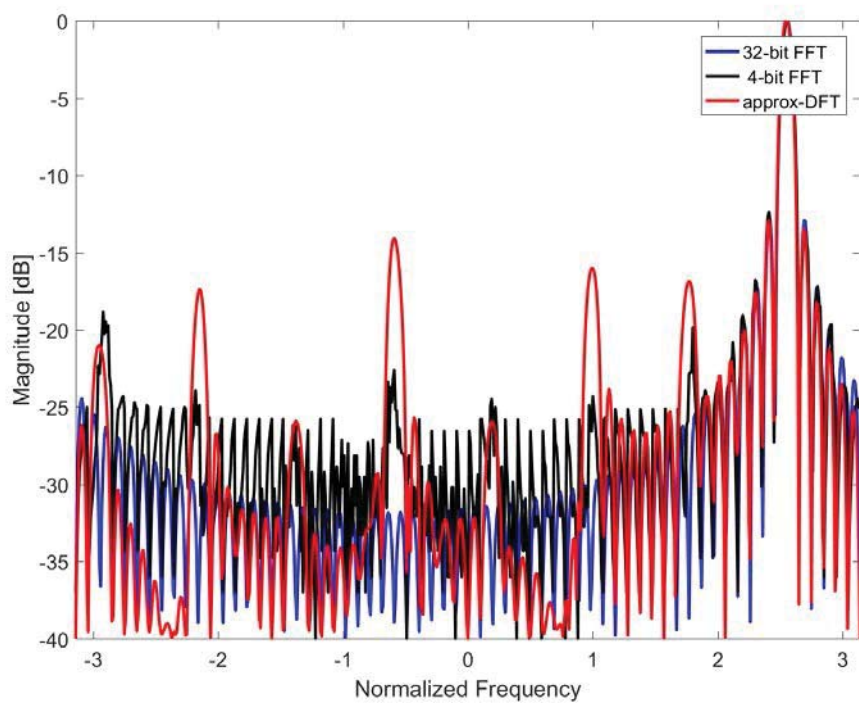


Figure 108: Output Comparison for Bin 39

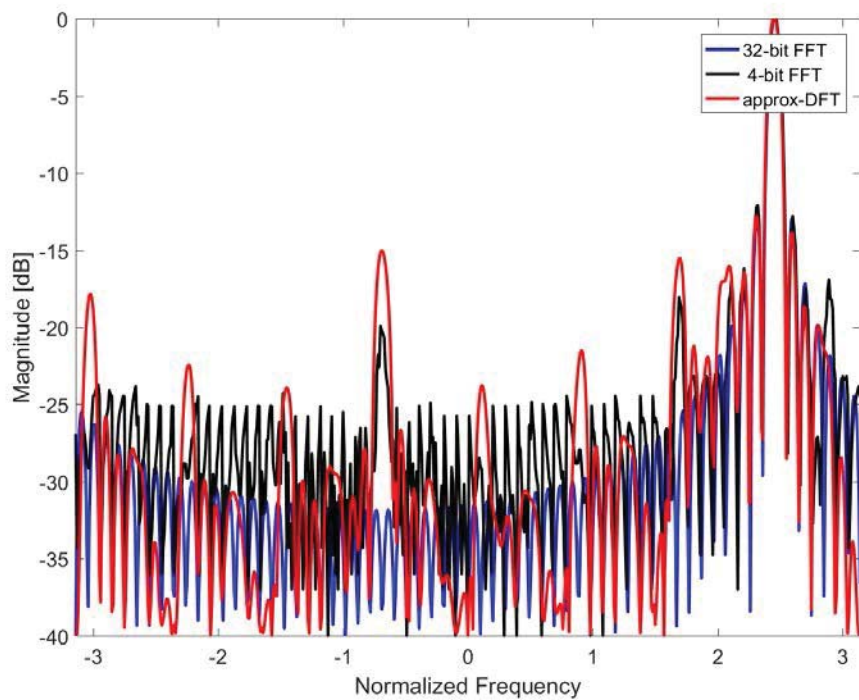


Figure 109: Output Comparison for Bin 40

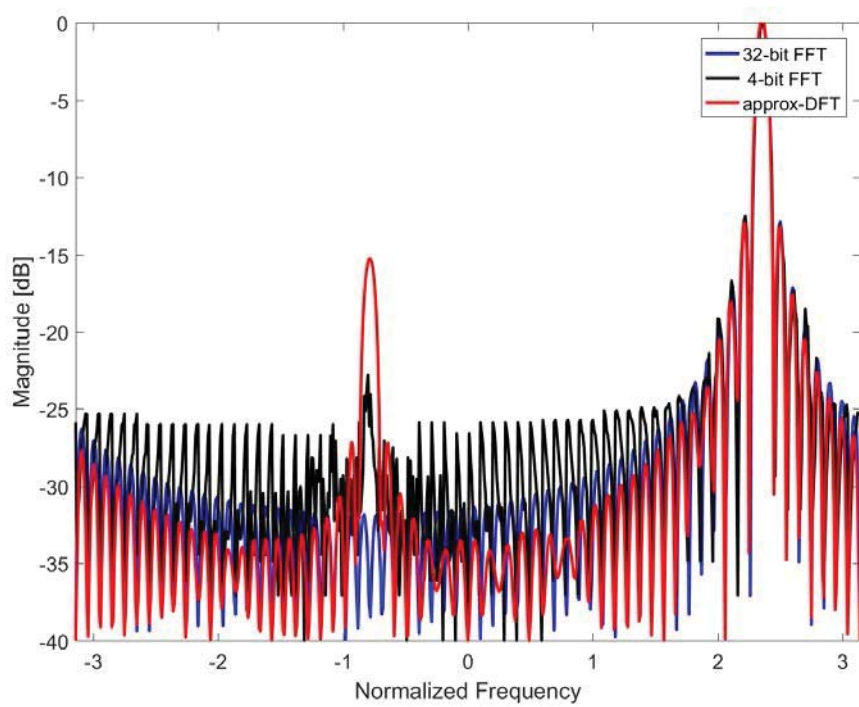


Figure 110: Output Comparison for Bin 41

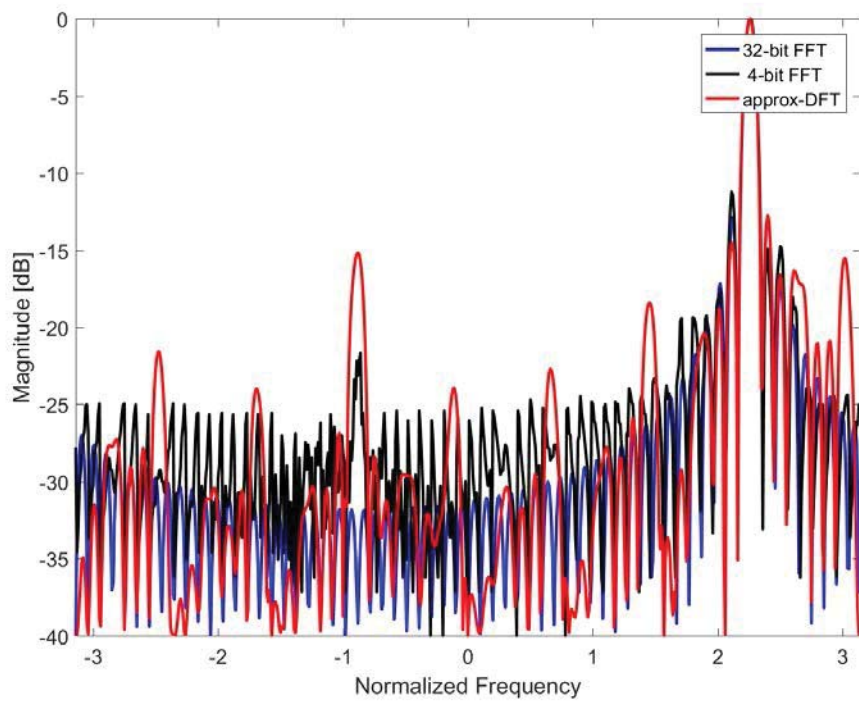


Figure 111: Output Comparison for Bin 42

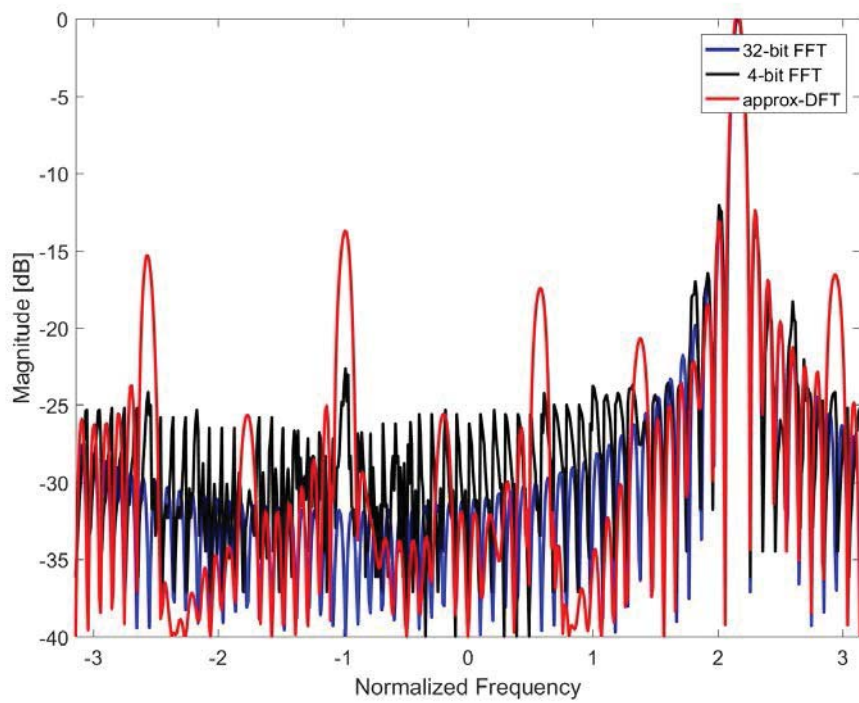


Figure 112: Output Comparison for Bin 43

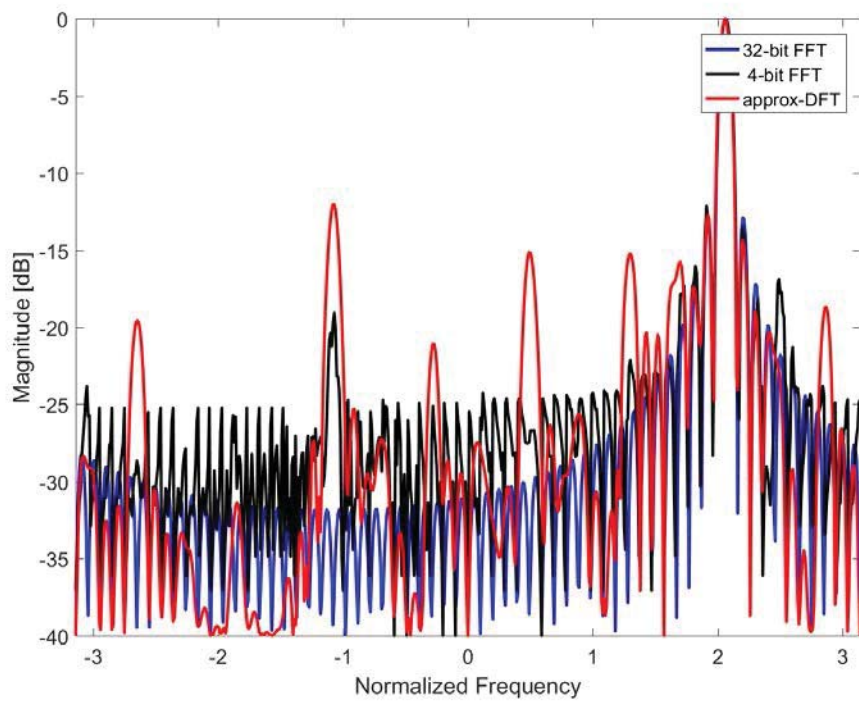


Figure 113: Output Comparison for Bin 44

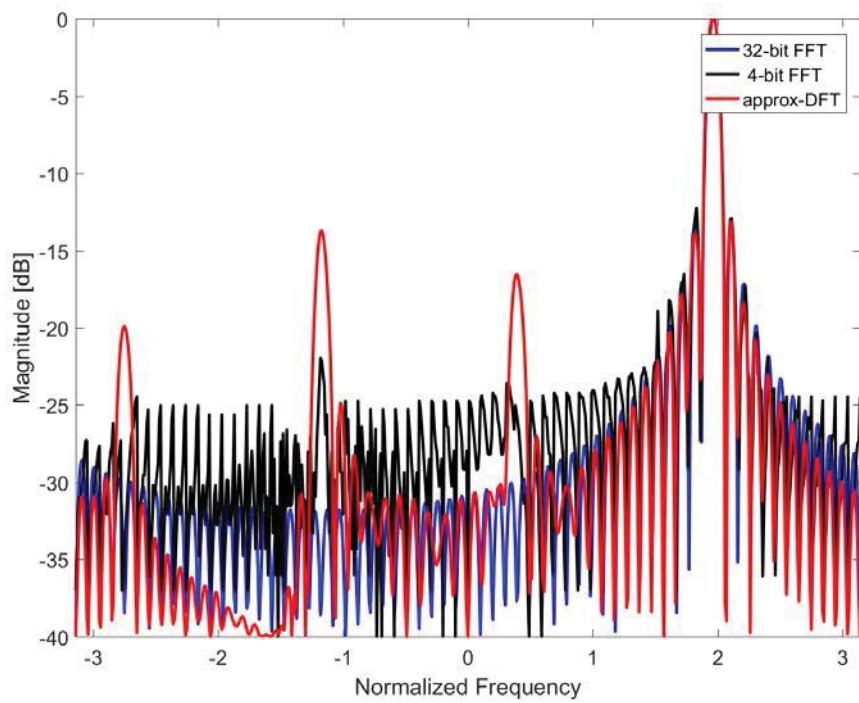


Figure 114: Output Comparison for Bin 45

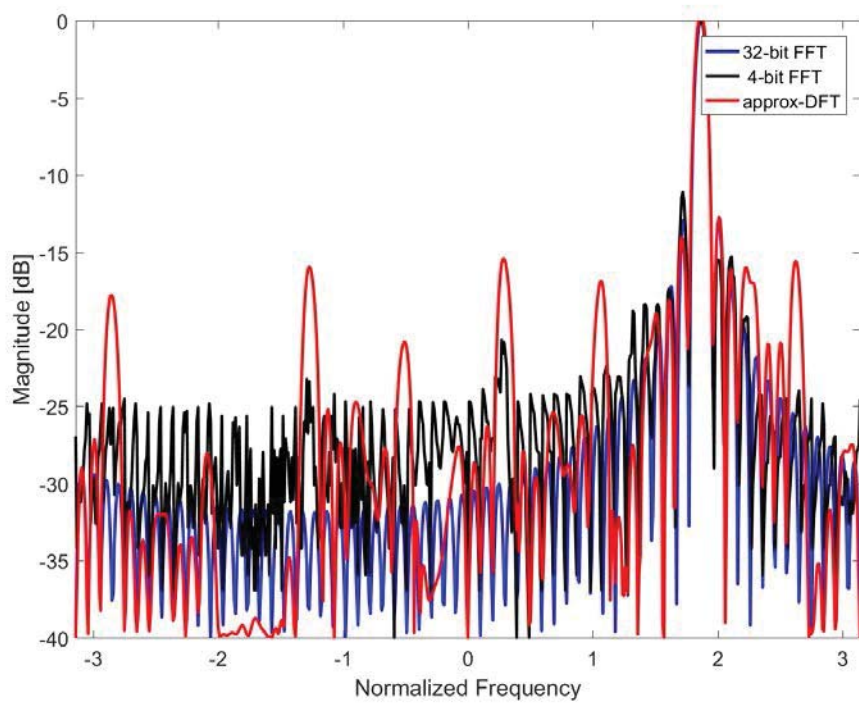


Figure 115: Output Comparison for Bin 46

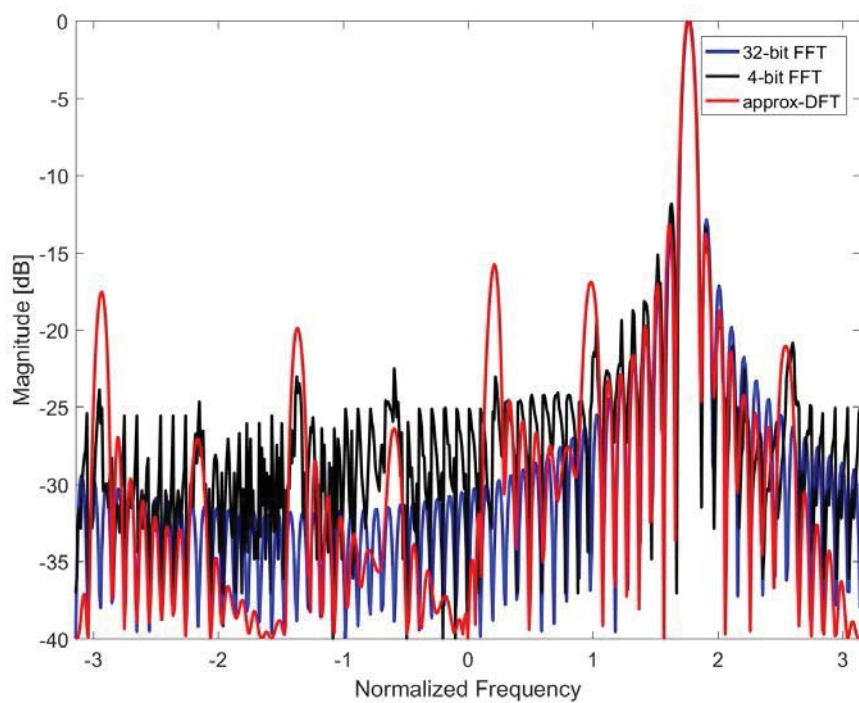


Figure 116: Output Comparison for Bin 47

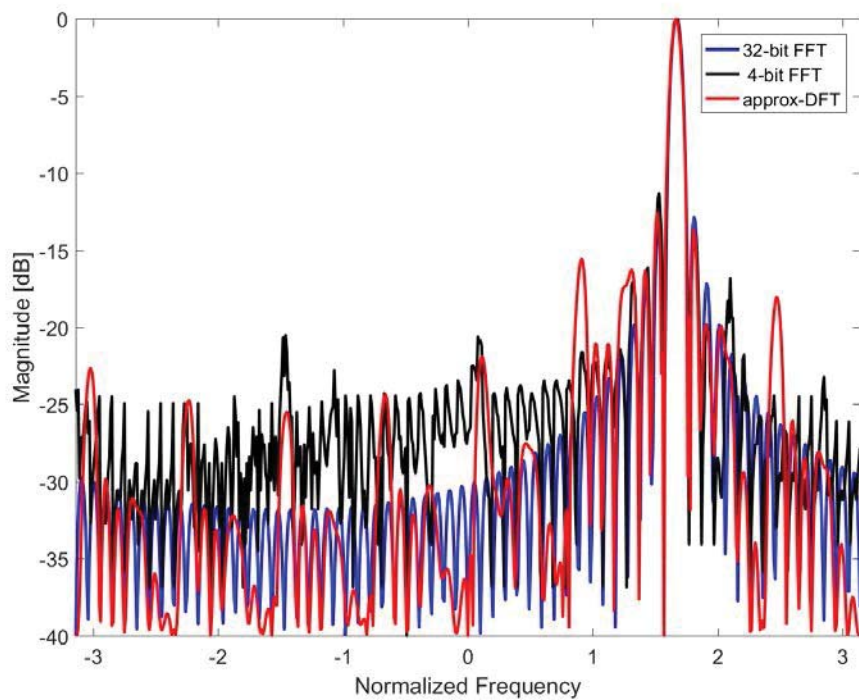


Figure 117: Output Comparison for Bin 48

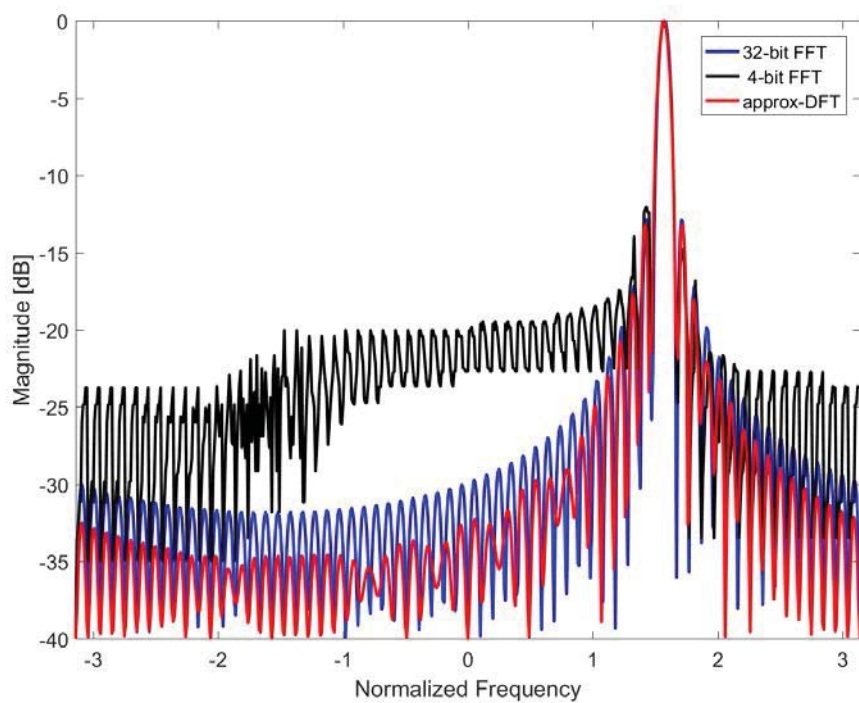


Figure 118: Output Comparison for Bin 49

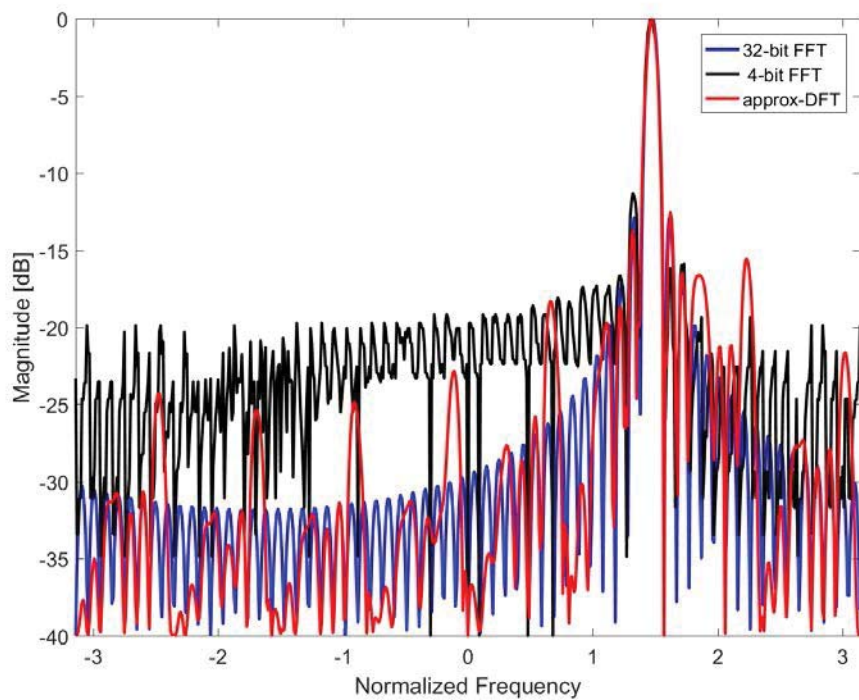


Figure 119: Output Comparison for Bin 50

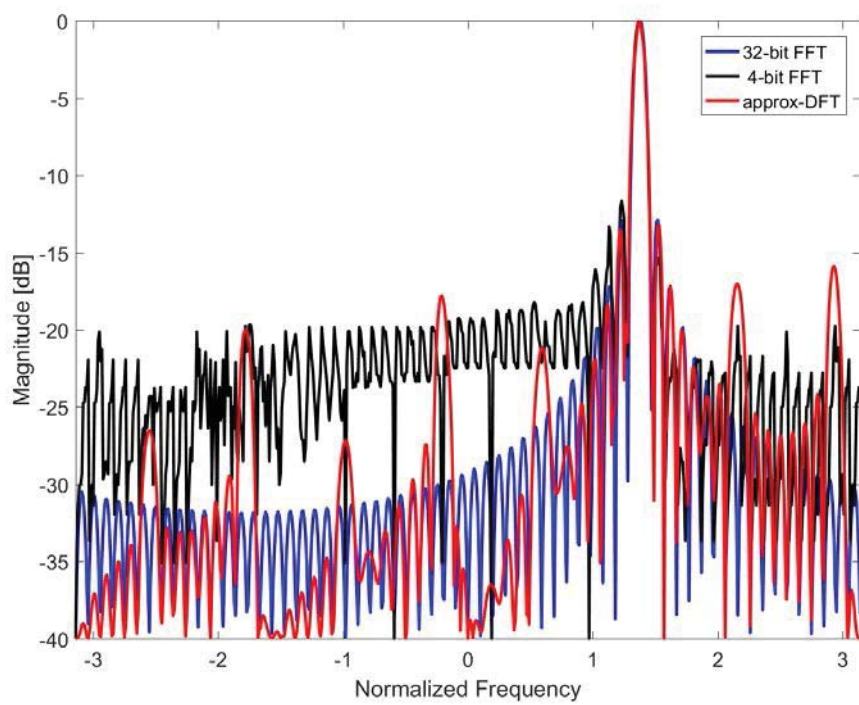


Figure 120: Output Comparison for Bin 51

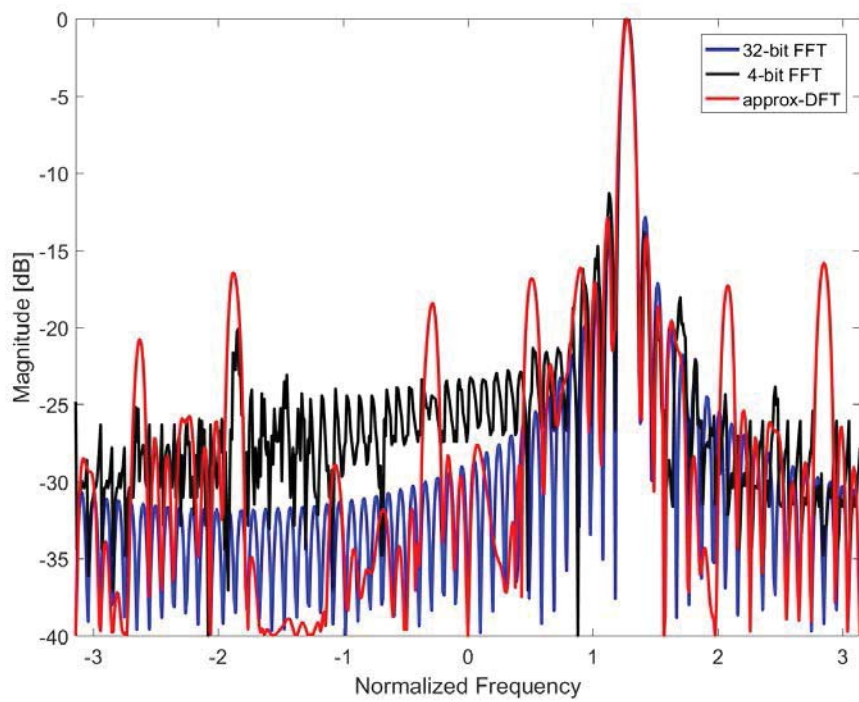


Figure 121: Output Comparison for Bin 52

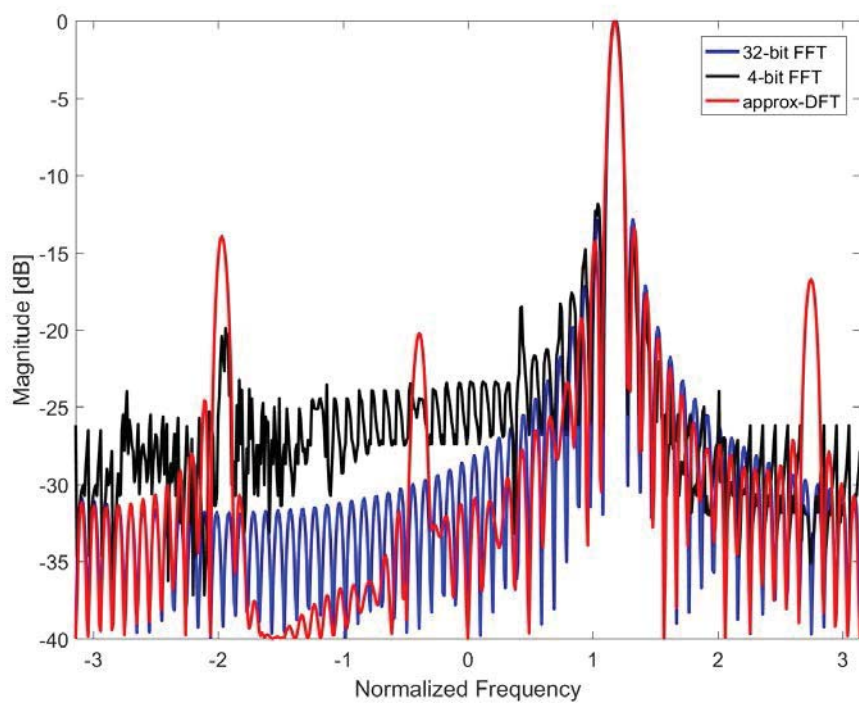


Figure 122: Output Comparison for Bin 53

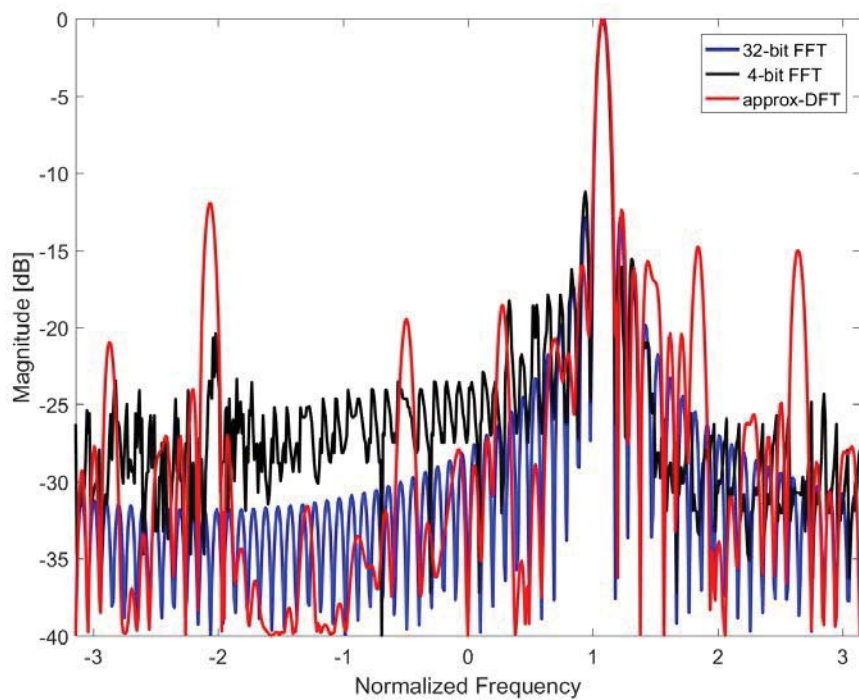


Figure 123: Output Comparison for Bin 54

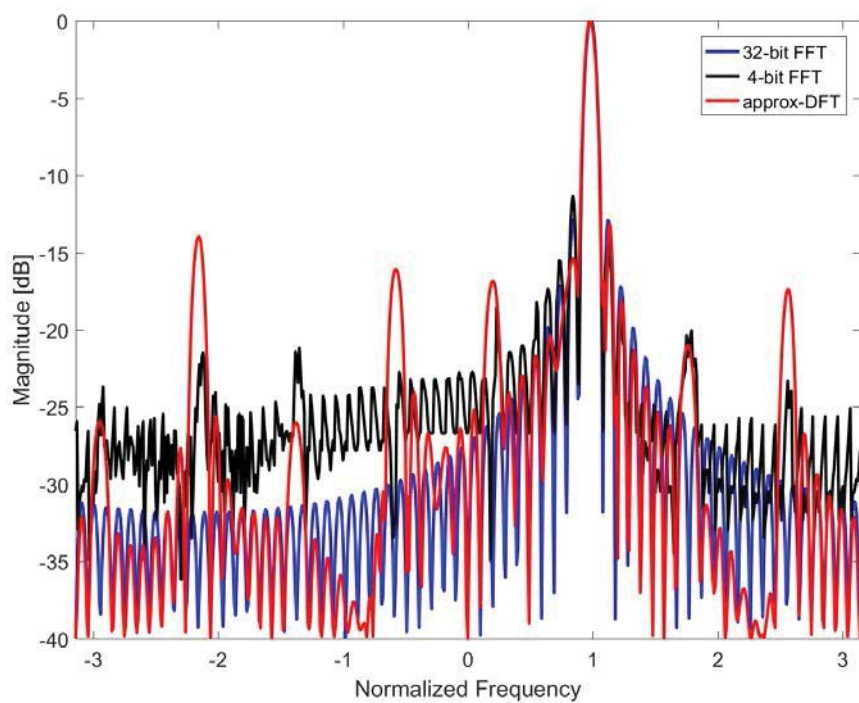


Figure 124: Output Comparison for Bin 55

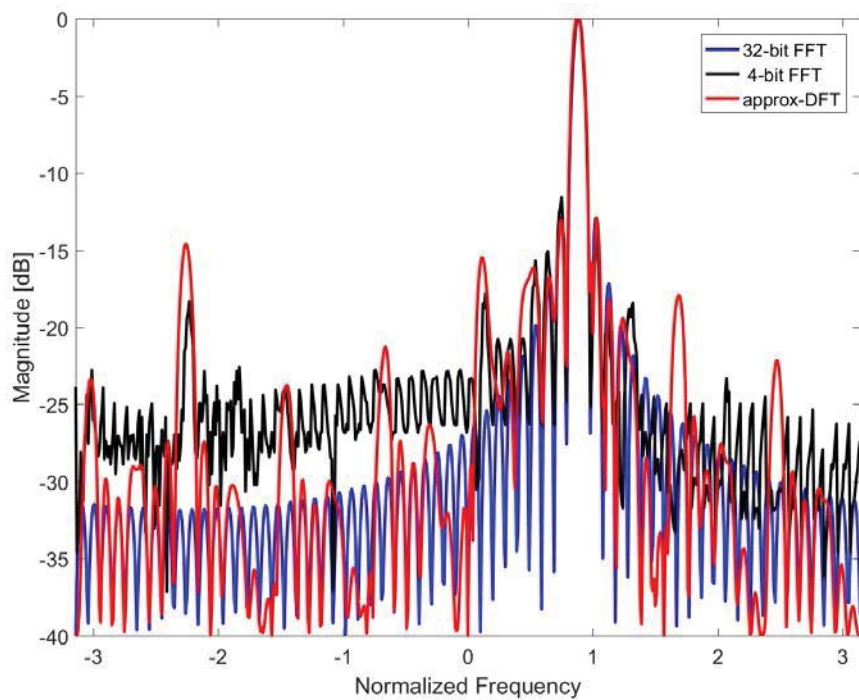


Figure 125: Output Comparison for Bin 56

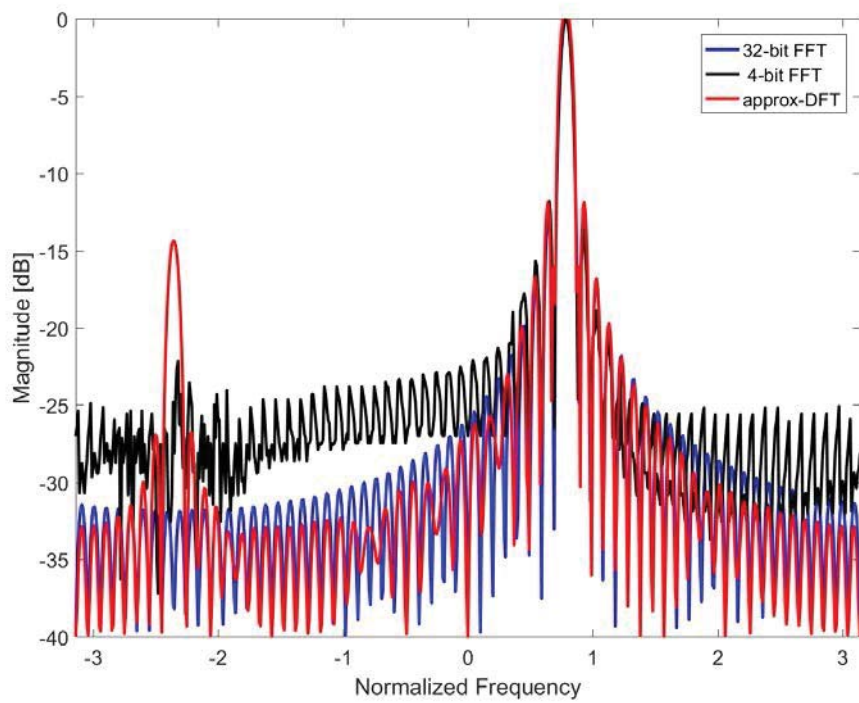


Figure 126: Output Comparison for Bin 57

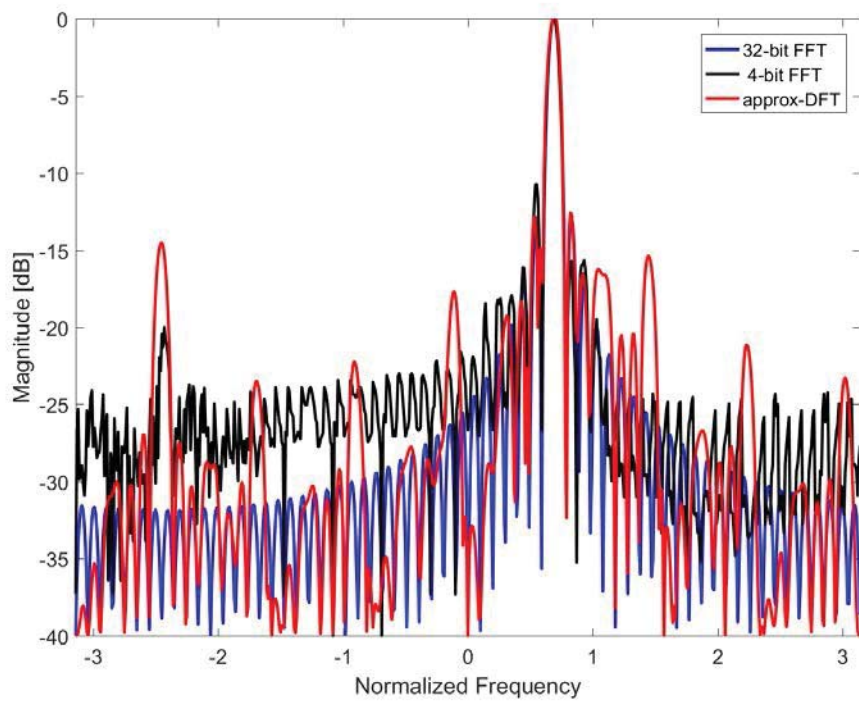


Figure 127: Output Comparison for Bin 58

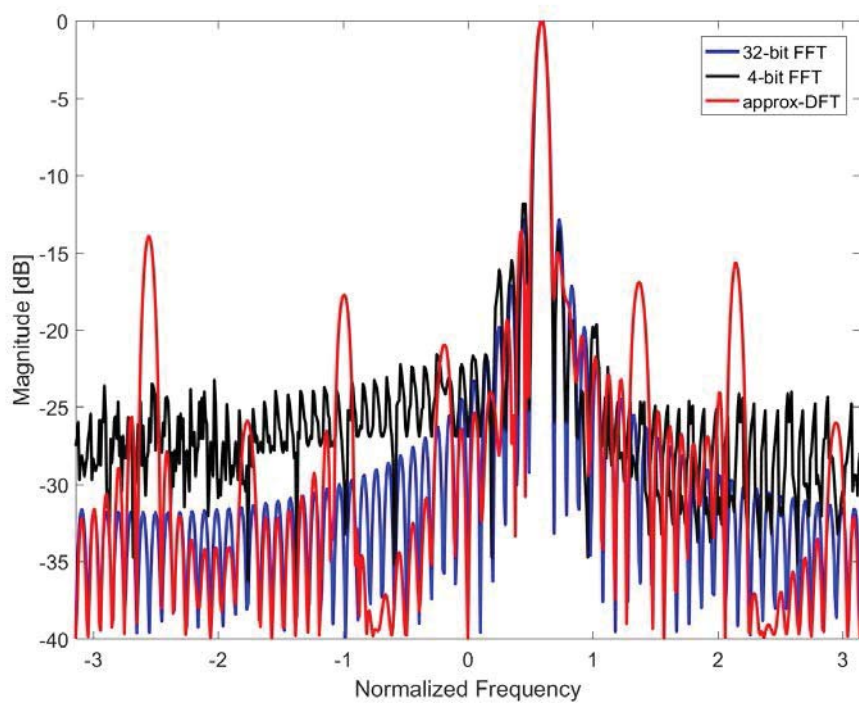


Figure 128: Output Comparison for Bin 59

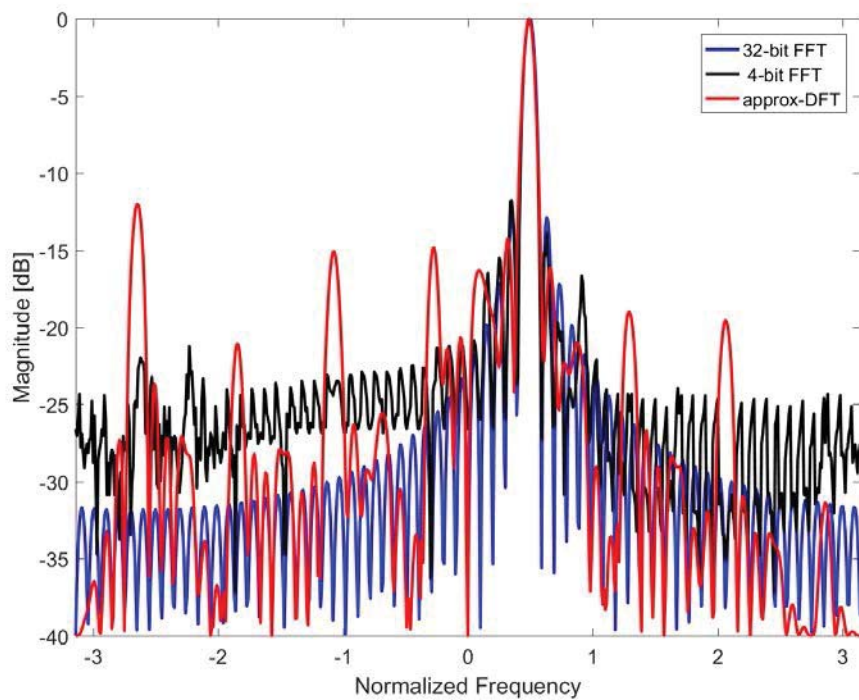


Figure 129: Output Comparison for Bin 60

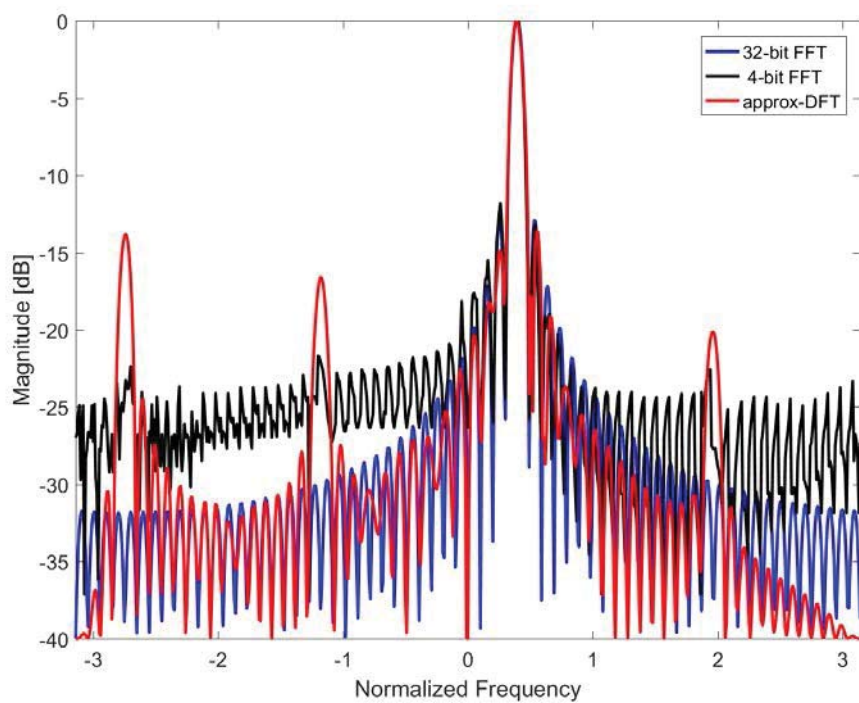


Figure 130: Output Comparison for Bin 61

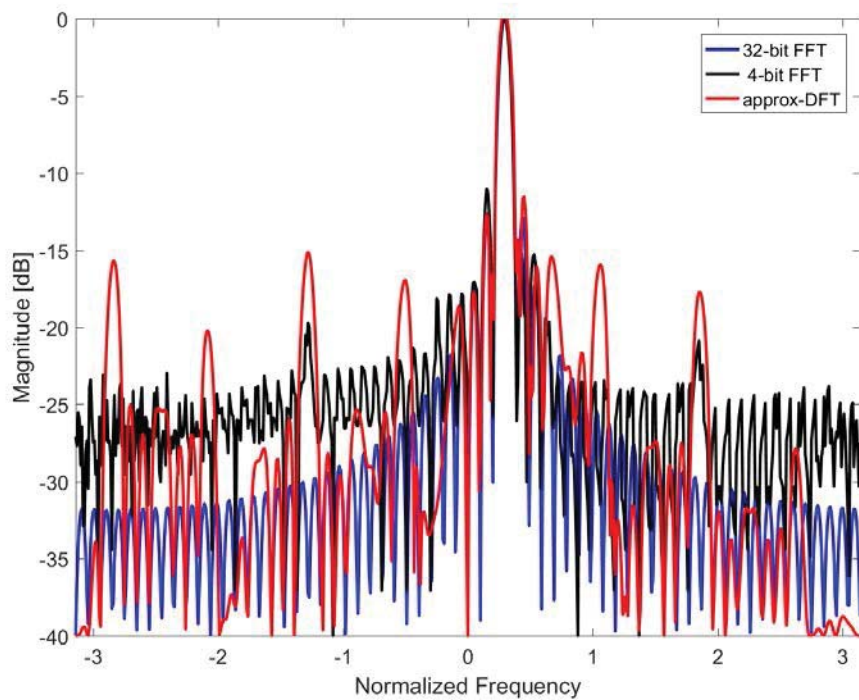


Figure 131: Output Comparison for Bin 62

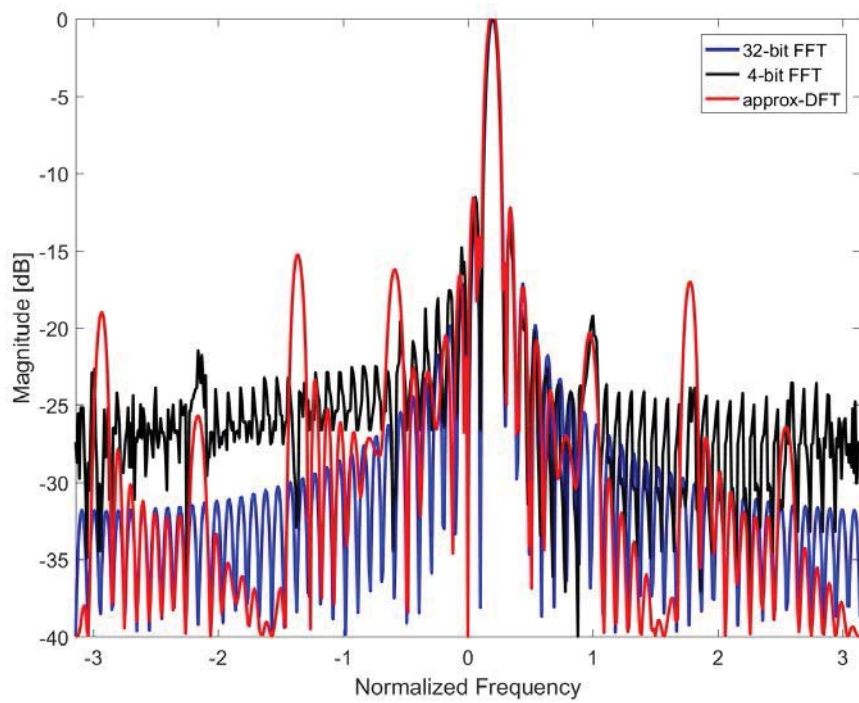


Figure 132: Output Comparison for Bin 63

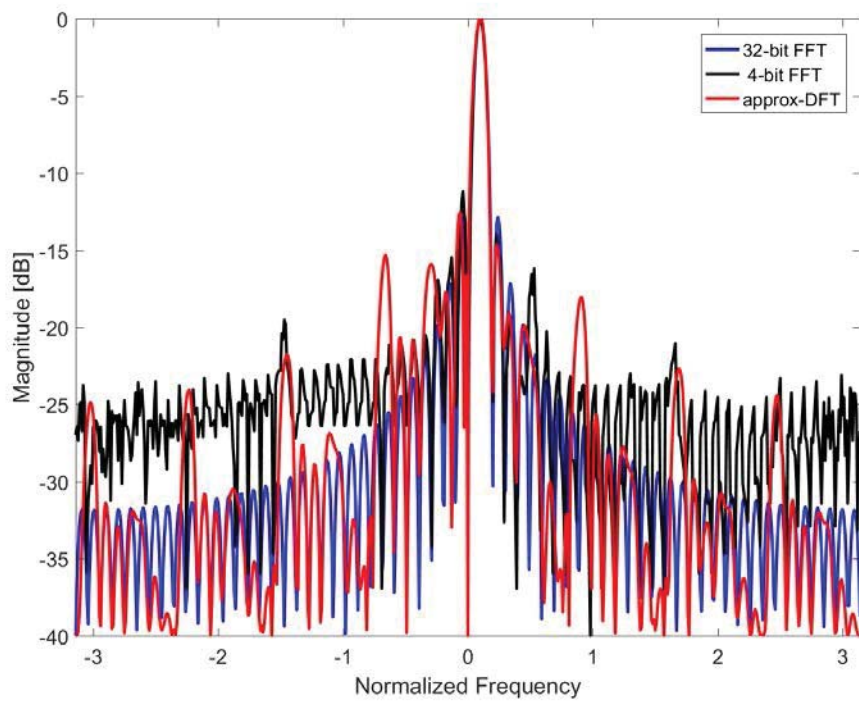


Figure 133: Output Comparison for Bin 64

3.5 VLSI Implementation and Comparison of the Hardware Complexities

All approximate transforms found were implemented on digital hardware targeting FPGA implementation. Xilinx tools were used to implement the designs in a fully parallel input parallel output architecture. In order to obtain a comparison of the performance metrics such as area, time and power of the approximate transforms, the corresponding exact transforms were also implemented. The implemented designs were pipelined for maximum speed of operation and were synthesized and mapped targeting the Xilinx Virtex-6 sx475t chip. Table 2 summarizes the hardware utilization and the critical path delay for 8-, 16-, 32-, and 64-point transforms (both approximate and exact). The comparison has been performed for 8- and 16-bit input word length sizes. The twiddle factor word length for the exact FFT designs has been fixed to 8 bits for all-point designs.

Table 2. Comparison of Hardware Resource Consumption using Xilinx Virtex-6 SX475T for different Numbers of Points with different Input Precision

FFT Design	Word Length	T_{CPD} (ns)		Slice Registers		LUTs		Occupied Slices		Flip-flops	
		Exact	Appr.	Exact	Appr.	Exact	Appr.	Exact	Appr.	Exact	Appr.
8-point	8-bits	2.107	1.929	1,411	1,288	1,456	1,012	459	345	1,633	1,231
	16-bits	2.125	2.009	1,705	2,280	1,905	1,690	572	582	2,055	2,131
16-point	8-bits	1.886	1.966	3,247	2,528	4,030	2,488	1,338	809	4,543	2,765
	16-bits	2.043	2.029	3,634	4,352	5,070	4,238	1,545	1,301	5,410	4,635
32-point	8-bits	3.420	2.212	4,074	6,420	7,193	5,866	2,265	1,888	7,287	6,465
	16-bits	3.611	2.085	6,698	10,788	11,920	9,837	3,507	2,702	12,019	10,252
64-point	8-bits	2.316	2.143	18,980	10,889	40,976	16,725	11,857	5,407	41,831	17,240
	16-bits	2.661	2.216	39,218	20,322	101,859	29,033	27,579	8,566	101,860	30,023

3.6 ASIC Realization Metrics Comparison

The designs were also mapped to 45-nm complementary metal-oxide-semiconductor (CMOS) technology cells (synthesis only) for a better performance level. Key quantitative measures of performance for the a-DFT realizations are listed in Table 3.

Table 3. Quantitative Measures of Performance for Approximate DFT Realizations

Performance Metric	16-point			32-point		
	16-point radix-2 FFT algorithm	a-DFT	Change	32-point Duhamel algorithm	a-DFT	Change
Area - A (mm^2)	0.295	0.166	44%↓	0.856	0.465	46%↓
Critical path delay - T (ns)	1.35	0.9	33%↓	1.73	0.86	50%↓
Frequency - F_{max} (GHz)	0.74	1.11	50%↑	0.58	1.16	100%↑
AT (mm^2ns)	0.398	0.149	63%↓	1.481	0.400	73%↓
AT ² (mm^2ns^2)	0.537	0.134	75%↓	2.562	0.344	86%↓
Dynamic Power - D_p (mW/GHz)	380.52	231.34	40%↓	1303	580	56%↓
Largest side-lobe level (dB)	-13.26	-13.05	0.21↑	ss-13.26	-11.03	2.23↑

3.7 Simulation of 2-D Beams Cross Sections

The computational complexity associated with obtaining N^2 simultaneous beams using an $N \times N$ rectangular aperture grows exponentially as $O(N^2 \log_2 N^2)$. In general, a 2-D signal $x(m, n)$ where $m = 0, 1, \dots, M-1$ and $n = 0, 1, \dots, N-1$, the 2-D DFT is defined as

$$X(k, l) = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} x(m, n) e^{\frac{-j2\pi k}{M}m + \frac{-j2\pi l}{N}n}.$$

This can be rewritten as

$$X(k, l) = \sum_{m=0}^{M-1} \left[\sum_{n=0}^{N-1} x(m, n) e^{\frac{-j2\pi l}{N}n} \right] e^{\frac{-j2\pi k}{M}m} = \sum_{m=0}^{M-1} G(m, l) e^{\frac{-j2\pi k}{M}m},$$

where $G(m, l)$ is the 1-D DFT along n . Therefore, the 2-D transform of an aperture array can be realized as a row-wise transformation of the column-wise transform. The replacement of the FFT with the a-DFT would reduce the required hardware complexity to a greater extent since zero

multipliers are involved. Thus, with the use of a-DFT cores, 2-D beams associated with the $N \times N$ aperture can be realized at zero multiplier complexity. For example, a radix-2 realization of 8×8 2-D FFT operation would require 64 real multipliers; 16×16 would require 768 real multipliers; and 32×32 would require 5632 real multipliers.

The 2-D beam plots obtained by the use of the a-DFT transforms were analyzed across the azimuth and elevation angle cuts. Following section provides 2-D beam plots and their sliced beam patterns over the azimuthal and elevation angles for 2-D beams arising from 8×8 , 16×16 and 32×32 a-DFT transforms. For the simulations, the angles are measured as shown in the Figure 134.

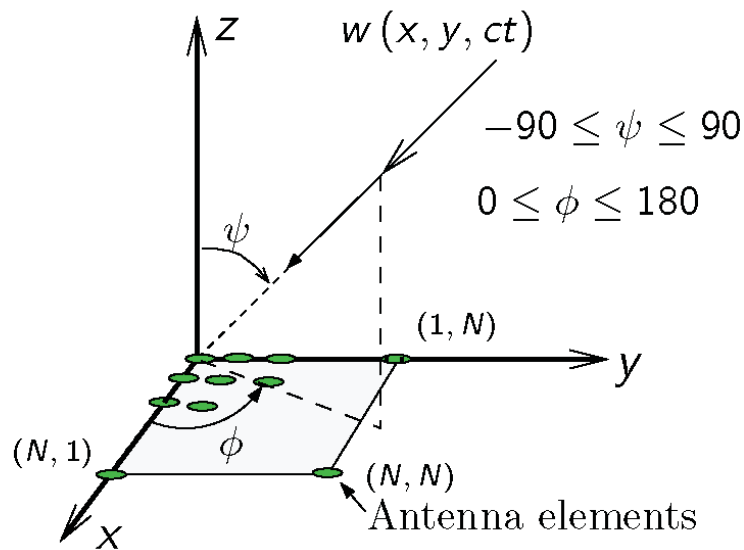


Figure 134: Symbol Convention for the Simulated Plots

3.7.1 8-point Approximation

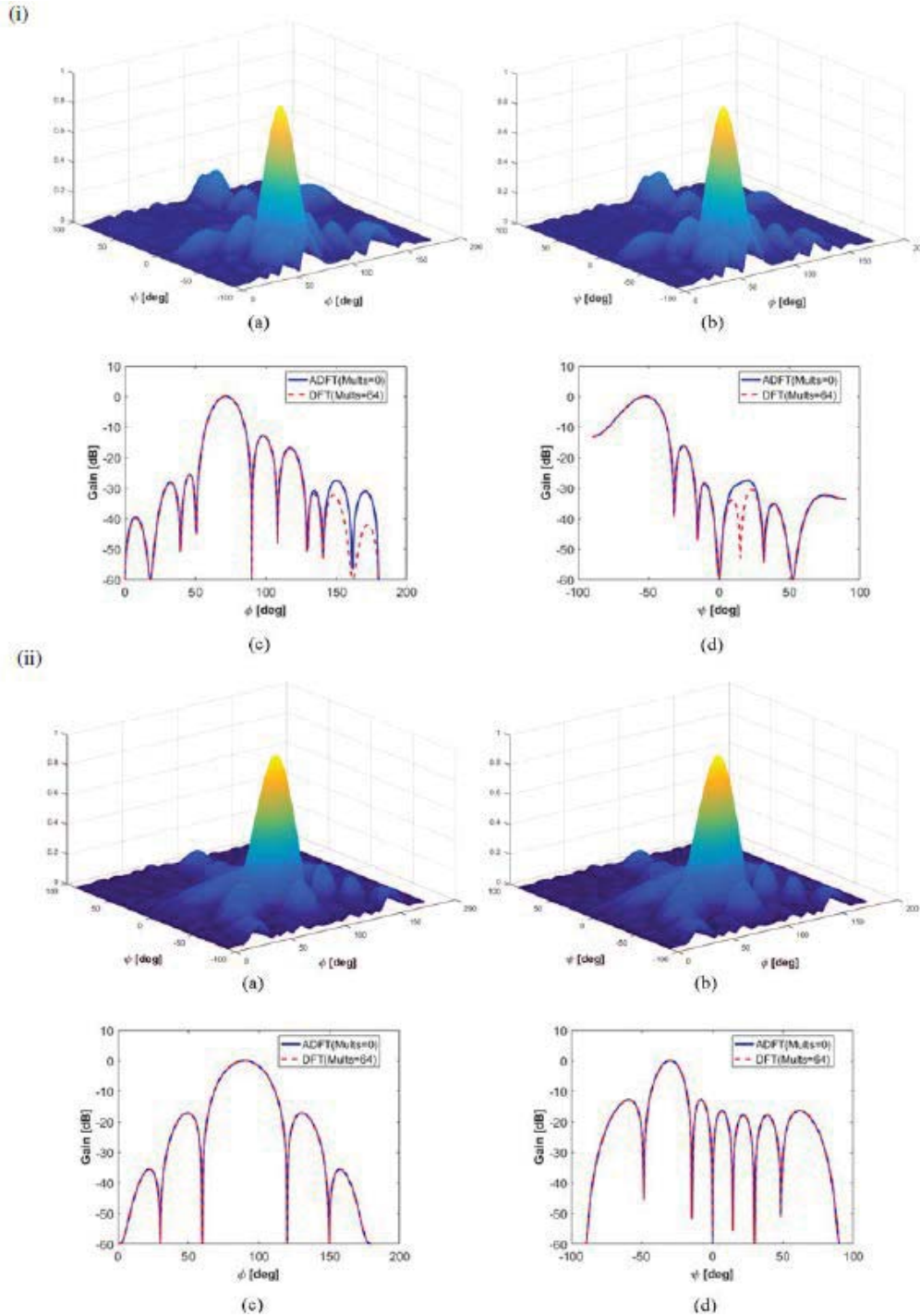


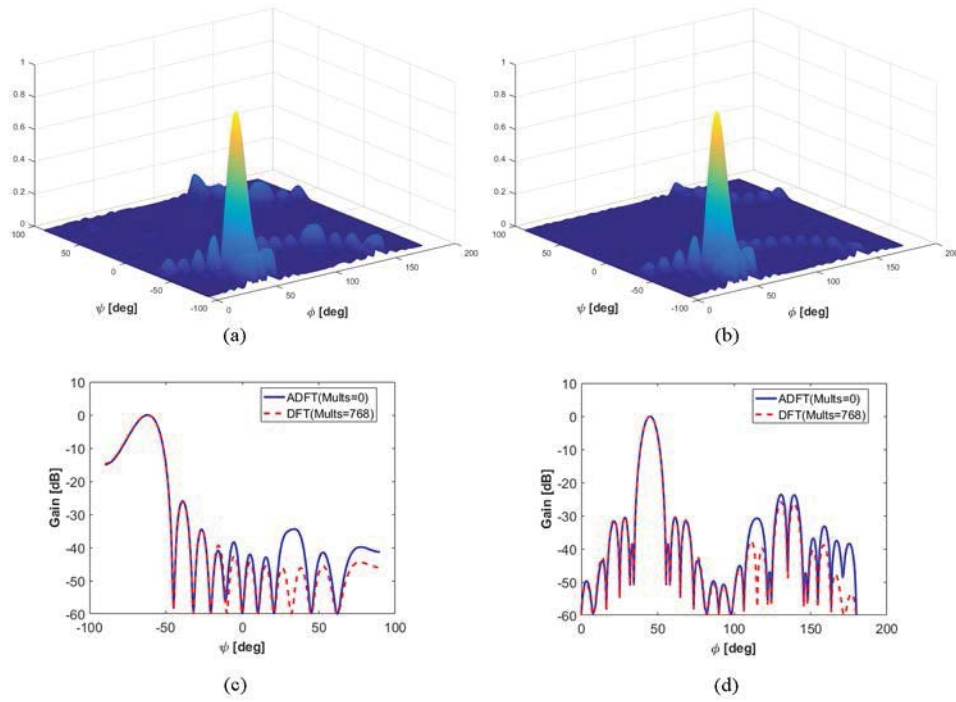
Figure 135: (i): 2-D Plots for $\phi = 90.00$, $\psi = -30.00$ and (ii) 2-D plots for $\phi = 71.60$, $\psi = -52.00$

Notes for (i): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -30.00$, and (d) along ψ for fixed $\phi = 90.00$.

Notes for (ii): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -52.00$, and (d) along ψ for fixed $\phi = 71.60$.

3.7.2 16-point Approximation

(i)



(ii)

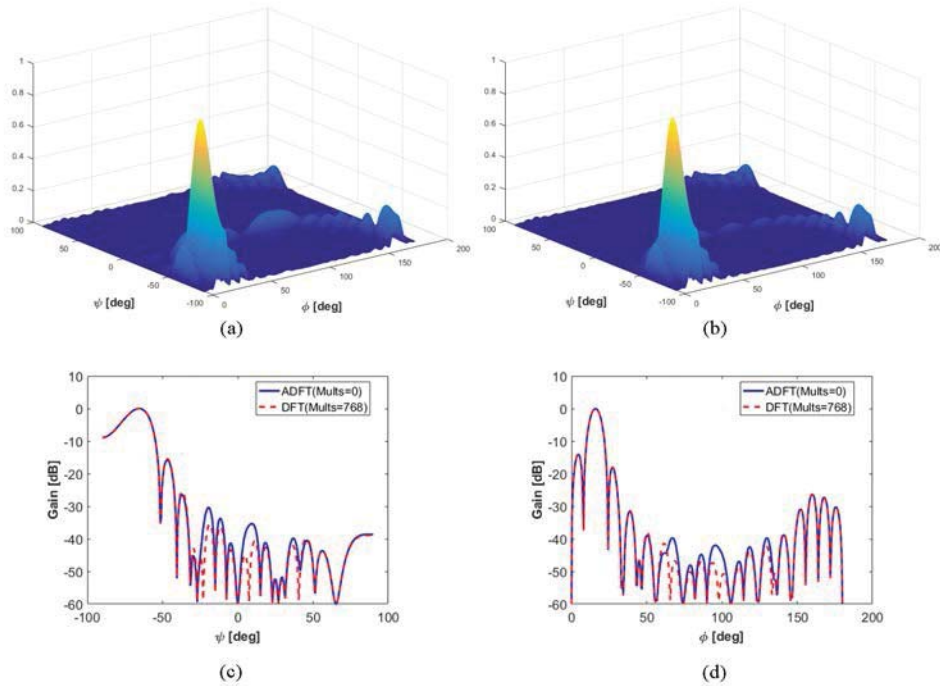


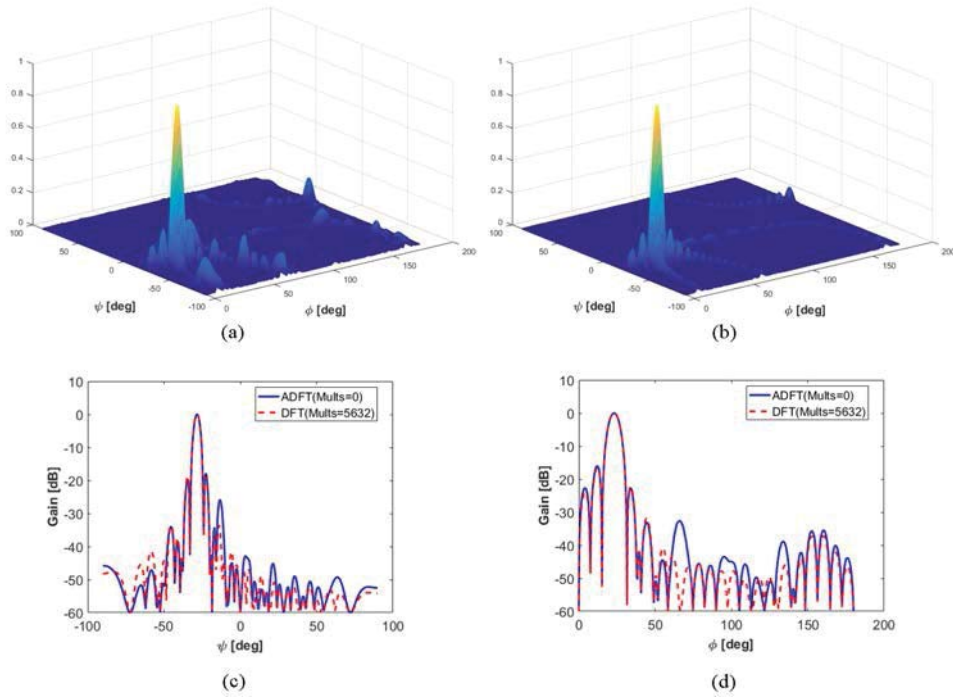
Figure 136: (i): 2-D plots for $\phi = 44.80$, $\psi = -62.00$ and (ii): 2-D plots for $\phi = 16.00$, $\psi = -65.50$

Notes for (i): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -62.00$, and (d) along ψ for fixed $\phi = 44.80$.

Notes for (ii): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -65.50$, and (d) along ψ for fixed $\phi = 16.00$.

3.7.3 32-point Approximation

(i)



(ii)

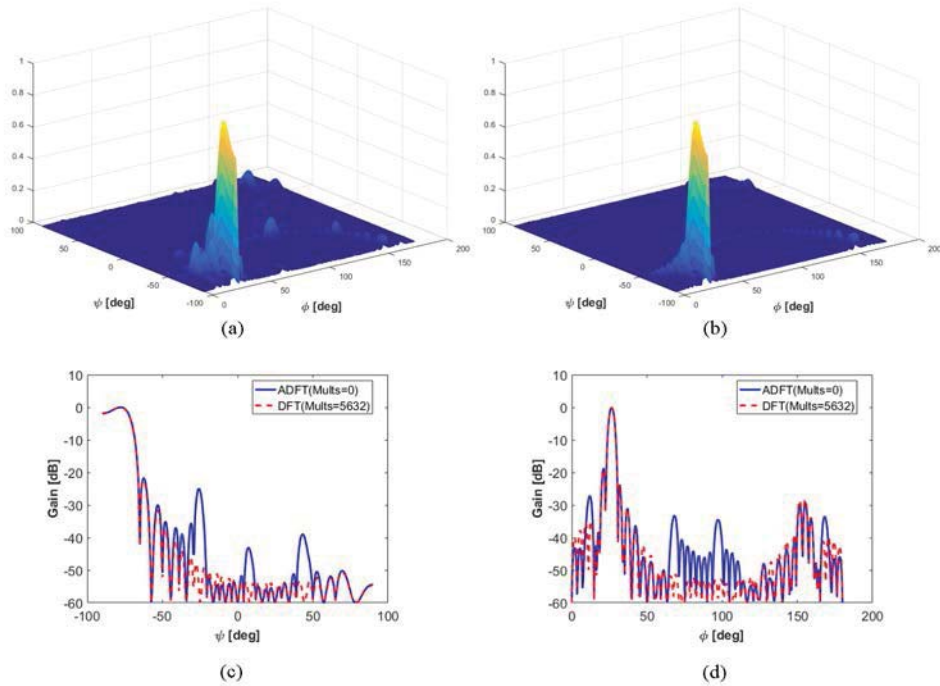


Figure 137: (i): 2-D plots for $\phi = 23.20$, $\psi = -28.50$ and (ii): 2-D plots for $\phi = 26.40$, $\psi = -78.00$

Notes for (i): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -28.50$, and (d) along ψ for fixed $\phi = 23.20$.

Notes for (ii): (a) a-DFT, (b) exact DFT, (c) along ϕ for fixed $\psi = -70.00$, and (d) along ψ for fixed $\phi = 26.40$.

4. HARDWARE SETUP

To physically obtain and measure the beams from the proposed approximate DFT algorithms (and compare them with the DFT beams), a 2.4-GHz RF system with a digital processing-end was designed and implemented. Figure 138 shows the overall architecture of the implemented beam measurement system. The initial system was designed as a 16 antenna-element system. Main subsystems were identified as the antenna array, RF receiver chain and the digital processing unit. Each antenna element was associated with an in-phase (I) and quadrature (Q) receiver chain where the amplification, mixing and filtering is performed. Next, the obtained downconverted based band signal is processed using a digital hardware through analog-to-digital conversion (ADC). In digital processing, the DFT-based multi-beamforming is performed. Each beam output is then further processed to integrate and estimate the received beam energy for a specific antenna orientation.

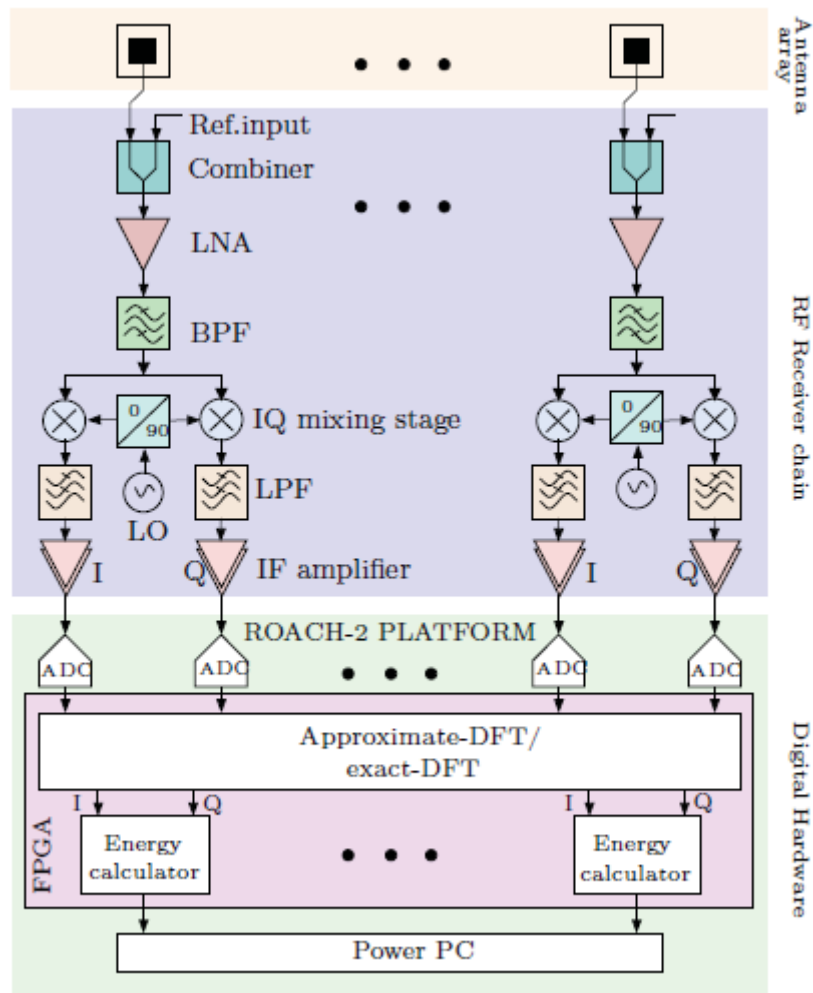


Figure 138: The System Architecture

4.1 2.4-GHz Antenna Array

A 16-element antenna array was designed to work 2.4 GHz. A single element patch was simulated and fabricated, as shown in Figure 139 (c). Figure 139 (a) and (b) show the simulated and measured $|S_{11}|$ respectively. Next, a 16-element array was constructed where the element spacing was set to $\lambda/2 \approx 62.5$ mm. Figure 139 (d) shows a picture of a built individual-element and the sub figure (b) shows the full 16-element antenna array. Each element was tested working using a transmitted 2.4 GHz signal. Figure 139 (e) shows the measured power pattern of the array-elements. Measurements were obtained using the setup described in Section 4.4.

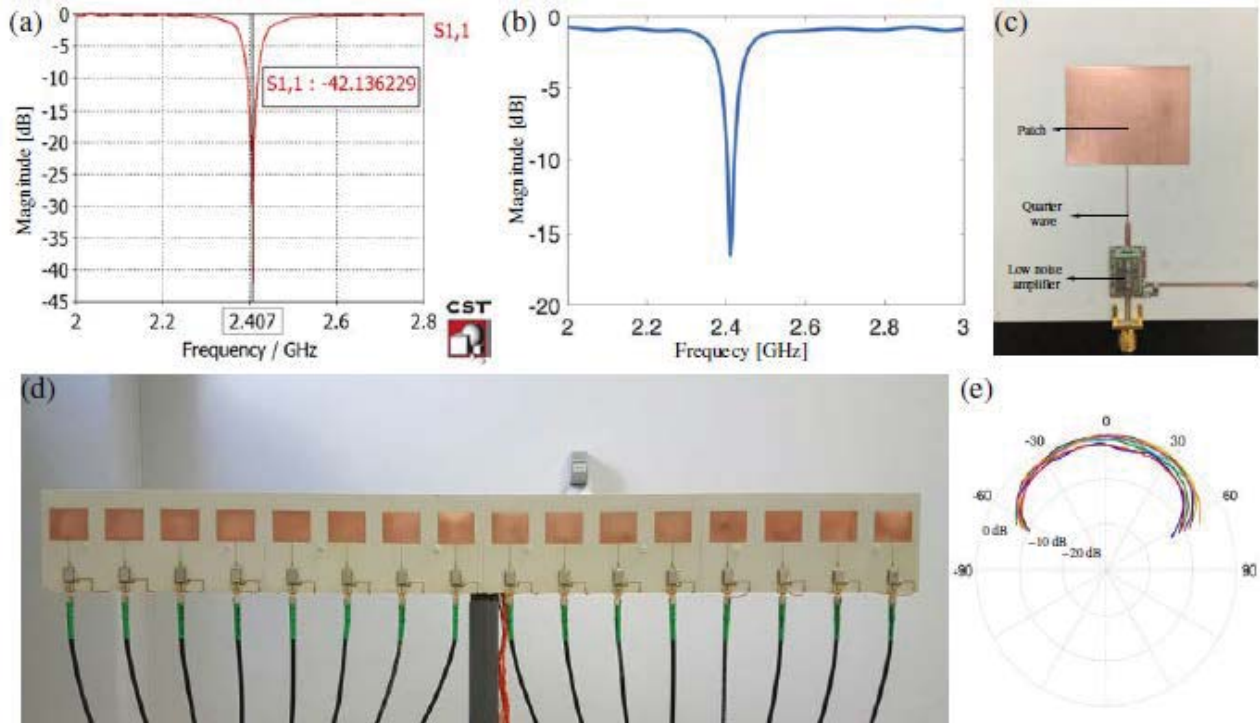


Figure 139: simulated and fabricated single element patch for 16-element antenna array

(a) Simulated s_{11} , (b) measured s_{11} for a single patch antenna, (c) fabricated 2.4 GHz patch antenna element with the integrated low noise amplifier, (d) full 16-element antenna array, and (e) measured antenna patterns.

4.2 RF Receiver Chain

The RF receiver chain was designed as illustrated in Figure 138. Commercial off-the-shelf (COTS) components were used to build the receivers. First, the captured signal is amplified using a low noise amplifier (LNA). Then it is bandpass filtered to filter out the 2.4-GHz signals. The amplified and filtered signal is then split in two to achieve in-phase quadrature (IQ) downconversion. A local oscillator (LO) signal is 90° split and fed to the two mixers to obtain the IQ downconverted signals. The mixer output is then low-pass filtered and again amplified to boost the filtered baseband signal. Figure 140 (a) shows the full 16-element receiver chains using the COTS components.

4.3 Digital Hardware and Design Architectures

Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) Reconfigurable Open Architecture Computing Hardware (ROACH) has been used in our systems to sample the intermediate frequency (IF) signal and perform the digital beamforming. ROACH-2 [6] is an open source platform which includes following notable features:

- Virtex-6 SX475T field-programmable gate array (FPGA),
- PowerPC 440EPx stand-alone processor to provide control functions,
- 2x Multi-gigabit transceiver card slots ($4 \times 10\text{GE}$),
- 2 ZDOK interfaces.

The two ZDOK interfaces can be used to integrate daughter ADC cards manufactured by CASPER to perform digitization of the signals. The current setup employs two ADC16x250-8 cards [7] where each card can accommodate up to 16 analog inputs. The two cards together provide 32 analog inputs enabling the sampling of 32 channels arising from the 16-element channels. The cards can be configured to achieve different sampling rates. i.e., 32 inputs up to 240 MHz, 16 inputs up to 480 MHz and 8 inputs up to 960 MHz. A picture of the ADC cards installed on the ROACH-2 platform is shown in Figure 140 (b). The ROACH-2 platform comes with a high-end Virtex-6 SX475T FPGA which can accommodate large designs. The device has 476,160 logic cells, 74,400 configuration logic blocks (CLBs) and 2016 DSP48 slices.

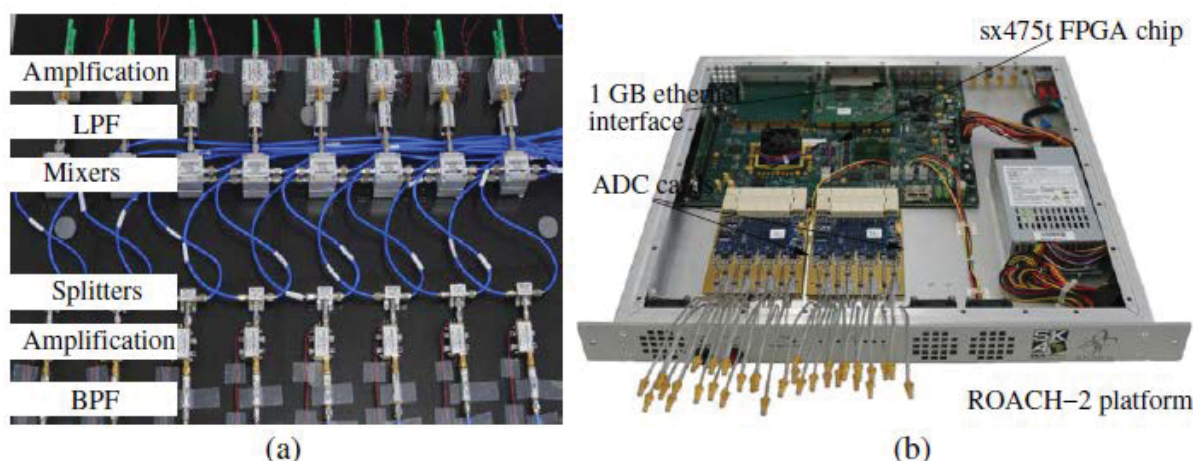


Figure 140: (a) Receiver Chains Implemented using COTS Components and (b) ROACH-2 Processing Platform with the Two ADC Cards Connected to the FPGA Board

FPGA Designs for Multi-Beamforming

The digital designs for performing multi-beamforming using the proposed algorithm and the exact DFT (for comparison purposes) were designed using Xilinx tools. The FPGA designs for both approximate and exact DFTs have been designed for 8-, 16-, 32- and 64- point transforms. Fully parallel input, parallel output architecture has been adopted while designing to achieve maximum speed of operation. The designs have been tested and verified using hardware cosimulation methods. The hardware resource consumption and the timing information were

recorded for both approximate and exact DFTs by synthesizing and mapping them to the Xilinx Virtex 6 SX475T chip. Table 2 (on page 127) summarizes the key figures of merit.

For obtaining the measurements, all the transform cores were configured to an 8-bit input word length. This was done since the ADC16x250-8 ADC cards used in the setup had an 8-bit output. The cores were pipelined so that they could be run at a clock speed of 200 MHz clock period.

Digital Circuit Architectures for Beam Measurements

Apart from the digital cores for performing the spatial DFT of the sampled signals, other additional circuitry needed to support beam measurement were also developed inside FPGA for convenience in manipulating the data in real time and for different angles. Figure 141 shows the overview architecture of the digital circuit.

The front portion of the digital architecture consists of the digital normalizing circuit, which is used to calibrate RF chains. The calibration procedure is described in Section 4.4. This stage consists of a set of multipliers (an N element design will need $2N$ multipliers in this stage) where one input of each multiplier is connected to a 32-bit software controllable register (SCR). The other input is the ADC channel. These software configurable registers are all first set to 1 to determine the calibration gains of each RF chain for a reference input. Once the calibration gains are determined for each channel, each SCR is overridden with the corresponding gain value.

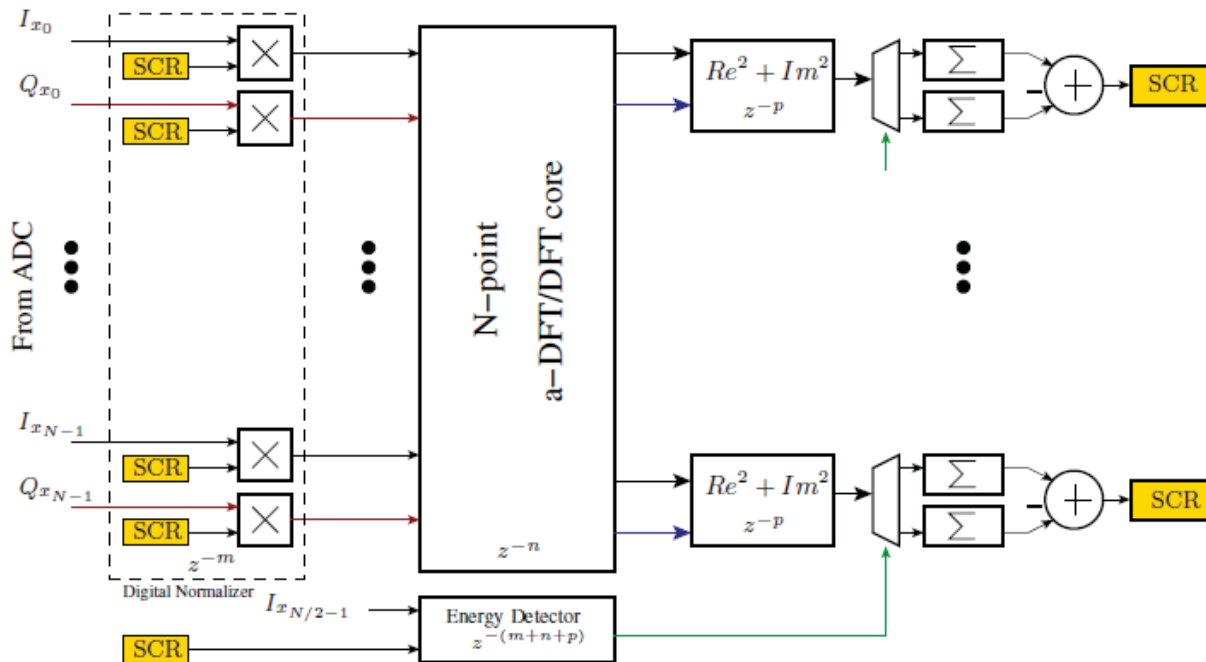


Figure 141: Digital Architecture for obtaining a-DFT/DFT Beam

After the digital normalizing stage, the signals are driven to the a-DFT/DFT digital core. The in-phase signal (either I or Q) will be fed to the real inputs of the core and the quadrature signal (or the other) will be fed to the imaginary outputs. Next, the real and imaginary outputs of the corresponding output bin of the digital FFT core are sent for calculating the instantaneous power

of the sample. This is achieved by performing $(\text{Re}\{Y_k\})^2 + (\text{Im}\{Y_k\})^2$ where $0 \leq k \leq N - 1$. This is implemented with two multipliers and one adder per channel. The word length of the input to this block will depend on the bit growth due to the a-DFT/FFT core. The output from this block will be sent to an accumulator to integrate over a pre-specified time period. The time of integration is designed to be modifiable through software control.

The overall architecture is designed to perform the functionality of a lock-in amplifier to filter out ambient 2.4-GHz radiation present in the environment. To achieve this, the transmitted signal will be switched on and off at a particular rate, and the energy level received when the transmitter is on and off are calculated separately. The transmitter design approach is discussed at the end of the Section 4.4. The digital circuit for the receiver has been designed to cope with this setup. For this purpose, two integrators will be used for each channel and these integrator are activated depending on whether the transmitted signal is on or off. An energy detector is employed at the front of the circuit to achieve this functionality. The Boolean output from this block will be used as a select signal of a demultiplexer (or demux) that selects one of the integrators when the RF is on and the other when RF is off. Finally, the difference of the two integrator values is computed as the received energy of a particular bin. Computed values are updated in FPGA memory and are read to the host server using the software routines.

4.4 Setup for Beam Measurement

Figure 142 shows the full experimental setup for obtaining the beam measurements. Figure 142 (a) shows the receive-mode 2.4-GHz array setup inside an anechoic chamber. A 2.4-GHz directional transmitter antenna is employed at one end of the chamber to generate a plane wave tone. The transmitter and the receiver array is separated by 2 meters to ensure that the receiver array is in the far field of the transmitter. The transmitter remains fixed and the receiver array is rotated around its center using a precision rotation platform controlled by software to take measurements of the received energy level for different angles. Figure 142 (c) and (d) show a close up of the receiver array and the precision rotation platform used to rotate the array, respectively. The receiver chains, FPGA setup, signal generators and other equipment are placed outside the anechoic chamber. The antenna array feeds the receiver chains via coaxial cables.

Figure 142 (b) shows the signal processing end of the beamformer. Three oscillators are used in the setup. One is used to generate the transmitted 2.4-GHz carrier tone. A “NOISE XT SLC” low jitter clock synthesizer was used to generate the LO signal. The third oscillator was used to clock the ROACH-2 (FPGA) and to perform the sampling of the IF signal. The ROACH-2 FPGA platform was connected to a host Linux server for software control of the measurement setup. The rotation platform motor controller was also connected to the same computer for simultaneous software control via single software integration.

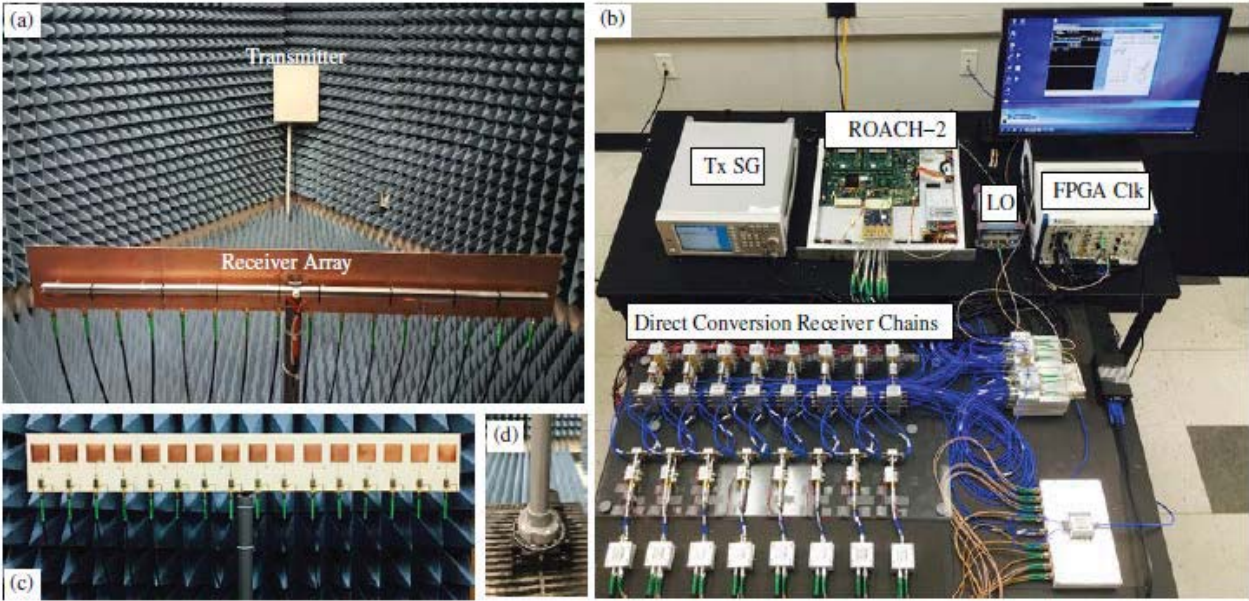


Figure 142: Experimental Setup

(a) Transmitter and receiver in the anechoic chamber, (b) receiver instrumentation setup including the RF receivers, (c) front-view of the antenna array, and (d) rotation platform.

Software End Integration

A fully Python based software controlled system has been developed to perform the beam measurement task in full automated manner on top of the software-to-hardware interface layer provided by the ROACH-2 platform. A sub Python routine was developed to control the motor for precise rotation of the array for beam angle measurements. An “8SMC4-USB” motor controlling platform [8] was used to issue commands from software routines to the platform via a virtual COM-port. ROACH-2 platform provides a middle layer to communicate between the FPGA hardware (memory) by connecting to the on-board computer. ROACH-2 is connected to the main host Linux server through a 1 Gbps ethernet connection. The main Python routine is programmed to access the ROACH-2 platform to perform control functions and read data from the FPGA memory while iteratively scanning through the angles. Altogether, this constitute a fully automated beam measurement setup, allowing all beam measurements can be performed in a single run.

Calibration

Prior to obtaining measurements, the circuits require calibration to achieve proper functionality. Basically, calibration was needed at two main points. First, each RF receiver needed to be calibrated since the mismatches occurred in amplification, mixing and filtering. In addition, calibration of the ADC chips integrated into the ROACH-2 platform was required.

ADC Calibration. Calibration of the ADC chips was performed with calibration scripts provided by CASPER [9]. These scripts facilitated calibration for a reference input signal of the same dynamic range as the actual input. A separate microwave circuit was included in the RF

front end to achieve this and calibration of the RF front ends was achieved as well. The calibration setup is described under “RF Receiver Chain Calibration”.

RF Receiver Chain Calibration. Due to mismatches of the 32 RF chains of the current setup, the outputs to a reference input signal were not uniform. Thus we modified our RF front end to include an additional microwave circuit. This allows calibration of each RF chain digitally using a reference input signal. The RF chain calibration setup is shown in Figure 143. A set of combiners was used at the front of each RF chain to facilitate another reference input to the RF chain.

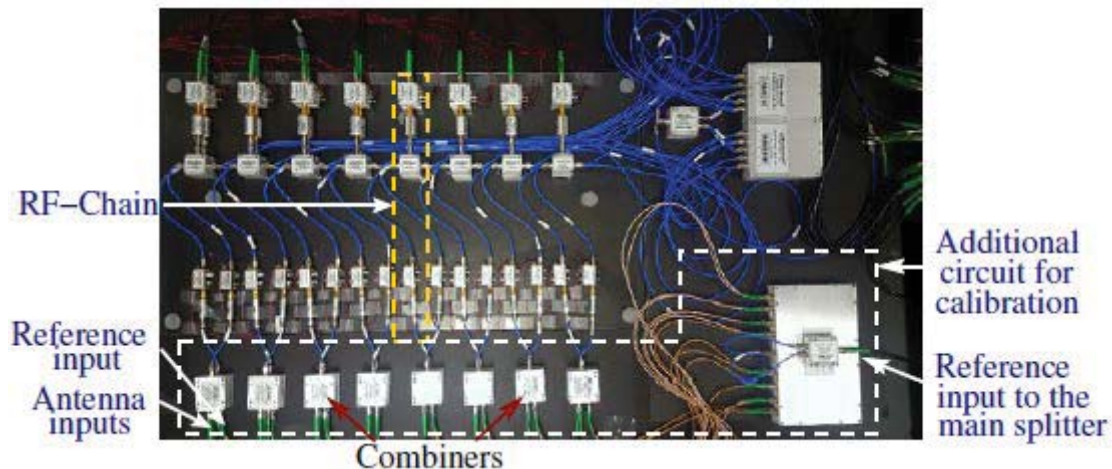


Figure 143: RF-chain Calibration Setup

This step eliminates the need for unscrewing and screwing back the SubMiniature version A (SMA) cables from antenna outputs to each RF chain each time a calibration is needed. These second inputs from each combiner were then connected to a splitter that could feed the same reference signal by splitting 16 channels. Figure 144 shows an illustration of the digital normalization used. Block RAM (BRAM) captured samples for a reference signal of 10 MHz resulting from a reference input signal of 2.4 GHz for each channel as shown in Figure 144 (a). Figure 144 (b) shows the digitally normalized signals that neutralize the effect of mismatches in the RF chain.

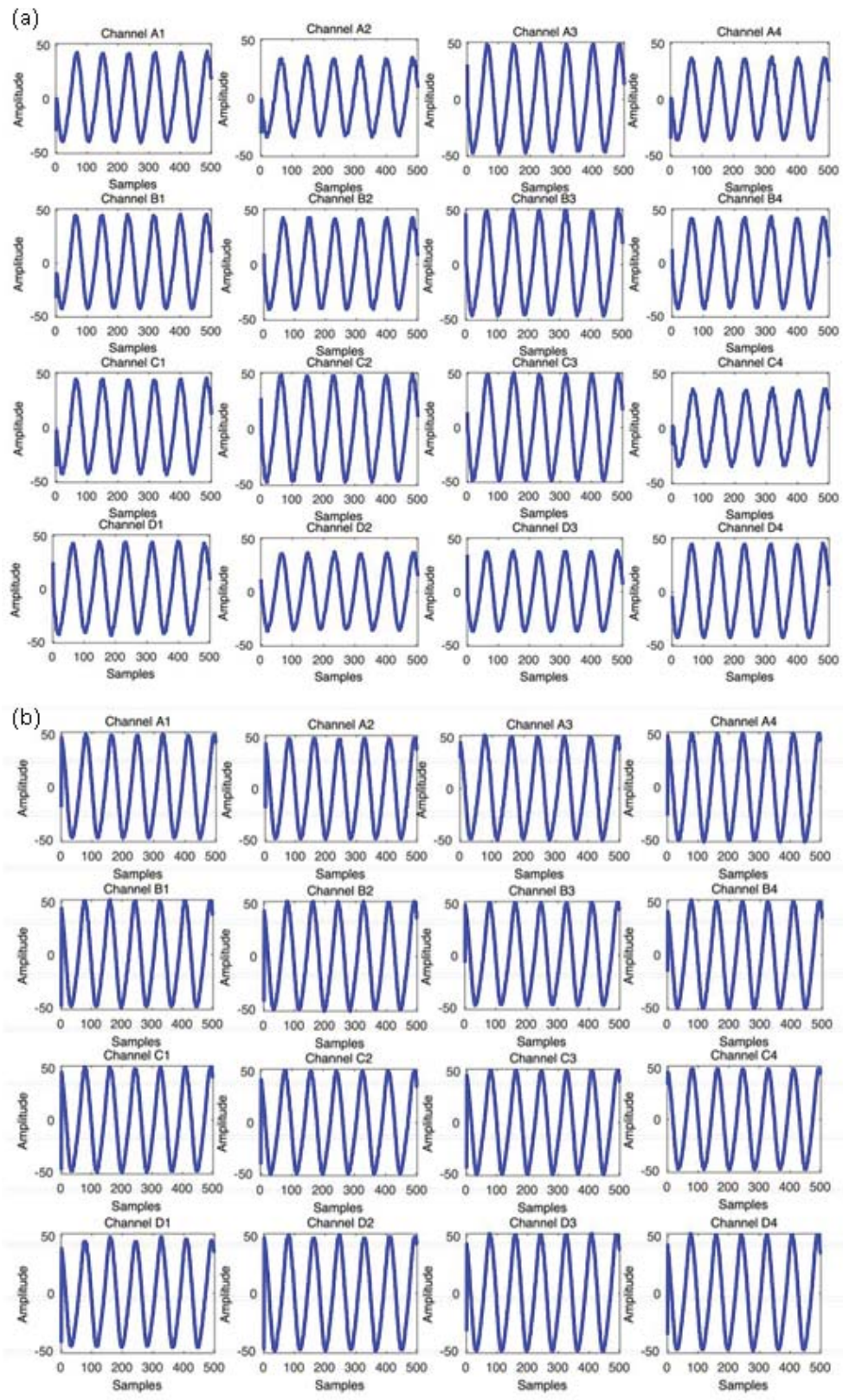


Figure 144: (a) BRAM Captured Reference Signals and (b) Digitally Normalized Signals

Lock-in Amplifier Setup for Obtaining Measurements

The transmitter component of the test setup was modified to realize a lock-in amplifier behavior to improve the measurement from any potential reflections or ambient 2.4-GHz radiation present in the room environment. For this purpose, the transmitting signal was converted to a continuous on-off pulse of a 2.4-GHz signal. Figure 145 (a) shows the block diagram of the hardware configuration used to generate such a transmitted signal. Instead of directly using a 2.4-GHz signal input, a 1.2-GHz signal was used. This signal was modulated to on-off keying by using an IF signal generated from another FPGA board (Xilinx Xtreme DSP kit 4 [10]) via its digital to analog converter (DAC). This signal was then split, mixed, and bandpass filtered to obtain the 2.4-GHz continuous pulse signal. Figure 145 (b) shows the COTS component realization of the transmitted signal generation circuit using commercially available mixers and amplifiers. The energy detector block shown in the digital circuit architecture in Figure 141 was used to detect the presence of the carrier. Figure 145 (c) shows a capture of samples from FPGA corresponding to such a transmission (downconverted).

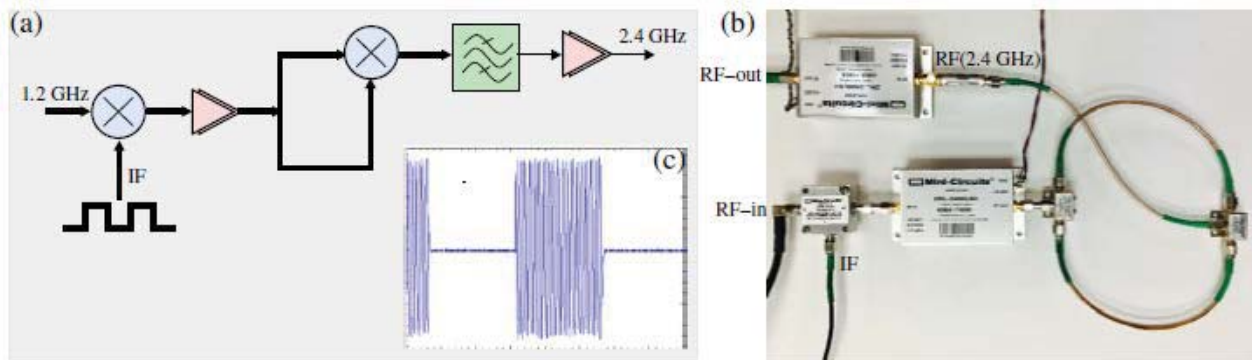


Figure 145: Lock-in Amplifier Design made for generating the Transmitted Signal with On-Off Keying

4.5 Beam Measurement Results

8-point Beam Measurements

The center 8-elements of the 16-element array were used to test and measure the beams obtained using the 8-point approximate transform. The digital design architecture shown in Figure 141 was used with the 8-point digital cores designed. The precision rotor stage was used to obtain the received energy for a resolution of 1° ranging from -65° s to $+65^\circ$ s of array broadside. Once the array is moved to a new position, all the integrators are reset and integration is started on all the beam output signals simultaneously to a preset amount of time (clock cycles). The computed values are then stored in the BRAMs of the FPGA. The Python routine is then used to communicate with the on-board PC on the ROACH-2 platform to read these values to the host PC and then record them.

The process is repeated for each angle according to the rotation resolution used, and the stored values were plotted in Matlab to generate the beam patterns. Same procedure is repeated using both the a-DFT and implemented DFT cores for comparison. Figure 146 shows the plots

generated from the measured values. The digital circuits were clocked at 200 MHz. The LO signal was maintained at 2.410 GHz generating a 10-MHz IF signal to the FPGA ADC inputs. A precision rotor stage was used to aid the precise rotation of the antenna array to record the received energy for different angles as shown in Figure 142. The XIMC multi-platform programming library [8] was used to command the rotation controller via a virtual COM-port interface. A fully Python based software controlled system was developed taking advantage of the software-to-hardware interface layer ROACH-2 provides. The software platforms are programmed to iteratively increment the position angle of the array to produce the beam patterns. Once the array is moved to a new position, all integrators are reset and integration is started on all beam output signals simultaneously for a preset amount of time (clock cycles). The computed values are then stored in the BRAMs of the FPGA. The Python routines are then used to communicate with the on-board PC on the ROACH-2 platform to read these values to the host PC and then record them. The process is repeated for each angle according to the rotation resolution used, and the stored values are plotted in Matlab to generate the beam patterns. The same procedure is repeated using both the a-DFT and implemented DFT cores for comparison. Figure 146 shows the plots arising from the measured values.

Also as a reference, Matlab-simulated beam patterns for each transform (approximate and exact) are also plotted, taking the element pattern into consideration. That is, the resultant beam pattern of the ideal beam pattern resulting from the transform and the element pattern is generated. To make this more realistic, a time domain simulation has been conducted, taking the measured element pattern of each antenna into account by scaling the signal at each antenna element by the gain according to the direction of reception. It should be noted that the plot containing Bin 4 is only shown for completeness. The beam direction for this bin is at the end-fire (90°) which falls into the null direction of each antenna pattern.

Figure 147 shows all the beam patterns in single plots. Figure 147 (a) shows the observed beam patterns using the approximate transform with the use of raw values measured at each bin output. It can be noticed that bins 1,2 and 6,7 do not follow the element pattern due to non-uniform gains inherent in the approximate transform. Figure 147 (b) shows the normalized beam patterns for the same beams in the log domain, where each beam output has been normalized to 1 by dividing by each beam's maximum value. Figure 147 (c) shows the beam patterns observed from the exact FFT implementation. Figure 147 (d) depicts the normalized beam patterns in the log domain. It should be noted that the end-fire beam corresponding to the beam output of bin:4 has been ignored in these plots.

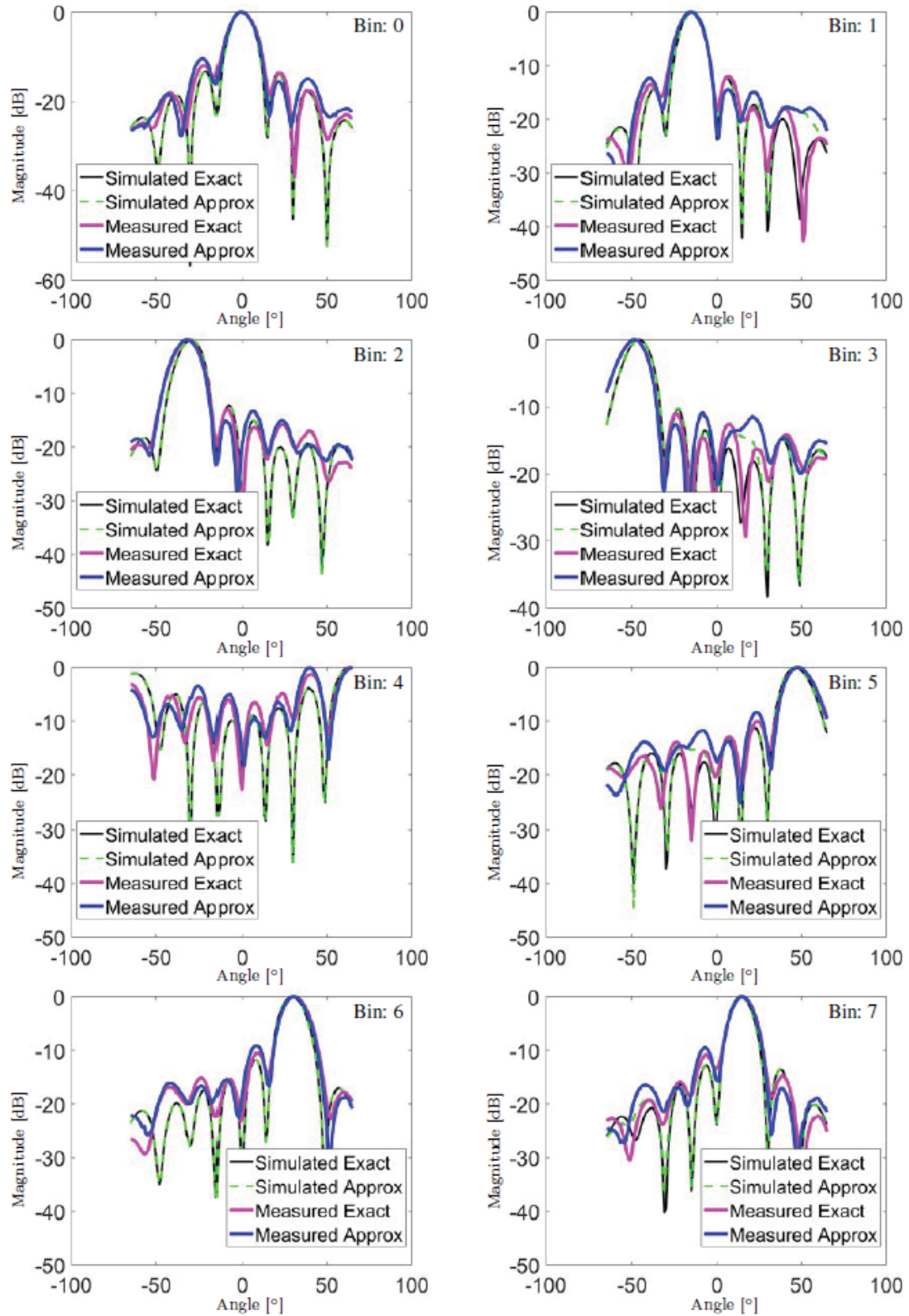


Figure 146: Measured and Simulated Beam Patterns for each Bin of 8-point Approximate and Exact Transforms

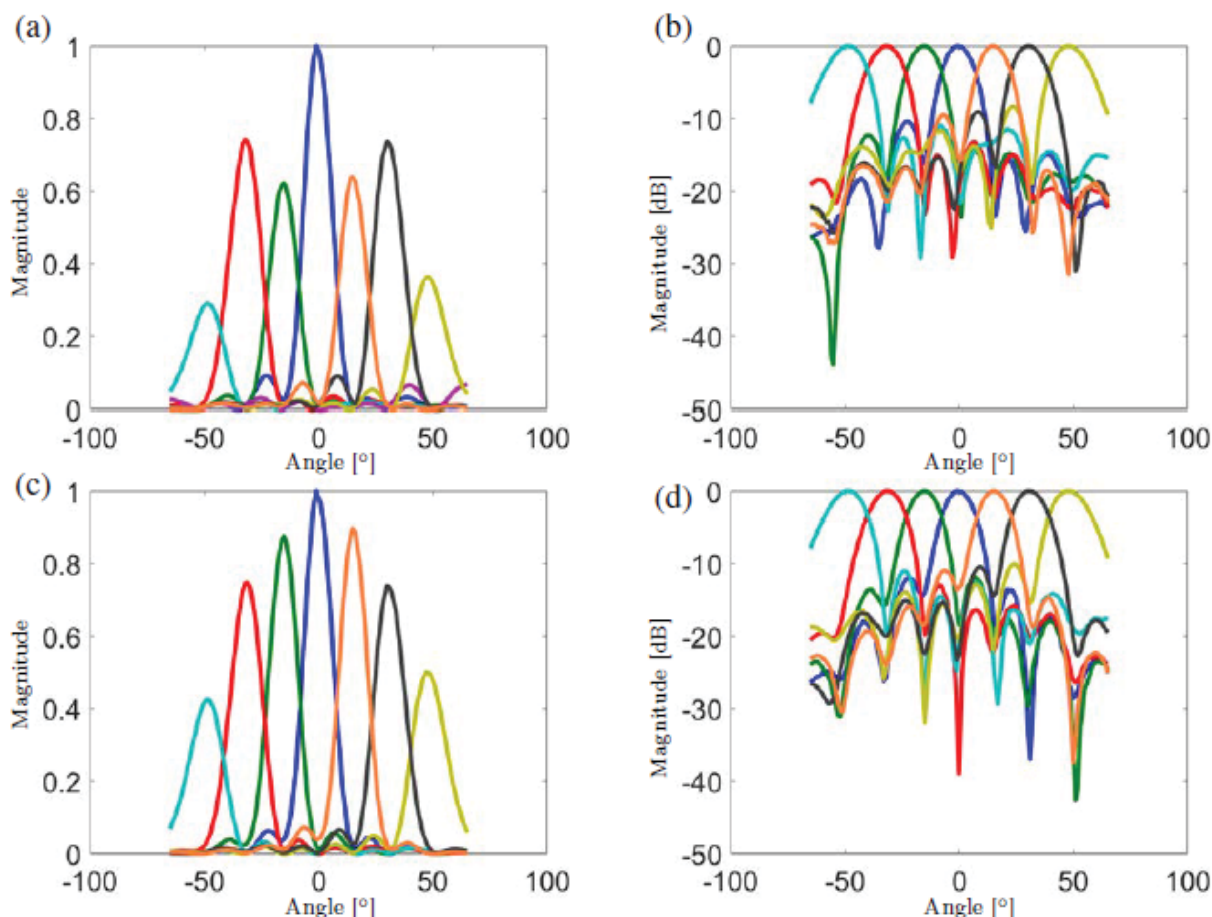


Figure 147: 8-point Beam Patterns in Single Plots

(a) All beam patterns using the approximate transform from the raw values measured at each bin output, (b) the normalized beam patterns in the log domain for the approximate transform, (c) all beam patterns obtained using the exact FFT core, and (d) the normalized patterns of (c) in the log domain.

16-point Beam Measurements

The same measurement procedure was repeated using the full 16-elements of the array to obtain the measurements generated from the 16-point approximate transform. For reference, the beams arising using the exact-FFT digital core were also measured. It is a critical fact that the separation between transmitter and the receiver needs to be high enough to ensure the assumption that a plane wave is received by the array. This is important to obtain a good measurement of the beam patterns. During broadside calibration it was observed that a significant phase deviation existed between the signals captured at two end-fire elements. This is due to the fact that the physical aperture size of the full 16-element array (96 cm) is comparable to the distance between the transmitter and receiver. Figures 148 and 149 show the individual beam plots arising from the measured values for both approximate and exact transforms. The transmitter and the receiver separation is constrained to the dimensions of the anechoic chamber and this issue has affected the side-lobe performance of the measured result. Bin 8 in Figure 149 corresponds to the beam looking at the end-fire which falls into the null direction of each antenna

pattern and is shown only for completeness.

Figure 150 shows all the beam patterns in single plots. Figure 150 (a) shows the observed beam patterns using the approximate transform with the use of raw values measured at each bin output. As for the case of the beams measured for the 8-point approximate transform, it can be noticed that bins do not follow the element pattern due to non-uniform gains inherent in the approximate transform. Figure 150 (b) shows the normalized beam patterns for the same beams in the log domain, where each beam output has been normalized to 1 by dividing from its maximum value. Figure 150 (c) shows the beam patterns observed from the exact FFT implementation. Figure 150 (d) depicts the normalized beam patterns in the log domain. It should be noted that the end-fire beam corresponding to output of bin:8 has been ignored in these plots.

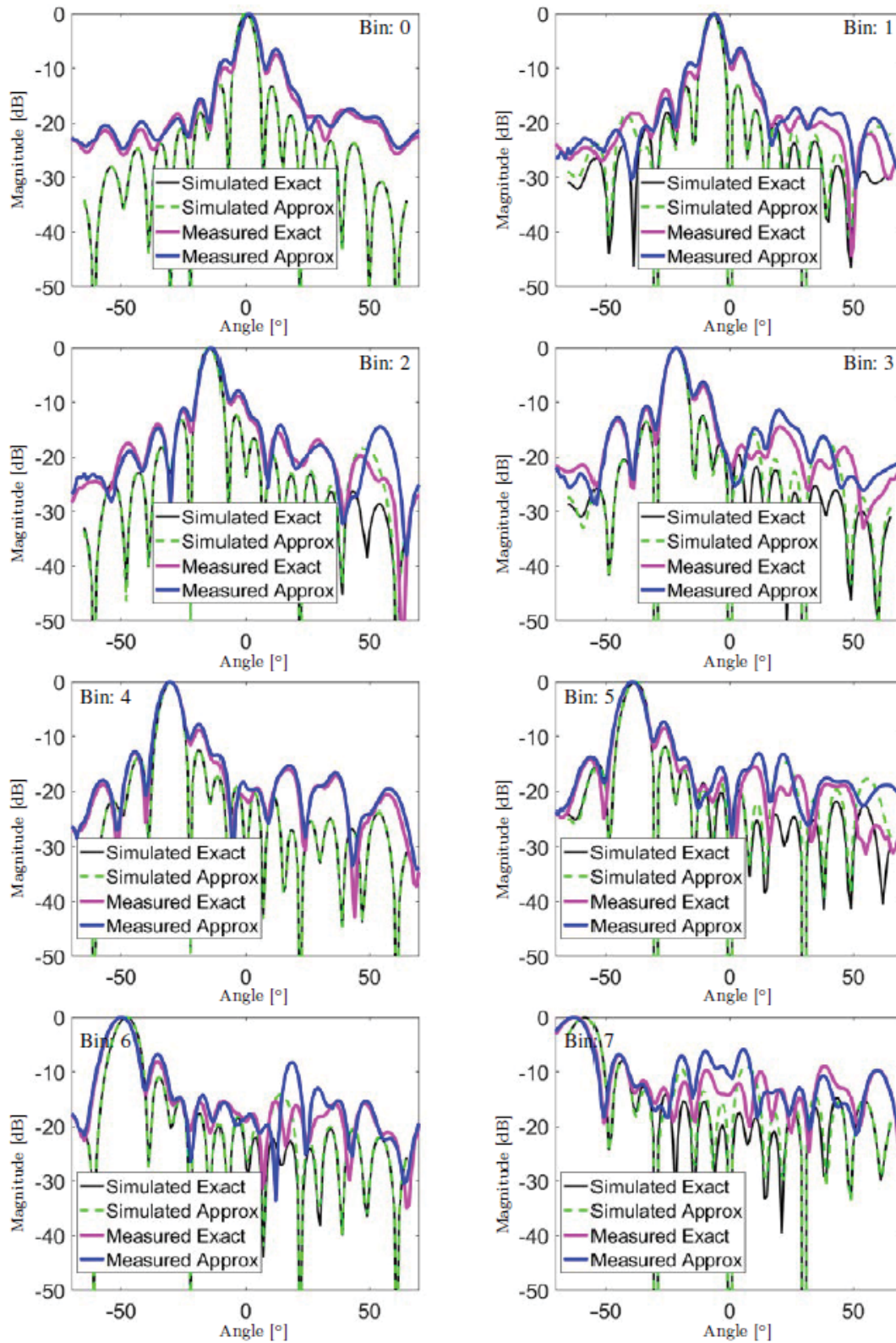


Figure 148: Measured Beam Patterns for Bins 0-7 of 16-point Approximate and Exact Transforms

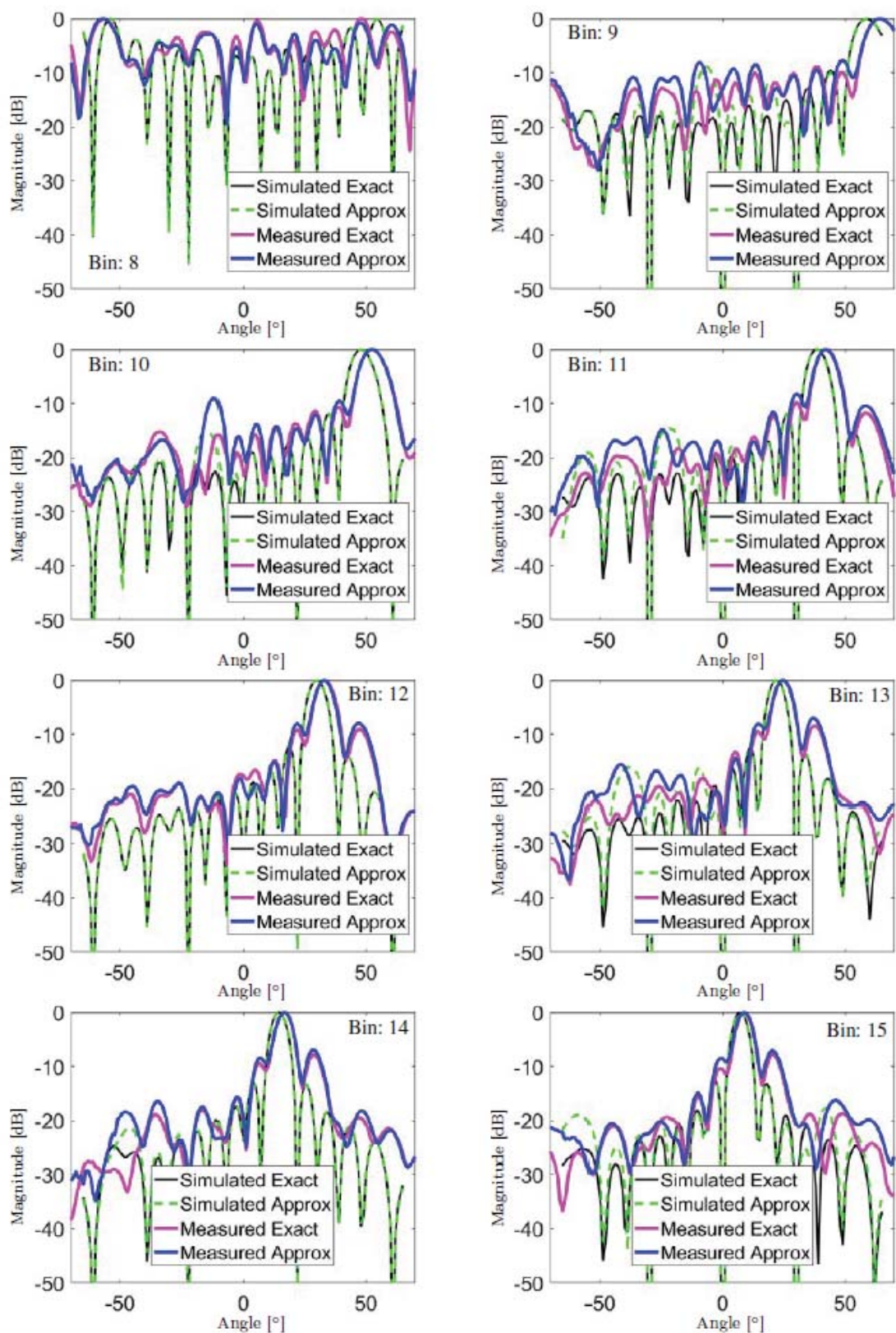


Figure 149: Measured Beam Patterns for Bins 8-15 of 16-point Approximate and Exact Transforms

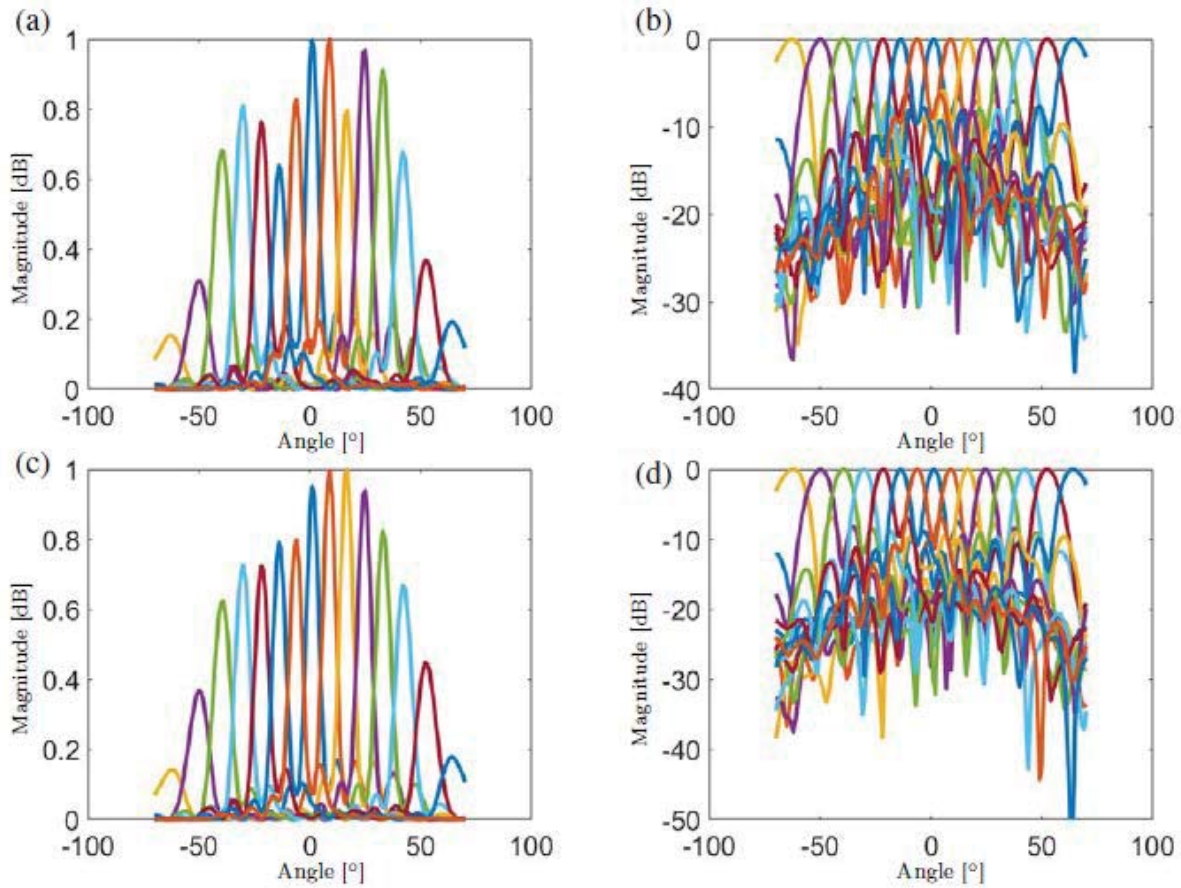


Figure 150: 16-point Beam Patterns in Single Plots

(a) All beam patterns drawn in one plot using the 16-point approximate transform from the raw measured values at each bin's output, (b) the normalized beam patterns (log domain) for the approximate transform, (c) all beam patterns obtained using the exact FFT core, and (d) normalized patterns of (c) in the log domain.

5. FUTURE RESEARCH

Fast cross correlation at massive throughput is a critically important aspect for military systems. Towards realizing fast, precise cross-correlations at massive throughputs (more than one billion parallel cross correlations per second) we reduce the multiplier complexity from $O(N \log N)$ to zero, for small $N \leq 32$ and $O(N \log N)$ to $O(N)$ for large $N > 32$ while maintaining the adder complexity at $O(N \log N)$.

Approximate DFT algorithms would positively impact systems having FFTs as building blocks e.g., radars, cross-correlators, uniform DFT filterbanks, fractional delays, orthogonal-frequency division multiplex (OFDM) systems, and multi-beam arrays. Our a-DFTs are not limited to sparse input signals and are multiplier-free, which leads to small size, weight, and power (SWaP) circuit realizations. Our algorithm is closed-form but trades off DFT-filterbank shapes by a small amount (bounded and with complete theoretical analysis available to understand the trade-offs involved as a function of frequency [bin number], error magnitude and distribution) in order to break the lower bounds of the FFT complexity without the need of sparse inputs. The proposed a-DFTs are suitable for the fastest digital signal processing (at microwave and mm-wave radio frequencies) at low circuit complexity, maximum speed and low power consumption while assuming non-sparse signals. Future studies for DARPA Microsystems Technology Office (MTO) will seek answers to the following scientific questions:

Q1. How can the DFT operation be replaced by a close approximation that does not need any (or significantly reduces the number of) multipliers? What are the suitable fast algorithms for realizing these multiplierless/low complexity DFT approximations at lowest adder complexity for transform sizes in the range of 128 to 4096 FFT points? This research question directly builds on the success of approximated-DFT in 8-, 16-, 32- and, 64-point cases, as explored in the first DARPA MTO seedling project.

Q2. How well do the a-DFTs compare with their exact DFT counterparts in terms of frequency responses of the filterbanks for the larger transforms ($128 \leq N \leq 2048$)? What is the error magnitude and distribution as a function of frequency? What is the trade-off between approximating the DFT and reducing the area on chip as well as power consumption? How can this trade-off be quantified for a scientific comparison and inform design choices by DoD? In particular, we are interested in exploring cross correlation as one of the major practical applications of the proposed approximate-DFT algorithms. The accuracy of the cross-correlation, both in time and frequency domains, will be studied and compared with a baseline for the exact-FFT complex correlation?

Q3. What is the performance trade-off considering finite precision arithmetic in both traditional FFT and the proposed a-DFT algorithms? How does baseline fixed-point FFT cores compare with a- DFT in a design space covering cross- and auto-correlation. For example, correlation function shape, reference thresholds for correlation based decision making, and calculation of power-spectrum.

Q4. How does baseline fixed-point FFT cores compare with a-DFT in a design space covering beam fidelity, pointing accuracy, requantization (digital) noise, area, time, area-time-squared, dynamic power consumption and clock speed ? How can the low-complexity multiplierless approximate-FFT be used in reducing the computational complexity of multirate digital FIR filterbanks? In multirate signal processing, FFT and IFFT are used extensively as vehicle for reducing the computational complexity of polyphase filterbanks. We explore the possibility of replacing the FFT with approximate-FFT and thereby reducing the filterbank complexity even further while making a compromise in filterbank accuracy.

Q5. What are the measured experimental responses and VLSI system implementation metrics for the proposed aperture multi-beam forming, multirate filter-banks and fast cross-correlation method?

Q6. When the input is totally real valued, can we replace a-DFT with sparse factor implementations of approximate discrete Hartley transforms (a-DHTs) and therefore obtain additional savings in multiplier complexity for fast complex correlators? Preliminary results indicate this is indeed possible, and that an additional saving of complexity by up to 50% over what we expect by adopting a-DFTs in place of FFTs may in fact be feasible for cross correlation.

Future work will involve the following:

- Recursive twiddle-factor quantization: consider fast algorithms for the DFT ($N \geq 32$) and optimally map the multiplicands into low-complexity dyadic rationals. An initial mapping would be to directly find the closest rational approximation to each multiplicand. Such an approach does not take into account the interplay among the multiplicands. Such relations have a significant role in finding good approximations. Therefore, mapping derived from multivariate analysis and multi-criteria optimization schemes might be sought.
- Hybrid transformation algorithms: combination of an approximate-DFT and exact FFT factorization towards yielding low-complexity and exceptionally large transform sizes which are intractable to derive using direct numerical search methods. In the first seedling, we searched and found three optimized versions of multiplierless approximations for the 32-point FFT. These a-FFT algorithms do not require any multiplications and are able to maintain the number of additions similar to available exact-FFTs (e.g., Duhamel algorithm). We will explore the use of Cooley-Tukey algorithm while starting from the multiplierless 32-point a-FFT such that larger sized a-FFTs can be found. In preliminary work, we have explored the use of this approach to create a 1024-point a-FFT (see Figure 151) that reduces the number of multipliers from $O(N \log_2 N)$ down to $O(N)$. Although this preliminary algorithm is not entirely multiplierless, it offers tremendous savings in hardware and power consumption by removing about 90% of the parallel multiplier circuits that would be needed if a 1024-point exact FFT was to be designed in digital VLSI. For example, for $N = 1024$, the exact FFT requires about 10240 parallel multipliers, while our preliminary algorithms require at most 1024 multipliers. This is an order of magnitude reduction in the number of multipliers on chip.

- Linear/quadratic optimization for approximate-DFT derivation: For larger transforms, such as $N = 1024$, the computational search space is $3^{1024 \times 1024} \approx 7.9 \cdot 10^{500297}$ - an intractably huge number. Therefore, when moving to large values of N , we will adopt a new scheme in this seedling project where we use methods based on linear/quadratic optimization to derive DFT-approximations for large block lengths ($N \geq 32$).

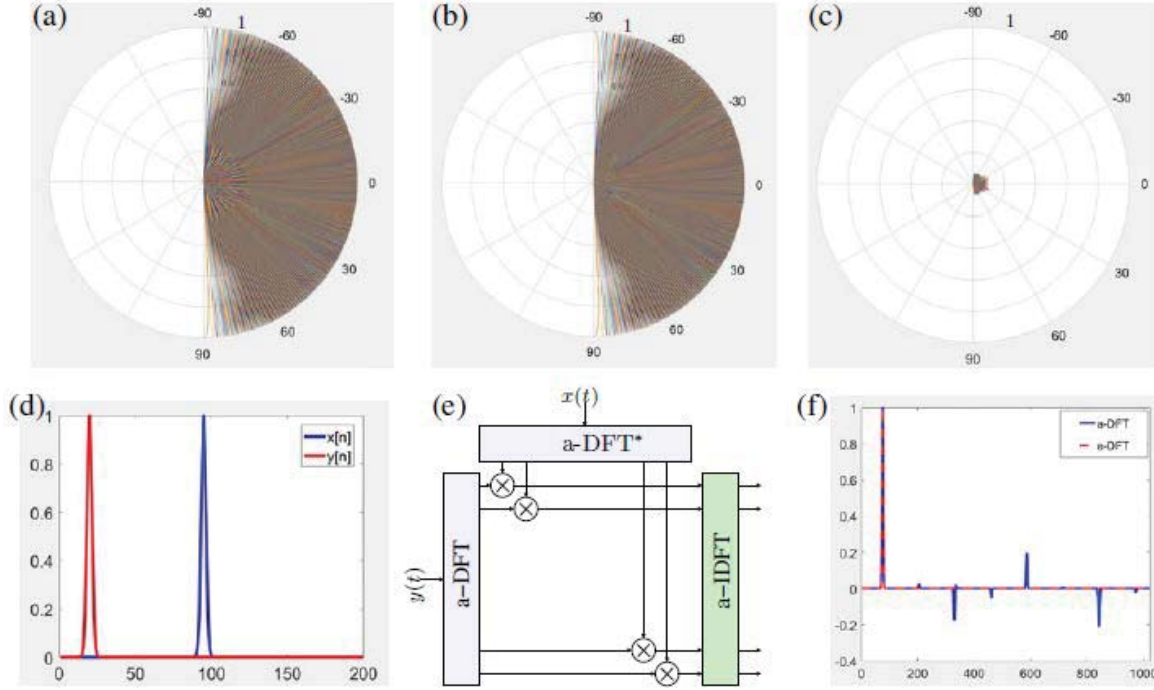


Figure 151: 1024-point Magnitude Beam Responses

(a) 1024-point a-DFT magnitude beam responses, (b) 1024-point magnitude exact-FFT beam responses, (c) differences in a-DFT and exact-DFT beams ($N = 1024$), (d) two pulses with time-delay, (e) a-DFT based complex correlator, and (f) cross-correlator outputs for approximate-DFT and exact-DFT.

Example: High-Throughput Approximate-FFT Cross-Correlation. Low complexity cross correlators suitable for massive computation can be derived from approximate-FFT algorithms by means of the convolution theorem. We know that FFTs are used for reducing the complexity of cross correlation in the time-domain ($O(N^2)$) down to $O(N \log N)$ in the Fourier domain. We reduce the correlation complexity even further, by reducing the multiplier complexity of the a-FFT down to $O(N)$. For a test case where $N = 1024$, this implies a dramatic 70 – 90% smaller VLSI circuit and power consumption over conventional FFT-based cross correlator designs. For a predicted clock frequency of 1 GHz, this implies that, for pipelined systolic digital CMOS realizations, the real-time throughput level is 1 billion 1024-point cross-correlations per second.

The replacement of the FFT with the proposed N -point approximate-FFT algorithms for large N reduces the multiplier complexity values for both cases to $O(N)$ without increase in adder complexity. In VLSI (45-nm CMOS) – a parallel (complex) multiplier can be about $\alpha = 10$ times larger in chip area compared to a (complex) adder, which implies that for $N \geq 1024$, the fractional savings in VLSI area can be an order of magnitude.

6. CONCLUSIONS

The use of approximate computing towards computing DFT was investigated with digital array processing for antenna beamformers in mind. Starting from 8-point DFT, the approximations for 16, 32 and 64 point DFT were proposed and evaluated in simulation. These proposed approximations reduce the required number of multipliers to zero. A new low-complexity approximate-DFT for 1024 points was also proposed. This approximation is also factorized, and employs 1024 multipliers.

For the approximate-DFT algorithms proposed, a sparse factorization has been found that reduces the adder complexity. Theoretical performance has been quantified with respect to the exact FFT implementation, and frequency bin-wise analysis has been given. The multiplierless transforms reduce the well-known $O(N\log N)$ multiplier complexity of FFT algorithms to zero for an N -point transform. The approximate transforms found have been implemented on FPGA using the sparse factorizations found for each case which leads to reduce the adder complexity implementations with zero multipliers used. Exact counter parts of each size of FFT were also implemented for comparison. The hardware resource utilization figures have been reported for both approximate and exact cases. The use of the approximate transforms for multi-beamforming in linear and aperture arrays was studied. Theoretical and numerical analysis was conducted for both 1-D and 2-D cases for analyzing the performance of the beams and side-lobes. Several examples have been shown confirming the adoptability of the proposed transforms in multi-beamforming applications.

A 2.4-GHz receive-mode multi-beamforming system was implemented in the lab to obtain the measured beam patterns arising from the proposed approximate transforms for verification of the algorithms. A 16-element linear patch antenna array was designed and build using Nyquist element spacing. 16 IQ direct conversion receiver chains were implemented using commercially available off the shelf components. The downconverted signals in the chains were then sampled and processed using ROACH-2 FPGA processing platform. The 8-point and 16-point approximate transforms were used in FPGA designs to calculate and measure the beam patterns from the constructed setup. The detailed description of the beamforming setup has been given and the measured beam patterns have been reported. The beam patterns arising from the exact DFT designs have also been measured and presented for comparison. It can be seen that the measured patterns for the approximate transform closely follow the beams obtained for the exact FFT-versions.

7. REFERENCES

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
ADC	analog-to-digital conversion
a-DFT	approximate-discrete Fourier transform
AESA	active electronically scanned array
AFRL	Air Force Research Laboratory
BRAM	block RAM
CASPER	Collaboration for Astronomy Signal Processing and Electronics Research
CLB	configuration logic block
CMOS	complementary metal-oxide-semiconductor
COTS	commercial off-the-shelf
DAC	digital to analog converter
DAR	digital array radar
DARPA	Defense Advanced Research Projects Agency
demux	demultiplexer
DFT	discrete Fourier transform
DSP	digital signal processing
FFT	fast Fourier transform
FPGA	field-programmable gate array
I	in-phase
IF	intermediate frequency
IQ	in-phase quadrature
LNA	low noise amplifier
LO	local oscillator
MTO	Microsystems Technology Office
OFDM	orthogonal-frequency division multiplex
PI	Principal Investigator
Q	quadrature
RA	Research Assistant
RF	radio frequency
ROACH	Reconfigurable Open Architecture Computing Hardware
SCR	software controllable register
SMA	SubMiniature version A
SWaP	size, weight, and power
ULA	uniform linear array
VLSI	very-large-scale integration