



AFRL-RY-WP-TR-2017-0115

ADVANCED TECHNOLOGY FOR ULTRA-LOW POWER SYSTEM-ON-CHIP (SoC)

Jason Woo, Weicong Li, and Peng Lu

University of California, Los Angeles

**JUNE 2017
Final Report**

Approved for public release; distribution unlimited.

See additional restrictions described on inside pages

STINFO COPY

**AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320
AIR FORCE MATERIEL COMMAND
UNITED STATES AIR FORCE**

NOTICE AND SIGNATURE PAGE

Using Government drawings, specifications, or other data included in this document for any purpose other than Government procurement does not in any way obligate the U.S. Government. The fact that the Government formulated or supplied the drawings, specifications, or other data does not license the holder or any other person or corporation; or convey any rights or permission to manufacture, use, or sell any patented invention that may relate to them.

This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with SAF/AQR memorandum dated 10 Dec 08 and AFRL/CA policy clarification memorandum dated 16 Jan 09. This report is available to the general public, including foreign nationals.

Copies may be obtained from the Defense Technical Information Center (DTIC)
(<http://www.dtic.mil>).

AFRL-RY-WP-TR-2017-0115 HAS BEEN REVIEWED AND IS APPROVED FOR
PUBLICATION IN ACCORDANCE WITH ASSIGNED DISTRIBUTION STATEMENT.

// Signature//

ALFRED J. SCARPELLI, Program Manager
Advanced Sensor Components Branch
Aerospace Components & Subsystems Division

// Signature//

BRADLEY J. PAUL, Chief
Advanced Sensor Components Branch
Aerospace Components & Subsystems Division

// Signature//

TODD W. BEARD, Lt Col, USAF
Deputy
Aerospace Components & Subsystems Division
Sensors Directorate

This report is published in the interest of scientific and technical information exchange, and its publication does not constitute the Government's approval or disapproval of its ideas or findings.

*Disseminated copies will show “//Signature//” stamped or typed above the signature blocks.

REPORT DOCUMENTATION PAGE					Form Approved OMB No. 0704-0188	
The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.						
1. REPORT DATE (DD-MM-YY) June 2017		2. REPORT TYPE Final		3. DATES COVERED (From - To) 22 September 2015 – 31 March 2017		
4. TITLE AND SUBTITLE ADVANCED TECHNOLOGY FOR ULTRA-LOW POWER SYSTEM-ON-CHIP (SoC)				5a. CONTRACT NUMBER FA8650-15-1-7574		
				5b. GRANT NUMBER		
				5c. PROGRAM ELEMENT NUMBER 61101E		
6. AUTHOR(S) Jason Woo, Weicong Li, and Peng Lu				5d. PROJECT NUMBER 1000		
				5e. TASK NUMBER N/A		
				5f. WORK UNIT NUMBER Y1DZ		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) University of California, Los Angeles 420 Westwood Plaza Los Angeles, CA 90095-1594				8. PERFORMING ORGANIZATION REPORT NUMBER		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Force				10. SPONSORING/MONITORING AGENCY ACRONYM(S) AFRL/Rydi		
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S) AFRL-RY-WP-TR-2017-0115		
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.						
13. SUPPLEMENTARY NOTES This report is the result of contracted fundamental research deemed exempt from public affairs security and policy review in accordance with SAF/AQR memorandum dated 10 Dec 08 and AFRL/CA policy clarification memorandum dated 16 Jan 09. This material is based on research sponsored by Air Force Research laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) under agreement number FA8650-15-1-7574. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation herein. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies of endorsements, either expressed or implied, of Air Force Research Laboratory (AFRL) and the Defense Advanced Research Agency (DARPA) or the U.S. Government. Report contains color.						
14. ABSTRACT The purpose of this advanced study is to provide an analytic framework for silicon on chip (SoC) technology that is based on numerical, simulation, and experimental analysis, with the aim to realize the radio frequency/analog devices in the Fin Field Effect Transistor (FinFET) platform and to provide the tunneling FinFET feasibility study for future ultra-low power digital applications.						
15. SUBJECT TERMS group IV tunnel field effect transistors, radio frequency metal-oxide-semiconductor field-effect transistor design						
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT: SAR	18. NUMBER OF PAGES 28	19a. NAME OF RESPONSIBLE PERSON (Monitor) Alfred Scarpelli	
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER (Include Area Code) N/A	

Table of Contents

Section	Page
List of Figures	ii
List of Tables	iii
1. SUMMARY.....	1
2. INTRODUCTION	2
2.1 Group IV Tunnel Field Effect Transistors Optimization.....	2
2.2 Analog Performance Optimization for 14nm Node FinFETs.....	2
3. METHODS, ASSUMPTIONS, AND PROCEDURES.....	3
3.1 Group IV Tunnel Field Effect Transistors Optimization.....	3
3.2 Analog Performance Optimization for 14nm Node FinFETs.....	9
4. RESULTS AND DISCUSSIONS.....	12
4.1 Group IV Tunnel Field Effect Transistors Optimization.....	12
4.2 Analog Performance Optimization for 14nm Node FinFETs.....	12
5. CONCLUSION.....	17
6. REFERENCES	18
LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS	20

List of Figures

Figure	Page
Figure 1: Experimental Results of State-of-the-Art TFETs.....	3
Figure 2: Key Limitations of Previous TFETs	3
Figure 3: Schematic of Calibrated SiGe/Si RITD.....	4
Figure 4: (a) Simulated Band Diagram of SiGe/Si RITD and (b) Calibrated Simulation Compared to Experiment	4
Figure 5: Schematics of Proposed Ge-pocket TFET with Design Parameters	5
Figure 6: I_{on}/I_{off} Ratio as a Function of L_g/λ	5
Figure 7: I_{on} for Ge-pocket TFET as a Function of Source Doping	6
Figure 8: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations Under $V_{GS}=0V$ and $V_{GS}=0.5V$ and (b) I_{on} as a Function of Pocket Doping Concentration.....	6
Figure 9: I_{on} of Ge-pocket with Different Channel Doping Concentrations.....	7
Figure 10: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations Under $V_{GS}=0V$ and $V_{GS}=0.5V$ and (b) I_{on} as a Function of Pocket Doping Concentration Optimum Drain Doping Concentration.....	7
Figure 11: Benchmark of Optimized Ge-pocket TFET against State-of-the-Art FinFETs in Terms of I_{on}	8
Figure 12: I_{on} for Ge-pocket TFETs with Different t_{pocket} and CG	8
Figure 13: I_{on} for Ge-pocket TFET with Different Source Doping Gradient and Pocket Doping Concentration with Pocket Doping Gradient of 5nm/dec.....	9
Figure 14: (a) Experimental FinFET Published by Intel [1] and (b) the Simulated Structure.....	9
Figure 15: Experimental Data vs. Simulated I-V Curves with Calibrated Mobility Model	10
Figure 16: Double Gated FET with Graded Channel	11
Figure 17: Optimized Doping and Ge Mole Fraction Profile along Channel Length Direction	13
Figure 18: (a) Electron Density Profile and (b) Velocity Profile in Channel Length Direction at 1nm from Channel Surface	14
Figure 19: Simulated g_{m_ext} of Optimized GC FinFET vs. 14nm-node FinFET Experimental Data published by Intel.....	14
Figure 20: Conduction Band Profiles along the Channel at 1nm from Gate Dielectric for Graded Channel Device and Homojunction Device	14
Figure 21: Output Resistance of Graded Channel and Homojunction Devices.....	15
Figure 22: (a) Long Channel MOSFET [9], (b) Short Channel MOSFET [10], and (c) Simulated Structure	15
Figure 23: C_G vs EOT for Silicon SOI and InGaAs MOSFET.....	16
Figure 24: g_m vs EOT for Silicon SOI and InGaAs MOSFET	16

List of Tables

Table	Page
Table 1. Projected Device Parameters Based on $\lambda=L_g/7$	5
Table 2. Design Parameters of 14nm-node FinFET	10
Table 3. Process Flow for SiGe RITD	12
Table 4. Design Parameters of the Purposed GC FinFET	13

Acknowledgement

The authors would also like to thank Janet Lin for proofreading and editing the final technical report.

1. SUMMARY

While tunnel field effect transistors (TFETs) have been extensively examined by many research groups in the past few years, TFETs have not shown significant performance advantages. These devices limitations were carefully analyzed in this project. Based on the understanding of the limitations of previous TFETs, Ge-pocket TFET was proposed for lower power applications with $I_{\text{off}}=10\text{pA}/\mu\text{m}$ and $V_{\text{DD}}=0.5\text{V}$. In this project, the optimized structure shows great potential in both L_g and V_{DD} scaling. The process flow for the proposed Ge-pocket TFET was designed. Vertical structure was adopted to demonstrate the concept of Ge-pocket TFET because of the need for sharp doping/composition gradient.

While fin field effect transistors (FinFETs) have shown great performance advantage over planar metal-oxide-semiconductor field-effect transistors (MOSFETs) for low power/high performance digital complementary metal-oxide-semiconductor (CMOS), their analog and radio frequency (RF) performance have major limitations and need to be enhanced by alternative engineering. FinFET analog performance optimization by graded channel (GC) design is examined. The analyses are carried out using the Sentaurus technology computer-aided design (TCAD) simulations. Doping profile in the source/drain (S/D) extension region is optimized to minimize extension parasitic resistance while avoiding increasing drain-induced barrier lowering (DIBL). SiGe/Si heterojunction leads to a more uniform electron distribution along the channel length direction compared with homojunction (Si) device, and thus improves $g_{m_{\text{int}}}$ and $DIBL$. An improvement of 100% in $g_{m_{\text{ext}}}$ has been achieved by the GC design at $I_{\text{DS}}=1\text{mA}/\mu\text{m}$ compared with that in experimental 14nm-node FinFET. The redistributed electric field along the channel length direction can result in a 20% better $DIBL$ and a 65% larger output resistance compared with experimental data. It has also been demonstrated that a further improvement in transconductance exists when switching channel material from silicon to InGaAs for the latest MOSFET generation.

2. INTRODUCTION

2.1 Group IV Tunnel Field Effect Transistors Optimization

TFET has been studied as an alternative for low power logic device in the past decade. So far, sub-thermal subthreshold swing (SS) and high I_{on} have been demonstrated experimentally on separate platforms. It is essential to combine these two desirable traits and develop a TFET with sub-thermal SS over 5 decades of I_{DS} and I_{on} comparable to International Technology Roadmap for Semiconductors (ITRS) Low Standby Power (LSTP) standards. In order to achieve this goal, the issues of previous TFETs have been pinpointed; Ge-pocket TFET, a very-large-scale integration (VLSI) -compatible solution, has been proposed.

2.2 Analog Performance Optimization for 14nm Node FinFETs

It has been widely accepted that transistor's external transconductance (g_{m_ext}) is affected by parasitic resistance and carrier transport. To the first order, the g_{m_ext} can be predicted by the following equations:

$$g_{m_ext} = \frac{g_{m_int}}{1 + g_{m_int} \cdot R_{parasitics}} \quad (1)$$

where g_{m_int} is the intrinsic trans-conductance and $R_{parasitics}$ is the source parasitic resistance. Cut-off frequency (f_T), which is a crucial parameter for analog performance, is related to g_{m_ext} by the equation:

$$f_T = \frac{g_{m_ext}}{2\pi \cdot C} \quad (2)$$

where C is the total gate capacitance. In 14nm node FinFET, C is dominated by interconnect capacitance, which can only be reduced in the back end process. Consequently, in the front end process, there are two possible ways to improve g_{m_ext} and thus f_T , improving g_{m_int} and reducing R_S . We demonstrate that both of these goals can be achieved by the GC concept and discuss the possibility of using high mobility InGaAs as channel material to further improve analog performance.

3. METHODS, ASSUMPTIONS, AND PROCEDURES

3.1 Group IV Tunnel Field Effect Transistors Optimization

Limitations of Previous TFETs

To identify the key physics bottlenecks of previously TFETs, the experimental results of three state-of-the-art TFETs were studied (Figure 1).

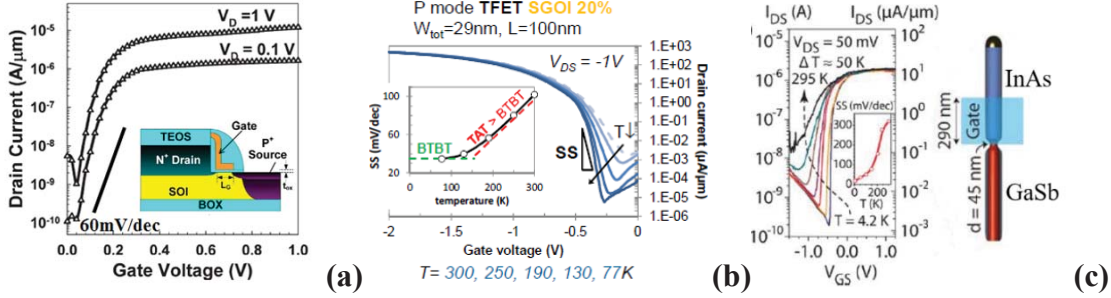


Figure 1: Experimental Results of State-of-the-Art TFETs

(a) SOI ($t_{ox}=2\text{nm}$, $L_g=70\text{nm}$, and $t_{soi}=70\text{nm}$) [1]; (b) tri-gate with SiGe source (equivalent oxide thickness (EOT) = 1.25nm , and $L_g=100\text{nm}$) [2]; and (c) nanowire with InAs/GaSb broken-gap (EOT = 1.3nm , and $d=45\text{nm}$) [3]

N-TFET with Sub-60mV/dec SS at room temperature was first realized on silicon on insulator (SOI) platform (Figure 1(a)). The device exhibits SS as low as 53mV/dec and I_{on} of $12.1\mu\text{A}/\mu\text{m}$ with $V_{DD}=1\text{V}$. The small I_{on} is due to the large tunneling resistance at source/channel junction as well as the small tunneling area.

Tri-gate p-TFET with SiGe source has demonstrated I_{on} of $190\mu\text{A}/\mu\text{m}$ under $V_{DD}=-0.9\text{V}$, which is one order of magnitude higher than the SOI n-TFET thanks to the small bandgap of SiGe and better electrostatic control. However, the average SS is approximately 80mV/dec and the degradation is likely due to the trap-assisted tunneling (TAT) at source/channel junction (Figure 2).

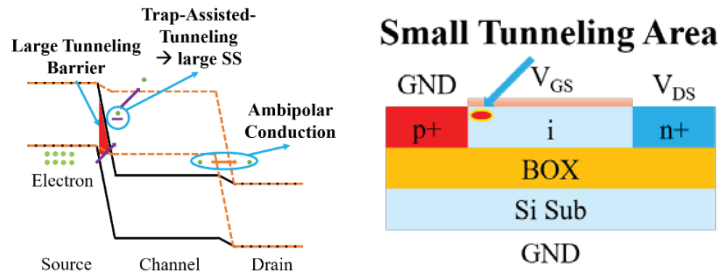


Figure 2: Key Limitations of Previous TFETs

Nanowire n-TFET with InAs/GaSb broken-gap exhibits $I_{on}=62 \mu A/\mu m$ with $V_{DS}=0.3V$ and $V_{GT}=0.5V$ thanks to the small tunneling barrier. SS is significantly degraded compared with group IV-based TFET due to material defect from immature material synthesis and fabrication process. Ambipolar conduction is also observed.

Previous TFETs suffer from four major limitations as shown in Figure 2.

Tunneling Model Calibration

Dynamical nonlocal band-to-band tunneling model was adopted for simulation, which calculates the tunneling path dynamically by following the gradient of valence band profile. The tunneling rate is computed by using Kane's model. The model provides a deep physical insight into TFETs operation, and gives good fits to both I_{on} and SS with two fitting parameters, A and B.

A Si/SiGe resonant interband tunneling diode (RITD) [4] was used for calibration (Figure 3).

5 nm n ⁺ Si
P δ -doping plane
104 nm n ⁺ Si
P δ -doping plane
1 nm undoped Si
1.5 nm undoped Si _{0.45} Ge _{0.55}
B δ -doping plane
1 nm p ⁺ Si _{0.45} Ge _{0.55}
264 nm p ⁺ Si
p- Si Substrate (3000-8500 Ω -cm)

Figure 3: Schematic of Calibrated SiGe/Si RITD

Quantization effect has been incorporated into the simulation by using Poisson Schrodinger solver. The quantization modifies the electrostatic potential profile and gives rise to subband. The formation of subband will modify the tunneling path (Figure 4(a)). The calibrated simulation shows a good agreement with experiment data (Figure 4 (b)).

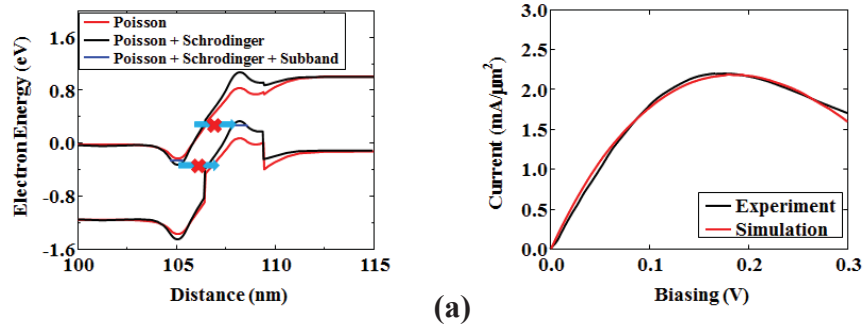


Figure 4: (a) Simulated Band Diagram of SiGe/Si RITD and (b) Calibrated Simulation Compared to Experiment

Proposed Structure

Based on the previous limitations on SiGe-based TFET, Ge-pocket TFET is proposed (Figure 5). Strained-Ge pocket is only adopted at the tunneling junction to enhance the tunneling probability. SiGe is chosen over Ge for source material because of the reduction in the strain, which allows a thicker defect-free SiGe layer. This is essential for steep switching behavior. Ge-pocket TFET is designed for lower power application with $I_{off}=10\text{pA}/\mu\text{m}$ and $V_{DD}=0.5\text{V}$.

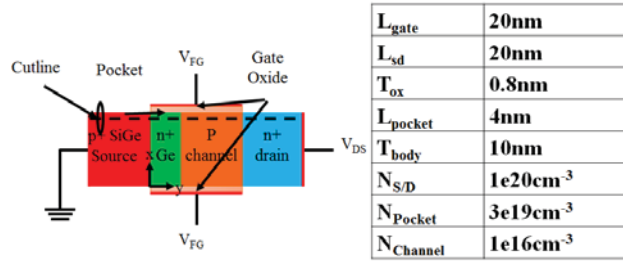


Figure 5: Schematics of Proposed Ge-pocket TFET with Design Parameters

Scalability

In order to study the scalability of the proposed structure, the concept of natural length was adopted. The natural length is given by:

$$\lambda = \sqrt{\frac{1}{2} \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{si} t_{ox}}$$

Device with different combinations of t_{si} and t_{ox} were simulated. The I_{on}/I_{off} is plotted against the ratio of L_g/λ (Figure 6). I_{on}/I_{off} increases as the ratio increases, and saturates when the ratio exceeds 8. A minimum ratio of 7 is needed to provide the necessary I_{on}/I_{off} for the proposed structure to be competitive against state-of-the-art FinFET technology. Based on the assumption that $L_g/\lambda=7$, the projected device parameters are given in Table 1.

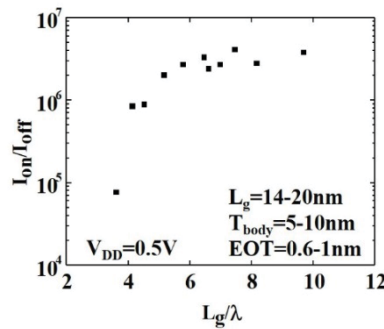


Figure 6: I_{on}/I_{off} Ratio as a Function of L_g/λ

Table 1. Projected Device Parameters Based on $\lambda=L_g/7$

L_g (nm)	20	16	14
EOT (nm)	0.8	0.7	0.6
T_{body} (nm)	8	5	5

Doping Optimization

Tunneling is sensitive to band profile and thus it is essential to investigate the impact of doping concentration on the proposed TFET's performance. Doping concentrations at all four regions, source, pocket, channel, and drain, have been optimized to improve I_{on} .

The impact of increasing Ge-pocket TFET's source doping is twofold. On the one hand, the tunneling probability is enhanced at source/pocket due to a higher electric field across it. On the other hand, the quasi-Fermi level of hole in the source region moves further away from the valence band edge, where electric field peaks. The optimum source doping concentration is determined to be $2 \times 10^{20} \text{ cm}^{-3}$ (Figure 7).

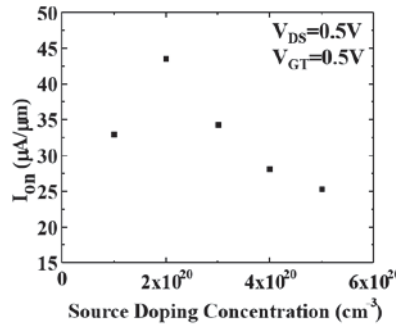


Figure 7: I_{on} for Ge-pocket TFET as a Function of Source Doping

$V_{GT}=V_{GS}-V_{TH}$ and $I_{DS}=10 \text{ pA}/\mu\text{m}$ under $V_{DS}=0.5 \text{ V}$ and $V_{GS}=V_{TH}$ for each device

The insertion of counter-doped pocket significantly increases the electric field across the tunneling junction, thus leading to an improvement in I_{on} [5]. However, a tunneling window will open even at off-state when increasing pocket doping beyond $4 \times 10^{19} \text{ cm}^{-3}$. This leads to a significant increase in leakage current (Figure 8(a)). Taking both effects into consideration, the optimum pocket doping concentration is $4 \times 10^{19} \text{ cm}^{-3}$ (Figure 8(b)).

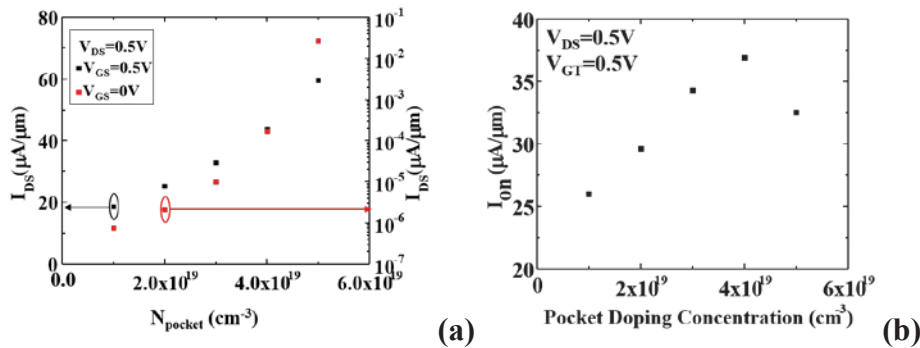


Figure 8: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations under $V_{GS}=0\text{V}$ and $V_{GS}=0.5\text{V}$ and (b) I_{on} as a Function of Pocket Doping Concentration

Due to the thin body nature of double-gate structure and light channel doping, the channel of Ge-pocket TFET is virtually undoped. The impact of channel doping is negligible (Figure 9).

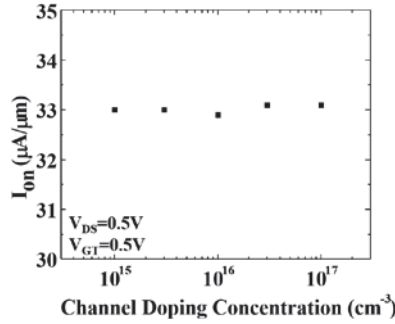


Figure 9: I_{on} of Ge-pocket with Different Channel Doping Concentrations

At off-state, increasing drain doping concentration leads a higher electric field penetrating into the channel region, and it lowers the conduction in the channel, which gives rise to a higher off-state current under a fixed bias (Figure 10(a)). It is desirable to have a lightly doped drain as long as the drain doping concentration is slightly higher than the electron density in the channel. After adjusting gate voltage to match I_{off} , a drain doping concentration of 10^{19}cm^{-3} yields the highest I_{on} (Figure 10 (b)).

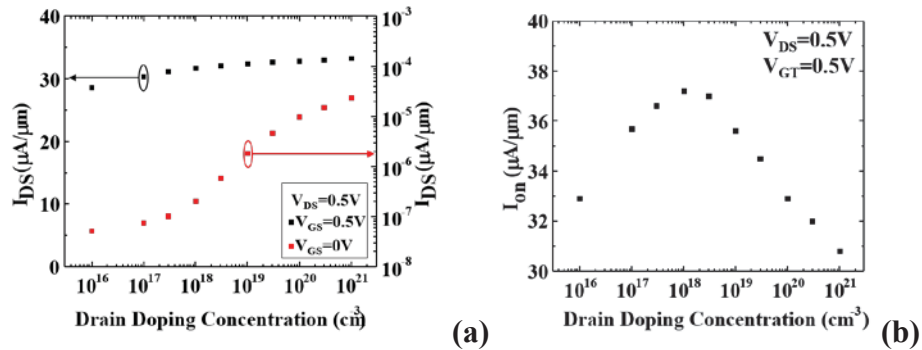


Figure 10: (a) I_{DS} for Ge-pocket TFET with Various Pocket Doping Concentrations under $V_{GS}=0V$ and $V_{GS}=0.5V$ and (b) I_{on} as a Function of Pocket Doping Concentration Optimum Drain Doping Concentration

Benchmark

The proposed structure with the optimized doping profile was benchmarked against state-of-the-art 14nm FinFET. It provides roughly 100% improvement in I_{on} at 14nm node ($L_g=20\text{nm}$) compared with Intel 14nm FinFET, and shows great potential in both L_g and V_{DD} scaling (Figure 11).

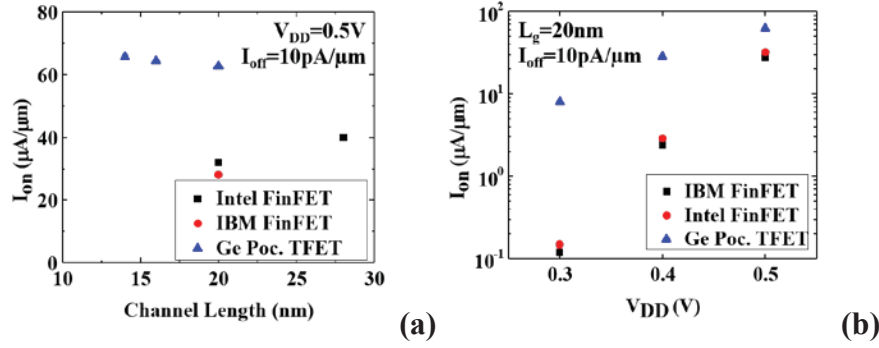


Figure 11: Benchmark of Optimized Ge-pocket TFET against State-of-the-Art FinFETs in Terms of I_{on}

The optimized structure in (a) gate length and (b) supply voltage scaling.

Composition and Doping Gradient

The success of Ge-pocket TFET relies on sharp material composition transition as well as doping profiles. The impact of material composition sharpness and doping gradient on the optimized device has been studied. Both increasing the Ge pocket thickness (t_{pocket}) and reducing the material composition gradient (CG) will result in a reduction in tunneling barrier; consequently, both on-state and off-state current will increase. Figure 12 plots I_{on} for the devices with different pocket length and composition gradient with adjusted V_{GS} to fix I_{off} to 10pA/μm. As the transition of material composition becomes sharper, ~80% I_{on} can be recovered compared to Ge-pocket TFET with abrupt material composition.

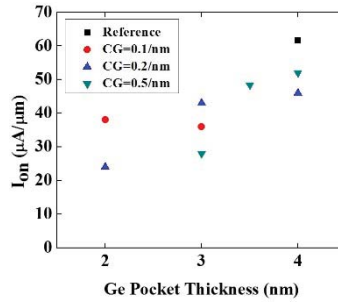


Figure 12: I_{on} for Ge-pocket TFETs with Different t_{pocket} and CG

The impact of doping gradient on TFET performance has been previously examined [6]. By using the doping compensation technique [7], the on-state current can be recovered (Figure 13). Simulations show that doping gradients of 6nm/dec and 5nm/dec are needed for source and pocket respectively to maintain >70% I_{on} of the device with box-shape doping profile.

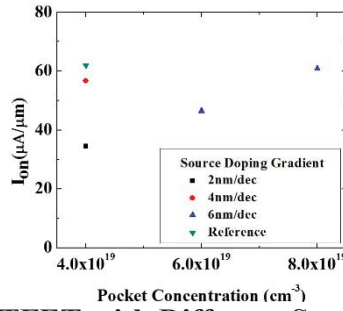


Figure 13: I_{on} for Ge-pocket TFET with Different Source Doping Gradient and Pocket Doping Concentration with Pocket Doping Gradient of 5nm/dec

3.2 Analog Performance Optimization for 14nm Node FinFETs

Simulation models and calibrations

Analysis in this project is carried out using the Sentaurus TCAD tools [9]. The design parameters of the simulated FinFET are based on the 14nm node FinFET published by Intel [8]. The device structure is demonstrated in Figure 14.

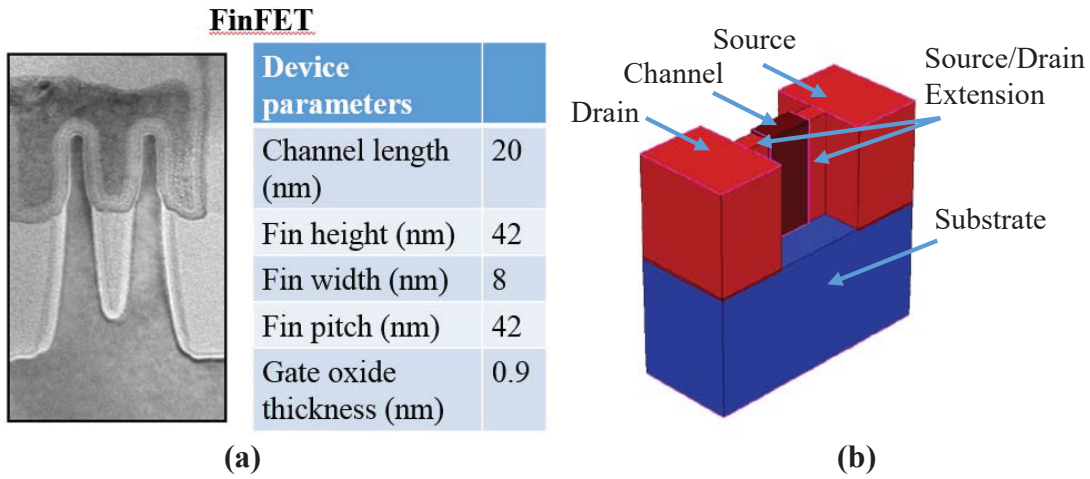


Figure 14: (a) Experimental FinFET Published by Intel [1] and (b) the Simulated Structure

Design parameters are listed in Table 2. A Drift-Diffusion model with modified saturation velocity is used in the simulation to capture the physics of velocity overshoot. Density gradient model and thin layer mobility model are used to simulate carrier quantum confinement as well as mobility degradation in the 8nm wide Fin. $R_{parasitics}$ has also been calibrated by fitting simulated and experimental g_{m_ext} . The total $R_{parasitics}$ is estimated to be 3kΩ/fin. The calibrated I-V curves are shown in Figure 15. The difference between simulated current and experimental data is less than 5%, suggesting that the modified transport parameters and saturation velocity is sufficient to study FinFET alternating current (AC) performance.

Table 2. Design Parameters of 14nm-node FinFET

Design Parameters	Value	Design Parameters	Value
Channel length	20nm	Gate dielectric EOT	0.7nm
Fin height	42nm	S/D extension length	10nm
Fin width	8nm	Fin pitch	42nm
S/D doping concentration	10^{20}cm^{-3}	Channel doping concentration	10^{16}cm^{-3}

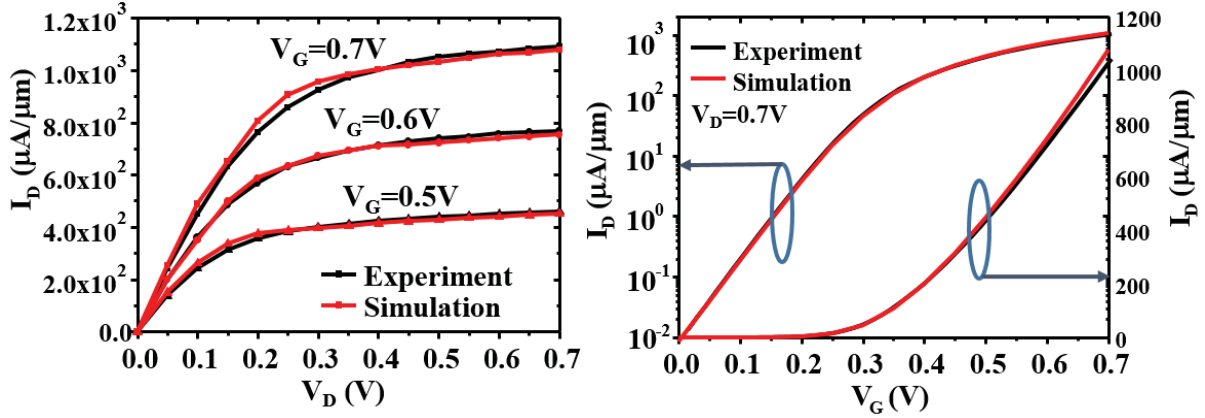


Figure 15: Experimental Data vs. Simulated I-V Curves with Calibrated Mobility Model

Physics of analog performance optimization by GC concept

The GC concept can be demonstrated with a double gate structure shown in Figure 16. An nFET is used as an example. In the proposed structure, GC concept is realized by SiGe/Si heterojunction ($\Delta\chi=0.16\text{eV}$ along the channel). SiGe with smaller electron affinity (4.05eV) is close to source side and tensile strained silicon with larger electron affinity (4.22eV) is close to drain side. The electron affinity grading can be tuned to achieve uniform electron distribution along channel length direction.

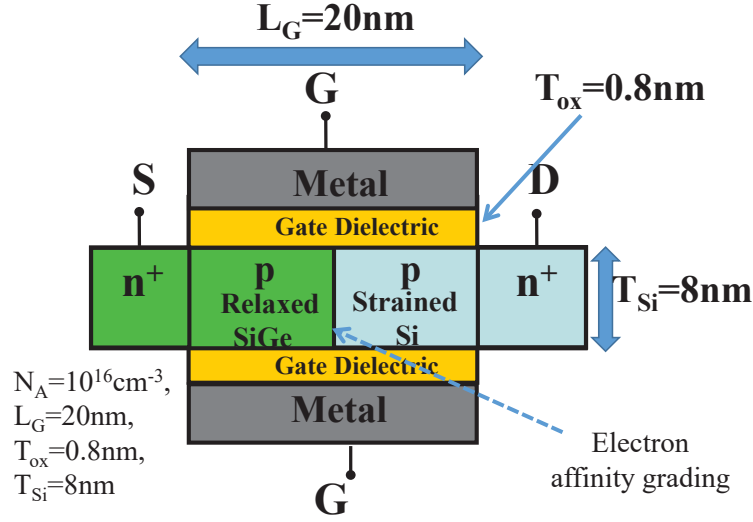


Figure 16: Double Gated FET with Graded Channel

In the proposed design, source and drain extension regions are heavily doped to reduce spacer parasitic resistance. The experimental FinFET $R_{parasitics}$ is extracted to be $3\text{k}\Omega/\text{Fin}$. Simulations show that this FinFET $R_{parasitics}$ is dominated by the S/D extension region resistance ($\sim 2\text{k}\Omega/\text{Fin}$), which is caused by insufficient doping concentration. It will be demonstrated later that the S/D extension resistance can be reduced from $\sim 2000\Omega/\text{Fin}$ to $365\Omega/\text{Fin}$, and thus improve g_{m_ext} .

The SiGe/Si heterojunction design can result in more uniform electron density and electron velocity distributions compared to a homojunction device. This uniform electron distribution causes the lateral electric field to redistribute, increasing the electric field at source side and decreasing the electric field at drain side. Higher electric field at the source side results in higher injection velocity, and thus improve g_{m_ext} . Lower electric field at the drain side will reduce the channel length modulation (CLM) and results in better output resistance [10-12].

4. RESULTS AND DISCUSSIONS

4.1 Group IV Tunnel Field Effect Transistors Optimization

Experiment Design

The success of fabricating the proposed structure depends on the quality of SiGe heterojunction. It is logical to use the resonant interband tunneling diode as a test structure to fine tune the growth condition. The process flow is listed in Table 3

Table 3. Process Flow for SiGe RITD

SiGe Resonant Interband Tunneling Diode Process Flow	
1	Thermal oxide growth
2	Patterning for selective area growth
3	Oxide etch
4	Photoresist strip
5	Pre-growth clean
6	SiGe growth
7	Contact hole patterning
8	Oxide etch
9	Photoresist strip
10	Ni deposition
11	Silicidation
12	Excess Ni removal
13	Al deposition
14	Patterning for contact pad
15	Al contact pad etch
16	Photoresist strip

4.2 Analog Performance Optimization for 14nm Node FinFETs

Analog performance optimization by GC design

A quantitative analysis was performed to study g_{m_ext} improvement by GC concept. An nFinFET was used as an example. Optimization of both doping concentration profile in the source/drain extension region and Ge mole fraction profile along the channel direction are required to maximize g_{m_ext} . Both of these profiles are assumed to be uniform along the Fin width and Fin height direction to reduce complexity. For Ge mole fraction profile optimization, the objective is to achieve a uniform electron density along the channel length direction, and thus improve g_{m_ext} and DIBL. For doping profile optimization, the goal is to minimize the extension region resistance while avoiding dopant encroachment into the channel, which can lead to enlarged DIBL.

The optimized device design is demonstrated in Figure 17. Design parameters are listed in Table 4. S/D extension doping profile is assumed to be formed by damage-free dopant implantation followed by laser annealing, resulting in a doping density gradient of 3nm/decade at the extension/channel junction and no mobility degradation [13-15]. Simulation shows that the S/D extension region resistance can be reduced from 2000 Ω /Fin [8] to 365 Ω /Fin.

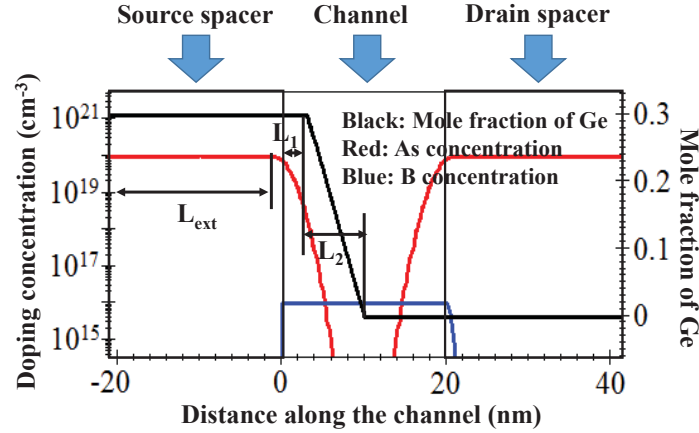


Figure 17: Optimized Doping and Ge Mole Fraction Profile along Channel Length Direction

Table 4. Design Parameters of the Purposed GC FinFET

Design Parameters	Value
L_1	3nm
L_2	7nm
L_{ext}	9nm
Contact resistivity	$2 \times 10^{-9} \Omega/\text{cm}^2$
Dopant gradient	3nm/decade

As shown in Figure 18, the optimized SiGe/Si heterojunction leads to a more uniform electron distribution along the channel length direction compared to homojunction (Si) device. The simulated g_{m_ext} of the purposed GC FinFET is shown in Figure 19. An improvement of 100% in g_{m_ext} has been achieved by the GC design at $I_{DS}=1\text{mA}/\mu\text{m}$ compared with that in experimental 14nm-node FinFET.

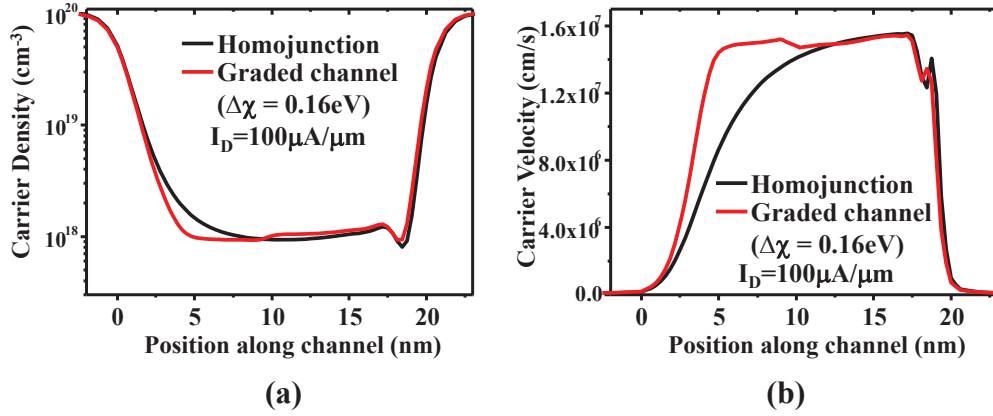


Figure 18: (a) Electron Density Profile and (b) Velocity Profile in Channel Length Direction at 1nm from Channel Surface

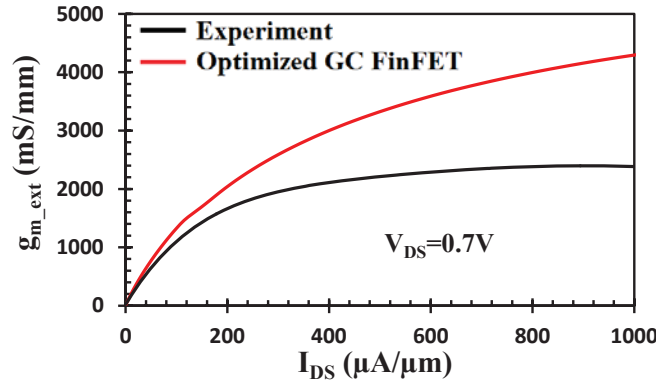


Figure 19: Simulated g_{m_ext} of Optimized GC FinFET vs. 14nm-node FinFET Experimental Data published by Intel

Apart from g_{m_ext} optimization, GC concept can also improve DIBL by screening the electric field from the drain side as shown in Figure 20. TCAD simulations show that DIBL is reduced from 60mV/V to 47.6mV/V. The reduced DIBL results in a 65% larger output resistance than homojunction device as shown in Figure 21.

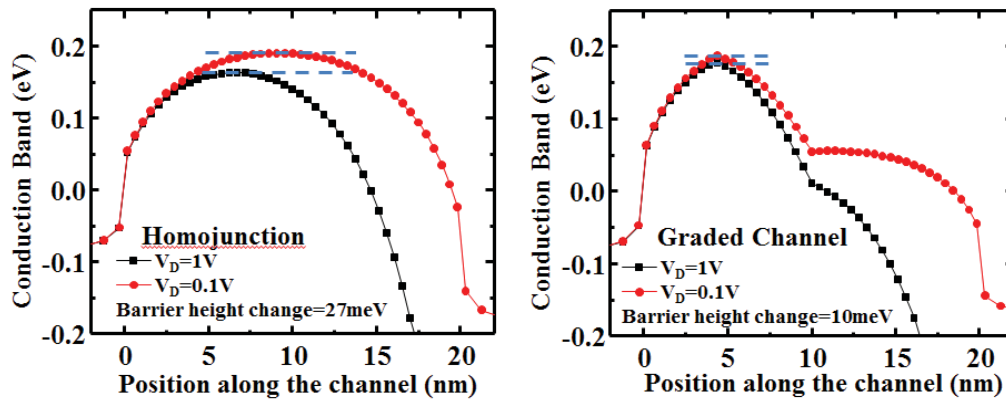


Figure 20: Conduction Band Profiles along the Channel at 1nm from Gate Dielectric for Graded Channel Device and Homojunction Device

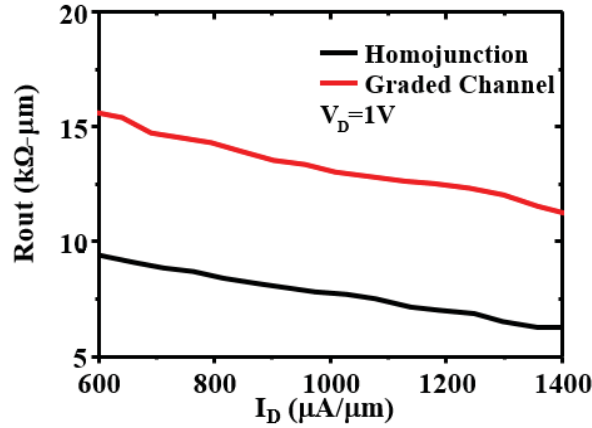


Figure 21: Output Resistance of Graded Channel and Homojunction Devices

Analog performance enhancement by using InGaAs MOSFET

Using high mobility channel material is another potential way to improve the analog/RF performance of MOSFET. Among all the materials, InGaAs has received extra attention due to its high electron mobility and versatile properties when changing composition. In order to study the analog performance of InGaAs MOSFET, we calibrated the simulation platform for InGaAs MOSFET for both short channel and long channel devices (Figure 22). Density Gradient model is used for quantum effect, Lombardi mobility model is used to account for surface mobility degradation, and Drift-Diffusion model with adjusted saturation velocity is used to simulate high field carrier transport.

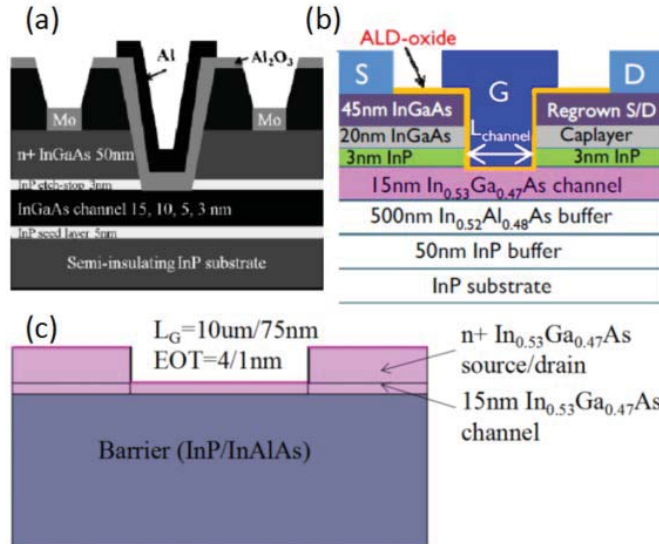


Figure 22: (a) Long Channel MOSFET [9], (b) Short Channel MOSFET [10], and (c) Simulated Structure

The gate capacitance (Figure 23) and peak transconductance (Figure 24) are compared to silicon SOI counterpart with same body thickness. It has been shown that in spite of a gate capacitance degradation introduced by the low density of state compared to silicon, there is still an

improvement of 80% in transconductance when switching channel material from silicon to InGaAs even for with EOT of 0.5nm.

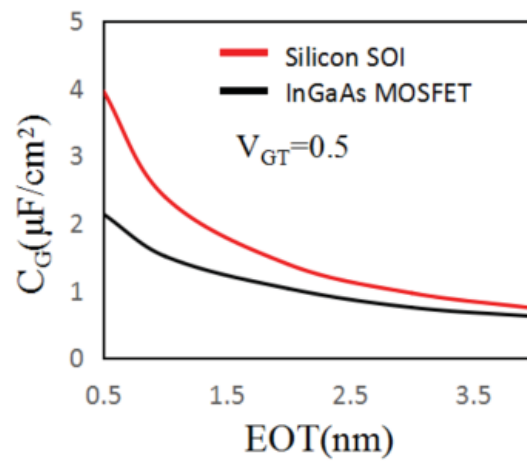


Figure 23: C_G vs EOT for Silicon SOI and InGaAs MOSFET

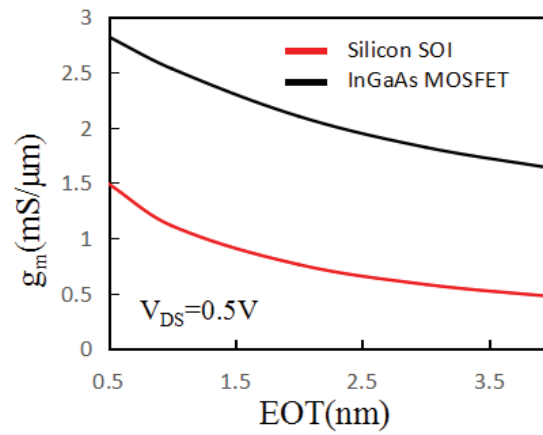


Figure 24: g_m vs EOT for Silicon SOI and InGaAs MOSFET

5. CONCLUSION

Based on the limitations of previous TFETs, Ge-pocket TFET was proposed for lower power applications with $I_{\text{off}}=10\text{pA}/\mu\text{m}$ and $V_{\text{DD}}=0.5\text{V}$. The doping was optimized, and the optimized structure shows great potential in both L_g and V_{DD} scaling. The process flow for the proposed Ge-pocket TFET was designed. Vertical structure was adopted to demonstrate the concept of Ge-pocket TFET because of the need for sharp doping/composition gradient. The impact of growth area on SiGe quality was also investigated by studying SiGe RITD with various dimensions. Ge-pocket TFET was fabricated with optimized SiGe growth condition.

FinFET analog performance optimization by GC design as examined. The analyses were carried out using the Sentaurus TCAD simulations. Doping profile in the S/D extension region was optimized to minimize extension parasitic resistance while avoiding increasing DIBL. SiGe/Si heterojunction led to a more uniform electron distribution along the channel length direction compared to homojunction (Si) device, and thus improved $g_{m_{\text{int}}}$ and DIBL. An improvement of 100% in $g_{m_{\text{ext}}}$ was achieved by the GC design at $I_{\text{DS}}=1\text{mA}/\mu\text{m}$ compared with that in experimental 14nm-node FinFET. The redistributed electric field along the channel length direction can result in a 20% better DIBL and a 65% larger output resistance compared with experimental data. It was also demonstrated that a further improvement in transconductance exists when switching channel material from silicon to InGaAs for the latest MOSFET generation.

6. REFERENCES

- [1] Choi, W. Y., Park, B.-G., Lee, J.D., Liu, T.-J.K., “Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS)”, *IEEE Electron Device Letters*, Vol. 28, Issue 8, pp. 743-745, 2007
- [2] Villalon, A., Le Royer, C., Nguyen, P., Barraud, S., Glowacki, F., Relevant, A., Selmi, L., Cristoloveanu, S., Tosti, L., Vizioz, C., Hartmann, J.-M., Bernier, N., Previtali, B., Tabone, C., Allain, F., Martinie, S., Rozeau, O., Vinet, M., “First Demonstration of Strained SiGe Nanowires TFETs with I_{ON} beyond $700\mu A/\mu m$ ”, *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp.1-2, June 2014
- [3] Dey, A. W., Borg, B.M., Ganjipour, B., Ek, M., Dick, K.A., Lind, E., Thelander, C., Wernersson, L.-E., “High-Current GaSb/InAs(Sb) Nanowire Tunnel Field-effect Transistors”, *IEEE Electron Device Letters*, Vol. 34, Issue 2, pp. 211-213, Feb 2013
- [4] Chung, S.-Y., Yu, R., Jin, N., Park, S.-Y., Berger, P.R., Thompson, P.E., “Si/SiGe resonant interband tunnel diode with f_0 20.2 GHz and peak current density 218 kA/cm^2 for K-band mixed-signal applications”, *IEEE Electron Device Letters*, Vol. 27, Issue 5, pp. 364-367, May 2006
- [5] Jhaveri, R., Nagavarapu, V., Woo, J.C.S., “Effect of Pocket Doping and Annealing Schemes on the Source-Pocket Tunnel Field-Effect Transistor”, *IEEE Transactions on Electron Devices*, Vol. 58, Issue 1, pp. 80-86, Jan 2011
- [6] Chang, H.-Y., “Asymmetric Devices for Mixed-Mode and Low Power Applications”, Ph.D. dissertation, UCLA, 2012
- [7] Tura, A., “Novel Vertical Tunnel Transistors for Continued Voltage Scaling”, PhD Dissertation, UCLA, 2010
- [8] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Moraka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince, S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Widemer, M. Yang, K. Zhang, “A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a $0.0588\text{ }\mu m^2$ SRAM cell size”, *IEEE Electron Devices Meeting*, pp. 71-73, Dec 2014
- [9] Sentaurus Device User’s Manual, Synopsys Inc., Mountain View, CA, USA, June, 2012
- [10] Chang, H.-Y., Woo, J.C.S., “The Improvement of Output Characteristics in Tensile Strained-Si-on-Insulator NMOSFET by Channel Band Gap Adjustment”, *IEEE Electron Device Letters*, Vol. 32, Issue 8, pp. 1032-1035, 2011
- [11] Gupta, G., Woo, J.C.S., “Novel Asymmetric SiGe/Strained-Silicon Heterojunction Channel MOSFET”, *International Conference on Solid State Devices and Materials*, pp.404-405, 2008
- [12] Yuan, J., Woo, J.C.S., “A novel split-gate MOSFET design realized by a fully silicided gate process for the improvement of transconductance and output resistance”, *IEEE Electron Device Letters*, Vol. 26, Issue 11, pp. 829-831, 2005
- [13] Zschätzsch, G., Sasaki, Y., Hayashi, S., Togo, M., Chiarella, T., Kambham, A.K., Mody, J., Douhard, B., Horiguchi, N., Mizuno, B., Ogura, M., Vandervorst, W., “High performance n-

- MOS finFET by damage-free, conformal extension doping”, *IEEE Electron Devices Meeting*, pp. 35.6.1-35.6.4, 2011
- [14] Sasaki, Y., Godet, L., Chiarella, T., Brunco, D.P., Rockwell, T., Lee, J.W., Colombeau, B., Togo, M., Chew, S.A., Zschaetsch, G., Noh, K.B., De Keersgieter, A., Boccardi, G., Kim, M.S., Hellings, G., Martin, P., Vandervorst, W., Thean, A., Horiguchi, N., “Improved sidewall doping of extensions by AsH₃ ion assisted deposition and doping (IADD) with small implant angle for scaled NMOS Si bulk FinFETs”, *IEEE Electron Devices Meeting*, pp. 20.6.1-20.6.4, 2013
- [15] Wang, C., Tang, S., Han, K., Persing, H., Maynard, H., Salimian, S., “A plasma doping process for 3D finFET source/drain extensions”, International Conference on Ion Implantation Technology, DOI: 10.1109/IIT.2014.6939993, 2014
- [16] Alian, A., Pourghaderi, M.A., Mols, Y., Cantoro, M., Ivanov, T., Collaert, N., Thean, A., “Impact of the channel thickness on the performance of ultrathin InGaAs channel MOSFET devices”, *IEEE International Electron Device Meeting*, p.437-440
- [17] X. Zhou, A. Alian, Y. Mols, R. Rooyackers, G. Eneman, D. Lin, T. Ivanov, A. Pourghaderi, N. Collaert, A. Thean,, “In_{0.53}Ga_{0.47}As quantum-well MOSFET with source/drain regrowth for low power logic applications”, Symposium on VLSI Technology, Sep 2014.

LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
AC	Alternating Current
CG	Composition Gradient
CLM	Channel Length Modulation
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
FinFET	Fin Field Effect Transistor
GC	Graded Channel
ITRS	International Technology Roadmap for Semiconductor
LSTP	Low Standby Power
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RF	Radio Frequency
RITD	Resonant Interband Tunneling Diode
S/D	Source/Drain
SOI	Silicon on Insulator
SS	Subthreshold Swing
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer-Aided Design
TFET	Tunnel Field Effect Transistor
VLSI	Very-Large-Scale Integration