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THERMAL ISOLATION AND DIFFERENTIAL COOLING OF HETEROGENEOUSLY INTEGRATED DEVICES

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14. ABSTRACT
The challenges of thermally isolating heterogeneously integrated components from one another was investigated. This work introduces the concept of microspreading resistance as a component of the thermal behavior of arrays of conductive vias. Recommendations for mitigating microspreading when it is undesirable is provided, and a formalism for incorporating it into existing equivalent thermal conductivity models of via arrays. After examining several heterogeneous integration approaches, it was determined that a segregated chiplet approach offered the most promising avenue for thermal isolation efforts.

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1.0 INTRODUCTION

Fundamental considerations limit the useful feature size of transistors and other microelectronic devices that constitute modern electronic products. Whether these limitations stem from the underlying nanophysics (e.g. electron tunneling) or from more familiar obstacles (e.g. diffraction limit of lithographic processes), size reduction and accompanying performance gains from the further miniaturization of transistors cannot continue indefinitely. Fortunately, there is considerable room for improvement in the interconnection and packaging of these products. By migrating components traditionally placed in separate packages – processors and memory, or amplifiers and their controllers – into the same package or even on the same die, significant gains can be realized.

A promising paradigms for this migration is heterogeneous integration (HI). This technology seeks to disrupt the traditional approach of a board of discrete, two-dimensional packages which must necessarily communicate with each other through long, limited-bandwidth interconnects. HI seeks to fabricate each component or device within a package in its optimal semiconductor material – e.g. silicon, InP, or gallium nitride. In this way economical, highly mature (and hence low feature size) silicon complementary metal-oxide-semiconductor (CMOS) circuitry can be used to control high performance III-V semiconductor transistors, amplifiers, and radio frequency devices in a hybrid, single-package circuit. Such systems are smaller and have better performance than those relying on components housed in separate packages.

A poorly understood feature of HI is that it presents additional challenges to the thermal management of the electronic package. Devices fabricated in different semiconductors have different thermal limits. Moreover, HI's greatest strength is in integrating components that have very different purposes and performance requirements, resulting in components with dramatic spatial variations in power output and maximum operating temperature. A uniform cooling approach must then seek to cool the entire package to the operating temperature of the most sensitive device, often resulting in an oversized thermal solution that may well negate any size, weight, and required power advantages gained from employing heterogeneous integration.

In analyzing the thermal characteristics of these high density packages, considerable attention is paid to the role of through-layer vias (TXVs) in conducting heat between layers of material and/or active chips. Just as TXVs provide a conductive pathway for electrical signaling, they can also be relied upon for heat transfer. This work seeks to contribute to the development of these technologies by enhancing the understanding of the impacts and possible advantages offered by arrays of TXVs to the thermal management of these systems.

TXV arrays and their host substrates can be treated as a composite material, an approach taken by equivalent thermal conductivity methods. During the course of modeling thermal isolation in HI systems, this work investigates current limitations of equivalent thermal conductivity for TXV arrays, identifies a new property of the arrays – microspreading resistance – that remedies the primary limitation, and conducts a series of experimental procedures capable of measuring the microspreading resistance of different arrays. This microspreading-augmented equivalent thermal conductivity theory is used to analyze the thermal isolation of heterogeneously integrated high power amplifier chips and their control logic on via-enhanced glass interposers.

To accompany this analysis, a demonstration of a mock HI system is experimentally measured. This system simulates the spatially variable power dissipations of an HI system using laser generated hotspots, and measures the resulting interposer surface temperatures using infrared thermography. With this measurement, the demonstration also validates the microspreading-aware thermal models, as well as highlighting the reduction in size of thermal keep out zones of sensitive devices compared to a bulk silicon interposer.

2.0 LITERATURE REVIEW

There are four main points of focus for this literature review. First, an overview of heterogeneous integration will outline the various approaches used to create electronic systems that incorporate devices of different semiconductor materials or of widely disparate thermal characteristics. As will be seen, many approaches pursue the "intimate" integration of CMOS and III-V devices, and while these achieve the shortest interconnect lengths, they also result in the spatial intermixing of the disparate devices leading to very poor prospects of thermally isolating them. Chiplet on carrier approaches segregate the disparate devices into individual chiplets, using either an active CMOS carrier chip or a passive interposer to host the chiplets. This approach has the best prospects for successful thermal isolation, with some promising results being shown using via-enhanced glass interposers.

The next point of focus (covered over two sections) will be on fabrication and reliability of through-layer vias and via arrays. Much of the literature in this area is generated from the 3D-Integrate Circuit (IC) community, but as the majority of HI approaches use through-layer vias for interconnection and via arrays have been identified as useful tool for thermal isolation, these publications will provide valuable background material. Reliability and manufacturing concerns will place constraints on feasible implementations of via arrays within the isolating glass interposer.

The third portion of this chapter (three sections) will present publications that model and/or measure the thermal properties of via arrays. Most models seek to treat the array of vias as a composite material, essentially smearing the vias and substrate into a homogeneous, anisotropic medium. The manner in which the anisotropic conductivity is obtained is categorized into two camps. One, the top-down approach, extracts these properties from detailed finite element models of via array unit cells. Because these cells are highly tailored to the arrays they represent, this approach tends to be very empirical in its conclusions, with results that are often applicable only to particular array being modeled. The other approach, bottom-up, adopts a physics-driven viewpoint and restricts itself to analytic models on simplified cells. The conclusions of this approach are often general, attempting to predict the effective conductivities of a variety of array geometries and materials. Following the discussion of array thermal modeling will be a presentation of experimental publications.

The last section of the literature review will introduce the topic of thermal constriction resistance. Also known as thermal spreading resistance, this phenomenon and its body of literature will factor into both of the thrusts of this work. In defining the concept of microspreading, many parallels will be drawn to the more canonical spreading resistance problem, and it will be argued that under particular conditions they collapse to the same model. Additionally, thermal constriction will appear in the thermal isolation application, where microspreading must be confronted in the approximation of the interposer as an equivalent medium, and which once homogenized becomes the anisotropic domain of a thermal spreading problem driven by the heated amplifier footprint.

2.1 Heterogeneous Systems

While the motivations and approach to any HI implementation vary from application to application, an excellent area to start is with Defense Advanced Research Projects Agency's (DARPA's) Diverse Accessible Heterogeneous Integration (DAHI) program [47]. DAHI seeks to integrate mature, high-density CMOS control circuitry with wide bandgap III-V devices (InP and GaN) to achieve smaller and lighter high-performance radio frequency systems. Performers in the program that embody particular approaches include Northrop Grumman Aerospace Systems (NGAS) [5, 48], Raytheon [49, 50], MIT Lincoln Labs [4], and HRL Laboratories [51]. The three primary approach styles are shown in Figure 1.

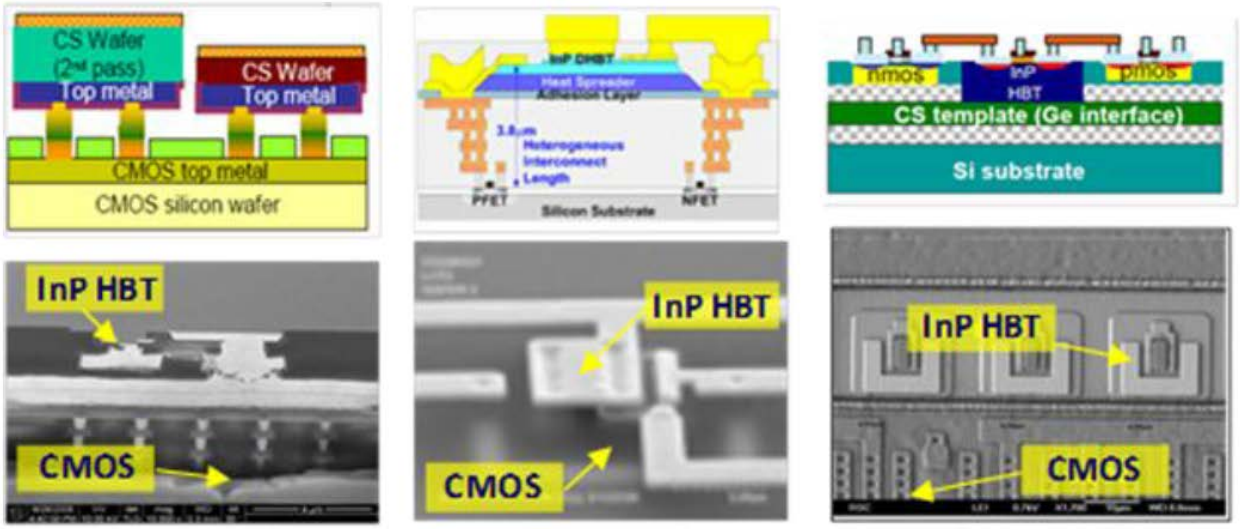

Figure 1: DAHI Integration Approaches
Images from left to right: from NGAS, HRL, and Raytheon

Raytheon uses an approach where individual transistors of either InP or GaN are interleaved as needed between CMOS devices fabricated on custom silicon-on-insulator (SOI) wafers. This is done by etching a "window" through the upper layer of silicon and oxide to access an underlying layer of germanium (for InP) or <111> silicon (for GaN). These layers provide the necessary lattice parameters for the low-defect epitaxial growth of the desired III-V semiconductor. After wide bandgap device fabrication, the heterogeneous devices are on the same planar active surface and are assembled into circuits using typical multilayer interconnects. MIT uses a similar approach, creating what they call a "hybrid wafer" where selective etching can expose lattice matched layers for epitaxial growth.

HRL uses a wafer-to-wafer approach where III-V devices are fabricated on dedicated wafers, separate from CMOS and interconnect layer patterning on a silicon wafer. Each of the two or more wafers are patterned with an array of metal "heterogeneous interconnects" (HICs) that correspond to mating HICs on the other wafers. The wafers are then bonded together using the HICs, completing the electrical interconnection between the heterogeneous devices. In this way there is an increased degree of verticality compared to the selective epitaxy approach embodied by Raytheon and MIT.

Northrop Grumman has selected a micrometer scale integration approach where GaN and InP devices are fabricated on individual wafers which are then diced into chiplets. These are then placed on a CMOS carrier chiplet, interconnected with several HICs on each chiplet in a manner similar to the wafer-level approach. While this approach creates the largest degree of segregation between the III-V and CMOS devices, the authors point out it allows a decoupled line yield as devices from each semiconductor process can be tested before heterogeneous integration. From a thermal point of view, this approach is also the most amenable to thermal isolation efforts since the disparate devices are contained within their own chiplets rather than dispersed among each other. Some thermal modeling of the NGAS design is performed by Harris, et al. [52]. Modeling chiplets that contain single GaN high electron mobility transistors (HEMTs) or InP heterojunction bipolar transistor (HBT), they find that the transistor temperature rise is about 145 °C for GaN and less than a degree for InP. They do not report CMOS temperature rise in the vicinity of the GaN chiplets.

To observe an existing treatment of thermal isolation on an HI system one must look outside the DAHI program. Cho, et al. [2] considered the thermal isolation of a microprocessor from temperature sensitive memory modules in a mobile electronics application. Normally mounted on a silicon interposer, these two chips have a high degree of thermal cross talk. Through finite element modeling, the authors found that using a glass interposer would provide a higher degree of thermal isolation between the two chips, with thermal vias helping to provide a conductive path through the thickness of the interposer for dissipated heat. The authors have since published experimental results for thermal behavior of thermal via arrays in glass interposers [21, 53], but have not yet experimentally demonstrated the isolation effect between two thermally disparate components. Such a demonstration is one chief aim of this project.

2.2 Fabrication of Via Arrays

Given the choice of relying on thermal via arrays for managing the temperature rise of the high power components in this projects HI application, it is important to survey the methods used to fabricate these arrays. Since the literature for fabrication of vias in silicon is much more mature, this review will restrict itself to fabrication in glass substrates. Tummala, et al. [10], provides a brief overview of hole formation methods; they include electric discharge, laser ablation, and "photo-via" formation in photosensitive glass. Limits on the minimum hole diameter for each method are driven by the thickness of the glass substrate used. In the authors' overview, holes as small as 20 µm diameter in 100 µm thick glass wafers were achieved using electric discharge, 10 µm diameter in 30 µm thick glass by excimer laser ablation, and 14 µm holes in UV-sensitive glass (thickness not stated). Sukumaran, et al [11], provides additional detail on laser ablation methods and possible applications for 15 µm diameter vias in 30 µm glass. They were also able to demonstrate copper redistribution layers (RDLs) of 4 µm line width at a pitch of 10 µm.

Corning Glass [7, 8] uses proprietary methods to fabricate holes down to 20 µm in 100 µm thick glass. One advantage the company claims is the ability to manufacture 300 mm diameter glass wafers with a falling film technique that results in a very low roughness average without the need for polishing. This helps to limit the possible size of surface flaws in the glass substrate, one of the failure mechanisms for stress or fatigue induced brittle fracture. Discussions with Corning recommend a minimum via pitch to diameter ratio of 2:1.

The filling of the via holes with conductive material generally follows a process of electroless copper seed layer deposition, followed by electroplating copper. The target copper thickness on the insides of the via holes is typically 6-8 μm [10, 11]. It can be difficult to completely fill via holes with copper without build up at the hole entrance leading to choking and a resulting void.

2.3 Reliability of Via Arrays

Also important for the eventual application of via arrays for thermal isolation is their reliability under thermomechanical stress. Due to the coefficient of thermal expansion (CTE) mismatch between substrate and hole metallization, vias can fail due to a variety of factors intrinsic to the array and substrate, before consideration of the larger system is made. Because publications on glass via array reliability are sparse, several works on reliability in through-silicon vias are included in this section.

Tong, et al. [13], derive analytical relations for the hoop stress in a silicon substrate based on two-dimensional plane stress and plane strain approximations. While the stress from a single through-silicon via (TSV) does not depend on TSV diameter (since the larger CTE induced strain from larger vias is exactly offset by the larger circumference available to absorb that strain), the pitch of adjacent TSVs does play a significant role. This is because the stress fields of nearby TSVs overlap, creating high stress regions along the lattice vectors of the array. Suhir [16] pursues a similar treatment, while also suggesting the use a compliant strain buffer layer at the interface of the via and silicon to reduce the stresses at the interface.

Kumar, et al. [14], provides an example of an investigation into the effects of the thermal strain generated in the direction along the via axis. When a copper via is heated, since it expands relative to silicon (or glass), the via will tend to extrude up and out of its hole. Under particular conditions the via can creep at the via/substrate interface, resulting in the extrusion becoming permanent even upon return to the original temperatures.

Concluding this section, Demir, et al. [15], performed accelerated lifetime testing of through-glass vias. Formed by excimer laser in 180 μm thick glass, the 60 μm diameter conformal (plated) vias were subjected to -55°C to 125 °C temperature cycling, as well as an electrical bias test for electromigration. The only failures the authors found they attribute to plating process defects.

2.4 Modeling of Thermal Via Arrays – Top-down Approaches

Top-down thermal modeling approaches to via arrays are characterized by the sectioning of the array into representative unit cells, and applying a finite element approach to these unit cells to extract effective behavior. Since finite element method (FEM) is being used, these unit cells often contain as much detail as possible with regards to the via construction, presence of interfacial layers, and sometimes materials or interconnections above or below the via array substrate. This level of detail increases the fidelity of the model to the array being considered, but as a result requires a fresh effort to design and mesh the unit cell for each new application.

One of the earlier examples of this modeling approach is exhibited by Chein, et al. [18]. The authors calculate an equivalent thermal conductivity for their TSV arrays by applying equal input and output heat fluxes at opposite cell faces to create first a cross-plane (along-via-axis) heat flow then an in-plane flow (perpendicular to the via axis). For their cross-plane models, the authors apply 500 W/m-K "buffer blocks" to the top and bottom surface, on the outside of which the heat flux boundary conditions are applied; see Figure 2. This is done to "smooth the heat flow" as it enters and exits the cell. Since the authors compute their effective conductivity in this case using a 2 µm slice of the model at the cell midplane, far from the buffer blocks, they argue that the exact nature of the blocks do not impact the result, while allowing them to handle the non-planar surface presented by the via pads overlying the wafer surface. Relatively unique among top-down approaches, the authors then proceed to model a survey of 500 different cells composed of different via diameters, lengths, pitch, and oxide thicknesses, presenting empirical equations determined by curve fitting the data.

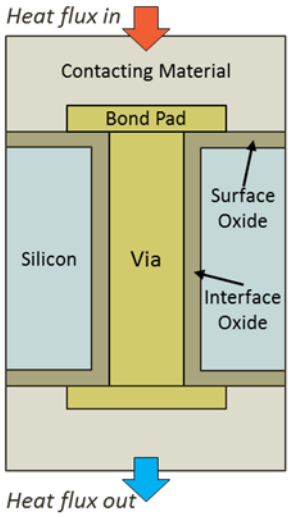

Figure 2: Side View of a Top-down Via Unit Cell, Vertical Conductivity

Cho, et al. [2], adopt this approach – complete with buffer blocks – to determine effective conductivity for via arrays in glass interposers and compare them against via arrays in silicon. Recognizing that vias formed in glass frequently have a larger entrance diameter than exit diameter, they model their glass vias using a conical copper section. As the authors are interested in a specific application, they constrain their interest to a single array arrangement for glass and for silicon.

A final example of a top-down approach is the treatment of Santos, et al. [20], of lateral thermal blockage due to TSV arrays. These authors are interested in the deleterious effect of the oxide layer present between copper vias and their silicon matrix on lateral effective conductivity. They find that despite the high conductivity of copper, the oxide layer prevents easy conduction through the via, resulting in a lower lateral effective conductivity than bulk silicon, trapping heat behind arrays of TSVs.

2.5 Modeling of Thermal Via Arrays – Bottom-up Approaches

Contrasted with top-down models, bottom-up approaches rely on simplified array unit cells and attempt to construct physics-based relations for vertical and/or effective thermal conductivity. They are often more concerned with determining the general behavior of cells as a function of array parameters than focusing on one specific array in particular application. Since they rely on simplified cells and other assumptions, there can be a loss in accuracy compared to a more detailed model.

An early example of a bottom-up approach is in Lee, et al. [22], a treatment of conformal vias in printed circuit boards. The authors use a thermal constriction treatment to derive the effective vertical conductivity, treating the organic board material as a volume with zero thermal conductivity. The thermal constriction then exists from the pads of the individual vias to the hollow cylinder of the via barrel. Li [23] performs an analysis on solder filled plated through-holes in printed circuit board (PCB), using an analysis that relies on series and parallel thermal resistances for each material in the through-hole unit cell.

Liu, et al. [25], analytically treats the lateral effective conductivity of a through-silicon via array. Identifying the interfacial oxide as an important factor, they segment the unit cell into five regions, four comprised of solely silicon away from the via, and one a square-sectioned region just containing the cylindrical via. They neglect the contribution of the silicon in the corners of this sections and derive an expression for the resistance across the oxide and copper via. This is assembled back into the larger cell using series and parallel resistances. They then calibrate their model using FEM.

A last example is provided by Zhang, et al. [27], in their modeling of TSV arrays. While they use a rule-of-mixtures to compute vertical conductivity (a typical assumption) the work is notable in their use of the Maxwell-Eucken Equation (described in [54]) for estimating lateral conductivity. They point out this is equivalent to assuming the vias can be treated as spherical inclusions suspended in a silicon matrix.

2.6 Experimental Characterization of Via Arrays

In a similar vein to reliability publications, thermal experiments on via arrays in glass are limited, while there is much more literature available for arrays in silicon and other systems that behave in a similar manner (plated through hole (PTH) in PCB, ball grid arrays, etc.). The primary focus is on the possible methods that can be used to evaluate arrays.

A first notable work is that done by Yamaji, et al. [30], using laser flash to measure the thermal resistance between stacked silicon die. The authors claim an accurate measurement of the resistance of an underfilled bond between two silicon samples, but are unable detect a significant (relative to uncertainty) change when the silicon is equipped with a copper via array that does not penetrate into the underfill. They do detect a change when gold microbumps are inserted between the die in the underfill region, but had particular difficulty in applying laser flash to the “heterogeneous specimens” presented by the gold/underfill medium.

Matsumoto and Taira [31] measured the thermal resistance of a controlled collapse chip connection (C4) solder bump array joining two silicon surfaces using a steady state American Society for Testing and Materials (ASTM)-style thermal interface test. While their measurements are on a C4 array of 100 μm ball at a 200 μm pitch, they include in their modeling a variety of ball sizes and with and without underfill. They note in their modeling that assuming a homogenized interfacial layer using a rule-of-mixtures for the solder and air or underfill results in an underprediction of the layer resistance.

A final publication, by Cho, et al. [21], evaluates the effective vertical conductivity of conformal via arrays in glass substrates. The measurements are performed using infrared (IR) thermography on samples heated from below, and loss through the exposed upper surface through convection and radiation estimated. The authors note significant discrepancies between experimental results and FEM calculations done along the lines of Chien, et al. [18], for the samples that have the largest vias and pitch dimensions. The authors attribute this to poor copper plating alignment in those samples, although an alternative explanation is that those samples should exhibit the largest microspreading resistance, and effect not captured by Chien's methodology.

2.7 Thermal Constriction Resistance

Thermal constriction resistance – also called spreading resistance – is a phenomenon that arises when heat is introduced into a material through a localized zone or "hotspot". Very early treatments on the subject by Mikic [32] and Yovanovich [33] were motivated by investigations into the underpinnings of the thermal contact resistance between material surfaces with defined surface roughness. While the underlying geometric problem exists in other fields, these authors laid the foundation for the concepts and terminology used within heat transfer.

The essential treatment of the subject is well described by a comprehensive review by Yovanovich [36]. The temperature rise of a localized hotspot on the surface of an infinite half-space can be related to the flux introduced through the spot through a thermal resistance R_T. When reducing the half-space to a finite volume, e.g. the base of a finned heatsink or a thin thermal spreader, is convenient to decompose this total resistance into a one-dimensional resistance defined by the dimensions of the volume, R_{1D}, and a spreading resistance, R_S, that accounts for the constriction effect produced by the spot. If the spot area is allowed to increase to the entire area of the material surface, R_S goes to 0.

Muzychka *et. al.* [42] investigated thermal constriction resistance in orthotropic heat spreaders. One method they use to simplify the system to be solved is to transform one or more spatial coordinates in order to recover an isotropic heat spreader from an anisotropic one. In the interposers considered in this project, where $k_z > k_x$, the appropriate coordinate transform would result in a system that is either stretched laterally or compressed vertically. For this project's purposes, the lateral transformation better facilitates comparisons between interposers with comparable vertical conductivity but with contrasting lateral conductivities. Thus, the lateral coordinate, x, is transformed:

$$\bar{x} = \frac{x}{\sqrt{k_x/k_z}} \tag{1}$$

Prior to making this transform, a further simplifying reduction to the system may be made. The chip, die attach layers, and upper spreading resistance can be combined into a single one-dimensional resistance. Instead of the uniform heat flux that is dissipated at the upper surface of the chip, a modified flux profile is dissipated through this resistance and into the interposer. This modified flux profile is based on the profile of the heat flux entering the interposer in an equivalent medium finite element model; rather than being uniform, more heat is transmitted at the edges of the chip than at the center, as a result of spreading within the chip.

Although this simplification of the chip layers is an approximation, it avoids the issue of transforming the chip material into an anisotropic volume when attempting to transform lateral coordinates. Negus *et. al.* [55] note that using equivalent circular hotspots with radii $a = \sqrt{A_s/\pi}$ (with A_s the area of the hotspot) introduces acceptably low error. Leveraging the work of Yovanovich [33], a flux profile of the form

$$f(u) = \frac{Q}{2\pi a^2}(1-u^2)^{\mu} \tag{2}$$

can be used, where $u = x/a$ is the relative position from center (at the chip-interposer interface), Q the total heat rate in W, and μ is the flux shape parameter. For an isoflux profile $\mu = 0$ is used, while for a profile that produces an isothermal interface $\mu = -1/2$. The FEM derived profiles for both example interposers lie between these theoretical profiles. Yovanovich *et.al.* [36] note that the isothermal interface condition provides an lower bound for computing the thermal constriction resistance (and thus average chip temperature), while the isoflux interface provides a upper bound, citing an 8% maximum discrepancy between the two for systems with circular hotspots.

Song *et. al.* [34] provide very simple, approximate, closed-form expressions for constriction resistances based on both average and maximum hotspot temperatures for circular hotspots with constant flux. Their expression for dimensionless constriction resistance, $\psi = \sqrt{\pi} k a R_c$ is

$$\psi_{ave} = \frac{1}{2}(1-\epsilon)^{3/2}\varphi_c \tag{3}$$

And

$$\psi_{max} = \frac{1}{\sqrt{\pi}}(1-\epsilon)\,\varphi_c \tag{4}$$

Where

$$\varphi_c = \frac{Bi\tanh(\delta_c\tau)+\delta_c}{Bi+\delta_c\tanh(\delta_c\tau)} \tag{5}$$

$$\delta_c = \pi + \frac{1}{\sqrt{\pi}\,\epsilon} \qquad Bi = \frac{hb}{k} \qquad \epsilon = a/b \qquad \tau = t/b$$

They assert that these correlations agree with full analytical solutions "to within 10% for the range of parameters commonly found in microelectronics applications." Since for this

discussion the hot chip is assumed to be far from the edges of the interposer, multiplying φ_c by ϵ/ϵ and taking the limit as $b \to \infty$ results in

$$\psi_{ave} = \frac{\sqrt{\pi}}{2}\psi_{max} = \frac{1}{2}\varphi_c \tag{6}$$

with

$$\varphi_c = \frac{\frac{ha}{k}\tanh\left(\frac{t}{\sqrt{\pi}a}\right) + \frac{1}{\sqrt{\pi}}}{\frac{ha}{k} + \frac{1}{\sqrt{\pi}}\tanh\left(\frac{t}{\sqrt{\pi}a}\right)} \tag{7}$$

3.0 MODELING EFFORTS

This chapter describes the modeling work in support of this project. The first subchapter introduces the case study that forms the basis of the HI thermal isolation application. The system considered is modeled using finite element analysis (FEA), including the detail of individual thermal vias. The second subchapter concerns finite element modeling of individual via unit cells, initially undertaken as a top-down, equivalent thermal conductivity approach. It is here that microspreading resistance is identified, defined, and analyzed. The third subchapter describes an analytical model of microspreading resistance, where the unit cell vertical resistance boundary value problem is outlined and solved. The final subchapter models the anisotropic thermal constriction problem associated with the original thermal isolation application. It distills the multitude of parameters that describe the system into the minimal set necessary to distinguish substantially different incarnations of the isolation problem, providing a compact parameterization of the available design space.

3.1 Case Study: Thermal Isolation of Heterogeneously Integrated Systems

The anchor point of this project is a numerical case study on the feasibility of a via-enhanced low-conductivity interposer for a high power heterogeneous system. As described in the literature review, a major advantage of heterogeneous electronic systems is the ability to design a composite device where the individual constituent components are fabricated in the semiconductor best suited to them. The prototypical example for our case study is a power amplifier fabricated in gallium nitride, with silicon CMOS control logic. The fast switching HEMTs in the GaN dissipate substantially more heat than the lower power CMOS components, leading to considerable spatial variation in dissipated power throughout the package. The GaN components can also tolerate higher operating temperatures (as high as 250 °C, compared with 70 °C for commercial CMOS) without suffering performance or reliability degradation. Without a strategy of thermally isolating the different components, heat generated in the GaN will diffuse into the silicon, necessitating a cooling solution that essentially cools the entire package to temperatures near the maximum safe temperature of the CMOS logic.

The ability to isolate components with different thermal requirements with a via enhanced low-k interposer was demonstrated for a consumer electronics application [2]. The case study in this project examined whether such an approach could work for the much higher heat loads associated with HI amplifier systems. It also proposed a new “differential” cooling strategy, where a baseline fluid cooling approach would be applied to the underside of the interposer, except in high power regions where a more intensive cooling solution would be implemented. The study considers a fluid microgap cooler as this baseline, and a manifold-fed microchannel cooler as the aggressive, site-specific solution.

As discussed in the last chapter, there are many approaches to heterogeneous integration. An approach where the amplifier and control logic are fabricated on one contiguous silicon substrate was discarded after initial finite elements models demonstrated the difficulty of thermally isolating the devices with such a strategy. The additional thermal pathway traveling laterally through the silicon substrate meant that regardless of the interposer or underside cooling strategy, maintaining substantially different temperatures in the amplifier and logic was unfeasible. Thus, a chiplet based system became the focus of the study. The final system configuration chosen is

shown in Figure 3. Two amplifier chiplets of GaN on silicon flank a central silicon CMOS chip. All three are mounted on a glass interposer, the thickness of which is 200 µm. A copper via array is inserted in the volume underneath the amplifiers, and convection boundaries applied to simulate the fluid cooling; a high convection coefficient of 30,000 W/m^2-K is applied under the arrays to represent the microchannels while the remaining microgap region is set to 3,000 W/m^2-K. Figure 4 provides the dimensions of the via array used, and Figure 5 presents a rotated view of the system, providing the chiplet power dissipation and convection coefficients used.

To analyze this system, a quarter-symmetry finite element model was constructed, with heat flux applied to the free surface of the chiplets such that the total heat entering each chip matched the target dissipation, and convection boundaries communicating with a fluid of reference temperature zero applied to the underside. In meshing the model, very fine element sizes were required in and around the copper vias. After performing a mesh convergence study, the resulting mesh contained just over 36,000 high-order hexahedral elements. For material properties a temperature independent conductivity was assumed to expedite this initial modeling; the values used are presented in Table 1.

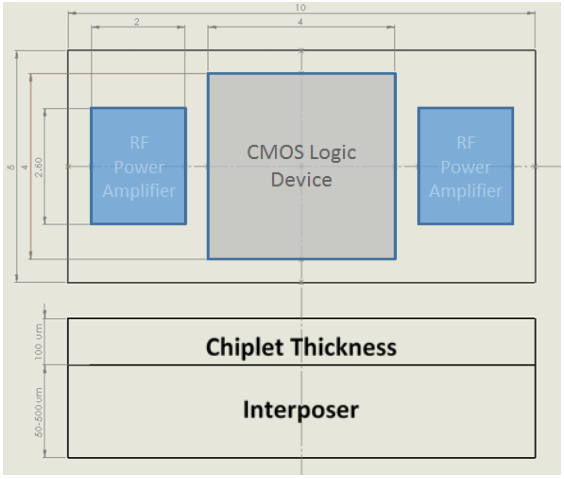

Figure 3: Layout for HI Case Study

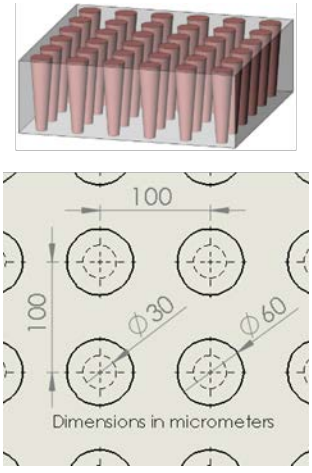

Figure 4: Array Parameters for Copper Vias

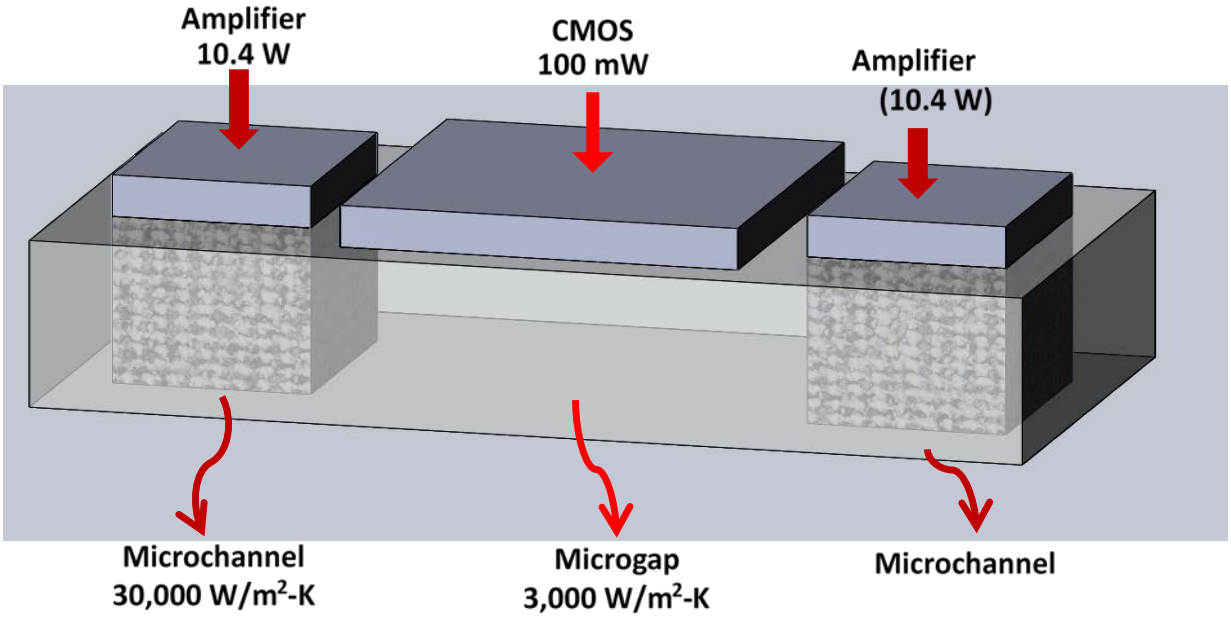

Figure 5: Rotated View of HI Case Study System Showing Input Power and Underside Cooling

Vertical scale exaggerated.

Table 1. Material Properties for HI Case Study

Material	Thermal Conductivity
Silicon	150 W/m-K
Glass	1 W/m-K
Copper	400 W/m-K
Sintered silver die attach	200 W/m-K
Silver metallization	401 W/m-K

Several variations on this model were investigated, where the thickness of the interposer was varied, the site specific cooling was set to microgap values, or the via array removed. All these changes had the expected effect: thinner interposers provided better isolation due to a lower lateral cross section and removing the high cooling coefficient and/or vias dramatically increased the temperature of the amplifier. The satisfying conclusion occurred when the glass material of the interposer was substituted with silicon (or with copper). Figure 6 and Figure 7 show simulation results for the baseline 200 µm glass interposer with vias and differential cooling compared against the results for the same systems where the glass has been replaced with silicon. In the model using glass, the amplifier peak temperature rise (relative to the fluid) reached 113 K, while the CMOS temperature rose on average only 5 K. With silicon, however, the amplifier temperature rise fell to 56 K, while the CMOS average rise increased to as high as 40 K. Given the assumed safe operating temperatures of 250 °C for the amplifier and 70 °C for the CMOS, the silicon interposer would limit the coolant temperature to 30 °C while the glass interposer would allow a coolant temperature of 60 °C.

The case study identified what is simultaneously the challenge and advantage of this low-k interposer approach: The interposer constrains the heat dissipated by the high-power components to a small footprint within the package. This creates a local hotspot on the underside of the interposer, where the large temperature difference from the fluid drives the convective heat removal. The approach relies on this difference to compensate for the effective loss of heat removal area since the footprint over which the significant heat removal occurs is reduced. The challenge then is to balance the constraining of dissipated heat with the available convection coefficient for a particular cooling solution; too much heat and the amplifier temperature will rise above allowable levels. Fortunately, since the other regions of the interposer need very modest heat removal rates, a more economical cooling solution can be employed for regions far from the hotspot.

In order to better explore ways to optimize the design of the interposer and site-specific cooling system, modeling efforts turned to equivalent conductivity methods to simplify the finite element models of the system. In this way, rather than needing to adjust and refine a very fine mesh for each geometry or array parameter change, the equivalent conductivity could simply be altered. However, in order to determine the appropriate equivalent conductivity to use, modeling at the array unit cell level needed to be performed. As will be shown in the next section, the interaction of the convection boundary on the underside of the interposer leads to cell responses not well handled by existing equivalent conductivity methods.

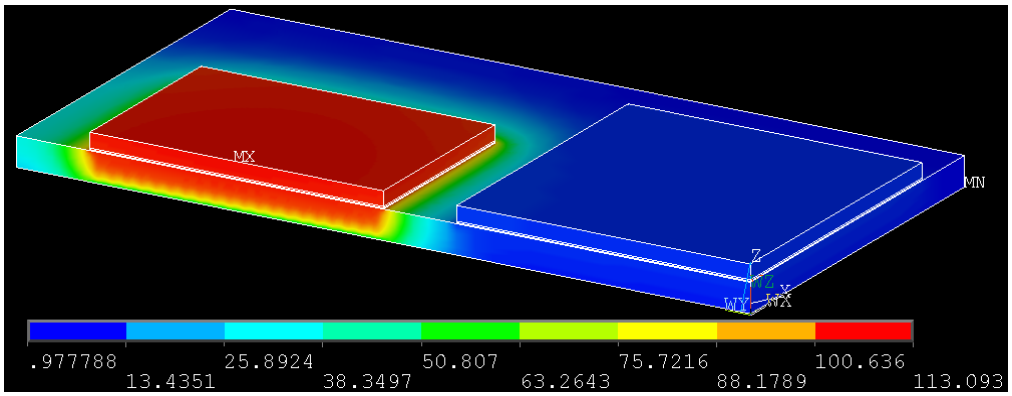

Figure 6: System in Package with Glass Interposer, Thermal Via Array, and Differential Cooling

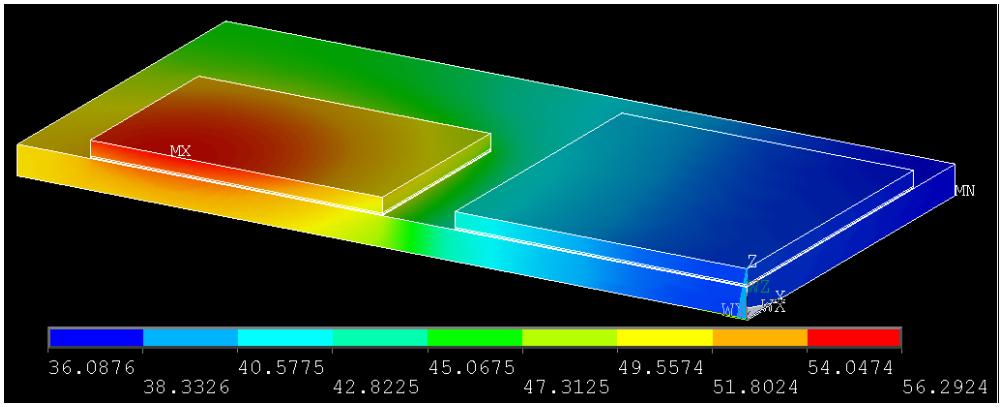

Figure 7: System in Package with a Silicon Interposer, Thermal Via Array, and Differential Cooling

3.2 Modeling Thermal Microspreading Resistance in Via Arrays

As noted in the last subchapter, fully detailed finite element models – incorporating individual thermal vias into the analysis – provide the best fidelity to the via array at the cost of cumbersome setup and extended meshing and simulation time. Replacing interposer regions equipped with via arrays with an equivalent homogeneous medium allows a more rapid assessment of the design and available tradeoffs inherent in a low-k interposer isolation approach. This homogenization is accomplished by extracting effective thermal conductivity properties from an array unit cell, as described in the literature review. Notable for the arrays investigated in this project, however, is the introduction of an additional thermal resistance to heat flow through the thickness of the interposer. This microspreading resistance is not treated in existing effective conductivity literature, and must be accounted for in order for a homogenized array to faithfully represent a fully detailed model.

3.2.1 Effect of Boundary Conditions on Array Vertical Thermal Resistance

As power dissipation in electronic systems continues to increase, lower thermal resistance solutions including thinner chips, higher conductivity substrates, as well as "inwardly-migrating" active thermal management measures [56] have proliferated. The close proximity of these active components to microfluidic coolers establishes a need for considering a broader range of thermal boundary conditions on the faces of the via unit cell, including constant heat flux and convective conductances, as well as isothermal conditions. Equation (8) provides an example of a convection condition, the same as that used in the isolation case study:

$$h(T_a - T(x,y)) = k(x,y)\frac{\partial T}{\partial z}(x,y) \tag{8}$$

where h is the constant heat transfer coefficient in W/m^2-K and T_a is the ambient fluid temperature.

In this section, these boundary conditions will be applied directly to the TXV surface, meaning that no pads, surface oxides, or other materials are considered. The top and bottom faces of the unit cell are then the reference surfaces used to determine $k_{eff,z}$. Once boundary conditions are specified, changing the temperature of an isoflux boundary or the fluid temperature of a convection boundary causes $\dot{Q}$ and $\Delta\bar{T}$ to change in constant proportion, since material properties are assumed temperature independent. In this way $k_{eff,z}$ is independent of choice of reference temperature. Thus, convection boundary conditions can be seen as a continuum linking isothermal boundaries and isoflux ones. As $h \to \infty$ the boundary becomes isothermal at T_a. As $h \to 0$ the flux crossing the boundary becomes uniform from point to point and

$$k_{eff,z} = \lim\left(\frac{\dot{Q}}{\Delta\bar{T}}\right)\frac{L}{A} \text{ as } \dot{Q}, \Delta\bar{T} \to 0 \tag{9}$$

When the boundary conditions on the upper and lower faces have the same h, or are both isothermal or both equal uniform flux, the resulting flow of heat is symmetrical about the mid-plane between the faces, and hence the mid-plane is an isotherm. An example of this is shown in

Figure 8. An equivalent half-cell model can be constructed using an isothermal boundary at one face and a copy of the original condition at the other; this cell will possess the same $k_{eff,z}$. Cells with asymmetrical boundary conditions will contain a planar isotherm offset from the mid-plane. It is possible to decompose such a scenario into two sub-cells, each with an isothermal and non-isothermal boundary, but the necessary length of each cell is not known in advance. Reflecting this insight, the present study will present results of $k_{eff,z}$ for cells with one isothermal boundary and one general boundary, serving as a solution "building block" and allowing cells with symmetrical boundaries to be constructed by symmetry, while providing a starting point for cells with asymmetrical boundaries.

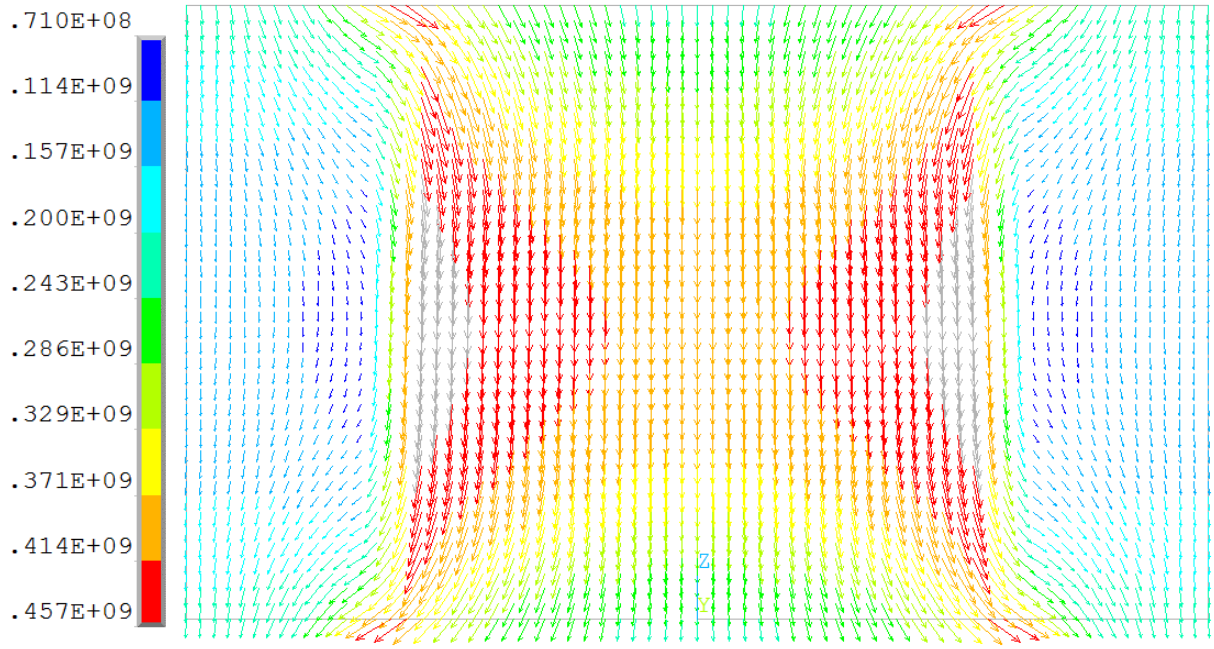

Figure 8: Heat Flux Vectors at a Vertical Cross-section of a Unit Cell
The top and bottom faces of the cell have constant flux boundary conditions of the same magnitude. The mid-plane contains an isotherm, as evidenced by the parallel flux vectors there. Units are in W/m^2-K

3.2.2 Outcome of FEA – Convection Boundaries

A base TXV array geometry was chosen, consisting of 60 µm diameter cylindrical copper vias arranged in a 100 µm pitch, aligned array embedded in a 200 µm thick glass substrate. Motivated by interest in enhanced low-conductivity interposers, these dimensions are within the realm of current manufacturing practice [9] and provide a high copper fill factor of 28%. The thermal conductivities for the glass and copper are 1 and 400 W/m-K, respectively. While the phenomenon of micro-spreading occurs to some degree in any via unit cell, the fitting parameters presented in this section are specific to this cell's materials and lateral dimensions. However, the methodology and correlation form are broadly applicable.

Modeling the cell in ANSYS finite element software, and applying an isothermal boundary to the bottom face of the cell and a convection boundary with varying h to the top, the thermal response and thus $k_{eff,z}$ of the cell was calculated using Eqs. (8-10). Cells subjected to very high h (10^{10} W/m^2-K) were modeled to illustrate that $k_{eff,z}$ for these cells agrees with those subjected to two isothermal boundaries. Cells subjected to very low h (1 W/m^2-K) were modeled to illustrate that $k_{eff,z}$ for these cells agrees with those subjected to one isoflux and one isothermal boundary. Plotted in Figure 9 are the $k_{eff,z}$ values for the 200 µm thick substrate as a function of applied h, as well as for fifteen other substrate thicknesses ranging from 25 to 500 µm.

What is immediately apparent is that in the isothermal limit, all substrate thicknesses exhibit the same $k_{eff,z}$, at 114.5 W/m-K. This agrees well with the rule of mixtures prediction, setting $\phi_{ox} = 0$ and $\phi_v = 28.3\%$. As the applied h decreases, however, the effective conductivity exhibits an orderly reduction, the final magnitude of which depends on the thickness of the substrate. Substrates with large thicknesses, and hence high aspect ratio vias, display the least reduction in $k_{eff,z}$ while low aspect ratio systems are affected the most.

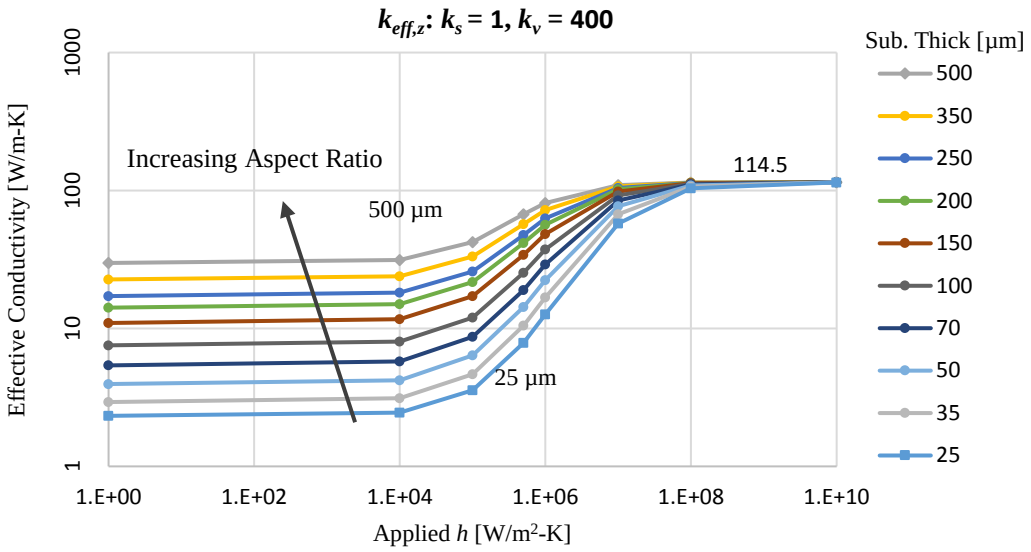

Figure 9: TXV Array $k_{eff,z}$ as Computed by FEA

The behavior of the unit cell can be explained by recasting the effective conductivity into a thermal resistance. The total (vertical) resistance R_T of the cell is given by

$$R_T = \frac{L}{A\, k_{eff,z}} = \frac{\Delta \bar{T}}{\dot{Q}} \tag{10}$$

Plotted in Figure 10 is R_T as a function of substrate thickness for five heat transfer coefficients. The curve with the lowest values has the highest h, corresponding to an isothermal boundary on the top face as well as the original isothermal condition on the bottom face. The fact that the resistance for these conditions increases linearly with cell thickness and has an intercept near the origin confirms the idea that heat flows one-dimensionally under these conditions. For thick

enough substrates, convection boundary curves evolve along a line above and parallel to the isothermal boundary curve.

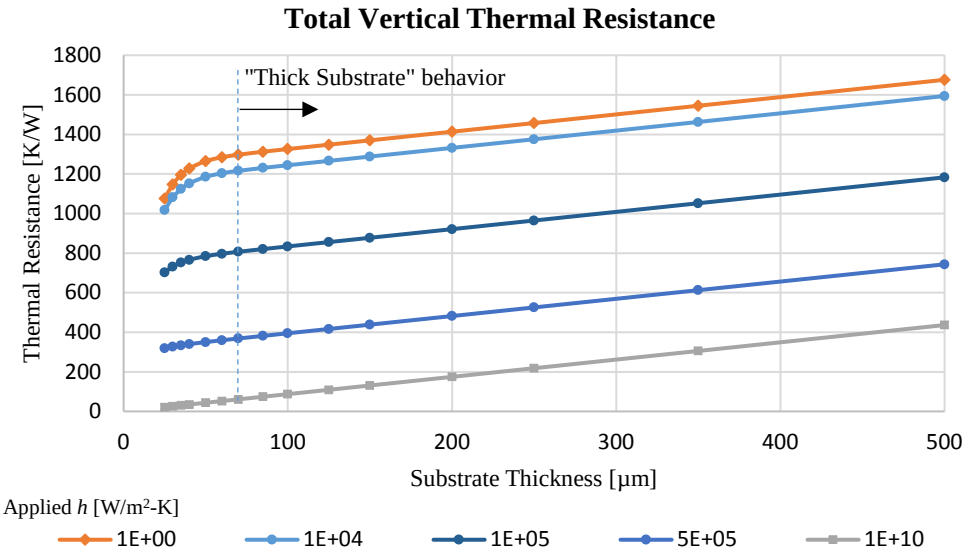

Figure 10: Via Cell Total Thermal Resistance, Calculated from $k_{eff,z}$ Data

This suggests that the total resistance of the unit cell can be ascribed to the sum of two effects. One is the one-dimensional resistance that linearly increases as the length of the cell increases, R_{1D}. The other, R_{sp}, is a resistance that grows quickly for thin substrates, and then converges to a constant value that depends on the applied h. R_{sp} for each case can be obtained by subtracting the R_{1D} from the total resistance. In this way, $k_{eff,z}$ can be modeled as

$$k_{eff,z} = \frac{L}{A(R_{1D} + R_{sp})} \tag{11}$$

where

$$R_{1D} = \frac{L}{A[\phi_v k_v + (1-\phi_v)k_s]} \tag{12}$$

and R_{sp} is identified as an ultimately constant spreading resistance that depends on the general boundary condition, the material properties and the lateral dimensions of the unit cell. This spreading resistance is due to the lateral flow of heat within the unit cell as flux entering the low conductivity substrate seeks the lower resistance path through the central via. This lateral flux component is visible in Figure 8.

Figure 11 shows this constant R_{sp} plotted versus the convection boundary heat transfer coefficient. R_{sp} is maximum when h is so low as to create an isoflux boundary. As h increases to isothermal conditions, R_{sp} drops to zero. A correlation for R_{sp} versus h is plotted as the curve connecting the points:

$$R_{sp} = \frac{R_{sp,max}}{1 + (\frac{hP}{k_s}/H_0)^{\beta}} \tag{13}$$

where $R_{sp,max}$ is the maximum spreading resistance seen with an isoflux boundary (here, 1240 K/W), P is the array pitch (i.e. unit cell width), and H_0 and β are dimensionless fitting parameters. The best fit for the data in Figure 11 is obtained with $H_0 = 15.5$ and $\beta = 0.96$.

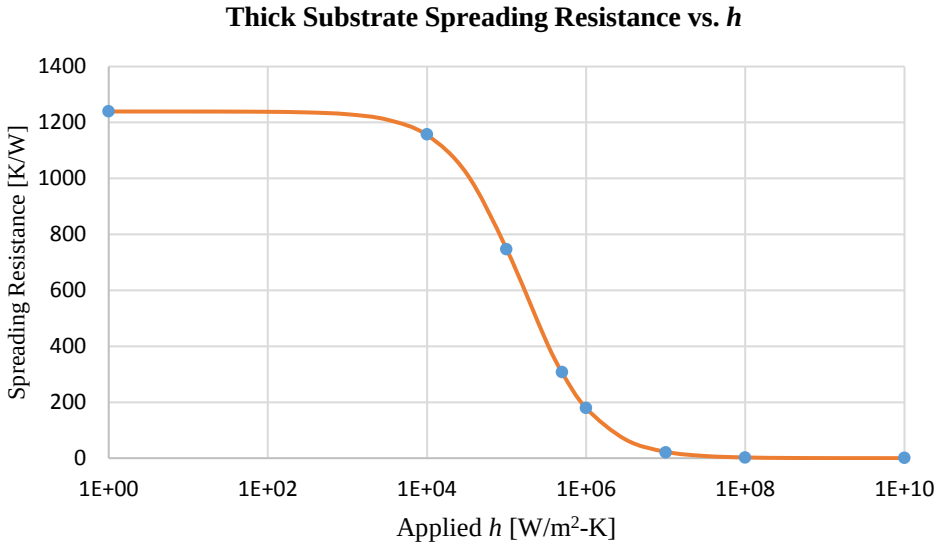

Figure 11: Spreading Resistance of Thick TXV Substrates
Each point is the intercept of the linear asymptote for data sets of the type in Figure 10 (there were three not included for clarity). The line connecting the points is the correlation given by Eq. (13).

3.2.3 Surface Films and Material Interfaces

Because no component of a thermal stack exists in isolation from the entire package, it is important to consider how various layers interact to affect the overall performance of the viaed layer or substrate. In this section, the effect of contacting materials bonded to the surface of a TXV is investigated. These materials may be die attach materials, metallization films, bulk substrates or even back end of line (BEOL) layers. The effect of surface oxide layers and/or bond pads could also be modeled as that of a contacting material, albeit one with a laterally varying conductivity.

Finite element modeling was performed in a fashion similar to the last section. An isothermal boundary was placed at the bottom face of 60 µm diameter, 100 µm pitch copper-glass via cell of varying thickness. Next, a film layer of varying thickness and conductivity was placed on the top face of the Cu-glass region. A boundary condition was then placed on the exposed top surface of the film layer, and all other surfaces insulated. Isothermal and isoflux film boundary conditions were investigated.

The $k_{eff,z}$ of the Cu-glass is then evaluated using Eqs. (8-10) by placing the upper reference surface at the glass-film interface and the lower at the bottom of the cell. In this way the resulting $k_{eff,z}$ measures the heat flow in the just TXV array itself, and not the film. Equivalent thermal resistance results can be obtained by including in the measurement the temperature drop across the film, which would then be subtracted out as an additional, static thermal resistance.

Plotted in Figure 12 are two solution sets for $k_{eff,z}$ of a 200 µm thick cell in contact with a film of conductivity $k_f = 40$ W/m-K. The set with the higher effective conductivities was evaluated from a system with an isothermal film boundary; the lower set from an isoflux film boundary. For very thin films, the $k_{eff,z}$ approaches the values of the cell possessed with an isothermal or isoflux boundary applied directly to the top of the substrate. As the film thickness increases, however, $k_{eff,z}$ converges to a single value. At this point, the boundary condition on the edge of the film is so far away from the Cu-glass region that its effect on the thermal conductivity is negligible and only the interaction of the via, substrate, and film material play a role in $k_{eff,z}$.

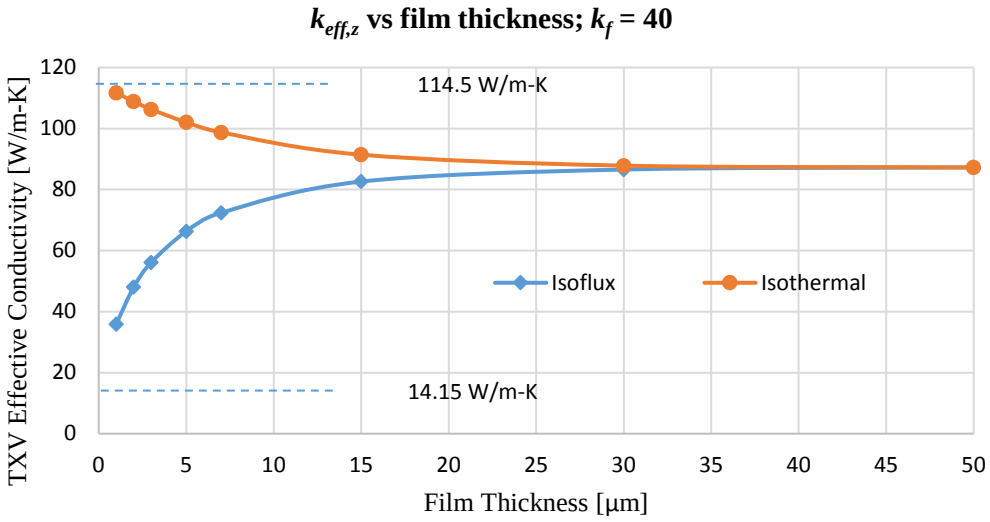

Figure 12: Evolution of $k_{eff,z}$ of a TXV Array as an Adhered Film Increases in Thickness
Film conductivity is 40 W/m-K, and substrate thickness is 200 µm.

Plotted in Figure 13 are these converged $k_{eff,z}$ values for sufficiently thick films of various conductivities and several substrate thicknesses. As in Figure 9, conditions that lead to more uniform substrate surface temperatures result in $k_{eff,z}$ closer to the rule-of-mixtures value. Instead of a high h convection boundary, here it is due to an interface with a high conductivity material. At the opposite end, the lowest conductivity film material produces a $k_{eff,z}$ close to that of an isoflux boundary.

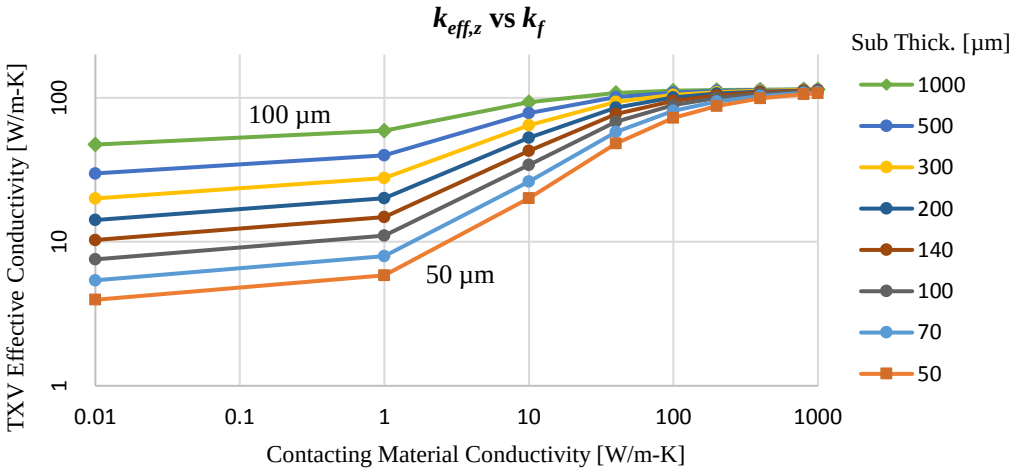

Figure 13: $k_{eff,z}$ versus Contacting Material Thermal Conductivity for Different Substrate/Cell Thicknesses

Recasting the $k_{eff,z}$ into thermal resistance and extracting the R_{sp} component as in the last section results in the data plotted in Figure 14. The curve in the plot is given by an analogous correlation:

$$R_{sp} = \frac{R_{sp,max}}{1 + (\frac{k_f}{k_s}/\kappa_0)^{\beta}} \tag{14}$$

where κ_0 and β are fitting parameters. Setting $\kappa_0 = 2$ and keeping $\beta = 0.96$ produces the curve shown. $R_{sp,max}$ remains at 1240 K/W since the geometry and materials of the TXV array are unchanged.

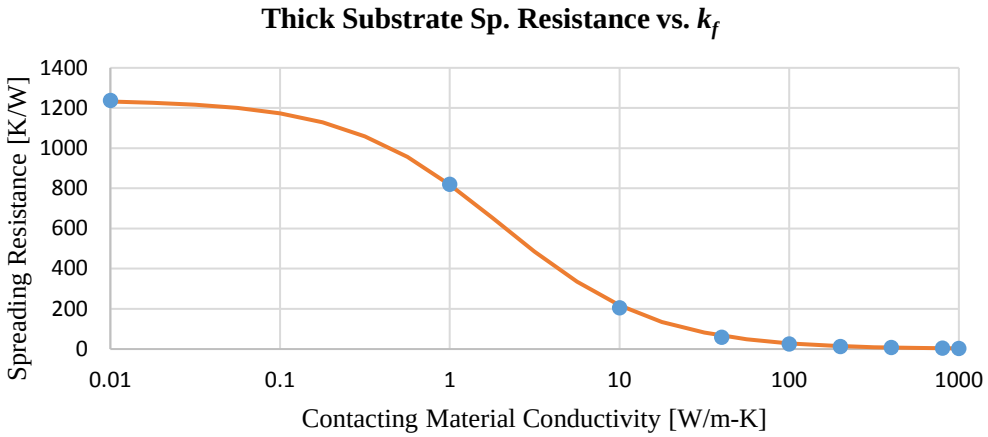

Figure 14: Spreading Resistance versus Contacting Material Conductivity
Each point is obtained from FEM data in Figure 13. The line connecting the points is the correlation given by Eq. (14).

From the work described above emerges a method of estimating the $k_{eff,z}$ of an entire cylindrical TXV array under general conditions. For a thick enough substrate, R_{sp} is insensitive to the length of the via. Two such substrate cells can be joined at the isothermal boundary condition, resulting in a larger cell with general boundaries on its upper and lower faces. The vertical effective conductivity of such a TXV array is then

$$k_{eff,z} = \frac{L}{A\left[R_{1D} + (f_u + f_l)R_{sp,max}\right]} \tag{15}$$

where

$$R_{1D} = \frac{L}{A[\phi_v k_v + (1-\phi_v)k_s]} \tag{16}$$

and u and l refer to the upper and lower surfaces of the TXV array and f is an "adjustment" factor depending on the conditions at that surface. For a convection boundary at the surface

$$f = \left[1 + (\frac{hP}{k_s}/H_0)^{\beta}\right]^{-1} \tag{17}$$

and for a material interface

$$f = \left[1 + (\frac{k_f}{k_s}/\kappa_0)^{\beta}\right]^{-1} \tag{18}$$

There are a few assumptions and restrictions upon which Eqs. (15-18) rely. First, the substrate containing the TXV array is assumed to be thick enough for the spreading resistances associated with each boundary to reach a constant value. For the materials, via diameter, and pitch used in this subchapter that thickness is about 120 μm. Increasing the substrate material conductivity or the via and cell aspect ratio will reduce this thickness. Applying Eqs. (15-18) to insufficiently thick substrates will result in an underestimate of $k_{eff,z}$, with the maximum error occurring when both TXV surface boundaries are isoflux and $f_u + f_l = 2$.

Second, the thickness of any contacting material used in Figure 15 must be large enough to disregard the conditions on the other side of the material or film. As suggested by Figure 12, for the array studied here this thickness is about 35 μm. Higher aspect vias and cells will reduce this thickness. Insufficiently thick contacting films will allow conditions on the other side of the film to influence the R_{sp} attributable to the film-TXV interface.

Third, the contacting materials considered have been of uniform conductivity. In practical TXV arrays, via bond pads provide a conductive material over part of the TXV array surface, and a comparison of their effect versus that of a film of uniform extent is currently being conducted. Surface oxide layers isolating vias and bond pads from a semiconductor substrate are also being investigated but are outside the scope of the work described in this subchapter.

3.2.4 Subchapter Summary

In the process of homogenizing a thermal via array, care must be taken in determining the effective vertical thermal conductivity. Rather than behaving as a bulk material, the array's thermal response includes important surface effects that depend both on the array parameters and the environment to which it is responding. These surface effects manifest in the form of a micro-spreading resistance that must be confronted in addition to the thermal resistance predicted by a rule-of-mixtures.

A framework is given for modeling the phenomenon of micro-spreading resistance. In this framework, an effort is made to decouple the intrinsic capacity of a via cell to exhibit micro-spreading, represented by $R_{sp,max}$, and the role of the array's environment in bringing this resistance into play, captured by f_u and f_l. This subchapter focuses its effort on the latter.

Motivated by glass interposer design, where micro-spreading plays a significant role, a case study is made using a copper-glass via array. While the correlations of Eqs. (13) and (14) remain faithful for uniform scaling of lateral cell dimensions and/or material conductivities (when $R_{sp,max}$ has also been appropriately scaled) it is acknowledged that changing the via fill factor or the cell conductivity ratio k_v/k_s requires adjustment of the fitting parameters. In [57] a large FEM survey on a variety of via cell sizes and conductivities if performed to better understand how the parameters must change, and a correlation to predict their values is presented.

Even so, the framework is able to make general recommendations for designers wishing to mitigate micro-spreading resistance. High aspect ratio vias result in a lower relative contribution of micro-spreading resistance to that of the 1D resistance. Additionally, the reduction of lateral scale increases the apparent h for convection boundaries (Eq. (13), always helpful) and increases the apparent film thickness (Figure 12, helpful for high conductivity films). Beyond aspect ratio, designers should endeavor to place the highest conductivity materials and highest h cooling available at the array surface.

This framework, when coupled with an analytic or empirical formula for $R_{sp,max}$ based on the internal cell parameters, will allow designers to estimate $k_{eff,z}$ for a wide range of TXV systems without direct analysis with FEM. This frees the designer to optimize a TXV array for a given system based on desired thermal conductivity properties.

3.3 Analytic Model of Microspreading in Via Array Unit Cells

This subchapter is an analytic treatment of the microspreading resistance that has been investigated during the course of this program. The hope is that in addition to providing a physics-based underpinning to the FEM-based correlations developed so far, the analytical model can point to useful relations for so far untreated facets of microspreading, such as the maximum (at isoflux) cell resistance or the effect of an interfacial resistance between the via and the substrate (as is seen in through-silicon vias due to their oxide liners).

The basis of the analytical model is the solution of the boundary value problem associated with a via cell experiencing an isoflux boundary condition on one exposed surface. As shown in Figure 15, the via cell is treated as an axisymmetric system containing the cylindrical via within a material having an outer diameter equal to the "equivalent pitch" of the array, such that the fill-factor of the cell matches that of the array. This outer surface is adiabatic, while the upper surface of the cell is subjected to a uniform heat flux and the lower surface fixed at a zero reference temperature. Between the via and the substrate is a finite interfacial conductance, *h*, that can be used to model the effects of imperfect interfaces or additional low conductivity layers between the via and the substrate.

The governing differential equation of this steady state problem is Laplace's Equation in two cylindrical dimensions, *r* and *z*. Because there are two media, the problem can be separated into two domains that are coupled along the interface at $r=a$. Thus the equations and boundary conditions to be solved are

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T_1}{\partial r}\right)+\frac{\partial^2 T_1}{\partial z^2}=0 \qquad \frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial T_2}{\partial r}\right)+\frac{\partial^2 T_2}{\partial z^2}=0$$

$$\frac{\partial T_1}{\partial z}(r,0)=-\frac{q}{k_1} \qquad \frac{\partial T_2}{\partial z}(r,0)=-\frac{q}{k_2}$$

$$T_1(r,L)=0 \qquad T_2(r,L)=0$$

$$\frac{\partial T_1}{\partial r}(0,z)=0 \qquad \frac{\partial T_2}{\partial r}(b,z)=0$$

$$\frac{\partial T_1}{\partial r}(a,z)=\frac{-h}{k_1}\left(T_1(a,z)-T_2(a,z)\right) \qquad \frac{\partial T_2}{\partial r}(a,z)=\frac{h}{k_2}\left(T_2(a,z)-T_1(a,z)\right)$$

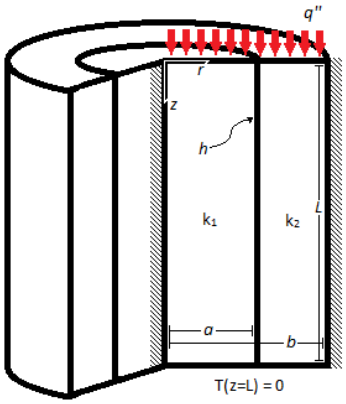

Figure 15: Schematic of Boundary Value Problem

In order to solve Laplace's equation using separation of variables, all but one of the boundary conditions should be homogeneous; each of these problems has two inhomogeneous conditions. To rectify this, each can be broken into a superposition of two subproblems that each satisfy only one inhomogeneous condition. To further simplify the solution, the problems can be nondimensionalized, using characteristic lengths a and L and characteristic temperature $Q = qL/k_1$, by transforming coordinates $\rho = r/a$ and $\zeta = z/L$ and solution $\Theta = T/Q$. This reduces the independent parameters of the cell from seven to four: (b/a), (L/a), $K = k_1/k_2$, and $H = ha/k_1$. The problems to be solved are thus:

$$\left(\frac{L}{a}\right)^2 \frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\Theta_{1,r}}{\partial\rho}\right)+\frac{\partial^2\Theta_{1,r}}{\partial\zeta^2}=0 \qquad \left(\frac{L}{a}\right)^2 \frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\Theta_{2,r}}{\partial\rho}\right)+\frac{\partial^2\Theta_{2,r}}{\partial\zeta^2}=0$$

$$\frac{\partial\Theta_{1,r}}{\partial\zeta}(\rho,0)=0 \qquad \frac{\partial\Theta_{2,r}}{\partial\zeta}(\rho,0)=0$$

$$\Theta_{1,r}(\rho,1)=0 \qquad \Theta_2,r(\rho,1)=0$$

$$\frac{\partial\Theta_{1,r}}{\partial\rho}(0,\zeta)=0 \qquad \frac{\partial\Theta_{2,r}}{\partial\rho}\left(\frac{b}{a},\zeta\right)=0$$

$$\frac{\partial\Theta_{1,r}}{\partial\rho}(1,\zeta)+H\,\Theta_{1,r}(1,\zeta)=H\,\Theta_2(1,\zeta) \qquad \frac{\partial\Theta_{2,r}}{\partial\rho}(1,\zeta)-KH\,\Theta_{2,r}(1,\zeta)=-KH\,\Theta_1(1,\zeta)$$

$$\left(\frac{L}{a}\right)^2 \frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\Theta_{1,z}}{\partial\rho}\right)+\frac{\partial^2\Theta_{1,z}}{\partial\zeta^2}=0 \qquad \left(\frac{L}{a}\right)^2 \frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\rho\frac{\partial\Theta_{2,z}}{\partial\rho}\right)+\frac{\partial^2\Theta_{2,z}}{\partial\zeta^2}=0$$

$$\frac{\partial\Theta_{1,z}}{\partial\zeta}(\rho,0)=-1 \qquad \frac{\partial\Theta_{2,z}}{\partial\zeta}(\rho,0)=-K$$

$$\Theta_{1,z}(\rho,1)=0 \qquad \Theta_{2,z}(\rho,1)=0$$

$$\frac{\partial\Theta_{1,z}}{\partial\rho}(0,\zeta)=0 \qquad \frac{\partial\Theta_{2,z}}{\partial\rho}\left(\frac{b}{a},\zeta\right)=0$$

$$\frac{\partial\Theta_{1,z}}{\partial\rho}(1,\zeta)+H\,\Theta_{1,z}(1,\zeta)=0 \qquad \frac{\partial\Theta_{2,z}}{\partial\rho}(1,\zeta)-KH\,\Theta_{2,z}(1,\zeta)=0$$

The subscripts in each problem refer to the material (1 for via, 2 for substrate) and to the direction normal to the boundary possessing the inhomogeneous condition. For each of the *r* and *z* subproblems, there is a physical interpretation. For the *z* problems, each material is unaware of the other, and heat conducts in through the upper isoflux surface, and down towards the bottom and the location of the interface. The heat leaves each material through the bottom fixed at zero, but also "convects to zero" at the location of the interface based on H and K.

In the *r* subproblems, the coupling between the two materials is introduced. The upper surface is now insulated, and heat is now introduced at the interface depending on the temperature in the material on the other side at the interface. This temperature used to introduce heat is the total temperature in the other material – that is, the superposition of that materials subproblems.

The eigenfunctions of these problems will involve trigonometric functions of the vertical dimension, ζ, and Bessel functions or linear combinations of Bessel functions (so called cylinder functions) of the radial dimension, ρ.

The solution for the dimensionless temperature field within the cell is

$$\frac{T_1(\rho,\zeta)}{Q} = \Theta_1(\rho,\zeta) = \Theta_{1,r}(\rho,\zeta) + \Theta_{1,z}(\rho,\zeta)$$

$$= 4H\sum_{n=1}^{\infty}\frac{\tilde{C}_n K^2 F_n + \psi_0(\lambda_n)G_n}{\tilde{A}_n\tilde{C}_n - I_0(\lambda_n)\psi_0(\lambda_n)}\cos\left(\frac{L}{a}\lambda_n\zeta\right)I_0(\lambda_n\rho) + 2H\sum_{m=1}^{\infty}\frac{J_0(\mu_m\rho)}{[H^2+\mu_m^2]J_0(\mu_m)}\frac{\sinh\left(\frac{L}{a}\mu_m(1-\zeta)\right)}{\left(\frac{L}{a}\mu_m\right)\cosh\left(\frac{L}{a}\mu_m\right)}$$

$$\frac{T_2(\rho,\zeta)}{Q} = \Theta_2(\rho,\zeta) = \Theta_{2,r}(\rho,\zeta) \ + \Theta_{2,z}(\rho,\zeta)$$

$$= 4H\sum_{n=1}^{\infty}\frac{I_0(\lambda_n)K^2F_n + \tilde{A}_n G_n}{\tilde{A}_n\tilde{C}_n - I_0(\lambda_n)\psi_0(\lambda_n)}\cos\left(\frac{L}{a}\lambda_n\zeta\right)\psi_0(\lambda_n\rho) + 2K^2H\sum_{k=1}^{\infty}\frac{\phi_0(\mu_k)\phi_0(\mu_k\rho)}{\frac{4}{\pi^2} - [(KH)^2+\mu_k{}^2]\phi_0{}^2(\mu_k)}\frac{\sinh\left(\frac{L}{a}\mu_k(1-\zeta)\right)}{\left(\frac{L}{a}\mu_k\right)\cosh\left(\frac{L}{a}\mu_k\right)}$$

With Θ_1 in domain	$\rho \in [0,1]\ and\ \zeta \in [0,1]$	(1.3)
With Θ_2 in domain	$\rho \in \left[1, {}^{b}/_{a}\right]\ and\ \zeta \in [0,1]$	(1.4)
with vertical eigenvalues	$\lambda_n = \frac{\left(n-\frac{1}{2}\right)\pi}{L/a} \quad for\ n = 1,2,3\ \ldots$	(1.5)
where cylinder functions	$\psi_\nu(\lambda_n\rho) = \underline{K_1}\left(\lambda_n\frac{b}{a}\right)I_\nu(\lambda_n\rho) + (-1)^\nu\underline{I_1}\left(\lambda_n\frac{b}{a}\right)K_\nu(\lambda_n\rho) \quad for\ \nu = 0,1$	(1.6)
	$\phi_\nu(\mu_k\rho) = \underline{Y_1}\left(\mu_k\frac{b}{a}\right)J_\nu(\mu_k\rho) - \underline{J_1}\left(\mu_k\frac{b}{a}\right)Y_\nu(\mu_k\rho) \quad for\ \nu = 0,1$	(1.7)
with radial eigenvalues	$\mu_m\ the\ mth\ root\ satisfying\ \ \mu J_1(\mu) - H J_0(\mu) = 0$	(1.8)
	$\mu_k\ the\ kth\ root\ satisfying\ \ \mu\,\phi_1(\mu) + KH\phi_0(\mu) = 0$	(1.9)
where contribution factors	$G_n = \sum_{m=1}^{\infty}\frac{1}{[H^2+\mu_m^2]}\cdot\frac{1}{\left(\frac{L}{a}\mu_m\right)^2 + \left[\left(n-\frac{1}{2}\right)\pi\right]^2} \quad for\ n = 1,2,3\ \ldots$	(1.10)
	$F_n = \sum_{k=1}^{\infty}\frac{\phi_0{}^2(\mu_k)}{\frac{4}{\pi^2} - [(KH)^2+\mu_k^2]\phi_0{}^2(\mu_k)}\cdot\frac{1}{\left(\frac{L}{a}\mu_k\right)^2 + \left[\left(n-\frac{1}{2}\right)\pi\right]^2}$	(1.11)
where convection factors	$\tilde{A}_n = \frac{1}{H}[\lambda_n I_1(\lambda_n) + H I_0(\lambda_n)]$	(1.12)
	$\tilde{C}_n = \frac{1}{KH}[-\lambda_n\psi_1(\lambda_n) + KH\psi_0(\lambda_n)]$	(1.13)
And non-dim. BVP parameters	$\frac{L}{a}, \frac{b}{a}, H = \frac{ha}{k_1}, K = \frac{k_1}{k_2}, Q = \frac{qL}{k_1}$	(1.14)

In order to calculate the cell's vertical thermal resistance, and from there the microspreading resistance, the average temperature of the upper surface must be known. In non-dimensional form, relevant average surface temperatures are:

$$\frac{\bar{T}_1}{Q} = \frac{2\pi \int_0^1 \rho\, \Theta_1(\rho,0) d\rho}{2\pi \int_0^1 \rho\, d\rho} = 2\tau_1$$	
$$\frac{\bar{T}_2}{Q} = \frac{2\pi \int_1^{b/a} \rho\, \Theta_2(\rho,0) d\rho}{\pi\left(\left({}^{b}/_{a}\right)^2 - 1\right)} = \frac{2}{\left({}^{b}/_{a}\right)^2 - 1}\tau_2$$	
$$\frac{\bar{T}}{Q} = \frac{2\pi\left[\int_0^1 \rho\, \Theta_1(\rho,0) d\rho + \int_1^{b/a} \rho\, \Theta_2(\rho,0) d\rho\right]}{\pi\left({}^{b}/_{a}\right)^2} = \frac{2}{\left({}^{b}/_{a}\right)^2}[\tau_1 + \tau_2]$$	

where the surface temperature integrals $\int_0^1 \rho\, \Theta_1(\rho,0) d\rho$ and $\int_1^{b/a} \rho\, \Theta_2(\rho,0) d\rho$ are

$$\tau_1 = \tau_{1,r} + \tau_{1,z} = 4H \sum_{n=1}^{\infty} \frac{\tilde{C}_n K^2 F_n + \psi_0(\lambda_n) G_n}{\tilde{A}_n \tilde{C}_n - I_0(\lambda_n)\psi_0(\lambda_n)} \frac{I_1(\lambda_n)}{\lambda_n} + 2H^2 \sum_{m=1}^{\infty} \frac{\tanh\left(\frac{L}{a}\mu_m\right)}{[H^2 + {\mu_m}^2]\left(\frac{L}{a}{\mu_m}^3\right)}$$	(2.1)
$$\tau_2 = \tau_{2,r} + \tau_{2,z} = 4H \sum_{n=1}^{\infty} \frac{I_0(\lambda_n) K^2 F_n + \tilde{A}_n G_n}{\tilde{A}_n \tilde{C}_n - I_0(\lambda_n)\psi_0(\lambda_n)} \frac{-\psi_1(\lambda_n)}{\lambda_n} + 2K^3 H^2 \sum_{k=1}^{\infty} \frac{{\phi_0}^2(\mu_k)}{\frac{4}{\pi^2} - [(KH)^2 + {\mu_k}^2]{\phi_0}^2(\mu_k)} \frac{\tanh\left(\frac{L}{a}\mu_k\right)}{\left(\frac{L}{a}{\mu_k}^3\right)}$$	(2.2)

From these temperatures, the microspreading resistance is (in one nondimensional form):

$$R_{sp}\pi k_1 b = \left(\frac{L}{a}\right)\left(\frac{b}{a}\right)\left\{\frac{2}{\left({}^{b}/_{a}\right)^4}[\tau_1 + \tau_2] - \frac{K}{(K-1) + \left({}^{b}/_{a}\right)^2}\right\}$$	(3.1)

These series solutions can be compared to previous results obtained by FEM. In the axisymmetric cells surveyed in the preceding chapter, there was assumed a perfect thermal interface between the cell materials. The maximum cell microspreading resistance was computed from cells that were subjected to an isoflux boundary condition in FEM. By summing a finite sequence of terms of the infinite series solution, the FEM data contained in Figure 16 can be reproduced. Just as decreasing the size of the elements in the FE model yields results closer to the "true" value of spreading, so to does the approximation from a finite series improve as more terms are added. To achieve good agreement with FEM (e.g. within 1%) for the large values of spreading resistance (such as when $k_v/k_s = 1000$) only around 10 terms are needed, while for systems where spreading is very small compared to the 1D resistance (like when k_v/k_s is close to 1), hundreds of terms are needed. This is because $[\tau_1 + \tau_2]$ factors into the total cell resistance, and resolving the comparatively small spreading component (by subtracting the second, 1D term in Eq. 3.1) requires many more terms.

As stated before, the FEM data assumed perfect thermal contact between the via and substrate. This can be approximated by choosing a large value of H (100 is usually sufficient). Alternatively, the analytical solution can be reduced by taking the limit $H \to \infty$ and making the approximation exact. In this limit, the solution is:

$$\lim_{h\to\infty}\Theta_1(\rho,\zeta) = \lim_{h\to\infty}\Theta_{1,r}(\rho,\zeta) + \lim_{h\to\infty}\Theta_{1,z}(\rho,\zeta)$$
$$= \sum_{n=1}^{\infty}\frac{4}{\lambda_n}\frac{K\psi_0(\lambda_n)\,O_n}{K\psi_0(\lambda_n)\,I_1(\lambda_n) - I_0(\lambda_n)\psi_1(\lambda_n)}\cos\left(\frac{L}{a}\lambda_n\zeta\right)I_0(\lambda_n\rho) + 2\sum_{m=1}^{\infty}\frac{J_0(\mu_m\rho)}{\mu_m J_1(\mu_m)}\cdot\frac{\sinh\left(\frac{L}{a}\mu_m(1-\zeta)\right)}{\left(\frac{L}{a}\mu_m\right)\cosh\left(\frac{L}{a}\mu_m\right)}$$

$$\lim_{h\to\infty}\Theta_2(\rho,\zeta) = \lim_{h\to\infty}\Theta_{2,r}(\rho,\zeta) + \lim_{h\to\infty}\Theta_{2,z}(\rho,\zeta)$$
$$= \sum_{n=1}^{\infty}\frac{4}{\lambda_n}\frac{KI_0(\lambda_n)\,O_n}{K\psi_0(\lambda_n)\,I_1(\lambda_n) - I_0(\lambda_n)\psi_1(\lambda_n)}\cos\left(\frac{L}{a}\lambda_n\zeta\right)\psi_0(\lambda_n\rho) + 2\sum_{k=1}^{\infty}\frac{\mu_k\phi_1(\mu_k)\phi_0(\mu_k\rho)}{{\mu_k}^2{\phi_1}^2(\mu_k) - \frac{4}{\pi^2}}\cdot\frac{\sinh\left(\frac{L}{a}\mu_k(1-\zeta)\right)}{\left(\frac{L}{a}\mu_k\right)\cosh\left(\frac{L}{a}\mu_k\right)}$$

With Θ_1 in domain	$\rho \in [0,1]\ and\ \zeta \in [0,1]$	(4.3)
With Θ_2 in domain	$\rho \in \left[1, {}^{b}/_{a}\right]\ and\ \zeta \in [0,1]$	(4.4)
with vertical eigenvalues	$\lambda_n = \dfrac{\left(n-\frac{1}{2}\right)\pi}{L/a} \quad for\ n = 1,2,3\ \ldots$	(4.5)
where cylinder functions	$\psi_\nu(\lambda_n\rho) = \underline{K_1}\left(\lambda_n\dfrac{b}{a}\right)I_\nu(\lambda_n\rho) + (-1)^\nu\underline{I_1}\left(\lambda_n\dfrac{b}{a}\right)K_\nu(\lambda_n\rho) \quad for\ \nu = 0,1$	(4.6)
	$\phi_\nu(\mu_k\rho) = \underline{Y_1}\left(\mu_k\dfrac{b}{a}\right)J_\nu(\mu_k\rho) - \underline{J_1}\left(\mu_k\dfrac{b}{a}\right)Y_\nu(\mu_k\rho) \quad for\ \nu = 0,1$	(4.7)
with radial eigenvalues	$\mu_m\ the\ mth\ root\ satisfying\ J_0(\mu) = 0$	(4.8)
	$\mu_k\ the\ kth\ root\ satisfying\ \phi_0(\mu) = 0$	(4.9)
where contribution factor	$O_n = \sum_{k=1}^{\infty}\dfrac{{\mu_k}^2{\phi_1}^2(\mu_k)}{\frac{4}{\pi^2} - {\mu_k}^2{\phi_1}^2(\mu_k)}\cdot\dfrac{1}{\left(\frac{L}{a}\mu_k\right)^2 + \left[\left(n-\frac{1}{2}\right)\pi\right]^2} + \sum_{m=1}^{\infty}\dfrac{1}{\left(\frac{L}{a}\mu_m\right)^2 + \left[\left(n-\frac{1}{2}\right)\pi\right]^2}$	(4.10)
And non-dim. BVP parameters	$\dfrac{L}{a}, \dfrac{b}{a}, K = \dfrac{k_1}{k_2}, Q = \dfrac{qL}{k_1}$	(4.11)

And for average surface temperatures:

$\lim_{h\to\infty}\tau_1 = \sum_{n=1}^{\infty}\dfrac{4}{\lambda_n^2}\dfrac{K\psi_0(\lambda_n)I_1(\lambda_n)\,O_n}{K\psi_0(\lambda_n)\,I_1(\lambda_n) - I_0(\lambda_n)\psi_1(\lambda_n)} + 2\sum_{m=1}^{\infty}\dfrac{\tanh\left(\frac{L}{a}\mu_m\right)}{\left(\frac{L}{a}{\mu_m}^3\right)}$	(5.1)
$\lim_{h\to\infty}\tau_2 = \sum_{n=1}^{\infty}\dfrac{4}{\lambda_n^2}\dfrac{-K\psi_1(\lambda_n)I_0(\lambda_n)\,O_n}{K\psi_0(\lambda_n)\,I_1(\lambda_n) - I_0(\lambda_n)\psi_1(\lambda_n)} + 2K\sum_{k=1}^{\infty}\dfrac{{\mu_k}^2{\phi_1}^2(\mu_k)}{\frac{4}{\pi^2} - {\mu_k}^2{\phi_1}^2(\mu_k)}\dfrac{\tanh\left(\frac{L}{a}\mu_k\right)}{\left(\frac{L}{a}{\mu_k}^3\right)}$	(5.2)

What is more interesting than just replicating prior FEM data is exploring the effects of finite interface conductances. Examining the case where $K = 3$ (the red crosses in Figure 16), which is of the order seen in through-silicon via systems, low values of H should lead to a much higher spreading resistance. This is seen to be the case in Figure 17, where the peak spreading resistance increases by as much as six-fold. Since the interface conductance of a TSV can be estimated from the thickness and conductivity of its oxide liner: $h = k_{ox}/t$, H can easily be put in terms of oxide thickness relative to via diameter, $\varepsilon = t/2a$, by: $H = ha/k_v = 1/(2k_v\varepsilon)$.

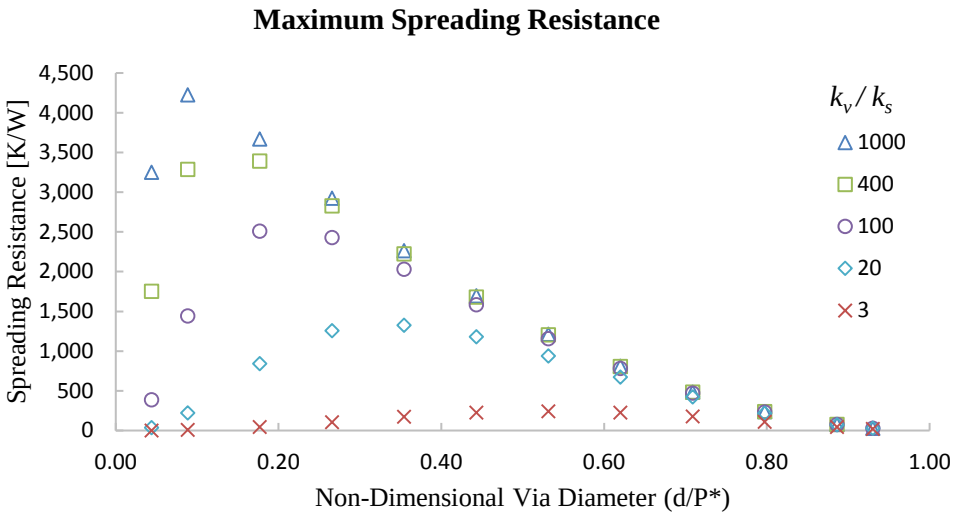

Figure 16: Maximum Cell Spreading Resistance as a Function of Via Diameter and Conductivity

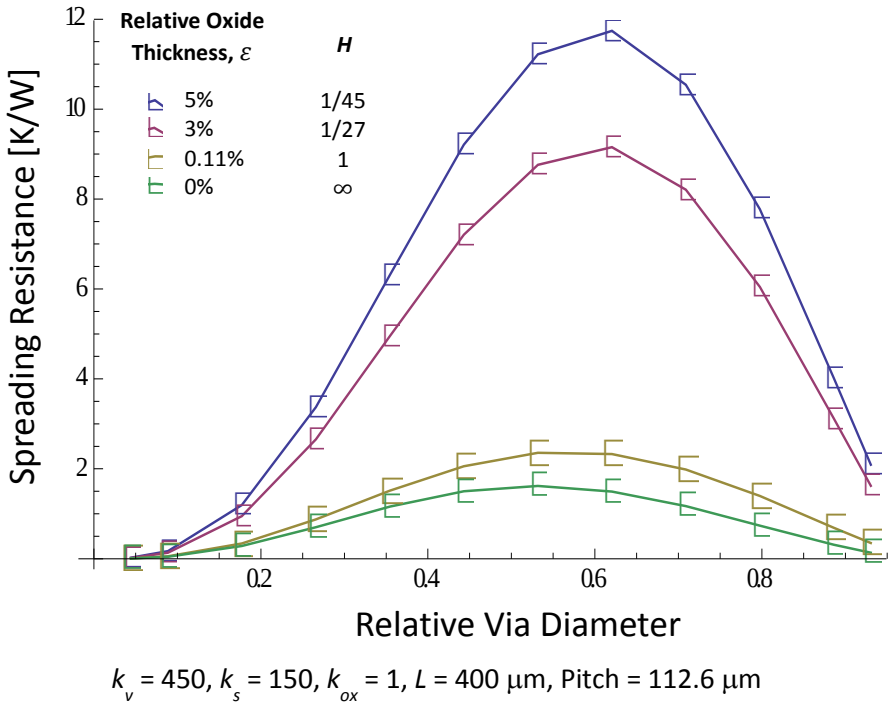

Figure 17: Spreading Resistance for a TSV-like System with Varying Interface Conductance

Much work remains to improve the usefulness of this analytic model. A useful, compact approximation or at least a precomputed root table and accuracy estimates would help reduce reliance on complex code necessary to compute eigenvalues and perform the many summations. In a different direction, generalizing this solution to the case where the cell surface is subjected to a convection boundary may provide some insight into the role of boundary conditions on microspreading, as was investigated in the preceding chapter. Another avenue is investigating how different cell geometries such as square via cells can be reconciled with the axisymmetric approximation, a task best suited for FEM. Lastly, integrating the solution along with any FEM-derived correlations for boundary effects or geometry into a solver tool that could be provided to thermal engineers to compute effective conductivities for arbitrary via arrays would provide the ideal method of disseminating this and related models to cooling system designers.

3.4 Anisotropic Thermal Constriction as Compact Model for Thermal Isolation Applications

In general, any thermal isolation application seeking to make use of a via-enhanced interposer to separate thermally disparate devices hosted on the same interposer will need to contend with a multitude of available design parameters. These pertain to the power dissipations and operating temperatures of the various electronic components, their locations on the surface of the interposer, details about the interposer and any vias it contains, as well as the cooling solution and any intervening layers.

In the previous case-study analysis, an effort was made to select only the design parameters that had the most significant impact on design goals, e.g. minimum device separation, operating temperatures, etc. However, even considering that relatively simple system, 15 or more parameters are needed to describe the construction of the via array, chiplet locations, differential cooling conditions, etc. To better examine the nature of the design tradeoffs available, two compact models that distill these parameters to a minimum required set were constructed. The first model retains the rectangular geometry of the amplifier while extending the edges of the interposer arbitrarily far from the device, while the second retains the close interposer edges but circularizes the system into an axisymmetric analogue.

As the first example or parameter reduction, the many details of the non-homogeneous interposer were assumed to be well modeled by an anisotropic effective conductivity and an upper and lower microspreading resistance, as described in previous subchapters. Then, the lateral dimensions of the system are scaled to transform the anisotropic conductivity to an isotropic one using the methodology in [42], while the spreading resistances are incorporated into the chip 1D resistance and the cooler convection coefficient, respectively. The final list of parameters used in this first compact model are listed in Table 2.

Table 2. Thermal Isolation Model Parameters

Hot device footprint	2 mm x 2.6 mm
Hot device dissipation flux	500 W/m^2-K (26 W total)
Hot device max temp, ΔT_h	155 K
Interposer Thermal Properties	*Varies by material*
Interposer Thickness	200 μm
Convection conductance *under the hot device*	30,000 W/m^2-K
Cold device max temp, ΔT_c	30 K

In this analysis, three interposer effective properties are chosen (representing copper vias in glass, copper vias in alumina, and bulk silicon) and the minimum device separation for the amplifier heat flux of 500 W/m^2-K was determined by examining the location where interposer surface temperature rise falls below 30 K. The interposer lateral dimensions were assumed to very large compared to the footprint of the amplifier, neglecting edge effects and obviating the need to specify interposer area dimensions. As expected, the highly isolating interposers required less device separation while at the same time producing elevated amplifier temperatures, as presented in Figure 18. The surface temperature of the interposer decays exponentially with distance from the edge of the amplifier chip.

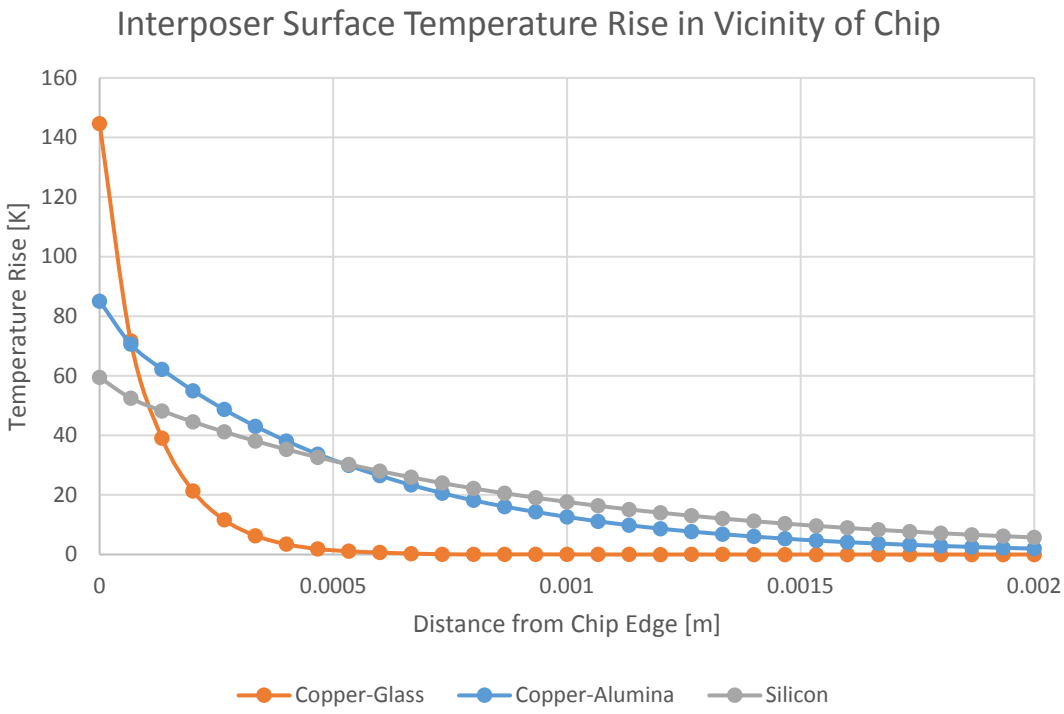

Figure 18: Interposer Surface Temperature Rise for Three Different Interposer Material Systems under the First Compact Model

The x-axis is the lateral distance from the amplifier chip edge. Interposer thickness is 200 µm and underside cooling is 30,000 W/m^2-K.

In a second model, seeking a further reduction of parameters, the interposer is treated as axisymmetric. In order to explore edge effects, a finite diameter for the interposer is reintroduced. It is chosen such that the area of the interposer is 25 mm^2, the same area as one half of the case study system, and as such containing one 5 mm^2 hotspot of constant flux representing the amplifier footprint. This leads to interposer and hotspot radii of 2.82 and 1.26 mm, respectively, as shown in Figure 19. The thickness of the interposer is chosen to be 200 µm for consistency with the case study and initial compact model.

The underside cooling is assigned a heat transfer coefficient of 30,000 W/m^2-K, and then repeated with a higher value of 100,000 W/m^2-K. The interposer is assigned a constant vertical conductivity of $k_z = 150$ W/m-K while the lateral conductivity, k_r, is allowed to vary between 1 W/m-K (glass) to 1000 W/m-K (a highly spreading material like highly ordered pyrolytic graphite). This simplified model is analyzed here using FEM, but it is hoped that will be straightforward to adapt existing thermal constriction models to treat it analytically. The spreading resistances are treated as in the first compact model: the lower resistance is wrapped into the heat transfer coefficient, and the upper one added to the 1D resistance of the amplifier chip, which together can be added as a static increase to the system thermal resistance.

One collection of parameters that make a cumbersome exercise of solving the reverse problem – the problem of determining some optimal system configuration that meets some specified device separation – are those consisting of the amplifier heat flux as well as the maximum operating

temperatures of the amplifier and CMOS. In this next phase of the model, rather than focusing separately on each maximum allowable rise (above that of the coolant fluid temperature), the ratio of the device max operating temperature rise $\Delta T_{cmos}/\Delta T_{amp}$ is be taken as the significant parameter. The amplifier flux is then be able to be related to ΔT_{amp} through the system thermal resistance, which can be extracted with FEM or with a thermal constriction solution [34, 36, 43]. For the system as described, this thermal resistance is plotted in Figure 20.

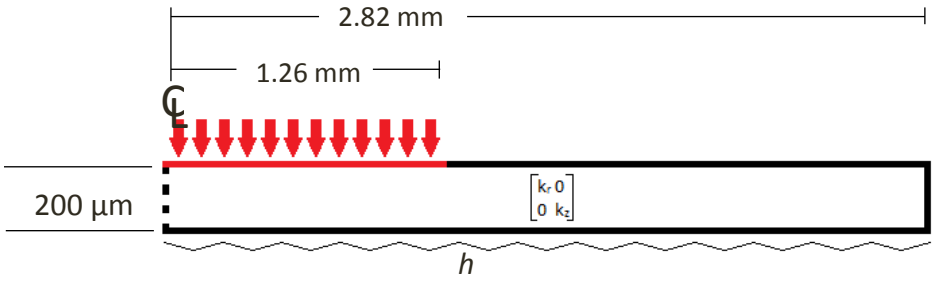

Figure 19: Schematic of Compact System Model

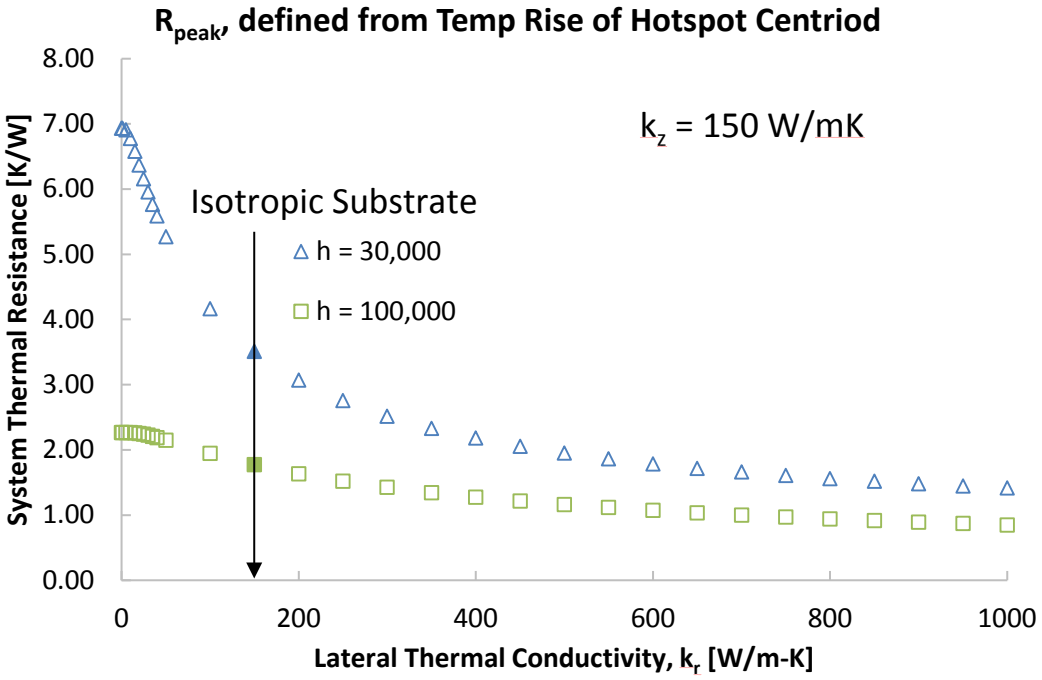

Figure 20: System Thermal Resistance, R_{peak} for Two Values of Underside Cooling Heat Transfer Coefficient

These total system resistances are straightforward to interpret. They are simply the temperature rise of the hottest point on the interposer, the centroid, per watt of heat entering through the hotspot. Figure 21 shows this temperature rise for a hotspot flux of 500 W/cm^2 – the same value used in the quarter four analysis – with underside cooling of 30,000 W/m^2-K. Since this corresponds to a hotspot power of 26 W, it is unsurprising that the peak surface temperature of about 180 K occurs for the $k_r = 1$ W/m-K interposer that has a resistance of about 7 K/W.

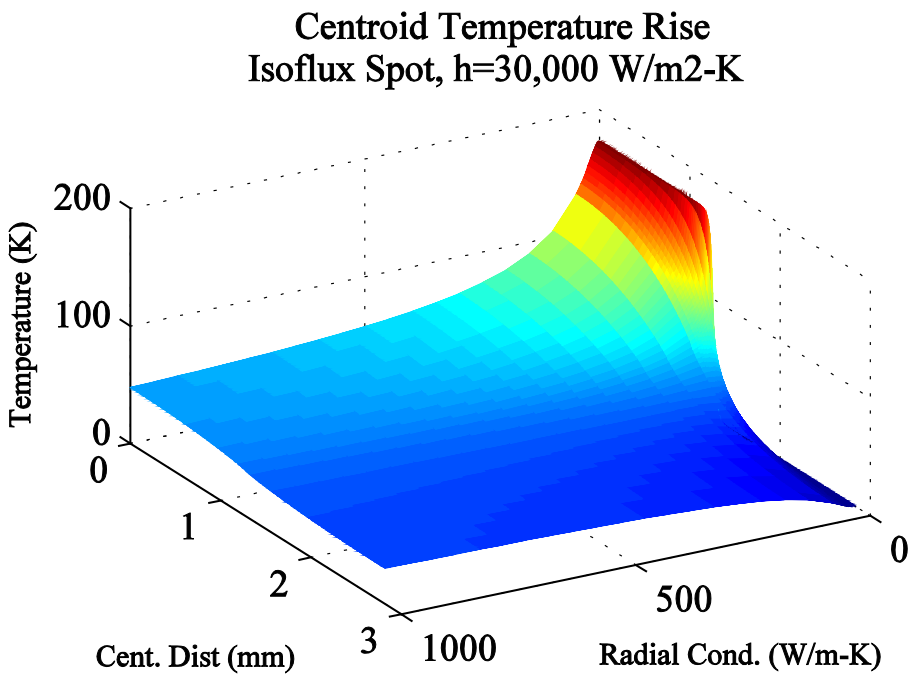

Figure 21: Raw Interposer Surface Temperature Rise for a Hotspot Flux of 500 W/cm^2 with Underside Cooling of h = 30,000 W/m^2-K and Varying Radial Conductivity, k_r
The hotspot radius is 1.26 mm.

What is more illuminating is when these surface temperatures are normalized by the centroid temperature for each system configuration. The result then represents the interposer temperatures that would occur if the amplifier is always run at its peak operating temperature. The ratio $\Delta T_{cmos}/\Delta T_{amp}$ then corresponds to a fixed cutoff height on a plot of these temperature as is shown in Figure 22. The intersection of this cutoff with the temperature curve for a given k_r then determines the device separation. Interestingly, since a constant-flux hotspot has been assumed, for cutoffs $\Delta T_{cmos}/\Delta T_{amp} \geq 0.5$, the device separation becomes negative for high-k_r interposers, as the edges of the amplifier drop below the maximum operating temperature of the CMOS devices. Though this quirk could be remedied by instead considering a constant-temperature hotspot, it is also simple enough to enforce a device separation ≥ 0.

If the family of curves plotted in Figure 22 are imagined as a surface, then the vertical contours of this surface would represent device separation vs. k_r for particular $\Delta T_{cmos}/\Delta T_{amp}$ cutoff ratios. Additionally, using Figure 20, k_r can be mapped to a system resistance, which also depends on other details of the system, such as h. In this way different systems can be compared on a consistent set of axes. Examples of this are shown in Figure 23 and Figure 24.

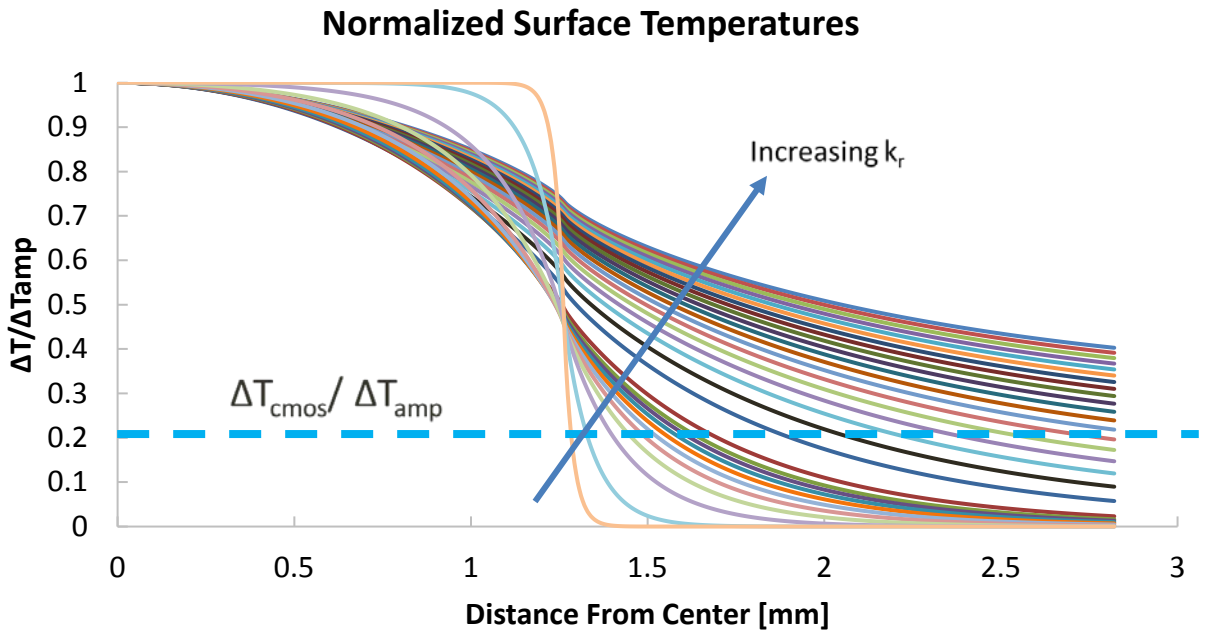

Figure 22: Interposer Surface Temperatures Normalized by Centroid Temperature
As $\boldsymbol{k_r}$ increases more spreading occurs, leading to less uniform hotspot temperatures and increased device separation for strict $\boldsymbol{\Delta T_{cmos}/\Delta T_{amp}}$ ratios. However allowable amplifier dissipation increases, as according to Figure 12. The black curve corresponds to an isotropic interposer, where $\boldsymbol{k_r = k_z = 150}$ W/m-K.

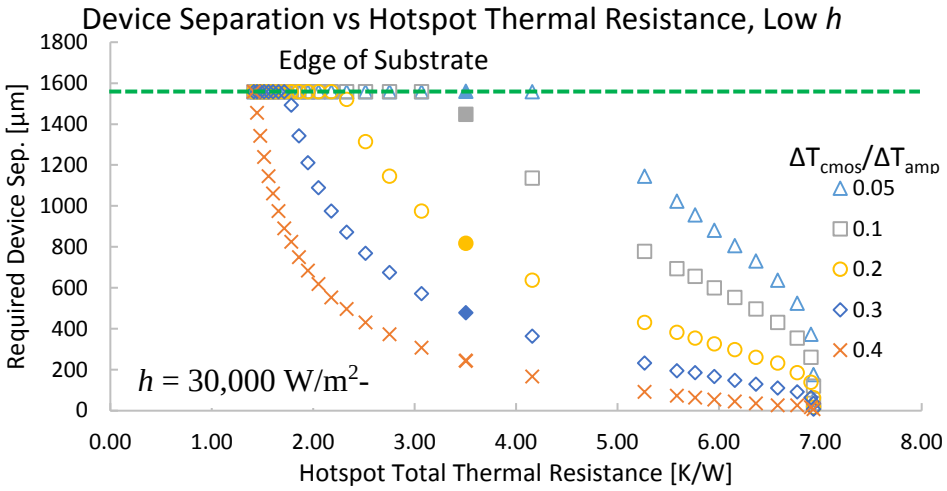

Figure 23: Device Separation vs. System Resistance Tradeoff Contours for the h = 30,000 W/m²-K case
Down and left are better, but for stricter cutoff ratios the contour is pushed out. Solid points correspond to an isotropic interposer, where $\boldsymbol{k_r = k_z = 150}$ W/m-K.

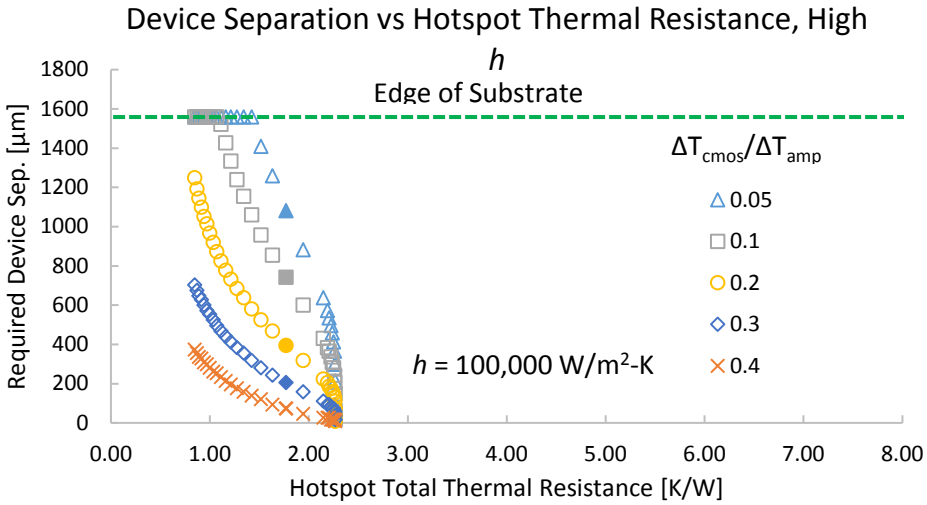

Figure 24: Device Separation vs. System Resistance Tradeoff Contours for the h = 100,000 W/m²-K case

Down and left are better, but for stricter cutoff ratios the contour is pushed out. Solid points correspond to an isotropic interposer, where $\boldsymbol{k_r = k_z = 150}$ *W/m-K.*

From these plots it can be seen that for strict cutoff ratios, there is a substantial tradeoff between device separation and system resistance. Low device separation reduced interconnect length and increases usable interposer real estate, but high system resistance requires the amplifier to be proportionately derated so that it doesn't exceed it operating temperature. For the strictest plotted ratio of 5%, the (isotropic) silicon interposer is unable to accommodate the CMOS device at all for h = 30,000 W/m²-K. Both these metrics can also be "inverted" so that the contours are Pareto curves, where the directions up and to the right are associated with improvements and the curves are the maximal designs for a given cutoff. Two examples of this are plotted in Figure 25 and Figure 26.

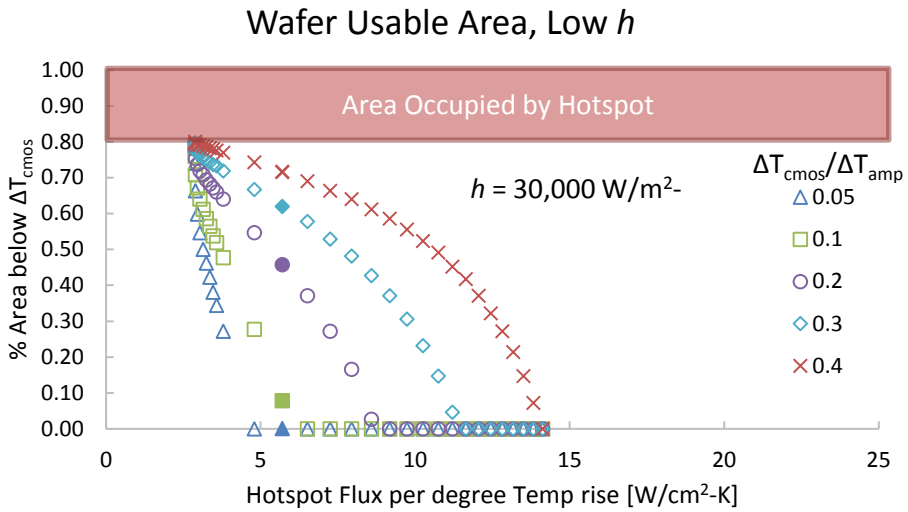

Figure 25: Usable Area vs Normalized Hotspot Flux for h = 30,000 W/m²-K

Up and right are better Lower cutoff ratios are more restrictive. Solid points correspond to an isotropic interposer.

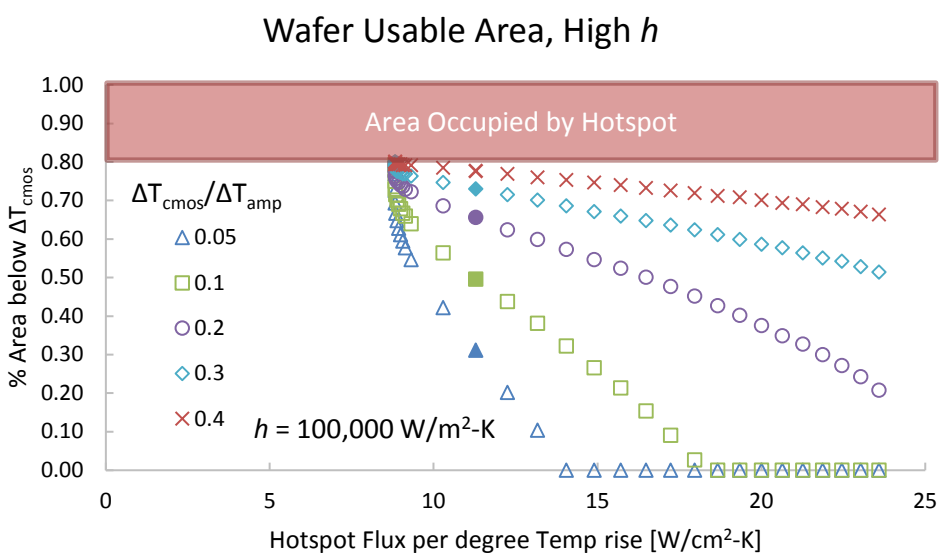

Figure 26: Usable Area vs Normalized Hotspot Flux for h = 100,000 W/m^2-K
Up and right are better. Lower cutoff ratios are more restrictive. Solid points correspond to an isotropic interposer.

In summary this new approach to modeling the interposer/cooler system looks to achieve a reduction in the number of distinct parameters needed to distinguish different classes of systems. By solving the constriction resistance problem, otherwise different systems can be compared on the basis of their system thermal resistance. This constriction problem also determines the interposer surface temperature distribution, which when combined with a specified CMOS cutoff temperature determines minimum CMOS separation from the high-power amplifier.

4.0 EXPERIMENTAL EFFORTS

The first section of this chapter describes a set of experiments that aim to validate the modeling of the thermal isolation case study, and demonstrate the principles described by the compact constriction system model. This section also introduces the design of the via array samples and the industry partners contracted to fabricate them.

A design of experiments of via array samples is contained in Table 3 and diagrammed in Figure 27. Two 15 cm diameter glass wafers, 400 µm thick, are each patterned into 16 test coupons. In each coupon, four 5 mm by 5 mm via arrays will be created with the array characteristics contained in the table. In addition to the table-defined parameters, half of the array samples (designated "A") are terminated with uniform 10 µm copper pads connecting all vias within the 25 mm^2 footprint. The other arrays have vias terminated with small nail-head pads individual to each via.

The through-holes for the vias were created with an excimer laser drilling technique by Corning Glass as a subcontractor under two via fill performers, who each filled one of the wafers. The first performer is Research Triangle Institute (RTI), providing conformal vias with a copper plating thickness of 10 µm. The second performer, Triton Microtech, providing entirely filled vias using a copper frit paste approach. As a result, there are 32 test coupons for various experimental objectives, with two coupons of each type for redundancy.

Table 3. Via Array Design of Experiments

Wafer	Segment	Array Type	Hole Size	Spacing Size	Fill Factor
Cu filled	1	Regular	50 um	100 um	19.6%
Cu filled	2	Regular	50 um	200 um	4.9%
Cu filled	3	Staggered	50 um	100 um	22.6%
Cu filled	4	Staggered	50 um	200 um	5.6%
Cu plated	1	Regular	50 um	100 um	10.5%
Cu plated	2	Regular	50 um	200 um	2.6%
Cu plated	3	Staggered	50 um	100 um	12.2%
Cu plated	4	Staggered	50 um	200 um	3.0%

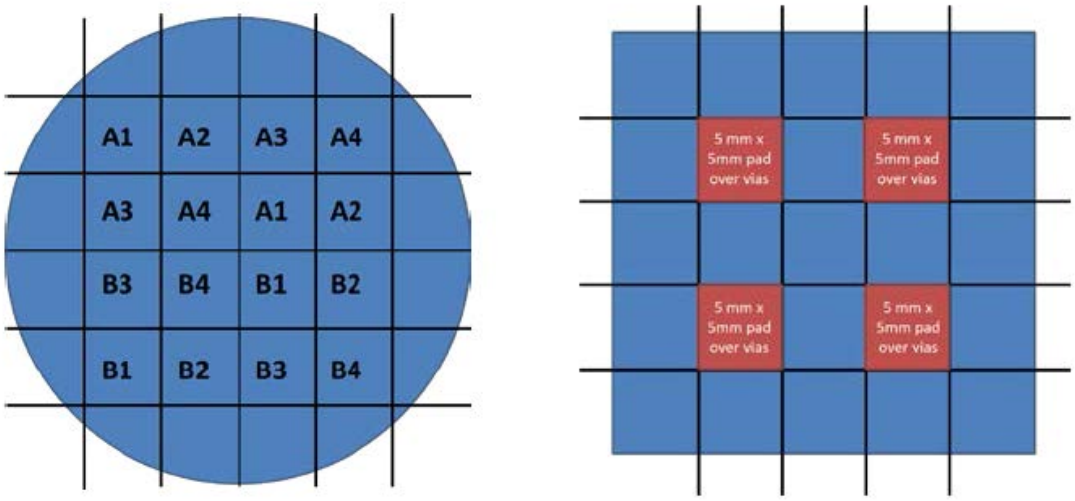

Figure 27: Glass Wafer Division into 16 Test Coupons
"A" coupons have uniform surface pads over arrays while "B" coupons have individually terminated vias. Right: Close-up view of a coupon and left: detailing the four identical via arrays.

4.1 Simulating a Heterogeneous System through Laser Spot Heating

As was shown in both the case study and the compact system model, in the heterogeneously integrated system considered in this work the CMOS power dissipation is negligible when compared to the dissipation of the power amplifier chiplets. As such, in order to simulate the system all that is needed is to introduce energy in the same amount over the same footprint as the amplifier chiplet, and observe the temperature rise across the interposer. The areas of the interposer that would be occupied by the CMOS can be either predefined – leading to a pass/fail assessment of the system's ability to control the CMOS temperature – or can be retrospectively defined as the interposer area with safe temperature levels.

Laser heating offers a very flexible method of delivering this energy into the interposer. The fiber laser available for the testing is straightforward to manipulate. It can produce a continuous wattage of 100 W, more than enough to simulate the 10 W amplifier. By focusing the laser spot to about 2.5 mm, the spot area is equivalent to the amplifier footprint. However, this illustrates one of the drawbacks of using the laser: the focused spot is round, and the flux distribution across the spot is Gaussian rather than uniform. This means that more of the heat dissipation occurs in the center of the spot, compared to an actual chiplet which will have a more uniform or edge-heavy distribution of flux entering the interposer. However, the ability to adjust and move the spot across multiple samples without contact outweighs this discrepancy in distribution.

Another advantage of the laser heat generation is its compatibility with IR thermography. The same high-emissivity coating that ensures good capture of the laser radiation is also used to obtain a high accuracy signal with the infrared camera. Coatings can range from carefully deposited ultra-black films to a simple graphite spray. The emissivity of the coating can be measured by the camera by using a coated reference sample at a known temperature. From initial testing with homogeneous reference samples, the graphite spray will likely be sufficient.

Presented in Figure 28 is the experimental setup that will be used to do the laser heating. The laser fiber is attached to a cradle with a focusing lens that focuses a spot on a stage-mounted cold plate. The spot size is calibrated by using a scanning razor method: a stage-mounted knife edge is placed between the laser and a power meter at the eventual location of the sample. By progressively blocking the laser spot, the spot diameter and a measure of the energy flux distribution can be obtained. A second calibration step is to correlate laser input current to output power. Lasing begins at an input current of about 7 amps, as determined by the power meter. For currents larger than 10 amps, the output power is linearly proportional to input current, as shown in Figure 29. With this information, the spot power can be adjusted "on-the-fly" during the course of sample testing.

As an initial test to demonstrate IR thermography, three homogeneous reference samples are heated with a 2.5 mm spot and imaged with a forward looking infrared (FLIR) Indigo IR camera. These samples include a pyrex, an alumina, and the best of three copper chiplets. However, prior to testing, these same samples were measured using a commercially available laser flash technique. The laser flash tester determines the thermal properties of the samples by monitoring the temperature decay of the sample after it has been subjected to a brief laser pulse. Table 4 contains the results of those laser flash tests, including the thermal conductivity. The copper sample with thickness 1.12 mm was selected – along with the pyrex and alumina – to be tested with the fiber laser.

With the conductivity of the samples measured, the IR imaging test could then proceed. Figure 30 shows the result of laser heating of the alumina and copper samples, respectively, at a laser output power of 1 W. The high-temperature laser spot can be seen in the center of each sample. On the image of the copper sample is an example of a pathline for data export. From the figure, two general trends can be seen: the less conductive alumina sample reaches a higher peak temperature while the temperature distribution across the surface of the copper is lower but more uniform.

This fact is corroborated by the temperature data collected by a pathline across the sample and through the hotspot. Figure 31 plots the temperature distribution across both the alumina and copper samples, bearing out the conclusions reached from inspection of the IR image. What is particularly interesting is that there are regions at the edge of the alumina sample that are cooler than the corresponding copper regions. This indicates that the suppression of thermal spreading in the alumina is sufficient to protect those regions from the dissipation occurring within the laser spot.

The relationship between peak temperature rise and laser power was also investigated in these two samples. As shown in Figure 32, the alumina peak temperature rises rather quickly, reaching 250 °C for an output power of 10 W. The copper sample is better able to conduct and spread the spot power, reaching a temperature of 100 °C at a power of 15 W.

So far the results of the spot heating on the pyrex sample have yet to be presented. Figure 33 plots the surface temperature distribution along the pyrex sample at a laser power of 1 W; the hotspot temperature of 235 °C immediately precluded further increases in spot power, as well as making capturing the entire surface temperature profile in one image difficult. The Indigo model

of camera used relies on non-uniform correction (NUC) software filters to properly measure object temperatures. Individual NUC settings are accurate for only limited temperature ranges, and because the pyrex sample provides such a high degree of isolation, the edges of the sample remain close to the cold plate temperature while the nearby hotspot reaches very high values. As such, the profile plotted in Figure 33 is a superposition of four different NUC settings. A more advanced model of FLIR camera – the Merlin – is able to correct for such wide disparities in temperature, which would remove the need to perform this superposition when using that camera.

The research proposed for this thrust involves applying this experimental setup to measurements on the via array samples. The laser spot will be focused on a region of the sample containing the array, mimicking the effect of the power amplifier. The resulting surface temperature distribution along the test coupon will represent the device temperatures at corresponding locations on the via-enhanced interposer modeled in the isolation case study. The effects of varying the via array parameters (through choice of one of the 32 coupons) on the temperature rise of the spot and nearby coupon areas will be assessed. The expectation is that the arrays with the highest fill factor will provide the lowest spot temperature, both through increased effective vertical conductivity and through a lower microspreading resistance. Given the conclusions of the full detail case study model in Figure 33, a 100 °C temperature rise above the coldplate within a 10 W, 2.5 mm diameter spot would be a satisfactory result for the highest fill factor via array.

It is anticipated that while all of the samples will provide better thermal isolation than the copper and alumina reference samples (leading to a smaller surface region above the CMOS cutoff temperature), the samples with the lowest fill factor, especially those relying on conformal vias, will have peak spot temperatures that exceed the maximum amplifier temperature. Tailored FEM simulations will be used to examine discrepancies between experiment and expectations, as well as estimate effective vertical and lateral conductivity within the array (by treating those values as fitting parameters within the models).

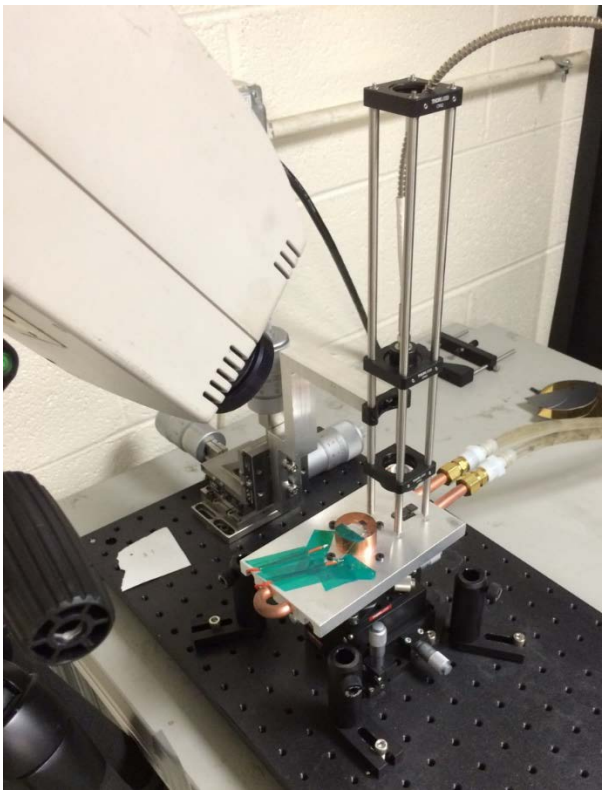

Figure 28: Experimental Setup
Including infrared camera, fiber laser, and water-cooled coldplate.

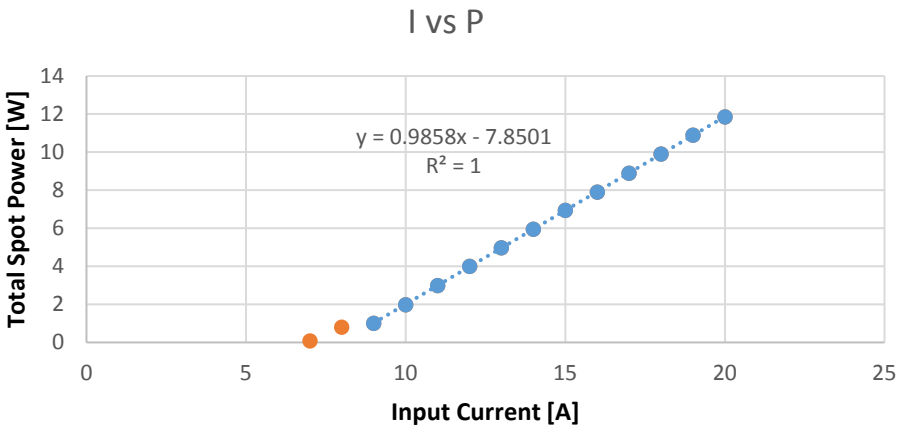

Figure 29: Laser Power Calibration Curve, Relating Spot Power to Input Current

Table 4. Laser Flash Measurement on Homogeneous Reference Samples

	Thick (mm)	Loss	Denisty (g/cm^3)	C_p (J/g-K)	α (cm^2/sec)	k (W/m-K)
Pyrex	1.003	0.065	2.20	0.750	0.00707	1.18
Copper	1.050	0.122	8.96	0.310	1.0679	296.20
Copper	1.120	0.387	8.96	0.277	1.39351	344.00
Copper	1.180	0.093	8.96	0.356	1.08741	344.60
Alumina	0.600	0.054	3.95	0.737	0.07887	22.96

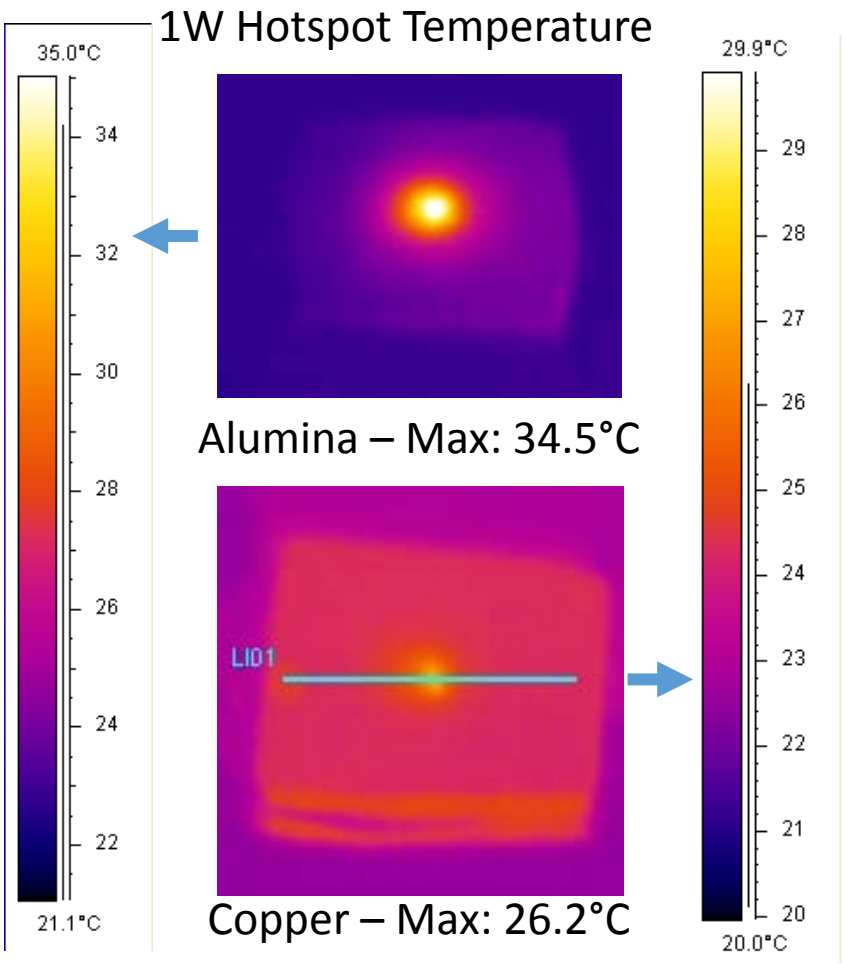

Figure 30: IR Images of Spot Heated Alumina (top) and Copper (bottom) Chiplets
On the copper image is an example of a pathline for data export and analysis.

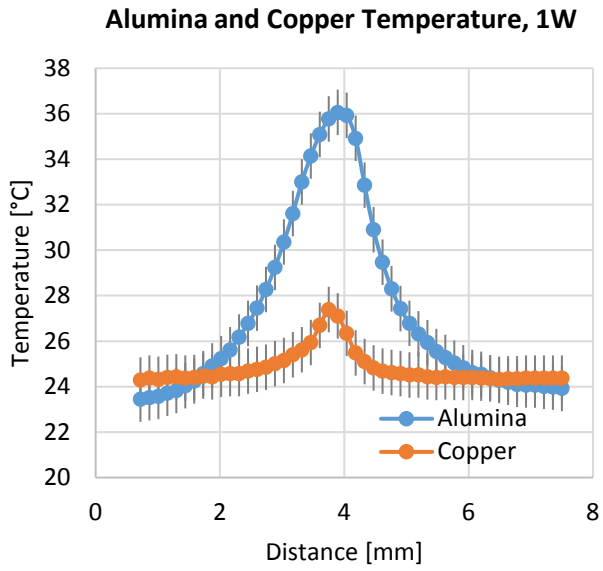

Figure 31: Reference Sample Surface Temperature Profiles through Midline from 1 W Laser Spot

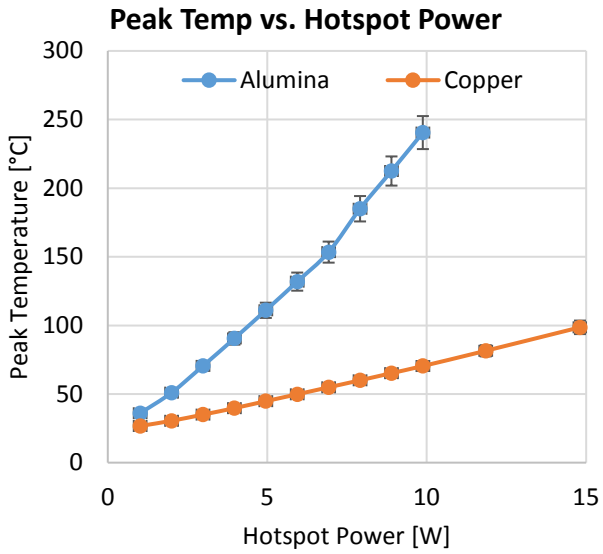

Figure 32: Peak hotspot Temperature as a Function of Laser Spot Power

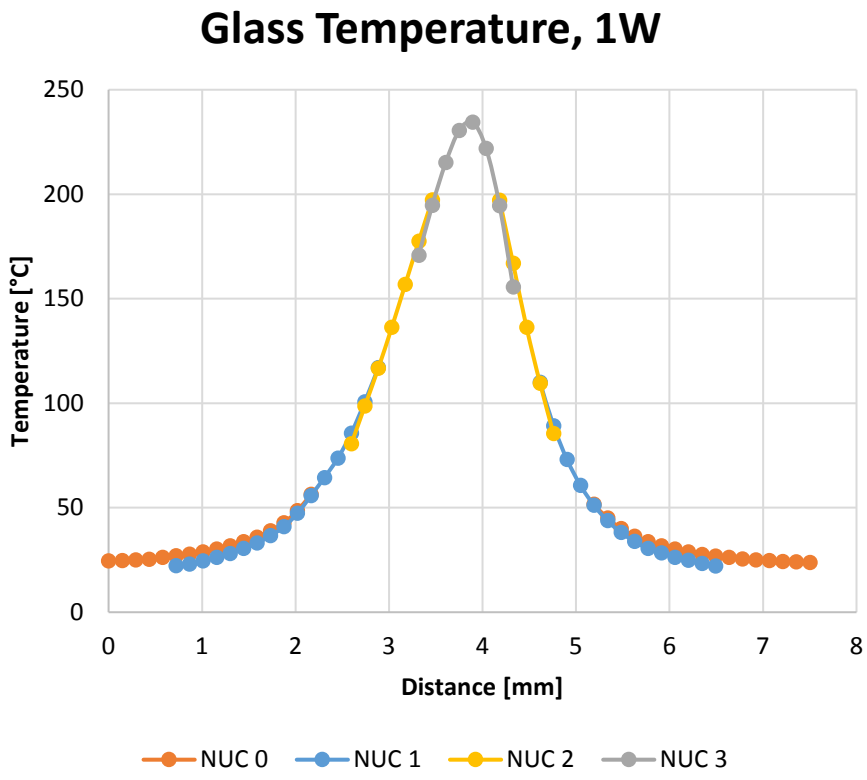

Figure 33: Glass Reference Sample Surface Temperature Profile Resulting from a 1 W Spot

Multiple correction filter setting are required to visualize and record temperature data.

4.2 Microgap Cooling of Thermal Via Arrays

As a final experimental objective, a single phase microgap cooler will be fabricated and applied to the most promising test samples. Such a cooler is straightforward to fabricate using standard machine shop capabilities, and will enable the thermally isolating interposer to be demonstrated in tandem with an embedded cooling approach. Of primary interest is the manner in which the flowing coolant interacts with the exposed via array, giving rise to convection driven microspreading. A series of modified FEM simulations will be created to accompany these microgap cooled via array experiments.

Because the cooler is intended to be reusable, it was determined that the most economical fabrication approach is to mill the cooler out of a small block of aluminum. This was chosen over photolithography and micromachining due to the need for several features at different depths: the o-ring seat, the inlet and outlet plenums, and the microgap itself. Each of these features would require its own mask and etch steps, and for a pair of microcoolers computer numerical control (CNC) machining offers a lower cost alternative. The challenge is the small size of the cooler module: since the target gap footprint is 5 mm x 10 mm, the cooler module itself is designed at 10 mm x 20 mm. In actually, due to the need for space for the inlet and outlet plenums, the gap footprint is 5 mm x 8 mm.

Aluminum is chosen for the cooler after consideration of its corrosion resistance and machinability. Other candidate materials are copper-based alloys and stainless steels. The primary feature of the cooler is the microgap surface, where surface finish and depth tolerance are much more important than in other features of the cooler. While metal edge-build up on the cutting tool could be an issue with the softer materials, the deep, narrow cut for the plenums would be more challenging in a hard material like stainless steel. Collaboration with technicians within the University of Maryland (UMD) Aerospace Machine Shop will help in identifying issues during the machining process.

The initial gap height of 200 μm was chosen based on the microgap modeling done earlier within this program. This gap will provide a good compromise between heat transfer rate and required pressure drop. It is also large enough to avoid surface tension-driven air bubble trapping identified in prior single-phase microgap experiments at UMD. The target nominal flowrate for this cooler is 5 mL/s, giving an average fluid velocity within the gap of 5 m/s. The anticipated pressure drop across the 8 mm long gap is 30 kPa, well below the imposed 50 kPa pressure limitation. Inlet/outlet temperatures and pressures will be monitored by in-line instrumentation, while flowrate will be determined from the rpm of a positive displacement gear pump.

Samples – whether silicon or glass-via interposers – will be installed on the cooler using two clamping brackets that will hold the sample against the o-ring seat. The brackets will be produced in a rapid prototyping polymer 3D printer to avoid additional machine shop time. With minor modifications the brackets could also be machined out of metal alongside the microgap manifold.

As the o-ring seal in the cooler must encompass the gap as well as both plenums, the outer dimensions of the sample must match that of the microgap manifold, 10 mm x 20 mm. This sample footprint size can be cleanly diced from the parent glass wafer such that it contains two

via arrays, as shown in Figure 34. The sample could also be taken from the edge of a coupon such that it contains only one via array which could be positioned at any location along the gap.

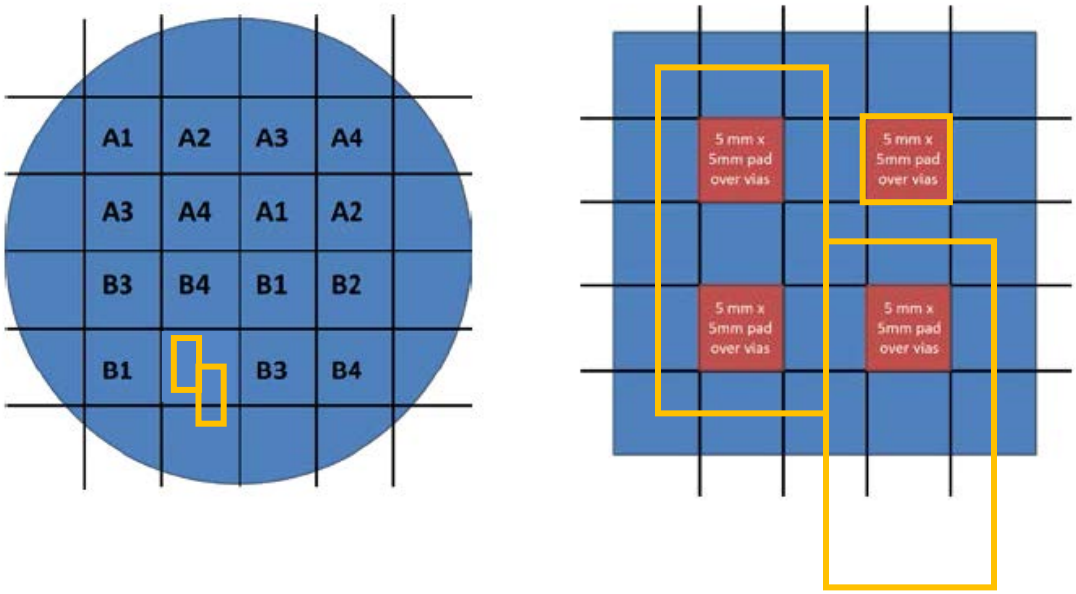

Figure 34: Sample Dicing Layout Compatible with Microgap Cooler Testing

When shifting to testing with the microgap cooler, flowrate vs pressure drop measurements will be made along with initial chip heater-driven heat transfer measurements. This will provide relations for the nominal heat transfer coefficient for this particular microgap design ahead of laser spot testing. Two additional rounds of laser spot heating will be performed on the samples used in the cold plate testing, using two cooler flowrates. One will be a high flowrate of 5 mL/s, the other will be a lower flowrate targeting a heat transfer coefficient of 3,000 W/m^2-K. If during testing additional flowrates may produce interesting operating points, those may be investigated as well.

5.0 CONCLUSION

The challenges of thermally isolating heterogeneously integrated components from one another was investigated. Due to the disparate thermal properties of the components, where some dissipate large amounts of power but withstand high operating temperatures while others are sensitive, low-power devices, thermal isolation of the devices can provide a means of managing the individual temperatures of each device type with a targeted, differential cooling approach. This differential cooler can be designed so that it requires less fluid pumping power than a cooler that must cool the entire electronic system to the safe operating temperature of the most sensitive devices. With the ability to specify the degree of isolation, important tradeoffs between device temperature rise and minimum device separation (and interconnect length) can then be made.

After examining several heterogeneous integration approaches, it was determined that a segregated chiplet approach offered the most promising avenue for thermal isolation efforts. Incorporating thermal via-enhanced glass interposers as the carrier for the heterogeneous chiplets provides necessary lateral thermal resistance to heat flow while providing a conductive path from the high-power components to underside cooling solutions. Substantial modeling efforts and an experimental survey of such via-enhanced glass interposers demonstrated the principles of isolation in these HI systems. Also explored is the integration of these interposers with single-phase embedded microfluidic cooling, an effort not yet represented in the literature.

This work introduces the concept of microspreading resistance as a component of the thermal behavior of arrays of conductive vias. It provides recommendations for mitigating microspreading when it is undesirable, and a formalism for incorporating it into existing equivalent thermal conductivity models of via arrays.

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LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ACRONYM	DESCRIPTION
ASTM	American Society for Testing and Materials
BEOL	back end of line
C4	controlled collapse chip connection
CMOS	complementary metal-oxide-semiconductor
CNC	computer numerical control
CTE	coefficient of thermal expansion
DAHI	Diverse Accessible Heterogeneous Integration
DARPA	Defense Advanced Research Projects Agency
FEA	finite element analysis
FEM	finite element method
FLIR	forward looking infrared
HBT	heterojunction bipolar transistor
HEMT	high electron mobility transistor
HI	heterogeneous integration
HIC	heterogeneous interconnect
IC	integrate circuit
IR	infrared
NGAS	Northrop Grumman Aerospace Systems
NUC	non-uniform correction
PCB	printed circuit board
PTH	plated through hole
RDL	redistribution layer
RTI	Research Triangle Institute
SOI	silicon-on-insulator
TSV	through-silicon via
TXV	through-layer via
UMD	University of Maryland