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Prediction and Measurement of Temperature Fields in Silicon-on-Insulator Electronic Circuits

Field-effect transistors (FETs) *in conventional electronic circuits are in contact with the high-thermal-conductivity substrate. In contrast, FETs in novel silicon-on-insulator* (SOI) *circuits are separated from the substrate by a thermally resistive silicon-dioxide layer. The layer improves the electrical performance of SOI circuits. But it impedes conduction cooling of transistors and interconnects, degrading circuit reliability. This work develops a technique for measuring the channel temperature of SOI FETs. Data agree well with the predictions of an analytical thermal model. The channel and interconnect temperatures depend strongly on the device and silicon-dioxide layer thicknesses and the channel–interconnect separation. This research facilitates the thermal design of SOI FETs to improve circuit figures of merit, e.g., the median time to failure* (MTF) *of FET–interconnect contacts.*

1 Introduction

The performance and reliability of electronic circuits are affected by temperature fields in transistors and interconnects. As transistor dimensions decrease, thermal conduction within a few micrometers of these heat sources governs an increasing fraction of the transistor-to-coolant temperature difference in an electronic system. This is very important in novel silicon-on-insulator (SOI) electronic circuits, where transistors are separated from the substrate by a thermally resistive silicon-dioxide layer, often fabricated by implanting oxygen ions into a single-crystal silicon wafer. Figure 1 is a cross section of a SOI field-effect transistor (FET), whose common dimensions are given in Table 1. Almost all of the device power is dissipated in the channel. The electrically insulating implanted layer prevents latchup between devices and reduces the parasitic capacitance of the transistor due to the substrate, facilitating faster circuits (Colinge, 1991). But the implanted silicon-dioxide layer has a low thermal conductivity, and impedes conduction cooling of the channel through the substrate. The SOI circuit designer must know the resulting temperature rise in interconnects and devices.

McDaid et al. (1989) showed that the temperature rise decreased the drain current of a SOI FET for given gate and drain voltages by assuming one-dimensional heat conduction through the implanted layer from an isothermal FET. Goodson and Flik (1992) predicted the temperature field in a SOI FET by treating the source, drain, gate, and interconnects as cooling fins for the Joule-heated channel. They showed that the temperature varies significantly within the FET, and indicated that the temperature rise could reduce the electromigration-limited reliability of interconnects. For application of SOI circuits below 77 K, e.g., in hybrid superconductor-semiconductor circuits, phonon-boundary scattering was shown to influence the temperature field strongly in FETs.

Experimental confirmation of the analysis of Goodson and Flik (1992) requires a technique for measuring temperature locally in transistors with spatial resolution comparable to the channel length, $2L_g$, which can be smaller than 0.5 μm. Lifka and Woerlee (1990) estimated the transistor-to-substrate thermal resistance for SOI circuits through the local melting of a coating, an approach that lacks the needed spatial resolution. Bunyan et al. (1992) used noise thermometry to measure temperatures in SOI transistors. This approach requires experimental structures very different from those in a circuit, yielding an impact on the temperature field that needs to be assessed. For non-SOI semiconductor devices, Brugger (1991) and Ostermeier et al. (1992) performed temperature measurements with submicrometer spatial resolution using micro-Raman spectroscopy. But the impact of the incident radiation on the performance of transistors is not known. The promising method of Majumdar et al. (1993) and Lai et al. (1993) uses an atomic force microscope to determine local temperature fields in circuits. Future research will almost certainly make this method effective for transistors with channel lengths much less than 1 μm.

This work develops a technique to measure the channel temperature of SOI FETs with a resolution in the direction of current flow of 0.32 μm, the FET channel length. The gate serves as an electrical-resistance thermometer for the channel temperature. This approach was used by Mautry and Trager (1990) for bulk (non-SOI) circuits, in which the characteristic length scale of the temperature field is much larger than FET dimensions. The gate is not isothermal in SOI circuits, in which the high thermal resistance of the implanted layer causes a large fraction of the channel-to-coolant temperature difference to occur within transistors. In the present work, thermal analysis yields the average channel temperature from the electrical resistance measured along the nonisothermal gate. Room-temperature data are compared with predictions of the analysis of Goodson and Flik (1992). Analysis estimates the impact of the channel–interconnect separation and the implanted-silicon-dioxide layer thicknesses on the reliability of FET–interconnect contacts.

This work helps to determine the effect of the implanted-layer thermal resistance on the practical potential of SOI technology. The experimental method developed here investigates thermal conduction processes within and very near transistors and interconnects. These conduction processes must be understood before transistor design based on thermal analysis, i.e., *device-level thermal design,* can accompany traditional electrical design of devices to yield circuits of optimal performance and reliability.

2 Thermal Analysis

SOI circuits are made of materials with very different thermal conductivities, shown in Table 2. Goodson and Flik (1992) used the difference in the conductivities to develop a simple thermal

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Contributed by the Heat Transfer Division and presented at the ASME/AIChE National Heat Transfer Conference, Atlanta, Georgia, August 8–11, 1993. Manuscript received by the Heat Transfer Division September 1993; revision received May 1994. Keywords: Conduction, Electronic Equipment, Measurement Techniques. Associate Technical Editor: R. Viskanta.

model for thermal conduction in SOI circuits. Section 2.1 reviews the analysis and Section 2.2 applies it to the experimental structure.

2.1 Steady-State SOI FET Thermal Model. The model of Goodson and Flik (1992) is for steady-state FET operation, which is the case in most measurements of FET electrical properties. The time required for steady state to be achieved is near $(d_o)^2/(k_o/C_o)$, where k_o/C_o is the thermal diffusivity of silicon dioxide, yielding about 200 ns at 300 K. The model is also useful for the case of steady-periodic power dissipation in clock-driven circuits at points separated from the channel heater by at least one thermal penetration depth. The thermal penetration depth in the silicon source and drain is approximately $(\tau k_d/C_d)^{1/2} = 0.4$ μm, where k_d/C_d is the thermal diffusivity of heavily doped silicon, and $\tau = 5$ ns is a typical clock period.

Heat flow from the tops of devices and interconnects is shown in Section 2.2 to be negligible. The channel was modeled as an isothermal heating source. This neglects the complex distribution of heating intensity in the channel, yielding a small error in the average channel temperature that is estimated at the end of Section 2.1. Variations in the temperature of the substrate–silicon dioxide interface are small compared to the channel-temperature rise. This interface was assumed to have the uniform temperature T_0.

The source, drain, gate, and interconnects were modeled by Goodson and Flik (1992) as one-dimensional cooling fins for the channel, arranged as shown in Fig. 2. The heat loss per unit fin length was assumed to be $h_f w_f (T_f - T_0)$, where T_f is the local fin temperature and w_f is the fin width in the direction normal to heat flow. The heat transfer coefficient is $h_f = \Psi k_o/d_{fo}$, where d_{fo} is the thickness and k_o/d_{fo} is the inverse volume resistance of the silicon-dioxide layer beneath. The dimensionless function Ψ was derived by Goodson and Flik (1992) to account for two-dimensional conduction in the silicon dioxide. The function depends

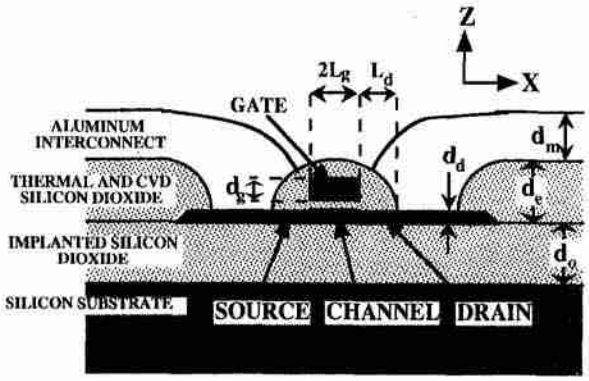


Fig. 1 Cross section of a silicon-on-insulator (SOI) field-effect transistor (FET)

Nomenclature

A = area, m^2
A_f = fin cross-sectional area, m^2
a = characteristic length of test structure, m
C = specific heat at constant volume per unit volume, $J\ m^{-3}\ K^{-1}$
c_p = specific heat at constant pressure per unit mass, $J\ kg^{-1}\ K^{-1}$
d = layer thickness, m
d_e = total thickness of thermally grown and CVD silicon dioxide, m
d_{go} = thickness of silicon-dioxide layer between gate and channel, m
d_o = thickness of implanted-silicon-dioxide layer, m
d_{fo} = thickness of silicon dioxide between fin and substrate, m
E_e = electromigration activation energy, J
$F_G(Y)$ = shape function for temperature distribution in gate
G = channel-to-air thermal conductance, $W\ K^{-1}$
g = acceleration due to gravity, $m\ s^{-2}$
h = heat transfer coefficient, $W\ m^{-2}\ K^{-1}$
I_D = drain current, A
I_G = gate current, A
J = current density, $A\ m^{-2}$
K_e = electromigration constant, s
k = thermal conductivity, $W\ m^{-1}\ K^{-1}$
k_B = Boltzmann constant = $1.38 \times 10^{-23}\ J\ K^{-1}$
k_c = channel thermal conductivity, $W\ m^{-1}\ K^{-1}$
k_o = thermal conductivity of silicon dioxide, $W\ m^{-1}\ K^{-1}$
k_s = thermal conductivity of lightly doped silicon, $W\ m^{-1}\ K^{-1}$
L_d = separation between gate and metal interconnect, m
L_g = half-length of gate in X direction, m
L_m = half-length of interconnect between devices in X direction, m
MTF = median time to failure, s
m = $(h/kd)^{1/2}$ = inverse thermal healing length of fin, m^{-1}
P = device power, W
P_{avg} = time-averaged device power, W
R_t = channel-to-substrate thermal resistance = $1/G$, $K\ W^{-1}$
R_G = electrical resistance of gate in Y direction, Ω
$R_G(T)$ = gate-electrical-resistance calibration function, Ω
T = temperature, K
T_c = average channel temperature, K
$T_G(Y)$ = gate temperature distribution, K
ΔT_G = average temperature rise in gate, K
$T_{m,max}$ = maximum interconnect temperature, K
T_0 = substrate temperature, K
V_G = voltage drop along gate, V
V_{GS} = gate-source voltage drop, V
V_{DS} = drain-source voltage drop, V
v = air velocity, $m\ s^{-1}$
w_f = fin width in X–Y plane, m
w_d = channel width in Y direction, m
w_c = separation between channel and gate contacts in Y direction, m
w_m = width of metal interconnect in Y direction, m
X = coordinate in plane of substrate, m
Y = coordinate in plane of substrate, m
Z = coordinate normal to plane of substrate, m
Z_1, Z_2, Z_3, Z_4 = constants, Eqs. (1)–(4)
β = coefficient of thermal expansion, K^{-1}
ϵ = emissivity
μ = viscosity, $kg\ m^{-1}\ s^{-1}$
ρ = mass density, $kg\ m^{-3}$
σ = Stefan–Boltzmann constant = 5.67×10^{-8} $W\ m^{-2}\ K^{-4}$
τ = clock period, s
Ψ = two-dimensional conduction function

Subscripts

d = property or dimension of source and drain
f = property or dimension of fin
g = property or dimension of gate
m = property or dimension of metal interconnect
o = property or dimension of silicon dioxide layer

Table 1 Common dimensions of SOI FET devices and those of the test structures used here

Dimensions	In FET (μm)	In Test Structure (μm)
implanted-SiO_2 thickness, d_o	0.4	0.293 - 0.503
additional-SiO_2 thickness, d_e	0.60	0.60
interconnect thickness, d_m	0.5	1
device thickness, d_d	0.08	0.041 - 0.177
gate thickness, d_g	0.30	0.29
gate-channel separation, d_{go}	0.0055	0.0055
channel-interconnect separation, L_d	0.5	0.8 - 3.8
gate half-width, L_g	0.25	0.16
device width, w_d	0.8	10
channel-gate contact separation, w_e	2	2

Table 2 Thermal conductivities of SOI circuit materials. These values are discussed in Section 2.2. The channel thermal conductivity was not used by Goodson and Flik (1992), but is needed in Section 3.2 for the analysis of the experimental data.

Region or Component	Material	Thermal conductivity at $T_0 = 303$ K (W m^{-1} K^{-1})
substrate	single-crystal silicon, 3 x 10^{15} boron atoms cm^{-3}	$k_s = 148^*$
channel	single-crystal silicon 6 x 10^{17} boron atoms cm^{-3}	$k_c = 148^*$
source and drain	single-crystal silicon, 1 x 10^{20} arsenic atoms cm^{-3}	$k_d = 63^*$
gate	polysilicon, 1 x 10^{20} arsenic atoms cm^{-3}	$k_g = 30^{**}$
interconnect	aluminum, 1 mass-percent silicon	$k_m = 239^*$
SOI implanted layer	silicon dioxide, implanted	$k_o = 1.40^{***}$
other insulating layers	silicon dioxide, thermally grown and CVD	$k_o = 1.40^{***}$

*Touloukian et al. (1970) **Tai et al. (1988) ***Sugawara (1969)

only on the ratio of the width of the fin and the thickness of the thermally resistive layer below the fin. The values of Ψ used here range between 1.016 and 1.028 for conduction from the source and drain, between 1.051 and 1.064 for conduction from the interconnects, and between 2.349 and 2.925 for conduction from the gate. The largest Biot numbers for the test structures in the present manuscript, $d_f h_f / k_f$, where k_f and d_f are the fin conductivity and thickness, are 0.028 for the source and drain fins, 0.029 for the gate fin, and 0.00782 for the interconnect fins. The fin thermal healing length is $1/m = (kA_f/hw_f)^{1/2}$, where k and A_f are the thermal conductivity and cross-sectional area of the fin. The distance from a heating source over which the fin temperature recovers to the substrate temperature is of the order of the healing length. The healing lengths are $1/m_m = (k_m d_m/h_m)^{1/2} \sim 7$ μm for the interconnects, $1/m_d = (k_d d_d/h_d)^{1/2} \sim 1$ μm for the source and drain, and $1/m_g = (k_g d_g/h_g)^{1/2} \sim 1.5$ μm for the gate.

The length in the X direction of the contact between the interconnect and the drain is approximately 3 μm. Because this length is substantially smaller than the healing length of the interconnect fins, Goodson and Flik (1992) neglected the different heat transfer coefficient between the interconnect and the substrate over this length. A single fin is used for the interconnect and the contact region with the heat transfer coefficient that prevails when the interconnect is above the thermal and CVD silicon-dioxide layers. This slightly overestimates the thermal resistance between the channel and substrate, but substantially simplifies the analysis.

The width of the interconnect, source, and drain fins in the Y direction, 10 μm, is larger than the healing length in these fins. This makes possible significant temperature variation in this direction, which is not considered by the present fin analysis. Temperature variation due to conduction from the sides of these fins is small because the thermal resistance for conduction by a unit area through one healing length in the fin, approximately $(d_m d_f)^{1/2}/(k_m k_f)^{1/2}$, is much smaller for each fin than the thermal resistance for conduction from a unit area of the fin side to the substrate, approximately d_m/k_m. But temperature variation in the Y direction due to conduction through the gate fin is significant. The error is estimated using an analytical solution to the three-dimensional thermal-conduction equation in the implanted silicon-dioxide layer and the channel, source, and drain. The difference between the conductivity of the channel and that of the source and drain is neglected and the source and drain fins are assumed to be very long in the X direction. Heat generation in the channel is modeled using a uniform heat-flux boundary condition at the top surface of the channel. Heat loss to the gate is modeled using a heat flux condition from the top of the channel near the edge, $w_d - d_d \le |Y| \le w_d$. The average channel temperature rise is slightly larger than those calculated by neglecting temperature variation in the Y direction in the channel, which is the approximation of the simple multifin analysis used in this manuscript. The relative error in the predictions given here is less than 3 percent for a channel width $w_d = 0.3$ μm and less than 7 percent for $w_d = 10$ μm.

The devices were assumed to be in an infinite linear array, each connected by an interconnect of length $2L_m$, and each dissipating the same power P. This idealization resulted in an estimate of the worst-case temperature distribution in a real circuit for a given value of the device separation, $2L_m$. It yielded the two planes of symmetry shown, which were adiabatic boundaries. The temperature and location in the interconnect are given by T_m and the parameter x_m, in the drain by T_d and x_d, and in the gate by T_g and x_g. The parameters x_m, x_d, and x_g are not related to the coordinates X, Y, and Z. The channel temperature is T_c. The gate is separated from the channel by a silicon-dioxide layer of thickness $d_{go} = 5.5$ nm, whose thermal resistance is negligible, yielding $T_g(x_g = 0) = T_c$. The fin equations were solved by requiring temperature continuity and energy conservation at the fin interfaces, yielding

$$T_m - T_0 = Z_1 \cosh [m_m(L_m - x_m)] \quad (1)$$

$$T_d - T_0 = Z_2 \exp[m_d x_d] + Z_3 \exp[-m_d x_d] \quad (2)$$

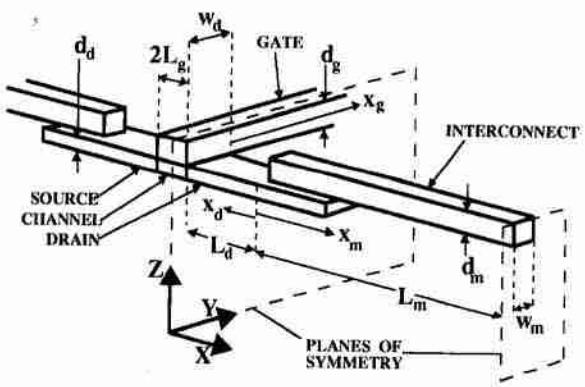


Fig. 2 Geometry of the thermal model of a SOI FET (Goodson and Flik, 1992)

$$T_s - T_0 = Z_4 \exp[-m_s x_s] \quad (3)$$

The variables Z_1, Z_2, Z_3, and Z_4 were determined by solving a set of four simultaneous algebraic equations, given in matrix form by Goodson and Flik (1992). The channel temperature is $T_c = T_s(x_s = 0) = Z_4 + T_0$. The maximum temperature in the interconnect, at the interconnect–device contact, is $T_{m,max} = T_m(x_m = 0) = Z_2 + Z_3 + T_0$. The channel-to-substrate thermal resistance is $R_c = Z_4/P$.

The isothermal-channel approximation does not account for the strong spatial dependence of the rate of heat generation in the channel (e.g., Ostermeier et al., 1992; Fushinobu and Majumdar, 1993). The greatest error occurs when the transistor is saturated, which results in heat generation predominantly near the channel–drain interface. An upper bound for the error is estimated using the fin method of Goodson and Flik (1992) and the assumption that all of the heat generation occurs within a region at the channel–drain interface of length in the X direction two orders of magnitude less than the channel length, $L_g/50$. Conduction to the gate and the difference between the channel thermal conductivity and that of the source and drain are neglected. This approximate analysis of the error yields a highly nonuniform channel temperature rise. But the *average* channel-temperature rise differs by less than 0.5 percent from that predicted by assuming an isothermal channel. The analysis of Goodson and Flik (1992) is therefore appropriate for predicting the average channel temperature rise, which is measured by the experimental technique developed here. In contrast, this analysis of the error shows that the isothermal-channel approximation results in a significant underprediction of the temperature rise of the drain–interconnect contact. For $L_{el} = 0.5$ and 1.5 μm, the relative errors are 13 and 11 percent, respectively.

The analysis neglects thermal boundary resistances. Goodson et al. (1994) measured the effective thermal conductivities for conduction normal to the implanted silicon-dioxide layers in the present study bounded below by silicon and above by aluminum. The data agree closely with the conductivity of bulk silicon dioxide, making a significant thermal boundary resistance between the implanted layer and the silicon dioxide unlikely. Data are needed for the boundary resistance between the buried silicon dioxide and the silicon device, as well as the resistances at the boundaries of the thermally grown silicon dioxide. Goodson et al. (1993) measured the effective conductivities for conduction normal to chemical-vapor-deposited layers fabricated using the same method as those in the present study. They obtained upper bounds for the thermal boundary resistance between the aluminum and the silicon dioxide that would not significantly change the values of h_f for the interconnects in the present work. The thermal resistances that impede conduction from the channel to the gate and from the source and drain to the interconnects are unknown. If significant, these resistances will cause the analysis here to underpredict the channel-to-substrate thermal resistance.

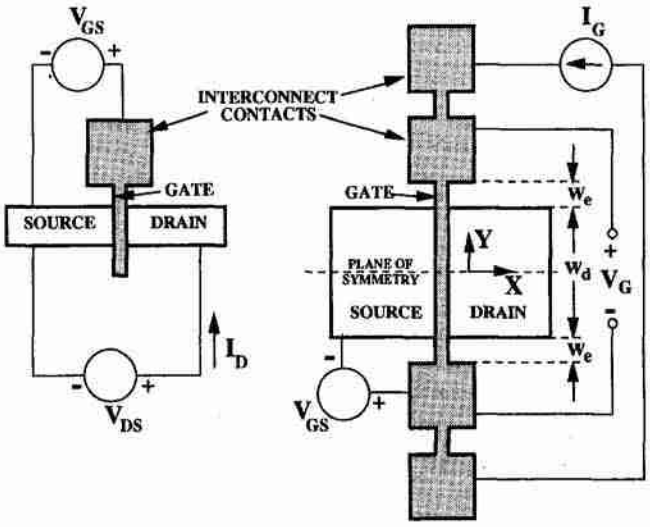
2.2 Application to the Experimental Test Structure

Thermal Conductivities. Table 2 gives the thermal conductivities used in the model. Goodson et al. (1994) measured the thermal conductivity of implanted-silicon-dioxide layers in SOI wafers near room temperature. The data agreed within the experimental error with the value recommended for bulk amorphous silicon dioxide (Sugawara, 1969), so the bulk value is used here. The bulk value is also used for thermally grown silicon dioxide, supported by the data of Goodson et al. (1993). The thermal conductivities reported for chemical-vapor-deposited (CVD) silicon-dioxide layers do not agree, but are in general less than the bulk value (Schafft et al., 1989; Brotzen et al., 1992; Goodson et al., 1993). Due to the lack of a consensus among the data for CVD silicon-dioxide layers, the bulk value is used in this case as well. The resulting error is very small because the thermal resistance of the implanted silicon-dioxide layer is much more important than that of the CVD layers.

The source and drain are single-crystal silicon doped with approximately 1×10^{20} arsenic atoms cm^{-3}. The most appropriate existing data are for bulk single-crystal silicon doped with 1.7×10^{20} phosphorus atoms cm^{-3} (Touloukian et al., 1970). There are no thermal conductivity data available for the gates in the present research, which were polysilicon heavily doped with arsenic atoms. Tai et al. (1988) and Völklein and Baltes (1992) measured thermal conductivities near 30 W m^{-1} K^{-1} in polysilicon layers heavily doped with phosphorus. The data are consistent with the thermal diffusivity data of Mastrangelo and Muller (1988), also for phosphorus-doped polysilicon layers. The conductivity $k_g = 30$ W m^{-1} K^{-1} is used here. The conductivity above 300 K of silicon with less than 10^{18} dopant-atoms cm^{-3} differs little from that of intrinsic silicon (Touloukian et al., 1970), which is used for k_c and k_s here. The thermal conductivity of aluminum layers containing 1 mass percent of silicon has not been measured directly. The thermal conductivity calculated using the Wiedemann-Franz law (Kittel, 1986) and the electrical resistivity measured here of these layers is within 4 percent of the thermal conductivity recommended for bulk aluminum (Touloukian et al., 1970), so the bulk value is used here.

The substrate temperature during the measurements was $T_0 = 303$ K, and the largest channel temperature was $T_c = 403$ K. The thermal model in Section 2.1 neglects the temperature dependence of the thermal conductivities of the SOI FET materials. This is a good approximation between 303 and 433 K for silicon dioxide and aluminum, whose bulk thermal conductivities vary by less than 13 and 2 percent in this range, respectively. But the thermal conductivity of the heavily doped silicon source and drain varies more significantly in this temperature range. To help overcome this difficulty, the temperature $(T_0 + T_c)/2$, averaged for all of the data, is used when interpolating k_d.

Dimensions. Figure 3 compares the experimental test structure with a FET device. The measured dimensions of the test structures are given in Table 1. The interconnect lengths are very long compared to $1/m_m$, so that $L_m = \infty$ is used. The gate of the FET in the test structure extends out from both sides of the channel to interconnect contacts in the Y direction. This results in a plane of symmetry normal to the Y axis, i.e., an X–Z plane, at $Y = 0$. The temperature field in each half of the test structure is predicted by the thermal model. The thermal analysis is applied using $w_d = (w_d)_{\text{test structure}}/2$, $w_m = (w_m)_{\text{test structure}}/2$, and $P = (P)_{\text{test structure}}/2$.



a) FET DEVICE. b) TEST STRUCTURE.

Fig. 3 Top views of: (a) FET device; (b) test structure

Parameter Uncertainties. An uncertainty in the predictions of the thermal analysis results from the use of parameters, e.g., thermal conductivities and dimensions, which may differ from those in the test structure. This uncertainty is estimated using the sum-of-squares technique (e.g., Holman, 1984) and the analytical model. The largest expected error is ±10 percent. The uncertainties in k_d and d_d are the largest contributors.

Heat Transfer to Ambient Air. The test structure is exposed to ambient air, but heat transfer to the air is neglected. This is justified by the small value of the channel-to-air thermal conductance compared to the channel-to-substrate thermal conductance, which is predicted in this work to be $1/R_c \sim 0.5 - 2 \times 10^{-4}$ W K^{-1}. The channel-to-air thermal conductance is of the order of that from an isothermal disk of radius a on the boundary of a semi-infinite medium of conductivity k, $G = 4ak$ (Carslaw and Jaeger, 1959). Using $a = w_d/2$ and the room-temperature conductivity of air yields $G = 5.2 \times 10^{-7}$ W K^{-1}. An order-of-magnitude analysis of the momentum equation estimates the air velocity near the device due to buoyancy forces (Rohsenow and Choi, 1961), $v = \rho g a^2 \beta (T_c - T_0)/\mu$, where g is the acceleration due to gravity, and ρ is the density, μ is the viscosity, and $\beta \sim 1/T_0$ is the approximate coefficient of thermal expansion of the air. Using room-temperature properties and $T_c - T_0 = 130$ K yields $v = 6.6$ μm s^{-1}. The thermal conductance contributed by the air motion is of the order of $G = v\pi a^2 \rho c_p = 6.2 \times 10^{-13}$ W K^{-1}, where c_p is the specific heat per unit mass at constant pressure of air. The thermal conductance due to radiation is of the order of $G = 4\epsilon\sigma T_0^3 A$, where ϵ is the emissivity of the surface, σ is the Stefan–Boltzmann constant, and A is the area of the emitting surface. Using $\epsilon = 1$ and $A = \pi a^2$ yields $G = 5.0 \times 10^{-10}$ W K^{-1} at room temperature.

3 Channel-Temperature Measurement Technique

This section describes the technique for measuring the channel temperature of SOI FETs. Section 3.1 describes the apparatus and the general procedure, and Section 3.2 calculates the channel temperature from the measured gate resistance. Section 3.3 determines the experimental uncertainty.

3.1 Apparatus and Procedure. Figure 3 shows the experimental structure. The electrical resistance of the gate depends strongly on temperature. It serves as an electrical-resistance thermometer. The calibration measures the gate electrical resistance, R_G, as a function of temperature when there is no drain current, i.e., when the gate is isothermal, yielding $[R_G(T)]_{\text{calibration}}$. The substrate temperature is controlled using a Temptronic Model TP38B chuck, a copper disk with a diameter of 88.9 mm and a thickness of 19.1 mm, to which the wafer is secured by suction. A thermocouple with one junction soldered to the chuck surface measures the chuck temperature. The chuck is maintained at the temperature T_0 and the gate resistance is measured for varying values of the drain-source voltage drop, V_{DS}, and the gate-source voltage drop, V_{GS}, i.e., for several different device powers, $P = I_D V_{DS}$.

The *average gate temperature* is defined as that of the gate segment whose resistance is measured, i.e., the segment between the voltage contacts. The average channel temperature is T_c, which is shown in Section 3.2 to be very well approximated by the average temperature of the gate segment over the channel. The average gate temperature considers the gate segments not over the channel heater, and is less than T_c. The FET gate-temperature variation is more important in a SOI wafer, where most of the temperature drop occurs within a few micrometers of the channel due to the implanted layer, than in a normal substrate, where the temperature-drop length scale is the thickness of the substrate, i.e., a few hundred micrometers. This temperature variation must be considered when calculating T_c from R_G.

3.2 Temperature Distribution in the Gate. The gate temperature variation in the Y direction is

$$T_G(Y) = T_0 + \Delta T_G F_G(Y) \tag{4}$$

where ΔT_G is the average gate-temperature rise from T_0 and $F_G(Y)$ is a shape function of average value unity that is defined for $|Y| < w_c + w_d/2$. For each measured R_G, ΔT_G is determined iteratively using

$$R_G = \int_{-w_c - w_d/2}^{w_c + w_d/2} [R_G(T_0 + \Delta T_G F_G(Y))]_{\text{calibration}} \frac{dY}{2w_c + w_d} \tag{5}$$

The thermal resistance of the silicon-dioxide layer between the channel and gate, $d_{ox}/(2L_g w_d k_{ox}) = 1.2 \times 10^3$ K W^{-1}, is small compared to the thermal resistance for conduction along the gate to the contact in the Y direction, $w_c/(2L_g d_g k_g) = 7.31 \times 10^5$ K W^{-1}. This means that the channel- and gate-temperature distributions are almost identical for $|Y| < w_d/2$. The average channel temperature is

$$T_c = T_0 + \int_{-w_d/2}^{w_d/2} \Delta T_G F_G(Y) \frac{dY}{w_d} \tag{6}$$

The channel-to-substrate thermal resistance is $R_c = (T_c - T_0)/P = (T_c - T_0)/(I_D V_{DS})$.

Two shape functions are now developed, from which Eqs. (5) and (6) yield upper and lower bounds for T_c for a given R_G. Each shape function must be even, due to the test-structure symmetry about $Y = 0$, and continuous. Because of the large width in the X direction of the gate-interconnect contacts, 4 μm, compared to the gate width, $2L_g = 0.32$ μm, the contacts are very nearly isothermal at the substrate temperature, T_0. This yields the boundary conditions $F_G(Y) = 0$ at $Y = \pm(w_c + w_d/2)$. For a given R_G, T_c calculated using Eqs. (5) and (6) increases with the difference between unity and the average of $F_G(Y)$ over $-w_d/2 < Y < w_d/2$, i.e., with the assumed difference between the average gate and channel temperatures. Shape LB assumes a linear temperature profile in the gate segments not over the channel, which neglects conduction down through the buried silicon-dioxide layer, and an isothermal channel. Both assumptions underestimate the difference between the average channel and average gate temperatures, yielding a lower bound for T_c. Shape LB is

$$F_G(Y) = \frac{w_d + 2w_c}{w_d + w_c}, \quad |Y| < \frac{w_d}{2} \tag{7}$$

$$F_G(Y) = \left[\frac{w_d + 2w_c}{w_d + w_c}\right] \frac{[(w_c + w_d/2) - |Y|]}{w_c}, \quad \frac{w_d}{2} < |Y| < w_c + \frac{w_d}{2} \tag{8}$$

An overestimate of the difference between the average gate and channel temperatures requires an overestimate of the temperature drop between the center and the edge of the channel in the Y direction. This is calculated by isolating the channel and gate from the source and drain, in which thermal conduction reduces the channel-temperature variation in the Y direction. The gate and channel are grouped together as a composite fin, which meets a fin of different internal properties and heat transfer coefficient at $Y = w_d/2$. Solving the heat equation in the two fins yields shape UB, which has a larger average in the channel region than shape LB. Values of $T_c - T_0$ calculated using shapes UB and LB differ by less than 8 percent, and the simpler shape LB is used here, Eqs. (7) and (8). This function does not describe the temperature distribution in the channel. Rather, it is a shape function which, when used in Eqs. (5) and (6), yields a value for T_c close to the *average* channel temperature. The difference between the upper and lower bounds is used in the experimental-uncertainty analysis.

3.3 Experimental Uncertainty. The uncertainty in $R_c = (T_c - T_0)/P$ has three significant, independent components: (*a*) There is a relative uncertainty of 4 percent in

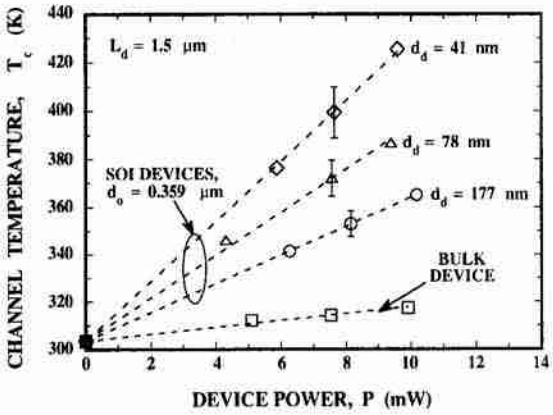


Fig. 4 Channel-temperature data for SOI FETs with varying device thicknesses, compared with data for a bulk (non-SOI) FET

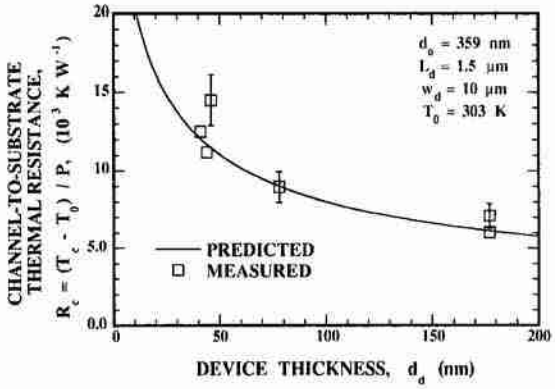


Fig. 5 The channel-to-substrate thermal resistance, R_c, as a function of the device thickness

$T_c - T_0$ due to the error in the substrate-temperature change measured by the chuck thermocouple (Goodson et al., 1994). (*b*) A relative uncertainty of 6.6 percent in $T_c - T_0$ is due to the measurement of R_G. (*c*) A relative uncertainty of 8 percent in $T_c - T_0$ is due to the approximate shape function for the temperature profile in the gate, as shown in Section 3.2. The total relative uncertainty in R_c is ±11 percent, determined using the sum-of-squares technique (Holman, 1984).

4 Results and Discussion

Section 4.1 compares data for the channel-to-substrate thermal resistance of SOI FETs with predictions of the thermal analysis of Section 2. The thermal analysis is used in Section 4.2 to estimate the influence of the implanted silicon-dioxide layer on the reliability of highly integrated SOI circuits.

4.1 Channel-to-Substrate Thermal Resistance. Channel-temperature measurements are performed on SOI test structures with varying values of L_d, d_d, and d_o. Test structures fabricated from bulk (non-SOI) wafers are measured for comparison. The device voltages satisfy $0\ \text{V} < V_{DS} < 3\ \text{V}$ and $V_{GS} = 2$ V and 2.5 V, which are typical operating conditions. The device powers vary between 3 and 14 mW, and the values of $T_c - T_0$ vary between 5 and 130 K. The power dissipated in the gate electrical-resistance thermometer is at least two orders of magnitude smaller than the device power.

The channel-to-substrate thermal resistance, R_c, varies by less than the experimental uncertainty for varying powers from a single device, as shown in Fig. 4 for three SOI devices and one bulk device, i.e., a device fabricated in a conventional wafer, which lacks the implanted silicon-dioxide layer in SOI wafers. The data for each device for varying powers fall near a line originating at $P = 0$ and $T_0 = 303$ K, whose slope is R_c. Values of R_c for the SOI devices are as much as 10 times larger than R_c for the bulk device, due to the thermal resistance of the implanted silicon-dioxide layer. The value of R_c decreases with increasing SOI device thickness, d_d. In Figs. 5 and 6, each data point is the average of the values of R_c measured in a single test structure. Uncertainty bars are only given for selected data to avoid cluttering of the figures. Each data point is the average of the values of R_c measured in a single test structure. Uncertainty bars are only given for selected data to avoid cluttering of the figures.

Figure 5 shows that the sensitivity of R_c to the device thickness is predicted by the thermal model of Section 2. Increasing d_d reduces the channel temperature for a given power. The parameters k_d and d_d are not independent, but always appear as a product in the solution for the temperature distribution (Goodson and Flik, 1992). Thus, the channel temperature is also sensitive to k_d, which depends on the doping level in the source and drain. The agreement is excellent considering the uncertainties of the thermal conductivities and dimensions used in the analysis. Section 2.2 estimated that the potential relative error in the predictions due to these uncertainties is ±10 percent. The differences in the experimental data at device thicknesses near 45 μm in Fig. 5 do not indicate a poor repeatability of the experimental method. Each data point is for a different experimental structure. Because R_c depends sensitively on the structure dimensions, the uncertainty in the measurement of structure dimensions can yield data on a single graph that are apparently inconsistent when only the uncertainty in the measurement of R_c is considered.

Figure 6 shows the dependence of R_c on the implanted-silicon-dioxide layer thickness. The data support the predictions of the model, and indicate that R_c is as sensitive to d_d as it is to d_o. This is in contrast to the predictions of McDaid et al. (1989), whose model assumed that R_c is independent of d_d. By modeling one-dimensional conduction in the implanted-silicon-dioxide layer, these researchers predicted that $R_c = d_o/(Ak_o)$, where A is the device area in the X-Y plane. This neglects the spreading of the temperature profile into the source and drain fins with increasing d_o, and is not consistent with the data. This can be remedied by a simple scaling analysis. The area in the source and drain with significant temperature rise is of the order of $A = 2w_d/m_d$, where the thermal healing length $1/m_d$ is approximately $(k_d d_d d_o/k_o)^{1/2}$. Using $R_c = d_o/(Ak_o)$ with this expression for A yields

$$R_c \approx \frac{1}{2w_d}\left(\frac{d_o}{k_o k_d d_d}\right)^{1/2} \tag{9}$$

which is in qualitative agreement with the data in Fig. 6. This shows that R_c is roughly proportional to $d_o^{1/2}$, and that the sensitivity of R_c to d_o and d_d is similar, i.e., halving d_o and doubling

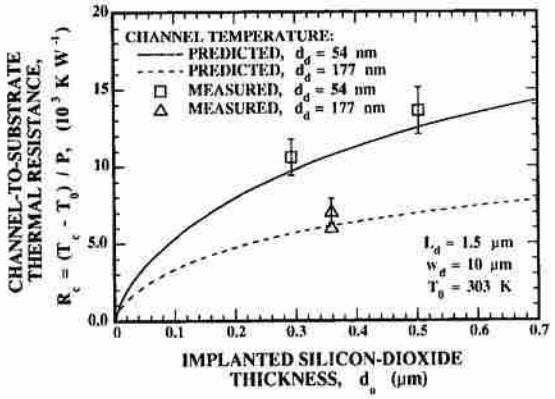


Fig. 6 The channel-to-substrate thermal resistance as a function of the implanted silicon-dioxide layer thickness

d_{ii} have the same impact, if all other parameters are held constant. Equation (9) is valid only when the thermal healing length in the source and drain is smaller than the channel–interconnect separation, i.e., $1/m_{ii} < L_{ii}$. Otherwise, there is significant heat conduction into the interconnects, which are more effective fins than the source and drain because of their large thickness and high thermal conductivities.

4.2 Electromigration-Limited Reliability of FET-Interconnect Contacts. The FET-interconnect contact temperature *increases* as L_{ii} is reduced, because this brings the contact nearer to the channel heat source. This reduces the reliability of the contact, whose electromigration-limited mean time to failure (MTF) decreases with increasing temperature. This section estimates the reduction of the MTF of FET–interconnect contacts due to the implanted layer in SOI circuits and demonstrates the potential for overcoming this problem through transistor-level thermal design. Electromigration is the motion of metal atoms in the interconnect in the direction of electron flow due to electron-lattice momentum transfer. This causes interconnect failure due to void formation, particularly near FET–interconnect contacts, where the flux of metal atoms diverges. The temperature dependence of the MTF limited by electromigration is (e.g., Black, 1967)

$$\mathrm{MTF} = K_e \exp\left(\frac{E_e}{k_B T}\right) \tag{10}$$

where E_e is the activation energy for atomic diffusion, $k_B = 1.38 \times 10^{-23}$ J K^{-1} is the Boltzmann constant, T is the temperature, and K_e is a function of the electrical current density, the geometry, and the microstructure and purity of the metal. Equation (10) agrees well with data for FET-interconnect contacts if $E_e = 0.5$ eV $= 8 \times 10^{-20}$ J is used (Chern et al., 1986).

The FET device dimensions in Table 1 are used with an interconnect length between devices of $2L_m = 4$ μm. The FETs experience steady-periodic heating with pulses of 1.61 W for one tenth of each clock cycle, where 1.61 W is the steady-state power of a SOI device with these dimensions (Woerlee et al., 1989). The analysis in Section 2 provides a good estimate of the nearly steady-state FET-interconnect contact temperature if the time-averaged power is used, $P_{\mathrm{avg}} = 0.161$ W. The resulting contact temperature rise is less than 8 K, and depends strongly on d_{ii} and L_{ii}. Figure 7 uses Eq. (10) to show the ratio of the MTF for FET–interconnect contacts in a SOI circuit to that for contacts in a bulk circuit. These predictions assume that the substrate temperature in the SOI case is equal to that in the bulk case. The difference between the two contact temperatures is due to the thermal resistance of the implanted silicon-dioxide layer. The MTF increases as L_{ii} is increased, because the interconnect moves away from the channel heater. It may be possible to improve circuit reliability by increasing L_{ii}, but this must be weighed against the need for compact devices. Reducing d_{ii} also increases the MTF, because this reduces the contact temperature.

Figure 7 provides the type of information needed to make decisions effectively during the design of SOI circuits, but the predictions are very approximate. Because Eq. (10) has only been experimentally verified using accelerated testing, i.e., the use of electrical current densities and temperatures which are higher than those found in an operating circuit, Fig. 7 can at best show the expected trends. In a real device, the rate of heat generation will be greatest near the drain contact, causing this contact to have the lowest MTF. But the isothermal-channel approximation of Goodson and Flik (1992) yields identical temperatures in the source and drain contacts. As discussed in Section 2.1, this underpredicts the temperature rise of the drain contact by as much as 13 percent. The resulting error in the normalized MTF in Fig. 7 is less than 10 percent.

5 Conclusions

The analysis of Goodson and Flik (1992) tends to underpredict the data presented here. This is due in part to the assumption of an isothermal channel, which results in about a 7 percent underprediction of the channel-to-substrate thermal resistance, as discussed in Section 2.1. The underprediction may be due in part to thermal boundary resistances in the structure, which, as discussed in Section 2.1, are not considered by the analysis. Another important possibility is that the thermal conductivities of the interconnects and source and drain, which have not been measured, may be less than the bulk values used here. Better agreement will require more research on thermal conductivities and boundary resistances in circuits.

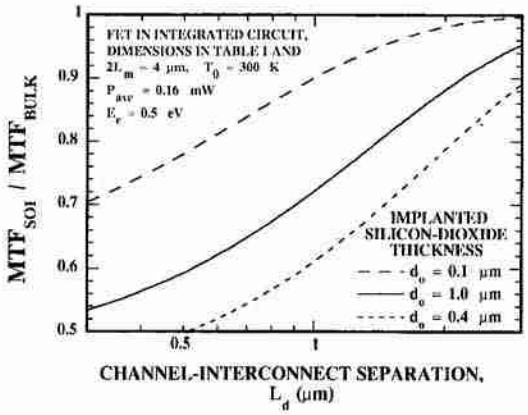


Fig. 7 Predicted dependence of the median time to failure (MTF) of FET–interconnect contacts on the channel–interconnect separation

The mean time to failure of a circuit and the channel mobility are important to the design of circuits. They are affected by the channel and interconnect temperatures, which are shown here to depend strongly on design parameters, e.g., k_{ii}, d_{ii}, d_{oi}, and L_{ii}. Some of these parameters also affect the electrical performance of the device directly. In order to achieve circuits of optimal performance and reliability, design for electrical performance should be accompanied by device thermal design, i.e., the choice of dimensions, materials, and processing techniques that enhance heat conduction within a few micrometers of the device. This work provides a basis for the thermal design of SOI FETs.

This work shows that the steady-state channel-temperature rise in SOI FETs due to Joule heating is significant. Electrical-property measurements performed on devices in the steady state are affected by this temperature rise due to the strong dependence of the channel mobility on temperature. The steady-state data may not be applicable to devices in an integrated circuit, where the channel-heating is time dependent. More work is needed to determine time-dependent temperature fields in integrated SOI circuits.

Acknowledgments

Professors Carl V. Thompson and Borivoje B. Mikic of M.I.T. provided valuable comments. K.E.G. and L.T.S. were supported by academic fellowships from the Office of Naval Research and AT&T Bell Labs, respectively. The SOI wafers used in this study were provided by IBIS Corp., Danvers, Massachusetts. D.A.A. and L.T.S. acknowledge the support of the Semiconductor Research Corporation (SRC) under contract No. 92-SP-309.

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