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MICROWAVE GENERATION FROM AVALANCHE TRANSIT TIME DIODES

FOURTH QUARTERLY REPORT

by

W. K. Niblack

NOVEMBER 1968

ECOM

UNITED STATES ARMY ELECTRONICS COMMAND • FORT MONMOUTH, N.J.

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SYLVANIA
SYLVANIA ELECTRIC PRODUCTS INC.
Subsidiary of GENERAL TELEPHONE & ELECTRONICS
SEMICONDUCTOR DIVISION
100 Sylvan Road • Woburn, Mass. 01801

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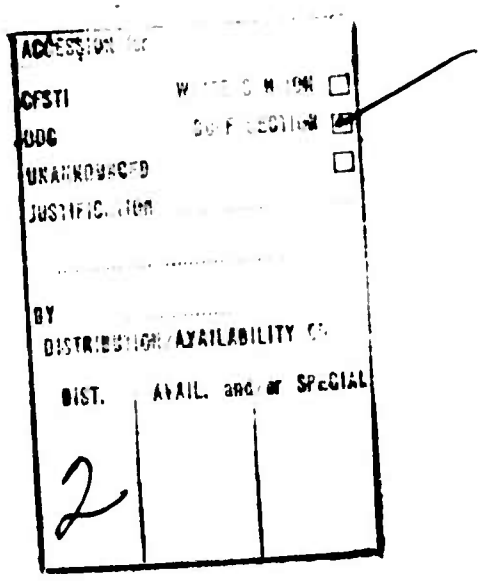

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TECHNICAL REPORT ECOM-0671-4

November, 1968

MICROWAVE GENERATION FROM AVALANCHE TRANSIT TIME DIODES

FOURTH QUARTERLY REPORT

1 APRIL 1968 TO 30 JUNE 1968

Report No. 4

CONTRACT NO. DAAB-07-67-C-0671

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DA PROJECT NO. 7910.21.243.38

Prepared by

W. K. Niblack

Sylvania Electric Products, Inc.
SEMICONDUCTOR DIVISION
Woburn, Massachusetts

The work prepared under this contract is part of PROJECT DEFENDER and was made possible by the support of the Advanced Research Projects Agency under Order Number 692, through the U. S. Army Electronics Command

for

U. S. ARMY ELECTRONICS COMMAND, FORT MONMOUTH, NEW JERSEY

Abstract

Work during the fourth quarter was devoted to optimization of device processing, geometry, development of a passivated-mesa process, identification of remaining material and related problems and evaluation of inverted chips as pulsed and CW oscillators. A process was perfected for inverted mounting which consistently resulted in very low thermal resistance on copper, and diamonds were successfully metalized and mounted which will allow a further reduction of thermal resistance in the next quarter. Effort has been aimed at fabricating passivated and unpassivated diodes capable of inverted mounting which will produce CW power in the half-watt range at X-band. In addition, extensive studies of the noise properties of avalanche diodes has resulted in circuit refinements which reduce the AM noise by as much as 15 db in the frequency range of 10 kHz to 100 MHz off carrier, resulting in sideband-noise-to-carrier ratios better than -120 db/kHz (for Q_L = 80 and 20 mW output).

FOREWORD

This program is a research and development effort designed to investigate avalanche transit time-generated oscillations in semiconductor devices, with the objective being the design and construction of avalanche transit time oscillators capable of delivery of at least 10 watts CW output power. The work prepared under this contract is a part of PROJECT DEFENDER and was made possible by the support of the Advanced Research Projects Agency under Order Number 692, through the U.S. Army Electronics Command.

This report was prepared by Walter K. Niblack, Head of the Advanced Microwave Device Development Section of Sylvania's Semiconductor Division with the assistance of A. H. Solomon, E. Scherer, and C. A. Levi of the Microwave Department.

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I INTRODUCTION AND SUMMARY

This program is a research and development effort to investigate avalanche transit time-generated oscillations in semiconductor junctions. Objectives include the investigation of semiconductor materials and junction techniques leading to the design and construction of avalanche transit time oscillators capable of delivering at least ten watts of CW output power. In addition, a pulsed device capable of at least 100 watts peak power output will also be developed. The approach to device development for high power will include the design of multi-junction diodes on a common high-thermal-conductivity substrate. Power combining techniques for paralleling many oscillators and/or amplifiers will also be investigated, with an ultimate objective of producing power outputs at a kilowatt level. Emphasis will also be placed on tunability, gain, bandwidth, efficiency, noise characteristics, reliability, stability, uniformity, reproducibility and cost.

I. 1 Program Goals

The overall goals of this program are:

1. Develop avalanche transit time diode oscillators capable of at least 10 watts CW power and 100 watts peak pulse power in the 1 - 12 GHz frequency range, with emphasis on C-band. No forced air or other external cooling means is to be employed.

2. Develop techniques for combining the outputs of many such oscillators to achieve higher output.

I. 2 Results Obtained During the Fourth Quarter

The work during this quarter has centered on attempts to discover the reason for our poor yield of high power diodes, and for the low burn-out encountered in many lots in the last quarter. Investigations of every step in the process were launched, and many difficulties, previously overlooked, were identified, starting with the basic epitaxial material, and on through the techniques of junction formation, mesa etching, metallization and bonding, as well as design of material specifications to achieve the desired parameters such as avalanche frequency.

Device testing has involved a large amount of simple evaluation of power output, noise, and burnout on many lots of material from various vendors, and using various processes. The results helped to identify problem areas. It was found that a low avalanche frequency is required for low noise-high power results.

Work on high power amplifiers has given us outstanding results. When

low-power low noise devices are used as sources, followed by avalanche diode amplifiers, low noise output results, even from diodes that are noisy as power oscillators. This suggests that an optimum source could consist of one diode optimized as low noise, low power oscillator, driving an avalanche diode power amplifier.

II JUNCTION DESIGN AND MATERIAL TECHNOLOGY

II. 1 Junction Design Improvements

It has been found that for stable, quiet operation it is helpful for the avalanche frequency to be less than half the operating frequency. In order to assure this, the resistivity of the starting material for this X-band Diode has been raised to 1.2 - 1.5 Ω cm. Diodes made from this material have given 200 mw (not inverted, thermally limited) with 5% efficiency and low noise.

II. 2 Epitaxial Junction Diodes

Epitaxial junction material was received from an outside vendor and evaluated. Although the resistivity of the N layer was low, (.5 Ωcm) low power oscillations were obtained in X-band.

An attempt to raise the resistivity by means of gold compensation is being evaluated. Material with a 1.5 Ωcm N layer is on order and is expected by early August.

II. 3 Material Studies

During this period, the study of factors leading to low efficiency and premature burnout has continued. These studies include the areas of materials, processes and diode design.

Both in-house grown silicon and silicon purchased from outside vendors has been investigated.

The results obtained in-house have shown a great reduction in stacking fault density is observed both by etching and by interference-contract microscopy. The number of stacking faults has been reduced to an insignificant level ($< 10/cm^2$). However, a concentration of imperfections not identified with a specific structure but manifested by a fine, stippled appearance at magnifications greater than 100X continues to be a variable. This has not yet been correlated with low burnout because of the complicating factor of diffusion induced dislocations.

In material obtained from outside vendors, a comparable situation exists. Low stacking fault density is observed, with the fine structures, less defect density being a variable in different lots. In the evaluation of diodes to be reported here, it should be noted that the best results were obtained on a lot which showed a low density of those defects.

II.4 Process Studies

Since it was necessary to process a large number of runs to evaluate both material and process variables, no attempt was made to go through the entire process of producing passivated flip-chips. Rather, samples were packaged and evaluated at the earliest stage of 'processing'. Diodes fabricated were thermally limited. In all, 35 groups were processed.

The variable under study was the predeposition cycle. It has been observed that material with initial good structure develops a high concentration of defects during junction formation.

Diodes exhibiting these defects also exhibit burn-out at low currents. The defects observed are attributed to strain induced in the latice by the high concentration of Boron introduced in predeposition.

The diffusion used in diode fabrication is Gaussian. Therefore, the highest boron concentration will occur during pre-deposition. A series of experiments involving changes in time and temperature of prelays has been undertaken. Only the group device at 950°C has been fully evaluated. Groups diffused at 925°C and 900°C are in process.

Predeposition done in a single 20 minute cycle was taken as the standard process. This was found to produce a significant amount of damage. It was found that if the predeposition were done in two stages, with the oxide removed in between, damage produced in the first stage was removed, in the second. Damage does not seem to reappear during drive-in if the glass is then removed following the second state of pre-deposition.

Experimental cycles and their results are summarized in Table I.

III DISCUSSION OF PROCESSING

III.1 Measurements and Process Control

During this quarter, a total of 159 slices were processed. These slices were from the following sources:

TABLE I

TABLE OF TYPICAL PROCESS DATA

SLICE #	3PP	Ris	Epi	Slice Thick	Temp Dep	Time Dep	4PP	Temp Re-Dep	Time Re-Dep
57984-16A1	90V	1.3-1.7	8.5μ	5 mil	950°C	10 min.	14.5	950°C	20 min
57985-15B2	"	"	"	"	"	20 min.	10.5	"	10 min
57984-16B2	"	"	"	"	"	20 min.	10.5	"	20 min
57984-15A2	"	"	"	"	"	10 min.	14.5	"	20 min
57984-16A2	"	"	"	"	"	10 min.	14.5	"	10 min
57984-13-1	82V	"	9 μ	"	"	20 min.	11.0	-	-
57984-15A1	90V	"	8.5μ	"	"	10 min.	14.5	950°C	10 min
57984-15B1	90V	"	"	"	"	20 min.	10.5	"	20 min
539-36	65V	-	11.1μ	7.4 mil	"	20 min.	10.0	-	-
523-34	52V	-	10.8μ	7.7 mil	"	"	11.0	-	-
64437-14	-	-	-	-	-	-	-	-	-
499-65	63V	-	10.9μ	7.5 mil	950°C	"	14.0	950°C	10 min
523-32	52V	-	10.8μ	7.5 mil	"	"	11.0	-	-
514-36	70V	-	10.4μ	7.6 mil	"	"	12.0	-	-
500-49	75V	-	11.7μ	7.6 mil	"	"	11.0	-	-
499-63	57V	-	9.8μ	7.7 mil	"	"	11.0	-	-
499-61	61V	-	10.1μ	7.7 mil	"	"	11.0	-	-
499-17	54V	-	11.4μ	7.4 mil	"	"	12.0	-	-
499-60	60V	-	10.0μ	7.6 mil	"	"	11.0	-	-
498-46	64V	-	13.1μ	7.2 mil	"	"	11.0	-	-
498-22	60V	-	11.0μ	7.3 mil	"	"	11.0	-	-
498-17	57V	-	11.9μ	7.4 mil	"	"	11.0	-	-
57984-16B1	90V	1.3-1.7	8.5μ	5 mil	950°C	20 min.	10.5	950°C	10 min

LE I

DATA FOR AVALANCHE DIODES

Time Re-Dep	ΔPP	Temp Drive	Time Drive	ΔPP	V/B	C+	P out	N	Cal Drive	(X Dep)	(X +)
20 min.	9.3	1150°C	35 min	2.2	70V_1ma	2.4pf			69	5.3	2.4
10 min.	9.2	"	"	8.2	"	"	25	1%	69	5.3	2.4
20 min.	8.7	"	"	1.0	"	"	2.6		69	5.3	2.4
20 min.	9.3	"	"	3.7	85V_1ma	2.2pf	8-18		69	5.3	2.4
10 min.	10.8	"	"	11.0	75V_1ma	2.7pf			69	5.3	2.4
-	-	"	"	2.9	85V_1ma	2.3pf	0		140	4.6	3.4
10 min.	10.5	"	"	12.0	80V_1ma	2.2pf	85	4.7	69	5.3	2.4
20 min.	8.3	"	"	5.6	85V_1ma	2.4pf	0		69	5.3	2.4
-	-	"	135 min	2.5	80V_1ma	2.5pf	20		133	3.6	5.9
-	-	"	180 min	5.8	60V_1ma	2.5pf	24		179	2.4	6.6
-	-	-	-	-	40-45	2.9pf	0				
10 min.	-	1150°C	180 min	5.0	50V_1ma	1.8pf	.05-1		158	2.8	6.3
-	-	"	180 min	5.8	60V_1ma	2.5pf	15-48		168	2.6	6.5
-	-	"	135 min	1.7	90V_1ma	2.2pf	10-29		98	3.8	5.1
-	-	"	135 min	1.7	116V_1ma	2.3pf	5-30		126	4.3	5.8
-	-	"	135 min	1.5	68V_1ma	2.5pf	30-65		111.8	2.9	5.3
-	-	"	135 min	1.8	70V_1ma	2.2pf	0		120	3.0	5.5
-	-	"	260 min	.55	55V_1ma	2.6pf	0		207	2.4	7.2
-	-	"	135 min	1.3	65V_1ma	2.3pf	0		119	2.9	5.5
-	-	"	260 min	1.4	70V_1ma	2.5pf	0		261	2.9	8.2
-	-	"	180 min	3.0	75V_1ma	2.3pf	9-30		152	3.1	6.2
-	-	"	260 min	1.0	65V_1ma	2.5pf	65		224	2.5	7.5
10 min.	9.3	1150°C	35 min	3.6	70V_1ma	2.4pf	27-190	4.9%			

B

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Sylvania Woburn	(Microwave Dept.)	HD Series
Sylvania Woburn	(Material Production Department)	WL Series
Semi - Metals		SM Series
Monsanto		(no letter)

All measurements made by the supplier were repeated by the Microwave Development Group. The measurements consisted of:

a. Epitaxial Layer Thickness
b. Epitaxial Layer Resistivity
c. Substrate Thickness
d. Substrate Resistivity

Epitaxial layer thickness was determined on the basis of infra-red interference measurements made on a Bechman DK5 infra-red spectrophotometer. On each reading, the wavelength of two peaks and two valleys of the infra-red spectrogram were measured and the thickness computed for each pair of readings by means of a computer program written for this purpose. The readings were checked for agreement. If disagreement was less than 10%, the readings were averaged, and the average value used for subsequent computation of junction design.

The epitaxial layer resistivity was measured, using a specially designed three point probe aperatus. In this measurement, one of a row of three tungsten probes, pointed at the ends, is pulse biased in the reverse direction with respect to the other probes, while contacting the epitaxial surface. The breakdown voltage of the point contact diode thus probed, is measured and from this value, the resistivity of the epitaxial layer is calculated.

From the above data, the junction design computation is made by means of a computer program which calculates the diffusion time and temperature necessary to allow the depletion layer to punch through at breakdown. The program demands the following data relevent to the slice:

Slice Identification
Epitaxial layer thickness
Epitaxial layer resistivity
Substrate four point probe reading (V/I)
Substrate thickness
Substrate dopant
V/I reading following deposition

A typical page of a computer output is shown in Figure 1.

```
DO PART 1
SLICE DESIGN CALCULATIONS FOR AOD'S, BY EZECAL

      SLICE=HD-719-2
      BV3PP=95
     EPITHK=8.5
     SUB4PP=.14
     SUBTHK=6.7
     SUBOUT=.5
     DEP4PP=10.5
     SUBDOP=SB


     TMPDEP=   950
      TIDEP=    20
     TMPDRV=  1150
      TIDRV=    48.74883911
       CJBV=      .3


     RHOSUB=      .01069232
     RHOEPI=    1.426719447
     RHODEP=    47.25
     DRV4PP=    16.47508887
     RHODRV=    74.13789922
      XJDEP=      .189107755
      XDEPL=    5.769462855
       XOUT=     .6447169939
         XJ=    2.085820211
       NEPI=    3.788675184*10↑15
      NSDEP=    4*10↑20
         NS=    2.729099088*10↑19
       DIAM=    5.671362443
         SC=    2.424176184*10↑19
          Z=     .06060440045

TIDRV(1100)=2.7*TIDRV(1150)
```

FIGURE 1

TYPICAL OUTPUT OF AVALANCHE DIODE DESIGN PROGRAM

Deposition time and temperature have been fixed at 950°C and 20 minutes, but may be varied.

Drive in temperature is taken as 1150°C and drive in time is an output variable.

In addition, variables such as junction depth, depletion layer width, outdiffusion from the substrate, sheet resistance of the "P+" layer. Doping of the various layers, and diameter for a nominal capacitance of .3 pf at breakdown are printed out.

Material structural perfection has been evaluated on samples from each group of wafers either by Sirtl or modified Dash etching. The Sirtl etch consists of 2 parts of hydrofluoric acid to 1 part of a saturated solution of Cr_3O_3 in water. Wafers are typically etched for 20 seconds, rinsed and evaluated.

The modified Dash etch consists of 2 parts hydrofluoric acid, 5 parts nitric acid, and 13 parts acetic acid. Wafers are mounted on a teflon disc and placed in a rotating beaker, mounted with its axis at 45° to the horizontal. The beaker is rotated at 70 - 80 rpm. Etching time is typically 5 minutes. Wafers are then rinsed in water, demounted and examined.

Both Sirtl and Dash etchings have been evaluated as damage removal etching for wafers preparatory to epitaxial growth.

During the initial phases of the study, it appeared that the wafers prepared by the Dash etch yielded epitaxial layers of greater perfection, when compared with those etched with Sirtl etch. However, it was found that the cleaning procedure, necessitated by the waxes used in mounting the wafers for Dash etching was responsible for the difference. This procedure is as follows:

Wafers are degreased in trichlorethylene, and then placed in head (100° - 120°C) sulfuric acid for 20 minutes. They then go through 3 cycles of:

Nitric acid (80 - 90°C)	5 minutes	
De-ionized water	5 minutes	
Dilute (1-1) hydroflouric acid		1 minute
Deionized water	5 minutes	

Seventy-one (71) wafers were especially grown in the Microwave Department epitaxial reactor for this study during this reporting period, these were divided into 17 groups, a group being defines as wafers grown in the same epitaxial reactor run, usually 6 wafers per run. In most cases, the wafers

were cut in half following diffusion and half processed through to the non-inverted configuration. If the diodes showed promise at test at this point, the remaining half was processed as invertable chips, and evaluated.

III. 2 Histories of Various Runs

Run D561, was grown on antimony doped slices from Sylvania's Woburn material production facility and had resistivities of .009 - .012 ohm-cm. Wafers were Sirtl etched before growth. The resulting epitaxial film was from 8.4 to 10.3 microns thick and the three point probe reading was from 73 - 78 volts. A boron predeposition at 1025°C for 10 minutes was followed by a drive-in of 60 minutes for wafers number 1 and 3 and 90 minutes for wafers numbers 2 and 4.

The observed structure on this run was poor, a stacking fault density of approximately 50/cm^2 was noted together with a high density of very fine etch pits and inclusions. The diodes resulting burned out at low (10 - 15 mA) currents and did not oscillate.

Run 570, made on a substrate from this same ingot at Run 561, also received in Sirtl etch prior to epitaxial growth. Film thickness was 8.0 to 9.4 microns, and the three point probe breakdown was 68 - 72 volts. A 1025°C boron predeposition for 10 minutes was used, and drive-in at 1150°C was for 65 minutes.

Dash-etch evaluation showed about 50/cm^2 stacking fault density with a high concentration of fine structures and a brownish discoloration. In addition, growth patterns traceable to the substrate structure were observed. Electrically, results were poor. The devices showed no oscillations and burned out at low DC power levels (<1W).

Run 575 consisted of two slices from an epitaxial reactor run of 5 slices. The run was a duplicate of run 570. Three point probe breakdown was 76 - 79 volts; epitaxial layer thickness was 10.3 micron. Boron deposition was at 1025°C for 10 minutes and drive-in was at 1150°C for 105 minutes. Because of the deeper drive-in, the diodes from these slices did not burn out at levels as low as previous runs of this series. However, no oscillation could be obtained.

Run 576 was grown under the same conditions as the previous run. One wafer was given a boron deposition at 1025 for 10 minutes, the other at 950 for 20 minutes. Both slices received a 45 minute drive-in at 1150°C. Comparison of the diodes resulting from each slice showed a higher current capability in the group deposited at 950°C, with 50 mw power out. The group deposited at 1025°C burned out at power levels below threshold of oscillation.

Run 577 again repeated the growth condition of previous runs, and showed similar structure. An attempt was made to determine whether the high deposition temperature or the larger deposition time was responsible for the differences discovered in run 576. Deposition was carried out in two steps of 10 minutes each at 1025°C. Drive-in was for 50 minutes at 1150°C. The results were identical with those obtained on the slice which had received the high temperature deposition in Run 576.

Run 584 was a repeat of Run 577, with the same results. This experimental series was carried out in parallel with epitaxial material from the sources. The degree of structural imperfection varied from lot to lot and of course the details of growth conditions were not under our direct control and were often undergrown.

The following runs were on Monsanto-grown material. Lot 24-6870 had a three point probe breakdown of 56-64 volt, and had an epitaxial layer thickness of 6.6 - 7.4 microns. They were given a deposition of 10 minutes at 1025°C. Drive was 30 minutes at 1150°C. No oscillation was obtained from these diodes, and burn out occurred at currents below 25 mA.

Lot 20-520 had three point probe breakdown voltages from 82 to 84 volt, and epitaxial layer thicknesses of 12.5 - 13.7 microns. A deposition of 20 minutes at 1025°C was used and drive-in was at 1150°C for 120 minutes because of the deeper junction, these diodes stood higher currents (~35 mA) but no oscillations were obtained, however.

Slice 20-527-32 was used as a control from another material lot. Results were the same.

Slices BH-1899-1, BH-1899-10, BH1901-12 and BH1901-21 were given a boron deposition at 950°C for 20 minutes and drive-in 60 minutes at 1100°C. They had three point probes breakdown voltages of from 70 - 83 volt and epitaxial layer thicknesses of 8.2 - 9.2 microns. These diodes withstood up to 50 mA current. They were thermally limited in the non-inverted configuration, but the efficiency did not exceed 1%. The reserve halves were then processed to flip chips and the resulting diodes were pushed to 70 - 80 mA. Power out did not exceed 100 mw, however.

Wafers 24-524-15, 24-523-16, 24-523-17, 24-523-20 ranged from 52-60 volt three point probe breakdown voltage and had epitaxial layer thicknesses of from 7.2 - 10 microns. They were pre-deposited at 950°C for 20 minutes, with drive-in at 1150°C, for 150 minutes for slices 24-523-15 and 24-523-16 and 55 minutes for slices 24-523-17 and 24-523-20. Diodes tested showed oscillations with efficiency of the order 1 - 2% and power output up to 105 mw.

Slices grown at the Sylvania Woburn Production facility were also included in this study. In general, the structure of this material was quite poor and the results obtained seemed to correlate more with the structure than the processing. Slices WL-5-4 and WL-5-6 were combined in one run with slices WL-6-1 and WL-6-21. The former were respectively 81 volt and 84 volt three point probe breakdown, and 7.9 and 8.1 microns epitaxial layer thickness. The latter were 67 volt and 75 volt three point probe breakdown and 8.9 and 7.9 microns epitaxial layer thickness. These slices were from the earlier part of the study and were given boron pre-deposition at 1025°C for twenty minutes. Drive-in was at 1150°C for 21 minutes for WL-5-4 and WL-5-6 and for 75 minutes for WL-6-1 and for 30 minutes for WL-6-21. All diodes from this run were ruined when the controller on the furnace in which they were being oxidized for surface passivation malfunctioned.

The run was repeated with wafers WL-6-15 and WL-6-24. The former had a three point probe breakdown voltage of 68 volt and an epitaxial layer thickness of 9.4 microns. The latter had a three point probe breakdown voltage of 67 volt and an epitaxial layer thickness of 9.5 microns. Boron predeposition was the same as in the previous run and the drive-in conditions were; 1150°C and 90 minutes. These diodes were found to give better than 100 mw output with efficiencies of 3 - 4%. However, the plating on the invertable halves of the slices was poor and high thermal resistance (20 - 30°C/W) were encountered, limiting the input power to 8W or less.

The micro-structure of the WL-6 lot of wafers was quite good. Unfortunately this last run exhausted that lot. The structure of the next lot, WL-9 varied considerably from wafer to wafer, and over a given wafer. The reasons for this have not been explained although much effort was expended to trace all factors in its growth.

Wafers WL-9-1, WL-9-2, WL-9-3, WL-9-4, WL-9-6, WL-9-7 and WL-9-8 were run as a lot. WL-9-5 was used to study imperfection distribution over the wafers as were pieces from each of the slices run. WL-9-1 had a 62 volt three point probe breakdown voltage and a 8.1 micron epitaxial layer thickness. WL-9-2 had a 64 volt three point probe breakdown voltage and a 7.8 micron epitaxial layer thickness. WL-9-3 had a 67 volt three point probe breakdown voltage and an 8.2 micron epitaxial layer thickness. WL-9-4 had a 67 volt three point probe breakdown voltage and an epitaxial layer thickness of 7.4 microns. WL-9-6 had a three point probe breakdown voltage of 68 volts and an epitaxial layer thickness of 7.7 microns. WL-9-7 showed a three point probe breakdown voltage of 65 volts. Its epitaxial layer thickness was 8.3 microns. Finally, slice WL-9-8 gave a three point probe breakdown voltage of 66 volts and an epitaxial function depth of 7.9 microns.

These wafers were given a 10 minute boron pre-deposition at 1025°C and wafers WL-9-1, WL-9-2, WL-9-3 were driven in 35 minutes. Wafers WL-9-4, WL-9-6, WL-9-7 and WL-9-8 were driven in 50 minutes.

The diodes from these wafers were found to give a wide variation in characteristics, both within a wafer and from wafer to wafer. Approximately 63% of the diodes burned out at currents near the threshold of oscillation. However, about 15% were stable to the thermal limit and of these, approximately 5%, gave powers in excess of 100 mw and efficiencies of the order of 3-4%.

Since reasonable results seemed to be obtained from the WL series of wafers with the higher temperature boron pre-deposition, it was decided to combine with two other lots of wafers.

Wafers WL-2-13, WL-2-15, WL-2-16, WL-4-9 and WL-4-11 were selected for a repeat of the previous run. WL-2-13 had an epitaxial thickness of 8.5 microns and a three point probe breakdown voltage of 70 volts. WL-2-15 showed a three point probe breakdown of 70 volts and an epitaxial layer thickness of 9.5 microns. WL-2-16 had a three point probe breakdown voltage of 70 volts and an epitaxial layer thickness of 9.5 microns. WL-4-9 has a 73 volt three point probe breakdown voltage and an epitaxial layer thickness of 7.7 microns, whereas WL-4-11 had a three point probe breakdown voltage of 75 volts and a 7.0 micron epitaxial layer thickness. Examination of structure showed a very high concentration of stacking faults in all wafers. They were given a 10 minute boron pre-deposition at 1025°C and the following drive-in: wafer WL-2-13, 1150°C, 60 minutes; wafer WL-2-15, 1150°C, 95 minutes; wafer WL-2-16, 1150°C, 75 minutes; WL-4-9, 1150°C, 35 minutes and WL-4-11, 1150°C, 35 minutes.

All diodes from wafers in this group burned out at low power levels.

Finally, a group of wafers supplied by Semimetals was used in this study. SM57985-9, SM57985-17, SM57986-5, SM57986-15, SM57987-2 and SM52602-10 were processed as a batch. SM57985-9 had a three point probe breakdown voltage of 68 volt and an epitaxial layer thickness of 6.5 microns. SM57985-17 had an epitaxial layer thickness of 7.1 microns with a three point probe breakdown voltage of 68 volt. On the other hand, SM57986-5 had a three point probe breakdown voltage of 70 volt and an epitaxial layer thickness of 6.3 microns, whereas SM57986-15 had an epitaxial layer thickness of 6.2 microns while its three point probe breakdown was 75 volt. But SM57987-2 had an epitaxial layer thickness of 6.4 microns with a three point probe breakdown voltage reading of 74 volt, and SM52602 showed a three point probe voltage reading of 68 volt for an epitaxial layer thickness of 6.8 microns.

All six wafers had a 1025°C - 20 minutes boron pre-deposition, but to ensure exact conformity to the calculated junction design, each slice was driven in repeatedly. Slice SM57985-9 was driven in at 1100°C for 27 minutes, SM 57985-17 at 1100°C for 60 minutes, SM57986-5 at 1100°C for 10 minutes, SM57986-15 at 1100°C for 25 minutes, SM57987-2 at 1100°C for 12 minutes and SM52602-10 at 1100°C for 40 minutes. Evaluation of this material gave a picture of good structure, with few stacking faults and little fine structure or brownish discoloration. All diode fabricated from these wafers showed burn out at 30 mA or less.

To determine if the lower drive-in temperature of the above run affected diode burnout, a recent group of Semimetal slices were run with a 1150°C drive-in. The slices were SM-57984-5, SM57984-6, SM57984-11 and 52656-12. Slice 57984-5 had a three point probe breakdown voltage of 69 volts and an epitaxial layer thickness of 6.2 microns. Slice SM57984-6 had an epitaxial layer thickness of 8.5 microns and a three point probe breakdown voltage of 74 volts. Slice SM57984-11 had a three point probe breakdown voltage of 100 volts and an 8.5 micron epitaxial layer thickness. Slice SM52656-12 was similar to slice SM57984-5 in that it had a 65 volt three point probe voltage breakdown and a 6.2 micron epitaxial layer thickness. All wafers were given a boron pre-deposition at 1025°C for 20 minutes and driven in at 1150°C. Drive-in times were 40 minutes for all four wafers. The appearance of the wafer samples after Dash etching was good. Few stacking faults were found and relatively little micro-structure. The results obtained on measurement of the diodes was similar to those obtained from the previous experiment; the diodes burned out at less than 30 mA.

In order to determine if the premature burn-out is eliminated by reducing the boron pre-deposition temperature, as was the case with material from the other sources cited above, a run was next made with the boron pre-deposition temperature lowered to 950°C. The slice runs were SM62028-2, SM62028-6, SM62028-7,SM62028-9, SM62028-11 and SM62028-13. Slice SM62028-2 had an epitaxial thickness of 7.2 microns and a three point probe breakdown voltage of 75 volts. Slice SM62028-6 had a three point probe breakdown voltage of 67 volts and an epitaxial layer thickness of 7.5 microns. Slice SM62028-7 gave 66 volt three point probe breakdown voltage and an epitaxial layer thickness of 8.7 microns. SM62028-9 had a three point probe breakdown voltage of 69 volts and an epitaxial layer thickness of 8.5 microns. Slice SM62028-11 had a three point probe breakdown voltage of 79 volts and an epitaxial layer thickness of 8.4 microns, while Slice SM62028-13 had a three point probe breakdown voltage of 67 volts and an epitaxial layer thickness of 8.4 microns.

Study of ths structure of these wafers revealed little fine pitting and few

stacking faults. Evaluation of the slices from this run again showed burn out at low current levels.

The above series of experiments shows the dependence of diode characteristics upon damage induced by high concentration of boron introduced during pre-deposition. Further experiments along this line are continuing.

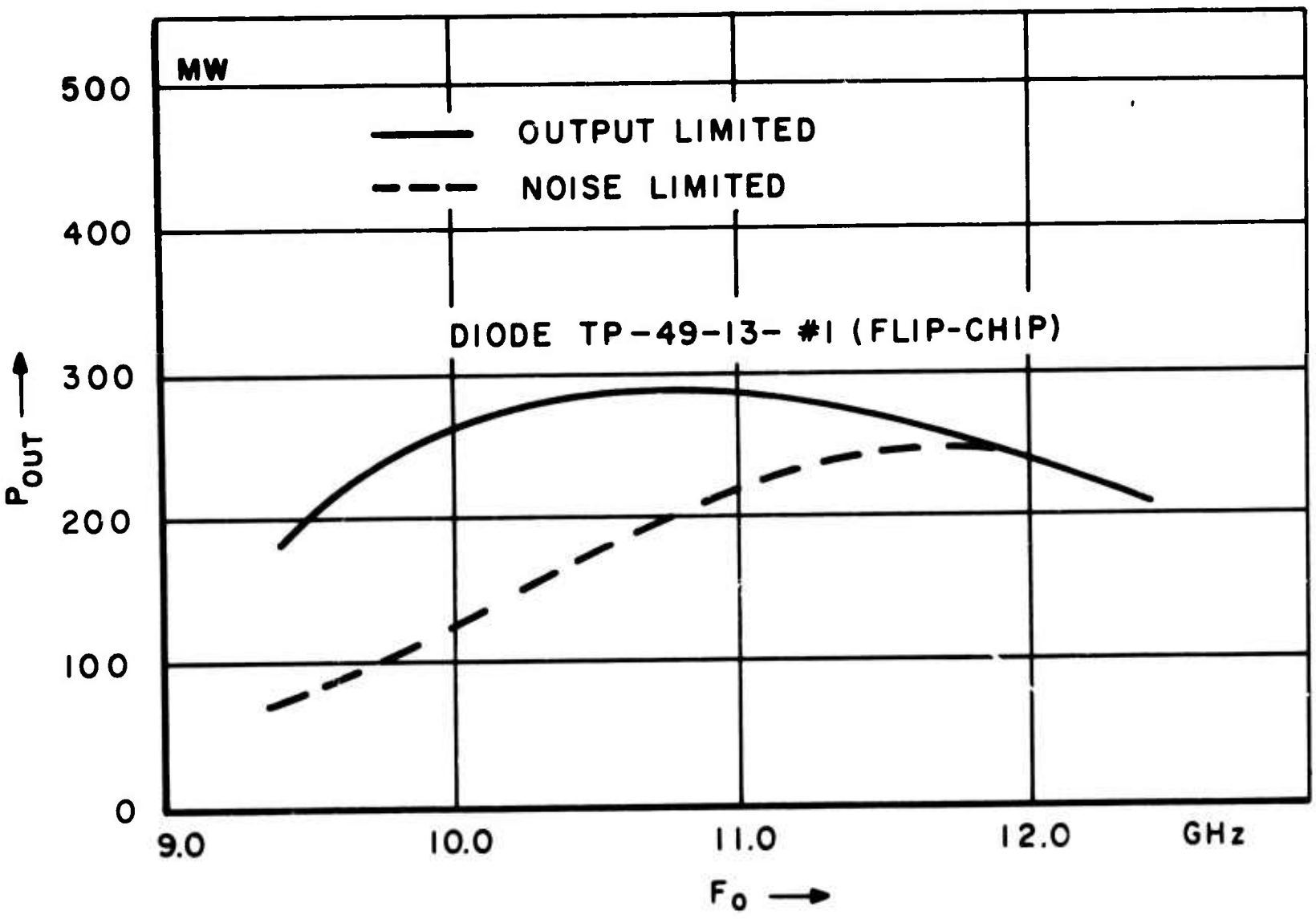
IV DIODE EVALUATION

During diode evaluation it was found, that the oscillator performance is critically dependent on the operating frequency, and current level. Figure 2 shows power output and efficiency of a TP-49 inverted diode. The solid curves represent the maximum power output and the corresponding efficiencies which could be obtained. The dashed curves indicate the maximum power output and efficiency limited by acceptable noise performance. It is clear that the useful power output of these diodes is noise limited below approximately 12 GHz. It was also found that these diodes tend to become very noisy (as observed on the spectrum analyzer) above a certain current density. The current level where this dispersion of the spectrum sets-in is a function of the operating frequency and goes approximately with the square of the latter. This agrees with theoretical considerations. The avalanche frequency increases with the square root of the current and is therefore shifted towards the oscillation frequency at high current levels. It was shown in the Second Quarterly Report (p. 10) that the intensity of the oscillator amplitude noise spectrum is determined by the noise measure M. Since M has a pole at w_a, the noise performance of the oscillator deteriorates rapidly as the avalanche frequency approaches the frequency of oscillation (or vice versa) Figure 3 shows the N/S ratio of an inverted-chip diode as a function of oscillation frequency (w_a constant). The curve shows a minimum, which, fortunately coincides approximately with the optimum output power range. However, the noise performance degrades much faster towards lower frequencies than does the power output. This is particularly true for high power diodes as can be seen from the previous graph. It follows then, that the avalanche frequency of high power diodes has to be lowered relative to a low power diode, if they are to give a clean output signal. Investigation of means to reduce the avalanche frequency are being carried out.

V LARGE SIGNAL AMPLIFICATION WITH AVALANCHE DIODES

V.1 Description of the Amplifier Circuit

It has been shown earlier, that amplification at microwave frequencies is possible. This is to be expected, since any negative resistance device has



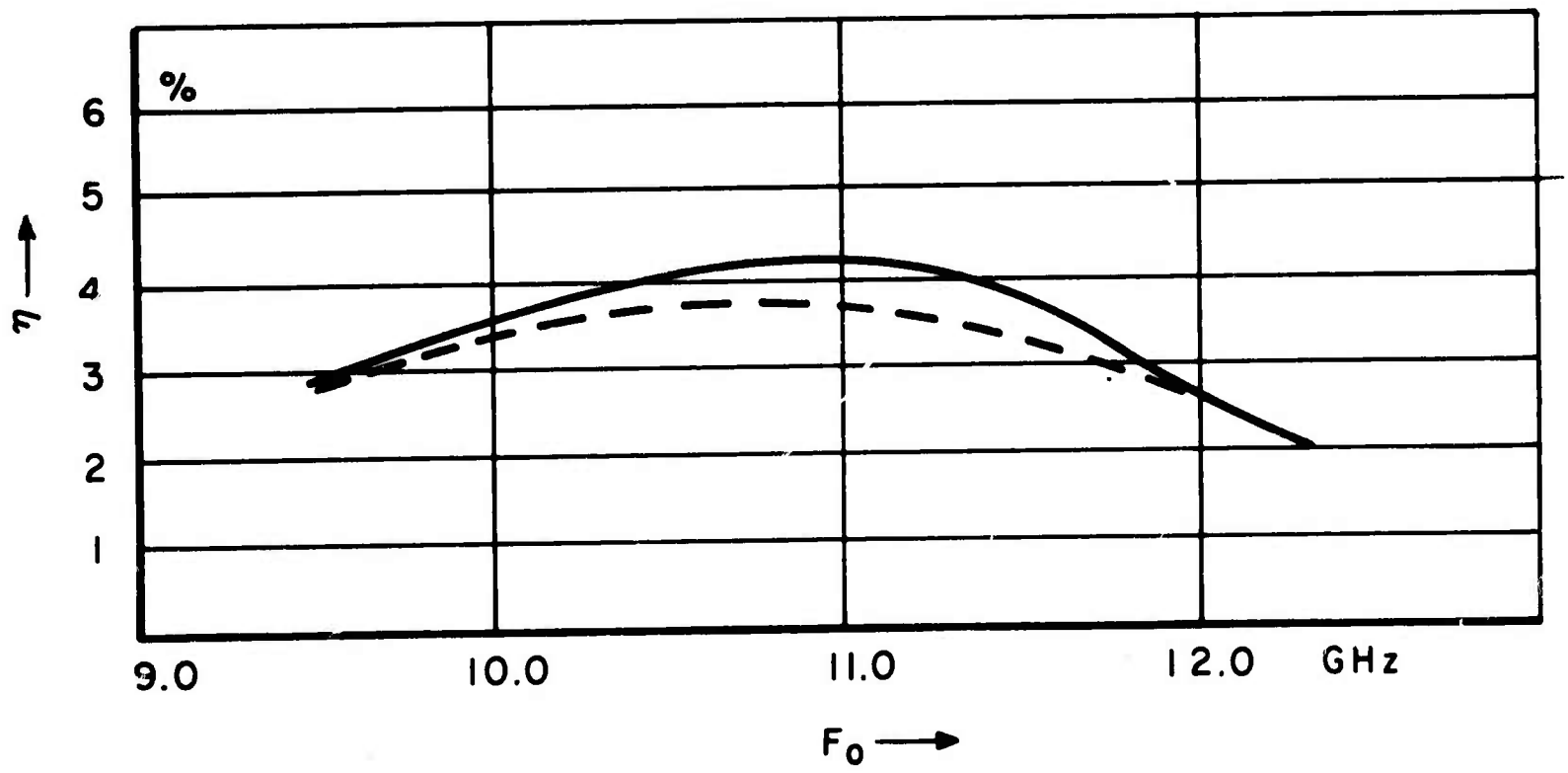


FIGURE 2

OUTPUT POWER OF AN AVALANCHE OSCILLATOR AS A FUNCTION OF FREQUENCY

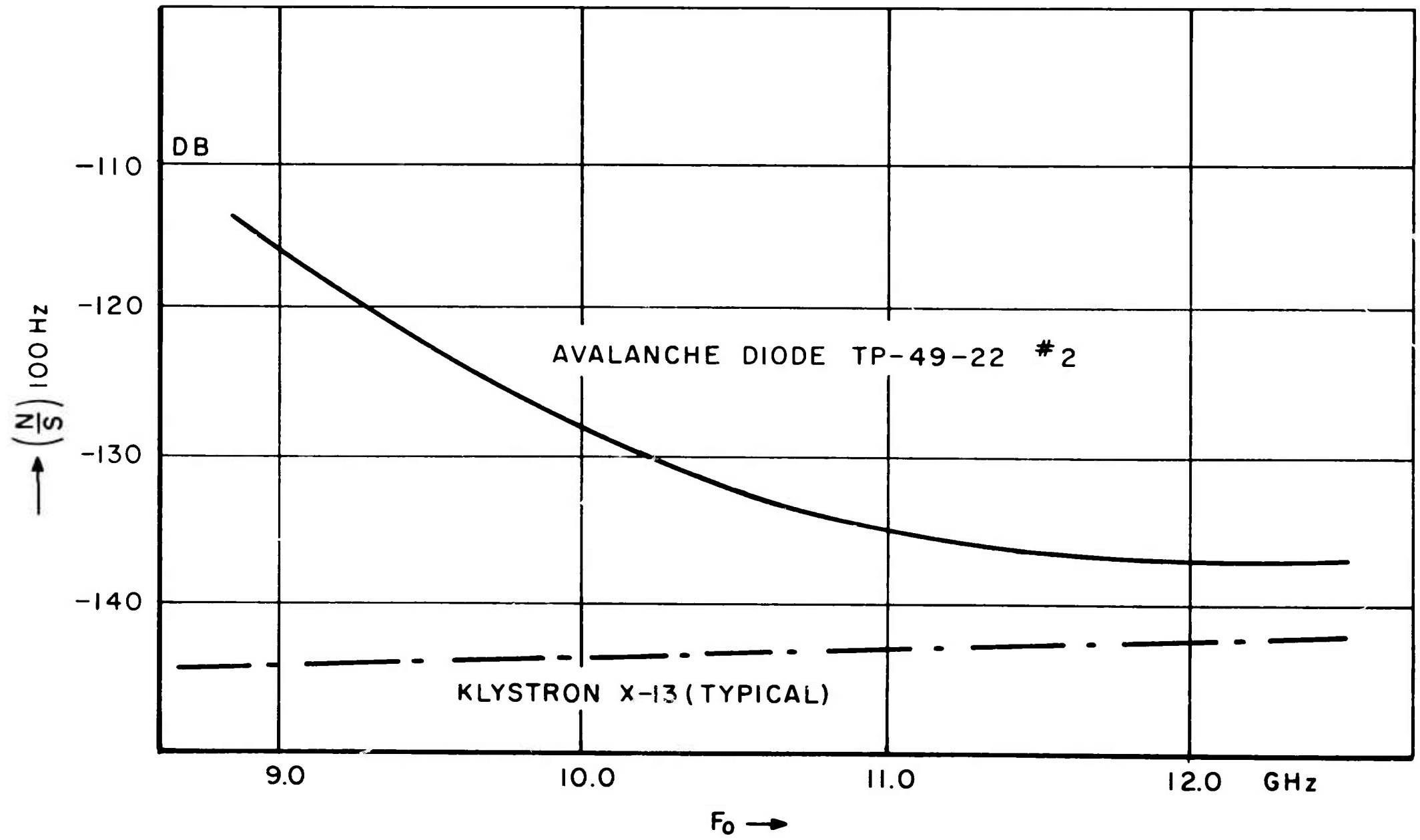


FIGURE 3

AM NOISE PERFORMANCE OF AN AVALANCHE OSCILLATOR AS A FUNCTION OF OPERATING FREQUENCY

potential amplifier properties if imbeded in a circuit providing the proper impedance levels and transmission characteristics. It was found that the standard oscillator test circuit can successfully be used. This is because the standard holder has a matching structure that is continuously and independently adjustable over a wide range (the impedance level presented to the diode, determines whether the circuit is an oscillator or amplifier.) The only additional requirement is some means of separating the incoming and reflected wave. A circulator or directional coupler can be used for this purpose. A block diagram of the circuit being used is shown in Figure 4. The directional coupler approach was chosen because of its inherently wider bandwidth capability. Figure 5 shows a plot of the swept output response of the amplifier for different input levels. The diode is an inverted chip device which gave 340 mW as an oscillator. It is seen that the stable realisable gain is decreased with increasing output level. This is due to saturation of the output power. At an output level of close to 400 mW, there is still a respectable gain of approximately 10db. These are believed to be the highest values obtained to date from an avalanche amplifier. It is also interesting to note how the bandwidth is changing. Even though the operation is highly non-linear, there seems to exist a gain-bandwidth relationship. Figure 6 shows the input-output relationship and gain of the same diode for fixed frequency.

V.2 Design Considerations for Avalanche Amplifiers

One of the objectives stated in the contract is the design of wideband avalanche oscillators and amplifiers. Since the design principles involved differ somewhat, they will be discussed seperately. The matching problems are similar to those encountered in the design of tunnel diode circuits, and some of the design theories can readily be adopted. There are, however, two major differences which should be kept in mind: These are:

a. The avalanche diode junction does not exhibit a significant negative resistance below a certain transition frequency f_a which is approximately one half the optimum operating frequency.

b. As a result of transit time effects, the magnitude of the negative resistance varies significantly over the useful range of operation. This is in contrast to the tunnel diode junction, whose negative resistance is practically independent of frequency.

The fact that the avalanche diode does not exhibit significant negative resistance below the frequency range of operation simplifies the problem of stabilization

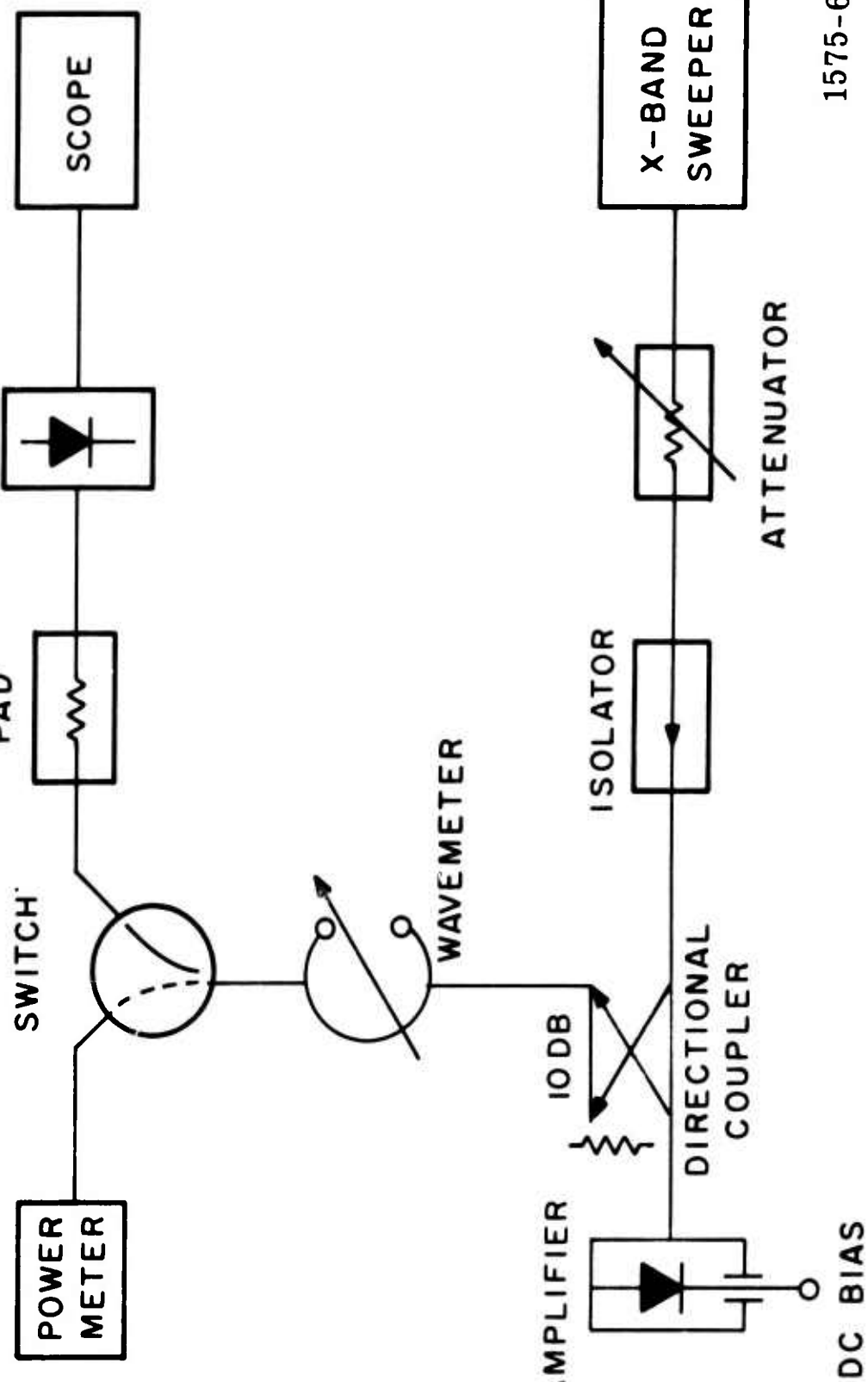


FIGURE 4
AVALANCHE AMPLIFIER TEST CIRCUIT

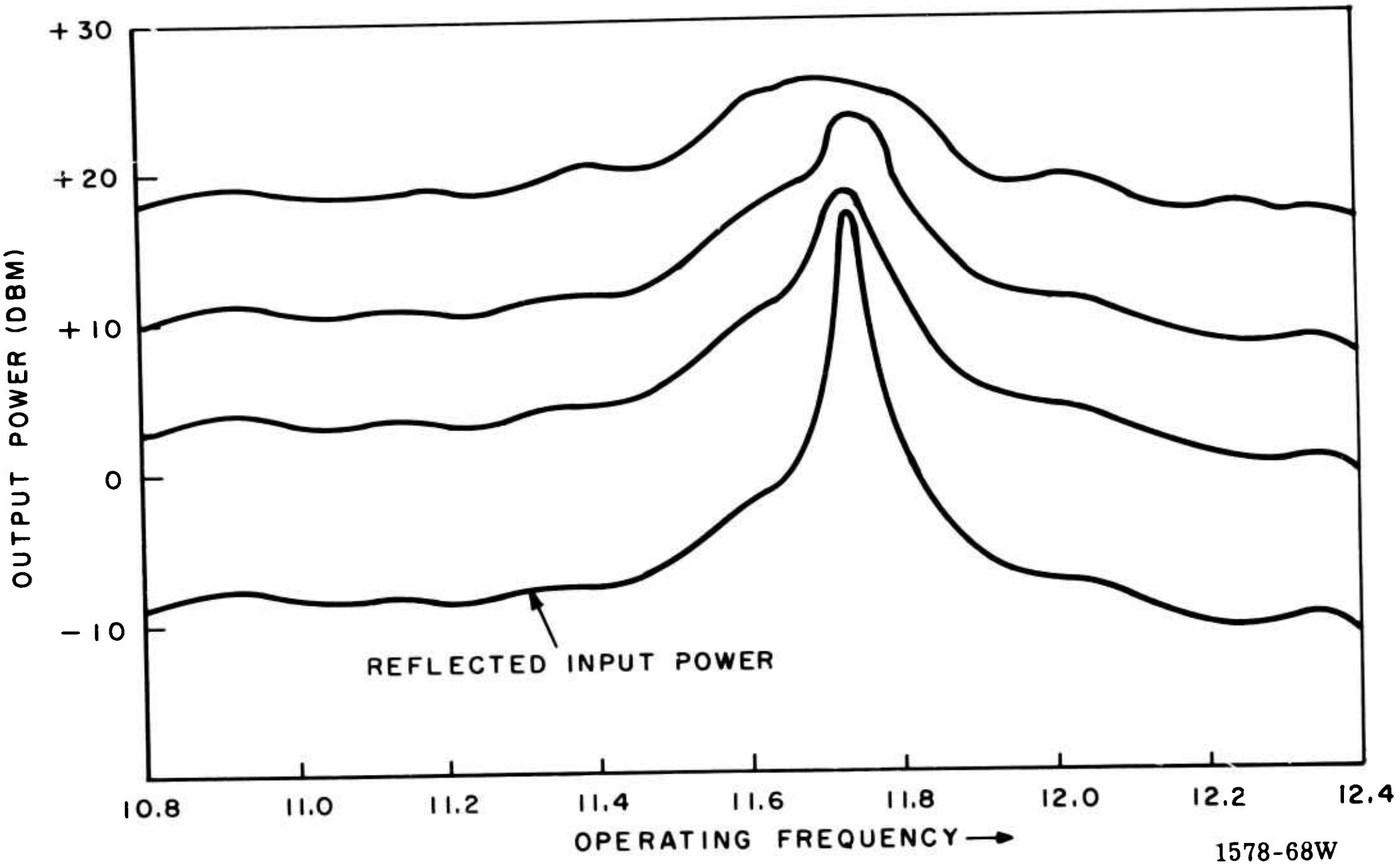


FIGURE 5
LARGE SIGNAL AVALANCHE AMPLIFIER
SWEPT OUTPUT RESPONSE AT VARIOUS INPUT LEVELS

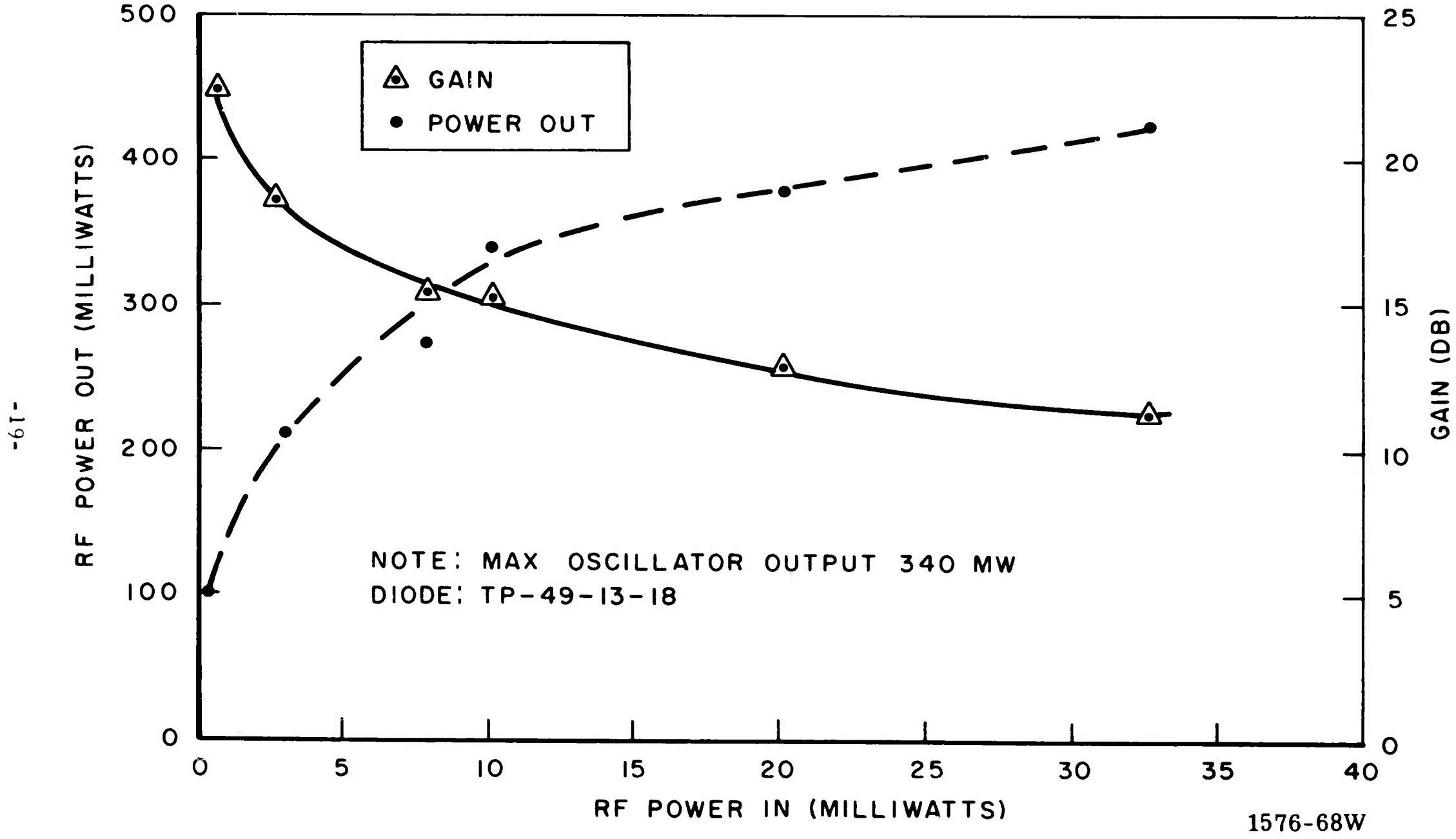


FIGURE 6

POWER OUTPUT AND GAIN OF AVALANCHE AMPLIFIER

compared to that associated with tunnel diode amplifiers. Avalanche amplifiers usually do not require out of band network stabilization.

The implication of b. is that the wide-band performance of avalanche amplifiers is severely degraded by the frequency dependence of the negative resistance. The potential gain-bandwidth capability of avalanche diodes, is less than that of the tunnel diode, unless a suitable form of compensation can be devised.

VI DESIGN OUTLINE FOR WIDEBAND TUNABLE AVALANCHE OSCILLATORS

One condition for steady-state oscillation is that the net reactance of the oscillatory loop be zero. The frequency of oscillation adjusts itself automatically so as to satisfy this condition. In order to extract maximum energy from the oscillator, it is necessary to present the proper load conductance to the diode circuit. If the diode conductance is fairly constant over the tuning range, the matching problem is reduced to the simple task of designing a broad-band impedance transformer as indicated in Figure 7a. In its simplest form, such a transformer can be realized in form of quarter wave sections of transmission lines of a resonant iris structure such as is being used in the present test holder. The broad-band tuning capability of this circuit has been established with up to 3GHz tuning range at X-band. It is believed that at the present, the major limitation is imposed by the diode itself through the frequency dependence of the negative resistance. Most of the efforts will be directed towards the problem of wide-band matching of avalanche amplifiers, where substantial improvements can be obtained over a simple structure by optimizing the matching network using modern network synthesis.

Design procedures for the design of wide-band matching networks and experimental results will be reported on in the next Quarterly report.

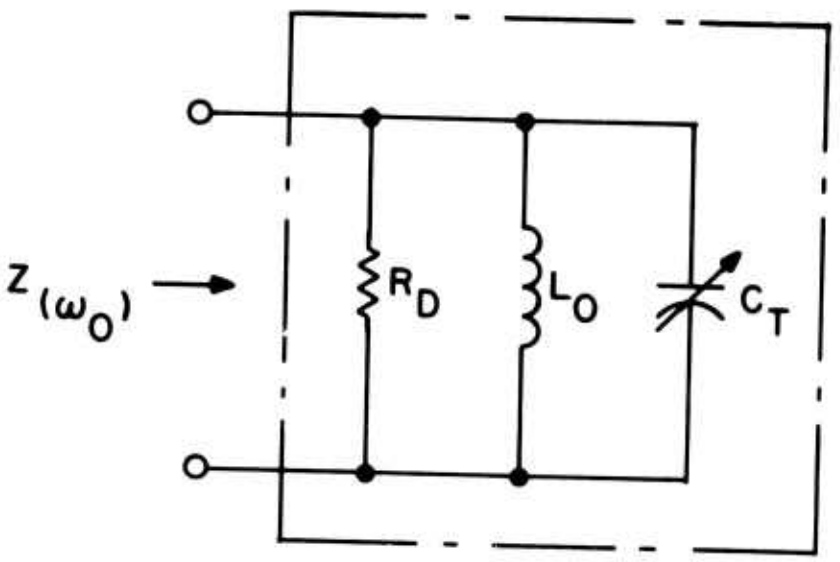
VII WORK PLANS FOR NEXT QUARTER

1. Continue investigation of material and process parameters required for diodes to stand high power inputs, particularly to solve the burn-out problem.

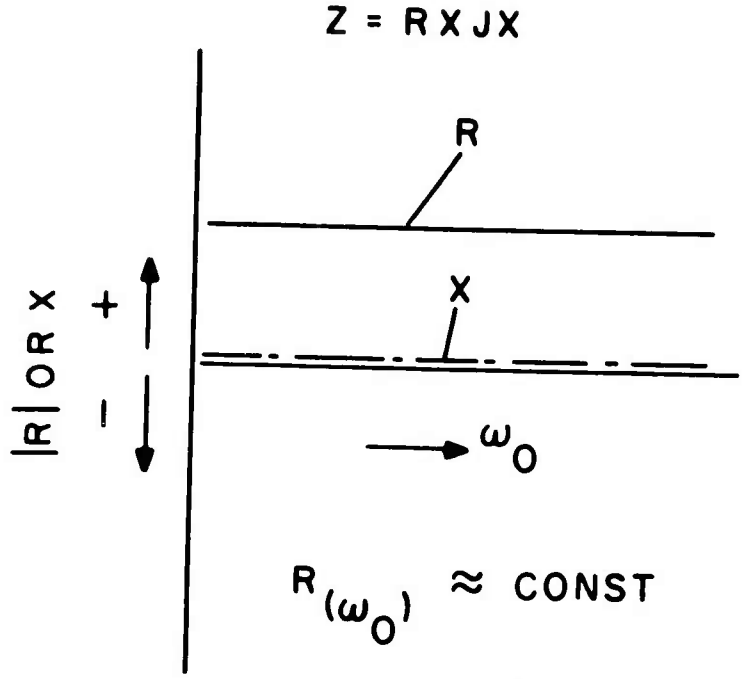
2. Optimization of design of high power inverted chip.

3. Improve performance of passivated devices.

a)



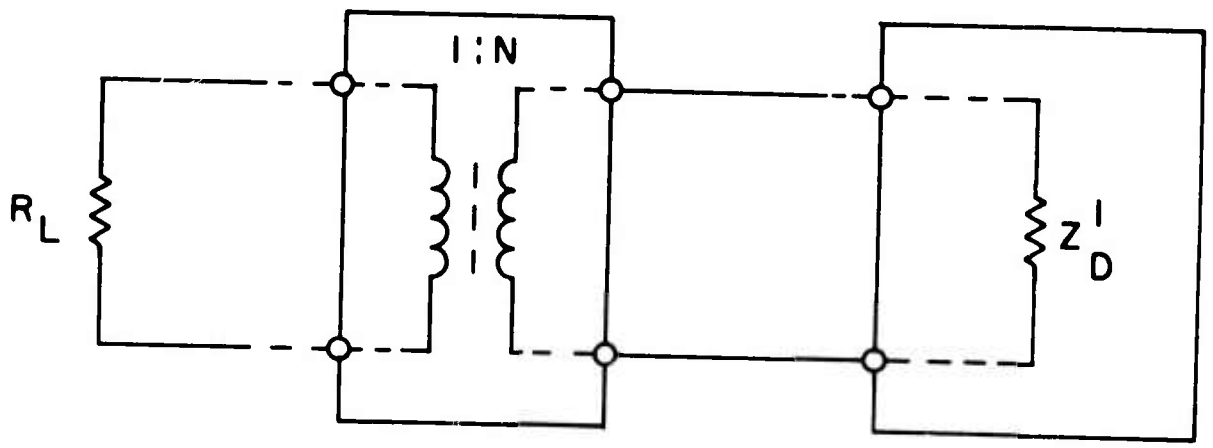
$$\omega_0 = \frac{1}{\sqrt{L_O\ C_T}} = f\,(a_v)$$



$R_{(\omega_0)} \approx$ CONST

$X_{(\omega_0)} = 0$

b)



LOAD

WIDEBAND IMPEDANCE TRANSFORMER

ACTIVE DEVICE APPROXIMATION INCLUDING PACKAGE

1577-68W

FIGURE 7
AVALANCHE OSCILLATOR DESIGN PRINCIPLES

4. Continue development of a high current pulsed source.

5. Start design of the diode and circuit for the pulsed oscillator.

6. Continue investigation of avalanche amplifier circuits and optimize diodes for this purpose.

7. Continue investigation of methods to reduce noise and measure efficiency of oscillators.

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13 ABSTRACT Work during the fourth quarter was devoted to optimization of device processing, geometry, development of a passivated-mesa process, identification of remaining material and related problems and evaluation of inverted chips as pulsed and CW oscillators. A process was perfected for inverted mounting which consistently resulted in very low thermal resistance on copper, and diamonds were successfully metalized and mounted in which will allow a further reduction of thermal resistance in the next quarter. Effort has been aimed at fabricating passivated and unpassivated diodes capable of inverted mounting which will produce CW power in the half-watt range at X-band. In addition, extensive studies of the noise properties of avalanche diodes has resulted in circuit refinements which reduce the AM noise by as much as 15 db in the frequency range of 10 kHz to 100 MHz off carrier, resulting in sideband-noise-to-carrier ratios better than -120 db/ kHz (for Q_L = 80 and 20 mW output).

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