PACKET RADIO EXPERIMENTAL REPEATER. TECHNICAL PLAN

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13 ABSTRACT

The ARPA packet switched interprocessor communications net provides a low-cost wideband transmission media. The expansion of this net via radio to subscribes or stand-alone radio packet nets is needed for future command and control communication. This document describes some of the background and system design guidelines for developing a packet radio repeater, describes its operation, and defines the functional design. The repeater consists of a radio section using spread spectrum, differently coherent MSK modulation/demodulation techniques, packet handling microprocessor, and program software. The design and fabrication of the repeater is in process. This is a working document and represents this status of development at this point in time.

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Technical Plan

Packet Radio Experimental Repeater

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SUMMARY

A. TECHNICAL PROBLEM

This project is one part of a larger effort directed at extending packet switching technology into the area of radio communications. The technical investigations are focused on a Packet Radio Network to serve fixed and mobile digital terminals in a tactical command and control environment. The objectives of the Collins investigations are:

- Perform research covering the application of radio frequency technology to packet switched communications.
- Participate in the overall ARPA Packet Communications Technology Program under the guidance of the Packet Radio Communications Working Group.
- Develop experimental equipments to support the propagation/noise measurements and packet radio system/network experiments.

B. GENERAL METHODOLOGY

The approach to the packet radio investigations is structured to provide a balance between analysis and experiments. Theoretical studies and laboratory experiments are directed at each of the following areas:

- Radio Networks - identification and evaluation of alternative network structures and operating disciplines.
- LOS Transmission - parametric investigation of the transmission variables such as operating frequency, area coverage, interference, power output and path losses.
- Modulation and Detection - investigation of signal processing techniques as related to contention, channelization, and coexistence properties.
- Equipment Design - identification and characterization of economic and technical constraints and limitations.
- Communications Security - evaluate the impact of encryption and traffic flow security requirements and disciplines on system design.

Results and data from these functionally orientated investigations are used in the design activities focused specifically on the experimental system and equipments. The design activities are organized as an iterative process to achieve a balance between the performance of the system, the techniques available for its creation and the constraints imposed by nature and technology.

C. TECHNICAL RESULTS

This quarterly report contains a technical plan for an experimental packet radio repeater. The characteristics planned for the initial packet radio system are identified, an experimental repeater to provide these system characteristics is defined, and the techniques

planned to implement the initial equipments are identified. Specific technical results reported or implied by the repeater technical plan include:

1. Frequency allocation data prepared

2. Repeater software organization and structure defined

3. Spread spectrum codes selected and acoustic devices ordered

4. Experimental radio system/station processor interface defined

5. Equipment form factor and printed circuit board/module profiles established

6. Many circuit functions designed, breadboarded, and being tested.

D. PLAN FOR NEXT QUARTER ACTIVITIES

The emphasis during the next quarter will be on the detailed design of the initial experimental repeater. Circuit design and layout will continue; modules and circuit boards will be fabricated, assembled, and checked out; and the pieces will be integrated into subsections. Tests will be run at this level to evaluate the design prior to the assembly of the initial experimental units.

Section 1

Foreword

An ARPA project is underway to extend packet switching technology into the area of radio communications. A network concept that utilizes the unique broadcast properties of radio systems, coupled with the asynchronous burst character of packet organized traffic, has been formulated. The network consists of an array of radio repeaters that handles addressed packets of digital information using two-radio broadcast techniques. The purpose of the network is to serve fixed and mobile digital terminals in a tactical command and control environment.

This document presents a technical plan for the design of an experimental packet radio repeater. The plan identifies specific system attributes for the initial repeaters, describes the operation of the repeater in terms of its network function, and presents the design baseline guiding the development efforts. This technical plan is not a specification or a final report, but rather a working document. It represents a "snapshot" of the design process taken at a particular point in time. The system and equipment designs presented can be expected to change as a result of test results and the continuing design effort.

A packet radio network is organized around three fundamental components: packet radio repeaters, one or more network management stations, and radio linked terminal devices. The repeater encompasses all of the technology and contains the basic functions required for any of these network components (with the exception of the specialized logic processes relating to end-to-end transfer protocols and certain top-level network management operations). For this reason, the repeater has been selected as the focal point for the initial system design of the packet transportation sub-net and as the equipment that will be developed for the initial system/network experiments.

The technical plan for the experimental repeater is presented in the following six sections. Section 2 provides an introduction to the experimental repeater and addresses such basic questions as: "What is a repeater," and What does it do?" The material in this section establishes a perspective for these questions and previews the more detailed answers contained in the later sections.

Section 3 identifies the principal system factors that impact repeater design. Relationships between performance, technique and environment are presented, and the characteristics planned for the initial experimental repeaters are identified.

Section 4 describes the organization and operation of a repeater in terms of its basic operations: receive packet, transmit packet, and header data processing. The basic functions planned to accomplish these processes are identified along with the interactions between the functions.

Section 5 and 6 focus on the internal repeater functions themselves and provide an additional level of detail. Section 5 describes the rf and signal processing functions in terms of how each will be accomplished. Section 6 describes the digital functions.

Section 7 is concerned with the integration of the various elements into a complete physical entity that is an experimental repeater. The packaging and power distribution plans for the initial versions of the experimental repeater are outlined in section 7.

This technical plan will be augmented by additional material dealing specifically with network design strategies, terminal and station design, and a plan for the experimental activities.

2.1 BACKGROUND

In the late 1960's, two developments oceurred whieh had a striking impaet on the eourse of digital network communieations: One was the creation of the Advaneed Researeh Projects Agency's (ARPA) resource sharing computer network, known as the ARPANET. The seeond development, whieh followed right on the heels of the first, was the multiple aecess radio network pioneered by the University of Hawaii and known as the ALOHA system. The unique attribute of these two networks is their departure from the conventional circuit switching teehnique. Rather, in eaeh instanee, a form of computerized switching is used in which addressed packets of information are used to communicate digital data between many sources and destinations.

A major reason that the ARPANET had such an impaet was that it offered switched wideband data communications at a potential cost far below that of other available alternatives, and that it afforded the same or better technical performance. The original objective was to find a way to interconneet a large number of computer resources distributed around the United States in such a way that they could be effectively shared. In the process of determining how best to connect these resources, the need for economic wideband switched digital service beeame elear.

The ALOHA system was derived from research efforts directed at finding means to connect remote terminals to the computation center in an effective manner. This led to the study and implementation of a system based on radio links and multiple access computer communication techniques. In the process, a new and fruitful aspect of switching technology based on radio transmission that is well suited to tactical command, control and communication networks was opened up.

In 1973 a Paeket Radio Communieations Working Group (PRCWG) was formed by ARPA to perform research and experiments directed at two primary goals. The first goal addresses the communication or packet transportation issues assoeiated with a distributed, mobile community of digital terminals. The second goal is directed at the eritieal shortage of rf speetrum and the need for improved frequeney management strategies. Both goals relate to the critical need for greatly improved eommunieations capability in the military tactical environment.

Each of the services has plans for the application of digital systems/eomputers in the taetical environment. These applieations, coupled with the present and projeeted needs for seeure voiee traffie, dictate that advaneed, eost-effeetive digital eommunication teehniques be found for Department of Defense applieations. Reliable, seeure, responsive digital networks are needed. The systems must perform their intended missions in a erowded, hostile rf speetrum; and the equipments to implement such systems must be light, eompaet, mobile, and require little power. It is toward this end that the Paeket Radio Projeet is headed.

2.2 NETWORK OVERVIEW

The Packet Radio (PR) network uses radio broadcast properties to provide area coverage for distributed command and control communications. The network traffic is formed into discrete segments, and a header is attached that defines how that segment is to be handled. These packets are then transferred between the network elements via the radio channel.

The radio channel and signaling strategies are structured to take maximum advantage of the statistics afforded by the discrete traffic segments. The radio channel resources are allocated on a packet basis, allowing more efficient utilization of the network. Each transfer between network nodes is an independent transaction, and the control mechanisms for managing these asynchronous actions are distributed throughout the network.

A PR network is organized around three primary functional components: PR terminal, PR station, and PR repeater. A terminal contains the rf, signal processing, and digital functions required to couple a data source/sink to the packet-organized radio channel and to exercise the required transfer protocols. Typical data devices considered for PR applications include: hand-held devices, tty-like devices, unattended sensors, display devices, and small computers.

The station consists of a "repeater" front-end that provides the coupling to the radio channel, plus the additional logical power to direct and monitor the network and traffic management operations. The station performs accounting, directory, and route determination functions for the radio system, and can also function as a gateway to other packet-switched networks.

The repeater serves two purposes: It contains the rf, signal processing and digital functions required to receive, regenerate, and retransmit packets, thereby extending the radio range between terminals and stations, and also contains the logic required for the distributed network management and flow control mechanisms.

The PR network concept provides a large degree of freedom in configuring the basic components for particular applications. Figures 2-1 through 2-3 illustrate general examples of the flexibility. In figure 2-1, dispersed data terminals can be interconnected or can interact with a data processor via a stand-alone PR network. Figure 2-2 illustrates a composite PR network to provide packet-switched connection between a number of distributed data processing locations and to further provide connections between the processing resources and a number of distributed digital terminals. This arrangement is representative of the application of PR to tactical command and control systems. Figure 2-3 portrays the network components arranged to provide an access/distribution coupling between a number of terminals and some form of a trunking or resource-sharing network. This example is representative of a PR extension of the ARPANET.

2.3 REQUIREMENTS AND OBJECTIVES

A PR network is defined as a flexible communications capability that can be tailored to a wide variety of tactical needs. The design objective is not to define a system that is "optimized" for a specific application, but rather, to create a "communications resource." This resource will include:

- A network architecture and a strict set of system disciplines that establish the network attributes.
- A family of hardware and software elements developed in accordance with these principles.

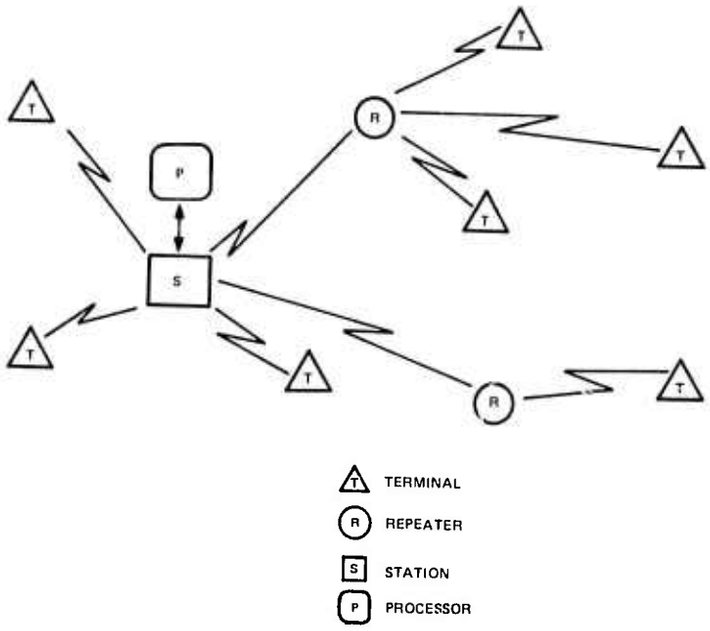


Figure 2-1. Stand-Alone Network.

- Instructions, procedures, and design aids that facilitate the direct application of this communication resource to specific missions, deployments and needs.

To guide the research process, a number of application-oriented factors must be addressed. This information is organized into three basic categories: (a) Traffic Characteristics, (b) User Environment, (c) Measures of Performance. A qualitative listing of significant characteristics is postulated covering these three primary topics.

a. Traffic Characteristics

This category addresses such questions as: "What types of service are required?" and "How many users are there?"

1. Digital Traffic. The network services digital transfers. The data is transferred sufficiently fast that it can serve interactive operations as well as more conventional communication requirements.

2. Large Number of Users. A particular network will support a large number of terminals; 100's to 1000's as opposed to 10 to 100 numbers.

3. Variety of Terminal Types. The network must accommodate many data sources/sinks including hand-held devices, TTY-like devices, display devices, printers, computing machines, and unattended sensors.

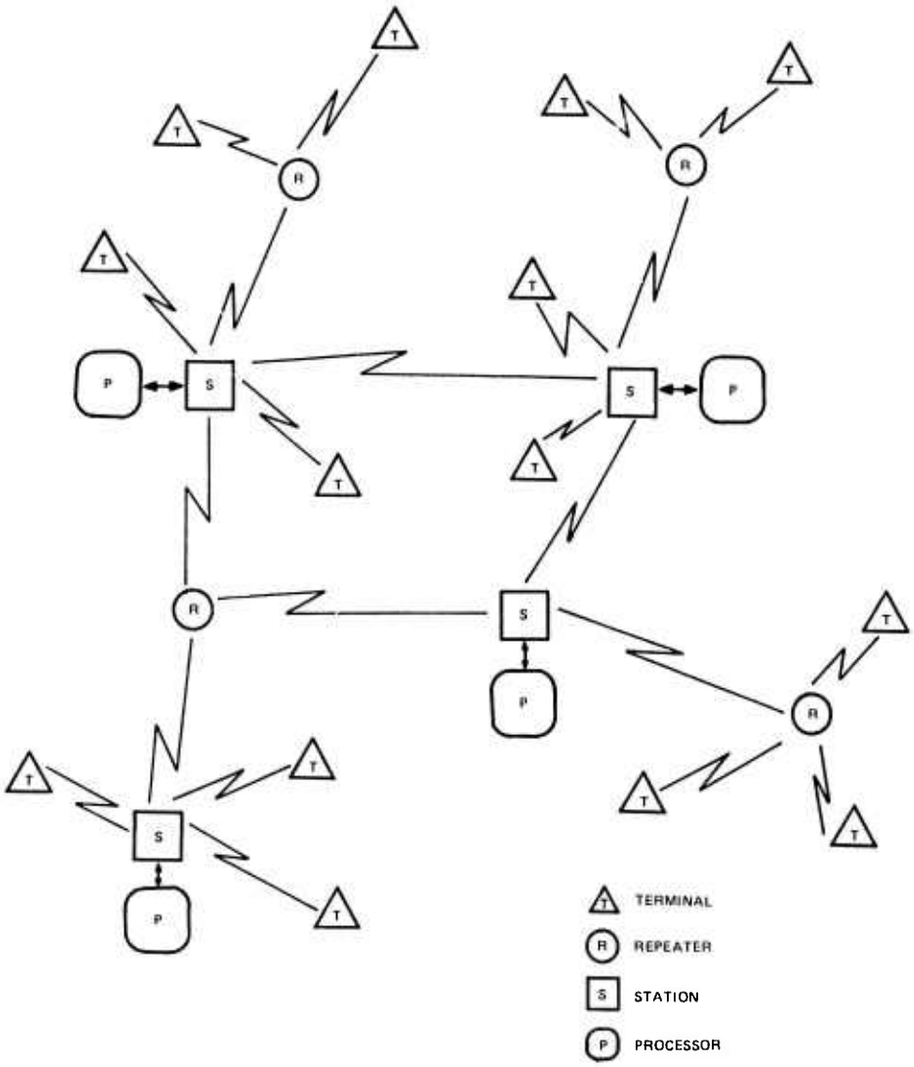


Figure 2-2. Composite Network.

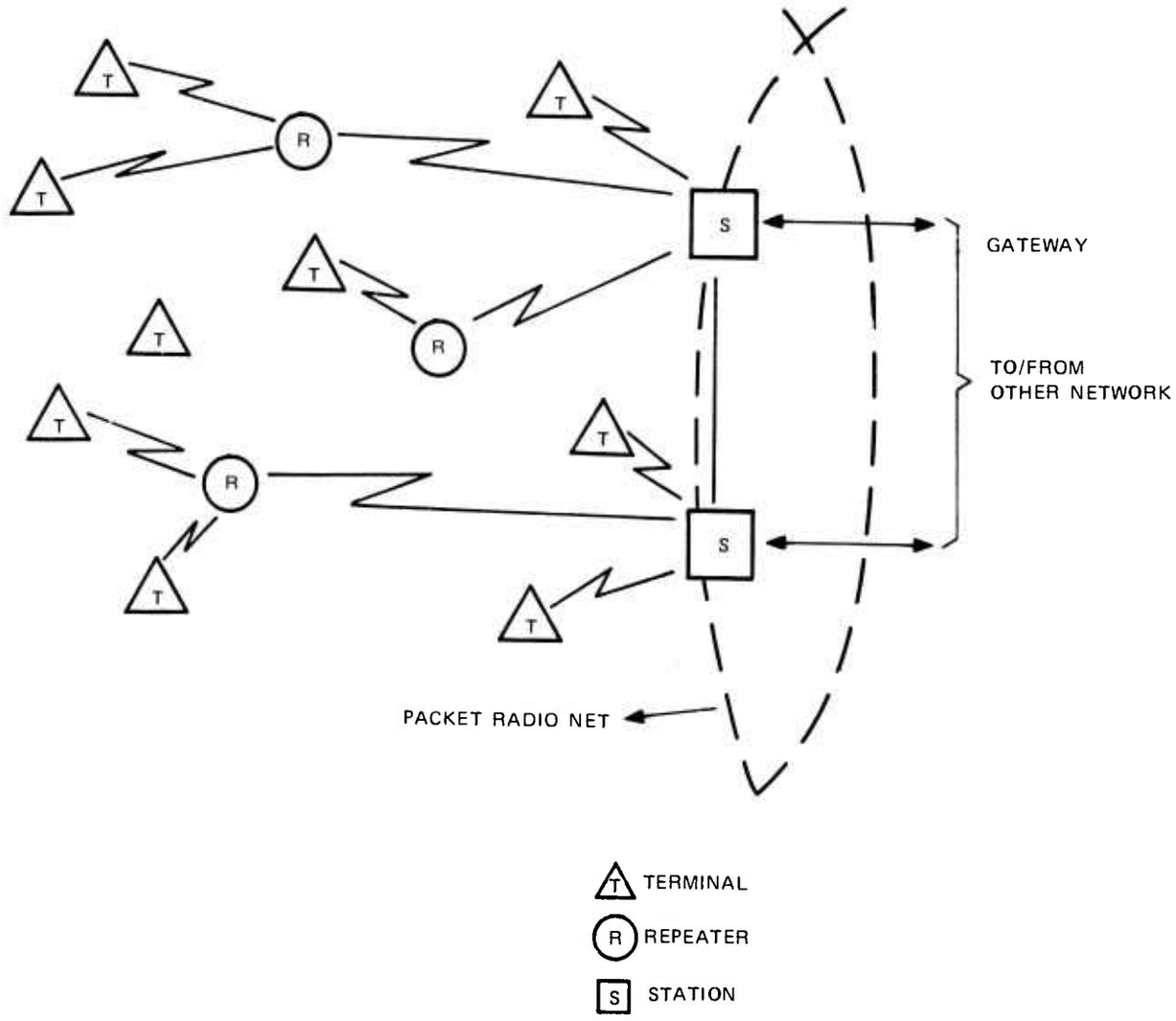


Figure 2-3. Internetwork Gateway.

4. Many Connection Options. In general, any user of the network can reach any resource served by the network: computing machine, another terminal, or another network.

b. User Environment.

This category highlights those non-traffic factors associated with a community of users that have a significant impact on the design of a network.

1. Area Coverage. The terminals can be dispersed over a large area: 100 to 1000 square miles.

2. Dynamic Deployment. The location of terminals within an area is a function of time. The network must accommodate terminals that change location on minutes to hours intervals, as well as terminals that must function well in motion.

3. All Types of Terrain. The geography of an area, and therefore the radio propagation environment in which a network will be deployed, cannot be controlled.

4. Crowded RF Spectrum. The network must coexist with other radio-based systems operating in the same geographic area. This includes systems that support the same users as the PR network (radars, point-to-point communication links, navigation systems, satellite systems, etc.) as well as radio systems intended to disrupt the network operation.

c. Measures of Performance

This category identifies the primary factors used to evaluate and judge a particular network approach.

1. Capacity. A measure of the traffic the network can handle at some specified level of performance is its capacity. This measure is highly dependent on the approach selected to provide the transfer paths (dedicated, switched, or shared channels) and the bit rates of the channel.

2. Response Time. A measure of the delay introduced into the user/destination transfer by the network is its response time. The factors that primarily affect response time are: bit rate, queuing delays, transmission errors, and transfer protocols.

3. Reliability. A measure of the probability that the network will be able to perform its intended mission is its reliability. Reliability is a function of the network topology, routing, and flow control procedures, interference thresholds, and equipment MTBF's.

4. Economics. The cost factors associated with achieving a particular level of performance are the economics. Costs are measured in terms of such important commodities as spectrum and prime power, as well as in dollars.

5. Security. A measure of the ability of the network to protect the users' information, including such factors as location, level of activity, and traffic content, is the security.

The qualitative indicators of the technical challenge provide a necessary perspective for the synthesis of a communications resource and the design of an experimental Packet Radio System.

2.4 REPEATER DEFINITION

The repeater is one of the three basic components of a PR network. Its purpose is to extend the effective radio range between stations and terminal, and to provide a mechanism for distributing the network management and flow control logic.

Physically, a repeater is made up of a radio section and a digital section as illustrated in figure 2-4. The radio section transforms an N bit digital data stream into a radiated rf signal and performs the inverse operation, rf signal to data and timing signals. The digital section

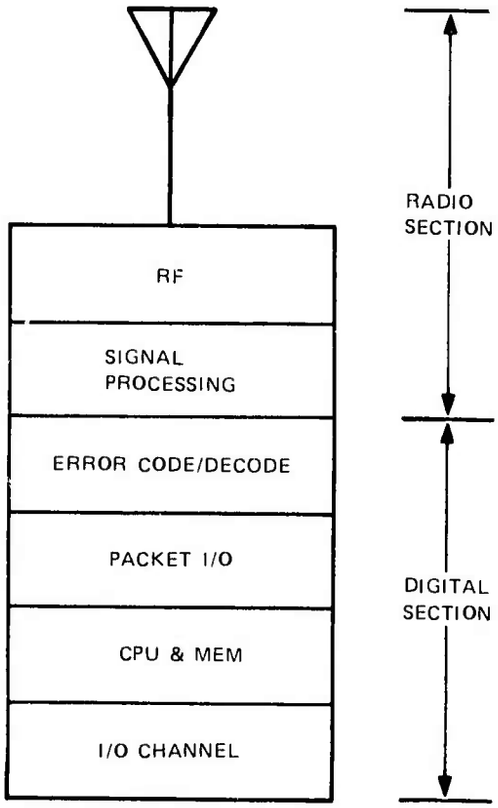


Figure 2-4. Packet Radio Repeater Basic Functions.

provides temporary storage for packets and contains the data processing programs and elements needed to accomplish the routing, error control, flow control, and management procedures required for network operation.

One of the objectives of the ARPA Packet Radio Project is to develop the capability to test the packet radio concept and designs by a series of experiments performed in a representative environment. The repeater design embodies the majority of the technical issues associated with the movement of packets within a network. For this reason, it has been selected as the focal point for the initial development effort. The design of the initial experimental repeaters is influenced by the following:

a. The experimental repeater is a flexible equipment designed with several degrees of freedom and with which specific communication link and basic network experiments can

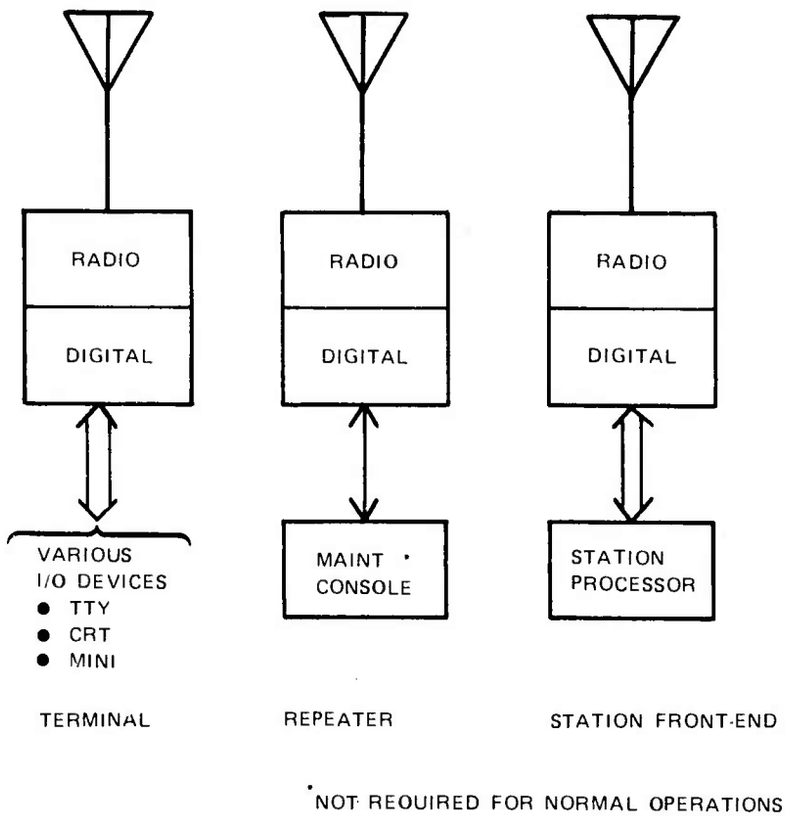


Figure 2-5. Configuration Options Packet Radio System Experiments.

be accomplished. The repeater is the primary element planned for the initial series of system experiments and, as such, muct be capable of performing the terminal access and station radio functions as well as the normal role defined for a PR repeater. The configuration options planned for the initial experimental units are illustrated in figure 2-5.

b. The experimental repeater serves as a vehicle for the investigation, development, and testing of promising new rf and device technology.

c. The experimental repeater is designed such that new techniques (for example, larger spreads, mutliple channels or frequency hopping) can be added as the exiperiments progress.

In accordance with these factors, the following guidelines are established for the implementation of the initial experimental equipment:

a. Modularity. The initial equipments will be organized and constructed as a set of functional modules. This is to facilitate the modification and/or change of specific features as the system design matures. Functional boundaries and defined interfaces will be established and strictly adhered to.

b. Size and Weight. Repeaters are ruggedized, man-transportable units. The initial equipments will be as compact as possible, using available components and construction techniques. The goal of small, compact equipments must be balanced against the requirements imposed by the experimental mission of the equipments (i.e., including option features and provisions for modification and change). The design goal for the experimental repeater is a volume equal to or less than 1 cubic foot (excluding batteries).

c. Low Power. Power drain is a very critical factor. Every effort will be made to reduce the power drain and to extend battery life. Low-power circuit techniques and devices are to be used and functions are to be turned off during periods when they are not needed. The design goal is 10 watts in receive.

d. Reliability. The prototype elements will be used to execute a series of experiments. The operation of these elements must be consistent and repeatable so as not to mask or degrade the experimental data. Also, the equipments must be available and operational a very large percentage of the time so that the experiments can proceed as scheduled. Quality components and construction techniques, coupled with well-conceived and tested designs, are needed. Maintenance features, including monitoring and self-test, must be considered during the design cycle and provided as an integrated part of each prototype equipment.

3.1 A PERSPECTIVE

The design of an advanced communication network is a complex, multi-level process. The goal is to achieve a balance between the need for the network, the techniques available for its creation, and the constraints imposed by nature and technology.

Figure 3-1 illustrates several of the dimensions involved in the design of a communication network, identifies typical variables involved at the different design levels, and provides a guide to impact between the design variables at the different levels. For example, the experimental repeater must ultimately be defined in terms of an effeetive radiated power (ERP), while the network is measured in terms of capacity. The translation between these two involves the consideration of such immediate factors as channel organization, range, bit error rate, path loss and power drain

One of the first steps accomplished by the Packet Radio Project was to qualitatively identify the attributes desired for an experimental packet radio system. These attributes are outlined in the following statements and provide a perspeetive for the discussion of the system and equipment parameters that follow.

a. Traffie Organized into Diserete Paekets. The paeket approach allows for asynchronous transfers within the network. This is desired to aecommodate the large number of users and the variety of terminal types.

b. Common Transmission Channel. The network uses a single eommon ehannel for all paeket transfers. This channel is shared by all network elements. The common channel structure is derived from the need for distributed, dynamie allocation of channel service and the corresponding need for minimum delay.

c. High Channel Capacity. The channel bit rate must be several orders of magnitude greater than the average rate of a typical terminal device. This is required to aeeommodate the eommon channel mode of operation and to minimize the link transmission time per packet, whieh is directly related to bit rate.

d. Omnidirectional Radio Broadcast. This relates to providing service for an area (not a specific location) and to the corresponding need for many terminals and repeaters to access the common channel.

e. Occupied Bandwidth Greater than Information Bandwidth. The Paeket Radio System will use spread spectrum signaling. The processing gain available from the additional bandwidth is used to provide multiple aecess provisions and a toleranee with respect to interfering signals.

f. Microprocessor in Each Equipment. Each network element has packet processing responsibilities associated with the requirement for distributed routing and flow eontrol meehanisms.

NETWORK MEASURES	SYSTEM VARIABLES	EQUIPMENT VARIABLES	ENVIRONMENTAL FACTORS
	PACKET OVERHEAD		
CAPACITY	CHANNEL ORGANIZATION	POWER OUTPUT	
	CHANNEL UTILIZATION	FREQUENCY	
	BIT RATE	OCCUPIED BANDWIDTH	PATH LOSS
	BIT ERROR RATE	SYNCHRONIZATION	MULTIPATH SPREAD
DELAY	PACKET SIZE	ANTENNA GAIN	PROPAGATION DELAY
	ACCESS QUE DELAY	PREAMBLE LENGTH	INTERFERENCE
	PROCESS QUE DELAY	MEMORY SIZE	
	ROUTING	WORD SIZE	
RELIABILITY	FLOW CONTROL	INSTRUCTION SET	
	TOPOLOGY	INSTRUCTION SPEED	
	RANGE	DYNAMIC RANGE	
	EQUIPMENT MTBF		

Figure 3-1. Typical Design Dimensions.

g. Low Bit Error Rate. Low bit and packet error rates are needed to avoid wasting the available network capacity and to minimize network delays associated with retransmissions.

h. Rugged, Lightweight, Low Power Equipment. The equipments must not restrict the flexibility and mobility of the users under tactical operating conditions.

Relationships between selected system characteristics and equipment parameters are outlined in the following paragraphs.

3.2 TRANSFER CHANNEL ORGANIZATION

A top-level question in the design of an experimental Packet Radio System is, "How should the various network elements be interconnected and how can the rf spectrum be organized to provide the desired interconnections?" Three basic interconnection techniques initially come to mind. The first provides a dedicated link between each pair of network elements that must exchange information. Another technique is to define a fixed number of transfer links and switch the terminations of these paths to serve the desired transfers. A third basic approach is to provide a single, high-capacity link and a suitable mechanism to allow all network pairs access to this common transfer media.

The latter scheme has been adopted for the initial experimental system. A single, common channel is defined in the frequency domain. Each network element (repeater, terminal and station) is configured such that it can send or receive packets via this common channel. The elements operate in a switched, half-duplex mode; that is, each element can transmit a packet or receive a packet, but not both simultaneously.

A simple "transmit when ready" philosophy, coupled with an acknowledgment protocol, is used to provide access to this common channel. Each network element transmits whenever a packet is ready. If the transfer is successful, an acknowledgment will be returned. If an acknowledgment is not received within a suitable time, the packet is launched again.

Theoretical models of this simple allocation scheme indicate a maximum value for the steady-state channel throughput equal to approximately one-sixth of the common channel capacity. When such factors as capture (receive one packet correctly when two or more conflict) and the network radio topology (not all elements mutually interfere) are taken into consideration, the utilization is shown to increase.

This approach has been adopted for the initial experimental system. It requires a minimum of complexity to implement and holds out the promise for effective use of rf spectrum and minimum delay when evaluated at the network level.

3.3 OPERATING FREQUENCY

The choice of an operating frequency band for the experimental system is bounded on the high end by the propagation losses between omnidirectional antenna and by the peak power characteristics of battery-driven microwave power sources. These two factors combine to reduce the received signal power and, therefore, the range as the operating frequency is increased. The lower bounds on the operating frequency are derived from the occupied bandwidth, small antenna size requirements and impulse noise considerations.

The system parameter that ties many of these factors together is range. For a line-of-sight path, omnidirectional antennas, and a fixed set of transmission characteristics (power, bandwidth, BER, etc.), the range relationship is:

$$d_2 = \frac{d_1}{f_2/f_1}$$

If the operating frequency is doubled, the range is reduced to one-half of the previous value. This relationship gives a worst-case indication of the impact of operating frequency on radio link range. Two additional factors are involved that tend to reduce the sensitivity of radio range to operating frequency.

The first factor is that the loss that will actually be experienced on packet radio links will be greater than free-space values due to the propagation environment. Okumura has published propagation data for a radio environment that approximates the conditions expected for packet radio. The primary parameters that influence the loss predicted in the Okumura model are the antenna heights at the two ends of the link and the character of the terrain traversed. With one antenna close to the ground (as it will be in a packet radio terminal application) and an "urban" environment (many obstructions and reflections), the path loss approaches a fourth power function of distance. This means that the radio range is reduced from that predicted by the free-space loss relationship and that the dependence of this range on operating frequency is also reduced. For those conditions where the fourth power law is in effect, the range versus frequency relationship approaches:

$$d_2 = \frac{d_1}{\sqrt{f_2/f_1}}$$

For this case, if we double the operating frequency, the range is reduced to approximately 0.7 of the value at the original frequency.

The second factor that has a bearing on the range/frequency question is the noise environment. Measurements indicate that noise decreases with increasing frequency at a rate of 4 to 6 dB per octave in the uhf and L-band range. The net effect is that, as the frequency is increased, a lower received signal power is acceptable to provide the same link performance, which in turn reduces the impact of operating frequency on range.

The conclusion is that packet radio range is not sharply influenced by the operating frequency and that the determination of a frequency range for the experimental system should be governed by antenna, power source and fractional bandwidth constraints and that the selection of specific operating frequencies should be based on the availability of experimental allocations in a government band.

Antenna size decreases linearly with frequency and the transportable antenna requirements for the experimental system can be satisfied at any frequency above about 100 MHz. The transmit power required (10 to 20 watts) can be provided by a transistor amplifier, with good efficiency, at frequencies up to at least 2 GHz.

The frequency range from 1.71 GHz to 1.85 GHz will be used for the initial experiments. It is in the desired 100-MHz to 2-GHz region and appears to provide the desired interference conditions with regard to existing occupants of the band.

3.4 BIT RATE

The maximum rate that an omnidirectional channel can support is limited by the effects of the delay spread due to multipath. An upper limit can be approximated by the general relationship that the symbol period be at least twice the delay spread:

$$T_{sym} = \frac{N_c}{R_d} \geq 2T_{ms}$$

where:

T_{sym} = Symbol period - seconds

N_c = Number of bits per symbol

R_d = Bit rate - bits/second

T_{ms} = Delay spread - seconds

Measurements of the propagation environment have been made in the San Francisco area as a part of the Packet Radio Project. The initial results indicate that delay spreads in the order of 2 to 3 microseconds will be common, but that spreads in excess of 5 microseconds are rare.

This data indicates that an upper limit for the symbol period in a severe multipath environment is 10 microseconds. If a 1-bit-per-symbol modulation technique is used, the channel rate is limited to 100 Kbps. Higher rates can be achieved in this same environment by using multiple bit-per-symbol coding (4 phase, 2-bit-per-symbol; or 8 phase, 3-bit-per-symbol, etc.). These techniques require additional equipment complexity and somewhat greater receive signal power to achieve the same level of performance.

A second primary consideration for the packet radio system is the impact of bit rate on range under conditions of limited peak transmitter power. As the range or link distance is increased, a constant power channel reaches a point where the rate becomes limited by the transmit power and path loss statistics. Beyond this range, the rate that the channel can sustain at a fixed BER drops off rapidly. Figure 3-2 illustrates typical range versus bit relationships, including the constraints imposed by the multipath delay spread.

Two data rates are provided in the experimental system. The rate for terminal/repeater transfers is 100 Kbps. This rate was selected to provide the maximum capacity in the anticipated multipath environment with a minimum of equipment complexity. The range predicted for this type link varies between 2 miles and 16 miles as a function of the character of the terrain.

The rate selected for repeater/repeater transfers is 400 Kbps. In general, repeater antennas will be higher than terminal antennas and will therefore experience less multipath and lower path loss. Also, the repeater/repeater link has 9 dBi antenna gain at each end. Range will again depend on the characteristics of particular paths, but values from 10 to 30 miles are possible depending on antenna placement.

3.5 MODULATION

The signaling waveform for the experimental repeater involves two levels of modulation. One level deals with making the transmission bandwidth much larger than the information bandwidth, and the other is concerned with forming the individual transmission symbols.

A spread spectrum mode of signaling has been selected for the experimental system. The processing gain associated with the expanded bandwidth can be used to provide a degree of "capture" for the multiple access channel or some protection against interfering signals. The spread techniques also reduce the effect of the packet radio signal on other systems in the same general frequency band.

A code-spread technique has been selected for the initial experimental repeaters. This approach offers the following advantages:

a. The energy distribution is evenly spread in frequency and constant with time during the transmission of a packet. This type of signal coordinates well within most types of existing services.

b. Surface Acoustic Wave (SAW) technology offers a simple and economic means for implementing this approach and the SAWD matched filters are self-synchronizing with respect to the code sequence.

c. The design is adaptable to addition of frequency hop spread spectrum if spread factors need be larger than that possible using code spread alone.

The spread factor for the experimental system is constrained by available device technology. Factors of a few hundred represent current SAWD technology for coded devices and larger spread factor units depart considerably from theoretical performance. A spread factor of 128 has been chosen for the 100-Kbps rate and 32 for the 400-Kbps rate. The ratio results in the same chip rate for the two data rates. This approach results in equipment simplification.

The technique selected for modulating the chips is MSK. Also known as fast FSK, FM-PSK, and staggered QPSK, this technique results in a constant amplitude signal that exhibits little band spreading when put through a class C amplifier. This is a desirable property as it

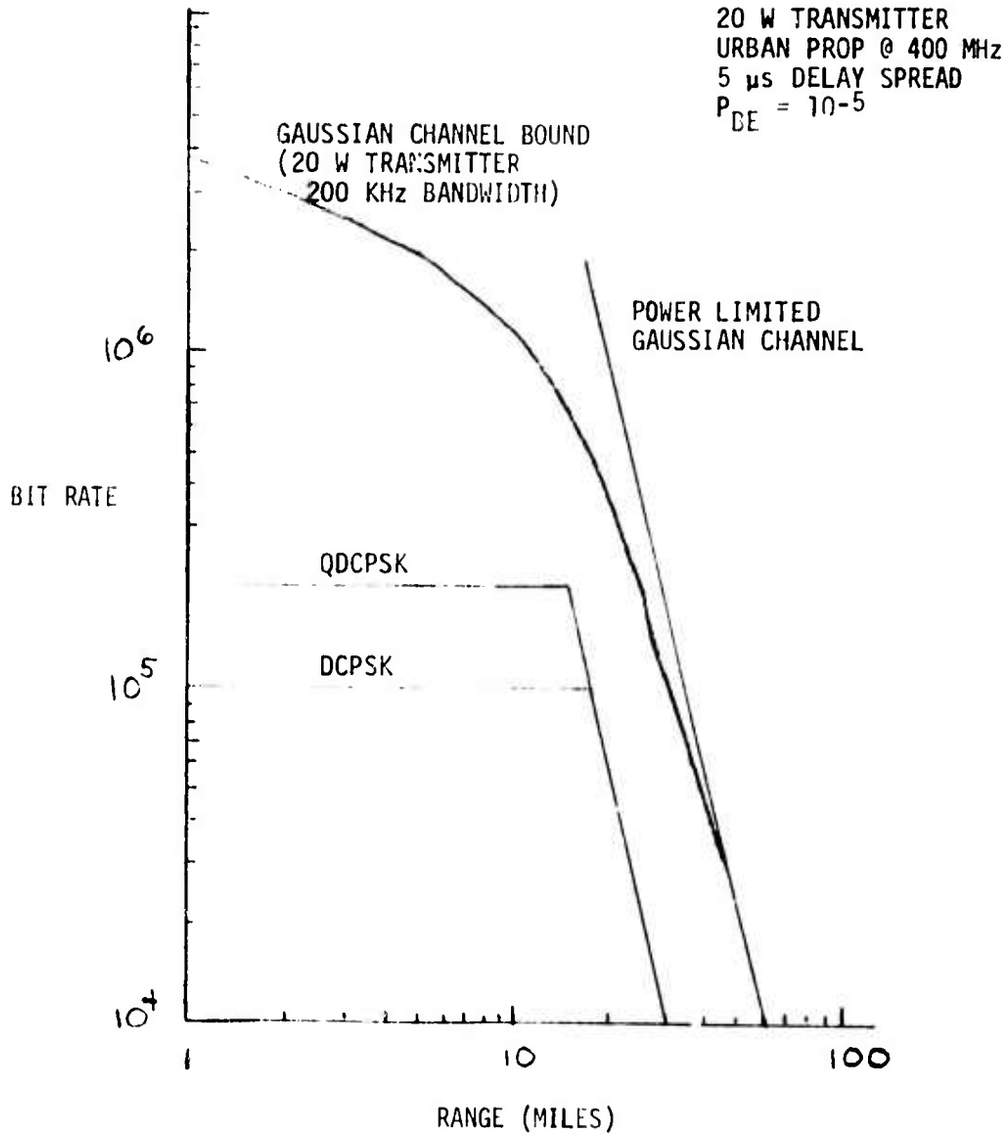


Figure 3-2. Typical RF Channels.

allows inereased power amplifier effieiency and minimizes the amount of high level output filtering required.

Figure 3-3 shows the power speetral density of the experimental repeater and illustrates the MSK speetrum, ineluding the effects of the 50-MHz output filter. Figure 3-4 illustrates the differenees in speetral density between MSK and biphase PSK.

3.6 DETECTION

A matehed-filter, differentially eoherent deteetion approach has been selected for the experimental repeater. Figure 3-5 gives a performance comparison in terms of BER versus signal-to-noise for several different detection schemes. The best performance is achieved by a coherent process (CPSK or CMSK) and the poorest results are obtained from noncoherent detection using different eodes for a 1 and a 0 (PO-MSK).

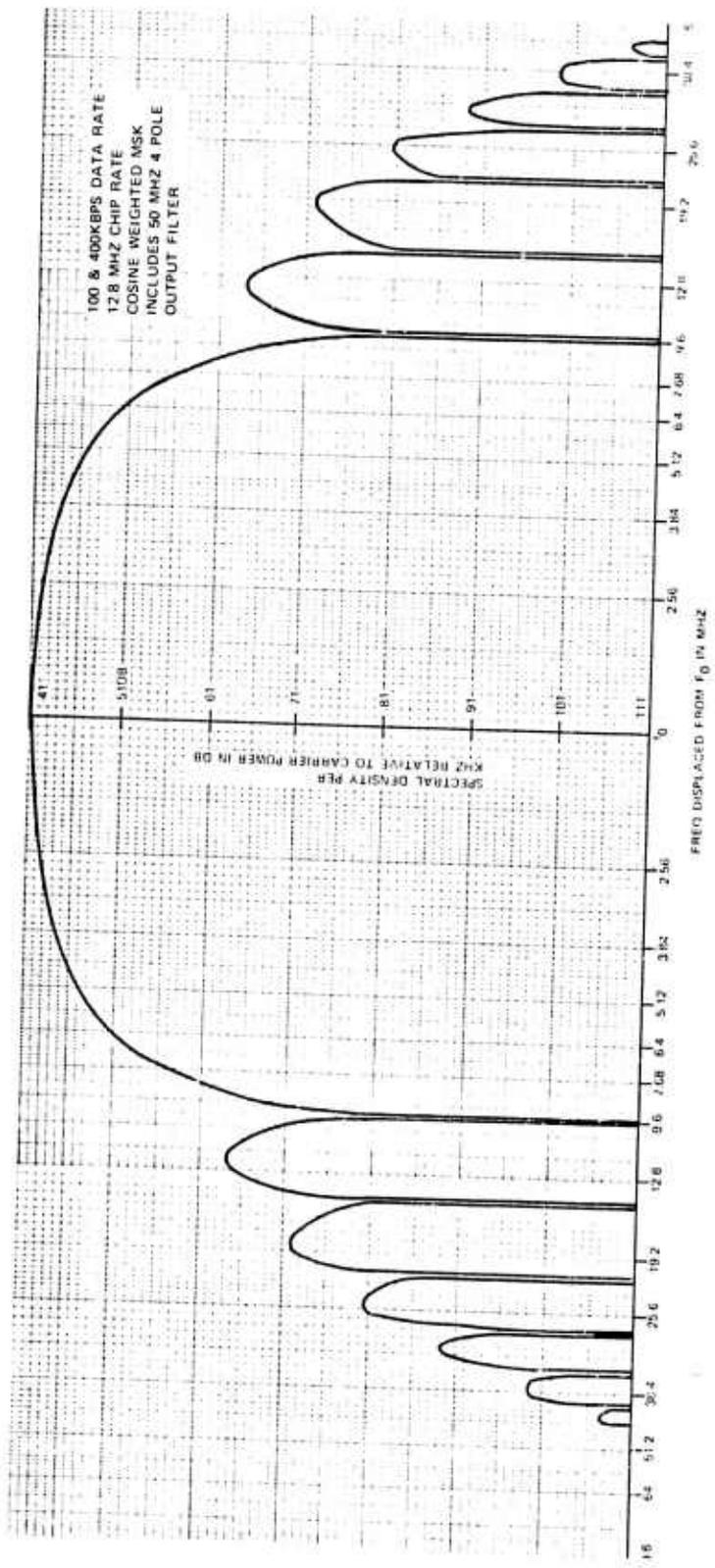


Figure 3-3. Power Spectral Density Experimental Repeater.

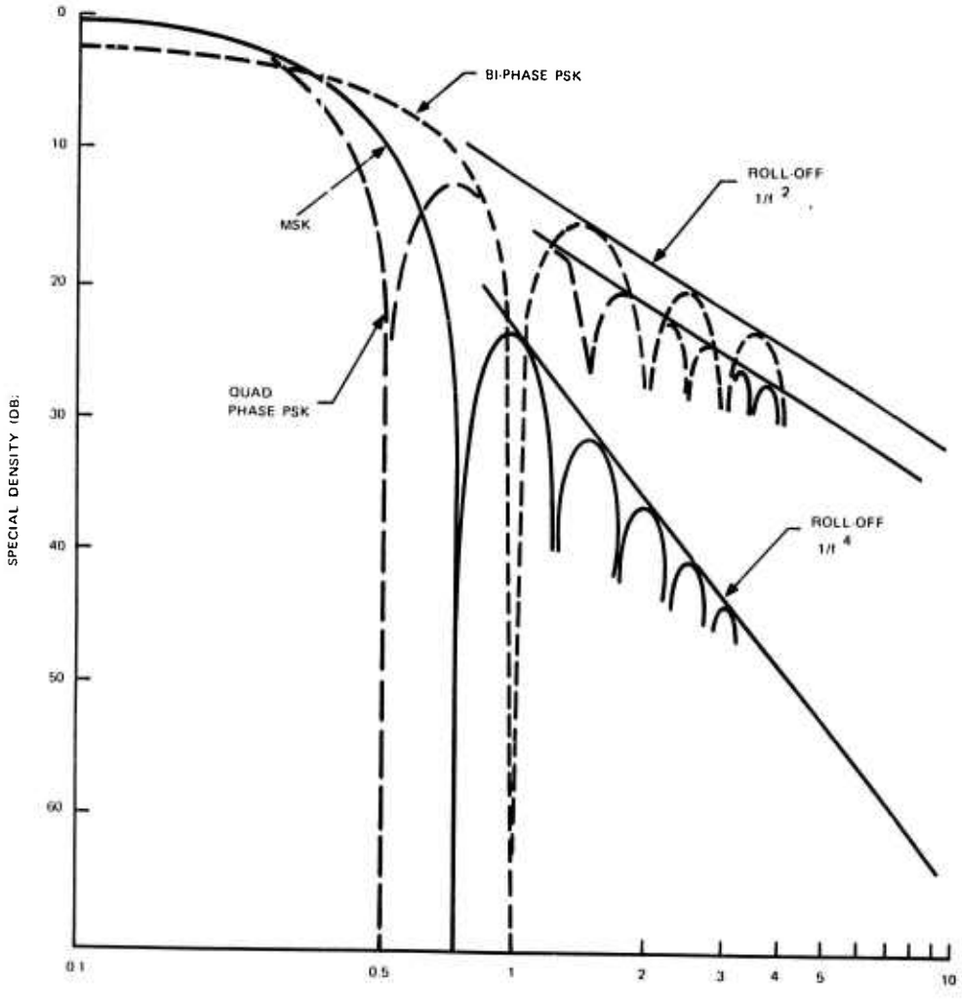


Figure 3-4. Relative Spectral Density.

The differentially coherent techniques require approximately 1 dB additional E_b/N_o to achieve the same BER as the coherent technique. This is a small price to pay when balanced against the additional equipment complexity required for coherent operation.

The matched filter will be implemented using a surface acoustic wave device. This technique is self-synchronizing with respect to the code sequence, and holds out the promise for small, low-cost, high-performance detectors.

3.7 PACKET ORGANIZATION

A packet is the container in which information is packaged prior to its introduction into the transportation sub-net. The packet is designed, as are containers for other transportation systems, with one eye on the type and character of the information it will handle and the other eye focused on the needs of the transportation system.

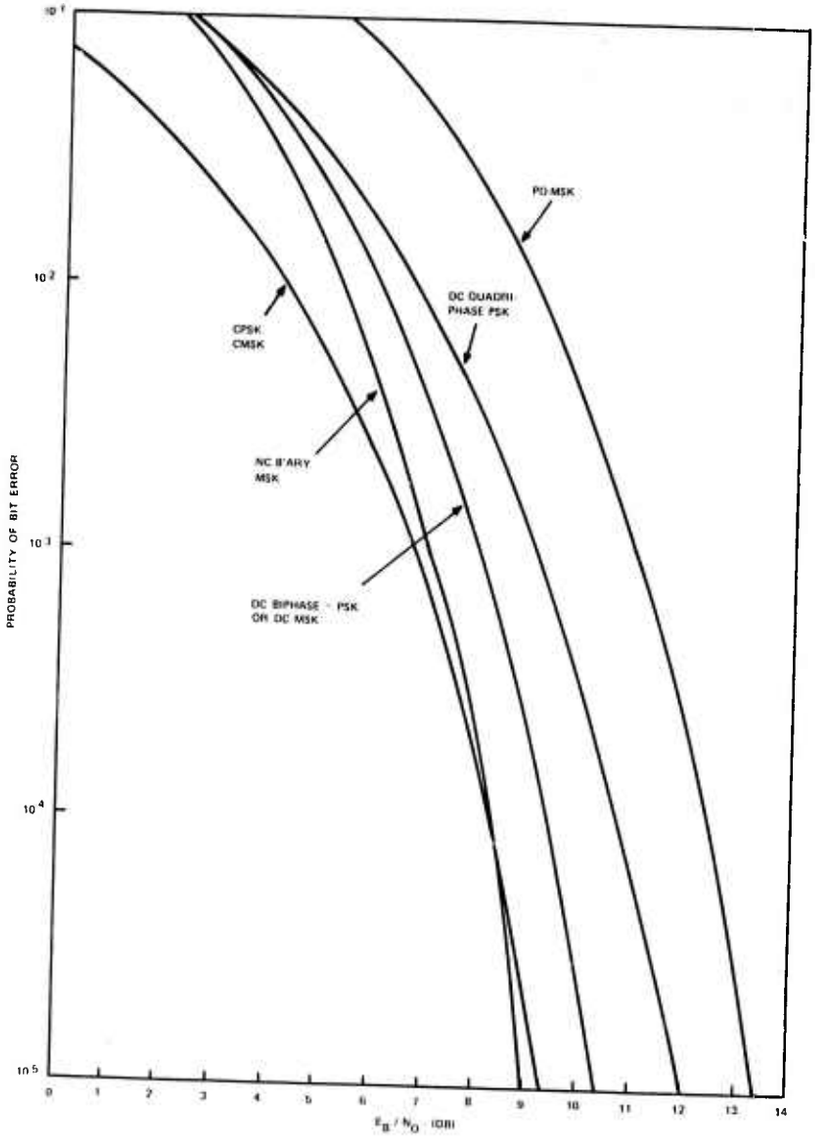


Figure 3-5. Detection Performance Comparison.

A packet is organized into four parts: preamble, header, text and checksum. Each part serves a specific role in the overall transfer process.

3.7.1 Preamble

The first bits of a packet form the preamble. This segment of the packet serves to announce the arrival of a packet and provides the time and the information for the radio system to condition itself to receive the remainder of the packet. During the preamble period, receiver gains are adjusted, bit timing is derived from the incoming signal, and a detector is conditioned to mark the precise end of preamble (EOP). The end of preamble signal serves as a delimiter for handling the packet segments that follow.

The preamble planned for the experimental system contains a maximum of 48 bits. The last 13 bits in this series contain a specific code used to detect the EOP.

3.7.2 Header

The header contains the instructions for the distributed network processor. Fields within the header define how the packet is to be handled at each step in the transfer process. A variable header length is planned for the experimental system. This provides considerable flexibility for experimentation. Fields planned for the header include:

a. Header Plus Text Word Count

b. Header Word Count

c. Packet Type - identifies a packet in terms of the purpose of its text (search, information, acknowledgment, control, etc.)

d. Routing Instructions

e. Terminal Identification

f. Destination Descriptors

3.7.3 Test

This segment of the packet contains the information to be transferred. The text segment is variable in length from 0 to a maximum of 128 sixteen-bit words minus the number of words in the header. The information contained in this segment can be in any form or character set.

The text segment can be used to transfer new parameters or program segments to repeaters during network operation and/or initialization.

3.7.4 Checksum

The header and text are processed through an error coder prior to transfer. The checksum from this encoding process is transferred as the last segment of a packet. Received packets are subjected to the inverse process and discarded (not acknowledged or forwarded) if errors are detected. A 16-bit checksum is planned for the initial implementation.

4.1 GENERAL DESCRIPTION

The function of the repeater in a PR network is that of "packet processor." The resources of the repeater are organized to serve three basic operations: receive a packet, logical testing of packets and transmit packets. Certain of the resources of a repeater (power amplifier, modulator, detectors, error coders, programs, etc.) are dedicated to specific operations, while other resources (central processing unit, memory, antenna, etc.) are shared by two or more of the operational processes. In addition to the operational processes, the repeater has internal control mechanisms that handle the common housekeeping tasks and coordinate between the basic operations.

A conceptual view of the basic organization of a repeater is presented in figure 4-1. The packet transmit and receive processes represent the primary input and output ports of the packet processor. The test operations determine what preprogrammed actions the repeater should take based on the contents of a particular packet. For example, if a packet has detected errors or is not labeled for this particular repeater, it will be discarded. In another case, the packet will be acknowledged, the header data modified per the routing program, and the packet forwarded to the transmit process.

The repeater is organized such that several operations can be underway at the same time. The transmit and receive operations are mutually exclusive since they share common elements in the rf chain, however, the two packets can be received concurrently and the packet testing programs can run at the same time as a transmit or a receive operation.

The experimental repeater has additional operational processes defined that provide flexibility over and above that required for a basic repeater. These processes include:

a. Output to station

b. Input from station

c. Terminal service

The station transfer processes are organized such that they can be executed concurrently with the basic repeater processes, subject only to the available memory restrictions. The terminal input/output (I/O) process does not have direct access to memory and, therefore, does not execute simultaneously with such operations as packet testing.

The hardware and software functions required to direct and accomplish these operations are described in sections 5 and 6 of this document. The following paragraphs of this section describe the logical operation of transmit and receive operations and identify the elements that operate on the packet as it is processed.

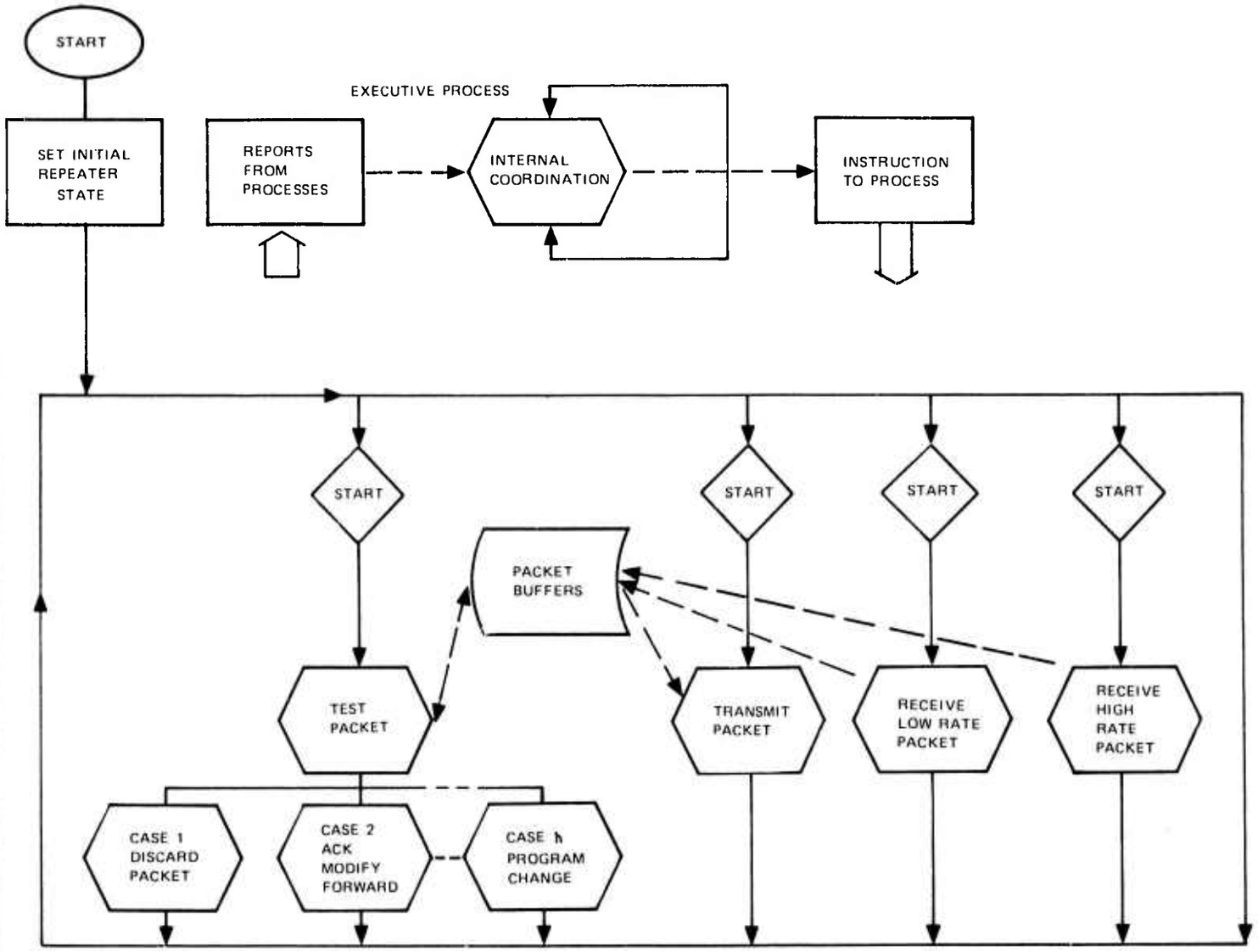


Figure 4-1. Repeater Organization.

4.2 RECEIVE PACKET

The experimental repeater has two receive packet processes: one for high rate (400 Kbps), and a separate process for low rate (100 Kbps), which can be used at the same time. Figure 4-2 outlines the logic of the receive process, and figure 4-3 illustrates the functional elements that operate on the packet as the process executes. The logic and information flow is the same for both the high and low rate process. The difference between the two is the actual implementation of the demodulator circuits.

Receive Packet is enabled by the internal coordination program. Instructions to this process cause its control logic to be reset and an address to be loaded that defines where a received packet will be stored. Following this instruction, the local control logic will set a RECEIVE ENABLE line. The repeater antenna is connected to the rf amplification and filtering

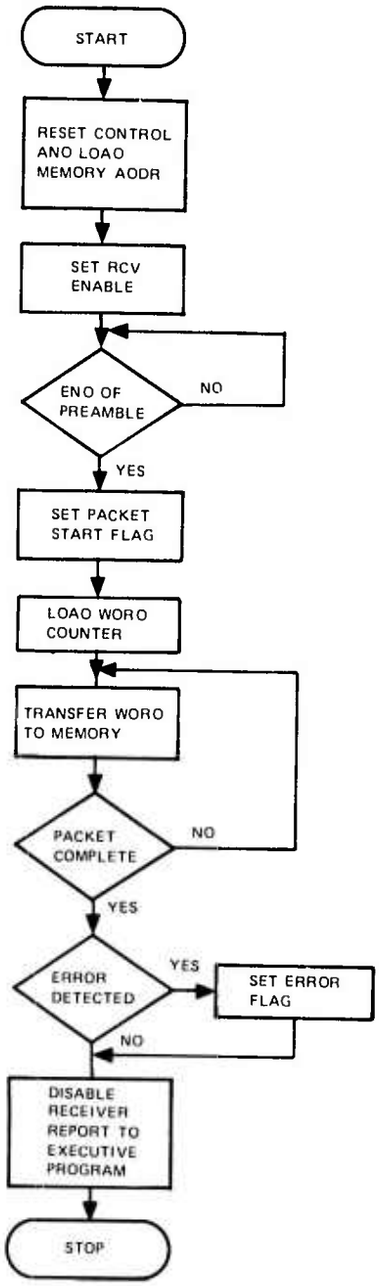


Figure 4-2. Receive Packet Logic.

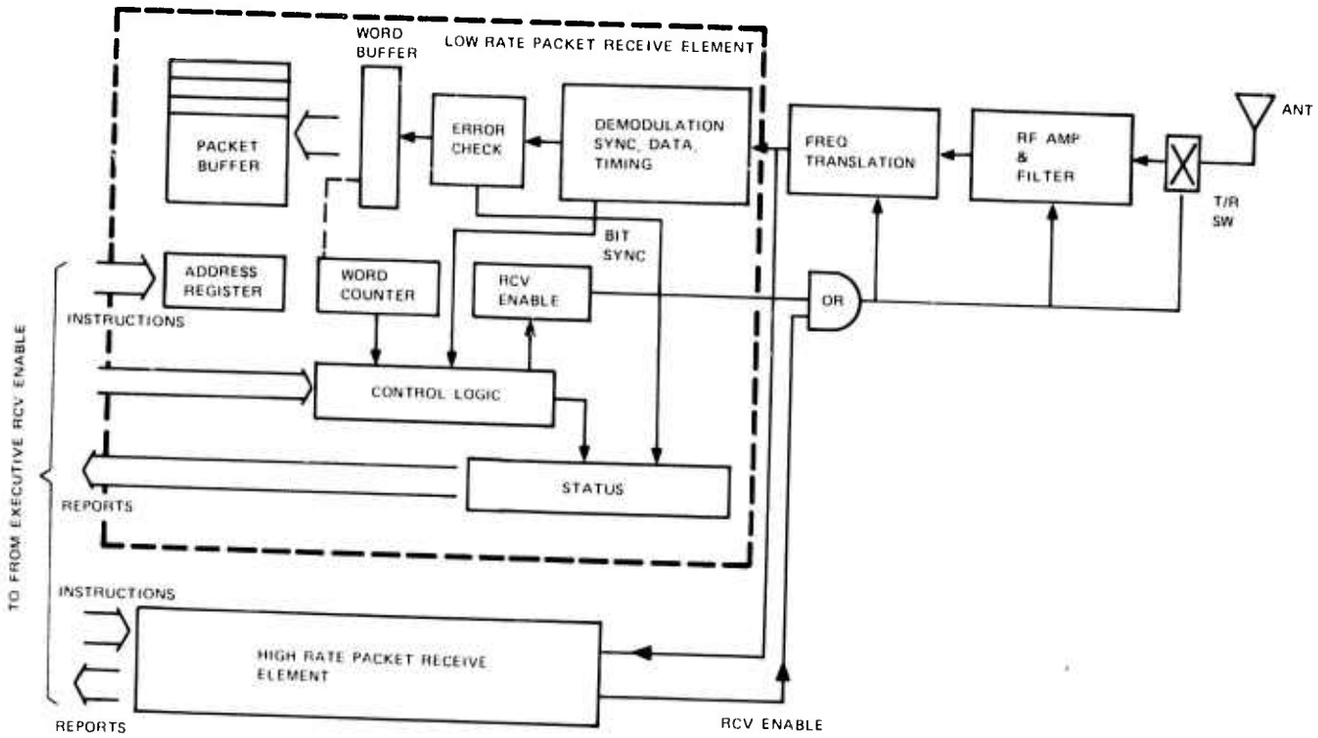


Figure 4-3. Reeeive Packet Information Flow.

elements, the L-band signal is translated to a nominal 70-MHz signal, and the demodulator is eonditioned to seareh for and loek onto a packet preamble. During the preamble seareh by the demodulator, bit timing is derived from the ineoming signal, the gain levels in the receive chain are adjusted and loeked, and the preamble bits are tested in the demodulator to uniquely define the end of the preamble.

When the local control logie receives the end of preamble signal, it initiates several actions. Other processes are informed via a status word that a packet transfer to memory is starting, the packet word counter is loaded from the ineoming data stream, the error cheek decoder is enabled, and a word-by-word transfer of the detected paeket data (to the assigned memory area) is initiated. The word transfers eontinue, under local eontrol, until the number of words stored is equal to the number of words expeeted. Following the last word of the paeket text, the state of the error decoder is tested, and the paeket error flag is set, if appropriate.

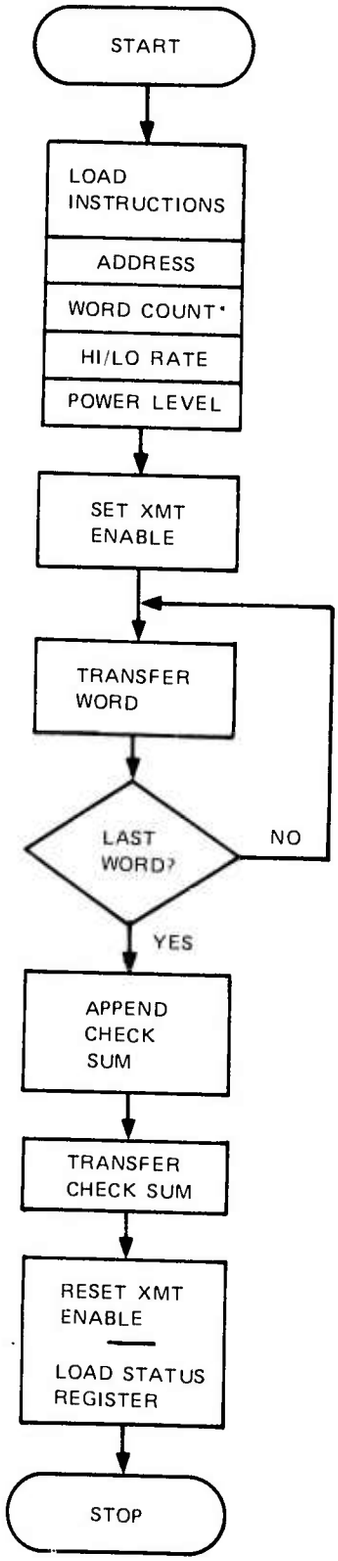
The receive process is now complete. The RECEIVE ENABLE line is reset and status is reported.

4.3 TRANSMIT PACKET

The transmit process logic is outlined in figure 4-4 and the corresponding information flow illustrated in figure 4-5. The process is initiated when instructions are received that specify the location of the packet to be transmitted, the number of words in the packet (including the preamble words for transmit), high or low rate transfer, and the desired power level.

When these instructions have been loaded, the TRANSMIT ENABLE line is set. This action forces the repeater functions into the transmit mode and opens a path from the specified packet buffer to the antenna. Following Transmit Enable, words are transferred from the packet memory to the bit-to-chip encoder via an error coding function. The encoder translates each bit into the appropriate 128-chip coded sequence. The chip sequence is then modulated on a nominal 70-MHz carrier. The signal is translated to L-band, amplified, and radiated.

When the word counter indicates that the last word has been transferred, a checksum from the error encoder is transferred. The packet transmit process is now complete. The enable line is reset and status reported.



* INCLUDES PREAMBLE

Figure 4-4. Transmit Packet Logic.

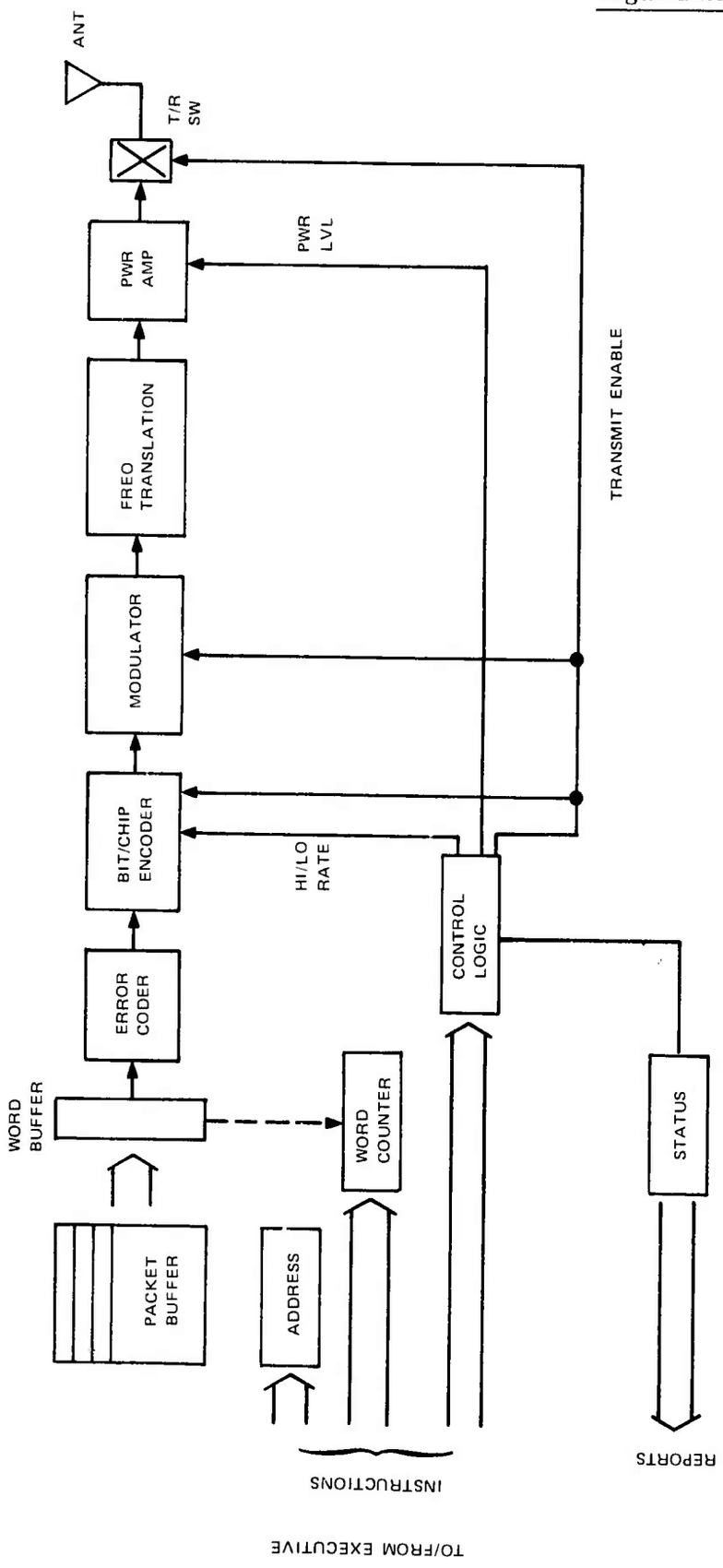


Figure 4-5. Transmit Packet Information Flow.

This section of the equipment plan for the ARPA Experimental Packet Radio Network describes the radio section of the packet repeater. The radio section includes the antenna, rf transmit and receive functions, and signal processing. The primary input and output interfaces to other parts of the repeater are digital interfaces to the processor described in section 6.

A general description of the radio section is given in paragraph 5.1, and detailed descriptions of the various subsystems forming the radio section are given in paragraph 5.2. The radio system described meets the performance objectives summarized in section 3. A radio system performance summary is given in paragraph 5.1.6.

5.1 GENERAL DESCRIPTION

The general description for the radio includes five major sections. Each section addresses major subsystems within the radio section.

A functional block diagram of the radio is depicted in figure 5-1. When in the transmit mode, packets in serial digital form flow from the microprocessor to the encoder/modulator. The encoder chip encodes the bit data and presents the chips to the minimum shift keying (MSK) modulator. The MSK modulator output is then up-converted (double conversion) to rf, where it is amplified to 10 watts minimum. The transmitter output is coupled to the antenna through the transmit/receive (T/R) switch, which also isolates the transmitter from the receiver.

In the receive mode, the T/R switch allows receive rf signals from the antenna to flow to the down-converter section. The down-converter (double conversion) output is signal processed and demodulated for serial bit data transmission to the microprocessor.

The system provides facilities for operation at data rates of 100 and 400 Kbps. The rf and if portions of the receiver are common for the two data rates up to the output of the noncoherent automatic gain control (agc). The signal is split at the output of the noncoherent agc, and beyond this point independent circuits are used for each of the two data rates.

5.1.1 Transmitter

A functional block diagram of the transmitter and receiver is shown in figure 5-1. The transmitter functions include the encoder/modulator, up-converter, power amplifier, T/R switch, and antenna.

The frequency generation and control/monitor logic is common to both transmit and receive functions, and the antenna is time shared between transmit and receive by means of the T/R switch.

The transmitter accepts a data packet (including preamble and header) in serial bit form from the microprocessor, chip encodes the bits with the spread spectrum code, converts this digital chip signal to constant envelope phase modulation MSK, up-converts to rf output

frequency, amplifies to 10 watts minimum, filters the up-converted signal, and couples the signal to the antenna, which radiates the packet radio signal.

Power dissipation in the transmitter is minimized by turning off power to transmitter functions when not transmitting.

5.1.2 Receiver

Receiver functions include rf preamplification, down-conversion, signal gain control (includes both noncoherent and coherent age), matched filter signal detection (surface acoustic wave devices, SWAD's), preamble detection, bit sync acquisition, and data detection. These receiver functions are shown in figure 5-1.

A matched filter is used to decode and demodulate at each bit rate. Dual rate detection is accomplished by using independent signal processing circuits for each rate following the first age stage (noncoherent age). Low rate (100 Kbps) is intended for terminal/repeater traffic, while high data rate (400 Kbps) is used for repeater/repeater traffic.

Higher rates are permissible on repeater to repeater links because of the higher gain of the repeater antennas and operation over unobstructed paths. Multipath effects are also expected to be minimum on repeater to repeater links, allowing operation at higher data rates.

The design will also provide for simultaneous operation of multiple detectors at each data rate, although the first systems delivered will be equipped with only one detector at each rate. Simultaneous reception of two or more signals is possible by operating each detector in a time gated mode. This is possible with the spread spectrum system since the correlation peak duration is much smaller than the bit period.

Terminals and repeaters communicating with a repeater are received in random clock phase, but clock frequency is sufficiently precise relative to the packet duration that the relative time positions between the correlation peaks of two received signals does not vary significantly over the duration of the packet. The effectiveness of this technique will depend on the extent to which multipath is absent and the degree to which transmit power control maintains a relatively constant receiver power level at the repeater independent of path length. The use of multiple detectors does not depend upon precise network synchronization, but rather, depends upon the statistics of random packet transmission.

The preamble (which does not include header of text) is organized to perform three basic functions in the receiver:

a. Automatic gain control (age) for receiver amplifiers to normalize rf signal levels for signal processing and detection circuits.

b. Bit rate acquisition and synchronization.

c. End of preamble (EOP) detection and start of text data to the microprocessor.

A total of 48 bits of preamble are used. The preamble format is shown in figure 5-2.

The last 13 bits are used for EOP detection. The method chosen for EOP detection (described in the design description section) is based primarily on ease of implementation and lowest power consumption consistent with high performance rather than use of shortest possible preamble.

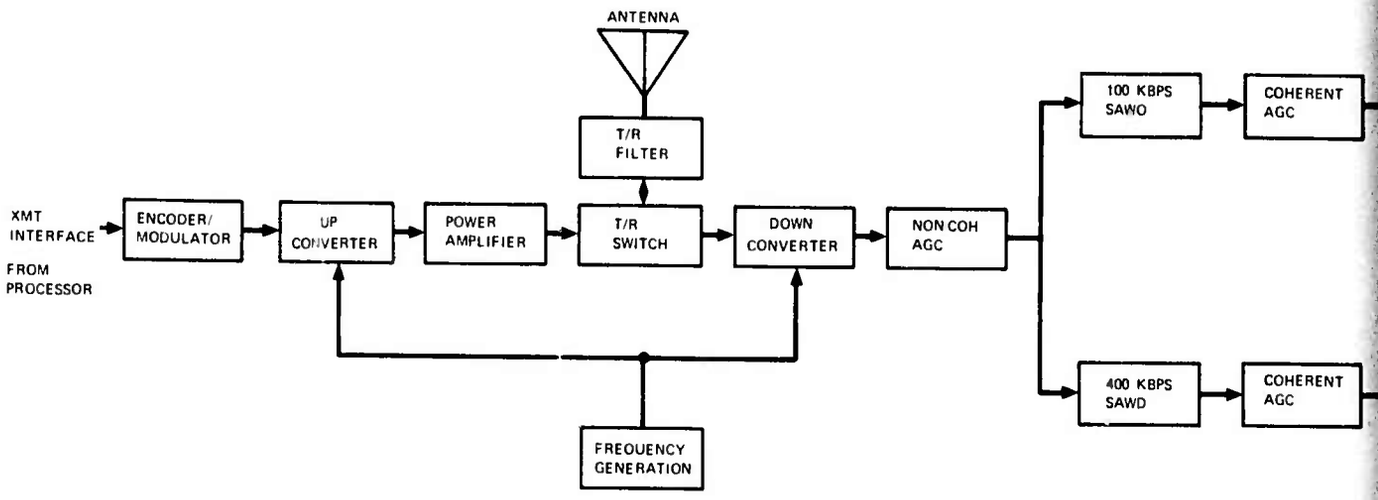

ANTENNA
T/R FILTER
XMT INTERFACE
FROM PROCESSOR
ENCODER/ MODULATOR
UP CONVERTER
POWER AMPLIFIER
T/R SWITCH
DOWN CONVERTER
NON COH AGC
100 KBPS SAWO
COHERENT AGC
400 KBPS SAWD
COHERENT AGC
FREQUENCY GENERATION

Figure 5-1.

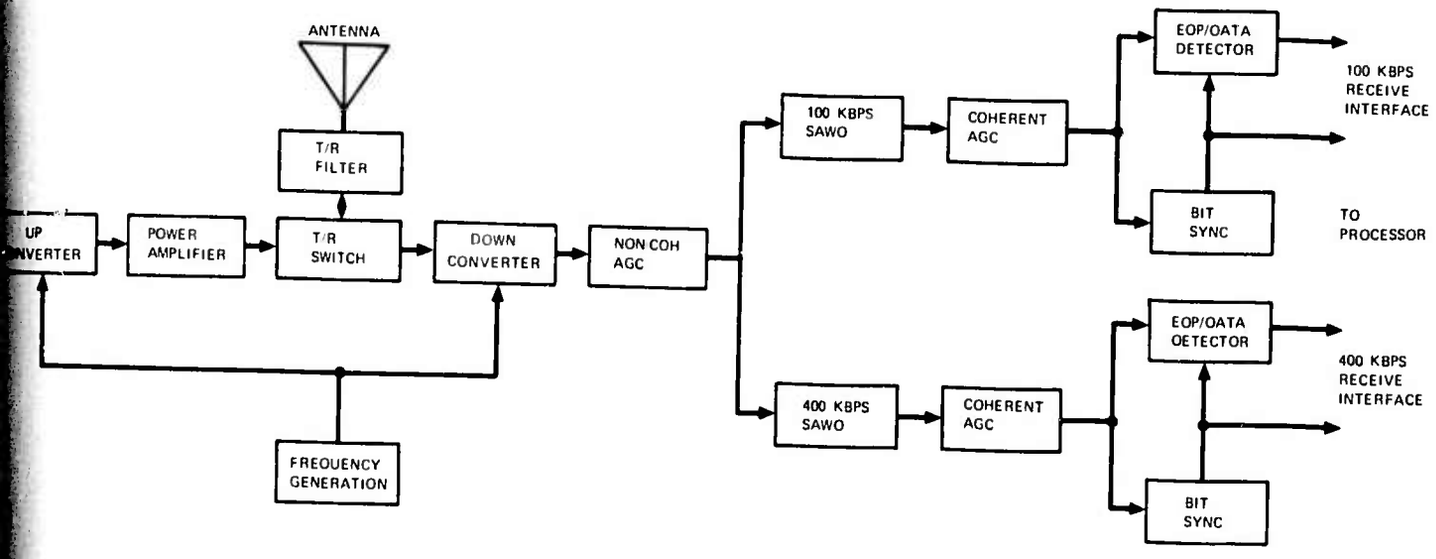


Figure 5-1. Packet Radio Functional Diagram.

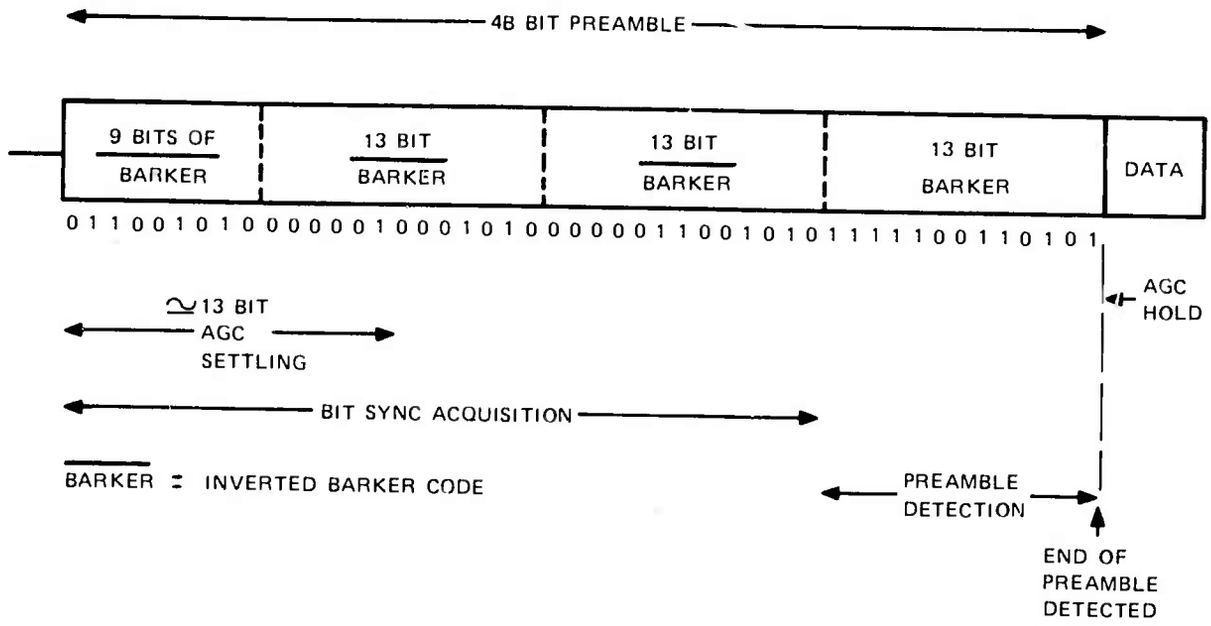


Figure 5-2. Preamble Organization.

Bit synchronization must be achieved prior to the last 13 bits of the preamble: hence, bit synchronization must be acquired within 35 bits from the start of the preamble. The coherent age requires 13 bits for stablization. Bit synchronization is achieved by conventional phase-lock loop methods with added techniques to reject multipath components. Preamble is generated by a 9-bit truncated Barker sequence followed by three 13-bit Barker sequences, transmitted sequentially by $\overline{\text{Barker}}$, $\overline{\text{Barker}}$, $\overline{\text{Barker}}$, Barker for 48 bits total. Preamble is generated in microprocessor software. Figure 5-2 shows the preamble organization and radio operations that occur.

5.1.3 Frequency Generation

The frequency generation equipment generates two types of signals: one is the local oscillator (LO) frequency generation for up-converter/down-converter use, the other is stable clock signals for chip and bit timing.

If SAWD's were of sufficient accuracy, only one frequency standard would be required for both frequency generation requirements: however, since SAWD's cannot be built to absolute frequency requirements in the time frame for the experimental packet radio initial development, different frequency standards are used to derive the local oscillator and clock signals. The first local oscillator may be adjusted to provide a ±20-KHz variation in the if center frequency to correct for the SAWD frequency tolerance.

The first LO generator employs a synthesizer with 6.4-MHz steps that is separate from the second LO injection and chip/bit frequency generation. Each has a stable frequency standard. When SAWD technology progresses to where absolute frequency requirements are feasible, one frequency standard may be eliminated from the frequency generation equipment.

5.1.4 Performance Specification Summary for Radio Plan

Frequency Band	50-MHz bandwidth, tunable in 1710- to 1850-MHz band
Frequency Channel Spacing	6.4-MHz steps, 20 steps, 1718.7155 to 1840.3155 MHz
Transmitter Power Output	10 watts typical at antenna, 20-dB power control in four steps
Transmitter Spurious Output	≥ 50 dB below desired output, 20-MHz bandwidth, not including modulation sidebands
Antenna	Colinear array with 9-dBi gain (repeater, station only)
Modulation	Code (pseudonoise) spread spectrum
Chip Modulation	MSK (minimum shift keying)
Occupied Bandwidth	20 MHz for 99.5-percent transmitter energy
Bit Modulation	Differentially coherent
Chip Rate	12.8 megachip per second (Mcps)
Bit Rates (Dual)	100 Kbps at low rate - terminal/repeater traffic 128 spread factor: 400 Kbps at high rate - repeater/repeater traffic, 32 spread factor
Receiver Processing Gain	+21 dB at 100 Kbps +15 dB at 400 Kbps
Receiver Signal Level	-106 dBm to 0 dBm (linear to -20 dBm) at 100 Kbps -100 dBm to 0 dBm (linear to -20 dBm) at 400 Kbps
Noise Figure	≤ 8 dB
Receiver Noise Bandwidth	20 MHz determined by if 6-pole Butterworth filter or equivalent
Interference Levels	In-band interferers (±10 MHz of carrier) ≤ 10 dB above signal provided that level is in linear range of receiver
Receiver Spurious Rejection	
Transmit/receive filter:	4-pole Chebyshev filter, BW = 50 MHz, mechanically tunable over 1710 to 1850 MHz band
Image rejection:	≥ 80 dB

Aecess	Random access
Range	Terminal/repeater - 1.4 mile for 99-pereent of detection in an urban environment. 5 miles for 50-pereent detection in a rural flat environment with a 45-meter antenna height. Repeater/repeater Line-of-sight for up to 32 miles (radio horizon)
BER Performance	$P_e \leq 10^{-5}$
Pseudonoise Spread Factor	128 chips/bit at low rate 32 chips/bit at high rate
Coding	64 ehips/MSK subchannel at low rate 16 chips/MSK subchannel at high rate
Preamble	Length - 48 bits 9-bit Barker inverted code plus two 13-bit inverted Barker codes, followed by 13-bit Barker eode
Preamble Detection	Probability - 0.999 design goal Probability of false alarm - 10^{-6}

5.1.5 Modem/Microprocessor Interface

See paragraph 5.1.6 for a complete description of this interface. The listing of individual funetion/wires and their purpose follows.

Tx Enable	a. Switches T/R switch to transmit (normally in receive mode). b. Turns power on to transmitter funetions (bit rate generator, ehip encoder, modulator. up-converters. power amplifiers). c. Monitors error eonditions before transmitting.
Tx Hi/Lo Data Rate	a. Signal from mieroproeessor defining which bit rate/ehip code to be transmitted. b. Signal must oceur with or before Tx Enable.
Tx Bit Rate	a. 100-Kbps or 400-Kbps square wave from radio rate selected by hi/lo control line.
Tx Cloek Rate	Same signal as Tx Bit Rate, but turned around by microproeessor. This allows eorreetion for time delay due to distanee between radio and miero-processor.
Tx Data	a. Data synehronous with Tx Cloek Rate. b. Data ineludes preamble.

Tx Power Control (3 bits)	Controls amount of attenuation below transmitter full power.
Frequency Control (6 bits)	Selects transmit frequency.
Rev Enable*	Enables age functions, bit synchronization, and EOP detection.
Rev End of Preamble*	Denotes EOP and start of receive data to microprocessor.
Rev Data*	Receive data following EOP. Data synchronous with bit clock.
Rev Bit Clock*	Bit clock at applicable bit rate.
Carrier Sense	Bit sync in-lock indication

5.1.6 Definition and Value of Terms

$_{L}R_{B}$	=	100.106 kHz	Low bit rate
$_{H}R_{B}$	=	400.424 kHz	High bit rate
$_{L}T_{B}$	=	$1/_{L}R_{B}$ = 9.9894 μs	Low bit period
$_{H}T_{B}$	=	$1/_{H}R_{B}$ = 2.49735 μs	High bit period
R_c	=	12.813568 MHz	Chip Rate
T_c	=	$1/R_c$ = 78.04 μs	Chip period
$_{L}N_{C}$	=	128	Chips/bit at low rate
$_{H}N_{C}$	=	32	Chips/bit at high rate
$2^{F}IF$	=	5 1/4 R_c = 67.271232 MHz	Second if
$2^{F}LO$	=	18 R_c = 230.64422 MHz	Second LO injection
$1^{F}IF$	=	23 1/4 R_c = 297.91545 MHz	First if
$1^{F}LO$	=	N. $R_c/2$ = 1420.8 through 1542.4	First LO injection (adjustable to correct for SAWD frequency offset)
F_0	=	$1^{F}LO + 1^{R}IF$ = 1718.7155 through 1840.3155	RF center frequency
F_O	=	6.40000 MHz	Channel steps at rf
1111100110101			13-bit Barker code

*Each multiple detector has an independent signal line. Carrier sense of all multiple detectors are wire-ORed together.

5.2 DESIGN DESCRIPTION

Each of the functional elements comprising the radio section, shown in figure 5-1, is discussed in further detail in this subsection of the report. In each, the functional element is briefly discussed and its interface defined.

5.2.1 Encoder/Modulator

a. Functional Description. The encoder accepts preamble, header, and packet data from the microprocessor interface, and chip codes the packet for code spread spectrum. The modulator accepts the coded packet in digital chip form and MSK modulates at the radio intermediate frequency. Refer to figure 5-3.

b. Functional Interfaces.

Tx Enable	COS-MOS logic level from microprocessor that enables encoder/modulator functions.
Hi/Lo Rate	COS-MOS logic level from microprocessor defining which data rate to transmit.
Bit Rate Clock	Either 100-Kbps or 400-Kbps square-wave, selected by Tx Hi/Lo Rate control line.
Tx Clock	Tx Bit Rate turned around by microprocessor. This accounts for time delays due to distance between radio and microprocessor.

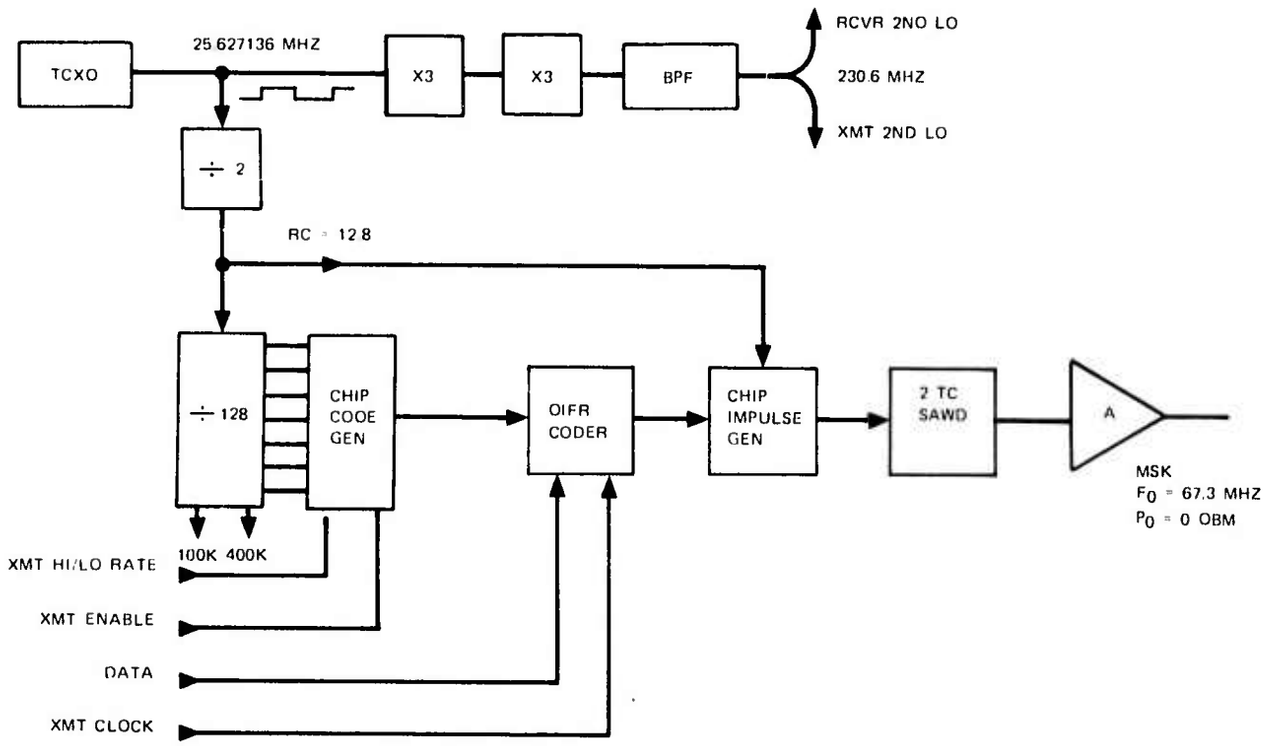


Figure 5-3. Encoder/Modulator.

Tx Data	COS-MOS logic level data from microprocessor.
MSK Output	f_o = 67.271 (±0.020) MHz (matched within ±0.003 MHz of receiver).
	P_o= 0 dBm, 50 ohms.

c. Operational Description. A functional block diagram of the dual rate encoder and modulator is shown in figure 5-3. Tx Enable applies power to the dividers operating off the 25.6-MHz TCXO, the chip coder, modulator, and other transmit functions such as upconverters and power amplifiers. Turn-on time is less than 1 bit period. The first bit transmitted may be garbled, but this is of no importance since the receiver utilizes the first few bits for adjustment of the noncoherent age and also requires 1 bit to set up differentially coherent encoding and detection.

Upon turn-on, the bit rate clocks of 100 Kbps and 400 Kbps are generated. If no faults are present in the radio (such as synthesizer out of lock), the selected rate (determined by Tx Hi/Lo Rate) is sent to the microprocessor.

Data and timing from the microprocessor are processed through the interface logic section. This section resynchronizes the data/timing from the microprocessor (which may be removed up to 1000 feet from the radio section or 3-μs delay) to the local bit timing.

Data is then differentially coherent encoded by the following algorithm, where superscript N is the present interval of time, and C is code to be transmitted.

Data^N	Code^{N+1}
0	C^N
1	$\overline{C^N}$

The code is stored in a high-speed read only memory (ROM) that is accessed by using the binary counter states to address the stored bits. Another input state is Hi/Lo Rate: 128 address bits from the counter are used to generate the 128-chip code in the low rate mode, while four consecutive 32-chip codes are generated per cycle of the counter, which correspond to 4 bit intervals at the high rate.

The counter and ROM must of necessity be fast to accomplish their function of generating chips in 1-chip intervals of 78 nanoseconds. (Figure 5-4 depicts the code spread format.) Hence, high-speed dividers and ROM are used: but these are only used in transmit mode, and power is removed when in the receive mode.

The chip code generator produces a pattern of positive and negative pulses corresponding to the chosen chip code. The input data is differentially coded and applied to the code control logic so that a code inversion between adjacent code patterns is transmitted as data "1" and no inversion is transmitted as data "0".

The impulses are applied to a SAWD filter. The impulse response of the SAWD is a cosine envelope of 2-chip-period ($2T_c$) length. The SAWD is impulsed every T_c period, so every impulse starts a cosine wave at 0, while the previous chip cosine wave is at a peak. Quadrature relationship of carrier at each T_c period is achieved by using an odd multiple of 1/4 cycles of center frequency chip frequency (five-1/4 cycles per chip). The resultant waveform is MSK, as shown in figure 5-5, and is seen to be a constant envelope signal. Every other chip is designated in-phase components, while quadrature

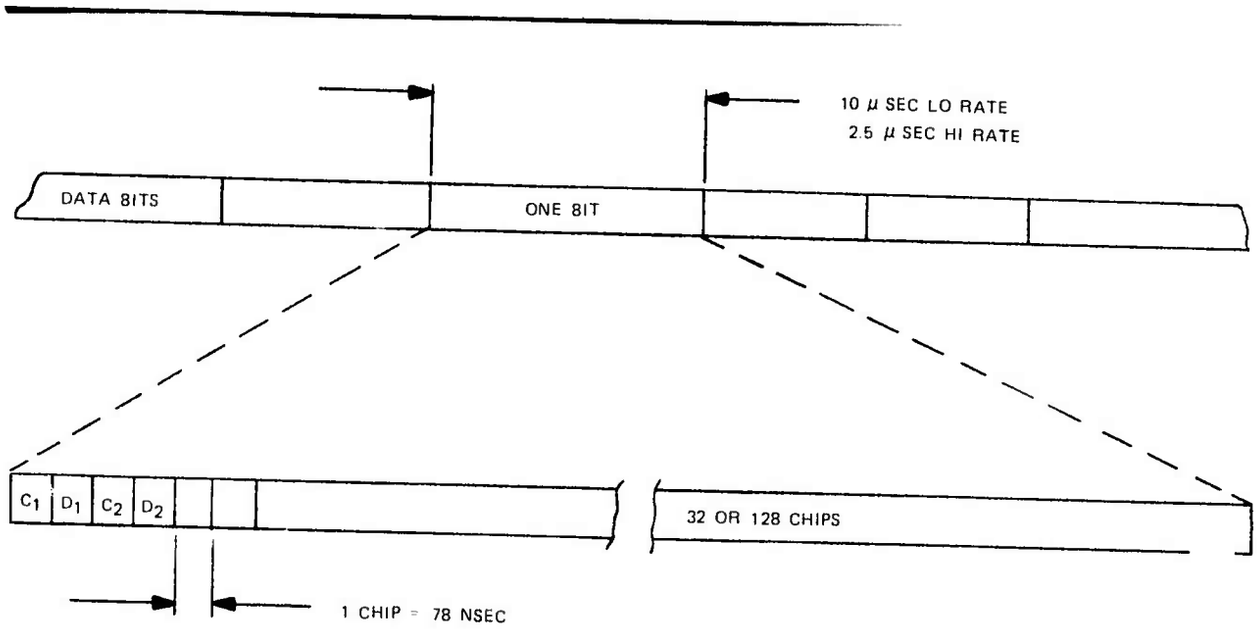


Figure 5-4. Code Spread Format.

components are alternately spaced. As a result of chip data shown, phase change is a ramp (see figure 5-5) with 90-degree transitions occurring through each chip period T_c. rather than a square wave as in PSK. Frequency shift keying (FSK) properties of $F = R_c/4$ are also shown.

The SAWD modulator output is then amplified to a suitable level for use in the up-converter.

5.2.2 Up-Converters

a. Functional Description. The up-converter is shown functionally in figure 5-6. It converts the 67-MHz if to the desired rf frequency. This is accomplished by mixing the if with a 230-MHz LO to produce 297 MHz and mixing this with a synthesizer-stepped LO to produce the rf frequeney. The resultant rf output is filtered, amplified, and applied to the input of the power amplifier.

It should be noted that even though the output waveform appears as a constant amplitude frequency signal, it is the sum of two biphase signals in quadrature and data may be recovered by coherent or differentially coherent PSK techniques.

b. Functional Interfaces.

IF Input

$2^{F_{IF}} = 67.27$ MHz

BW $\simeq$ 20 MHz

$p^{IF} \simeq 0$ dBm

LO Inputs

$2F_{LO}$ = 230.6 MHz

$1F_{LO}$ = 1420.8 to 1542.4 MHz

ΔF_{LO} = 6.4 MHz

$P_{LO} \simeq$ +7 (±3) dBm

RF Output

F_O = 1718.7155 to 1840.3155 MHz

ΔF_O = 6.4 MHz

P_O = 0 dBm

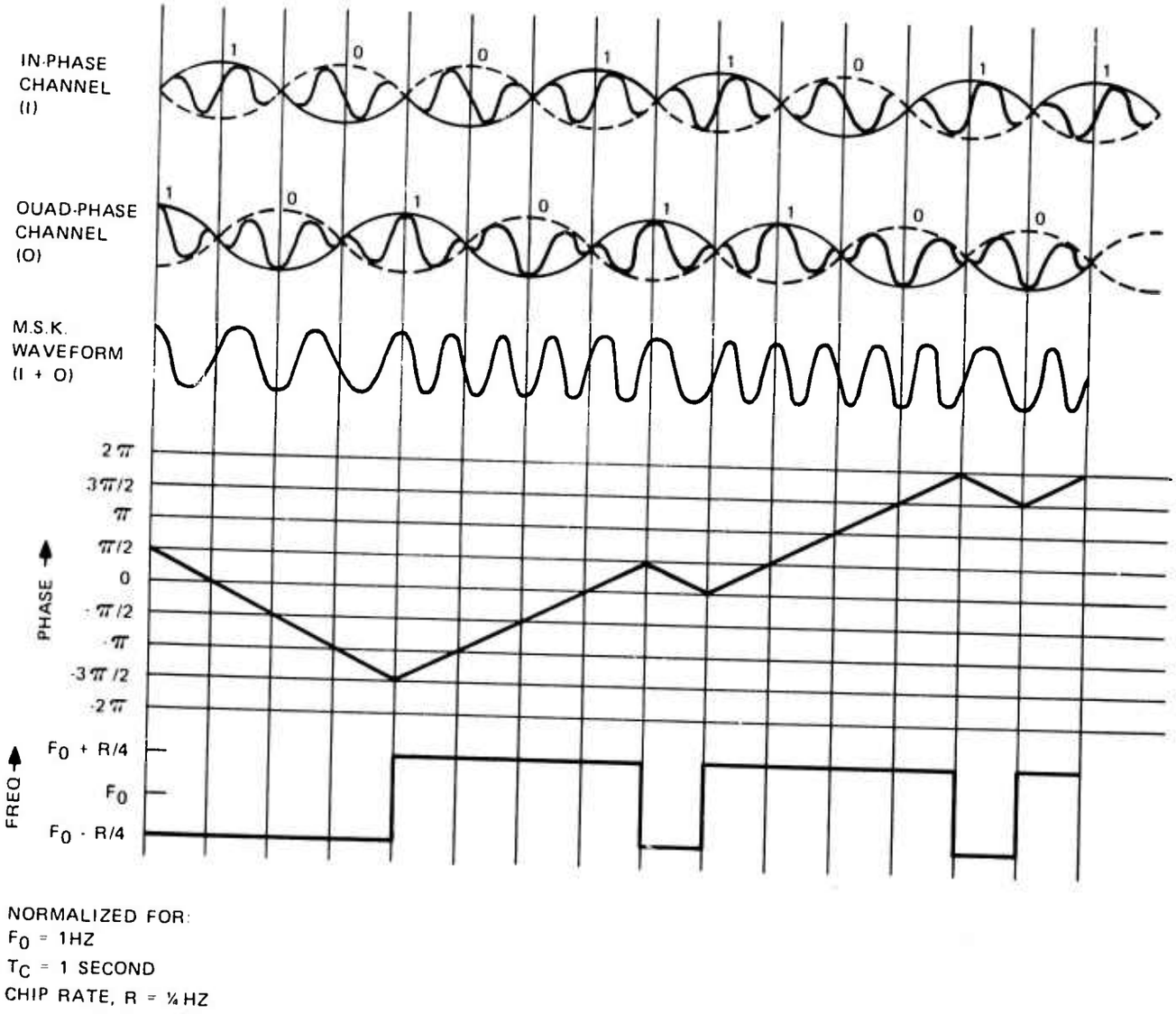


Figure 5-5. Waveforms, Example of Minimum Shift Keyed (MSK) Constant Amplitude Data Signal.

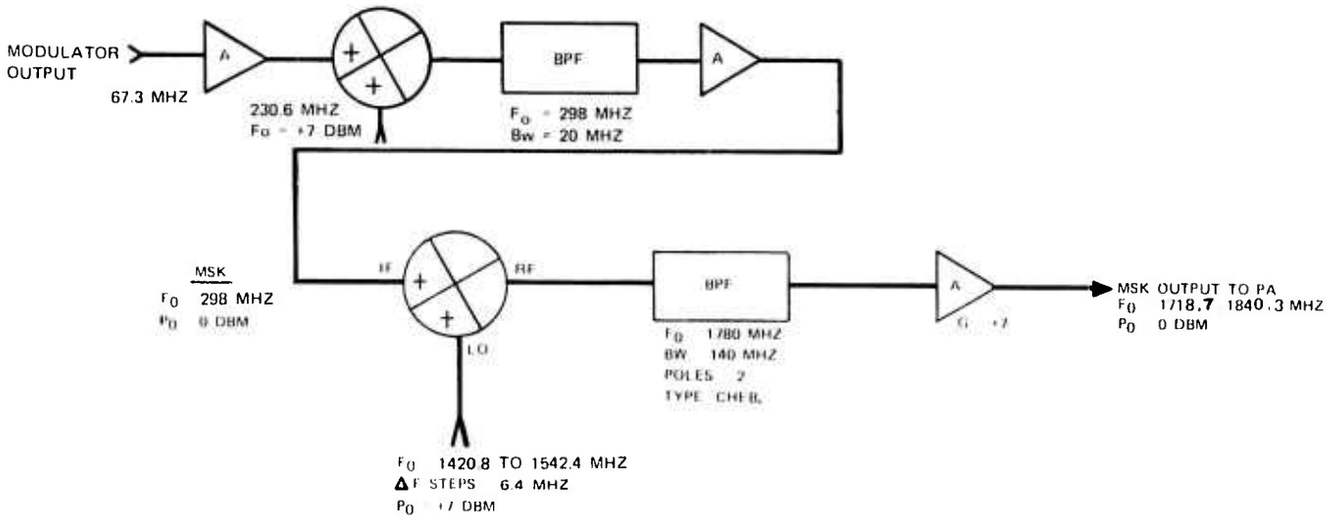


Figure 5-6. Up-Converter.

e. Operational Description. The functional diagram of the double conversion up-converter is shown in figure 5-6. Doubly balaneed mixers are used to minimize undesired mixer produets. The LO and intermediate frequencies are chosen so that even-order produets whieh fall in band are 4th order and higher in the first conversion, and 6th order and higher in the second. Mixers used are well balanced (50 dB) to reduce even-order products. Odd-order products are well out of band where they can easily be filtered by the bandpass filter shown.

The first conversion is physically part of the rf subsystem, which is described in the following paragraph.

5.2.3 Power Amplifier and Power Control

a. Functional Deseription. A functional diagram of the power amplifier and power control is shown in figure 5-7. The rf input is from the up-converter, and the output is conneeted to the antenna through the transmit/reeeive (T/R) switch. To minimize dc power drain, the class A preamplifier stage is switched ON only when transmitting.

Four control lines operate attenuators before and after the power amplifier (PA). Redueing the drive to the PA not only reduees output power, but also dc input power. The power eontrol is used to minimize mutual interference with other network elements by radiating only sufficient power to aehieve reliable communication over any particular path.

The PA and power eontrol circuits are combined with an up-converter stage, T/R switch, rf preamplifier, and first down-eonverter in hybrid microelectronic form. A functional block diagram of the rf subsystem is shown in figure 5-8.

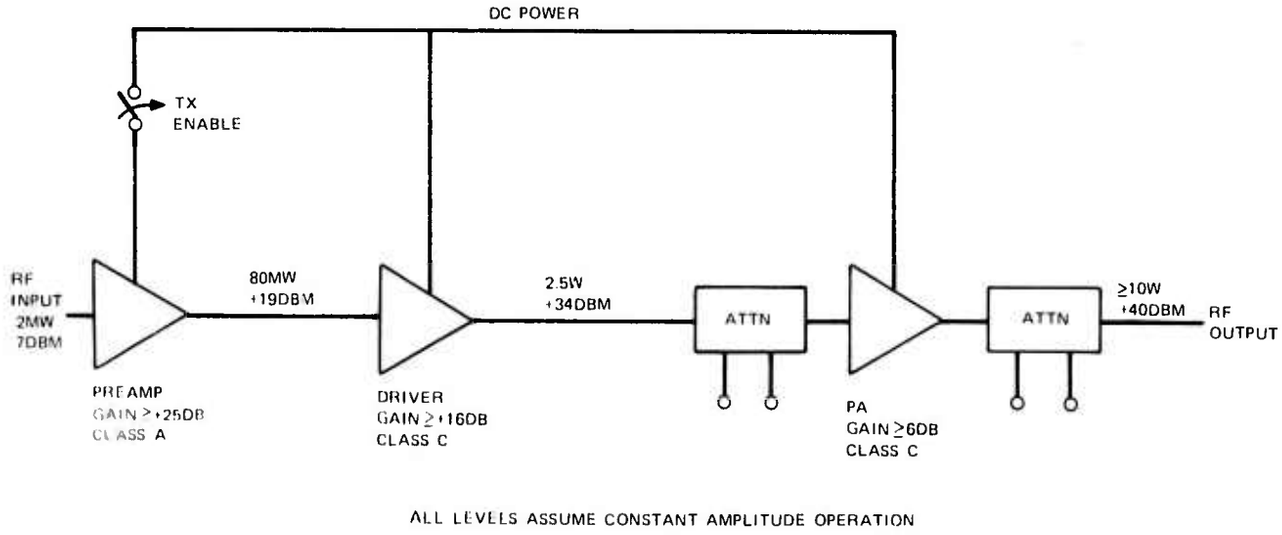


Figure 5-7. Power Amplifier and Power Control.

b. Funetional Interfaee.

Frequeney	1710 to 1850 MHz
Bandwidth ±1 dB	140 MHz
Gain	≥ 40 dB
Output Power	≥10 W
Input VSWR	≤ 1.5:1
Load VSWR	≤1.2:1
Input RF Power	≥0.2 MW
Input DC Power	33 W maximum target for eontinuous operation
Supply Voltage	24V ±0.05 RF output power redueed if 24 vdc voltage is redueed
Noise Output	-172 dBm/Hz (quieseent)
RF Power Control	20 dB minimum range in four steps
Component Junetion Temp.	≤150° C

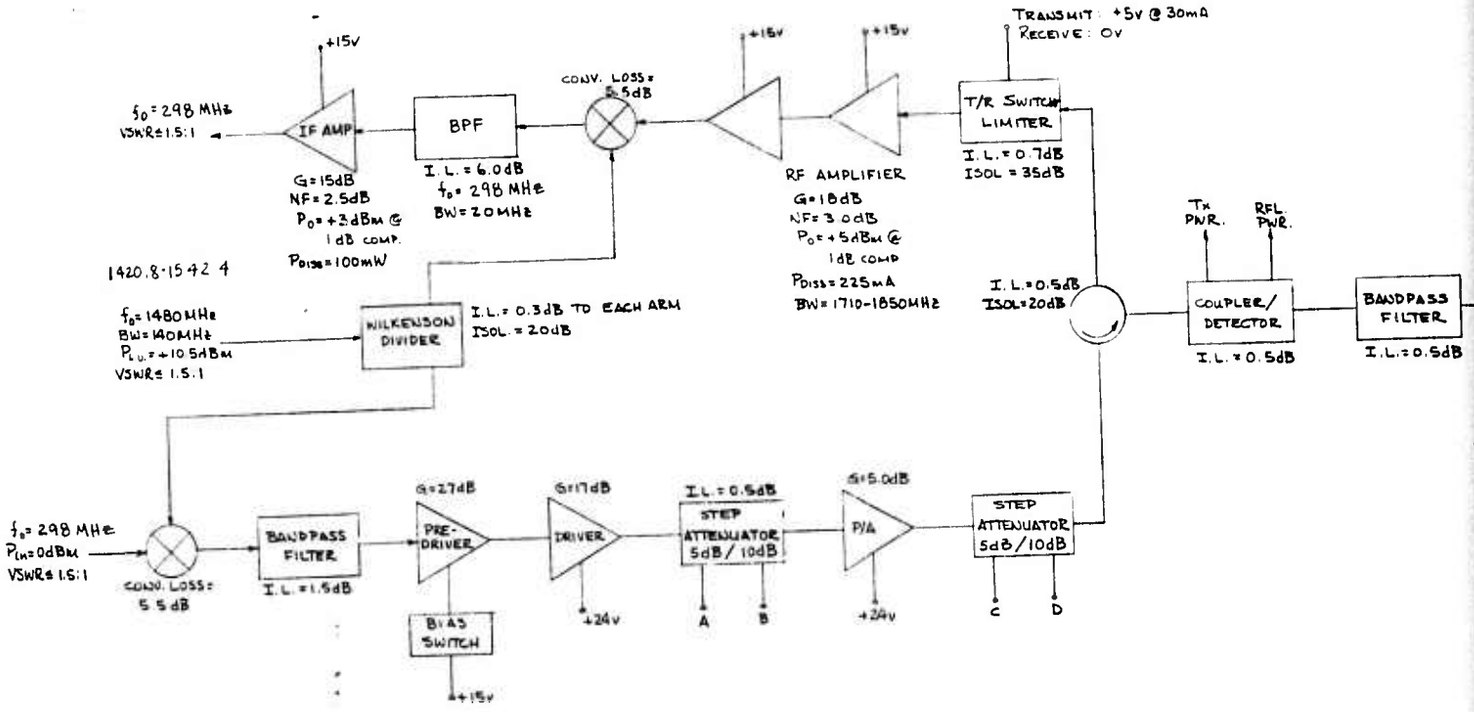


Figure 5-8. RF Subsystem.

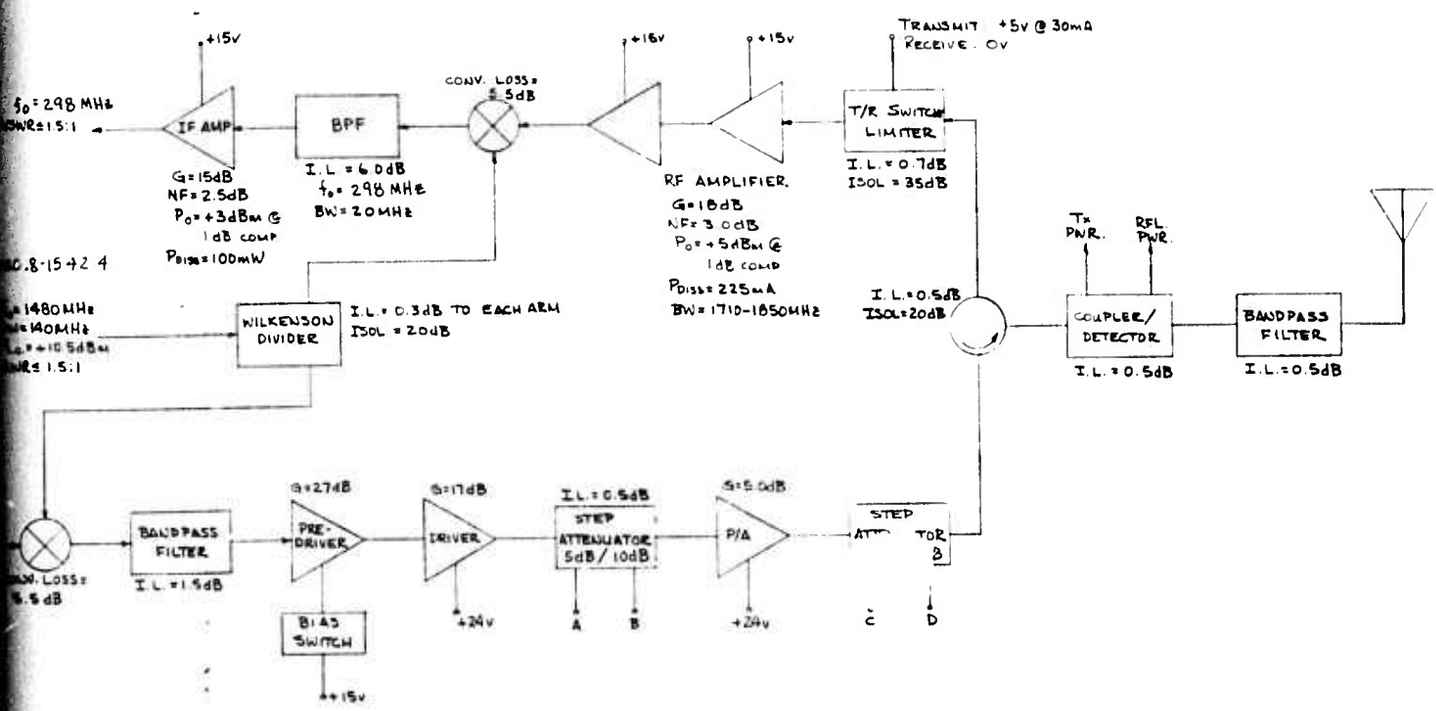


Figure 5-8. RF Subsystem.

5.2.4 T/R Switch

a. Functional Description. A functional diagram of the T/R switch assembly is shown in figure 5-9. In the transmit mode, the PA output is coupled through the circulator to the forward and reflected power monitor. If there is no reflected power from the antenna system, the circulator provides isolation between the transmitter and receiver. Since there is the potential of reflected power, a switched termination is provided at the receive port of the circulator while in the transmit mode to absorb reflected power, thus protecting both the receiver and the solid-state PA from damage. In the receive mode, the transmitter is inhibited and the switch allows a minimum attenuation path to the receiver down-converter. The forward and reflected power monitor indication are for maintenance and in-service monitoring.

b. Performance Summary.

Frequency	1710 to 1850 MHz
Bandwidth (±1 dB)	140 MHz
Insertion Loss	
RCV Mode	≤1.7 dB
XMT Mode	≤1.0 dB

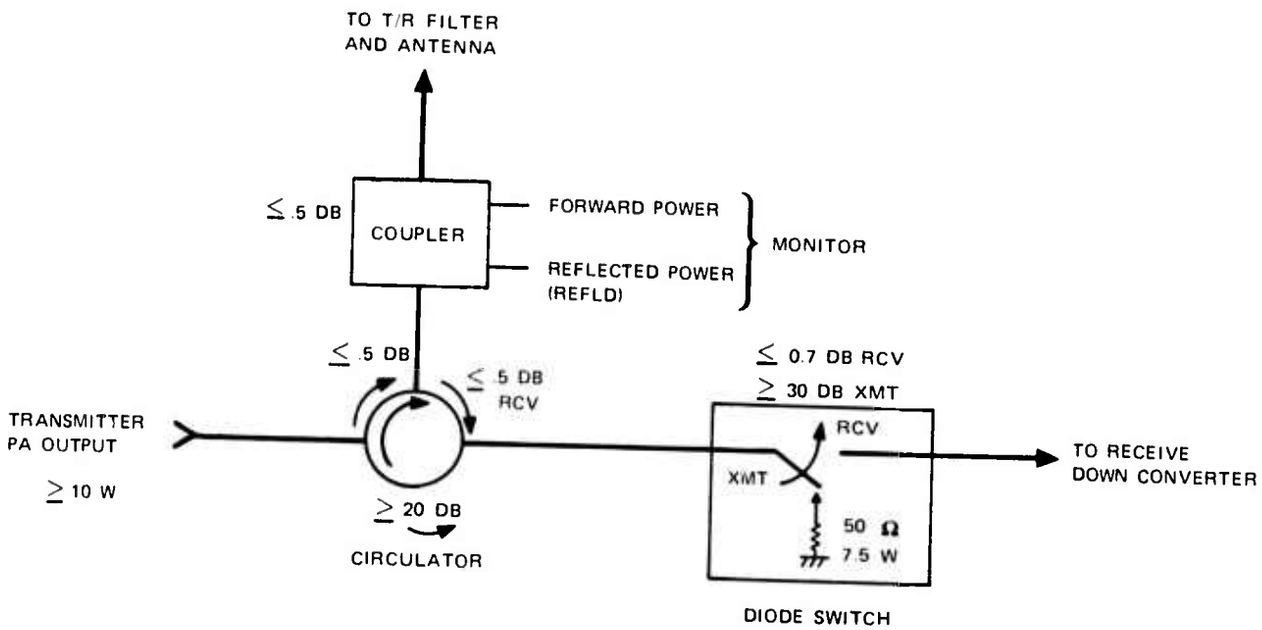


Figure 5-9. T/R Switch.

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Transmitter Receiver Isolation	≥35 dB
Reflected Power Termination	50 ohms, 7.5 W
VSWR All Ports	≤1.2:1
Receiver Limit	+10 dB nominal

5.2.5 T/R Filter

a. Functional Description. The purpose of the T/R filter is twofold. One purpose is to eliminate out-of-band spurious signals when transmitting. The second is signal rejection to the receiver from unwanted signals seen by the antenna.

To meet these requirements, a 4-pole Chebyshev filter is used.

b. Functional Interface.

Frequency Passband	50 MHz, tunable to any center frequency in 1710- to 1850-MHz band
Insertion Loss	≤0.6 dB
Phase Linearity	+15 degrees over any 20-MHz bandwidth
Impedance	50 ohms
VSWR	≤1.2:1
Out-of-Band Rejection	4-pole Chebyshev filter characteristics
Image Rejection	1100 to 1250 MHz: 80 dB
Transmit Power Level	>12 W maximum
Type of Design	A tunable cavity filter
Power Dissipation	Depending upon insertion loss, up to 1 W of forward power

c. Operational Description. The primary requirement for the T/R filter is receiver out-of-band signal rejection, particularly image frequencies. Secondary consideration is transmit up-converter spurious attenuation.

Image rejection of 80 dB is desirable. For down-conversion to 298 MHz, the image frequencies for low side LO injection is approximately 1100 to 1250 MHz. A filter attenuation curve for a 4-pole 0.05-dB ripple Chebyshev filter centered at 1780 MHz is shown in figure 5-10. Also shown in this figure is the response of the 140-MHz bandwidth filter employed at the up-converter output.

Image rejection is seen to be 80 to 90 dB at the image frequencies shown. The transmit LO is attenuated by both a 2-pole (in the up-converter) and a 4-pole T/R filter. Total filter attenuation of the LO signal between the down-converter and antenna is 75 to 95 dB

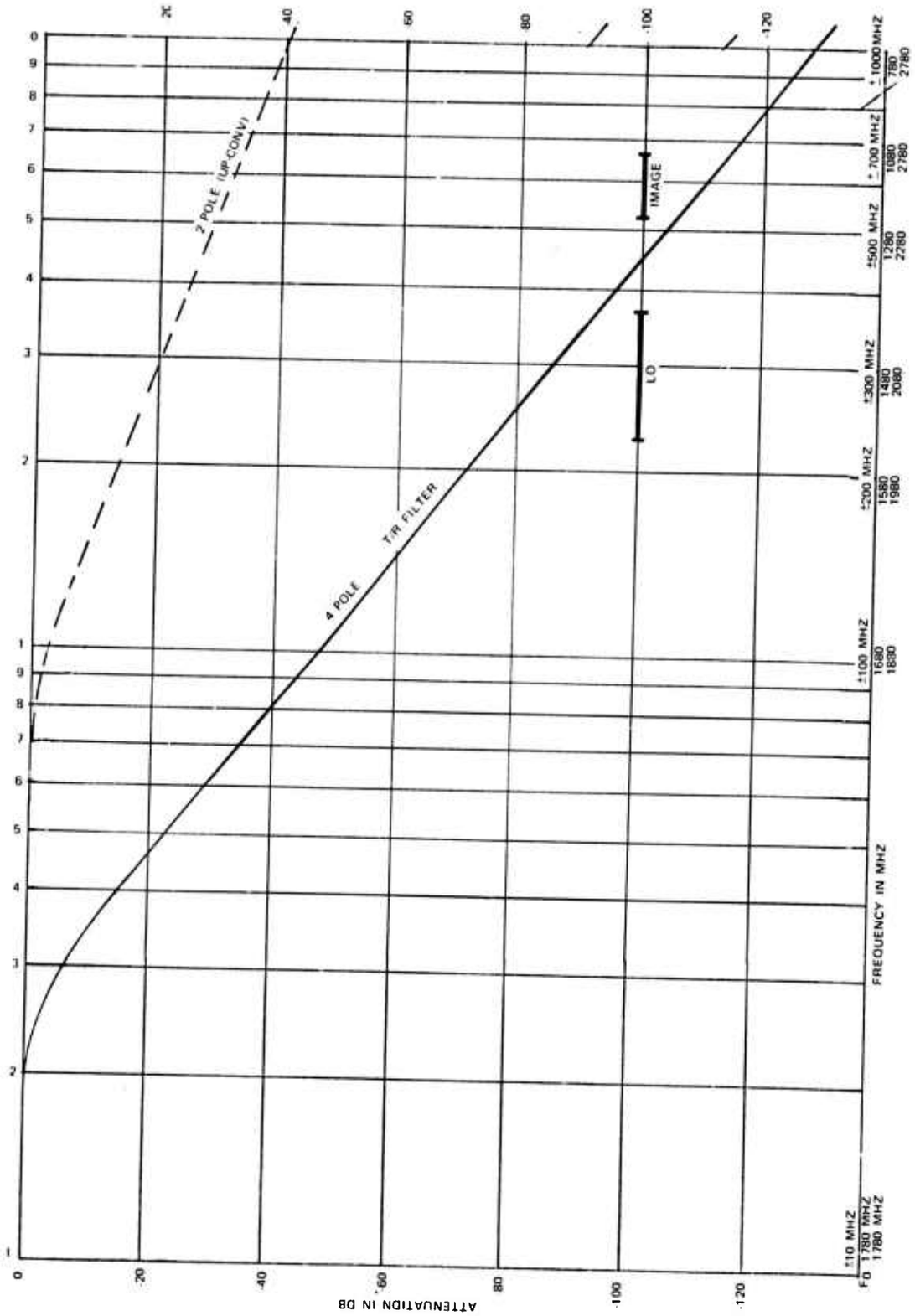

Figure 5-10. T/R and Up-Converter Output Filter Characteristics.

minimum. Further reduction of LO leakage results from balance of the doubly balanced down-converter.

5.2.6 Antennas

a. Functional Description. Two antennas are being developed: (1) a small omni 0-dBi gain antenna for use with terminal equipment, and (2) a 9-dBi gain antenna for use with the repeater which is omnidirectional in the azimuth plane but has sufficient vertical directivity to achieve a gain of approximately 9 dB.

The 9-dBi gain antenna consists of sleeved dipoles stacked colinearly. The feed arrangement is designed to maximize bandwidth.

The antenna will be a cylinder approximately 2 inches in diameter and 24 inches long. Figure 5-11 shows the expected antenna pattern.

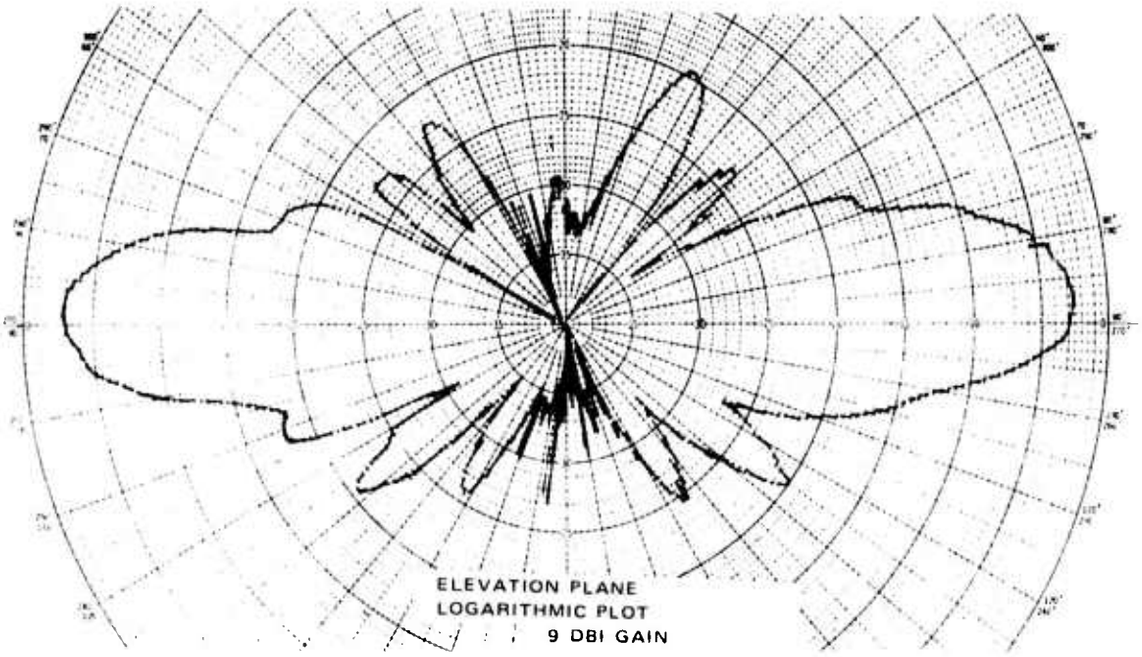

Figure 5-11. Typical Antenna Elevation Pattern.

b. Performance Summary.

	9-dBi Antenna	0-dBi Antenna
Frequency	1710 to 1850 MHz	1710 to 1850 MHz
Polarization	Vertical	Vertical
Maximum Input Power	50 W	25 W
Input VSWR	≤ 1.5:1	≤ 1.5:1
Impedance	50 ohms	50 ohms
Gain Flatness over BW	≤ 1-dB target	≤ 1 dB

5.2.7 Frequency Generation

Two precision frequency sources are required: (1) local oscillators (LO) and (2) chip/bit clock. Because of SAWD frequency tolerances, these are generated separately (two frequency standards) although ideal SAWD's would permit use of one standard.

a. LO Generation Functional Description. The first LO frequency is generated and power split for simultaneous transmit LO and receiver LO injection as illustrated in figure 5-12. A digital frequency synthesizer is employed. The frequency synthesizer provides 20 frequencies in 3.2-MHz increments. Doubling the synthesizer output produces twenty 6.4-MHz steps from 1420.800 to 1542.4 MHz. With a first if frequency of 297.9155 MHz, this produces an rf center frequency range of 1718.7155 to 1840.3155 in 6.4-MHz steps. By moving the standard frequency ±11 ppm, the LO frequency may also be moved ±11 ppm, or about ±20 kHz. This allows setting the input and output frequencies to the precise chosen value when using if SAWD's, which may be in error by as much as ±20 kHz due to manufacturing tolerance.

The LO frequency is controlled by six control lines from the microprocessor. These control lines program the loop feedback counter divide ratio (÷222 through ÷ 241).

The LO frequency standard maintains a stability (±1 ppm) with temperature over an adjustment range of ±11 ppm. The frequency is 4.000 MHz, which is in the optimum frequency range of Temperature Compensated Crystal Oscillators (TCXO's).

b. Chip/Bit Clock Generation Functional Description. The stable clock generator employs a frequency standard followed by various dividers to obtain the required frequencies with commercially available integrated circuit dividers. The frequency standard is a TCXO operating at 25.627136 MHz. A X9 multiplier (two X3 circuits) is used to generate the second LO injection of 230.6 MHz from this TCXO. This TCXO provides ±1-ppm absolute frequency stability. Note that this TCXO X9 and bit clock divider circuit are the same as described in the encoder/modulator.

c. Functional Interface.

1. First LO Outputs.

Two outputs, one transmit and one receive

P_o = +7(±3) dBm at 50 ohms

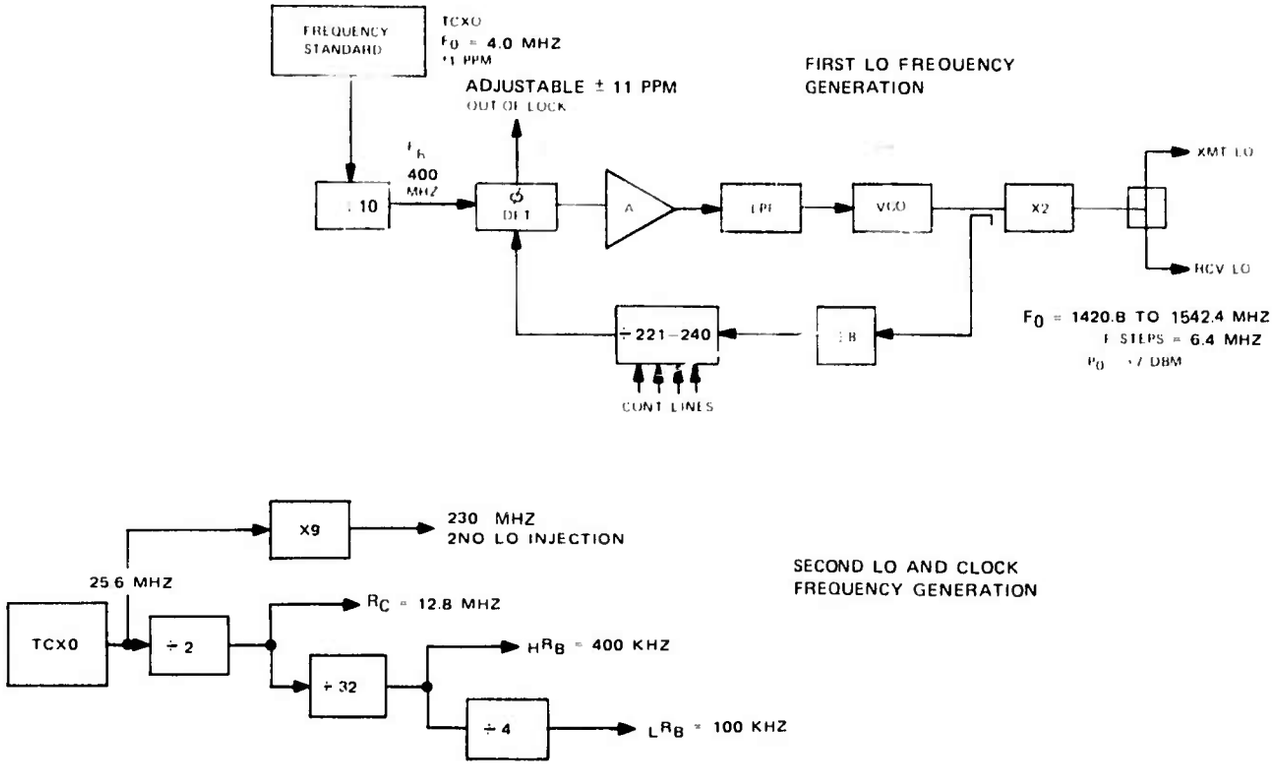

Figure 5-12. Frequency Generation.

Frequency = 1420.8 through 1542.4 MHz

Frequency steps = 6.4 MHz

Frequency switching speed ≤ 1 ms to be within 10 degrees of final phase

4.0-MHz TCXO stability: ≤ ppm

4.0-MHz TCXO settability: ≥ 11 ppm

2. Second LO Outputs.

   Two outputs, one transmit and one receive

   P_o +7(±3) dBm at 50 ohms

   Frequency 230.6 MHz

   25.6-MHz TCXO stability = ±1 ppm

3. Control Lines. Six logic lines from microprocessor whose states correspond to required output frequency.

4. Chip/Bit Clocks.

   TCXO Stability = ±1 ppm

   R_c = 12.8 MHz

   L^RB = 100-Kbps clock

   H^RB = 400-Kbps clock

5. Status Output.

   Out-of-lock indicator

d. Performance Summary.

1. First LO Injection. A voltage-controlled oscillator (VCO) is used to produce an output in the frequency range of 700 to 800 MHz. Its single sideband (ssb) phase noise specification is -65 dB in a 1000-Hz bandwidth. Frequency doubling and normalizing to a 1-Hz bandwidth results in a noise level of -90 dB/Hz. Considering the data rate and characteristics of the phase-lock loop, this is more than adequate for the required bit error rate (BER) performance.

   Spurious signals include reference frequency components (400 kHz) and power supply ripple and noise components that modulate the VCO. The latter is a design problem involving shielding, supply line filtering, and choice of phase-lock loop parameters. Reference frequency components can be eliminated by loop filtering, but at the expense of requiring lower loop bandwidth and lower switching speeds. With 10-kHz loop bandwidth, 110 dB of loop filtering of 400-kHz reference frequency components can easily be obtained. Resultant spurious output is calculated to be -60 dB.

2. Loop Program Counter. The divide ratio is determined by two sequentially variable dividers, as shown in figure 5-13. The divider provides division ratios from 222 to 241. Small frequency increments are controlled by programming the first counter to divide by 11 a variable number (N) times, and then switching to a count of 10 for the remainder of the cycles defined by the second counter. The second counter is programmed for counts of 22, 23, or 24 and provides the larger frequency steps.

5.2.8 Down-Converter

a. Functional Description. A functional diagram of the double conversion down-converter is shown in figure 5-14. Its function is to convert the rf (1718 to 1840 MHz) received from the T/R switch to the if (67.27 MHz). This is accomplished by first preamplifying

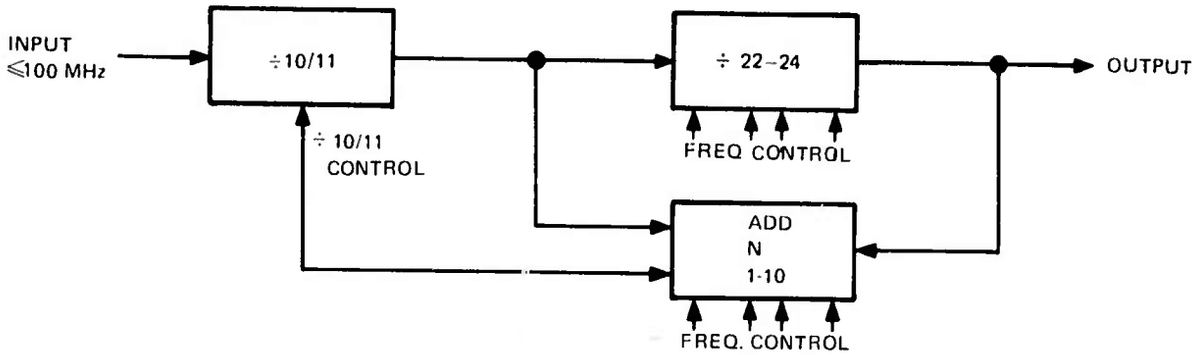

Figure 5-13. Programmed Divider (222—241).

the rf signal and then mixing in a doubly balaneed mixer with the reeeiver First LO frequeney (1420.8 to 1542.4 MHz). The output of the mixer is filtered through a 20-MHz wide 3-pole Chebyshev bandpass filter and further down-converted to 67.27 MHz. Both if filters reject the spurious frequencies, including the upper sideband frequency. The filtered if is preamplified before interconnection to the input of the agc amplifier.

b. Funetional Interfaees.

RF Input	1718.7 to 1840.3 MHz MSK
Power	-106 to 0 dBm
NF	≤ 8 dB

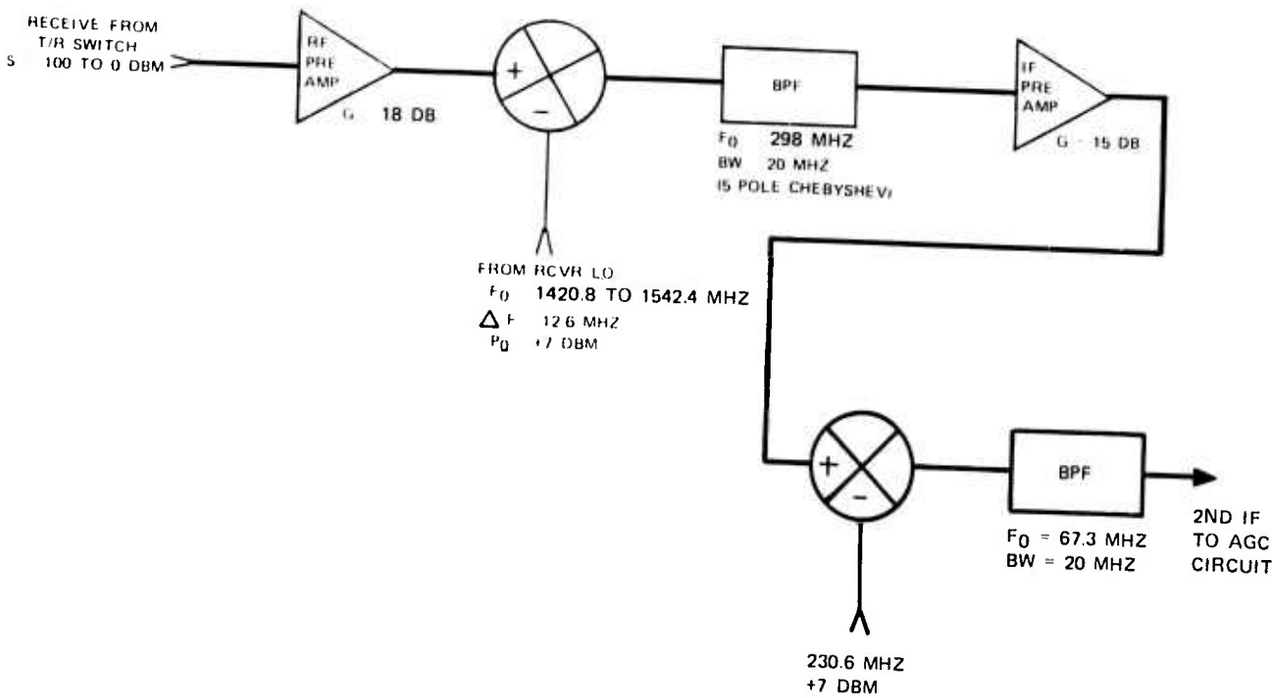

Figure 5-14. Down-Converter.

First LO Input	1420.8 to 1542.4 MHz
Power	+7 (±3) dBm
Second LO Input	230.6 MHz
Power	+7 (±3) dBm
IF Output	67.27 MHz MSK
Bandwidth	20 MHz
P_0	-88 to 9 dBm

5.2.9 Noncoherent AGC Amplifier

a. Functional Description. The noncoherent age amplifier shown in figure 5-15 is located before the matched filter (SAWD) and provides the SAWD with a constant level input signal. The amplifier functions in a linear mode only. Since the input signal can consist of desired plus interfering signals, a second level of age amplification is necessary to provide a constant level of desired signal to the signal processor. This is provided by the coherent age amplifier. Thus, if a large interferor is present, the signal component to the input to the SAWD is lower than desired, but the gain is restored after the signal-to-interference ratio has beem improved by the correlation properties of the SAWD. This two-stage approach reduces the dynamic range requirements of any one amplifier and allows independent control of the composite RF level and the correlation peak level.

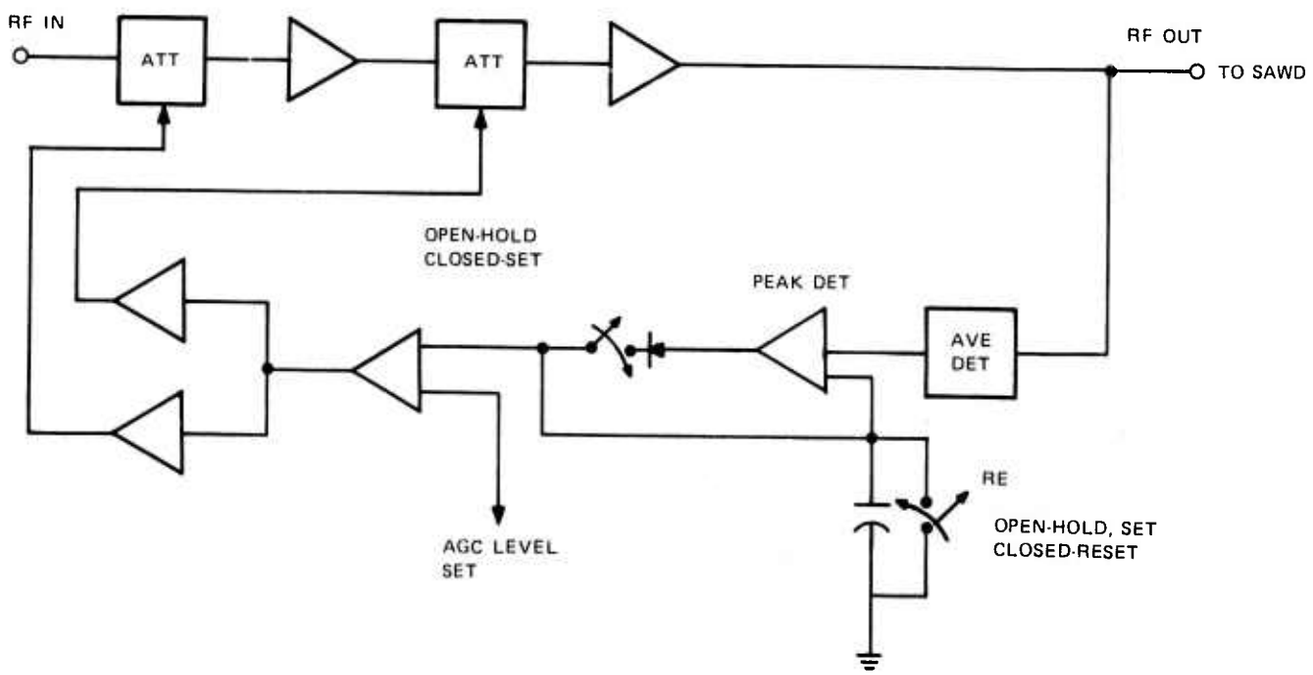

Figure 5-15. Noncoherent AGC Amplifier.

b. Functional Interfaee.

Amp Input	IF signal from down-converter
Amp Output	IF signal out of age amplifier to SAWD
Rcv Enable	Control gate from microprocessor
EOP	EOP flag from preamble detect — activates hold mode

e. Operational Description. The operation of the noneoherent agc amplifier is shown in figure 5-16. (Refer to figure 5-15 for a diagram of the circuit and to figure 5-17 for mode control waveforms.) The agc loop is disabled until a Receive Enable (RE) signal is received. The period during which the RE signal is not present is defined as the

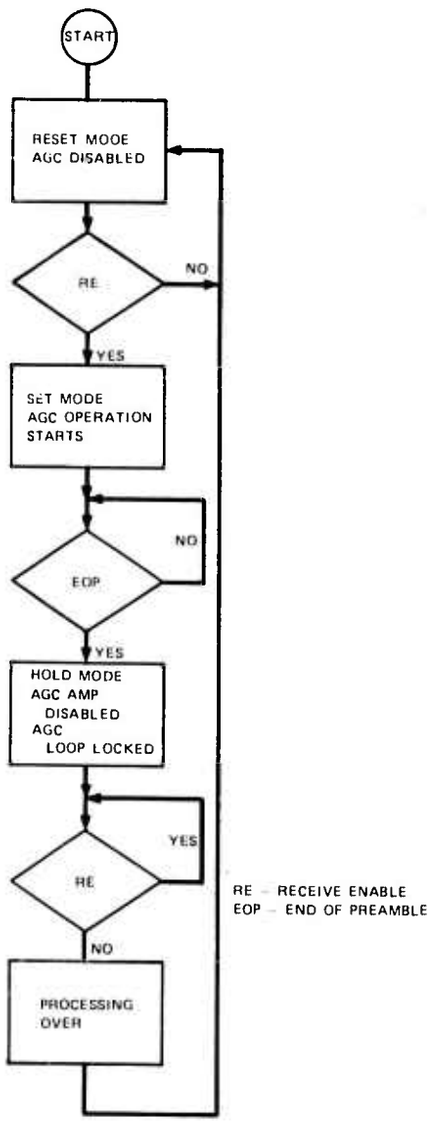

Figure 5-16. Noncoherent AGC Operational Flow Chart.

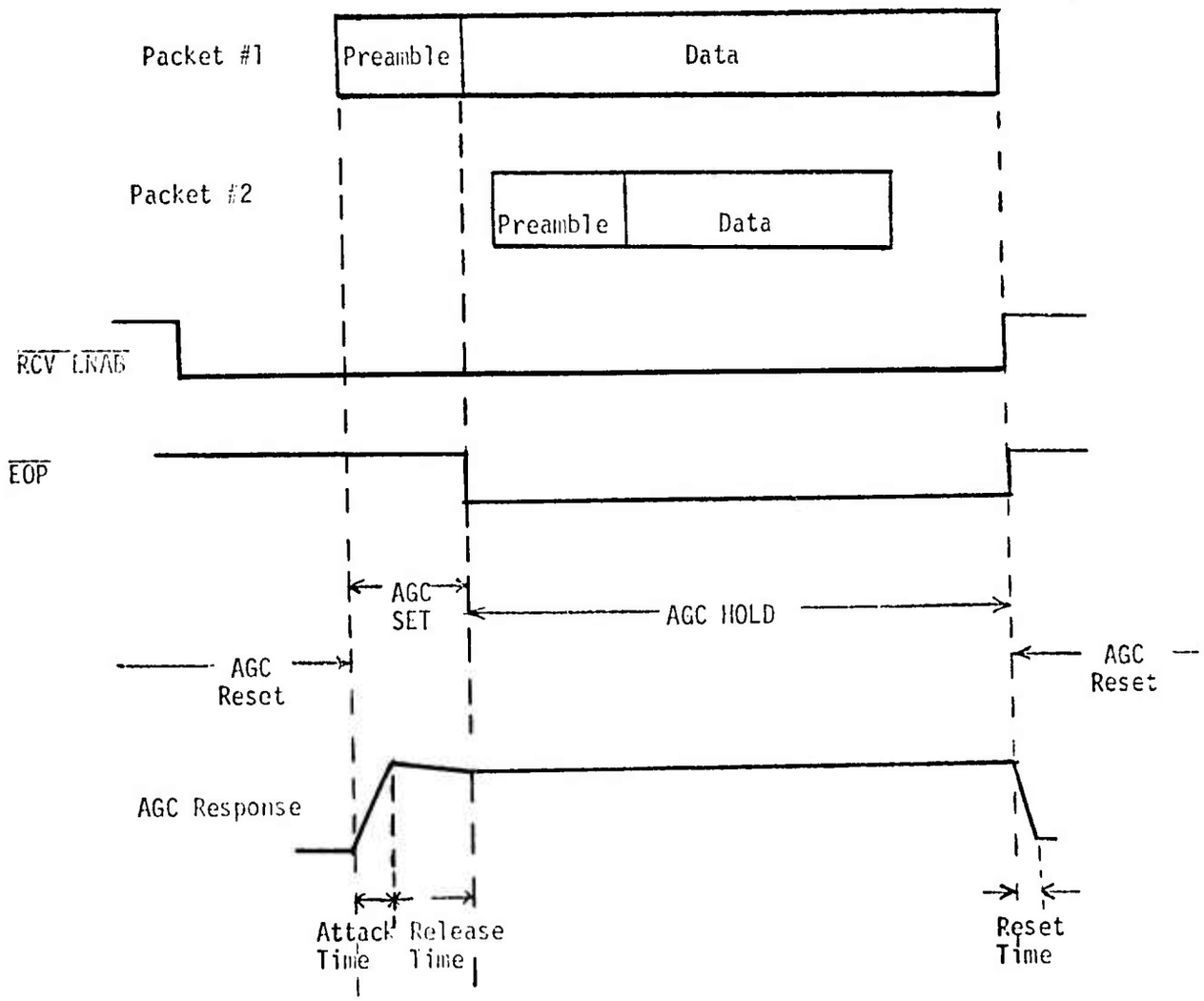

Figure 5-17. Noncoherent AGC Modes.

Reset/Release time. The Receive Enable (RE) control signal activates the receiver, and the noneoherent age is eontrolled by any signal, noise or interferenee present. When the preamble of a data packet is received, the agc rapidly settles to the level required to normalize signal plus noise plus interference to an output level of -10 dBm. The agc settling time is from 1- to 4 bit periods, allowing a major portion of the 48-bit preamble for settline of the eoherent age, aequisition of bit sync and deteetion of the end of preamble.

With receipt of the EOP signal, the hold mode begins. The loop amplifier is disabled, and the agc voltage stored in the peak detection circuit holds the gain constant during the rest of the packet. This mode of operation persists until the RE signal is removed, again placing the agc circuit into the Reset/Release mode.

5.2.10 Signal Processing and Detection

a. Functional Description. The remaining paragraphs of the radio equipment description describe the functions and operations of receive multiple signal processing. The signal processing equipment extracts bit data from the rf analog signals. Data detection may occur at two rates in repeater/station configurations. The equipment is also designed to provide simultaneous detection of two or more signals at a common data rate by time gating techniques. This is possible provided the correlation peaks of the multiple signals do not overlap and provided the signals received do not exceed a relative dynamic range of 10 to 15 dB. The signal processing equipment provides for the following rates and multiple detectors:

1. 100 Kbps — Terminal/repeater
2. 400 Kbps — Repeater/repeater
3. 100 Kbps — Multiple detectors - stations (optional, not being implemented)
4. 400 Kbps — Multiple detectors - stations (optional, not being implemented)

Multiple signal processing is functionally depicted in figure 5-18. The signal processor performs data recovery for 100 Kbps, 400 Kbps, and multiple channel detection at these two rates. For terminal operation, the processing equipment is needed for only the 100-Kbps rate. For repeater (and station) operation, equipment for both the 100-Kbps and 400-Kbps rates is required. Both the 100-Kbps and the 400-Kbps outputs are connected to the microprocessor. Multiple detectors can operate at either rate. The maximum number of time slots for multiple detectors at 400 Kbps is three. The higher spread factor of the 100-Kbps rate results in a maximum of 14 time slots for multiple detection at this rate; however, it is not expected that more than two detectors at either rate will be effective. Multiple detectors do not require multiple SAWD's, but use the SAWD correlation outputs that are time displaced within a bit period.

Multiple signal processing, as with single rate processing, requires preamble detection, bit sync acquisition, and data detection. The following paragraphs elaborate on each of these areas.

b. Operational Description — Signal Processing/Detection. A functional block diagram of signal processor and differentially coherent detector is shown in figures 5-19 and 5-20. Figure 5-20 also shows how code spread MSK demodulation and differentially coherent detection is achieved. MSK demodulation is further described in paragraph 5.2.11. The differentially coherent detector compares the phase of two adjacent bits and, hence, only requires coherency over the period of 2 bit intervals.

The coherent detectors are constructed using two identically coded matched filter lines, but with one delayed very accurately by a bit period T_B. The two outputs are differentially (bit-to-bit) compared in the 180-degree hybrid. For instance, a 0 data bit is transmitted as C C (Code, Code) or $\overline{C}$ $\overline{C}$. The two SAWD outputs have identical autocorrelation pulses and will be in-phase with respect to each other. Thus, the Σ hybrid output will have autocorrelation pulses added while the Δ port will be cancelled (no output). Similarly, a data bit 1 is transmitted as either C $\overline{C}$ or $\overline{C}$ C. Here, the Σ port will be cancelled and the Δ hybrid port output will have autocorrelation pulses.

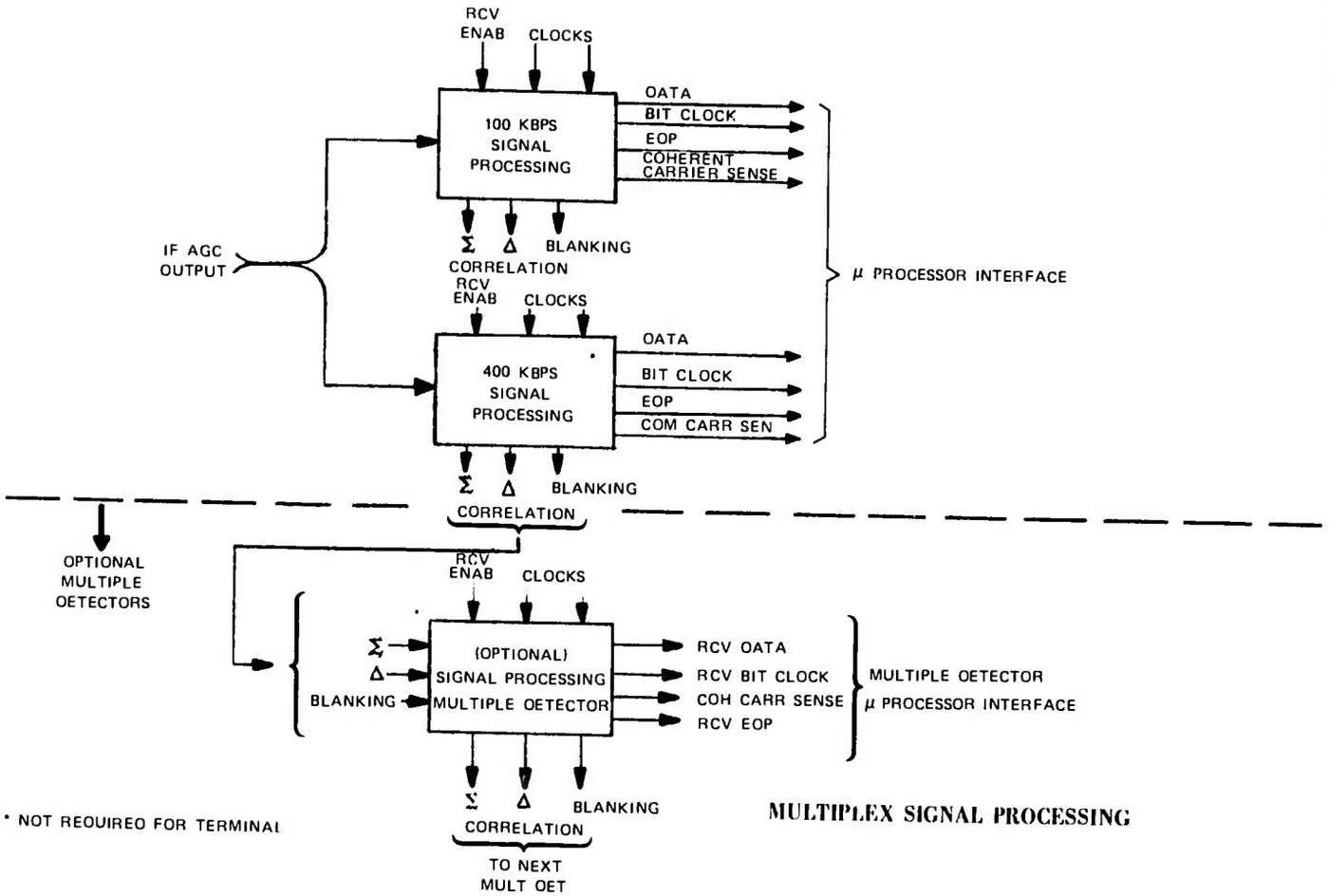

Figure 5-18. Multiple Signal Processing.

Each Σ and Δ output is amplified, envelope detected, and gain normalized (coherent agc function) to a constant peak correlation level. Since coherent phase comparison has already been accomplished in the hybrid, only amplitudes of Σ , Δ outputs are of interest.

Data detection is now merely a "largest of" comparison of envelope detected Σ and Δ outputs. If Σ channel is larger than Δ channel, a data bit 0 is detected; and if Δ is larger, a data bit 1 is detected.

Detection is achieved by sampling with a timing window that is $2T_c$ seconds wide where T_c is the chip interval, storing the peak value during that timing window, and making a

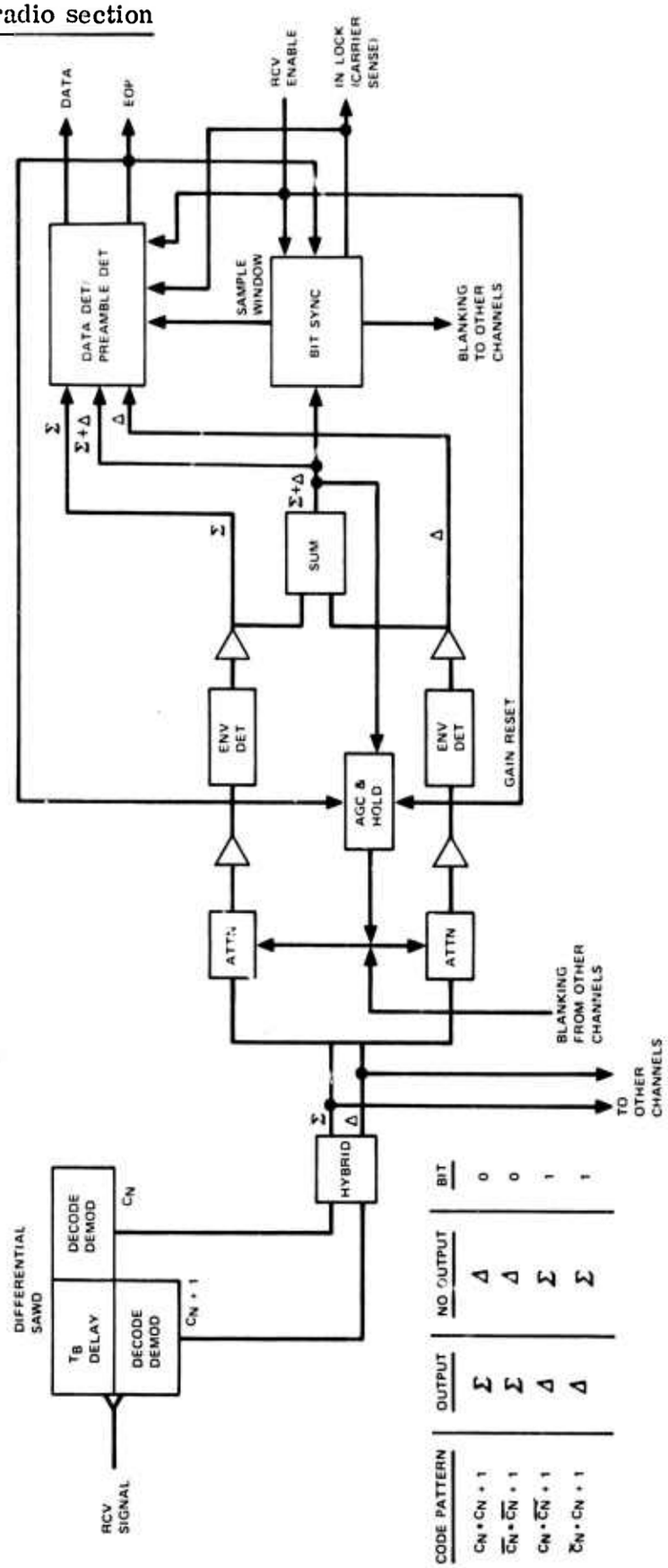

Figure 5-19. Signal Processing.

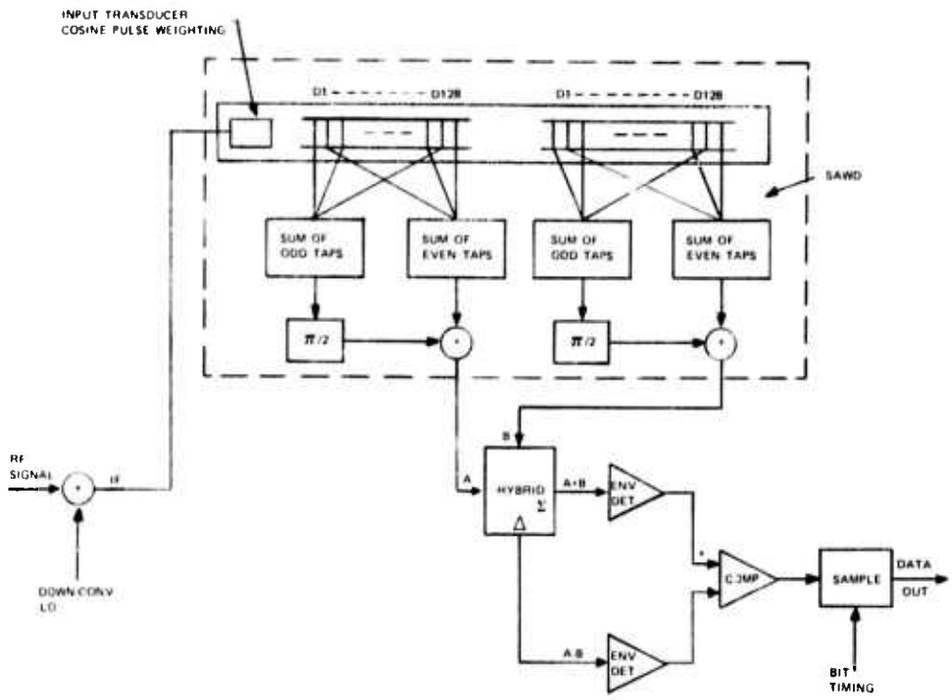

Figure 5-20. Differentially Coherent MSK Demodulator.

bit decision at the end of the timing window. This form of detection degrades performance by only 0.5 dB from the ideal timing case.

The end of preamble (EOP) detector searches the incoming serial data for the Barker code pattern. EOP sets age circuits to a hold state, changes bit sync acquisition (to tracking), and informs the microprocessor of start of data.

The bit synchronizer employs the envelope of $\Sigma + \Delta$ detected outputs to derive bit timing. An analog phase-lock loop tracks correlation pulses in a narrow time window after the preamble. The narrow time window improves multipath rejection.

Multipath components are signals that arrive at the receiver antenna at a different time from the most direct signal. Different time of arrivals are due to signal reflections off buildings, hills, trees, vehicles, aircraft, etc., which all have different signal propagation paths. Multipath results in delayed signals; however, some reflected signals may be stronger in level than the most direct propagation path. This might occur when the antenna is behind a building or hill, where another building may provide a reflection with a much better propagation path.

Another multipath effect is doppler shift due to moving reflectors (vehicles, aircraft, or tree leaves in a breeze), or a moving transmitter and/or receiver. Measurements indicate that non-moving transmitters and receivers will observe very little multipath amplitude change and doppler frequency spread over the duration of a packet. Moving transmitters and/or receivers cause serious fading and excessive doppler shifts during the duration of a packet. Since age levels are held constant gain throughout the packet following preamble, serious signal distortion will be caused and, hence, data errors. Initial repeaters will not be designed for mobile operational, though it appears that satisfactory mobile operation can be provided using diversity and/or error correction

techniques. Other multipath effects such as dispersive fading are not of importance for the relatively short distance anticipated for packet radio.

During preamble, multipath is overcome by searching for a maximum peak signal and locking the bit sync to that peak signal. Since the coherent age normalizes the output levels to maximum peaks, be they multipath delayed peaks or not, bit sync also senses on these peaks. Therefore, the largest received signal is used for data detection even though it may be a multipath delayed signal. This is discussed in more detail in a later paragraph on bit sync.

Signal processing for 100 Kbps and 400 Kbps is essentially the same. Identical circuits are used, with different component values unique to each bit rate.

5.2.11 Differentially Coherent Detection with SAWD's

a. Functional Description. The SAWD input is a wide-band spread spectrum if signal normalized to a constant level by the noncoherent age circuits. The age maintains signal plus noise plus interference constant at the noncoherent age output: hence, the desired signal component may vary. For example, prior to correlation S/N = -10 dB corresponds to E_b/N_o = 11 dB for the 128 spread system (100 Kbps). Also, discrete in-band interferers may override the noncoherent age control circuits, and such signals may exceed the desired signal by 10 to 15 dB before the error rate becomes excessive.

The output of the SAWD's is the autocorrelation of input code spread signal with the tap coded SAWD's. The output autocorrelation pulses are compared to the correlation pulse from the previous bit, and are coherently combined in a hybrid.

b. Functional Interface.

1. RF Input
2. Σ Channel RF Out
3. Δ Channel RF Out

c. Operational Description. Pseudonoise code spread spectrum demodulation is most easily achieved with tapped delay line matched filters. SAWD's are ideally suited for this purpose. MSK demodulation is also ideally suited for SAWD's since the transducer weighting corresponding to transmitted symbol shaping (half cosine weighting) is easily produced on SAWD's. Figure 5-20 shows the demodulator implemented with SAWD's. Figure 5-5, MSK Waveforms, shows the in-phase and quadrature carrier components that are modulated with in-phase and quadrature envelopes (cosine weighting). SAWD input transducer design matches envelopes, while alternate tap spacings (odd taps, even taps) are code matched to the transmitted code. Figure 5-20 conceptually shows these alternate taps to be summed separately, one component phase shifted 90 degrees and the resultant signal summed as one SAWD output. The second coded section is identical to the first, except delayed 1 bit period T_B. T_B delay, conceptually shown in series in figure 5-20, is, in practice configured in a separate acoustic path for distortion reasons as shown in figure 5-29. Also, the $\pi/2$ phase shift shown in series with the taps is, in practice, achieved by tap spacing shift of 90 degrees in electrical length of carrier phase. Hence, the phase shifting and summing functions shown conceptually as separate functions in figure 5-20 are all simply accomplished by proper placement and connection to SAWD taps, as shown in figure 5-21. The autocorrelation peak of the tapped waveform is shown in figure 5-22.

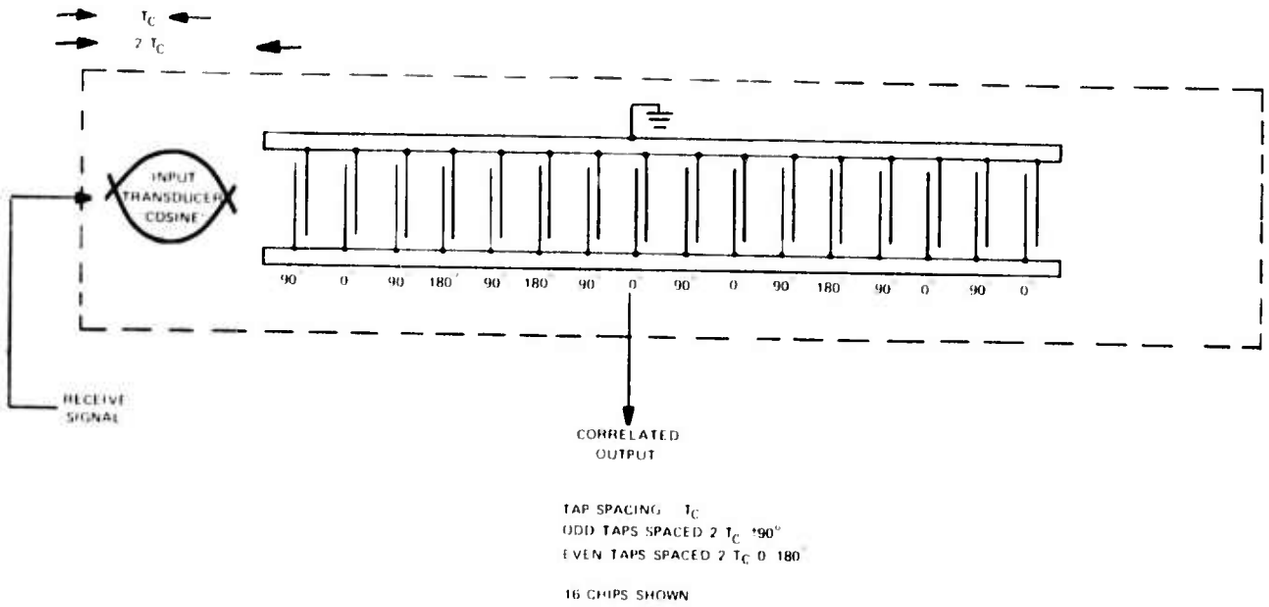

Figure 5-21. SAWD Implementation for MSK.

d. Coding. Since autocorrelation of multiple signals in a tapped matched filter will be necessary if multiple detectors are employed, the choice of coding for code spread systems becomes highly important. The code C for both high rate and low rate was selected considering the minimum peak sidelobe level, minimum mean sidelobe level, and minimum cross-correlation between codes.

C C * C corresponds to a data bit 0 being transmitted and results in different sidelobes as when C C * C = 1 is transmitted.

Theoretical peak to sidelobe ratios for the codes that are being used for the experimental packet radio system are summarized as follows:

1. High Data Rate (32-Chip Length)

	Peak/Highest Sidelobe	Peak/Mean Sidelobe
C * C (code not repeated)	16.2 dB	25.24 dB
C C * C (code followed by code)	12.04 dB	21.70 dB
C C * $\overline{C}$ (code followed by code inverse)	14.54 dB	22.36 dB

2. Low Data Rate (128 Chip Length)

C * C	19.86 dB	30.14 dB
C C * C	18.06 dB	26.24 dB
$\overline{C}$ C * C	17.04 dB	28 dB

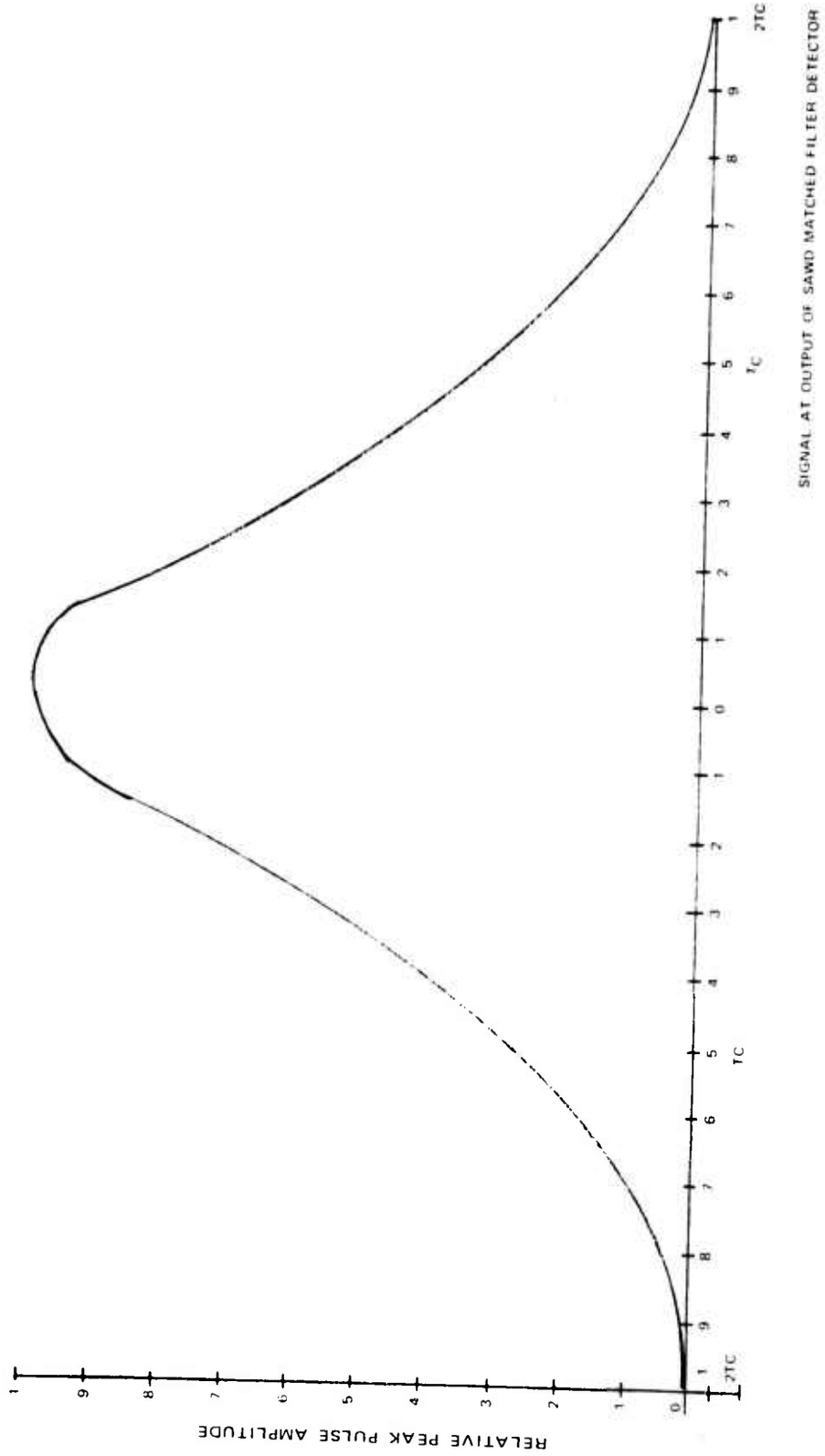

Figure 5-22. Autocorrelation of MSK.

3. Cross-correlation	Peak/Highest Sidelobe	Peak/Mean Sidelobe
High data rate into low data rate	11.8 dB	22.6 dB
Low data rate into high data rate	8.1 dB	15.96 dB

5.2.12 Coherent AGC Amplifier

a. Functional Description. The coherent agc follows the SAWD's and amplifies the decoded/demodulated signal to a constant peak level. Figure 5-23 shows the coherent agc. The coherent agc circuit also includes envelope detectors for baseband processing of Σ and Δ channels. Envelope detectors are operated in linear mode for correlation peaks, but for low level signals (such as sidelobes and multipath) envelope detection is square law.

b. Functional Interface.

Σ IF	Input from SAWD A
Δ IF	Input from SAWD B
Σ	Σ output
Δ	Δ output
$(\Sigma + \Delta)$	$(\Sigma + \Delta)$ output

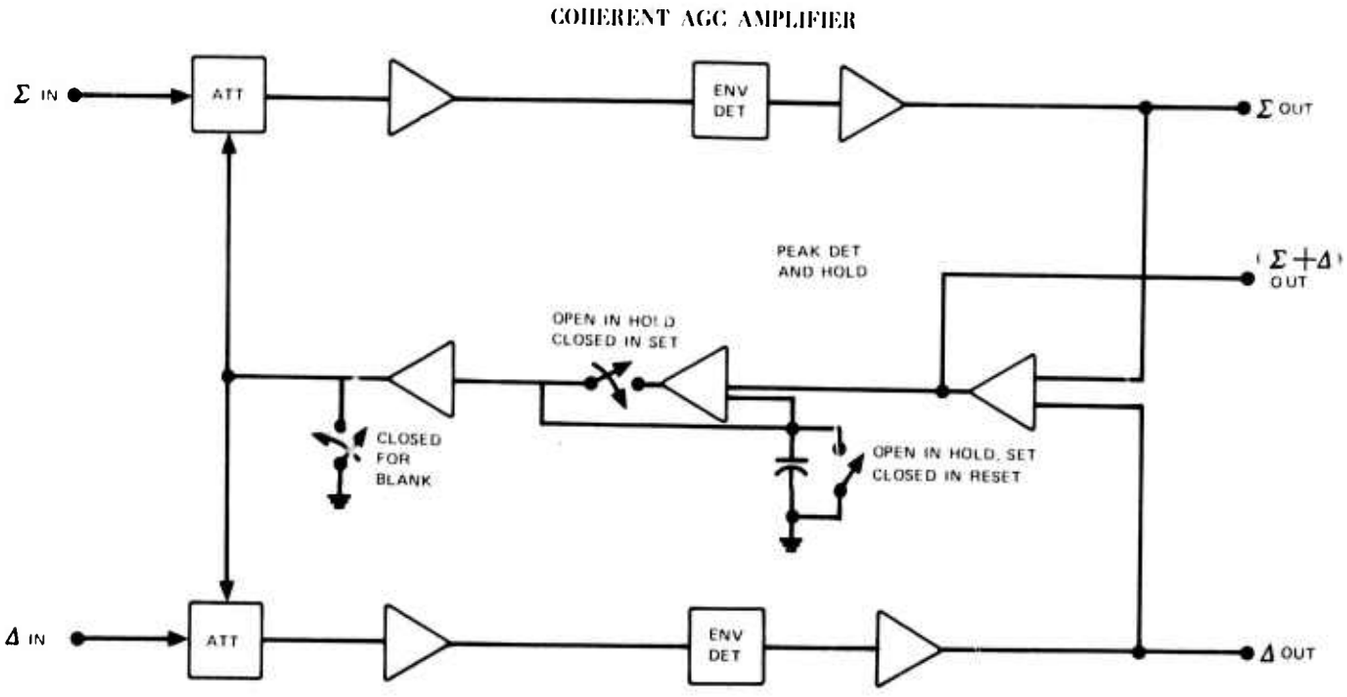

Figure 5-23. Coherent AGC Amplifier.

c. Operational Description. The operation of the coherent age amplifier is depicted in figure 5-24. (Refer to figure 5-23 for a block diagram of the circuit and to figure 5-25 for mode control.) The basic operation of this unit is similar to that of the noncoherent age amplifier, with two exceptions: envelope detection and baseband outputs. Both age amplifiers possess the same three operational states: Reset, Set, and Hold; however, the coherent age has an additional Blanking state. The blanking pulse disables the receiver, as might be implemented by operating the input attenuators (maximum attenuation) to the coherent age amplifier. Thus, while the age loop basic sequence of operations remains unaffected, the normal operation of the receiver is interrupted by these blanking pulses. The coherent age operates on the Σ and Δ peak outputs, controlling each one separately but deriving the control voltage from the sum of the Σ and Δ signals. Blanking pulse capability is required only if the system is operated with multiple detectors in the "time slotted" mode.

5.2.13 Bit Synchronization

a. Functional Description. The purpose of the bit sync (figure 5-26) is shown to align the data sampling pulses with the received bits. The bit sync is required continuously throughout the detection of an incoming packet.

b. Functional Interface.

Σ and Δ Baseband	Receive packet inputs from SAWD detectors. Used for bit timing acquisition.
Rcv Enable	Input from microprocessor which allows the bit sync to operate.
EOP	End of preamble flag generated by preamble detector. Signifies end of locking sequence and allows various system parameters to be set if in-lock has occurred.
Bit Timing	Output of bit sync. Bit stream synchronized to packet bit rate.
Sample Window	Sampling pulse used to sample input data stream. $8T_c$ in duration when out-of-lock. $2T_c$ in duration when in-lock.
Blanking Output	Output of bit sync for multiple detector case, which is used to blank other detectors ($8T_c$ in duration).
In-Lock	Signal generated by a bit sync detector indicating that the synchronization of an incoming packet has been achieved.

c. Operational Description. The basic operation of the bit synchronization (bit sync) circuit is depicted by the flow diagram shown in figure 5-27. Note that the autocorrelation signal must pass through the anti-multipath (A MP) gate before it enters the bit sync. This analog gate is open during the start of a synchronization sequence, permitting a continuous flow of data to reach the bit sync circuit; however, after synchronization or lock-up is achieved, an 8-chip period window, centered over the incoming data chips, controls the gate. This reduces the number of multipath returns reaching the bit sync, thus improving operation of the circuit.

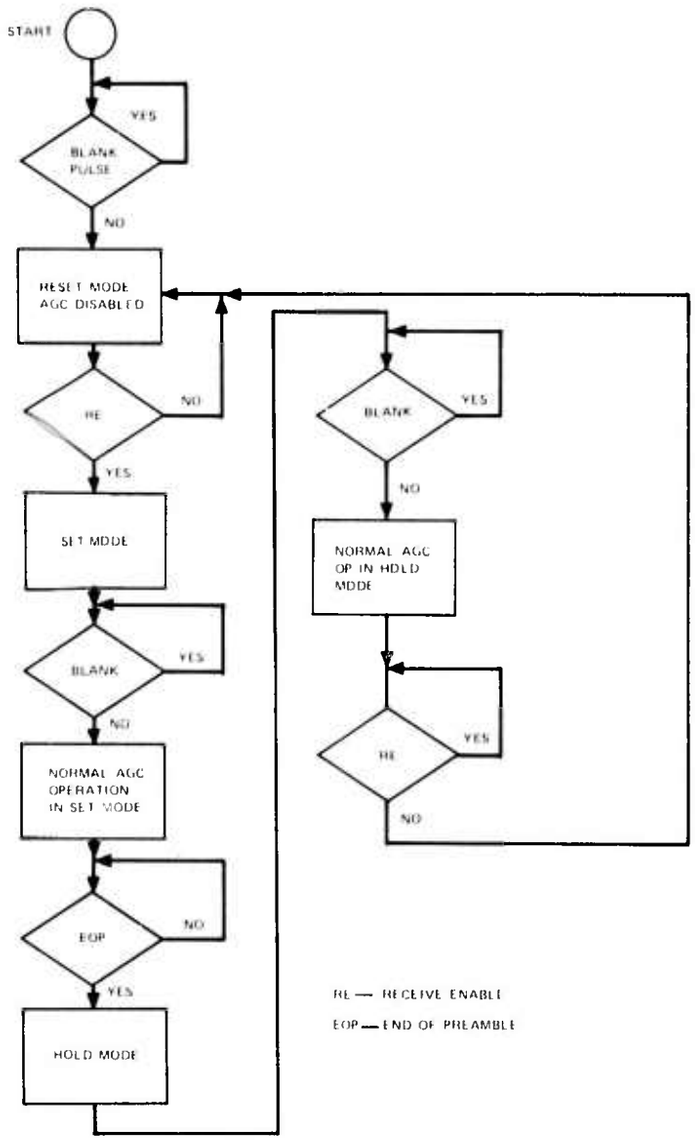

Figure 5-24. Coherent AGC Amplifier Flow Chart.

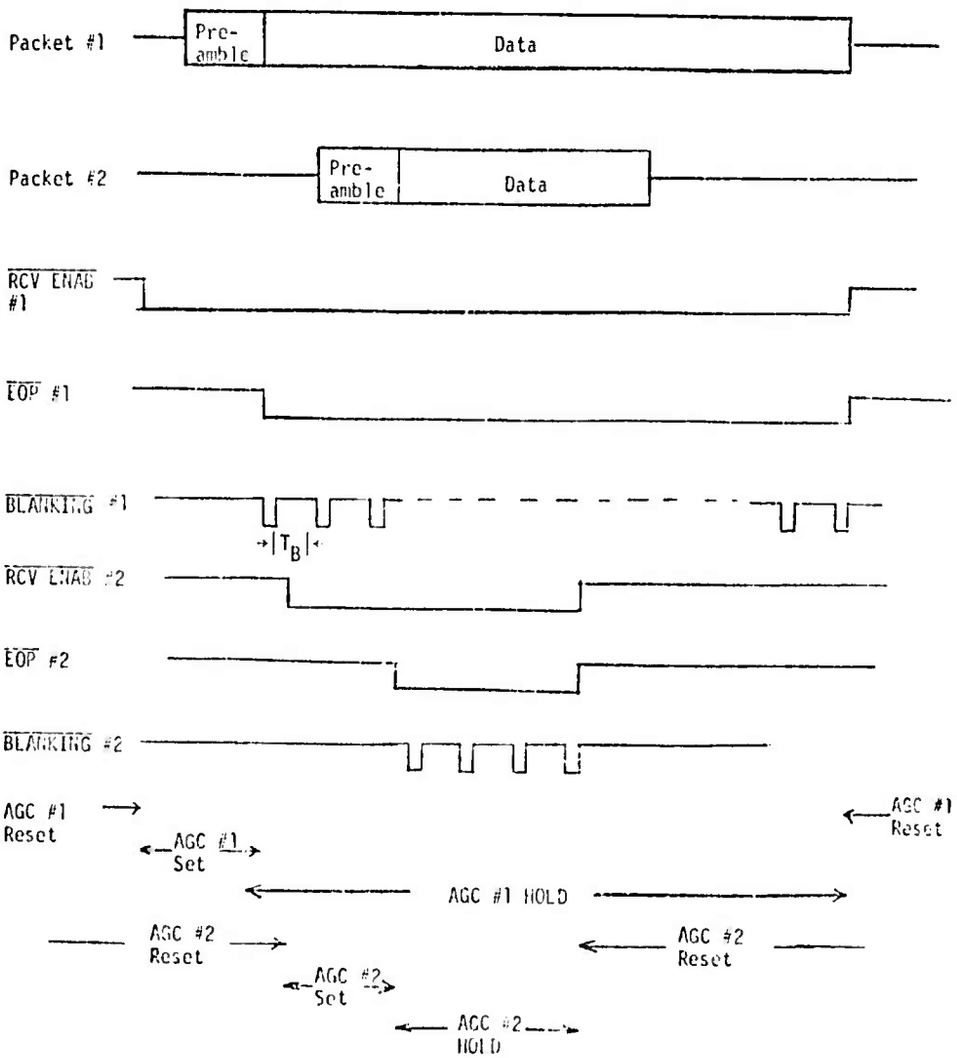

Figure 5-25. Coherent AGC Modes.

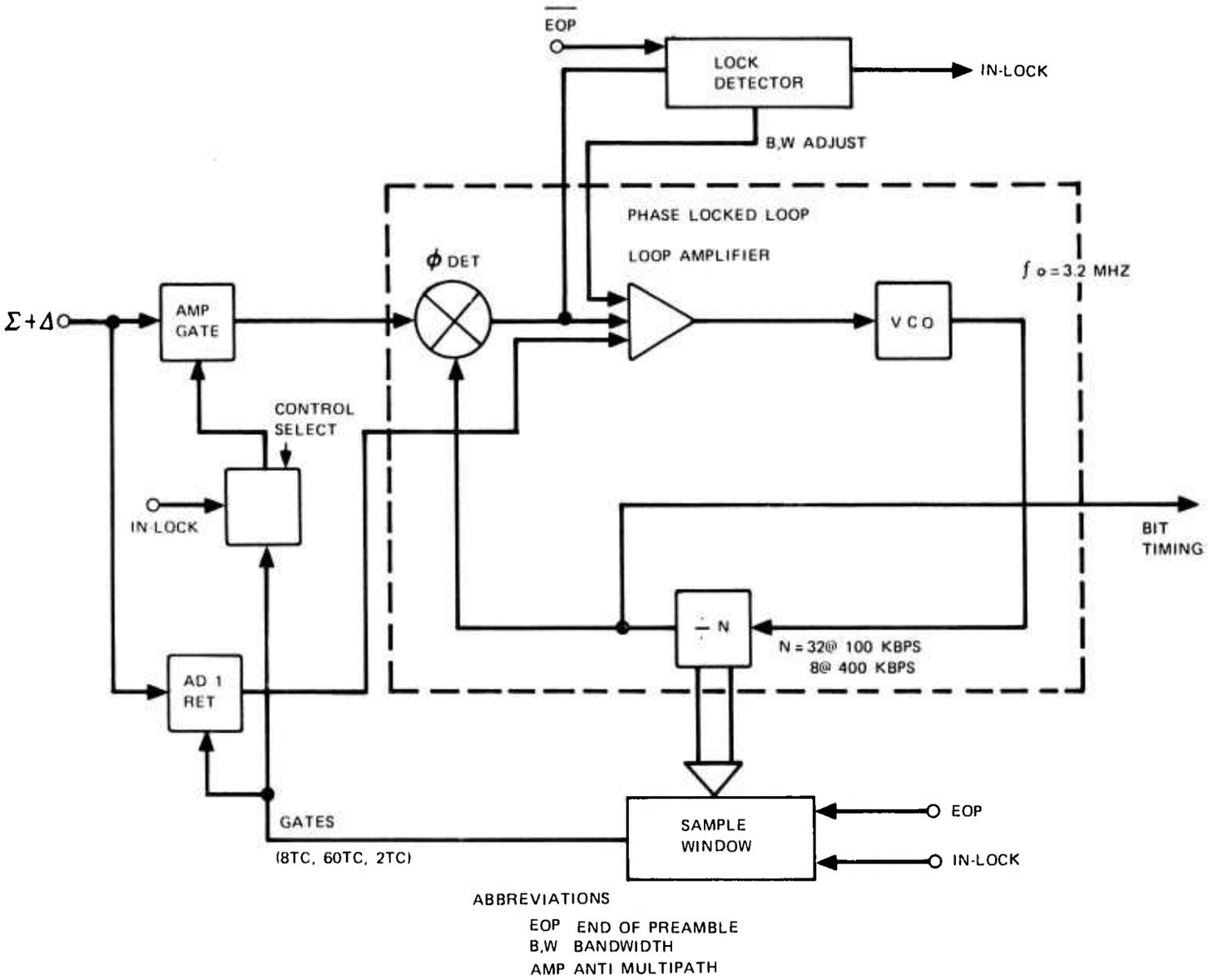

Figure 5-26. Bit Synchronization Functional Block Diagram.

Returning to the description of the actual synchronization sequence, note that the chain of events required to phase lock the signal processor to an incoming packet begins with the receipt of a Receive Enable (RE) gate from the system's microprocessor. Before the beginning of a sequence, the bit sync phase-lock loop (BSPLL) is free running. The following description pertains to 100-Kbps operation. The PLL's bandwidth (BW) is set at 10 kHz, and the sample window circuit is generating three gates. They are an $8T_c$ Sample Window, a $60T_c$ Advance gate, and a $60T_c$ Retard gate. Refer to the timing

*T_c — chip period.

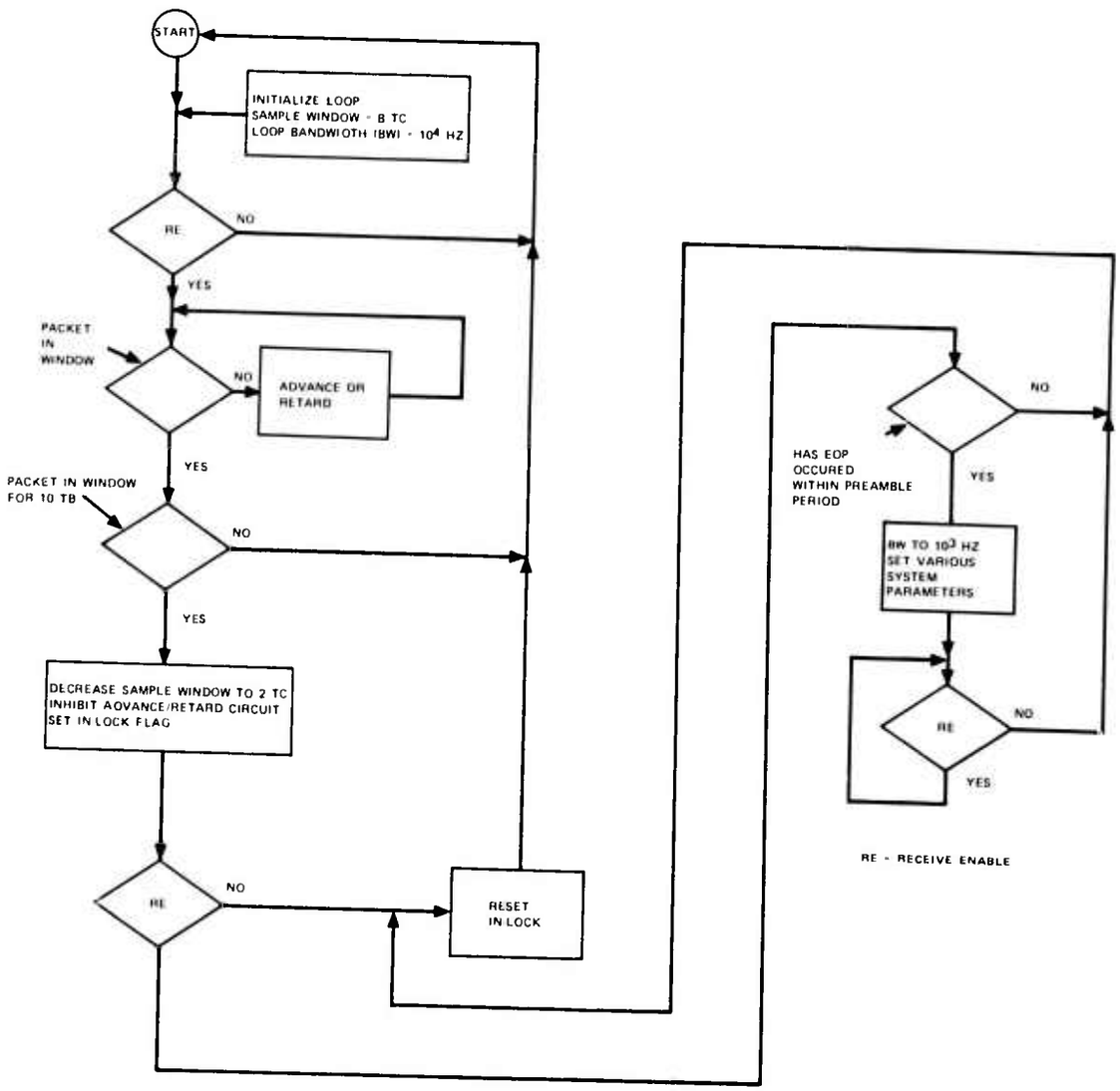

Figure 5-27. Bit Sync Flow Chart.

diagram (figure 5-28) and the cireuit block diagram (figure 5-26) for details. The packet ean occur at any time during the repetition period oi the paekets (either 100 kHz or 400 kHz). This neeessitates the determination of the exaet loeation of the paeket bits. This is done in two parts. (Refer to figure 5-28.) First, the total period is divided into two parts ($60T_e$ eaeh) and eaeh part is examined by the $60T_e$ advanee and retard gates. A eomparison of the deteeted signal found in each window is made with the signal found in the $8T_e$ window. Depending on the results of the comparison, a eontrol voltage is generated which slews the bit syne PLL voltage controlled oscillator (VCO) sueh that the largest signal amplitude oeeurring during the $128T_e$ window is plaeed under the $8T_e$ gate. This eircuit (the advanee/retard unit) allows the proeessor to funetion in the presenee of severe multipath propagation. The advance/retard circuit allows the processor to aequire the largest signal not blanked by a prior signal in the $128T_e$ window. This

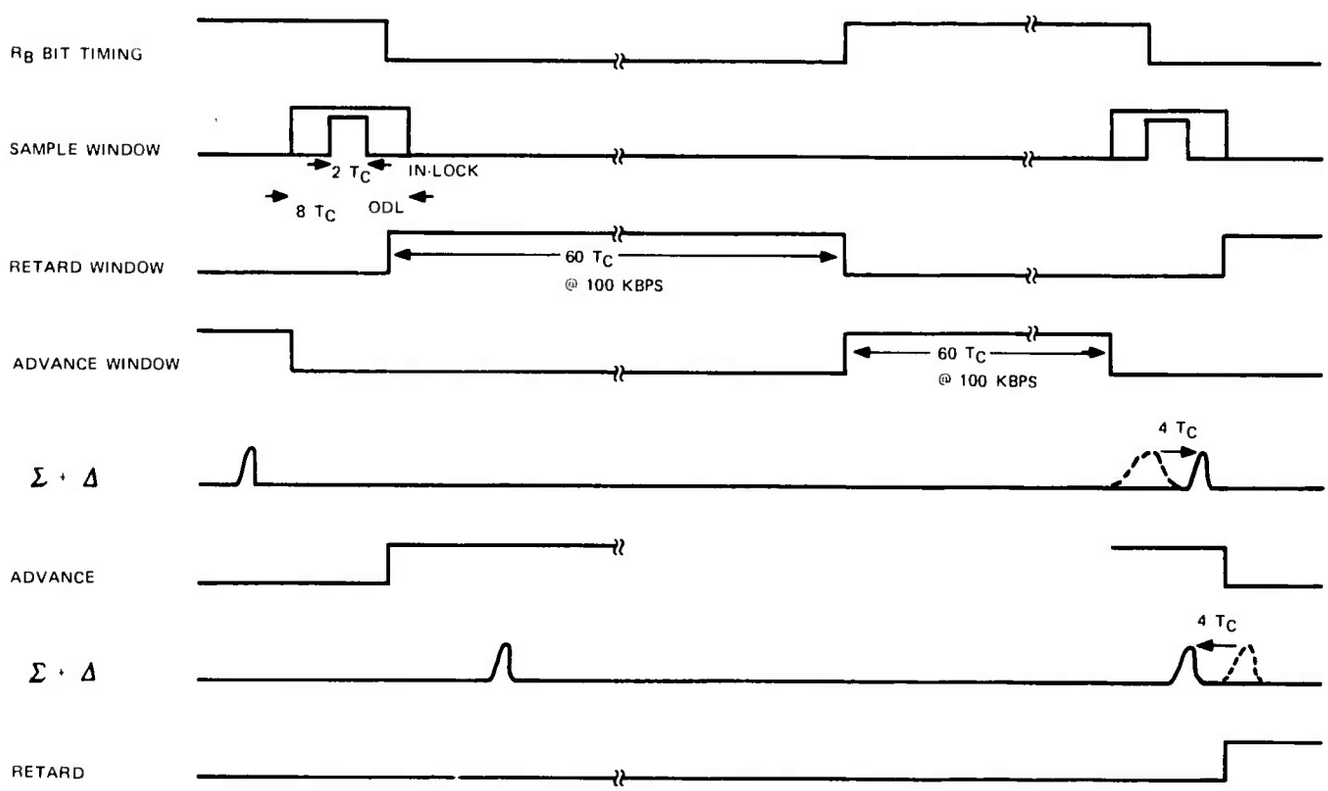

Figure 5-28. Bit Syne Advanee/Retard Timing Waveforms (100-Kbps Rate).

operation (locking of the bit sync clock to the largest signal) is consistent with the operation of the coherent age, which also reacts to peak signals. At this point the normal PLL action (the second step in the process) precisely locks the frequency of the VCO to the signal repetition rate. It is necessary for the signal in the $8T_c$ window to remain there for 10 bit periods ($10T_B$) to ensure complete phase locking. This is monitored and, if the above mentioned condition is met, the in-lock flag is raised. However, if this criteria is not met, the search continues. The in-lock condition causes the sample window to be reduced from $8T_c$ to $2T_c$, the advance/retard circuit to be disabled and sets a coherent carrier sense flag. At this point the receive enable signal must be present. If the RE command is not present, the bit sync circuit resets itself and awaits the start of another cycle.

The next step in the chain requires that an EOP message be generated by the preamble detector. (This must occur $38T_B$ or less after lock-in.) This signal is ANDed with the delayed in-lock signal. This then establishes the end of the bit sync procedure. If an EOP message is not received, the bit sync returns to its initial state and awaits the start of another cycle. However, if bit sync is accomplished, this final step causes the bit sync PLL to reduce its bandwidth, thus reducing tracking phase error.

5.2.1.4 EOP/Data Detector

a. Functional Description. The end of preamble (EOP) detector (figure 5-29) functions to determine the occurrence and timing of the end of the preamble of a received packet. This alerts the processor to the start of data. The EOP sets the noncoherent and the coherent age to a hold state, informs the microprocessor of the start of data, and in conjunction with the lock-in signal (from the bit sync), adjusts the bit sync phase-lock loop. The data detector is an integral part of the total EOP detector. Its output is a packet data bit stream. This information is delivered to the microprocessor for processing.

b. Functional Interface

Σ and Δ Baseband	Receive packet inputs from SAWD detectors ($\sim$1 volt peak)
Rcv Enable	EOP detection enabling function.
EOP Output	End of preamble detection signal.
Sample Window	$2T_c$ window, generated by the bit sync, which is used to sample the incoming bits.

c. Operational Description. A logic diagram defining the operation of the EOP detector is shown in figure 5-30. Refer to figure 5-29 for a block diagram of the circuit. The sequence of events which lead to an EOP message begins with the receipt of a Receive Enable (RE) flag from the system's microprocessor. Once activated (by the RE message), the circuit receives the envelope detector Σ and Δ outputs associated with the preamble of an incoming packet.

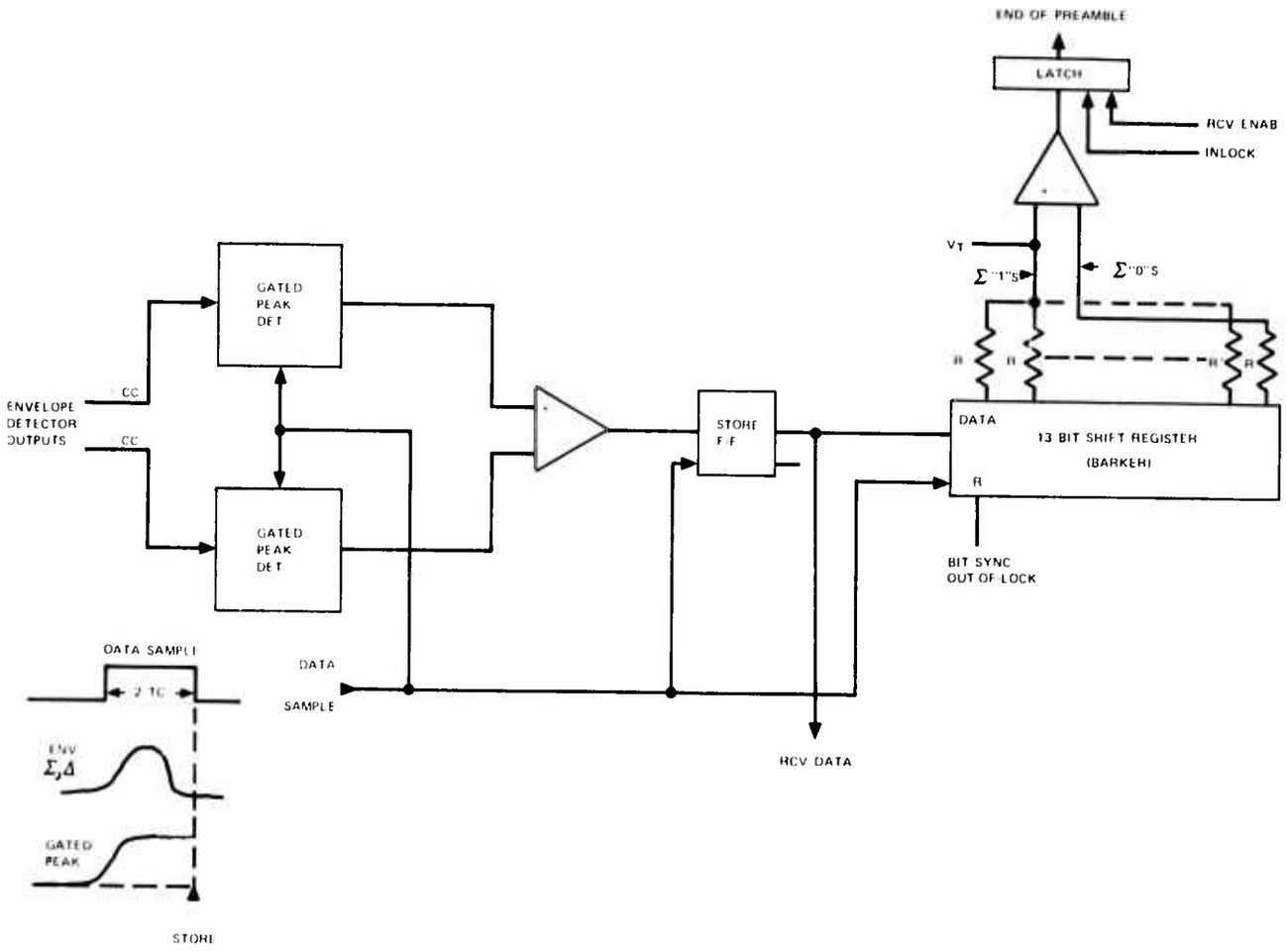

Figure 5-29. End of Preamble/Data Detection.

The Σ and Δ bit envelopes are peak detected and compared to each other. Note that the characteristics of the incoming signals are such that, for valid data, the Σ and Δ signals are complementary. That is, if the Σ signal is a logic 1, the Δ signal will be a logic 0. Thus, the effect of comparing the two signals (Σ and Δ) is to produce a series of 1's and 0's corresponding to the original input coded message. The output of the comparator is serially entered into a 13-bit shift register. The shift register circuit is matched to the 13-bit Barker preamble code. Thus, if a valid signal is entered, the output of the register circuit is a maximum value. This value is compared to a threshold signal. Note the threshold will only be exceeded if a correct preamble is received. Hence, if a threshold crossing occurs in conjunction with an RE flag, an EOP

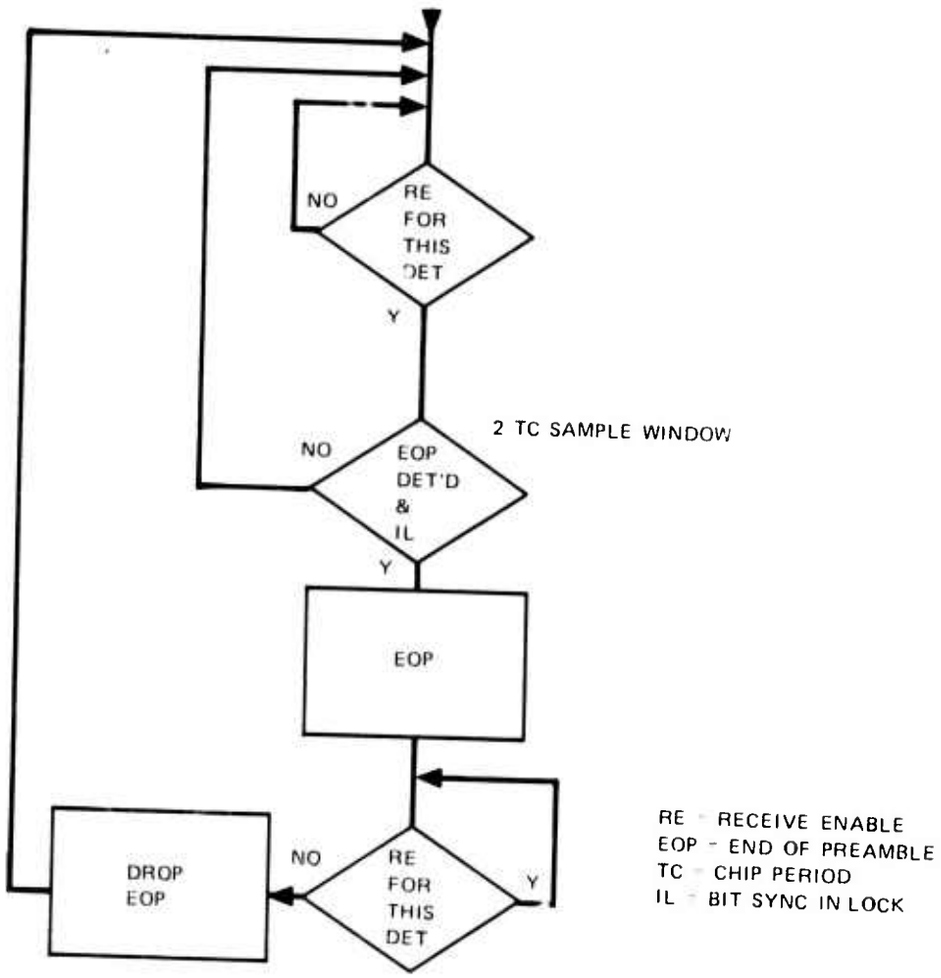

Figure 5-30. End of Preamble Operational Flow Chart.

message is generated. The comparison results in the determination of the "most likely" bit transmitted when both detectors may have substantial output due to high noise or interference levels. The data detector is an integral part of the EOP detector. The data stream emerges from the comparator circuit and is output to the microprocessor.

6.1 GENERAL DESCRIPTION

The digital section of the experimental repeater is illustrated in figure 6-1. It can interface with a radio transmitter and receivers, station processor, and a terminal device. It provides the basic input/output and processing capabilities to implement the experimental repeater functions of:

a. Packet Transmission and Reception

b. Packet Processing and Repeater Control

c. Interaction With an Operator

d. Repeater Development and Test Aids

The experimental repeater is used as a repeater, station front end, or terminal. Additionally, during the experimental phase, the terminal interface is used to provide system test aids.

The digital section of the experimental repeater controls the transmission and reception of packets, buffers (stores) and processes the packets to implement the packet I/O protocol, and implements repeater control functions specified by some packets. For station applications the basic repeater transfers and processes packets between the station and radio interfaces. For terminal applications it interfaces the operator to the packet radio network via radio packet I/O.

6.1.1 Hardware

The major elements of the digital hardware are shown in figure 6-2. The figure illustrates the basic processor and radio, station and terminal interfaces.

The processor consists of the CPU, address register/decode, DMA access control and memory. The CPU is implemented with the National Semiconductor IMP-16 MOS devices and is compatible with the IMP-16C and IMP-16P basic machine languages. The extended instruction set is not implemented. The address decode provides for addressing 4K of RAM and 4K of PROM memory located respectively from 0-4K and 61-65K (1K equals 1024 sixteen-bit words). Additionally, it provides for addressing 64 peripheral interface registers. The DMA access control arbitrates and controls access to memory for the DMA channels.

The I/O interfaces are provided by the DMA channels, interrupt register, and I/O channel. All DMA channels are identical and provide direct memory access (write/read) to the memory for the radio and station interfaces. A DMA channel is required for the radio transmitter, one for each radio detector and two for the station DMA interface. The repeater software initializes the DMA channels via the loading of DMA channel registers. The DMA process then proceeds with no further supervision by the CPU software. The Tx/Rx interface (if.) and station in/out if provide the electrical interfaces to the DMA channel and peripheral devices.

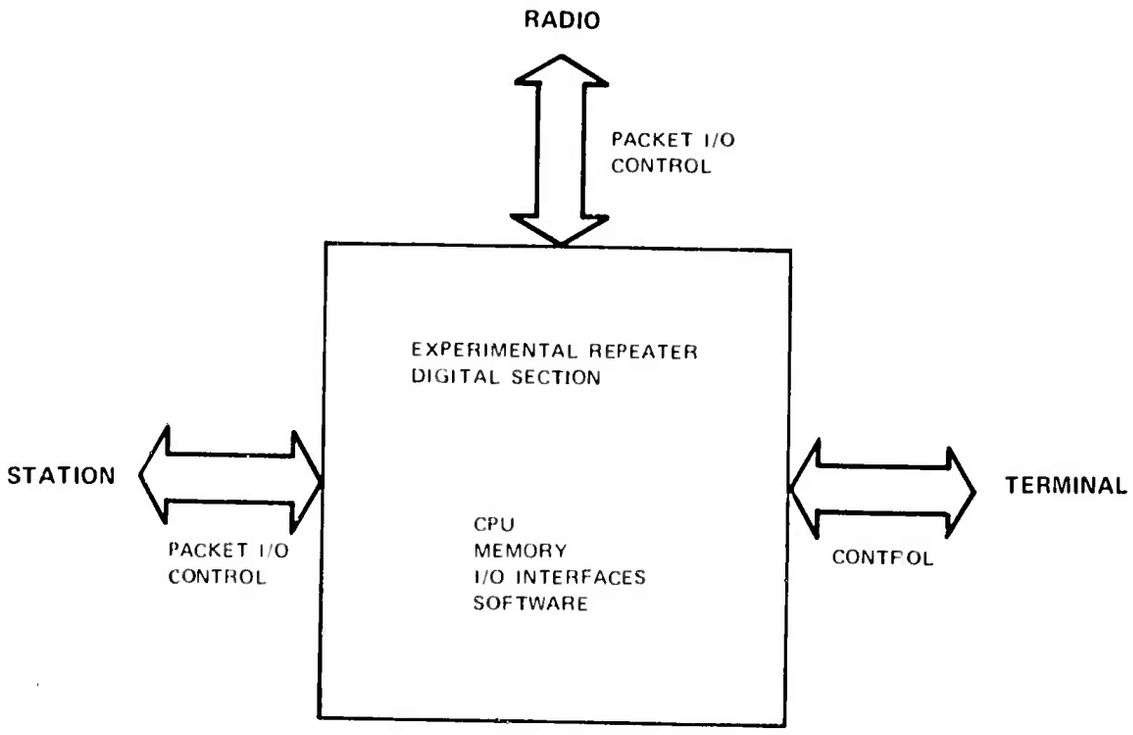

Figure 6-1. Experimental Repeater Digital Section Interfaces.

The interrupt register accessible by the CPU software contains one bit for each device capable of interrupting the CPU. These bits are decoded by the software upon occurrence of an interrupt to determine the interrupt source. Interrupts may occur for each DMA channel, I/O channel, time interval clock, or operator (manual).

The I/O channel provides a character (8-bit) serial interface to a terminal. Initially the terminal shall be a tty/paper tape console.

6.1.2 Software

The software system is a multiprogrammed, interrupt driven system - multiprogrammed in the sense that more than one independent program may coexist in the system and the state of the system is saved and restored as control is transferred from one program to another. The system is interrupt driven in that current programs are interrupted and control passed to other programs for processing as a result of the computer interrupts.

The system is structured into three processing modes described as foreground, background, and executive processing as illustrated in figure 6-3. Foreground processing is reserved for packet I/O and processing. It has higher priority than background processing in that it receives control as a result of computer interrupts from the DMA channels (indicating packet service is required) and maintains control until packet processing is completed. Background processing is, in general, reserved for programs which service the local terminal and low priority programs in the overlay area. Executive processing is reserved for the operating system program and programs which provide system test aids and system visibility for the

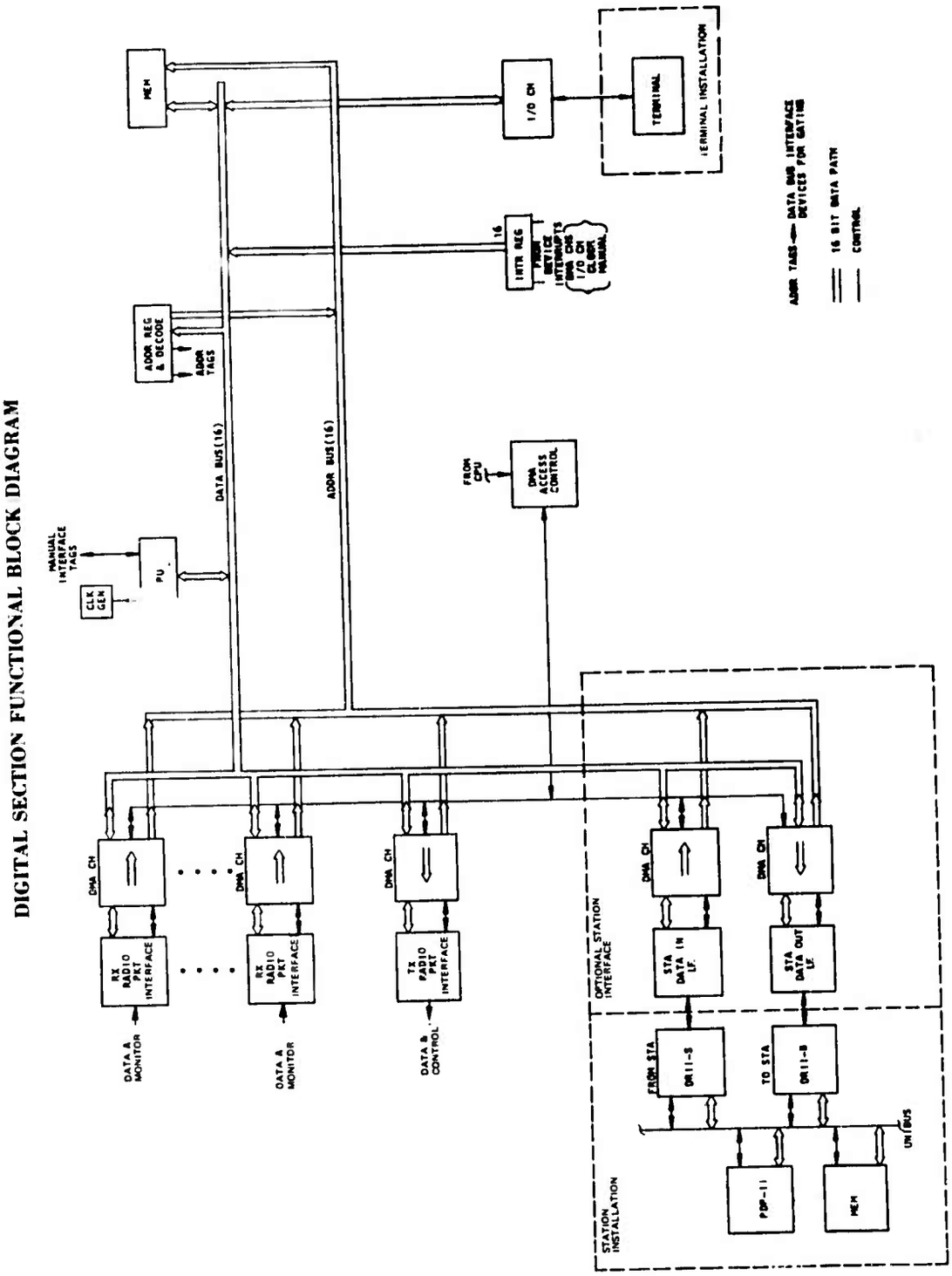

Figure 6-2. Digital Section Functional Block Diagram.

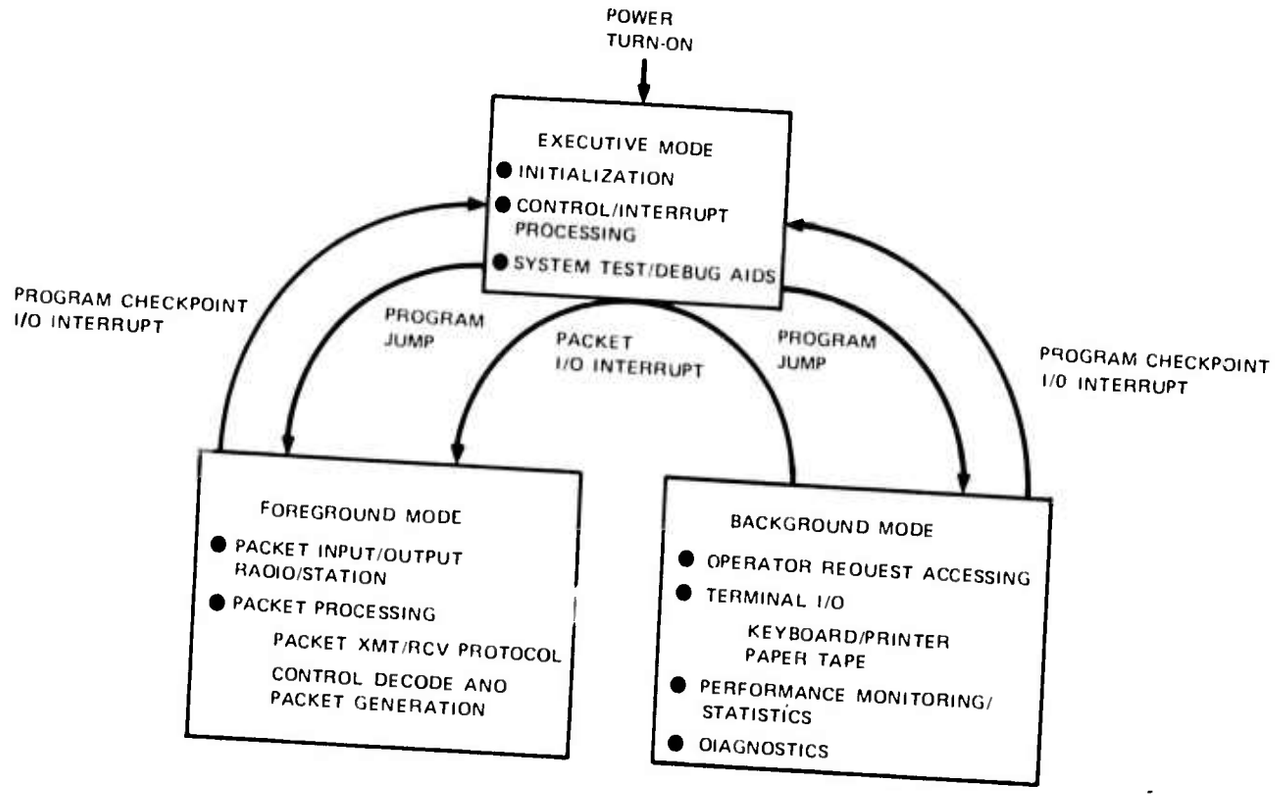

Figure 6-3. Repeater Software Processing Organization.

maintenance/test operator. The executive mode suspends both foreground and background processing to permit system operational snapshots, software/hardware debug, and system test.

Several software routines are provided which can be executed in a foreground, background, or executive mode. These common routines include I/O modules and utilities. When used, they assume the processing mode of the requesting program for the duration of that particular processing task.

The software provides an executive processing mode that can be invoked by an operator at the console keyboard. This mode suspends foreground and background processing until reinstated by the operator. Within this processing mode the operator may inspect the state of the system, display CPU registers, program address counters, display or alter memory and other features required for efficient system testing. Normal operation may be reinstated at the point of interruption or other points at the discretion of the operator at the console keyboard.

6.2 HARDWARE ELEMENT DESCRIPTIONS

6.2.1 CPU Architecture

The CPU is a 16-bit parallel microprocessor configured around the National Semiconductor MOS/LSI devices. These devices consist of four Register and Arithmetic Units (RALU's) and one Control Read Only Memory (CROM). The control and interface circuits external to

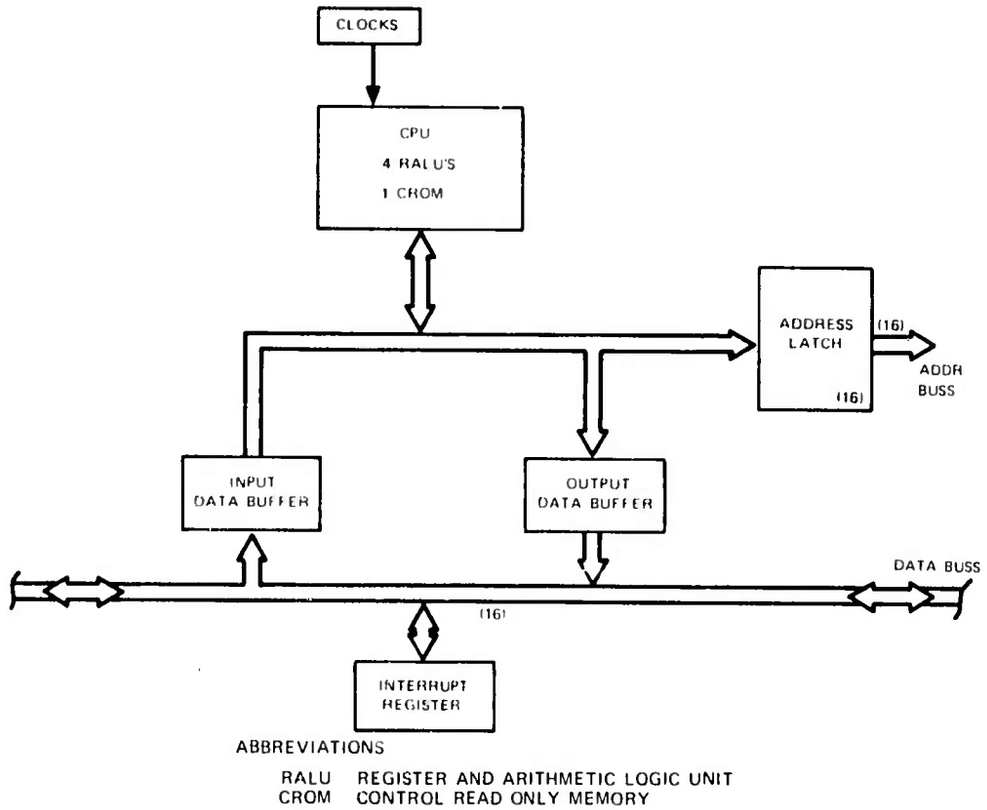

Figure 6-4. Central Processing Unit.

the MOS/LSI devices are implemented with complimentary MOS circuits where feasible to minimize power consumption. Figure 6-4 is a simplified block diagram showing the major functional units.

The CPU is interrupt driven. A single-level interrupt is implemented along with an interrupt status register. It is possible to identify the interrupting device(s) by reading this one register. The software can determine who is interrupting and priorities may be assigned for servicing. An external clock interval interrupt is provided to allow gross time-outs of various functions.

Data to/from memory or peripheral devices and the CPU is gated through the input/output buffers. These buffers allow separation between the internal CPU bus and the external data bus. Data from the CPU which is address information is stored in the address latch. Subsequently, this address is decoded appropriately for accessing a memory location, a peripheral device or a specific external register.

The CPU timing is based on a microcycle. With the low power C-MOS control logic, a microcycle is approximately 4 microseconds. Each microcycle is divided into eight time intervals to control specific events within a microcycle.

The instruction set is implemented with a microprogram contained in the CROM. Each macroinstruction in a program is decoded and directed to the appropriate control sequence entry point in the microprogram. The instruction set consists of 43 instructions.

Conditional jump condition inputs and control flag outputs are provided. These functions are implemented in logic external to the MOS/LSI chips. They are tested and controlled by macroinstructions. A total of four jump conditions and six control flags is available for use.

6.2.2 Memory and Address Organization

Memory will be implemented with solid-state semiconductor devices. Both Random Access Memory (RAM) and Programmable Read Only Memory (PROM) can be used. RAM is used for packet buffers, program overlay areas and other temporary storage. PROM is used to store firmware such as the operating system program.

The addressing structure will locate RAM at the lower address bits and the PROM at the high order bits. Memory is defined and divided in terms of pages. A page is 256 words (x 16 bits) of storage. The addressing structure allows for 15 pages (4096 words) of RAM and 15 pages (4096 words) of PROM. The initial implementation of a repeater will be 2048 words of RAM and 1024 words of PROM. This is based on the preliminary estimate of the operating system software. Additional memory up to 4096 words each can be added by simply adding the memory circuit boards and wiring.

RAM:

Figure 6-5 shows the structure for one page of RAM. A C-MOS memory will be used that is 256 x 1 bit. For 256 words, 16 paks will be required. For 1024 words, 64 paks are required. The C-MOS device was chosen because of its low power consumption.

Operating characteristics are:

Read Cycle Time:	1.2 microseconds
Write Cycle Time:	1.2 microseconds

PROM:

The programmable read only memory is a p-channel, MOS/LSI device that is organized as a 256 x 8 bit memory. Two devices are required to give 256 words of storage. Figure 6-6 shows the structure for four pages (1024 words) of PROM using eight integrated circuits.

The PROM access time is 1.2 microseconds.

6.2.3 Memory Read/Write Timing

The memory timing logic accepts memory cycle requests and allocates memory access. The CPU has priority over the DMA channels. Therefore, whenever the CPU requests a memory cycle, it is granted. The DMA channels bid for a memory cycle asynchronous to the CPU timing or to other DMA channels.

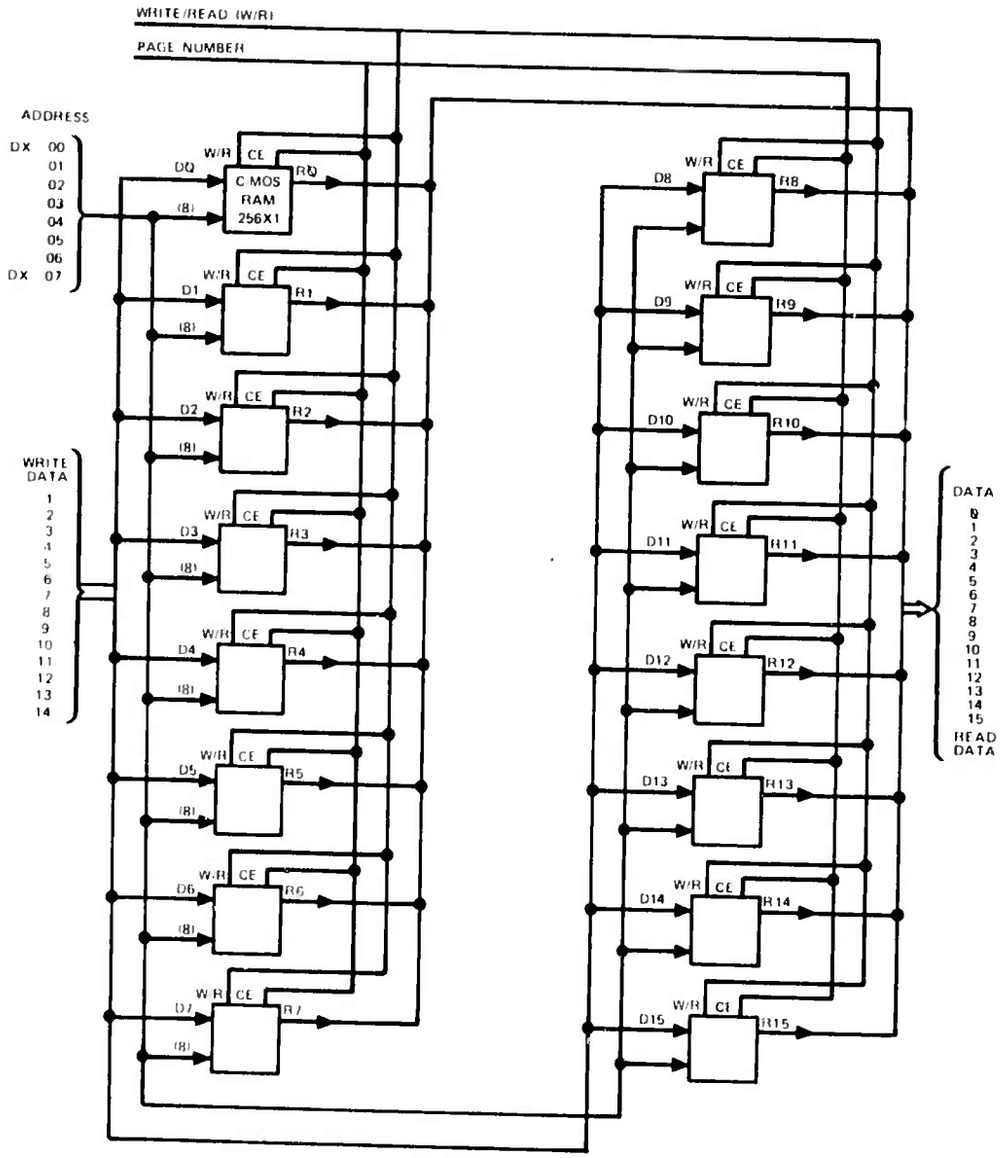

Figure 6-5. Typical RAM Structure (256 Words).

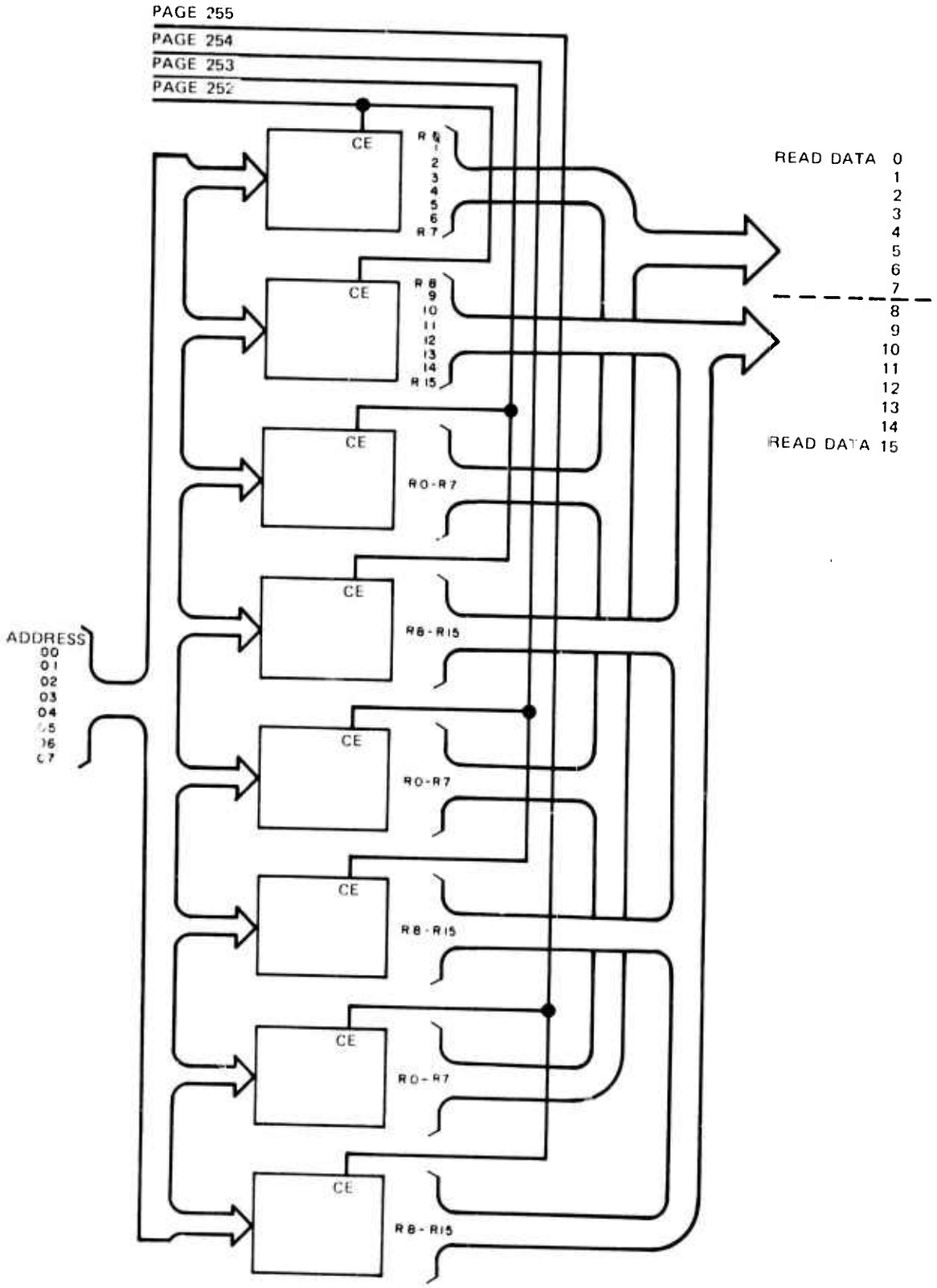

Figure 6-6. Typical PROM Structure (1024 Words).

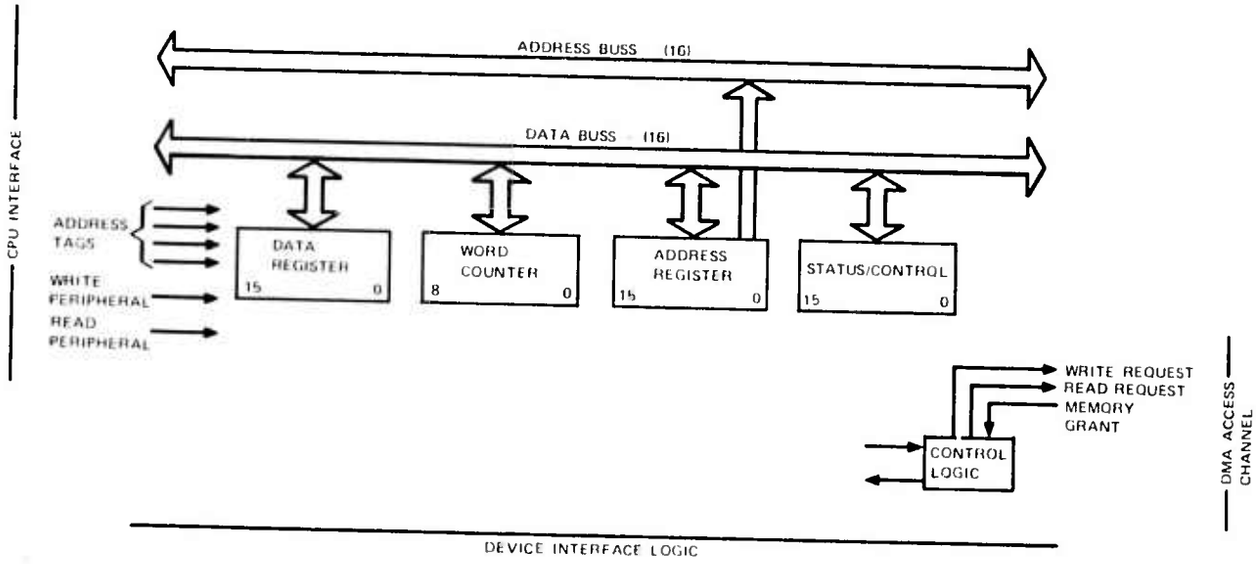

Figure 6-7. Direct Memory Access (DMA) Channel.

In the absence of a CPU memory cycle request, the memory timing logic will allocate memory cycles to the DMA channels on a "cycle stealing" basis. This logic will also provide gating of the timing signals that interface with memory.

6.2.4 DMA Channel

Data is transferred through the various packet interfaces using a direct memory access (DMA) channel. A diagram of the DMA channel is shown in figure 6-7. The hardware is identical for all applications, both transmit, receive and radio and station front-end users.

The logic consists of an address register, a word counter, a data register, a status/control register and control logic. The application of a DMA channel to a specific use is done by assignment of specific bits in the status/control register and by hardware strapping options.

The DMA channel accesses memory on a cycle stealing basis. This is a true cycle steal as the CPU is given priority to seize a memory cycle. The DMA channel can access memory only if the CPU does not make a memory request. When a DMA channel needs to transfer data to/from memory, a bid is made for a memory cycle. Several channels may bid for memory asynchronously. They will be serviced in a rotary basis when a memory cycle is available. The only timing restriction occurs when a channel cannot be serviced before another word is received (data TO memory) or requested (data FROM memory), and overrun occurs. This places a restriction on the data rate and the number of DMA channels that can be implemented. In the experimental system two radio receive channels (data rates 100 Kbps and 400 Kbps) and one radio transmit channel are implemented. Additionally, the two channels required when used as a station front end can be accommodated.

6.2.4.1 Reeeive Data From Radio

Before the radio is enabled to receive a packet, the DMA channel must be initialized. The address register is loaded with the starting address of the packet buffer and the status/ eontrol register is loaded with the appropriate data to enable the radio receive channel. For the receive data application, the word counter is not loaded from the CPU. The packet word length information comes in as a parameter in the packet and is loaded into the word counter. This allows handling variable length packets.

When the sync signal is detected that indicates a packet is being received, the DMA channel causes an interrupt to the CPU and begins to request memory write cycles as the words are received. When the word counter reaches count zero, the packet is complete and another interrupt is initiated to inform the processor of packet complete. The DMA channel then drops reeeive enable line.

6.2.4.2 Transmit Data To Radio

When a packet is ready to transmit, the CPU initializes the DMA channel by loading the address register with the starting address of the packet buffer, the word counter with the number of words in the packet, and the status/eontrol register with the necessary bits to enable the radio transmit channel. The DMA channel will then make memory read requests. When the word counter has counted to zero, indicating the end of the packet from memory, an interrupt to the CPU is generated. The CPU can then return the radio to the receive mode.

6.2.5 Radio Interface

The radio interface contains the interface logic between the modem and the DMA channel of the microproeessor as shown in figures 6-8 and 6-9. This interface logic will contain the following funetions:

- Rx Data Serial/Parallel Conversion
- Cyclic Redundancy Error Check for Rx Data
- Cyclie Redundancy Error Character Generator for Tx Data
- Interface Control Signals

6.2.5.1 Receive Data

When a channel is initialized to reeeive a packet, the CPU will cause Rx enable to go high. When a packet is received, the sync line goes high and the NRZ serial Rx data is cloeked into the serial in/parallel out shift register by the Rx clock. The data is clocked into the error checking circuit as it is received. A word counter counts 16 bits and transfers the word to the data latch. A memory write request is raised to the DMA channel to initiate a bid for a memory cycle.

This sequenee continues until the end of the packet. The error check logic will then determine if an error has been made. The CPU will check the error bit to determine if the packet data is correct. If the error is set, the packet is abandoned.

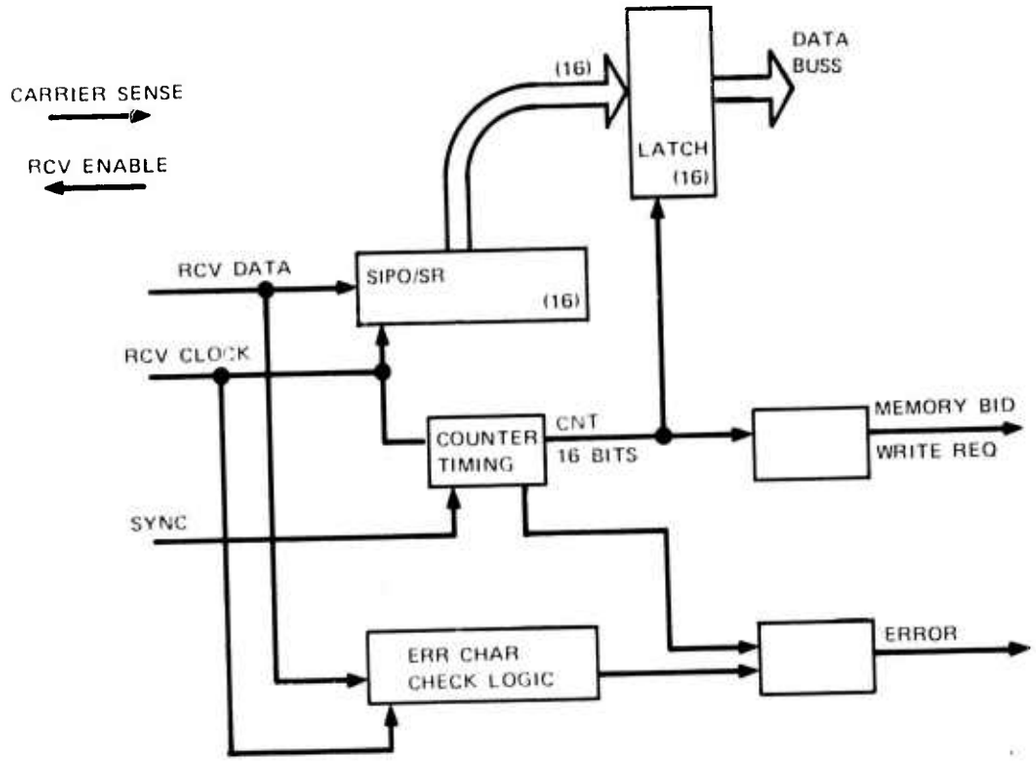

Figure 6-8. Radio Interface – Reeeive.

The packet may be abandoned at any time by dropping Rx enable. For example, the address information in the packet header could indicate that the packet is not intended for this repeater. The CPU could cause Rx enable to drop which would allow the radio to drop syne on this packet. The channel eould then be reinitialized to search for another packet.

6.2.5.2 Transmit Data

The initialization that must occur at this interfaee before transmitting a paeket includes setting the power and frequency control bits and the transmit rate. These eontrol bits are transferred to the interface when Tx enable goes high. The radio will perform its internal functions such as adjusting power, setting frequency, switching the antenna from Rx to Tx, etc. When the radio is ready for Tx data, the bit clock will be returned across the interface. Receiving the bit clock is defined as a data request and the Tx data will be transferred across the interface synchronously.

The complete packet will be sent from memory. This will include the preamble, header, text, and error check word. At the end of the packet, the Tx enable signal will go low. The radio will complete transmitting any bits that are buffered and when all the data has been transmitted will turn off the bit clock to the interface.

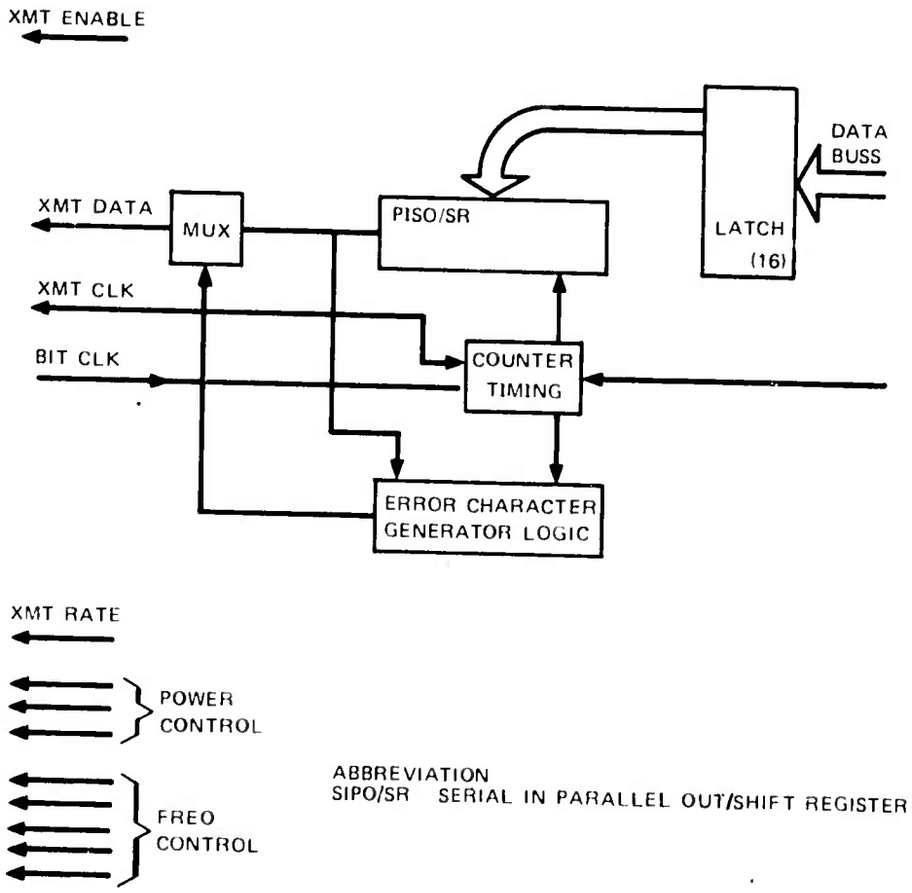

Figure 6-9. Radio Interfaee – Transmit.

6.2.5.3 Remote Installation

For installations whieh require the equipments to be separated, this separation will oeeur at the radio interface. An example of this requirement would be at a station installation where the antenna, rf section, etc., might require locating at the top of a building or other high point, and the processor and other peripheral equipments would be loeated in other parts of the building. Sinee it is desirable to have the flexibility of remote installations, the radio interface is designed to be tolerant of timing variations that result from variable eable lengths.

Separate line driver/line terminator circuits will be required for remote installations. These circuits are not included as a part of the basic repeater. Cable lengths are expeeted to be less than 1000 feet.

6.2.6 Input/Output Device Channel

This I/O channel is provided in the basic repeater primarily as a test/maintenance aid. It also allows a repeater to function as a terminal or drop repeater in some applications. When used as a repeater, the power to the I/O ehannel will be turned off when not in use.

The I/O ehannel (figure 6-10) gives the capability to load programs using KBD or paper tape and to enter/receive packets in the network. The ehannel communicates with the CPU via

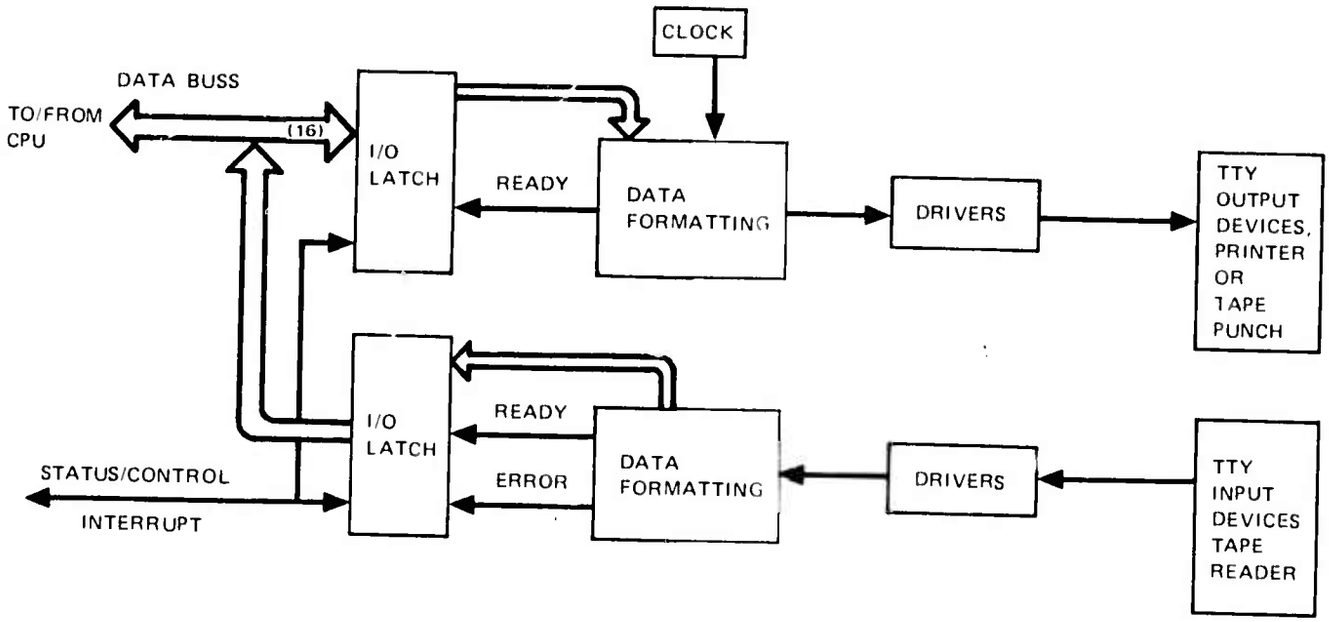

Figure 6-10. I/O Channel.

the data bus in a FDX mode. The status/control/data register is provided. The data formatting for the terminal device (tty) is done in the I/O channel logic.

Drivers and terminators are added to the device interface to convert the RS-232 interface levels.

6.3 SOFTWARE ELEMENT DESCRIPTION

The software elements planned for the initial packet repeater are illustrated in figure 6-11. The elements provide the operating environment and processing capability necessary for the experimental repeater to function as a terminal, repeater or station front end during the initial system/network tests.

6.3.1 Executive Program/Interrupt Process Routines

This program implements the foreground, background, and executive processing modes and provides the path through which control is transferred from one mode to another. It saves and restores the machine state for foreground/background modes represented in the four registers, status flags, program counter, and CPU stack.

The interrupt routines are entered upon occurrence of a CPU interrupt through location 0001_{16}. The routine reads the interrupt register and decodes the source of the interrupt. Interrupts are serviced from:

Clock (fixed time interval)

DMA Channels (radio/station packet I/O)

I/O channel (tty, paper tape console)

Manual (operator)

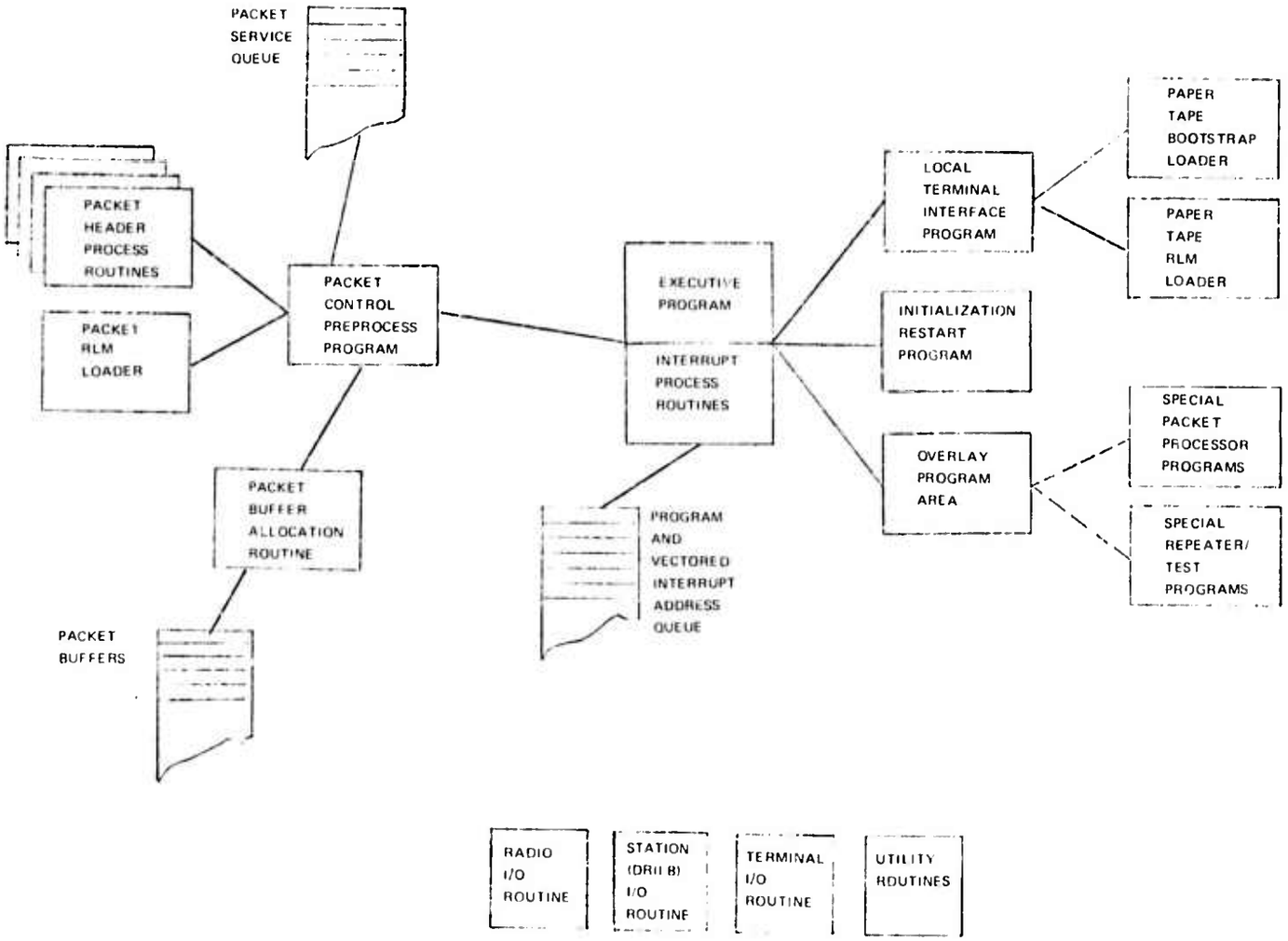

Figure 6-11. Packet Radio Repeater Software.

The clock interrupt routine will increment a location in the memory base page for use by programs that require an estimate of elapsed time.

The DMA channel interrupt routines will, in general, make an entry in the packet service queue for use by the packet handling programs. The entry identifies the packet buffer. The interrupt routine reads the DMA channel registers and stores this information in the appropriate packet buffer. The interrupt signifies the beginning of packet Tx/Rx or packet Tx/Rx complete. The DMA channel interrupt routines will return control to the point of interruption (foreground, executive modes) or checkpoint background and initiate the foreground to immediately begin processing of the packet.

The I/O channel interrupt routine will input or output a single character to the I/O channel (console) per interrupt. An unsolicited special character (to be defined) input shall be recognized as an operator request to enter the executive processing mode to implement the system test aids.

The manual interrupt shall be recognized as an operator request to reinitialize the repeater.

6.3.2 Initialization/Restart Program

This program is responsible for initialization or restart of the repeater software from a power-off state.

Initialization resets the software to an idle, initial beginning state. Any prior operating history is lost. Initialization is normally invoked by the operator turning repeater power on.

Restart restores the software to the prior operating state upon the occurrence of a CPU interrupt from a DMA channel or the operator. The prior operating state is DMA channels enabled to receive packet traffic and the software has removed power from certain repeater elements and halted due to absence of processing requirements.

The program begins at location $FFFE_{16}$ and upon completion enters the executive program to initiate background and/or foreground processing.

6.3.3 Packet Control/Preprocess Program

This program is responsible for packet I/O control and packet processing common to all packets. It requests packet buffers, enables DMA channels, checks for packet errors, decodes the repeater address and packet type code, and calls the appropriate packet header process routine for detailed packet processing. The packet processing sequence is determined by sequential, first in/first out entries in the packet queue.

6.3.4 Packet Header Process Routines

These routines called by the packet control/preprocess program perform the detailed processing of packets. They process a packet in memory, modify the packet header, determine the disposal of the packet, and perform control functions specified by some packets. Several routines shall be required: in general, one for each packet type. Some of these routines shall be unique to the repeater application, repeater station front end or terminal.

6.3.5 Packet RLM Loader

This routine is a special packet header process routine. It shall load software contained in packet text into the overlay program area for execution.

The software shall be contained in Relocatable Load Module (RLM) format records as defined by the National Semiconductor IMP-16 language assemblers.

The loaded programs shall perform their processing function and release the overlay area for subsequent programs. This feature shall be provided mainly for use by special purpose programs (special packet handling, performance monitoring, diagnostics) and other low-use programs, thereby reducing memory requirements for repeaters and terminals.

6.3.6 Packet Buffer Allocation Routine

This routine provides supervision of the packet buffer space. It is called by programs requiring a packet buffer or is called to release previously acquired buffers for reuse by the system. Each packet buffer in memory consists of the following:

a. Preamble (for packet transmission)

b. Packet header, text, error flag

c. DMA channel register values at point of interruption

d. Additional information which defines the processing of the packet (Tx, Rx, requires passive acknowledge, etc.)

6.3.7 Paper Tape Loaders

Two paper tape loaders are provided to load programs or data into the repeater memory. The bootstrap loader loads absolute software or data from the console (I/O channel) paper tape reader. The paper tape format containing binary data shall be as follows:

Word 1	Load address
2	Number of data words
3-N	Data words
N+1	Entry address

The data may be software or packets for test simulations.

The RLM paper tape loader loads software in absolute (non-relocatable) RLM format records as defined for the National Semiconductor IMP-16.

The loaders shall normally be called by the operator via appropriate console keyboard entry.

6.3.8 Local Terminal Interface Program

This program provides the operator at the tty console keyboard with system supervision and control, system test and debug aids, and terminal operation via appropriate keyboard input. The operator directed functions are listed as follows:

a. Initiate programs at defined locations

b. Insert software breakpoints for program trace

c. Display and modify selected memory locations

d. Display CPU; program counter, registers, status, stack

e. Load programs and data from paper tape

f. Dump loadable memory image to paper tape

g. Load and display packet buffers

h. Modify selected parameters which determine packet I/O characteristics

Some functions shall execute in the background processing mode and simulate terminal operation. System test aids function in the executive processing mode.

6.3.9 Radio/Station I/O Routines

These routines shall be called by the packet control/preprocess programs. They shall enable selected DMA channels and control the DMA channel registers as defined by the input linkage. One packet input or output shall be specified per call.

6.3.10 Terminal I/O Routine

This routine shall be called to provide input and output to the I/O channel tty/paper tape terminal. The routine/call shall provide the capability to:

a. Output a message to the printer

b. Input a message from the keyboard

c. Call for tty input (single character)

d. Output a character to paper tape

e. Input a character from paper tape

6.3.11 Utility Routines

Additional routines may be developed which are useful to several programs. These routines shall be callable via indirect jump to subroutine through the memory base page. These routines shall be reentrant or, if in use, appear busy to requesting programs.

Equipment integration, as described in this section, is only directed at packaging and the power system. The interfaces between the radio/signal processing section and the digital section or their subassemblies are covered elsewhere in this document.

7.1 PACKAGING

Since this is intended to be an experimental system, the design is expected to change several times in order that different design and operational approaches can be investigated. The packaging effort is directed at obtaining a total repeater package of 1 cubic foot, but maintaining the flexibility to easily change out functional subassemblies. Figure 7-1 shows the repeater as a pole-mounted package.

7.1.1 Baseline Concepts

a. Repeater Sections. The design technology relates to two major areas: (1) digital and (2) rf and signal processing. The size of the two sections is projected to be about equal. Separation of the experimental repeater into two major hardware groups, allows that the final package can be made square for repeater pole mounting (stacking sections), long and narrow for a man-portable terminal (sections end-to-end), or even two completely separate sections. The interface to the experimental station proeessor will require the repeater digital section to be close to the processor. The radio/signal processing section neeas to be at the antenna to minimize rf losses in cabling to the antenna. Thus, the development of the initial experimental units is based around two equipment sections.

b. Module Functions. In either section, the subassemblies or modules will be printed circuit cards. The objective is to have each major function (frequency synthesizer, data deteetors, bit sync, memory, CPU, etc.) as a separate module. The modules are plug-in. If a different CPU, frequency synthesizer, data deteetion, etc., design is to be tried, the change need not affect the other functions requiring design modifieation.

   This approach does not provide the most compact unit. The seleetion of components and packaging density is only pursued to the point of having a function fit in a module.

c. Module Impact on Package Size. A number of module designs have been developed and are described in the following paragraph. The module packages have been and continue to be evaluated to satisfy the function design. To conform to a card cage design, the height and depth of the modules are fixed. The only variables are module width and quantity. Each card eage section will be approximately 8 inches high and 8 inches deep with the length being determined by the final design of the modules and funetions. Figure 7-1 reflects the quantity of modules required for repeater operation.

7.1.2 Module Design

For most functions, the required circuit area is approximately 30 square inches. An edge-on connector was selected for its simplicity and the wide range of interconnections it allows. For rf

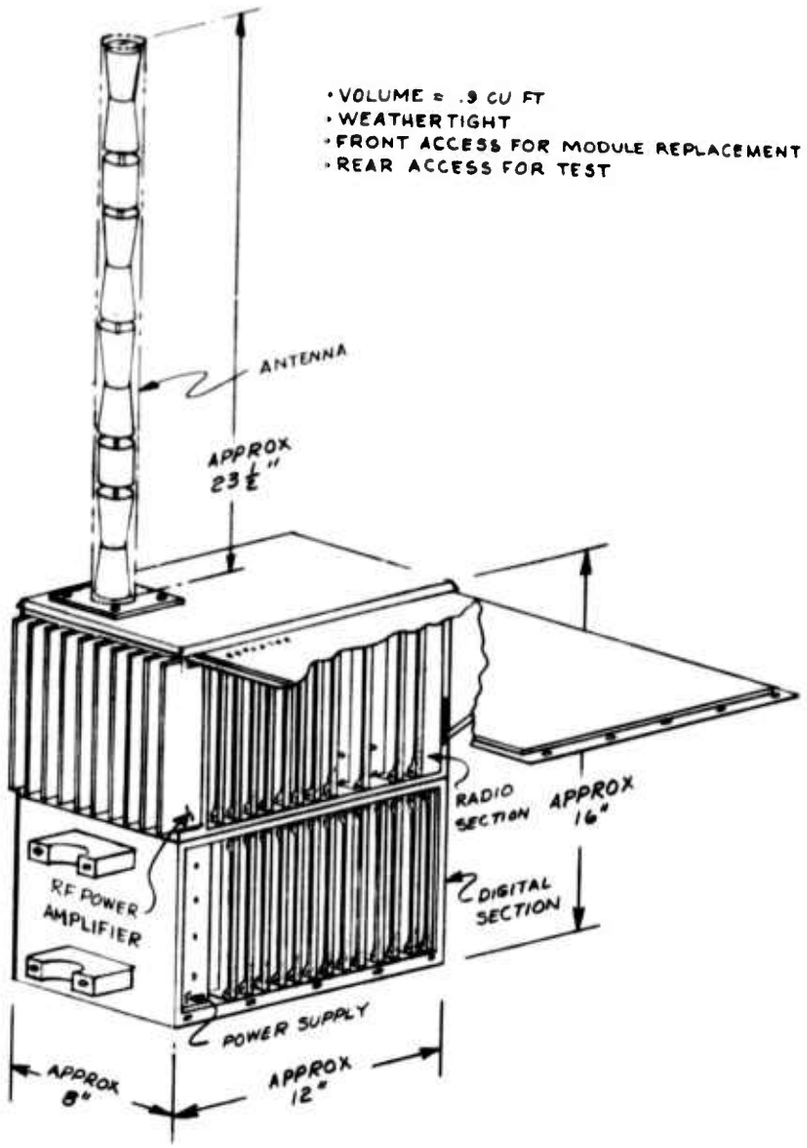

Figure 7-1. Repeater Configuration.

modules, shielding was considered necessary and coaxial connectors were selected to mount to the module shield. The following is a summary of the module designs defined to date.

a. Basic Unshielded Printed Circuit Card. Figure 7-2 shows the basic unshielded circuit card used primarily for the digital circuits. A ground around the usable circuit area allows the addition of a low-grade shield if digital switching produces interferenee. Figure 7-3 shows the low-grade shielded module.

b. Shielded Modules. Figure 7-4 shows a tall shielded module. The circuit card is mounted on standoffs from the edge-on connector mounting board. Figure 7-5 shows the tall shielded module circuit board mounting for one or two circuit cards. The two circuit cards make maximum use of the space. Where tall components are required, such as temperature compensated crystal oscillators (TCXO), this module must be used.

   Not all shielded circuits use tall components; thus, a short shielded module is also used. Figure 7-6 shows this option.

7.1.3 Miniaturization

Where practical and considered necessary, hybrid thin film assemblies are developed using chip components to reduce size. A good example of this is the random access memory (RAM). Use of discrete dual inline packages (DIP), allows 32 DIP to fit on an unshielded board. This provides 512 words, each word being 16 bits. The 30 square inches can be shrunk to a 1.4- x 2.4-inch thin film package that has the same capability. As a result, between 3K and 4K words of RAM memory can be obtained on one board that previously would only hold 0.5K words. This is typical of the magnitude of change possible without using Large Scale Integration (LSI) techniques. The change is a result of removing the input/output space to the circuits. The same problem is present with the circuit card. Area for handles, card guides, and connectors is a significant percentage of the space.

7.2 POWER

The objective of a repeater is to have unattended operation for periods of several months. This means that power drain must be a significant factor in design approach and selection of components. Figures 7-7 and 7-8 show the range of weight and size of batteries to power a device that consumes an average power of 10 to 60 watts. A maximum and minimum range of weight and size are presented on the basis of batteries available on the market. The curves show that power consumption must be minimized to obtain realistic battery sizes.

7.2.1 Design Guidelines

There are two basic considerations in reducing power: (1) low power circuit designs and (2) switching of power so that only needed system functions are ON at any given time. The low-power circuit design means selection of a circuit and obtaining low-power devices to implement that design. The two aspects are also complicated by tradeoffs in circuit space and design simplicity.

In general, the simple design satisfies low power and minimum space considerations. Power consumption must be considered on an equal plane with how to implement the circuit. Complementary MOS (CMOS) circuits require microwatts of power, but operate at slower speeds. Low-power Schottky circuits take less power than conventional logic. Where speed is critical, emitter coupled logic (ECL) can be used, but at a significant increase in power. Shopping around for a component generally reflects a wide range of primary power required. Operational amplifiers can be obtained from the microwatt power range to hundreds of milliwatts.

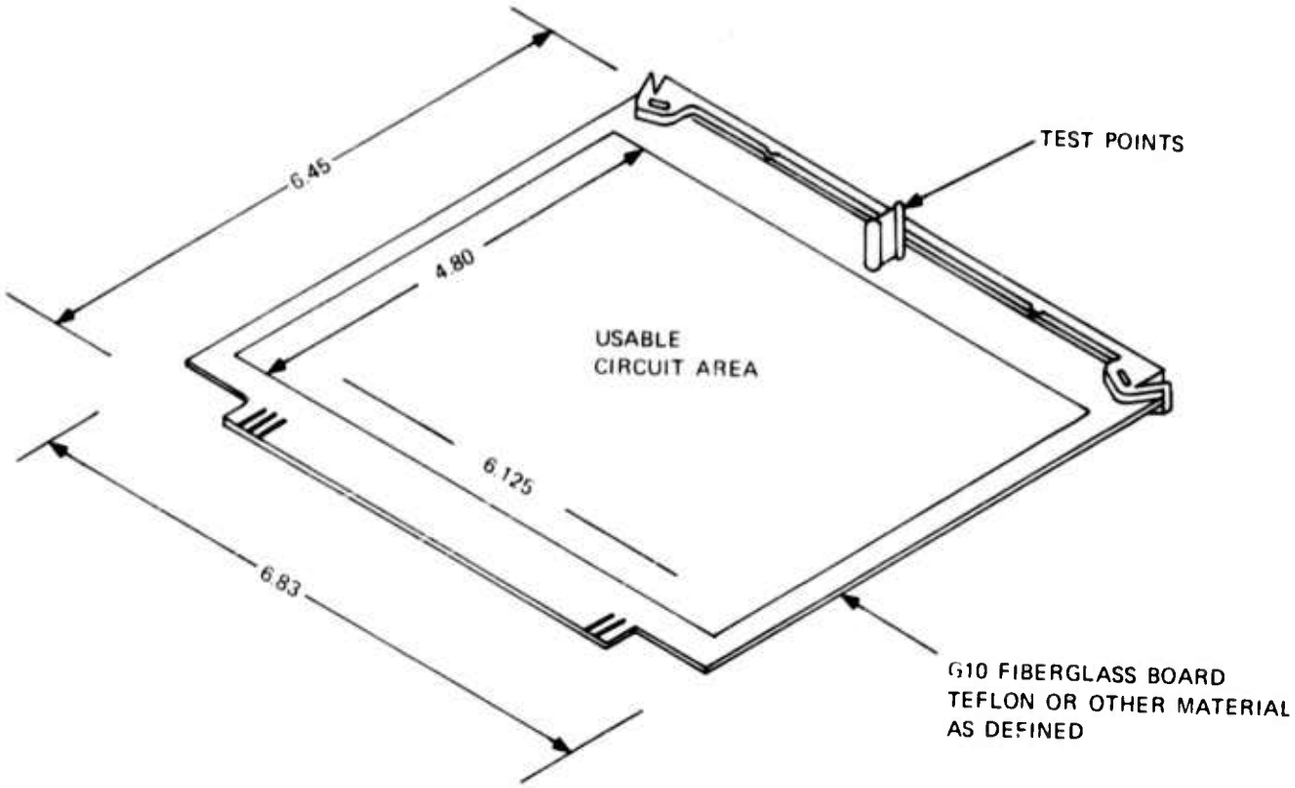

Figure 7-2. General Printed Circuit Board (PCB) Configuration.

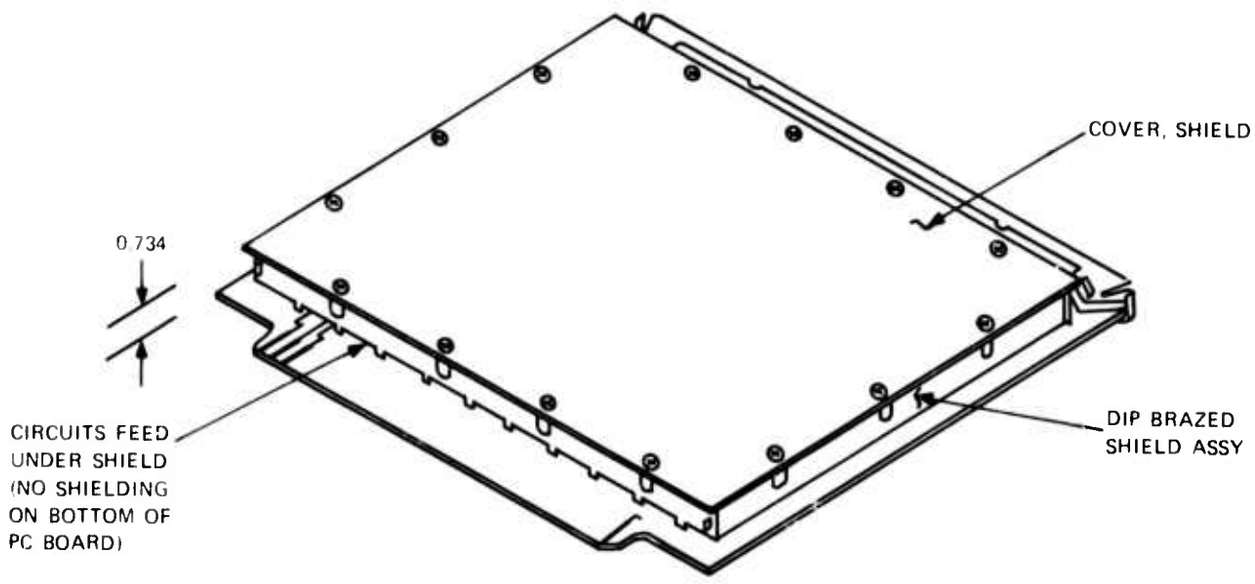

Figure 7-3. Low-Grade Shielded Module.

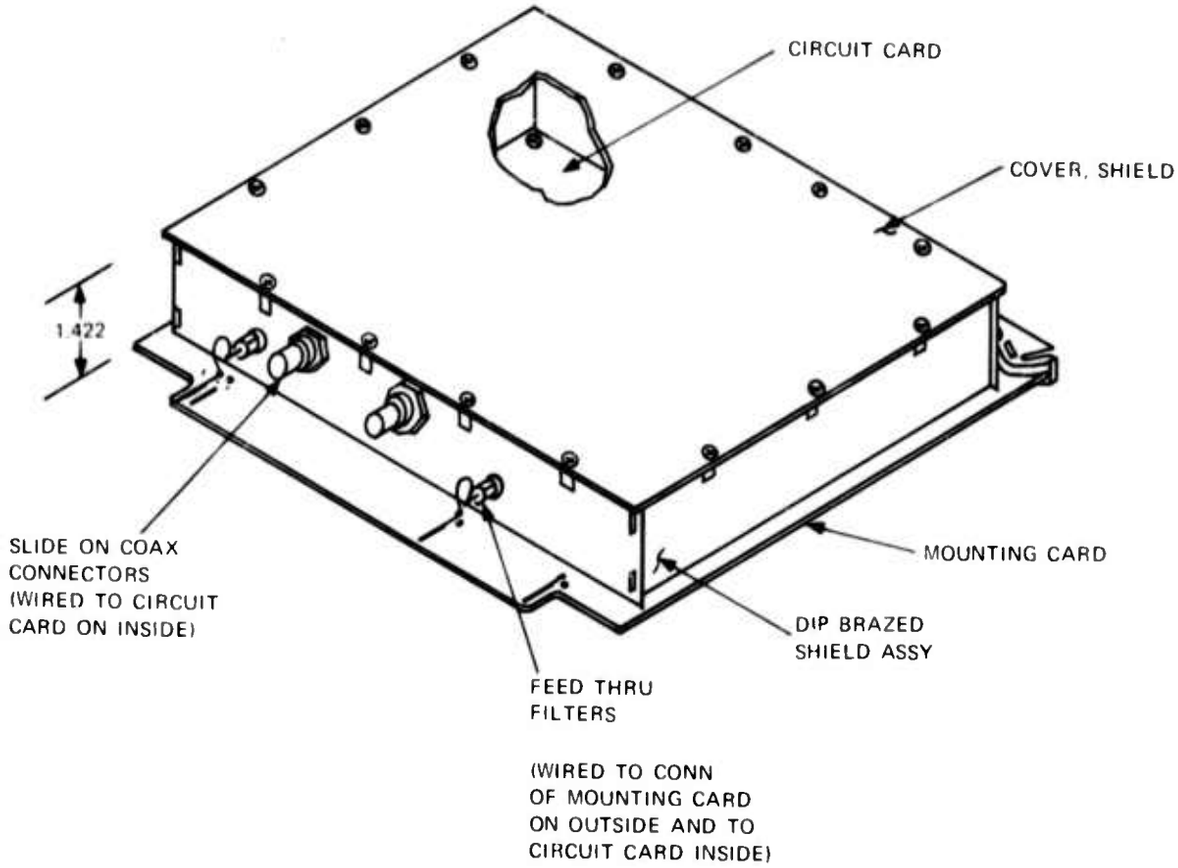

Figure 7-4. Tall Shielded Module Assembly.

Many devices rated at ±15 volts can be operated at ±5 volts, thereby reducing power. This design process is working very effectively to minimize power.

Where the power drain is significant and for a function not always required, turning the function OFF represents power savings. The switching time must be considered early in the design, as has been the case in the present development. The turn-on/turn-off, initialization transients, and the power required to hold the circuit OFF affect this decision. The transmitter driver circuits are OFF when not transmitting. The final output is a high efficiency class C amplifier.

In the processor, the Programmable Read Only Memory (PROM) is power switched on a bit-by-bit basis. The CPU itself is cycled to a standby mode if there is no packet traffic.

A target of 10 watts for a standby receive mode is established. During the transmit time period, 40 to 50 watts are required. This places large surges on the power stream. Most of the surge power is used at 24 vdc for the rf power amplifier.

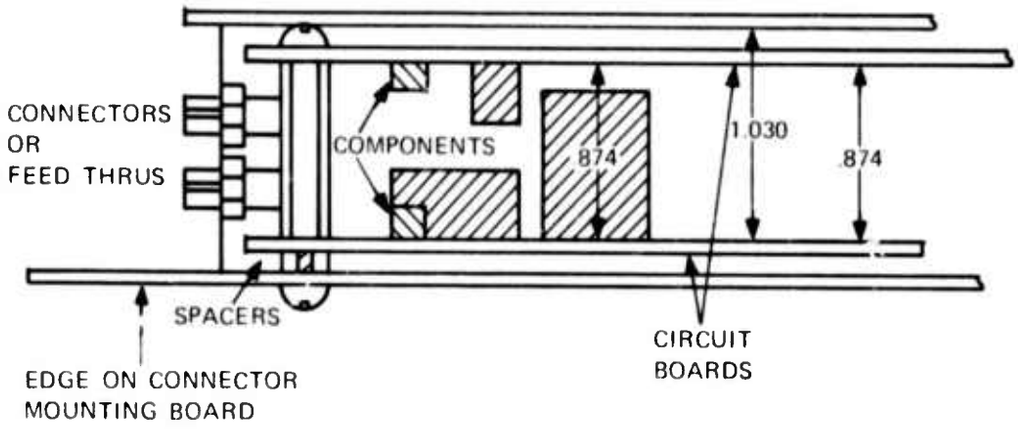

Figure 7-5. Tall Shielded Module Board Mounting.

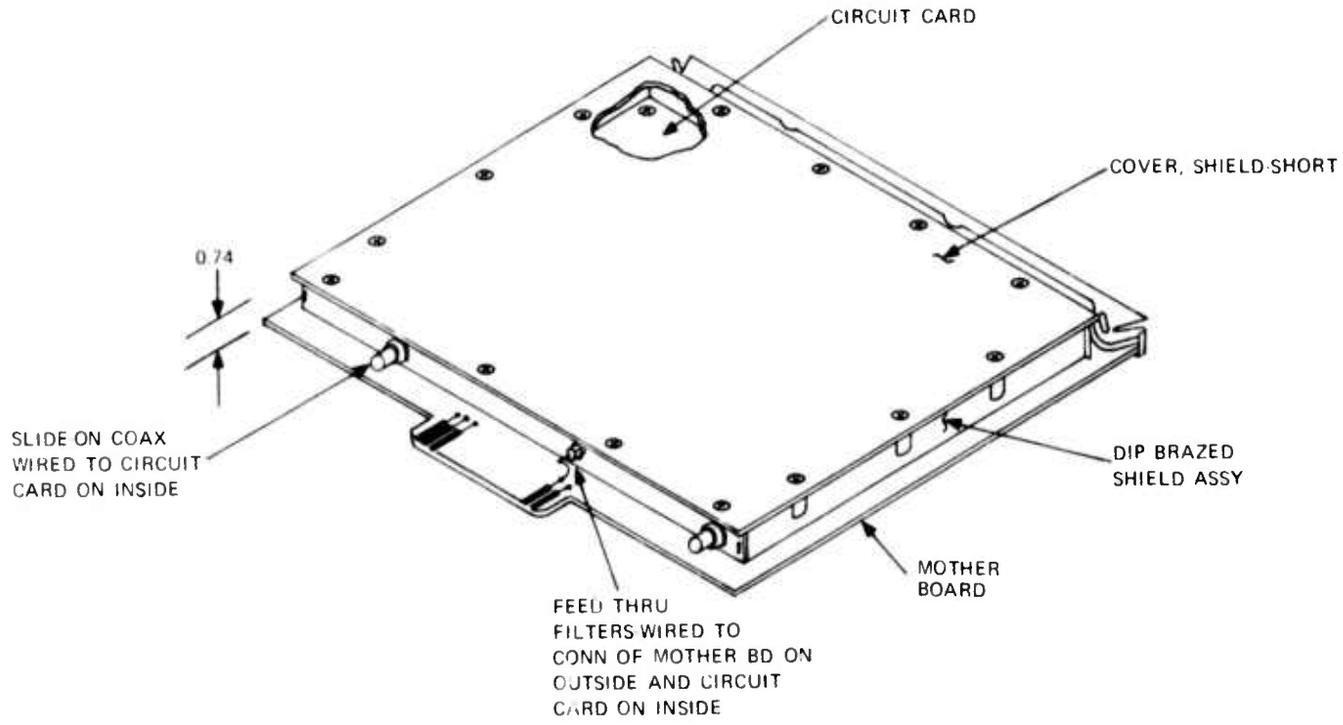

Figure 7-6. Short Shielded Module Assembly.

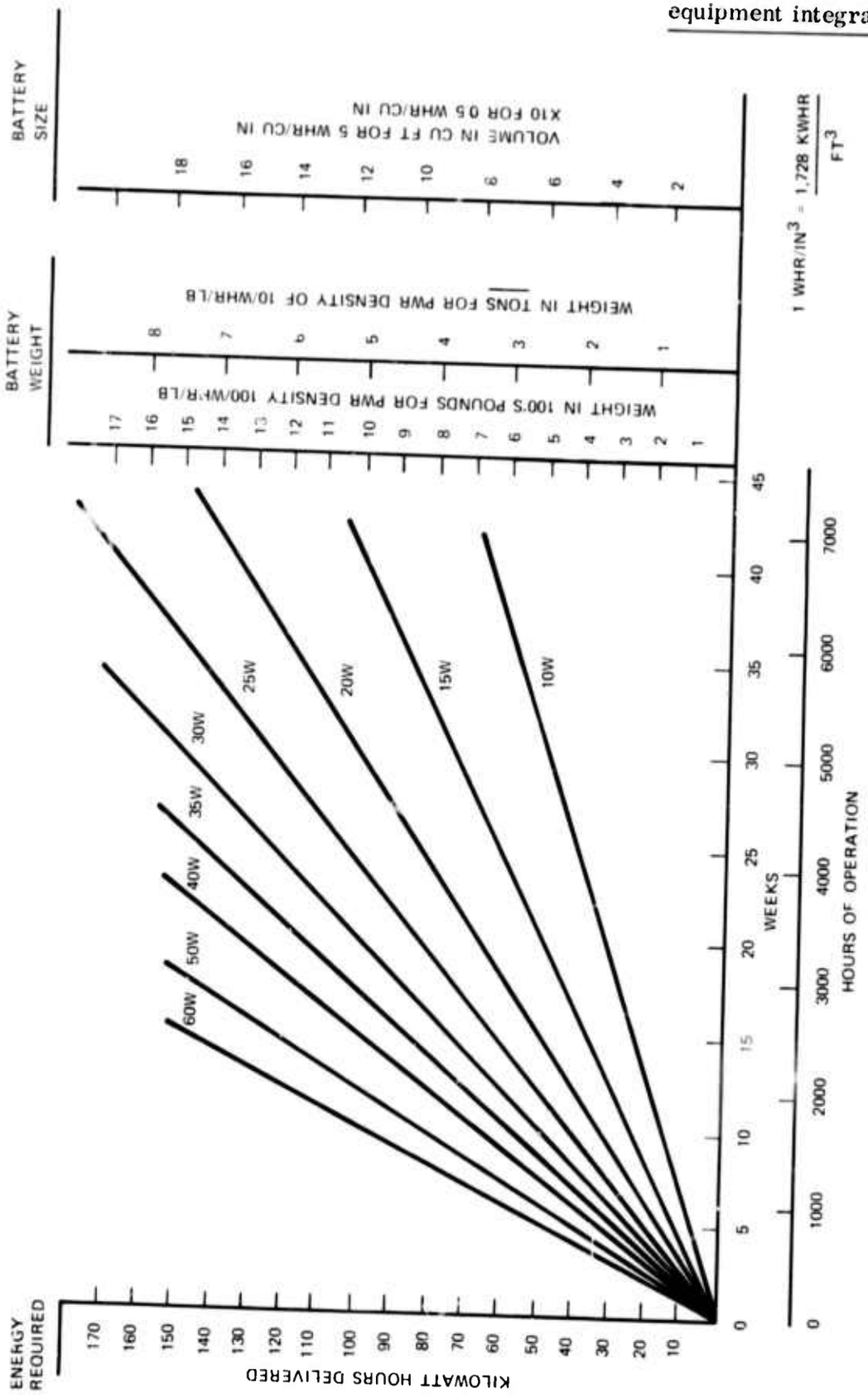

Figure 7-7. Battery Capacity-Weight-Size Versus Duration of Operation (Long Term).

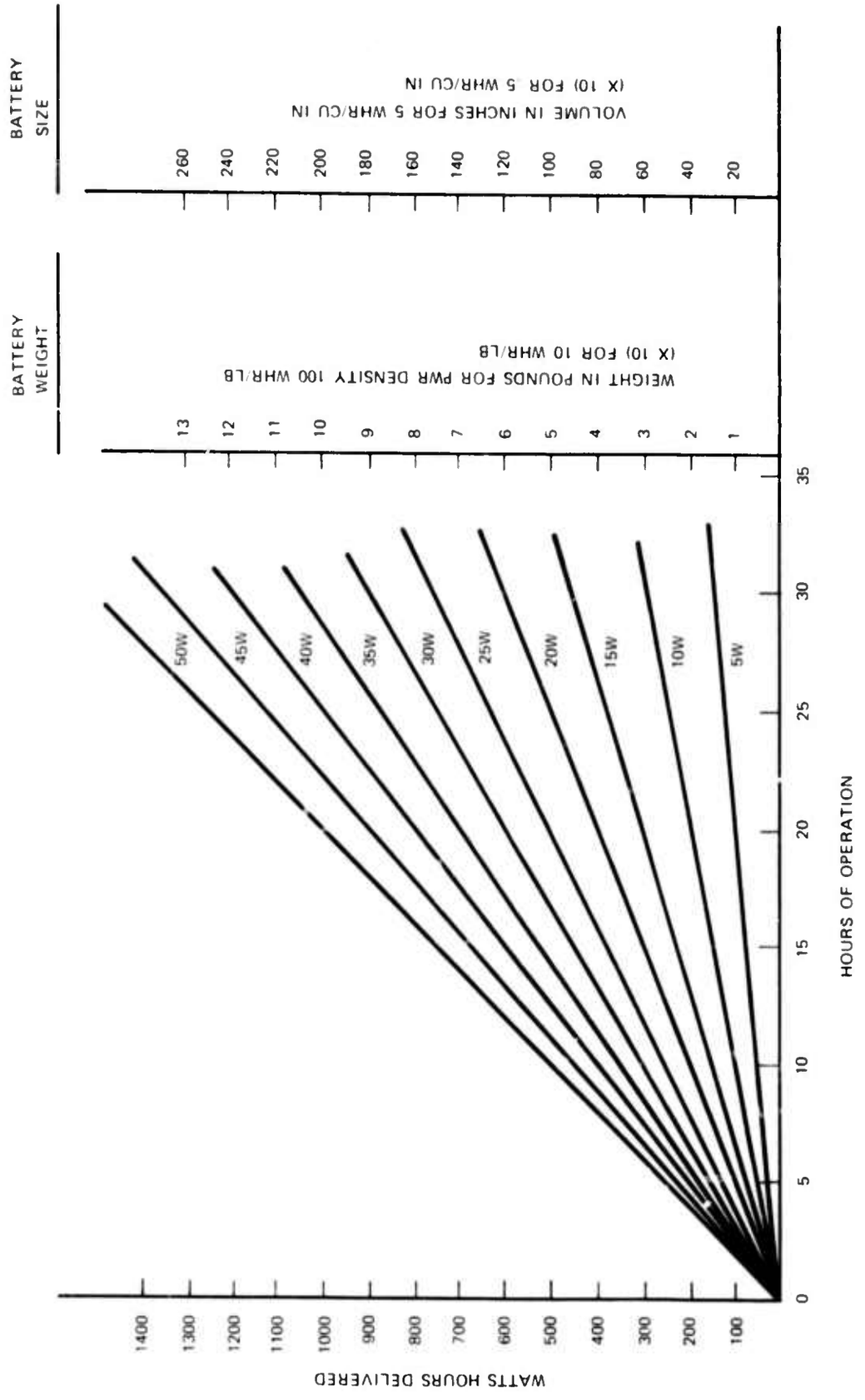

Figure 7-8. Battery Capacity-Weight-Size Versus Duration of Operation (Short Term).

7.2.2 Power Supplies

Due to the high surge power required at 24 vdc, a primary power source of that voltage was selected. The other voltages for the circuits were reduced to the following:

+15V	RF/IF amplifiers, operational amplifiers, and frequency standards.
+5V	TTL and CMOS logic and comparators, and amplifiers operating at reduced voltages.
-5VDC	ECL logic and comparators, operational amplifiers operating at reduced voltage.
-12VDC	PROM's and miscellaneous special circuits.

These voltages are obtained by dc-to-dc converters operating from 24 vdc. The efficiency of the converters ranges from 60 to 80 percent, thus representing a significant portion of the total input power. The operation of the rf power amplifier directly from the dc source improves the overall efficiency.

Switching regulators have been selected for their high efficiency, small size, and low weight. The switching frequency is approximately 25 kHz, allowing simple filtering.