May 1968

R&D OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS

Prepared by

Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania 19422

Prepared for

Massachusetts Institute of Technology
Lincoln Laboratory

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Massachusetts Institute of Technology
Lexington, Massachusetts

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Twelfth Interim Report
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ABSTRACT

A research and development program directed toward the development of high speed computer subsystem fabrication technologies is described and the results of device yield and speed-power dissipation improvements are reported. Small geometry, shallow diffused, npn silicon transistors are utilized in simple ECL circuit forms to achieve high performance at low power dissipation in complex array structures. Various component interconnection technologies are being developed and characterized for high density, high speed subsystems. Multilevel single chip and multichip assemblies are being investigated. Reliability studies of functioning arrays have been initiated.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

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SECTION I - INTRODUCTION

1.1 PROGRAM OBJECTIVES

1.1.1 Phase I

The primary goal of Phase I was the establishment of the technological requirements for achieving very high speed computer systems through the fabrication and use of ultrahigh-speed bipolar digital LSI microcircuit arrays.

1.1.2 Phase II

The goal of this program remains basically the same as that of Phase I except that it has been extended to emphasize the development of compatible methods of assembly of digital subsystems, so that the inherent high speed performance of the arrays is translated most efficiently to the subsystem and system levels.

1.2 SCOPE OF REPORT

This report summarizes the work performed during the period April 1 to December 31, 1967 on Phase I and Phase II of the research and development program, "R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems." The period April 1 to June 30 represents the last quarter of Phase I while the period July 1 to December 31 constitutes the first two quarters of Phase II.

This report is titled "Twelfth Interim Summary Report" because both of the program phases reported on are extensions of Lincoln Laboratory Subcontract No. 295 (Prime Contract No. AF 19(628)-5167) which began in July of 1964. The two programs previously conducted under this subcontract were entitled "R&D of a New Class of NPN Silicon Switch Exhibiting UHF Capabilities" and "R&D Program to Design and Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Times of 1 Nsec."

1.3 AREAS OF INVESTIGATION

1.3.1 Introduction

The basic approach that has been taken on this program toward the achievement of very high digital system and subsystem operational speeds has been to develop compatible LSI techniques around the high speed microcircuit capability that was developed and demonstrated during a previous program. It has been shown that digital bipolar microcircuits which operate at 200-400 ps propagation delays (see Eighth Quarterly Summary Report - R&D Program to Fabricate Digital Monolithic Microcircuits Having Average Propagation Delay Time of 1 Nsec.) can be practically made by proper use of small component geometries (2.5μ) and shallow component diffusions ($\leq$0.5μ). These per-stage speeds could not be realized at a systems level if conventional

microcircuit packaging and system interconnection techniques were used because of the parasitic loading and signal path delay effects inherent to such an environment. LSI promises to allow high speeds at the systems level by reducing the number of packages and system interconnections, thereby providing an environment for the basic gates, flip flops, etc. which has a minimum delaying effect on signal propagation.

The primary goal of establishing the technological requirements for the fabrication, testing and proper implementation of ultrahigh-speed microcircuit arrays has required efforts in a number of related areas including:

a. Continued development of design principles and fabrication techniques for improving the switching speed-power dissipation properties of the basic microcircuit forms which are used as building blocks in the arrays.

b. Optimizing the yield of these building block microcircuits through improving the yield of the components (especially the high frequency, small geometry transistors) which form the microcircuits. As a result of improving the yield, increasing amounts of high speed logic circuitry can be incorporated in a single monolithic silicon chip, thus allowing a reduction in overall system parasitics, with a consequent improvement in speed.

c. Development and optimization of techniques for forming efficient and reliable multilevel interconnection systems for complex microcircuit arrays.

d. Development of techniques of testing complex arrays to high confidence levels.

e. Development of special packages, in some instances, to accommodate the need for a greater number of leads per package.

f. The development of new techniques for the failure analysis of high speed arrays. This effort is complicated not only by the small geometries involved but also by the presence of the multilevel metalizations.

A number of vehicles were mutually chosen by Lincoln Laboratory and Philco-Ford and used in the technology development efforts required in the above enumerated areas. These vehicles are described in paragraph 1.3.2.

A significant portion of the effort in Phase II is being devoted to the development of subsystem assemblies which are compatible with high speed arrays. If subsystem assemblies are to preserve the basic speeds of microcircuits and microcircuit arrays, the assemblies must have minimum degrading effect on speed. The subassembly techniques are briefly described in paragraph 1.3.3.

As microcircuit complexities increase and the device manufacturer becomes concerned with larger portions of systems, there arises a greater need for communication between groups working at the device level and at the systems level. Each group must become more familiar with the other's requirements. Part of the effort in Phase I and Phase II has been to develop clear communication between the microcircuit technologists at Philco-Ford and the systems personnel at Lincoln Laboratory. As one exercise to achieve this communication goal the group at Lincoln Laboratory designed, with guidance and assistance from Philco-Ford, a high speed complex LSI array which is now being fabricated.

One of the natural consequences of increasing the complexity of microcircuit chips is an increase in what has come to be called turn-around time. Turn-around time is the period from the microcircuit fabricator's receipt of a circuit design to his delivery of the equivalent microcircuit or microcircuit array. Lincoln Laboratory and Philco-Ford R&D are cooperating to develop and implement computer-aided microcircuit design and automatic mask making techniques to reduce turn-around time.

Increased chip complexity also complicates the testing of arrays to high confidence levels, and the analysis of failures. Lincoln Laboratory personnel are developing the necessary

programs and hardware for computer testing and failure analyzing the various arrays being fabricated on this program.

1.3.2 High Speed Arrays

Table I lists the high speed arrays which have been either under development or have been designed during this reporting period.

TABLE I

HIGH SPEED ARRAYS USED FOR PROGRAM

Type of Array	Type of Logic	Component Count		Chip Size ($mils^2$)	No. of Pads	Levels of Interconnects
		Transistors	Resistors			
3-Bit Parity	ECL	40	18	30 x 34	12	2
9-Bit Parity	ECL	160	72	45 x 51	23	3
27-Bit Parity	ECL	520	234	90 x 85	59	3
1 x 1 Functional Multiplier	ECL	120	54	60 x 34	15	3
1 x 1 Associative Memory	RTL	21	25	32 x 30		2
4 x 4 Associative Memory	RTL	352	424	96 x 75	26	3
16 x 16 Read Only Memory	E.F. Transistor	256	---	42 x 42	32	2

Fundamentally, all of the above arrays except the Read Only Memory are test vehicles intended to present the various challenges of design, fabrication and testing that are characteristic of small geometry, high speed LSI arrays.

The Parity Arrays, employing nonsaturating ECL, were the first vehicles to be investigated. They differ from one another mainly in complexity, as indicated in Table I, and therefore serve as valuable guides in characterizing process yields and in determining the optimum chip size for small geometry arrays fabricated with our present laboratory technologies. The 3-, 9- and 27-Bit Parity Arrays are formed by interconnecting 1, 4, and 13 parity cells, respectively, through the use of multilevel interconnects. A detailed description of the parity cell was given in the Tenth Interim Report.

The 1 x 1 Functional Multiplier Array (FMA) has been designed by appropriately interconnecting the components of three parity cells. Basically an exercise in implementing the universal cell approach to LSI, this FMA also serves as a vehicle for examining the effect on array yield of what we believe to be an improved multilevel interconnection design. Although the 1 x 1 FMA and a 1 x 4 version were both originally intended to be implemented in the arithmetic section of the central processor of a medium size computer, the decision

was made to design a more universal basic cell and consequently redesign the arithmetic arrays. Functional evaluations of the present 1 x 1 FMA will help determine the more optimum cell design.

The 1 x 1 and 4 x 4 Associative Memory Arrays (AMA) are relatively simple and complex arrays, respectively, employing saturating RTL. Besides representing a microcircuit array design which originated basically with a systems technology group (rather than with device technologists), these arrays are intended to permit investigation of the technology requirements for fabricating high speed saturated logic arrays.

The Read Only Memory (ROM) is an array which is to be used as a microprogrammer. Presently designed as a high speed transistor array (common emitter configuration), it has the flexibility of being programmable at either the wafer level or package level.

1.3.3 Subsystem Assembly Techniques

As a second goal, Phase II calls for development of compatible methods of assembly of high speed digital subsystems.

Conceptually, the method of obtaining the highest speed per circuit stage in a digital system is to maximize the component density per chip and thereby minimize the number of packages required in the system. Signal delays due to interconnection

path lengths and capacitive loading contributed by packages are thereby minimized. Furthermore, because of reduced loading, the reduced requirements for drive circuitry will result in the ability to design more logic onto chips of a given size. Since practical chip size will ultimately be limited by device yields and photomask process limitations, a subsystem assembly technique is required which will make use of the optimized chips (optimized in terms of yield and performance) and yet preserve the high speed inherent to the chips by maintaining minimum signal path lengths and minimum package parasitics. A wafer-chip assembly approach which employs face down bonding techniques developed by Philco-Ford* has been the first subassembly technique to be investigated.

A face down bonded version of the 9-Bit Parity Checker employing 3-Bit Parity Arrays as circuit chips, has been the vehicle selected for investigating this technique.

1.3.4 High Performance Microcircuits

One of the tasks of the programs has been to continue developing improved microcircuit design techniques, using relatively simple microcircuit forms as vehicles. Two ECL 3-input gate microcircuit designs are being investigated.

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*Kraynak, P. and P. Fletcher, "Wafer-Chip Assembly for LSI," 1967 Internation Electron Devices Meeting, Washington, D.C., October 16-18, 1967.

Both microcircuits are emitter follower input current switches and have been designed to have a low propagation delay-power dissipation product. One (designated SMX9) emphasizes ultrahigh-speed (<200 ps propagation delay); the other (designated SMX8) emphasizes very low power dissipation (1 mW) at moderate speeds (1 to 2 ns propagation delay).

Special techniques employed to attain the design goals of these microcircuits include the implementation of micron geometries, two level metalization and tantalum resistors.

SECTION II - SPECIFIC DEVELOPMENTS DURING REPORTING PERIOD

2.1 SUMMARY

During the earlier part of this reporting period successful array fabrication was hampered due to environmental problems related to our relocated laboratory facility at Blue Bell. Intensive remedial efforts, however, led to subsequent restoration of class 100 clean room conditions to the critical fabrication areas and the achievement of transistor yield levels (>90%) higher than that previously experienced (≈90%) in our laboratory facility at Lansdale.

Additional improvements in array transistor yields at the microcircuit level have been achieved through appropriate improvements in mask making techniques, microcircuit design, diffusion processing and wafer handling techniques. Process changes aimed at improving yields throughout the processing of multilevel structures have also been successful to the extent that defect densities in the deposited insulating layers have been substantially reduced, and the problem of open and high resistance vias which previously plagued small area vias has been drastically reduced. This overall improvement in array technology has resulted in as many as 47 functional 3-Bit Parity Arrays per wafer. This represents a 12.4% array yield and a calculated 95% transistor yield (assuming random defect densities).

Based on this and similar data including wafer mapping of functional 3-Bit Parity Arrays it appears that successful fabrication of arrays of the complexity of the 1 x 1 Functional Multiplier and the 9-Bit Parity Array (the equivalent of three and four 3-Bit Parity Arrays, respectively) are now possible. Wafer lots of both these array types are being processed.

Designs were completed, photomasks were obtained and processing was begun on the 1 x 1 Functional Multiplier Array and the 1 x 1 and 4 x 4 RTL Associative Memory Arrays. Processing of the 1 x 1 Functional Multiplier Arrays is nearly complete.

Preliminary design has been completed for a 16-word, 16-bits-per-word, bipolar transistor Read Only Memory Array. Final design will be completed early in the next quarter. This array, which will attempt to use fusing to provide flexible "off the shelf" programing, will either itself be used in the central processor of a medium sized (3000 word) computer or will be used as a debugging vehicle for a 64-word, 64-bits-per-word version which is being planned.

The wafer-chip (interconnection substrate) for the face down bonded version of the 9-Bit Parity Checker has been designed and fabricated. Initial attempts at assembling the 9-Bit Parity Checker subsystem by the face down bonding of 3-Bit Parity Arrays indicated the technique is very promising and can be expected to lead to single package, very complex, high speed LSI subsystems in much

less time than would be required (because of various yield factors) to build a single monolithic chip having the equivalent circuit complexity.

The first wafer of discrete 1 mW, complementary output, ECL microcircuit gates (SMX8) was fabricated and evaluated during this period. Initial evaluations indicate that the 1 mW, 1 to 2 ns performance goal defined for this microcircuit might be difficult to attain unless parasitic capacitances can be further reduced. The lowest raw circuit delay obtained at 1 mW operation has been 6.3 ns. Propagation delay was reduced to 3.5 ns by increasing the circuit power dissipation to 2.5 mW.

An ultrahigh-speed monolithic ECL gate (SMX9) employing micron transistor geometries, and intended to operate at propagation delays of less than 200 ps, is also being fabricated. The first samples of this circuit are expected during the next quarter.

2.2 ARRAY FABRICATION

The implementation of small geometry, high performance LSI presents many and varied challenges and problems in all phases of array design, fabrication, test and use. High speed arrays have critical structural requirements and constraints (i.e. small geometries and shallow diffusions) which intensify the normal yield loss factors. Early during this period we found that considerable additional effort was needed to improve device yields. Consequently a major effort involved the critical investigation of all facets of array design and fabrication (including array photomask fabrication) in order to minimize the yield loss factors.

Yield loss factors can be categorized into two groups:

1. Factors related principally to fabricating array substrates to the microcircuit level or first level of metal.
2. Factors related to fabricating the multilevel interconnection structure.

2.2.1 Array Yields at the Microcircuit Level

Detailed analyses of arrays fabricated throughout this period have led to a number of design and process changes specifically aimed at improving yields at the microcircuit level

(especially the transistor yield). It was found during the analyses that yield losses, to varying degrees, were attributable to:

1. Environmental dust conditions
2. Environmental related impurity contamination
3. Wafer handling techniques
4. Process-induced dislocations in the silicon substrates
5. Misalignment and misregistration of photomask patterns
6. Photomask pattern variations

2.2.1.1 Laboratory Dust Counts

At the beginning of this reporting period it was found that the environmental control system in our new laboratory facility was not adequate for consistently maintaining class 100 clean room conditions. Subsequent strategic improvements in air filtration and pressurization, however, resulted in much improved dust control.

2.2.1.2 Environmental Contamination

Newly instituted in-process quality control tests revealed a trace n-type contamination of array wafers being processed. It was believed that this contamination strongly contributed to the fluctuating transistor yields which were experienced. Sample

transistor yields varied in the range of 50 to 90%, whereas previously the yields were consistently in the range of 80 to 90%. Removal of the source of contamination helped restore transistor yields to the previous levels.

2.2.1.3 Handling Techniques

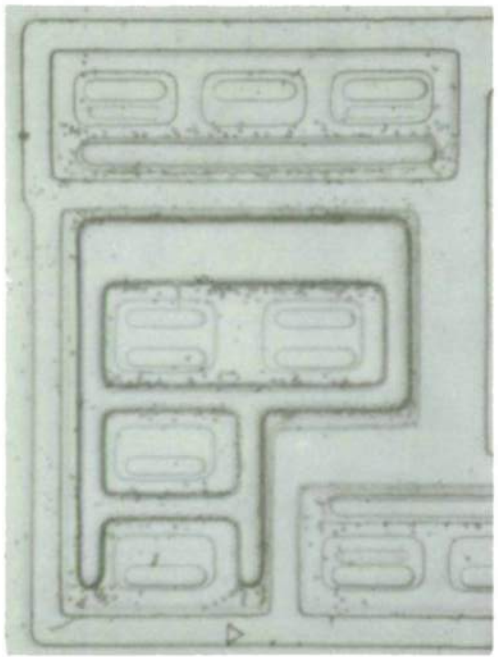
Special precautionary procedures have been instituted to keep wafers completely enclosed except when they are being handled in clean ambients. As a further measure to maintain the ultimate in wafer environment, laminar flow wafer cleaning stations and laminar flow furnace loading ports which will be joined by a pass-through are being procured. When installed, they will not only insure that virtually no room dust can enter and contaminate the diffusion tubes, but also will allow wafers to be processed through the critical steps from cleaning through diffusion (or oxidation) under ultraclean environmental conditions.

In addition, the handling of individual wafers is being done by means of special pickup tools wherever possible. These handling aids reduce the defects caused in the photoengraved patterns of wafers during normal handling in photoresist processing because the wafers, although "held" by the tools, never come in contact with them.

2.2.1.4 Process-Induced Dislocations

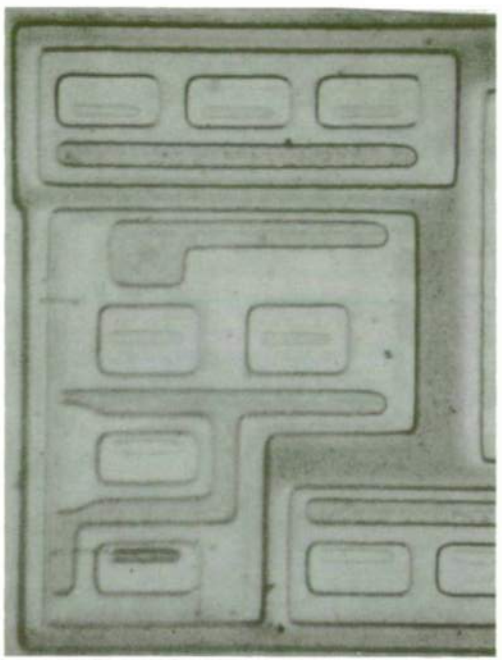
Process-induced dislocations also appear to have been a major cause of transistor E-C (emitter to collector) and E-B (emitter to base) shorts and, consequently, a major cause of yield loss in arrays. Excellent correlation has been obtained between transistor and array yields and dislocation densities attributable to a high concentration (10^{21} atoms/cc) collector diffusion (feedthrough diffusion) which was performed immediately after oxidation of the epitaxial layer for purposes of reducing collector resistance in transistors. It was found that these dislocations can be avoided by either reducing the doping concentration during this diffusion or by eliminating the diffusion. Figure 1 shows samples of 3-Bit Parity Array wafers representative of the effect of 10^{21} atoms/cc, 10^{20} atoms/cc, and no collector feedthrough diffusion on visibly detectable dislocations, and on measured transistor and array yields. (Dislocations are made visible by subjecting wafers to a Sirtl dislocation etch.)

All ECL arrays are now being processed without the feedthrough diffusion. In the fabrication of RTL arrays, feedthrough diffusion may be necessary to control $V_{CE(sat)}$ and storage time but the diffusion will have to be restricted to a surface concentration level of 10^{20} atoms/cc.



Wafer No. 12B

Wafer No. 4B



Wafer No. 14B

Wafer No.	Surface Concentration of n+ Collector Feedthrough Diffusion	Transistor Yield
12B	10^{21} atoms/cc	30%
4B	10^{20} atoms/cc	95%
14B	No n+ diffusion	93%

Figure 1. Effect of diffusion-induced dislocations on transistor yield.

2.2.1.5 Photomask Misregistrations and Misalignments

Analyses of processed wafers have shown that misregistration between photomask patterns have also affected yields. Techniques were developed to minimize misregistrations occurring during the step-and-repeat operation of mask generation.

In general, on small geometry microcircuit arrays, the designed patterns and spaces (0.1 mil in many cases) serve as excellent alignment aids in themselves. However it was found that there are cases when auxiliary alignment aids can improve overall alignment accuracies. Appropriate alignment aids have been designed and tested, and will be implemented in all future layout designs.

2.2.1.6 Photomask Pattern Variations

It has been found that in certain cases, photomask patterns which are designed to have the same dimensions, do not reproduce identically during photomask fabrication due to pattern-optics interactions. That is, two patterns of identical geometric dimensions can reproduce differently, depending on the pattern environment surrounding the two. The effect has been predominant on metal interconnection masks and has had an adverse effect on microcircuit yields, principally by causing electrical opens. To minimize this effect, certain metalization contact linewidths have been increased to 0.15 mils wherever possible while still maintaining 0.1-mil spacings.

Implementation of the appropriate technology improvements discussed in subsection 2.2 resulted in improved transistor yields such that yields greater than 90% are consistently being obtained. Transistor yield is sampled by measuring 100 randomly selected transistors on each wafer at the microcircuit level, using a special test metalization pattern which is replaced by the array cell metal pattern after the testing. Table II shows the improved transistor yields measured in this manner on four of the first 3-Bit Parity Array wafers to be fabricated using the improvements cited above.

TABLE II

TRANSISTOR YIELDS MEASURED ON ARRAY WAFERS
MADE WITH IMPROVED TECHNOLOGY

Wafer No.	Transistor Yield	Failure Causes		
		E-B Leakage	E-C Leakage	C-B Leakage
14D	92%	6%	1%	1%
17A	97%	2%	1%	0%
17B	96%	0%	4%	0%
17C	97%	1%	2%	0%

2.2.2 Multilevel Interconnection Processing Yields

In general, the two major yield limiting factors in the processing of multilevel metalization structures are: 1) insulator defects, which lead to interlevel metal shorts, and 2) high

resistance or electrically open vias, which in the extreme cases result in some portions of the arrays not being interconnected. The net effect of small geometry arrays on these yield factors is to minimize the insulator defect problem due to reduced conductor crossover areas which stem from the narrower metal linewidth and shorter metal runs. However, due to topographical features unique to small geometry arrays, there tends to be a counteracting detrimental effect on the inherent quality of deposited insulators employed in multilevel structures.

In small geometry arrays the problem of via resistance is aggravated because the via crossectional areas are typically 1/3 to 1/10 the area of vias in larger geometry arrays. Whereas larger geometry LSI arrays employ vias with a minimum area of 0.25 mil^2 to 0.375 mil^2, small geometry arrays employ vias with minimum areas of 0.03 mil^2 to 0.09 mil^2.

2.2.2.1 Insulator Processing - Defect Density Evaluation

There are two categories of defects experienced in insulating films employed in multilevel structures:

1. Defects which are generated during film formation (intrinsic defect densities);
2. Defects which are generated during via photoengraving.

In previous reports (Tenth and Eleventh Interim) we described how 2-step via etching sequences were employed to minimize defects generated during the photoengraving of vias. During this period we determined that improvements in intrinsic defect levels were also necessary in order to guarantee that array yields are relatively unaffected by insulator defects.

The quality of an insulating layer is generally characterized by a defect density number. It is well known for instance that for a capacitor structure which has an insulator with a given characteristic defect density, the yield of defect-free capacitors decreases as capacitor area increases, yield being predicted by the statistical formula:

$$Y = e^{-nA} \tag{1}$$

where Y is the probability of obtaining a defect free capacitor,

n is the insulator defect density,

A is the capacitor area.

Similarly, in a multilevel structure, the yield of defect-free structures is dependent upon the total crossover area between metalization lines in the structure. However, we also determined that for multilevel crossovers, a significant number of insulator defects also occur characteristically along crossover steps.

Consequently, to accurately predict the effect on yield of insulator defects in any multilevel structure (regardless of metalization geometries), the insulator must be characterized in terms of a defect area density and a linear density for crossover steps. Yield in this case, is more accurately predicted by

$$Y = e^{-nA-m\ell} \tag{2}$$

where m is the number of defects per unit length of crossover periphery,

ℓ is the total crossover periphery.

Determining n and m separately from statistical yield data taken on test structures is very difficult. Consequently, we have taken the approach of using insulator test structures which reproduce the topographies of actual multilevel array structures. By doing so the area to periphery ratios of the crossovers of both test and actual structures are the same. It can then be assumed that the ratio of m and n will be the same for both structures, and the yield of defect-free multilevel structures can be predicted from statistical data obtained on insulator test structures using the formula

$$Y = e^{-n'A} \tag{3}$$

where Y is the probability that an array has defect-free crossovers,

n' is the "effective" defect density determined from test structures,

A is the total crossover area.

Defect densities used to calculate the yields described later (page 28) were obtained using test structures which simulate actual small geometry multilevel array structures. A picture of a typical test structure for characterizing the insulators in an array having two levels of metalization is shown in Figure 2.

It has been found that insulators employed in 2-level small geometry arrays are more susceptible to crossover periphery defects than are those used in large geometry arrays due to the unique topographies of small geometry microcircuit structures. Since the oxide cuts and contacting metalization are, in many cases, the same width on the microcircuit level of small geometry arrays, topographical voids or crevices can be created due to pattern misregistrations. This is illustrated in Figure 3. Impurities and/or volatiles can be trapped in these voids prior to insulator deposition, to cause defects in the insulator deposited on them.

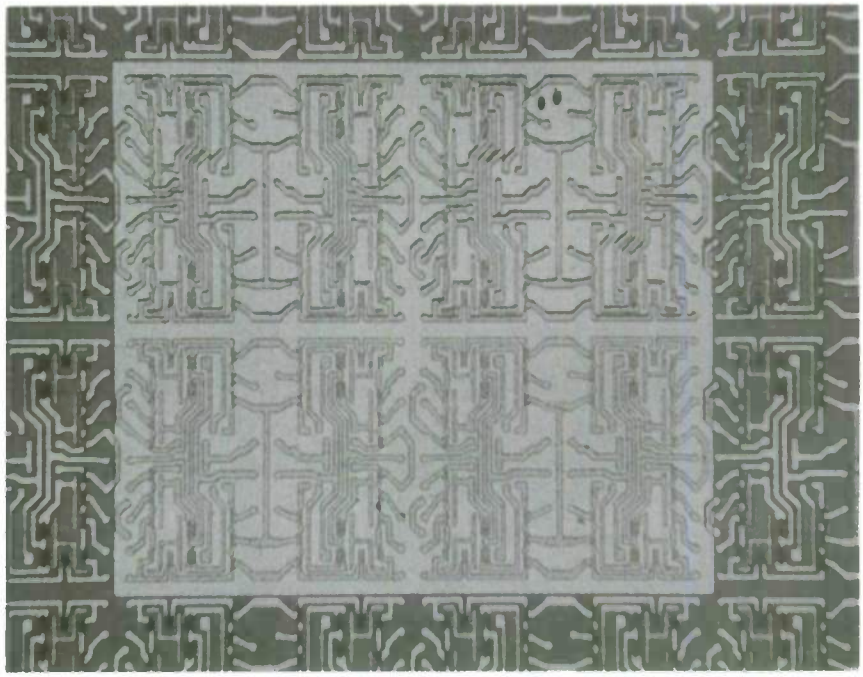


Figure 2. Top view of small geometry array insulator test structure.

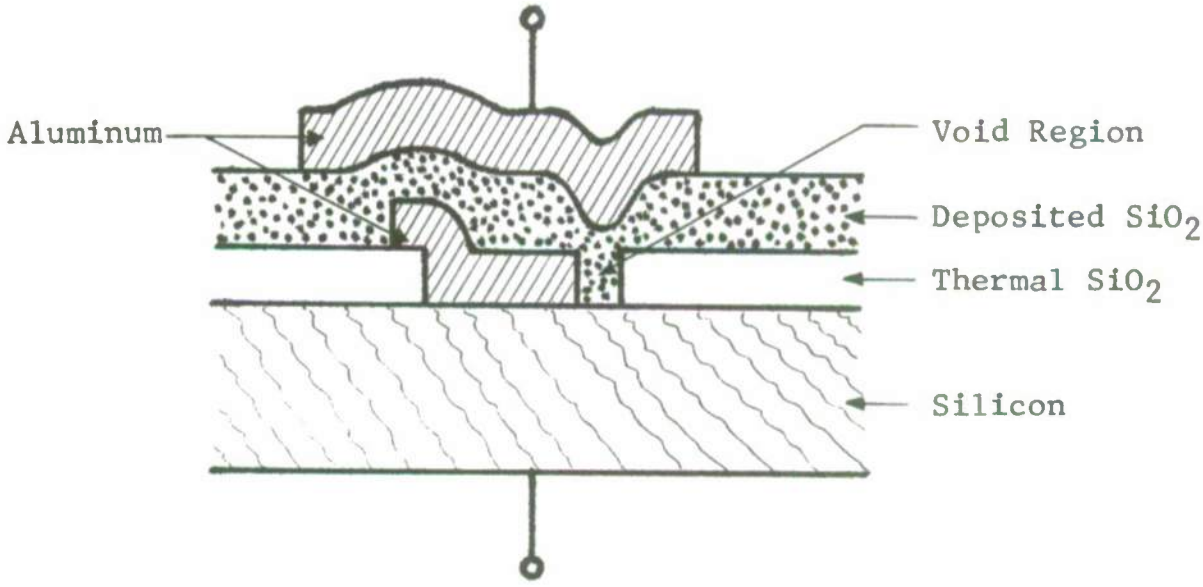


Figure 3. Sketch of cross section of a small geometry array structure in the vicinity of contact cut.

During this reporting period a number of experiments were performed toward the goal of obtaining insulating films with minimum intrinsic defect densities on small geometry microcircuit substrates. The experiments included an evaluation of r-f sputtered oxides versus silane deposited oxides and an evaluation of the effect of wafer cleaning procedures on the defect densities of deposited oxides. The test structure employed is shown in Figure 2. It was formed by:

1. Etching a small geometry microcircuit interconnection pattern in a thermally oxidized SiO_2 layer typical of those employed in microcircuit structures,
2. Evaporating aluminum and delineating in the aluminum the same interconnection pattern,
3. Cleaning the wafer in preparation for insulator deposition,
4. Depositing the insulator,
5. Evaporating aluminum and delineating a counterelectrode.

This structure presents a severe test to deposited insulators and leads to worst-case defect density characterizations for the insulators of 2- and 3-level metal systems for two reasons:

1. Not all crossovers between the first and second metalization levels in small geometry arrays are

typified by the test structure, in that all cross-over peripheries in the test structure can have voids (due to lack of overlap between the metal and the oxide cuts) whereas some crossovers in an actual array are of the conventional variety.

2. The crossover between the second and third levels of metal are all of the conventional variety.

A monitor structure which was simply a bare silicon wafer upon which the insulator to be tested and a counterelectrode were deposited was also included in each test to determine film properties which are not influenced by substrate topography. A number of conclusions were drawn from these tests:

1. The intrinsic defect densities of deposited oxides are strongly affected by the surface topography of the substrate. Topographies which are typical of small geometry array substrates that are complete to the point of first metal delineation increase the "effective" (see equation 3) oxide defect densities by as much as 25 times over densities on substrates with flat topographies.
2. Silane oxides (deposited at 370°C and at the rate of 4 kÅ/min) are inherently more defect free than

are r-f sputtered oxides (200 Å/min sputtering rate). On monitor structures, area/defect values or inverse defect densities as high as 150,000 $mils^2$/defect were obtained on silane deposited oxides, whereas the best results obtained on r-f sputtered oxides of equal thickness (7000 Å) were 6000 $mils^2$/defect. On test structures, the typical area/defect properties on r-f sputtered oxides was 500 to 3500 $mils^2$/defect. For silane oxides 10,000 to 20,000 $mils^2$/defect was typical.

3. Test structures (small geometry topography) were much more sensitive to cleaning procedures than were monitor structures, in terms of the resultant quality of insulating films deposited on them.* This implies that cleaning procedures for arrays must be much more thorough than for substrates with flat topography in order to obtain comparable properties for deposited insulators.

In order to estimate what levels of insulator perfection are required to fabricate, at high yields (95% initially and subsequently 99%), arrays with defect free insulators, calculations were made of the minimum area/defect properties required

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*Cleaning procedures which gave similar insulator qualities on monitor substrates, gave radically different results on test structures.

in the deposited insulator oxides of the largest, most complex array that we are attempting to fabricate, i.e. the 27-Bit Parity Array (754 components, 400 $mils^2$ of conductor crossover). A random defect model was employed and two assumptions were made:

1. Photoengraving decreases area/defect values by a factor of 2 to 3. This assumption is based on experience with our two-step photoresist process for etching vias (see Tenth Interim Report).
2. The insulating layer between the second and third metalizations is 2 to 3 times more defect free than the insulator between first and second metalizations. This assumes that the second insulator will be thicker ($\approx$1.5 times) than the first insulator and will be covering more conventional topography (no voids along metal steps) than that covered by the first insulator.

Calculations indicate that for the worst case 95% yields of defect-free 27-Bit Parity Arrays can be produced with the best process now available (i.e silane deposited oxides on properly cleaned wafers with 10,000 to 20,000 $mils^2$/defect values on test structures). An improvement in insulator quality of approximately 5 is required to attain the 99% level of defect-free arrays of this complexity. Similar

calculations indicate that 3-Bit Parity Arrays (two levels of metal with ≈20 $mils^2$ of crossover) can be easily made at 99% defect-free levels, while 9-Bit Parity Arrays (three levels of metal with 100 mil^2 of crossover) can be made at confidence levels of 98% to 99% with present insulator processing techniques.

2.2.2.2 Via Photoengraving and Via Resistance Evaluation

Circuit interconnections between the various levels of metalization in arrays are made through holes, commonly called "vias", photoengraved in the insulating layers which insulate consecutive metal layers. Since aluminum is the most widely used metalization in microcircuits, and the favorable reliability properties of aluminized microcircuits are documented, it becomes more attractive to employ aluminum for all levels of metalization in arrays. However, aluminum is a metal that easily oxidizes and therefore high resistance and open via paths can occur if the aluminum metalization layers are not carefully processed. Furthermore, these via problems also result if the insulating layers and vias are not carefully processed.

The problem of high resistance vias and open vias has been informally acknowledged by most manufacturers of large

geometry LSI arrays which employ aluminum metalizations. We believe that the problem generally can be minimized with careful processing followed by a high temperature anneal. In principle, annealing temperatures as high as 576°C (just below the silicon-aluminum eutectic) can be used.

The problem of high resistance and open vias in small geometry LSI arrays is more difficult to resolve because:

1. Via crossectional areas are typically 0.03 to 0.09 $mils^2$, some 5 to 10 times smaller than the minimum sizes of vias in large geometry LSI arrays. The effects of residual oxidized aluminum or residual deposited SiO_2 in vias are exaggerated by the smaller via size.
2. Annealing temperatures must be restricted to levels below 550°C.

Several different approaches have been pursued during this period to reduce via resistance in small geometry LSI arrays:

1. Backsputtering of the wafer prior to top metal evaporation, in order to "clean up" the aluminum in the bottom of the via.
2. Glow discharge cleaning of wafers for the same reason as in 1.

3. Use of thin films of metals (for example titanium) beneath the top level aluminum, to reduce residual Al_2O_3 (which is believed to be a major contributor to increased via resistance) which may exist in the via regions. The reduction of Al_2O_3 was to have been effected by a prescribed heat treatment.
4. Use of bimetal first-level metalizations consisting of aluminum covered by a thin film of a metal the oxide of which is readily reduced by aluminum.

Only the last approach has been successful in minimizing via resistance. Structures have been made on which via resistances were typically 0.32 to 0.35 Ω for via sizes on the order of 0.023 $mils^2$. This level of conductance could be achieved using annealing temperatures substantially less than 450°C and compared favorably with scaled conductance levels measured in vias of large area LSI structures using all-aluminum. Thus far, bimetal layers have been used for subinsulator metalization in arrays having only two levels of metalization. The approach has been successful to the extent that the best die sort yields of 3-Bit Parity Arrays obtained to date have been obtained by use of the bimetal first-level metalization (see paragraph 2.3.1). However, the use of bimetal metalization is being

treated as an interim solution to the problem of high resistance vias until all aspects of its effects on the overall reliability of arrays has been thoroughly evaluated. Bimetal metalization will soon be evaluated in a three-level metalization system. Meanwhile experiments will continue to be conducted towards successful implementation of an all aluminum system.

2.3 HIGH SPEED ARRAYS

2.3.1 3-Bit Parity Array

The 3-Bit Parity Array has 58 components and two levels of metalization. A photomicrograph of this array is shown in Figure 4. Figure 5 shows the schematic diagram of the array. Realization of 3-Bit Parity Arrays requires a capability to fabricate transistors at yields greater than 85% and a capability to fabricate a two-level interconnection structure which employs vias of 0.03 to 0.05 $mils^2$.

During a considerable portion of this reporting period, problems with relatively low transistor yield (defined in paragraph 2.2.1) and high via resistance precluded the successful fabrication of 3-Bit Parity Arrays. However, implementation of improved microcircuit processing techniques (paragraph 2.2.1) has improved transistor yields to greater than 90%, and implementation of the improved first-level metalization film (paragraph 2.2.2.2) has minimized the via resistance problem to the extent that the best die sort yields of 3-Bit Parity Arrays yet to be obtained, were obtained on the first wafer lot to be completed with the improved processing. Figure 6 shows a map of the wafer (No. 14A) which had the best yield. The yield was calculated to be $\approx$ 5.3% when all arrays on the wafer, including those at the periphery, were included in the calculation.

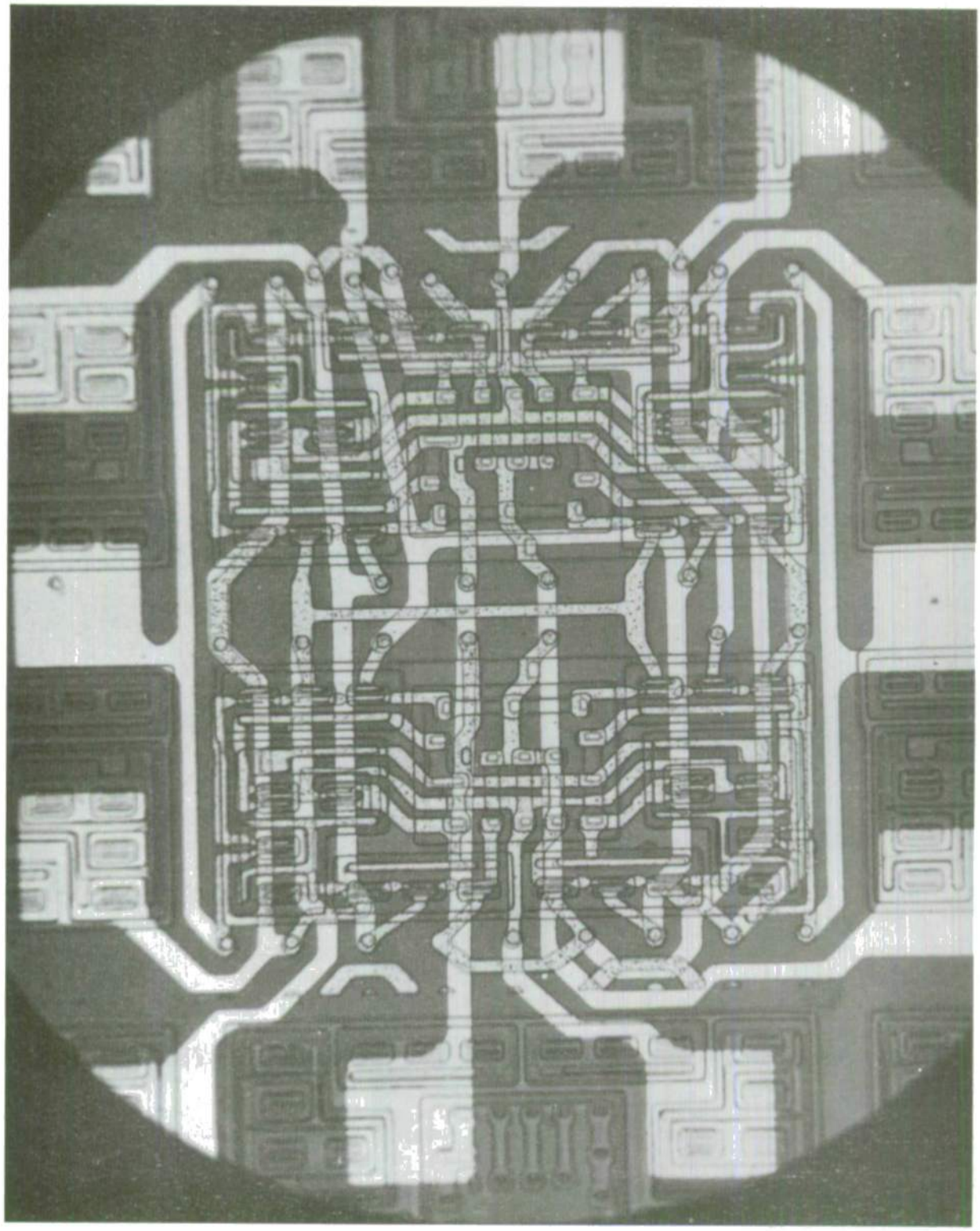


Figure 4. Photomicrograph of 3-Bit Parity Array.

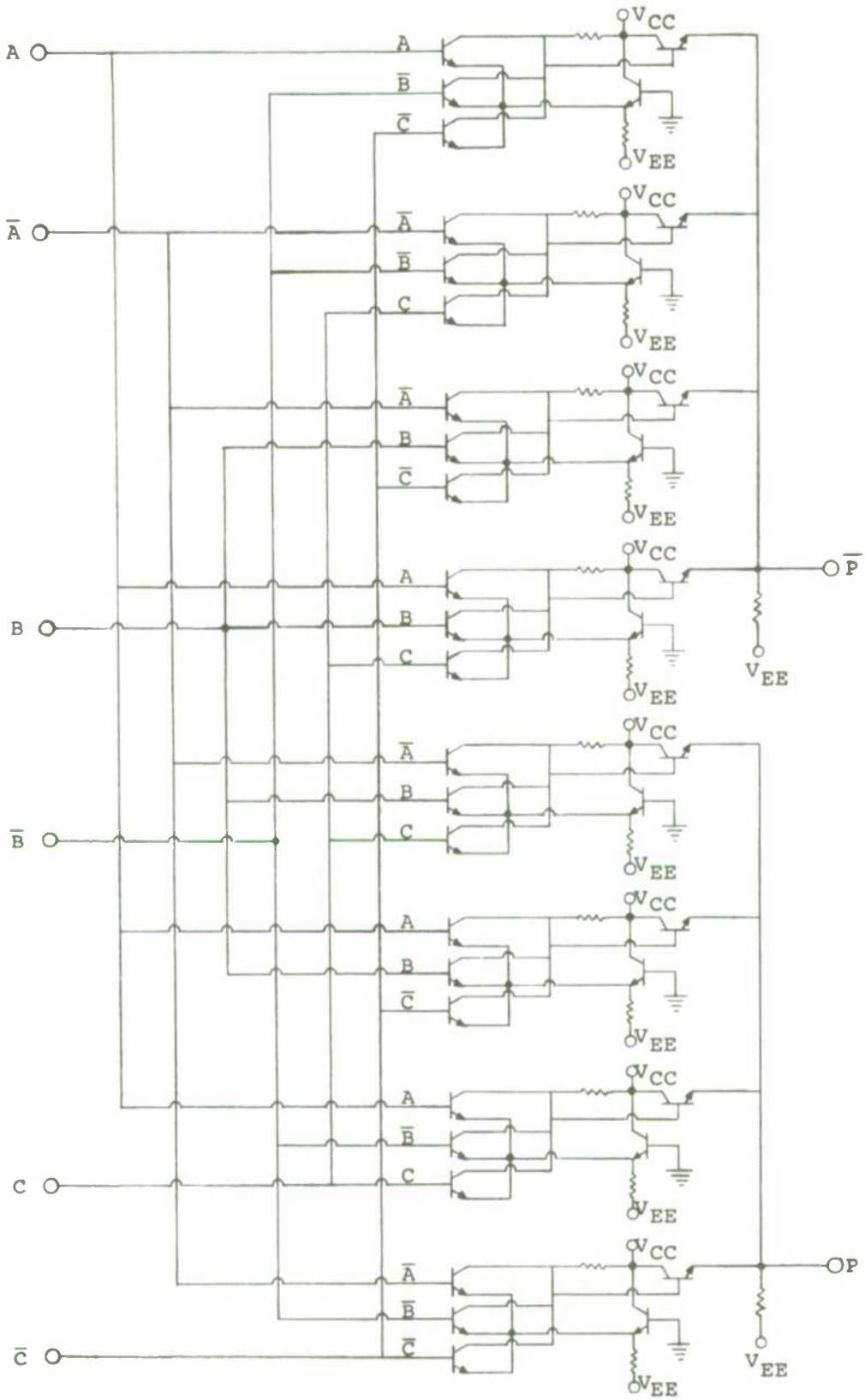
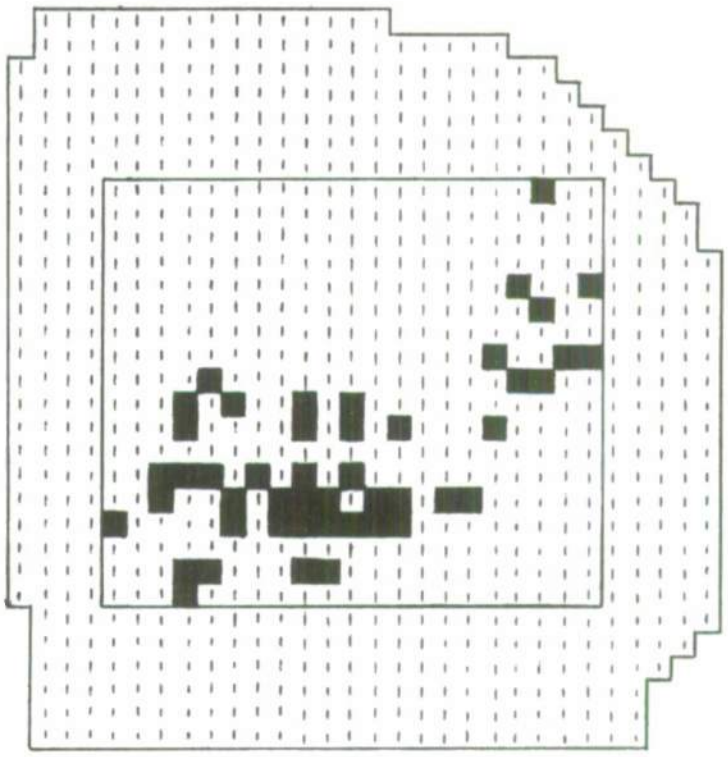


Figure 5. Schematic diagram of 3-Bit Parity Array.



Overall array yield ---------- 5.3%

Array yield in center of wafer ------- 12.4%

Overall calculated transistor yield -- 93.0%

Transistor yield in center of wafer -- 95.0%

Figure 6. Wafer map showing location of functional 3-Bit Parity Arrays on Wafer No. 14A.

The central portion of the wafer (enclosed by rectangular box in Figure 6) showed a yield of 12.4%. Based on a random-defect model, transistor yields for the entire wafer and for the central portion are calculated to be 93% and 95%, respectively.

We expect that the remaining 3-Bit Parity Array wafers being processed will have array yields that are equivalent to or better than that of Wafer No. 14A. This optimism is supported by transistor yield data already obtained on these wafers and the fact that these arrays will be processed with an improved cell metal mask redesigned to include the linewidth control described in paragraph 2.2.1. A substantial number of 3-Bit Parity Arrays from previous wafers failed due to circuit opens attributable to overly narrow device contact fingers.

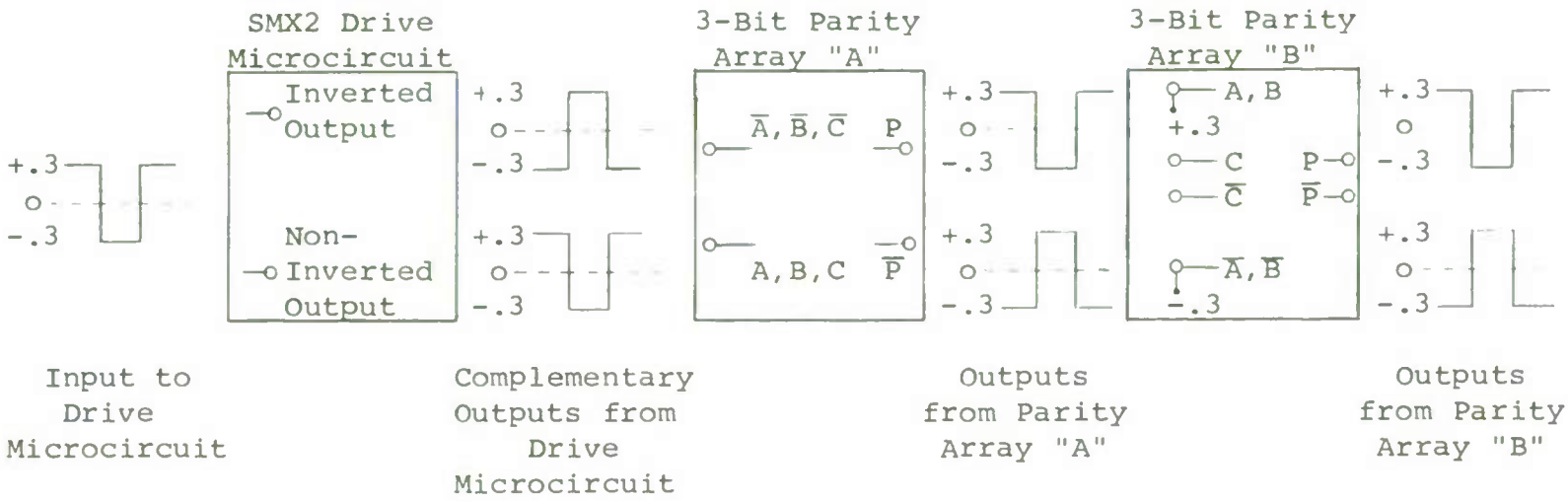
It should be pointed out that some of the 3-Bit Parity Arrays being processed employ ⟨100⟩ orientation silicon substrates, whereas the remainder employ conventional ⟨111⟩ substrates. Substrates of ⟨100⟩ orientation have been reported to improve the yields of devices (by reportedly allowing more uniform diffusion control and, consequently, finer control of basewidth and collector to emitter leakage), but thus far no pronounced yield difference has been apparent between devices fabricated on the two differently oriented substrates. This substrate

comparison will be continued on other wafers, so that data can be accumulated on a sufficient number of wafers to make the comparison more meaningful.

A group of fifteen 3-Bit Parity Arrays are being tested for reliability. The tests include thermal shock, back bias-temperature, and operational-temperature sequences. Initial results should be available during the next quarter.

The switching speed properties of typical 3-Bit Parity Arrays were measured using the test arrangement indicated in Figure 7, which permits the determination of array propagation delay time under two simulated system conditions. Array A simulates a case in which all 24 of the array input transistors are being switched while the array is driving a fanout of four. Array B simulates the case in which 8 of the array input transistors are being switched while the array has no circuit fanout, driving only the capacitance of the test probe (1.8 pF).

The average propagation delay for arrays tested in Position A was 1.48 to 1.53 ns. Propagation delay for arrays in Position B was 0.91 to 1.00 ns. The microcircuit employed to drive 3-Bit Array A is a high speed ECL gate (the SMX2 developed on an earlier program) having a raw delay of <0.4 ns and a propagation delay of 0.90 ns when driving a fanout of 12 as



	Average Measured* Propagation Delay	Operating Conditions	
		Fan-In	Fan-Out
SMX2 Drive Microcircuit	.90 nsec.	1	12
3-Bit Parity Array "A"	1.50 nsec.	12	4
3-Bit Parity Array "B"	.95 nsec.	4	0**

* These measurements include the effect of package and stray capacitances.

** Parity Array "B" drives test probe capacitance of 1.8 pF.

Figure 7. Illustration of test method used to measure propagation delay time through 3-Bit Parity Arrays, and chart of propagation delays.

when driving Array A. The average power dissipated by the 8-gate, 3-Bit Parity Arrays was 57 mW.

2.3.2 9-Bit and 27-Bit Parity Arrays

The 9-Bit Parity Array is a three-level metal array which comprises the componentry of four 3-Bit Parity Arrays. The array if formed essentially by interconnecting 2 x 2 matrixes of parity cells. Calculations (random-defect model) have shown that transistor yields on the order of 97% are required for fabricating functional arrays of the complexity of the 9-Bit Parity Array. The transistor yield data obtained on wafers of 3-Bit Parity Arrays, and the die sort mappings of functional arrays on completed wafers of 3-Bit Parity Arrays (Figure 6 for example), indicated a level of transistor yield such that achievement of functional 9-Bit Parity Arrays was considered possible. The processing of two lots of 9-Bit Parity Arrays was begun during the latter part of this period. Results should be available during the next quarter.

The 27-Bit Parity Array also employs three levels of metal interconnects and comprises the circuitry of thirteen 3-Bit Parity Arrays. Although no wafers specifically designated as 27-Bit Parity Arrays are in process at present, the test results from the first lot of 9-Bit Parity Arrays to be completed may suggest that the remaining lot be processed as

27-Bit Parity Arrays. This is possible because all parity array wafers are processed using identical masks up to the point where the scribe pattern is photoengraved in microcircuit thermal oxide. The second lot of 9-Bit Parity Array wafers will not be scribe cut until the first lot is evaluated.

Photomicrographs of previously completed 9- and 27-Bit Parity Arrays are shown in Figures 8 and 9, respectively. Functional block diagrams of both arrays are shown in Figure 10.

2.3.3 Functional Multiplier Array (FMA)

One of the study vehicles selected for Phase II of the program was a 1 x 1 FMA. This array is formed by appropriately interconnecting, through three levels of metalization, the components of three parity cells. Functionally, this array multiplies two binary digits and performs a summing operation. Figure 11 illustrates, in schematic form, the manner in which the gates of the parity cell are interconnected to perform the desired multiplier function. Figure 12 is a photomicrograph of the FMA.

The FMA serves a number of purposes:

a. It is an exercise in the universal cell approach to small geometry LSI. In implementing the interconnected gates of the parity cells it utilizes more components than if it had been designed through the microcircuit

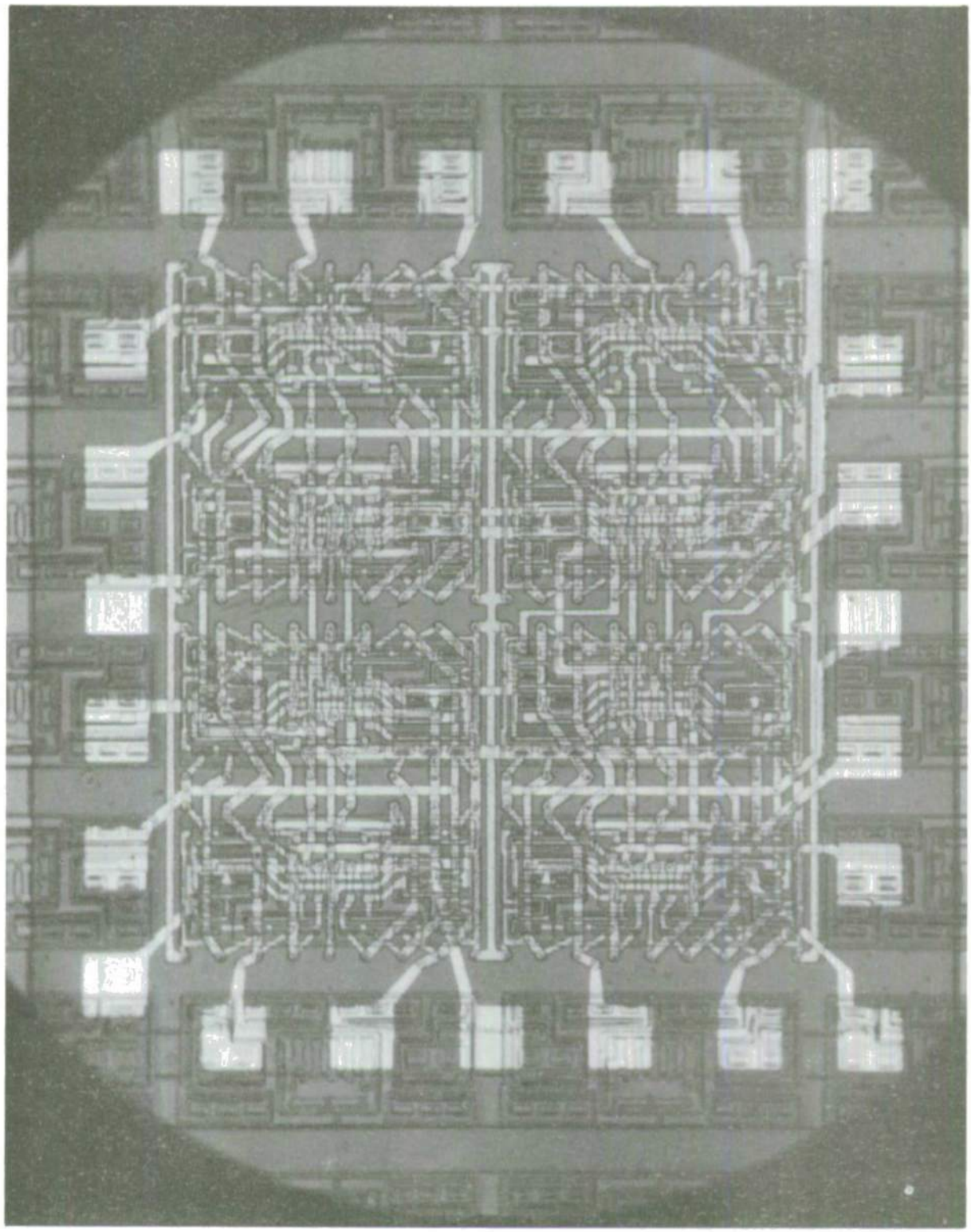


Figure 8. Photomicrograph of 9-Bit Parity Array.

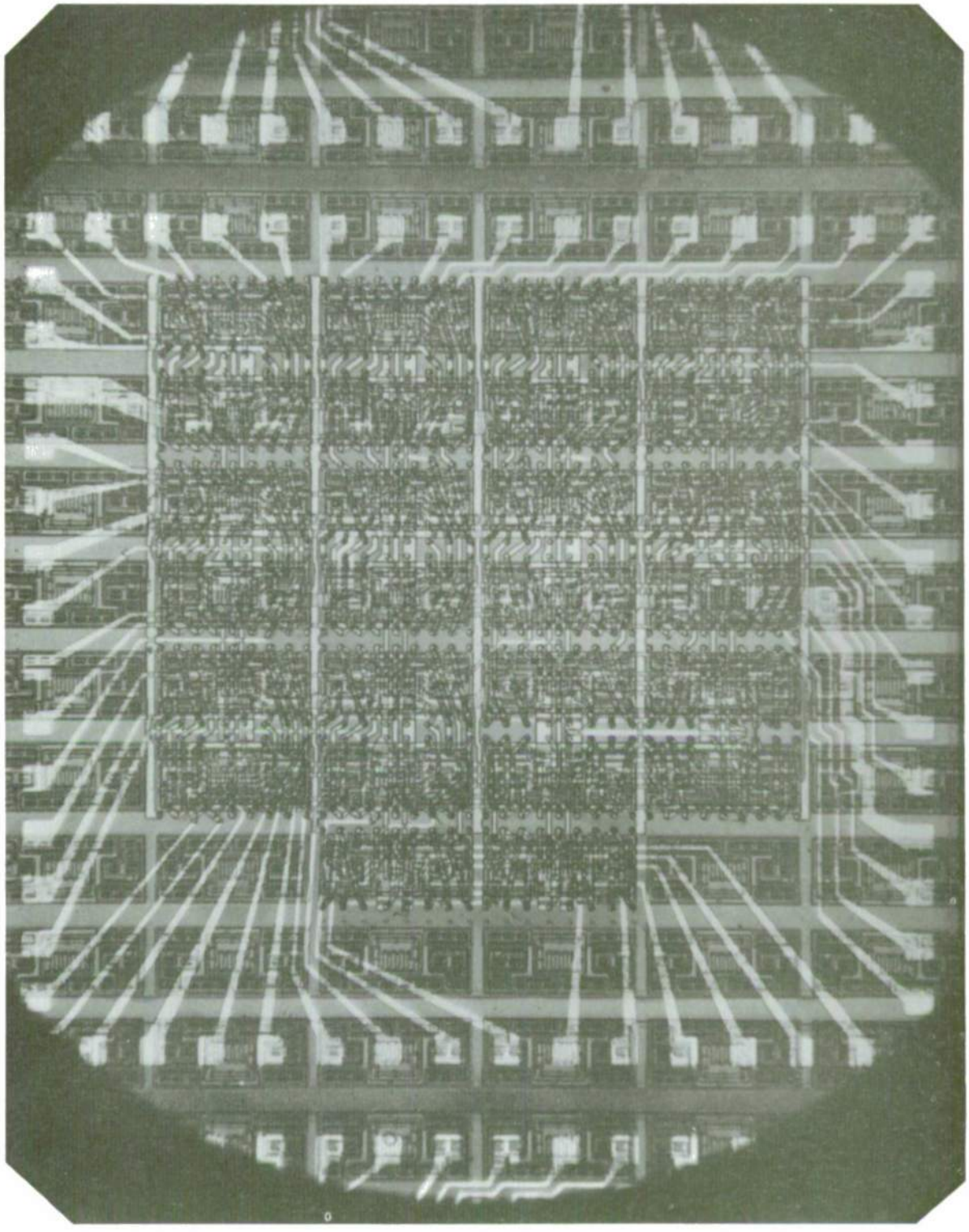
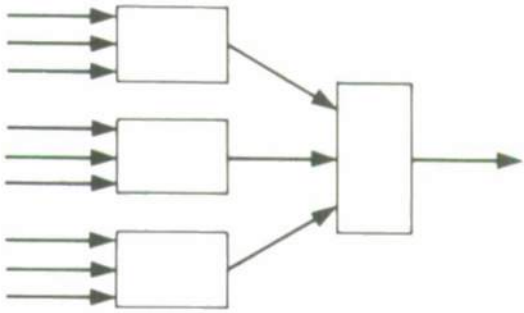
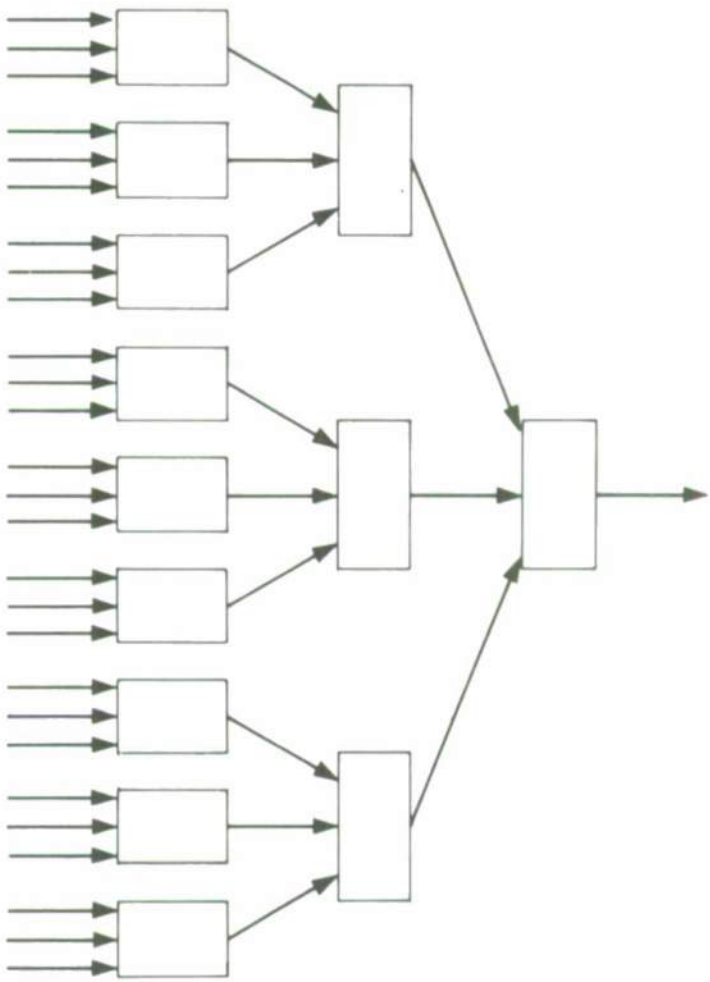


Figure 9. Photomicrograph of 27-Bit Parity Array.



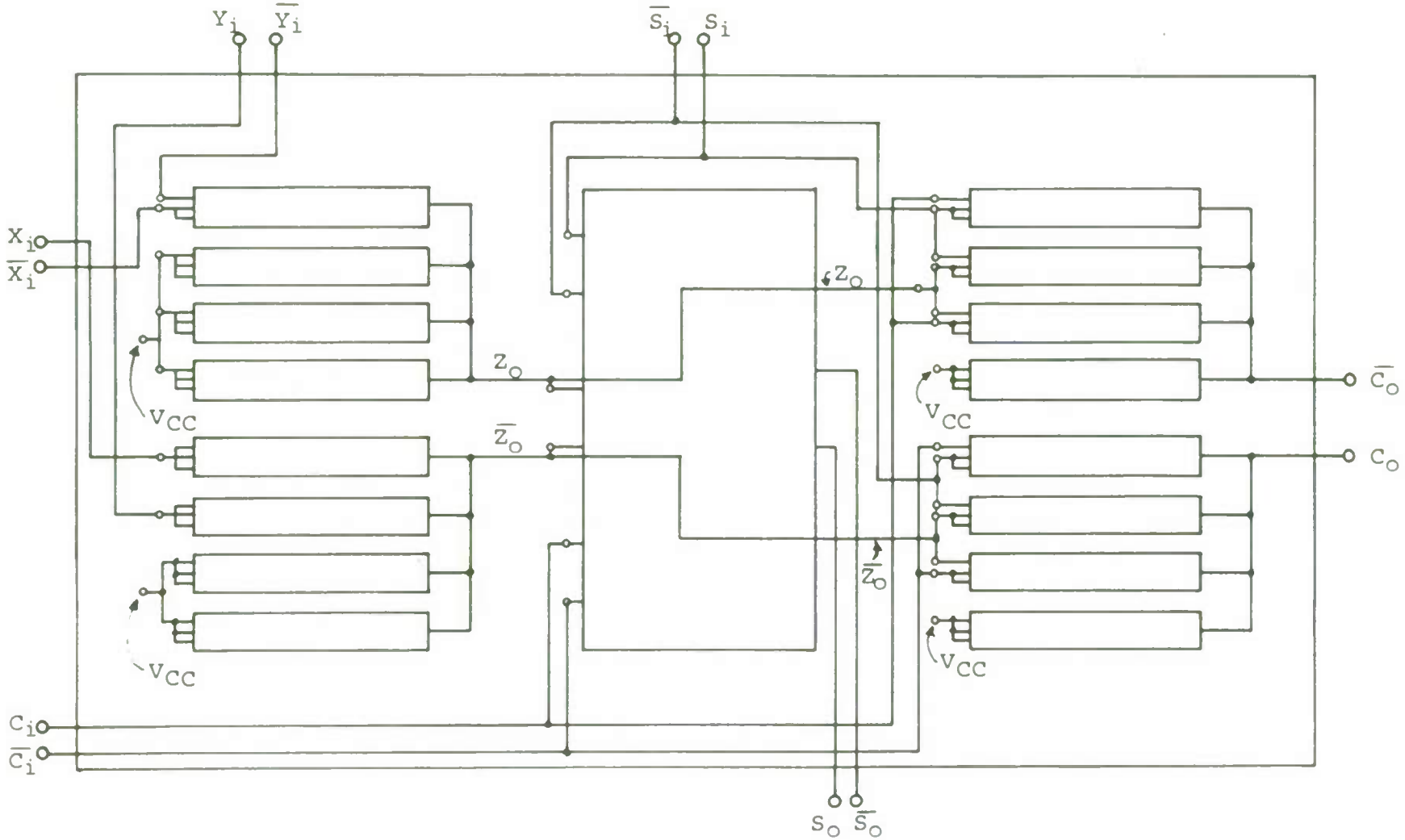
a. 9-Bit Parity Checker (160 transistors and 72 resistors -- a total of 232 components; power dissipation = 144 mW).



b. 27-Bit Parity Checker (520 transistors and 234 resistors -- a total of 754 components; power dissipation = 468 mW).

NOTE: Each rectangle represents a 3-bit parity circuit.

Figure 10. Functional block diagrams showing formation of 9-Bit and 27-Bit Parity Checkers by extensions of the 3-Bit Parity Circuit.



Note: This diagram illustrates the implementation of the circuitry of three 3-Bit Parity Cells to form the Multiplier. The small rectangles represent the basic 3-input gates of the parity cell; the large rectangle represents a 3-Bit Parity Circuit.

Figure 11. Schematic diagram of 1 x 1 Functional Multiplier.

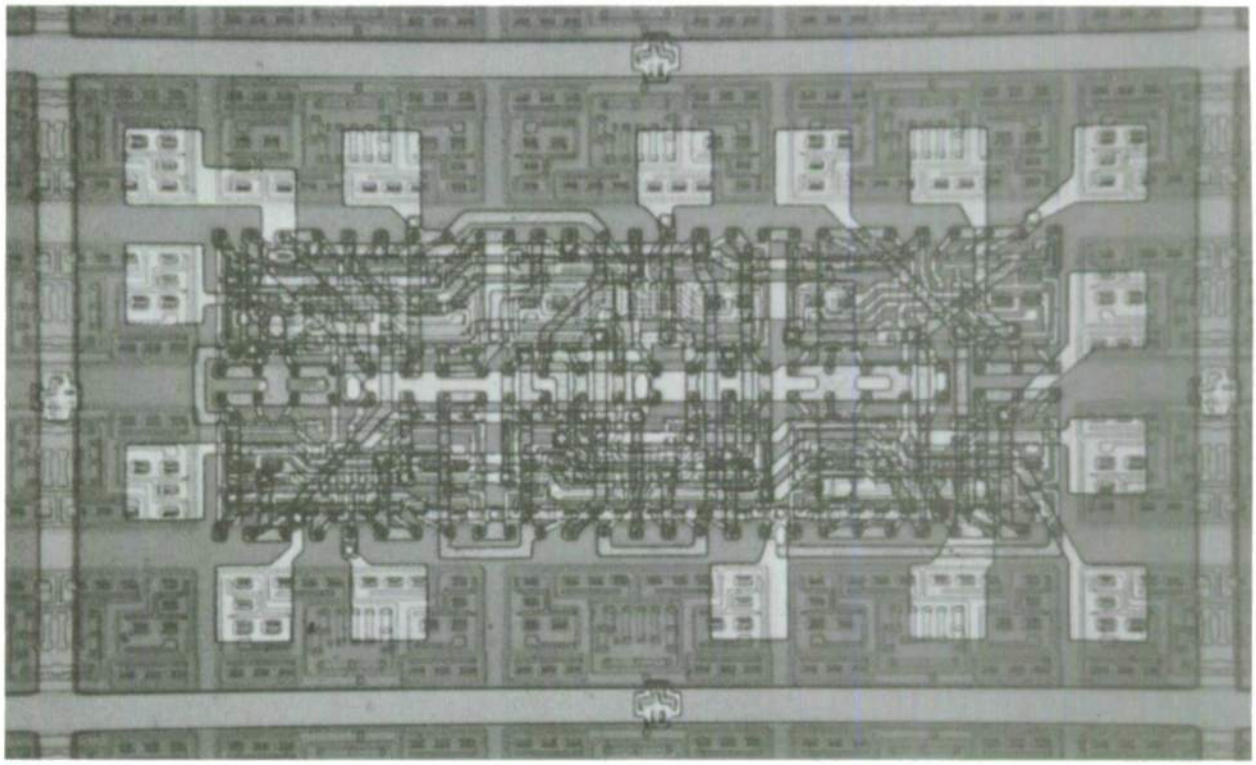


Figure 12. 1 x 1 Functional Multiplier Array.

level for its specific function. The excess components can significantly affect array yield. On the other hand, by utilizing the parity cells as universal cells, it is possible to create a new array function without redesigning microcircuit-level masks. Inasmuch as the FMA employs a cell design which has been largely debugged and the properties of which are reasonably well known, not only can a savings in time be realized but also an improvement in array yield.

b. It allows evaluation of array yield for a chip which has a complexity between that of the 3-Bit Parity Array and the 9-Bit Parity Array. Being 25% less complex than the 9-Bit Parity Array, such a chip should be easier to fabricate.

c. It affords an opportunity to rather simply implement and study changes in multilevel design rules. The need for these changes became evident during the fabrication and evaluation of parity arrays. The sizes of vias were increased from 0.2-mil diameter to 0.25 mil and 0.3-mil diameters. The spacings and overlap between vias and via pads were also increased to facilitate alignment and fabrication.

The first of the wafers being processed as FMA's has been completed and is being evaluated. Results on these and subsequent FMA's will be given in the next interim report.

2.3.4 RTL Associative Memory Arrays (AMA)

1-Bit and 16-Bit AMA's employing 0.1-mil device geometries and resistor-transistor logic (RTL) have been designed by Lincoln Laboratory (with guidance from Philco-Ford) during this period. The AMA's (see Table I for chip size and complexity) will serve as program vehicles for studying fabrication needs and performance properties of high-speed saturated arrays. Of particular interest will be the effect which gold diffusion, used for lifetime control, has on device yield. Four lots of RTL arrays are now being fabricated. Evaluations of the first completed arrays is expected to be accomplished during the latter part of the next interim. Figure 13 shows a schematic diagram of the circuitry of the 1-Bit, 1-Word Associative Memory Cell (including drive circuitry).

The AMA design effort has served the purposes of improving communication and of broadening the mutual understanding between groups that are principally identified as microcircuit fabricators and groups that are principally identified as systems and applications people. This area of mutual concern and

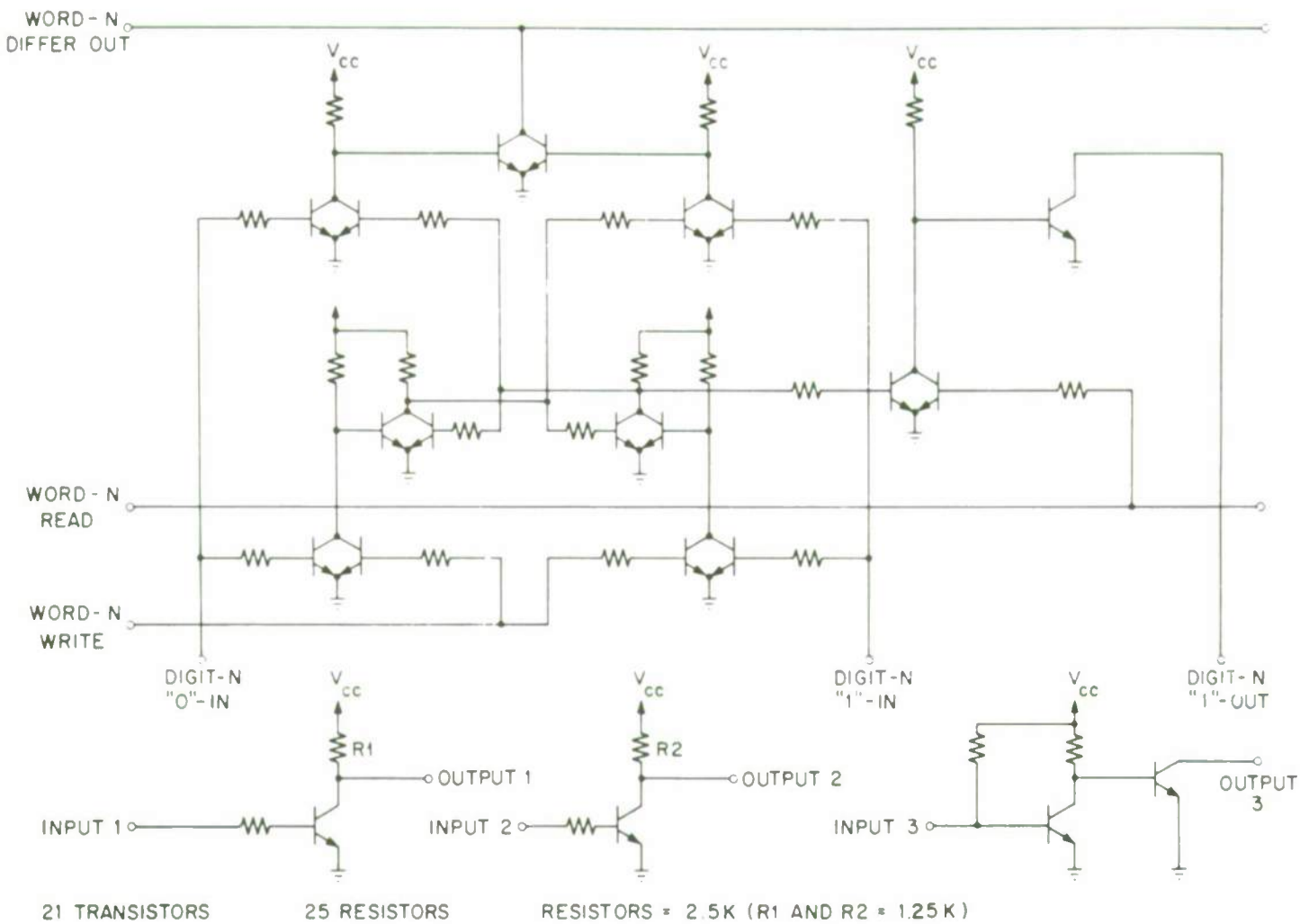


Figure 13. Schematic diagram of 1-Bit, 1-Word Associative Memory Cell (including drive circuitry).

cooperation will be further enhanced during the next period, when a cooperative effort will be made to combine the micro-circuit design and fabrication knowledge of the Philco-Ford R&D laboratory and the graphics and system design experience of Lincoln Laboratory in developing computer-aided layout design techniques for high speed arrays. The ultimate result of the effort should be gross reduction of design time and cost, as well as a substantial decrease in turn-around time.

2.3.5 Read Only Memory Array (ROM)

Program plans for Phase II call for the development of a high speed ROM which will either be implemented in a prototype special purpose computer being designed at Lincoln Laboratory or serve as a debugging vehicle for an improved redesigned version. The ROM chip that was decided upon is to have the capability of storing 64 words at 64 bits per word. One desired feature of the array is that it have the flexibility of being programmable in packaged form. This could be accomplished by providing a microelectronic fuse in each component of the bit and word lines. Such a ROM array would allow a programmer to change programs simply and quickly by procuring arrays which are stored "on the shelf" unprogrammed and programming them by electrically opening the appropriate fuses.

After considering possible forms for the ROM including an array of Schottky diodes, and performing some fabricating tests, it was decided from performance and fabrication considerations, that a 64 by 64 array of transistors, connected as emitter followers, would best meet the desired goals. The preliminary design employs a 0.1-mil geometry transistor with an emitter stripe of 0.1 x 0.3 mil and a 0.25 mil^2 base area. This design, which includes multilevel metalization, is such that programming of the ROM can be accomplished at the chip or package level by implementing the fuse concept or at the wafer level by means of a single photoengraving operation. Both approaches will be evaluated.

A final layout design, and subsequent photomask fabrication are expected to be completed during the next period.

2.4 ARRAY PACKAGING

For the most part the arrays developed thus far have been packaged using flatpacks manufactured by Philco-Ford. The 3-Bit Parity Array, 9-Bit Parity Array and Functional Multiplier Array are packaged in Philco-Ford standard line 14-, 24- and 16-lead packages, respectively. The 27-Bit Parity Array required the development of a 60-lead flatpack. This package, shown in Figure 14, was fabricated in limited quantities to package and evaluate the 27-Bit Parity Array. A commercial package developed for this application would not necessarily have the same configuration. Final testing of arrays in the 60-lead package is accomplished by soldering the package leads into an appropriately designed printed circuit board, shown in Figure 15, which can be connected to the testing apparatus by means of commercially available sockets.

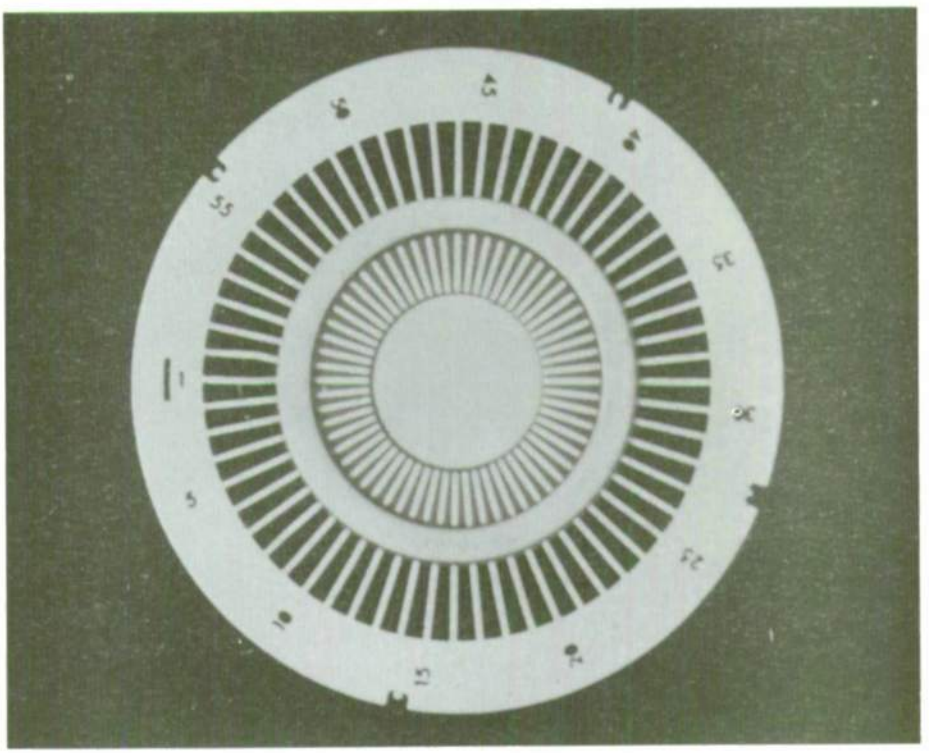


Figure 14. Sixty-lead experimental package.

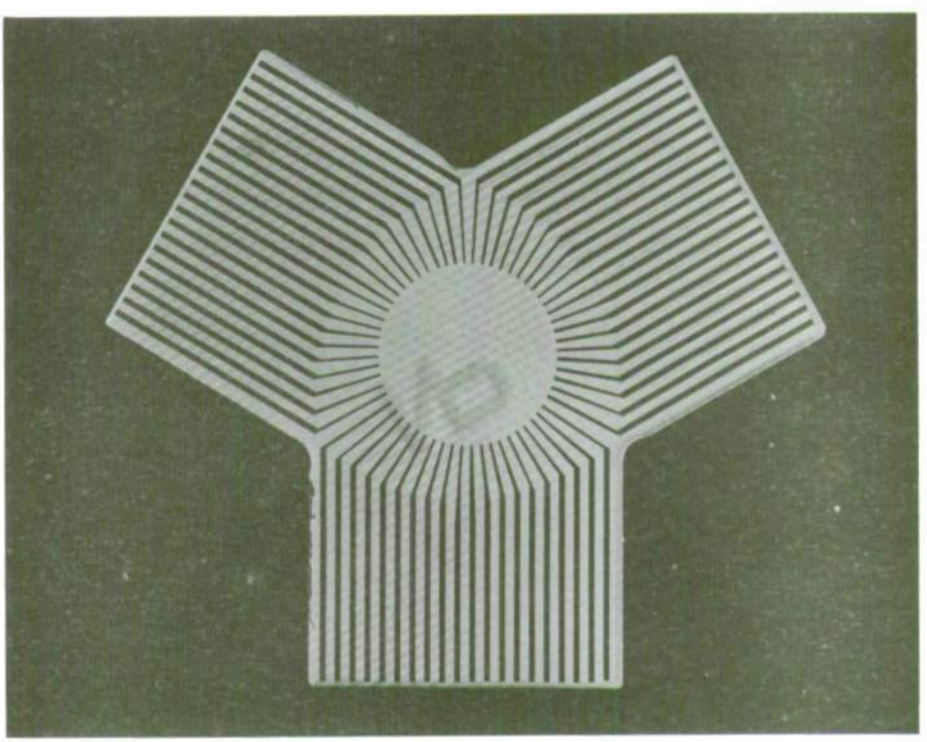


Figure 15. Experimental printed circuit test board for 60-lead package shown in Figure 14.

2.5 ARRAY EVALUATION AND FAILURE ANALYSIS

Exhaustive testing of complex arrays is a very difficult, expensive and time consuming task, in terms of both the equipment required and the time required to design test sequences. On this program, die sort testing has been done with both standard and special probes developed by Philco-Ford in conjunction with a Functional Tester which was designed and provided by Lincoln Laboratory. The Array Functional Tester shown in Figure 16 can test the Parity Arrays and the Functional Multiplier. The test sequences, for example, test all gates for all possible combinations of inputs in the 3-Bit Parity Array, and exercise at least once each gate in the 9- and 27-Bit Parity Arrays.

Due to the large number of terminal pads on arrays of the complexity of the 9- and 27-Bit Parity Arrays, special probe assemblies were required for die sort testing. Figure 17 shows the probe board assembly developed by Philco-Ford for testing the 27-Bit Parity Array. This probe is capable of contacting fifty-nine 2.5 x 2.5 mil pads with 2.5 mil spacing. The probes are fixed-positioned and individually spring loaded.

Testing of the Parity Arrays after packaging has been conducted using the Array Functional Tester for low frequency measurements and specially designed test sets for high speed measurements.

Figure 16. Array functional tester.

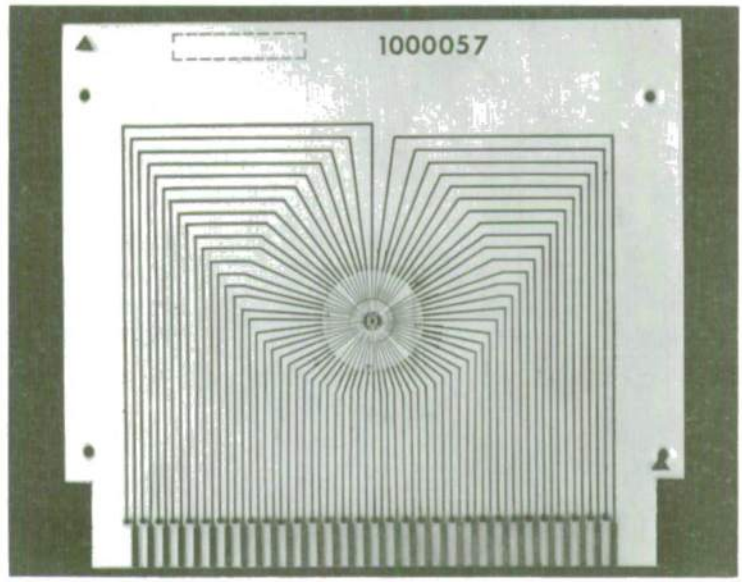
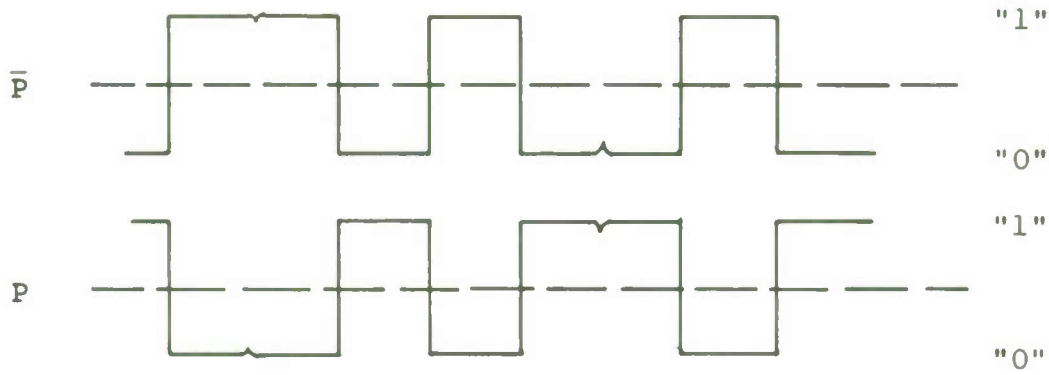


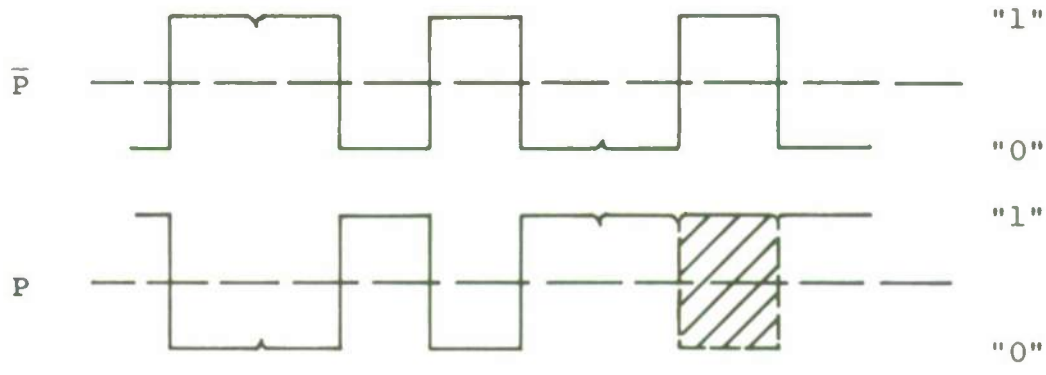
Figure 17. Fifty-nine pin micro test probe.

Array failure analysis was initially accomplished solely by a 2-point pad probing technique. However, this technique was later supplemented by a technique which obtains analytic information from the output waveforms displayed by the Array Functional Tester on a sampling scope. By using the combination of the two techniques it has been possible, in many cases on 3-Bit Parity Arrays, to pinpoint, to particular components or sections of the arrays, failures due to opens or shorts. Open vias can also be localized using these techniques. As an example, Figure 18a shows the output waveform of a properly functioning 3-Bit Parity Array. The waveform of Figure 18b signifies that any one of four specific transistors has an open lead or a defective emitter-base junction. Although these techniques have been valuable in analyzing 3-Bit Parity Arrays, similar analyses become more difficult with increased array complexities.

Failure analyses can also be performed by probe testing the internal interconnections of the arrays to some degree. However, because of the small conductor linewidths (typically from 0.2 mil to 0.5 mil) employed in small geometry arrays, and due to the fact that the metalization lines at various levels cannot be probed without destroying (by etching away) the overlying insulator and metal, the technique is somewhat



a. Proper output waveforms for given sequence of test inputs which completely exercise the 3-Bit Parity Array.



b. Waveforms which are obtained, for example, when a specific single input transistor has an electrical open or a degraded emitter-base diode.

Note: "1" = +0.3 V
"0" = -0.3 V

Figure 18. Output waveforms of properly functioning 3-Bit Parity Array (a), and of malfunctioning 3-Bit Parity Array (b).

restricted. Nevertheless, the technique has occasionally been valuable in analyzing certain gross circuit and component properties by probing the first level metalization after removing the upper levels of the multilevel structure.

2.6 SUBSYSTEMS ASSEMBLY -- FACE DOWN BONDING

In line with the program goal of developing a compatible assembly technique for interconnecting high speed microcircuit array chips into a subsystem, through means other than conventional packaging and wiring, a face down bonded version of the 9-Bit Parity Array is being developed. The technique involves face down bonding of four 3-Bit Parity Array chips onto a silicon substrate, referred to as a wafer-chip, which has a metalization pattern that appropriately interconnects the 3-Bit Parity Arrays to perform the 9-Bit Parity Circuit function.

The face down bonding concept of subassembly is versatile in a number of ways:

1. The wafer-chip can be completely passive, that is it can be an oxidized silicon substrate having a metalization pattern appropriately processed with Au-plated contact bumps to interconnect various completed microcircuit chips which are face down bonded onto it.
2. In addition to interconnecting microcircuit chips by means of a metalization pattern, the wafer-chip can be utilized as a power bus.
3. The wafer-chip interconnection pattern can be a multi-level structure, with the wafer chip substrate being used as a power bus lending still another option.

Theoretically, an array interconnection structure of four or more metalization levels can be constructed using the subassembly concept of face down bonding to a wafer-chip while only two levels of metalization are required on the microcircuit chips. This technique offers minimized total subsystem yield problems by obviating the yield problems inherent to implementing three or more levels of interconnects on a small-geometry array chip by transferring most of the multilevel interconnections to the wafer-chip, wherein the multilevel processing is not limited by device sensitivities.

In our first attempt to implement face down bonding as a subsystem assembly technique for high speed systems, the wafer-chip (for the 9-Bit Parity Array) has but one level of metalization, with the wafer-chip substrate being used as a ground reference supply bus. Bonding can be accomplished by either the solder technique described by Kraynak and Fletcher*, or by thermocompression and/or ultrasonic bonding.

Prior to the end of this reporting period the mask set for fabricating the wafer-chip for the 9-Bit Parity Circuit

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*Kraynak, P. and P. Fletcher, "Wafer-Chip Assembly for LSI," 1967 Internation Electron Devices Meeting, Washington, D.C., October 16-18, 1967.

was completed, photomasks were made and the first wafers of wafer-chips were fabricated. Figure 19 shows this wafer-chip with Au-plated bumps and four 3-Bit Parity Array chips which are to be face down bonded to the wafer-chip. The first attempts at subsystem assembly were made using recently purchased face down chip bonding equipment which employs ultrasonic bonding, thermocompression bonding and a combination of both bonding techniques. Preliminary assembly experiments revealed the need for modifications in this bonding equipment. In particular, an improved chip-to-chip alignment aid and an adjustment for leveling the circuit chips relative to the wafer-chip were found necessary. The inability to reproducibly level the wafer-chip and circuit chip relative to one another resulted in nonuniform bond strength in different parts of the subassembly and prevented completion of 9-Bit Parity Circuit subassemblies.

The equipment has been returned to the manufacturer for the necessary modifications. Additional development of the subsystem assembly technique will be conducted when the modified bonding equipment is returned by the manufacturer. The alignment accuracy that is expected to be achieved with the equipment is at least ±0.25 mil.

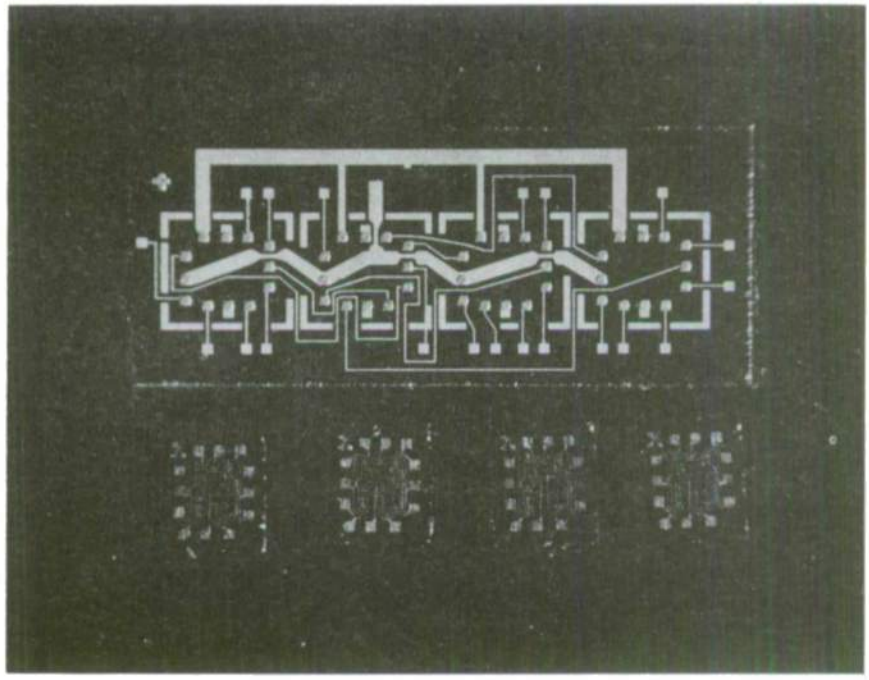


Figure 19. Components (3-bit parity circuit chips and interconnection wafer-chip) for face down bonding assembly of a 9-Bit Parity Subsystem.

2.7 NEW MICROCIRCUITS

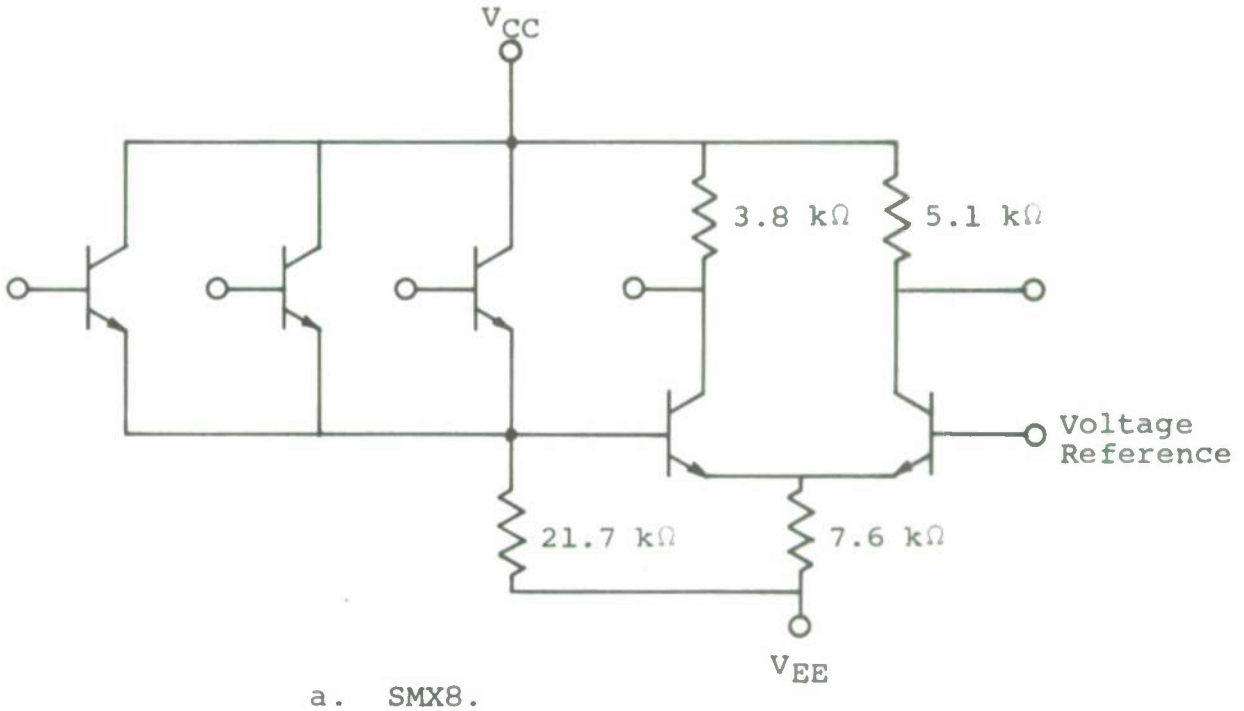
The Eleventh Interim Report stated that two new ECL gates were designed, both of which were to have relatively-low propagation delay-power products. The first microcircuit, designated SMX8, employs 0.1-mil geometry devices and tantalum resistors, and emphasizes low power dissipation. It is intended to operate at 1 mW dissipation at anticipated propagation delays of 1 to 2 ns. The microcircuit transistor has a single stripe emitter of 0.1 x 0.3 mil and a base area of 0.25 mil^2. A schematic diagram for the SMX8 is shown in Figure 20a.

The second microcircuit, designated SMX9, employs micron geometries and diffused resistors, and is designed to operate at very high speed (propagation delay expected to be less than 0.2 ns) with power dissipation of 35 to 40 mW. Signal swings are 800 mV. A schematic diagram for the SMX9 is shown in Figure 20b.

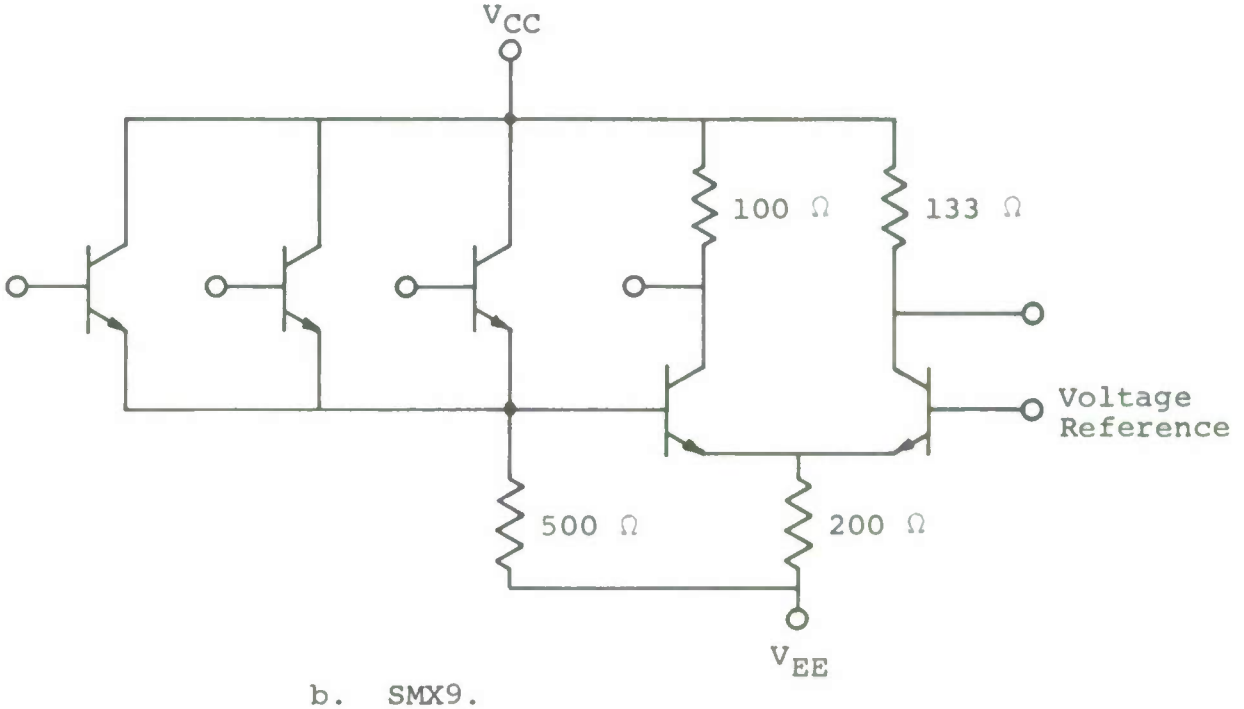
Both the SMX8 and SMX9 are 3-input gates, with emitter follower inputs and complementary outputs. Both employ two levels of metalization to minimize pad capacitances and to effect low capacitance crossovers.

2.7.1 SMX8 ECL Gate

Figure 21 is a photomicrograph of an SMX8. The first SMX8 microcircuits fabricated have been fully evaluated.



a. SMX8.



b. SMX9.

Figure 20. Schematic diagrams for two new ECL gates.

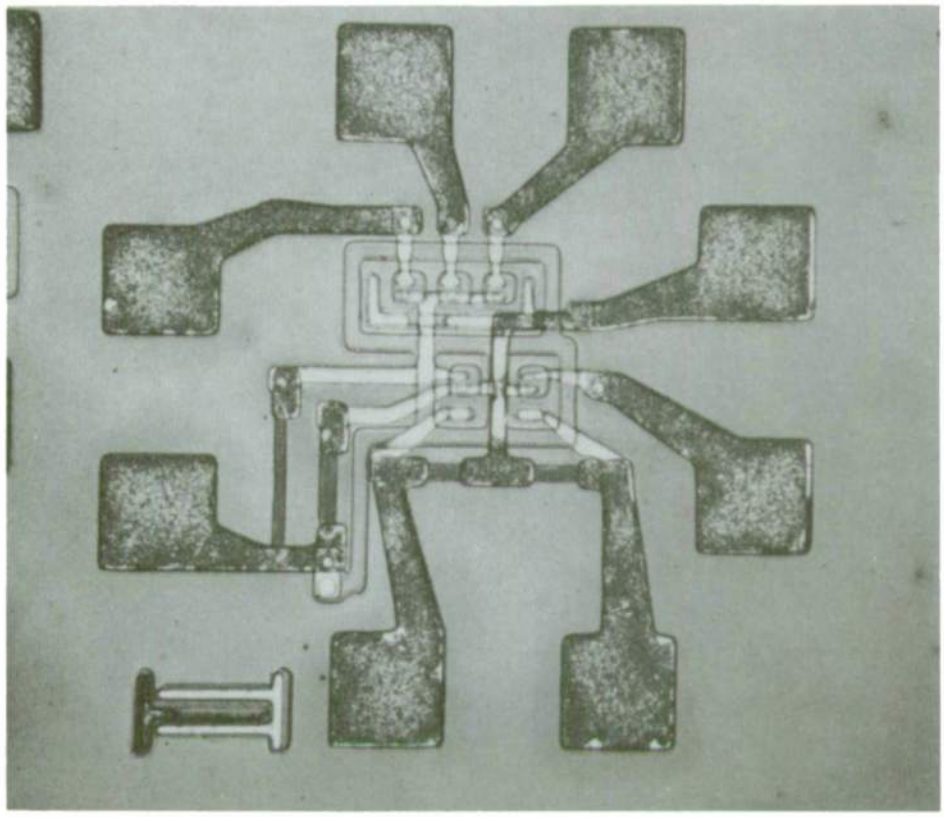


Figure 21. Photomicrograph of 1 mW, high speed ECL gate (SMX8).

Test results indicate that the performance goals of 1 mW power dissipation and 1 to 2 ns propagation delay were not fully achieved on these first samples. The lowest propagation delay that was obtained for 1 mW operation was 6.3 ns.

The speed-power curve shown in Figure 22 was obtained using microcircuits from a single wafer by stabilizing the microcircuit tantalum resistors in different parts of the wafer to different values. The fact that τ_{pd} falls as a function of increasing power indicates that the SMX8 microcircuits are load- or capacitance-limited in the region of 1-mW power dissipation. If the microcircuit were device limited, τ_{pd} would increase with increased power dissipation. The speed limitation due to loading is not surprising since the load resistors are in the range of 4 to 5 kΩ. However, load capacitances were expected to be lower than indicated by the test data, especially since special measures were taken to minimize the capacitances. The special measures include the use of a very small transistor (0.03 $mils^2$ emitter, 0.25 $mils^2$ base area), Ta resistors having high sheet resistivity, and bilevel metalization wherein the resistors and pads are fabricated on the second level. Accurate determination of the raw chip delay was difficult due to the high sensitivity of the microcircuit to parasitic capacitances, including the capacitance of the

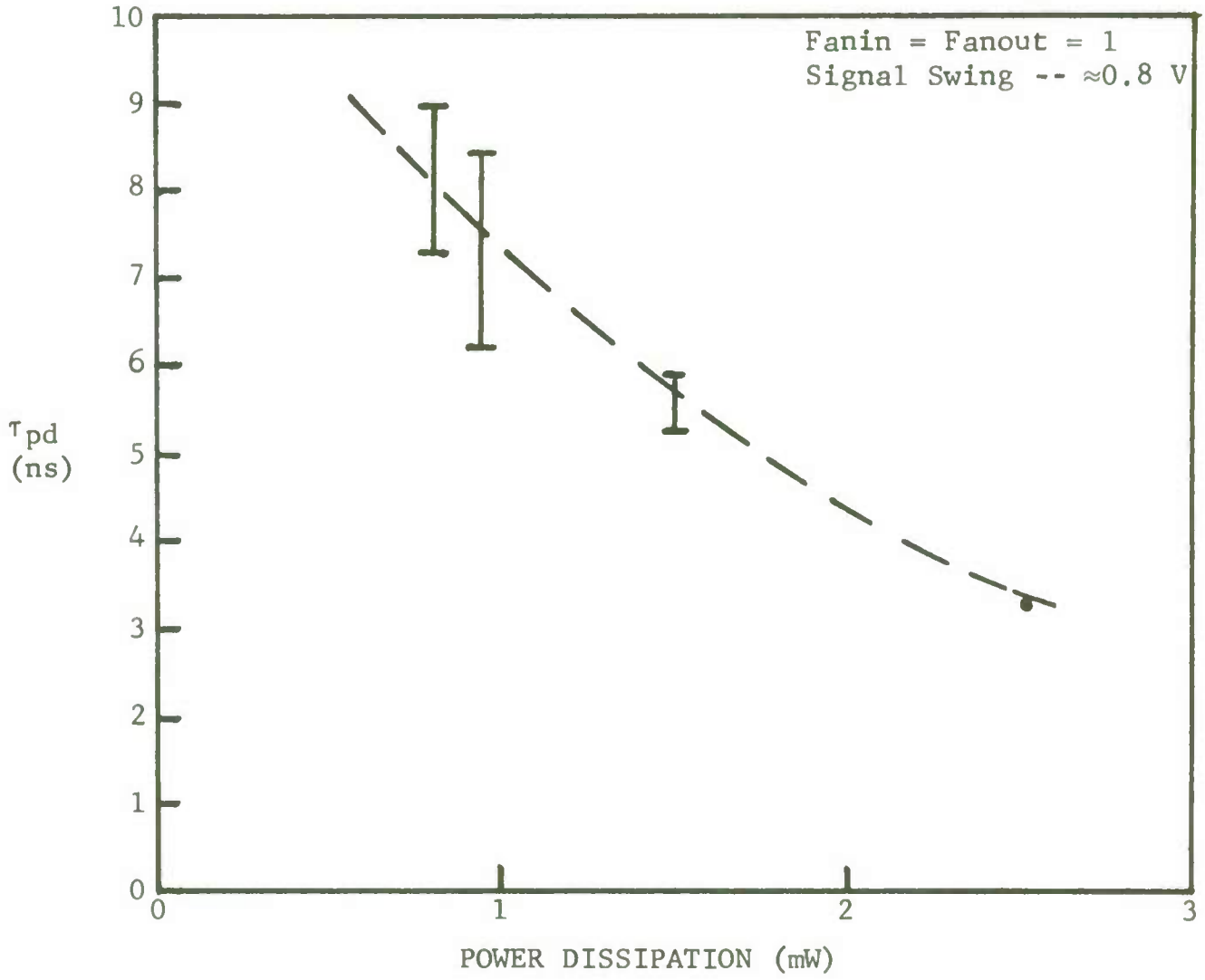


Figure 22. Propagation delay time versus power dissipation for the emitter follower input, complementary output, ultrasmall geometry ECL gate (SMX8).

measuring probes. However, ring oscillator measurements of propagation delays agreed with the delays obtained on individually packaged microcircuits.

Future work on the SMX8 will be mainly confined to analyzing the contributions which the microcircuit is making to the net parasitic capacitance, and attempting to minimize those contributions.

2.7.2 SMX9 ECL Gate

Completion of SMX9 gate microcircuits has been delayed due to priority requirements of other phases of the program. It is hoped that the first samples can be completed during the next interim.

SECTION III - FUTURE PLANS

Phase II plans for the next interim include:

a. A continuing effort to improve fabrication techniques for increasing device and circuit yields at the microcircuit level.

b. A continuing effort to develop more effective multilevel interconnection structures. This effort will include continued evaluation of the reliability effects of implementing the bimetal metalization films discussed in this report (paragraph 2.2.2.2). Efforts will also be renewed to implement an effective all-aluminum multilevel metalization system.

c. An attempt to establish an optimum chip size for small geometry LSI based on yield results for the various arrays presently being fabricated.

d. Continued cooperation with Lincoln Laboratory personnel to develop computer aided design techniques (CAD) for the layout of high speed microcircuit arrays. It is anticipated that new layout designs of microcircuits and arrays be implemented utilizing CAD, possibly even in the next interim.

e. Completion of the final design and start of fabrication of the Read Only Memory.

f. Continued experiments with face-down-bonding subassembly techniques.

g. Speed analysis of the SMX8 microcircuit, and fabrication and test of the SMX9.

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13. ABSTRACT

A research and development program directed toward the development of high speed computer subsystem fabrication technologies is described and the results of device yield and speed-power dissipation improvements are reported. Small geometry, shallow diffused, npn silicon transistors are utilized in simple ECL circuit forms to achieve high performance at low power dissipation in complex array structures. Various component interconnection technologies are being developed and characterized for high density, high speed subsystems. Multilevel single chip and multi-chip assemblies are being investigated. Reliability studies of functioning arrays have been initiated.

14. KEY WORDS

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ultrasmall geometry