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ASD-TR-61-11
VOLUME III

SOLAR CELL ARRAY OPTIMIZATION

TECHNICAL DOCUMENTARY REPORT ASD-TR-61-11, VOL. III

December 1962

FLIGHT ACCESSORIES LABORATORY
AERONAUTICAL SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO

PROJECT NO. 8173, TASK NO. 817301-6

PREPARED UNDER CONTRACT NO. AF33(616)7415
BY ASTRO-ELECTRONICS DIVISION
DEFENSE ELECTRONIC PRODUCTS
RADIO CORPORATION OF AMERICA
PRINCETON, NEW JERSEY

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FOREWORD

This report was prepared by the Astro-Electronics Division of RCA under USAF Contract No. AF 33(616)-7415. The contract was initiated under Project 8173, "Photostatic Energy Conversion Techniques," Task 817301-6, "Photoelectric Power." The work was administered under the direction of the Directorate of Aeromechanics, Deputy for Technology, Aeronautical Systems Division, Wright-Patterson Air Force Base, Ohio. Mr. David Massie was the project engineer.

This report covers work done from October 1961 through June 1962.

In the performance of this work, the Astro-Electronics Division was assisted by personnel of RCA Laboratories. This report is the third and final progress report on the solar cell array program. Volume II was published in December 1961 and the initial report which was not designated Volume I but was called Summary Technical Report, was published in August 1961.

ABSTRACT

This technical report presents the results of the research and fabrication phase of Contract No. AF33 (616)7415. The over-all objective of the work is the achievement of the maximum electrical power conversion, in space, of solar energy per unit of system weight. The objectives of this phase were: (1) to continue research on photovoltaic materials, (2) to develop the crystal-layer conversion process to the point of fabricating cells for delivery, and (3) to fabricate for delivery one square foot of large-area, thin-film, CdS photovoltaic cells.

Research of photovoltaic materials has shown the feasibility of fabricating cells with the p-n junction far removed from the surface by means of heterogeneous cell formation, of fabricating cells by the silk-screen technique of applying the active material, and also has shown that CdS polycrystalline cells are more resistant (by a factor of 10^4) to 1.6 Mev protons and (by a factor of 10) to 0.8 Mev electrons than are n-on-p silicon cells.

Five cells of small area were fabricated for delivery and demonstrated the feasibility of making cells from converted CdS layers. The maximum efficiency of these cells was about 0.7 percent; additional research work is needed to explore the possibilities of increased efficiency.

Three specimen arrays composed of four-inch-square cells totalling two square feet in area were delivered. Reproducibility in performance of four-inch-square cells was improved to the extent that the last five cells fabricated exhibited conversion efficiencies of at least one percent with the efficiency of the best cell at 1.2 percent. This efficiency is to be compared with the maximum efficiency of 5.7 percent obtained for small-area cells of 0.2 cm^2. One array, which contained five cells, demonstrated the potential of integrated circuitry for large-area cells to overcome the high sheet resistance which is inherent in all large-area cells. This array also demonstrated the use of 0.002-inch flexible plastic as cell substrate providing power density of 5 to 7 watts per pound. With this type of substrate material, the potential power-to-weight ratio for four-inch-square cells approaches 20 watts per pound. It is anticipated that with further development, the conversion efficiency can be significantly increased with concomitant improvement in power-to-weight ratio.

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INTRODUCTION

The work described in this report* covers both a research and a fabrication phase directed toward demonstrating the potential of large area, thin-film cadmium sulfide photovoltaic cells. The research phase was concerned with investigations of photovoltaic materials and of the crystal layer conversion process. This process results in the growth of size of the crystals comprising the thin-film layer, thus the process is aimed toward obtaining the high conversion-efficiency characteristic of single crystals. This work, which led to the delivery of five cells made of converted cadmium sulfide layers, is described in Sections I and II. The fabrication phase culminated in the delivery of three demonstration arrays composed of large-area cells on various kinds of four-inch square substrates. The CdS cell fabrication work is described in Section III.

The appendices of the report contain both the results of thermal and electrical tests performed on thin-film, large-area cadmium sulfide photovoltaic cells and a materials report describing the fabrication of the four-inch by four-inch cells.

This work has as its ultimate objective the attainment of a solar power source with output power per pound greater than that of solar sources currently in use. The effort during this final phase of the contract has confirmed the feasibility of fabricating large-area (approximately four-inch-square) cells; it has demonstrated the use of a thin (approximately 0.002-inch) flexible plastic for the cell substrate with real potential for cell weight reduction; it has demonstrated the possibility of use of integrated circuitry in order to make full use of high conversion efficiency of small-area cells and yet maintain low fabrication cost inherent in large-area cells. Although additional research and development are needed to reduce process problems and to confirm the potential of the crystal layer conversion process, the feasibility of fabricating a cell from a converted CdS layer was shown. In addition, other phases of work such as experiments concerned with radiation resistance, alternate means of depositing the active material (by silk screening), alternate barrier-forming methods (heterogeneous cells), and variation in processing parameters were performed and are described in detail. The research and fabrication work described here has taken a step forward toward meeting the overall objective in providing additional guide lines by which further improvements in the state of the art may be accomplished.

*Sections I and II are concerned with work performed by RCA Laboratories. Section III describes work performed by the Astro-Electronics Division.

Manuscript released by the authors July 1962 for publication as an ASD Technical Report.

TECHNICAL DISCUSSION

I PHOTOVOLTAIC MATERIALS

INTRODUCTION

During the earlier work as described in detail in the two previous reports*, research on photovoltaic materials resulted in the successful fabrication of photovoltaic cells made of polycrystalline films of cadmium sulfide (CdS). These layers of CdS were about 20 microns thick and were obtained by evaporation techniques. Most of the cells had initial efficiencies between 3 and 3.5 percent for areas of about 1.6 cm^2 although one cell made during the research work exhibited an efficiency of 4.5 percent for that area.

Much of the subsequent work on problems associated with the fabrication of large-area cells of the above type is described in Section III of this report concerned with "CdS Cell Fabrication."

The continued research on the materials has been concerned primarily with

1. Attempts to determine the nature of the barrier layer that forms on the standard CdS cells,

2. Attempts to exploit the potential of the Van Cakenberghe crystal conversion process for application to the production of thin-film CdS photovoltaic cells (This process converts the microcrystals of a thin evaporated layer into larger crystals and thus offers the possibility of obtaining cell efficiencies which approach the higher values obtainable with bulk single crystals.),

3. The study of heterogeneous cells,

4. Measurements of the resistance of the standard CdS cells to radiation, and

5. Fabrication of cells from CdS layers obtained by sintering techniques.

The main objectives of the research performed during the last period on photovoltaic materials have been to increase the conversion efficiency of cells fabricated from layers converted by the Van Cakenberghe process, and to evaluate the photovoltaic response of heterogeneous cadmium telluride-cadmium sulfide (CdTe-CdS) cells and cells formed from CdS layers obtained from sintering techniques.

*ASD Technical Report 61-11; Summary Technical Report on Research and Development program involving Solar Cell Array Optimization of August 1961, and Solar Cell Array Optimization (Volume II) of December 1961.

TECHNICAL DISCUSION

1. CdS CELL PROCESS CONSIDERATIONS

a. p-Type Barrier Formation. The material used to convert the n-type CdS has been copper in the form of a paste applied to the CdS surface. Originally the paste was applied to the surface and allowed to dry prior to heating. After the baking process, considerable time was required to remove the dried copper paste. Work on this particular phase of the process resulted in simplifying the process by removing the copper paste from the CdS layer before the paste has dried. The CdS layer is then placed in an argon atmosphere and heated up to 300°C. This simplified procedure, which is more compatible with the production of many and/or larger cells, has resulted in no significant differences in the efficiency of microcrystalline cells.

b. Analysis of Darkened CdS Layer. In order to produce the barrier layer, the copper paste procedure as described above is followed. This barrier layer (which becomes very dark in color) was examined to determine its chemical composition, and thermal probe measurements indicated that the darkened layer is a p-type semiconductor. X-ray diffraction experiments resulted in reflections which could not be correlated with any suspected or catalogued compounds. The darkened layer was then selectively removed by chemical treatment of the film and x-ray powder patterns were obtained from this material. These indicated the presence of a greater amount of copper sulfide (Cu_2S) than CdS. It is not known why the Cu_2S appeared in the second set of x-ray experiments and did not appear in the first. Perhaps the Cu_2S was distributed in only a very thin layer which was not sensitive to the x-rays, or perhaps a more involved compound of copper was present which was reduced to Cu_2S during the removal of the darkened layer. The results suggest that Cu_2S is an important component of the p-type barrier layer, but the spectral response curves indicate that a simple model of an abrupt junction between CdS and Cu_2S is not sufficient.

2. VAN CAKENBERGHE CONVERSION

Complete details of research performed on the Van Cakenberghe conversion process are given in the Section II, entitled "Crystal Layer Conversion." However, some work motivated by materials considerations will be described briefly here.

Early attempts to fabricate cells by the Van Cakenberghe process resulted in a cell with an active area of about 0.6 cm^2 and with a conversion efficiency of about 0.6 percent. The open-circuit voltage was relatively low (0.29 volts) and thus indicated the presence of short circuits in the cell. These short circuits were probably caused by traces of silver that remained in the grain boundaries of the layer after the conversion process. There is also difficulty in forming the barrier layer by the copper treatment; the layer is not as uniformly dark as that produced on the microcrystalline films.

A recrystallized layer which was "doped" with indium to increase the conductivity was fabricated into a photovoltaic cell. Isolated portions of the cell produced higher open-circuit voltage (V_{OC}) and short-circuit current (I_{SC}) values than the complete cell. Such an effect emphasized the existence of short circuits at the grain boundaries of the complete cell.

Short circuits caused by the silver between grain boundaries were eliminated by the use of a wash of potassium cyanide (KCN) followed by a bake in hydrogen sulfide (H_2S) at 450°C.

3. HETEROGENEOUS CELLS

From theoretical considerations of the basic requirements for high-efficiency cells, it appeared that a heterogeneous cell composed of highly conducting large-bandgap n-type material on the light-incident side, and a p-type material with bandgap for optimum efficiency with respect to the solar spectrum, could potentially be more efficient than any homogeneous cell. In addition, the junction can be placed far from either surface, which should reduce the sensitivity of cell response to ambient conditions. Because of these considerations, heterogeneous cells of CdS–CdTe were fabricated by vacuum evaporation techniques and evaluated by their photovoltaic response and by their current-voltage (I-V) junction characteristics. The n-type CdS layer was evaporated first on a glass substrate followed by the p-type CdTe layer. The CdTe layer was co-evaporated with copper in order to produce a conductive p-type layer. The double layer was then heated to 450°C in argon in order to fabricate a photovoltaic cell. The power output of these cells was very low (V_{oc} = 0.27 volt, Isc = 2.5, 2.2 and 4.0 ma for areas of 1.5, 1.1 and 1.6 cm^2 respectively); however, the efficiency deterioration was reduced greatly from that observed in the "first" CdS–Cu cells. The light source used to obtain the electrical values given above was one calibrated at 100 milliwatts per square centimeter for the CdS–Cu cells. Figure 1 gives typical current-voltage (I-V) curves for these cells and Figure 2 gives the spectral sensitivity

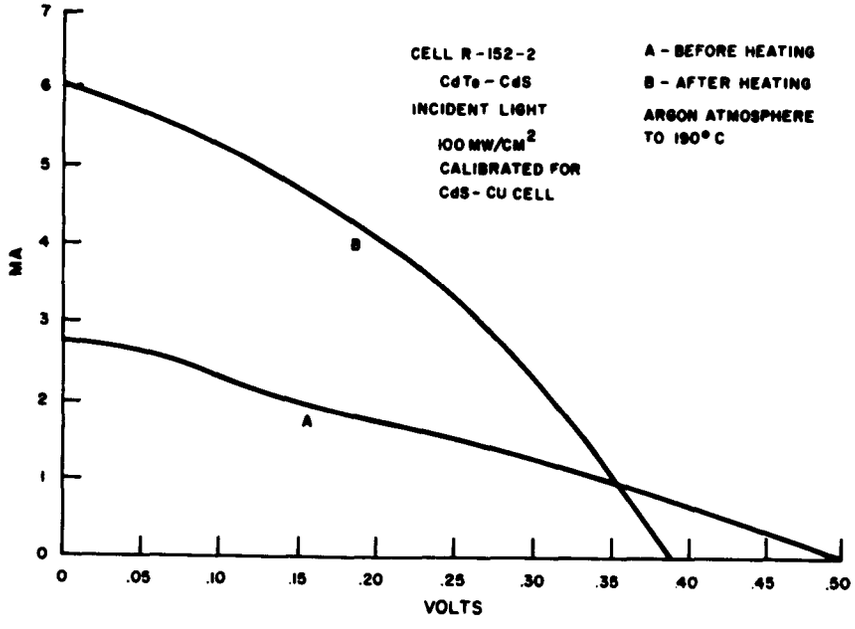
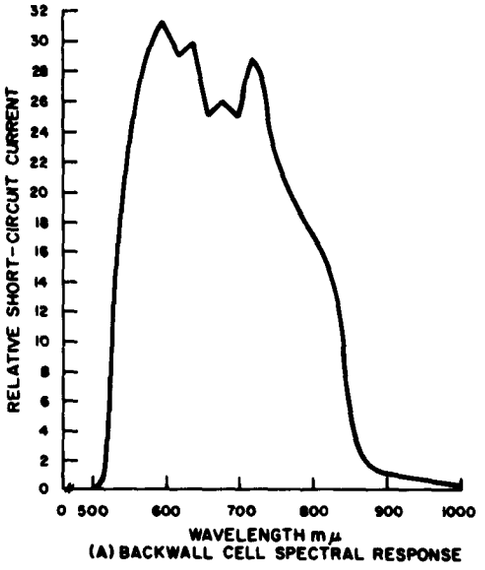


Figure 1. Heterogeneous Cell Characteristics



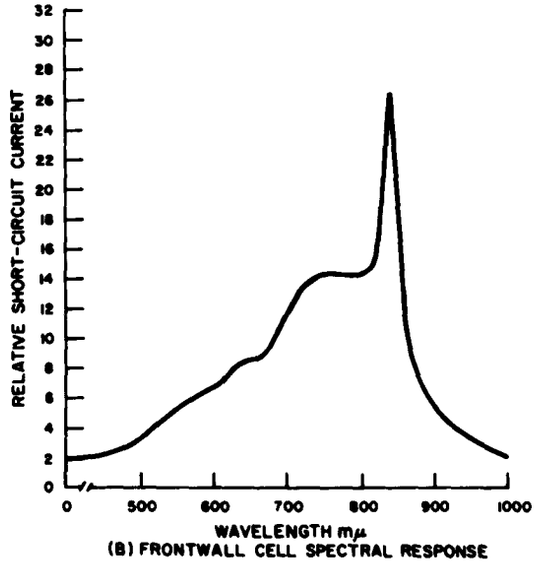


Figure 2. Spectral Response of Cells

of these cells when operated in frontwall and backwall fashions. The I-V curves in the dark show a very large forward to reverse current ratio (10^5 at 1 volt) indicating a well-defined junction. Although this characteristic deteriorated somewhat upon standing in air for several days, the high ratio could be re-established by reheating in argon. (The effect of the reheating on cell performance is also given in Figure 1.) Further work is required to determine the factors which are currently limiting the performance of these cells.

4. RADIATION EFFECTS ON CdS-Cu CELLS

a. Protons. Preliminary tests were performed on two CdS thin-film polycrystalline cells to determine radiation damage of the cells when subjected to radiation of 1.6 Mev protons. The total flux striking the two cells was about 10^{15} protons per cm^2. The short-circuit current of one cell decreased by 33 percent and of the other cell by 66 percent. The short-circuit current of a typical silicon cell is reduced 33 percent when irradiated with a flux of only about 10^{11} protons per cm^2. Thus the CdS cells appear to be more resistant to proton damage than silicon cells, in fact, the CdS cells withstand about 10^4 more protons per cm^2 before their short-circuit current is degraded to the same level as silicon cells.

b. Electrons. Two CdS thin-film cells were subjected to 0.8 Mev electrons with the following result: A cell with initial efficiency of less than one percent was subjected to a flux of 9.7×10^{15} electrons per cm^2 and a cell with efficiency of 3.4 percent was bombarded by a total flux of 8.8×10^{16} electrons per cm^2. The efficiency of the first cell decreased by 11 percent and the second by 39 percent. A greater decrease in efficiency after bombardment for cells of high efficiency than for cells of low efficiency is usually observed for silicon and for gallium arsenide photovoltaic cells also.

The efficiency of n-on-p silicon cells drops by about the same percentages as above when subjected to flux levels about one-tenth those falling on the CdS polycrystalline cells.

5. SINTERED LAYERS

The use of a silk-screen process for applying thin layers of material is attractive from the photovoltaic cell standpoint because it offers a means of making large-area thin-film layers at low cost. Experiments were performed to exploit this process using CdS as the active material and processing the layers in such a manner as to produce a photovoltaic cell.

Six materials were tried as substrates:

Flexible:

1.	"Tissueglas" - glass paper	0.002 in. (thick)
2.	Soft glass fabric	0.003 to 0.005 in.

3.	Mica	0.001 to 0.005 in.
4.	Molybdenum	0.002 in.

Rigid:

5.	Borosilicate glass 7052, 7740	0.08 to 0.10 in.
6.	Soft glass	0.08 in.

Satisfactory cells were made only on the materials Numbers 5 and 6. Deterioration of the glass-fiber structure occurred during application of the transparent conductive coating on item 1 and 2, the conductive coating did not adhere properly to the mica, and an insulating layer was formed during sintering of a CdS layer on the molybdenum substrate.

The CdS layers were deposited by silk-screen printing a substrate with a CdS "ink" made of highly purified cadmium sulfide, analytical reagent grade cadmium chloride, N300 ethyl cellulose and dibutyl Carbitol (diethylene glycol dibutyl ether). After the ink was screened onto the substrate it was allowed to level and then dried in air at a temperature of about 125°C for 10 minutes. When dried, the coating was sintered at a temperature of about 550°C. The sintering step converts the ink to a relatively conducting coating, owing to the presence of chloride and excess cadmium.

A sintered layer, 0.0002 inches thick deposited on conducting glass with an evaporated tin metal electrode on the exposed side, showed a volume resistance of 90 ohms. Layer thickness varied between one and five microns depending on the number and nature of the applied coatings. Coatings containing nine percent ethyl cellulose binder produced more homogeneous polycrystalline sintered layers than coatings containing higher concentrations of ethyl cellulose. Inks containing 2.5 percent cadmium chloride were the most useful in forming continuous sintered layers. Layers prepared by double coating, i.e., screening and sintering and then again screening and sintering, were most free of pinholes. Sintered layers prepared for inks containing unstable "impurity compounds", so that stoichiometry would be changed or excess halide would be present in the polycrystalline layer structure, showed no improvement in finished cell characteristics.

Fabrication of the photovoltaic cell was completed by applying an opaque layer of copper paste to the exposed surface of the sintered cadmium sulfide layer. The barrier layer formation was obtained as follows. The copper layer was applied by placing the CdS sintered layer in a copper organic dispersion heated to 70°C for 15 minutes. The part was next withdrawn from the bath and the organic film containing the metallic copper was removed from the sintered layer surface by the use of an organic solvent. The dried coppered surface was then covered with a microscope slide, and this assembly was in turn covered with powdered CdS. The unit was placed in a standard sintering container and fired at 285°C for two minutes. Finally the container was removed from the oven and cooled rapidly. Metallic contact to the exposed darkened surface of the CdS film was made by means of a layer of evaporated tin. Although care was taken to prevent short circuits between the darkened surface of the CdS film and the tin oxide transparent electrode, the shape of the current-voltage curve as seen in Figure 3 indicates some short-circuiting to be present.

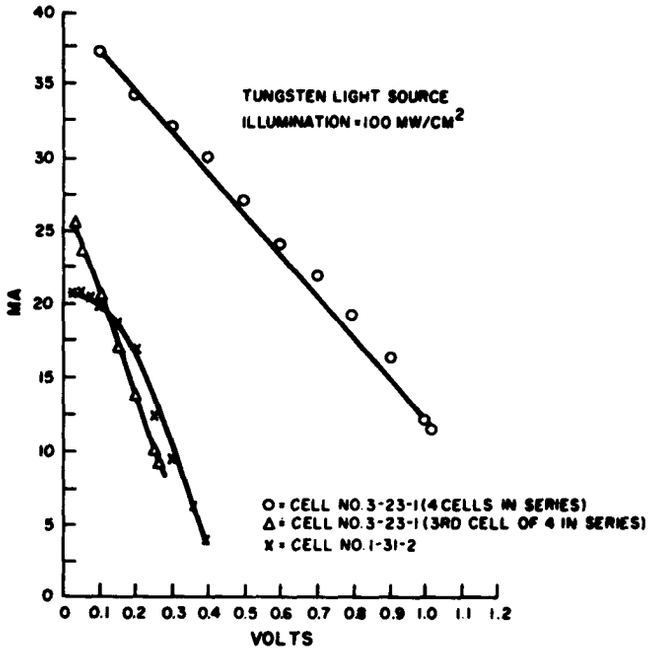


Figure 3. Current-Voltage Characteristics for Several Silk-Screened Photovoltaic Cells

The data for the electrical performance reported in Table I were taken under a tungsten light source with an intensity of 100 milliwatts per square centimeter calibrated for a silicon photovoltaic cell. Small-area cells were made on hard glass and the larger-area cells were made on 3 x 4 inch soft glass flats.

TABLE I. TYPICAL CELLS MADE WITH THIN FILM SINTERED CdS

Cell No.	Substrate	Area cm^2	Voc (Volts)	I_{sc} (ma)
	Hard Glass			
1302	7740	1.0	0.35	9.3
1312	7740	1.0	0.44	21.5
1316	7740	1.0	0.41	5.4
A03	7052	1.0	0.42	9.1
A04	7052	1.0	0.41	15.2
	Soft Glass			
311	Lime	56.0	0.425	35.2
3231	Lime	48.5	1.48	37.4
(4 strips in series)				

As can be seen from the above data, relative electrical output does not increase with cell size. The major problem appears to be the relatively high series resistance presented by the transparent tin-oxide electrode. No work was done to solve this problem.

Life test data showed that for a completed glass device with an active area of 48.5 cm^2 and composed of 4 cells in series there was no change in characteristics after a 60-day holding period in a desiccator (V_{oc}: 1.48 volts, I_{sc}: 37.4 ma).

SUMMARY AND CONCLUSIONS WITH RESPECT TO PHOTOVOLTAIC MATERIALS

The Van Cakenberghe conversion process is not suitable for fabrication of high-efficiency, broad-area cells in its present form because of difficulties due to the grain boundaries. Improvements may come after further study to eliminate problems associated with the grain boundaries.

Heterogeneous cells offer some potential in their characteristic of having the barrier layer far removed from the surface of the cell. However, work performed during this study was only preliminary and further study is required to evaluate their possibilities more fully. This work would include additional tests to determine effects limiting the performance of cells made to date as well as to optimize process conditions (such as evaporation methods) to control conductivity and thickness of the two layers.

While efficiencies and reproducibility of cells obtained in the preliminary experiments by sintering techniques were not high, the feasibility of fabricating cells by the silk screen technique was demonstrated.

Radiation experiments show that CdS polycrystalline cells are much more resistant (by a factor of 10^4) to 1.6-Mev protons than are silicon cells. The CdS cells are also ten times as resistant to 0.8-Mev electrons as are n-on-p silicon cells.

II CRYSTAL LAYER CONVERSION

INTRODUCTION

Some success has been achieved in increasing the efficiency of photovoltaic cells made from evaporated polycrystalline films of cadmium sulfide (CdS) (see previous section). In principle, however, single crystal material will be capable of higher efficiency than polycrystalline material because the high degree of order represented by the single crystal material reduces the defects (grain boundaries) at which recombination, scattering, and anomalous conduction can take place. In practice this principle is also verified; photovoltaic cells made from polycrystalline films have not yet shown efficiencies as high as can be obtained with cells made from bulk single crystals of CdS. Since a recrystallization method (hereafter referred to as the Van Cakenberghe process), for converting polycrystalline films of CdS into single crystal films has been discovered (See References 1, 2)* the possibility exists for preparing thin film CdS photovoltaic cells having the higher efficiencies possible with single crystal material. The present work represents an investigation of the underlying mechanism controlling the process, so that reproducibility and control of the process can be obtained to enable the production of films having the properties needed for high efficiency photovoltaic cells. Much progress has been achieved in this direction, but as yet it is not sufficiently advanced for the production of efficient photovoltaic cells from recrystallized films (the maximum efficiency obtained to date is between 0.5 and 1.0 percent.) The main problem remaining is the lack of control of the size and orientation of the single crystals, which leads to problems with the formation of the barrier layer and short circuits through the film. The problem of controlling the resistivity of the recrystallized films has been partially solved.

In studying the recrystallization process, much information concerning the nucleation and growth properties was obtained by direct observation of the process in situ. This is possible with CdS because it has sufficient birefringence so that the orientation changes characteristic of the crystal growth can be seen between crossed Polaroid sheets. By this means, the effects of various parameters such as substrate material, activator material, ambient gases, and CdS evaporation conditions were observed. In addition, x-ray analysis is as well as electron microscopy and diffraction, helped to determine the structural character of the films. The electrical properties of the recrystallized films were determined by measurements of conductivity, photosensitivity, Hall effect, and optical absorption. Photovoltaic cells were fabricated from recrystallized films to check the performance of the material in this application.

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* References appear at the end of the section.

TECHNICAL DISCUSSION

1. THE VAN CAKENBERGHE PROCESS

The Van Cakenberghe process consists of three basic steps. First, a microcrystalline film of CdS 1 to 20 microns thick is vacuum deposited onto a substrate (e.g., glass) under special evaporation conditions (substrate temperature and shielding arrangement) which determine the subsequent recrystallization properties of the films. Second, a very thin layer (on the order of 100 A) of an activator, such as silver or copper, is deposited. Third, the film is annealed in an inert (argon) atmosphere where recrystallization begins at one (or a very few) nucleation site once a critical temperature has been reached. The speed of advancement of the recrystallization front across the film is extremely high (on the order of several millimeters per minute). The critical temperature may have any value between 350°C and 600°C, depending on which activator is used, whether or not a little oxygen is present in the ambient gas, and the initial CdS evaporation conditions.

Under the best conditions obtained so far, using a silver activator, single-crystal areas up to one centimeter across have been obtained. These large crystals usually contain many small-angle grain boundaries, but uniform subgrains up to one millimeter across have been obtained. Figure 4 shows a typical recrystallized area where the subgrains present a feathery appearance.

With a silver activator and no oxygen in the ambient gas, the critical temperature is in the range of 475°C to 600°C, depending on the conditions of the initial CdS deposition. If a small amount of oxygen is admitted to the ambient gas, the critical temperature is reduced to between 350°C and 450°C, and the resulting crystals are considerably smaller (a few tenths of a millimeter across). With a copper activator, similar results are obtained without adding oxygen to the ambient gas. Other atmospheres in which recrystallization has been attempted are hydrogen and vacuum. In neither case did recrystallization occur, although in the case of hydrogen, nucleation sites were seen to form with a high concentration along the edge of the film (where nucleation is most probable for films which do recrystallize). Both hydrogen and vacuum are reducing atmospheres. These results suggest that oxygen may be intimately involved in the recrystallization process, but the effect of different ambients has not yet been investigated in much detail.

The amount of activator used is not critical as long as the minimum amount is supplied. This minimum amount has not been determined accurately, but 14 A of silver on 2 1/2 microns of CdS was found to be sufficient. A small amount of the activator becomes incorporated in the CdS lattice (less than 10 parts per million is

Figure 4. Typical Recrystallized Area, Between Crossed Polaroids (7X)

estimated from the level of the photocurrent resulting from impurity excitation relative to that due to interband excitation; this is indicated in Figure 9); the excess is segregated by the crystal growth process and appears as small droplets scattered over the surface, especially at the grain boundaries. Although Van Cakenberghe lists several activators for which he claims success, not all were found to work in this laboratory. Of the four tested (silver, copper, indium, lead) only silver and copper were successful in promoting recrystallization.

The recrystallization process appears to be completely independent of substrate material. Films have recrystallized on all substrates tested, including soft, medium, and hard glasses, tin oxide coated glass, silver-coated glass, carbon-coated glass, self supporting carbon films, and cleaved mica. Other workers have observed recrystallization on sheet metal substrates (see Reference 3). However, if there is a large difference in the expansion coefficients of the CdS and the substrate, the thicker recrystallized films have a tendency to break away from the substrate upon cooling to room temperature (e.g., films thicker than ten microns on Pyrex). In rare cases such films may develop striations instead of separating from the substrate as seen in Figure 5, as if stress has been relieved by a plastic deformation mechanism such as slip. The striations are parallel in any one crystal, and x-ray analysis indicates that these striations are always parallel to the line of intersection between (110) planes and the surface.

Figure 5. Film with Striations, Between Crossed Polaroids (5X)

Measurements of the speed of advancement of the growth front during recrystallization over a wide range of temperatures indicate a general trend toward higher speeds at the higher temperatures. However, the large scatter of the data (plotted in Figure 6) indicates that some other parameter besides temperature is also involved. Evidently this parameter (as yet unknown) may vary for different regions of a given film since in some instances the growth speed is different for different parts of the same film.

The most critical step in the Van Cakenberghe process is the initial CdS deposition. In order to obtain films which will recrystallize, the substrate temperature during deposition must be in the range of 150 to 250°C (200 to 225°C appears to be optimum) and the evaporation must be carried out in some kind of closed vessel (or partially closed vessel) as shown in Figure 7. The cadmium and sulfur vapors become partially trapped in this inner chamber and an unusually high vapor pressure of cadmium and sulfur exists in the neighborhood of the substrates. This allows deposition at these high substrate temperatures without loss of material and deposition occurs under conditions more closely approaching equilibrium between solid and vapor. The resulting films consist of highly ordered, relatively large-size crystallites. X-ray diffractometer studies of these films indicate a very high degree of preferred orientation; the basal (001) plane of nearly all crystallites is very nearly parallel to the substrate. The diffraction pattern may show only the (002) and higher order diffraction lines. However, there is some variation in the intensity of these lines from sample to sample, with the appearance of small peaks of other diffraction lines (pyramidal planes) in some cases. The average crystallite size appears to be about 0.1 micron.

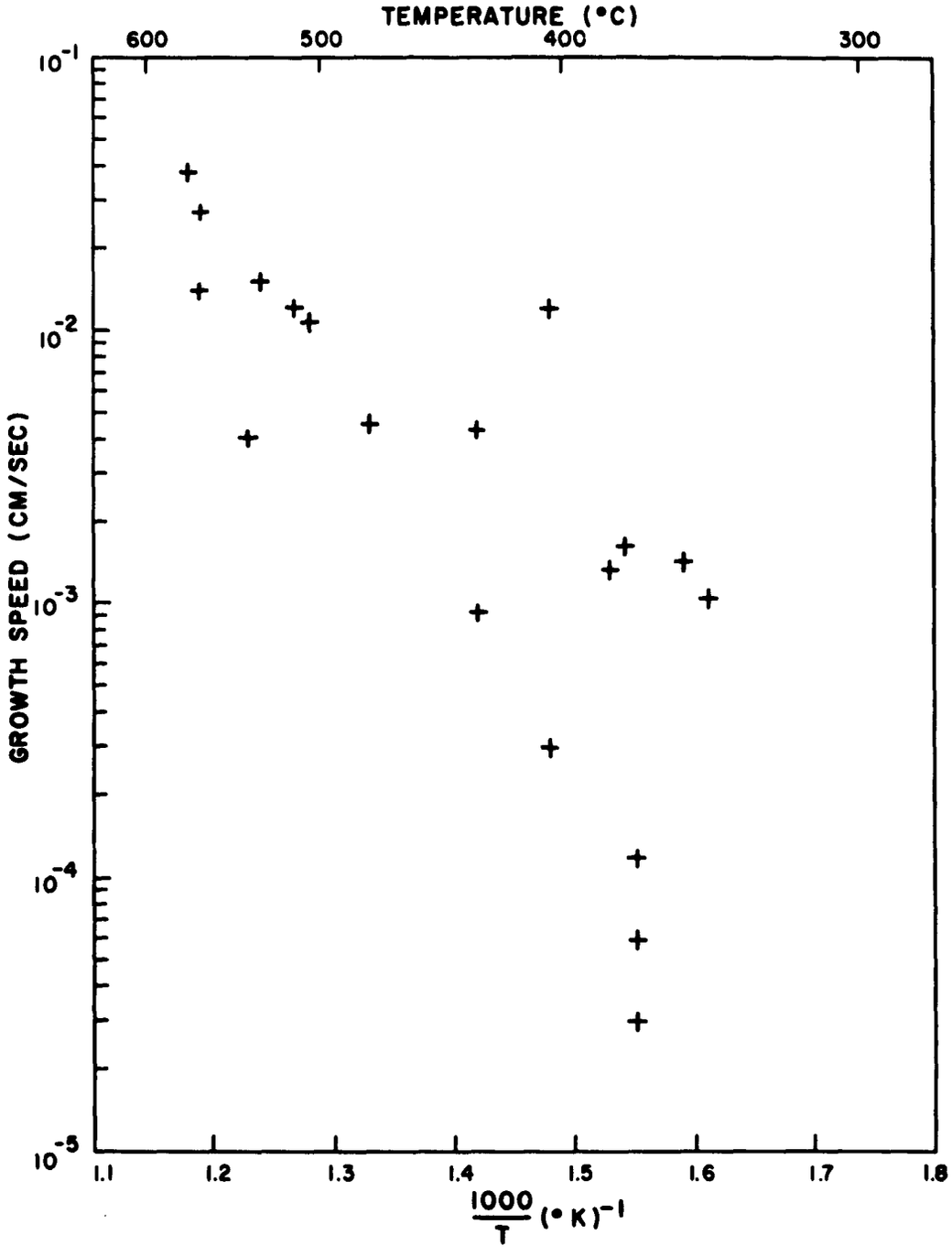


Figure 6. Plot of Log Growth Speed vs. Reciprocal Temperature

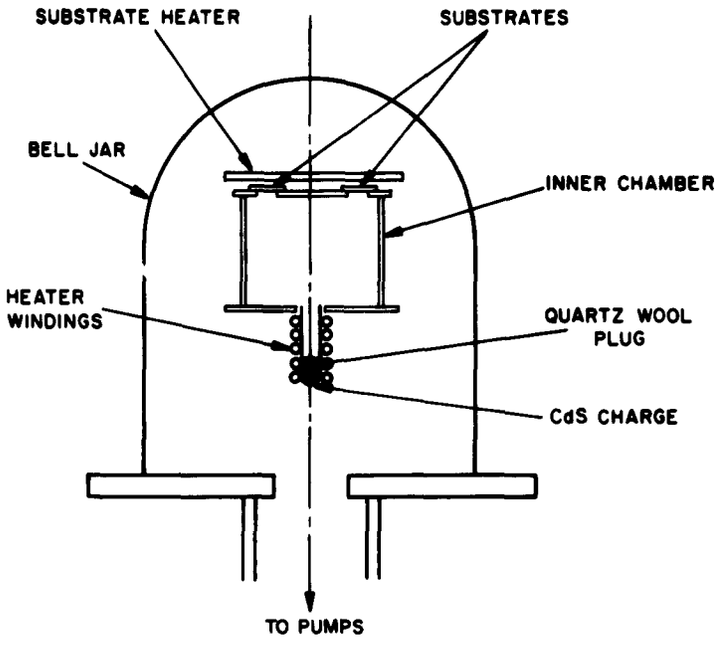


Figure 7. Schematic Diagram of Evaporation Chamber

The conditions during the CdS deposition which determine the critical temperature and the texture (size and shape of crystals) of recrystallized films are not under control at present. It is observed that all films produced together during the same CdS evaporation behave the same during recrystallization, but films produced at different times behave differently even though the evaporation conditions were the same as far as could be controlled. Observations of the variations of residual gas pressure in the bell jar during deposition indicate that a strong interaction takes place between the depositing CdS and the residual gases, even though only very small openings in the inner chamber are available for exchange of gas. It is strongly suspected that the amount and kind of residual gases which become incorporated in the films are the uncontrolled parameters which affect the recrystallization properties. The control of these parameters is the next step for attaining larger crystals, better reproducibility, and a deeper insight into the mechanism of the recrystallization process.

Initially it was expected that the recrystallization process could be observed directly by transmission electron microscopy, using the electron beam itself to heat the sample locally. This method is now considered impractical for two reasons. An attempt to recrystallize a film in vacuum was unsuccessful, and attempts to recrystallize, by the standard procedure, the very thin films (< 1000 A) needed for electron microscopy have failed. Since the detailed mechanism of the Van Cakenberghe process is not yet understood, the reason for failure in these cases is not apparent.

Electron micrographs of these very thin films show that a typical crystallite is about 0.1 micron across; this agrees with the estimates of crystallite size in the thicker films. However, transmission electron diffraction patterns of these very thin films surprisingly do not show any preferred orientation of the crystallites; this is in marked contrast to the very high degree of preferred orientation exhibited by the thicker films, and may be a clue to the explanation of the failure of the Van Cakenberghe process in these cases.

2. TENTATIVE HYPOTHESIS FOR THE MECHANISM

The following hypothesis is proposed to account in a general way for the mechanism of the Van Cakenberghe process. It is consistent with the experimental observations made to date and is at present a qualitative rather than a quantitative theory since it does not postulate the specific details of the process, such as a description of the atomic exchange processes by which the cadmium and sulfur atoms are transferred from the microcrystallites to the large growing crystal. Therefore, numbers cannot be calculated from this theory to compare with experimental results. However, such a qualitative theory is extremely valuable as a guide for future experimentation, which in turn can lead to a more quantitative theory.

a. Nucleation. Nearly all of the microcrystallites composing the vacuum deposited CdS films are oriented with their basal (001) plane parallel to the substrate. However, a few of the microcrystallites will have other crystallographic planes parallel to the substrate. This is more likely to occur at the film edges where the deposition is influenced by a nearby mask, or in the body of the film where deposition is influenced by some gross defect such as a speck of dirt. Those crystallites having one of the pyramidal planes (102), (103), (104), (105), (106), (107) or (108) parallel to the substrate are energetically favored for grain growth, and these grains grow to between one and ten microns across.* These exaggerated grains are the nuclei for the extended growth characteristic of the recrystallization process, and account for the observed orientations of crystals in the recrystallized films (x-ray diffractometer traces of recrystallized films show these orientations; most commonly, the reflection from the (105) plane is the strongest). The formation of many such nuclei at the preferred sites indicated above has been observed in films for which the extended growth was prohibited. However, when recrystallization is not prohibited, nucleation is restricted to only a very few sites, sometimes only one. The extended growth process is extremely fast compared to the grain growth process forming the nuclei; thus, once recrystallization has begun, very few additional nuclei can form in the short time remaining before the entire film has recrystallized.

* It is not yet understood why these particular orientations are favored in CdS, but the phenomenon of grain growth of favored orientations has been observed in other materials (e.g., see Reference 4).

b. Extended Growth. Two important general parameters which characterize extended growth processes are the driving force (the free energy difference between initial and final states) and the activation energy (the barrier height between initial and final states). In the present case it is believed that the driving force is due to the difference in surface energies between the microcrystallites and the large growing crystal. Difference in strain energies is not a likely source of the driving force since films recrystallize equally well on all substrates tested, including extremely thin self-supporting carbon. Neither is a temperature gradient involved. Growth has been observed to take place equally well along a temperature gradient, against a temperature gradient, and in no temperature gradient. From observations of the speed of advancement of the growth front and its detailed motion around inclusions it appears that a "liquid-like" transition phase exists at the growth front which lowers the activation energy for transfer of atoms from the microcrystallites to the larger growing crystal. This transition phase advances across the film, "dissolving" the microcrystallites before it and depositing material on the growing crystal behind it. Most of the silver (and maybe other impurities) is carried along in this transition phase much like impurities in the molten zone of a zone-refining process, except that in the present case the "molten zone" (the transition phase) is formed chemically rather than thermally. It is believed that the activator (perhaps together with the impurities which are present) is responsible for the formation of this transition phase, although its detailed composition and its relationship to the chemistry of CdS are not yet determined. The observed critical temperature may be the temperature required for this transition phase to form, or it may be the solution temperature of a dispersed phase formed by impurities in the film; similar exaggerated growth after the solution of a dispersed phase in aluminum alloys has previously been observed (See Reference 5). The effect of a different activator (copper vs. silver) on the critical temperature tends to support the former explanation; the effect of different CdS evaporations on the critical temperature tends to support the latter explanation, although it is not inconsistent with the former explanation, since impurities may also be involved in the formation of the transition phase. Direct evidence of the influence of impurities on the critical temperature was observed with indium-doped films. The indium was added by deposition on top of the silver layer before recrystallization. The critical temperature was observed to increase continuously with increasing amounts of indium from 500°C (no indium) to almost 600°C (500 A of indium on 6-1/2 microns of CdS).

In an area where sufficient activator has been deposited, the speed of advancement of the growth front is determined by the kinetics of the process by which atoms are transferred from the microcrystallites to the growing crystal. In general, three steps in this process can be considered independently: the solution of atoms from the microcrystallites, the mobility of transfer of atoms in the transition phase, and the deposition of atoms onto the growing crystal. The growth speed is determined by the slowest of these steps, and will depend only on temperature unless the detailed nature of the mechanism is also changed. For example, a different activator or different impurities may change the composition of the transition phase; greater amounts of a given impurity might decrease the mobility of atoms in the transition phase (analogous to the decrease of electron mobility by impurities in a semiconductor). The large scatter in the growth speed data (plotted in Figure 6) indicates that some such involved mechanism is operating in the films that have been studied to date. In areas where sufficient activator has not been deposited the growth speed is much lower. In these

areas the excess silver at the growth front must diffuse into the unrecrystallized area and form the transition phase before the growth front can advance. This type of diffusion-limited growth has been observed in one area where an extremely thin layer of silver was deposited (14 A), and in many cases it is observed just beyond the edge of the silver deposit at distances up to one millimeter from the edge.

The many small-angle grain boundaries, which are always found within the large crystals in recrystallized films, may be due to defects such as inclusions formed by impurities in the films. The inclusions may introduce dislocations into the lattice of the growing crystals such as to effect a slight rotation of the crystal lattice. Some types of defects (such as those introduced by the presence of oxygen in the ambient gas during recrystallization) are more likely to introduce large-angle grain boundaries. The activator itself may contribute to the formation of these defects in some cases, as indicated by the much smaller crystals usually obtained with a copper activator compared to those obtained with silver.

Knowledge and control of the impurities which enter the films during their formation, as well as a more complete description of the effects of a wide variety of ambient gases, appear to be essential for further understanding of the process. It will then be possible to determine what phases formed are active in the recrystallization process, and what defects or inclusions may be formed which introduce grain boundaries and limit crystal size. The potential benefits of this knowledge include the ability to produce consistently single-crystal films of CdS having the high degree of perfection needed for the full potentialities of devices such as photovoltaic cells, as well as the possibility of applying the principles to materials other than CdS.

3. ELECTRICAL PROPERTIES

Measurements of various electrical and optical properties of recrystallized films, such as conductivity, Hall mobility, photoconductivity, and optical absorption, give some insight into the nature of the electronic states existing in this material. A change in optical absorption is readily detectable with the naked eye; the color changes from an orange-yellow to a more definite yellow with sometimes a faint tint of green. Optical absorption spectra as shown in Figure 8 always show a small shift of the apparent absorption edge to shorter wavelengths and an increased absorption in the neighborhood of 6000 A after recrystallization.

A large increase in the Hall mobility is effected by recrystallization. The microcrystalline CdS films have mobilities of one cm^2 per volt second or less, whereas recrystallized films have mobilities in the range of 20 to 30 cm^2 per volt second, and some as high as 70 have been seen. None of these measurements were made on areas that did not contain some grain boundaries, and this may partially account for the difference between the mobilities in these films and those in bulk crystals (200 to 300 cm^2 per volt second).

Some of the most informative measurements were those involving photoconductivity. Spectral response curves of Figure 9 show the effect of the acceptor center introduced by the activator (silver or copper) in the neighborhood of 6000 A. From the relative magnitude of this response to that at about 5000 A (due to interband

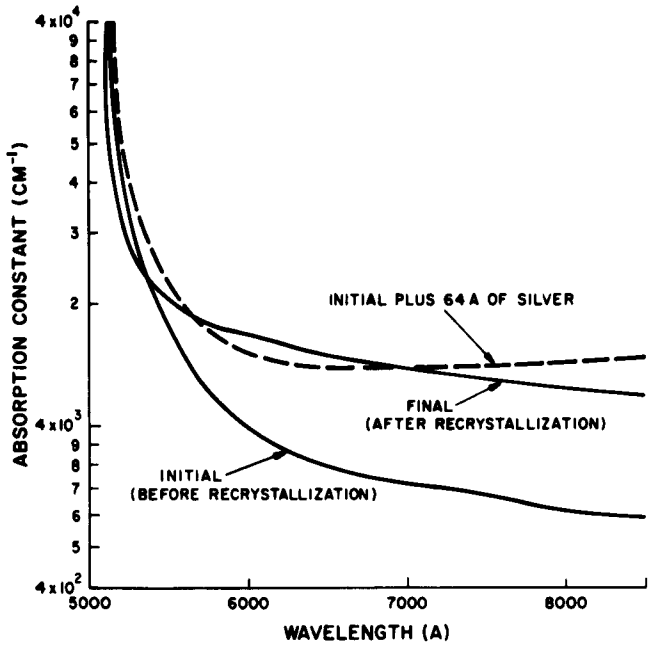


Figure 8. Optical Absorption Spectra of CdS Films at Room Temperature

excitation) it appears that less than ten parts per million of these acceptor centers are introduced into the lattice during the recrystallization process. The thermally stimulated current response shown in Figure 10 indicates the existence of a wide distribution of compensated donor centers (traps) from about 0.18 to 0.60 electron volts below the conduction band, containing a total concentration of 10^{18} to 10^{19} traps per cm^3. Since the recrystallization process increases the dark resistivity by many orders of magnitude (values as high as 10^8 to 10^9 ohm cm), it appears that the effect of recrystallization is to introduce a large number of acceptor centers which very nearly compensates the large donor concentration present in unrecrystallized films. Evidently the acceptor centers introduced by the activator do not account for the total concentration of acceptor centers introduced during the recrystallization process.

In recrystallized films the light-to-dark conductivity ratio may reach values as high as 10^5 or 10^6 at high light levels (100 to 1000 foot-candles). This high sensitivity to light is due mainly to the large increase in the dark resistivity (discussed above); light conductivities at high light levels are not very different from those found in unrecrystallized films that have been baked. For application in photovoltaic cells high conductivity material is needed to reduce series resistance. Fortunately, solar cells are operated at very high light levels where the conductivity of the recrystallized material is reasonably high. However, recrystallized films can be obtained with

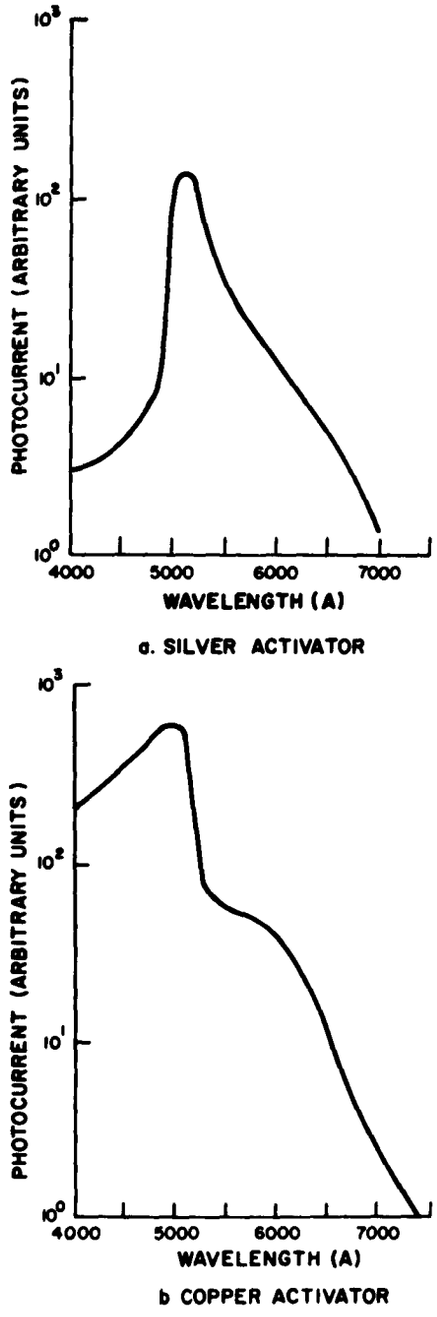


Figure 9. Spectral Response of Photoconductivity, Recrystallized Films

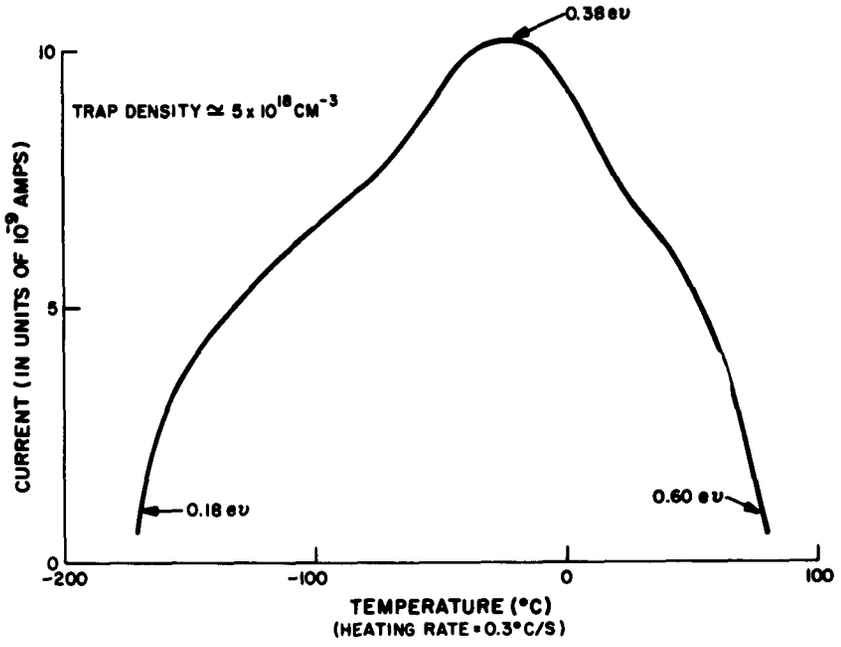


Figure 10. Thermally-Stimulated Current

very low dark resistivities by "doping" with indium (resistivities as low as 0.3 ohm cm have been attained). This is done by depositing indium on top of the silver before the film is recrystallized. The indium does not seem to affect the texture (crystal size and shape) of the recrystallized films but the critical temperature for recrystallization increased significantly with increasing amounts of indium. Figure 11 shows the results of measurements of conductivity as a function of indium thickness. To a first approximation the photocurrent is independent of the indium concentration; only the dark current is affected. There is also evidence that the indium is not distributed uniformly throughout the entire film; conductivity measurements in different areas of the same film may give different results. Evidently some of the indium may also be segregated from the CdS by the crystal growth process. Perhaps the segregation coefficient may vary with the orientation of the growing crystal. Detailed photoconductivity and optical absorption measurements have not yet been made on indium doped samples.

4. APPLICATION TO SOLAR CELLS

The procedure used to fabricate photovoltaic cells from the recrystallized CdS films (formation of the barrier layer) is identical with that used to fabricate cells from the microcrystalline films. The best cells obtained to date have efficiencies of about

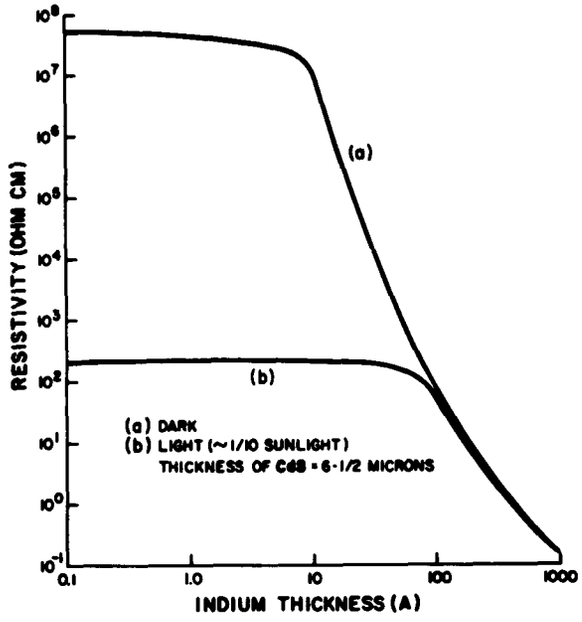


Figure 11. Resistivity of Indium-Doped Films

0.5%, with open circuit voltages of about 0.3 volts and short-circuit currents of about 10 ma per cm^2. However, most of the cells have shown much lower efficiencies and open-circuit voltages. In all cases the cells seem to be hampered by short circuits between the barrier surface and the tin oxide electrode on the substrate. To investigate this problem in more detail the current-voltage (I-V) characteristics of recrystallized films (between an electrode on top of the film and the underlying tin oxide electrode) have been studied. In all cases the CdS layer was completely short-circuited after the application of only a few volts (sometimes less than one volt was sufficient). The source of these short-circuit paths was thought to be the few remaining grain boundaries which are continuous between the top surface of the film and the substrate; in addition, these grain boundaries are sites where silver has accumulated during the crystal growth process. The first attempt to eliminate the short-circuit problem was the isolation of areas containing no large-angle grain boundaries. No significant improvement was observed. Evidently some of the small-angle grain boundaries are equally effective short-circuit paths. For the second attempt, films were baked at 450°C for one half hour in hydrogen sulfide (H_2S) with the expectation of converting the conducting silver in the grain boundaries into non-conducting silver sulfide (Ag_2S). This approach so far has been completely successful only if the excess silver on the surface has been removed before baking by washing in potassium cyanide (KCN). Films treated in this way can withstand about ten times as much voltage (20 to 50 volts) as untreated films; this is comparable to the breakdown voltage of unrecrystallized areas. Preliminary measurements on these films indicate that the dark

resistivity is reduced to about 10^6 ohm cm, but the light resistivity is unchanged or increased by this treatment. Also, the effects of indium doping seem to be nullified by this treatment, and the conductance of the tin-oxide electrode on the substrate is destroyed. These side effects of this baking process are generally undesirable. Other attempts to eliminate the short-circuit problem have been deposition of a CdS overlay on the recrystallized film and deposition of a CdS overlay on the silver layer before recrystallization. In the first case there is a problem in obtaining a uniform overlay deposite; the depositing CdS seems to avoid the previously recrystallized film. In the second case the two layers recrystallize semi-independently in some areas and the grain boundaries in the two layers do not coincide. The short-circuit problem is apparently eliminated in these areas (the films can withstand up to 150 volts before breakdown). However, other areas evidently recrystallize with coincident grain boundaries in the two layers. In these areas there is no improvement; short circuits are formed as readily as in single layer films.

It is possible that one of these methods could be developed to produce films satisfactory for fabrication of efficient photovoltaic cells. However, it would seem more fruitful to eliminate the trouble at its source, i.e. eliminate the grain boundaries. This involves a more fundamental study of the effects of impurities on the recrystallization process (discussed earlier). Some work in this direction has begun. A completely sealed all-quartz inner chamber for evaporation of the CdS has been built (as in Figure 12) and some preliminary tests of this chamber have been made. The chamber can be completely baked at high temperature before closing the lid. The first few layers of CdS deposited on the walls should be a perfect getter for all residual

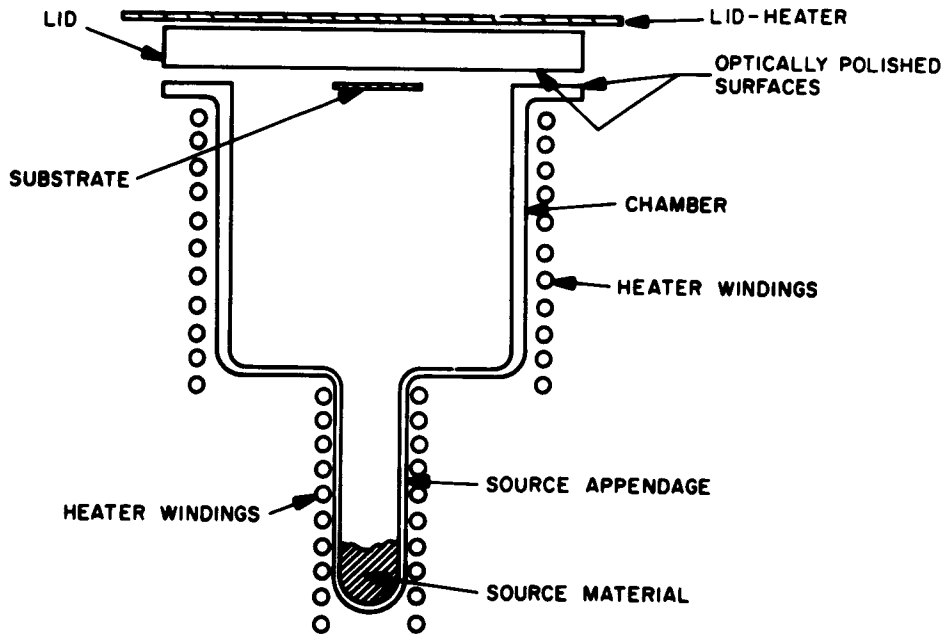
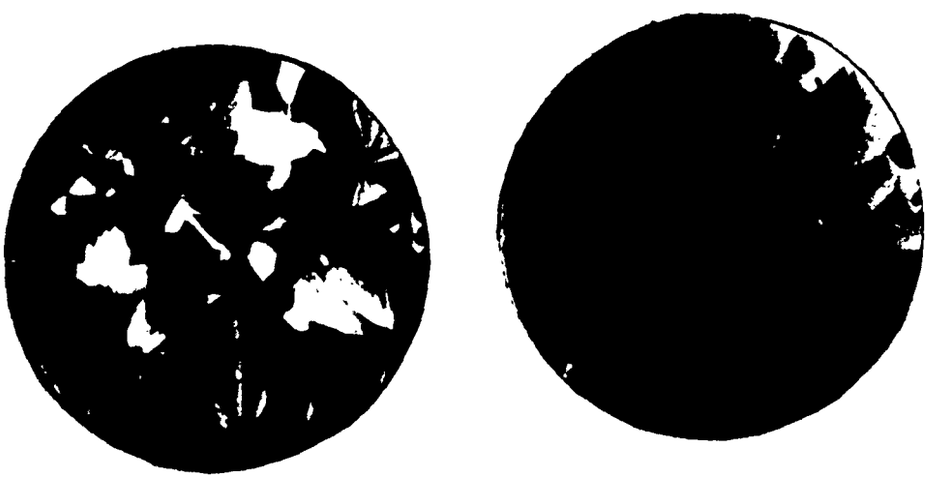


Figure 12. Schematic Diagram of Completely Sealed Chamber

gases that can react with the deposit in any way. No further source of gas is present inside the chamber. All heaters and gaskets as well as bell jar surfaces and diffusion pump back-streaming are external. Thus, once the chamber is cleaned up, any pressure within the chamber should be solely due to the vapor of the material being deposited and residual gases trapped within this material. Since the latter can be investigated independently and cleaned up by proper preparation in advance, the resulting films should be much cleaner than those obtainable in any conventional vacuum system.

In addition to the short-circuit problem there appears to be a problem in forming the barrier layer on recrystallized films. The amount of darkening of the surface due to the formation of the barrier layer is not uniform but is a very sensitive function of crystal orientation in the film (as seen in Figure 13). It is found qualitatively that those crystals whose c-axis is tilted the greatest (from the normal to the substrate) show the least darkening; crystals whose surface is more nearly parallel to the basal (001) plane are the darkest. The copper treatment which forms the barrier layer apparently is more effective on surfaces which are close to (001) planes. Since the mechanism of the formation of the barrier layer is not understood it is hard to account for this orientation dependence. However, processes which may be involved, such as diffusion, alloying and etching, are known to be anistropic in many cases. The fact that similar copper treatment of bulk CdS crystals does not show such large differences



a. Observed Between Crossed Polaroids Before Treatment

b. After Copper Treatment; No Polaroids (Diameter = 3/8 in.)

Figure 13. Effect of Crystal Orientation on the Amount of Darkening by the Barrier-Forming Copper Treatment

in darkening on the different surfaces indicates that this problem can be solved. The surfaces of these bulk crystals probably contain residual damage from previous polishing operations. The interaction of the copper with these surfaces may be determined more by the characteristics of the damaged layer than by the particular crystallographic plane parallel to the surface. This suggests that attempts to correct the problem of non-uniform darkening on recrystallized layers might begin with pretreatment of the surface by etching or polishing. However, as in the case of the short-circuit problem, a more satisfactory solution would seem to be elimination of the grain boundaries, so that the entire surface of the film would be completely homogeneous.

SUMMARY AND CONCLUSIONS WITH RESPECT TO CRYSTAL LAYER CONVERSION

The Van Cakenberghe process is a solid-state recrystallization phenomenon whereby microcrystalline, thin-film deposits are converted into films that are single crystals over large areas. The process as applied to CdS has been studied under a wide variety of conditions in an effort to understand the detailed mechanism involved, and to obtain better control of the properties of the recrystallized films. The procedures for successful operation of the process have been established. These include special conditions for the evaporation of the CdS which produce highly ordered microcrystalline films with a fixed (within wide limits) impurity content, the addition of an activator (silver or copper), and annealing in an inert atmosphere. The process is sensitive to different amounts and types of impurity which are added or removed at any stage of the procedure; at present, only the impurities incorporated in the films during the CdS deposition are not under sufficient control. The process appears to be completely independent of substrate material. The main defects in the films prepared to date are the many small-angle grain boundaries. A tentative qualitative hypothesis for the mechanism of the process is advanced to guide future experiments. Its main points are: (1) nucleation is controlled by the energetically favored grain growth of microcrystallites having certain specific orientations with respect to the matrix, (2) extended growth is driven by the free energy difference between the microcrystallites and the large growing crystal, (3) the activation energy for the extended growth is reduced by the formation of a transition phase in which atoms are highly mobile; the activator is an essential component of this transition phase but the CdS and impurities may also be components. In order to determine in more detail the nature of this transition phase, as well as to eliminate the grain boundaries, the impurities which enter the films during the CdS deposition must be controlled (reduced to a negligible level). It is expected that this can be accomplished by means of a modified arrangement for evaporation of the CdS which makes use of a completely sealed quartz chamber within the vacuum system. The effects of controlled amounts of impurities can be studied by introducing them at a later stage (by deposition or by addition to the ambient gas present during recrystallization).

A variety of electrical measurements indicate that the recrystallization process introduces a large number of acceptor centers which almost completely compensate the large number of donor levels initially present. The recrystallized films therefore having a high dark resistivity (10^8 to 10^9 ohm cm), a high trap density (10^{18} to 10^{19} cm^{-3}), and a high light-to-dark conductivity ratio. Some of the acceptor centers (but probably not all) are associated with the activator used for recrystallization. The high dark resistivity can be reduced many orders of magnitude by "doping" with indium. The electron mobility is increased more than an order of magnitude (from less than one to about 30 cm^2 per volt second) by recrystallization.

When photovoltaic cells are fabricated from recrystallized films two main problems are encountered. First, the grain boundaries, which are sites of excess silver, act as short circuits through the cell and second, the barrier layer does not form uniformly over the entire surface but the amount of darkening is sensitive to the orientation of the different crystals in the film. Due to these problems, solar cells with efficiencies greater than one percent have not been fabricated from these films. Attempts to eliminate the short-circuit problem included baking in H_2S and overlay depositions of CdS. Some success has been achieved, but further tests and evaluation are required for conclusive evaluation. Because of the problems that have arisen in connection with the grain boundaries and limited size of crystals now obtainable in recrystallized films, it is recommended that in the future emphasis be placed on more fundamental studies of the effects of impurities on the recrystallization process.

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III CdS CELL FABRICATION

INTRODUCTION

This section describes the works on cell fabrication by the evaporation method of cadmium sulfide-layer deposition. The objectives included the following:

a. Further increase in cell area,

b. Reduction in cell weight,

c. Increase in efficiency for large area cells,

d. Elimination or reduction of deterioration of cells with time, and

e. Delivery of one square foot of cells completely assembled and tested.

Progress was accomplished on the first four of these objectives and cells comprising two square feet in area were prepared and delivered. Individual cell area was increased to 100 cm^2. Feasibility was shown of reduction of cell weight (from that of the 15-mil glass substrate type) by an order of magnitude to 0.015 gram per cm^2 on a flexible substrate, with a potential power density of 10 to 20 watts per pound or better. Cell efficiency was increased by 96 percent from 1.38 percent (of a year ago) to 2.7 percent on the 25 cm^2-size substrates, and by 100 percent from 0.5 percent to 1.1 percent on the 100 cm^2-size substrates. Cell performance deterioration has been reduced to the extent that no decay in efficiency occurred in a number of cells during a three-month shelf life.

Techniques of making terminal contacts to individual cells were developed in anticipation of assembly of cells into arrays. It was found that a large area contact (such as that resulting from the use of a wire mesh) instead of a point contact substantially increases the power output of the cell as expected.

TECHNICAL DISCUSSION

Experiments with materials and processes were conducted concurrently with the work of increasing the cell area. The cells delivered incorporate all the improvements which were developed. Details of these are described in the following pages of this report.

1. MATERIALS

The materials used in the study are as follows:

a. Cadmium sulfide; RCA Lancaster No. F-2108 luminescent powder

b. Fine copper powder (75 to 100 micron particles) suspended in an organic lacquer binder

c. Hydrochloric acid; CP grade

d. Tin, granular; Fischer Scientific Co.

e. Conductive epoxy cement; Epoxy Products No. 3021

f. Silver wire mesh, 0.005-inch wire diameter by 0.017-inch opening; Newark Wire Cloth Co., No. 35 x 40

g. Solvent; Reliable Chemical and Paste Co., Dare Thinner

h. Gold Wire

i. Chromium-coated filament

j. Substrate; Borosilicate glass plates were used for most of the cells, in two thicknesses: 0.060-inch and 0.015-inch. These plates were coated with tin oxide to provide electrical resistance of 30 to 60 ohms per square and optical transmission of 80 percent. An experimental organic polymer film 0.001 inch thick was also tested as a substrate and useful cells were fabricated on it. The optical transmission curves of the polymer film and of the borosilicate glass are shown in Figure 14.

2. EQUIPMENT

The major equipment used in the study is listed below.

a. Vacuum Systems. Two vacuum systems were used, both of which were equipped with 18-inch by 30-inch bell jars. The first system, a Veeco VS 400 (shown in Figure 15) is capable of attaining a vacuum of 10^{-8} millimeters of mercury and has been used for CdS evaporation. The other system, a Kinney PW400, is used mainly for the evaporation of metals and other materials. As shown in Figure 16, special fixtures were designed and built for this second system to accommodate three separate inner chambers (made of seven-inch-diameter glass tubing). Each chamber consists of an evaporator, a substrate support, and a heater; in operation, three evaporations with three substrates can be performed simultaneously in one pump-down. Alternatively, deposition of three different materials, with one following the other on the same substrate, can be accomplished in one pump-down by means of mechanical motion in transporting the substrate from one chamber to the next. This arrangement saves considerable pump-down time. Both systems are equipped with Welch 1397 mechanical pumps (which reduces pumping time) and four inch oil diffusion pumps.

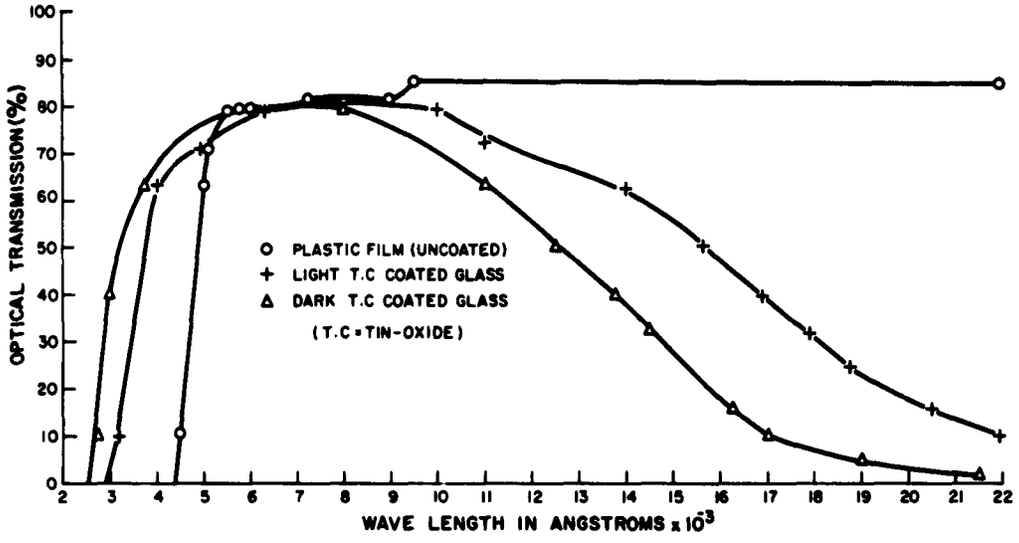

Figure 14. Optical Transmission Curves of Substrates

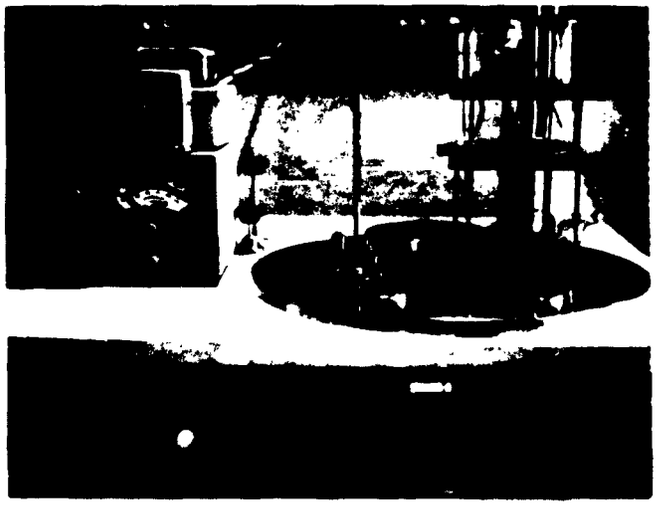

Figure 15. Veeco Vacuum System, with CdS Evaporator

Figure 16. Kinney Vacuum System, with Special Fixtures

b. Copper Diffusion. The diffusion of the copper is performed in argon within a tube heated to 300°C in a furnace as shown in Figure 17.

c. Cell Testing Rack. This equipment consists of a tungsten light source, a water filter, a cell mounting, a milliameter, a Keithley VTVM Model 200, and a Moseley 3S x-y Recorder as illustrated in Figure 18.

3. PROCEDURE

The glass substrate is first thoroughly cleaned with a detergent then soaked in distilled water for one hour (with the distilled water changed every 15 minutes).

After removal from the soaking bath, the substrate is rinsed with distilled water, acetone, and finally with isopropyl alcohol; it is then placed in a stainless-steel-mesh basket suspended in a vapor degreaser employing isopropyl alcohol as a cleaning agent. (The vapor degreaser is a corrosion-testing apparatus with a water-cooled condensing column to prevent the escape of the vapor into the room.) The substrate remains in the degreaser for one hour with the alcohol boiling.

For the plastic substrate, the plastic film is attached, by means of epoxy cement, to a frame made of tantalum strips. It is then cleaned by the same process as for the glass sheets as described above. Electrically conductive coatings of chromium and gold are evaporated on the film.

Figure 17. Copper Diffusion Tube, in Furnace

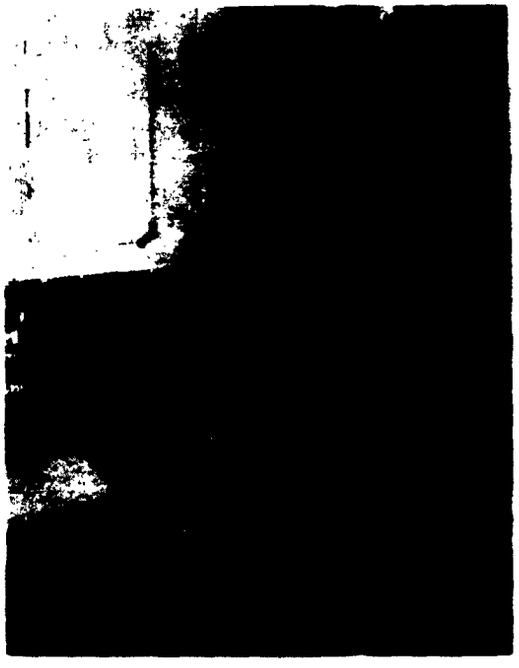

Figure 18. Cell Testing Rack

The evaporator, shown in Figure 19, is charged with 40 to 50 grams of CdS and a plug of quartz wool five millimeters high is inserted in the tube above the charge. A secondary heater, consisting of several turns of tantalum wire is inserted in the mouth of the evaporator tube and pressed against the quartz wool.

A clean glass chimney tube, five inches high and six inches in diameter, is mounted above the evaporator. The tube has a slit at right angles to its axis through half the diameter at a distance of one inch from the top.

The substrate is assembled with a mask and heater on top of the chimney. (The substrate heater is a glass sheet with a conductive coating on one side.) A thermocouple is placed in contact with the 1/16-inch glass substrate, or against the substrate heater for the 15-mil glass or the plastic-sheet substrates.

A shutter is placed in the chimney-tube slit, the system is closed by means of a bell jar, and evacuation to a pressure of 10^{-6} millimeters of mercury (or less) is started. The substrate heater is turned on to degas the substrate at 200°C to 250°C for one hour. (150°C for the plastic substrate). Meanwhile, the CdS powder in the evaporator is degassed at 500°C for 30 minutes, then the temperature (of the CdS) is raised to 1000°C, and the substrate temperature is reduced to 175°C (for the glass material): The deposition of the CdS on the substrate begins when the shutter above the evaporator is opened; the deposition time usually lasts 50 minutes for a layer thickness of 40 to 60 microns. Pressure within the bell jar ranges from 3×10^{-7} to 8×10^{-7} millimeters of mercury during deposition.

After removal from the bell jar the CdS layer is inspected for pinholes or other obvious defects and its thickness measured with a microscope. It is then etched for five seconds in a solution of hydrochloric acid (1:1). The barrier layer is formed by immersing the CdS layer in a copper paste (and rotating the layer) at 60°C to 70°C for 45 minutes, then heating the substrate to 300°C in argon.

The top electrode is applied by evaporating tin over the barrier layer. The silver-wire mesh is then attached to the tin with the conductive epoxy cement and a lead wire is soldered to the silver mesh. For the other electrode, stranded wire is cemented to the substrate around its periphery and a lead wire soldered to the stranded wire.

4. EXPERIMENTS AND RESULTS

In the course of the work, a number of experiments were performed in addition to preparing, assembling and testing cells for delivery. A description of these experiments follows:

a. Cell Area. Most of the cells produced last year were of a one-inch by one-inch size with a few two-inch square cells. This year, the cells produced are principally of a four-inch by four-inch size except for a few smaller units fabricated for special purposes. In the transition to large-area cells, much work was required to modify processes to enable reproducibility of useful cells. A new substrate-degreasing apparatus was constructed to provide a sufficiently clean surface to alleviate the CdS-layer peeling problem.

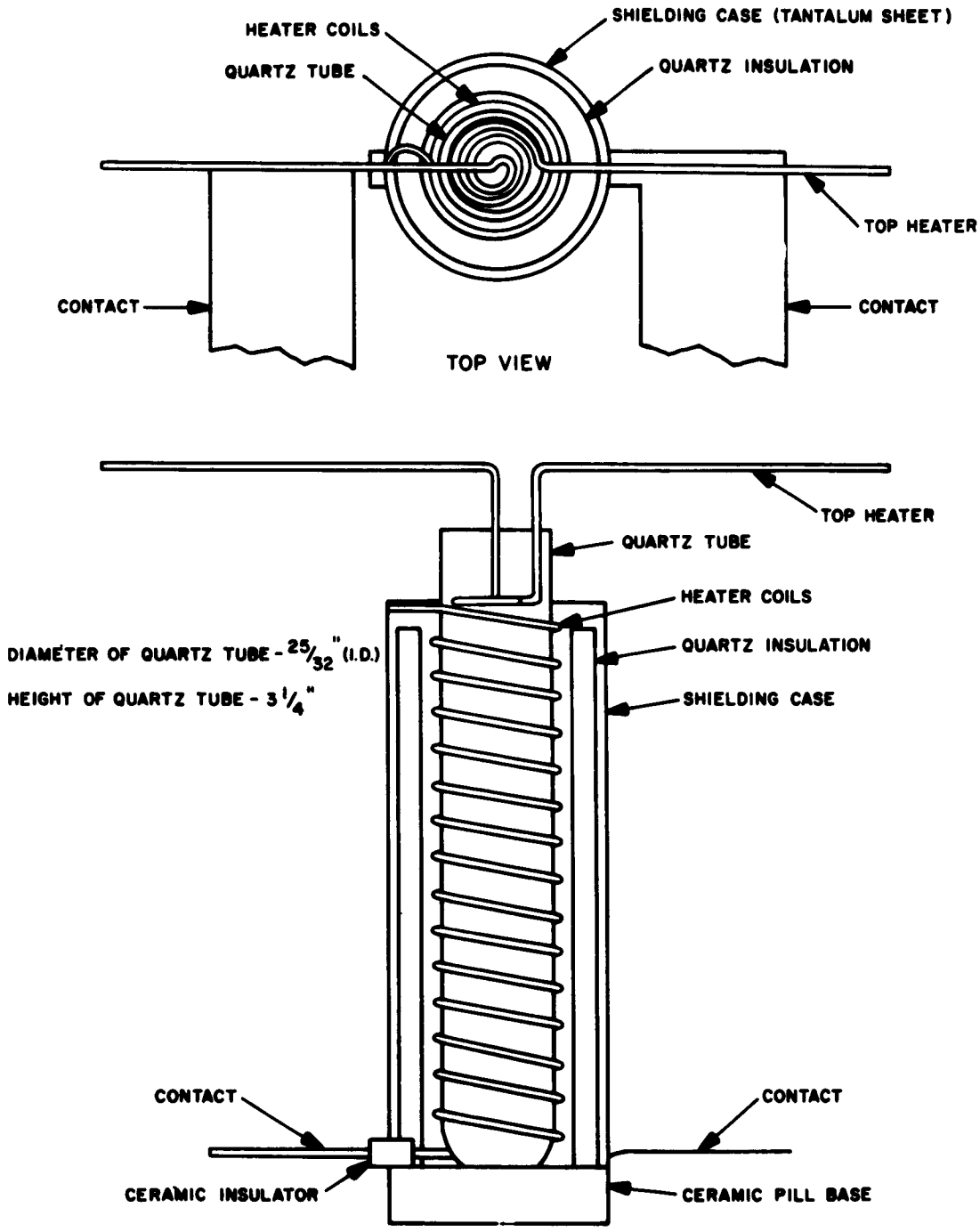

Figure 19. Cadmium Sulfide Evaporator, Sectional Diagram

Uniform deposition of the CdS layer over the large areas proved extremely difficult. Initially, four evaporators, each six centimeters high and one-and-one-half centimeters in diameter were used as sources at a distance of seven inches from the substrate. The principal disadvantage of this arrangement was the necessity for repeated evaporations to build up the required CdS layer thickness since each evaporation produced only 10 microns or less. Previous experience indicated that electrical leakage through pinholes would result from thin layers; also, such cells exhibit a low conversion efficiency. To increase the CdS vapor pressure without raising the evaporator temperature, the distance between the source and the substance was reduced to three inches. The CdS layer thickness was increased by this method but the coating was very uneven. The portions of the substrate directly above each of the four evaporators displayed a ring about one-half inch in diameter. The center of this ring showed heavy deposits of CdS with a light deposit immediately adjacent to it. The light deposit is probably due to excessive heat radiated from the Vycor* tube of the evaporator. The overall substrate temperature was also raised to 250°C.

The cells prepared from such layers produced a very low yield. The same condition continued with a four-inch distance between the source and substrate. This distance was next increased to six inches with some improvement of the CdS layer uniformity, but the reproducibility was less than desirable both in layer thickness and texture.

The design of the evaporator was then changed. First a molybdenum-wire-coil evaporator 1.25-inches long and 0.75-inch diameter, coated with aluminum oxide (alundum) was tested; this proved unsatisfactory due to cracking of the alundum coating. Next, an evaporator was constructed with an eight-centimeter-long, two-and-a-half-centimeter-diameter Vycor tube around which tantalum heater wire was wound as in Figure 19. An auxiliary heater is used at the top of the evaporator to insure that no CdS powder would be carried to the substrate by sputtering. This evaporator has sufficient capacity for CdS powder that one unit of this design replaces the four used previously.

A distance of five inches between source and substrate was used with the single evaporator at the center. This arrangement has eliminated the non-uniformity of CdS deposit and substrate overheating observed in the earlier models, besides enabling better control of the layer thickness. Most of the later cells were prepared with this system. The effect of the CdS layer thickness may be seen in the results listed in Table II below.

TABLE II. VARIATION OF CONVERSION EFFICIENCY WITH CdS LAYER THICKNESS (ALL 4" x 4")

Cell No.	CdS Layer Thickness, Microns	Isc, Ma	Voc volts	Pm mw	η efficiency, %
220	13	345	0.39	42	0.48
183	23	216	0.42	40	0.49

*Corning Glass Co. Trademark

TABLE II. VARIATION OF CONVERSION EFFICIENCY WITH CdS LAYER THICKNESS (ALL 4" x 4") (Continued)

Cell No.	CdS Layer Thickness, Microns	I_{sc}, Ma	V_{oc} volts	P_m mw	η efficiency, %
190	32	360	0.40	47	0.55
186	73	470	0.39	66	0.85
222	98	660	0.43	100	1.12

b. Cell Weight. Two approaches were followed to reduce the cell weight. Since the weight of the substrate is the controlling factor, one approach is to reduce the thickness of the glass plate and the other is to employ a lightweight material other than glass. For the first method, glass plates four inches square and 0.015-inch thick were obtained and handling techniques were developed for the processing. A number of finished cells were prepared as listed in Table III; reproducibility is very good as the performance of later cells indicates.

TABLE III. ELECTRICAL CHARACTERISTICS OF CdS CELLS ON 0.015-INCH-THICK GLASS SUBSTRATE (ALL 4" x 4")

Cell No.	I_{sc} ma.	V_{oc} volts	P_m mw	η efficiency, %	Remarks
192	288	0.39	39.0	0.67	single cell
194	190	0.85	55.0	0.76	two in series
197	95	0.82	24.0	0.34	two in series
198	242	0.82	62.0	0.80	two in series
204	114	0.64	25.2	0.34	two in series
206	164	0.82	42.5	0.56	two in series
207	152	0.75	35.0	0.48	two in series
208	235	0.75	70.0	0.95	two in series
209	450	0.43	73.0	1.03	two in parallel
226	485	0.43	82.0	0.92	single cell

An experimental plastic film, of thickness from 0.001 inch to 0.003 inch, was tested as a substrate. In order to maintain a flat surface throughout the processing at various temperatures, a frame and a technique of attaching the plastic to the frame were developed. At first, a frame material having a coefficient of thermal expansion higher than that of the plastic film was used. This frame was satisfactory if sufficiently heavy to withstand the stress resulting from the film. In order to reduce the size and weight of the frame, strips of tantalum metal were used for the frame material. The

plastic film is preheated to 200°C, attached to the tantalum frame with Eccobond* epoxy cement 104A and 104B, and then cured. This frame and technique proved very satisfactory and most of the four-inch-square cells were prepared in this manner.

Very thin layers of chromium and gold are deposited on the plastic film by vacuum evaporation to provide one of the two electrodes of the cell. For backwall type of cells, metal layers have been obtained with optical transmission of 60% and resistance of 20 to 30 ohm-cm. Metal layers of less than one ohm-cm were used for frontwall type of cells. Since the CdS layer is deposited at 175°C and the barrier layer is formed at 300°C, fabrication of the cells on plastic substrates is further complicated by the differences in the coefficients of thermal expansion of the plastic (approximately 5×10^{-5} per °C), the CdS layer (approximately 4×10^{-6} per °C), and the gold (approximately 14×10^{-6} per °C). Because of the higher coefficient of thermal expansion of the plastic film, the gold layer would tend to develop cracks during heating and to peel during cooling. To compensate for this difference, the chromium and gold layers were deposited at 200°C so that during cooling these layers would be under compression because of the greater amount of contraction of the plastic. During heating, this strain is relieved, and cracks do not result.

To prevent short circuits between the barrier layer and the gold layer, an insulating coating of calcium fluoride (about 1/4-inch wide) is deposited around the periphery of the gold layer by vacuum deposition.

The rest of the processes for the production of the plastic-substrate cells are the same as those for the glass-substrate units. When making front-wall type plastic-substrate cells, grids of silver paste were used as the top electrode. Characteristics of some of the plastic-substrate cells are shown in Table IV.

TABLE IV. ELECTRICAL CHARACTERISTICS OF CdS CELLS ON PLASTIC SUBSTRATE

Cell No.	I_{sc} ma.	V_{oc} volts	P_m mw	η efficiency, %	Remarks
152A	8	0.40	1.2	0.42	Backwall, 1" x 1" size
152B	25	0.46	3.5	0.29	Backwall, 2" x 2" size
223	83	0.30	7.6	0.15	Frontwall, 4" x 4" size
227	135	0.36	13.6	0.23	Backwall, 4" x 4" size
230	130	0.36	12.0	0.21	Backwall, 4" x 4" size

Table V below lists cell weight and power density (in watts per pound) for cells fabricated on various substrates. Conversion efficiency of 1.1 percent was used in all cases for this computation since this efficiency has been obtained for four-inch-square cells and can be reproduced. It is anticipated that higher efficiencies may be possible for this size of cell with further development. Note that the cell weight of the plastic-substrate cells does not include the weight of the metal frame, since in ultimate

*Emerson and Cuming, Inc.

application, the frame will probably be removed before assembly. One set of data is given for cells with a silver wire mesh attached (to provide a large-area contact) and one set of data is for the cells without the wire mesh. The weight of the wire mesh and the conductive epoxy cement used to fasten the mesh to the cell is apparently capable of considerable reduction.

TABLE V. WEIGHT AND POWER DENSITY OF CdS CELLS ON VARIOUS SUBSTRATES

Substrate	Cell Weight, grams		Power Density W/Lb.	
	with Mesh	without Mesh	with Mesh	without Mesh
Glass, 4" x 4" x 0.062"	47.1	41.7	1.1	1.2
Glass, 4" x 4" x 0.015"	17.2*	14.1	2.9	3.5
Plastic, 4" x 4" x 0.002"	4.6	1.5	10.7	33.3

*Two meshes for two 2" by 4" cells on one 4" x 4" plate.

c. Conversion Efficiency. Attemps to obtain higher conversion efficiency have always been the major objective. Numerous attempts have been made to achieve this, and a description of these follows.

(1) CdS Layer Thickness. The effect of the CdS layer thickness on conversion efficiency is clearly shown in Table II; this effect has also been observed in smaller cells. A 100-percent increase in efficiency coupled with a very high short-circuit current (as shown in the I-V curve of cell Number 222, Figure 21) indicated a much more efficient utilization of photon energy, a nearly optimum non-stoichiometry of cadmium and sulfur, and possibly, better crystal orientation. The fact that the open-circuit voltage remains unchanged indicates that the barrier layer is the same and that there are no short circuits due to pinholes when the CdS layer is thicker than a certain minimum limit. (This limit is much below 98 microns.)

(2) Doping of the CdS Layer. Several materials and techniques were tested in doping the CdS layer. A positive indication was observed when the CdS layer was heat-treated at 400°C for four hours with CdS powder doped with copper and chloride ions. A 40-percent (or greater) increase in conversion efficiency for the doped, heat-treated layers over untreated layers is shown in Table VI below.

TABLE VI. EFFECT OF COPPER- AND CHLORIDE-ION DOPING ON CdS CELL EFFICIENCY †

Cell*No.	Doping and Heat Treatment	I_{sc} ma.	V_{oc} volts	P_m mw	η efficiency, %	Increase in efficiency %
176-10	none	34	0.47	8.2	2.4	-
176-14	none	31	0.48	8.2	2.4	-
176-15	Cu, Cl ions; 400°C, 4 hr.	47	0.45	11.5	3.4	41

TABLE VI. EFFECT OF COPPER- AND CHLORIDE-ION DOPING ON CdS CELL EFFICIENCY † (Continued)

Cell* No.	Heat Treatment	I_{sc} ma.	V_{oc} volts	P_m mw	η efficiency, %	Increase in efficiency %
189-1	none	15	0.44	4.0	2.2	-
189-5	none	32	0.45	8.5	2.6	-
189-7	Cu, Cl ions; 400°C, 5 hr.	49	0.43	10.0	3.1	31
189-9	Cu, Cl ions; 400°C, 5 hr.	33	0.44	5.8	3.2	31
199-6	none	35	0.42	9.4	2.7	-
199-2**	Cu, Cl ions; 400°C, 4 hr.	42	0.41	9.3	3.4	26

* First three digits indicate CdS evaporation number and last one or two digits indicate cell number of evaporation; e.g. 176-10 means cell No. 10 of evaporation No. 176.

** Glass container broke during heating and air leaked in.

† All cells on 1" x 1" substrate

J. Dresner in work* at RCA Laboratories, found the introduction of copper and chloride ions as above to result in some conversion of the CdS film into small crystallites and in an increase of Hall mobility from five to 300 cm^2 per volt-second. Dresner believes that the copper ions constitute the acceptor impurity while the chloride ions contribute to the conductivity. The conductivity of such films ranges up to 10^{11} ohm-cm in darkness to 10^4 ohm-cm in light.

Several attempts were made to apply this process to the four-inch-square cells, but in all cases blistering and peeling occurred in the CdS layer. This is attributed to gas evolution from the glass substrate during the heat treatment since the temperature used is much higher than that in the degassing procedure before CdS deposition. Further work will be performed with a high-temperature heater for substrate degassing.

In two experiments zinc sulfide (ZnS) was incorporated because of its higher band-gap energy of 3.2 volts. In one experiment, CdS evaporation 134, 0.5 percent of ZnS was introduced into the CdS powder; in a second case, evaporation 137, five percent ZnS was used. The results are shown in Table VII below.

*J. Dresner, RCA Laboratories, Private Communication

TABLE VII. EFFECT OF ZINC SULFIDE ON CdS CELLS

Cell No.	ZnS %	I_{sc} ma.	V_{oc} volts	Pm mw	η efficiency %
134-2	0.5	26	0.48	7.0	2.2
134-3	0.5	31	0.49	8.8	2.7
137-1	5.0	0	0.67	-	-
137-4	5.0	0	0.62	-	-

The ZnS, in sufficient quantity appears to increase the output voltage of the cells. However, the high resistance of the cells (4.8×10^4 ohm at 1.2 volts backward, 8×10^2 ohms at 1.2 volts forward compared with 1.2×10^4 and 8×10^1 for regular cells) limits the output current.

Addition of 0.1 percent of potassium iodide to the CdS powder did not appear to improve the cell efficiency. The resistance was reduced to 12 ohms in the forward direction and 22 ohms in the backward direction, indicating that the combination of potassium iodide with zinc sulfide should be tried in the future.

Diffusion of chloride ions into the CdS layers was tested by heating the layers in an atmosphere of ammonium chloride and hydrogen sulfide at 300°C overnight. The layers become heavily etched but no improvement in efficiency was observed.

Finally, the introduction of copper by co-evaporation with CdS, and also by sputtering from a copper rod into the CdS layer, was tried. Both processes were followed by heating in argon at 450°C for 2 to 4 hours. Neither of these layers produced any output.

(3) Effect of Oxygen. R. Williams, *, in his work on the photoconductivity of single-crystal CdS, found that the presence of oxygen on the crystal surface increases the photovoltage. CdS layers were heated in air at 400°C to 500°C for various lengths of time. White deposits, believed to be cadmium sulfate, were observed on the surface. Under a high-powered (800 X) microscope, numerous large particles were seen dispersed in the layer; X-ray diffraction, however, indicated only CdS. The crystal orientation changed somewhat in this process, with the C-axis inclined rather than normal to the substrate. Since thick CdS layers tend to develop cracks, especially when heated to higher temperatures, successive depositions of very thin CdS layers (with heating in air following each deposition) were also tried. In all the tests, no increase in electrical output was seen. Williams' results were obtained for the photovoltage between the bulk of the CdS single crystals and the free surface exposed to various atmospheres. The difference in results between Williams' experiments and those described here may be attributed to the broad-area metal contact on the CdS polycrystalline cells.

*R. Williams, RCA Laboratories; Private communication

(4) Effect of Substrate Temperature. The temperature of the substrate during the CdS layer deposition was found to have a significant effect on the conversion efficiency of the cells. This is shown in Table VIII, below.

TABLE VIII. EFFECT OF SUBSTRATE TEMPERATURE ON CONVERSION EFFICIENCY OF CdS CELLS

Cell No.	Substrate Temp. °C	I_{sc} ma.	V_{oc} volts	Pm mw	η efficiency, %	Remarks
101-1	175	35	0.47	8.0	2.5	1"x1" cell
101-4	175	35	0.50	6.8	2.1	1"x1" cell
102-2	250	24	0.48	4.5	1.5	1"x1" cell
102-4	250	32	0.36	4.2	1.3	1"x1" cell
103-1	125	24	0.47	5.3	1.6	1"x1" cell
103-2	125	27	0.46	5.4	1.7	1"x1" cell
104-2	125	14	0.48	3.3	1.2	1"x1" cell
104-3	125	17	0.46	4.2	1.3	1"x1" cell
105-2	135	26	0.46	5.8	1.8	1"x1" cell
105-3	135	27	0.47	6.7	2.2	1"x1" cell
108-1	96	-	-	-	-	1"x1", CdS layer peeled
108-3	96	-	-	-	-	1"x1", CdS layer peeled
109-1	200	28	0.46	7.2	2.2	1"x1" cell
109-3	200	30	0.45	6.6	1.9	1"x1" cell
121	200	194	0.48	40.8	2.4	2"x2" cell
122	175	180	0.49	39.0	2.3	2"x2" cell

The layers deposited at a low substrate temperature appear to be dark and of low resistance, probably due to an excess of cadmium in the layer. Those deposited at a high temperature exhibit a light yellow color and a high resistance due to the chemical composition closer to the stoichiometric ratio of cadmium and sulfur. The optimum substrate temperature appears to be between 175°C and 200°C where layers of orange-brown color are produced.

(5) Effect of Etching Solution. Before forming the barrier layer, CdS layers are normally etched with a 6-molar solution of hydrochloric acid. Nitric acid and sulfuric acid etching as well as no etching were also tested. These results are shown in Table IX below.

TABLE IX. EFFECT OF ETCHING SOLUTION ON CONVERSION EFFICIENCY OF CdS CELLS*

Cell No.	Etching Solution	I_{sc} ma.	V_{oc} volts	Pm mw	η efficiency, %
116-1	HNO_3	43	0.48	11.6	3.4
116-2	HCl	44	0.49	12.3	3.6
116-3	H_2SO_4	43	0.49	11.1	3.3
116-4	none	44	0.49	12.3	3.5
120-1	HCl	40	0.47	12.1	3.6
120-2	HNO_3	40	0.46	11.6	3.5
120-3	H_2SO_4	42	0.46	12.4	3.8
120-4	none	40	0.46	10.8	3.3

*All cells 1" x 1" size

The etching apparently increases the efficiency (over no etching) and the hydrochloric acid produces more consistent and slightly higher average efficiency than the other acids.

(6) Effect of Barrier-Layer Forming Technique. Normally, the barrier layer is formed by immersing the CdS layer in a suspension of finely divided copper in an organic vehicle. Other techniques including evaporation of copper (Cu), cuprous oxide (Cu_2O) and cuprous sulfide (Cu_2S), as well as sputtering of copper, were investigated. The results are listed in Table X. It is indicated that none of these methods is equal to the one presently in use.

(7) Effect of Metal Grids. As the cell area increases, the conversion efficiency decreases as shown in Figure 20. An empirical equation for this curve shows

$$N = 5.7 - 2.33 \log A,$$

where

N is conversion efficiency in percent,

A is cell area in cm^2.

This reduction in efficiency seems to be due principally to the increase in the series resistance of the cells. The effects are shown in Figure 21 for a one-inch-square cell (Cell No. 131-4), a two-inch-square cell (Cell No. 127), and for a four-inch-square cell (Cell No. 222). The current-voltage curve loses its rectangularity as the area increases. In attempts to reduce this resistance, grids of several metals were evaporated onto the glass substrates. CdS layers were deposited over the grids and fabricated into cells. These results are shown in Table XI.

TABLE X. EFFECT OF ALTERNATE BARRIER-FORMING TECHNIQUES ON EFFICIENCY OF CdS CELLS

Cell No.	Barrier Layer	I_{sc} ma.	V_{oc} volts	Pm mw	η efficiency, %
111-1	Evaporated Cu_2S	6	0.13	-	-
111-2	Evaporated Cu_2S	7	0.16	-	-
111-3	Evaporated Cu_2S	12	0.23	-	-
124-1	Evaporated Cu_2S	5	0.22	-	-
124-3	Evaporated Cu_2S	4	0.18	-	-
144-3	Evaporated Cu_2S	4	0.13	-	-
114-1	Evaporated Cu_2O	2	0.10	-	-
114-4	Evaporated Cu_2O	0	0	0	0
115-1	Evaporated Cu_2O	0	0	0	0
115-2	Evaporated Cu_2O	0	0	0	0
132-2	Evaporated Cu	0	0	0	0
132-4	Evaporated Cu fired at 450°C in air	0	0	0	0
133-1	Evaporated Cu	0	0	0	0
133-2	Evaporated Cu fired at 500°C in air	0	0	0	0
133-3	Evaporated Cu fired at 450°C in argon	0	0	0	0

TABLE XI. EFFECT OF METAL GRIDS ON EFFICIENCY OF CdS CELLS

Cell No.	Metal Grids	I_{sc} Ma.	V_{oc} volt	Pm mw	η efficiency, %	Remarks
121	Ag	194	0.48	40.8	2.4	2"x2" size
122	Ag	180	0.49	39.0	2.3	2"x2" size
127	none	168	0.53	38.4	2.2	2"x2" size
133A	Sn	133	0.44	20.0	1.2	2"x2" size
135	Al	156	0.47	27.5	1.6	2"x2" size
146	Au	160	0.47	34.8	1.9	2"x2" size
158	Pt.	205	0.40	40.0	0.5	4"x4" size
162	Pt.	265	0.45	50.0	0.6	4"x4" size
179	Cr-In	205	0.41	40.0	0.6	4"x4" size

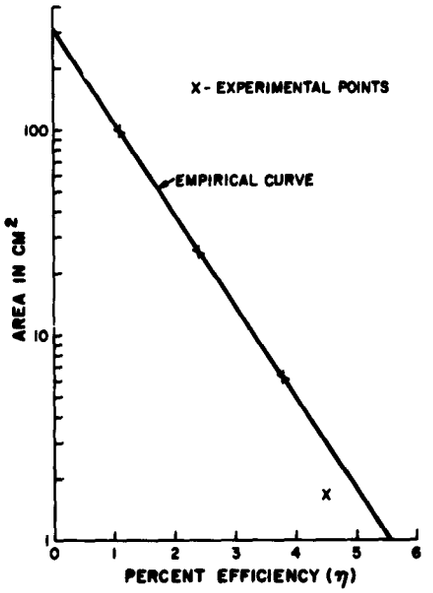

Figure 20. Effect of Cell Area on Efficiency

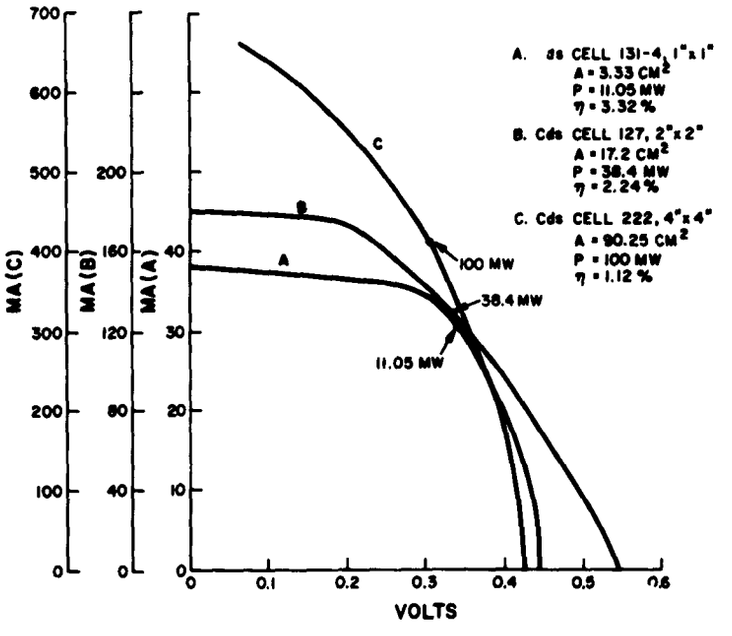

Figure 21. I-V Curves for CdS Cells (1" sq., 2" sq., 4" sq.)

In another experiment, a very thin layer of indium was first evaporated on a four-inch-square substrate and CdS deposited over it. The layers were then fired at 400°C for two hours in argon in order to diffuse the indium into the CdS layer, thus improving its optical transmission and reducing the resistance of the CdS layer. However, when it was fabricated into a cell, no electrical output was observed. The chemical composition of the CdS layer changed as it turned into a light yellow color.

The use of silver grids on the two-inch-square cells may have slightly improved the efficiency when only the active area is used for computing the cell efficiency, but the reduction of transmitted light in the area covered by the grids also decreases the electrical output of the cell, therefore the overall conversion efficiency is not materially affected. In this work, conversion efficiency is reported on the basis of the entire CdS area without subtracting the areas covered by grids or wire mesh. This method of calculation is believed to be the only accurate and practical method.

(8) Effect of Integrated Circuitry. High series resistance appears to be inherent in all large area cells. In order to achieve high power-to-weight ratio and maintain low cost, employment of integrated circuitry seems to be a logical solution. Here a number of cells can be prepared on a large substrate by the same process used for a single cell. By proper application of electrodes, these cells can be connected in series or in parallel. For instance, a CdS layer can be deposited on a 4"x4" substrate in four equal areas by one evaporation through the use of a mask. Barrier layers are then formed over the four CdS layers, also by one operation. With proper masks, electrodes are prepared on the four cells, for series or parallel connection, by one evaporation. In so doing, both high conversion efficiency and low cost can be realized. This is illustrated in Table XII, by the cells on 4"x4" substrates, measured as single cells and then as sub-divided cells.

The reduction in series resistance is seen by the increase in rectangularity of the current-voltage curves when the unit is connected as (1) a single cell, (2) two cells in parallel, (3) two cells in parallel and two in series and (4) four cells in parallel. The curves are shown in Figures 22 and 23; Figures 24 and 25 illustrate the parallel and series connections, respectively. Thus the integration of a number of cells on a single substrate enable further increase in the size of each unit without sacrifice in efficiency and at lower cost, when both cell fabrication and interconnection are considered.

d. Cell-Efficiency Decay. The efficiency of CdS cells has been observed to deteriorate very rapidly in storage. However, cells stored in a vacuum or with a drying agent such as phosphorous pentoxide (P_2O_5) seem to suffer no decay in efficiency. An experiment was performed with two cells in order to identify the cause.

One cell, No. 131-4, was exposed to 100-percent relative humidity at 100°C; the other, cell No. 131-3, was subjected to the same temperature, but the relative humidity was that of room air (20 to 30 percent). The efficiencies of these cells were measured (at room temperature) after each hour of exposure for three consecutive hours. After the third hour, the conditions for the two cells were interchanged, i.e, cell No. 131-3 was exposed to the 100°C, 100-percent relative humidity condition and cell No. 131-4 was exposed to the 100°C, 20 to 30 percent relative humidity. The results of these test are shown in Figures 26 and 27.

TABLE XII. EFFECT OF INTEGRATED CIRCUITRY ON CdS CELL EFFICIENCY

Cell No.	Subdivision	Electrical Connection Mode	I_{sc} ma.	V_{oc} volts	Pm mw	η efficiency, %
182	none	-	315	0.42	45	0.53
182	Two	in parallel	375	0.42	62	0.72
182	Four	in parallel	390	0.42	81	1.22
186	none	-	88	0.43	11	0.14
186	Two	in parallel	164	0.43	21	0.27
186	Four	in parallel	194	0.43	26	0.32
194	Two	in series	240	0.86	69	0.80
194	Four	in series	108	1.75	57	0.81
194	Four	Two in series Two in parallel	228	0.86	72	1.00
194	Four	in parallel	464	0.43	81	1.10

The curves show that the effect of moisture on the conversion efficiency is quite drastic during the first hour of exposure where the efficiency reduction is about 46 percent in the 100-percent relative humidity exposure, over an order of magnitude greater than that of the cell exposed to low humidity. After the first hour, the efficiency of the cells decays at about the same rate, approximately ten percent per hour. The effect is also shown for the other cell (131-3) when the humidity was increased during the fourth hour. It is probable that the cells were almost saturated with water vapor during the first hour of exposure to high humidity and that the subsequent exposure reflects the thermal effect in low humidity.

Several methods were investigated to eliminate or reduce the decay in conversion efficiency. These included covering the cells with (1) polystyrene deposited by the glow-discharge methods, (2) silicon oxide (SiO) coating by evaporation, (3) SiO and polystyrene (4) Kodak Photo Resist (KPR) coating, (5) SiO and KPR, (6) thin Mylar* film attached with adhesive, and (7) thin copper sheet attached by ultrasonic soldering. Covering with materials (3) and (6) slows down the decay but does not eliminate it.

Since the resistance through the cell increases with decay, an investigation of the electrode contact was pursued. Instead of the silver paste as customarily used for the electrodes, metallic silver (Ag) was evaporated in a vacuum over the barrier layer. Evaporated tin (Sn), zinc and cadmium, and a high-temperature silver paste were also evaluated. With the exception of those cells with evaporated zinc and

*DuPont trade name

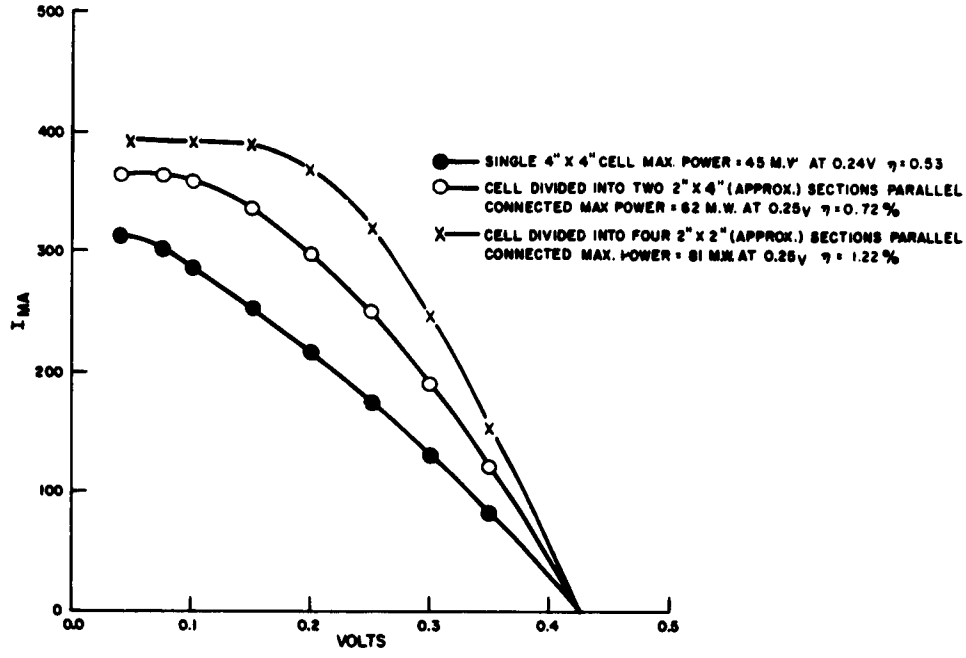

Figure 22. Integrated Circuitry Experiment

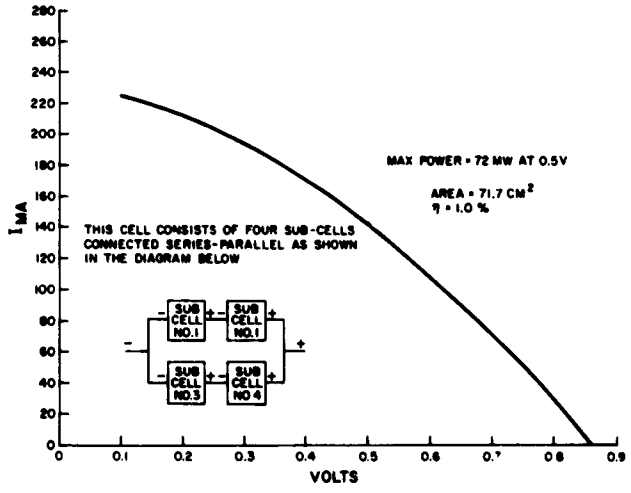

Figure 23. Integrated Circuitry Experiment

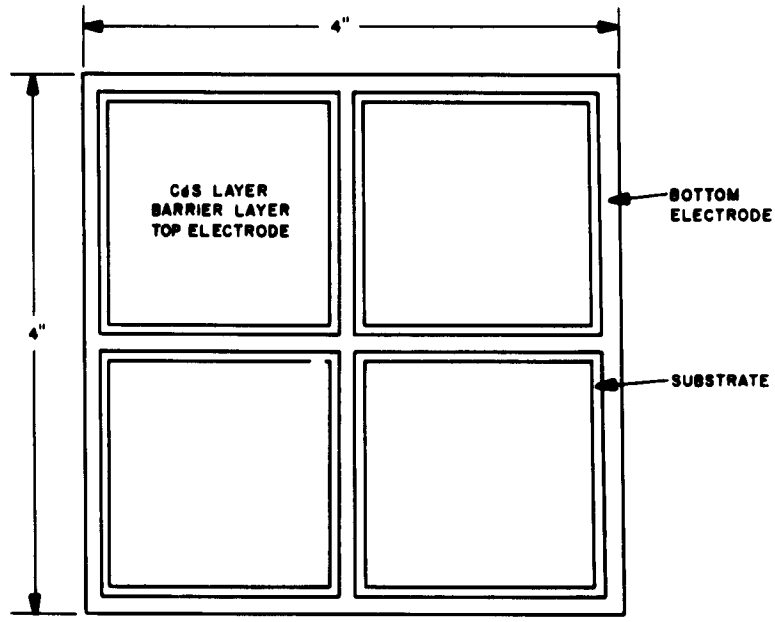

Figure 24. Four Cells in Parallel, Top View

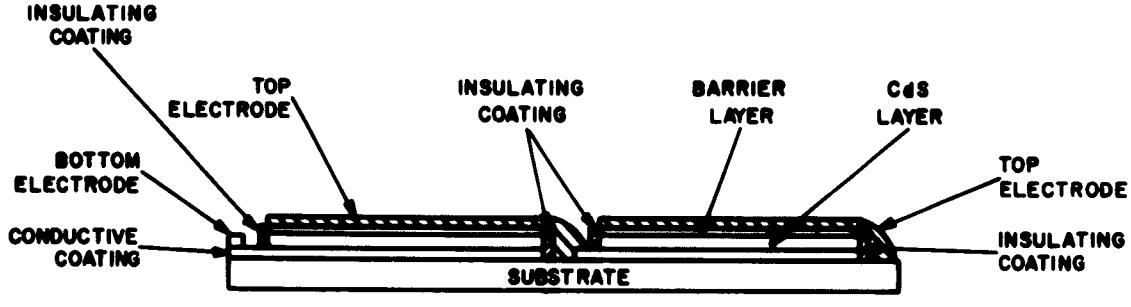

Figure 25. Two Cells in Series, Side View

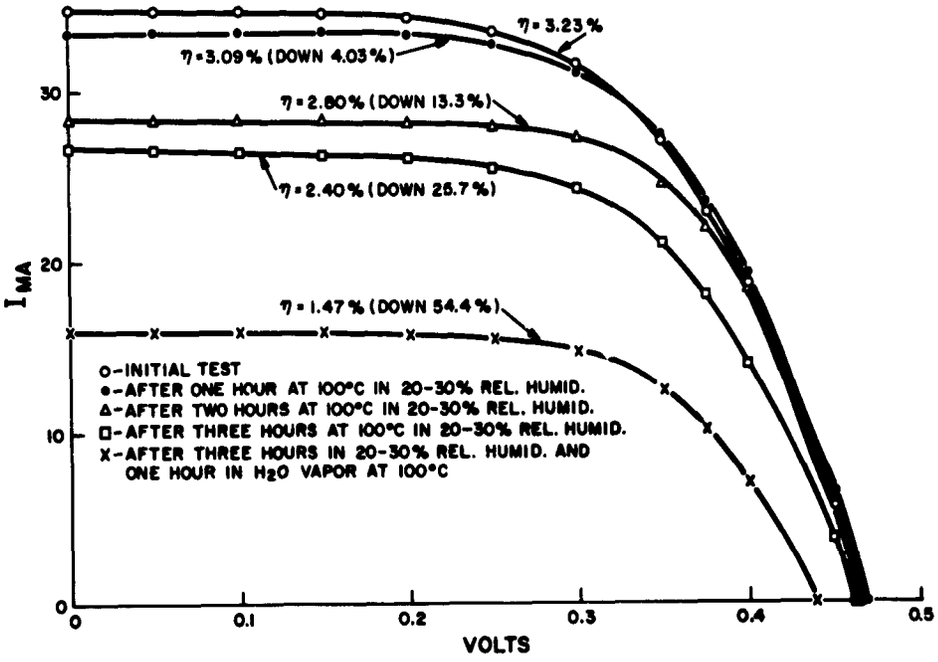

Figure 26. Humidity Test, Cell No. 131-3

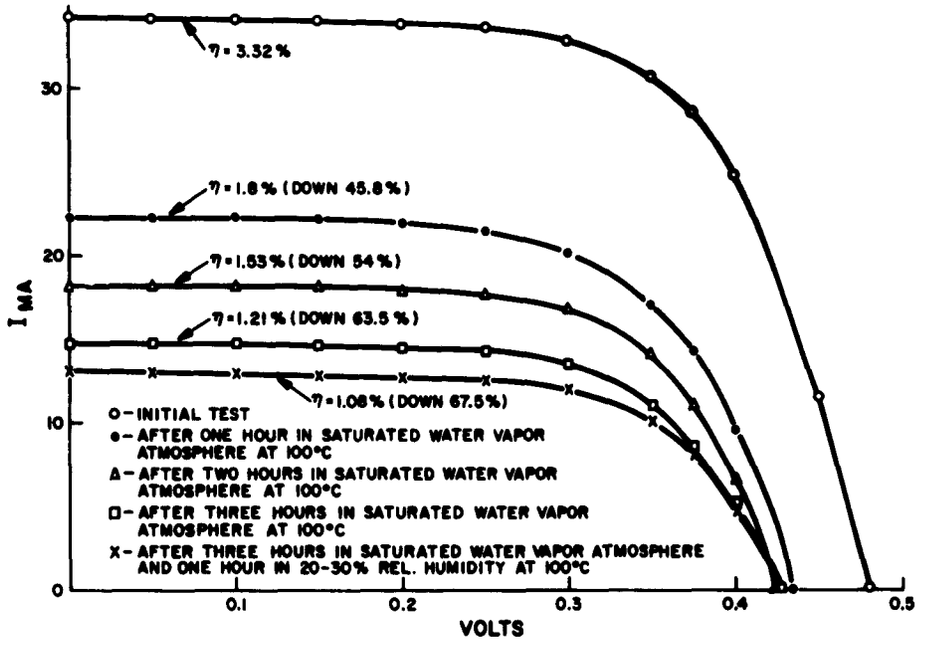

Figure 27. Humidity Test, Cell No. 131-4

cadmium electrodes, which gave very low initial electrical output, the efficiencies of the rest of the cells (17 of them) were monitored during a three-month storage period. Cells with evaporated silver and tin electrodes showed no decay as compared with control cells having regular silver paste as electrode. These results are shown in Table XIII.

The cells with evaporated silver or tin electrodes tend to have lower open-circuit voltage with consequent lower efficiency, than cells with regular silver paste electrodes. The low voltage is probably due to short circuits. To overcome this, a very thin layer of phthalocyanine was evaporated over the barrier layer before the deposition of the metal layer. This material was chosen because of its low resistivity (it is a semi-conductor in comparison with other organic compounds) and its low sublimation temperature. The effect of phthalocyanine on the photo-voltage is shown in Table XIV.

e. Effect of Nuclear Radiation. An experiment was conducted to investigate the effect of fast neutrons and gamma rays on materials and devices. Three CdS Cells and a microscope light source were placed in the "swimming pool" of the Industrial Reactor Laboratories near Princeton. Wire leads were soldered to one cell for monitoring during the irradiation; the I-V characteristics of the other two cells were measured before and after the test. Two separate tests were performed on the same cells. For the first test the radiation level was $2X10^4$ γ per hour per cm^2 (gamma between zero and five MeV) and the total flux was $1.7X10^{12}$ fast neutrons (above 0.4 ev) per cm^2 for the four-hour period. Thermal neutrons below 0.4 ev were shielded out with metallic cadmium. In the second test the radiation level was increased to 10^6 γ per hour per cm^2 and a flux of 10^9 fast neutrons per cm^2 per second. The results are shown in Figure 28 for cell No. 139-3 and in Figures 29 and 30 for the other two cells, Numbers 134-2 and 134-4. Maximum power points were used for the monitoring cell since the light source was not calibrated. The effect of the nuclear radiation on these cells is relatively slight; it is felt that the reduction in power output is probably due to the thermal effect, since equipment adjacent to the cells during the test generated a considerable amount of heat. The maximum power output of cells 134-2 and 134-4 actually exhibited an increase after the second irradiation, possibly due to an annealing effect.

It is of interest that cell No. 134-2, which showed a 25-percent decrease of power output, has a "regular" silver paste top electrode while cell No. 134-4, with only a 7-percent loss of power output, is furnished with a high-temperature silver-paste top electrode.

This preliminary radiation test indicates that polycrystalline CdS cells are probably more resistant to nuclear radiation than are single-crystal cells.

f. Electrical Contact to Cells. Cells usually exhibited lower efficiency with lead wires soldered directly to the electrodes than when measured on the test rack. This may be attributed to three factors: (1) the point contact of the lead wire as compared with the large-area contact on the test racks, (2) effect of heating on the barrier layer during soldering, and (3) discontinuity of the evaporated metal layer caused by soldering.

An improved soldering technique was developed for attaching lead wires. This technique consists of soldering the lead wires to a wire mesh which in turn is fastened to the metal layer electrodes by means of a silver paste or a conducting epoxy cement.

TABLE XIII. EFFECT OF ELECTRODE CONTACT ON THE DECAY OF CdS CELL EFFICIENCY

Cell No.	Electrode Contact	Initial Efficiency, %	Final efficiency, % after 3-months	Decay (% of initial eff.)
125-1	Regular Ag paste	2.70	1.10	59.2
125-2	Regular Ag paste	2.60	0.86	67.0
125-3	evap. Ag	1.72	1.72	0
125-4	evap. Ag	1.75	1.75	0
132-1	evap. Ag	0.54	0.60	0
132-3	evap. Ag	0.24	0.25	0
136-2	evap. Ag	1.23	1.23	0
136-4	Regular Ag paste	0.57	0.22	62.0
134-2	Regular Ag paste	2.17	1.39	36.0
134-4	Hi-temp Ag paste	1.73	1.73	0
139-2	Hi-temp Ag paste	1.32	1.32	0
143-1	Evap. Sn	0.97	1.00	0
143-3	Evap. Sn	1.66	1.66	0
145-1	Regular Ag paste	2.07	0.96	53.6
145-2	High-temp. Ag paste	1.85	1.85	0
145-4	Hi-temp. Ag paste	1.65	1.65	0
147-1	Evap. Ag	0.97	0.95	2
147-2	Evap. Ag	1.05	1.00	5
147-3	Hi-temp. Ag paste	1.65	1.63	1
147-4	Regular Ag paste	2.50	0.68	72
148-3	Hi-temp. Ag paste	1.75	1.70	3
148-4	Regular Ag paste	3.15	1.09	65.5
150-3	Evap. Sn	2.10	2.10	0
150-4	Evap. Sn	1.90	1.90	0

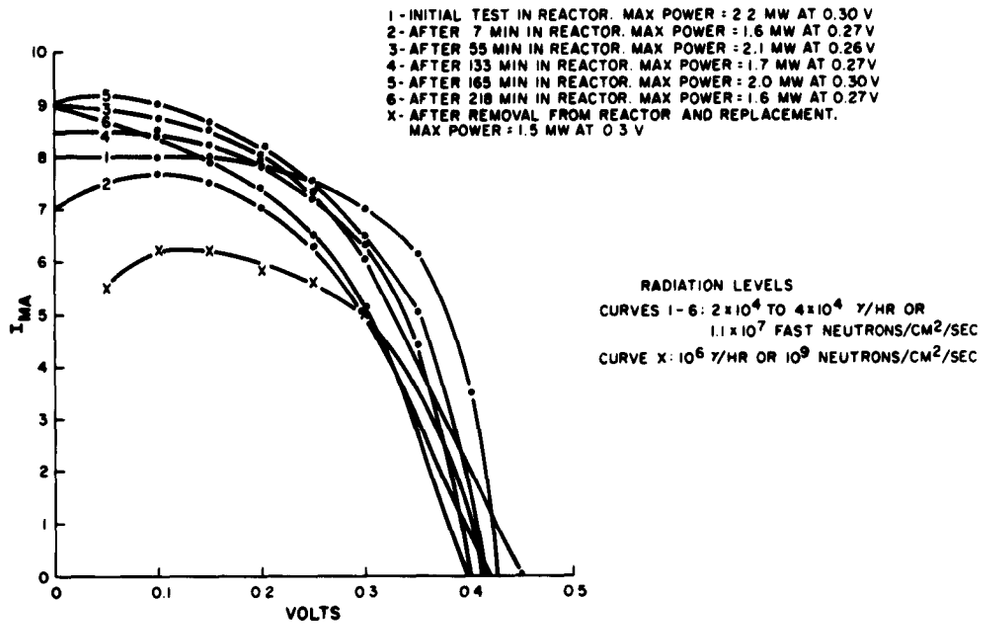

Figure 28. Nuclear Radiation Test, Cell No. 139-3

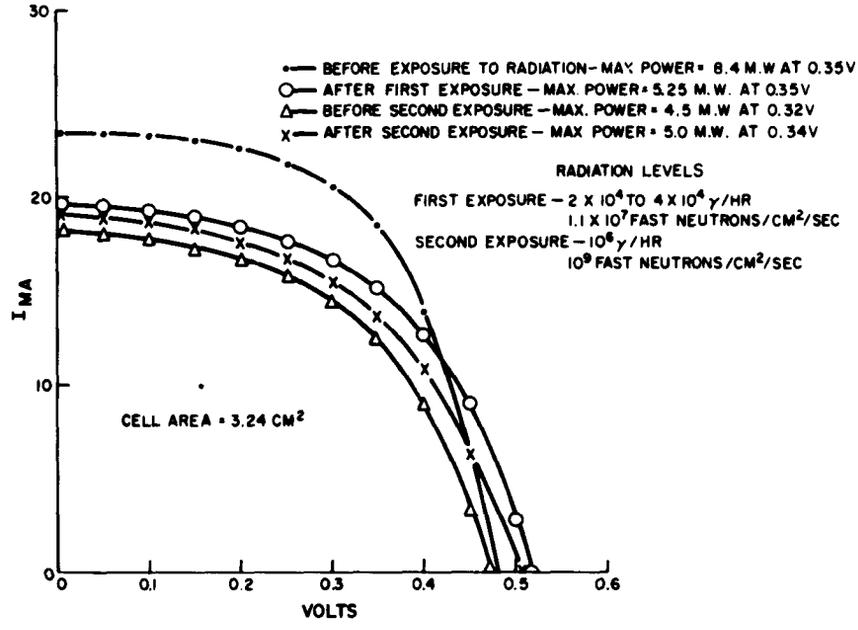

Figure 29. Nuclear Radiation Test, Cell No. 134-2

TABLE XIV. EFFECT OF PHTHALOCYANINE ON PHOTOVOLTAGE OF CdS CELLS

Cell No.	Phthalocyanine	Evaporated metal electrode	I_{sc} ma	V_{oc} volts	Pm mw	η efficiency, %
143-1	no	Sn	19	0.37	3.6	1.00
147-2	no	Ag	22	0.38	3.8	1.05
156-1	yes	Ag	23	0.47	4.2	1.54
156-3	yes	Ag	20	0.48	3.8	1.48
191 (4"x4")	no	Sn	275	0.26	22.5	0.26
190 (4"x4")	yes	Sn	300	0.42	45.0	0.63
204 (4"x4") two in series	no	Sn	114	0.64	25.2	0.34
208 (4"x4") two in series	yes	Sn	235	0.75	70.0	0.95

The use of this method enabled the cells with wire leads to operate at efficiencies comparable with those of the cells tested with the large-area contacts in the test rack. The efficiencies of cells with the wire-mesh contact and those with point contact only are listed in Table XV.

TABLE XV. EFFECT OF LARGE-AREA AND POINT CONTACTS CdS CELL EFFICIENCY

Cell No.	Efficiency, %	
	Large Area Contact with Wire Mesh	Point Contact without Wire Mesh
145-2	1.61	
145-4		0.74
150-3	2.10	
150-4		1.30
150-2		0.70
186 - 4"x4" (Section 1)	0.55	
168 - 4"x4" (Section 2)		0.42

The conductivity of the conductive epoxy cement is not as high as desired and its pot life (useful period after mixing of components) is rather short. If not used immediately after mixing the two components, the conductivity of the cement decreases.

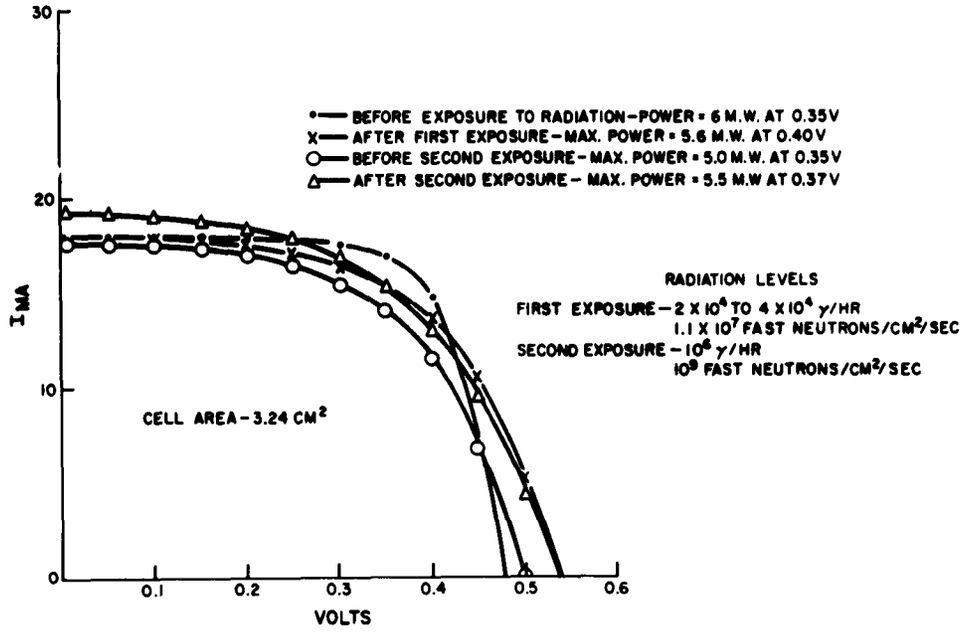

Figure 30. Nuclear Radiation Test, Cell No. 134-4

Inasmuch as the cement does provide better adherence than silver paste and is the best available for curing at room temperature, it was used for the cells that were delivered. An attempt is being made to find an epoxy cement with a higher conductivity and a longer pot life.

SUMMARY AND CONCLUSIONS RELATING TO CdS CELL FABRICATION

During this study, two square feet of CdS thin-film cells on four-inch-square substrates were delivered, as shown in Figure 31. In addition, the feasibility was established of using a flexible substrate with a potential power-to-weight ratio of from ten to twenty watts per pound. The conversion efficiency of large-area cells was increased by 100 percent - from 0.5 percent to 1.1 percent for four-inch-square cells. Cell storage deterioration was reduced to the extent that no decay occurred in a number of cells after a period of three months. Employment of integrated circuitry indicates a method for the further increase in the efficiency of all large-area cells.* Preliminary experiments demonstrated polycrystalline CdS cells to be quite resistant to gamma and neutron radiation. Additional development is necessary to explore the maximum efficiency, maximum power-to-weight ratio, and lowest cost.

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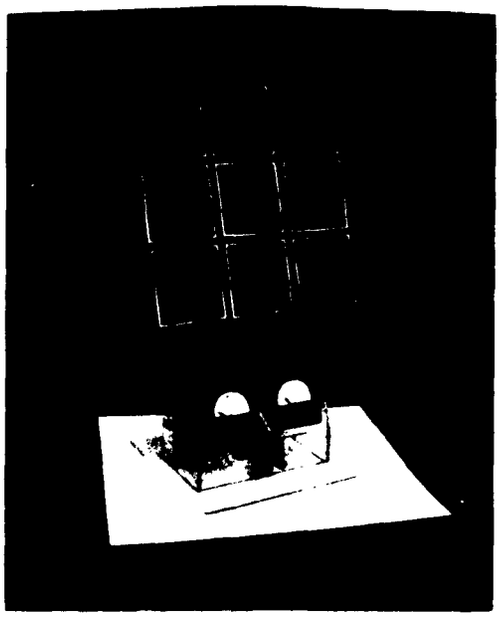
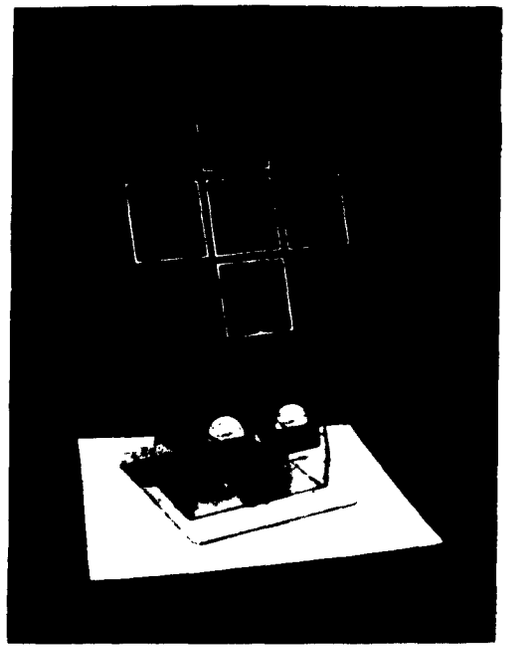
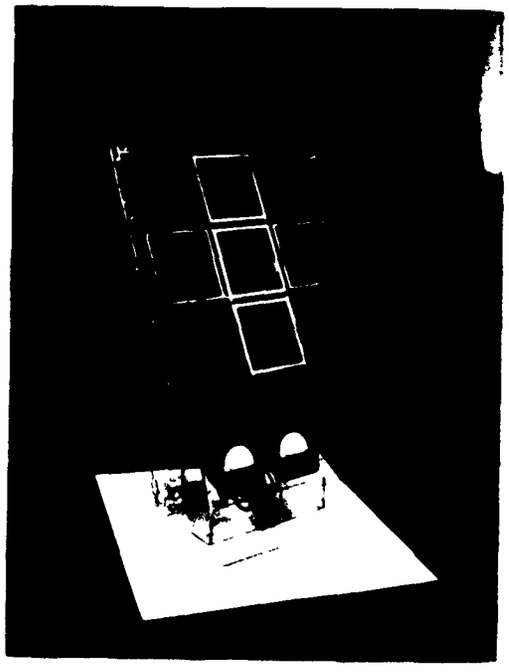
* During fabrication of small CdS cells for radiation testing being carried out under Contract AF33(657)8490, an efficiency as high as 5.7% for a cell area of 0.2 cm^2 was obtained on a 1/16 inch glass substrate.



a. Array No. 1, 1/16-inch Glass Substrate



b. Array No. 2, 0.015-inch Glass Glass Substrate



c. Array No. 3, Integrated Cells 1/16-inch Glass Substrates; Front- and Backwall-Cells on 0.002-inch Plastic Substrates

Figure 31. Solar Cell Arrays

TECHNICAL SUMMARY

Thin-film, large-area cadmium sulfide photovoltaic cells have been fabricated. Low sheet resistance was found to be extremely important to cell conversion efficiency in the course of the work and is at present the major obstacle to the achievement of high efficiency from single large-area cells. The use of integrated circuitry appears to be one fruitful method of overcoming the sheet resistance problem in achieving the high efficiency of small cells while retaining the low cost of large-area cells.

The utility of a thin, organic-plastic film as a substrate for large-area, thin-film CdS cells has been established, thus demonstrating the potential for very high power-to-weight ratios for CdS cells.

Limited experiments showed CdS polycrystalline cells to be more resistant to radiation in space than are silicon cells. CdS cells are ten times as resistant to 0.8 Mev electrons as n-on-p silicon cells and are 10^4 as resistant to 1.6 Mev protons. As tested in a swimming pool reactor, no significant effect on CdS cell efficiency by fast neutrons and gamma rays was observed. In addition, thermal tests showed that although the efficiency of CdS cells decreased by about 40 percent when heated from 0°C to 100°C in vacuum, the effect was reversible and the original efficiency was substantially restored when the temperature returned to the initial value.

Cells fabricated by the crystal-layer-conversion method have been delivered. Some success has been achieved and additional tests and investigations are required for further evaluation of the process.

In view of (1) the high conversion efficiency of relatively small cells (5.7% for cell of 0.2 cm^2 area), (2) the demonstration of the feasibility of making useful large-area cells, (3) the demonstration of cell fabrication on a thin plastic substrate, and (4) the practicability of integrated circuitry, it is recommended that future work dealing with large-area, thin-film, CdS photovoltaic cells be concerned with the attainment of optimum values for the various parameters listed in order to fully exploit the potential of such cells.

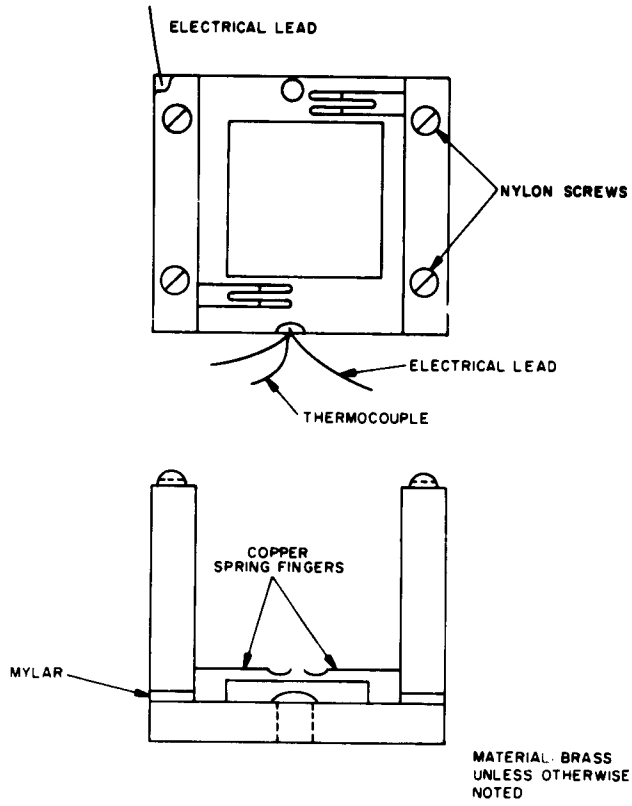


Figure A-1. Cell Holder

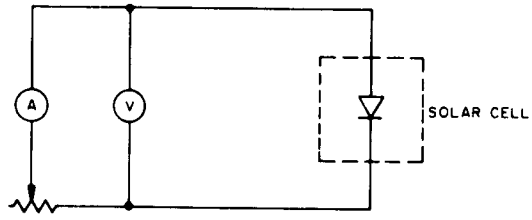


Figure A-2. Test Circuit

APPENDIX A

PERFORMANCE TESTS OF CADMIUM SULFIDE SOLAR CELLS

1. THERMAL

Samples of cadmium sulfide (CdS) solar cells, similar to those that were prepared for delivery, were thermally cycled in a vacuum of 10^{-3} to 10^{-5} Torr. Although the original specification required cycling between -30°C and +60°C, it was decided to extend the range upward to 100°C as a result of preliminary tests.

a. Test Apparatus. The test enclosure for the cells was an 18-inch bell jar. Heating and cooling were accomplished by bolting a brass cell-holder, as shown in Figure A-1, to a mantle containing two 450-watt, electrical strip heaters and three cooling coils. The mantle was so oriented in the bell jar that the cell was vertical. The cooling coils carried trichlorethane from an external refrigerator, and cooling was controlled by the refrigerator thermostat setting; the heaters were adjusted by means of an autotransformer. The sample temperature was assumed to be that of the cell-holder which was monitored by a copper-constantan thermocouple soldered to its base. The thermocouple voltage was measured by means of a Leeds and Northrup Type 8690 Potentiometer. The output of the spot lamp used to illuminate the sample cell was controlled by an autotransformer, which was in turn connected to a line-voltage regulator, thus insuring a uniform voltage on the lamp. The lamp was about nine inches from the cell.

A silicon cell (with a copper-constantan thermocouple soldered to the back) was also placed in the bell jar, about six inches in front of the sample cell and slightly below it. The silicon cell was sufficiently far from the mantle that temperature changes of the mantle did not significantly affect the cell. This silicon cell was used as a standard for the light source; before readings were taken for the CdS cell under test, the silicon cell output was observed and adjustments made, when necessary, to assure that the light level remained constant during the thermal-cycle test. The thermocouple on the silicon cell was required to assure that the temperature of the silicon cell remained constant during the thermal-cycle test.

The data for the current-voltage (I-V) curve of the sample was measured with the circuit shown in Figure A-2; a Weston precision milliameter was used for measuring the current and a RCA Senior VoltOhymst for voltage. In order to insure that no local heating occurred in the sample during the tests, it was necessary to shield the

cell from the light or to switch the light off when readings were not being taken. Individual points of the curve were taken at intervals of thirty seconds to allow heat accumulated by the cell to be dissipated into the holder.

b. Results. The tests were performed on two sample glass substrates 1 inch square and 1/16 inch thick. One sample (125-3) had an evaporated-silver bottom electrode and the other (143-3) had an evaporated-tin bottom electrode.

After three full cycles, there was no change in the appearance of the cells and no evidence of the CdS layer peeling from the substrate. I-V curves of both samples, taken before and after the thermal testing,* show no essential difference (as seen in Figures A-3 through A-6 and Tables A-I through A-IV). Discrepancies between short-circuit currents for a particular cell as recorded in Figures A-3 through A-6 are due to variations in the light of the light sources used for the tests. The spot light was used for the tests recorded in Figures A-3 and A-4, while for the tests of Figures A-5 and A-6, the light was from a broad-area source adjusted and calibrated to simulate 100 milliwatts per cm^2 for CdS cells.

In addition to the thermal environmental tests, cell efficiency was determined as a function of temperature. This is shown in Figure A-7 which represents the efficiency-temperature curves for a 3-percent CdS solar cell and a 10-percent silicon cell. The CdS cell (See Reference 1) is obviously much less temperature-dependent than the silicon cell.

Thermal tests were also performed on the cells after the wiring was applied. This wiring consists of a wire mesh attached to the center electrode and a solid wire to the edge of the cell. The addition of the wiring for this limited number of tests resulted in slight changes in cell performance - principally lowered V_{OC}. The cells were subjected to a temperature variation of -30°C to +100°C; there was no evidence of peeling of wires from the cells.

*Figures A-8 and A-9 show the I-V curves for the same cells with epoxy and wiring added, before and after cycling. Note that some decrease of the electrical output is evident; since this does not occur in the first set of curves (without the epoxy) this lower efficiency is attributed to the high resistance of the epoxy.

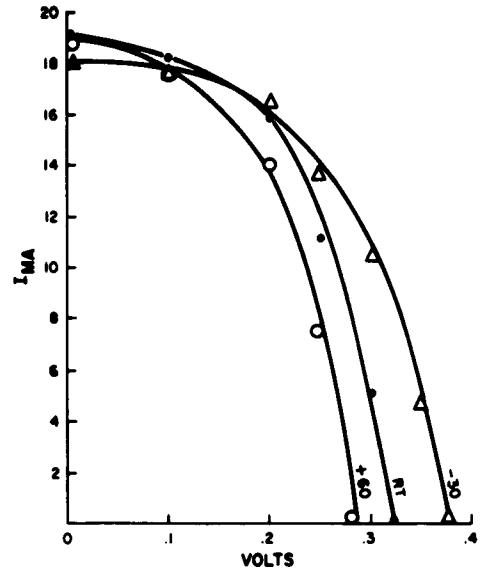


Figure A-3. Thermal-Cycling Test Using Spot Light Source (125-3)

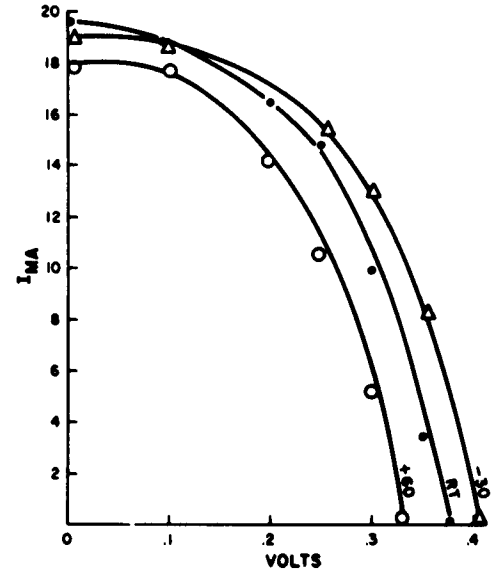


Figure A-4. Thermal-Cycling Test Using Spot Light Source (143-3)

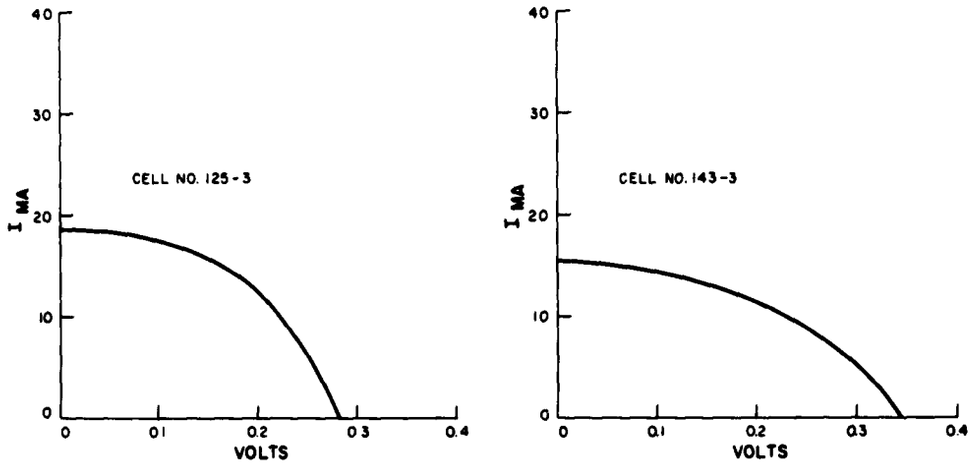


Figure A-5. I-V Curves, Before Thermal Cycling, Using Standard Calibrated Light Source

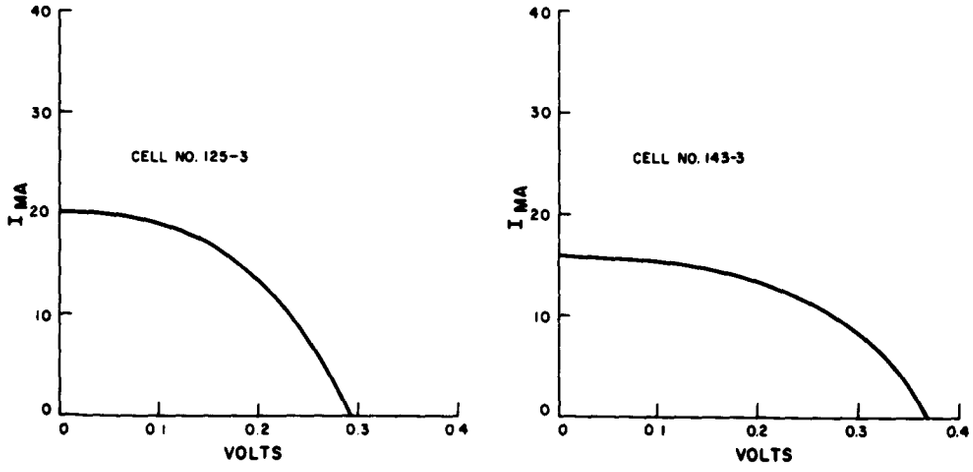


Figure A-6. I-V Curve, After Thermal Cycling, Using Standard Calibrated Light Source

TABLE A-I. THERMAL CYCLING TEST RESULTS, CELL 125-3, NO WIRING ATTACHED

T°C	I_{sc}	V_{oc}	V_o = .10	.20	.25	.30	.35
RT	19.5	.320	18.6	15.2	11.6	3.8	
30	19.9	.305	18.4	14.6	9.7	1.5	
40	19.3	.299	18.0	13.8	7.8	-	
50	19.4	.295	18.4	13.8	7.8	-	
60	19.4	.290	18.4	12.9	7.4	-	
70	19.5	.262	18.0	11.4	5.7	-	
80	19.3	.260	17.5	9.0	-	-	
90	19.6	.230	17.0	7.1	-	-	
100	19.7	.240	16.6	8.6	-	-	
80	19.6	.240	17.6	9.0	-	-	
70	19.6	.250	17.4	9.0	-	-	
60	19.2	.260	17.0	9.4	1.2	-	
50	19.2	.260	17.0	10.5	2.8	-	
40	18.8	.270	17.0	11.0	4.6	-	
30	18.8	.280	17.2	12.0	6.5	-	
20	18.2	.320	17.2	13.6	9.6	3.7	
10	17.5	.335	16.8	14.3	11.2	6.8	
0	17.5	.335	16.8	14.3	11.2	5.6	
-10	17.5	.335	17.0	14.3	10.6	5.6	
-20	17.4	.352	16.6	14.0	10.6	7.0	
-30	17.2	.360	15.8	14.4	11.6	7.3	
-20	17.1	.350	16.8	14.2	11.6	7.9	
-10	17.4	.350	16.8	14.6	11.6	6.9	
0	17.8	.340	16.9	14.0	10.6	5.6	
RT	19.0	.320	18.3	15.8	11.1	5.1	-
30	19.0	.320	18.3	15.6	11.9	4.4	-
40	18.9	.325	18.9	15.9	10.9	1.4	-
50	18.9	.305	18.0	14.6	9.8	-	-
60	18.9	.295	17.6	14.0	7.5	-	-
70	19.0	.283	17.5	13.4	6.6	-	-
80	19.1	.279	17.5	12.8	3.2	-	-
90	19.3	.259	17.6	11.0	-	-	-
100	19.9	.249	17.6	9.6	-	-	-
90	19.9	.249	17.5	9.0	-	-	-
80	19.6	.260	17.8	10.4	2.8	-	-
70	19.6	.261	18.4	12.0	3.9	-	-
60°	19.6	.270	18.4	12.0	4.9	-	-
50°	19.6	.270	18.4	12.3	5.3	-	-
40°	19.5	.283	18.4	13.0	6.6	-	-
30°	19.5	.290	18.4	13.1	7.1	-	-

TABLE A-I. THERMAL CYCLING TEST RESULTS, CELL 125-3, NO WIRING ATTACHED (Cont'd)

T°C	I_{sc}	V_{oc}	V_o = .10	.20	.25	.30	.35
20°	19.0	.300	18.0	14.6	9.6	-	-
10°	19.0	.320	18.0	14.5	9.6	3.8	-
0°	18.9	.330	17.9	14.8	11.2	4.0	-
-10°	18.6	.350	18.0	15.4	12.2	6.0	-
-20°	18.3	.350	17.6	15.4	12.7	.5	2.0
-30°	17.9	.380	16.6	15.4	13.6	10.6	4.1
RT	19.0	.321	17.9	14.8	9.6	4.1	
30	18.7	.318	17.9	14.0	9.8	3.6	
40	18.4	.305	17.5	13.0	8.9	1.2	
50	18.4	.299	17.0	12.3	7.6	-	
60	17.6	.284	16.3	11.4	6.0	-	
70	17.5	.280	15.9	10.4	5.4	-	
80	17.5	.270	15.9	10.6	4.1	-	
90	17.3	.250	15.9	9.2	-	-	
100	17.9	.240	15.0	7.5	-	-	
90	18.0	.240	15.9	7.4	-	-	
80	18.3	.250	15.5	8.0	-	-	
70	18.5	.260	16.1	9.0	-	-	
60	18.5	.270	16.1	9.4	3.5	-	
50	18.4	.272	16.4	10.1	4.0	-	
40	18.6	.280	16.1	10.6	5.0	-	
30	18.4	.305	17.0	11.4	6.4	-	
20	18.0	.310	16.8	11.4	7.3	1	
10	18.0	.316	16.6	12.0	8.1	2.4	
0	17.6	.320	16.6	12.5	8.5	3.5	
-10	17.6	.322	16.8	14.0	9.2	3.5	
-20	17.2	.340	16.8	14.0	10.0	5.2	
-30	17.0	.340	15.8	14.0	10.0	5.0	
-20	17.0	.338	16.2	14.0	9.6	4.8	
-10	17.0	.336	16.3	13.8	9.4	4.7	
0	17.3	.336	16.4	13.8	9.0	4.2	
10	17.6	.320	16.4	13.6	8.9	3.0	
20	17.8	.310	16.4	12.0	8.1	2.5	

TABLE A-II. THERMAL CYCLING TEST RESULTS, CELL 143-3, NO WIRING ATTACHED

T°C	I_{sc}	V_{oc}	.10	.20	.25	.30	.35
RT	20.0	.368	19.0	15.9	13.3	9.6	2.4
30	19.8	.362	18.9	15.7	13.5	8.9	1.8
40	19.6	.358	18.4	15.8	13.5	8.8	-
50	19.4	.350	18.3	15.6	12.7	8.2	-
60	19.2	.340	18.0	14.8	11.8	7.4	-
70	19.0	.330	17.4	13.6	11.0	5.6	-
80	18.7	.320	16.9	13.4	9.8	3.4	-
90	18.8	.310	16.8	12.4	8.7	2.1	-
100	18.4	.305	16.6	11.4	7.2	-	-
90	18.5	.305	16.5	11.5	7.6	-	-
80	18.7	.310	11.0	13.3	8.9	-	-
70	18.8	.320	17.5	13.6	9.6	-	-
60	19.0	.330	17.7	14.3	10.3	4.2	-
50	19.2	.332	18.0	14.5	10.6	5.4	-
40	19.3	.338	18.0	14.9	11.0	5.5	-
30	19.4	.341	18.2	14.9	11.6	6.2	-
20	19.4	.362	18.6	15.9	13.6	9.6	3.8
10	19.4	.362	18.6	15.8	13.6	9.6	3.8
0	19.5	.381	18.6	16.2	14.4	12.0	5.5
-10	19.5	.381	18.6	16.5	14.6	11.5	5.6
-20	19.5	.392	18.7	16.6	14.9	12.0	6.4
-30	19.3	.405	18.6	16.8	15.1	12.6	8.6
-20	19.5	.405	18.8	16.6	15.2	13.0	8.6
-10	19.5	.40	18.6	16.6	14.9	12.4	7.4
0	19.4	.395	18.5	16.5	14.8	12.0	7.2
10	19.5	.391	18.5	16.5	14.5	11.8	6.5
20	19.4	.380	18.6	16.3	14.0	10.6	5.3
30	19.3	.370	18.3	15.8	13.8	10.1	4.2
40	19.3	.360	18.2	15.4	-	8.2	2.5
50	19.2	.354	18.1	15.3	12.8	8.5	-
60	19.1	.346	17.9	14.9	12.0	6.8	-
70	19.0	.338	17.8	14.4	10.9	5.4	-
80	18.9	.320	17.8	14.0	10.1	4.6	-
90	18.7	.310	17.4	13.5	8.9	1.8	-
100	18.5	.305	17.2	12.8	8.2	1.5	-
90	18.6	.310	17.2	13.2	8.6	1.7	-
80	18.9	.320	17.6	13.9	9.8	4.6	-
70	19.1	.328	17.9	14.6	10.8	4.2	-
60	19.2	.335	18.0	14.6	11.0	5.3	-
50	19.4	.340	18.3	15.3	12.0	5.8	-
40	19.5	.350	18.4	15.4	12.7	7.5	-
30	19.4	.360	18.5	15.6	12.8	7.8	-
20	19.5	.361	18.6	16.2	13.6	8.3	2.3

TABLE A-II. THERMAL CYCLING TEST RESULTS, CELL 143-3, NO WIRING ATTACHED (Cont'd)

T°C	I_{sc}	V_{oc}	.10	.20	.25	.30	.35
10	19.5	.370	18.8	16.5	10.8	9.6	5.2
0	19.5	.380	18.8	16.6	14.7	11.0	4.6
-10	19.6	.380	18.7	16.8	14.8	11.5	5.2
-20	19.6	0.4	18.8	17.2	15.5	12.5	7.6
-30	19.7	.410	19.0	17.4	15.6	13.3	8.2
-20	19.5	.400	18.8	17.4	15.6	13.2	8.6
-10	19.5	.400	18.8	17.3	15.6	13.2	8.6
0	19.5	.395	18.6	17.1	15.4	12.8	7.5
10	19.4	.380	18.6	17.0	15.2	11.5	7.2
20	19.5	.378	18.6	16.8	14.8	11.2	5.6
RT	19.5	.380	18.6	16.3	14.8	9.9	3.4
30	19.4	.359	18.4	16.0	13.4	9.4	2.0
40	19.3	.350	18.0	15.6	13.0	8.6	-
50	19.2	.345	18.0	15.2	12.4	7.0	-
60	19.0	.330	17.6	14.3	10.6	5.2	-
70	18.8	.315	17.3	13.6	9.4	2.8	-
80	18.6	.305	17.2	13.0	8.2	1.6	-
90	18.4	.300	16.6	12.4	7.4	-	-
100	17.8	.270	16.3	11.9	5.6	-	-
90	17.8	.298	16.4	11.9	7.9	-	-
80	18.4	.305	16.9	12.6	7.9	-	-
70	18.6	.310	17.4	13.6	8.8	-	-
60	18.8	.315	17.6	14.0	9.8	2.7	-
50	19.0	.325	17.9	14.7	10.7	4.6	-
40	19.1	.340	18.1	15.6	12.4	7.6	-
30	19.2	.359	18.4	16.1	13.6	9.2	-
20	19.3	.361	18.3	16.2	13.6	9.4	2.7
10	19.2	.378	18.4	16.4	14.4	10.5	4.5
0	19.1	.390	18.5	16.7	14.9	11.9	6.6
-10	19.0	.399	18.5	17.0	15.2	12.5	7.6
-20	18.9	.400	18.5	17.1	15.3	13.0	8.2
-30	18.7	.400	18.6	17.1	15.4	13.1	8.2
-20	19.0	.400	18.4	17.0	15.6	13.4	7.6
-10	19.1	.400	18.4	16.6	14.9	12.3	7.5
0	19.1	.390	18.3	16.6	15.0	11.7	6.6
10	19.1	.380	18.3	16.5	14.4	11.1	5.1
20	19.1	.375	18.2	16.1	13.9	10.4	4.4

TABLE A-III. THERMAL CYCLING TEST RESULTS, CELL 125-3, WITH WIRING

T°C	I_{sc}	V_{oc}	.10	.20	.25	.30
RT	19.0	.31	18.1	14.4	8.9	2.1
30	19.1	.29	18.1	13.6	7.2	-
40	19.3	.28	18.1	12.4	7.9	-
50	19.3	.26	17.8	12.0	5.2	-
60	19.3	.27	17.1	11.4	4.5	-
70	19.3	.26	17.1	10.8	2.2	-
80	19.3	.24	17.0	8.7	-	-
90	20.0	.22	16.2	5.0	-	-
100	19.8	.18	13.8	-	-	-
RT	19.1	.30	18.5	14.6	9.0	
10	19	.30	18.3	14.6	9.3	
0	19.1	.31	18.5	14.5	10.2	
-10	18.6	.32	18.3	14.5	10.2	
-20	18.5	.34	18.0	14.5	10.3	
-30	18.5	.36	18.3	14.5	10.1	
RT	19	.259	16.8	9.5	1.7	
30	19	.259	16.8	8.6	-	
40	19.2	.251	16.6	7.6	-	
50	19.4	.250	16.6	7.3	-	
60	19.4	.245	15.9	7.3	-	
70	19.3	.240	15.9	6.5	-	
80	19.4	.238	15.9	5.6	-	
90	19.3	.220	15.6	5.4	-	
100	19.1	.218	15.1	3.4	-	
20	20	.240	16.9	6.0	-	
10	19.4	.245	16.9	8.0	-	
0	18.8	.259	16.6	9.9	1.5	
-10	18.5	.260	16.8	10.1	3.5	
-20	18.5	.265	17.0	10.6	3.7	
-30	18.2	.275	16.5	10.6	4.0	

TABLE A-IV. THERMAL CYCLING TEST RESULTS, CELL 143-3; WITH WIRING

T°C	I_{sc}	V_{oc}	.10	.20	.25	.30	.35
RT	14.0	.370	13.4	11.5	9.5	6.4	1.7
30	14.3	.352	13.6	11.5	9.4	6.0	-
40	14.2	.350	13.5	11.4	9.2	5.8	-
50	14.1	.338	13.4	11.0	8.8	4.5	-
60	14.1	.328	13.3	11.4	7.6	3.1	-
70	14.3	.318	13.1	10.2	7.0	2.6	-
80	14.0	.310	13.0	9.7	6.3	1.7	-
90	14.0	.300	12.8	9.6	6.0	-	-
100	13.8	.295	12.5	8.8	5.1	-	-
0	14.4	.350	13.5	11.3	8.6	5.6	-
10	14.3	.355	13.4	11.4	9.4	1.0	
0	14.1	.365	13.5	11.5	9.5	1.7	
-10	14.0	.380	13.5	12.0	10.4	3.6	
-20	14.0	.389	13.7	12.0	10.6	4.3	
-30	14.0	.400	13.6	12.3	10.9	5.0	
RT	14.0	.360	13.6	11.6	9.3	6.0	
30	14.2	.360	13.6	11.5	9.4	6.1	
40	14.1	.348	13.5	10.9	8.7	5.0	
50	14.1	.340	13.4	10.9	8.4	4.8	
60	14.0	.330	13.4	10.6	7.8	3.2	
70	14.0	.320	13.0	10.1	7.2	2.6	-
80	14.0	.300	12.8	9.4	5.6	-	-
90	13.9	.299	12.5	9.1	5.4	-	-
100	13.6	.280	12.1	8.1	4.2	-	-
20	14.2	.350	13.5	11.3	8.9	5.4	-
10	14.1	.360	13.5	11.6	9.5	6.2	-
0	14.3	.365	13.8	11.8	9.6	7.2	2.1
-10	14.2	.370	13.5	11.9	10.0	7.2	3.0
-20	14.1	.378	13.6	11.9	10.1	7.6	3.4
-30	14.1	.380	13.7	12.0	10.2	8.0	4.0

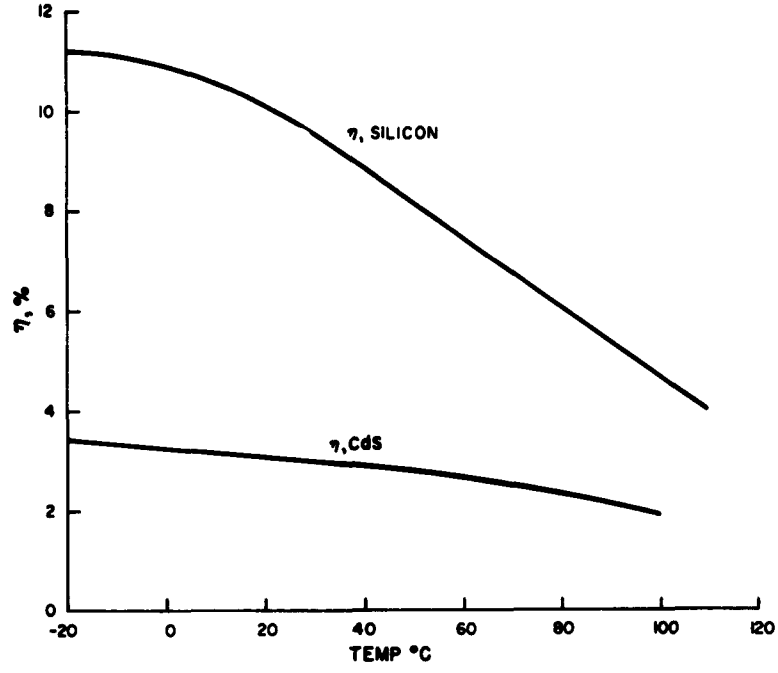


Figure A-7. Efficiency vs. Temperature; CdS and Si Cells

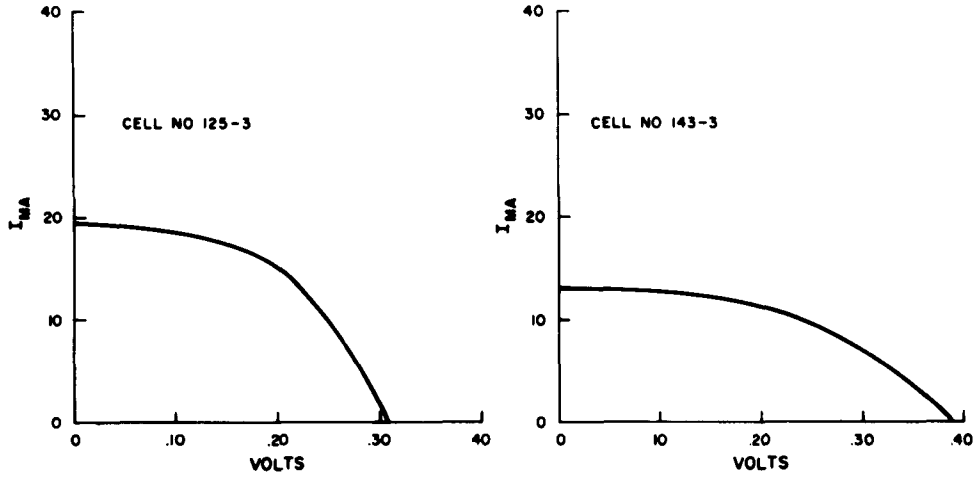


Figure A-8. I-V Curves, Before Thermal Cycling, Using Standard Calibrated Light Source; with Epoxy and Wiring

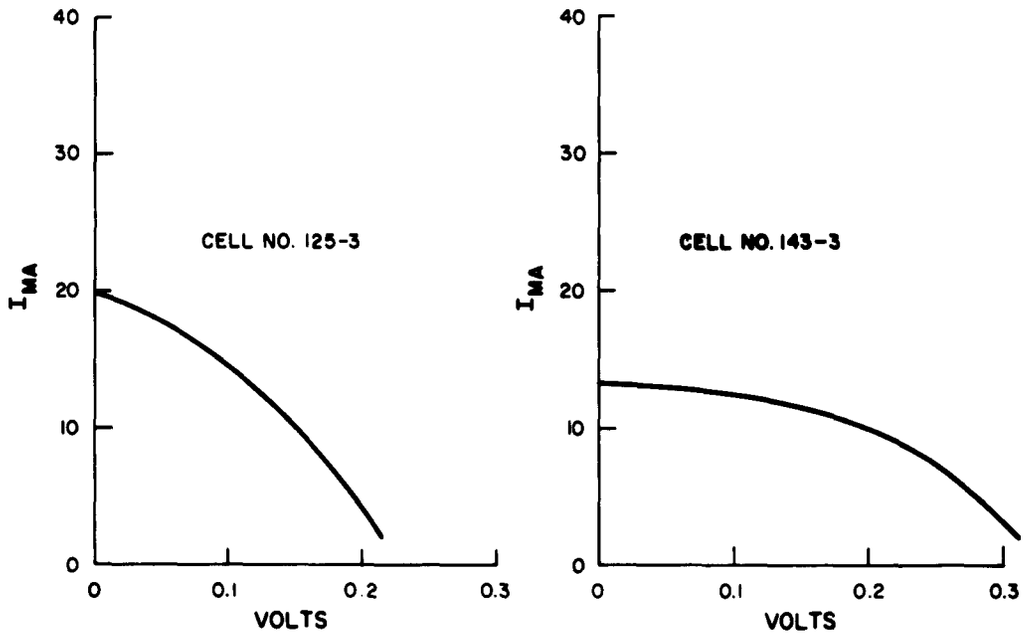


Figure A-9. I-V Curves, After Thermal Cycling, Using Standard Calibrated Light Source; with Epoxy and Wiring

2. ELECTRICAL

Groups of cells of similar types were tested for current-voltage (I-V) characteristics under short-circuit, open-circuit, and various load conditions. Results were tabulated and are illustrated in the various curves. In two cases, the cells were arranged into an array and tested for the same characteristics. The illumination was the standard 100 milliwatts per cm^2 (from tungsten lamps with a filter except for the arrays, where sunlight was used because of the large area).

a. Polycrystalline Cells. Three groups of cells (as seen in Figure 31 of Section III of this report) were tested with the results summarized in Table A-V. In the first two groups, on 1/16-inch glass and 15-mil glass respectively, arrays were formed from the cells and tested. The third group consisted of a miscellaneous assortment of types and no array was tested. Figures A-10 through A-30 illustrated the I-V curves of the individual cells and arrays.

b. Recrystallized Cells. These cells were tested in the same manner as the polycrystalline cells and the results shown in Table A-VI. Figures A-31 through A-35 are the I-V curves for these cells.

TABLE A-V. ELECTRICAL CHARACTERISTICS OF CdS CELLS AND ARRAYS

Cell No.	I_{sc}	V_{oc}	P_m	Eff., %	Power Density, Watts/Lb. With Mesh	Power Density, Watts/Lb. Without Mesh	
Array No. 1							All 4x4 inch cells on 1/16 inch glass.
172	253 ma	0.42v	54 mw	0.68	0.68	0.74	
173	280	0.45	50	0.60	0.60	0.66	
184	445	0.43	66	0.75	0.75	0.82	
195	285	0.37	38	0.50	0.50	0.55	
200	275	0.35	34	0.46	0.46	0.50	
216	345	0.38	46	0.60	0.60	0.66	
219	305	0.32	38	0.48	0.48	0.52	
220	340	0.39	42	0.48	0.48	0.52	
221	350	0.41	52	0.64	0.60	0.70	
Array	310	3.0	298	0.4			All cells in series regardless of electrical match.
Array No. 2							All 4x4 inch cells on 15 mil glass. Four cells composed of two 2x4 components.
204	114	0.64	25	0.34	0.9	1.1	In series
207	152	0.75	35	0.48	1.3	1.5	In series
208	235	0.75	70	0.95	2.5	3.0	In series
209	450	0.43	73	1.03	2.7	3.3	In parallel
226	485	0.42	82	0.92	2.4	3.0	
Array	500	1.7	285	0.75			Cells 204, 207 and 208 in parallel; Cells 226, 209 and above combination in series.
Array No. 3							Assorted cells.
194	103	1.55	52	0.75	0.72	0.82	Four 2x2 inch components in series
229	340	0.48	60	0.9	0.87	0.98	Four 2x2 inch components in parallel.
230 (Backwall Plastic)	130	0.36	12	0.2	2.1	6.4	
227 (Backwall Plastic)	133	0.35	14	0.23	2.3	7.0	
223 (Front-wall Plastic)	83	0.30	7.6	0.15	1.5	4.5	

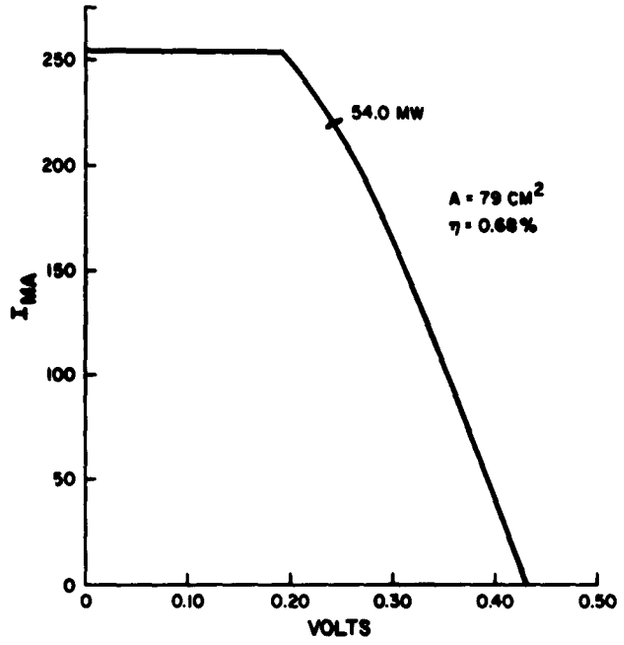


Figure A-10. I-V Curve, Cell No. 172 (Array No. 1)

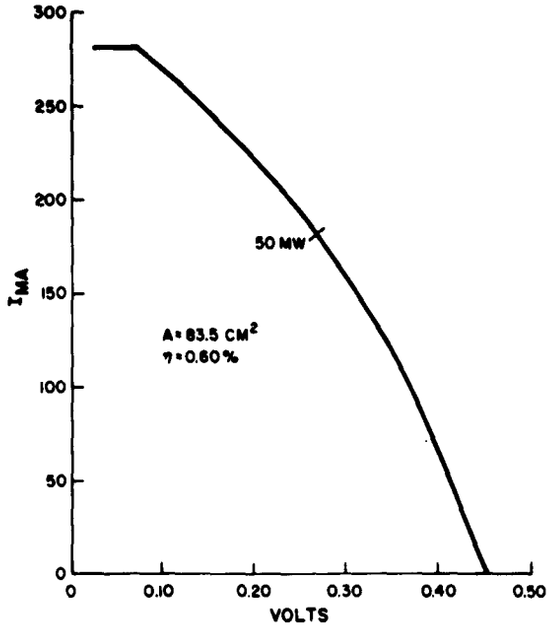


Figure A-11. I-V Curve, Cell No. 173 (Array No. 1)

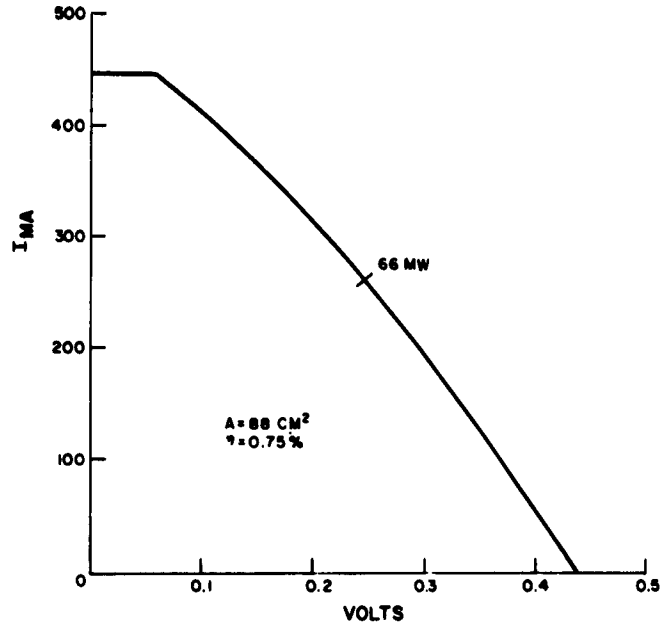


Figure A-12. I-V Curve, Cell No. 184 (Array No. 1)

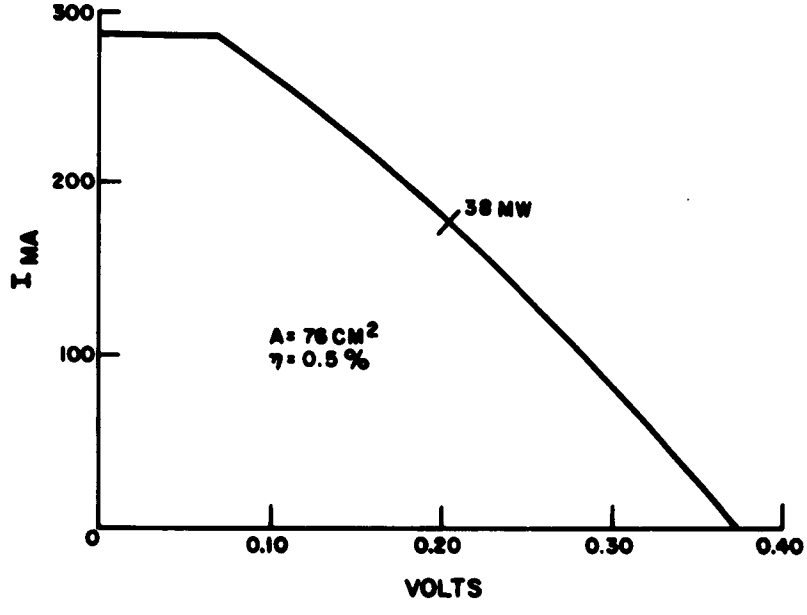


Figure A-13. I-V Curve, Cell No. 195 (Array No. 1)

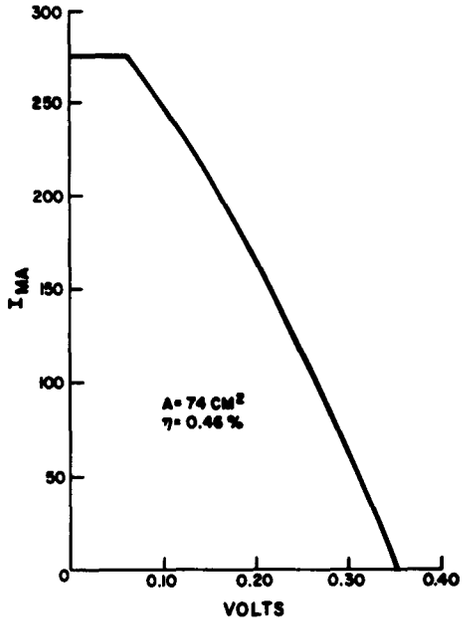


Figure A-14. I-V Curve, Cell No. 200 (Array No. 1)

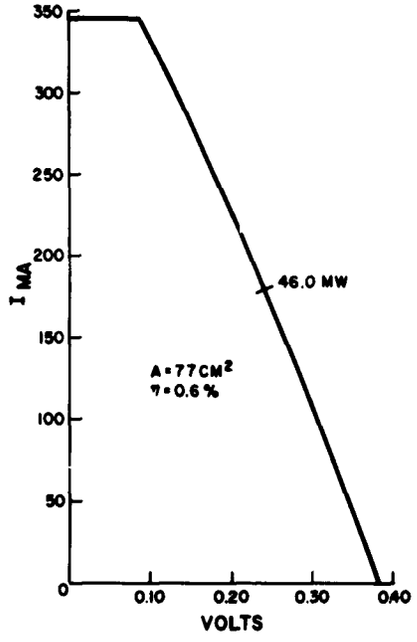


Figure A-15. I-V Curve, Cell No. 216 (Array No. 1)

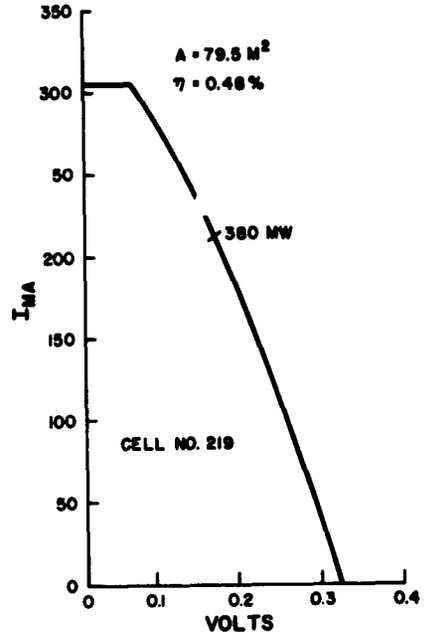


Figure A-16. I-V Curve, Cell No. 219 (Array No. 1)

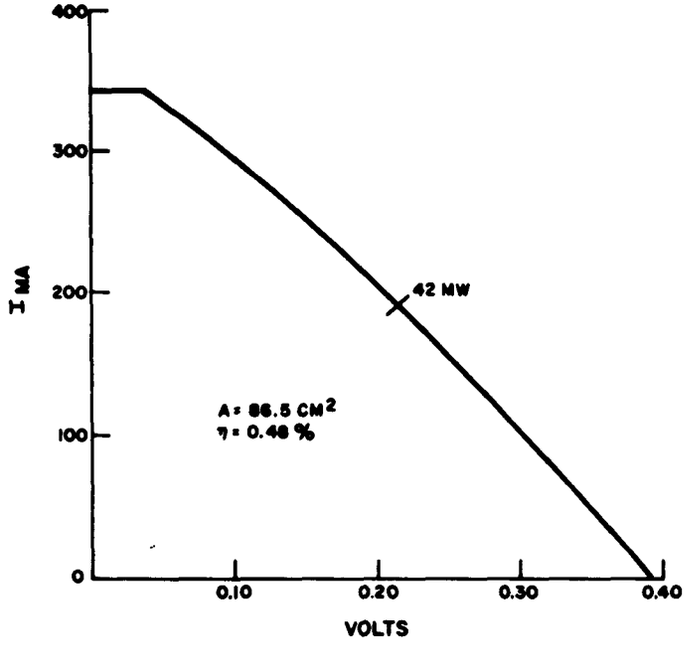


Figure A-17. I-V Curve, Cell No. 220 (Array No. 1)

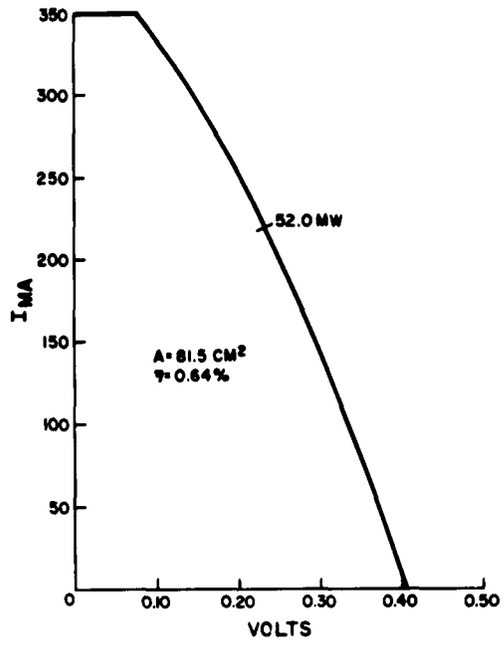


Figure A-18. I-V Curve, Cell No. 221 (Array No. 1)

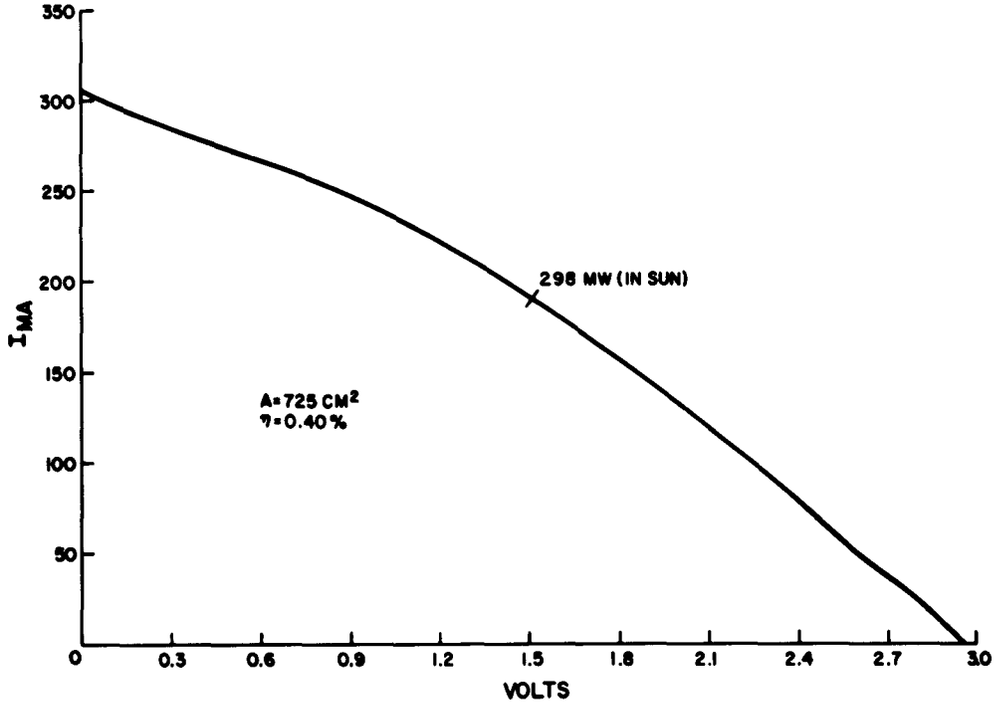


Figure A-19. I-V Curve, Solar Cell Array No. 1 (9-Cell Array in Series, in Sunlight)

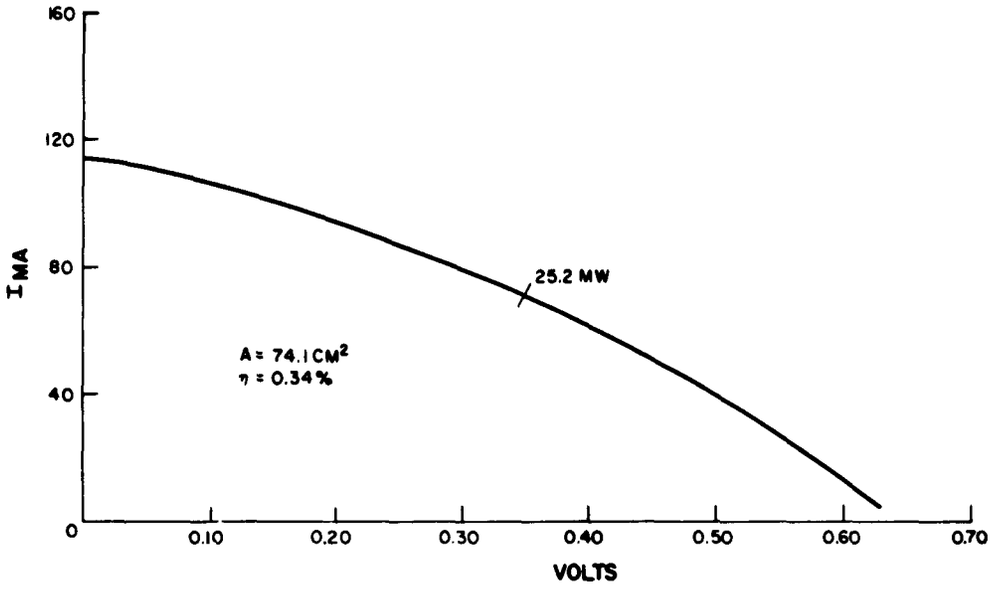


Figure A-20. I-V Curve, Cell No. 204 (2 in Series, Array No. 2)

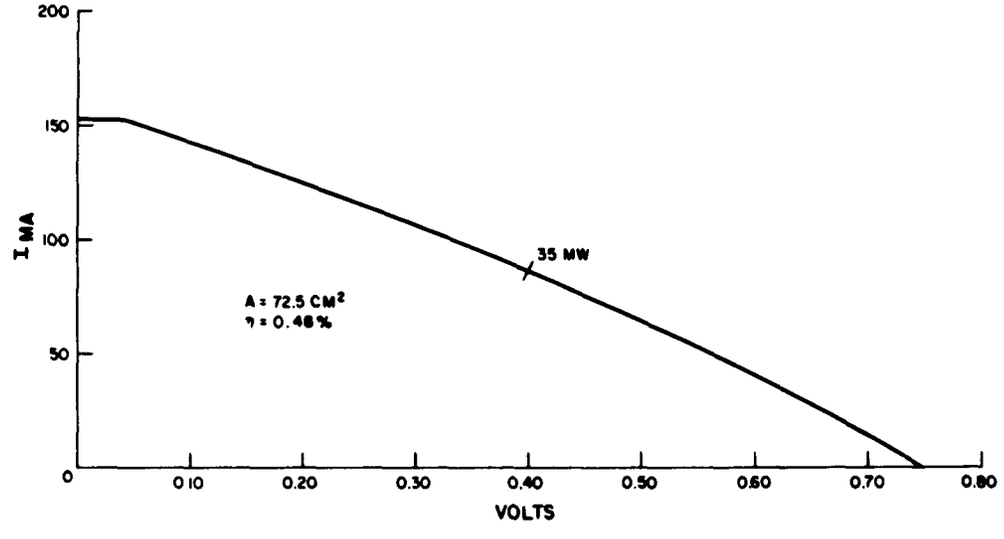


Figure A-21. I-V Curve, Cell No. 207 (2 in Series, Array No. 2)

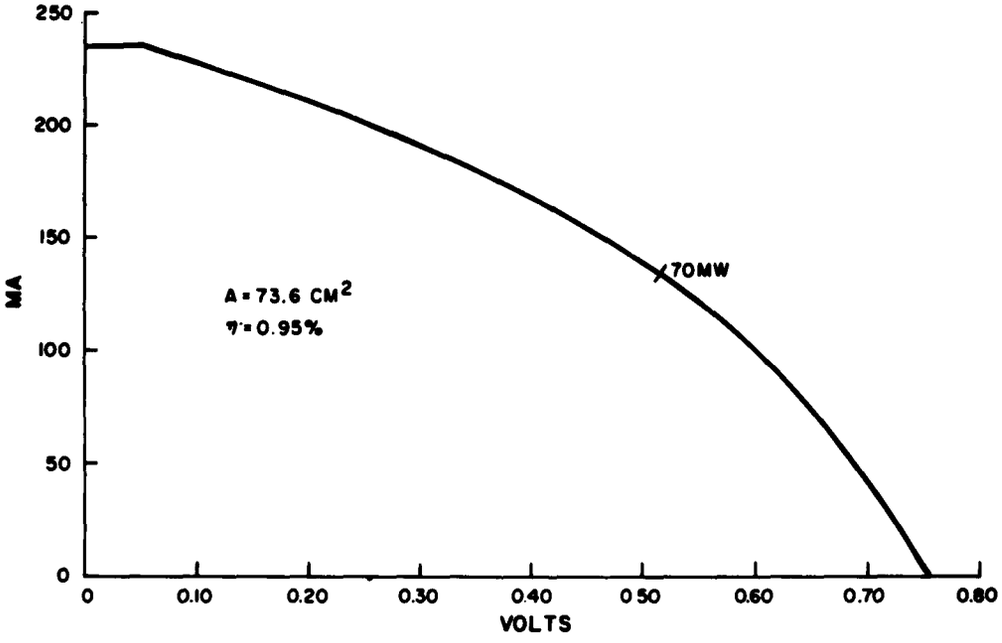


Figure A-22. I-V Curve, Cell No. 208 (2 in Series, Array No. 2)

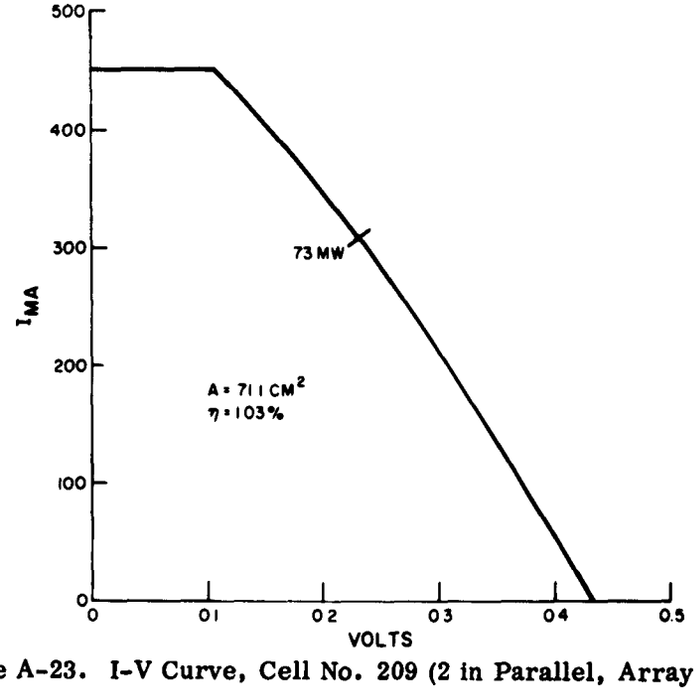


Figure A-23. I-V Curve, Cell No. 209 (2 in Parallel, Array No. 2)

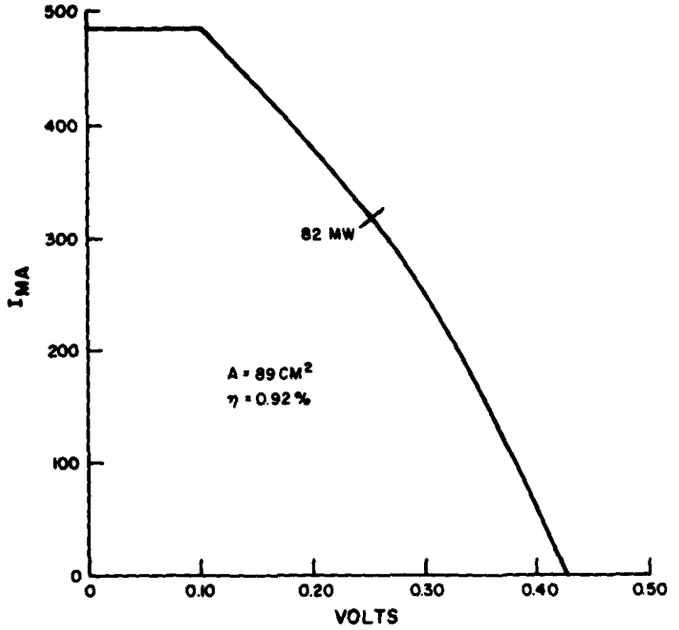


Figure A-24. I-V Curve, Cell No. 226 (Array No. 2)

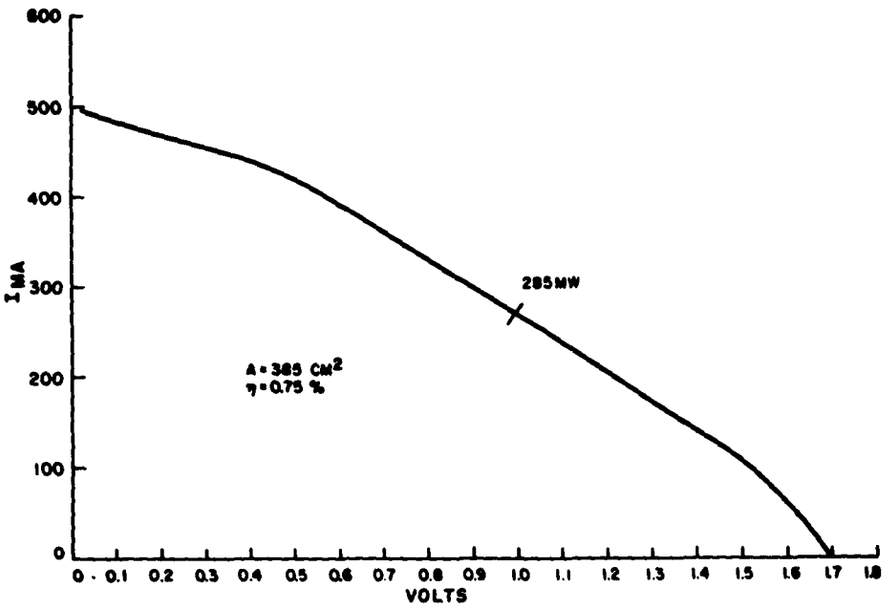


Figure A-25. I-V Curve, Solar Cell Array No. 2 (5-Cell Array in Series - Parallel)

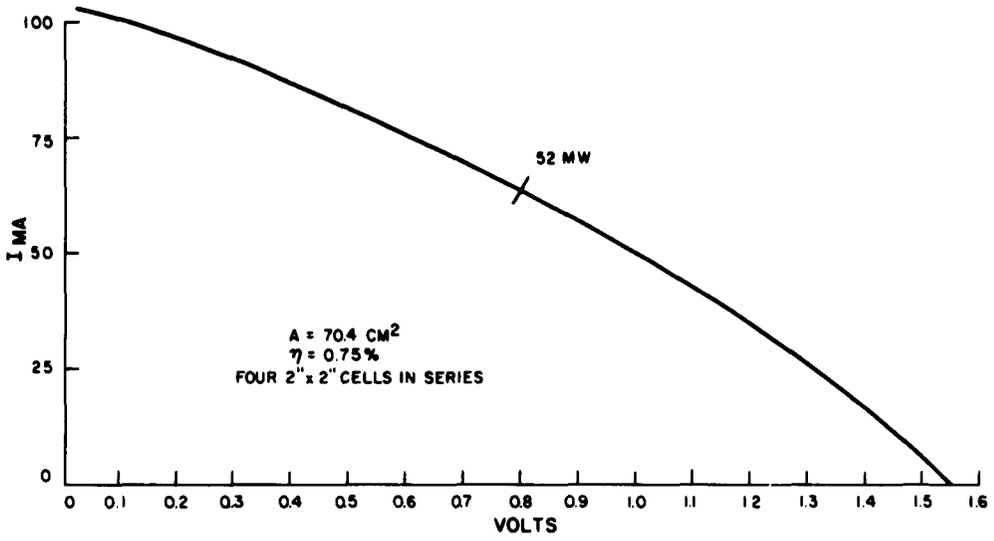


Figure A-26. I-V Curve, Cell No. 194 (Array No. 3)

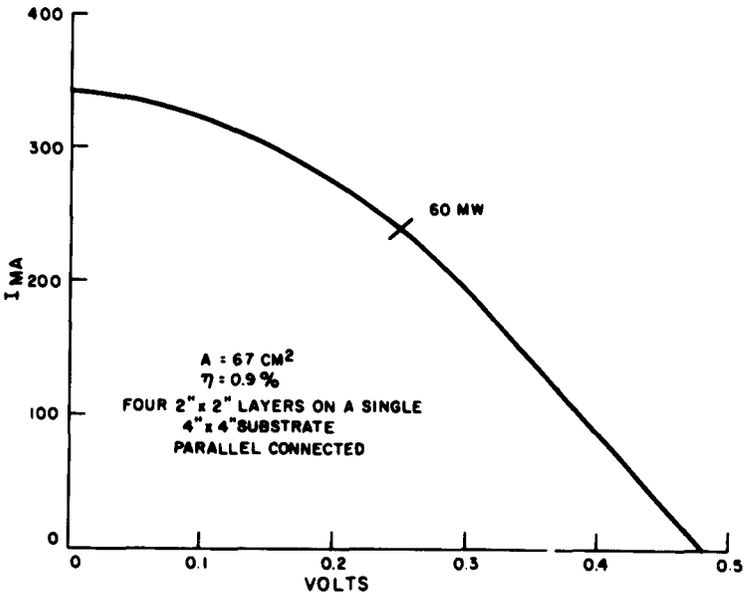


Figure A-27. I-V Curve, Cell No. 229 (Array No. 3)

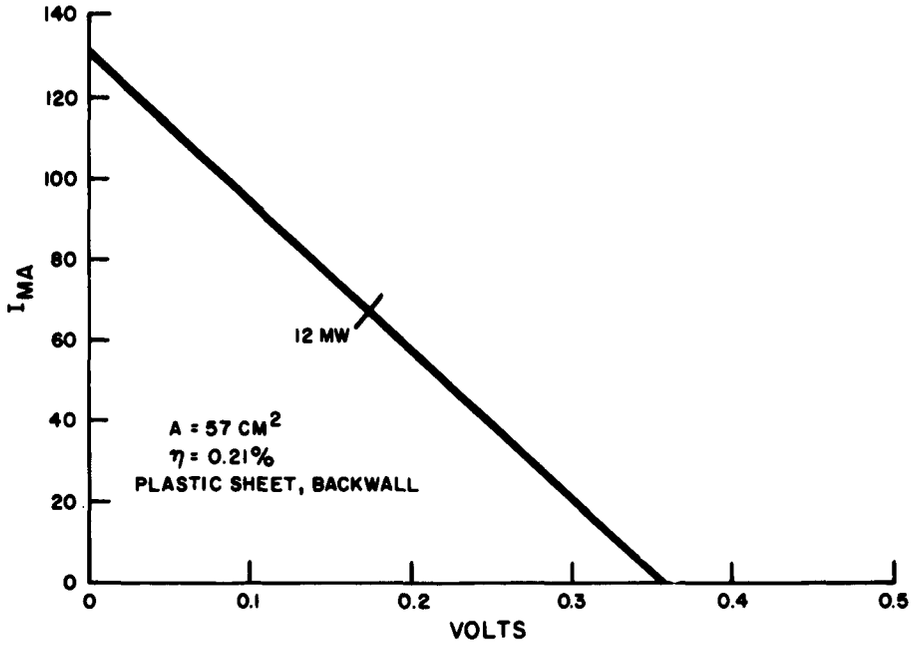


Figure A-28. I-V Curve, Cell No. 230 (Array No. 3)

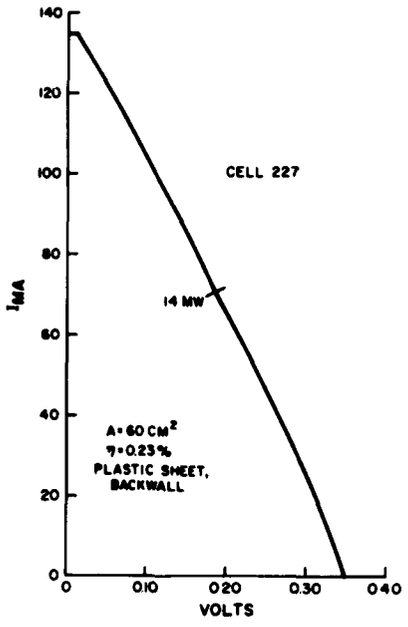


Figure A-29. I-V Curve, Cell No. 227 (Array No. 3)

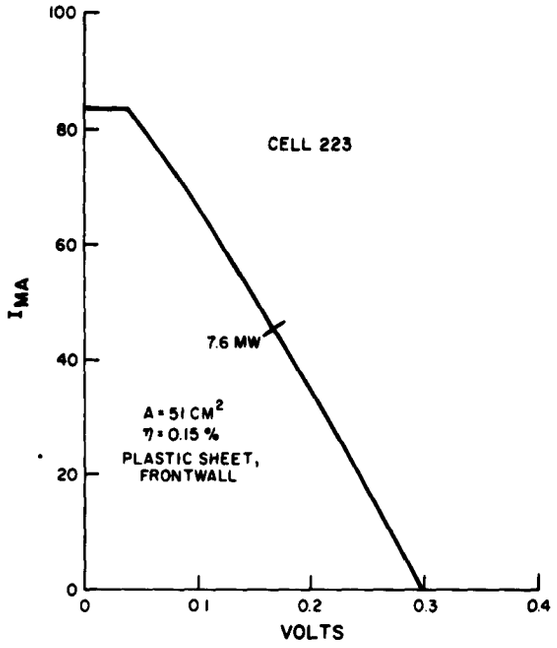


Figure A-30. I-V Curve, Cell No. 223 (Array No. 3)

TABLE A-VI. RECRYSTALLIZED CdS SOLAR CELLS
SUMMARY OF ELECTRICAL DATA

(measurements made on June 11, 12, and 13, 1962)

Cell	Area (cm^2)	Open Circuit Voltage (Volts)	Short Circuit Current (ma)	Efficiency %
RE - 1	1.71	0.17	6.4	0.17
RE - 2	0.49	0.16	3.0	0.28
RE - 3	0.39	0.27	2.7	0.63
RE - 4	0.30	0.27	2.0	0.71
RE - 5	0.19	0.28	1.1	0.60

Light source: Tungsten Lamps with a water filter, calibrated to 100 mw/cm^2 in terms of a "standard" micro-crystalline CdS solar cell.

REFERENCES

1. Escoffery and Luft, Optical Characteristics of Silicon Solar Cells and of Coating for Temperature; Solar Energy, p.1, Vol. 4, No. 4.

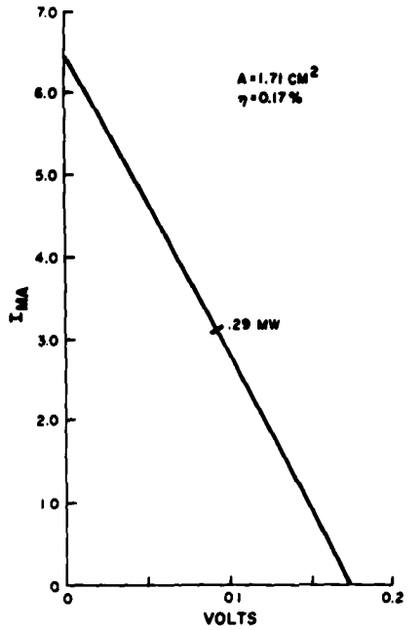


Figure A-31. I-V Curve, Recrystallized Cell No. RE-1

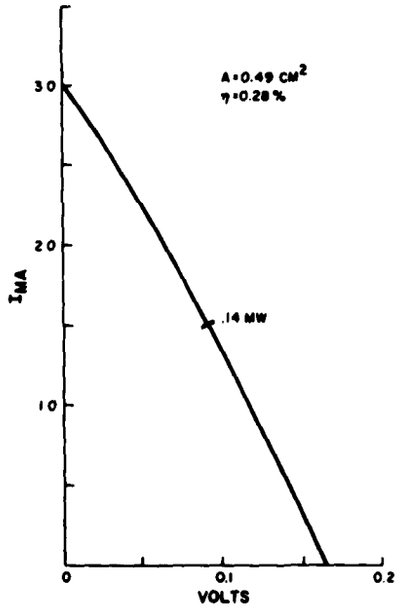


Figure A-32. I-V Curve, Recrystallized Cell No. RE-2

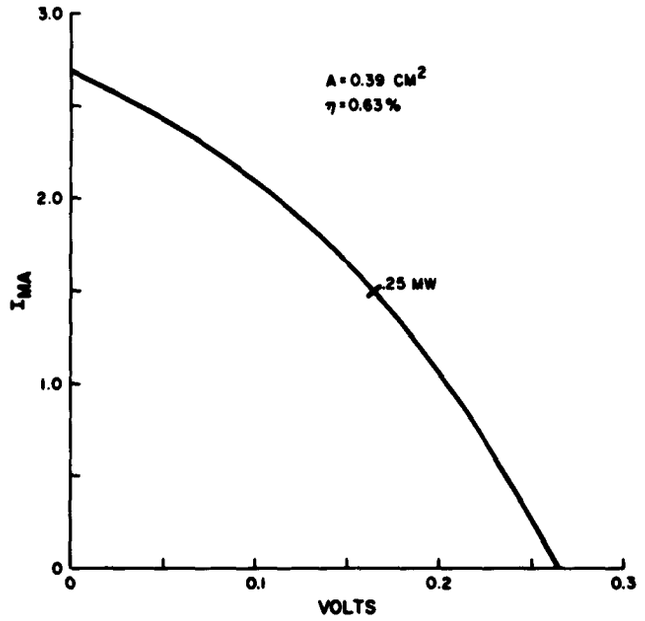


Figure A-33. I-V Curve, Recrystallized Cell No. RE-3

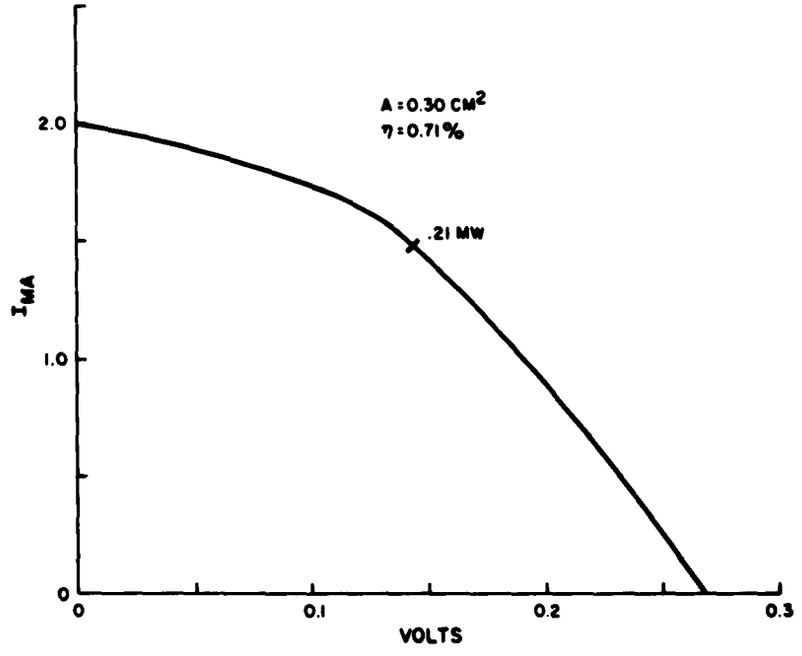


Figure A-34. I-V Curve, Recrystallized Cell No. RE-4

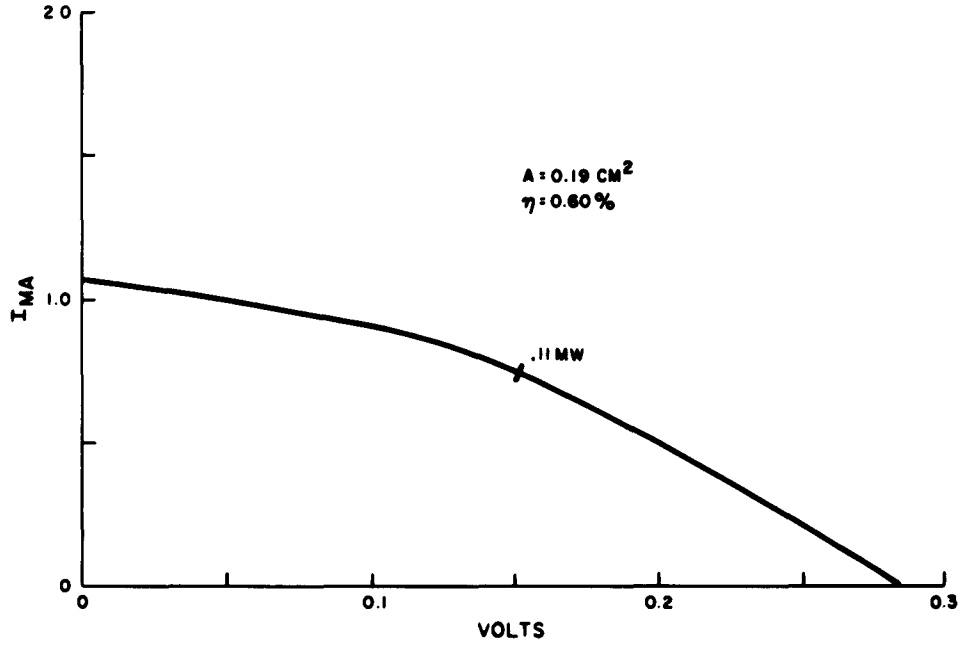


Figure A-35. I-V Curve, Recrystallized Cell No. RE-5

APPENDIX B

MATERIALS SECTION (TABLE LXXV)

I. LARGE-AREA CdS CELLS

INTRODUCTION

The fabrication of cadmium sulfide (CdS) solar cells can be divided into four processing stages:

(1) Preparation of the substrate,

(2) Evaporation of the layer or coating,

(3) Barrier formation, and

(4) Electrode application and test.

A listing of the materials employed in this study is included.

1. Materials

a. Cadmium sulfide (CdS); RCA Lancaster No. F-2108 luminescent powder

b. Fine copper powder (75 to 100 microns), suspended in an organic lacquer vehicle

c. Hydrochloric acid, CP grade

d. Tin, granular; Fisher Scientific Co.

e. Conductive epoxy cement; Epoxy Products No. 3021

f. Silver wire mesh, No. 35 x 40, 0.005-inch wire diameter with 0.017-inch opening; Newark Wire Cloth Co.

g. Solvent; Reliable Chemical and Paste Co., Thinner Mixture

h. Gold wire

i. Chromium-coated filament

j. Substrate; Borosilicate glass plates used for most of the cells in two thicknesses: 0.060-inch and 0.015-inch. These plates were coated with tin oxide providing electrical resistances of 30 to 60 ohms per square and optical transmission of 80 percent. An experimental organic polymer film of 0.001-inch thickness was tested as a substrate, and useful cells were fabricated with it.

TECHNICAL DISCUSSION

1. Preparation of the Substrate

a. Glass Substrates

Many of the cells were produced on the 1/16 inch thick Pyrex glass made conductive on one side by a layer of tin oxide. In order to reduce weight, some cells were made on Pyrex glass ground to a 0.015-inch thickness before deposition.

The preparation process requires that the substrate first be thoroughly washed with a detergent then soaked in distilled water for one hour (the distilled water is changed every 15 minutes).

After removal from the soaking bath, the substrate is sprayed with distilled water, acetone, and finally with isopropyl alcohol; it is then placed in a stainless-steel-mesh basket suspended in a vapor degreaser employing isopropyl alcohol as a cleaning agent. (The vapor degreaser is a corrosion-testing apparatus with a water-cooled condensing column to prevent the escape of vapor into the room.) The substrate is left in the degreaser for one hour with the alcohol boiling. Care must be taken to prevent contamination of the cleaned substrate, once it is removed from the alcohol. This concludes the preparation process and the substrate is ready for deposition.

b. Plastic Sheet Substrate

The plastic sheet is cut to 4-by-4-inch size and attached (by means of epoxy cement) to a frame made of tantalum. The tantalum frame is made of four strips each 3-3/16 by 3/16 inches by 20 mils thick, which are spot-welded at the ends to form a square. The plastic and frame assembly are cleaned by the same process as for the glass sheets described above. Electrically conductive coatings of chromium and gold are evaporated on the plastic sheet. The deposition of the evaporated CdS layer follows that of the conductive layer.

2. Evaporation of the CdS Layer

The evaporator shown in Figure B-1 is charged with 40 to 50 grams of CdS and a plug of quartz wool five millimeters high is inserted in the tube above the charge. A secondary heater, consisting of several turns of tantalum wire, is inserted in the mouth of the evaporator tube and pressed against the quartz wool. A clean glass chimney tube, five inches high and six inches in diameter, is mounted above the evaporator. The tube has a slit three millimeters wide at right angles to its axis through half the tube diameter at a distance of one inch from the top.

A mask rests on the chimney tube and supports the substrate and the substrate heater. (The substrate heater is a glass sheet with a conductive coating on one side.) A thermocouple is placed in contact with the 1/16-inch glass substrate, or in contact with the substrate heater for the 15-mil glass substrate or the plastic sheet substrate.

Electrical connections are attached to the heater and a shutter is placed in the chimney tube slit (see Figure B-2 for the equipment at this point). The system is then closed by the bell jar and evacuated to a pressure of 1×10^{-6} millimeters or less. The substrates are then heated to 250°C for the glass material, or 150°C for the plastic, and maintained at this temperature for one hour. Temperature regulation is accomplished by an indicating pyrometer controller (Semi-Ply-Trol 4531) which obtains its signal from the thermocouples inserted between the heater and the mask. Meanwhile, the evaporator is turned on and its temperature is brought up to 500°C for a 30-minute period then the temperature is raised to 1000°C. At this time substrate temperature is reduced to 175°C for substrates other than plastic film. When the temperature of 1000°C has been attained in the evaporator, an atmosphere of CdS develops; with the evaporator temperature stabilized at 1000°C, the shutter in the chimney tube is opened and CdS deposition begins. Evaporation is maintained under these conditions for about 50 minutes. The substrate is then allowed to cool to about 75°C before removal from the vacuum system.

3. Barrier Formation

After the CdS-coated substrates are removed from the vacuum system, they are checked for pinholes and other obvious defects. Next, the thickness is checked by focusing a microscope (with a vertical micrometer drive) on the top, then on the bottom, of the deposited layer. This measurement is made primarily for recording purposes and determines efficiency parameters.

The layer is etched for five seconds in a 5.8-molar solution of hydrochloric acid, and then immersed in distilled water. The layer is dried and placed in a holder attached to a motor shaft which rotates at 60 rpm. The holder with the CdS layer in it, is placed in the copper paste (which consists of 75- to 100-micron copper particles suspended in a lacquer vehicle at a temperature of about 70°C) and left to rotate for 45 minutes. The substrate with the CdS layer is then removed by washing with lacquer thinner (Reliable Paste and Chemical Co. Dare Thinner).

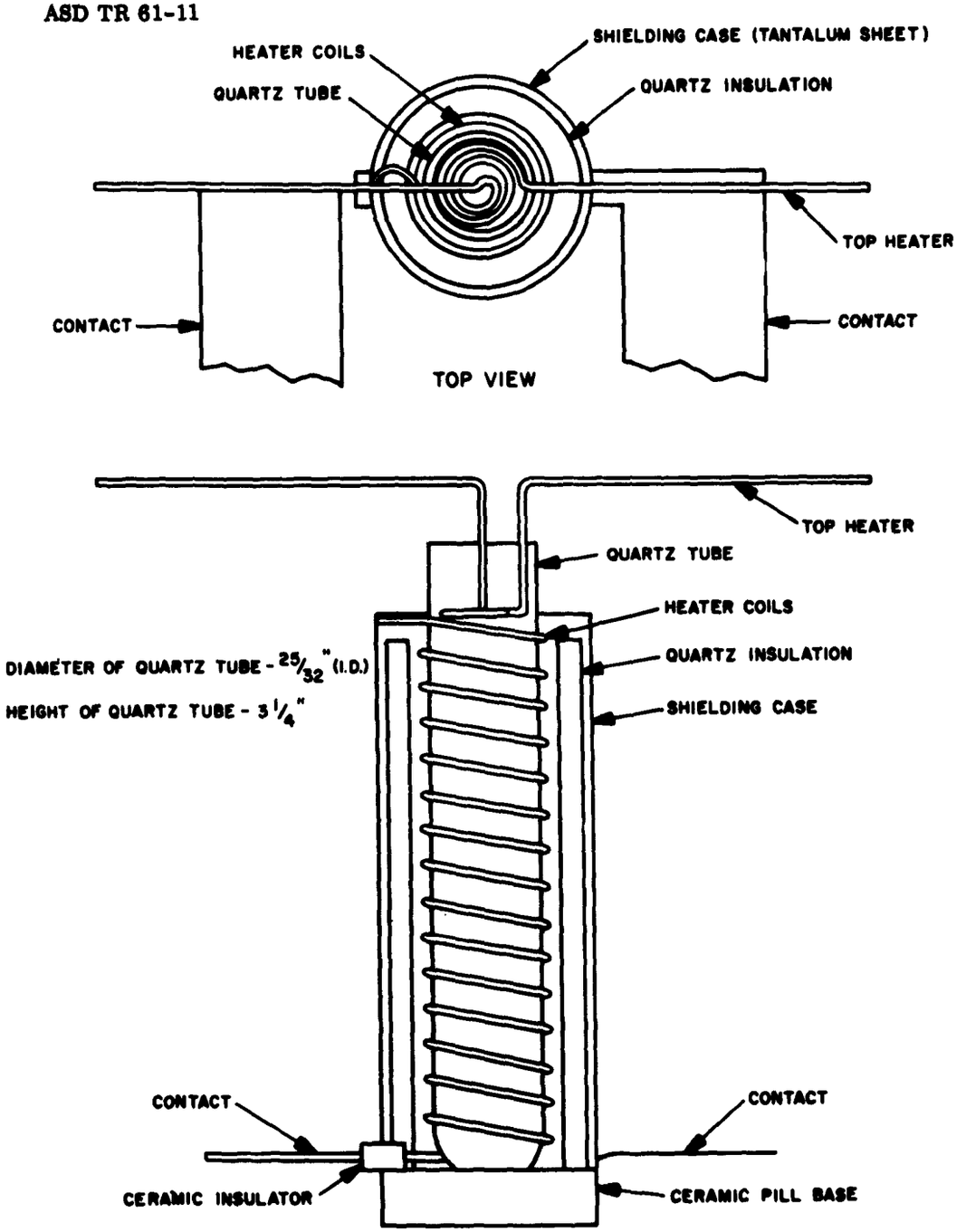


Figure B-1. Cadmium Sulfide Evaporator, Sectional Diagram

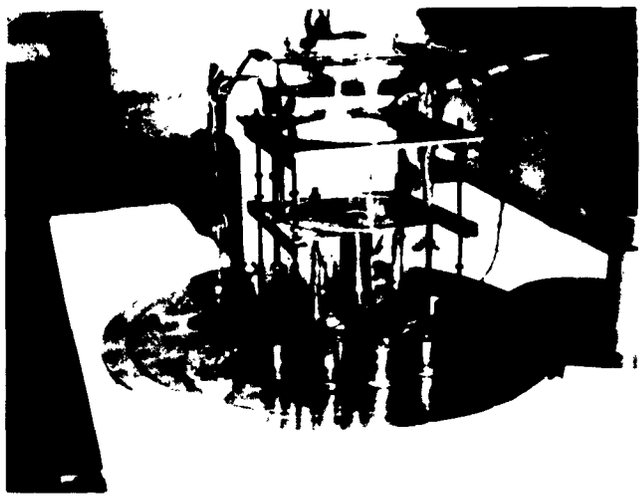


Figure B-2. Cadmium Sulfide Evaporator Before Application of Bell Jar

The dried layer is then placed in a tube (as in Figure B-3) and flushed with dry argon for one hour after which the tube is placed in a furnace (Lindberg B6) at 450°C, and left there until the substrate temperature (measured by a thermocouple in the tube) reaches 300°C. At this point (about three minutes) the tube is removed from the furnace and allowed to cool.

4. Electrode Application and Test

The upper electrode is applied to the CdS layer by one of two methods. One method, used principally during the early part of the work, is to apply a silver paste (DuPont No. 4817). Another method is that of evaporating tin over the barrier layer. The latter method was found to result in a reduction of the deterioration of the cell.

Silver wire mesh is attached to the tin conductive layer with a conductive epoxy cement (Epoxy Products No. 3021). One lead wire is soldered to the wire mesh and for the second electrode, stranded wire is cemented to the substrate around the periphery of the cell and a lead wire attached.

For the frontwall cell on plastic-sheet substrate, the top electrode was composed of thin lines of silver paste acting as a grid type of electrode.

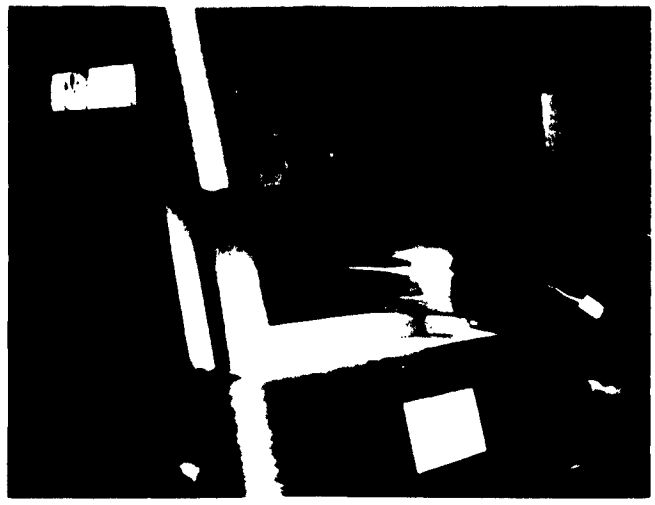


Figure B-3. Copper Diffusion Tube, In Furnace

After the electrodes have been applied, the cell is electrically tested under a battery of five tungsten-filament lamps (Sylvania 150-watt, 125-volt Projector Flood as in Figure B-4), the output of which is regulated by a variable transformer. The intensity of this light source is adjusted to provide the same short-circuit current from a reference "standard cell" as that obtained from a cell which has been calibrated by a pyroheliometer. The test cell, then, is in effect calibrated against the sun.

After the current-voltage characteristics and the active area of the cell have been measured, the cell efficiency can be determined.

II. VAN CAKENBERGHE CELLS

The delivered cells made by the Van Cakenberghe process were produced under a variety of conditions. Since this phase of the work was primarily of a research nature, detailed instructions for producing such cells cannot be given.

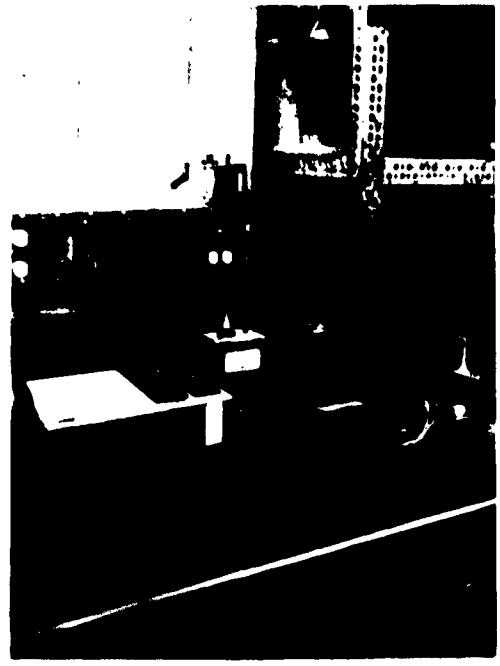


Figure B-4. Solar Cell Test Stand

The basic steps of the Van Cakenberghe process (which is described in Section II of this report) include the following:

1. Cadmium-sulfide, polycrystalline layer formation
2. Deposition of the activator layer
3. Recrystallization procedure
4. Barrier formation and special handling

Aeronautical Systems Division, Dir/Aeromechanics, Flight Accessories Lab, Wright-Patterson AFB, Ohio. Rpt Nr ASD-TR-61-11, Vol III. SOLAR CELL ARRAY OPTIMIZATION. Final report, Dec 62, 94p. incl illus., tables, 6 refs.

Unclassified Report

The over-all objective of the work is the achievement of the maximum electrical power conversion, in space, of solar energy per unit of system weight. The objectives of this phase were: (1) to continue research on photovoltaic materials, (2) to develop the crystal-layer conversion to the point of fabricating cells for delivery, and (3) to fabricate for delivery, one square foot of large-area, thin-film, CdS photovoltaic cells.

(1) Research of photovoltaic materials has shown the feasibility of fabricating cells with the p-n junction far removed from the surface by means of heterogeneous cell formation, of fabricating cells by the silkscreen technique of applying the active material, and also has shown that CdS polycrystalline cells are more resistant (by a factor of 10^4) to 1.6 Mev protons and (by a factor of 10) to 0.8 Mev electrons than are n-on-p silicon cells.

(2) The maximum efficiency of converted cells was about 0.7 percent; additional research is needed.

(3) Efficiency of the best four-inch-square cell was 1.2 percent. This is to be compared with the maximum efficiency of 5.7 percent obtained for small-area cells of 0.2 cm^2. One specimen array, which was delivered, contained five four-inch-square cells and demonstrated the potential of integrated circuitry for large-area cells to overcome high sheet resistance. This array also demonstrated the use of 0.002-inch plastic as cell substrate providing power density of 5 to 7 watts per pound. With this type of substrate, the potential power-to-weight ratio for four-inch-square cells approaches 20 watts per pound.

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1. Power conversion
2. Solar energy
3. Photovoltaic cells
4. Crystals
5. Solar cells

I. AFSC Project 8173, Task 871301-6
II. Contract AF 33(616)-7415
III. Astro-Electronic Div., Defense Electronic Products, Radio Corp. of America, Princeton, N. J.
IV. Aval fr OTS
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