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SYMPOSIUM ON MICROMINIATURIZATION OF ELECTRONIC ASSEMBLIES

TECHNICAL PAPERS

SPONSORED BY

DIAMOND ORDNANCE FUZE LABORATORIES

WASHINGTON 25, D.C.

30 SEPT – 1 OCT 1958

TECHNICAL PAPERS

presented at the

Symposium on Microminiaturization

of

Electronic Assemblies

compiled by

Eleanor F. Horsey

Ordnance Corps
Diamond Ordnance Fuze Laboratories
Washington 25, D. C.

30 Sept - 1 Oct 1958

F O R E W O R D

In March 1958 the First Annual Miniaturization Award, sponsored by Miniature Precision Bearings, Inc., was presented to the Diamond Ordnance Fuze Laboratories (DOFL) in recognition of the development and application of a photolithographic transistor by a group of its technical personnel comprising Edith M. Davies, Norman J. Doctor, Jay W. Lathrop, James R. Nall, and Thomas A. Prugh.

Following that time, the requests by both military and industrial engineers for information in respect to this and other developments in the general field of microminiaturization of electronic assemblies increased to the point where it appeared that an instructional-type Symposium would meet a real need.

The Chief of Ordnance approved such a Symposium. Philip J. Franklin, Chief, Materials Branch, DOFL, was appointed Chairman of the Symposium and unclassified papers were solicited from the Army, Navy, and Air Force.

The Symposium was held at DOFL on 30 September and 1 October 1958. The Chairman introduced Lt. Col. John A. Ulrich, Commanding Officer, Diamond Ordnance Fuze Laboratories, who described the "Status of Microminiaturization". Col. H. McD. Brown, Commanding Officer, U. S. Army Signal Research and Development Laboratory, then discussed "Future Demands on Microminiaturization in Military Electronics".

Twenty-one technical papers were presented in four sessions: Session 1 - Techniques, moderator Thomas A. Prugh, DOFL; Session 2 - Component Parts I, Moderator A. W. Rogers, U. S. Army Signal Research and Development Laboratory; Session 3 - Component Parts II, moderator Norman J. Doctor, DOFL; and Session 4 - Systems and Circuits, moderator Harold M. Nordenberg, Bureau of Ships.

On the evening of the first day of the Symposium a dinner was held at The Broadmoor, following which Dr. William H. Martin, Director of Research and Development, Office of the Secretary of the Army, gave an address entitled "Cutting the Lead Time". At the close of the Symposium, attendees were conducted on a tour of the Materials, Micro-Systems and Electron Devices Branches of DOFL.

There are included herein the twenty-one papers which were presented at the Symposium. The introductory speeches, and the discussion from the floor, are not included and will not be published separately.

These twenty-one papers will be published in a special issue of ELECTRONIC DESIGN and copies may be purchased from that periodical, address: Hayden Publishing Co., Inc., 830 Third Avenue, New York 22, New York, Attention: L. D. Shergalis, Associate Editor.

Philip J. Franklin

PHILIP J. FRANKLIN
Chairman
Symposium on Microminiaturization
of Electronic Assemblies

Diamond Ordnance Fuze Laboratories
1 October 1958

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MINIATURE INCANDESCENT INDICATOR LAMPS

Donald J. Belknap and Lloyd R. Crump
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Very small incandescent indicator lamps have been developed which will operate on the limited currents available in many miniaturized transistor circuits. Two types have been constructed having identical filaments and operating characteristics: (1) a miniature type having a glass bulb 0.200 inch long and 0.135 inch in diameter with the leads projecting from the base, and (2) a microminiature type having a sealed glass tube 0.100 inch long and 0.035 inch in diameter with one lead projecting from each end. When operating at 1 volt and 35 milliamperes of current these lamps produce a light easily visible from any point in a normally lighted room. Raising the potential to 1-1/2 volts increases the current to about 40 milliamperes and produces a very bright, and a very small source of illumination. Throughout the normal range of operation these lamp currents are well below the upper limit of about 50 milliamperes available in miniaturized transistor circuits currently under development in these laboratories. Operational characteristics and construction details are discussed.

Introduction

With the recent trend toward microminiaturization a need has arisen for a small indicator lamp which will operate on the limited currents available in many miniaturized circuits. This need has been emphasized by the recent techniques developed within DOFL for incorporating transistors along with printed circuit components on small ceramic wafers. Light indicators have not been available which are compatible in size with these miniaturized circuits and which will operate on the power available.

Two small incandescent lamps shown in Fig. 1 have been developed to meet this need. The miniature type shown at the right of the 1/2 inch square ceramic wafer and the microminiature type shown at the left contain identical tungsten filaments and have essentially the same operating characteristics; the main differences are in the envelope and in the methods used in sealing.

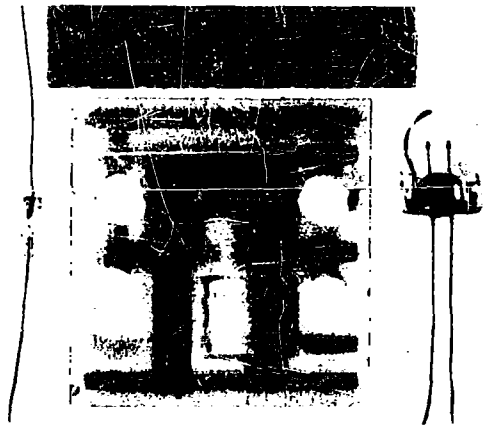

Figure 1. The two types of miniature indicator lamps compared with a 1/2 inch square ceramic wafer containing a printed circuit.

Operational Characteristics

These lamps have been designed to operate in the range of 1 to 1-1/2 volts and to draw currents of the order of 35 to 40 milliamperes. Fig. 2 shows a current versus voltage plot of a typical lamp and also gives the color temperature in the region in which the lamp would normally be operated. The light from the lamp operating at 1 volt and 35 milliamperes of current is sufficiently bright to be easily visible from any point in a normally lighted room. For other purposes, such as use of the lamp for a very small source of illumination, the filament can be operated at higher temperatures to give greatly increased light intensity.

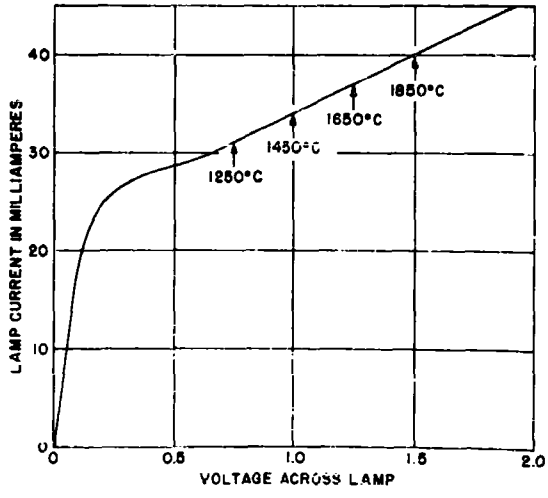

Figure 2. Current versus voltage of a typical miniature lamp with approximate color temperatures given in the range of normal operation.

Additional information concerning operation of this microminiature lamp as a light indicator is given in Fig. 3. The upper trace shows potential as a function of time for a 25 cycle/sec, 1.5 volt square-wave used to switch the lamp on and off. A photomultiplier tube was placed close to the lamp and the combination enclosed in a nearly light-tight container in order to exclude room light. A dual beam oscilloscope was used to permit direct comparison of the output of the photomultiplier tube with the corresponding voltage across the

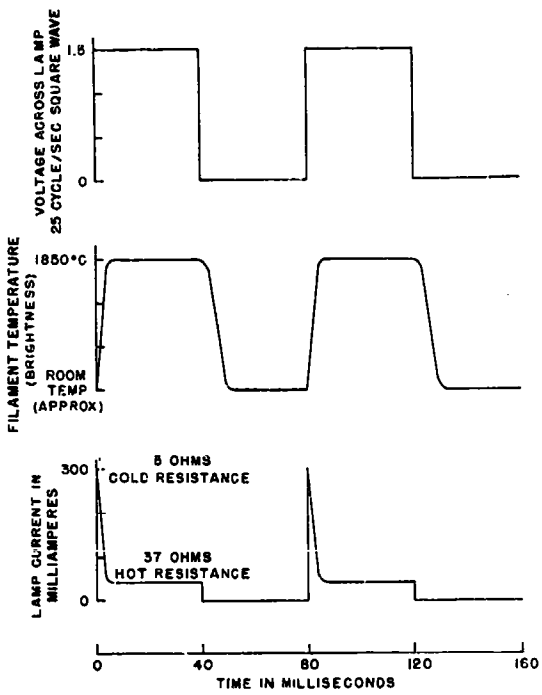

Figure 3. Experimental data on lamp operation as a light indicator.

lamp. The lamp brightness indicated by the photomultiplier tube is shown in the center trace of the figure. The bottom trace shows the current simultaneously flowing through the lamp.

It is evident from the center trace that the rise time of the light output is somewhat shorter than the decay time. The upper limit of frequency at which the light will go completely on and completely out is about 100 cycles/sec. As the frequency is raised to successively higher values the light output continues to be modulated, but the difference between minimum and maximum brightness becomes successively smaller. The peak current indicated in the bottom trace will not in general be as high as the value given by the ratio of steady-state lamp voltage to cold filament resistance. This is because any electrical circuit, in practice, contains at least a small amount of inductance which prevents an applied voltage from appearing instantaneously across the lamp.

Construction Details

The filaments of these lamps are made of 0.00033-inch tungsten wire wound on a 0.002-inch mandrel. Fifteen and twenty turns have normally been wound, although filaments with fewer turns and one with sixty turns have also been tested in experimental lamps.

The general shape of the larger lamps, which were constructed first, can be seen from the sample lamp shown at the right in Fig. 1. Each of these lamps has a length of about 0.200 inch and a diameter of about 0.135 inch. In constructing a lamp of this type, the envelope is first blown from pyrex glass. A bead, also of pyrex glass, is formed with the two kovar lead wires passing through it. After the filament is spot welded in position, titanium hydride is painted on those surface areas of the bead and envelope which are to be sealed together. The assembled lamp is then placed in a carbon crucible which is surrounded by a metal container. The metal container with its contents is placed in a bell jar and after evacuation is heated by means of an rf induction coil surrounding the bell jar. When a sufficiently high temperature is reached, a small piece of lead previously placed in contact with a painted area of the bead melts and flows along all of the painted areas, making a solid lead bond between the bead and base of the glass envelope. This procedure has produced very good vacuum-tight seals.

Fig. 4 shows schematically the construction details of the smaller lamps. Half-inch lengths of 0.005 inch platinum wire which are to form the lamp leads are first flattened for a short distance at one end. Glass beads are formed on the leads by sliding small bushings up against the flattened ends and heating in a small flame. The flattened ends of the platinum leads are then bent back to form hooks for the attachment of the very small filament wire. The glass sleeve, 0.035 inch in outside diameter and 0.100 inch in length, which is to be positioned over the beads to form the major portion of the lamp envelope, has the edges of one end turned in very slightly by heating the end at the edge of a small flame. This will permit the lamp to be sealed later in a vertical position with the glass sleeve hanging from the upper bead. The parts of the lamp are then assembled in a jig. With the glass sleeve slid to one side, the ends of the filament are placed in the hooks at the ends of the platinum leads, and these hooks are closed by pinching. Several spot welding methods of attaching the very small filament wire to the platinum leads were tried on early lamps and found to be less satisfactory. After attachment of the filament an alignment of the parts is made including suitable spacing of the platinum leads to produce a small separation between turns of the filament.

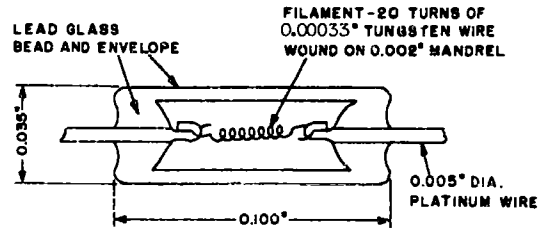

Figure 4. Construction details of the smaller lamp.

Heating coils of about 0.080 inch inside diameter wound from 0.009 inch tungsten wire and having 7 turns are positioned around each end of the assembled lamp. The jig containing the lamp and heating coils is then placed in a vertical position in a small bell jar, which is pumped out to a vacuum of about $5X10^{-5}$ mm Hg. The voltage across the two heating coils, which are connected in series, is controlled with a variac. To correct for differences in the rate at which the two ends of the lamp seal, the relative heat intensity of the two coils is controlled by using a slide wire rheostat connected across the two coils with the slide connected to a point between the coils. Observation of the sealing process through a stereoscopic microscope aids in controlling the heat while the ends of lamp are being fused.

Indications are that these lamps will have very long lifetimes, particularly when operated at the relatively low filament temperatures adequate for satisfactory performance as light indicators. Actual life tests under various types of operation have not yet been made. Over a period of about three months, however, several lamps of both types have been operated at frequent intervals as demonstration items. Lamps have also been subjected to voltages somewhat higher than normal during tests to determine electrical and temperature characteristics. The only lamp to burn out was one of the first ones constructed which was operated continuously for two months in a repeated cycle of one second on and one second off.

As a consequence of their small physical size, these lamps also appear to be very rugged, although again, controlled tests have not yet been carried out. Lamps informally tested by dropping several times onto the laboratory floor from a height of about six feet have suffered no noticeable damage.

Conclusion

These experimental lamps satisfactorily meet the requirements of the transistorized circuits for which they were originally designed as light indicators. The requirements were (1) very small physical size, (2) operation on about 1.3 volts, (3) a steady-state current drain of less than 50 milliamperes and (4) reasonably rapid on-off cycling time. Ruggedness and long life were also desired and although tests on these qualities have not yet been made it is expected that they will present no great problem. By suitably changing the size of the filament wire and the number of turns, it is possible to design lamps of similar geometry to meet different voltage and current requirements. Undoubtedly many other applications exist in which these lamps will also prove useful.

Acknowledgement

The sealing of the larger lamps, employing titanium hydride and lead, was done by Frank Brewer of the National Bureau of Standards, who generously gave of his time and employed facilities and techniques which he had previously developed for making ceramic to metal seals.

THE APPLICATION OF VACUUM EVAPORATION TECHNIQUES TO MICROMINIATURIZATION

L. Harold Bullis and William E. Isler
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Techniques of vacuum evaporation, and a general survey of the application of these techniques to the microminiaturization of components and printed circuits, are discussed together with some of the problems encountered in such work. Progress in this area at the Diamond Ordnance Fuze Laboratories is described with emphasis on vacuum deposited silicon monoxide capacitors. Capacitors having dielectric thicknesses varying from 0.46 to 2.23 microns have been prepared. Capacitance per unit area was found to be 0.0019 to 0.0099μf per cm^2, breakdown strength 1.1 to 3.5 kilovolts per mil, d.c. insulation resistance greater than 10,000 megohms, and dielectric loss less than 1%. The average dielectric constant was six. Preliminary work concerning the vacuum evaporation of fused silica for capacitor dielectrics is discussed. An indication of some developments which may be anticipated in the future is also included.

INTRODUCTION

In an attempt to obtain maximum circuit performance for minimum circuit volume, increasing emphasis is now being placed upon the use of electronic assemblies containing the smallest possible components supported by the thinnest possible wafers[1]. A logical extension of this trend involves the reduction of components to essentially two-dimensional thin films supported by extremely thin substrates. Such assemblies, when stacked, would produce units having a very large number of components per unit volume.

One of the most effective methods of producing thin films of a large variety of materials is that of high vacuum evaporation. It is not difficult to visualize the use of this technique for the production of complete electronic circuits, and the formation of such circuits is one of the ultimate objectives of the vacuum evaporation program of the Diamond Ordnance Fuze Laboratories (DOFL). This paper is chiefly concerned with some aspects of this program and with pointing out some of the ways in which vacuum evaporation techniques can be of value in microminiaturization.

VACUUM EVAPORATION TECHNIQUES

Vacuum evaporation involves heating a material in vacuum to such a temperature that a vapor pressure of at least 10^{-2} mm Hg is obtained. This value of vapor pressure was found to give a practical rate of vaporization for aluminum[2]; it is generally taken as a minimum value for the vaporization of most materials, whether metallic or dielectric. Table I compares the melting temperatures of some materials of interest in vacuum evaporation[3] with the temperatures required to obtain this value of vapor pressure for the same materials.

A typical arrangement for vacuum evaporation is shown schematically in Figure 1. Large currents of the order of hundreds of amperes are passed through low-resistance bus bars, labeled (a) in the figure. Connected between the bus bars is a high-resistance filament (b) containing the material to be vaporized (c), the charge. The filament becomes extremely hot and vaporizes the charge which then travels in straight atomic or molecular rays until it condenses upon a suitably placed substrate (d). A mask (e) is used to confine the deposit to the geometrical pattern desired. If the charge approximates a point source, vapor will travel equally in all directions and deposit a film of uniform thickness upon a spherical substrate (f) having the source as its center.

Table I. Comparison of melting-point temperatures of some materials with temperatures required for a vapor pressure of 10^{-2} mm Hg.(a)

Material	Melting point, T_m, °C	Vaporization point, T_v, °C
Group I, $T_v > T_m$:		
Aluminum (Al)	660	996
Gold (Au)	1063	1465
Fused silica (SiO_2)	1610	1725
Group II, $T_v \sim T_m$:		
Cryolite (Na_3AlF_2)	1000	1000
Magnesium fluoride (MgF_2)	1395	1400
Palladium (Pd)	1555	1566
Group III, $T_v < T_m$:		
Cadmium (Cd)	321	264
Silicon monoxide (SiO)	>1250	1250
Cadmium sulphide (CdS)	1750	1380

(a) See reference 3.

Materials commonly used for filaments are high-melting-point metals such as tantalum, tungsten, and molybdenum. The choice of a suitable filament material is governed primarily by the temperature to which the charge must be heated, the degree to which the charge wets the filament, and the prevention of chemical reaction between

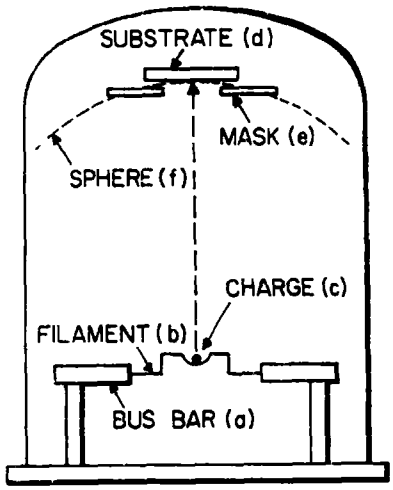


Figure 1. Experimental arrangement for vacuum evaporation.

the charge and filament at the maximum temperature used. Filament assemblies vary from simple wires and conical baskets to more elaborate configurations such as ceramic crucibles encircled by metal bands. Since the typical substrate is flat, rather than spherical, the largest dimension of the substrate must be small compared to the distance between the substrate and the source if a film of uniform thickness is desired.

Of considerable importance in vacuum evaporation work is the measurement and the control of film thickness, and several methods are available for accomplishing both objectives.[4] These include the use of: (a) special microbalances of high sensitivity, (b) the interference of monochromatic light transmitted through or reflected from a thin film, (c) the absorption or polarization of light by a thin film, and (d) the change in a specific property of a thin film, such as electrical conductivity. The control aspect is typically more difficult than is measurement, and good control in general requires the performance of a considerable amount of preliminary experimental work.

STATUS AND PROBLEMS IN VACUUM EVAPORATION

There are at least three different ways in which the use of vacuum-deposited thin films can assist in reducing circuit volume. First, it is possible to deposit a thin-film component in an area of a conventional printed circuit which might otherwise be wasted. Second, the geometry of the thin film can be used to advantage. For example, the capacitance of a capacitor of given area can be increased by making the dielectric extremely thin. Third, use can be made of the inherent properties of thin films. For example, the resistivity of many thin metal films increases as the film thickness decreases. The second and third items are likely to be of more value in microminiaturization than the first item.

Considerable work has already been done in producing components by vacuum evaporation. Thus far, primary emphasis has been placed upon the development of thin-film resistors. This work is extensive and no attempt will be made to review it here beyond citing a few references[5,6,7] Progress has been sufficient to enable the commercial production of several types of pure-metal thin-film resistors.[8,9] These resistors are small by comparison with wire-wound resistors of similar resistance values and characteristics. Their maximum size is about 2 inches in length by about 1/4 inch in diameter. They have low residual noise levels, high stability, excellent temperature coefficients, and excellent high-frequency characteristics. Values are limited to several hundred kilohms because the conductivity of pure metal films is relatively high even for extremely thin films. Although these commercial resistors are obviously too large for use in microminiature circuits, their desirable properties can be expected in thin-film resistors deposited directly into such circuits.

Experimental, thin-film capacitors have been produced by several laboratories in the United States using vacuum evaporation techniques. Thus far the most promising results have been achieved using dielectrics of silicon oxide[10,11] and aluminum oxide.[12] The best quoted values[10] not necessarily values for a single capacitor, show a capacitance per unit area of approximately $0.005\mu f/cm^2$, an insulation resistance of 100 kilomegohms, and a loss factor of less than one percent. Thus far, however, no procedure has been developed for systematically producing low-loss, high-quality capacitors. The work to date, including that described later in this paper, can best be said to have demonstrated the feasibility of forming capacitors by vacuum evaporation; the improvement and adaptation of such capacitors to microminiature circuits are problems which still require solution.

In addition to resistors and capacitors, selenium rectifiers are now being made by vacuum evaporation techniques. Thin-film inductors and other components appear entirely feasible. Since contacts and wiring for interconnecting components can also be deposited, it thus appears entirely possible to deposit complete electronic circuits in which the wiring, contacts, and components consist of thin films. Preliminary work in this direction is being conducted at several laboratories[11,13] as well as at DOFL.

The formation of complete circuits by vacuum evaporation at present involves several formidable difficulties. One such difficulty lies in the fact that once circuit values have been determined, components must be deposited in the circuit within the tolerances specified; in general, no sorting, selecting, or trimming processes are possible. Such deposition requires great precision of the evaporation process and hence precise control throughout the entire

deposition period of such variables as pressure, temperature, and rate of charge-evaporation. It appears most feasible to assign a calculated area within a circuit to a component and then to obtain the exact value desired by varying the thickness of the component. Such a procedure requires the use of a precision monitoring system to enable deposition to be stopped when the desired value has been reached. For example, the resistance of a resistor might be continuously monitored from outside the vacuum chamber as the resistor formed. Similarly, the thickness of a capacitor dielectric might be monitored by light reflected either from the capacitor or, preferably, from a dummy plate placed at a convenient point within the chamber. In the latter case, the thickness of the capacitor dielectric would be calibrated in terms of the thickness of the film deposited on the dummy plate.

Another difficulty involves the successive deposition, in a single evacuation, of all the varied materials required for a given circuit. Several problems are likely to be encountered. First, at least one filament must be included in the vacuum chamber for each material to be evaporated. If contact of the completed circuit with air must be avoided, an additional filament may be required for deposition of a protective overcoating on the circuit prior to admission of air to the chamber. Ideally, each filament must be centered below the substrate and, failing the use of a multiple chamber, such arrangement is, of course, impossible. Second, some of the various materials to be evaporated will have to be heated to extremely high temperatures and, in the course of depositing successive layers of different materials, the high source-temperatures might damage previously deposited elements of the circuit, all of which are exposed to heat radiated from the source. Third, multiple evaporations make necessary the interchanging and moving of masks within the evacuated chamber. The mechanical manipulation of such masks may be very complicated when small areas and intricate configurations are involved.

Two other problems are worthy of mention. First, extreme cleanliness is necessary in vacuum evaporation work to assure adequate adherence of the deposited layers to the substrate and to each other. Gross quantities of contaminants are removed from a substrate by standard cleaning techniques involving various types of washes and degreasing solutions. However, the unavoidable exposure of a substrate to air between the final cleaning step and the evacuation of the vacuum chamber, is sufficient to recontaminate it. It is thus necessary to subject substrates to the cleaning effect of a low-pressure glow-discharge just prior to film deposition. Second, not even the glow-discharge treatment is sufficient to remove from a substrate all dust particles, some of which may produce pinholes in the vacuum-deposited films. Such pinholes, depending upon their location, might ruin a particular component and force rejection of an entire circuit. Factors other than the presence of dust on a substrate may also be responsible for pinholes. No explanation as yet advanced has adequately accounted for the formation of pinholes, nor has a means been devised for their complete elimination.

VACUUM-DEPOSITED CAPACITORS MADE AT DOFL

Initial work at these laboratories involved the formation and study of thin-film capacitors having vacuum-deposited silicon monoxide as the dielectric. The comparatively wide attention this material has received is largely due to the ease with which it can be evaporated and the availability of considerable information concerning it.[14,15,16] Subsequently, the work was extended to the study of silicon dioxide (fused silica) as a capacitor dielectric.

The apparatus used is shown in Figure 2. It

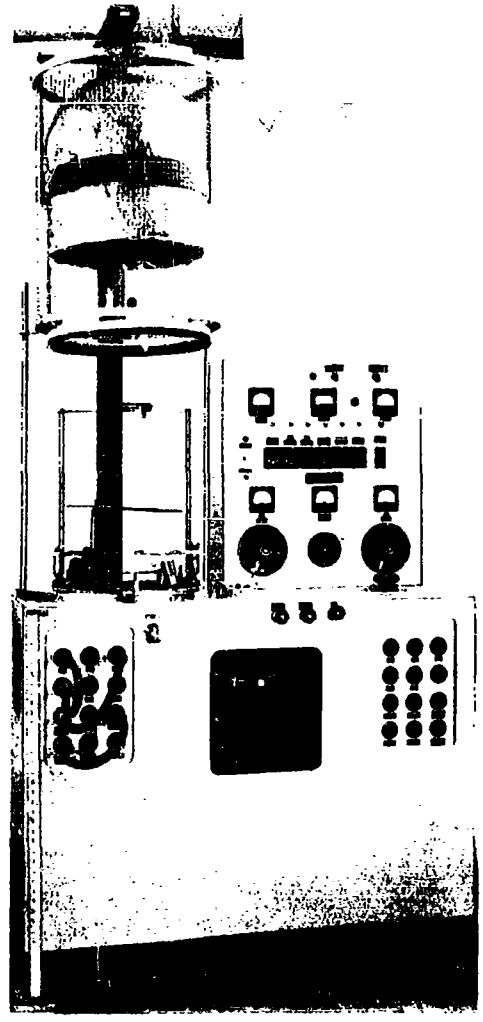


Figure 2. Laboratory vacuum evaporator.

consists of a chamber which can be evacuated by high-speed pumps, a central control panel, and two low-voltage high-current power supplies. Although this apparatus was built to order, it can be considered fairly typical of experimental equipment used in research laboratories. A close-up view of the baseplate of the evacuation chamber and fixtures is shown in Figure 3. A filament of the type shown between the two bus bars is primarily suitable for the heating of metals, but filaments suitable for heating dielectric materials can readily be substituted.

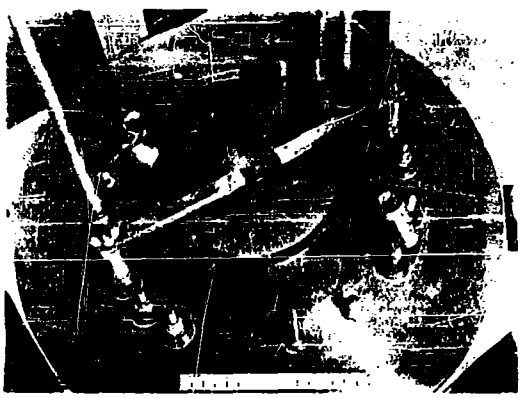


Figure 3. Baseplate of vacuum evaporator.

A. Silicon monoxide dielectric

Initially, several groups of capacitors were made by depositing three successive film-layers; the central layer was silicon monoxide, and the outer layers consisted of a variety of metals. No attempt was made to closely control the thicknesses of these preliminary units, and several were discarded after inspection for flaws or after testing. It was possible, however, to obtain values of capacitance per unit area, dissipation factor, direct-current insulation resistance, dielectric thickness, dielectric constant, and breakdown strength for many of the capacitors; average values are given in Table II. In addition to the six electrode metals shown, copper was also used but in all cases films of it peeled away from the dielectric.

Measured values of capacitance per unit area varied from 0.0019 to 0.0099$\mu f/cm^2$ for dielectric film thicknesses of from 2.23 to 0.46 microns, respectively. Calculated values of dielectric constant varied from 5 to 7 with an average value of 6. Minimum dissipation factor was 0.9%, and maximum direct-current resistance was in excess of 10,000 megohms. These preliminary data confirm those described in the section on "STATUS" indicating that it should be possible to form excellent capacitors by vacuum evaporation.

It is evident from the data for dissipation factor and direct-current resistance that the best capacitors were those formed with electrode films of noble metals. Gold is to be particularly recommended for thin-film electrodes because of its high conductivity, inertness to oxidation, and ease of deposition. The present data are too limited, however, to indicate whether the good properties of these capacitors were principally derived from the use of noble-metal electrodes or were due principally to other factors such as dielectric thickness. However, as might be expected, there does appear to be a tendency for insulation resistance to increase and dissipation factor to decrease with increasing dielectric film thickness regardless of the electrode metal used.

As shown in Figure 4, voltage breakdown strengths varied from 1.1 to 3.5 kilovolts per mil as dielectric thickness decreased from

Table II. Electrical properties of thin-film vacuum-deposited silicon-monoxide-dielectric capacitors.

Electrode metal	Number of samples	Capacitance per unit area, $\mu f/cm^2$	Dissipation factor, %	Direct-current resistance, megohms	Dielectric thickness, microns	Dielectric constant	Breakdown strength, kv/mil
Ag	6	0.0019	0.9	>10,000	2.23	5	1.1
Au	2	0.0031	1.9	>10,000	1.62	6	1.9
Mg	10	0.0060	> 5.1	--	1.07	7	---
Sn	9	0.0069	2.5	4,100	0.92	7	3.3
Zn	12	0.0098	4.3	230	0.47	5	3.5
Al	4	0.0099	3.9	40	0.46	5	---

about 0.09 to about 0.02 mil. Additional data would be necessary to establish whether a maximum value of breakdown strength is being approached at a dielectric thickness of approximately 0.02 mil.

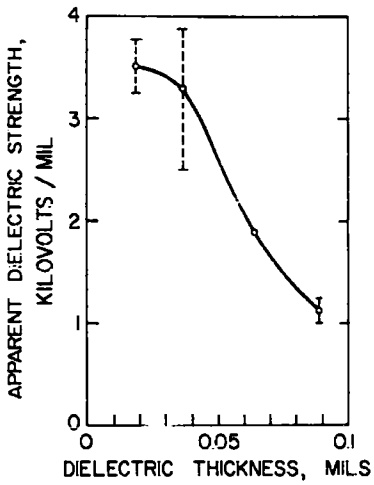
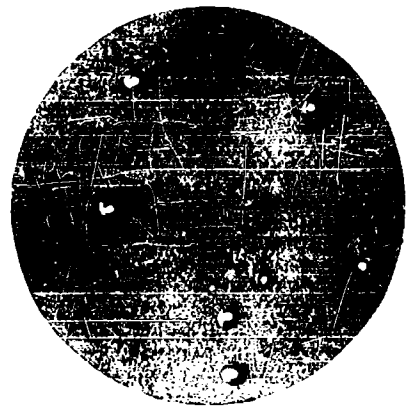


Figure 4. Apparent dielectric strength of silicon monoxide films as a function of film thickness.

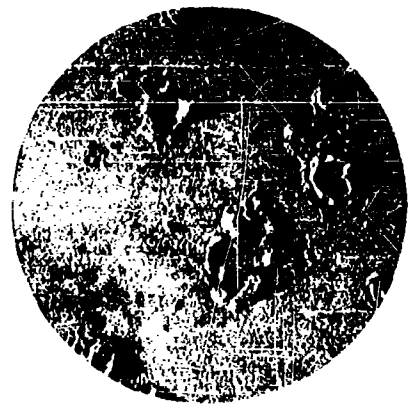
The breakdown strength discussed above requires further explanation since the capacitors produced did not consist of perfect films but rather of films containing minute pinholes. The pinholes in the dielectric film sometimes became filled with metal when the counter electrode was applied, thereby shorting the capacitors. Such shorts are analogous to those found in metallized paper capacitors.[17] They were removed, and hence the capacitors cleared, by sending energy pulses through the capacitors. This process required careful control to prevent damage to a capacitor by a pulse of excessive energy. The result of an optimum energy pulse is shown in Figure 5a; the shorting material was removed with virtually no disturbance of the surrounding areas. The result of an excessive energy pulse is shown in Figure 5b; a crater-like effect was obtained as a result of the explosiveness of the clearing action which destroyed the surrounding area and deposited debris over the capacitor surface. Complete breakdown of the capacitor is shown in Figure 5c.

B. Silicon dioxide dielectric

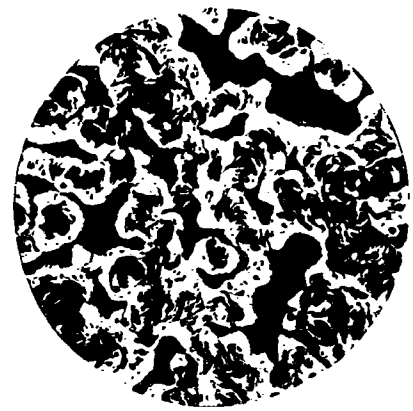
The dielectric breakdown strength of fused silica, given as 15,000 volts per mil in 1/8 inch sheets[18] is among the highest known. The use of this material as a capacitor dielectric at normal temperatures should, therefore, permit excellent voltage ratings for thin-film capacitors. The stability of fused silica under normal conditions should result in additional desirable capacitor characteristics.



a. Constructive clearing.



b. Destructive clearing.



c. Complete breakdown.

Figure 5. Behavior of silicon-monoxide-dielectric capacitors when subjected to pulses of increasing energy, X33.

The vacuum evaporation of fused silica, however, is difficult for several reasons. First, silica is extremely difficult to heat in vacuum because it absorbs little radiant energy.[19] Second, it must be heated to a temperature in excess of 1700°C.[20] Third, it decomposes readily under the conditions usually encountered in vacuum evaporation.[21] Several techniques have been suggested for circumventing these difficulties but all have undesirable features. One such technique involves the deposition of silicon monoxide followed by conversion to the dioxide.[22] Unfortunately, such conversion, for films of appreciable thickness, requires a prolonged high-temperature oxidation[23] which could impose severe limitations upon any other circuit elements present. Another technique involves the slow evaporation of silicon monoxide in poor vacuum to obtain conversion of the monoxide to the dioxide by means of molecular collisions prior to deposition.[24] Such condition, however, are known to produce porous films and require excessive periods of time. A third technique involves mixing reducing materials or metals, such as aluminum, with the silica to act as a flux in aiding heat transference to the silica.[25] However, this usually results in reduction of the silica to silicon monoxide. It has, therefore, seemed best to employ a fourth technique, the direct evaporation of silica, despite the heating difficulties previously mentioned.

In the direct evaporation work, reduction of the silica was avoided by using a beryllia (BeO) crucible rather than a standard metal filament. It was then found possible to melt and vaporize silica directly. A comparison of films formed by the latter three of the four above-described methods is given in Table III.

Table III. Comparison of several methods of forming silicon oxide films on fused silica plates.

Method of formation	Time required, minutes	Thickness, A	Deposition rate, A/sec	Estimated SiO_2, %
Flux	2.5	460	3.0	< 33
Direct	38.	1880	0.8	89
Conversion	150.	2580	0.3	97

It is evident that the direct evaporation method represents a compromise between the desired high percentage of SiO_2 in the film and the speed of formation. Ultraviolet transmittance measurements were used to estimate the amount of dioxide present in each film, assuming the other film component to be the monoxide. This procedure was possible because the transmittance of the dioxide is much greater than that of the monoxide in this spectral region. For example, Figure 6 shows that at 300 mμ, the wavelength used, the difference is greater than 90%. This

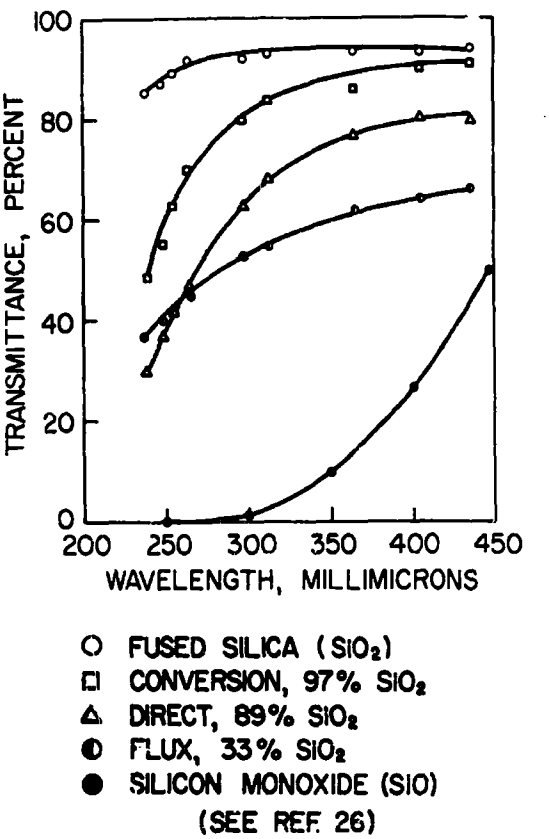


Figure 6. Comparison of the ultraviolet transmittance of silicon monoxide and silicon dioxide (fused silica) with that of several mixed silicon oxides.

curve for pure silica was derived from measurements on a silica plate and that for silicon monoxide from a film of pure material of thickness 330A.[26] The ultra-violet transmittance of the films of Table III is also shown in Figure 6.

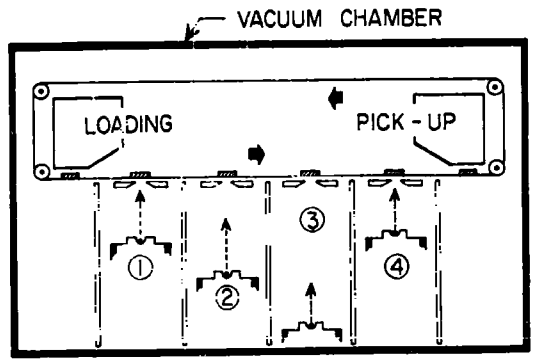
The direct evaporation of pure silica at present represents a compromise between the other two methods but, in recent work at these laboratories, concentrations of silica up to 96 percent have been obtained by the method. It is possible that with further development of techniques, fused silica may be even more successfully evaporated in this manner.

FUTURE POSSIBILITIES

The use of vacuum evaporation techniques in

microminiaturization has scarcely begun. Many developments can be expected in the future as the potentialities of the method become more widely appreciated. For example, one can expect considerable progress in both the techniques of vacuum evaporation and the number of materials available for use.

A considerable amount of effort and ingenuity will be required in perfecting suitably precise monitoring systems, in exercising adequate control over process variables such as pressure and temperature, in eliminating pinholes, and in avoiding contamination of the thin-film layers. Since there clearly is a limit to the area which can be assigned to a resistor or to a capacitor in a microminiature circuit, techniques will have to be devised for depositing high-resistivity as well as high-dielectric-constant materials. Such techniques would enable the extension of the range of values possible with vacuum-deposited resistors and capacitors to include most values likely to be encountered in microminiature transistor circuits. Many technical difficulties may be more readily resolved on a production basis than they are in the laboratory.[27] For example, circuits could be formed by transporting the base substrates on a conveyer arrangement located in a vacuum chamber divided into several compartments, as shown in Figure 7. This would: (1) enable positioning of the circuit to best advantage with respect to each source, (2) reduce danger of overheating the circuit, possibly by providing cooling during exposure to sources of the highest temperature, and (3) make possible the use of stationary rather than movable masks. Undoubtedly, printed circuit techniques, such as the use of masks of photosensitive resist[28,29], will aid in solving many difficulties.



① WIRING AND ELECTRODES

② RESISTORS

③ DIELECTRICS

④ WIRING AND ELECTRODES

Figure 7. Possible method of circuit fabrication by vacuum evaporation.

The usefulness of presently available as well as new materials in microminiaturization work depends upon the ease with which they can be obtained in a microminiature circuit in exactly the location and configuration desired. In general, however, all materials which are now being applied by coating and molding methods of one kind or another can be considered for use in vacuum evaporation work provided only that they can be vaporized without undesired decomposition. In particular, when semiconductor materials can be deposited as single crystals, transistors and diodes will be capable of being formed "in situ" and thin-film circuits and solid circuits will be a reality. In addition, there is the intriguing possibility of forming useful materials "in situ" as a result of chemical combination of various elements and compounds during deposition. For example, by the simultaneous evaporation of barium oxide and titanium dioxide under controlled conditions it might be possible to form and deposit barium titanate from the mixed vapor. In analagous fashion, metal alloys might be deposited after vaporizing the individual constituents at predetermined rates, and combining them in the vapor phase. The investigation of such vapor phase reactions may produce remarkable results.

These and other developments appear certain to assure increasing use of vacuum evaporation techniques in microminiaturization.

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SOME CIRCUIT TECHNIQUES TO ELIMINATE LARGE-VOLUME COMPONENTS: A LITERATURE SURVEY

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The construction of electronic devices of microminiature size requires that the component parts occupy a small volume. This requirement is most difficult to execute at audio and sub-audio frequencies where large-valued components are necessary. The results of a literature survey indicate that it is possible to eliminate large-volume component parts in amplifiers, filters, and oscillators by employing various circuit techniques. Positive feedback permits the elimination of by-pass capacitors. Direct coupling eliminates d.c. blocking capacitors. Resonant resistance-capacitance networks, either passive or active, can be substituted for the bulkier inductance networks normally used in filters and oscillators in the audio and sub-audio frequency ranges. Of particular interest are the zero phase shift network for use as an interstage coupling, and the parallel-T network for sharply tuned amplifiers and oscillators.

INTRODUCTION

Conventional circuit designs of amplifiers, filters, and oscillators for the audio and sub-audio frequency ranges are relatively straightforward. However, the execution of these designs into practical operating devices of microminiature size is often complicated by the large values, large volumes, and possibly inferior performance that certain component parts may assume when operated in these ranges.

For many years, engineers have attempted to eliminate large component parts by employing various circuit techniques. While most of these techniques were initially developed for use with vacuum tubes, the extension of these principles to transistor circuits is logical. This paper is a result of a literature survey conducted to uncover and collect in one body some of these techniques; it will disclose their basic operating principles and how they might be applied in the field of microminiaturization. The presentation is given in three main groups: amplifiers, simulated reactances, and filters and oscillators.

I. Amplifiers

A. Positive feedback techniques

Positive feedback or regeneration results when a portion of the amplified signal is returned to the amplifier input in the same phase as the original input signal. This has the effect of increasing the amplifier gain by a considerable amount. If the amount of positive feedback is made great enough to make up for attenuation in the various coupling networks, the amplifier will oscillate at some frequency governed by the constants in these coupling networks and the phase shifts through the amplifier. When this condition prevails, no input signal is required in order to obtain an output from the amplifier.

In designing amplifiers for miniature circuits, it is generally desirable to get maximum amplification per stage, using a minimum number of components, and yet have the system relatively free from instability or oscillation. A controlled amount of positive feedback incorporated in the amplifier design can achieve these ends in vacuum tube circuits, and to some extent in transistor circuits. In a typical two-stage resistance capacitance coupled amplifier, to establish the proper d.c. operating conditions for the tubes, cathode bias is generally employed. The cathode by-pass capacitors are the most bulky of the components employed since values of the order of 10μf and larger are required for audio-frequency applications. If these capacitors are omitted, a great reduction in gain results from negative current feedback in the cathode bias resistor. Sulzer(1) describes a method of applying controlled positive feedback between the stages to offset this reduction in gain, and it is shown in Figure 1. The positive feedback is applied by a resistor Rf connected between the cathodes. A similar method of applying positive feedback between the screen grids of two pentode stages to eliminate the screen by-pass capacitors is also described.

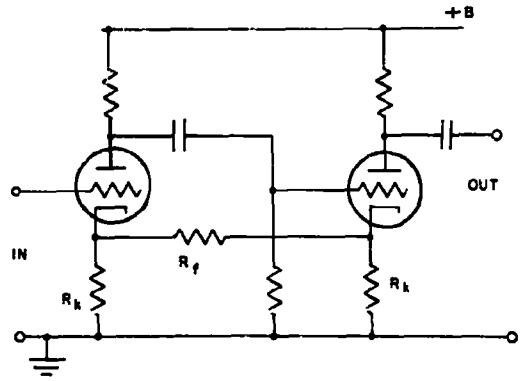

Figure 1.-Two-stage resistance-capacitance coupled amplifier with positive feedback.

Anspacher(2) gives an analysis of a two-stage pentode amplifier circuit without any by-pass capacitors, the resulting degeneration being nullified by means of positive feedback between the two screen grids.

Unlike vacuum tubes, transistors require a forward bias to establish the proper d.c. operating conditions. This may be supplied in several different ways. In order to stabilize the transistor against thermal runaway, d.c. feedback which tends to bias the transistor toward cutoff as the collector current rises, is commonly used. A resistor is connected in the emitter circuit to stabilize emitter current. The emitter resistor

is generally by-passed to prevent loss in gain due to degeneration, as in vacuum tube circuits.

Alexander[3] describes a transistor audio amplifier, similar to the previous vacuum tube circuits, where positive feedback between the emitters is used to obviate the requirement for large by-pass capacitors across the emitter resistors. It is shown in Figure 2.

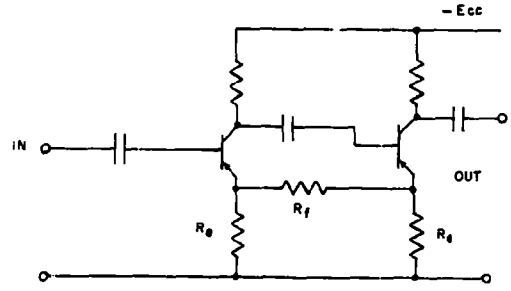

Figure 2.-Two-stage resistance-capacitance coupled transistor amplifier with positive feedback.

An additional economy, although not related to positive feedback, is demonstrated in this circuit. It involves the elimination of the two-resistor forward biasing network in each base circuit. This function is accomplished by the voltage drop that appears across the base-emitter junction as a result of the leakage current of the transistor. This biasing method is not recommended, since it is sensitive not only to temperature variations, but also to differences between transistors.

B. Direct-coupled amplifiers

A somewhat different technique for eliminating large-volume components and improving the low-frequency response of an amplifier is to employ direct-coupling. In this case, the coupling capacitors and cathode by-pass capacitors are eliminated. Unfortunately, due to the direct-coupling, any drift in the input stage is reflected as a rather large voltage excursion at the output. Various means have been employed to eliminate the drift problem, including chopper stabilization. Much of this information is summarized by Landee et al[4].

"The use of PNP transistors made by fusion techniques and surface-barrier transistors permits a direct connection of the collector of one stage to the base of the following stage without the use of interstage biasing arrangements. This is possible since the collector resistance is high and the current gain is close to its nominal value when the collector-to-base voltage is zero or slightly positive. At low level stages, the use of this technique results in very simple circuitry. However, the collector-voltage swing of any stage directly coupled to the base of a following stage is restricted to a very small voltage (0.2 to 0.6v). Since the transistors are operated as current amplifiers, the small allowable collector-voltage swing does not adversely affect the operation of low-level stages. In many practical amplifiers this technique may be employed for coupling the first two or three stages of a high-gain amplifier. ..." Hurtig[5]. An amplifier circuit of this type is shown in Figure 3. It has a power gain of 70db and incorporates d.c. feedback for stabilization.[6]

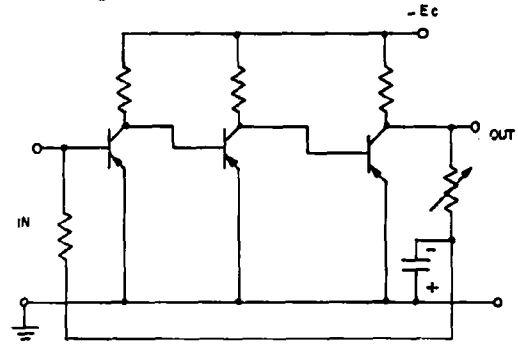

Figure 3.-Direct-coupled transistor amplifier.

As in the case of the vacuum tube, d.c. drift cannot be ignored. It is unfortunate that the temperature sensitivity of transistors increases the drift. However, if this circuit is employed as a low-level, high gain pre-amplifier, capacitive coupling at the output will remove the d.c. component without affecting its properties as an a.c. amplifier. The economy of component parts and the high gain cannot be overlooked for application in microminiature sub-assemblies.

Another type of direct-coupling scheme used with transistors is called complementary symmetry, and is discussed by Sziklai[7]. This method employs both PNP and NPN transistors. It is possible to eliminate emitter by-pass capacitors and some load resistors, although the power supply connections may be somewhat more complicated. This method is shown in Figure 4 and can deliver a voltage gain of the order of 25 per stage.

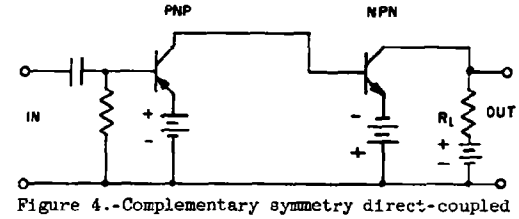

Figure 4.-Complementary symmetry direct-coupled transistor amplifier.

Perhaps the most popular use of the principle of complementary symmetry is in Class B power amplifier applications. The advantage of Class B operation is that the circuit draws negligible current until signal is applied. In the usual configuration, both an input and an output transformer are required. Sziklai[7] describes a circuit of a Class B power amplifier with a direct-coupled complementary symmetry driver. It is shown in Figure 5. This amplifier does not contain any parts other than the transistors themselves and operates from

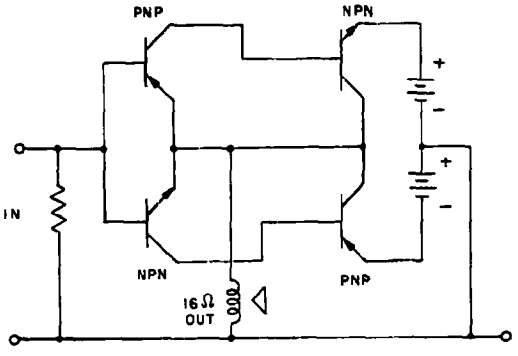

Figure 5.-Complementary symmetry Class B power amplifier with direct-coupled driver.

a high impedance signal source directly into a 16-ohm loudspeaker voice coil. The low output impedance and the stable operation are made possible by the over-all feedback which extends down to d.c. Incidentally, this is a zero-center d.c. amplifier. Its economy of component parts recommends it for microminiature power amplifier applications.

II. Simulated Reactances

With certain circuit configurations, an active element such as a vacuum tube or transistor may behave as a reactance. Some well known applications of this phenomenon are the reactance modulator used in frequency modulation, and the Miller integrator and operational amplifiers used in analog computer work. Very often, however, the reactance effects are not pure, but also introduce resistive effects. For purposes of power supply filtering, the resistive effects are not considered to be as important as the reactive properties of the device. Linvill[8],[9] gives theory on RC active filters using transistors.

A. Inductance

Towner[10] describes a circuit which is composed of resistive and capacitive elements, and three tubes as amplifiers. The device behaves as a true inductance in that it differentiates square waves, integrates triangular waves, and resonates with capacitance across its terminals. Some of the applications described are for a low frequency sine wave oscillator and as a filter circuit for tone control purposes in audio amplifiers.

Tomer[11] describes a circuit wherein a pentode tube may be used in place of a high inductance choke in a power supply filter. While not a pure inductance element, the high a.c. plate resistance and low d.c. drop through the tube permit the circuit to fulfill the requirements ordinarily imposed on a filter choke.

Stern[12] describes a transistor simulated inductance using only capacitance as the reactive parameter. A series simulated inductance is shown in Figure 6.

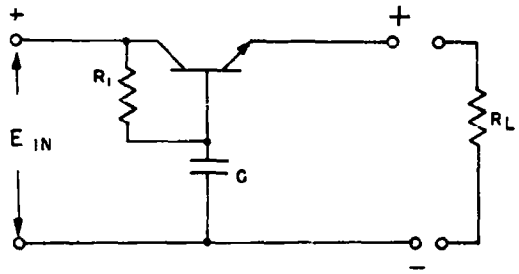

Figure 6.-Transistor-simulated series inductance.

B. Capacitance

The Miller integrator is a particular kind of operational amplifier. It is basically an amplifier stage with a capacitive feedback path from plate to grid. The apparent capacitance between grid and cathode terminals is a function of the size of the feedback capacitor and the gain of the stage. In effect, the plate-to-grid capacitance is amplified by the tube. Thus, it is possible to use a relatively small capacitance with a high gain stage to obtain a large circuit capacitance of low volume.

Stern[12] shows a circuit for a transistor-simulated shunt capacitance, and it is reproduced in Figure 7. The value of the capacitance used in the base path is multiplied by the transistor gain. As in the simulated inductance case, these circuits are inoperable above the transistor cut-off frequency. Oakes and Lawson[13] use a similar capacitance multiplier circuit in a transistor power supply filter.

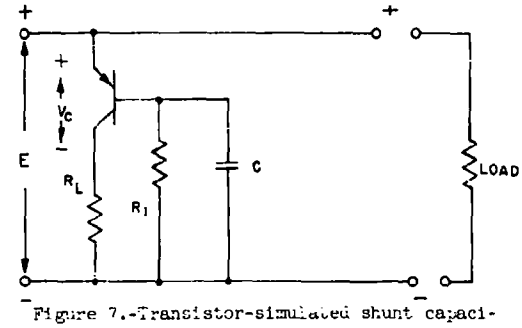

Figure 7.-Transistor-simulated shunt capacitance.

III. Filters and Oscillators

The usual inductance-capacitance filters and oscillators assume very large physical proportions when designed for low frequency operation. In addition, at sub-audio frequencies, the circuit Q of the inductors is so low that inductance-capacitance filters and oscillators are not practical. Both these factors have spurred circuit designers to develop alternative approaches.

It has been known for many years that certain resistance-capacitance networks exhibit some of the properties of resonance. That is, in the region of resonance, the phase shift changes quite rapidly with frequency, and the networks show a peak of transmission or attenuation. Some of the better known passive resonant networks are the Wien bridge, the parallel- or twin-T, and the bridged-T. Ladder networks (or cascaded L sections) as passive structures behave as low-pass or high-pass filters.

When these resistance-capacitance networks are used in the feedback loop of an amplifier, it is possible to achieve steeper curves of amplitude vs. frequency (higher Q) than the passive case, or even to invert the transmission characteristics of the network.

Resistance-capacitance oscillators are similar in theory. Sufficient in-phase feedback is employed to overcome the attenuation in the coupling network, and the amplifier then supplies its own input. The frequency stability, of course, is determined by the rate of change of phase with frequency at the resonant frequency of the network.

A. Ladder networks (cascaded L sections)

The simplest network to be considered here is the single L section, shown along with its transmission and phase characteristic in Figure 8.

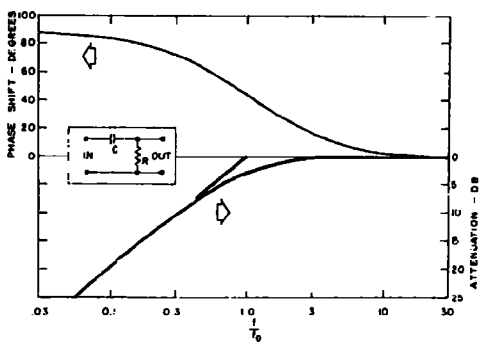

Figure 8a.-Single-section high-pass filter with attenuation and phase characteristics.

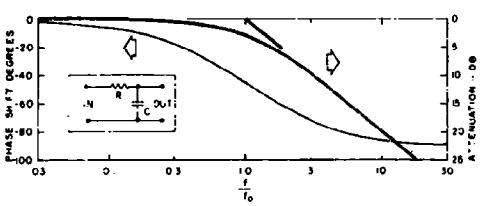

Figure 8b.-Single-section low-pass filter with attenuation and phase characteristics.

It has an attenuation asymptotic to 6 db/octave beyond the "corner" frequency of $\omega=1/RC$, and a maximum phase shift of 90°. Depending on the configuration, either low or high frequency attenuation may be obtained.

The attenuation rate of these networks may be made steeper by cascading two or more sections. For each section, an additional 6 db/octave slope, and 90° phase shift are obtained. Thus, for example, a three-section ladder has an attenuation of 18 db/octave beyond its corner frequency, and a maximum shift of 270°. One such network is shown with its characteristics in Figure 9.

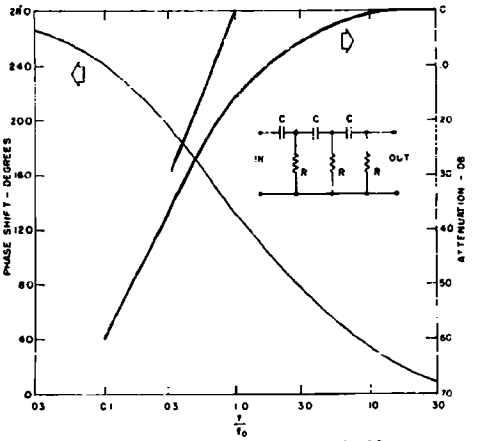

Figure 9.-Three-section high-pass ladder network with attenuation and phase characteristics.

It can be seen that there is a phase shift of 180° at a frequency $f=1/2\pi RC\sqrt{6}$ for this high pass filter. Although the three-section ladder network has no "resonant" frequency, it has been used in a tuned amplifier circuit by Hansel[14], and is commonly employed in resistance-capacitance (phase-shift) oscillators as described by Ginzton and Hollingsworth[15]. The network is connected in a negative feedback path between the input and output of an amplifier stage. At some frequency there is an additional 180° phase shift contributed by the network. Thus, positive feedback is obtained, and the amplifier response will show a peak at this frequency.

If the amplifier gain is made sufficiently large to overcome the attenuation in the network, the circuit will oscillate. For a network composed of equal resistances and equal capacitances, there is an attenuation of 29 at a phase shift of 180°, requiring a loop gain of at least this amount for the circuit to oscillate. Sulzer[16] suggests a modification of the ladder network by "tapering" the sections so that the succeeding sections do not load the input sections. The attenuation in this network is only about 8 for a phase shift of 180° and so low μ tubes may be used in the oscillator.

Hooper and Jackets[17] have reported on a transistorized RC phase shift oscillator.

Epstein[18] describes a variation of this ladder network which has a gain greater than unity with 130° phase shift. Thus it is possible to construct an oscillator with only a cathode follower as the active element. Waidelich[19] gives a practical design procedure for oscillators of this type.

Smiley[20] describes another variation of the phase shift oscillator in which the ladder sections are separated by active vacuum tube stages. Use is made of the Miller effect to increase the effective value of the capacitances in the network, permitting ultra-low-frequency operation with relatively small components. A further advantage of this oscillator is that three-phase output is available.

Sturm and Cottrell[21] developed a transistorized three-phase, phase shift oscillator in which the ladder sections are separated by active transistor stages.

Hadfield[22] describes a null network composed of two ladder networks connected to a common source. It is shown in Figure 10. The null frequency is controlled by means of a very high resistance potentiometer connected across the output terminals of the individual networks. One of these networks is a phase lead network; the other is a phase lag network. The voltages at the respective outputs of these networks are opposite in phase at all frequencies and a zero output or cancellation can be obtained at any frequency by a suitable setting of the potentiometer. A more detailed analysis is presented by Clothier[23] and a variation called the variable-T is discussed by Reid[24].

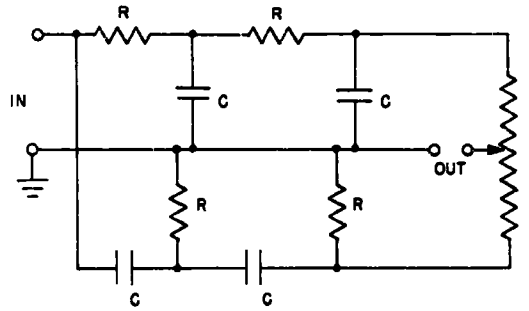

Figure 10.-Hadfield's null network.

B. The zero phase shift network

A simple selective network, sometimes referred to as a zero phase shift or twin RC network, and discussed in detail by Punnett[25], is shown in Figure 11 along with its phase and transmission characteristics. Superficially, it appears to be a Wien bridge, and it has been referred to as such many times in the literature. Actually it is not, since the true Wien bridge is a four-terminal network having no common connection between the input and output. This network is a three-terminal network and it has a common connection between input and output. It has a peak in transmission and 0° phase shift at its "resonant" frequency. Its attenuation is asymptotic to 6 db/octave each side of this frequency. If the general case for this network is considered, it is found that the highest selectivity occurs when m=n=2. The resonant frequency obeys the relation $f=1/2\pi RC$.

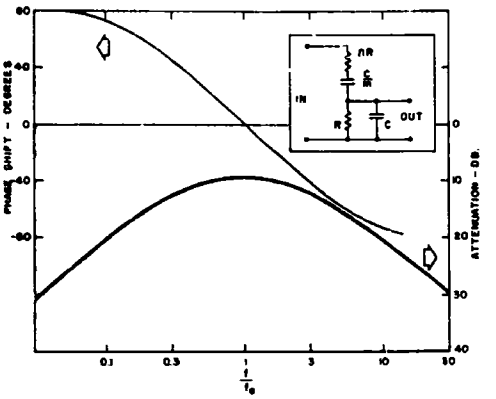

Figure 11.-The zero phase shift network with attenuation and phase characteristics.

Two other networks composed of the same basic elements in different configurations, but having the same tranamission characteristics are shown in Figure 12.

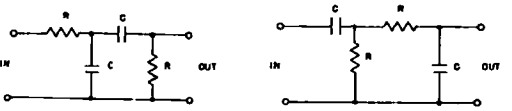

Figure 12.-Two variations of the zero phase shift network.

Whitmer[26] describes a three-stage, broadly tuned bandpass amplifier employing two of these networks for interstage coupling. While not as selective as other circuits, the simplicity of the network and the absence of critical tuning requirements are advantageous.

Beattie and Conn[27], and Punnett[25] employ this network as the interstage coupling in a two stage amplifier with a positive feedback loop, thereby obtaining a tuned amplifier system with Q's up to 20. Transistorized versions, while feasible, have not yet been described in the literature.

If the loop gain of the amplifier system is made greater than 3, the circuit will oscillate at a frequency determined by the network and the amplifier phase shifts. Such a vacuum tube oscillator has been described by Terman[28]. Transistor oscillators of this type have been described and analyzed by Achuthan[29] and Hooper and Jackets[17].

Another variation of this network is also described by Punnett[25] and consists of connecting the network to the output of a phase splitter. The operation approaches that of the Wien bridge by being more sharply tuned than the simple selective network and having zero output at its resonant frequency.

C. The Wien bridge

A popular tuned RC network, the Wien bridge, is

shown in Figure 13 along with its transmission characteristics. It is more sharply tuned than the previous network, with a theoretical infinite attenuation and a discontinuous phase shift at its resonant frequency. It has been employed in tuned amplifiers by Shaw[30] and in oscillators by Clarke[31]. It has a rather serious disadvantage in that it is a four-terminal network having no common connection between input and output, thus requiring an isolating transformer in many oscillator and amplifier circuits. However, it is possible to employ this network without a transformer. The network may be tuned by varying either the two capacitors or the two resistors in the right-hand branches simultaneously. The resonant frequency obeys the relation $f=1/2\pi RC$.

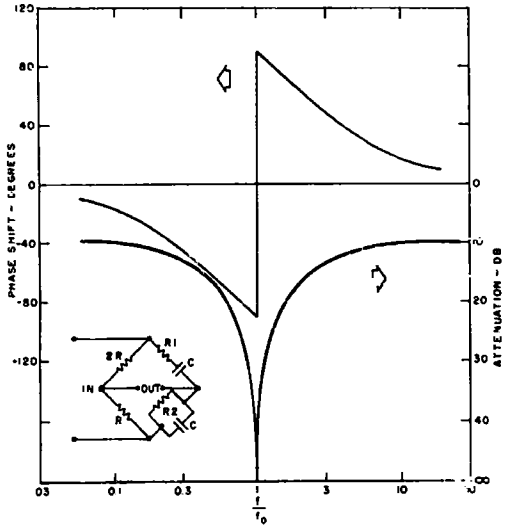

Figure 13.-The Wien bridge network with attenuation and phase characteristics.

D. The parallel-T network

Probably the most widely used RC selective network is the parallel-T or twin-T network. It has a higher Q than the previously discussed simple networks, less than the Wien bridge, and has a theoretical infinite attenuation and a discontinuous phase shift at its resonant frequency. A carefully constructed unit can have an attenuation of 120 db at this frequency. This network, invented by Augustadt[32], is shown in Figure 14 along with its transmission characteristics. The resonant frequency is given by $f=1/2\pi RC\sqrt{2n}$ where, for the highest Q, $n=1/2$.

The parallel-T is a three-terminal network; there is a common connection between input and output. This feature makes the applications rather straightforward since no isolation transformer or special circuitry is required. Analysis of the parallel-T network and suggested applications have been made by Hastings[33] and Stanton[34].

One of the sharpest criticisms directed toward the parallel-T network is the fact that in order

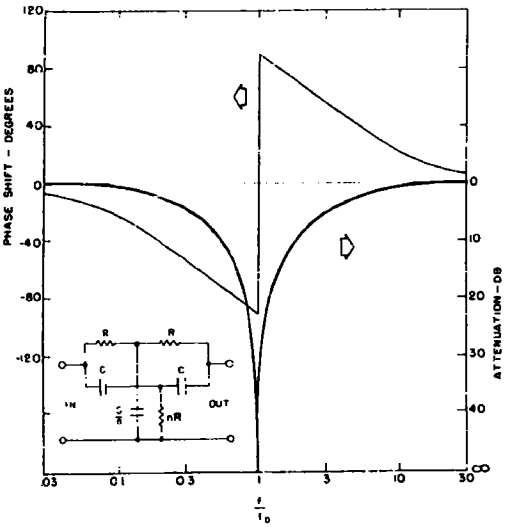

Figure 14.-The parallel-T network with attenuation and phase characteristics.

to vary the tuning frequency, three circuit parameters must be adjusted simultaneously and with perfect tracking to maintain the sharpness of rejection. White and Morgan[35] have made an ingenious modification that permits adjustment of the null frequency over a two-decade range without changing any of the circuit parameters. They split the input to the parallel-T, and in the case illustrated in Figure 15, each T is fed from one section of a dual potentiometer. The null frequency is then only a function of the ratio of the voltages applied to the two T's and the null frequency of the basic network.

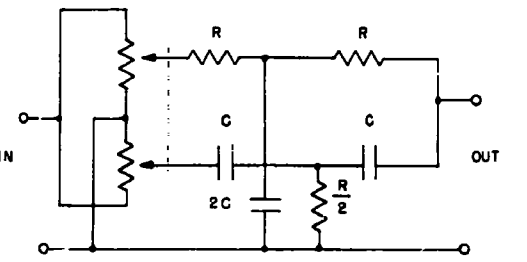

Figure 15.-The dual-input parallel-T network

The use of the parallel-T network in vacuum tube tuned amplifiers was first described by Scott[36], but subsequent articles by Fleisher[37], Punnett[25], Stanton[34], and Hyde[38] are more detailed. The tuned amplifier consists basically of a stage of gain with the parallel-T network in the negative feedback loop, and is shown in Figure 16. There is degeneration at all frequencies except at the resonant frequency of the network which is a transmission null. At this frequency,

the amplifier gain is a maximum, resulting in a peak in the amplifier response. Among the articles showing practical circuits of tuned amplifiers employing this network are those by Dixon and Phillips[39], Gitzendanner[40], Rayner[41], and Roualt[42].

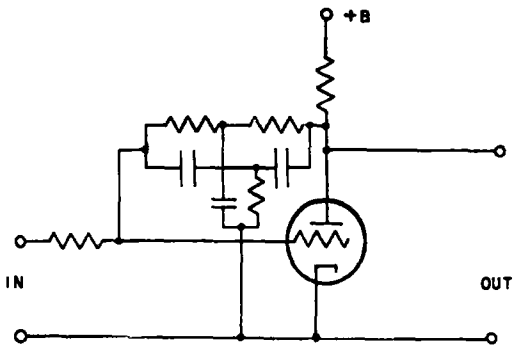

Figure 16.-A simple tuned amplifier employing a parallel-T network in the negative feedback loop.

Bowers[43] calls attention to an interesting variation of the parallel-T network. If the multiplying factor, n, of the shunt arms of the network is less than 0.5, there is only a partial null and the network phase shift attains a value of 180° at the resonant frequency. The phase vs. frequency characteristic is degraded from the discontinuous function of the infinite attenuation network to a less rapid change, the slope becoming smaller as n is decreased. Attenuation and phase shift for various values of n are shown in Figure 17. In the previously described amplifier, this phenomenon results in positive feedback or regeneration at the resonant frequency of the filter, thus increasing the amplifier gain at that frequency. Bowers[43], McGaughan[44], and Smith[45] have shown practical tuned amplifiers based on these principles. A similar circuit, but using transistors, is described by Sohrabji[46].

If the loop gain of the amplifier is made large enough to overcome the transmission losses of the network, the system will oscillate at a frequency determined by the network and the phase shift in the amplifier. The choice of n of the network is dictated by the open loop gain of the oscillator and the frequency stability that is desired. Vacuum tube oscillators of this type have been described by Smith[45] and Tucker[47]. A complete design procedure for parallel-T oscillators is given by Lynch and Robertson[48]. A transistor version is shown by Sohrabji[46].

Frequency discriminators utilizing parallel-T RC networks are advantageous for low frequency applications. There are two basic methods: two networks may be used directly, or in the inverse loops of feedback amplifiers. Tillman[49] and Stine[50] describe practical circuits and design techniques for these discriminators.

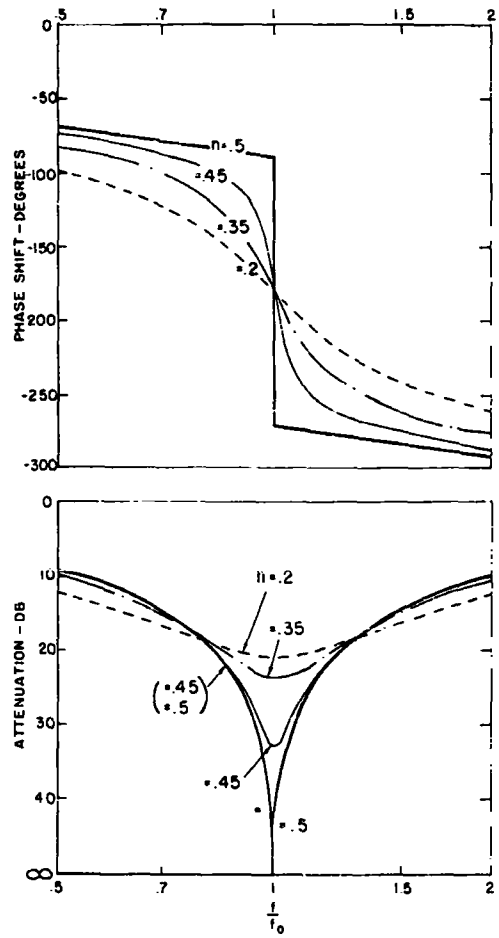

Figure 17.-Attenuation and phase characteristics of a parallel-T network with various values of n.

E. The bridged-T network

Still another frequency selective RC network is the bridged-T, described by Sulzer[51] and others. The network and its transmission and phase characteristics are shown in Figure 18. It has a minimum of transmission and 0° phase shift at its resonant frequency, $f=1/2\pi RC$. The unsymmetrical networks are characterized by a higher Q than is available from other networks containing only four components. Its relative simplicity and ease of frequency adjustment also make this network attractive for use in a tuned amplifier or oscillator.

Tisdale[52] used the bridged-T network in conjunction with RC ladder sections to obtain a continuously adjustable low-pass filter. Sulzer has used this network in a vacuum tube[53] and a transistor[54] audio oscillator which feature low harmonic distortion.

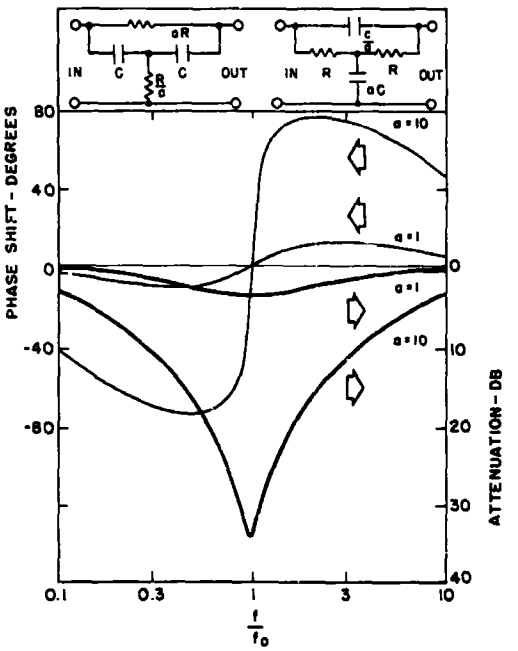

Figure 18.-The bridged-T network with attenuation and phase characteristics.

CONCLUSIONS AND RECOMMENDATIONS

The use of positive feedback techniques offers a means to eliminate large volume by-pass capacitors in amplifier circuits, although the amplifier gain is made more sensitive to power supply and temperature variations.

Direct coupling and complementary symmetry transistor circuits can be employed to eliminate some coupling capacitors and resistors. However, direct coupled circuits should be restricted to small signal applications since drift may cause the amplifier to operate in a non-linear region thus introducing distortion. Here, again, temperature variations will cause drift in transistor amplifiers.

Simulated reactances permit the substitution of small volume active networks for the larger passive components ordinarily used in power supply filters.

Resistance-capacitance networks can be used in place of the simpler but bulkier inductance-capacitance filters, especially at the low audio and sub-audio frequency ranges. Passive ladder networks can be used for low- or high-pass filters. Of the networks considered here, only one type, the zero phase shift network, exhibits a peak in transmission at its resonant frequency. Because of its simplicity and absence of critical adjustment, this network is suited for printed circuits. Minor frequency adjustments can be made by varying one of the resistance elements. It is especially suited for interstage couplings since no additional d.c. blocking capacitors are required.

The remaining applications for R-C networks as filters involve their use in feedback amplifiers. For maximum stability of operation, the network is placed in the negative feedback loop thus reducing the amplifier gain at all frequencies removed from the minimum transmission frequency of the filter. There are four minimum or null transmission networks which have been considered here: Hadfield's ladder network, the Wien bridge, the bridged-T, and the parallel-T. The first two are more complicated circuitwise or possess more elements than the latter two, while offering no compensating advantages. The R-C bridged-T is appealing because of its simplicity, but Brown[55] comments that its amplitude rejection characteristic is poorer than that of the parallel-T network and is, therefore, less desirable for use in a tuned amplifier.

The most versatile (and hence most popular) network is the parallel-T and its modifications. While the basic infinite attenuation network is rather difficult to adjust for optimum rejection at a particular frequency, the variation suggested by White and Morgan[38] nullifies the criticism directed toward the network for variable frequency operation. This variation makes it possible to have operation over a two-decade range without any additional critical adjustments to the network. Another variation of the parallel-T yields a positive feedback voltage at the resonant frequency. Thus additional gain might be obtained from a tuned amplifier, and a stable R-C oscillator is easily obtained by the proper choice of network parameters.

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THE DESIGN OF A TRANSISTOR NOR CIRCUIT FOR MINIMUM POWER DISSIPATION

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Abstract

This paper describes a method of designing a transistor NOR circuit for minimum power dissipation ($I_C^2R_C$). Expressions for collector current (I_C) and input current limiting resistor (R_1) which give a minimum in power dissipation are derived in terms of the basic NOR circuit parameters (B/S, I_{CBO}, M, and N). Graphical results indicating minimum power dissipation as a function of leakage current (I_{CBO}), minimum base to collector current gain (B/S) and number of output circuits (N) are presented. The number of inputs (M) is fixed at two for these curves.

Introduction

The transistor NOR circuit is capable of performing all of the English logic functions AND, OR, and NOT, and is therefore extremely useful in computer systems. The NOT function is performed by a NOR with one input. The AND function is performed by three NOR circuits and the OR function is performed by two NOR circuits as shown in Figure 1.

The basic building block, the transistor NOR circuit as shown in Figure 2, employs a junction transistor in the common emitter configuration. The transistor is used as a two-position switch rather than as a linear device. In other words, the transistor can exist in its normal "cut-off" state or in a state of saturation which can be referred to as an "on" state. In the "cut-off" state the transistor will have a relatively high impedance between its collector and emitter in the order of megohms. In the saturated state the transistor has a negligible impedance between its collector and emitter; this impedance is in the order of ohms.

Referring to Figure 2, the circuit consists of M input lines with input resistors R_1 and a base bias resistor R_T. The positive bias V_{BB} supplied through R_T causes the transistor to be turned off and thereby to exist in the "cut-off" state if all of the inputs (A, B, and C) are near zero volts. The transistor is turned "on" if one or more of the inputs (A, B, C) are at a negative voltage V_C. V_C must be sufficiently large such that the current I_B flowing through resistor R_1 is equal to or greater than I_C/B, where B is the base to collector short circuited current gain, and I_C is the maximum current flowing in the collector resistor R_C.

$$I_C = \frac{V_{CC}}{R_C}$$

When the transistor is in the "cut-off" state the output voltage is approximately the same as the supply voltage V_{CC}. When the transistor is in the saturated state most of the collector supply voltage V_{CC} appears across R_C and the output is near ground potential. It can be stated concisely that a voltage signal is present on the output if voltage signals are not present on any of the inputs. Conversely, a voltage signal is not present on the output if voltage signals are present on any or all of the inputs.

A basic question encountered in using the NOR circuit is "will the circuit operate properly when a single collector is required to drive a certain desired number of output circuits?" An expression for this number of outputs, N, in terms of the circuit components, was derived by W. D. Rowe.[1]

$$(1)\quad N = I_C \frac{1}{SI_B + I_{CBO} + \frac{0.25(M-1)}{R_1}} + \frac{R_1}{V_{CC}}$$

where I_{CBO} is the maximum expected base to collector leakage current with the emitter open circuited, 0.25 is the base to emitter voltage for germanium transistors, and S is the safety factor employed to compensate for a decrease in gain of the transistor and other circuit parameter tolerances. This expression will be used as a starting point. In deriving the above expression, it was assumed that V_{BE}, the base to emitter voltage when the transistor is in the "on" state, was very much smaller than V_{CC}, the collector supply voltage and that the leakage current I_{CBO} was very much smaller than I_C, the maximum current flowing in the collector resistor. It was also assumed that the transistor acts as a perfect switch when the transistor is in the saturated state. Consequently, under saturated conditions $-V_{CC} = I_CR_C$. All results will be based on these assumptions.

Given a certain number of inputs to a NOR circuit which is to drive a certain number of output circuits, it is desired to minimize the power dissipation $I_C^2R_C$ in the collector resistor R_C, subject to the restriction that equation (1) be satisfied. The minimization of $I_C^2R_C$ with respect to base resistor, R_1, and collector current I_C, is the object of this paper.

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Derivation of Minimum Power Dissipation Expression

A. Input Current Limiting Resistor (R_1)

Equation (1) may be rewritten in the form

$$(2)\quad R_C = \frac{R_1}{\dfrac{1}{\dfrac{S}{B} + \dfrac{I_{CBO}}{I_C} + \dfrac{0.25(M-1)}{R_1 I_C}} - N}$$

If this expression is differentiated with respect to R_1, maintaining S/B, I_{CBO}, M, N, and I_C constant, and the derivative set equal to zero, one obtains

$$\frac{1}{R_1+NR_C} - \frac{1}{R_1} = \frac{\left(\frac{S}{B}\right)I_C + I_{CBO}}{\left[\left(\frac{S}{B}\right)I_C+I_{CBO}\right]R_1 + 0.25(M-1)}$$

Solving this equation for R_1 gives

$$(3)\quad R_1^* = \frac{0.25(M-1)}{I_C\left\{\pm\sqrt{\frac{1}{N}\left(\frac{I_{CBO}}{I_C}+\frac{S}{B}\right)} - \left[\frac{I_{CBO}}{I_C}+\frac{S}{B}\right]\right\}}$$

R_1^* is the expression for the input-current limiting resistor which gives a minimum in R_C and also a minimum in power dissipation ($I_C^2R_C$), if such a minimum exists. The expression for power dissipation is obtained by multiplying equation (2) by I_C^2. Therefore

$$(4)\quad I_C^2R_C = \frac{I_C^2R_1}{\dfrac{1}{\dfrac{S}{B} + \dfrac{I_{CBO}}{I_C} + \dfrac{0.25(M-1)}{R_1 I_C}} - N}$$

B. Collector Current(I_C)

Substituting equation (3) into (4) gives

$$(4a)\quad I_C^2R_C = I_C^2\left[\frac{0.25(M-1)}{I_C\left\{\pm\sqrt{\frac{1}{N}\left(\frac{I_{CBO}}{I_C}+\frac{S}{B}\right)} - \left[\frac{I_{CBO}}{I_C}+\frac{S}{B}\right]\right\}}\right] \Bigg/ \frac{1}{\dfrac{S}{B} + \dfrac{I_{CBO}}{I_C} + \dfrac{0.25(M-1)}{\left\{\pm\sqrt{\frac{1}{N}\left(\frac{I_{CBO}}{I_C}+\frac{S}{B}\right)} - \left[\frac{I_{CBO}}{I_C}+\frac{S}{B}\right]\right\}0.25(M-1)}} - N$$

Differentiating this expression with respect to I_C, maintaining S/B, I_{CBO}, M and N constant, setting the derivative equal to zero and solving for I_C, the following is obtained.

$$(5)\quad I_C^* = \frac{I_{CBO}\left(-1 + 4N\frac{S}{B} + \sqrt{1+8N\frac{S}{B}}\right)}{2\left[\frac{S}{B} - N\left(\frac{S}{B}\right)^2\right]}$$

I_C^* is the expression for the collector current which gives a minimum in power dissipation. Minimum power dissipation will be designated as $(I_C^2R_C)^*$.

When (5) is substituted into (3) R_1^* reduces to

$$(6)\quad R_1^* = \frac{0.25(M-1)}{I_{CBO}}$$

The expressions (5) and (6) for the collector current (I_C^*) and the input-current limiting resistor (R_1^*) when substituted in equation (4)(power dissipation) give a minimum in power dissipation($I_C^2R_C$)*.

Relationship of Minimum Power Dissipation to Variables

Using the derived expressions for R_1^* and I_C^* a program of moderate complexity was devised for the IBM 704 Computer to calculate minimum power dissipation as a function of I_{CBO} (base to collector leakage current), B/S (Base to collector current gain with safety factor), M (number of input circuits), and N (number of output circuits). The computed values provide sufficient data for the creation of informative graphical results.

Referring to Figure 3, it is seen that minimum power dissipation decreases with a decrease in the number of output circuits. The minimum power dissipation decreases with an increase in B/S, and this decrease approaches a limit as B/S becomes infinite. Using the expressions for I_C^* and $I_C^2R_C$, one can calculate:

$$\text{Lim}\ (I_C^2R_C)^* = 4N(M-1)I_{CBO}$$

$$B/S \rightarrow \infty$$

It is also interesting to note that as N decreases to 1, B/S becomes decreasingly significant in the determination of minimum power dissipation.

Referring to Figure 4, one can see that I_C^* (the collector current which gives a minimum in power dissipation) also decreases with a decrease in the number of output circuits. I_C^* decreases with an increase in B/S and this decrease approaches a limit as B/S becomes infinite. One can calculate this limit to be:

$$\text{Lim } I_C^* = 4N\, I_{CBO}$$

$$B/S \longrightarrow \infty$$

Again it is interesting to note that as N decreases to 1, B/S becomes decreasingly significant in the determiniation of the collector current which gives a minimum in power dissipation.

From the equation (5), it is readily observed that I_C^* is linearly related to I_{CBO}:

$$I_C^* = K_1 I_{CBO} \text{ where } K_1 = f(N, S/B)$$

Using this fact along with equation (6), it can also be determined that minimum power dissipation is linearly related to I_{CBO} and $0.25(M-1)$:

$$(I_C^2 R_C)^* = K_2 0.25(M-1) I_{CBO}$$

where $K_2 = F(N, S/B)$

Then the collector resistor

$$R_C = \frac{K_2\ 0.25\ (M-1)\ I_{CBO}}{I_C^2}$$

$$= \frac{\left(I_C^2 R_C\right)^*}{(I_C^*)^2}$$

$$= \frac{K_2}{K_1^2} \times \frac{0.25(M-1)}{I_{CBO}}$$

The collector supply voltage:

$$V_{CC} = I_C R_C$$

therefore

$$V_{CC} = K_1 I_{CBO} \times \frac{K_2}{K_1^2} \times \frac{0.25(M-1)}{I_{CBO}}$$

or simply

$$V_{CC} = \frac{K_2}{K_1} \times 0.25(M-1)$$

Typical Design of NOR Circuit For Minimum Power Dissipation

The information given in the previous section may be correlated and used to design a NOR circuit for minimum power dissipation. Specifically if a transistor NOR circuit is to have two inputs (M = 2), drive nine circuits (N = 9), employ transistors with Betas of 50 (B = 50), and I_{CBO}'s of 10^{-6} amperes, correct values of V_{CC}, R_C, I_C and R_1 can be ascertained to effect minimum power dissipation. For this particular design situation a safety factor of 2 is employed. The B/S factor is therefore 25. The values of I_{CBO}, B, and M used in this typical example were chosen because of their practicability to current design situations. The value of N was chosen because the assumptions made in the Introduction are less valid for lower values of N.

If expressions (5) for I_C^* and (6) for R_1^* along with the above values for I_{CBO}, B/S, M and N are substituted in the power dissipation expression (4) a minimum value of power dissipation can be determined. The calculations yield

$$R_1^* = \frac{0.25(M-1)}{I_{CBO}} = .25 \times 10^6 \text{ ohms} = 250K$$

and

$$I_C^* = .047 \times 10^{-3} \text{ amperes} = 47\ \mu a$$

Therefore minimum power dissipation using eq.(4)

$$(I_C^2 R_C)^* = .177 \times 10^{-3} \text{ watts} = 177\ \mu \text{ watts}$$

The collector supply is then calculated to be

$$V_{CC} = \frac{I_C^2 R_C}{I_C} = \frac{.177 \times 10^{-3} \text{ watts}}{.047 \times 10^{-3} \text{ amperes}} = 3.75 \text{ V}$$

Consequently

$$R_C = \frac{V_{CC}}{I_C} = \frac{3.75 \text{ V}}{.047 \times 10^{-3} \text{ amperes}} = 79K$$

To show that expression (1) is satisfied for this design, the specified values are substituted into (1). This substitution yields the necessary equality. Therefore, the design is valid for satisfactory circuit operation.

As was mentioned in the Introduction, it was assumed in deriving expression (1) that $V_{BE} \ll V_{CC}$ and that $I_{CBO} \ll I_C$. However, if these assumptions are not made, then equation (1) becomes

$$(7)\quad N = \frac{\left[-\left(\frac{V_{CC} - V_{BE}}{R_C}\right) - I_{CBO}\right]}{\left[SI_B + I_{CBO} + \frac{0.25(M-1)}{R_1}\right]} - \frac{R_1}{R_C}$$

Then if the specified values used in the above typical example are substituted in (7) it is

found that the number of suceeding NOR circuits that can be driven by a NOR circuit is eight as opposed to the nine outputs that was desired. Therefore, this error can be compensated for by designing for an N greater than the actual desired N.

Conclusion

For $V_{BE} \ll V_{CC}$ and for $I_{CBO} \ll I_C$ expressions were derived for the input current limiting resistor (R_1*) and for the maximum current flowing in the collector resistor (I_C*) which give a minimum in power dissipation. It was shown that a minimum in power dissipation does exist. However, when the base voltage (V_{BE}) is not very much smaller than the transistor collector bias (V_{CC}) and the leakage current is not very much smaller than the maximum current flowing in the collector resistor, the expressions for R_1* and I_C* are not completely valid, particularly when a NOR circuit design employs a small number of output circuits and when high Beta transistors are being used. Future study will be conducted relative to designing a NOR circuit for minimum power dissipation when V_{BE} is not $\ll V_{CC}$ and I_{CBO} is not $\ll I_C$.

Acknowledgment

The author wishes to thank Mr. T. A. Prugh and Mr. P. Emile for their guidance in the preparation of this report.

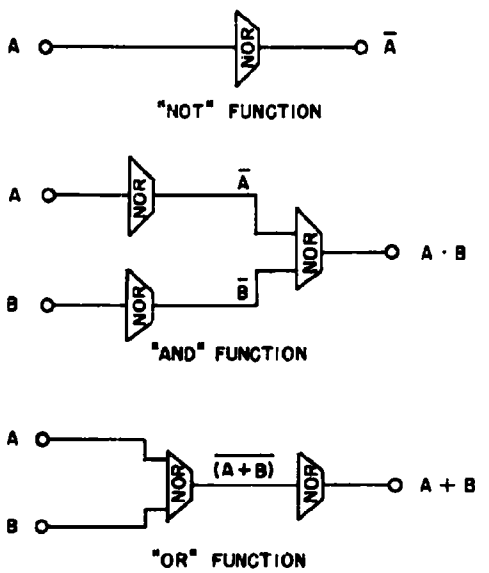

Figure 1 English Logic Functions By NOR Circuits

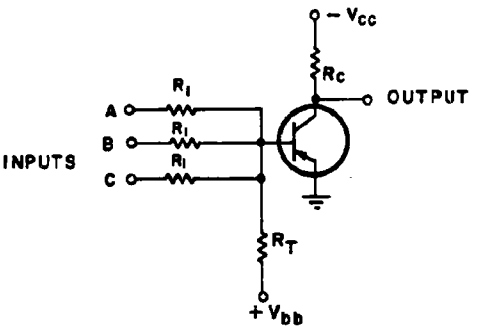

Figure 2 Basic Building Block NOR Circuit

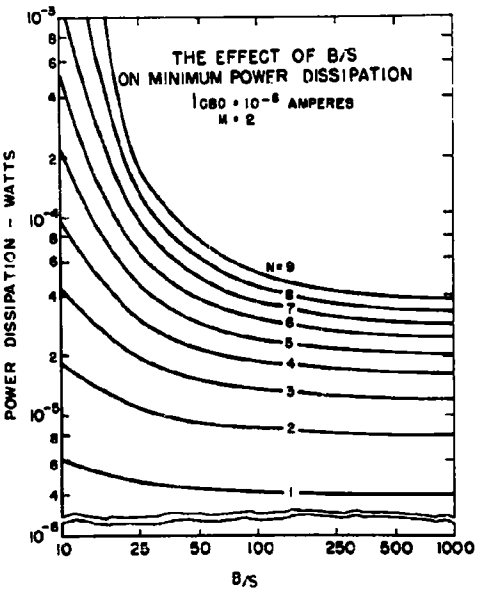

Figure 3 The Effect of B/S on Minimum Power Dissipation

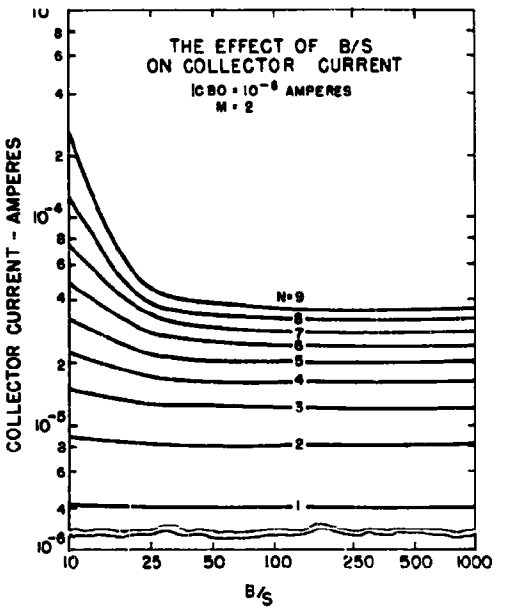

Figure 4 The Effect of B/S on Collector Current

FINE-LINE ETCHED WIRING

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In order to facilitate the interconnection of microminiature components and sub-assemblies, an investigation was made of techniques for producing fine-line conductors. By careful control of certain of the variables present in the normal photo resist and etching process, a pattern consisting of 2.5-mil-wide lines with 2.5-mil-wide spacings between the lines was successfully reproduced on copper-clad laminates although undercutting of the 1.35-mil-thick copper reduced the line width to about one mil.

As a corollary to the above work, copper films, 0.3 to 0.6 mil in thickness, were chemically deposited on plastic, and lines as narrow as 2.5 mils, with 2.5-mil-wide spacings between them, were etched in these films with negligible undercutting and without breaks or bridges.

Conductors 10 mils in width but having 4-mil-wide spacing had been produced previously by electroetching precious metals deposited on glass. An electroetching technique was necessary because chemical etching of precious metals would require the use of strong acids which would degrade the photo resist.

Need for still finer line etched wiring is not anticipated but techniques for producing fine-line printed wiring by "silk"-screening need to be developed.

INTRODUCTION

The recent emphasis on the microminiature packaging of electronic circuits has necessitated a reevaluation of current processing techniques to determine their limitations and capabilities.

A typical etched circuit board bears copper conductors which vary in width from 30 to over 60 mils with a minimum spacing between conductors of about 30 mils. In low-power, low-voltage circuits, however, these "minimum" widths can undergo appreciable reduction without impairing the operation of the assembled circuit. With such a reduction, techniques for preparing the conductor become critical.

In a recent article, Overas[1] reported the results of a survey to determine the capability of the printed circuit industry to produce fine-line conductors with fine-line inter-conductor spacings. The narrowest line and spacing used were 0.2 mm (7.8 mils) in width. The general conclusion of the survey was that the photo engraving process is capable of producing such small elements but that the majority of the commercial fabricators do not exercise sufficient process control to produce them.

About a year ago, a need arose in these Laboratories for a method of preparing fine-line conductors from a precious metal which had been vacuum deposited on a glass insulator. An electroetching procedure was developed. The particular pattern that was required, and which was reproduced, comprised a 10-mil-wide conductor having 4-mil-wide spacings. Because of this work it was believed that it should be possible to chemically etch at least as fine lines in copper.

Work was then instituted to determine: (1) how fine a line could be resolved and chemically etched in copper, and (2) which processing variables had the greatest effect on the final results. This recent work was divided into two parts: (1) chemical etching of copper-clad laminates, and (2) chemical etching of chemically deposited copper. The results of this work are given herein, together with a description of the earlier work on electroetching of a precious metal on a glass insulator.

The photo resist processes used in this work deviated only slightly from the normal techniques[2] used in the printed circuit industry. The methods used for the chemical etching of copper were also based on normal industrial procedures[3,4]. The etchant used for the electroetching of precious metals was derived from a publication[5] on stripping metallic coatings but, as indicated above, the electroetching procedure itself was developed in these Laboratories.

EXPERIMENTAL METHODS

A. Preparation of Test Patterns

1. For recent work on copper.

The original layout for the test pattern was made on a sheet of stiff white Bristol board of area 23 x 39 inches. Thirty-six strips of black adhesive tape 0.25 inch in width were laid down on this board in parallel strips 0.25 inch apart, and selected ends were connected so as to form two adjacent continuous lines which zig-zagged back and forth across the length of the board.

The outside line was 664.25 inches long while the inside one was 661.75 inches long; hence, for the two 0.25-inch-wide lines, the length-to-width ratios were respectively: 2657:1 and 2647:1.

The final layout was then photographed and reduced 25, 50, and 100 times to give negatives

having equal line-and-space widths of, respectively, 10 mils, 5 mils and 2.5 mils. The three patterns are shown in Figure 1.

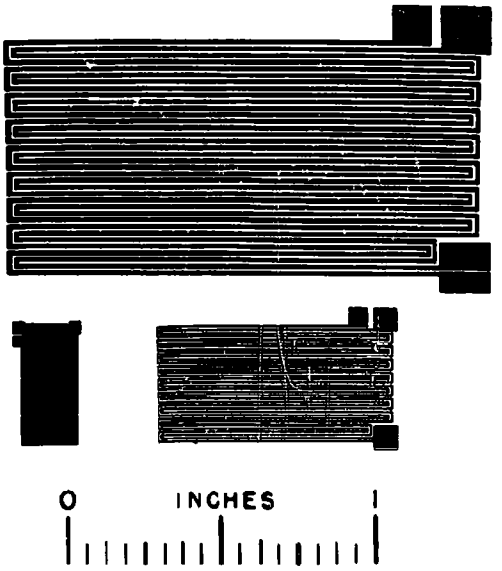


Figure 1. Test patterns for fine-line etching: top, 10-mil-wide lines with 10-mil-wide spacings; lower right, 5-mil-wide lines with 5-mil-wide spacings; lower left, 2.5-mil-wide-lines with 2.5-mil-wide spacings.

Since the length-to-width ratios for each of the two lines remained constant, regardless of the size of the pattern, the resistance of the two lines also remained constant and it was possible to compare etching results directly by use of the following formula:

$$R = \frac{\rho L}{WT}$$

where R = resistance, ρ = resistivity, and L, W, and T are the size parameters of the conductor.

For example, for patterns etched in "1-oz" copper-clad laminates, the following values were substituted in the above equation: $\rho = 1.724 \mu\Omega$-cm (for copper), T = 1.35 mils (for "1-oz" copper-clad laminates), and the appropriate length and width of the lines of one of the patterns. Then the theoretical resistance, R, was calculated to be 1.336 Ω for the outside line of the pattern and 1.331 Ω for the shorter inside line; and, for copper films only 0.45 mil in thickness, the respective values were calculated to be 4.008 Ω and 3.993 Ω.

2. For earlier work on precious metals.

The pattern used in this work had been specified beforehand and had been made by milling a rigid five-ply black-and-white-layered plastic laminate through the black surface to the first white ply beneath it. The laminate was about 12 inches long by about 2 inches wide and the white line milled into it was designed to produce two separate electrodes in somewhat the configuration of two black combs laid down in the same plane with their teeth interlocked. The line was bent 180° at 7/16-inch-long intervals to form the teeth of the pattern. After milling the pattern into the laminate, it was photographed and reduced to give a pattern about the size of the normal glass slide employed in light microscopy (see Fig. 2). In the negative of

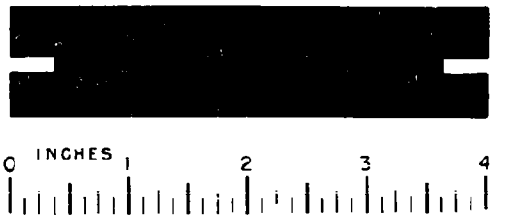


Figure 2. Pattern for fine-line etching: 10-mil-wide lines with 4-mil-wide spacings

this pattern, the single black line was 4 mils in width and the transparent gaps were 10 mils in width.

B. Fine Lines Produced by Chemical Etching of Copper-clad Laminates.

1. Cleaning specimens of copper-clad laminate.

Squares approximately 1.75 x 1.75 inches in area were cut from commercial 1/32-inch-thick epoxy-glass-cloth laminate clad with "1-oz" copper (1.35 mils in thickness). Any squares which had visible scratches, pits, or other defects, were discarded. The squares were degreased in the vapors of boiling trichloroethylene, dipped for five seconds in a 10% solution of hydrochloric acid to remove oxides, washed, and dried.

2. Application of resist to laminates.

Throughout all of this work every effort was made to keep the laminates and negatives as free of dust as possible, particularly when the laminates were coated with wet resist or when the dried resist was being exposed to light through the negative. The resist itself was a commercial solution which was filtered prior to use to remove any sediment or other foreign matter.

The arms of the turntable shown in Figure 3 were covered with two-sided adhesive tape, the squares of laminate were laid on the arms, and resist was poured over the top surface of each

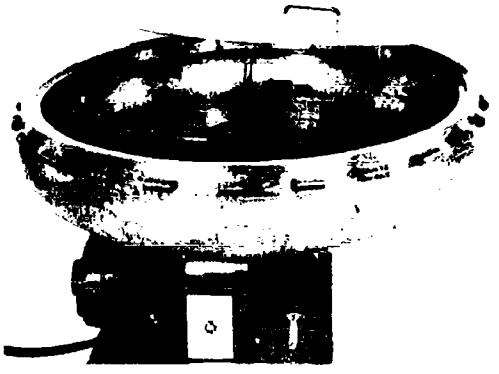


Figure 3. Variable-speed whirler for application of thin films of resist to surfaces of laminates.

piece of laminate. The cover was put on the whirler and the arms were whirled for 2 minutes at room temperature and at speeds of 50, 100, or 200 rpm. The speed of the turntable was then brought to 200 rpm and an infrared lamp was trained on the whirling arms for an additional 3 minutes, at which time the coated surfaces were dry.

Other similar squares of laminate were dipped in resist, allowed to drain in the dark for 2 minutes at room temperature, and then dried in an oven at 60°C for 3 minutes. Two ovens were used; one was a mechanical convection-type yielding circulating air and the other was the more conventional gravity convection-type yielding relatively still air.

3. Exposure of sensitized laminates.

The negative was laid on the glass plate of the commercial vacuum-frame-type printer, as shown in Figure 4, with the emulsion side up. The dried sensitized test plates were then laid on the negative with the resist-coated side against the negative. In this position, the negative-laminate assembly was located about 12 inches above the carbon arc lamp shown in the bottom of the printer. The hinged lid was closed, the space between the lid and the glass was evacuated, the arc was struck, and the specimens were exposed to the carbon arc for 1 minute.

In order to compare the resolution to be obtained when contact between negative and resist-coated laminate is made by vacuum, as described above, with the resolution to be obtained when only contact pressure is applied, two plates which had been dip coated and dried in the gravity-convection-type oven were covered with negatives and placed negative side down as before on the glass of the vacuum frame directly above the carbon arc lamp. Instead of closing the frame and evacuating the enclosure, however, a sheet of glass was placed over the pieces of laminate and weighted with two one-kilogram weights. Then the pieces were exposed to the arc for one minute.

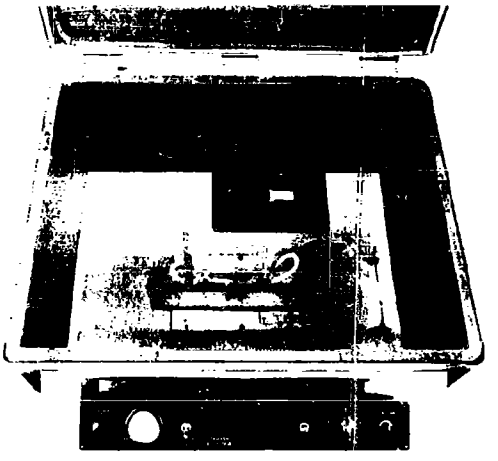


Figure 4. Commercial vacuum-frame-type printer showing carbon arc in bottom of printer and a negative of one of the test patterns positioned on top of glass of frame.

4. Development of pattern on laminates.

The pieces described above were developed by suspending them in the vapors of boiling trichloroethylene. From 0.75 to one minute was required to remove all of the unexposed resist and produce a sharply defined pattern. The developed plates were then heated for 5 minutes at 60°C.

Additional pieces of laminate which had been dip-coated with resist, dried in the gravity-convection-type oven, and exposed for one minute in the vacuum frame were used to test two developers in the liquid state. The pieces were immersed in the liquid at room temperature for the lengths of time shown in Table I. The

Table I.- Developers tested

Developer	Time applied, minutes
Trichloroethylene vapor	1
Trichloroethylene vapor	2
Trichloroethylene liquid	1
Trichloroethylene liquid	2
Commercial liquid supplied for the commercial resist employed	2

developers were agitated by rocking the containers. The units so developed were then rinsed in running water and dried for 5 minutes at 60°C.

Some additional plates were developed in the vapors of boiling trichloroethylene but were not heated prior to etching.

5. Etching of pattern on laminates.

A 25% solution of ammonium persulfate was prepared and warmed to about 70°C. The warm solution was placed in a small bubble etcher which consisted of a water-jacketed glass funnel having a fritted glass bottom (see Figure 5). Hot water was circulated through the jacket and a stream of air was passed up through the fritted glass by means of an air line connected to the bottom outlet of the funnel. The flow of air was regulated to provide continuous bubbling over the entire surface of the etchant.

The pieces of laminate were dropped into the etcher pattern-side down and were held suspended on the surface of the liquid by the force of the bubbling action. The unwanted copper was etched away in 1.5 to 2 minutes.

After the pieces were etched, they were washed in running water and allowed to dry without wiping or blotting so that the resist on the copper pattern was undisturbed.

6. Testing of pattern on laminates.

The width of the lines of patterns developed in the vapors of trichloroethylene was measured with a microscope equipped with a micrometer eyepiece. The resist was removed from the terminal points and measurements of the resistance of the copper lines were then made on a digital ohmmeter; results are given in Tables II and III.

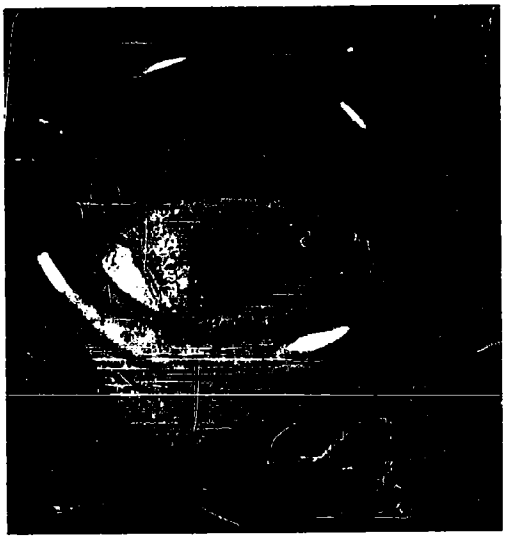


Figure 5. Bubble etcher comprising a water-jacketed glass funnel containing a fritted glass bottom up through which compressed air is forced.

Table II.-Effect of variations in the method of applying, drying and exposing the resist upon the average resistance of conductors etched on copper-clad laminates.

Variation in treatment of resist	Average resistance, ohms					
	Line width, mils					
	10(a)	10(b)	5(a)	5(b)	2.5(a)	2.5(b)
1. Whirler coating at designated rpm						
50	1.7	1.7	1.9	1.9	(c)	(c)
100	1.6	1.6	1.9	1.9	(c)	3.1
200	1.6	1.7	2.0	2.0	(c)	(c)
2. Dip coating in designated oven						
Gravity convection-type	1.7	1.7	2.0	2.0	3.0(d)	3.4
Mechanical convection-type	1.7	1.7	2.1	2.1	3.1(d)	3.1(d)
3. Type of pressure during exposure						
Weights	1.6	1.6	1.9(d)	1.9(d)	(c)	(c)
Vacuum	1.9	1.9	2.2	2.2	2.9(d)	2.9(d)

(a) Outside line of pattern, length-to-width ratio of 2657:1.
(b) Inside line of pattern, length-to-width ratio of 2647:1.
(c) Unmeasurable because of open conductors or bridges between conductors.
(d) Only one of the two specimens was satisfactory.

Table III.-Effect of varying the developer upon the average resistance of conductors etched on copper-clad laminates.

Developer	Time, min.	Average resistance, ohms, Line width, mils					
		10(a)	10(b)	5(a)	5(b)	2.5(a)	2.5(b)
Trichloroethylene vapor	1	1.9	1.8	2.0	2.0	2.8	2.9
Trichloroethylene liquid	1	1.8(d)	1.8(d)	2.3(d)	2.4	(c)	3.4(d)
Trichloroethylene vapor	2	1.9	1.9	2.3	2.3	3.4	3.2
Trichloroethylene liquid	2	1.9	1.9	2.3(d)	2.2(d)	(c)	(c)
Commercial developer	2	2.1	2.0	2.6	2.6	4.3(d)	4.2(d)

(a) Outside line of pattern, length-to-width ratio of 2657:1.
(b) Inside line of pattern, length-to-width ratio of 2647:1.
(c) Infinite resistance due to breaks in conductors.
(d) Only one of the two specimens was satisfactory.

C. Fine Lines Produced by Chemical Etching of Deposited Copper

1. Depositing copper on resin specimens.

A dozen disks of cured epoxy resin 2 inches in diameter and 1/4 inch in thickness were sanded on one surface to produce a uniform matte finish. They were cleaned with a commercial cleaning powder, rinsed, and then heated in several changes of water. The commercial product(6) used for chemical deposition of the copper was supplied in the form of concentrates from which three solutions were prepared by the addition of suitable amounts of distilled water. The clean plastic disks were immersed in the first solution for 2 minutes, rinsed thoroughly in cold running tap water, immersed in the second solution for 2 minutes, again rinsed thoroughly in running water, and finally immersed for 15 minutes in the third solution. It is believed that the third solution is essentially a modified Fehling solution with formaldehyde as the reducing agent. The first two solutions prepared the surface of the plastic for the reception of the copper and the third solution deposited the copper film which, after washing and drying, was a dull dark copper color.

2. Application of resist to resin specimens.

Because of the relatively porous nature of the deposited film, all resist was applied by dip-coating. This method gave a slightly thicker film than that produced by the whirler. The method of dip-coating was the same as that described previously for use in the gravity convection oven. However, some disks were given one coat of resist, dried, and then given a second coat.

3. Exposure and development of pattern on resin specimens.

The procedures of exposure and development were the same as those described previously for the majority of the laminate samples. The dry sensitized disks were covered with the negative, placed in the vacuum frame, and exposed to the carbon arc for one minute. The patterns were then developed by suspending the disks in the vapors of boiling trichloroethylene for 45 to 60 seconds.

4. Etching of pattern on resin specimens.

The bubble etcher was not used for etching these films. Instead, the pieces were immersed in a petri disk containing warm 40% ferric chloride because the time of etching of the thin copper films could be more easily controlled with this simpler apparatus. After 10 to 15 seconds, the unwanted copper had etched away. The disks were then washed and allowed to dry.

5. Testing of pattern on resin specimens.

The resist was removed from the terminal points of the patterns and resistance measurements were made. The average resistance of the 5-mil-wide lines was 150 ohms and that of the 2.5-mil-wide lines was 195 ohms.

Because of the unexpectedly high resistance values, one of the patterned disks was encapsulated in epoxy resin to protect the copper film, and sliced to reveal its cross section. Although the thickness of the film was variable due to the matte finish of the disk, its thickness was measured under a microscope and found to be ca. 0.3 to 0.6 mil.

Attempts to measure the thickness with an interferometer failed due to the matte finish of the disk.

6. Electroplating of the chemically deposited copper.

An effort was made to improve the continuity of the deposited copper films with a thin copper plating. The patterns were removed from some of the plastic disks by abrading them with sand paper. The disks were then thoroughly cleaned and recoated with copper, as described previously. A plating bath consisting of 330 ml of water, 60 g of $CuSO_4$, and 22 ml of conc. H_2SO_4 was prepared. The disks were plated in this bath for 5 minutes at a current density of 17 amp/sq ft. Two coats of resist were applied to the disks and then they were exposed, developed, and etched as before. The average resistance of the 2.5-mil-wide lines was now 25 to 35 ohms and that of the 5-mil-wide lines was 35 to 45 ohms. The thickness of the plated film was not appreciably greater than that of the unplated film but the plated film appeared to be less porous.

D. Fine Lines Produced by Electroetching of Precious Metals on Glass.

1. Application of pattern to metallized glass.

The substrate in this case consisted of a glass slide on which a thin film of palladium had been deposited by vacuum evaporation techniques. Such a metallized glass slide is shown in Figure 6a.

The slides were degreased in the vapors of boiling trichloroethylene, cooled to room temperature, and dipped in a filtered bubble-free solution of resist. They were stood on end, allowed to drain briefly in the dark at room temperature, and were then placed in an oven at 50°C to dry. Then they were dipped again in resist, stood on the opposite end, and drained and dried in the dark.

A dried slide was aligned with the negative, placed in a small laboratory-built vacuum frame, and exposed to a sun bulb at a distance of seven inches for three minutes.

The pattern was developed in the vapors of boiling trichloroethylene.

2. Attempts at chemical etching of palladium

Although palladium is soluble in both aqua regia and hot nitric acid, previous experience in etching had shown that the resist tended to break down in these acids so neither of them was tested. A bath of hot sulfuric acid dissolved the palladium but also attacked the resist. Cold sulfuric and hydrochloric acids either did not seem to etch the metal, or else were so slow as to be impractical. Methods of etching other than chemical methods were indicated.

3. Electroetching of palladium.

A narrow strip of resist was cleaned from one end of the patterned slides in order to bare the palladium. A low-curing-temperature silver paint was applied to this area and dried in an oven at 50°C.

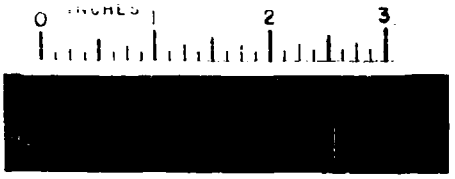
A patterned slide was then placed in a 5-percent solution of hydrochloric acid and connected as the anode of a cell while a bar of steel served as the cathode. When current was applied, gassing began and became vigorous as the current was raised. The resist broke down before any patterns were completely etched through.

Next, a bath containing a 71 percent solution of sulfuric acid was set up with the work as the anode and a steel bar as the cathode. Various current densities from 0.42 to 1 amp/sq in. were tested. Some gassing occurred but it was much less vigorous than that obtained in the hydrochloric acid bath. However, the pattern etched through along the upper third of the slide before any etching occurred along the bottom portions of the slide.

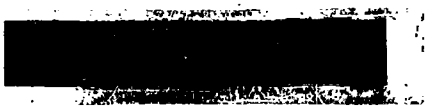
The negative by which the pattern had been placed on the slide was modified to contain an opaque strip completely around, and about 1/4 inch from, the outermost edges of the pattern. A sensitized slide was exposed through this negative and developed. A strip free of resist now surrounded the pattern. A low-curing-temperature silver paint was applied to this strip to form a large peripheral electrode. The silver was covered with microcrystalline wax before placing the slide in the bath. A slide so prepared for etching is shown in Figure 6b. Slides treated in this manner etched more evenly than before but the center longitudinal area farthest from the electrode connection was still the last to etch. However, on using a current density of 0.73 amp/sq in. (350 ma for this pattern), and reducing the current roughly 50 ma every 30 to 60 seconds, slides were obtained in which the patterned area was completely etched through and no breaks appeared in the remaining metallic film. The need for stepwise etching was found to depend on the uniformity of thickness of the metallic film, i.e. non-uniform films always required several stepwise reductions in current to etch the pattern satisfactorily.

Etched slides were removed from the bath, washed in running water, and dried. They were then held in the vapors of boiling trichloroethylene until all the wax was removed. Cotton was then dipped into clean solvent and rubbed gently over the surface of the slide. This latter treatment removed both the resist and the silver because the resin binder in the silver paint had been extracted from the paint during the vapor treatment to remove wax. A sample

finished slide is shown in Figure 6c.



(a) Palladium-metallized glass slide.



(b) Metallized glass slide bearing resist, electrode pattern (not visible), and silver peripheral electrode protected with wax.

(c) Finished palladium electrodes on glass, after electroetching and removal of wax, resist, and silver.

Figure 6. Step-by-step procedure of preparing palladium electrodes on a glass substrate by electroetching methods.

4. Testing of palladium electrodes.

Microscopic examination of the finished electrodes showed that the average line width of the individual bars of palladium that formed the "teeth" of the pattern was 10 mils. Microscopic measurements on the negative of the pattern yielded a similar line-width value, thus indicating that undercutting during etching was negligible.

DISCUSSION

A. Fine Lines in Copper-clad Laminates by Chemical Etching

The dipping process of applying resist to copper-clad laminates produced a coating which was slightly thicker at one edge of the plate than at the other due to the vertical draining position of the plates. Whirling produced a more uniform coating which varied inversely in thickness with the speed of the turntable. The patterns developed satisfactorily on all of the plates having 10-mil-wide lines, regardless of the method of application and drying of the resist and, as seen in Table II there was no significant difference in the measured resistance of these copper conductors. However, as the line width was reduced, differences due to the method of application of the resist began to appear. The 2.5-mil-wide lines and spaces were more consistently etched without breaks in the lines, or bridges between conductors, when resist was applied by dipping and draining than by whirling. Although one might expect the best pattern definition to be obtained with very thin coats of resist, actually the best definition was obtained with the thicker dip-and-drain coatings probably because these coatings had better physical strength and hence better adherence to the copper. Variations in the type of oven employed to dry the coatings did not yield significantly different results.

The use of contact pressure during exposure of the sensitized plates did not yield as satisfactory results as the use of a vacuum frame, as shown in Table II. Although all the patterns applied under contact pressure appeared to develop satisfactorily, and the 10-mil-wide lines also etched satisfactorily, the 2.5-mil-wide lines were badly undercut after etching and no continuous conductors of this size were obtained. Poor contact between the negative and the laminate probably led to light scattering under the negative and, hence, to variations in the width of the lines being printed. This variation was also observed in some of the work reported by Overas[1] where a spring-loaded printing frame was used instead of a vacuum frame. On large sheets of laminate, where warpage of the board may be pronounced, fine-line patterns would be even more difficult to obtain without a vacuum frame.

Table III shows the results obtained on varying the developer. The most acceptable results were obtained with trichloroethylene vapors as indicated by the fact that conductors etched with them gave the lowest values, i.e. values which most nearly approached the theoretical value of ca. 1.3 ohms. With these vapors, a developing-time of one minute was superior to one of two minutes, again because lower resistance of the lines resulted after one minute. Low resistance values accompany negligible undercutting of the resist during the etching process.

The patterns developed in liquid trichloroethylene were not only more undercut than those from the vapors, but were also blotchy, and numerous open conductors were obtained, particularly in the 2.5-mil-wide lines. The conductors developed with the commercial developer had higher resistances than those obtained from either form of trichloroethylene; one of the 2.5-mil-wide lines was continuous, but had relatively high resistance, while the same pattern on another plate was almost completely etched away. It is believed that the liquid developers have a detrimental effect on the bond between the resist and the copper and that a loss of adhesion of the resist occurs

at the edges of the pattern. The etchant is thus able to penetrate under the resist during an earlier stage of etching and undercutting is facilitated.

When the developed plates were heated after being removed from the developer, regardless of which developer was used, less undercutting and breakdowns in the pattern occurred than with unheated plates.

The small bubble etcher containing hot ammonium persulfate provided very even etching of the copper. However, on some of the test pieces, the 5- and 10-mil-wide lines were completely etched through in a matter of 10 to 15 seconds before the same condition was reached with the 2.5-mil-wide lines, probably due to the freer flow of etchant in the wider spaces. Therefore, the comparatively slower method employing ferric chloride was preferred for fine-line work in cases where close control of the temperature and time in the bath were necessary, as in etching the thin films of deposited copper.

In these Laboratories, data are not yet available which will allow comparison of results obtained with the bubble etcher with results obtained with a spray etcher. Overas[1] reported that "1-oz" copper can be etched in 3 minutes by spraying. This is a longer time than was required in these Laboratories with the bubble etcher, but Overas used ferric chloride at a temperature lower than the 65-70°C used here with ammonium persulfate. In either case, in order to prevent excessive undercutting, very close control of the time of exposure of the laminate to the etchant would be necessary when operating at elevated temperatures.

From the measurements of resistance of some of the conductors contained on plates which had been developed in the vapors of trichloroethylene for 1 minute, the average line width of the conductors etched from the 10-mil pattern was calculated to be 7.8 mils, that of the conductors produced from the 5-mil pattern 3.4 mils, and that of the conductors produced from the 2.5-mil pattern 1.1 mils. The microscopic measurements showed the average line width for the 10-mil pattern to be 8.8 mils, that for the 5-mil pattern to be 3.6 mils, and that for the 2.5-mil pattern to be 1.1 mils. The apparent differences for the wider lines are probably due to undercutting which causes the cross-section of the conductor to look like a wedge, rather than a rectangle. The wedge would not be detectable when the conductors were viewed from the top, but the true average line width would be less than the apparent line width measured across the top of the conductor.

B. Fine Lines in Deposited Copper by Chemical Etching

When placing patterns on the thin films of copper deposited on plastic, it was necessary to apply two coats of resist in order to cover the porous metal in a continuous film of resist. When only one coat of resist was applied to the metal, the final etched pattern was usually full of pinholes. Patterns protected with two coats etched to produce few obvious pinholes and breaks in the lines.

As stated previously, the resistance of the lines etched from the 5-mil pattern averaged 150 ohms, and that from the 2.5-mil pattern 195 ohms, but the resistance of similar copper-plated lines was 35 to 45 ohms and 25 to 35 ohms, respectively. Since the theoretical resistance of these lines is about 4.0 ohms, these measurements indicated that, although the copper plating decreased the porosity of the films, it did not make them continuous. The porosity of these films is believed to be due to the matte finish of the surface of the plastic but, since this type of surface is necessary to achieve adhesion between the metal and the plastic, control of the roughness of the surface becomes important, especially when minimum resistance is required.

The etched films were examined under the microscope both for pinholes and undercutting. For the 5- and 2.5-mil patterns, the lines etched from the electroplated films had an average width of 4.9 and 2.4 mils, respectively. For the same patterns, the lines etched from the chemically deposited unplated films averaged 4.8 and 2.3 mils, respectively. Thus, the amount of undercutting was about the same for the two types of lines. However, the electroplated films were superior in respect to continuity (absence of pinholes), as was expected based on their lower resistance values.

C. Fine Lines in Precious Metals by Electroetching

In the electroetching process, the etchants used on the film of palladium were based on those recommended[5] for stripping rhodium from nickel-plated brass because of the similarities between rhodium and palladium. The hydrochloric acid etching bath, however, had to be rejected due to the vigorous gassing. When large bubbles bumped repeatedly against the narrow bars of resist between adjacent sections of the line to be etched, the adherence of the resist to the palladium weakened and the pattern broke down before it was etched. Although the sulfuric acid bath also produced gas, the bubbles were generally smaller, and fewer in number and, hence, less active against the surface of the slide.

Standard procedures for stripping metallic coatings from plated articles call for the use of a solution which will attack the coating without affecting the underlying metal. For the present application, however, the underlying base was glass so there was little danger that it would be attacked. However, this construction complicated the work in other respects, as indicated in the discussion that follows.

Since glass is a non-conductor of electricity, it was necessary to depend entirely on the film

of palladium to conduct the current. Due to the resistance of this film of metal, the distribution of current over the length of the electrode pattern originally supplied was not uniform and etching occurred first at the points closest to the electrode connection. When a highly conductive silver paint was applied around the slide to form a peripheral electrode, fairly uniform etching was achieved. However, the center longitudinal area farthest from this peripheral electrode was usually still the last to etch because it had the longest current path from the electrode connection.

The proneness of the palladium to etch first at points closest to the electrode connection was also reflected in the tendency of the pattern to etch first at all its edges. Therefore, if etching proceeded at a very rapid rate, and severed the contact at the pattern's edge, the palladium in the center of an area which should have etched out completely was left without any connection to the electrode; hence, it remained on the slide. It was necessary, therefore, to etch slowly enough to obtain a uniform removal of metal so that, by the time the edges of the gap were completely formed, the center of the gap was also completely free of metal. At the same time, etching had to proceed rapidly enough to avoid undercutting and also breakdown of the resist which occurs with prolonged immersion in an acid bath. It was necessary, too, to reduce the current periodically in order to maintain approximately the same current density as the line was etched and the remaining area to be removed was decreased.

A shield with an adjustable-size slot, placed between the slide and the steel electrode, would probably facilitate removal of given areas of palladium from the glass. Such a device would shield those areas where etching was to be retarded and leave open the area which was to etch first. In this way, etching might be induced at the center of the area to be removed, rather than at the edges as occurred in this work.

This electroetching procedure was also found applicable to the preparation of chromium electrodes on glass. Such electrodes, suitably treated with a moisture-sensitive material[7] are now undergoing tests as humidity sensing elements in radiosondes.

D. Future Needs in Fine-Line Fabrication

Although etched lines finer than those described in this paper will probably not be required, methods of making fine lines by other processes are needed. For example, screened lines finer, and having more accurate edge-definition, than those now producible are desired when working with small printed ceramic wafers such as those used in the work reported by Doctor and Hebb[8]. One such wafer measures 0.5 x 0.5 x 0.020 inch and bears screened resistors, screened conductors, miniature capacitors[9], caseless transistors[10], and caseless diodes[11], a total of 14 components exclusive of the conductors. Because the conductors and resistors occupy the major portion of the tiny wafer, their reduction in size now becomes critical.

If it appears that such components are better made by vacuum evaporation techniques[12] than by screening techniques, then procedures for making fine-line patterns by vacuum deposition would be needed.

CONCLUSIONS

In conclusion, it has been shown that lines as narrow as 2.5 mils with 2.5-mil-wide spacings can be formed from thin films of copper, either thin foil on laminates or chemically deposited copper. However, on laminates bearing "1-oz" copper, lines as narrow as 5 mils are more practical than 2.5-mil-wide lines; with the latter lines, the rejection rate was too high to give predictable yields of good plates. Conductors 10 mils in width and having 4-mil-wide spacing between lines have been formed by electroetching such metals as palladium and chromium.

In order to achieve satisfactory results with any fine-line patterns, however, the following points are emphasized:

1. The metal surface should be clean and free of pinholes, scratches, and other defects. Such defects, which are almost unnoticed when normal-sized patterns are being produced, can rupture or otherwise mar the continuity of a fine-line pattern.

2. In laying out a fine-line pattern, the following effect should be considered. When wide spaces are etched away between conductors, more undercutting of the conductors occurs than when the space is narrow, probably due to the freer flow of etchant in the larger space and consequent more rapid replacement therein of exhausted etchant with fresh etchant.

3. The resist should be free of foreign particles and air bubbles and the clean metal surfaces should be dipped in it and dried under as dust-free conditions as possible.

4. The dry sensitized panel and the negative should be held together in a vacuum frame during exposure. The negative should be placed with the emulsion side against the coated panel in order to minimize the diffusion of light between the negative and the sensitized surface. As in condition number 3 above, dust-free conditions should prevail.

5. The developer should be chosen to have no detrimental effects on the bond between the resist and the metal. The vapors of boiling trichloroethylene, and an exposure time of 45 to 60 seconds, are recommended for fine-line

work.

6. The developed plate should be heated before being etched because heating appears to set the pattern and make it more resistant to undercutting.

7. The etchant and etching process should be chosen to: (1) give uniform removal of metal, (2) allow ready removal of the specimen from the etchant and, (3) permit rapid washing to stop the etching action.

ACKNOWLEDGMENT

The author wishes to acknowledge the contribution of Frank E. Jones of the National Bureau of Standards in supplying both the pattern and the metallized glass slides for the electroetching work on palladium.

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INTERCONNECTION OF MICROMINIATURE ELECTRONIC SUBASSEMBLIES

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Methods for interconnecting extremely small modules, such as printed wafers having volumes of ca 0.005 cubic inch, are under investigation in these laboratories. The basic technique involves stacking wafers so that all leads protrude from one side of the assembly, encapsulating the assembly in resin, facing off the side containing the leads in order to expose the interconnection points as cross sections of the wires, and then interconnecting these points. Feasibility of interconnecting these points either by chemically deposited copper or by printed silver wiring was demonstrated with modules larger than 0.005 cubic inch. These techniques will be extended to the small printed-wafer modules as soon as sufficient numbers become available.

INTRODUCTION

The assembly of electronic equipment requires the electrical connection of various component parts according to a prescribed plan. In many circuits the actual physical size and location of the individual parts is of little concern as long as the electrical connections indicated in the schematic are made. For this reason, assembly techniques are numerous and, in most equipment, are dictated by strictly economic considerations. When considering equipment intended for military applications, however, several other criteria must also be considered. These criteria include: (1) low weight and small volume, (2) rugged assembly to enable survival in high shock-and-vibration environments, and (3) ease of repair by personnel having a minimum of special training.

Miniaturization techniques go a long way toward meeting both of the first two criteria. The facts that miniature assemblies occupy less volume and are lower in weight than their full-size counterparts are self-evident. It is also well known that tiny structures are much more resistant to damage from shock and vibration than large structures. This effect is due to the fact that forces generated by accelerations are proportional to mass, and hence to the third power of length, while strengths are proportional to cross-sections and, hence, to the second power of length. Therefore, as a structure is reduced in size, its mass is diminished much faster than its cross-section, and its structure becomes more resistant to damage from forces due to acceleration.

It is the third criterion which spurred the development of the electronic "module", that is an individually fabricated subassembly that may be replaced in toto when repair becomes necessary. Optimum complexity for individual modules has been the subject of several recent papers [1],[2] and it is not the purpose of this paper to dwell in this area. The general conclusions of most writers on this subject are these: (1) the more complex the module, the smaller the number of intermodule connections that must be made, and (2) the less complex the module, the more likely that it will find repeated use in an equipment and the lower the cost when it must be discarded.

Figure 1 summarizes some recent miniaturization work reported previously[3]. It shows four steps of miniaturization of a binary divider module. Figure 1A shows a module which employs a miniature vacuum tube. The other component parts are mounted in the base of the socket by conventional techniques and interconnection to the larger assembly is made by the octal plug upon which the entire circuit is constructed. This particular binary divider occupies a volume of about 2 cubic inches and requires about 2 watts of power.

Figure 1B shows a transistorized version of the same binary divider circuit. This module demonstrates not only the power-saving advantage offered by transistors over vacuum-tubes (10 milliwatts as opposed to 2 watts) but also the use of the very popular etched wiring technique. Interconnection of modules of this size is accomplished by etched wiring connectors into which the individual subassemblies can be plugged. Many varieties of modularization at this size-level have appeared in the literature. Among them are the "plus"-module[4], so called because of the +-shaped three-dimensional design, and the sandwich or cord-wood module[1]. In most cases, the printed or etched wiring that fits into the connector is plated with a hard, corrosion-resistant metal. In other cases, an auxiliary set of terminals is attached to the wiring board and these terminals plug into the connector.

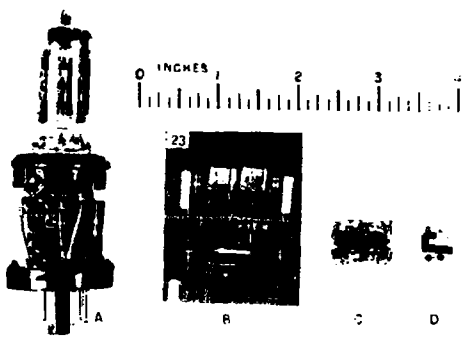

Figure 1. - Miniaturization of a binary divider module from vacuum-tube version A to normal transistorized version B, to "hearing-aid"-sized-component version C to caseless-component version D.

Figure 2 shows again the transistorized etched-board module (top left), an etched wiring connector (bottom left), and a 10-stage binary counter (right) made from ten of these modules, ten etched wiring connectors, and hook-up wire. The counter packaged by these techniques occupies about 22 cubic inches and requires about 100 milliwatts of power.

Figure 1C shows the natural continuation of the etched-wiring-board technique using very tiny "hearing-aid"-sized component parts. The step from B to C is not entirely the result of the component manufacturer's ability to shrink the size of his components. It required the development of new, low-voltage, low-power circuitry by the systems engineer[5],[6]. Since simple shrinkage in component size usually results in decreased power rating (or voltage rating) this circuit development became a must. Interconnection at this level can be accomplished neatly with a secondary etched wiring board.

Figure 3 shows again the hearing-aid-sized module (foreground), an etched interconnection board (top left), and the final ten-stage counter (right). This counter occupies about 1.6 cubic inches and requires about 20 milliwatts of power. When this degree of miniaturization is reached, the question arises as to what should be considered a module. This 10-stage binary counter occupies less volume than the 1-stage binary divider based on a miniature vacuum tube. If it were desired to make the 10-stage counter a module in itself, the entire subassembly might be encapsulated as is. On the other hand, if repairability at the 1-stage level were desired, the individual stages could be separately encapsulated before inserting them into the interconnection board. Commercially[7],[8], the use of header mountings for modules at this level of miniaturization is popular although they detract

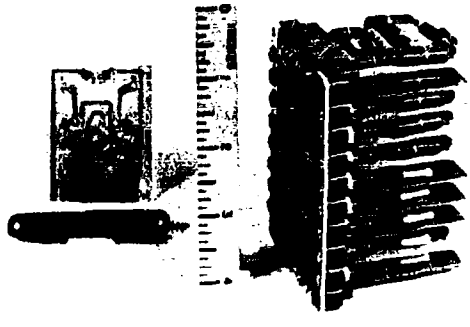

Figure 2. - Ten-stage binary counter (right) made from normal transistorized etched-wiring-board modules (top left) and etched wiring connectors (bottom left).

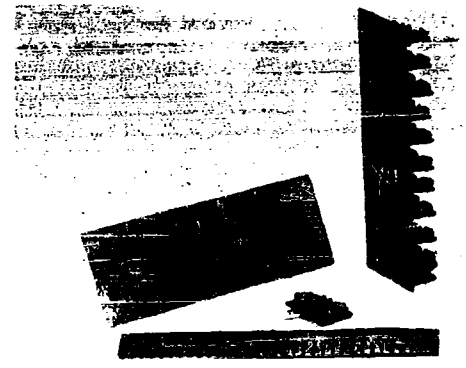

Figure 3. - Ten-stage binary counter (right) made from etched interconnection board (left) and "hearing-aid"-sized transistorized modules (foreground).

from the high component densities, i.e. number of component parts per unit volume, which can be obtained.

Figure 1D shows the so-called "DOFL-2D" binary divider[3], 2D because of its near 2-dimensional configuration. This wafer circuit, when unencapsulated, occupies a volume of approximately 0.005 cubic inch and yet is electronically equivalent to the preceding modules. Its tremendous volume efficiency is due to elimination of cases for individual parts, and the use of many printed-circuit techniques[3],[9]. If such modules were mounted in headers, they could undoubtedly be interconnected using the secondary etched-wiring-board technique already described. Mounting of each binary divider in a header, however, would greatly reduce the volume efficiency at this level of microminiaturization. On the other hand, the mounting of several interconnected stages within a single header would not only provide encasement for the uncased component parts but also allow high component densities.

Figure 4 shows a DOFL-2D binary divider module and the stack of ten of these modules required to produce a counter equivalent to those shown in Figures 2 and 3. The volume of this counter is only ca. 0.2 cubic inch. It requires 20 milliwatts of power. Note the fifty protruding lead wires which must be interconnected. If connectors comprising etched wiring boards are ruled out because their interconnecting wires would be spaced no more than 10 mils apart, two other possible techniques exist. The first would require welding the tiny wires, using procedures developed in the subminiature vacuum tube field. The only demand which would be made on the DOFL-2D wafer is that the material chosen for the lead wires be weldable. It is of interest to note that at least one organization[10] is presently fabricating self-supporting modules at the hearing-aid level of miniaturization using welding techniques.

Figure 4. - Ten-stage binary counter (right) made from printed wafer modules (left); not interconnected.

The second technique is one now under investigation at these laboratories because it appeared to be especially suited to the 2-D level of microminiaturization. It involves: (1) stacking wafer stages in the configuration shown in Figure 5, using spacer materials where necessary, so that all lead wires protrude from one side of the assembly, (2) encapsulating the assembly in resin, (3) facing off the side containing the wires on a lathe or milling machine so that the interconnection points appear as cross-sections of the lead wires, and (4) interconnecting these points. Descriptions of the several methods of interconnection considered thus far in these laboratories form the principal subject of this paper.

DEPOSITED-METAL INTERCONNECTIONS

One procedure for making interconnections between these cross sections of wire involves first depositing a metal over the entire faced-off surface. To date, copper deposited by chemical reduction[11] has been employed for this purpose. Using photolithographic techniques[12], a resist would then be laid down on the copper surface, exposed through a mask of the desired interconnection pattern, developed, and washed. The extraneous copper could then be etched away. Finally, the deposited interconnection wires would be protected by a layer of plastic. This technique should yield a completely interconnected stack of wafers. Figure 6 shows such a stack; the bottom plate is not a module but serves only to hold the lead-out wires.

In a variation of the above-described procedure, interconnection paths have been milled in the faced-off side of the encapsulated stack, metal deposited over the entire side, and the metal not in the grooves then removed either with an abrasive or by a second facing-operation.

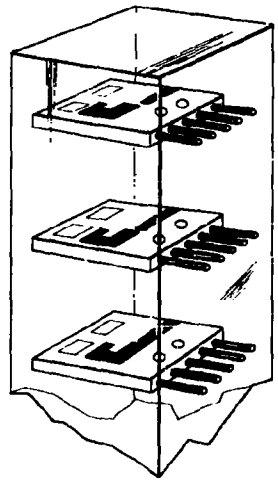

Figure 5. - Stack of wafer modules encapsulated in resin and faced off to expose cross sections of lead wires.

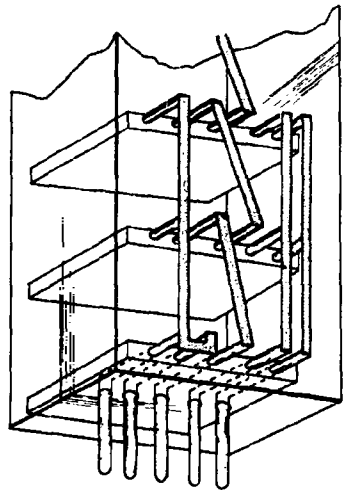

Figure 6. - Stack of wafer modules encapsulated in resin and faced off to expose cross sections of lead wires which are then interconnected by deposited copper films.

Before employing either of these procedures to build a counter, the feasibility of deposited-copper interconnections was demonstrated by test specimens such as that shown in Figure 7. The specimens were prepared in the following fashion. Pairs of duplicate wires of several types were placed in rows in a polyethylene mold of dimensions 1.5 x 1.0 x 0.3 inches. The wires were allowed to extend through the bottom and above the top of the mold. The mold was then filled with a liquid epoxy resin to which had been added 7.5 parts of diethylaminopropylamine per hundred parts of resin. The resin was allowed to gel at room temperature, was then cured overnight at 65°C, and finally cured for 2 hours at 100°C. The plastic block containing the embedded wires was then cut in half in a direction perpendicular to the wires in order to form two specimens. The cut surfaces were then roughened with sand paper, cleaned with detergent, and masked with tape so as to leave an unmasked path between each set of duplicate wires. The specimen was then rinsed in isopropyl alcohol and copper was chemically deposited on the unmasked areas by the following commercial procedure[11]. The specimen was immersed in a sensitizing solution for two minutes, rinsed in cold tap water, immersed in another sensitizing solution for two minutes, and rinsed again. The pieces were next placed in a reducing solution containing copper ions and held there for six to twenty minutes at room temperature. The specimens were then rinsed and the tape was stripped away to leave deposited copper bands like those shown in Figure 7. A thin layer of epoxy resin was poured over the copper and cured to protect the film from abrasion.

Electrical continuity between wires of each set was checked using an ohmmeter. The types of wires tested are listed in Table I and all made adequate connection. The test specimens were next temperature cycled five times from -55°C to +85°C and retested. No connections failed.

Table I. - Types of wires that have been successfully connected by deposited copper films.

Type of wire	B and S Gage No.	Number of pairs of duplicate wires tested
Columbium	20	8
Copper, bare	20	13
Copper, tinned	22	13
Gold	28	8
Nichrome	30	13
Silver	21	8
Tantalum	20	13

Next, it was decided to interconnect an operating circuit by deposited-copper techniques. Due to the lack of a sufficient number of wafer modules (these modules are still in themselves research models) it was decided to substitute "hearing-aid"-sized modules. Five NOR[13] circuits were chosen for interconnection because together they would constitute a half adder. Also, this NOR circuit was being extensively evaluated by a circuit research group of these laboratories[11].

Figure 8 shows the half-adder. Interconnection was accomplished on two opposite surfaces so that two methods employing deposited copper films could be evaluated. The view on the left-hand side of Figure 8 shows interconnections composed of copper

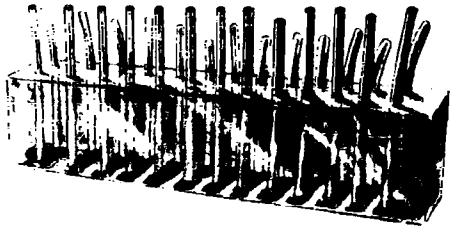

Figure 7. - Test specimen for evaluation of deposited copper interconnections.

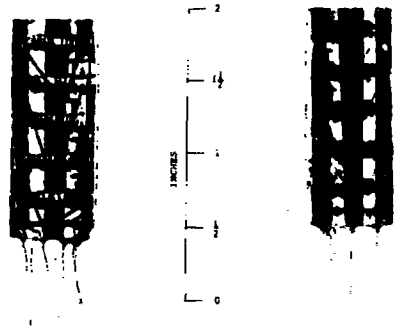

Figure 8. - Half-adder made from five NOR modules interconnected by deposited copper wiring: front of unit (left) employs copper-filled grooves; back of unit (right) employs copper bands applied through a mask.

deposited in milled grooves 10 mils wide by 5 mils deep. The copper was chemically deposited over the entire side, using the procedure described previously, and the copper not in the grooves was sanded off by hand. The view on the right-hand side of Figure 8 shows deposited-copper interconnections made by the masking-tape procedure. Electrical tests of this half-adder showed operation comparable to that of hand-wired units.

SCREENED-SILVER INTERCONNECTIONS

Other procedures for making interconnections between the cross sections of the wires will readily occur to those familiar with the techniques of printed circuitry. An obvious one, and one which has been employed in these laboratories, is the application of a silver pattern by "silk"-screening. The applicability of this method was demonstrated on a free-running multivibrator. All the component parts were encapsulated with their leads protruding from a single side of the block. The block was faced-off and the component parts were interconnected with screened silver paint applied across exposed cross-sections of the lead wires by well-known screening techniques[15]. The multivibrator operated in all respects as well as a solder-assembled unit.

DISCUSSION

The first method proposed in this paper for accomplishing deposited copper interconnections involves the use of a photolithographic procedure. In quantity production, a photolithographic procedure should prove inexpensive and yield extremely fine lines. However, this procedure has not yet been adapted to the application at hand for the following reasons. First, the technique itself has been proven to be feasible[16] and the details of its application to the present problem were of secondary interest compared to the achievement of reliable electrical contact between lead wires and deposited copper. Secondly, the details of making and aligning pattern negatives for masking the interconnection patterns between the cross-sections of the wires in the encapsulated assembly have to be worked out but are needed only after feasibility has been demonstrated.

Feasibility of deposited and screened metal interconnections has been demonstrated. This technique promises minimum-volume interconnection for minimum-volume wafer subassemblies, and places phenomenal component densities within reach.

Finer interconnections can probably be produced via the deposited-metal methods than with screened-silver methods because ink forced through a stencil will flow to some extent before it hardens, and produce lines wider than those of the stencil. Ten-mil-wide lines with four-mil-wide spacings have been produced with resist-masked and electroetched vacuum-deposited-palladium[16]. Similar definition has been achieved with resist-masked and chemically-etched chemically-deposited-copper[16]. Ten-mil-wide screened lines would be considered excellent at the present state of the screening art.

It should be noted that fine-line interconnections have a finite resistance that must be taken into account in circuit design. For lines like those shown in Figure 8, this resistance is of the order of one ohm which, for the circuits described in this work, is negligible. The thickness of deposited copper is estimated between 0.3 and 0.6 mil[16].

Future work must include: (1) development of methods for aligning photographic negatives on encapsulated assemblies, (2) an evaluation of long-term storage effects on deposited and screened interconnection wires, and (3) the construction of interconnected stacks of wafer-type DOFL-2D modules.

ACKNOWLEDGEMENT

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DESIGN OF A TWO-TRANSISTOR BINARY COUNTER

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Abstract

The binary counter discussed is an Eccles-Jordan type two transistor flip-flop with a two-diode steering network. The design of such a circuit is considered as a three-level problem. The first level is the design of a circuit for laboratory breadboard operation. The criteria used for circuit synthesis are (1) output signal required, (2) input signal available and (3) required speed of operation.

The second level of design is that of a circuit for use in a piece of field equipment where marginal checking and unit replacement are possible. The additional design criteria used are (4) total power consumption, (5) circuit tolerances, (6) environmental temperature problems, (7) total number of components and (8) cost per unit. The third level of design is that of a circuit to go into a piece of field equipment where unit replacement is not possible, due to potting, inacessibility or small size (microminiaturization). The main problem in the third-level design is to develop a rigid acceptance or rejection test to predict the future performance of a circuit before potting. Three methods which have been used at DOFL in the testing of 2D-wafer binary counter modules are discussed.

In conclusion, it is pointed out that the three-level design requires thorough circuit analysis to devise acceptance tests and trained personnel or special equipment to implement the tests. However, the net result will be more reliable electronic systems for both military and commercial applications.

Introduction

In the past, the design of a binary counter has been approached as a problem of selecting the components for proper operation of a circuit in the laboratory. The difficulties involved in designing a circuit to operate reliably under field conditions have been left to the individual engineers in most cases. In this paper three distinct levels of circuit design will be discussed. The first level of design is that of a circuit to operate in the laboratory. The second level of design is that of a circuit to operate in a field system where marginal checking and unit replacement are possible. The third level of design is that of a circuit to operate in a field system where unit replacement is not possible because of inaccessibility or small size (microminiaturization). The design difficulty increases going from the first through the third levels of design.

The operation of a binary counter will be described. Next, a procedure for determining the circuit components will be derived from a few basic criteria. This is the first level of design. The additional criteria for a second level design will be discussed. Finally, some procedures which have been tried in a third level design will be discussed.

Operation of Binary Counter

The binary counter is a two-state device which can be triggered alternately from one state to the other by successive pulses on a single input line. The binary counter consists of two parts, a flip-flop circuit which acts as a memory, and a steering circuit which directs the input pulses to the proper side of the flip-flop. The action just described results in a division by two or counting, i.e. if a square wave of one frequency, f, is applied to the input, a square wave of $1/2$ f is obtained at the output. The frequency, f, may be any frequency below the maximum counting rate of the binary counter. The binary counter discussed in this paper is an Eccles-Jordan type two-transistor flip-flop with a two-diode steering network.

A saturated two-transistor flip-flop equipped with set and reset networks is shown in Figure 1. The transistors in this circuit are either saturated (presenting an impedance of less than 10 ohms from collector to emitter), or are cut off (presenting an impedance greater than 100 kilohms from collector to emitter). With the values of collector resistors generally employed, the voltage drop across the transistor in the saturated condition is of the order of 0.1 volt. The collector current flowing when the transistor is cut off is between I_{CBO} and βI_{CBO} ($I_{CBO} < I_C < \beta I_{CBO}$). The cut-off collector current is limited to I_{CBO} if the base of the "off" transistor is positive with respect to the emitter; it is close to βI_{CBO} if the base of the transistor is left floating.

The flip-flop circuit is arranged so that if one transistor, say T_1, is cut off, the negative voltage at its collector turns the opposite transistor, T_2, on. This will be arbitrarily called the "one" state. The other stable state, "zero," occurs when transistor T_2 is off and T_1 is on. The circuit can be triggered from the "one" state to the "zero" state by a positive

pulse applied to the "reset" input, cutting off transistor T_2. Similarly, the circuit may be triggered from the "zero" state to the "one" state by the application of a positive pulse to the "set" input.

If the "set" and "reset" inputs of the circuit in Figure 1 are tied together, the circuit will operate as a binary counter. In this case the positive input pulse goes to both transistor bases, but can only cut "off" the conducting transistor. This circuit is sensitive to the relation of the size of the cross-coupling capacitors, C_C, and the shape and duration of the trigger pulse. Wider variations in this pulse may be tolerated, and the cross-coupling capacitors may be omitted, if the input pulse is steered to the proper transistor. The input circuit may be converted to a steering circuit by connecting the diode biasing resistors R_{K1} and R_{K2} to the collectors of T_1 and T_2 respectively.

The binary counter shown in Figure 2 has such a steering circuit input. In addition, the resistors R_S have been returned to a positive voltage source, V_{BB}, to insure cut-off of the resistors. The steering circuit operates as follows: Assume transistor T_1 is cut off and T_2 is conducting. Point B is at ground. Diode D_2 is biased slightly in the forward direction through resistor R_{K2} since point F is slightly negative with respect to point D. Diode D_1 is biased V_C volts in the back direction through resistor R_{K1} since the collector voltage of T_1 is $-V_C$ volts. A positive pulse applied to the input proceeds through capacitor C_R and diode D_2 to turn transistor T_2 off and cause the flip-flop to change state. The positive pulse does not go through diode D_1 since that diode remains biased in the back direction as long as the input pulse is less than V_0 volts. When the flip-flop changes state, capacitor C_R (point D) charges toward $-V_C$ through R_{C2}, R_{K2}, and the resistance of the signal source. This voltage biases diode D_2 in the back direction. After the flip-flop transition, point C begins to fall toward ground potential. If the input to the binary counter was a narrow pulse from a low impedance source, the counter is ready to receive another pulse as soon as the diodes are biased properly by the transitions just mentioned. A narrow pulse means a pulse that is of shorter duration than the sum of the transition time of the flip-flop and the rebiasing time of the gates.

In many applications the input to the binary counter is a square wave from a previous stage as shown in Figure 2. In this case the time constants R_TC_S and R_TC_R also play a part in determining the recovery time of the counter. The waveforms during operation (Fig. 3) help make this clear. When transistor T_T is "off," the voltage at the input to the binary stage is $-V_C$. The voltage at diode D_1 (point C) is also $-V_C$ if transistor T_1 is "off." When transistor T_T turns "on" at time X_0 the input is effectively returned to ground. Capacitor C_S instantaneously draws current through R_{K1} and R_{C1}. Point C rises sharply toward ground and then begins to charge back to $-V_C$ through R_{C1}, R_{K1} and C_S. Shortly thereafter, due to the positive pulse coupled through capacitor C_R and diode D_2 to the base of transistor R_2, the flip-flop changes state. Now transistor T_1 is "on" and point C again moves toward ground. This transient at point C does not show on the waveform at C since the input pulse is long compared to the transition time of the flip-flop. Point C instead appears to hold at ground potential until time X_1. The level drifts at the collectors and the bases of T_1 and T_2 as well as the recovery transient $(R_{K2} + R_{C2})\,C_S$ of diode D_2 at point D are readily apparent. When transistor T_T turns "off" again at time X_1, point C is driven to $-V_C$ and point D is driven to $-2V_C$. Point C recovers to ground with a time constant $(R_{K1} + R_T)\,C_S$ while point D recovers to $-V_C$ with a time constant $(R_{K2} + R_T + R_{C2})C_R$. When point D is driven to $-2V_C$ a negative pulse appears at B, the collector of the "off" transistor T_2. The subscripts are reversed and the letters A and B, C and D, and E and F are interchanged for the next cycle of operation, $X_2 - X_4$.

First Level Design of Binary Counter

In the first level of design of a binary counter, one needs to consider only the following basic points:

1. Output signal power required.
2. Input signal power available.
3. Speed at which the stage must count.

The maximum speed at which a binary counter will operate depends on the alpha cutoff frequency of the transistors used, in addition to other factors to be discussed. In the type of circuit herein mentioned a good "rule of thumb" is that the maximum speed that a counter will run reliably is a factor of 1/10 the alpha cutoff frequency of the transistor. To realize this speed, cross-coupling capacitors must be used. For instance, in the case of the surface barrier transistor, the maximum speed of operation is about 300 kc without capacitors and about 2 mc with cross-coupling capacitors of the proper value.

By employing emitter-follower coupling and faster gating this factor can be increased to about 1/5. If complementary symmetry circuits and high speed gates are used, this factor can be increased to about 1/3 or 1/2.5.[1,2] If one chooses the maximum frequency of operation of the binary counter to be 1/10 alpha cutoff, the minimum alpha cutoff of the transistor to be used is specified. To decide exactly what transistor to use one may also wish to consider size, β and material (germanium or silicon).

Another good "rule of thumb" is that the output voltage obtained from a circuit of this type is from 0.7 V_{CC} to 0.8 V_{CC}, where V_{CC} is the collector supply voltage. Therefore when the desired output voltage is specified the supply voltage can also be immediately specified.

It may be shown that the relationship

$$(1)\quad R_B \simeq \frac{\beta}{4} R_C$$

gives a safety factor (S = 4) to allow for decrease in β and still insure saturated operation for a grounded emitter switch as used in the basic flip-flop.[3] In the basic flip-flop the size of the collector resistor, R_C, is limited by several factors. The minimum R_C is limited by the maximum current rating of the transistor and/or the allowable power dissipation by the flip-flop. The maximum R_C is limited by the load R_L which must be driven from the collector.

$$(2)\quad R_L = \frac{R_B R_{EXT}}{R_B + R_{EXT}}$$

where R_B is a base biasing resistor and R_{EXT} is the external load resistance. Assuming that the maximum R_C is desired, one can compute R_C in the following manner.

The voltage, V_C, at the collector of the "off" transistor will be

$$(3)\quad V_C = V_{CC} \frac{R_L}{R_L + R_C}$$

neglecting I_{CBO}. Substituting $V_C = 0.7\ V_{CC}$ the following equation is obtained.

$$(4)\quad 0.7V_{CC} = V_{CC} \frac{R_L}{R_L + R_C}$$

Completing the solution for R_C in terms of R_L equation (5) is obtained

$$R_C = \frac{0.3}{0.7} R_L = \frac{1}{2.3} R_L \quad \text{or}$$

$$(5)\quad R_C \simeq \frac{1}{3} R_L$$

Substituting for R_L from equation (2) into equation (5) the following is obtained:

$$(6)\quad R_C \simeq \frac{1}{3} \cdot \frac{R_B R_{EXT}}{R_B + R_{EXT}}$$

Substituting for R_B, $R_B = \frac{\beta}{S} R_C$, the following is obtained:

$$R_C = \frac{1}{3} \frac{\beta/S\ R_C R_{EXT}}{\beta/S\ R_C + R_{EXT}}$$

$$(\beta/S\ R_C + R_{EXT})\ 3R_C = \beta/S\ R_C R_{EXT}$$

$$(7)\quad R_C = \frac{(\beta/S - 3)\ R_{EXT}}{3\ \beta/S} \quad \text{or}$$

$$(8)\quad R_C = \frac{\beta - 3S}{3\beta} R_{EXT}$$

The value of R_C is thus specified in terms of the β of the transistor to be used, the safety factor S and the external load to be driven. If the load is capacitive it is well to specify R_C such that

$$(9)\quad R_C C_L \leq \frac{1}{10f}$$

where C_L is the loading capacitance and f is the maximum frequency at which the circuit is to operate. This will insure reasonably square output waveforms.

Sample calculations of R_C from eq. (7) for two transistor types follow:

For 2N128 β = 20, S = 4

$$R_C = \frac{5 - 3}{15} R_{EXT} \simeq \frac{1}{7} R_{EXT}$$

For 2N77 β = 50, S = 4

$$R_C \simeq \frac{12 - 3}{36} R_{EXT} = \frac{1}{4} R_{EXT}$$

The results indicate that if all other factors are equal, the use of the transistor with the higher β will result in a larger R_C (and therefore lower power dissipation for the counter).

Using equation (8), an expression for R_B in terms of the external load, the β of the transistor and the safety factor can be obtained.

$$(10)\quad R_B = R_{EXT}\ (\beta/3S - 1)$$

In the derivation of equations (7) and (10) it was assumed that $V_C >> V_{BE}$, the base to emitter voltage of the saturated transistor, and that $R_B >> R_I$ where R_I is the input impedance of the saturated transistor.

The resistor R_S is chosen to limit the effect of I_{CBO} in the "off" transistor. It should be 5 or more times larger than R_B ($R_S \geq 5R_B$) to prevent loading of the "on" transistor. Often R_S is returned to a positive voltage $+V_{BB}$ rather than to ground. In this event $+V_{BB}$ is chosen such that

$$\frac{+V_{BB}}{R_S} \geq I_{CBO}$$

at the highest expected temperature.

For shortest recovery time of the binary, R_K should be small. However, a lower limit for R_K of about $5R_C$ ($R_K \geq 5R_C$) is necessary to limit feed-through and loading. A value often used is $R_K = 10\ R_C$.

The cross-coupling capacitors C_C should be large enough to transfer enough charge to switch the transistor from "off" to "on." They should not be so large as to transfer appreciable charge to the collector, of say, T_1, when T_2 is "on" and the reset diode, D_2, is pulsed. Theory predicts that for the highest speed of operation $V_C C_C$ should be greater than Q_A, the charge stored in the base region of the "on" transistor, excluding charge due to saturation.

It may be shown that the charge required to turn "off" a transistor is approximately

$$(11)\quad Q_T = Q_A + Q_S = \frac{I_C^*}{2\pi f_{\alpha co}} + \frac{K\,(S-1)}{\beta}\, I_C^*$$

$$\text{if } I_B >> I_C^* = \frac{V_{CC}}{R_C},$$

through use of Ebers' and Moll's one-dimensional transistor theory. The charge Q_S is the additional charge stored in the base region due to saturation. The factor "K" depends on the forward and reverse alphas and alpha cutoff frequencies. For the 2N77 type transistors this factor is about 2.0×10^{-6} seconds. The factor "S" is the safety factor previously mentioned. For S = 1 the transistor is at the edge of saturation and no charge is stored due to saturation. Experimental measurements have determined that the theoretical values given by equation (11) agree with the actual turn-off charge within 20% for the transistor types 2N207, 2N217, GT763, 2N128.[4]

One may choose

$$(12)\quad V_C C_C = 1.4Q_A = \frac{1.4I_C^*}{2\pi f_{\alpha co}} = \frac{1.4V_{CC}}{2\pi f_{\alpha co} R_C}$$

and get equation (13) by the following substitutions:

$$0.7V_{CC} C_C = \frac{1.4V_{CC}}{2\pi f_{\alpha co} R_C}$$

$$(13)\quad C_C = \frac{1}{\pi f_{\alpha co} R_C}$$

In practice the value of C_C used is usually 2 to 5 times larger than the value of C_C calculated from equation (13). This allows for external capacitive loading of the collector. If highest speed of operation is not of importance the cross-coupling capacitors are unnecessary with the type of steering described in this paper. In the event that the cross-coupling capacitors are omitted the transition time of the flip-flop is approximately equal to the time for the "off" transistor to turn on with current drive through R_B only. This switching time may be computed directly from Ebers' and Moll's equations or from some nomograph such as "Switching Time Nomographs" by T. A. Prugh, Electronics, 31, No. 17, p. 72, April 25, 1958. It is difficult to calculate the transition time if the cross-coupling capacitors are included. However, experimental results show that the transition time for a circuit with cross-coupling capacitors can be less than 1/3 the transition time for the same circuit without cross coupling capacitors.

The input capacitors C_S and C_R should be as small as possible to allow shortest recovery time of the binary counter. However, for good operation of the binary counter described herein, the input pulse must completely switch the "on" transistor to "off." This requires that

$$V_I C_S = V_I C_R \geq Q_T$$

where V_I is the minimum input voltage to the binary counter and Q_T is the charge required to turn "off" the "on" transistor. In cases where the turn-off charge and minimum input signal are known the values of C_S and C_R may be computed directly. If Q_T is not known then

$$C_S = C_R \geq \frac{3Q_A}{V_I}$$

will give usable values of C_S and C_R. In circuits which use cross-coupling capacitors it is well to specify $C_S = C_R = 3C_C$. Much larger values of C_S and C_R are sometimes used but one must insure that the time constants $R_{K1}C_S$ and $R_{K2}C_R$ are small compared to the time between input pulses.

For room temperature operation and at collector current levels high compared to βI_{CBO}, e.g. $I_C^* > 1$ ma. for 2N77 type transistors, practically any diodes will suffice, e.g. 1N99, 1N34, 1N56. For operation at high temperature or at collector current I_C^* comparable to βI_{CBO} the back impedance of the diodes must be high (greater than 10 megohms). Otherwise voltage leakage to the transistor bases from points C and D will offset the effect of the positive bias voltage and cause the circuit to fail.

Summary of Basic Design

Given the basic criteria of

1. Output Signal Power Required, V_C, R_{EXT}, C_L
2. Input Signal Available, V_I
3. Maximum Counting Speed

to design a two-transistor binary counter as shown in Figure 2 one proceeds as follows:

1. Select a transistor with $f_{\alpha CO} \geq 10\ f$.
2. Choose $V_{CC} \geq 1.4\ V_C$
3. Compute R_C from

$$R_C \leq \frac{\beta - 3S}{3\beta} R_{EXT}$$

choosing $S = 4$ and/or insure that

$$R_C C_L = \frac{1}{10\ f}$$

4. Compute R_B from

$$R_B = \left(\frac{\beta}{3S} - 1\right) R_{EXT}$$

5. Choose $R_K = 10\ R_C$
6. Choose $R_S = 5\ R_B$
7. Choose $V_{BB} \geq I_{CBO} R_S$ for worst I_{CBO} expected
8. Compute C_C from

$$C_C = \frac{3}{\pi f_{\alpha CO} R_C}$$

9. Compute $C_S = C_R$ from

$C_S = C_R = 3C_C$ if cross-coupling capacitors are used. Compute $C_S = C_R$

$$C_S = C_R \geq \frac{6}{\pi f_{\alpha CO} R_C} \quad \text{if}$$

cross-coupling capacitors are not used. Insure that

$$R_{K1} C_S = R_{K2} C_R \quad \frac{1}{4f}$$

10. Choose high back impedance germanium diodes or silicon diodes for higher temperature or low current ($\beta I_{CBO} \geq I_C^*$) operation. Choose any germanium diode for high current. ($\beta I_{CBO} < I_C^*$) and room temperature operation.

Additions for Second Level Design

The second level of design is that of a circuit to work in a field system, such as a computer in which marginal checking and unit replacement are allowed. At the second level of design other factors enter, such as:

5. Total power consumption
6. Circuit tolerances (margin)
7. Temperature considerations (environmental)
8. Total number of components
9. Cost per unit

Often in large systems, although impedance levels may be fixed, the supply voltages and current levels may be flexible. In such cases a generalized common-emitter NOR circuit may be considered. This circuit may then be designed for minimum power dissipation.[5] Two NOR circuits connected properly form a binary counter, if steering circuits are also supplied.

The circuit tolerances of a binary counter must be known if the circuit is to be used in a large system. This covers items such as: "will the circuit fail to operate if the input voltage decreases 20%; if the supply voltage drops 10%; if the collector resistors are different by 30%?" One arrives at the concept of margins and marginal checking to evaluate circuits. The curves in Figure 4 show one concept of margins. The plots are allowed percentage decreases of input voltage before failure occurs vs. counting frequency. The curve labelled "A" is for a type of direct-coupled binary counter. The curve labelled "B" is for an optimized emitter-follower-coupled binary counter. Either of the circuits will operate if the input voltage is above the lines shown.

Consider the case of operation at 10MC. This is practically the upper frequency limit of circuit A. A 1% decrease in the input signal from the nominal 100% input level would cause this circuit to fail. Circuit B, on the other hand, will operate if the signal decreases 15% from its nominal input value at 10MC. However, at 1MC the situation has changed. At this point the circuit A will operate if the input voltage is decreased 50% from the nominal value while circuit B must receive a signal within 30% of its nominal value to operate properly. For 10MC operation it is clear which circuit would be used for reliable operation. For 1MC operation there is a choice.

In marginal checking, the problem is to find a so-called "handle" to vary which will cause circuits which are near failure, or "marginal," to fail. In the case of the binary counter a good "handle" in many cases proves to be the positive voltage supply, $+V_{BB}$. If a circuit is near failure because of high I_{CBO} due to temperature or age, lowering the positive voltage will cause the circuit to fail. If the circuit is near failure due to a decrease in β, increasing the positive voltage above the design value will cause the circuit to fail. Upper and lower limits before failure may be set in both cases.

The design value of the positive voltage, in particular, must be determined by the highest expected temperature of operation and the ex-

pected I_{CBO} at that temperature. However, if low temperature operation is also anticipated the safety factor (S) must be chosen high enough that the decrease in β with lower temperature will not cause circuit failure. Silicon transistors must almost certainly be used if high temperature operation is desired, e.g. 150° C.

The number of component parts used in a binary counter circuit is a compromise between a conservative design using 8-10 transistors per stage with each transistor performing a simple separate function (e.g. logical binary counter) and a design using only 2 transistors. Reliability may be higher for the more conservative design, but, on the other hand, it may not be since long-term reliability varies inversely with the number of active components. Local experience has shown that the binary counter design (without the cross-coupling capacitors) performs very well for low frequency operation (less than 10kc) with the 2N207 audio transistor. With cross-coupling capacitors and using surface barrier transistors the circuit performs with greater than 10% margins up to 2 MC. If emitter-followers are added and higher speed steering gates used, the circuit will operate up to 20 MC. This last is a maximum frequency and 10 MC or 16 MC is thought to be a more practical limit, i.e., 10% or greater margins on input voltage and other design values. The binary counter presented herein represents a good compromise among the various factors mentioned. There are circuits which operate faster and there are circuits which theoretically would be more reliable for random counting in that RC time constants would not be used, e.g. the logical binary counter.[6,7]

The average cost of assembly of several breadboard systems at DOFL has been $10 per transistor and associated components. Considering the cost of the transistors, diodes, resistors, and capacitors, the type of binary counter described herein has cost about $30 per stage in a breadboard version. If the cost per transistor remained unchanged the logical binary counter would cost approximately $100 per stage in a breadboard version. Microminiaturized binary counter modules now under investigation may eventually cost in the range of $1-$3.

Third Level Design

The third level of design is that of a circuit to be used in a system where unit replacement is impossible. This situation occurs in microminiaturization.

The design requirements for a circuit to go in a sealed system are more rigorous than for a circuit which can be replaced if defective. After the circuit has been designed and thoroughly tested in a breadboard model, it is necessary to specify a rigorous acceptance or rejection test for the field models. Analysis of the circuit must be so complete that off-value, weak, or defective components can be identified merely by observing a single output waveform. This should be possible even if the circuit is not malfunctioning at the time of the observation. The circuit may then be rejected before potting or final sealing, or at least restricted to uses in which its weaknesses will not endanger future operation of the system. For instance, if it were discovered that the I_{CBO} of the transistors was higher than the design value, the circuit might still be used in low temperature applications if all its other characteristics were acceptable.

If the circuit uses standard size components the waveforms at several points may be monitored. In the case of the binary counter described in this paper the waveforms at points C and D (Figs. 2 and 3) give much information about the circuit. For instance, the decay times of the step waveforms indicate the time constants $R_K C_S$ and $R_K C_B$. These time constants compared to the input frequency show how close the circuit is to its maximum frequency of operation. The voltage levels at points C and D indicate the collector voltage of the off transistor and thereby indicate the I_{CBO}. The height of the positive spike can be used as a measure of the charge required to turn off the "on" transistor if the input signal and diode characteristics are known. This height indirectly measures the alpha cutoff frequency of the transistors in the binary counter. The points C and D in a binary counter would then be good points to monitor for an acceptance test.

In the microminiaturized DOFL-2D binary counter wafers now being studied only one output terminal is available.[8] This point is the output of one collector which would normally drive the following stage. The resistors in this wafer are carbon deposited strips, the capacitors are silver fired areas, the diodes are germanium dots and the transistors are bits of germanium mounted in holes in the 1/2 inch by 1/2 inch by 1/50 inch ceramic plate (hence the name 2D). Checking the internal connections with a probe and an oscilloscope is difficult unless the probe is very small. If the wafers are potted or stacked, this becomes impossible. Three different approaches have been made to find out about the individual circuits through the use of the external connections only.

First, resistance measurements have been made between all terminals taken two at a time. This method can identify some catastrophic failures and is good to detect "leakage paths." However, the test is a dc test and somewhat limited in scope.

Secondly, a series of so-called "standard tests" was set up, and run under the following conditions:

$-V_{CC}$ = -1.5 volts
$+V_{BB}$ = +1.5 volts
Input signal 1.5 volts p-p
Square wave from source as in Figure 4
R_T = 1 K at a frequency of 1 kc
Room temperature (30°)
Circuit unloaded except by oscilloscope

The following tests were performed:

(1) Output voltage was measured; waveshape noted.
(2) Positive voltage decreased to zero or until circuit fails to operate correctly. Output voltage at V_{BB} = 0 or plus bias voltage when failure occurs was measured.
(3) Upper and lower limits on input voltage before failure was measured.
(4) The collector voltage was lowered until the circuit failed. Operation at -3 volts was also checked (yes or no)
(5) Maximum resistive load and maximum capacitive load before failure was measured.
(6) Upper frequency limit was determined. Also, resistor R_T was varied from 100 to 10 K and the upper frequency limit was noted at each value of R_T.
(7) Circuits were labelled and any anomalies noted.

The expected results of the standard tests can be computed from the circuit design. These results are then compared with the results obtained from a breadboard model. Any differences are corrected by improved theory and re-design. Next, the results from the 2D wafers are compared with the breadboard circuit results. Any differences will be due to off-value, weak or defective components. In some cases the values of the components in the circuit (2D) can be determined and if they are too far off, the information can be fed back to the makers of the 2D wafers.

The third method of analysis which has been tried is as follows. Resistors, capacitors and diodes in a breadboard model of the binary counter are systematically bridged, shorted or opened. Also, transistors with very high β and very low β are substituted in the unit. The effect of these mutations is observed on the accessible waveforms, in the case of the 2D binary counter, the output waveform. Knowing these causal relationships a first order analysis of the circuit condition can be made by carefully observing pips, slopes and amplitudes of the output waveform.

Summary of Third Level Design

The additional problem encountered in third-level design, or the design of units for non-relaceable enclosure in field equipment, is the development of a rigid acceptance or rejection test. This test must do more than give a yes, no answer to the question, "Is the circuit working now?" The test must determine whether the margins of the circuit are large enough so that the circuit will continue to operate for a time longer than the projected life of the piece of equipment. This may be shelf-like or operational-life or both. Three methods have been presented for use in such a test. The first uses resistance matrix methods, the second uses a series of "standard tests" and the third uses a detailed waveform analysis. The waveform analysis seems the simplest to use if enough information can be gotten from it. However, this method also requires the most complete circuit analysis. It may further require specially trained personnel or special equipment to implement the tests.

Conclusions

The binary counter is now being studied from the standpoint of a third-level design. Attempts will be made to refine the technique. Other circuits will also be studied from this standpoint. The application of a thorough design procedure, as exemplified by the three-level design, will result in more reliable electronic systems for both military and commercial uses.

Acknowledgments

The author wishes to acknowledge the helpful discussions with T. A. Prugh during the preparation of this report. The author also wishes to thank N. J. Doctor, Amiel I. Goodman and E. L. Cox for their contributions to the formulation of the test procedures described in this paper.

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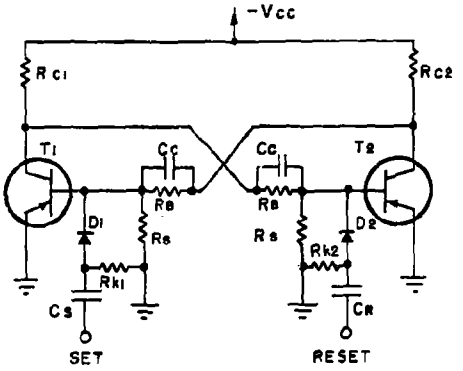

Figure 1. Two-Transistor Flip-Flop With Set and Reset Networks

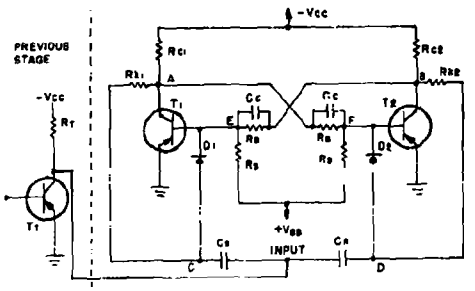

Figure 2. Two Transistor Binary Counter

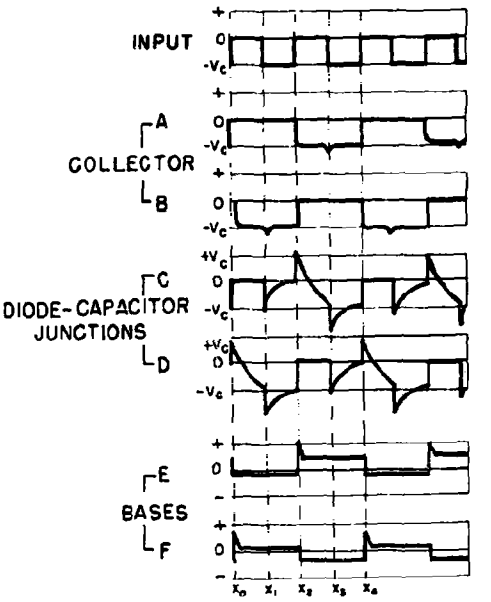

Figure 3. Waveforms in Two Transistor Binary Counter

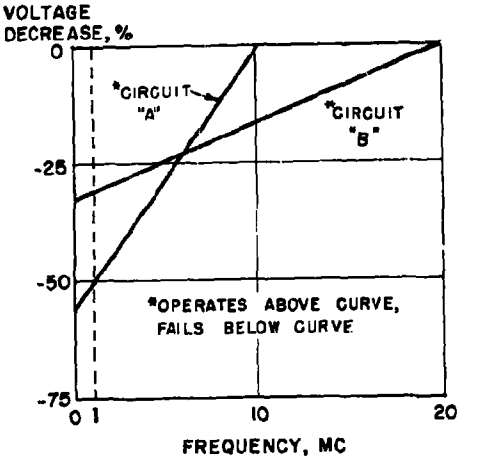

Figure 4. Input Voltage Decrease Before Failure vs. Counting Frequency

PROGRESS IN THE ARMY MICRO-MODULE PROGRAM

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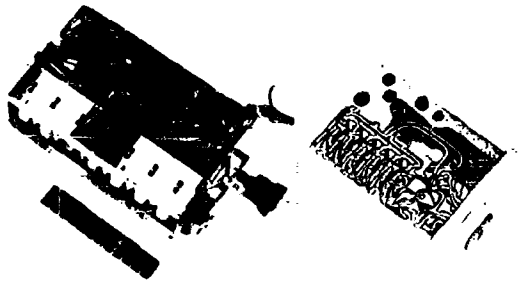
Army Signal Corps progress toward miniature electronic equipments exploting the transistor and printed circuits, will be reviewed. Micro-miniaturization objectives will be quantitatively developed. The criteria which guided the establishment of the Army's definitive Micro-Module program will be presented. The specific functional objectives of the Army Micro-Module program in terms of audio, IF, RF and computer circuits will be presented. The range of Army tactical environments from portable and ground equipments thru missile and satellite environments will be discussed as micro-module requirements. Reliability attributes and requirements of micro-modules will be analyzed. Recently developed Micro-Miniature techniques adaptable to Micro-Modules will be reviewed. Individual component capabilities and solid state circuits available at present and anticipated in the near future will be presented. Effect of Micro-Modules on Army Electronic Equipments will be discussed. Overall advantages to the Army in terms of increased tactical capabilities, (namely size reduction, reliability increase, cost reduction, and maintenance reduction) thru broad use of Micro-Modules will be given.

Extensive effort has been applied in the field of microminiaturization in the past two years....(1,2,3,) and some examples of effective microminiaturization can be cited to show that progress is being made. But this growth of our microminiaturization capabilities has been random and uncoordinated....lacking unity in the goals being sought and in the methodology employed. Prior to the advent of the transistor and printed circuits, the zenith of accomplishment in practical miniaturization capability was typified by the Army's Handy Talkie. The density of the parts packed into this chassis is about 8000 parts/cu. ft. (Fig. 1a). A very substantial further miniaturization and simplification of manufacture of military electronics, resulted from the use of transistors and solder dipped printed wiring.



(a) (b)

Figure 1. - Army's Handy Talkie (a) and Helmet Radio (b).

These tools have been applied to the Army's Helmet Radio, (Fig. 1b) an extremely compact receiver-transmitter with an orderly disciplined layout, making much better utilization of space. Here we have improved our miniaturization capability about 6 fold, from the 8000 parts/cu. ft. for the handwired set over 50,000 parts/cu. ft. for the printed circuit design.

We recognize however that we are reaching a new limit to size reduction with presently available construction approaches....a new plateau, so to speak, beyond which we see only small incremental improvements toward the more compact requirements demanded for Army electronics.

The Army micro-module program offers a practical, feasible approach which will permit the attainment of packaging densities of 500,000 parts/cu. ft. The key to this system is simple.. ..all the elements (the resistors, capacitors, inductors, transistors and so on) have similar physical size and shape so that they can be very efficiently stacked with each other. An aggregate of stacked elements is appropriately interconnected with riser wires, is encapsulated and becomes a monolithic non-repairable body. This body called a micro-module performs a circuit function and in effect becomes a sub-assembly of a completed equipment. The micro-module system will be capable of performing a full range of basic electronic circuit functions involving a 1 to 2 watt maximum power dissipation per module, an initial upper frequency limit of 70 mc with progressive capability to 150 mc and maximum digital switching rate of 10 mc.

Specific micro-modules will be designed and constructed to demonstrate and to provide for adequate evaluation of a full range of basic audio, I-F, RF, digital computer, and oscillator circuit capability.

We have divided the Army equipment into five categories each of which we associate with a unique set of environmental requirements. These requirements are spelled out quantatively as the goals of the full micro-module program (Fig. 2). The spectrum of temperature requirements for these equipments, ranges from -55°C to 85°C for ground portable devices, projectiles and satellites up to 200°C for vehicular and missle applications. The range from 85°C to 125°C is our goal for the first two year phase of the program. Vibration requirements range from the standard 10 to 55 cycles for the found and vehi-

ENVIRONMENTAL SPECTRUM

	AMBIENT TEMPERATURE RANGE °C	VIBRATION CPS	ALTITUDE FT.	SHOCK G	SPIN RPM
PORTABLE	-55 To +55	10-55	10,000	20	
VEHICULAR	-55 To +125	10-55	10,000	20	
GUIDED MISSILE	-55 To +200	10-2000	150,000	20	
PROJECTILE	-55 To +55	10-2000	150,000	15,000	20,000
SATELLITE	-55 To +125	10-2000	VACUUM	15,000	20,000

Figure 2. - Categories of Army equipment, and environmental requirements for each category.

cular equipments to 10 to 2000 cycles up to 20 g's for the other equipment categories. The ability of Army equipments to work in their extreme air pressure environments is defined by the following requirements: Portable and vehicular equipments must operate without malfunction of any kind at altitudes up to 10,000 ft. Missile and projectile altitude extremes have been set at 150,000 ft. The satellite electronics environment has been set down as dead vacuum for all practical purposes.

All micro-modules will be required to withstand 50g, 8 millisecond shocks as a minimum. In addition the projectile and satellite modules will be required to withstand 15,000 g's of 8 millisecond duration as well as a spin of 20,000 rpm.

Other standard tests such as high and low temperature and long term storage, moisture and temperature cycling and salt tests complete the list of Army tactical environments to which the micro-modules will be subjected.

Reliability goals have been expressed in terms of mean time to failure for a 50 part module. Basically, the 50 part module reliability requirement is for 15,000 hours or about 21 months mean time to failure within the temperature range -55°C to 85°C and under the various Service environments just discussed. Probably a more familiar way to interpret this initial goal is an average part failure rate of about one tenth of 1%/1000 hours.

It is believed that this goal can be reached because of the following inherent reliability advantages of micro-modules:

First there is the basic simplicity in circuit part construction; next, is the fact that the circuits and micro-elements are simultaneously designed for compatibility. Third, is the complete freedom to explore new materials, configuration processes and assurance measures, without being limited by conventional state of the art. Fourth, the high degree of automation toward which micro-modules have been tailored means greater uniformity and more reproducible reliability. Fifth, reliability risks due to improper electrical and mechanical application of parts would be eliminated. And finally, the rigid one piece construction offers extreme ruggedness.

A typical example of the effect of micro-modules on Army Electronic equipments can be illustrated by the electronics contained in a satellite. (Fig. 3) They consist of disks five inches in diameter and three-quarters of an inch thick. Six of them are stacked, and with their battery supply fill a cylinder 8-1/2" long. Also shown on the extreme right is the micro-module equivalent which is 1/10 the size. The size differential is really significant, and should be considered from two points of view:

(1) In terms of the reduction in the number of pounds of dead weight and fuel required to propel the smaller package into space, or

(2) If the total size and weight is not changed how much more electronics could be crammed into the satellite. The added electronic circuitry could serve a variety of functions such as increased instrumentations.

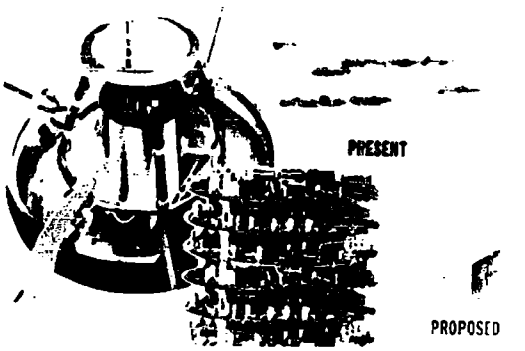


Figure 3. - Present and proposed micro-module version of Vanguard satellite equipment.

Our micro-module program will increase the Army's tactical capabilities first by reducing the massiveness of our new electronics by a factor of ten; second by gaining greater performance dependability of micro-module circuitry due to superior shock and vibration resistance of these tiny aggregates; third by reducing the economic burden of our growing electronics. It is expected that up to 50% cost reduction will be realized in the construction of finished equipments in large quantity production using this concept. The fourth tactical advantage, reduced maintenance, perhaps can be best expressed this way: If we had this concept in full effect today, we could keep our current equipments in combat readiness with only 1/5 of the present technical manpower and maintenance monies.

(4) Now I would like to review the progress to date on the micro-module program in regard to the wafers, resistors, capacitors, inductors and crystals, scheduled for intial micro-element design. Major effort is directed towards ex-

ploiting existing state-of-the-art to the micro-module concept through appropriate design re-packaging.

First let us look at the micro-element wafer. (Fig. 4) The current design has 12 notches and is .3" x .3" sq. x .010" thick. Wherever possible, the substrate wafer will be functioning part of the micro-element. In certain applications, it will be used as a support for the element. Of the many substrate materials investigated, alumina and glass show the most immediate promise.

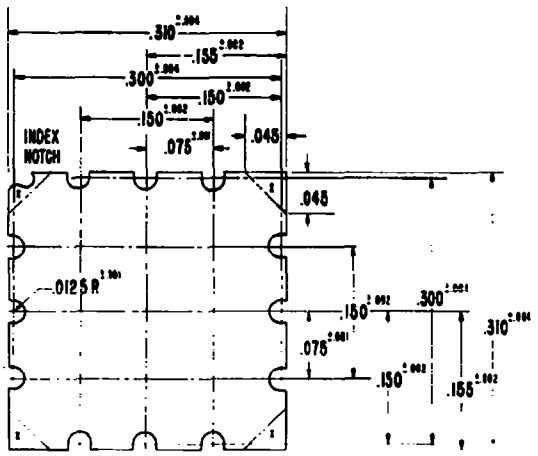


Figure 4. - Standard substrate wafer for micro-module program.

The methods of assembly of the micro-element into the micro-module, whether it is used as a support or as a functioning wafer in the module, are being investigated. (Fig. 5) One possible solution is the use of conventional riser wires which are soldered to each of the wafer notches. Another assembly method under investigation is the use of wafers without notches, where the

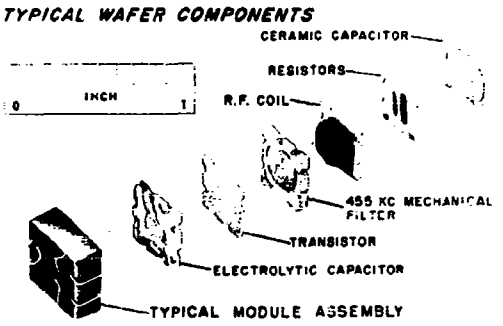


Figure 5. - Typical wafer components for micro-modules.

riser wires are welded directly to the wafers. The inherent advantages of using the unotched wafers are greater soldering surface, more adaptable to welding techniques, and increased clearance between risers, which are rectangular in cross section.

Shown at the top of Fig. 6 is a commercial precision metal film resistor element evaporated on the glass substrate which is approximately 40 mils thick. It has been cut out of its overall protective envelope. Directly below is the .3 x .3 inch micro part shape. The active resistor area of the element shown on top is approximately .08 square inches. At the present time, only nichrome and tin oxide film resistors on glass substrates will be considered. Since the resistor covers an area where a great deal of experience exists in industry, an appreciable portion of the effort has been spent in attempting to determine suitable subcontract sources. RCA is now negotiating with several resistor manufacturers for the purchase of either a nichrome or tin oxide element on the .3 x .3 x 10-mil wafer. The completed wafer will then be evaluated for conformance to specification requirements. Resistors of ohmic value ranging from 1,000 ohms to 110,000 ohms have been made from nichrome films evaporated on .3 x .3 x 10-mil glass and were found to have excellent TC and stability characteristics.

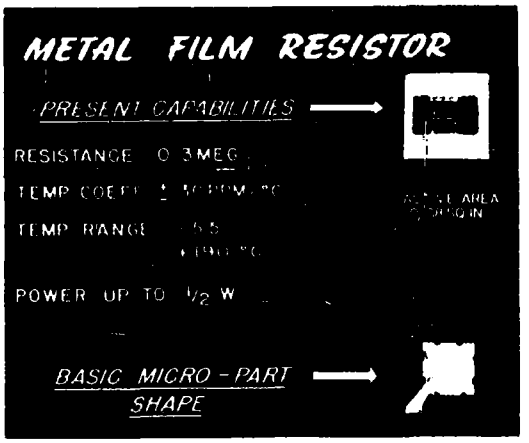


Figure 6. - Commercial metal-film resistor compared in size with basic micro-part.

Let us now review the capacitor progress.

The capacitors fall into three basic categories:

1) Precision

2) General Purpose

3) Electrolytic

Shown in Fig. 7 is a typical micro-element capacitor. The substrate is actually the dielectric for the capacitor. By using different materials as the dielectric the characteristics of the units can range from precision temperature coefficient types to general purpose, high capacitance, by-pass, and coupling units. Capacitance values as high as 1,000 mmf for the precision types can be obtained on the single wafer. By making use of the extremely high dielectric constant materials we are able to achieve capacitance values as high as .2 mfd per wafer. Micro element capacitors with dielectric constants varying from 15 to 6,000 are being purchased by RCA.

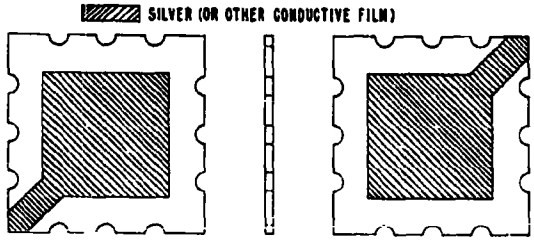


Figure 7. - Capacitor micro-element.

In addition to the basic ceramic wafer capacitor an evaluation is being made of the multi-layed capacitor. In this case, a number of layers of dielectric and electrodes are deposited on a ceramic substrate. The dielectric will vary from approximately 15 to 8,000 again covering the precision and general purpose applications. Purchase orders have been placed for a quantity of these multi-layer capacitors.

Work on an entirely different system of producing thin film capacitors is being actively pursued. The film consists of titinate particles in the matrix of SiO_2 (fused quart structure) producing dielectric constants from 4 to 80. The useful thickness of the film is approximately .8 mils with an 0 temperature coefficient and with Q's approaching a thousand and yielding a capacitance of 600 mmf per micro element.

Electrolytic capacitors will be used to cover the capacitor range from 0.2 to several microfarrads. The solid tantalum capacitor is ideally suited for this application. A sintered slug approximately 20 mils thick has been produced and adapted to the micro-element design yielding a capacitance of approximately 10 mfd. Another material, columbium, is also being evaluated for use in electrolytic capacitors. The sintered slug used in the construction of the solid unit may possibly be used as the basic micro-element part.

Now let us look at the progress on inductors.

Toroids have initially been chosen for the inductor since they permit achievement of higher inductances and less stay magnetic fields compated to other known configurations. Fig. 8 shows a toroid coil mounted on a micro capacitor element comprising a tuned circuit.

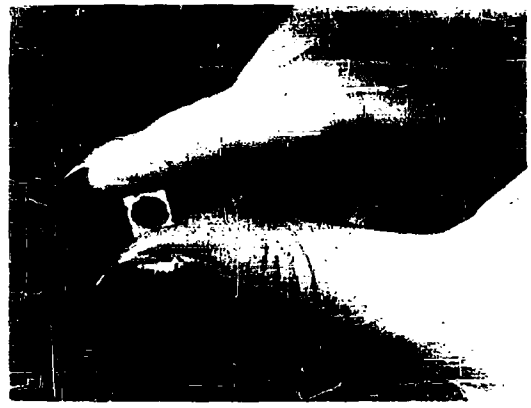


Figure 8. - Tuned-circuit micro-element.

Since, in this configuration, the coil characteristics are almost completely controlled by the core material, in this case ferrite, major effort has been expended on control of material properties.

Work to date has resulted in a ferrite material whose temperature coefficient of permeability can be controlled from -200 to $\pm$ 5,000 ppm/°C with a tolerance of $\pm$ 56 ppm/°C. Coils having the required inductance and Q have been made on a .2" OD toroid.

The final item that I will review is the Quartz Crystal.

Quartz crystal units, used for frequency control applications, are capable of being reduced in size to be compatable with other portions of the Micro-Module Program.

Presently we are concerned with the status of crystal units in the 7 to 70 mc range. On the left hand side of Fig. 9 is the sub-minia-

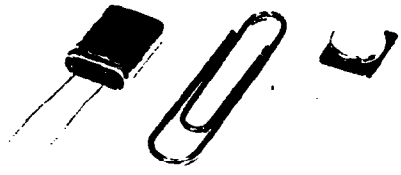


Figure 9. - Comparison of size of cased conventional and micro-module crystals.

ture holder which is now used.

On the right side is shown a 8 mc crystal mounted in a plastic holder to demonstrate one form for a MM crystal. Final fabrication would contemplate a ceramic holder 1/16 the size of the unit on the left.

Present plans call for fundamental crystals from 7 to 20 mc and overtone units from 20 to 70 mc. The tentative power ratings are 5 mw and 1 mw for the respective types.

1. Conference on Modular Electronic Packaging, ABMA, Huntsville, Alabama, 23-24 July 1958.

2. Professional Group on Production-Techniques Sysposium, New York City, 6 June 1958.

3. Army Signal Corps Presentation on the Micro-Module Program, Washington, D. C. 3 June 1958.

4. First Quarterly Progress Report Contract DA36-039-SC-75968.

TWO-DIMENSIONAL TRANSISTOR PACKAGING

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Miniaturization techniques were first successfully applied to circuit wiring and to passive components. The relatively large size of semiconductor components became the limiting factor in further reducing over-all circuit volume. To overcome the problem of the large transistor package, several techniques have been developed at DOFL for working with caseless transistors. These techniques allow the active element of the transistors to be incorporated as an integral part of a two-dimensional ceramic printed circuit plate. Foremost of these is the extension of photolithographic techniques, first developed for the fabrication of transistors, to the case where the transistor can be effectively masked and placed in a two-dimensional printed circuit plate so that the leads may be vacuum deposited to connect the base and emitter contacts to the printed wiring. In addition, two methods of encapsulating alloy-type transistors have been developed, one non-hermetic and the other hermetic. In the non-hermetically sealed technique, a low-frequency transistor is sealed in a two-dimensional printed circuit structure by inserting the transistor, collector side down, into a machined depression in which a small hole has been sandblasted through the ceramic. By heating, the collector material is caused to flow through the hole to form a contact. Connections to the printed wiring are made with a conductive epoxy silver cement.

In the second technique, the transistor is hermetically sealed, emitter and base side down, in a ceramic similar to the one above. The hermetic seal is effected by metalizing the ceramic around the depression and emitter and base holes, sealing high melting point solder over the base and emitter connection holes, and then sealing a metal plate over the machined depression which receives the transistor. The metal cover plate makes ohmic connection with the collector of the transistor. These sealed units have been exposed to various environments with no change in transistor characteristics.

Modern weapons systems require electronic circuitry which is able to perform extremely complex functions. However, the increased emphasis on computer type circuitry for such applications as guidance, fuzing and fire control has not been accompanied by any increase in the space available and in fact, because of new operational demands on the systems, there is often less space. The achievement of such complex circuitry in a limited volume has been made possible through transistorization of equipments. However, for many applications, the transistor, a miniature component in itself, is rapidly becoming the limiting factor in further reducing circuit size. This situation has occurred largely because of improved methods of printing resistors and the development of barium titanate capacitors. It is becoming apparent that the device designer must now consider the ultimate spatial utilization of his device as well as its electrical characteristics.

The case of the smallest hearing aid type transistor occupies a volume of 1700×10^{-6} in^3 and if lead connections are considered this is increased still further. Compared to a 10K printed resistor with a volume of 0.8×10^{-6} in^3 and 0.01μf barium titanate capacitor with a volume of 60×10^{-6} in^3, it seems truly gigantic. However, the active volume of a high frequency transistor, defined conservatively as the volume of the semiconducting material, is only about 15×10^{-6} in^3. If the transistor is to become comparable in size with the other components, its case must be discarded and its leads printed two-dimensionally. This paper will describe several techniques which have been developed at DOFL for working with caseless transistors.

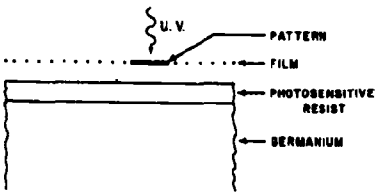
*Present address: Texas Instruments Inc.

High Frequency Transistors

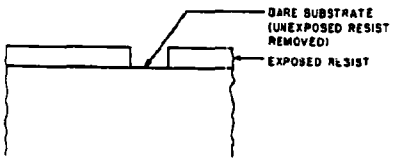
As the operational frequency range of transistors is extended, the dimensions must necessarily shrink. One of the most exacting operations involved in fabricating high frequency transistors is the attachment of leads to the small active areas. A photolithographic technique has been developed which permits connections to be made to these areas and at the same time allows the transistor to become an integral part of a printed circuit. In this technique, parts of the transistor are selectively masked with an insulating film, over which connections may be vacuum deposited. The principle is illustrated schematically in Figure 1. The presensitized coating (resist) is all organic and is applied in liquid form and allowed to dry. When dry, it is exposed to ultra-violet radiation through a suitable pattern or mask. Portions of the coating which are not exposed to the ultra-violet will be removed by the developing process, revealing the original substrate. Leads may now be deposited which contact the device only at these points where the resist has been removed.**

An example of the use of this process is found in making the connections from a diffused base type transistor to the wiring on a ceramic printed circuit board. The transistor (which itself is made by photolithographic techniques) is shown in Fig-

**For details of coating and fabrication techniques, see DOFL TR-608, "The Use of Photolithographic Techniques in Transistor Fabrication (U)", J. R. Nall, J. W. Lathrop, 1 June 1958.

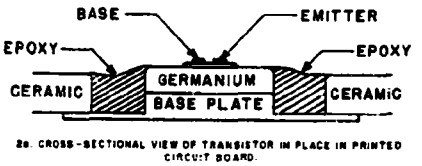


A. Pattern exposure process.

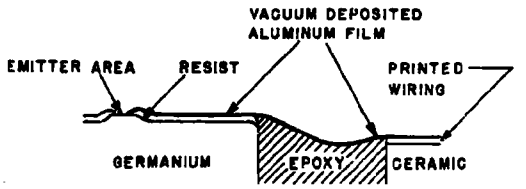


B. Surface after development.

Figure 1. Exposure and development of a photo resist pattern.



2b. CROSS-SECTIONAL VIEW OF TRANSISTOR IN PLACE IN PRINTED CIRCUIT BOARD.

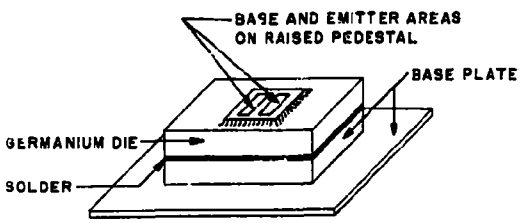


2d. CROSS-SECTIONAL VIEW SHOWING VACUUM DEPOSITED LEAD.

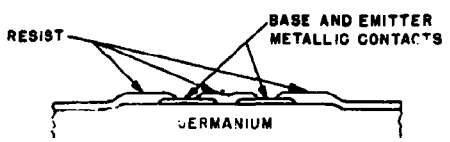
FIGURE 2. ASSEMBLY DIAGRAM.

gure 2a. The base and emitter contact, 0.004" x 0.012" each, are on a pedestal which was etched from the germanium die. The die, 0.045" x 0.045"x 0.010", is soldered to a base plate which becomes the collector contact. Photo resist is applied to the transistor surface and exposed so as to bare only two rectangular areas directly over the metallic bars as shown in Figure 2b. Note that the resist forms a protective coating over the active areas of the transistor. While obviously not a hermetic seal, field effect measurements on germanium surfaces exposed to various ambients indicate that this coating does give some added short-term stability to the device. The transistor with the resist coating is next inserted into a hole in the ceramic board and the space between the transistor and board filled in with an epoxy resin as shown in Figure 2c. The epoxy need have no special properties as far as the electrical operation of the device is concerned since it does not come in contact with any of the active areas. Mechanically, the resin serves to attach the transistor firmly to the printed board and at the same time forms a bridge upon which the leads will be deposited. Epon 828 has served satisfactorily.

The final step in the sequence is the actual deposition of the leads. For large areas the leads can be screened on, but for dimensions like those discussed here, vacuum deposition is much more satisfactory. Mechanical masking is used to confine the deposited area during deposition.



2a 3-DIMENSIONAL VIEW OF TRANSISTOR SOLDERED TO BASE PLATE.



2c ENLARGED CROSS-SECTIONAL VIEW OF TRANSISTOR SURFACE

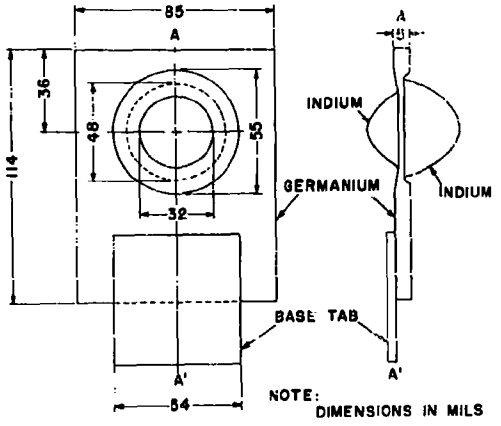
FIGURE 2. ASSEMBLY DIAGRAM.

Figure 3. Leads Vacuum Deposited to Base and Emitter.

This masking need not be exact; it is only necessary that the two areas on the transistor not be shorted and that they be electrically connected to their respective printed leads on the board. One half of the completed unit is shown schematically in Figure 2d. Figure 3 is a photomicrograph of a unit with evaporated leads.

Low Frequency, Non-Hermetically Sealed Transistor

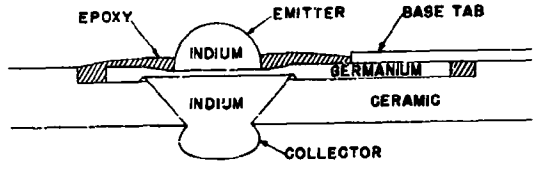
The dimensions of a typical low-frequency germanium alloy transistor are shown in Figure 4.



TYPICAL LOW-FREQUENCY GERMANIUM ALLOY TRANSISTOR.

Figure 4.

The emitter and base connections are made on one side of the die while the collector is made on the other. The grooves around the emitter and collector are made by electrolytically etching the device. This is standard semiconductor practice, following alloying, to remove any material shorting the junctions and to give a low surface recombination velocity. Figure 5 shows how this type of unit may be incorporated into a printed circuit. A ceramic board, 0.020" thick, which has the printed wiring and resistors on it, is machined to give a level rectangular depression approximately as deep as the thickness of the transistor die and slightly larger in area. At the point in the depression where the collector will fall, a hole with tapered sides is sandblasted through the ceramic. The transistor is now coated with a photosensitive lacquer and allowed to dry. The lacquer is applied so as to form a thin protective coating for the transistor in order to prevent shorts during the following steps. The transistor is then inserted into the depression collector side down. Since the conical hole is smaller than the indium collector, the transistor will not lie flat in the bottom of the depression. The transistor and ceramic circuit board are raised in temperature to above the melting point of indium and pressure is applied to the top side of the die. This forces the molten indium of the collector to completely fill the tapered hole, with some indium even passing through and forming a ball on the other side of the ceramic. The conical shape of the hole minimizes spreading of the indium and the photosensitive lacquer coating of the transistor prevents shorts from occurring if spreading does occur. Epoxy is now placed around the transistor, filling the space between the die and the ceramic and also covering the exposed semiconductor surface but not the emitter or base tab. After the epoxy has set up, the excess indium on the emitter is removed so that it is level with the epoxy surface. The indium from the collector which has formed a contact on the other side of the ceramic may be connected to the printed wiring. Connections from the emitter and base tab to the printed wiring on the ceramic surface are made with a conductive epoxy silver cement.*



TRANSISTOR INTEGRATED INTO PRINTED CIRCUIT BOARD.

Figure 5.

Low Frequency, Hermetically-Sealed Transistor

The type of construction described above serves to incorporate the transistor in a printed circuit, but does not in any way serve to protect the device from ambients. Presumably, the entire circuit would have to be encapsulated under these conditions. It is possible, however, by some modification of the processing to provide only the transistor with a hermetic enclosure and at the same time retain the two-dimensional printed circuit structure.

The method of construction is shown in Figure 6. A rectangular depression is machined in the ceramic printed circuit board approximately two to three times as deep as the thickness of the transistor die and slightly larger in area. Two holes with tapered sides are sandblasted through the ceramic in the recessed area as shown.

The ceramic is metalized and coated with an indium solder around each hole on the one side and around the periphery of the depression on the other. The ceramic is metalized: (1) around the

* T. J. Kilduff and A. A. Benderly, "Conductive Adhesive for Electronic Applications", Electrical Manufacturing, June 1958, pp. 148 - 152.

base and emitter holes in a circular pattern fifty mils in diameter, (2) around the periphery of the rectangular recession in a strip 30 mils wide. These indium solders have different melting points; the former, indium-silver, has a melting point in the order of 230°C; the latter, indium-tin, 117°C. The process of metalizing the ceramic is essentially that given by Nolte and Spurck* and involves firing coatings of molybdenum and manganese at 1350°C in wet hydrogen. The moly-manganese mixture forms a chemical bond to the ceramic under these conditions, insuring a true hermetic seal. Nickel oxide is then coated over this metalized surface and reduced to give a layer of nickel. In order to facilitate wetting by the indium solders, a layer of gold is deposited over the entire metal surface by immersing the ceramic board in a gold displacement bath.

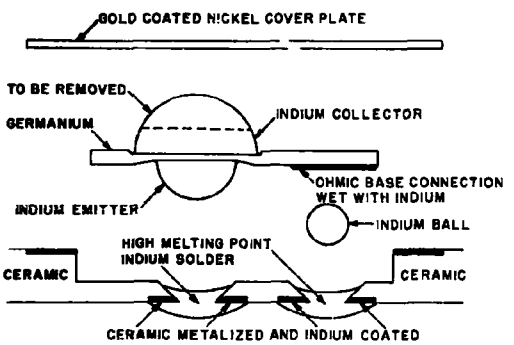


Figure 6. Cross Sectional View of Components for Hermetically Sealed Package.

After the transistor has been coated with the photosensitive lacquer, the base tab is removed and an ohmic connection made to the base; tin solder, for example. This ohmic connection may be coated with indium to insure good wetability during subsequent processing. Previous to inserting the transistor into the ceramic, the ceramic is metalized and coated with indium as mentioned above. When the high melting point indium solder is applied to the metalized surface around the base and emitter holes, it fills the lower portion of the hole cavities while at the same time wetting the gold around the holes. Since this solder melts at 230°C, it will not be disturbed during subsequent operations where solders having lower melting points are used. A ball of indium is placed in one of the holes and the transistor placed over it in the depression so that the emitter falls in the empty hole and the base contacts the indium ball in the other. The ceramic and transistor are raised in temperature above the melting point of indium and pressure is applied as before. This forces the indium into the two holes and at the same time causes the ball to wet the ohmic base connection. Epoxy is now placed around the recessed transistor, filling the space between the die and the ceramic and also covering the exposed semiconductor surface except for the raised collector contact. After the epoxy has set up, part of the collector is removed to the level of the epoxy surface and the cover plate is soldered on. The melting point of this solder, as mentioned, is 117°C. In soldering the cover plate to the metalized ceramic in an inert atmosphere, a solder connection is also made between the plate and the collector. Thus, the transistor is completely sealed in an inert atmosphere in a ceramic package only 0.020 inches thick. Examples of this type of construction are shown in Figures 7 and 8.

* H. J. Nolte and R. F. Spurck, Television Engineering, p. 14, November 1950.

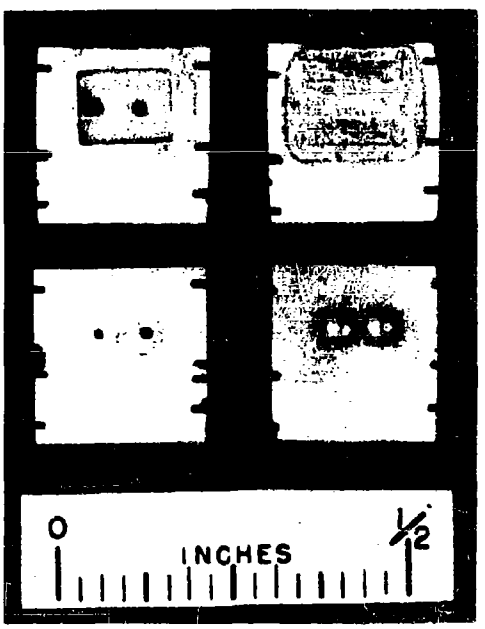


Figure 7. Top and Bottom View of Unfinished and Finished Hermetically Sealed Package.

Left - Top and bottom view of ceramic prior to insertion of transistor and final sealing. The ceramic is metalized around the periphery of the recession in the top view and around the base and emitter holes in the bottom view.

Right - Top and bottom view of the finished hermetically sealed assembly. The collector side of the transistor has been sealed with the nickel plate as shown in the top view, while the base and emitter contacts have been sealed by the solder which has wet the metalized ceramic and partially filled the hole cavities.

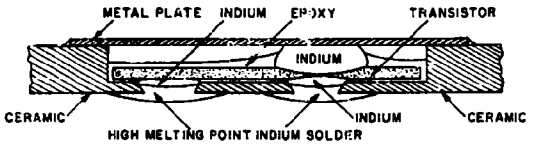


Figure 8. Cross Sectional View of Hermetically Sealed Transistor Package.

These units have been exposed to an ammonia vapor for thirty minutes and to an atmosphere of 95% humidity and 71°C for a period of sixteen hours with no change in transistor characteristics.

Acknowledgements

The authors wish to express their appreciation to the following people for their assistance in the preparation of materials and fabrication of devices: Mr. Robert Martin, Mr. Gerald Wetzel and Mrs. Margaret Jones.

THE USES OF THIN FILMS IN MICRO-MINIATURISATION OF ELECTRONIC EQUIPMENT

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A survey is made of recent advances in thin films (< 0.001 in.) of various types in the United Kingdom. They are discussed as conductive, partly conductive and non-conductive for inter-component connections, resistors and capacitors respectively. Some work on magnetic films is also described.

For resistors, oxides or alloys of metal produced either chemically or by evaporation, are considered, their stability and properties discussed.

For capacitors, anodic films of aluminium or tantalum are satisfactory for high values of capacitance where a fast response is not essential; ceramic or plastic films are best where it is. Plastic films are being produced in copolymers of styrene with excellent thermal characteristics.

The problem of combining organic and inorganic techniques and requirements in the finished 'solid circuit' units are considered in detail.

1. INTRODUCTION

The semiconductor diode and transistor have made it possible to make very small units. The associated passive elements such as resistors, capacitors, inductors, etc. are considerably larger than is required in view of the small wattage dissipation, low impedance and low voltage operation which are characteristic of the transistorised circuit.

A common shape for components is cylindrical, but this is limited in the degree to which it can be miniaturised, and the associated leads already present problems of reliability. In any typical tubular component most of the available volume is taken up by material which plays no part in the electrical performance. Examples of this are shown in Figure 1. When used in power dissipating circuits with valves or power transistors, the resistor mass itself provides a high thermal capacity and thus evens out any hot spots. As, however, the heat is dissipated by a combination of conduction through the leads and radiation from the surface, a high surface area together with robust leads is desirable. In this respect the cylindrical shape of both body and leads is far from ideal, possessing a low surface area to volume ratio - only the sphere has a lower ratio. In each case an increase in power loading could be made by opening out the cylinder and its leads into flat strips. This can result in an increase in the wattage loading, or the size for a given rating can be made very much smaller.

The requirements for thin films are suggested to be as follows:-

(a) For resistance films of 200-500 ohms per square - a thickness of a few hundred Å.

(b) For high value capacitative films $> 0.1\ \mu F$ - a thickness of 0.0001 inch.

(c) For inductive films - a thickness of 200 - 300 Å. (Above this eddy current losses can be appreciable.)

2. SUBSTRATES OR BASE MATERIALS

The three classes of material which can be used are:-

(a) Inorganic materials (ceramics, glasses, etc.)

(b) Plastic materials (P.T.F.E. - Teflon - etc.)

(c) Semiconductor materials (silicon, germanium, etc.)

Ceramics are probably the simplest to use as it is possible to deposit silver or other compositions by chemical means or by evaporation. By the choice of a suitable permittivity material, high value capacitors may be obtained by metallising both sides of the base.

Plastics do not make good bases; although they have excellent electrical properties, their low resistance to heat precludes their use in "fired-on" processes, while their high vapour pressure and occluded gases make them difficult to use in vacuum systems.

The use of a sheet of semiconducting material - such as silicon - as a base is very attractive as by suitable alloying and doping, the active elements can be produced directly on to the substrate instead of being added separately as is required when using other materials.

3. APPLICATIONS OF MICRO-MINIATURISED UNITS

At present it is only possible to foresee the application of micro-miniaturisation to simple sub-units such as those used in computors.

Such sub-units are required in large quantities with identical or similar characteristics; they are of low impedance and low frequency and use low voltages with quite small currents. Where high frequencies are involved there are problems of cross-talk and drift to consider.

These sub-units consist essentially of switching circuits and use is made of semi-conductor diodes as circuit elements. A typical circuit is shown in Figure 2 - an arithmetical stage for a data processing computor.

4. THE PREPARATION OF RESISTIVE FILMS

Resistors of platinum/gold alloy deposited on to glass have been developed[1] at the Royal Radar Establishment and are now in production[2]; they have excellent temperature coefficients and are very stable. An alloy of 80 per cent gold and 20 per cent platinum gives a resistivity of 60 microhms-cm. in a thickness of 1000 Å with a temperature coefficient of 0.025 per cent, while an alloy of 60/40 gold/platinum has a resistivity of 75 microhms-cm. in the same thickness and its temperature coefficient is then 0.06 per cent.

The method of manufacture is as follows. A flat, glass disc is coated with the alloy and glue. After degreasing, a thin, uniform film of precious metal resinate is applied to the surface by spinning. The coated disc is fired to burn off organic matter and a film of photo-sensitive glue is spun on. A pattern of 24 resistive elements is obtained by exposure to ultra violet light through a negative made from a previously prepared master. After development in water, the unexposed portions are removed by etching. The width and pitch of the pattern are calculated to give the right value of resistance. The developed pattern is hardened and the unexposed portion of metal film is etched away.

The glue pattern is removed and silver electrodes are applied by a silk-screen process. The disc is then fired to bond the silver electrodes to the resistive elements to provide a reliable, noise-free joint. The elements are protected with silicone lacquer and the single units are cut from the disc. Fixing leads to the electrodes with 300°C solder completes the making of the resistor.

The final value of resistance is adjusted by cutting through the requisite number of trimming bars. By suitable design of the master an accuracy of 0.1 per cent is obtainable. The complete stages in the process of manufacture are shown in Figure 3.

So far this process has only been applied to making actual resistors but by scaling it down it can be adapted to making the complete circuit. The resolution that can be obtained by the photo-mechanical process is well demonstrated[3] when it is applied to the making of transistors on a dice only 0.05 inch square.

Higher resistivity is obtained from films of nickel/chrome, and recent advances[4] in the evaporation of this alloy make this an attractive proposition. Typical properties of the alloy as used in resistors are:-

Thickness Å	Resistance ohms/sq	Temp. Coeff. ppm/deg.C
50	300	+ 24
80	210	- 38
90	180	- 27

Early experiments have shown that Ni/Cr is a very promising alloy for deposited resistors. The alloy is deposited on to a glass substrate in a vacuum of 10^{-4}mm. Hg. An alumina crucible in a heated strip is used as a source but a more convenient source is made from a conical spiral of tungsten wire coated with an alumina-water paste heated to 1750°C by means of an electric current while under vacuum. Any cracks which develop can be painted over with the paste mixture. Such sources can be used up to ten times before the alumina has absorbed so much Ni/Cr that it disintegrates.

In general, the higher the temperature of the source, the higher is the percentage of nickel in the alloy. A temperature of 1600°C will result in an alloy of 80 per cent Nickel/20 per cent Chrome which is close to that of the original.

It is essential to heat the substrate before evaporation, as failure to do so results in unstable films. A temperature of 350°C has been found satisfactory, although higher temperatures would have been used if the glass substrate could withstand it. Figure 4 shows the resistance change against temperature for films of thickness varying from 50 to 100 Å. Three Ni/Cr films were evaporated on to glass substrates, one 180, another of 210 and the third 300 ohms/square. The source temperature was 1600°C and the substrate was held at 350°C for half an hour. The lower limit before instability is about 50 Å, giving an ohms/square value of 300. (See Figure 5.) A temperature coefficient of ± 50 ppm/deg. C is very satisfactory. A value of 300 ohms/square is reasonable as it allows a 50,000 ohms resistor to be made from a 1 in. length of 0.010 in. wide line (as would be obtained from photo-etching a deposited film into thin strips).

Various methods of controlling the thickness of deposit have been tried - the most satisfactory has been that of the monitored square. A glass slide has silver electrodes between which the alloy is deposited at the same time as the work. Continuous monitoring by a bridge allows evaporation to be stopped by shuttering when the required value is reached, although some allowance is essential to take up differences during the final baking process. These variations in baking time are shown in Figure 6, where it will be seen

that on four different samples the resistivity was different after half an hour in a vacuum oven. The general tendancy was for an increase followed by a fall to the final cold value, but from these examples it is obviously difficult to predict the final value.

Because of its excellant temperature/resistance properties, this alloy is being carefully studied[5] as, even in the micro-miniaturised sub-units, a high order of stability will be required once the initial novelty of being able to make them at all has passed. However, the resistivity as given is not entirely satisfactory, because to make very small units would entail (as stated above) a line width of not more than 0.010 in. which, although practicable, in thin film form requires scrupulous care in processing with a probable high reject rate in production.

An alloy of chromium 20 per cent, iron 3 per cent, aluminium 3 per cent and nickel 74 per cent (Karma alloy) looks interesting. Early experiments in evaporation of this alloy gave a resistivity of 400 ohms/square, and evaporation at 1650°C on to a cold, glass substrate produced a film with good adhesion and apparently good stability. Work on this material continues, but at the same time alloys with much higher resistivities are being sought.

Practical resistors have been made in the way described and values up to 1 megohm have been obtained by photo-mechanical processing. A circuit using Ni/Cr resistors and nickel electrodes is shown in Figure 7.

5. THE PREPARATION OF CAPACITATIVE FILMS

Dielectrics for capacitors can be made in the form of strips or films as thin as 0.00025 in. (in glass) or 0.005 to 0.010 in. (in ceramics) but it is probably more convenient to evaporate them on to a metallic substrate which forms one electrode with a further metal evaporated layer to provide the other. Repetition of this process can build up a stacked film capacitor of high value of the type required in low impedance circuits where capacitors of values exceeding 1000 pF are more frequently used than those of lower values, and a microfarad or more is commonly used.

Single thickness films of high permittivity are attractive and, if only a few molecules in thickness, high value capacitors could be realised. A useful formula for capacitance is:

> "1,000 micro-microfarads per square centimetre in area per micron in thickness."

This formula results in a value which is approximately 10 per cent too high.

In a proposed standard[6] module of 0.31 in. square, about 1 cm. square could be considered as the working area, of which 5 mm. square could be allowed as a maximum for one component.

If a high permittivity material such as barium titanate is used, a K of 1000 can be expected; using this formula it would be possible to make a capacitor of 0.25 μF within the allotted area. Care would be necessary to ensure that its well known ferroelectric properties and its low Curie point do not interfere with its operation as a capacitor, but for use with transistors with their inherent low operating temperature this is quite possible.

Experimental capacitors have been made by producing an oxide film on tantalum[7,8] in a mixture of phosphoric acid and amyl alcohol. The dielectric thickness was about 1200 Å. After drying, a layer of zinc oxide was evaporated on to its surface and a counter electrode of silver followed. Manganese dioxide is more usual than zinc oxide, but the latter is easier to evaporate. These oxide coatings increase the breakdown voltage but the exact mechanism of its action is debatable.

A sample capacitor made by this method had a capacitance of 0.1 μF for 0.6 sq.cm. with a power factor better than 1 per cent, which is good enough to warrant further work on this system - in particular, investigating the effects of different thicknesses of zinc oxide layers on breakdown. A multi-layer capacitor can be made by utilising both sides of the tantalum and in this way a capacitance of several microfarads is obtainable.

Silicon monoxide has also been examined. Silicon and silica in the ratio of 1 : 2 were mixed together and fired in a quartz tube at a temperature of 1100°C in a vacuum of 10^{-4} mm. Hg. The silicon monoxide was evaporated from a molybdenum boat, this was followed by an evaporation of zinc oxide for the same reason as in the tantalum films. There was no appreciable difference between the use of hot or cold substrates and good, uncracked films were obtained up to thicknesses as great as 0.02 in. However, the power factor of these films was very high, at best being between 40 and 50 per cent which makes such materials of little interest for this work.

In some circuits, a rapid discharge time of less than a microsecond is required. This is not possible with electrolytic capacitors and must be considered as a limiting factor. (Whether tantalum oxide capacitors work by reason of ionic or electronic conduction is debatable. If the latter, they will have rapid discharge times.)

Apart from those mentioned, there are many materials which can be evaporated for use as capacitor dielectrics. Among these can be listed

the following:-

Magnesium fluoride
Calcium fluoride
Calcium silicate
Zinc sulphide
Lead sulphide
Cadmium sulphide

Some of these are well known as lens blooming agents, and zinc sulphide has been used extensively in infra-red detectors. With a permittivity reported[9] as 8.2 at 10^{12}c/s and measured locally as about 9 at 10^{6}c/s, it is considered to be worth examining.

To obtain high stability and low coefficient of temperature will be just as big a problem as with resistors, and very thin films will not be practicable if they are unstable. This means that as no compromise is possible between high capacitance and stability, this latter must be made the dominant factor. In consequence, it is most important to develop a multi-layer film capacitor as it is essential to achieve values in excess of 0.1 μF and preferably of at least 1.0 μF.

6. PLASTIC FILMS

Although inorganic materials can be evaporated more readily, plastics have already been made in very thin films and their progress has been sufficiently fast to justify the belief that they may be used in micro-miniaturisation techniques although they will probably be used as components to be added separately.

Following the work by The Bell Telephone Laboratories[10] on cellulose/acetate/butyrate, thin films have been made in the United Kingdom from high molecular weight polystyrene and copolymers of this with poly-α-methylstyrene[11]. These films are cast on to a carrier of polyethylene-terephthalate (Mylar or Melinex) from a solvent solution, the carrier being subsequently stripped after the film has been metallised, demetallised and slit for the making of metallised capacitors. So far very thin films have not been made - about 0.0005 in. or 5 microns being used to gain experience, as a good deal of "know how" is necessary for these processes. It is the necessity of handling on a substrate that makes it essential to use cast films; extruded films of this thickness would be far too thin and fragile to handle. A cast film limits the material to one which can be dissolved fairly readily and this is the reason that an otherwise ideal material - polyethylene-terephthalate - is unsuitable and polystyrene is preferred. The cellulose materials have a history of poor weathering in the tropics[12]; they are poor electrically and, compared with high molecular weight polystyrene, inferior in heat resistance. As developed, it is anticipated initially that 70°C will be reached as a working temperature, which will be increased to 100°C when such problems as residual solvent removal, etc. have been overcome. (The softening point of the bulk material is in excess of 120°C.)

Capacitors have been made from these films but early models have been made from multi-layer wound foils. As the final units will almost certainly be required in the form of single sheet "castellated" metallised capacitors, work has now been directed into making this type only and already the thin film has been stripped from its substrate after metallising. Demetallising and slitting processes are being developed.

The gain in capacitance/volume ratio is calculated as 5 : 1 over conventional metallised paper capacitors. It is unfortunate that polystyrene has a permittivity of only 2.5 but this is the price paid for an almost perfect dielectric material. Experiments have been made with high permittivity fillers and it has been found possible to achieve a permittivity of five while still in very thin films (0.001 in.) cast from solvent solutions.

A novel method of making large value capacitors is by using differential solvents. On to a substrate of polyester film a layer of polystyrene is cast and dried as usual. It is metallised and another insulating layer of cellulose nitrate is cast on top. As the metallised layer is not a barrier for the styrene solvent, a material dissolving in a different solvent is needed. So far, cellulose nitrate has been used experimentally and although this is by no means a good dielectric, it can be cast from solvents which do not attack the polystyrene. By building up multi-layers, say ten, it is possible to strip off the substrate as the dielectrics are strong enough in the form of laminae to support themselves. By this technique it should be possible to produce capacitors of very high capacitance per unit volume.

As the range of plastic dielectrics is constantly being extended there may be improved materials suitable for making thin films with higher permittivity and heat resistance together with freedom from pinholes. From the so-called inorganic polymers such as boron and phosphorus nitride it may be possible to produce a substrate suitable for use in evaporating plants, but with improved moulding, shaping and machining properties. In this respect, the military demand for high temperature dielectrics may result in materials suitable for this new technique, but so far in the United Kingdom experimental materials of this type have been far too brittle for serious usage.

On the whole, plastics do not seem to hold much promise for these techniques except as an interim measure for use in separate components until such time as all the components are made

in situ on a substrate which itself forms an integral part of the sub-unit.

7. THE PREPARATION OF MAGNETIC FILMS

The choice between magnetic films of metal or of ferrite is in favour of the former because they have superior physical properties and they are easier to evaporate as an alloy.

It is reported [13] that the following comparison may be made between the characteristics of ferrite and metal magnetic films:-

	Ferrite	Metal film
Speed of operation	1 μS	3 x 10 m μS
Drive Power	800 mA into 50 ohms (valve)	400 mA into 5 ohms(transistor)
Repetition rate	500 kc/s	5 Mc/s
Physical size	Similar	Similar

Both have rectangular hysteresis loops and are suitable for use in memory planes.

Most of the films consist of nickel/iron in the ratio of 8 : 2 evaporated on to a substrate heated to 300°C in a magnetic field of about 50 oersteds. Eddy current losses are high for a thickness exceeding a micron or so, and interferance between opposite domain walls can occur if the thickness falls as low as about 20 Å; the usual thickness is between 300 and 1000 Å. Crucibles of silica are used, but a big problem is in maintaining the purity of the deposited film because, as is well known, iron is very sensitive to minute traces of silicon.

Attempts are being made to deposit a conducting layer on top of the magnetic film with an intervening layer of an insulant, but so far great difficulty has been experienced with pinholes.

To be able to produce a complete memory device by deposition would be a tremendous advance over the painstaking method of ferrite-core threading practised at present, and there is the additional advantage that the speed of operation is much improved by keeping down the lengths of conductor.

8. CONSTRUCTION OF SUB-UNITS

After many years experience it is still difficult to obtain components which pass the arduous specifications set by Military and Government departments, particularly under conditions of shock and vibration. It must be assumed that these same conditions will be applied to micro-miniaturised circuits - indeed, if past experience is anything to judge by, conditions will be come more onerous.

Printed circuits, envisaged over ten years ago, are only just coming into service, and their acceptance by military departments is by no means certain in the United Kingdom even now. There is widespread suspicion that the printed circuit is only a manufacturing device that offers nothing in reliability or serviceability. There is certainly some justification for the latter belief because the printed wiring unit is very difficult to repair and requires new techniques on the part of military servicemen. The policy of replacing one sub-unit with another instead of repairing is not widely accepted in the United Kingdom, particularly by the Royal Navy, who take the view that because of limited storage space it is essential to be able to replace every small component part of electronic equipment used on ships.

A further consideration is one of economics. In a recent technical article the statement was made that it is possible to pack 1000 semi-conductor circuit elements in a volume of one cubic inch. Assuming the cost of each element to be a dollar, then a throw-away unit valued at 1000 dollars is quite uneconomic. It may be possible to build in a reliability factor far greater than any to date, but this is very difficult. In the meantime, it must be assumed that the individual parts may fail and so either the sub-unit must be cheap enough to be thrown away or simple enough to repair. If made along the lines discussed, using high stability components, it is unlikely that this latter alternative can be achieved, which means that efforts must be made to obtain far greater reliability.

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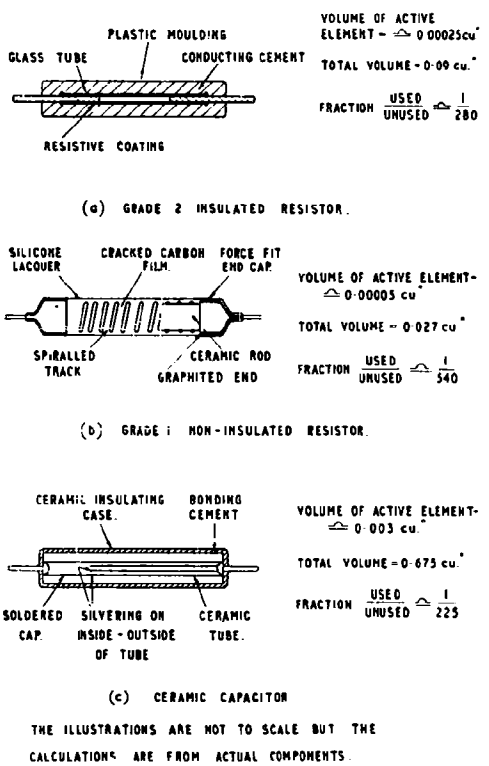


Figure 1. - Comparison between active and non-active volume of typical components.

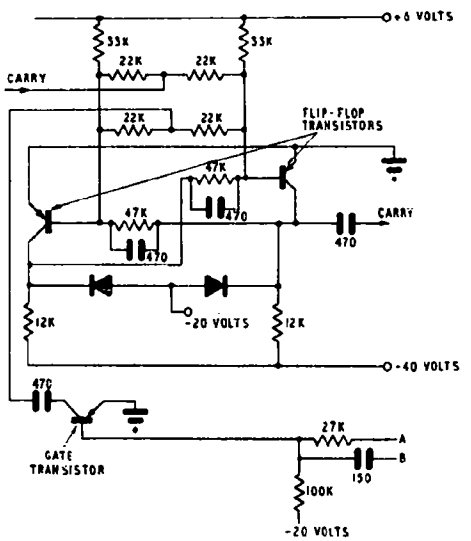


Figure 2. - Circuit for one digit of a transistor adding register and associated "AND" gate.

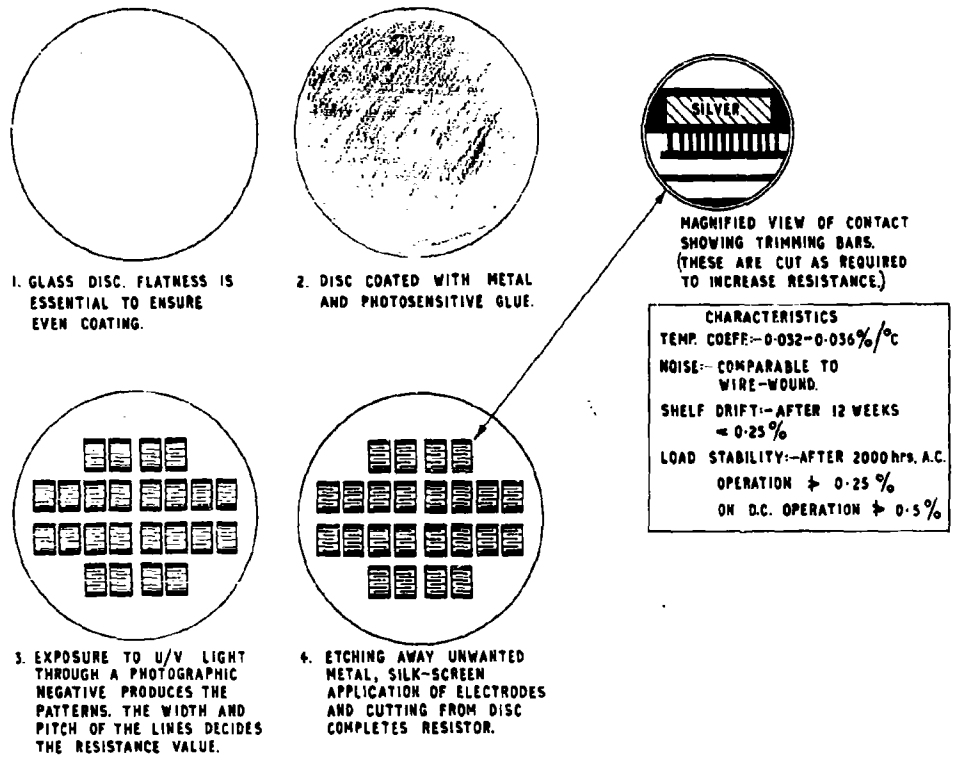


Figure 3. - Stages in the making of metal-film resistors.

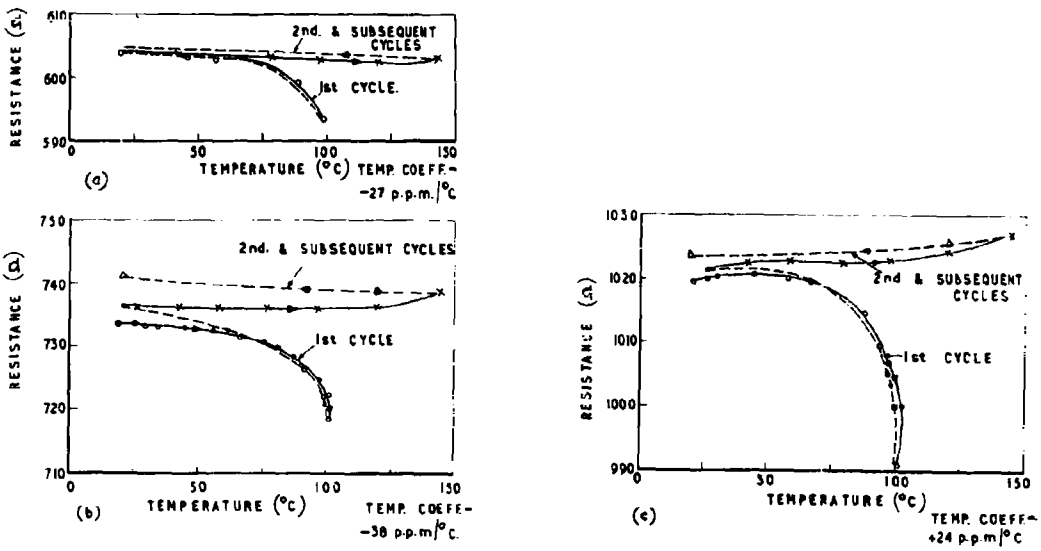


Figure 4. - Resistance / temperature characteristics of nichrome films.

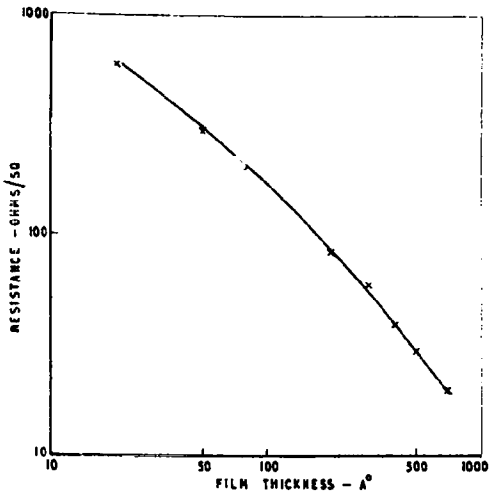
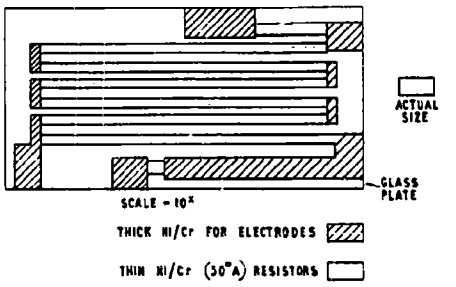
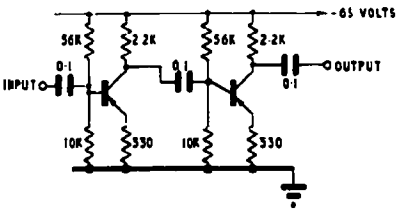


Figure 5. - Variation of resistance with thickness of evaporated film.



(a) RESISTOR AND CONDUCTOR PATTERN PRINTED ON GLASS



(b) CIRCUIT OF ABOVE AMPLIFIER (TRANSISTORS AND CAPACITORS ADDED.)

FIG.7
CIRCUIT OF SIMPLE AMPLIFIER USING EVAPORATED Ni/Cr RESISTORS.

Figure 7. - Circuit of simple amplifier using evaporated Ni/Cr resistors.

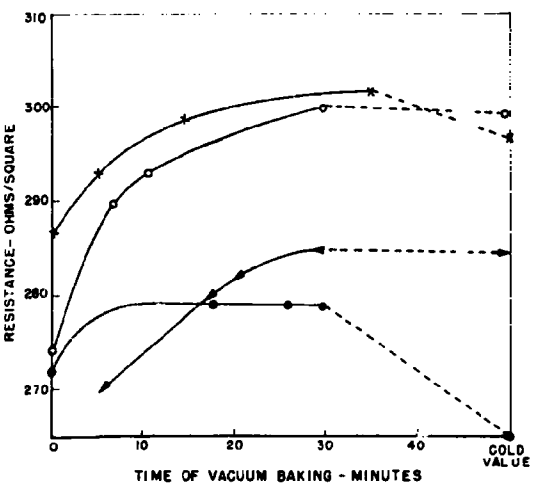


Figure 6. - Variation of resistance with baking time for four evaporated films.

LAYERIZED HIGH-DIELECTRIC-CONSTANT CAPACITORS

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Microminiature ceramic capacitors having a capacitance of about 1 μfd/in^2 and losses of 3 to 5% have been made from a very thin layer of material consisting predominately of barium titanate. The units were made by: (1) casting a thin film by a doctor-blade technique, (2) sintering a plate cut from this film, (3) reducing in hydrogen to make the plate semiconducting, (4) reoxidizing the surfaces while firing-on the silver electrodes to form an insulating dielectric, and (5) cutting the plate into 0.1-inch squares. Fabrication conditions were chosen to create the best compromise among the several desired properties, i.e. low loss, high capacitance, and high percentage of usable units. The leakage resistance of the units was found to be voltage dependent and at voltages of about two volts and below was of the order of several megohms; at higher voltages it dropped rapidly to the kilohm range. The loss showed a sharp increase above two volts. The capacitance was moderately temperature-and-voltage dependent although the curves showed no sharp peaks. Other electrical characteristics and suggested improvements are also described.

INTRODUCTION

Microminiature electronic circuit packages require physically small capacitors having capacitance values in the range of their larger counterparts. In a capacitor of small volume, the capacitance may be made large either by reducing the thickness of the unit or by employing as the dielectric a material of extremely high dielectric constant. Clearly, the maximum capacitance would result if both of these methods were used simultaneously, that is, if a very thin film were formed from a high-dielectric-constant material.

Barium titanate ($BaTiO_3$) is a ferroelectric material [1] having an extremely high dielectric constant, ca. 10^3 at 25°C. The dielectric constant is, unfortunately, temperature dependent, exhibiting at the Curie point (120°C) more than a tenfold increase over its value at 25°C. Various additives, such as strontium titanate, can be used to lower the Curie temperature to as low as -200°C [2] and thus relegate the strong temperature-dependence to a position outside the range of normal operating temperatures. Rare earth oxides also have a marked effect on the dielectric properties [3]. Barium titanate has a dielectric loss of 2 to 3% which is slightly higher than that of most other materials in use although losses can be diminished by special firing techniques [4].

When heated at high temperatures in a reducing atmosphere, the Ti^{4+} ion in the $BaTiO_3$ is reduced to Ti^{3+} by removal of an oxygen atom. This reduced titanate has a very high dielectric constant and is a semiconductor due to the loosely bound electrons resulting from the lattice defects [5]. That is, the Ti^{3+} ion can be thought of as a Ti^{4+} ion plus an electron. Under the influence of an electric field, this electron can move along the lattice from one reduced ion to an adjacent unreduced site resulting in the latter becoming a reduced site. The reduced material, even though it has a high dielectric constant, is useless as a dielectric because it is very conductive. However, if the reduced material is fired briefly in air, a very thin film of unreduced titanate should be formed on its surfaces since the missing oxygen atoms responsible for the lattice defects would be replaced in the structure. The body of the unit would still be a conductor and would consequently act like a small series resistance. Two electrodes placed on the surface films would complete the capacitor. The entire unit would be relatively thick compared to the thickness of the actual capacitive layer. A model of such a unit can be found in Figure 1. R_s represents the series resistance due to the resistivity of the inner semiconductor and R_p represents the parallel resistance due to the resistivity of the reoxidized films.

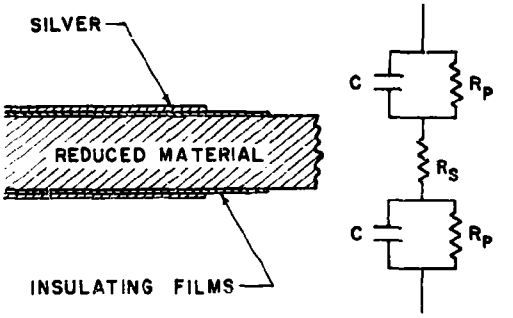

Figure 1.-Physical and electrical models of layerized high-dielectric-constant capacitors.

The losses of the layerized capacitors would be of three types: (1) intrinsic or polarization loss which is due to the nature of the dipolar structure of the film and is independent of the film thickness, (2) parallel loss which is due to the leakage resistance of the film and increases with decreasing thickness of the film, and (3) series loss which results

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from the resistivity of the inner semiconductor and from the resistance of the electrodes themselves.

Dielectric constant, k, is normally calculated for a parallel plate capacitor using the formula $k = tC/0.225A$, where t is the thickness in inches, C is the capacitance in micromicro farads, and A is the area in square inches. For true dielectric constant, the actual thickness of the insulating layer is used for t. When the site of capacitive action and the associated thickness are not known exactly, an effective dielectric constant is often obtained by using the total thickness of the unit for t. Effective dielectric constant is not used in this work.

In 1946, the Herlec Corporation [6] reported work on "ultra-high-dielectric-constant" materials. A ceramic having a $BaTiO_3$ base was reduced in city gas which contains carbon monoxide to obtain units reported to have an effective dielectric constant of 125,000 to 175,000 and a loss of approximately fifty percent. These units were not reoxidized and their high dielectric constants are characteristic of materials containing conducting particles.

Wentworth in 1947 produced high-dielectric-constant but lossy materials by a carbon monoxide reduction of $BaTiO_3$ ceramics containing other titanates, zirconates, and antimony oxides [7].

Other units, similar to those to be described in this report, have been made by Onondaga Pottery Company [8] who reduced the titanate with carbon monoxide and reoxidized it when firing-on the silver electrodes in air. Roup and Butler [9], using carbon as a reducing agent and fired silver as electrodes, developed a unit which is believed to have resulted in production of a commercial unit [10] having a capacitance of about four microfarads per square inch. Recent work by Roup and Kilby [11], using hydrogen and waffle-surfaced specimens, has resulted in units with a still higher capacitance per unit area.

These commercial units are, however, not available in the sizes and shapes required for the work in process at The Diamond Ordnance Fuze Laboratories (DOFL). Therefore, it was necessary to fabricate usable units and study the effects of processing variables on the properties of the units.

EXPERIMENTAL TECHNIQUES AND DATA

1. Formulating of specimens

Thin-film specimens were prepared by a doctor-blade technique as follows. Ceramic powders were combined to make a mixture having a total weight of fifty grams and then were mixed with the materials listed below and ground overnight in a ball mill.

Butyl Cellosolve	0.35	ml
Toluene	12	ml
Resin solution	15	ml

The resin solution consisted of:

Glycerol ester of hydrogenated resins	15	gm
Methyl abietate	15	gm
Ethyl cellulose	6	gm
Amylnaphthalene	5.2	ml
Fatty acid esters of hexitol anhydride	1.0	ml
Diethyl oxalate	1.8	ml
Toluene	65.2	ml

A portion of the milled material was poured onto a plate (Fig. 2A) having edges raised 0.02½

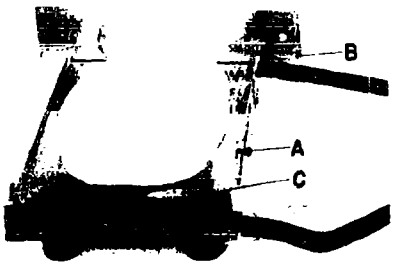

Figure 2.-Apparatus for casting and drying thin ceramic films: (a) plate, (b) doctor blade, and (c) removal knife.

inch above the flat surface. A straight-edged blade (Fig. 2B) was drawn along the raised edges of the plate forming wet film of the desired thickness. Hot water passing through copper tubing attached to the bottom of the plate heated it from below while an infra-red lamp eight inches above the plate heated it from above. After fifteen minutes, the lamp was removed and cold water was run through the copper tubing. When the film reached room temperature, it was removed by passing a thin blade (Fig.2C) between it and the plate. This dried film was a flexible sheet 0.012 inch in thickness and was cut into 7/16-inch squares. Squares of larger size were impractical due to cracking during sintering, a result of non-uniform shrinkage.

The various ceramic powder mixtures that were prepared are listed in Table I.

Table I. - Composition of formulations

Formulation	Composition	
BA	$BaTiO_3$	81%
	$SrTiO_3$	10%
	$CaZrO_3$	7%
	$MgZrO_3$	2%
BB	BA	99.5%
	CeO_2	0.5%
BC	BA	99.8%
	Sm_2O_3	0.2%
BD	BA	99.5%
	Nd_2O_3	0.5%
BE	BA	99.5%
	La_2O_3	0.5%

2. Firing procedure

The 7/16-inch squares were fired three times; first to sinter, second to reduce, and third to apply electrodes and reoxidize the surfaces of the bodies.

A. Sintering. - The 7/16-inch squares were stacked between platinum separators and a small amount of 100-mesh ZrO_2 powder was sprinkled between the platinum and ceramic to prevent sticking. Stacks were fired in a platinum wound furnace for 1 hour at 1350°C.

B. Reducing. - The samples were placed on ZrO_2 bats and reduced in a dry hydrogen atmosphere. To determine optimum time and temperature for the reduction process, samples of formulation BA were fired at each of four temperatures for periods of 10 and 60 minutes. Results of electrical measurements on these specimens after processing are given in Table II. Most specimens were fired for ten minutes at 1200°C, cooled in about five minutes to below 300°C and then removed from the furnace. The specimens looked black or blue-black at this stage. In Table III, samples fired in dry hydrogen are compared electrically with samples fired in hydrogen wetted by bubbling through water.

Table II

Effect of various reducing times and temperatures on the capacitance per unit area and the dissipation factor of layerized reduced titanate capacitors.(a)

Reduction temperature, °C	Time, min.	Capacitance/area, μfd/in²	Loss %
1100	10	0.34	2.6
		0.37	1.7
	60	0.42	1.8
		0.54	2.2
1200	10	0.46	2.0
	60	0.59	1.7
		0.46	1.7
1300	10	0.59	2.0
		0.51	2.0
	60	0.41	1.7
1400	10	0.41	2.8
		0.39	3.0
	60	0.40	3.4

(a) Formulation BA. Silver paint electrodes fired for 2 minutes at 800° C.

Table III

Effect of reducing in wet vs. dry hydrogen on the capacitance per unit area and dissipation factor of layerized reduced titanate capacitors.(a)

Hydrogen	Capacitance/area, μfd/in²	Loss, %
Dry	0.48	4.1
	0.59	2.4
	0.50	2.5
	0.54	2.3
	0.55	2.6
Wet	0.094	9.1
	0.099	11.4
	0.098	9.3
	0.12	11.3
	0.10	9.6

(a) Formulation BA
Sintered 60 minutes at 1350° C.
Reduced 10 minutes at 1200° C.
Electrodes fired 2 minutes at 800° C.

C. Electrode application and reoxidation of surfaces. - Gold or silver electrodes were used on samples. Gold electrodes were vacuum deposited in place without resorting to glow-discharge cleaning. Silver electrodes were applied either by brushing or by screening a thin layer of silver paint onto the ceramic. After applying the silver paint to each side of the ceramic, it was dried for a few minutes at 100°C until it was not tacky and the units were then placed on 20-mesh ZrO_2 grains on a small steatite plate.

In order to determine optimum firing time, both at 700° and 800°C, in a furnace having an air atmosphere, sixteen reduced 7/16-inch squares were fired at various times from 1.5 to 8 minutes. The results of electrical measurements on these specimens, after cutting to still smaller size, as described in the next section, are given in Table IV and Table V; the specific firing conditions in each experiment are indicated in the footnotes of each table. When the specimens were removed from the furnace, the small fired squares were allowed to slide onto a cool surface of insulating stabilized zirconia brick.

3. Cutting to size

After application of electrodes, the 7/16-inch squares formed by the doctor blade technique were cut to 0.1-inch squares by a method analogous to that used to cut glass. Half of the unit was supported. Then it was ruled with a scribe having a tungsten carbide tip so that the scratch was in line with the edge of the support. Pressure was then exerted downward on the unsupported half.

Table IV

Effect of varying the firing time at 700° C. on the capacitance per unit area and the dissipation factor of layerized reduced titanate capacitors[a]; silver paint electrodes.

Sample No.	Time, min.	Capacitance/area, μfd/in²	Loss, %
1	1.5	2.6	18.5
2		2.2	36.0
3		1.7	8.3
4		0.96	3.1
5		1.7	23.0
6		2.2	24.7
7		1.3	34.3
	Av.	2.1	21.1
8	2	1.6	38.8
9		2.3	18.1
10		1.9	8.5
11		1.9	11.3
12		2.0	23.3
	Av.	1.9	20.0
13	4	1.5	42.6
14		0.88	2.7
15		0.81	2.7
16		0.86	10.4
	Av.	1.01	14.6
17	8	0.69	10.7
18		1.2	38.8
19		0.62	5.8
20		0.95	41.1
	Av.	0.86	24.1

(a) Formulation BA, film specimens, 0.1-inch squares. All samples reduced in dry hydrogen for ten minutes at 1200° C.

Table V

Effect of varying the firing time at 800° C. on the capacitance per unit area and the dissipation factor of layerized reduced titanate capacitors[a]; silver paint electrodes.

Sample No.	Time, min.	Capacitance/area, μfd/in²	Loss, %
1	1.5	0.67	12.4[b]
2		0.86	37.6[b]
3		0.60	2.6
4		0.67	3.1
5		0.66	25.9[b]
6		0.58	2.9
7		0.56	2.9
	Av.	0.60	3.0
8	2	0.55	12.1[b]
9		0.50	2.9
10		0.50	2.4
11		0.51	2.4
12		0.46	2.2
	Av.	0.49	2.5
13	4	0.35	2.0
14		0.34	2.1
15		0.38	3.1
16		0.33	2.2
17		0.34	20.9[b]
	Av.	0.35	2.6
18	4.25	0.28	2.0
19		0.28	2.0
20	8	0.22	2.7
21		0.18	3.6
22		0.20	2.9
23		0.19	2.8
24		0.20	2.8
25		0.24	2.7
	Av.	0.20	2.9

(a) Formulation BA, film specimens 0.1-inch squares. All samples reduced in dry hydrogen for 10 minutes at 1200° C.

(b) These values were not included in the averages since these units would normally be rejected for use in an actual circuit.

4. Testing

A commercial capacitance bridge was used at one-volt peak voltage and at one kilocycle for determinations of capacitance and dissipation factor. The results of these measurements for each formulation can be found in Table VI. There was no dc bias across the unit except when leakage resistance and capacitance as functions of dc voltage were measured. To measure leakage resistance, a dc power supply was connected to the capacitor in series with an ultra-sensitive microammeter. The voltage across the unit was read on a vacuum tube voltmeter having an input resistance of 11 megohms and the resistance was calculated from Ohm's law. A plot of leakage resistance versus dc voltage for two specimens made from formulation BA can be found in Fig. 3. The effect of variation of voltage on the resistance was determined by measuring the resistance first at one volt, then at a somewhat higher voltage, then again at one volt, and then at a voltage greater than the previous maximum. This procedure was continued to nine volts, each time returning to one volt after the increase. The results of these measurements are given in

Table VI

Effect of additives on the capacitance and loss of layerized reduced titanate capacitors at 1 kc.

Type	Additive	Capacitance/area, μfd/in²	Loss, %
BA	None	0.48	4.1
		0.59	2.4
		0.50	2.5
		0.54	2.3
BB	CeO_2	1.1	3.6
		1.0	3.2
		1.1	7.6
		0.9	3.2
BC	Sm_2O_3	0.82	2.7
		0.76	2.9
		0.87	2.8
		1.1	3.0
BD	Nd_2O_3	1.4	4.5
		1.1	7.0
		1.1	4.5
		1.0	11.6
BE	La_2O_3	1.1	4.2
		1.2	4.1
		1.0	4.1
		1.0	7.3

Sintering conditions -- 1 hour, 1350° C.
Reducing conditions -- 10 minutes, 1200° C.
Reoxidation conditions -- 2 minutes, 800° C.

Table VII

Effect of increasing voltage pretreatments on leakage resistance at one volt.

Type BA		Type BC	
Volts	Resistance, megohm	Volts	Resistance, megohm
1	10	1	10
3	3	3	3
1	6	1	9
4.8	0.06	5	1
1	1	1	8
5.8	0.06	6.2	0.7
1	1	1	1
7	0.03	7	0.6
1	0.03	1	5
8	0.01	8.2	0.5
1	0.03	1	4
9	0.01		
1	0.2		

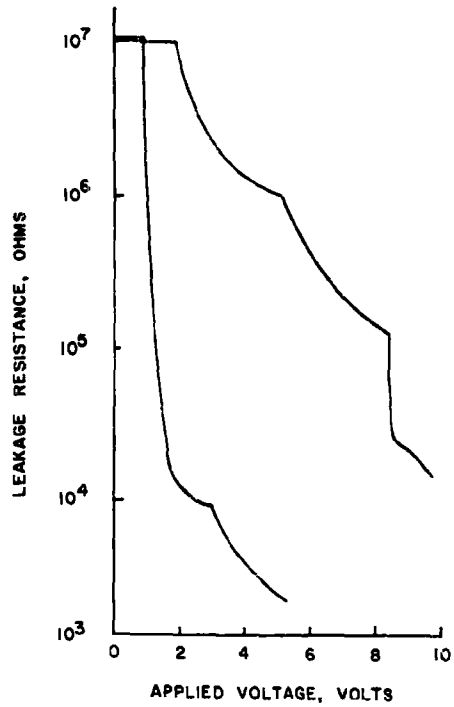

Figure 3.--Resistance as a function of applied dc voltage for layerized capacitors of type BA.

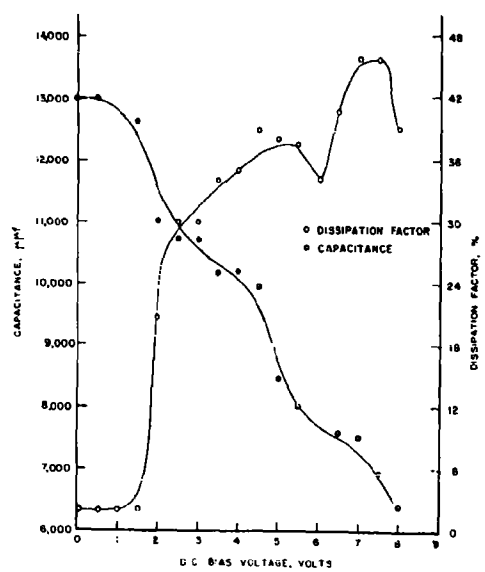

Figure 4.--Capacitance and loss as a function of dc voltage for layerized capacitors of type BD.

Table VII in the order in which they were determined. When capacitance and loss as a function of dc voltage were measured, the power supply and a large inductor in series were placed across the unit. The purpose of the inductor was to prevent the bridge from being loaded by the bias supply. The results of these measurements on a unit of type BD can be found in Fig. 4.

The specimens were placed in an insulated box for measurement of the effects of temperature on the electrical parameters. A fan circulated air over small pieces of dry ice to cool the test chamber to about -40°C. To raise the temperature, warm air obtained from a heater contained in a separate compartment was circulated through the box. The ambient temperature of the test box was controlled automatically by a thermocouple attached to the heater control. The capacitors were mounted on a ceramic plate by means of a conducting plastic cement[12] and embedded in an epoxy resin to prevent condensed water vapor from shorting the units. The leads were attached within the box to electrodes which were connected externally to the measuring circuits. The results of the temperature study can be found in Figure 5 which

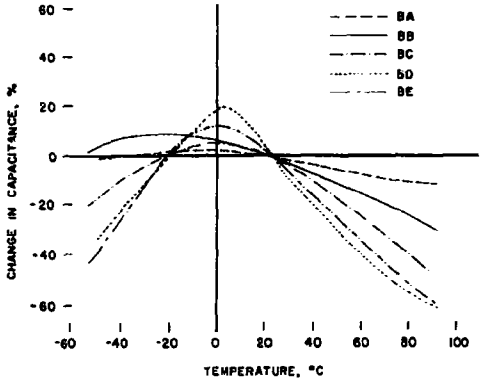

Figure 5.-Percent change of capacitance of all formulations as a function of temperature, percent change of capacitance calculated from a reference point at 25°C.

indicates percentage change of capacitance as a function of temperature for all formulations. Figure 6 shows the same measurements made on both a reduced and an unreduced sample of formulation BB.

Resistance as a function of time at constant dc voltage was measured with an automatic voltage recorder using the circuit shown in Figure 7. The resistor R was adjusted to bring the indicator to the region of the scale where the deflection was at a maximum, and then was not changed during a run. Resistors of known value were substituted for the test unit to calibrate the chart.

A 10^7-ohm resistor was permanently connected across the capacitor being tested to avoid

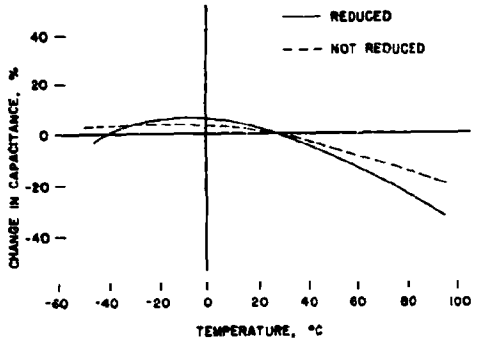

Figure 6.-Percent change of capacitance of reduced and unreduced type BB capacitors as a function of temperature, percent change of capacitance calculated from a reference point at 25°C.

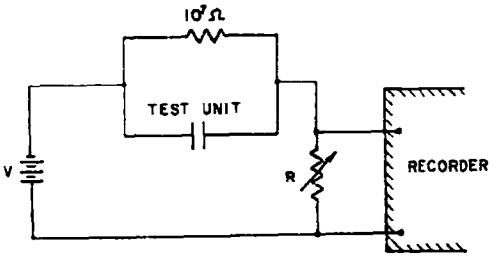

Figure 7.-Test circuit for continuous measurement of dc resistance as a function of time.

damaging the instrument by pickup whenever the unit was removed from the test circuit. This limited all measurements to slightly less than 10^7 ohms.

Capacitance as a function of time (aging) was determined simply by measuring the capacitance of a given unit at prescribed times up to 1300 hours.

Capacitance and loss of several capacitors cut from the edges of the 7/16-inch squares are shown in the upper half of Table VIII. After abrading the edges of the capacitors, the same electrical properties are shown in the lower half of Table VIII.

Table VIII

Effect of abrading away the sides of edge pieces from a 7/16-inch-square of a type BA layerized, reduced titanate capacitor

Condition of capacitor	Unit No.	Capacitance/area, $\mu fd/in^2$	Loss, %
Before abrasion	1	0.60	18.8
	2	0.88	30.6
	3	0.92	34.5
After abrasion			
	1	0.55	2.6
	2	0.49	2.6
	3	0.51	6.6

To determine whether the capacitance is a volume or surface phenomenon and to estimate the thickness of the surface layer, one electrode and adjacent oxidized surface were removed by abrading with 600-mesh carborundum on a glass plate. An electrode was then put on the exposed face both by vacuum deposition and by painting on an air-dry silver paint. Electrical measurements were then conducted on the specimens. Results are discussed below.

Several units were embedded in an epoxy resin and a cross section was cut with a saw. The surface was polished with fine emery and examined under a fifty-power binocular microscope with reflected light.

DISCUSSION

It was found that capacitors with a high capacitance-to-volume ratio could be produced from ceramic formulations consisting predominately of $BaTiO_3$ by sintering, reducing, and reoxidizing while firing-on silver paint electrodes in air. Gold electrodes applied by vacuum deposition did not produce capacitors but instead yielded low-value resistors. Neither gold nor silver reacts chemically with the ceramic. It is unlikely that the glass particles in the silver paint had any effect, since the paint normally produces low-resistance bonds, or that the organic binder in the paint had any effect because it would be completely combusted. Therefore, the differences between the capacitors bearing the two different types of electrodes must have resulted from the fact that the application of the silver electrodes required heating of the material. It was found that the reduced ceramic could be reoxidized throughout its volume by continuous heating in air for about 15 minutes at temperatures suitable for electrode firing.

It was concluded that the process of firing the electrodes resulted in formation of a thin film like the original unreduced ceramic, and having a high dielectric constant, and that it was this thin insulating film that became the capacitor dielectric. It is of interest that no previous theory has been found in the literature that explained the capacitive action of reduced titanate capacitors by means of such a reoxidized layer. However, the presence of such a film would permit an explanation of the properties of the capacitor, in particular the frequency dependence, by means of the early theories of J. C. Maxwell [13] and K.W.Wagner [14] which treated the capacitance of multilayered dielectrics. When the units with gold electrodes applied by vacuum deposition were subsequently fired for 1.5 minutes at 700°C., high capacitance and low loss resulted, as expected.

For the capacitor to have low series resistance, the inner layer of reduced titanate should have high conductivity. Since the conductivity is a result of the reduction process, there should be an optimum reduction time and temperature. From Table II it can be seen that, over a broad range of reduction temperatures and times, there is no detectable difference in dielectric properties. Apparently the conductivity increases rapidly early in the reduction step so that further treatment produces no real improvement. It is important that the reduced units be cooled in the hydrogen atmosphere and not be permitted to come in contact with oxygen until near room temperature. If these precautions are not observed, uncontrolled reoxidation will occur.

Table III gives some representative values for the finished capacitors which were reduced in both wet and dry hydrogen. The lower capacitance and higher loss of the wet-hydrogen-type compared with that of the dry-hydrogen-type suggests that the reoxidized layer of the former type is thicker and that the series loss is greater. This effect can be explained by means of the following well known reaction between titanium dioxide (TiO_2) and hydrogen:

$$2TiO_2 + H_2 \longrightarrow Ti_2O_3 + H_2O$$

When a crystal of the oxide is exposed to hydrogen, the entire crystal is not converted to Ti_2O_3 (which may be written $TiO_{1.5}$) but rather gradually loses oxygen atoms and passes through such non-stoichiometric structures as $TiO_{1.8}$. The conductivity of the reduced material increases with increasing removal of oxygen. Although TiO_2 does not exist as such in the crystal lattice of barium titanate, the removal of oxygen atoms by the hydrogen gas, with the resultant formation of water, is still the essence of the reduction process. At high temperatures the above reaction is known to be reversible with equilibrium lying to the right. If water is removed by constantly flushing the system with fresh hydrogen, the reaction will go to completion to the right. However, if the hydrogen is wet, the equilibrium is reached with loss of the reduced titanate present, i.e. with less oxygen removed from the lattice. This means that the conductivity of the reduced material is lower and increases the series resistance and hence the loss of the unit. Since there is now partially reoxidized, **i.e.** incompletely reduced, material on the surface, the reoxidation that occurs during firing of the electrodes produces a thicker insulating layer. This decreases the capacitance as was observed. The increase in parallel resistance due to the greater thickness is, however, overshadowed by the increase in series resistance and the net loss would increase as observed.

Using the formula for capacitance of a parallel plate condenser, and assuming that the dielectric constant of the layer is several thousand, a thickness for the reoxidized surface layer of about one tenth to one half mil is obtained. This is in agreement with the amount of material which must be abraded away to remove one of the series capacitances. However, examination by reflected light under a fifty-power microscope shows no film of this thickness. It is conceivable that the film cannot be seen by reflected light. It is also possible that the film is thinner and the dielectric constant lower than expected or that no well-defined layer exists. That is, the layer would gradually

merge into the conducting body of the unit.

Since the capacitance and also the loss due to leakage resistance are a function of the thickness of the film and, therefore, of the time during which the film is being formed, it was necessary to determine the optimum firing time. From Table V it can be seen that two minutes at 800° C. gives high capacitance without excessive loss. The magnitude of the loss of the poorer units is of no real consequence since these units would be rejected from the lot before a capacitor was chosen for a circuit. A high percentage of rejects is obtained with a firing time of 1-1/2 minutes with only a 20% increase in capacitance above that obtained by firing for 2 minutes. Therefore, on an economic basis, the two-minute firing time is more advantageous. Table IV indicates that at 700° C. the capacitance can be more than three times as great although this is at the expense of higher loss. For example, of the twenty units listed in Table V only six have a loss of less than 10% and these six units have a capacitance more nearly equal to that obtained for a firing time of two minutes at 800° C. It is clear that if a higher capacitance unit were desired, it could be made at the lower temperature although the material waste would be greater. The high loss for all rejects examined has been found to be due to decreased leakage resistance. Units having a loss of 25% or greater invariably had a resistance of less than 100 kilohms at 1-1/2 volts; that of the normal units with lower loss was usually on the order of several megohms.

A very significant observation was made from these experiments. Before any systematic experiments were performed to determine optimum firing conditions, the units were always fired at 700° C. for 1-1/2 minutes. These conditions were employed for several months with great success although Table IV indicates that difficulty should have been experienced. In order to understand this anomaly it should first be realized that a high temperature is required for reoxidation and that, when the unit is placed in the furnace, it is at room temperature. It is to be expected that a thermal insulator (the ceramic) and a thermal reflector (the silver) will not equilibriate with the furnace very rapidly. In addition, the solvent in the silver paste must evaporate and, in so doing, cool the sample. It was found that when a silvered reduced sample was placed in a furnace at 700°C for a series of fifteen-second exposures, little or no reoxidation occurred, as evidenced by no decrease in conductivity. From this the conclusion arises that more than fifteen seconds is required for the unit to attain the reoxidation temperature. This time was increased by the addition of excess solvent to the silver paste.

It was found that the only part of the procedure that had been changed at the time units could no longer be fabricated at 700° C. had been that the silver paste had been diluted with turpentine. Although it has not yet been proven, it is suggested that this step was the source of the difficulty. Turpentine contains among other things significant amounts of unsaturated structures, which in the presence of atmospheric oxygen form polymers at room temperature. These polymers are quite involatile and at 700° C. they would tend to char rather than burn away. The result is that probably the silver and the ceramic face would be covered with films of high polymeric carbonaceous residues. Carbon has been used by Soup and Butler[67] to reduce the titanates. It is clear that, in the presence of the carbon and the polymers films, formation of the reoxidized film is severely hampered. Table IV indicates that increasing the time to eight minutes still does not improve the situation. However, it is well known that the time required to remove polymers by combustion at elevated temperatures is often much longer. The question then is why the turpentine does not seem to interfere when the units are fired at 800° C. The explanation is, doubtless, that at 800° C., most of these high polymers tend to undergo complete combustion rather than thermal degradation. In any event, at 800° C. the reducing carbon and the polymer sludge are not present on the ceramic face and proper oxidation occurs.

From this discussion it can be seen that reoxidation conditions are critical and may not remain constant from one batch to another. When difficulty is experienced, it is suggested that the optimum firing conditions be determined.

It was likely that each unit consisted of two capacitors, since both sides of the plate are reoxidized in series with each other, and with the conductor between them (Figure 1). To verify this, one of the silver electrodes was ground away, removing as little of the surface as possible. The aim was to eliminate the insulating layer. A gold electrode was then vacuum deposited onto this side. The capacitance was remeasured and was found to be nearly doubled, as would be expected if one of two equal capacitors in series were shorted.

Table VI shows the effect of various additives on the capacitance and loss measured at 25° C. The spread of values for supposedly identical units is still sufficiently great that a statement cannot be made to the effect that one additive produces a substantially greater increase than another. However, a valid conclusion is that the capacitance can be increased considerably by addition of rare earth oxides to the original mixture.

Since in some circuit applications, a capacitor has a dc voltage across it, the effect of this voltage on the unit must be determined. Figure 3 indicates the effect of this voltage on the leakage resistance. The immediate observation is that the units are definitely non-ohmic. The graph gives data on only two samples. There is much individual variation but the general property of alternating flat and sharply dropping regions is characteristic of all. It is thought that these drops are due to a succession of partial dielectric breakdowns or pinhole formation in the insulating film.

It has been observed that the leakage of a sample depends to a great extent upon its elec-

trical history. Table VII indicates for two different samples that the resistance does not return to its low-voltage value after a high voltage has been applied; that is, the unit is not only non-ohmic but also not reversible. Such variation does not seem to follow a regular pattern and differs from one unit to another.

It was of interest to determine whether the capacitance of one of the 0.1-inch-square units was in any way dependent upon the part of 7/16-inch square from which it came. It was found that edge pieces from the larger square were considerably more lossy than those in the body of the square. It was found that often in the silvering operation some of the silver slipped around the edge and had shorted the units. However, there were many cases in which no silver on either side of the larger square reached the edge and the loss of these edge units was still excessive. In such cases the high loss was usually accompanied by higher capacitance than normal. It was found that if the edge of the unit was abraded away, the loss and capacitance assumed the normal values. Table VIII shows the capacitance and loss of three such units before and after abrasion. No explanation has as yet been given for this phenomenon. It is recommended that for production purposes the edge pieces be made very narrow and discarded.

Figure 4 illustrates the dependence of capacitance on voltage for a single typical unit. The details of the curve vary from sample to sample but the sudden increase in loss and the continual capacitance decrease are characteristic. No explanation has been given yet for the general shape of the curve.

The temperature-capacitance characteristics of units containing various additives can be seen in Figure 5 which shows the percentage change of capacitance from the room-temperature value as a function of temperature. The material with no additives, BA, shows the least variation. Of the additives, CeO_2 produced the least change. Although for most purposes a perfectly flat curve would be ideal, it should be noted that a controlled amount of temperature dependence can be obtained by proper choice of additives. Such elements may be useful in special applications.

Figure 6 indicates the percentage change of capacitance as a function of temperature for the formulation containing CeO_2. If the insulating layer is unreduced titanate as has been proposed, then it would be expected that the curves for the unreduced and for the reduced and reoxidized specimens would be identical. The close similarity indicates that the hypothesis is probably correct. The difference between the two curves is possibly due to interfacial polarization.

Any usable capacitors must be relatively stable with time. The resistance of several units was observed at constant voltage for as long as eighteen hours. It was found that, up to two-volts bias, the leakage resistance never dropped below one megohm. For higher values, up to 4.5 volts, the leakage resistance often dropped to as low as 200 kilohms.

The variation of capacitance with time with no applied voltage (aging) was found to be 2-3 % per decade. This followed the typical exponential decrease with the most rapid decrease occurring during the first few hours after the temperature of the unit was raised above the Curie-point temperature.

Studies of the characteristics of the materials used and of the phenomena involved in the production techniques described above are being continued. There is some evidence that the sintering operation may be unnecessary and that sufficient sintering can occur during the reduction process provided that the temperature is raised to approximately 1400° C. It is also possible that chemical reoxidation and subsequent chemical deposition of electrodes will produce units having greater uniformity. Other additives remain to be tested, including bismuth stannate which is known to flatten the temperature-capacitance curve. It is known also that titanium dioxide can be rendered semiconducting by addition of small quantities of tri- and pentavalent oxides. It is possible that the titanates can be similarly affected by antimonates, tungstates, and molybdates. The insulating film could then be formed by chemical removal of the acceptor or donor atoms from the surface of the plate. There is some evidence that the capacitance can be increased substantially by roughening the surfaces of the reduced unit before reoxidation, in so doing increasing the effective surface area.

CONCLUSIONS

Microminiature ceramic capacitors having a capacitance of about 1μfd/in^2 and losses of 3 to 5% have been made from a very thin layer of material consisting predominantly of $BaTiO_3$. The units were made by: (1) casting a thin film by a doctor-blade technique, (2) sintering a plate cut from this film, (3) reducing in hydrogen to make the plate semi-conducting, (4) reoxidizing the surfaces while firing-on the silver electrodes to form an insulating dielectric, and (5) cutting the plate into 0.1-inch squares. The step providing for surface reoxidation (Step No. 4) was the most critical and care in selecting the time and temperature for this operation must be exercised.

Because of the strong voltage dependence of the leakage resistance of these capacitors, the recommended maximum voltage rating is 2 volts.

ACKNOWLEDGMENT

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A FAMILY OF STANDARD TRANSISTOR SWITCHING CIRCUITS

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This paper describes the progress to date in designing a compatible set of standard circuits for use in experimental breadboard systems. The circuits, such as multivibrators, binary counters and inverters, are simple building blocks which can be interconnected to perform complex functions. The circuits, which are shown in detail, are designed for use at frequencies up to approximately 15 KC and temperatures up to 45° C. Design changes are presented for modifying the limits as may be required for a specific application. An electronic timer is described which illustrates the use of the standard circuits to generate time intervals of 5, 10, or 15 seconds following an initiating trigger. Future effort will be directed toward adding additional circuits to the available types and obtaining more complete theoretical and experimental data on present and newly added circuits.

INTRODUCTION

Standard circuits and modules are being increasingly considered by the electronics industry. This interest is understandable when the amount of time spent in designing a given type circuit over and over again is added up. Also from the standpoint of mass production a few widely applicable standard circuits would permit low unit cost and high reliability.

The microminiaturization program adds an additional incentive. As the circuits get smaller and are manufactured by printing or vacuum-deposition methods, the system designer will become primarily interested in the functioning of logical blocks rather than the individual component part values. In order to achieve reliable building blocks, the circuit design can and should be considered in detail only during the overall design of the particular wafers or modules. These modules then are stocked as the smallest component to be handled in development and production activities.

In connection with research and development work of the Diamond Ordnance Fuze Laboratories, it has been found that the circuits to be described are useful for rapid assembly of working systems. The circuits are primarily of the low power level, information handling type. Typical applications include digital computing and timing operations. The circuits are restricted to those using the transistor as an off-on or relay-type device.

SPECIFIC CIRCUITS

The circuits are listed in Table I in the order they will be discussed. The particular circuit types were chosen, in part, because they have been studied extensively. As a result, detailed information is available or calculable on the design, performance, and limitations of the circuits. Specific component part values are shown in the schematics. From the standpoint of presently used techniques of making microminiature assemblies, the resistor elements are the easiest to handle. Accordingly the circuits are designed to use no inductors and as few capacitors as possible.

(1) Inverter (IN)

The Inverter circuit[1] shown in Figure 1, as its name implies, inverts the input signal. For - 1.5 volts in, the output is 0; for 0 in, - 1.5 volts out. One inverter stage can drive several other inverter stages or similar type loads.

(2) Inverter Less Load (INLL)

A degenerate form of the Inverter is shown in Figure 2. The load resistor of 1 K ohm, normally found in the collector circuit, is omitted. This circuit is used to couple a signal to a common load resistor fed by several circuits.

(3) NOR

The NOR circuit[2, 3] is similar to the Inverter except for the number of inputs. The NOR shown in Figure 3 has two inputs. In principle, any number could be used. In practice, the two-input version is a compromise between versatility and noncriticalness. The two-input NOR has many similar logical properties to the two-grid pentode gating circuit. The logical function performed by the NOR is shown beside the schematic of Figure 3. When neither A nor B is present an output exists. The NOR is an elemental building block. With one or more NOR circuits all the logical functions including NOT, AND, OR can be performed.

TABLE I

LIST OF STANDARD CIRCUITS

Inverter	(IN)
Inverter Less Load	(INLL)
NOR	(NOR)
Flip-Flop	(FF)
Binary Counter	(BC and BCR)
Monostable Multivibrator	(MMV)
Free Running Multivibrator	(FRMV)
Lamp Control	(LC)
Power Switch	(PS)

(4) Flip-Flop (FF)

A bistable circuit can be formed by connecting two Inverter circuits together to form a toggle or Flip-Flop.[4] The schematic is shown in Figure 4. Information can be coupled into the Flip-Flop by connecting the collector of an INLL circuit to one of the collectors of the FF.

(5) Binary Counters (BC and BCR)

The Flip-Flop can be modified by the addition of input pulse steering circuits to obtain a Binary Counter [5, 6] as shown in Figure 5. The added capacitors, diodes and resistors provide alternate feeding of the input pulses to one transistor, then to the other.

When initial conditions need to be set into the Binary Counter, diodes coupled to the base of each transistor can be added as shown in Figure 6.

(6) Monostable Multivibrator (MMV)

The Monostable Multivibrator[7] is used to generate a gate or time delay following an initiating trigger pulse. The design shown in Figure 7 has the delay time adjusted by choice of the coupling capacitor between the two transistors. The start trigger is coupled into the "normally-on" transistor by means of a capacitor, resistor, and diode network.

(7) Free Running Multivibrator (FRMV)

The Free Running Multivibrator[8] of Figure 8 is a source of two symmetrical square waves of opposite polarities. The frequency is set by the cross-coupling capacitors.

(8) Lamp Control (LC)

The Lamp Control circuit of Figure 9 is used when visual indication is required of the binary state of Flip-Flops or Binary Counters. A two-stage circuit is used because the lamps have a drain of about 50 milliamperes. A single transistor could not reliably give enough current gain. Both this circuit and the following Power Switch circuit are designed to be driven by an output signal from one of the previously described circuits.

(9) Power Switch (PS)

The Power Switch circuit of Figure 10 is similar to the Lamp Control circuit except for the output load. The Power Switch circuit will provide a heavy duty positive step in voltage at its output. One use of the circuit is to set or reset a number of Binary Counter stages simultaneously.

COMMENTS ON DESIGN AND PERFORMANCE

Elaboration of several points concerning these circuits will now be made under the following headings:

1. Choice of transistor type
2. Transistor specifications
3. Choice of diodes
4. Choice of supply voltages
5. Upper frequency limit
6. Upper temperature limit

(1) Choice of Transistor Type

The specific circuits shown are designed for pnp transistors. Simple changes in the polarities of capacitors, diodes, and power supplies would permit the use of npn types. The pnp alloy germanium types are the most common transistors manufactured and are well suited to the circuits. Typical transistors are the 2N77, 2N105, and 2N207. The latter transistor has been used extensively in making small etched board modules. Higher frequency types include the 2N139 and those of the series 2N112-2N114. The microalloy 2N393 is a type of even higher frequency. For high-temperature operation, a silicon alloy type would be necessary.

(2) Transistor Specifications

Two parameters are of major importance to the proper operation of the circuits: common emitter current gain (β) and collector cut-off current (I_{CBO}). The drop in β with decreasing temperature sets the lower temperature limit of circuit operation. The increase in I_{CBO} with increasing temperature sets the upper temperature limit for the circuits. Beta values of 50 or greater are required for all transistors except the output transistor in the Lamp Control Circuit. This latter transistor was chosen to have a β greater than 100.

The β of the 2N207 drops to about 50% of its room-temperature value at -40° C. The circuits should perform properly down to this temperature although experimental tests have not verified the fact. The circuits are designed to operate with transistors having an I_{CBO} value up to 30 μa. For the 2N207 type, this value is reached at approximately 60° C.

(3) Choice of Diodes

The diodes used in the Binary Counter are non-critical in terms of the characteristics of presently available diodes. Point contact germanium diodes of minimum quality have been used. The 1N90 is typical. It has a minimum forward current of 5 ma at 1 volt and a maximum reverse current of 500 μa at 50 volts.

Junction diodes of equivalent dc characteristics should operate as well as point contact types in the low-frequency circuits considered so far. If the maximum upper operating temperature is desired for the circuits, the diode should be chosen for minimum reverse current at the upper temperature point.

(4) Choice of Supply Voltages

The circuits are designed to operate from two single cells, one for the negative source and one for the positive source. Either 1.3-volt mercury cells or 1.5-volt dry cells are satisfactory. Two-volt lead-acid cells can be used if the Lamp Control Circuit has a 2-volt lamp (No. 48 or 49).

(5) Upper Frequency Limit

The circuits have not been designed for optimum frequency response. Circuit simplicity and reliable low-frequency operation were stressed in these designs. The Binary Counter, using transistors such as the 2N77 or 2N207, has an upper input counting rate of approximately 15 kc. The input capacitors were chosen for these transistors and would need to be reduced in value to permit higher counting rates with higher frequency transistors. The Lamp Control circuit is limited in speed by the thermal response-time of the lamp. Observation of several switching cycles per second is possible. The other switching circuits have a transient response-time of about 20 microseconds.

(6) Upper Temperature Limit

If 2N207 transistors and 1N90 diodes are employed in the circuits with other component parts as shown, the upper temperature limit is approximately 45° C. It is stressed that the particular design-values are not chosen to give high-temperature performance.

TECHNIQUES FOR IMPROVING PERFORMANCE

The circuits presented in the schematics have upper limits in frequency of tens of kilocycles and in temperature of approximately 45° C. The natural question is how to improve these limits, if necessary, for a particular application.

The upper frequency limit can be raised by two approaches. The first is to keep the previously described circuit topology and use higher frequency transistors and correspondingly lower capacitors[6] in the Binary Counter stages. Most of the circuit speeds are limited by the transistors and not by wiring capacitances. The upper speed is roughly proportional to the alpha cutoff frequency of the transistors.

The second approach is to use a more complex circuit[2] and more efficiently utilize a particular transistor-type. Speed-up or commutating capacitors can be used to provide better coupling between stages. The transistors can be operated in a non-saturating mode; thus reducing switching time appreciably. Complementary-symmetry operation can be used to obtain positive drive in the rise and fall times of a waveform.

In an analogous manner, the upper temperature limit can be improved. Keeping the same circuits, transistors with lower I_{CBO} currents can be used (if available). The silicon alloy types will prove attractive as they become more readily available at modest prices. The base bias resistors and/or positive supply voltage can be modified for higher temperature operation. More involved circuitry can be used to boost the upper temperature limit.

A REPRESENTATIVE APPLICATION OF THE CIRCUITS TO A SYSTEM

An example of the use of the standard circuits to construct a more involved system is shown in Figure 11. The system is an electronic timer for generating 5, 10 or 15 second intervals following the activation of a push button.

One-second pulses are generated by dividing down the 60 cps line voltage through a six-stage binary divider (BCR-1 through BCR-6) with feedback to reduce the division ratio from 64 to 60. The input power line voltage is shaped to drive the binary counter by feeding through the two inverter stages (1N-1, 1N-2). The NOR block is a gate described later on.

The basic counting register is another set of binary counter stages (BCR-7 through BCR-10). Three time-periods are provided, i.e., 5, 10 and 15 seconds. Using the one-second pulses as an input, the 4-stage binary counter has sufficient capacity (16 counts) to count the maximum time. The four stage counter is preset to the proper count to permit reaching its maximum count at the desired time. The "SET TIME" switch sets up the proper path for preset pulses at the start of the time interval.

The time interval is initiated by pressing the "START" push button. This flips BCR-12, used as a flip-flop, to a position which causes the NOR-1 circuit to pass 60 cps pulses to the 60:1 divider chain. This change in state of BCR-12 also triggers a monostable multivibrator (MMV) of approximately 1 ms duration. This 1 ms pulse is amplified in the power switch (PS) and used to preset all the BCR stages to their

proper positions. The preset pulse is fed through the "SET TIME" switch to the proper terminals of the BCR stages in the counting register to give the desired time interval. For example, to generate a 10-second interval, BCR-8 and BCR-9 are preset to their non-zero positions. Since BCR-8 has a value of 2 counts, and BCR-9 has a value of 4, a total of 6 counts is subtracted from the total capacity of the 4 stages. Thus, 16 less 6, or 10, one-second pulses are required to cycle the counter to a point where BCR-11 is flipped.

The fifth stage (BCR-11) of the counting register is used as a temporary memory to show that the time interval is over. This stage flips at the end of the time interval and flips back again 16 seconds later. This second change is used to reset BCR-12 and thus stop pulses from passing through the NOR-1 circuit. This completes the cycle of the timer. Pressing the START button initiates a new cycle.

Visual indication of the counter operation is provided by the lamp control circuits (LC-1 through LC-5). One is connected to each of the binary counter stages in the counting register (BCR-7 through BCR-11). The stages LC-1 through LC-4 indicate the instantaneous binary count in the register. LC-5 operated by BCR-11 indicates the end of the time interval.

CONCLUSIONS AND RECOMMENDATIONS

The family of circuits described herein represents a preliminary effort to solve the standard-circuit problem for those applications requiring low-frequency switching operations in a moderate temperature range. To the present, no attempt has been made to extend the frequency range above 15 kc or the temperature above 45° C although techniques for extending these ranges have been suggested. The use of several standard circuits in the construction of an experimental digital timer has been demonstrated.

Two directions for additional work appear attractive. First, an investigation should be made of circuits which may use the transistor in a more efficient fashion than present circuits. Second, linear circuits such as amplifiers should be examined for possible inclusion in the family of standard circuits. However, before adding any new circuit to the family, detailed theoretical and experimental work should be carried out to assure a complete understanding of its capabilities and limitations.

ACKNOWLEDGMENTS

The circuits described are the result of the contributions of many people. Helpful discussions were held with Philip Emile, Jr. and E. L. Cox. Specific thanks are due Amiel Goodman and Jack Nimitz for conducting temperature studies on the circuits.

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(5) Hunter, L. P., op. cit., p. 15-40.

(6) Emile, P., "Design of a Two-Transistor Binary Counter", a paper presented before the Symposium on Microminiaturization of Electronic Assemblies, Diamond Ordnance Fuze Laboratories, Oct. 1, 1958.

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(8) Emile, P., DOFL Report No. TR-487, "Design Considerations for Two Types of Transistorized Multivibrator Circuits", 1 Nov. 1957.

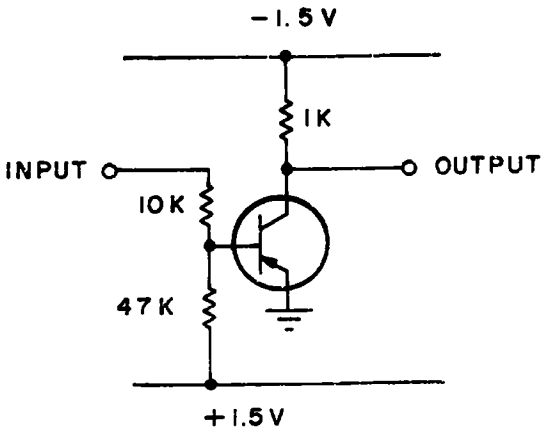


Figure 1. Inverter (IN)

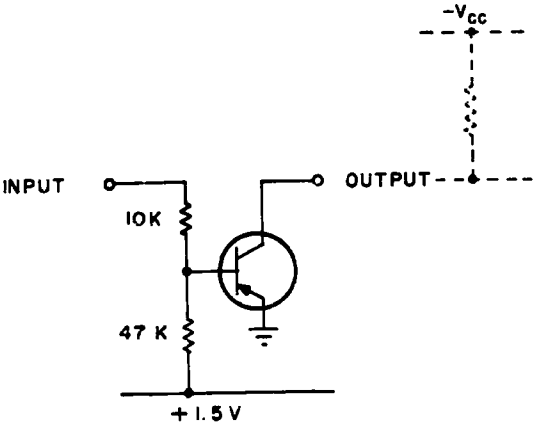
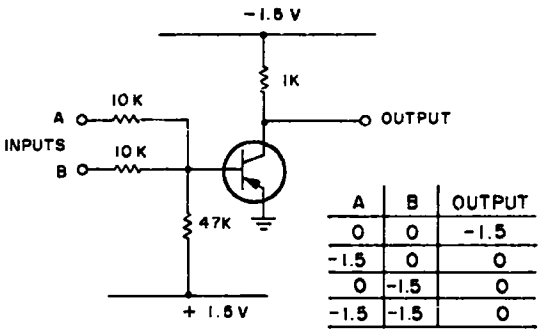


Figure 2. Inverter Less Load (INLL)



A	B	OUTPUT
0	0	-1.5
-1.5	0	0
0	-1.5	0
-1.5	-1.5	0

Figure 3. NOR

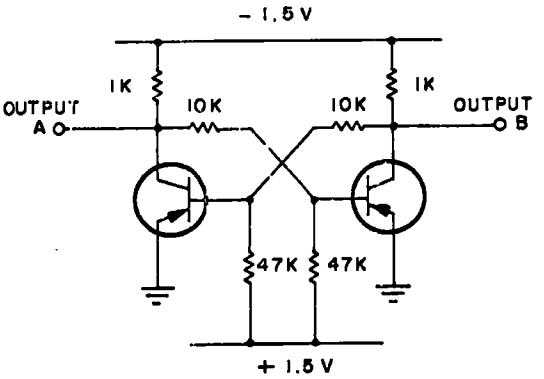


Figure 4. Flip - Flop (FF)

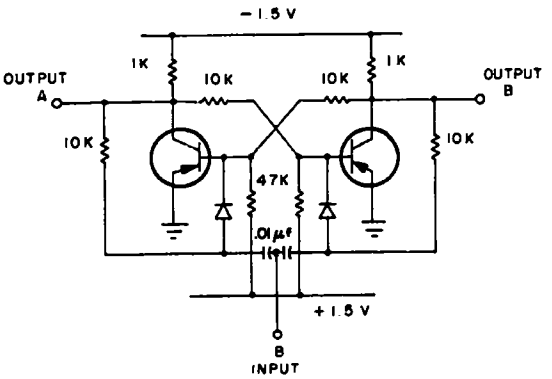


Figure 5. Binary Counter (BC)

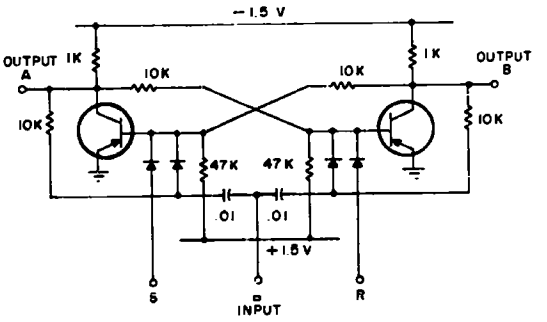
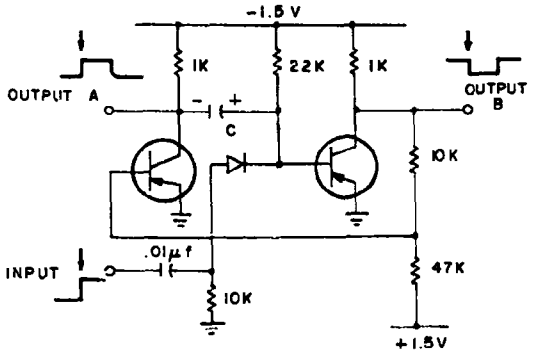


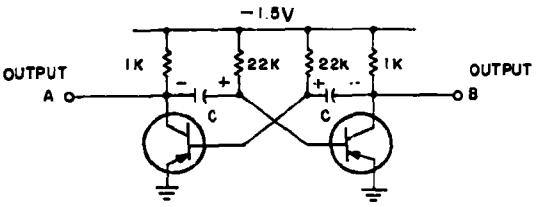
Figure 6. Binary Counter Resettable (BCR)



$T_{MS} = 15.4\ C_{\mu f}$

$C_{\mu f} = .065\ T_{MS}$

Figure 7. Monostable Multivibrator (MMV)



CHOOSE C FOR DESIRED FREQUENCY

$C_{\mu f} \cong \frac{32.4}{f_{cps}}$

Figure 8. Free Running Multivibrator (FRMV)

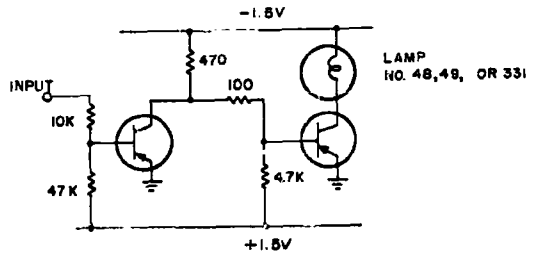


Figure 9. Lamp Control (LC)

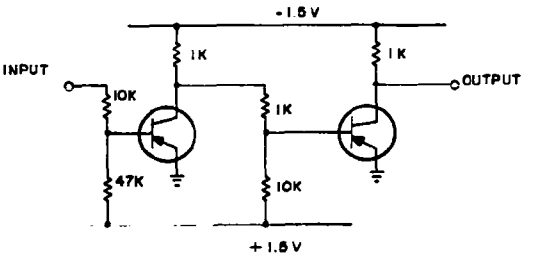


Figure 10. Power Switch (PS)

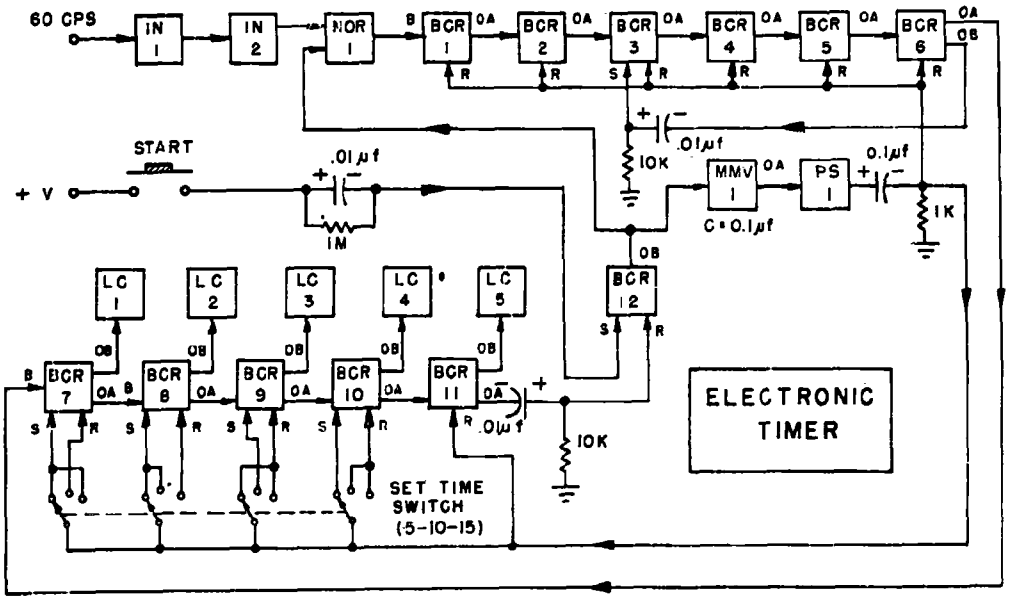


Figure 11. Block Diagram of Electronic Timer

THE ROLE OF SEMICONDUCTORS IN THE ARMY MICROMODULE PROGRAM

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ABSTRACT: The technical requirements for the Micromodule Program, as it is applied to semiconductors, are described in detail. Five major groups were established to characterize electric parameter requirements for transistors, and six major groups for diodes and rectifiers. The types of transistors to be modularized include low power audio and switching, very high frequency at 12.5 Mc to 30 Mc, and 70 Mc, and a power oscillator with one-watt power output at 70 Mc. The diodes include rectifier-detector, computer, regulator (zener), reference, AFC and FM modulator, and reactance tuning types. Similarity to commercial types is shown. The entire program is geared to the current state of the art in semiconductors.

Various approaches to repackaging semiconductors with hermetic seals are shown and described.

The transistor program is initially limited to germanium types; however, silicon will be used in later phases. Silicon is used almost exclusively in the diode portion.

Work now in progress is described.

INTRODUCTION:

Semiconductors play an impressive and significant role in the Army Micromodule Program. Because of the inherent advantages in size and power requirements of these devices, the initial effort was geared to the use of transistors and diodes as active elements.

The present program aims at the repackaging of existing transistor and diode types into wafer form factors, the dimensions of which have been tentatively set as .300 x .300 x .030 inches.

For the purpose of defining the characteristic requirements for parameters and circuit usage, the microtransistors and microdiodes, as they will hereafter be called, are separated into distinct groups. At present, there are five major groups for microtransistors, and six major groups for microdiodes.

TECHNICAL REQUIREMENTS:

The technical requirements or objective specifications for these devices are shown in Tables I and II:

TABLE I
TECHNICAL REQUIREMENTS FOR MICROTRANSISTORS

Group	Application	Typical Types
A	Audio	2N140
B	Switching	2N404
C	12.5 to 30 Mc IF	2N384
D	70 Mc IF	2N700
*E	70 Mc 1 watt	(Under Development)

*Group E represents the upper limit.

TABLE II
TECHNICAL REQUIREMENTS FOR MICRODIODES

Group	Application	Typical Types
F1	Low Frequency Rectifier-Detector	1N277
F2	Fast Sw Computer Silicon Junction	1N643
G1	Regulator	1N665 1N667
G2	Reference	1N430
H1	Reactance Modulator AFC and FM	V39 V56
H2	Reactance Tuning	V27E V58E

The above technical requirements are for the IPS Program. All work is geared to current state of the art, and little or no research and development is permitted. The initial phase of the microtransistor program is directed toward germanium devices, but silicon microtransistors will certainly be incorporated into the program later on. Except for one germanium group, the microdiode program is an all-silicon program.

The initial work is directed toward ambient temperatures of -65°C to +85°C, and junction temperatures of +100°C for the germanium microelements. With the advent of silicon into the program, these temperatures will be raised to +125°C ambient and +200°C junction temperature.

In addition to testing electrical parameters, extensive life tests will be conducted at high storage temperatures, and tests for mechanical ruggedness and operation under different environmental conditions will be carried out. These tests will be performed only on devices which have passed hermetic seal tests.

For parameter characterization, only one microdiode or microtransistor per wafer is contemplated; however, it is anticipated that multiple mountings per wafer can be accomplished.

The wafer material or substrate has not been definitely selected. It may be necessary to utilize different substrate materials for each of the groups previously mentioned. Substrate materials now under test include alumina and glass, beryllium oxide, and synthetic ceramics such as Mycalex.

SEMICONDUCTOR MICROMODULE PROGRAM:

The semiconductor micromodule program is divided into three phases in terms of samples. These are designated preliminary, prototype, and final samples.

Preliminary Samples. The preliminary samples (see Figure 1) are constructed in the following manner: Electrically tested and satisfactory pellet assemblies are used. The connector wires are reinforced with a silicone resin, and .003 inch nickel leads are welded to the base tab and existing clipped emitter and collector leads. After suitable bakeout, the pellets and base tabs are glued in place on the wafer substrate with an epoxy resin. The collector lead is threaded through a hole in the side of the wafer, and the base lead is soldered to its terminal. The collector is then soldered to its terminal. The assembly of the two wafers is accomplished by using an epoxy resin for the adhesive. These "in plastic" samples (see Figure 2) will not be evaluated in life tests, but will be used as tools by circuit designers attempting to translate circuits pertaining to specific equipment subassemblies into the micromodule concept. To accomplish this breadboarding, sufficient quantities of the different groups will be assembled.

Prototype Samples. Prototype samples (see Figure 3) will aim at true hermetic sealing. The pellet assembly (which has been tested electrically, or life tested at high storage temperature for increased reliability) is positioned in the wafer, and the base tab is held by solder to one corner. Connection to the emitter and collector is made by using drilled inserts to accommodate solder. The use of a dielectric coating over the pellet assembly is being considered to shield it from the solder poured into the connector holes. The base lead, which is normally attached to a side terminal of one wafer, could be brought through the top wafer to reduce capacitance if necessary.

The main seal uses a solder ring (see Figure 4), and may be made by using hot techniques involving simple heating, cold techniques involving molecular bonding of metals, resistance heating, or RF heating. Since the transistor elements are sensitive to fluxes, no fluxes will be used in any of the sealing approaches. With the use of a cold swaging seal using indium solders, additional mechanical strength can be achieved by injecting a plastic having the same thermal expansion coefficient into the space between the wafers, but external to the seal.

If resistance heating is used, the unused portion of the wafer will serve for electrical contacts, and direct heating will melt the solder. An alternative approach is to have many holes in the wafer to achieve contact resistance soldering.

In connection with these methods, work is in progress on ceramic-to-metal and metal-to-metal bonding using various metallizing compounds.

Other possibilities for hermetic sealing include a molded-in contact point for either emitter or collector connection, or deformation of an indium or solder-filled insert making contact with a resin-coated shaved dot. An alternative procedure is to fill the hole with solder, making contact to the shaved dot. The third approach is to utilize a metal shell insert for solder filling. Still another method is to use copper tubing soldered to the main seal and brought through holes in one of the wafers. The metal-to-ceramic bond has been evaluated and found to be hermetic (see Figure 5).

Final Samples. The final samples will undoubtedly be developments of prototype samples.

MICRODIODE PROGRAM:

The microdiode program is also in three phases. The preliminary samples phase consists of remounting available diodes in wafers. Glass silicon diode envelopes are fractured, and a .001 inch diameter copper lead is welded to the aluminum stud. For germanium diodes, a small hole is cut into the glass envelope, and an epoxy resin is placed at the wire-to-germanium surface for mechanical rigidity.

Prototype samples of hermetically sealed microdiodes will be worked on by subcontractors; therefore, no information is available regarding techniques other than those used in the transistor effort.

CONCLUSIONS AND RECOMMENDATIONS:

The semiconductor micromodule program shows great promise for achieving workable devices in a new form factor. Consideration should be given to utilizing the hermetically sealed semiconductor wafer configuration or package as separate or discrete devices outside of a stacked micromodule. This would require the attachment of terminal leads.

The successful completion of the repackaging phase of the program will represent a major advance in semiconductor electronics.

Figure 1. - Microtransistor, Preliminary Sample, Group C

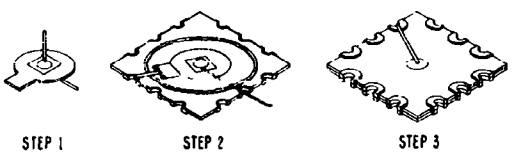

Figure 2. - Plastic Sealed Module Samples

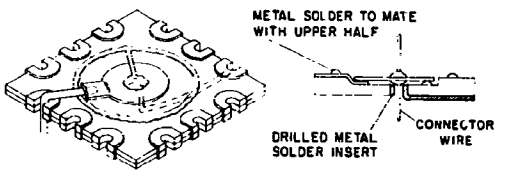

Figure 3. - Experimental Transistor Hermetic Seal

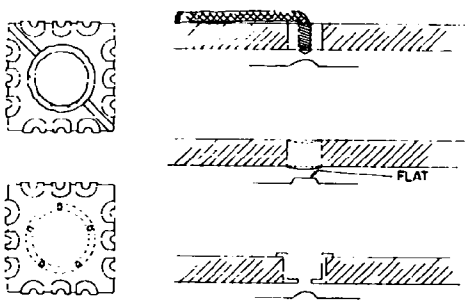

Figure 4. - Construction Items For Hermetic Sealing

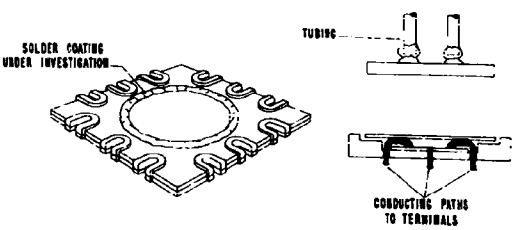

Figure 5. - Hermetic Seal Test of Bonding to Substrate

DEVELOPMENT OF MINIATURE ELECTRIC DETONATORS

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Picatinny Arsenal, Dover, New Jersey

A minimum effort has been expended on the development of miniaturized detonators. Work has not progressed rapidly in this field because definite requirements, which are now essential before development of a specific initiator can be started, were lacking.

Under the project "Supporting Research for Fuzes" a series of detonators having a diameter of 0.147 inch is being developed. These detonators were to be developed with the thought in mind to save space or provide a way for the fuze designer to produce a more versatile fuze utilizing essentially the same space.

In the miniature (.147-inch diameter) detonator series development has been completed on the carbon bridge detonators of wire lead and "button" lead types. Further developments in this miniature detonator series will include spark gap and wire bridge type detonators.

In the paper entitled "Explosive Trains for Miniature Electric Initiators", discussion was centered around the physical limits of propagation of the detonation wave of explosive trains. It can be stated that, from the point of view of the initiator design, these lower limits of design have not yet been reached, especially the limits on diameter. This is true principally because the requirements for the smaller initiators have not been made known. At present, the smallest electric detonators developed by the Ordnance Corps is a family of four 0.147-inch diameter detonators. These detonators, for lack of specific requirements, were not developed for any one particular fuze application but were designed, based on the best judgment of what the initiator designer thought the fuze designer might require in the way of a smaller detonator.

These 0.147-inch diameter detonators, which are designated as the T60, T61, T62 and T63 electric detonators (Ref 1, 2 and 3) all utilize the so-called "carbon bridge" as the transducer of electrical energy into a form of energy required for the initiation of primary high explosives.

The explosive train of the T60 and T62 detonators consists of a spot, intermediate and base charges of colloidal lead azide, lead azide and RDX, respectively. The explosive train of the T61 and T63 detonators is identical to that of the T60 and T62 except the colloidal lead azide used as the spot charge is replaced with milled lead styphnate. This change renders the detonator somewhat more sensitive but increased their functioning time.

All four detonators are housed in stainless steel cups approximately 0.006 inch thick. The T60 and T61 detonators are wire lead types utilizing a Bakelite plug to hold the wires, whereas the T62 and T63 detonators have the so-called "button" type contact. The length of these detonators, excluding the wire and button contacts is 0.342 - .010 inch. The resistance of the bridge circuits ranges from 1,000 to 10,000 ohms. The functioning characteristics of these detonators are as follows:

Electric Detonator	Functioning Level Capacitor Discharge Microfarad	Volts	Ergs	Function Time Requirement less than, microseconds
T60	.0022	300	1000	5
T61	.004	100	300	
	.021	65	450	50
T62	.0022	300	1000	5
T63	.004	100	300	
	.021	65	450	50

Each of these detonators is capable of initiating an RDX lead high order across an air gap of 0.090 inch.

Detailed information on the development of the T60 and T61 electric detonators can be found in Ref 4.

As mentioned above, each of the detonators just discussed is assembled with a carbon bridge. During the past 10 years considerable amount of work has been conducted in studying the mechanism through which such a bridge initiates an explosive material. As a result of work conducted principally through contracts of Ref 5, a much better understanding of the carbon bridge has been made available.

It is believed that the mechanism of the bridge as applied in initiating explosives is two-fold depending principally upon the characteristics of the functioning energy; more specifically, on the magnitude of the voltage used. At relatively low voltages, the bridge reacts similarly to a carbon resistor in that it dissipates the electrical energy into heat energy in accordance with Joules Law, I^2Rt. At relatively high voltages, however, it is postulated that conductive paths through the bridge are heated to such an extent that the negative temperature coefficient of resistivity of graphite becomes apparent. As a result the bridge becomes hotter and hotter finally resulting in the production of an ionized path with subsequent arcing. The production of the arc coincides with the initiation of the explosives. Details of this work is included in reports of the contracts of Ref 5.

During the past two years, a limited amount of work has been conducted in the study of "printed circuit" bridges. These bridges are made in a manner similar to those used to lay down resistors in the conventional printed circuit practice. Results of preliminary work indicates that such bridges can be used in the design of electric initiators. Through the use of such techniques and materials presently available, it is visualized that a bridge of an initiator can be developed with almost any resistance characteristics (both static and dynamic) to match any power source with any desired sensitivity level.

In line with the work being conducted towards miniaturization of fuze components, there is no overwhelming reason why we cannot expect to utilize printed circuit techniques in the application of fuze explosive components. Of course, due to the hazardous nature of explosive materials (especially when assembled as a fuze component), certain precautions will have to be taken.

Some work has already been conducted in providing multi-purpose detonators. While this may not reduce the size of present day fuzes, it will enable the fuze designer to produce a more versatile fuze of the same size. Two such detonators, under development, are the T29 and T48. These detonators can be initiated directly by either mechanical or electrical energy. The intermediate and base charges of these detonators are common to both initiating systems. The maximum diameters of the T29 and T48 detonators are 0.241 and 0.192 inch, respectively. Further consideration for the design of multi-purpose detonators, including delay components, is under consideration.

REFERENCES

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2. Ordnance Corps Drawing FXP-94405A dated 2 May 1957, "Detonators, Electric T60 and T61, List of Parts. List of Specifications and Standard".

3. Ordnance Corps Sketch PX-98-1507 dated 15 November 1957, Detonators, Electric, Button Type (.147 dia). Contour Drawings.

4. R. E. Tresona and D. E. Seeger, "Development of Electric Detonators T60 and T61", Picatinny Arsenal Technical Report - in preparation.

5. Picatinny Arsenal contracts with The Franklin Institute, Laboratories for Research and Development, Nos. DAI-36-034-501-ORD-(P)-29; DAI-36-034-ORD-2142; DA-36-034-501-ORD-73

ANTENNA MINIATURIZATION

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The reduction of the resonant length of linear antennas by various loading methods is described. It is shown how folding may be used to improve the impedance and bandwidth characteristics of loaded antennas. Methods of reducing the size of slot antenna systems are also considered.

One of the more important problems confronting the designer of antennas for military applications is that of finding sufficient space for efficient radiating and receiving systems. The problem is particularly acute aboard ship, on aircraft, and on missiles. One phase in the solution of this problem is the investigation of methods of reducing the physical size of an antenna system without seriously degrading the electrical characteristics.

Let us first consider methods of miniaturization of the dipole (or monopole) type of antenna. The classical methods of reducing the length of linear antennas has been either inductive or capacitive loading. Capacitive loading is accomplished by placing a conducting surface at the extremity of the radiating element. When a large degree of loading is desired, the resulting configuration is generally so ungainly that its use is limited to a few special applications. Inductively loaded antennas are, in general, more compact, since loading is accomplished by placing a solenoidal coil in series with the radiating elements. Inductive loading of the monopole was investigated experimentally.[1] Several test monopoles between 0.065λ and 0.171λ were loaded to resonate at 100 ± 1 mc.

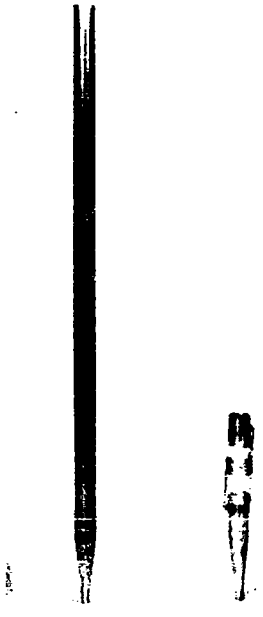

Figure 1. Standard monopole and 0.072λ test monopole.

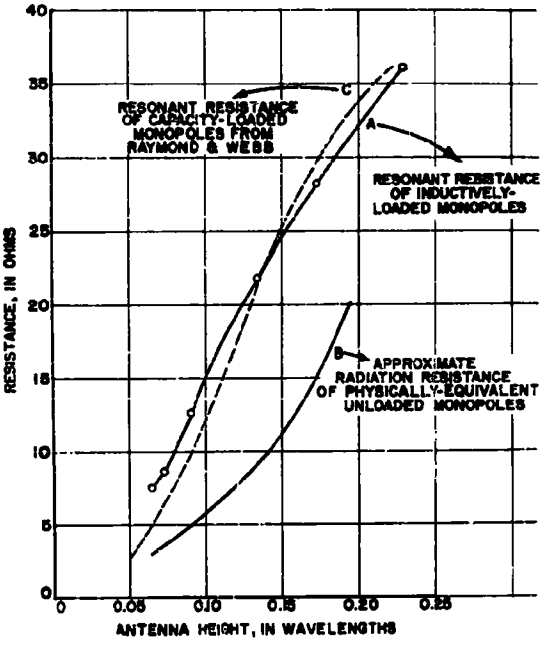

Figure 2. Resistance at resonance vs antenna height for series of inductively-loaded monopoles.

An unloaded monopole, .228λ high, was used as a standard of comparison. The unloaded monopole and one .072λ in length are shown in Figure 1. Measurements show that as the antenna is successively shortened, the radiation and bandwidth are reduced. In Figure 2, Curve A shows the radiation resistance of the antenna as a function of the antenna height in wavelengths. Also shown is the resistance of shortened unloaded antennas and, for comparison, the radiation resistance of similar capacitively loaded monopoles plotted from data published by Raymond and Webb[2]. It can be seen that for heights less than 0.16λ, the loaded antenna, besides being resonant, has more than twice the resistance of its unloaded counterpart.

There will be power dissipated in the windings of the inductor. This power loss, along with the decrease of bandwidth and resonant radiation resistance, limits the extent to which inductive loading can be employed in shortening the antenna.

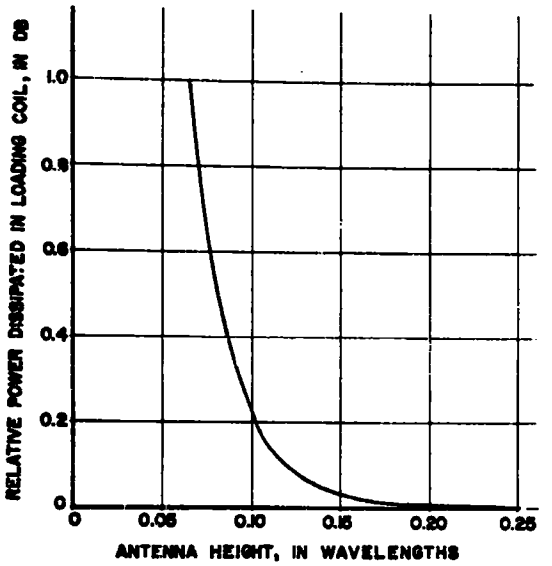

Figure 3. Relative power dissipated in loading coil vs antenna height for series of inductively-loaded monopoles.

The position of the coil affects to some degree power dissipation and radiation resistance. It was found that coil losses were minimum when the distance from the top of the antenna to the lowest terminal of the inductor is about one-third the total height of the antenna. The amount of power dissipated in the loading coils of the shortened antennas was determined by comparison of their power radiated with that of the unloaded standard. The results are shown in Figure 3. The .065λ loaded antenna radiates about 80% of the power fed it, which is satisfactory for most practical applications.

The impedance and bandwidth of an antenna may be increased by folding, i.e., placing one or more elements in parallel with the driven element. Figure 4 shows a diagram of an inductively loaded, folded monopole[3]. By varying the ratio of D_f/D_d, the diameter of the folded element to the driven element, a range of radiation resistances is available. For example, the resonant resistance of an antenna .072λ long, which was tested, had a range of resonant radiation resistance of from 20 to several hundred ohms.

The capacitively loaded monopole, although requiring more space, has the advantages of no coil loss and better bandwidth. Figure 5 shows a typical capacitively loaded, folded monopole. E. W. Seeley has reported that it is possible to build efficient antennas of this type with a length of only .03λ with a resonant resistance of 50 ohms and half-power bandwidth of 8%[4]. A practical form of the capacitively loaded monopole at low frequencies is the guy wire-loaded, folded monopole pictured in Figure 6. The antenna pictured has a radiation resistance of 47 ohms at 11 mc, although its height is less than .10λ. This type of antenna has application aboard ship and at air stations where large vertical structures are prohibitive. For example, the main mast of a destroyer could be used as part of such a system, producing an antenna system resonating at about 1 MC.

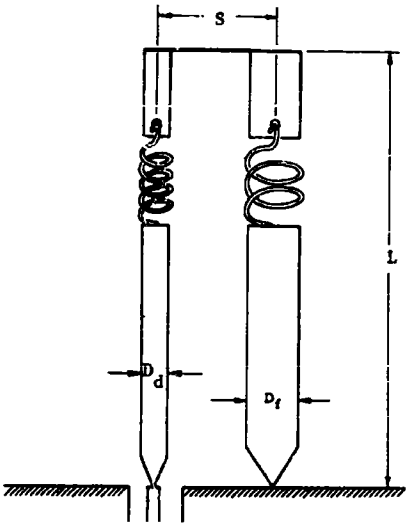

Figure 4. Inductively loaded, single-folded monopole.

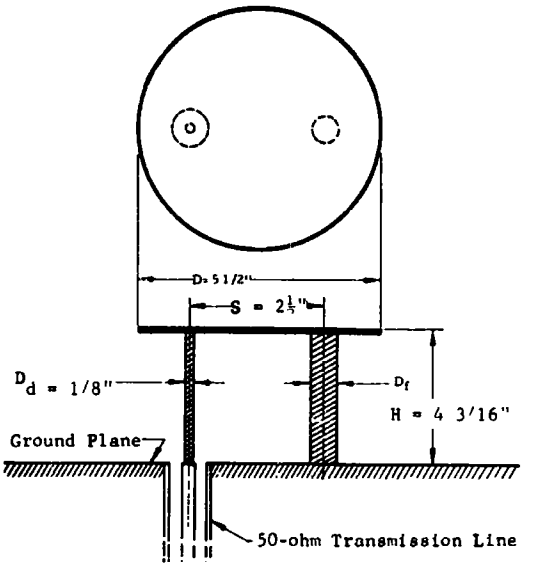

Figure 5. Capacitively loaded, folded monopole.

Height - 8.66 ft
Diameter of grounded conductor - 1.0 in
Diameter of feed conductor - 0.156 in
Resonant frequency with 3 guy wires - 14.15 mc
Resonant frequency with 6 guy wires - 11.82 mc
Resonant frequency with 6 guy wires
and skirt joining guy wires 8.5 ft
down from the top - 9.2 mc

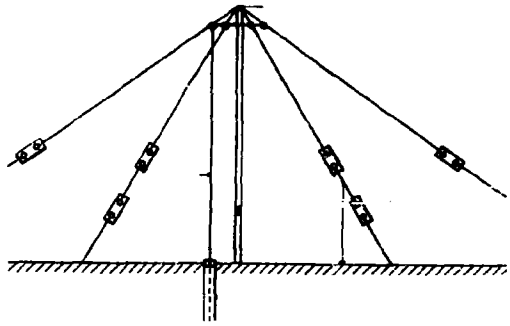

Figure 6. Guy-wire-loaded, folded antenna.

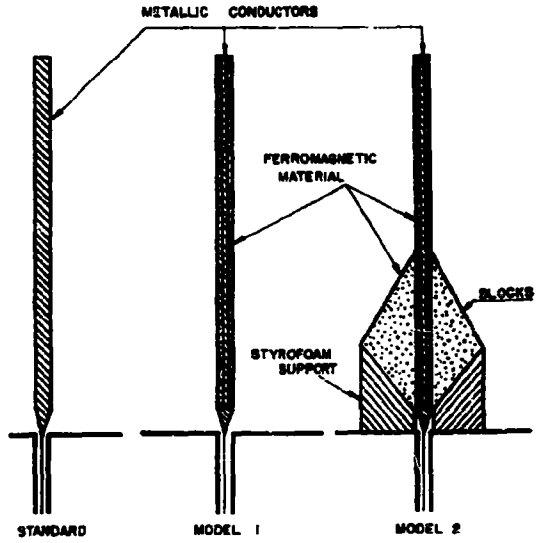

Figure 7. A standard monopole and two ferromagnetically loaded monopoles.

In addition to inductive or capacitive loading, it is also possible to decrease the resonant length of an antenna by surrounding it with a dielectric sheath[2]. This, too, will reduce the radiation resistance by an amount proportional to the degree of loading. There will also be power losses due to the dielectric.

Ferromagnetic materials may be similarly used. Figure 7 shows experimental monopoles used to test ferromagnetic loading[1]. Models 1 and 2 in this figure were loaded with a cylinder of ferromagnetic material around the metal radiator. Model 2 also had ferromagnetic blocks stacked around the base which provided additional loading. The effects of loading are shown in Figure 8. It can be seen that the resonant frequency is lowered by 10% and 20% in the two models and that radiation resistance is slightly lowered. Ferromagnetic loading has been found to be particularly effective used with loop antennas.

The slot antenna has application in flush mounted systems of missiles and aircraft. Here reduction in size is very important. The reduction of slot antenna systems can be approached in two ways:
1) shortening the slot length by loading, and
2) reduction of the cross-section or volume of the transmission line or cavity associated with the slot.

Let us first consider reducing the slot length. The simple slot is operated at resonance where it is physically one-half wavelength. Methods of reducing the length of the slot antenna and making compensating changes in the electrical characteristics are suggested by considering methods which have been used with linear antennas.

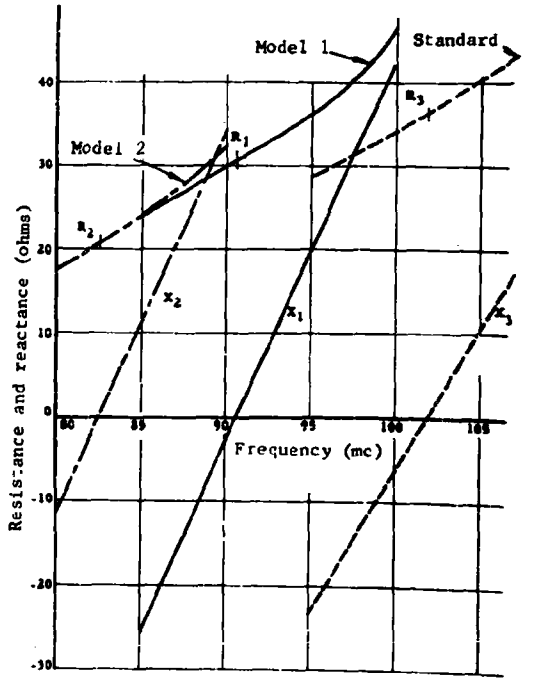

Figure 8. Resistance and reactance vs frequency for two ferromagnetically loaded monopoles and an unloaded standard monopole.

A method which has been used to load the slot is to deform the slot to a dumbell shape shown in Figure 9. The length L for a particular frequency is shortened as a the diameter of the end circles is increased and b the gap distance is decreased. A dielectric cover used in practical applications also loads the slot and shortens its electrical length. The amount of shortening depends on the dielectric constant and the thickness of the cover. Similarly ferrites may be used to load and shorten the length of the slot.

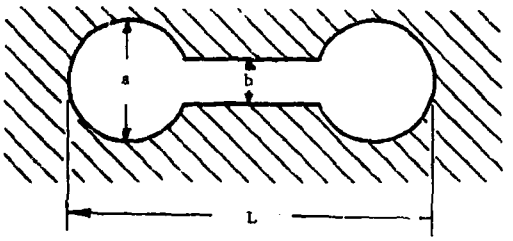

Figure 9. Dumbell shaped slot.

Folding may be accomplished by cutting a slot parallel to the driven slot and connecting them at the ends. Folding will, in general, decrease the radiation resistance and can be used for matching purposes. Experimental investigations have been made at NOLC to determine the possibilities of loading and folding methods applied to slot antennas[5]. A slot was cut in a sheet of copper-clad, Teflon-impregnated fiberglass, Figure 10a. This was mounted in a copper ground plane and fed at the center with a 50 ohm transmission line. Impedance measurements were made to determine resonant frequency and radiation resistance. The 90% and 50% power bandwidths were found by means of the Smith Chart. The simple slot was resonant at .4 wavelength due to the loading of the dielectric. The 50% and 90% power bandwidths were 32% and 12% respectively. The slot was deformed to the dumbell shape keeping the physical length the same, Figure 10b. The resonant length was reduced to about .24 wavelength which is a reduction of over 50% from the 1/2 wavelength of an unloaded slot; however, the 90% power bandwidth was reduced to 5% and the radiation resistance increased to 2000 ohms, too high for good matching. Next, folding was tried, Figure 10c. For a folding slot of the same width as the driven slot, the 50% and 90% power bandwidths were increased to 60% and 14%, i.e., greater than the simple slot. Resonant resistance was 300 ohms and 30 ohms at first and second resonances. Variation of the ratio W_f/W_d, the folded slot width to the driven slot width, gives a range of values for the radiation resistance as shown in Figure 11, making efficient matching possible. Varying the ratio W_f/W_d has relatively little effect on the bandwidth or resonant length of the slot. Loading and folding does not seem to have too great an effect on the radiation pattern. A check was made on the polarization. The maximum E field was perpendicular to the loaded folded slot, with the cross polarization down 30 db.

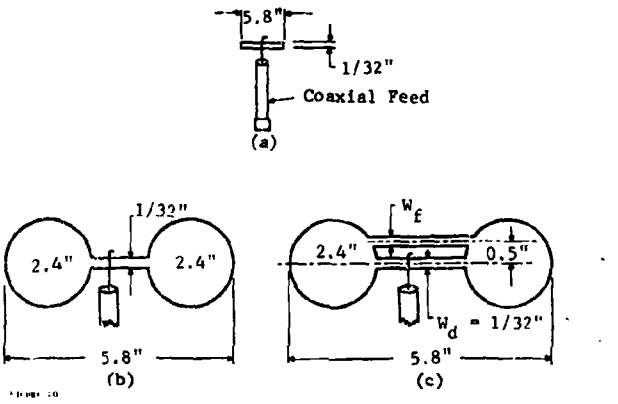

Figure 10. Slot configurations.

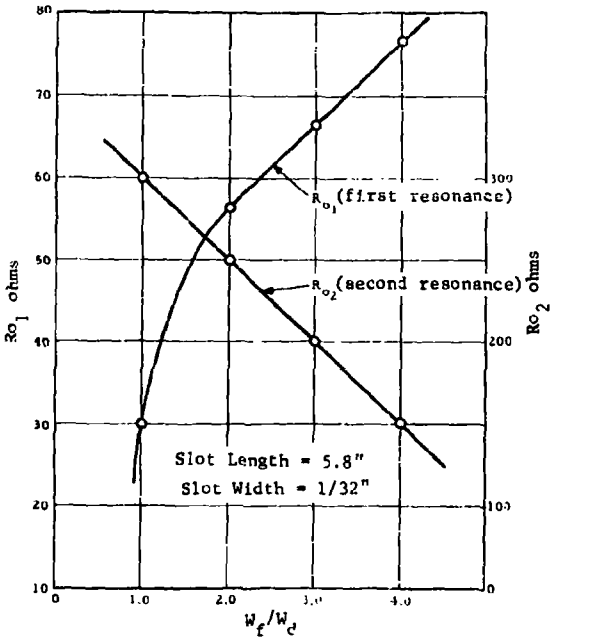

Figure 11. Resonant resistance vs folded slot width.

The slot antenna being somewhat comparable to an elongated loop would seem to offer good possibilities for ferrite loading. Some experimental investigation has been carried out at NOLC using ferrites to load slots[3]. The commercially available IRN-8 and IRN-9 ferrites were used. Strips were cut to be inserted in the slot. The slot was fed at the center and impedances plotted by the standing wave method. The loading reduced the resonant length of the slot by 39% and 43% for the ferrites used. Radiation resistance increased from 320Ω to 495Ω and 545Ω. Bandwidth was reduced from 9.4% to 3.9% and 3.3%.

As was stated before, a slot antenna system may be reduced in size by decreasing the volume or cross-section of the associated cavity or transmission line used in practical applications. The cavity does not need to be resonant at the same frequency as the slot, so this does not restrict the size of the cavity. However, the cavity presents a parallel reactance to that of the slot, the value of which depends on the cavity dimensions. Therefore, a reduction in cavity size could affect the resonant length of the slot. It has been reported that this effect is negligible if the cavity is about $\frac{1}{4}\lambda$ deep. If the cavity depth is reduced to less than this the slot will be loaded so as to increase its resonant length.

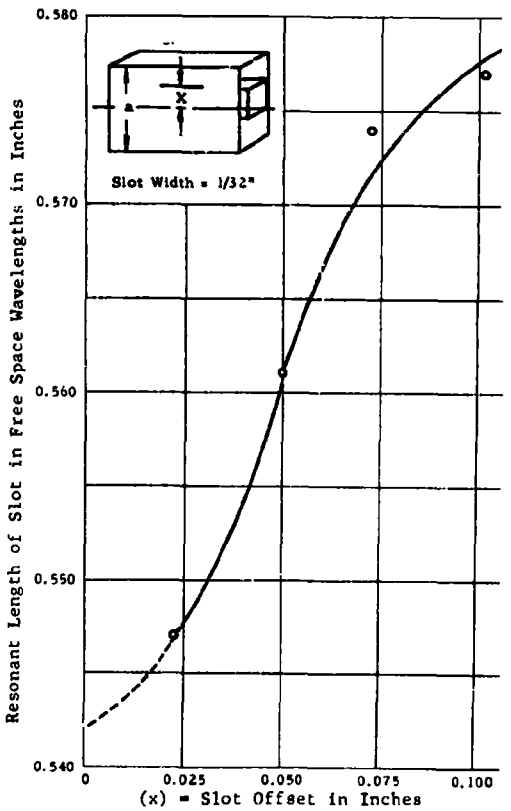

Figure 12. Longitudinal shunt slot in ridge waveguide.

There are two ways which have proved satisfactory in miniaturization of the transmission line section; these are use of TEM line and the use of ridge waveguide. It has been shown that the series inclined slot can be used in TEM guide and the associated volume reduction as compared with the standard TE_{01}-mode guide is as much as 100[6]. Figure 12 shows a ridge section using X-band waveguide at C-band with the resonant length plotted as a function of the slot offset. The maximum reduction in volume of the cavity has been 10 for this configuration.

In summary, it can be stated that it is possible to considerably reduce the resonant length of linear antennas without seriously degrading their electrical characteristics by various loading and methods used in conjunction with folding. An example given, a capacitively loaded, folded monopole, had a length of only .03 wavelength with satisfactory electrical characteristics.

The length of the slot antenna may be shortened using loading methods similar to those used for linear antennas and a cavity behind a slot may be reduced in size, but for depths less than $\frac{1}{4}\lambda$ it will load the slot so as to increase the resonant wavelength. Use of TEM line or ridge waveguide permits a reduction in volume of the feed line.

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SURVEY OF EQUIPMENT ADAPTABLE TO MICROMINIATURE CIRCUIT TECHNOLOGY

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Because of the small physical size and delicate nature of the component parts in microminiature circuit assemblies, special problems will arise in processing and orienting each element in the circuit during assembly operations. Elements to be considered include dielectric base plates, conductors, resistors, capacitors, transistors, diodes, inductors, and protective coatings.

This paper presents several modes of handling each of the above elements. The equipment described is either currently being used for fabricating microminiature electronic circuit units or is currently being used for fabricating larger assemblies but appears to be adaptable to microminiature assemblies. Both hand and automatic equipment are considered.

INTRODUCTION

In recent times there is an increasing demand for greater versatility in military electronic devices and hence for more complex circuitry with an accompanying greater bulk[1],[2]. Microminiature circuits permit the use of electronic assemblies that otherwise would be too large to incorporate in missiles and satellites. Circuit assemblies having component densities of over two thousand components per cubic inch are considered microminiature for the purposes of this paper.

It is encouraging to hear of the strides which are being made in the microminiaturization of electronic assemblies by hand methods in the laboratories. This is a necessary first step, but in order to fully realize the military and civilian potential of microminiaturized devices, optimum means of producing these devices in large quantities are necessary. For maximum saving of space, each component of the circuit is placed in a module without any individual casing[3],[4],[5] or other protective element and is dependent on the protection afforded by the final circuit package. Each element of the circuit is, therefore, small in physical size and extremely delicate in nature. Due to the small dimensions of each element, extreme precision must be employed in placing each component in its proper position in the circuit since only a minute misalignment of any element may cause an improper contact with the rest of the circuit elements. At the present time, microminiature modules are being assembled by tedious hand methods. By mechanization, these units can be produced more efficiently and with increased reliability[6] since the error due to the human element would be minimized. In this paper, equipment adaptable to the assembling of microminiature circuit assemblies will be discussed.

Several types of elements that must be handled in the fabrication of a microminiature electronic circuit are as follows:

1. Dielectric base plates
2. Conductors
3. Resistors
4. Capacitors
5. Transistors and diodes
6. Inductors
7. Protective coatings

Each element will be discussed as to type, general physical characteristics, status of the art in handling the component, and equipment that could be adapted to handling the component in production. Figure 1 illustrates a microminiature circuit assembly and also the individual components used in the circuit.

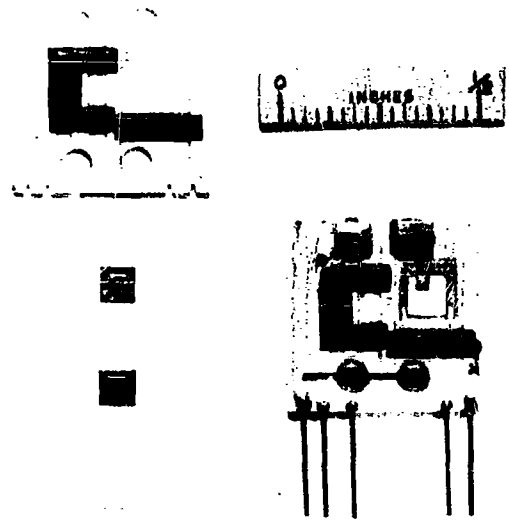

Figure 1. Lower right, a microminiature electronic module which will permit a component density of 2800 components per cubic inch; upper left, the base-plate wafer with conductors and resistors printed on it; lower left, top to bottom, a transistor, a diode, and a capacitor - for insertion in the holes in the base plate.

1. Dielectric base plates

In a sense the base plate is the nucleus of a microminiature electronic unit; it is essentially the matrix. The base plate is a thin wafer of dielectric material and upon it are attached all the components of the circuit. In an effort to miniaturize, the physical dimensions of the base plate are kept so small that

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it in itself is fragile, but the finished unit becomes rugged because of the addition of a protective coating and the arrangement of the components on the base plate. At the Diamond Ordnance Fuze Laboratories, an electrical grade of steatite is used for this wafer which is usually twenty thousandths of an inch thick and either one-half inch square or one-quarter inch square. Holes are placed in the wafer to receive the transistors and diodes, and cavities are made for capacitors. The fragile wafers are at present handled by hand methods with the aid of tweezers and micromanipulators. In mechanizing the assembly-operation of microminiature electronic circuits, one of the most formidable problems is the handling and indexing of these wafers without damage during the successive operations involved in producing a finished unit. The operation to be performed on the wafer is an important factor in the selection of a mechanism for conveying and positioning the wafers. Because of this, detailed descriptions of handling and holding devices for the wafers will be given in the sections which deal with the attachment of the particular components to the circuit, rather than in this section.

Certain phases of the handling are, however, basic and can be applied generally to all operations, for example, the feeding of the wafer to the conveyor before processing and the removal of the wafer from the conveyor after processing. The conveying device for all operations could be either some type of endless belt or an indexing rotary table. Fig. 2 is an

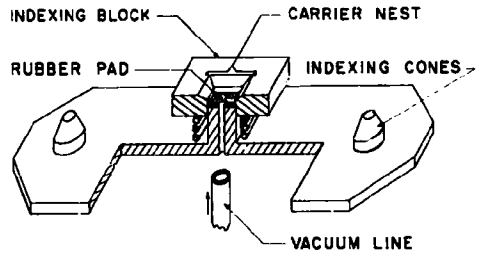

Figure 2. Carrier assembly for conveying and indexing wafers, showing spring that holds indexing block in raised position.

illustration of a conveyor carrier assembly that could be used with either of these conveying devices. The wafer is dropped into the carrier nest and is hence oriented with the indexing cones that orient the printing head with the wafer. The wafers can be picked up from a stack and placed on the conveyor carrier by an arm with a vacuum finger (Figure 3). If there is any particular desired orientation for the wafers, they should be put in the stack oriented. Vacuum could also be used to hold the wafer on the conveyor before, during, and after the particular operation. Because the wafer is very light in weight, the vacuum technique is particularly adaptable in that a relatively low vacuum applied to a small area will be able to support the weight of the plate.

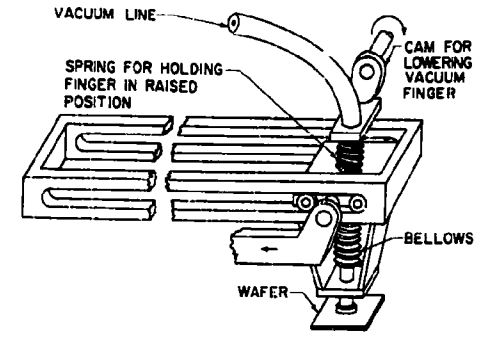

Figure 3. Vacuum-finger-type mechanism for feeding dielectric wafers from a stack to a conveyor.

A vacuum arm may not be practical as a take-off mechanism for a wet printed wafer because the vacuum finger would smear the wet pattern on the top of the plate. A device which would appear suitable for the removal of the wafer from the conveyor is an arm with a tweezer-type end, Figure 4. This arm would pick up the wafers by their edges and place them on the conveyor that will carry them to the next operation.

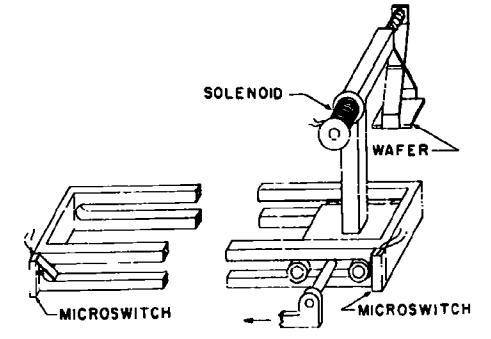

Figure 4. Tweezer-type-arm for feeding or removing wafers to or from a conveyor.

A straight pusher-type of take-off mechanism, where a finger pushes the wafer off the conveyor and onto some horizontally moving receiving device, can also be employed. Another type of take-off mechanism can be used where the carrier is made so that at the take-off position a member of the carrier assembly raises the wafer vertically; a fork-like finger can then pick up the wafer and transfer it to a position over a second conveyor where the wafer is displaced onto the conveyor by a pusher in the fork arm

mechanism, Figure 5.

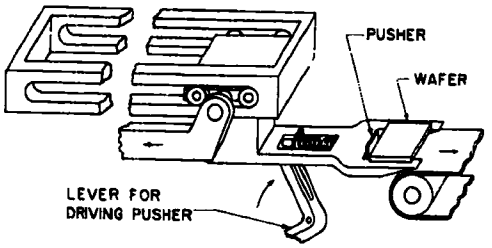

Figure 5. Fork-type arm for transferring printed wafer.

2. Conductors

In a microminiature electronic circuit with component densities in excess of two thousand per cubic inch, the conductors, except for terminal leads, are usually of the deposited metal type. The conductor patterns can be deposited on a dielectric material by screen printing, spraying, or vacuum deposition. Terminal leads are attached to the unit by soldering or by conductive cements.

Hand operated equipment is currently being used for screen printing conductive patterns onto dielectric circuits. Screen printing has been carried out for many years[7]. Automatic machinery for screen printing is currently available for large plates and appears to be adaptable to small wafers. Here the problem is not so much in the printing operation itself as in the feeding, conveying, indexing, holding and take-off of the fragile wafer.

An example of an automatic high-speed screen printing machine is shown in Figure 6. This machine is capable of printing conductive

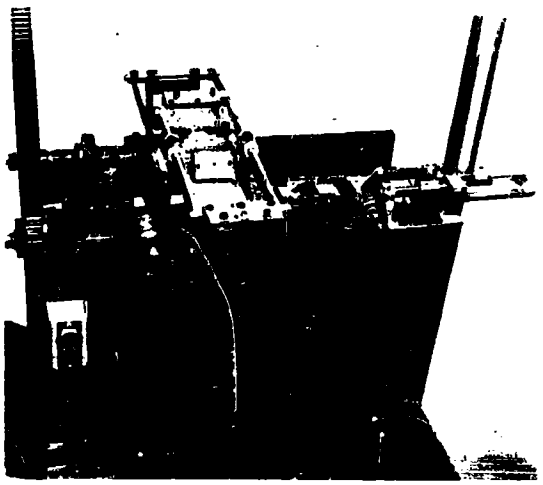

Figure 6. Top view of screen printing machine showing (right to left): feed, conveying, printing head, and take-off mechanisms.

patterns on dielectric plates at rates of six thousand plates per hour. The dimensions of the plates currently printed on this machine are one inch wide, one and one-quarter inch long and one tenth of an inch thick. This machine appears to be adaptable to printing the microminiature wafer. The printing head of this machine would be maintained essentially as is. The stack feed with the pusher on the bottom of the stack is not desirable for thin wafers because the bottom wafer would be carrying the weight of the stack and this, coupled with the force of the pusher necessary to push the wafer onto the conveyor, would probably break the wafer. A stack feed could be used where the wafers are removed from the top of the stack and the level of the top of the stack is maintained by a rod which is driven upward a distance equal to the thickness of one wafer for each cycle of the machine, see Figure 7. The wafers can be taken from the top of the stack by either a tweezer-type arm or a vacuum-type arm similar to the ones described earlier in the section on base plates. Power to operate this arm can be obtained by linking to

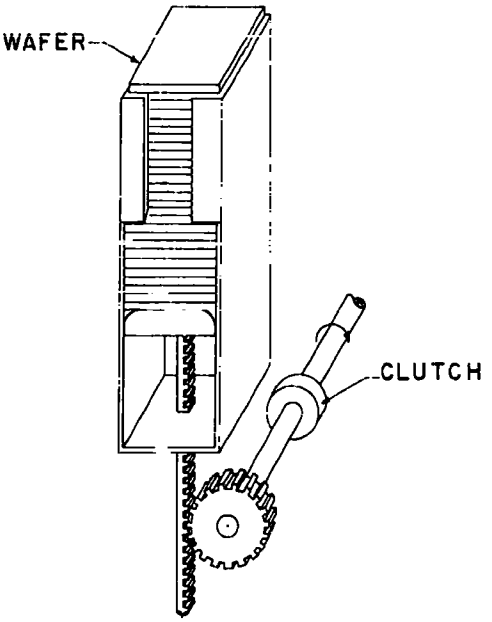

Figure 7. Stack feed with mechanism for maintaining top wafer at constant level.

the same mechanism that drives the pusher in the present machine. Vacuum instead of spring-loaded levers can be used to hold the wafers during the printing operation. Although a pusher-type take-off could possibly still be used, a fork-type or tweezer-type arm, as previously described, appears to have excellent adaptability to this take-off operation. The plates taken off the machine would probably be placed on trays or a conveyor belt instead of the racks shown in Figure 6. This machine

definitely appears to be adaptable to microminiature applications.

In the redesign of a screen printing machine, such as the one shown in Figure 6, an indexing rotary table, instead of an endless belt conveyor, should be considered, because it probably will be necessary to have more complex carriers than those presently employed and a rotary table requires only a few carriers. In order to eliminate the requirement that each carrier be indexed precisely with respect to the printing head of the machine, and to provide for precise indexing of the pattern on the wafer, the printing head and conveyor could be modified. Figure 8 illustrates schematically a possible modification. The portion of the printing head that carries the patterned screen can be made to float, that is, to have some movement in the plane of the wafer surface, angularly and in two directions perpendicular to each other. The patterned screen frame can then have two members with tapered holes which will mate with tapered pins that are a part of the carrier unit, and are precisely located with reference to the wafer indexing mechanism. This modification would optimize the indexing accuracy of the machine, which, in its current form, produces ninety-four percent acceptable plates.

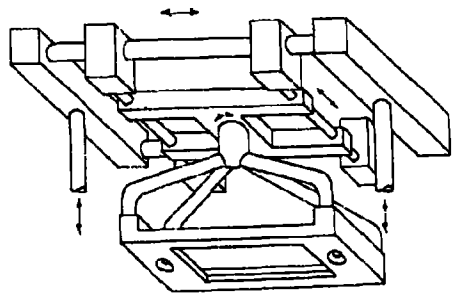

Figure 8. Floating head showing freedom of motion in the printing plane, angularly, and in two directions perpendicular to each other.

Conductors are also deposited on dielectric wafers by vacuum deposition methods[8],[9]. A boat containing the metal to be evaporated, and then deposited on a dielectric, is heated in a high vacuum chamber. The metal molecules are deposited on the dielectric in a pattern governed by the mask which is placed on the dielectric wafer. At the present time, vacuum deposition is generally a batch-type process. Several properly masked wafers and the boat containing the metal to be evaporated are placed in a vacuum jar, the jar is evacuated, the metal source is heated, the metal is vaporized, and hence deposited on the wafers. The vacuum is released, the jar is raised and the patterned wafers are removed. This batch process could be made continuous by placing a supply of blank wafers in the bell jar and, by the use of remotely controlled mechanisms, the wafers could be continuously fed and indexed behind masks containing the desired patterns. The wafers would be shielded from the unwanted metal vapor both before and after the deposition of the metallic pattern. Vacuum deposition appears to be adaptable to microminiature applications.

Conductor patterns can be placed on dielectric wafers by spraying techniques. A mask containing the desired pattern is placed over the wafer and a spray of silver paint is directed over the mask. A silver pattern similar to the one on the mask is left on the plate. Spraying is not as widely used as screen printing. The masking problem becomes somewhat difficult in the spraying process and hence the pattern definition is sometimes not sharp. Smearing of the mask with the wet paint also contributes to poor pattern definition. This is a problem in the larger patterns, and will become an even greater problem in the microminiature applications. It appears that where silver patterns are to be applied a screen printing process will generally be employed.

Wire is used for terminal leads as shown in Figure 1. The wire is approximately twelve thousandths of an inch in diameter. The wires are now placed in the circuit assembly by hand operations. They are attached to the circuit either by soldering or with a conductive cement[10]. Soldering presents problems in the small wafers: the heat applied to components, such as transistors and resistors, can modify their electrical characteristics, and the thermal shock on the thin wafers, due to local applications of intense heat required for soldering, may cause the wafer to crack.

In production, wire could be fed from spools, through dies, cut to size, and attached to the circuit with conductive cement. The wire is placed in slots in the wafer as shown in Figure 1 and the conductive cement is applied. The viscosity of the cement is such that it holds the leads to the circuit until the cement is cured.

3. Resistors

Methods which have been employed to apply printed resistors to circuits are as follows:

1. Screen printing
2. Injection molding
3. Pen
4. Vacuum evaporation
5. Tape

The same screen printer as that shown in Figure 6, and described earlier for applying conductive patterns on dielectric materials, could be used for printing resistors simply by using an appropriate pattern and a resistor ink formulation, rather than silver paint. Hand screening methods are presently being used in the laboratory production of printed resistors for microminiature circuits. Screen-printing of resistors has proven to be satisfactory but the method is not as versatile as some others which allow greater control in the depth of each resistor.

The injection molding method for resistor

printing is based on the pressure filling of an appropriate matrix with resistor ink and transfering the ink from the matrix to the surface of the dielectric plate(11). A schematic diagram of this process is seen in Figure 9.

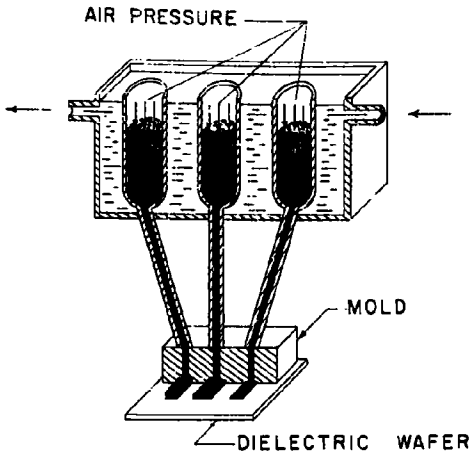

Figure 9. Schematic diagram of water-jacketed-injection molding printer showing delivery of ink from three reservoirs to a three-cavity mold.

The value of the printed resistors is controlled by varying the resistor ink formulation used, and by varying the dimensions of the matrix-cavities which in turn define the length, width, and depth dimensions of the resistor. Figure 10 shows an injection molding-type machine for printing resistors. This machine is designed so that it can simultaneously print up to twelve resistors on a dielectric plate, each having, if necessary, a different formulation of resistor ink.

At the feed position of the machine, cams open the spring loaded levers which hold the dielectric plates indexed with respect to two perpendicular edges on the conveyor carrier. At present each blank plate is manually placed in the carrier nest. The conveyor carries the plate to the printing position. The printing head of the machine floats, i.e. it can move parallel to and perpendicular to the conveyor and it can also move angularly. When the plate is indexed in the printing position, the printing head is lowered by two positive displacement cams, one on each side of the machine. When the printing head approaches the conveyor carrier, two cone-shaped holes engage two cone-prongs on the carrier assembly. Since the cones on the carrier assembly have been precisely located with respect to the edges used to index the dielectric plates, the matrix is precisely indexed with the dielectric plate. The matrix, which is usually made of a resilient material, makes contact with the dielectric plate with enough pressure so that the resistor ink will not seep but with not so much pressure that it will distort the shapes of the cavities in the matrix. When the matrix is in contact with the plate, air pressure is applied to the ink reservoirs so that ink flows into the cavities in the matrix. The pressure is applied for the length of time required to fill the matrix cavities. The part of the machine cycle during which pressure is applied to the ink is made variable by using a solenoid valve and a cam-actuated

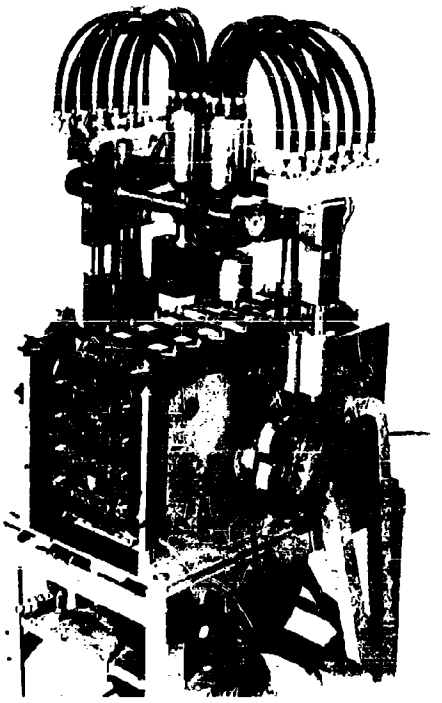

Figure 10. View of injection molding-type resistor printing machine showing (top to bottom): ink reservoirs, floating head, conveying mechanisms, and positive displacement cam for raising and lowering printing head.

switch to control the air pressure. When the filling time is up, the pressure is released from the ink reservoir and the printing head is raised by the positive displacement cams. The printed plate then eventually advances to the take-off position where cams again release the pressure of the spring loaded levers on the edges of the plates permitting them to be removed from the carrier nests. This machine is designed so that there can be variations in the pressure of the printing ink, the temperature of the printing ink, the pressure of the matrix, the speed of the machine during the printing phase of the cycle, and the speed of the machine during the transfer phase of cycle.

With the microminiature wafer, control of the pressure between the matrix and the wafer may become critical because too much pressure may break the wafer and yet sufficient pressure is required to obtain a seal between the matrix and the wafer surface. This machine can print two plates at a time and appears to be readily adaptable to microminiature circuit applications. As in the screen printer, the primary problems arise in the handling of the base plates. Here, also, the previously described feed mechanisms of tweezer-type or vacuum-type transfer arms can be used to place the wafer on the conveyor carrier nests from the top of a stack like that shown in Figure 6. The motion for actuating the transfer arms can be obtained by linking to the up-and-down motion of the printing head. Carrier nests similar to the ones described in the base-plate section of this paper may be employed. Vacuum can be used to hold the wafer during the printing operation. Take-off mechanisms similar to the ones suggested previously in this paper can be used. Here also an indexing rotary table could be used very effectively.

The pen method is another process by which resistors can be printed[12]. The mechanism, as illustrated in Figure 11, is essentially a tube containing resistor ink. The tube has a hypodermic-needle-like outlet. The ink is forced out of the outlet by air pressure. The

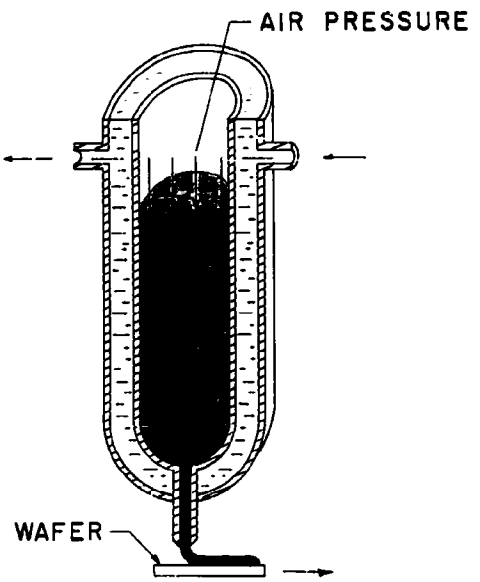

Figure 11. Schematic diagram of water-jacketed pen-type printer showing delivery of ink to a moving plate.

tip of the needle is passed across the surface of the dielectric plate leaving a ribbon-like layer of wet resistor ink on the plate. In this process, a pen assembly is required for each different resistor to be printed. Therefore, the wafer must be conveyed and indexed to as many pen stations on a machine as there are resistors on the plate. This method permits control of the length, width and depth of the resistor. The speed at which the pen passes over the plate, the temperature of the ink and the pressure applied on the ink can all be controlled. This method has been used for large plates and has worked quite satisfactorily. It requires a separate printing operation for each resistor but appears to be adaptable to microminiature applications.

Thin-film resistors produced by vacuum evaporation techniques can also be used in microminiature circuit assemblies. In the vacuum deposition of resistive materials, as with conductive materials, batch processes are presently used but, as stated previously in this paper, a continuous-type production operation could be obtained.

Another type resistor that can find applications in microminiature circuit assemblies is the tape resistor[13]. The resistor ink is placed on a thin asbestos tape by a continuous spray process and the resultant resistor tape is then cut to the desired dimensions and placed on the circuit plate. This process has been used in the production of large printed circuit assemblies with satisfactory results and could be applied to the microminiature applications by adapting similar machinery.

4. Capacitors

An example of a typical capacitor[14] used in microminiature circuits is the one shown in the lower left hand corner of Figure 1. It is a wafer one tenth of an inch square and one hundredth of an inch thick and has a capacitance of one hundredth of a microfarad. Silver electrodes are screened on each side of the wafer. These wafers are attached mechanically and electrically to the circuit with conductive cement. In the DOFL units, a cavity for receiving the small capacitors is placed in the wafer with a cavitron after the conductor pattern has been fired on the wafer. The capacitor could also be attached to the circuit by soldering, but in that case thermal shock may be a problem and, since the capacitor is placed in a cavity in the wafer, a conductor would have to be applied in the cavity and contact made with the rest of the circuit.

These small capacitors could be placed in the circuit with a machine having similar feed, conveying, indexing and take-off mechanisms as discussed previously in this paper. With the wafer indexed in the machine, a mechanical arm could move precisely over the area where the capacitor is to be attached and apply conductive cement to the area. Then a vacuum type-arm could pick a capacitor from a stack and precisely place it in the circuit. This insertion of the capacitors could be done by a two-station only machine or by two stations of a machine which also inserted transistors, diodes and inductive components.

Another approach to the capacitor insertion

problem is to use a body with high dielectric constant as the base plate and let it serve as the dielectric of the capacitor. This would eliminate the capacitor insertion problem and require only the printing of the electrodes which would be done during the conductor printing operation.

5. Transistors and Diodes

Transistors and diodes, as seen in Figure 1, are similar in physical size and nature and, therefore, they will be discussed here as one type of component.

The microminiature transistors used are produced by applying photolithographic and vacuum deposition techniques to a germanium wafer forty-five thousandths of an inch square and ten thousandths of an inch thick. A more detailed description of the fabrication of these transistors is available in the literature [3], [15]. These transistors are presently being produced by hand methods in the laboratory [16], but can be mass produced by implementing photolithographic and vacuum deposition techniques for large scale production.

The finished transistors and diodes, as seen in Figure 1, consist of the processed germanium wafer. They are soldered to a thin metal base plate in order to facilitate the insertion of the component in the circuit assembly. The transistor is placed in a hole in the dielectric base plate and the thin metal base plate which has been soldered to the transistor overlaps the hole edges and locates the transistor so that the surface of the transistor-contacts are in the plane of the base-plate surface. Voids in the hole in the ceramic wafer between the transistor and the wafer are filled with a suitable resin prior to depositing leads connecting the transistor with the rest of the circuit. Contact between the transistor and the rest of the circuit is made by vacuum depositing aluminum leads from the contacts on the transistor to the proper points on the conductor pattern on the ceramic wafer.

In a mechanized assembly operation, the base wafer would first be indexed on a conveyor and, by the use of vacuum finger-type arms, the transistor or diode would be placed in the proper hole in the base wafer. Conductive cement would be used to make contacts between the baseplate of the transistor and the circuit. After the conductive cement had cured, a supply of the semi-finished electronic assemblies would be placed in the chamber of the vacuum deposition machine so that, by remote controlled arms, each assembly would be placed in position behind a mask and the necessary leads vacuum deposited to each assembly. As the successive components are placed on the base wafer, the assembly may become awkward to handle. In some instances, it may be desirable to time the placing of one of the components so that it can be used for orienting the assembly in a succeeding operation.

6. Inductors

Inductive components tend to be large and, although considerable progress has been made in miniaturizing them, there does not exist at the present time an inductive component that meets the size requirements of the microminiature circuit assemblies being considered in this paper. Attempts by some laboratories to produce microminiature inductive components have not as yet produced satisfactory components. Small inductive coils have been developed by the manufacturers of hearing aids and although they represent great accomplishment in microminiaturization they occupy greater volumes than entire micro-miniature circuit assemblies.

The approach taken at the present time, in order to realize optimum space savings, is to substitute R-C circuits for inductive circuits wherever possible. A paper will be presented at this symposium which will consider some aspects of this approach [17]. In some cases, coils can be printed [18], but they require considerable surface area of the base plate and only a very limited range of values from one tenth to one microhenry can be achieved. In the limited number of cases where printed coils can be used, the same printing methods described earlier for printing conductors or resistors can be applied.

7. Protective coatings

Protective coatings are an essential part of any printed circuit assembly. This is especially so of a fragile microminiature circuit assembly for operational military applications which must undergo extreme environmental and handling conditions. Units are protected against moisture, heat, pressure, shock and vibration, arcing between components, and long periods of storage under adverse conditions [19]. Each microminiature circuit can be protected individually, or where the individual circuit is a stage of a larger assembly, the entire unit can be protected.

Methods which are generally used for applying protective coatings to electronic circuit assemblies are as follows:

1. Screen printing
2. Spraying
3. Dipping
4. Potting

The same screen printing equipment that is used for printing conductors and resistors can be used for applying protective coatings. Screen printing is generally used when certain portions of the circuit are to be electrically insulated prior to completing the assembly operations.

A plastic protective coating can also be sprayed on either the finished unit or at some intermediate stage during the fabrication of the electronic assembly.

Protective coatings can be applied to a unit

by dipping the entire unit in an appropriate coating material. Care must be taken that the coating material can be applied and cured at a temperature sufficiently low that it will have no ill effects on the components in the circuit. In selecting a dip-coating material it is also desirable that it jell at room temperature so that it will not run off prior to curing. In production, the coating can be applied to each unit by using an endless belt conveyor to which the units will be fed and the conveyor will convey the units through the dipping and curing operation. The conveyor can be made to index over a pot containing coating material at proper temperature. The pot then would raise to immerse the unit and lower at a desired rate to produce a satisfactory coating.

Potting is a process that will be especially useful in protecting larger units such as stacks of small assemblies [20]. The stacks can be placed in reuseable molds or in casings that will stay with the unit. The potting material can then be poured into the mold or casing as it is conveyed by resin dispensing equipment. Descriptions of equipment and techniques for applying casting resins are available in the literature [21], [22].

CONCLUSIONS

There is little doubt that many problems must be solved in mechanizing the fabrication of microminiature electronic assemblies, but none of the problems appear to be insurmountable. In general, most of the operations have been employed successfully in applications dealing with larger units. The methods and equipment must be extended to cover the microminiature assembly.

Caution should be exercised in deciding the degree of mechanization that is economically desirable to achieve [23]. A certain amount of mechanization will be essential to the production of large quantities of electronic assemblies. However, since microminiature technology is so new and there is almost day-to-day change in the type of components used, machine developments should not be undertaken where the equipment cannot be amortized [24]. In all cases equipment should be designed so that it can be adapted to meet new requirements.

ACKNOWLEDGMENT

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A STUDY OF THE ELECTRONIC PARTS & ASSEMBLIES OF THE HAWK, LACROSSE I, & NIKE HERCULES MISSILES

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The HAWK, LACROSSE, and NIKE HERCULES missiles represent the latest in Army Ordnance. Each contains complex electronic packages requiring high reliability. In order to enhance the missiles survival during severe operating environments and to reduce the size and weight of the missiles' payload, present state-of-the-art miniature parts are being used.

This study will compare in the above missiles:

a. The relative number of miniature electronic parts
b. The use of printed wiring
c. The use of machine assembly
d. The efficiency in the use of available space.

Summary:

My subject deals with the present day selection and application of electronic parts in guided missile systems. In particular, the missile electronics of the HAWK, NIKE HERCULES, and LACROSSE I systems will be reviewed. Although this material does not cover radical innovations in the field of miniaturization, the program chairman has seen fit to include this paper on the program. Perhaps an understanding of present applications would enable those of you in design work to get an added feel for military requirements.

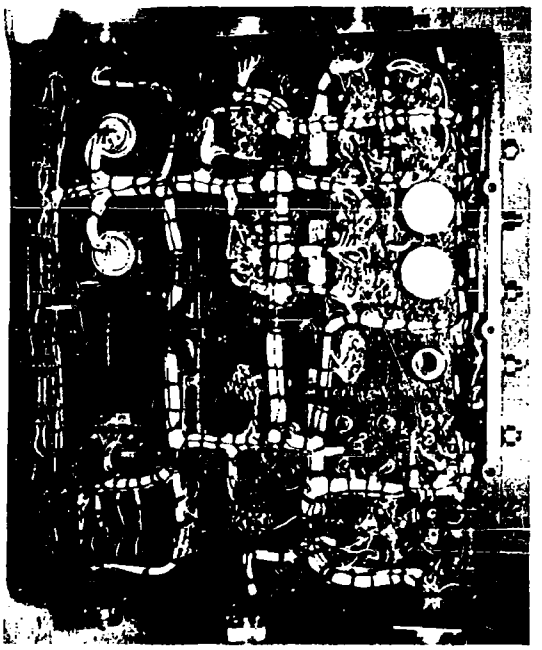
Introduction:

Greater demands in accuracy and reliability of missiles are changing the appearance of the missile electronic package. Our first generation of systems, the NIKE AJAX and CORPORAL, used JAN or commercial parts with conventional World War II wiring in typical black boxes. In the present day systems, NIKE HERCULES, HAWK, LACROSSE, and DART, a transition is evident by the admixture of some printed wiring boards, encapsulated sub-assemblies, and a wide use of non-standard parts. The next generation may use guidance packages of throw-away micro-miniature assemblies where space restrictions are imposed by waveguides and hydraulic systems, rather than by electronic and electro-mechanical assemblies.

Problem Area:

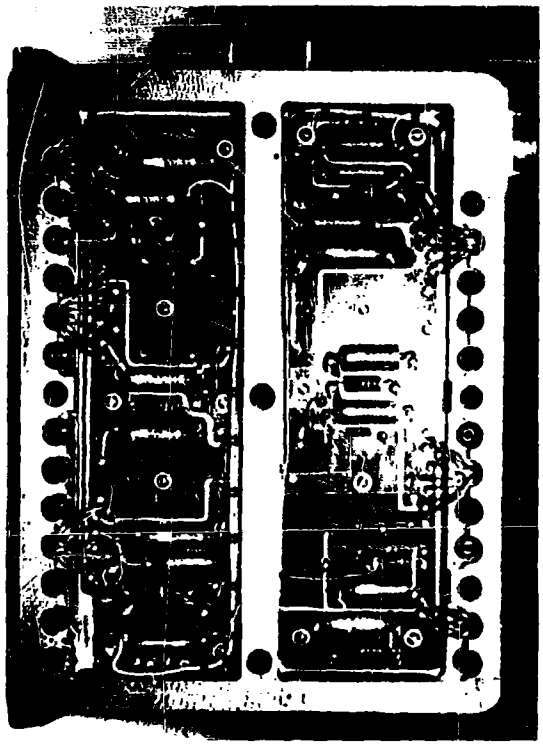
To define our problem in packaging electronics, consider the CORPORAL. A CORPORAL battalion is authorized some 320 vehicles of equipment TO&E 6-545D. Both operators and maintenance technicians are highly skilled and well trained for their mission. Obviously, the use of micro-miniature parts, modular packaging amenable to machine assembly, and a revision of operation and maintenance concepts to allow more replacement and less repair would reduce the complexity of present operations.

Slide one shows a typical CORPORAL wiring and layout. Note the lack of heat sinks, the absence of support ribs in the chassis, and the maze of wiring.



Slide 1: CORPORAL

The CORPORAL system is not to be written off because of outdated packaging. Readiness dates prevented the designers from incorporating new techniques during R&D. The CORPORAL III system has modern ground equipment and would correct the outdated features in the ground equipment as noted by this slide. Furthermore, in field test firings, the CORPORAL IIA has demonstrated a higher reliability than any other Army missile system. This reliability has been the result of many factors including a product improvement program whereby over half the missile electronic circuits as noted in slide one, were converted to configuration as shown in the following slide.



Slide 2: CORPORAL

HAWK:

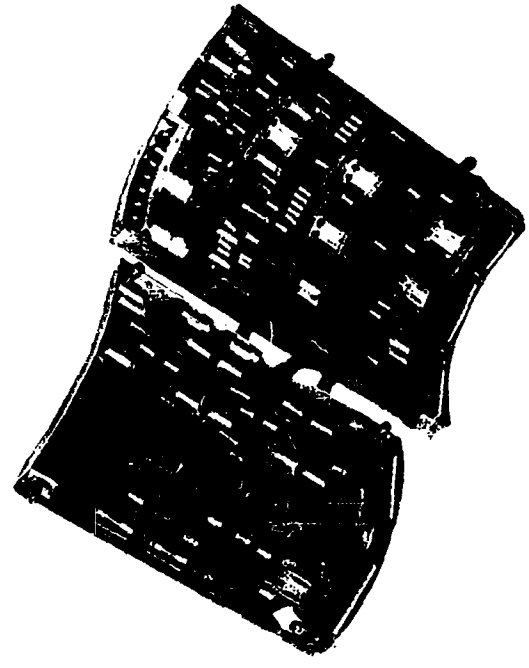
A picture of our progress can be portrayed by a look at our present day developments. The HAWK missile-borne electronics is packaged principally within two units: the seeker and the autopilot. Many parts have been made non-standard by additional environmental requirements; that is, by further selection processes at the plant.

The HAWK missile electronics part breakdown is approximately:

Capacitors:		
Ceramic		46
Mica		46
Tantalum		35
Paper		156
Glass		73
Electrolytic		3
Titanium Dioxide		8
	Total	367
Tubes:		146
Crystals and Crystal Diodes:		81
Transformers:		55
Resistors:		
Composition		484
Wirewound		11
Deposited Carbon		373
	Total	868
Inductors:		
AF Reactors		3
AF Toroids		3
RF Coils		46
RF Toroids		3
Others		4
	Total	53

This total count is over 1520 electronic parts exclusive of cables and connectors.

The parts are laid out within the cylindrical section of the missile for ready accessibility. Batteries, dynamotors, and large heavy hardware are mounted along the longitudinal axis whereas the circuit parts are neatly mounted on curvilinear laminates in periphery and parallel to the missile skin. Raytheon was directed to provide for repair by part replacement and a more accessible layout for the electronic parts would be hard to visualize. The following slide shows the nature of the assembly of the cylindrical platters.



Slide 3: HAWK

The electronic part density in the HAWK missile is in the vicinity of 2,000 per cubic foot. The present day maxima using printed wiring boards is around 50,000.

HERCULES:

The NIKE HERCULES missile guidance package has undergone a recent packaging redesign. The new package is a "modular" one with subassemblies more readily accessible and is commonly called "the mushroom guidance" package.

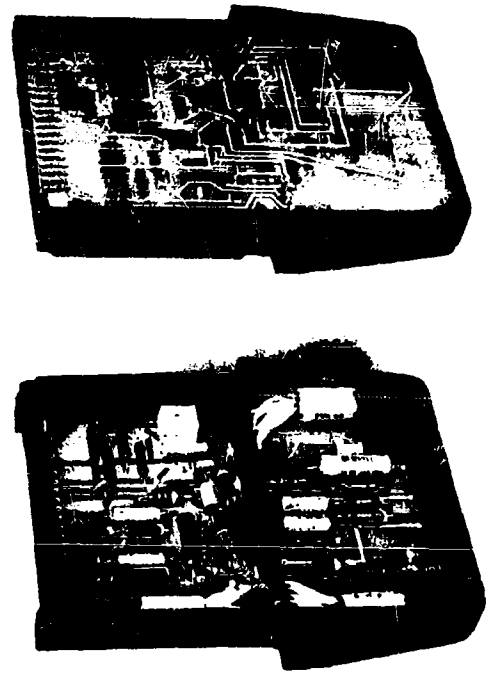
The HERCULES missile electronic parts count is approximately:

Capacitors:		
Mica		25
Paper		97
Tantalum		8
Glass		7
Ceramic		15
Others		17
	Total	169
Resistors:		
Composition		107
Wirewound		12
Deposited Carbon		120
Variable		31
	Total	270
Vacuum Tubes:		40
Crystals and Crystal Diodes:		80
RF Inductors:		18
Audio Coils and Transformers:		15
Other Parts:		10

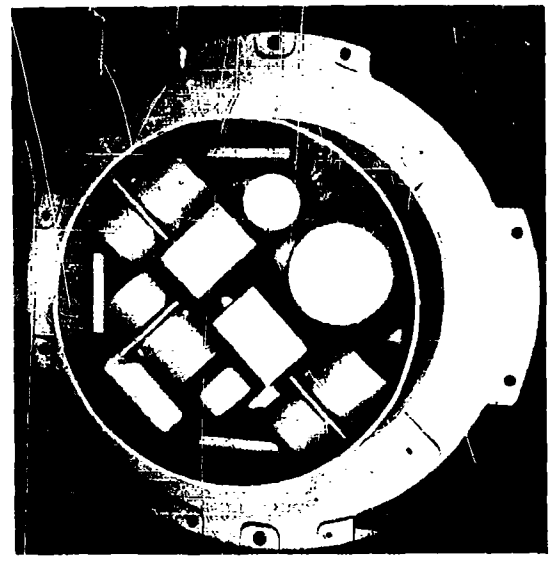
This total count is approximately 602 parts.

Actually, for a tactical operation, the parts count for the HERCULES might be considered less than the 600 items assembled. Over half the parts are mounted in printed wiring boards and therefore would not be subject to individual replacement. The Western Electric process for assuring good solder joints to printed wiring boards requires a 3 cycle thermal shock after soldering. Field replacement of an item to the board where soldering is involved is not planned. The high failure items, vacuum tubes, are mounted on the cast frames that house the printed board assembly and are replaceable if need be, although even this item is considered better replaced at 5th echelon.

There are 22 printed wiring boards in the HERCULES guidance package. Reliability tests showed no general necessity for encapsulation, therefore, only one subassembly is sealed in epoxy resin and a second unit in silastic rubber. The majority of the coils, however, have been encapsulated for better configuration with respect to assembly in the modules and for environmental protection.



Slide 4: A HERCULES Module



Slide 5: Mock-up of HERCULES "Mushroom" Instrument Side

LACROSSE:

The LACROSSE I missile guidance package in contrast to HAWK, provides all presently available techniques of assembly. The five missile electronic Ord 7 assemblies contain 20 potted subassemblies and use 18 printed wiring laminated boards.

The LACROSSE electronic parts count for the missile is as follows:

Capacitors:		
Mica		102
Glass		32
Paper		40
Tantalum		2
Ceramic		3
Variable		5
	Total	174
Resistors:		
Wirewound		23
Composition		207
Deposited Carbon		53
Variable		13
	Total	296
Inductors, AF:		15
Inductors, RF:		109
Diodes & Crystals:		30
Tubes:		47
Relays:		10
Miscellaneous:		26

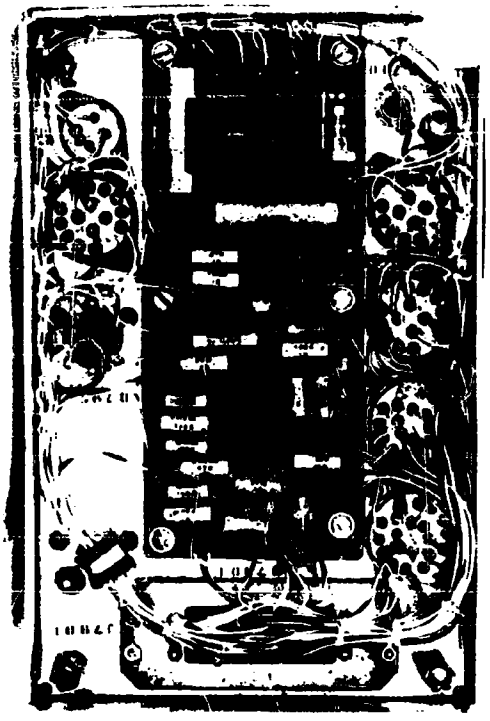
The total count then is approximately 697. The following slide shows the layout.

The LACROSSE guidance package is subdivided into five chassis, replaceable by an operator when failure is evident as indicated by an automatic tester. Piece part repair within the five chassis is accomplished by back-up Ordnance Corps maintenance technicians. Parts density in the LACROSSE I missile is of the order of 1,000 per cubic foot. Many RF cavities contribute to the relative low part density.

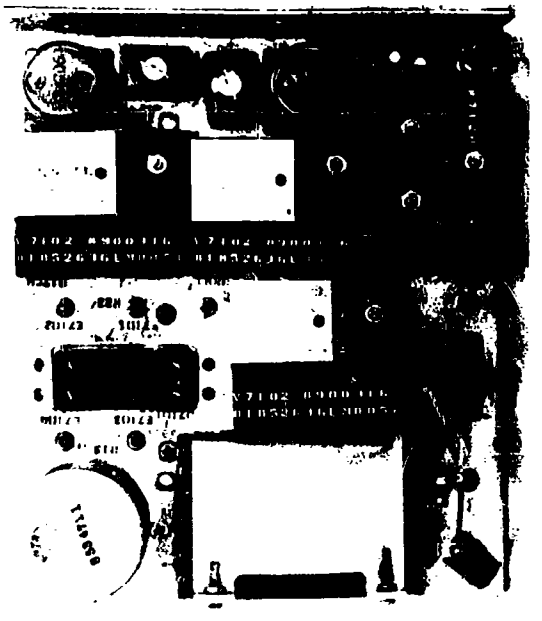
In comparison, the three missiles compare thusly:

	Missile Electronic Parts		
	HAWK	HERCULES	LACROSSE
Total Parts	1520	602	697
Non-Standard	90%	50%	80%
Type Maintenance-Replacement	Part	Module	Part & Potted Assy

Until early this year, the maintenance philosophy promulgated by the Ordnance Corps for missile systems was based on AR 750-5, that is, the traditional five echelons. By interpretation, field repair meant test equipment for fault isolation to the piece part and repair by part replacement.



Slide 6: A LACROSSE Chassis Wiring



Slide 7: Top View of LACROSSE Chassis

This maintenance philosophy has been modified, and repair is now permitted by replacement of modules. Accordingly, the SERGEANT, NIKE ZEUS, & LACROSSE MOD I systems will be packaged in modular form and a reduction in field repair and maintenance skills is evident in their TO&E's.

The use of non-standard parts is of great concern in the industrial phase of a missile program. Each part peculiarly stocked as a replacement part adds an additional burden on the supply system. Furthermore, if the part is a new development which may be inadequately tested, it is also a threat to reliability. Many of the parts in the systems discussed have been made non-standard by the addition of specifications for environmental extremes of temperature and shock not contained in the Mil Spec of the comparable part.

A part selected by environmental testing does not necessarily have a greater resistance to failure than one not so selected. However, complex missiles can hardly be expected to function unless constructed under extreme conditions of quality control and this begins with incoming inspection of electronic parts. Reliability takes precedence over standardization.

By the reliability formula, or the produce rule, the overwhelming number of missile-borne electronic parts makes the guidance package the most suspect for in-flight failures.

When initiating this study, I expected to find a relationship between reliability and missile electronic part selection and assembly. However, no trend was evident. In field test firings the missile with the greatest part-count has shown the greatest reliability. Factors other than complexity must be more influential in field operations.

The electronic package in one guided missile is only 2% of the total weight of the missile and 2% of the volume. Miniaturization of components in servo or hydraulic systems would pay off greater dividends in space savings than in the electronic area.

Miniaturization efforts on electronic parts and assemblies will be the trend for our future systems. The criteria of reliability and ruggedness point toward miniaturization as a possible solution for better performance. Although the HAWK, HERCULES, and LACROSSE I may derive no benefit from the miniaturization efforts described at this symposium, our missile designers are anxious to incorporate new features in the next generation of systems now in the planning stage.

THE STABILITY OF SEMICONDUCTORS IN MICROELECTRONIC ASSEMBLIES

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As progress is made in the direction of microelectronic circuit development, the problems of stabilization and protection of the components and especially the semiconductors assume a major role. The several processing steps leading toward the completed and stabilized unit and the determination of the extent of the semiconductor stability are considered. A description is given of the use of the "Field Effect" technique for rapid observation of stability. The measurement and analysis of the effects of some semiconductor surface treatments are described.

Introduction

The need for stable and dependable electronic devices in fuzing and other ordnance assemblies is self-evident. For stability in microminiaturization, careful consideration should be given to the components of the assembly. The close physical association of the many components each with exacting electrical and material requirements makes necessary a detailed understanding of the properties of these components. This is especially true of the semiconductor components of the assembly. These are by their very nature sensitive to a disturbance of their properties by slight contaminating influences. In their preparation the semiconductor material is some purified to the highest purity attainable and is then deliberately contaminated. This controlled contamination (doping) introduced during the process of growing a single crystal produces the desired degree of imperfection which determines the electrical properties of the device to be fabricated from the material. The control of these and other imperfections are essential for a good semiconductor device.

In a transistor fabricated from such material, the circuit designer looks for high and stable alpha, low and stable saturation current and high and stable breakdown voltage and other properties sufficient for the application. The device designer knows that the desired stable electrical characteristics can be obtained only by starting with a properly prepared material. For example, the recombination lifetime of the current carriers in the prepared material must be appropriate to the particular device to be fabricated. Recombination lifetime is not fundamentally a material property but varies rather with the mode of preparation (imperfections grown in the crystal and surface imperfections) and the impurity. Even when the device has been prepared from a good stable single-crystal material, the inherent imperfection of the surface, affecting the recombination lifetime, exerts a strong influence on the characteristics of the device.

Assuming a well prepared bulk material, we will be concerned here principally with the stability of the semiconductor surface.

Desired Surface Properties and Their Control

At the surface of the semiconductor device it is desired to have a small surface recombination velocity S and a small surface conductivity G. These are controlled by electrically (or chemically) shifting the surface potential (difference in potential between the bulk interior and the surface) and by forming layers with small numbers of recombination centers. Surface recombination velocity and surface conductivity are inter-related in such a complicated fashion that it appears best to obtain greater experimental confirmation of the theory[1,2] before discussing it. It will be sufficient to say here that the general shape of the conductivity curve as a function of surface potential is a U-shaped curve and the recombination velocity versus surface potential is an inverted U-shape curve. Experimentally the recombination curve (to the extent to which it has been verified to date) is a superposition of several curves of this last described simple inverted U-shape curve. Despite the great complexity of recombination theory required to explain the behavior of the semiconductor, it is possible to observe patterns of behavior that are quite reproducible within a certain range of experimental or ambient conditions. Some of these are illustrated by the experiments to be described following the initial discussion of the surface conditions.

The scope of this paper will be limited to a description of the processing steps which might be used to obtain a good stable semiconductor surface, the surface properties observed, and the technique of measurement. This is followed by experimental data illustrating the behavior observed on a number of samples of n-type germanium with various surface treatments.

Surface Recombination Velocity

The symbol S will be used in the following discussion to denote surface recombination velocity in cm/sec. This is of the same significance as velocity of carrier flow as used to calculate the current density flow in the usual sense where,

$$J = q\,n\,s$$

q = charge on one carrier (1.6×10^{-19} coulombs)

n = number of carriers/cm^3

s = average velocity of carrier flow in cm/sec.

J = resulting density of current flow in amperes/cm^2

For a thin slab of germanium, the carrier lifetime τ ordinarily obtained by observing the decay of a photoconductive current after an instantaneous flash of light is,

$$\frac{1}{\tau} = \frac{1}{\tau_S} + \frac{1}{\tau_B}$$

Usually τ_B, the bulk lifetime is large enough to be neglected in comparison with τ_S, the surface recombination lifetime. The surface recombination velocity[5,6] for a thin slab (with all dimensions large compared to the thickness and with the thickness small compared to the diffusion length constant of the material) is given by,

$$S = x/2\tau$$

where x is the thickness of the slab. Figure 1 shows this relation for the experimental germanium samples, with dotted curves indicating the change for a plus or minus 20 percent change in the 10 mil thickness.

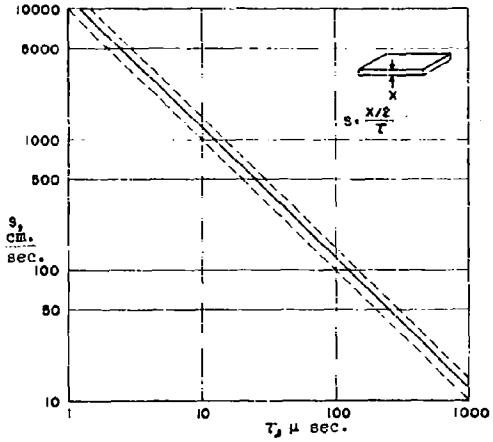

Figure 1. Surface Recombination Velocity S versus Charge Carrier Lifetime τ. (for 10 mil thick slab of semiconductor)

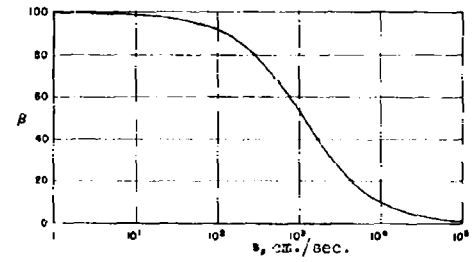

Figure 2. Grounded Emitter Current Gain (β versus Surface Recombination Velocity S. (for assumed conditions β = 50 at S = 1250)

The effect of S, the surface recombination velocity, on the beta or alpha c-b as it is often called, is illustrated for an assumed case in Figure 2. Variations in S up to 200 produce relatively small beta variations. However, a beta drop to 70 percent occurs when S goes to 500.

While the value of S is important, most of the detailed information about the surface is obtained from the field effect[7] experiment.

Field Effect

In this experiment, a small bar (width about 8 x thickness and length about 40 x thickness) of germanium has leads attached to its ends through which a small d-c current is passed. (See Fig.3). Over the surface of the bar, a plate electrode (P) is located as closely as possible but insulated from the bar. An a-c voltage in the frequency range of 50 to 3000 cps connected to the plate electrode causes changes in the conductivity of the surface which appear as a modulation of the d-c current. This conductivity change is observed by means of the oscilloscope as shown in the test circuit in Figure 3. The effect of the capacitance current through the sample is balanced out by an equivalent capacitance C_B and resistor R_B. The curves appearing on the oscilloscope show the change in surface conductivity G versus surface charge (surface potential Y is related to surface charge through the capacitance of the plate P to the surface) due to the field effect. When a minimum appears in this curve, this point is related to the theoretical curve of G versus Y (or G versus

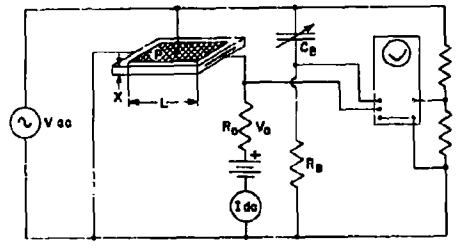

Figure 3. Field Effect Experiment.

surface charge) shown in Figure 4 so that the space charge and the charge in the traps is then known.[7] The theoretical curve of Figure 4 gives the true conductivity of the surface when the effect of traps is negligible. The trap is probably a crystal imperfection which withholds an electron from the conduction band or a hole from the valance band. The experimentally observed curve is wider due to charge held in traps which is not able to contribute to the conductivity of the surface. Hence, the horizontal difference between these two curves (plotted with surface charge as the horizontal coordinate) when the minimum points are coincident will give the charge in the traps. This is the charge in the so-called fast traps. The slow traps are so unresponsive that they only exert a fixed biasing potential which requires seconds to minutes or hours to change. With this

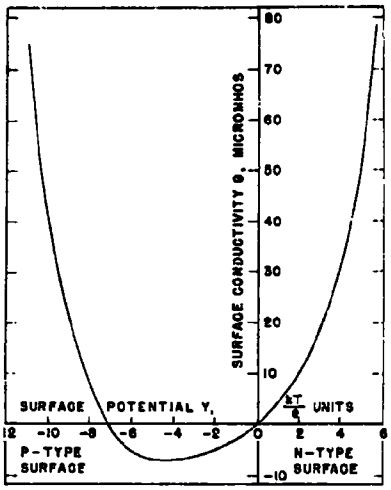

Figure 4. Trap Free Surface Conductivity G versus Surface Potential Y for 8.0 Ohm-Cm N-type Germanium.

information plus the recombination data, the experimental results can be correlated with the theory. Due to complexities mentioned earlier, no attempt at correlation will be made here. The experimental results will be used to monitor surface stability.

Surface Stability

In the field effect experiment the patterns appearing on the oscilloscope (See Figure 5) show clearly the type of surface present on the semiconductor. The type of surface conductivity (either n-type or p-type) is shown by the slope direction of the curve for the surface conductivity, since near the minimum point in the curve a change from n-type, through intrinsic, to a p-type surface is indicated. The untreated semiconductor surface is observed to change from a strong n-type surface to a strongly p-type surface and back again as the gaseous ambient surrounding it is changed from wet nitrogen through dry nitrogen and dry oxygen to ozone and back again. The sensitivity of the semiconductor surface to such an "ambient cycle" is made use of here to test the surface stability. The degree to which the surface is resistant to disturbance by the "ambient cycle" (a similar cycle known as the "Brattain-Bardeen cycle" is referred to frequently in the literature[4]) will be used as a measure of surface stability. Some change is usually observable even with specially treated and coated surfaces. Figure 5 shows the relative tendency of various ambients[3] or chemicals to produce n-type or p-type surfaces and the corresponding patterns observed on the oscilloscope. The patterns are sections of the corresponding surface conductivity curves produced when the semiconductor surface potential (or surface charge) is artificially shifted back and forth by a high voltage (audio frequency of 50 cps to 3000 cps) applied to a small metal plate located close to the semiconductor surface.

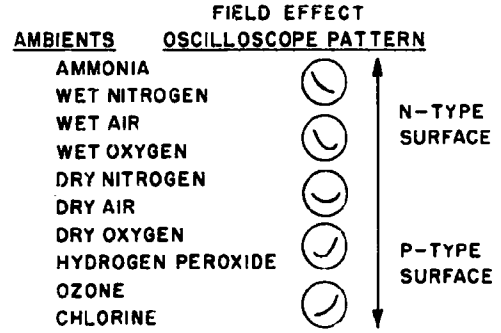

Figure 5. Ambients Arranged According to the Degree of N-type or P-type Surface Produced on Germanium.

The observed pattern is not uniquely related to the ambient since the previous history of the surface leaves a residual effect. The patterns shown in Figure 5 are normal for the nearest group of ambients and change in the direction shown as the ambients shift the surface toward more n-type or p-type conductivity.

Experimental Curves

A photograph of oscilloscope tracings for a piece of untreated 8.0 ohm-cm n-type germanium is shown in Figure 6. Curve a is for a dry oxygen ambient. Curve b showing a strong p-type surface occurs for 10 seconds spark discharge producing ozone in the oxygen. The surface potential drifts back to curve c 3 minutes after the sparking is stopped. Curve d in Figure 7 occurs after 5 minutes in dry nitrogen. Curve e showing a strong n-type surface occurs when the nitrogen is passed through water for 10 seconds. Curve f results 1 minute after returning to dry nitrogen.

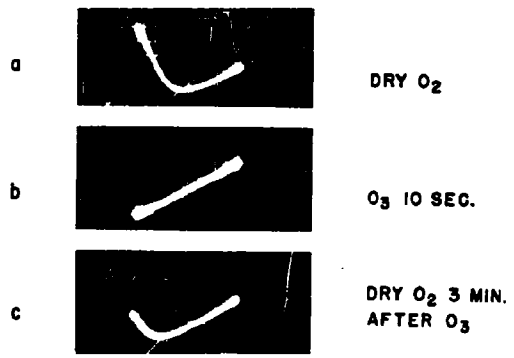

Figure 6. Experimental Surface Conductivity versus Applied Field for Oxygen and Ozone.

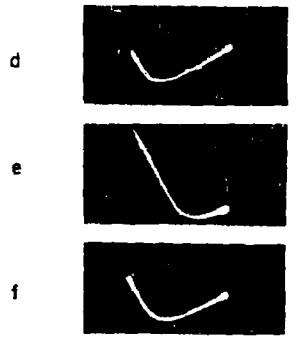

Figure 7. Experimental Surface Conductivity versus Applied Field for Dry and Wet Nitrogen.

This illustrates how readily the ambient atmosphere can shift the surface from strongly p-type to strongly n-type.

Figure 8 shows similar curves on this sample after it has been coated with a silicone resin. The center curve k obtained after 5 minutes exposure to ozone shows only a slight change in the p-type direction compared to a change completely to a p-type surface in 10 seconds when the surface is uncoated.

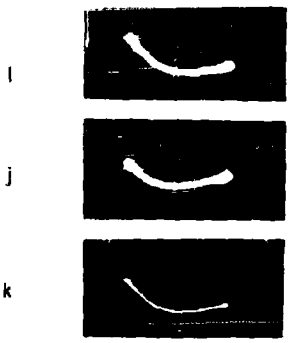

Figure 8. Experimental Surface Conductivity versus Applied Field for a Stabilized Surface Exposed to Oxygen and Ozone.

The surface recombination velocity S is shown in Figure 9 for this sample. After coating and drying it was baked for one hour in room air at 110°C. A change in S from 250 to 320 occurred during the bake. It remained stable in room air for 20 hours, when it was "ambient cycled". A change from 320 to 250 occurred during the 24 hour period immediately following the "ambient cycling", but no further change was noted.

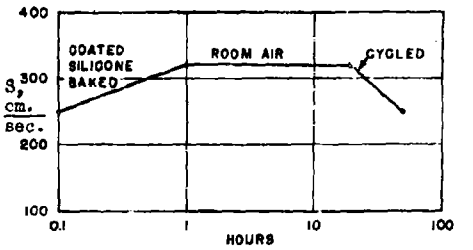

Figure 9. Surface Recombination Velocity S versus Hours Time in Room Air for Silicone Coated N-type Germanium.

Some typical curves illustrating several surface treatments under study at DOFL are shown in Figures 10, 11, 12 and 13.

In Figure 10, a piece of the same 8 ohm-cm n-type germanium which had been cleaned with household cleanser (Ajax) showed an S of 830. Etching in superoxol etch bath (1 part HF, 1 part H_2O_2, 4 parts H_2O) plus a U-P (ultra-pure deionized water) wash reduced the S to the neighborhood of 200. When "ambient cycled" S increased to 420. Cleaning again in household cleanser increased S to 700. A U-P wash reduced S from 700 to 500. Etching again reduced S to 180.

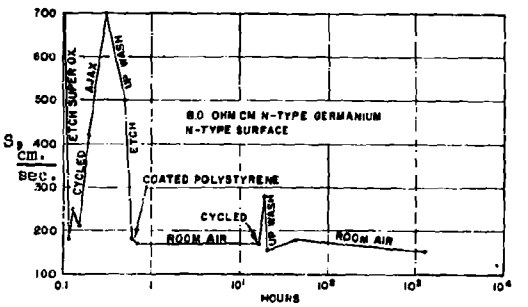

Figure 10. Surface Recombination Velocity S versus Hours Time in Room Air for Polystyrene Coated N-type Germanium.

A coating of polystyrene was then applied. The S decreased to 170 and remained there for 16 hours. On "ambient cycling", the S increased from 170 to 280. A U-P wash reduced S from 280 to 155. Over the next 24 hours, S rose to 180 but was at 155 after 1200 hours in room air.

Germanium pieces #7 and #8 from this same crystal slice (8.0 ohm-cm n-type) were etched, washed and dried. Number 7 was coated with an epoxy and dried. Number 8 remained uncoated. Baking for 1 hour in air at 110°C (See Figure 11)

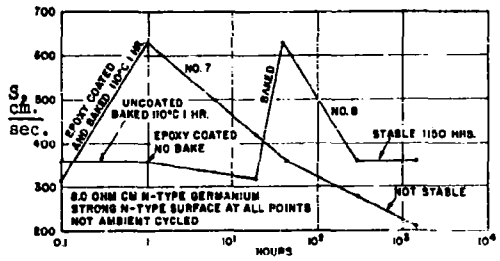

Figure 11. Surface Recombination Velocity S versus Hours Time in Room Air for (7) Epoxy Coated and Baked and (8) Baked, Epoxy Coated, and Baked N-type Germanium.

changed S from 320 to 630 on the coated sample #7 but made no change in the uncoated sample #8. After the bake, the #8 sample was similarly coated and dried. At 18 hours, the S of this sample had decreased from 360 to 320. Four hours later, it had increased from 320 to 410. It was then baked for 1 hour at 110°C when the S increased to 630. In Figure 11, it is seen that #7 shows a continuous improvement over a period of more than 1000 hours. Sample #8 remains at a constant value of S = 360 for over 1000 hours. The value of S near 250 is best for the #7 sample but the stability is best for #8. Apparently, the oxidation due to the initial bake of the uncoated #8 resulted in better stability after coating.

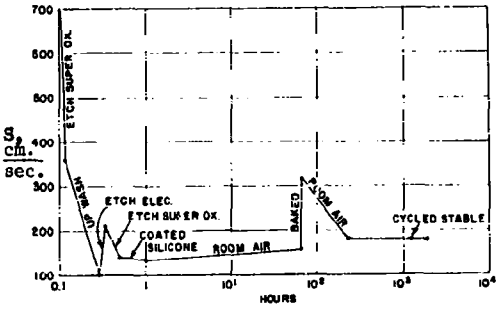

Figure 12. Surface Recombination Velocity S versus Hours Time in Room Air for Silicone Coated N-type Germanium.

Figure 12 for sample #9 shows the S reduced from 1250 to 360 by an etch in superoxol. A U-P wash reduced S from 360 to 100. An electrolytic etch (in 10% KOH) raised S to 210. Another etch in superoxol reduced S to 140. This sample was then coated with a silicone resin and dried. Over a 60 hour period S changed only slightly(140, 135, 155). On baking, S increased from 155 to 315. The S remained constant at 180 for over 1000 hours after the bake. "Ambient cycling" at 1362 hours showed no detrimental effect although ozone shifted the surface from strong n-type to slightly p-type.

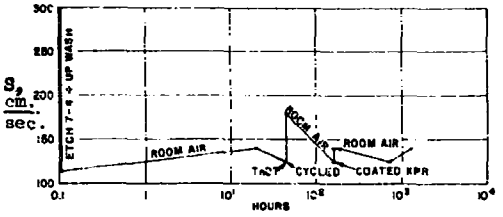

Figure 13. Surface Recombination Velocity S versus Hours Time in Room Air for N-type Germanium Treated with Tn-BT and KPR Coated.

The data of Figures 11 and 12 suggest that a coating of silicone resin is more effective than an epoxy coating in maintaining surface stability. This is not necessarily true since the treatments to which the samples were subjected were not otherwise identical.

Some chemical treatments have been observed to render the germanium surface insensitive to ambient conditions. In the DOFL laboratories, Dr. M. Schwarz found[8] tetra n-butyl titanate (Tn-BT) to restore and in some cases improve the alpha of a group of transistors. Further investigation shows a strong n-type surface of low S and with resistance to "ambient cycling". Figure 13 shows an S change from 125 to 180 due to "ambient cycling" although the surface remained strongly n-type throughout. Some small change occurred also after coating and developing a photo-resist (KPR) layer on the surface. The surface remained substantially stable.

Another chemical treatment observed to improve surface stability involves the methylchlorosilanes.[9] Observations made so far show a surface with stable S and considerable resistance to "ambient cycling".

General Discussion

In the study of semiconductor surfaces a number of general observations and tentative conclusions have been made. Some of these will be listed here.

Many of the germanium etching baths (for example the superoxol etch bath) leave weak n-type or weak p-type surfaces on the semiconductor. These surfaces are easily disturbed by slight traces of stray contaminants. Vapors encountered during removal from the bath, the rinsing, the drying and the room ambients all can easily change such surfaces.

A semiconductor surface remaining stable for hundreds of hours in room air can show a large change due to a few seconds exposure to nearly pure oxygen, a small percent of ozone, a high relative humidity, or a slight amount of chemical vapors.

A semiconductor having a strong n-type surface on an n-type bulk material if "ambient cycled" to a strong p-type surface and back again will usually show a net increase in surface recombination velocity after this cycling.

Strongly n-type or strongly p-type surfaces both can show low surface recombination velocity on either n-type or p-type germanium bulk material; but surface conductivity tends to be high, with resulting surface currents or channels.

A value of recombination velocity should be chosen for the particular device with the surface potential held stable at a compromise value such that surface conductivity and surface recombination velocity are not too high.

A slight oxidation of the semiconductor surface, such as produced by a low temperature bake in air, or merely ageing in air of 50 percent relative humidity plus a coating such as photo-resist, silicone resin, or low catalyst epoxy, improve semiconductor surface stability.

Chemical treatments of the semiconductor surfaces, forming highly stable oxides or silicates directly on the surface, produce stable surfaces resistant to ambient fluctuations.

Conclusions

A combination of chemical treatment plus coating shows promise for producing stable microminiaturized assemblies. In the final stages of fabrication the semiconductor device should be etched, cleaned, and processed to produce the desired surface. This surface should be made resistant to ambient disturbance so that surface properties do not change over the period of normal life expectance and in any of the environments to which it might be exposed. These environments include assembly, testing, potting and encapsulation procedures during microelectronic circuit fabrication as well as the applications environment of the equipment.

The progress made to date gives hope that the early "mystic" approach to the complex chemical properties of the surface are yielding to improved scientific understanding.

Acknowledgement

The germanium crystals used in these experiments were grown in the Diamond Ordnance Fuze Laboratories by Dr. R. Glang and associates. Various chemical procedures have been suggested by Dr. M. Schwarz, Mr. J. R. Nall and Dr. R. Glang.

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EXPLOSIVE TRAINS FOR MINIATURE ELECTRIC INITIATORS

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The use of standard explosive train components now available creates a minimum size barrier below which such components are valueless. In order to reduce the size of a miniature electric initiator explosive train to a level where it would be of value in the miniature components now desired, new explosive devices are required. These devices will require selective sensitivity to be capable of self-propagation in the desired size ranges while maintaining safety, and have enough output to successfully transmit the detonation. The use of 0.040-inch outside diameter low-energy detonating cord together with miniaturized detonators now under development at Picatinny Arsenal will be a major break-through in this direction. A similar development,"string igniter", promises equal miniaturization potential for propellant ignition trains.

Ideally the fuze designer would like to eliminate the explosive portion of his fuze altogether. Since he cannot do this and initiate the main explosive charge of the munition, the next best thing is to make the explosive train as small as possible. Until quite recently, it was believed that the minimum diameter for propagation of tetryl, RDX and PETN in light confinement was 0.125, 0.100 and 0.050 inch, respectively. Miniaturization of explosive trains was considered to have reached a limiting value. Recently, however, there have been some developments that are changing the picture. I will discuss some of these briefly.

The most important break-through in this field was the development of low-energy detonating cord (LEDC)[1] by the joint efforts of the Ensign-Bickford and duPont Companies. LEDC consists of a very small continuous column of explosive in a metal tube. A number of different explosives have been found satisfactory. Core loads in a wide range can be prepared. The metal tube can be reinforced with plastic or textiles to resist abuse. LEDC can be used for a noiseless mainline, for bottom initiation of cap sensitive powders, for short delays, as a propellant igniter, for explosive disconnects, for crimping of metals, for de-icing airplane wings and for conveying detonation through explosives or through mechanical devices with little or no shielding. It has been made in production in loads of .01 grain per foot and experimentally in designs involving a million feet per pound of explosive. The rate of detonation, if PETN is used, is about 6500 meters per second and the value is uniform with 1%.

Although LEDC has some merit as a propellant igniter, a variation known as "string igniter"[2] is much better for this purpose. This is a small diameter continuous metal tubing containing a detonating ignition core composition. It can be supplied in various diameters and its ignition characteristics can be tailored to a specific application. It can be supplied having velocities ranging from 3000 to 6500 meters per second, depending on the type and amount of core composition. The detonation of the explosive disperses radially hot metal particles both from the core and from the metal jacket which have excellent ignition properties. While LEDC requires black powder, or similar material to ignite propellants, "string igniter" can ignite certain propellants directly when slight confinement is provided.

Initiation for both LEDC and "string igniter" can be accomplished by low energy electric initiators. The weakest duPont low-energy electric end primer [2], the X-257D, is 1¼" long, .240" diameter and contains 0.5 grain lead azide. The smallest diameter duPont LEDC electric cap[3] is 17/32" long, .190" diameter and contains 2.0 grains lead azide. There is no reason why designs of this kind cannot be made smaller[4]. Information concerning smaller items will be presented in a paper entitled "Development of Miniature Electric Detonators". Since there undoubtedly are applications where LEDC or "string igniter" could be used if its initiator were of the same diameter, it appears that diameter of initiator is the bottleneck in the development of miniature explosive trains.

The most commonly used explosive in initiators is dextrinated lead azide. This material is required to change the weak impulse from the priming charge into a detonation so that the base charge can be initiated. There are now available other materials which are more efficient, especially in small items, than dextrinated lead azide. Among these are polyvinyl alcohol (PVA) lead azide, developed by the Olin Mathiesen Chemical Co., RD-1333 lead azide, and RD-1343 lead azide, both of which were developed in England. To show the greater efficiency, 85 milligrams of dextrinated lead azide is required for initiation of RDX in the .128" inside diameter M47 detonator, while 25 milligrams of RD-1333 does an equivalent job. This means that detonators can be made shorter to do the same job. The smallest standard Ordnance Corps detonator, the M55, has a diameter of .145" and a length of .140". This represents what can be done in stab-type detonators by use of PVA lead azide. Electric detonators, which have more confinement due to the design of the detonator, should offer even greater possibilities in reduction in length.

Under Contract 537[5] between Diamond Ordnance Fuze Laboratories and the American Cyanamide Co., it was shown that tetryl, RDX and PETN, when mixed with zirconium or titanium, can be initiated by means of a spark gap using 1000 volts and less than 10,000 ergs. Work of a similar nature both with and without primary explosives is underway at Fort Halstead, England, under the Mutual Weapons Development Program and monitored by Picatinny Arsenal. There is definite evidence that insensitive detonators

requiring no primary explosive can be developed and this may lead to smaller explosive trains by elimination of some components or explosives as well as elimination of out-of-line devices.

Work at Picatinny Arsenal during recent years has shown that copper chloretetrazole[6] can be initiated by stab action and can also act as a base charge. Stab-type detonators containing this material are being studied and if the preliminary results are borne out in engineering-type tests, a smaller detonator for the 20mm M505 fuze may become available. It is entirely possible that a miniature electric detonator containing an electrosensitive explosive in combination with copper chlorotetrazole can also be developed.

Another Picatinny study has involved the use of sensitizers[7] with explosives, which could lead to reduction in the number of explosive charges in an item. It was shown that 95/5 PVA lead azide/tetracene loaded in M26 percussion primers will function properly. Although such a mixture will not stand up under adverse storage conditions, it is entirely possible that more stable sensitizers can be found and that they can be used in miniature electric initiators by proper choice of spot charge.

In conclusion, there appear to be numerous methods of reducing the number of explosive charges in initiators and there are devices available which will transmit detonation in very small diameters. Combinations of these devices and emphasis on development of smaller initiators should certainly lead to miniature and even microminiature explosive trains.

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SHIPBOARD GUIDED MISSILE WEAPON SYSTEM SIMULATORS

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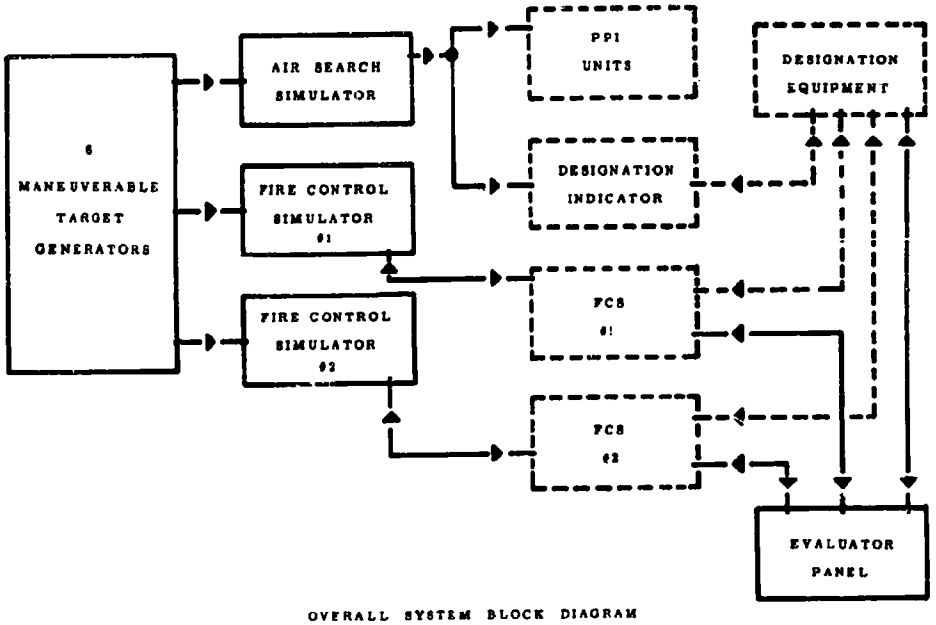
Extensive and complex simulator systems have been developed for training of Armed Forces personnel at shorebased schools in the fields of Fleet Air Defense Weapon Systems and CIC training. With the advent of Shipboard Guided Missile Weapon Systems, a new concept of installing simulator systems aboard Naval vessels has been implemented. Due to the critical need for minimum weight, size and power requirements for shipboard installations, extensive redesign and new techniques have been investigated in the areas of transistorization and micro-miniaturization. This paper will trace the trend in transistorization and assembly miniaturization from shorebased to shipboard weapon system trainers. Circuit, component and assembly package designs will be reviewed in detail.

The U. S. Naval Training Device Center, Office of Naval Research, conducts research, development and production of training equipments in the fields of aeronautics, armaments, electronics, optics, graphics, weapon systems, etc. This paper will discuss the specific area of shorebased and shipboard Guided Missile Weapon Systems as it applies to the Operational Fleet requirements.

The prime function of a Guided Missile Weapon System trainer is to develop and maintain proficiency of the gunnery, missile and CIC teams in the phases of target detection, acquisition, tracking, synthetic firing and assessment of operator and system performance. A typical shorebased type trainer, overall system block diagram as shown in Figure 1, generates six maneuverable air targets which are fed simultaneously to air search and fire control radar simulators. The video output of the air search radar simulator is fed to operational PPI and Designation Indicators. The Fire Control Radar Simulator outputs in turn are fed to the radar equipments of two different



OVERALL SYSTEM BLOCK DIAGRAM

Figure 1

types of Fire Control Systems. Operators of the designation indicators obtain simulated video target data and transmit designated information to the Fire Control Directors to assist the Fire Control radar operators to acquire the targets. The Fire Control Radar system continuously transmits repeat back data to the designation indicators to indicate director position and proceeds to acquire the target in automatic track. Acquisition and tracking phases are completed upon the "locking on" of the target and transmission of target position data to the Gunnery and Missile Computers. The synthetically generated problem is continued to the point of synthetic firing. Assessment of results is made by time measurements of different phases of problem generation, acquisition, tracking, firing and target kill probability determination.

The equipment as described in Figure 1 consisted of 4 major consoles with a total weight of approximately 3,000 pounds. Table I is a chart which shows the relation between operational equipment to be activated and console and weight requirements for both shorebased and shipboard trainer systems.

Based on the above analysis and a review of relative degree of design complexity, it was established that in order to meet the shipboard requirements, an approximate shrinkage in weight and size of 50% would be required. To accomplish this shrinkage, it was agreed with contractor[1] personnel that the following areas would be investigated.

a. Transistorization.
b. Conversion from 60 cycle power to 400 cycle power.
c. New assembly and sub-assembly design concepts.
d. Development of new techniques.

A program was instituted for the complete investigation of the simulator design to achieve a maximum degree of circuit transistorization and miniaturization. Functionally a radar simulator system consists of three basic sub-systems; namely Target Motion Generation, Radar Comparators and Radar Simulators. The detail design of this type simulator is covered in the following paragraphs to clarify the type of engineering techniques employed in simulation equipment, and Figure 2 indi-

SIMULATOR EQUIPMENT	OPERATIONAL SHORE BASED	OPERATIONAL SHIPBOARD
AIR SEARCH	SIMPLE BASIC TYPE	COMPLEX DESIGN
HEIGHT FINDER	NOT REQUIRED	COMPLEX HEMISPHERICAL SEARCH TYPE
FIRE CONTROL OR MISSILE GUIDANCE #1	GUNNERY FIRE CONTROL TYPE	COMPLEX MISSILE ACQ-TRACK SYSTEM
FIRE CONTROL OR MISSILE GUIDANCE #2	GUNNERY FIRE CONTROL TYPE	COMPLEX MISSILE ACQ-TRACK SYSTEM
PERFORMANCE ASSESSMENT	RECORDER UNITS, TIME SEQUENCE EVALUATORS	TIME OF FLIGHT COMPUTER PROBABILITY OF KILL COMPUTER SCORING DEVICE
NUMBER OF CONSOLES AND WEIGHT LIMITATIONS	4 - CONSOLES - NO. LIMITATION ACTUAL WEIGHT 3000#	3 - CONSOLES 3100 - 3200#

COMPARISON OF SHIPBOARD - SHORE-BASED SIMULATOR

TABLE I

cates the type circuit assemblies involved in the transistorization and miniaturization program.

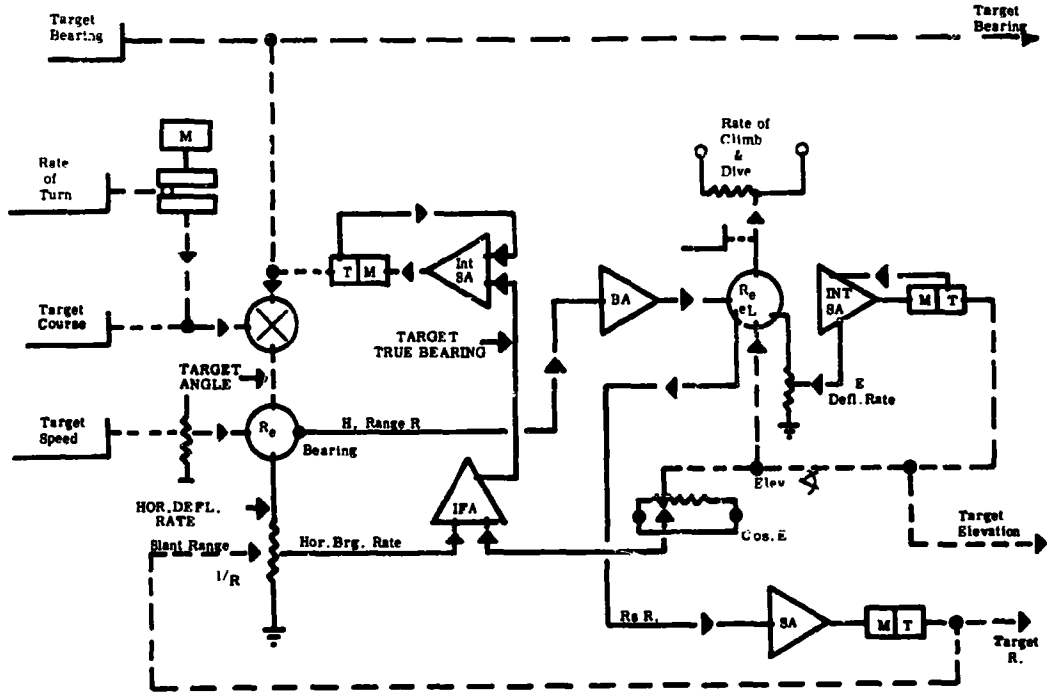
TYPICAL CIRCUIT PACKAGE
Figure 2

The function of a target generator is to generate synthetically the action of a moving target such as an aircraft, submarine or surface craft. Figure 3 is a flow diagram of the functions involved in a typical target generator unit.

Target course is manually set by means of a controllable input. For course changes, a rate of turn unit utilizing a mechanical integrator is provided. The output from the mechanical integrator together with the target course output produces target angle shaft data. This output is compared with true target bearing through a differential to the shaft of the bearing resolver. The insertion of target speed to the bearing resolver will provide an output of horizontal deflection rate. This quantity multiplied by $1/R$ potentiometer will produce horizontal bearing rate. To compute the true target bearing rate, horizontal bearing rate must be multiplied by the secant of the elevation angle. This is accomplished by feeding horizontal bearing rate into an inverse function amplifier, whose feedback is derived from a cosine potentiometer driven by the target elevation servo. The output of the inverse function amplifier is then fed into the true target bearing integrator servo amplifier.

The integrator servo amplifier is often called a rate servo amplifier. In this type of servo, the rate of rotation of the integrator motor shaft is made proportional to the input voltage.

The quantity of horizontal range rate also obtained from the bearing resolver is fed into a booster amplifier whose output drives one stator of the elevation resolver. The other stator of



TARGET POSITION GENERATION CIRCUIT

Figure 3

this resolver is fed from a voltage derived from the target rate of climb and drive control potentiometer. The shaft of this resolver is driven by target elevation angle which can also be a manual input. The resultant outputs of this resolver will be slant range rate and elevation deflection rate.

The elevation deflection rate is multiplied by the $1/R$ function and results in angular elevation rate. This quantity is then fed to the true target integrating servo amplifier whose output shaft is true target elevation angle.

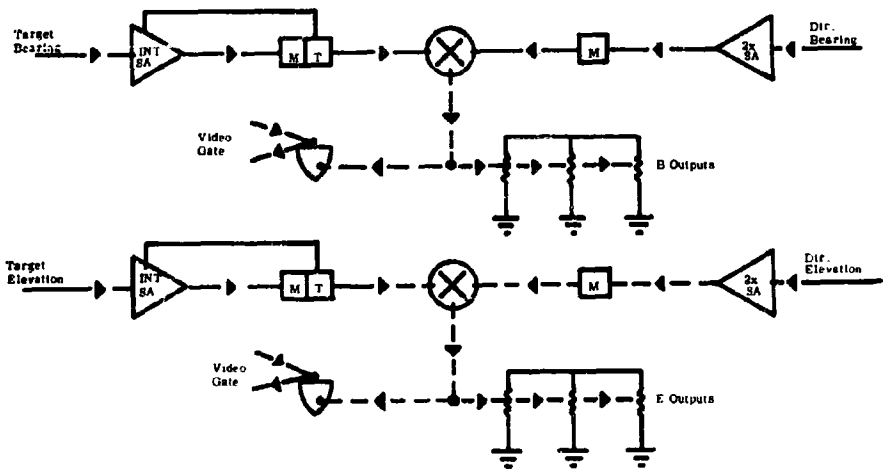
The output of slant range rate is fed to the range integrating servo amplifier whose output shaft is target range.

Thus we see that the prime function of the target generation system is to provide input capabilities of bearing, rate of turn, course, speed and elevation and outputs of target range, bearing and elevation. The next phase to review is the comparator assemblies. The prime function of the comparator units is to match position data of the synthetic target in space with the positional data of the radar antenna and theoretical radar beam characteristics and present signals to the operational radar indicators when they normally would display target information.

The function of the bearing error comparator, Figure 4, is to compare the shaft rotation of the true target bearing obtained from the target generator unit to the shaft of the radar director bearing, through a mechanical differential. The output shaft of the differential is coupled to a three section bearing comparator potentiometer which provides target bearing error electrical signals.

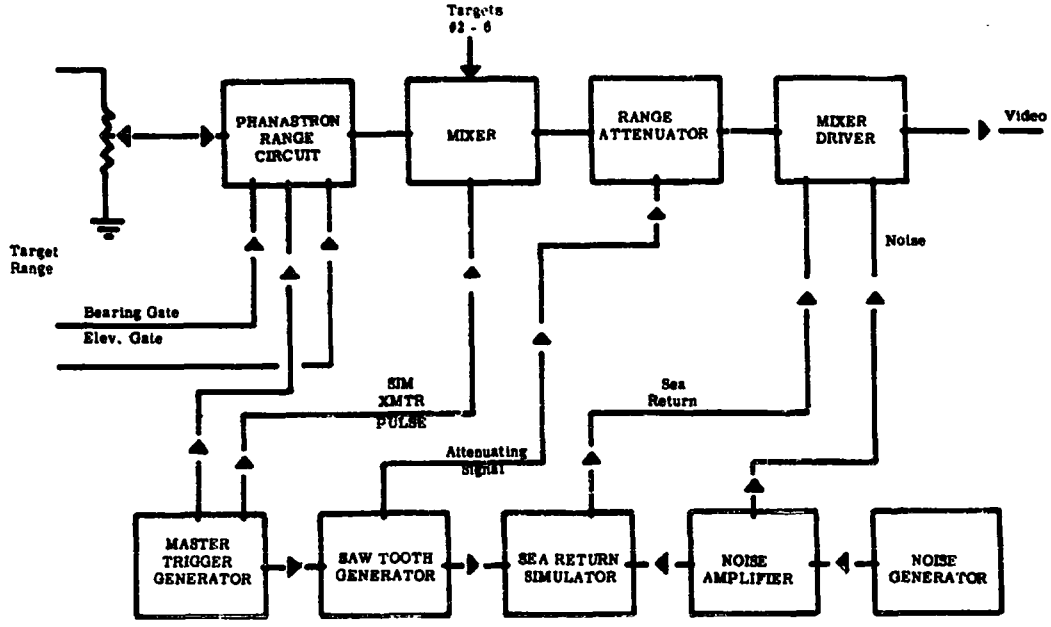
The elevation error comparator unit compares the shaft rotation of the true target elevation (target generator unit) to the shaft rotation of the director elevation through a mechanical differential. The output shaft of the differential is coupled to a three section elevation comparator potentiometer which provides target elevation electrical signals. In addition the video gates as shown are utilized for adjustment of beam width characteristics of radar equipment. The error signal voltages and video clamp (beam characteristic) units are then fed to the radar simulator units where they are converted from voltage signals to appropriate IF and video for display on appropriate indicator units.

The bearing and elevation voltages and gates and target range obtained from the target position generation and comparator assemblies are fed to the radar simulator assembly as shown in Fig. 5



BEARING & ELEVATION COMPARATOR CIRCUITS

Figure 4



RADAR SIMULATOR DIAGRAM

Figure 5

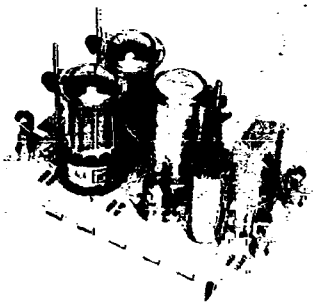
Target range D.C. voltage is fed to the phanastron circuit which is used as a square wave generator. The master trigger is utilized to initiate the phanastron circuit and the level of D.C. range voltage determines cut off time. The result is a positive square wave pulse, whose width is dependent on the range voltage. The square wave is differentiated to obtain the video at the correct range or time displacement from the master trigger. The raw video pulse is fed to the mixer stage where all targets are mixed. Blocking oscillator circuits are utilized to sharpen pulse shapes. The raw targets from the mixer unit are then fed to the range attenuator which decreases signal amplitude with range so as to present typical operational characteristics. Additional features provided to add realism to the presentation are noise and sea return. The output video is then presented to operational indicators.

Summarizing the characteristics of the overall Radar Simulator systems just reviewed establishes that the following assemblies and circuits are capable of transistorization and miniaturization:

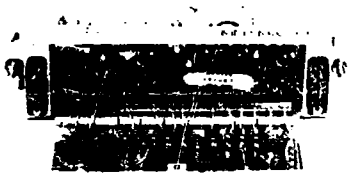
1. Target Motion Generators - Servo, booster, inverse function, isolation, unit gain amplifiers, electro mechanical assemblies, motors and power supplies.
2. Radar Comparators - Same as target motion generators.
3. Radar Simulators - Electronic circuits such as phanastron, differentiators, sweep, blocking oscillators, noise and sea return generators, multivibrators, etc.

Figures 6 - 8 are photographs of type construction design utilized prior to transistorization. The units utilized miniature tubes, 60 cycle power source and ± 300 V. D.C. regulated power units as shown in Figures 9 and 10. Dimensions are as shown in the above figures and weight varied from 2 pounds to 3½ pounds dependent upon size. In transistorization of these units, molded card type and tube type assemblies were utilized as shown in Figures 11 and 12. The size of the units are as shown in the above figures and weight is approximately 6 to 8 ounces. As a majority of the circuits described in Figures 3 - 5 were transistorized, extensive decreasing in weight and size was realized. In the shipboard type trainer, the tubular type transistorized assemblies are used extensively as compared to the molded card type. The advantages lie in greater maintainability and replacement. The disadvantages are larger size and weight. Since the units have to be capable of replacement, it was agreed that the use of the tubular transistorized type is preferred. When one considers that approximately 50 - 60 of these type circuits are utilized, the size is quite appreciable. In addition, the console and chassis assembly are decreased in size.

TARGET MIXER ASSEMBLY - TOP VIEW
Figure 6



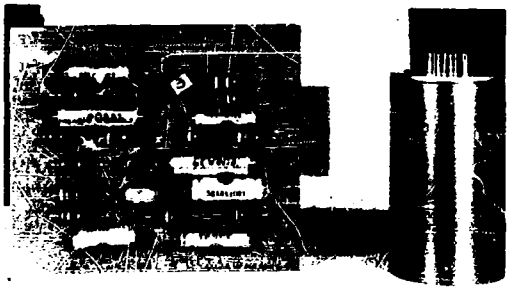
300 V DC POWER SUPPLY - TOP VIEW
Figure 9



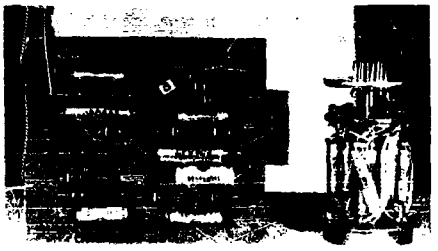
TARGET MIXER ASSEMBLY - OPEN SIDE VIEW
Figure 7

300 V DC POWER SUPPLY - OPEN SIDE VIEW
Figure 10

RADAR SIMULATOR CHASSIS
Figure 8

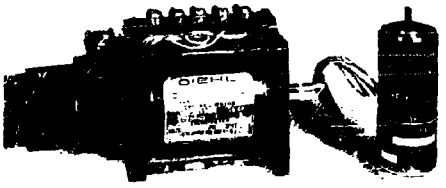


SIDE VIEW OF TRANSISTORIZED ASSEMBLIES
Figure 11



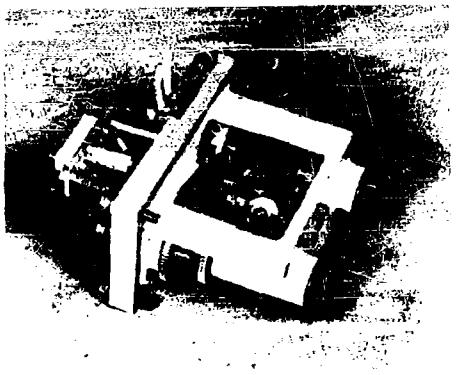
TRANSISTORIZED ASSEMBLIES - CASE REMOVED
Figure 12

Another obvious shrinkage was obtained in converting the system from a 60 cycle power system to a 400 cycle system. The major weight saving was in transformers, filters and motor assemblies. Figure 13 shows a comparison of a 60 cycle and a 400 cycle servo motor. The weight and size shrinkage ratio was approximately 4:1.

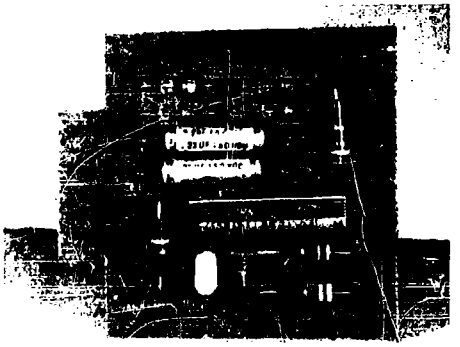


COMPARISON OF 400 CYCLE & 60 CYCLE COMPONENTS
Figure 13

Another area of miniaturization was the careful investigation of design techniques utilized and possible use of other techniques. Figure 14 shows the electro-mechanical assembly which is utilized as the bearing gate simulator described in Figure 4. After careful study, a design technique utilizing target input to the rotor of a control transformer and antenna position data fed to the stator leads was developed. The error signal was fed to a D.C. level comparator circuit as shown in Figure 15. Bearing width is readily adjustable by changing the D.C. level. The weight and shrinkage ratio gained was approximately 10:1.



BEARING GATE COMPARATOR CIRCUIT - MECHANICAL
Figure 14

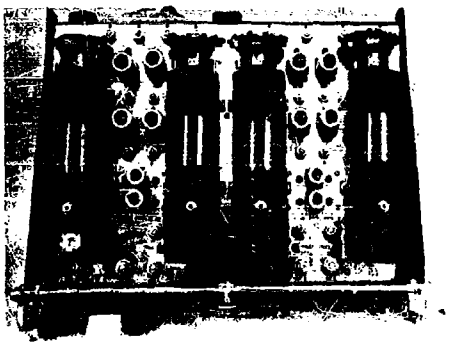


BEARING GATE COMPARATOR CIRCUIT - ELECTRONIC
Figure 15

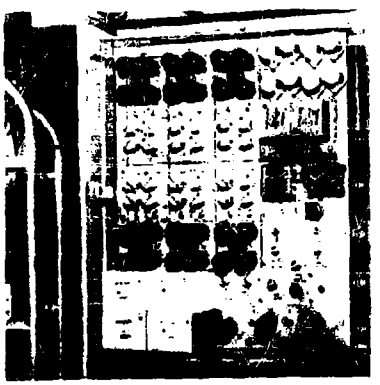
Another typical example of circuit redesign was the replacement of CRT tubes and associated circuits utilized for simulation of complex conical and spiral scan simulation of fire control simulators with ring modulators. Figure 16 shows a 4 target conical spiral simulator chassis utilizing CRT as compared to Figure 17 which is a six target chassis utilizing ring modulators. Size and shrinkage accomplished was approximately 3:1.

Another extensive saving in weight and size is realized in power supply units utilized with transistors. Regulated power supply units as shown in Figure 9 were decreased in voltage and current

requirements. Power supply shrinkage ratio varied from 5:1 to as high as 10:1. A complete analysis of the simulator system showed that approximately 80 - 85% of the circuits involved in this type design are capable of transistorization.



CRT TYPE CONICAL SPIRAL SIMULATOR
Figure 16



RING MODULATOR TYPE CONICAL SPIRAL SIMULATOR
Figure 17

In summary it can be stated that shrinkage of 50% was accomplished by use of the following rules which were discussed previously, namely as follows:

a. Complete analysis of circuit design. Transistorize only when warranted and conforms with good design practices. In some specific cases it was found that conventional miniature tubes were better suited and provide the most efficient design.

b. Use 400 cycle supply in lieu of 60 cycle whenever possible.

c. Investigate alternate design techniques when possible and warrented. It must be realized, gentlemen, that transistorization and miniaturization are not the panacea for all design problems. Its application is usually expensive and time consuming. However when the ultimate requirement is a maximum shrinkage of size and weight, these factors can be realized using the above analytical approach without the sacrificing of good design practices and equipment reliability and maintainability.

1 Belock Instrument Corporation, College Point, is prime contractor of shorebased and shipboard simulators.

MINIATURE MICROWAVE MAGNETRONS

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ABSTRACT: Miniature microwave magnetrons developed under Signal Corps sponsorship are described. These tubes are capable of operating under conditions of extreme shock, vibration, and constant acceleration. Mechanical and electrical operating characteristics are given; limitations in the use of these miniature magnetrons and operating restrictions on equipments utilizing the tubes are discussed. Finally, the outlook for the future in the field of ruggedized miniature microwave magnetrons is presented.

Introduction

For many years the magnetron has been recognized as a highly efficient generator of microwave energy. In the past the majority of tube uses have required the relatively high output powers produced by the magnetron. Recently, with the advent of complex electronic airborne systems such as radar beacons, the magnetron, because of its structural simplicity and high efficiency, has gained additional importance. In this paper I shall describe several magnetrons which were designed for applications requiring tubes of minimum size and weight, maximum efficiency, and extremely rugged construction. The tubes discussed were developed under Signal Corps sponsorship, and are presently being used in a number of experimental systems.

Description

Miniature magnetrons, like standard-size magnetrons, can be divided into two types, the pulsed and the cw. At present, because most systems use the pulsed magnetron, many more tubes of this type have been developed.

Pulsed Magnetrons

The general configuration of a pulsed magnetron can be seen in Figure 1. A tube of this type generally has a cylindrical geometry with no radial protrusions, thus making it ideally suitable for use with cylindrical modules.

The pulsed magnetrons to be described are the BL-211 and the BL-212, manufactured by Bomac Laboratories, and the YK-362A and the YK-530, manufactured by the Raytheon Manufacturing Company.

The BL-211 and BL-212 magnetrons are electrically and mechanically similar, both tubes having the same external configuration and the same size and weight. The essential difference between the two is one of fabrication technique. Closer controls during production of the BL-211 and slightly different assembly procedures allow this tube to withstand more severe environmental conditions than the BL-212.

The YK-362 and YK-530 tubes are similar electrically, but differ mechanically. Besides being slightly larger and heavier than the YK-362, the YK-530 employs a more rugged tuner, which assures operation at a relatively constant frequency under extreme environmental conditions.

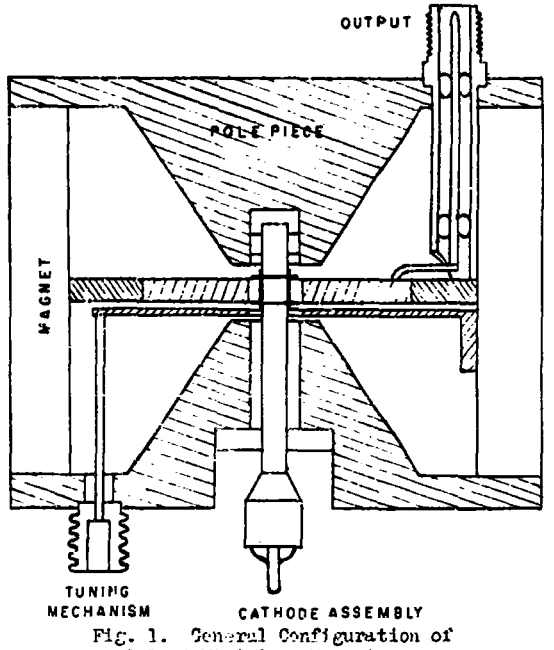

Fig. 1. General Configuration of Pulsed Miniature Magnetrons

The most significant characteristics of these tubes are shown in the following table:

TABLE I
Significant Characteristics of Pulsed Beacon Magnetrons

Characteristic	YK-362A	YK-530	BL-211	BL-212
Frequency (Mc)	9300-9500	9300-9500	5400-5900	5400-5900
Peak Power Output (kw-Min.)	60	60	100	100
Life (Hrs-Min.)	250	250	250	250
Weight (Oz-Approx.)	4	5	6	6
Size (In.)				
Length	2.00	2.50	3.25	3.25
Diameter	1.25	1.25	1.25	1.25

Pulsed beacon magnetrons operate, in general, at a peak voltage of from 1.2 to 1.5 kilovolts with pulse durations of 0.25 to 1.0 microseconds at repetition rates ranging from 100 to 4000 pulses per second.

The BL-211 and the QK-530 tubes can be considered companion tubes, since they are both designed to operate in the same types of equipment. The major differences between the two are their physical construction and frequency coverage. The tubes are shown in Figures 2 and 3.

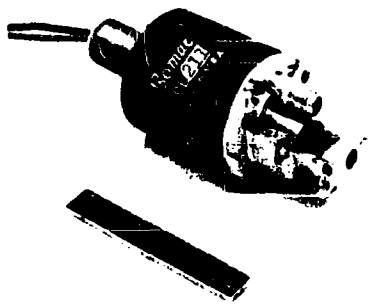

Fig. 2. BL-211 Miniature Beacon Magnetron

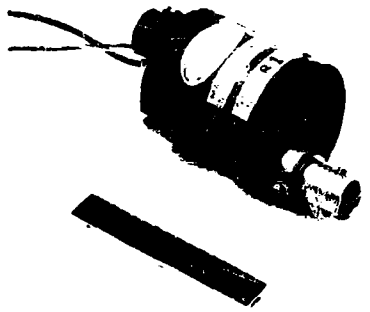

Fig. 3. QK-530 Miniature Beacon Magnetron

Both tubes have been evaluated thoroughly by engineers at the Army Signal Research and Development Laboratory at Fort Monmouth, and are capable of operating under conditions of extreme shock, vibration, and constant acceleration.

One test used to evaluate the ability of these magnetrons to withstand extreme shocks was the following: The tubes were placed in a cylindrical package within an artillery shell, and the shell fired vertically. The tubes successfully withstood accelerations between 12,000 and 13,000 g. The tubes have also survived centrifuge tests where the applied acceleration was in the order of 20,000 g, and have operated satisfactorily when subjected to vibrations at a 30-g level from 50 to 2000 cycles per second. In addition, they also passed all tests simulating the environmental conditions to which they will be subjected when in actual use.

Like the BL-211 and the QK-530, the BL-212 and the QK-362A can also be considered companion tubes with the same differences (physical construction and frequency coverage). These tubes have also been thoroughly evaluated at USASRDL, and are capable of performing satisfactorily when subjected to vibrations of from 55 to 2000 cycles per second at a constant acceleration of 12 g. When centrifuged, the tubes are capable of withstanding 100 g in a plane parallel to the axis of the tube.

CW Magnetrons

In general, cw magnetrons are not voltage tunable; that is, the output frequency is essentially independent of the cathode-to-anode voltage. However, in this paper we shall describe a unique tube, the Z5299 voltage-tunable magnetron, developed by the General Electric Company. The tube utilizes an all-ceramic and metal sandwich, allowing operation in temperatures of 200°C without cooling. (The tube could probably withstand much higher temperatures.) The ceramic sandwich construction provides a very rugged tube. Unfortunately, the environmental capabilities of this tube have not yet been thoroughly evaluated, although the standard tube vibration tests have been made with satisfactory results. The tube and an experimental package are shown in Figure 4.

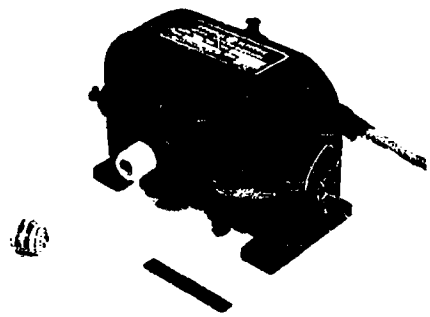

Fig. 4. Z5299 Voltage-Tunable Magnetron and Experimental 5283 Package

Unlike the pulsed magnetrons previously discussed, the voltage-tunable magnetron does not contain the microwave circuit and magnet, but instead utilizes a microwave circuit which is external to the vacuum envelope. The method of operation and the application determine the size

of the microwave circuit. In some applications the total package size could probably be reduced to that of a baseball.

Significant characteristics of the Z5283 voltage-tunable package are given in the following table:

TABLE II
Significant Characteristics of
Z5283 Voltage-Tunable Magnetron Package

Frequency	2200-3850 mc
Peak Power Output	1 W (Min.)
Life	250 Hrs (Min.)
Weight	5 Lbs (Approx.) 0.3 Oz.*
Size	
Length	5 In. 0.66 In.*
Height	4 In.
Depth	3.50 In.
Diameter*	0.71 In.

*Tube Only

From the data in the above table it can be seen that the output frequency is a function of the applied cathode-to-anode voltage; in fact, the frequency actually approximates a linear function of the applied voltage. In applications requiring a frequency-modulated microwave source, the voltage-tunable magnetron can be used to great advantage.

Operating Limitations

There are certain restrictions in the manner in which miniature microwave magnetrons may be used.

In order to avoid operating instabilities, the load to which a miniature [illegible] should be as well matched [illegible] not exceed a VSWR of 1.5:1. [illegible] isolator should be used [illegible]

Because the shape of the [illegible] to the miniature pulsed magne[illegible] critical, the rise time of [illegible] very much the same as that [illegible] netrons (approximately 0.15 [illegible] top portion of the pulse should [illegible] possible. While this requirement [illegible] larger magnetrons, it is even [illegible] miniature tubes since the cath[illegible] their small size, must operate [illegible] ture-limited emission region; [illegible] cant advantage of the miniature [illegible] pulsed voltage can be applied [illegible] impossible in standard magnetrons [illegible] higher operating voltages.

In standard magnetron types [illegible] ble, and in fact necessary, [illegible] voltage during operation and [illegible] bombardment to supply the power [illegible] ode. However, we cannot rely on [illegible] in miniature tubes because of [illegible] and because of the variation in [illegible] rates during operation.

Since the mass of the permanent [illegible] devices is relatively small, [illegible] easily reduced to the point where [illegible] to operate the tube. Therefore, [illegible] that all magnetic materials be [illegible] possible from the tube while it [illegible] or operated.

Future Trends

It is foreseen that with the [illegible] efficient magnet and cathode [illegible] ceramics, great strides will be [illegible] of miniature microwave magnetrons [illegible] that magnetrons of this type will [illegible] with higher frequencies, output [illegible] ciency. Improved construction [illegible] under study will also make possible [illegible] rugged" magnetron.

★U. S. GOVERNMENT PRINTING OF