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Nanostructure effects in Si-MOSFETs

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Abstract. In this article we present a summary of the most important critical issues in nano-scaled field-effect transistors. The controversial issue of alloy scattering and the phenomenon of velocity overshoot which are important in the nano-scale regime are reviewed and discussed. The emerging $Si_{1-x}Ge_x$ technology contribution to improve scaled Si MOSFETs is presented. Achievements and problems associated with channel engineering and alternative gate electrodes and high-κ dielectric materials are also addressed. Finally, during the presentation we will discuss our results on filtering out hot carriers using channel engineering. We will also discuss our results on scaling down the MOS transistor to a single electron tunneling MOS transistor made in Si and with properties like room temperature Coloumb oscillations.

1. Introduction

The relentless scaling of Si MOSFET devices, which has offered outstanding improvement in performance seems to have reached an end. The gate oxide thickness is now in the direct tunneling regime <3 nm, which calls for other materials with higher dielectric constant to replace SiO_2, the substrate doping concentration $\sim 1 \times 10^{18}$ cm^{-3} is also in the limit of source/drain-substrate p-n junction leakage current. Control of doping concentration and doping profile for source/drain still poses a challenge. Shallow S/D extensions alone is not enough; the surface impurity concentration should be as high as to achieve the desired improvement in the overall device characteristics. When low doping concentration is used, ultra shallow junctions can be achieved but this degrades the current drivability. In the nanometer regime, special techniques have been adopted to fabricate 40-nm gate length n-MOSFET with 10 nm depth source/drain junctions [1].

For a 14-nm gate length transistor, two gates separated by thick SiO_2 were used with the upper gate requiring 7 V to form the channel [2]. It is well known that, in such a regime, MOSFET devices suffer from significant fluctuations in the threshold voltage and in the output characteristics together with other various issues [3]. In order to suppress such effects and to explore the ultimate CMOS limit of about 25-nm gate length, a double-gate MOSFET device structure, is proposed and demonstrated experimentally [4]. However, the fabrication of such devices is by no means simple and requires more stringent methods; both gates have to be self-aligned to the source and drain. On the other hand, though it appears now that conventional Si technology is hard to beat, the emerging SiGe technology is expected to boost the performance of Si-based devices beyond that of Si. At least the Ge material, due to its favorable electrical properties, would probably be in every Si chip in future generations [5–9]. The $Si_{1-x}Ge_x$ alloys started to attract researchers' attention since more than sixty years ago [10]. Numerous scientific research papers are published where different $Si_{1-x}Ge_x$ alloy based devices were demonstrated and studied, see e.g. [11–21] and references there in.

2. Transport issues

2.1. Velocity overshoot

When the channel length of the MOSFET device is scaled down to 100 nm and below, the carrier transport along the channel can be considered as quasi-ballistic transport and, depending on the scattering events in the channel, the effect of velocity overshoot can be observed. For conventional Si MOSFETs, the overshoot phenomenon has been predicted theoretically in the 70s [22, 23] and observed experimentally in the mid 80s at different temperatures, namely 300 K, 77 K and 4.2 K [24, 25]. Velocity overshoot is important for increasing the transconductance and thus the speed of the device.

For strained Si or strained SiGe MOSFET devices, investigation of velocity overshoot has so far been mostly theoretical calculations and computer simulations. These simulations, though some of them approximate, provide useful information and predict the anticipated trend of carrier transport in the velocity overshoot regime [26–28]. Velocity overshoot has been predicted to occur closer to the source end and more pronounced in strained Si and strained SiGe channel MOSFETs than in conventional Si devices [26].

2.2. Alloy scattering

The significance of alloy scattering in the $Si_{1-x}Ge_x$ material system still remains a subject of debate. This controversy has both experimental and theoretical grounds. First of all it is important to have a well-defined theoretical formulation to evaluate the alloy scattering potential U_{al} because being a fitting parameter appears to be the origin of the debate. Different researchers chose different values and the spread of these values is large, e.g., $U_{al} = 0.2$ eV [29], 0.27 eV [30], 0.3 eV [31], 0.6 eV [32–34], 0.9 eV [35], and 2.0 eV [36]. It is worth mentioning that the value of 0.3 eV used in [31] is equivalent to that of 0.6 eV quoted in [32] and [33] and the factor of 2 is due to a difference in the volume of the primitive cell. The alloy scattering rate is known to be proportional to $x(1-x)(U_{al})^2$, where x is an alloy concentration. Therefore, one would expect that the contribution of alloy scattering is maximum at $x = 0.5$ and could be underestimated for small values of U_{al} or overestimated for larger values.

If we assume that alloy scattering is the only dominant mechanism at low temperatures then it would be easy to obtain a good estimate for the alloy potential and the case is reversed if any other scattering mechanism such as interface roughness and/or interface impurities is present. Recalling the dependence of the alloy scattering rate on the alloy concentration given above, it is experimentally observed that a strained $Si_{0.7}Ge_{0.3}$ grown on Si at 500 °C showed a significantly lower mobility due to interface roughness compared to the case when grown at 450 °C [37]. Also they obtained a higher mobility in $Si_{0.5}Ge_{0.5}$ strained layers on Si, which may rule out the significance of alloy scattering, in contrast to recent claims.

Beside the difficulty in extracting the alloy potential, in the presence of other scattering mechanisms, by fitting theoretical calculations to experimental data, experiment is normally for Hall mobility μ_H, which is related to the drift mobility μ_d via the relation $\mu_d = \mu_H/r_H$. The Hall factor r_H is a complicated function of the magnetic field and the scattering mechanism in the structures. Note that in thin quantum wells or inversion layers, typically less than 10 nm thick, the carriers can be considered as a two-dimensional hole/electron gas and quantum Hall effects can be observed [38]. Although the Hall factor r_H can, generally, have values between 1–2, it has also been observed experimentally to have values much lower than 1, depending on the Ge content and the doping concentration [39].

3. Channel engineering issues

The low mobility results in a low transconductance and hence the need for a wider PMOSFET transistor. Early suggestion of using $Si_{1-x}Ge_x$ technology in field effect devices was implemented during the 80s [40]. This pioneering work where a silicide Schottky gate was used in a MODFET structure was not successful due to the large leakage current at temperatures higher than liquid nitrogen. The use of buried strained- $Si_{1-x}Ge_x$ in a MOS structure as the main conducting channel was then left as the best alternative provided that strong inversion in the buried channel occurs before that in the surface low mobility Si channel [41, 42]. Beside being a solution to overcome the low hole mobility, the valence band alignment in the $Si/Si_{1-x}Ge_x$ heterojunction creates a quantum well (QW) channel that offers confinement away from the Si/SiO_2 interface [43]. The use of a single $Si/Si_{1-x}Ge_x$ QW for the PMOS transistors, although resulted in performance improvement, has still not offered the expected gain.

Improvement of the single QW PMOSFET performance can be achieved by using a modulation doped heterostructure. Here a single or double delta-doped layer is inserted either above and/or below the QW channel. Very high record hole mobility in excess of $19.000\,cm^2/V\,s$ at 7 K was reported for a single modulation doped QW structure [44]. A similar study intended to compare normal and inverted modulation doped QW structures showed that the mobility is higher for a normal modulation doped QW when compared to an inverted structure having the same inner physical parameters [45]. On the other hand, double modulation doped QW structure is expected to be advantageous for conductivity due to the confinement at both edges of the QW however, the result of Hall mobilities indicates a reduced mobility when compared to single modulation-doped structures [46]. The preceding discussion indicates that the design of the QW plays an important role in the performance of the PMOS QW based transistor. Theoretical investigation of the confined carrier concentrations in single QW $Si/Si_{1-x}Ge_x$ PMOSFET has indicated that at strong inversion most of the carriers accumulate at the heterointerface [47]. This accumulation is expected to be one of the most limiting factors in degrading the mobility. There have been many reports that dealt with different Ge profile in the QW, these include trapezoidal [48], and different triangular Ge profiles [49, 50]. Here, grading the Ge profile is advantageous in creating a wide QW. Carrier concentration investigation indicates that the carrier concentration is following the high Ge grading profile. Most recently, adding to the existing different QW based PMOSFET, we have proposed and investigated the feasibility of different designs of a double retrograde $Si/Si_{1-x}Ge_x$ QW structures [51–53].

Figure 1 shows the calculated valence band profile and the hole distribution. As it is clear, and in contrast to other single QW profiles, the peak of the carriers lies at the center of the main conducting channel. It is important to mention that recent studies indicates that interface roughness might be more dominating than other scattering mechanisms that contributes to mobility degradation [33]. Note that high quality interface will reduce the low-frequency noise and this is particularly important for microwave applications [54]. The retrograde structure also offers more engineering possibilities for further performance improvement. For example, the cap layer can be made ultrathin (1 nm or less) to suppress its inversion and keep the rather good quality of SiO_2/Si interface.

Figure 2 shows the reduction trends in the threshold voltage as the channel length is reduced. The drain-induced barrier lowering (DIBL) at a channel length of about 0.217 μm is only 77 mV/V for 2.5 V operation, indicating a potentially acceptable short-channel behavior for this retrograde DQW device. In addition, for this structure, it should come as no surprise that hot-carrier degradation and loss of the inversion charge in the nanometer-

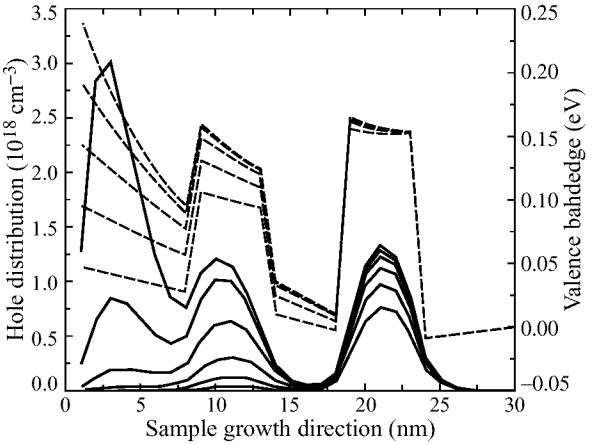

Fig. 1. Calculated valence band profile (dotted lines) and the 2D hole distribution profile (solid lines) along the sample growth direction as a function of gate voltage for the retrograde DQW structure.

scale devices will be improved because carriers have to travel longer distances to reach oxide interface.

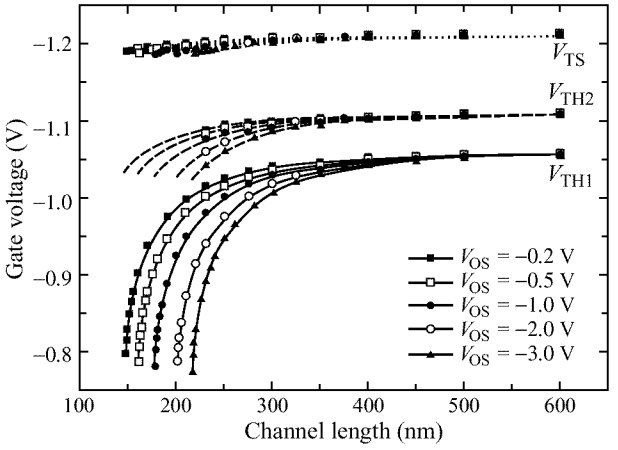

Fig. 2. The threshold voltage dependence on the channel length and drain voltage for the SiGe retrograde DQW shown in Fig. 2, but with a cap of 2 nm.

For engineering the channel for better electron confinement, a tensile strained Si is used as the main conducting channel. This is beneficial over the QW PMOS in the fact that alloy scattering effect is minimal. However, the growth of tensile strained Si is technologically not easy. The growth of relaxed $Si_{1-x}Ge_x$ virtual substrates for the growth of tensile strained Si is of global interest nowadays. These virtual substrates must contain low density of threading dislocations to be accepted electrically. There has been mainly three contending routes to engineer the growth of relaxed $Si_{1-x}Ge_x$ or relaxed pure Ge virtual substrates; (i) post processing of strained $Si_{1-x}Ge_x$ [55], (ii) use of an intermediate strain relieving compositionally linear and/or stepwise $Si_{1-x}Ge_x$ graded buffer layer [56, 57] and (iii) direct Ge epitaxy or surface mediated growth [58, 59]. Both Molecular Beam Epitaxy (MBE) and

different Chemical Vapor Expitaxial reactors have been used for the hetero-epitaxy of these virtual substrates. Recently, chemical mechanical polishing at intermediate growth levels is introduced to achieve higher surface quality and has shown remarkable improvement of the final relaxed Ge virtual substrate layer [60]. Although with today's technology, relatively thin very high quality 100% relaxed Ge buffer layers containing low threading dislocation densities have been achieved, still more research needs to be carried out in order to improve the surface morphology, which suffers roughness and undulations [61]. Finally, we will present new results from extraction of hot carriers in the channel. The hot carriers are filtered drown to the substrate by different engineering techniques [82, 83]. The goal of this technique is to reduce power consumption in CMOS circuits by using the heat generated from the carrier relaxation, to charge up the battery. The influence of this technique on circuit properties will also be discussed [84].

Examples of alternative metal gate electrodes are: damascene metals W/TiN or Al/TiN, Copper, Cu [67] and Tantalum, Ta [68]. Such metal gates can indeed be used to eliminate gate depletion. This, however, yields a buried-channel device, which suffers from more short-channel effects than the surface-channel device, but with better channel mobility [69].

One of the promising candidates among gate materials that is completely compatible with standard CMOS processing and suitable in dual N^+/P^+ gate technology is the p-type poly-$Si_{1-x}Ge_x$ gate [70–72]. This material has been shown to benefit from improved resistivity, tunable work function, and reduced gate depletion and boron penetration, compared to P^+ poly-Si [73–75]. The tunable work function of the poly-SiGe gate can be used to adjust the threshold voltage, while engineering the channel profile can be used to control short channel effects [76]. Figure 3 shows the dependence of the gate work function on the Ge content. It is worth mentioning here that the feasibility of a pure Ge ($x = 1$) gate has also been studied within an industrial 0.18-μm CMOS process with well controlled short-channel effects and reduced gate depletion [77].

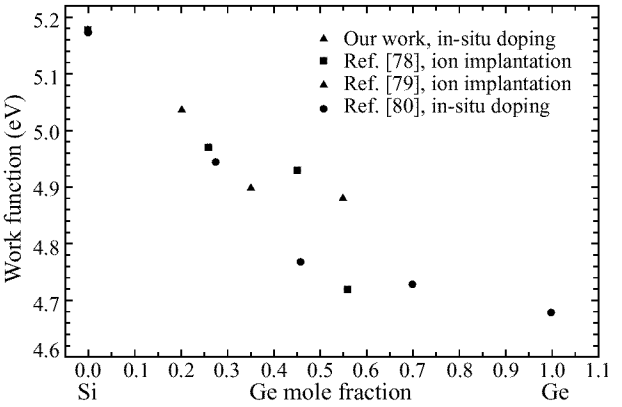

Fig. 3. The work function of B-doped P^+ poly-SiGe gate material as a function of Ge content.

4. New concept: The single electron transistor

The physical scaling consequences mentioned above, in addition to the power dissipation problem in a giga bite scale integrated Si chip have lead to the need of new engineered devices. The single electron transistor (SET) which uses the Coulomb blockade oscillation

was suggested as a possible candidate [81]. Randomly arranged metal islands were used when single electron transistor phenomena was first discovered in 1951 [85]. The first SET, where the number of electrons could be controlled by an external gate was demonstrated in 1987 [86]. However an isolated metal island has to be less than 5 nm in size to output a room to temperature Coulomb blockade oscillations. Silicon nano-crystals have shown to provide room temperature operation of the SET. Semiconductor SETs were first demonstrated in 1989 [87, 88]. During the talk we will present our results on e.g. room temperature Coloumb oscillations in Si based SETs [89, 90].

5. Conclusions and future perspectives

The general trend in most of today's Si-based MOSFETs research is to introduce new exotic methods to suit, in part, metal and/or mid-gap gate materials, high-κ dielectrics, and double gate technology, in order to explore the ultimate limit of these devices. Although this may offer an improved performance for some time, it also poses more processing complications. Without such complexities, the chance for the emerging SiGe technology to be in the main stream and to boost Si-based devices would be greater than ever in the very near future. Even, if we are to resort to low-temperature CMOS technology, where the performance is better by a factor of about two, the chance would still be bigger for SiGe. However, some more research is to be carried out for both n- and p-channel SiGe based MOSFETs. For the p-channel devices, more experimental work in the appealing issue of optimized carrier confinement is needed and a more accurate systematic study for the parameters of alloy and deformation potentials is indispensable. In addition, virtual substrate morphology and surface properties for the n-channel devices need to be improved.

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