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VGS Compensation Source Follower for the LTPS TFT LCD Data Driver Output Buffer

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ABSTRACT

Low Temperature Poly-Silicon (LTPS) TFT technology for LCD has been developed for a long time. Because of its higher mobility, scan driver and data driver could be fabricated on the glass panel to form a fully integrated display panel and reduce its cost. In this paper, new circuits for buffering the DAC in the data driver will be proposed. These circuits have the advantages of lower power and smaller area than the conventional ones. They all extend their full swing from 2 to 10 volts in 12 μ s and have 6-bit resolution at least. Furthermore, the circuits have no feedback system as the operational amplifier (OP) does, which is hard to design in the current LTPS technology.

Keywords: Low Temperature Poly-Silicon TFT, source follower, output buffer, data driver

1. Introduction

Poly-silicon TFT (Thin Film Transistor) technology has been established for applications in active matrix liquid-crystal displays. In order to achieve finer gray scale for better image quality, data driver should be designed with lots of efforts. In the amorphous TFT technology, the scan driver and the data driver are fabricated on the silicon wafer, and then packaged and assembled with the glass panel with expensive and complicated process. Thus, the driver directly fabricated on the glass together with the pixel array is a trend in the future. This paper is focused on the design of the integrated data driver in the LTPS technology. The data driver we proposed in this paper contains a DAC and an analog buffer. The DAC in our circuit contains 2 capacitors and the switch circuit. It has no driving capabilities to drive the load of the data line. So we need a buffer to keep the converted analog voltage and provide enough driving capability. Conventionally the OP is configured as a unit gain buffer as the traditional analog buffer. However, in the LTPS technology, the TFT has much poor performance than the silicon MOS transistor. This makes the OP hard to design. We have proposed many other buffer circuits to take place of the OP in the data driver on the panel.

2. DEVICE CHARACTERISTICS

The i_d - v_d , i_d - v_g curve of our models is shown in figure 2.1(a) 2.1(b):

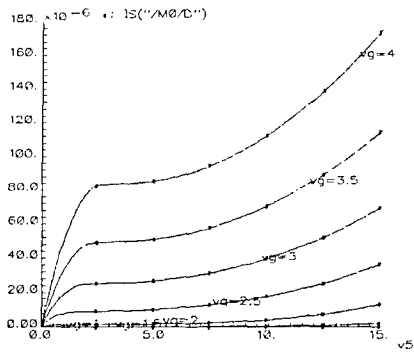


Figure 2.1(a) the i_d - v_d curve of the LTPS models.

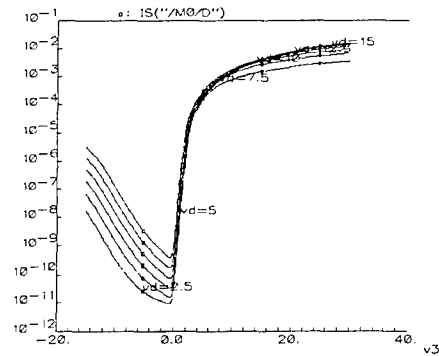


Figure 2.1(b) the i_d - v_g curve of the LTPS model.

From these curves, we can find many disadvantages for the LTPS TFT in the analog circuit. First, the mobility of the LTPS TFT is about 1/10 of the silicon MOS transistor. In order to get the enough current to drive the LCD panel, the size of the TFT must be at least 10 times of the silicon MOS transistor. Second, the threshold voltage of the LTPS TFT is larger than the silicon. This will make the output swing be limited. Third, there is leakage current when the MOS is in the cut-off region. Fourth, in the saturation region, the current of the TFT has greater variation than the MOS on the silicon. And finally, the kink effect makes smaller the saturation region of the TFT. All the above characteristics make the constant current source, which is very critical in analog circuits, has a very small swing.

New circuits are proposed in this paper to replace the operational amplifier as a unit gain buffer to save the area. In order to improve the output impedance of the biasing current sources in the proposed buffer circuits, cascoded structure of current source is necessary. Therefore, 15 volts of the power supply is applied to keep sufficient output range. In this way, the analog output buffer can be used in the driver on the panel. The details will be discussed in the following section.

3. DATA DRIVER STRUCTURE

The overall data driver structure is shown in figure 3.1:

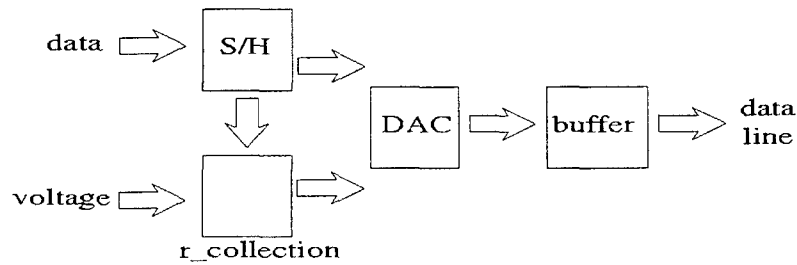


Figure 3.1 the data flow of the data driver in LTPS panel

Neglecting the circuit for sample and hold, the most important part of a data driver contains the gamma correction circuit, DAC, and the buffer. Our gamma correction circuit selects the reference voltages for the DAC according to the first 3 MSB of the digital input such that the converted analog output is a piecewise linear approximation to the transparency-to-voltage curve of the liquid crystal.

The DAC structure used in our data driver is shown in figure 3.2:

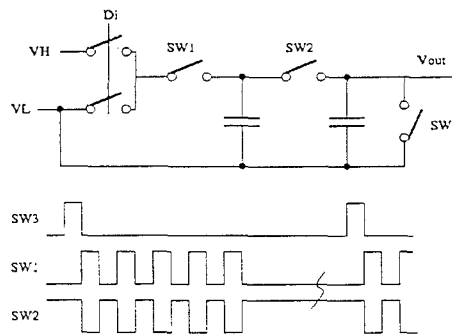


Figure 3.2 the DAC and the control signal in the data driver

The DAC contains 2 capacitors of the same size and several switches.

There are three steps before the output voltage is evaluated. In the first step SW3 is turned on to reset voltages on each node and capacitor. In the second step the non-overlap signals for SW1 and SW2 evaluate the output voltage on the node Vout according to the digital input Di, which is given serially with LSB first to choose VH or VL. The output voltage of the DAC, Vout, at the m-th time that SW2 is on is given by the following equation:

$$V_m = \frac{V_{m-1} + D_m(V_H - V_L)}{2}$$

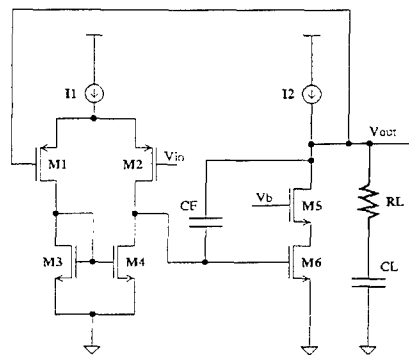
Since the reference voltage VH and VL are chosen by the first 3 MSB of the digital input, only 5 bits of the digital input has to be given serially as Di in the circuit. As SW2 is turned on at the 5th time, it enters the third step. All the switches are hold still to keep the output voltage such that the buffer to be introduced later can drive

the data line according to the converted analog voltage in this step.

We can find that the DAC structure is very simple. The advantage of this DAC is that it has small area and consumes very low power. The control circuit will cost a little area but it won't be a problem since all DACs in the data driver can share the same control circuit. The major issue of this DAC on the LTPS technology is that it needs an output buffer to drive the large capacitor on the data line. This is what we are going to discuss in this paper. Some solutions are proposed under below.

Approach I

Traditional output buffer uses the operational amplifier that is configured as a unit-gain buffer. Here we also designed a two stage operational amplifier as the output buffer with the LTPS technology. The circuit and some device parameters are shown in figure 3.3:



component	M1	M2	M3	M4	M5	M6	CF	CL	RL
size	80/8	80/8	30/8	30/8	150/8	150/8	15p	10p	2k

Figure 3.3 the operational amplifier schematic and the size

Because the gain-bandwidth product is too small, we added M5 cascoded on M6. This makes the operational amplifier have higher gain and can have enough speed with reasonable size. The operational amplifier we designed has 66.2db DC gain and 400k unit gain frequency. It have 10-bits resolution and the slew rate reaches 0.9v/us. It can slew the voltage from 0v to 10v within 12usec. The drawback of this circuit is that the capacitor CF for compensation is too large to fit into the limited area of the driver integrated LTPS TFT LCD panel.

Approach II

The second approach is based on the source follower. Since the source follower output has a nearly constant voltage difference, slightly greater than the threshold voltage of the TFT, with the input, we tried to save the voltage difference in the capacitor and then add it back to the input such that the difference can be compensated. Suppose that only one stage of the source follower is used, the magnitude of the stored voltage difference is

about the range of the threshold voltage. While this voltage difference is added back to the gate of the TFT, the output voltage at the source of the TFT will shift by the same magnitude with some offset, which is again resulted from the channel length modulation and kink effect of the source follower itself. Therefore, we proposed new circuits using two stages of the source follower with different type of TFT. The stored voltage on the capacitor is the difference of the threshold voltage of the two TFT in this case. The offset of the new circuits will be greatly reduced because the gate and source of the TFT will have smaller shifting after the compensation. The circuits are shown in figure 3.4. The two switches labeled as SW1 are turned on in the first step such that the difference of the input and output are stored in the capacitor. Then in the second step these two switches are off and SW2 is turned on, so that the stored voltage difference is added back to the input and results in a compensated output.

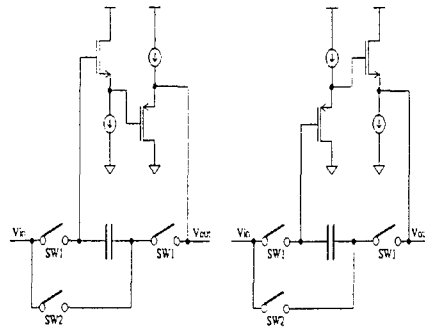


Figure 3.4 the circuit of the source follower with compensation capacitor

To be more specific, we use one p-type source follower and an n-type one to cancel the drop of the source followers in the first step. In this way, the voltage difference between the output and input will be $|V_{gsp}| - |V_{gsn}|$, which is much smaller than $|V_{gs}|$ in a single source follower. In this step, the voltage is also stored in the capacitor. In the second step it will be added back to the input and reflected to the output. This can compensate the offset left by the first step. The above source follower based unit gain buffer is of the class A buffer. The circuit we proposed had been simulated on smart-spice with the LTPS TFT models. The resolution of the DAC can achieve 6-bit. And the settling time (from 2v to 10v) can be within 10u. The DAC with this spec can be used in some low-end products.

The output current of the above class A buffer is the current of the constant current source minus the current provided by the TFT. This kind of the buffer has poor current efficiency. We further improved the circuit to be a class AB buffer structure which is shown in figure 3.5:

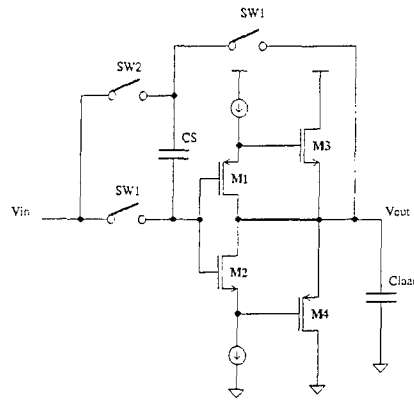


Figure 3.5 the improved circuit of the driver buffer

The basic function of the circuit is exactly the same as the class A ones. This kind of buffer has higher current efficiency. The dark line in the circuit is important since it makes M1 and M2 stay in the saturation region to keep V_{gs} constant. With this circuit, the DAC can reach 6-bit resolution with little current. The side effect of this circuit is that it has a little bit smaller range for operation.

The simulation result is shown in figure 3.6 (a) and 3.6 (b). The curve in figure 3.6 (a) is run in the UMC silicon models. The resolution can achieve 10-bit resolution in this model and the maximum speed can be up to 10Mhz. The curve in the figure 3.6 (b) is run in the LTPS models. The maximum error between the output and the input is 100mv in the output range 2v-10v. The result is worse than the UMC models, but it can achieve 6-bit resolution.

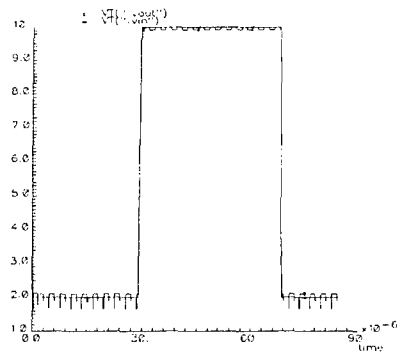


Figure 3.6 (a) the step response of the circuit in UMC model

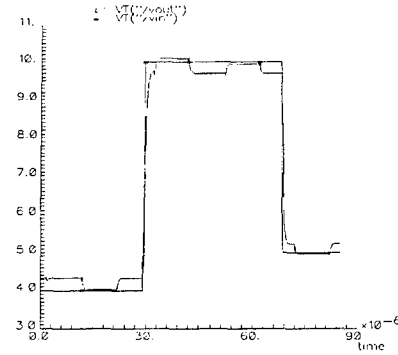


Figure 3.6 (b) the step response of the circuit in LTPS models

Approach III

The circuit we designed in approach I have an additional capacitor that take a lot of area and add more complexity in the circuit design. In approach II, the capacitor for compensation in the second step will be a load to our DAC, which is composed of capacitors. This makes the resolution as low as 6-bit only. Furthermore, the switches in the circuit also affect the accuracy of the analog circuit by clock feed-through and charge injection effects. The third approach we propose here is going to remove the switches and the capacitor in approach II. The circuit we design is shown in figure 3.7:

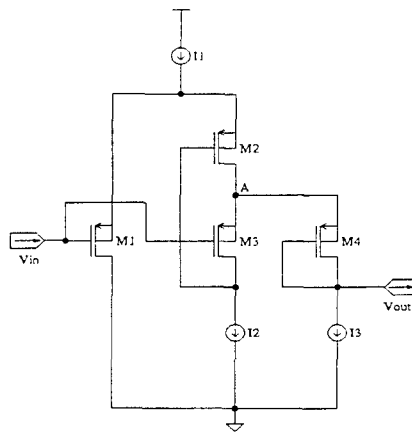


Figure 3.7 A new unit gain buffer

The basic idea of this circuit is also based on the source follower. A diode is used to compensate the voltage drop V_{gs} caused by the source follower. The basic component of these circuits is the two PMOS M3 and M4. M3 is the source follower that tracks the input voltage, and M4 is a diode with a constant voltage drop. The current flowing in M3 and M4 are fixed by current sources I2 and I3. The configuration of M1, M2, and M3 is widely used in high swing cascoded bias circuits. This configuration guarantees that these three transistors are all in the saturation region. M4 is a diode with constant current so that V_{gs} of M4 is kept constant. We make M3 and M4 of the same size and the two current mirrors I2 and I3 exactly the same. Then we can find that $V_{gs1} = V_{gs2}$ and $V_{out} = V_{in}$.

For the concern of loading to the previous stage, which might be a DAC without strong driving capability, we can use two such buffers to transfer the load effect. We design the first buffer with smaller size connected to the DAC to lower the load of DAC. And the second buffer is designed with larger size in order to push the large load of the LCD panel.

This circuit has been simulated with our LTPS model. The advantage of the circuit is that the area is smaller than operational amplifier. The circuit doesn't have any capacitor and switch. Its resolution can be up to 8-bit. They

can charge or discharge 10pF of capacitor connected with 3K of resistor, which is a simplified model of the loading on a data line of the TFT LCD panel, within 10us. The simulation result is shown in figure 3.8 (a) and figure 3.8 (b). Figure 3.8 (a) is the sweep response of the circuit with Vin from 0v to 15v. The curve is the value of Vout-Vin. The error between Vout and Vin in the curve is +/-25mv when the input is 1.5v~10v. Figure 3.8 (b) is the step response of the circuit. We can see that the circuit can charge the load from 1v to 10v within 10usec.

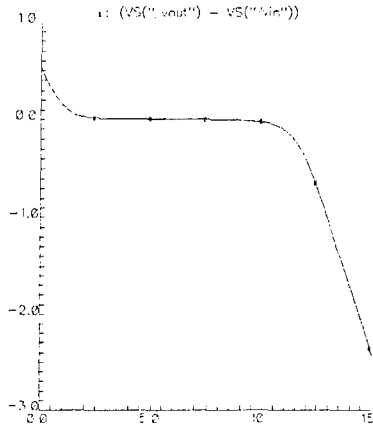


Figure 3.8 (a) the sweep response of the circuit,
Vin from 0v to 15v

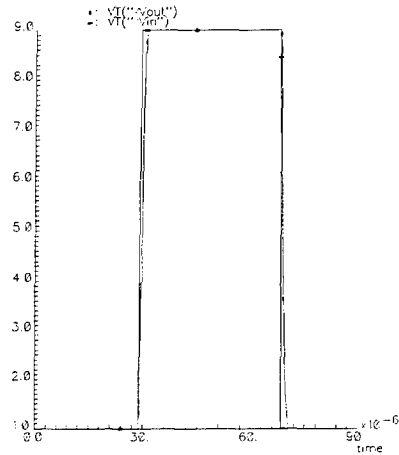


Figure 3.8 (b) the step response of the circuit

5. CONCLUSION

We have proposed various types of output buffer that could be implemented on the LTPS TFT LCD as part of the integrated data driver circuit. Since mobility of the LTPS technology is not as high as that of silicon, any circuit to be realized with the LTPS technology will take larger area than those to be implemented on silicon wafer. The output buffers we proposed have simple and realizable structure for the data driver such that they all have much smaller size than any conventional buffer configured with OP. On the other hand, these circuits also have higher speed than the OP. These circuits outperform the OP in many aspects except that they can only reach 6 to 8 bits of resolution. However, the resolution of these buffers can be improved easily as the processing technology is improved.

6. ACKNOWLEDGMENTS

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7.REFERENCES

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